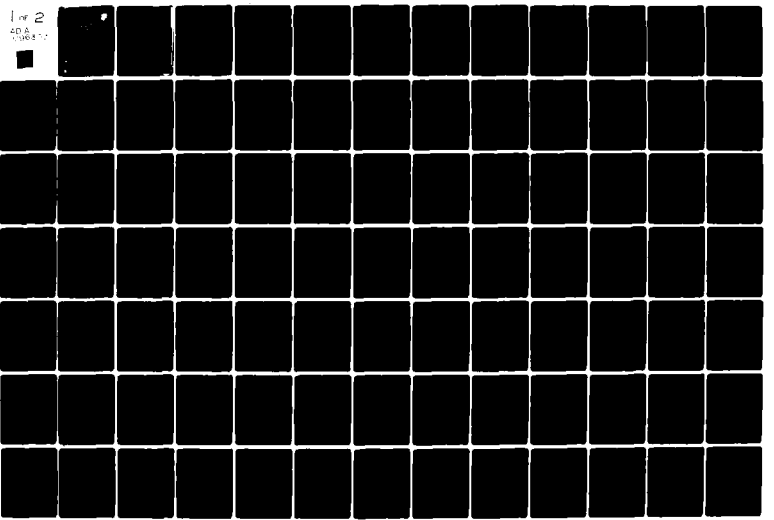
AD-A096 307 IBM FEDERAL SYSTEMS DIV MANASSAS VA F/G 9/2
ELECTRICAL CHARACTERIZATION OF COMPLEX MEMORIES - BYTE WIDE STA--ETC(U)
JAN 81 A H TABER, R A MOYERS F30602-79-C-0162
UNCLASSIFIED RADC-TR-80-401-PT-1 NL



RADC-TR-80-401, Part I (of two)
Final Technical Report
January 1981

ELECTRICAL CHARACTERIZATION OF COMPLEX MEMORIES BYTE Wide Static RAMs

IBM Corporation

A.H. Taber
R.A. Moyers

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-80-407, Part 1 (of two) has been reviewed and is approved for publication.

APPROVED: Allen P. Converse

ALLEN P. CONVERSE
Project Engineer

APPROVED: David C. Luke

DAVID C. LUKE, Colonel, USAF
Chief, Reliability & Compatibility Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (RBRA), Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return this copy. Retain or destroy.

19 TR-80-401-PT-1

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: RADC-TR-80-401, Part 1 (of two)	2. GOVT ACCESSION NO.: AD-A096304
	3. RECIPIENT'S CATALOG NUMBER:
4. TITLE (and Subtitle): ELECTRICAL CHARACTERIZATION OF COMPLEX MEMORIES - BYTE WIDE STATIC RAMS. Part 1.	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report, June 1979 - September 1980
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): A.H. Taber, R.A. Moyers	8. CONTRACT OR GRANT NUMBER(s): F30602-79-C-0162
9. PERFORMING ORGANIZATION NAME AND ADDRESS: IBM Corporation, Federal Systems Division, Manassas VA 22110	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F, 23380185
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (RBRA), Griffiss AFB NY 13441	12. REPORT DATE: January 1981
	13. NUMBER OF PAGES: 107
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Allen P. Converse (RBRA)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Memory	Semiconductor
Static RAM	Testing
Characterization	Electrical Performance
Random Access Memory	Monolithic

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes work performed from June 1979 to September 1980 on electrical characterization of 1KX8 and 2KX8 static RAMs. The objectives of the project were to find 1KX8 and 2KX8 devices that were both attractive to the user and deliverable by industry; electrically characterize these devices; and generate a draft 38510 specification for each using characterization data as a basis for establishing performance limits.

(Cont'd on reverse)

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED 409604

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

limits.

These goals were met and it was concluded that at least one company in the merchant semiconductor industry can produce 1KX8/2KX8 static RAMs that will operate over the temperature range of from -55°C case (instant on) to +125°C case (operating) with cycle times of 90/200 NS minimum, and power supply tolerances of ±10 percent.

One of the problems encountered in establishing future performance limits was the relative newness of high speed (less than 100NS) 1KX8 RAMs and the lack of any American 2KX8 static RAMs other than engineering prototypes. As a solution, performance limits for the existing parts were proposed, and limits for several faster speed grades predicted by scaling. Further work might include testing of the enhanced speed versions of the 1KX8 and 2KX8 to justify these proposed limits.

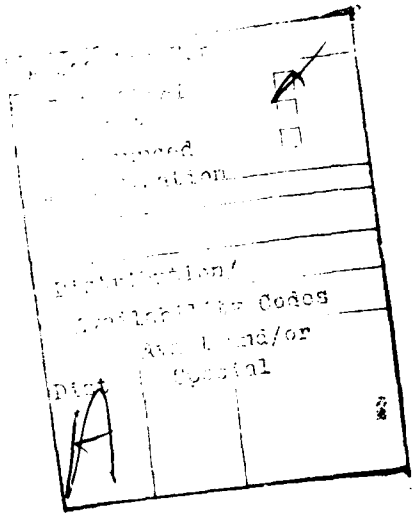


TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

EVALUATION

The objectives of this program were two fold: (1) to evaluate the performance of byte-wide static RAMs for use in military systems and (2) to evaluate a bit threshold measurement technique for Ultra-Violet Erasable PROMs (UV-EPROMs). Both of these objectives were met, and this report describes the techniques employed and presents some of the data generated in achieving the program results. Because of the diversity of the two tasks, the final report is divided into two parts: (I) "Byte-Wide Static RAMs" and (II) "Assessment of a Circuit Implementation to Measure EPROM Data Storage Margins".

Part I describes the evolution of MOS static RAMs with by-eight organizations. Specifically, 1Kx8 and 2Kx8 devices were evaluated to assess their performance in a military environment. Limits for performance were established for existing devices, and they were predicted for future devices. These limits were documented in Mil-M-38510 detail specifications (slash sheets) which resulted from the program.

Part II describes a threshold measurement technique for Ultra-Violet Erasable PROMs which was implemented in a vendor's 16K device. The technique was evaluated in terms of its potential usefulness as a system level verification test to determine projected data retention times.

The specifications which resulted from Part I will allow the procurement of reliable military grade products, and the preliminary work performed in Part II will allow the prediction of expected data retention times for UV-EPROMs. Both of these efforts have been performed in support of Mil-M-38510, "General Specification for Microcircuits", and they should enhance the reliability of military systems.

ALLEN P. CONVERSE
Project Engineer

1.0 INTRODUCTION

The work presented here is the static RAM portion of an RADC contract entitled "Electrical Characterization of Complex Memories."

The 8K byte-wide NMOS static RAM is a part which has been available for several years in a standard package and pinout. Until recently, however, the type of performance offered to the user has ranged from medium (∿150NS) to slow speed (>250NS). Now, with a new scaled process, one domestic vendor has successfully produced high speed 8K RAMs and is evaluating 16K designs.

The inherently wide temperature performance of these NMOS static RAMs has made it possible for the government to be offered this same high speed performance advantage in many control store/main store applications. With this in mind, IBM Federal Systems Division (FSD) has performed electrical characterization on these 1KX8 and 2KX8 static RAMs. As a separate data item, drafts of the MIL-M-38510/XXX military specifications for 1KX8 and 2KX8 static RAMs were prepared and submitted to RADC as part of this project.

This final report is comprised of a large quantity of reduced data which justifies the limits set forth in the proposed draft specifications for the dash 01 8K and 16K devices. Limits for the faster dash numbers were scaled. It is hoped that it will serve as a comparison reference manual for future product designs and revisions.

2.0 OBJECTIVES OF THE PROJECT

The objectives of the project were as follows:

1. Characterize 1KX8 and 2KX8 static RAMs for the purpose of establishing draft specification limits.

2. Attempt to demonstrate that alternate devices made by different vendors are interchangeable on a pin and performance basis.

3. Generate draft 38510 slash sheet specifications and proper test procedures for the 1KX8 and 2KX8 static RAMs using characterization data as a basis for establishing performance limits.

3.0 CONCLUSIONS

All objectives of the project were met. It has been concluded that at least one company in the merchant semiconductor industry can produce 1KX8/2KX8 static RAMs that will operate over the temperature range of $-55^{o}C$ case (instant on) to $+125^{o}C$ case (operating) with cycle times of 90/200 NS minimum, and power supply tolerances of $\pm$10 percent. The data presented in Appendices I (1KX8 RAM), and II (2KX8 RAM) are the basis for the conclusion. The recommended limits for all parameters for the 1KX8 and 2KX8 static RAMs are given in Appendix III (Recommended Parameter limits). It is felt that these recommended limits, with minor exceptions, will satisfy the majority of users and future suppliers as these devices become adopted throughout the industry.

With respect to "device interchangeability" it was found that, although several American and Japanese vendors are making functionally similar 1KX8 and 2KX8 RAMs, no other proposed American devices are fast enough to meet the recommended performance limits established for the subject RAMs at this time. In addition, it is felt by IBM that the 1KX8 will never become an industry standard. This is due to its late introduction with respect to the 2KX8, which is already being made in Japan.

4.0 OPERATION OF THE 1KX8/2KX8 RAMs

Due to the relatively short exposure of the Mostek RAMs in the industry so far, it may be appropriate here to discuss their operation.

Figure 1 shows the pinout of the 2KX8 RAM in a 24 pin DIP. The 1KX8 RAM pinout is identical to the 2KX8 except that pin 19 is a no-connect. Timing diagrams for read and write cycles are shown in figures 2 and 3. For the 1KX8/2KX8 RAMs, addressing 1 of 1,024/2,048 bytes requires handling a 10/11-bit address word. This is accomplished by supplying a 10/11-bit address field to the 10/11 address inputs $(A_0 - A_9)/(A_0 - A_{10})$.

The RAMs are in a read mode whenever the $\overline{WE}$ (write enable) input is at a logic "1" (high) level. A transition on any of the address inputs will disable the 8 data output drivers after time t_{AZ} (address data off time). Valid data will then be available to the 8 data output drivers within time t_{AA} (address access time) after the last address input is stable, provided that the $\overline{OE}$ (output enable) and $\overline{CE}$ (chip enable) access times are satisfied. This is shown in read cycle 1, figure 2. If $\overline{OE}$ or $\overline{CE}$ access times are not met, data access will occur relative to the limiting parameter, t_{OEA} or t_{CEA} (output enable access time or chip enable access time), rather than the address. Output enable access is shown in read cycle 2, figure 2. Chip enable access is shown in read cycle 3, figure 2. The state of the 8 data I/O (input/output) signals is controlled by the $\overline{CE}$ and $\overline{OE}$ inputs. A logic "1" on $\overline{CE}$ and/or $\overline{OE}$ will cause the 8 data output drivers to go to a high impedance state after time t_{CEZ} or t_{OEZ} (chip enable data off time or output enable data off time).

The device is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ inputs are in the logic "0" (low) state. The write cycle can be initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. In this case the leading edge of the $\overline{WE}$ pulse will latch the status of the address bus. A write cycle can also occur when $\overline{WE}$ goes low before $\overline{CE}$. In this second case, the leading edge of $\overline{CE}$ will latch the address status. In either case, the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, address setup and hold times, and write pulse width are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then the leading edge of $\overline{WE}$ will cause the outputs

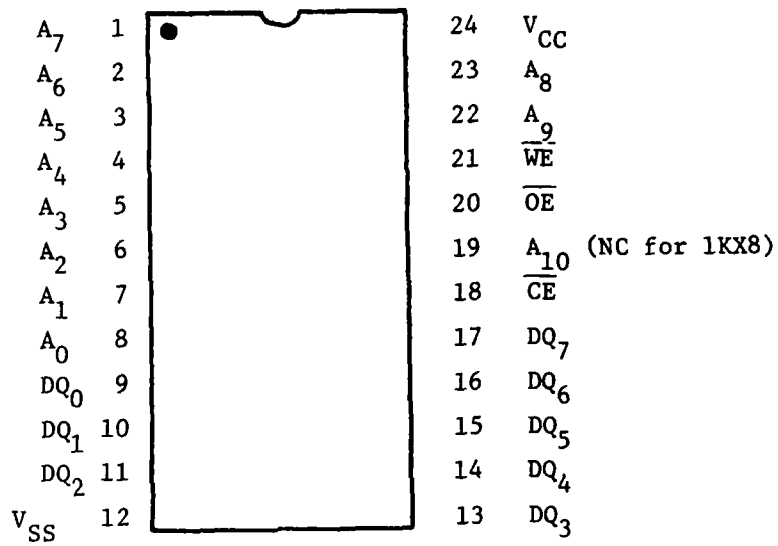


Figure 1 Terminal connections for 1KX8/2KX8 static RAM

READ CYCLE TIMING

1KX8/2KX8 STATIC RAM

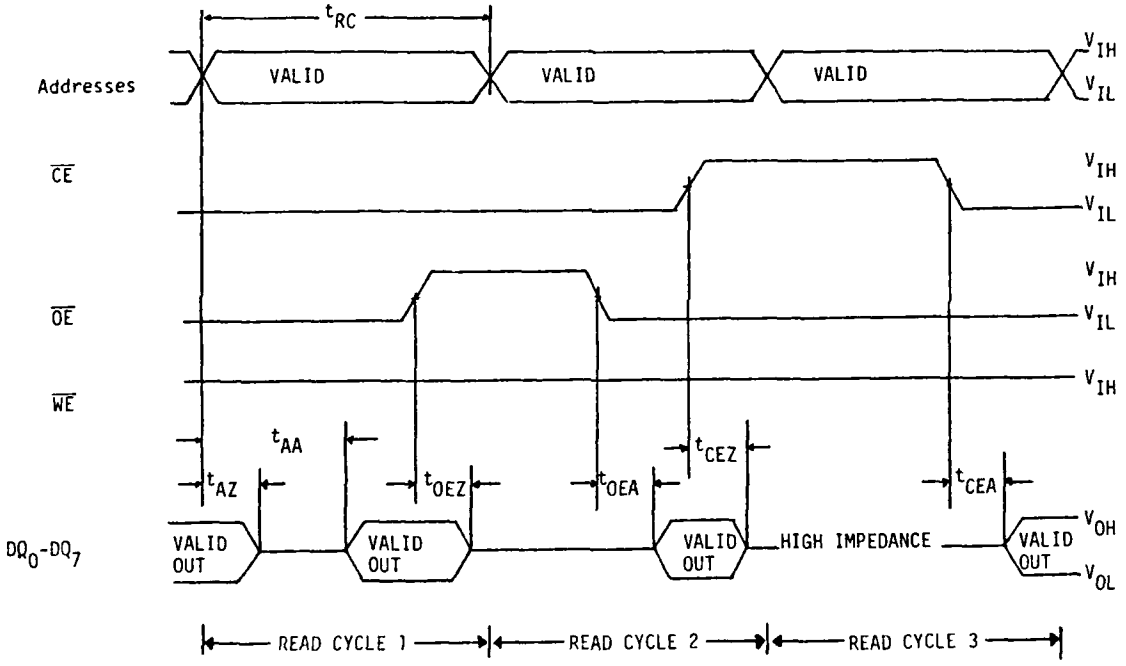


FIGURE 2. Read cycle waveforms

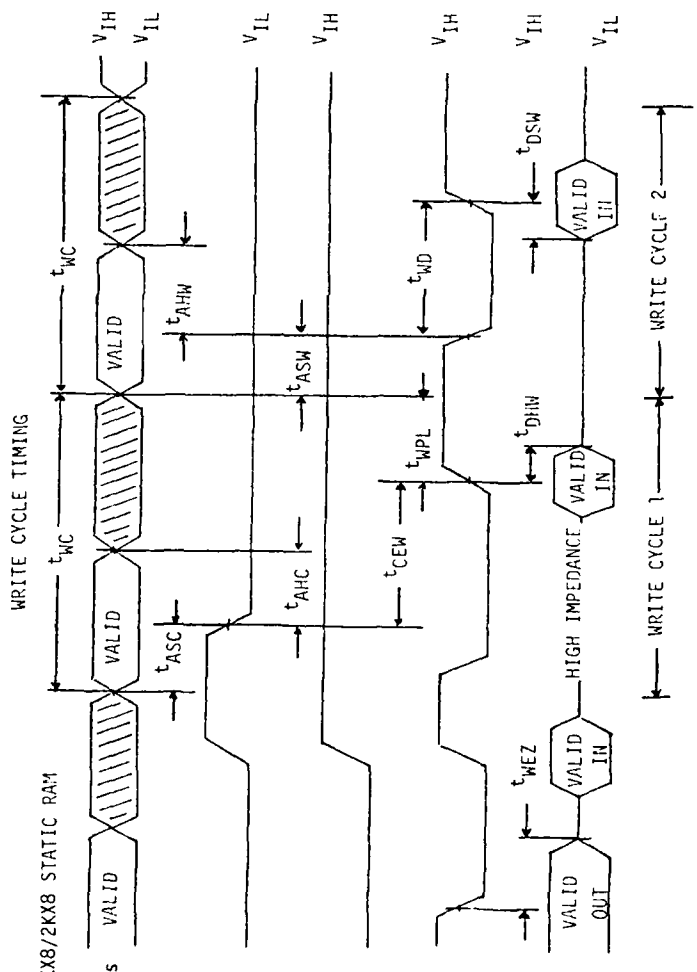


FIGURE 3 Write cycle waveforms

to go to a high impedance after time t_{WEZ} (write enable data off time). For write to occur, data in must be valid for time t_{DSW} (data to write setup time) prior to the low to high transition of $\overline{WE}$. The data input signals must remain stable for time t_{DHW} (data hold time after write) after $\overline{WE}$ goes high. The $\overline{WE}$ control will disable the data out buffers during the write cycle. However, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

5.0 PROFILE OF THE 1KX8/2KX8 STATIC RAMs

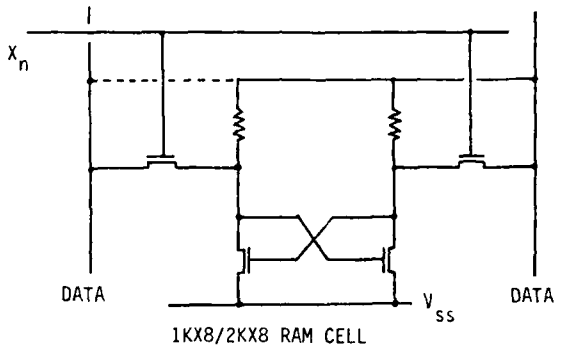
To give some perspective to the devices under investigation by this project, the following table illustrates some aspects of the process, design, performance, and packaging.

MOSTEK 1KX8/2KX8 STATIC RAM PROFILE

	1KX8 RAM	2KX8 RAM
Part No.	MK4801A Rev J	MK4802 Rev A
Die Size	490 mm^2	908 mm^2
Die Aspect Ratio	1.7:1	3.1:1
No. of Poly Levels	1	1
No. of Metal Levels	1	
Cell Size	840 mm^2	840 mm^2
Typ. Access (t_{AA})/cycle (t_{RC})	55/55 NS	110/110 NS
Supply Voltage	5.00 V	5.00 V
Package	24 pin DIP	24 pin DIP
Cell load resistor	10^9 Ω poly	10^9 Ω poly
Gate Oxide Thickness	500 Å	500 Å
Channel Length	2.5μm	2.5μm
Junction Depth	0.4μm	0.4μm

The 4801A Rev J and 4802 Rev A RAMs are both descendents of Mostek's 4118 1KX8 RAM, which was first produced using Mostek's "Poly R" process several

years ago. When Mostek developed its "Scaled Poly 5" process, the 4118 was scaled down in size by about 30% and, with some design changes, became the 4801A. The Mostek 1KX8/2KX8 RAM cells use polysilicon load resistors to maintain data on their cross-coupled flip flop structure, as shown in figure 4. In order to improve the cell layout, power is supplied to each cell by one of the metal data lines rather than a V_{CC} rail. Both data lines are normally high, but during the short time that one of them may go low, the state of the cell is maintained due to the long time constant of the load resistors and the cell flip flop node capacitance. Spider networks, of 8 resistors each, supply power to groups of 4 cells in the array.



1KX8/2KX8 RAM CELL
Figure 4

The RAMs contain circuitry to sense transitions on the address inputs. In the read mode a transition on any address will disable the output buffers and start a series of internal clocks that controls the operations required to retrieve data. When data access is complete, power consumption drops by about 15 percent. During the write mode, internal latches store the status of address at the latter occurring low going edge of $\overline{WE}$ or $\overline{CE}$, making the RAMs safer to use. On the 4118 device, there is a latch function available on pin 19 that latches the status of address and $\overline{CE}$ when brought low. This latch circuitry has been disabled on the 4118A, 4801A, and 4802. Instead, pin 19 is a no-connect on the 4118A and 4801A, and an address input on the 4802. The pinout of the 4801A and 4802 devices conforms to Jedec standard JC-42-78-4A for 24 pin 1KX8 and 2KX8 static RAMs.

The next version of the 4802, the Rev C, will be somewhat different from the Rev A. The modifications to the Rev A will include the addition of metal V_{CC} rails in the array and circuitry to perform a "Datasave" mode whereby data can be maintained in the array during loss of power to V_{CC} by supplying 4 volts at about 100 microamps to the $\overline{WE}$ pin. The reason for the dedicated V_{CC} rails in the array is to provide a means for maintaining data during the Datasave mode without keeping much of the support circuitry alive. The V_{CC} rail modification involves a change in the metal layer but doesn't affect the size of the cell or array. The Rev C, like the Rev A, will still be intentionally slowed down to ease debug. This is done by the use of 2 tapped delay lines--one affecting the read cycle and one affecting the write cycle. The speed of the internal timing and the delay lines is affected in the same way by such factors as temperature and process variation, so it should be easy to adjust the delay lines for higher speed once the rest of the design has been optimized.

6.0 CHARACTERIZATION

6.1 SAMPLES

In order to arrive at a set of specification limits that was both attractive to users and deliverable by industry, it was necessary to choose samples that represented the latest available product during the course of the project. Figure 5 is a chart depicting the samples that were characterized.

The 1KX8 devices were of two date codes; 8015 and 8033. Both were Mostek's commercial revision J, although the earlier date code part had the latch feature on pin 19 that is not offered on the later devices. These parts represented some of the faster of Mostek's commercial production parts, whose speed distribution was centered around 90 NS at 70°C at that time.

The 2KX8 devices were of 3 date codes; 8022, 8031, and 8033. They represented some of the faster samples of Mostek's Rev A part, which was an engineering version of the 2KX8 that was intentionally slowed down to ease

debugging of its functionality and which did not contain some of the design improvements that Mostek plans to use on their production version. The Rev A part at that time had a speed distribution centered around 200 NS at 70°C.

1KX8				2KX8			
PART NO.	DATE CODE	QTY	SPEED	PART NO.	DATE CODE	QTY	SPEED
MK4801P-70[1]	8015	1	70NS	MK4802P	8022	2	--
MK4801AP-70	8033	15	70NS	MK4802P-1	8033	4	120NS
				MK4802P-3	8031	16	200NS

1 Includes Latch Feature (Pin #19) - Not offered on production device

2 Commercial (0-70°C) Address Access Max Specification

8K/16K Samples Characterized

Figure 5

6.2 TEMPERATURE FIXTURING

The temperature forcing system used for the entire range of -55°C to 125°C was a Thermonics model T-2050 thermo gas system (liquid nitrogen).

Temperature measurements were made with a Digitec Thermocouple Thermometer (Model 590TC). A copper constantan thermocouple was held against the center of the underside of the device package while in the test socket by a small piece of foam rubber.

During characterization, temperature-controlled forced air was blown across the device package and the upper portion of the socket at 5 cuf/min. The thermocouple then read the average temperature of the underside of the package and the foam rubber holding it in place. Because of the immersion

of the socket in the airflow, it was assummed that there was a negligible temperature differential between the socket and package and that the thermocouple readings were a true indication of the case temperature.

6.3 MEMORY TEST SYSTEM

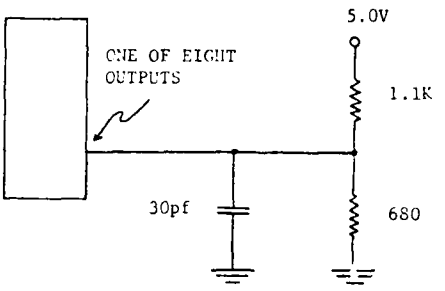
The memory test system used for all testing was a Fairchild/Xincom model 5582 with a model 7710 host computer. The Xincom 5582 provides a flexible timing system with cycle times down to 40 NS at 156 picosecond edge resolution while a programmable test pattern computer generates the complex algorithms needed for worst case data pattern evaluation. The 5582's X-Y address scrambling capability was used, along with vendor bit maps, for true topological addressing. For DC characterization, the 5582 contains a programmable DC parametric unit which has the ability to force and measure both voltage and current on any pin.

6.4 TEST ALGORITHMS

The test algorithms are given in Appendix V. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory. Each algorithm serves a specific purpose. All are commonly known patterns and should be quite simple for most test systems to implement. Because of the layout of the memory array, it is not possible to topologically descramble more than 2 of the 8 outputs at one time, so 4 passes with 4 sets of topo are necessary to completely check for pattern sensitivity.

6.5 TEST LOADS

All measurements, except pin leakage and standby supply current, were done with the 8 outputs loaded as in figure 6. The 30 picofarad capacitor provided some AC load for the access time measurements while still being



OUTPUT TEST LOAD
Figure 6

small enough to allow disable time measurements. The two resistors provided a reasonable load when measuring V_{OL} and V_{OH}, and also pulled the outputs quickly toward a midpoint value for the disable time measurements.

7.0 PRESENTATION AND EXPLANATION OF THE DATA

All electrical measurements were taken at -55°C, +25°C, and +125°C case temperature. After reduction, they were plotted to a smooth curve format so that parameter values could be lifted for other intermediate values.

The AC and DC data were plotted so that all information concerning each parameter is presented on a single page. The first plot at the top of the page shows the cumulative distribution of the sample group for that parameter. The second plot shows how the parameter varies with power supply voltage (V_{CC}), while the third plot illustrates how the parameter performs over the full temperature range.

There were 28 AC measurements taken over the range of 4.5 volts to 5.5 volts at all three temperatures. All parts were tested at 4.5 volts. Then, devices representing the slow, fast, and typical portions of the group's speed distribution were chosen to be tested at 4.75, 5.00, 5.25, and 5.50 volts. These numbered about one half of the total samples. The AC measurements consisted of read access and cycle times, write conditions

and cycle times, and output disable times. The disable times were measured as the time it took the output to change from a good high or a good low to a point that was closer to the high impedance state by 100 millivolts. Minimum disable times were measured to the first change in the outputs. Maximum disable times were measured to the last change in the outputs before reaching a quiet state.

The 5 DC measurements were performed at the same voltages as the AC measurements. Read and write mode supply currents from V_{CC} were measured at 180 NS cycle times only, but the currents at other frequencies can be estimated assuming that current increases linearly with frequency and using the standby mode current to represent zero frequency. V_{OL} and V_{OH} were measured using the card loads of figure 6, so the output current can be calculated using these resistor values. For a V_{OUT} of 2.4V, I_{OUT} is about -1MA and for 0.4V, it is about 4mA.

8.0 RECOMMENDATIONS FOR FURTHER INVESTIGATION

Further work with the 1KX8/2KX8 RAMs might include the following:

1. Evaluation of the enhanced speed versions of the 8K/16K to justify the dash 02-03 (8K) and dash 02-05 (16K) limits.

2. Investigation of the data retention modes that will be available on some of the 2KX8 RAMs. This mode could satisfy some short term non-volatile military applications via battery backup.

3. A study of the effects of alpha particles on 1KX8/2KX8 RAMs. Many RAM designs use high resistance poly loads in the array to reduce power consumption. This may increase their susceptibility to soft errors.

4. Testing of the 1KX8/2KX8 RAMs in high density packages such as flat packs or leadless carriers as these become available.

APPENDIX I

1KX8 STATIC RAM

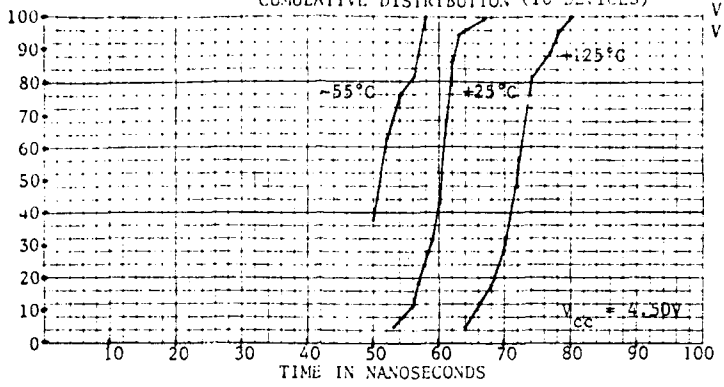
Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

1KX8 STATIC RAM
RANDOM READ CYCLE TIME

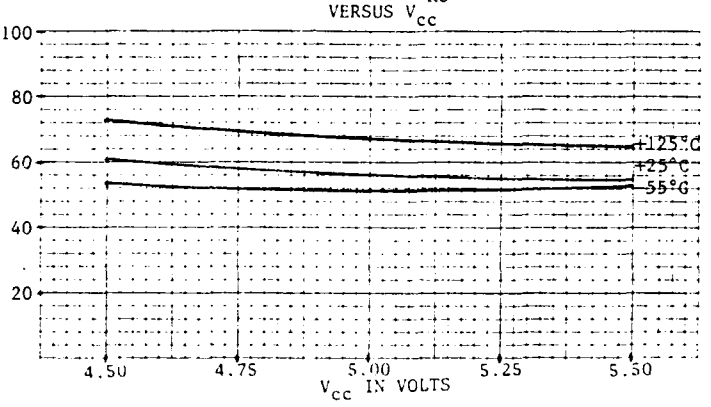
By AT/RM Date: 10/80
LOAD: fig. 6
ADDR PAT: RCGAL
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

T_{RC}

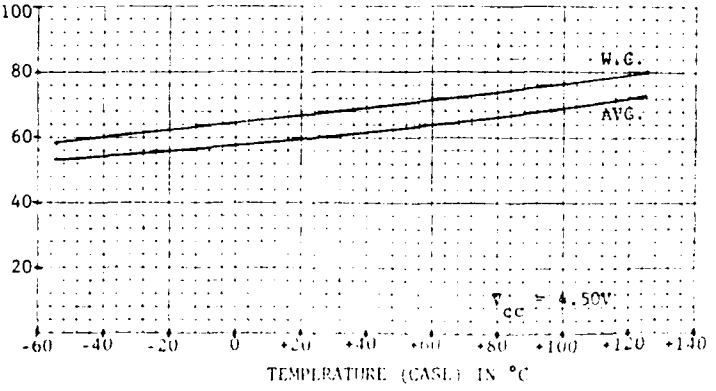
CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{RC}
VERSUS V_{cc}



VERSUS TEMPERATURE



1KX8 STATIC RAM

RANDOM WRITE CYCLE TIME

t_{WC}

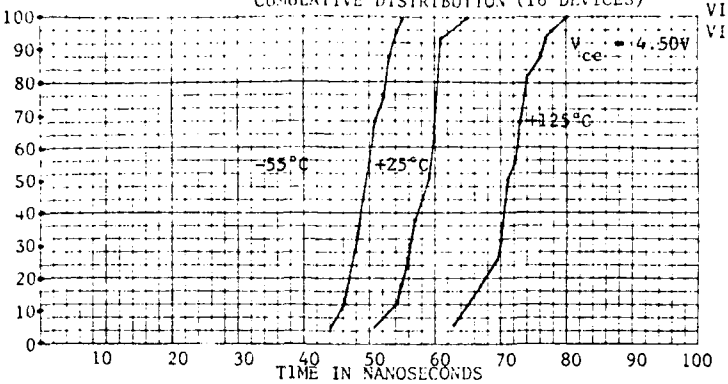
RANDOM WRITE CYCLE TIME MEASUREMENTS OF THE 1KX8 RAM WERE INCONCLUSIVE. THEREFORE, NO DATA IS PRESENTED HERE

Vendor: Mostek ±
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

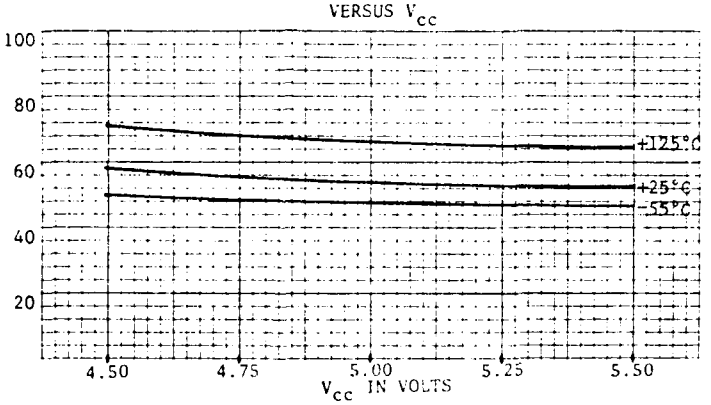
1 KX8 STATIC RAM
ADDRESS ACCESS TIME

By AT/RM Date 10/80
LOAD: fig 6
ADDR PAT: RCGAL
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

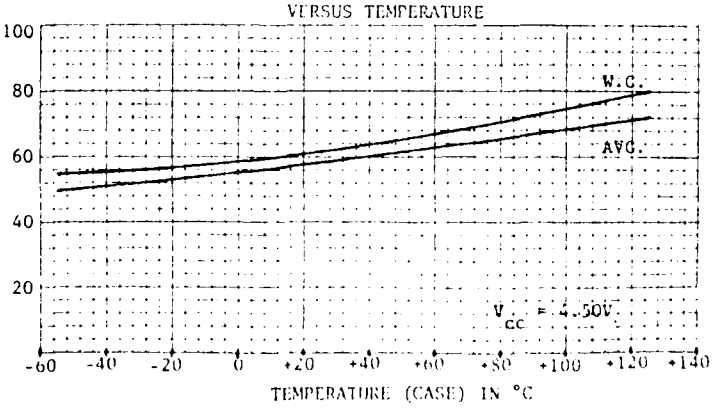
T_{AA}
CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{AA}
VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

P/N: MK4801P-70, MK4801AP-70

REV: J

Date Codes: 8015, 8033

#DEVICES: 16

1KX8 STATIC RAM

CHIP ENABLE ACCESS TIME

T_{CEA}

By AT/RM Date 10/80

LOAD: Fig. 6

ADDR PAT: ADCOMP

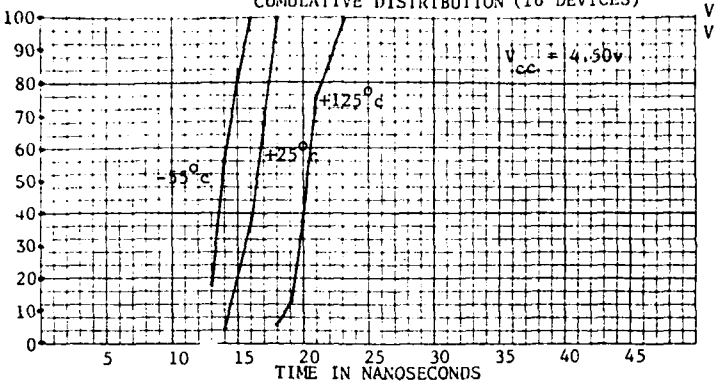
DATA PAT:

VIHC 3.0v

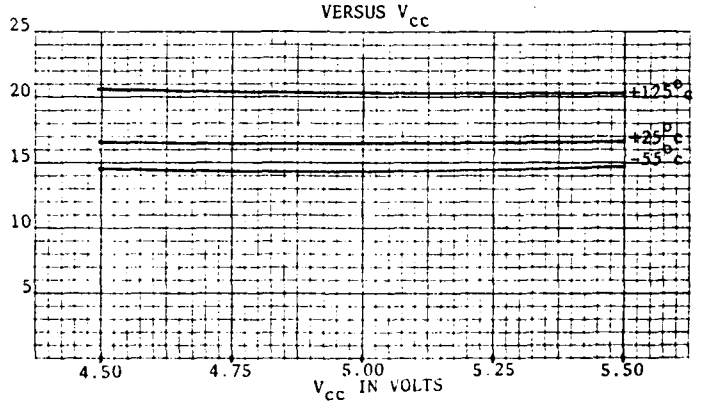
VIH 3.0v

VIL 0.0v

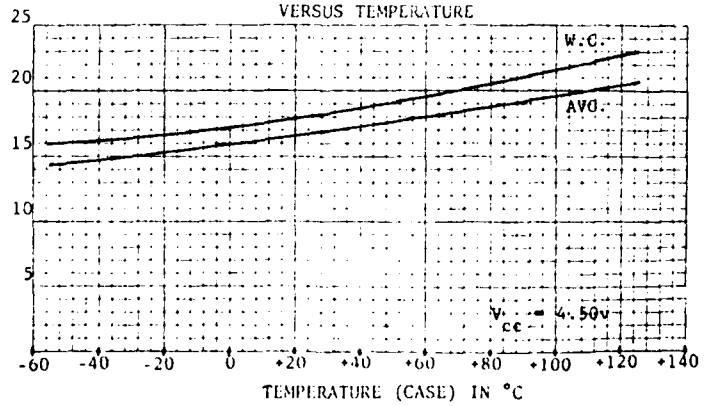
CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{CEA} VERSUS V_{cc}



VERSUS TEMPERATURE



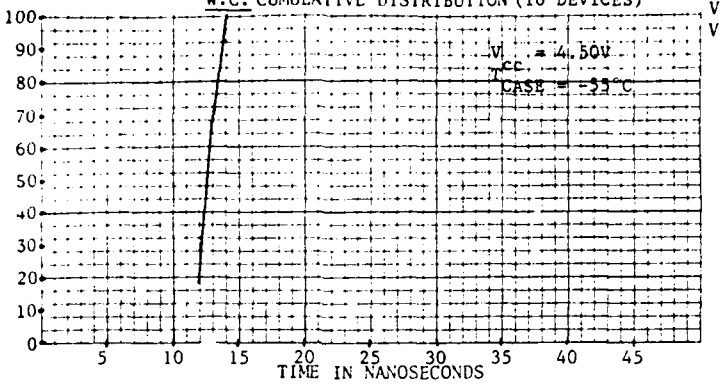
Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

1 KX8 STATIC RAM
MINIMUM CHIP ENABLE DATA OFF TIME
FOR A LOGIC 0

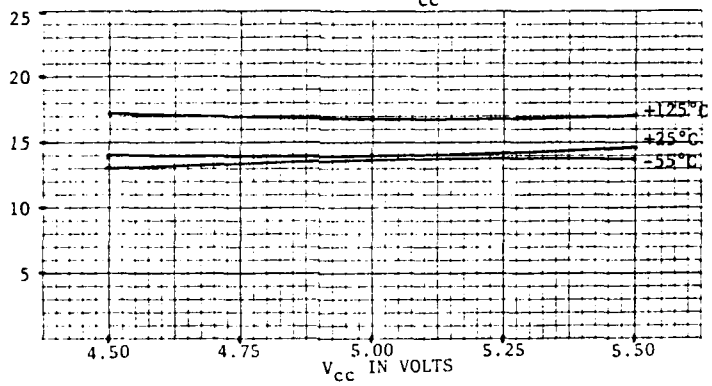
By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROS
VIHC 3.0V
VIH 3.0V
VIL 0.0V

T_{CEZO} MIN.

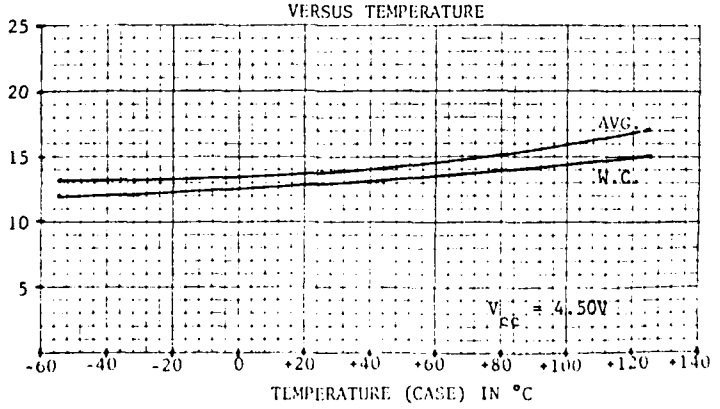
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{CEZO} MIN.
VERSUS V_{cc}



VERSUS TEMPERATURE

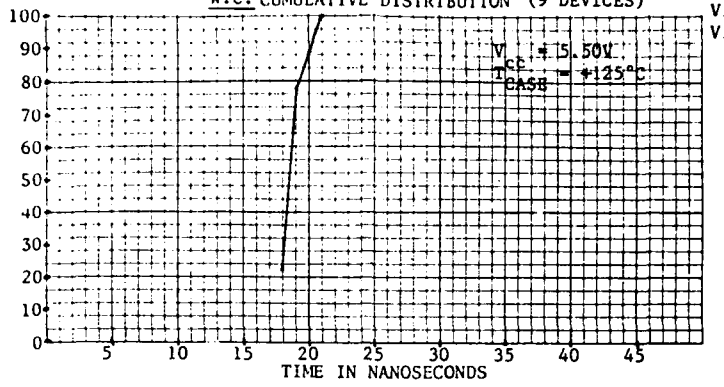


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

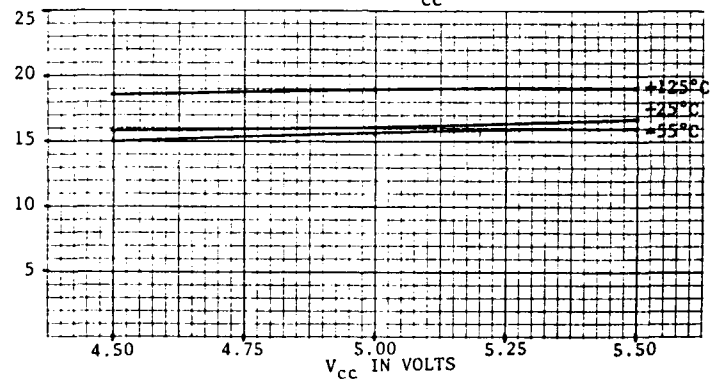
1KX8 STATIC RAM
MAXIMUM CHIP ENABLE DATA OFF TIME
FOR A LOGIC 0
T_{CEZO} MAX.

By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROS
VIHC 3.0V
VIH 3.0V
VIL 0.0V

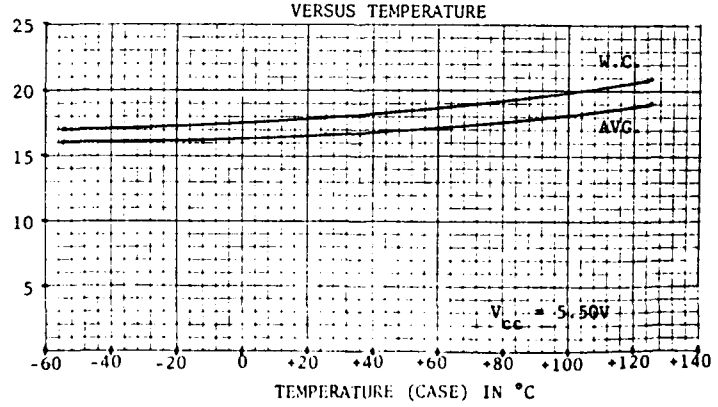
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE T_{CEZO} MAX.
VERSUS V_{cc}



VERSUS TEMPERATURE

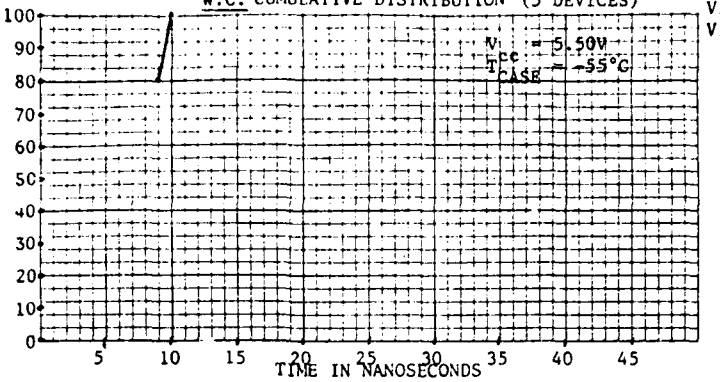


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

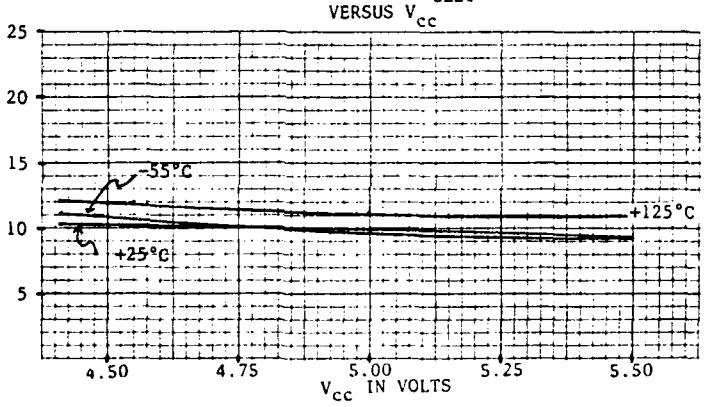
1KX8 STATIC RAM
MINIMUM CHIP ENABLE DATA OFF TIME FOR A LOGIC 1
T_{CEZ1} MIN.

By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

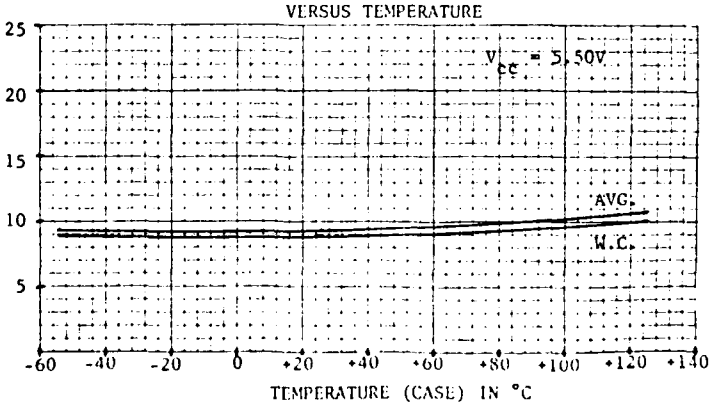
W.C. CUMULATIVE DISTRIBUTION (5 DEVICES)



AVERAGE T_{CEZ1} MIN. VERSUS V_{cc}



VERSUS TEMPERATURE

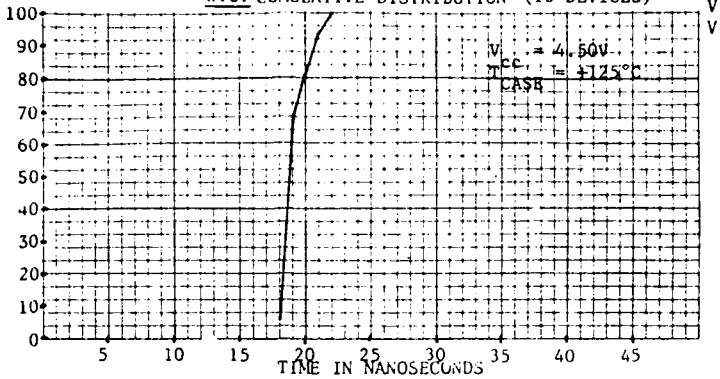


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

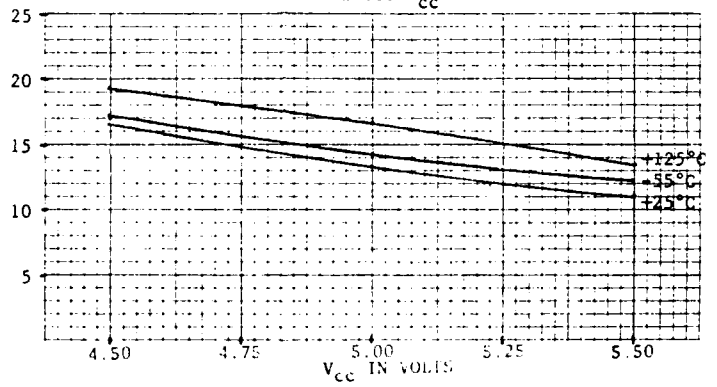
1KX8 STATIC RAM
MAXIMUM CHIP ENABLE DATA OFF TIME
FOR A LOGIC 1

By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

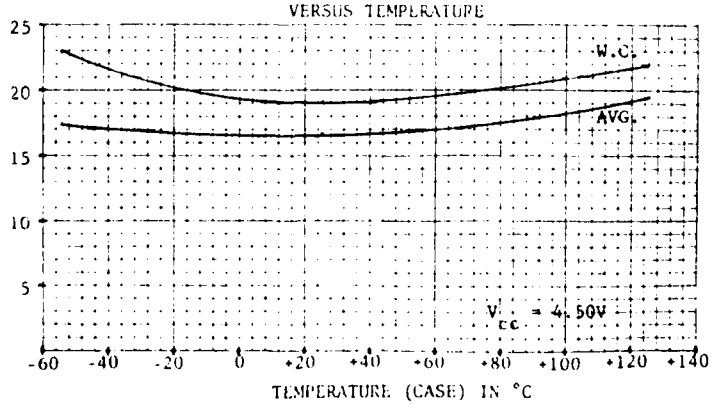
T_{CEZ1} MAX.
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{CEZ1} MAX.
VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek — 1KX8 STATIC RAM — By AT/RM Date 10/80

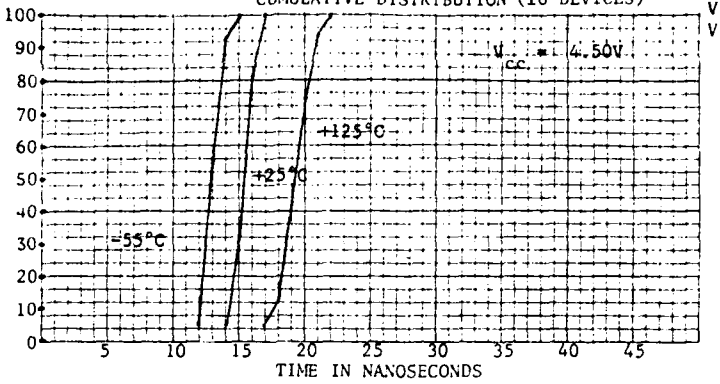
P/N: MK4801P-70, MK4801AP-70 OUTPUT ENABLE ACCESS TIME — LOAD: fig 6

REV: J — ADDR PAT: SLDIAG

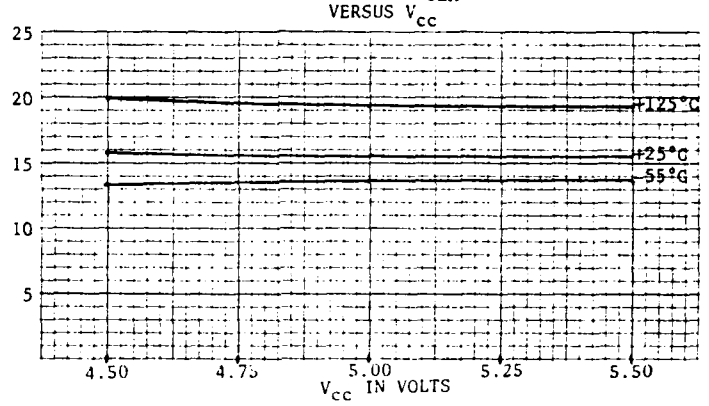
Date Codes: 8015, 8033 — T_{OEA} — DATA PAT:

#DEVICES: 16 — VIHC 3.0V — VIH 3.0V — VIL 0.0V

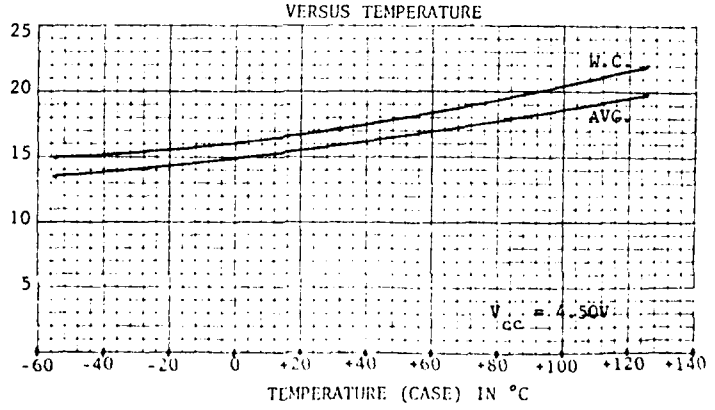
CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{OEA} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

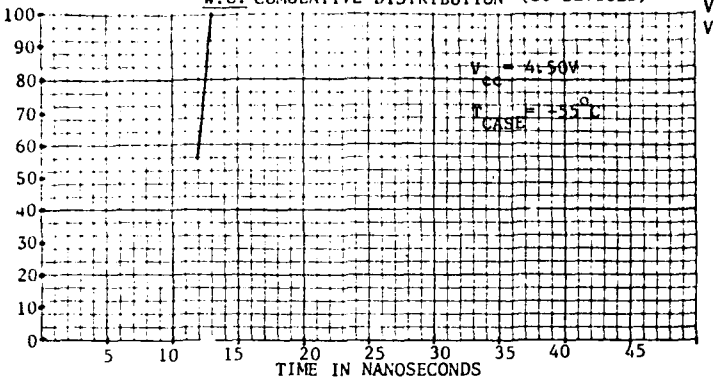
1KX8 STATIC RAM

MINIMUM OUTPUT ENABLE DATA OFF TIME FOR A LOGIC 0

t_{OEZO} MIN.

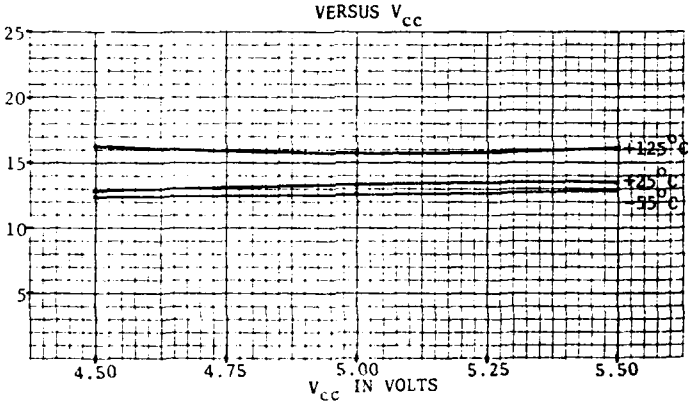
By AT/RM Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)

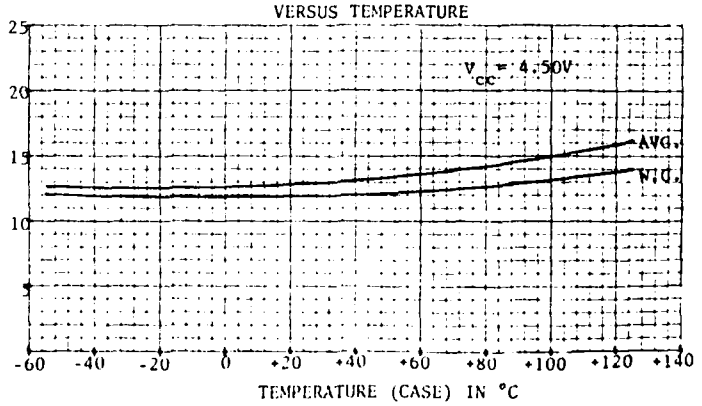


AVERAGE t_{OEZO} MIN.

VERSUS V_{cc}



VERSUS TEMPERATURE



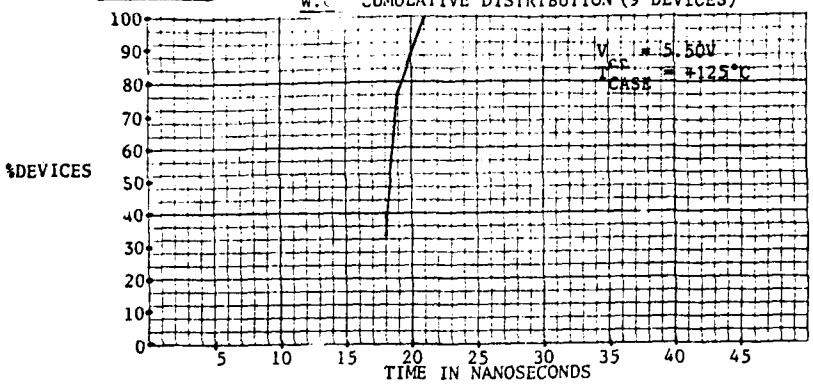
Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

1KX8 STATIC RAM
MAXIMUM OUTPUT ENABLE DATA OFF TIME
FOR A LOGIC 0

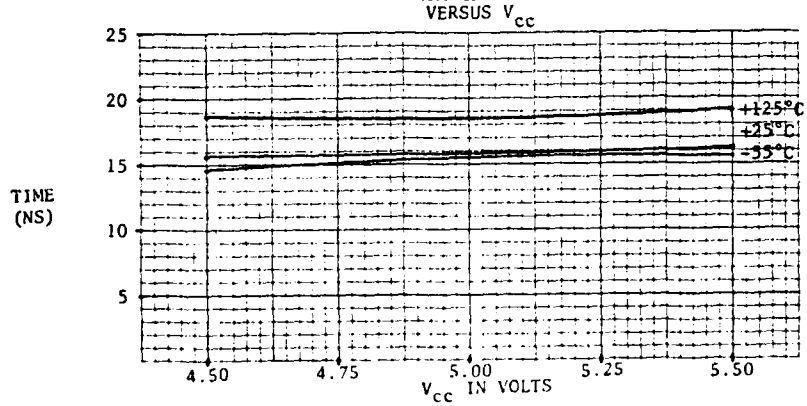
By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROS
VIHC 3.0V
VIH 3.0V
VIL 0.0V

T_{OEZO} MAX.

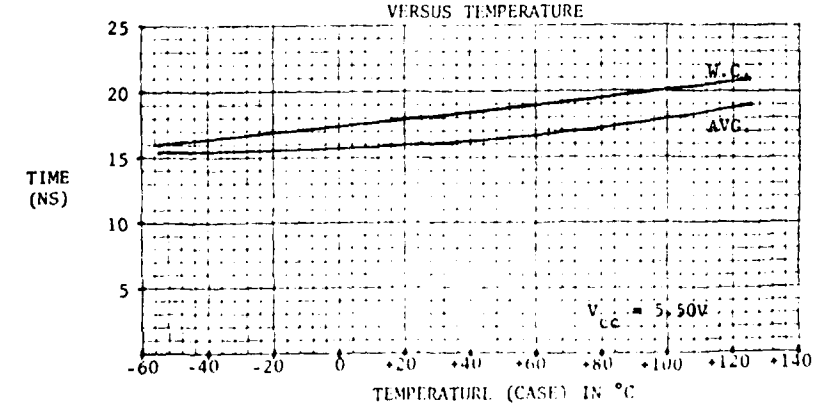
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE TOEZO MAX.
VERSUS V_{cc}



VERSUS TEMPERATURE

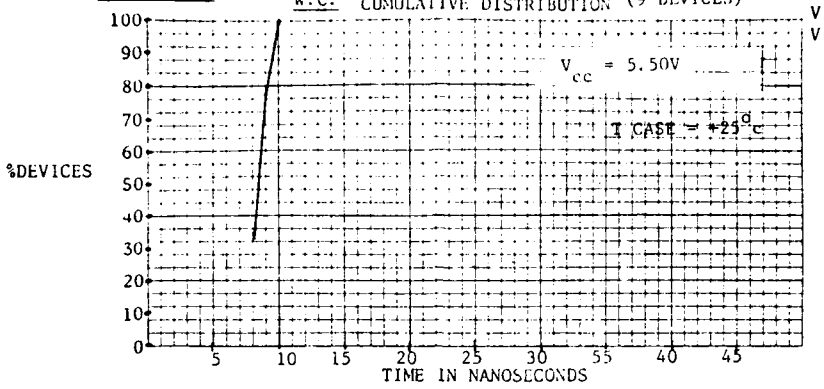


Vendor: Mostek
P/N: MK4801-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

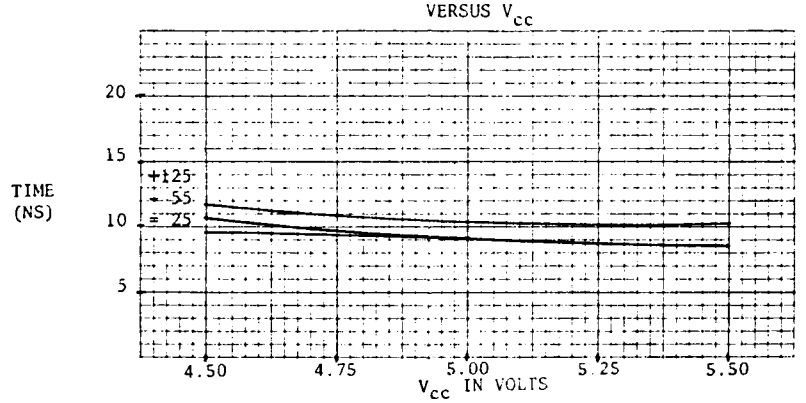
1 KX8 STATIC RAM
MINIMUM OUTPUT ENABLE to DATA OFF TIME FOR A LOGIC 1
T_{OEZ1} MIN.

By RM/AT Date 10/80
LOAD: Fig 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0v
VIH 3.0v
VIL 0.0v

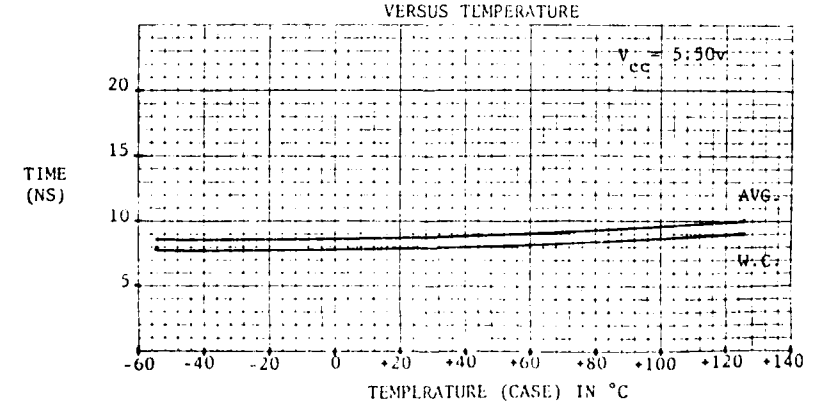
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE T_{OEZ1} MIN. VERSUS V_{cc}



VERSUS TEMPERATURE

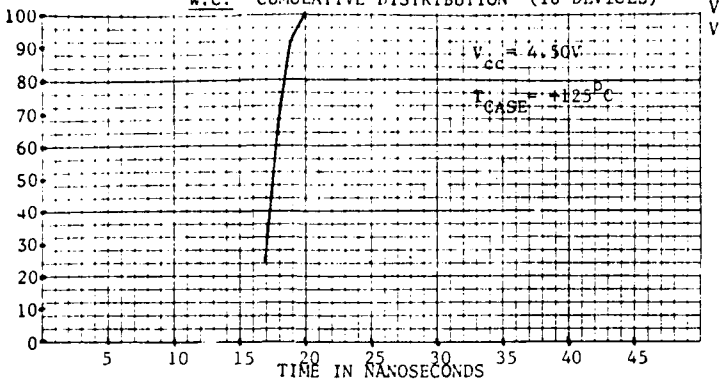


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

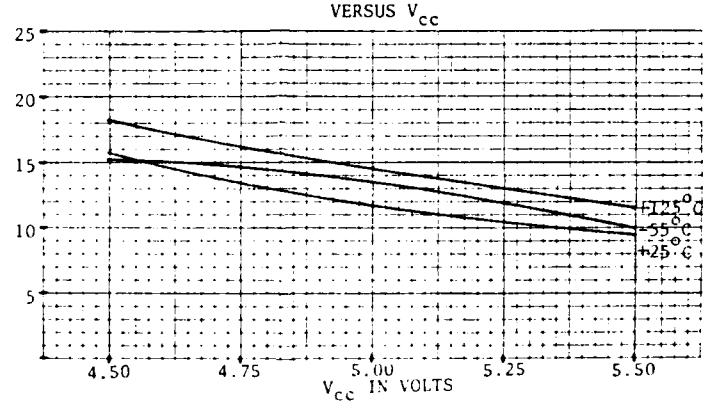
1KX8 STATIC RAM
MAXIMUM OUTPUT ENABLE DATA OFF
TIME FOR A LOGIC 1
t_{OEZ1} MAX.

By AT/RM Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

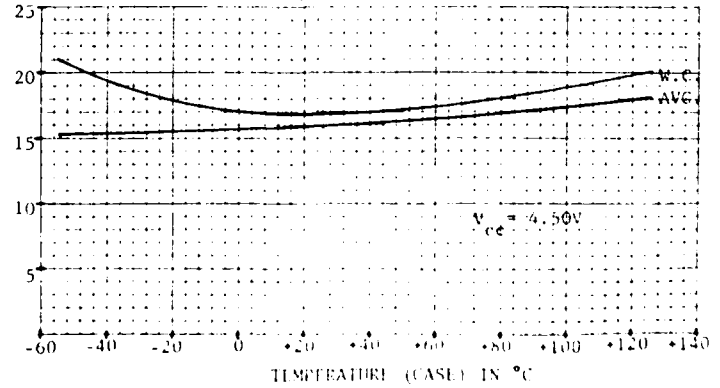
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE t_{OEZ1} MAX.
VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

P/N: MK4801P-70, MK4801AP-70

REV: I

Date Codes: 8015, 8033

#DEVICES: 16

1 KX8 STATIC RAM

MINIMUM ADDRESS DATA OFF TIME FOR A LOGIC 0

T_{AZO} MIN.

By AT/RM Date 10/80

LOAD: fig. 6

ADDR PAT: SEQ. RFAD

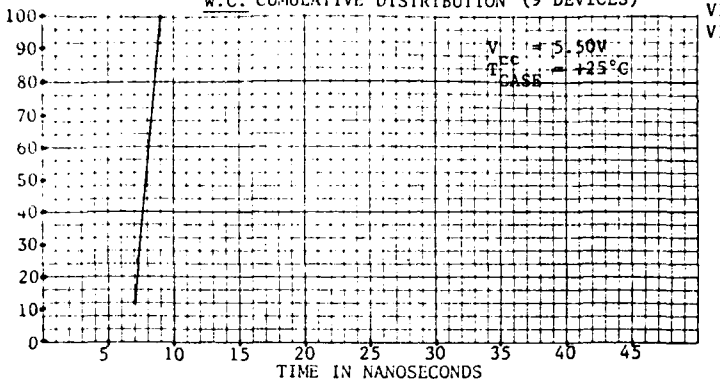
DATA PAT: ALL ZEROS

VIHC 3.0V

VIH 3.0V

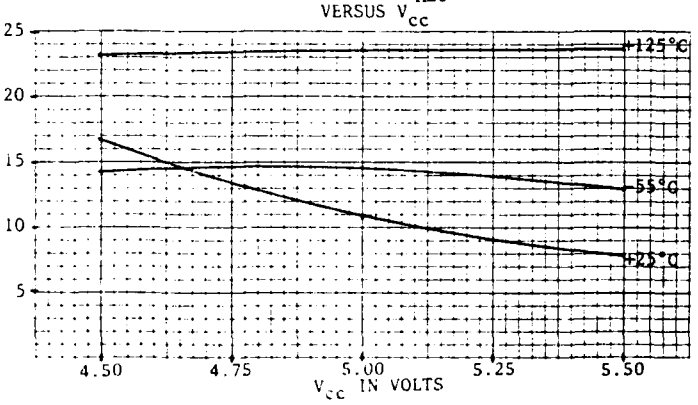
VIL 0.0V

W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)

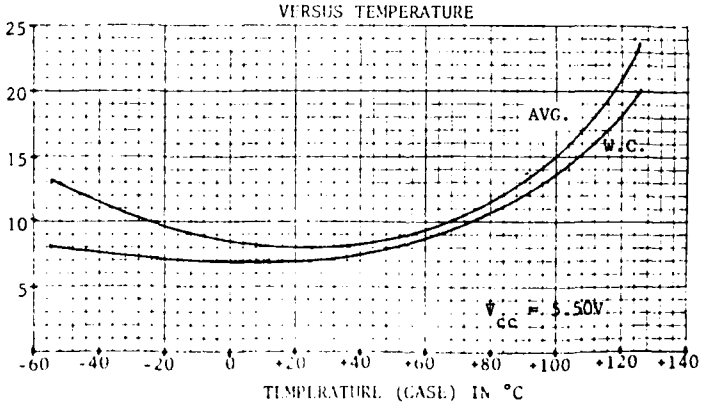


AVERAGE T_{AZO} MIN.

VERSUS V_{cc}



VERSUS TEMPERATURE



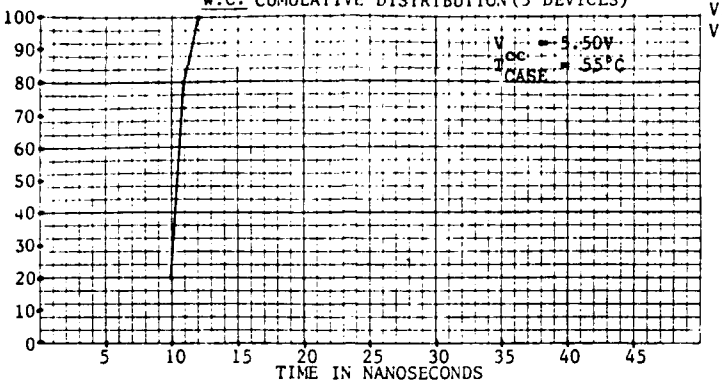
Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

1KX8 STATIC RAM
MINIMUM ADDRESS DATA OFF TIME
FOR A LOGIC 1

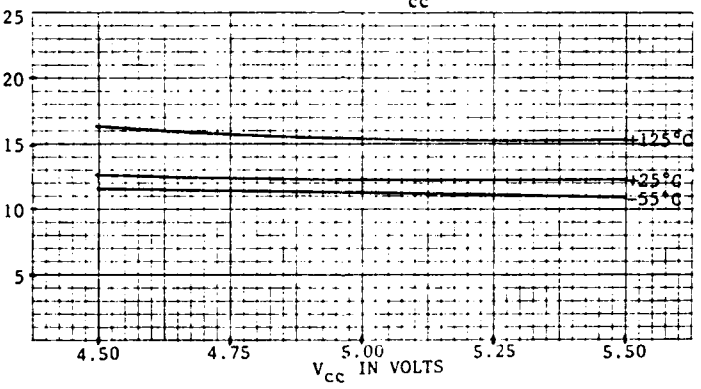
By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

T_{AZ1} MIN.

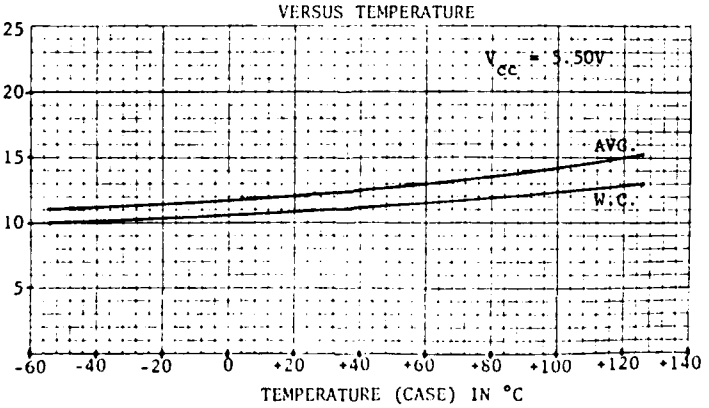
W.C. CUMULATIVE DISTRIBUTION (5 DEVICES)



AVERAGE T_{AZ1} MIN.
VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

P/N: MK4501P-20, MK4501AP-20

REV: J

Date Codes: 8015, 8035

#DEVICES: 10

16K STATIC RAM

ADDRESS SETUP TIME BEFORE CE

t_{ASC}

By AT/RM Date 10/80

LOAD: Fig. 6

ADDR PAT: DUALWC

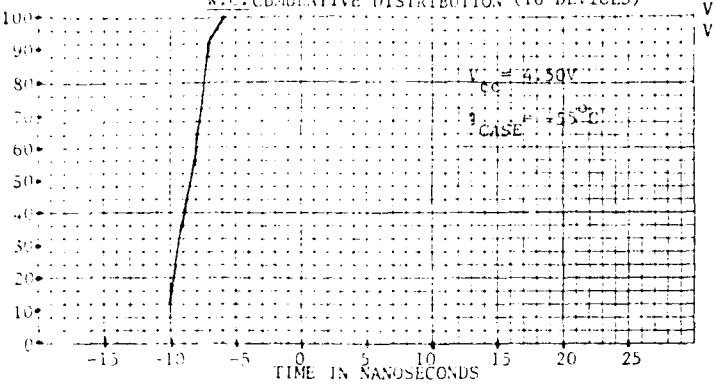
DATA PAT:

VIHC 3.0V

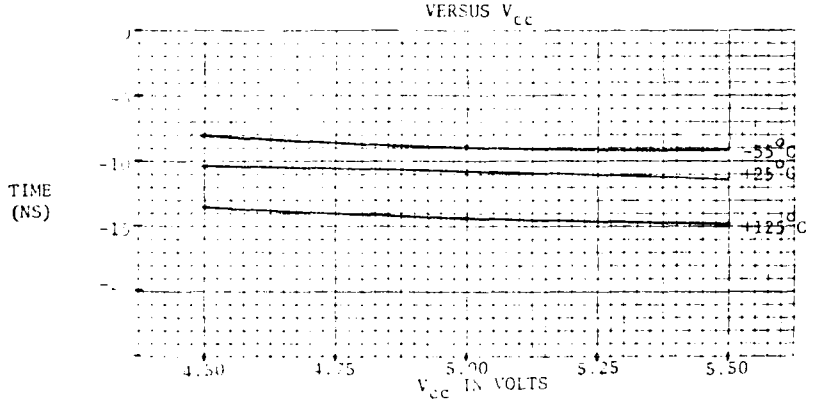
VIH 3.0V

VIL 0.0V

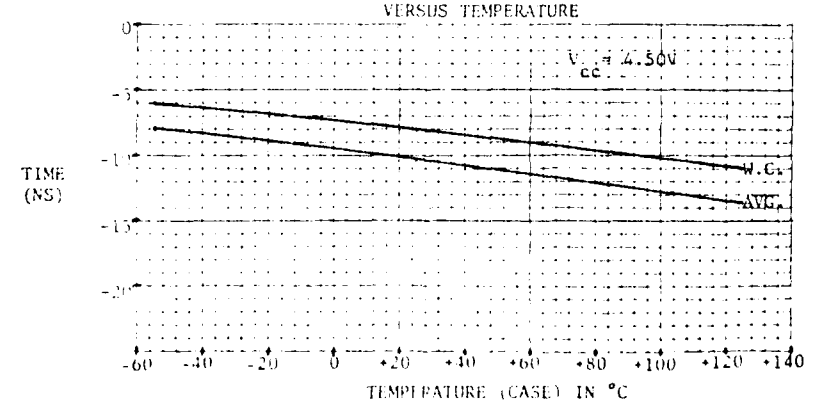
W.C. CUMULATIVE DISTRIBUTION (10 DEVICES)



AVERAGE t_{ASC} VERSUS V_{CC}



VERSUS TEMPERATURE

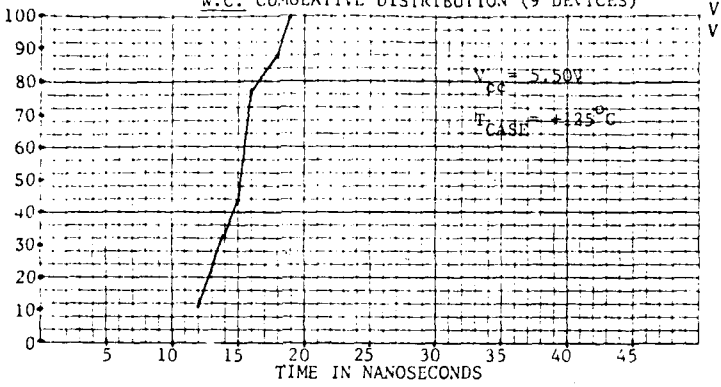


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

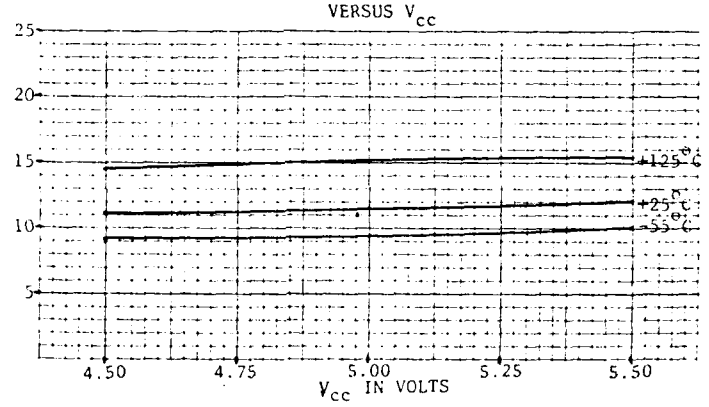
1KX8 STATIC RAM
ADDRESS HOLD TIME AFTER $\overline{CE}$
t_{AHC}

By AT/RM Date 10/80
LOAD: Fig. 6
ADDR PAT: DUALWC
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

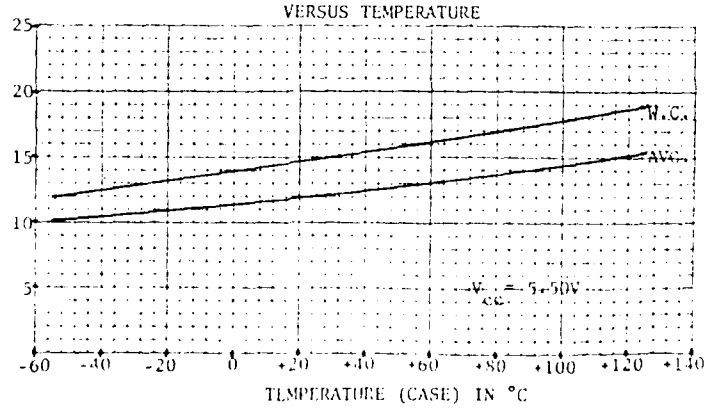
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE T_{AHC} VERSUS V_{cc}



VERSUS TEMPERATURE



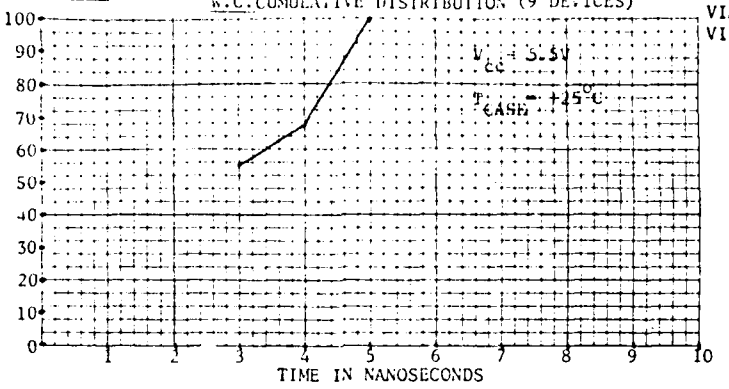
Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

1KX8 STATIC RAM
DATA TO WRITE SETUP TIME

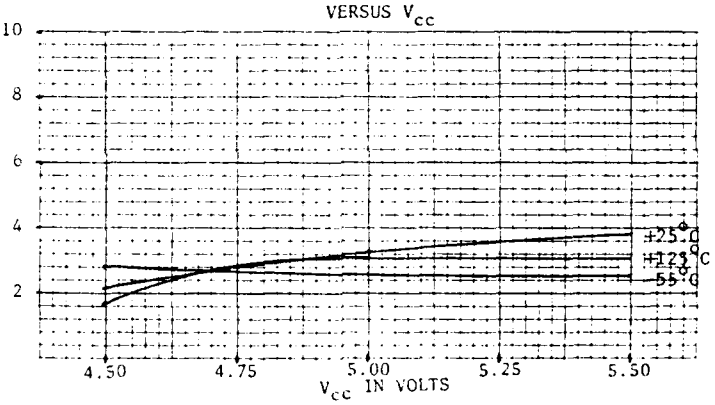
By AT/RM Date 10/80
LOAD: Fig. 6
ADDR PAT: DUALWC
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

t_{DSW}

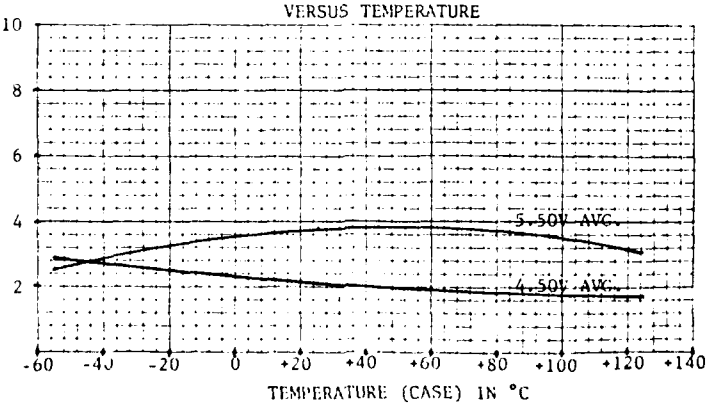
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE t_{DSW} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

P/N: MK4801P-70, MK4801AP-70

REV: J

Date Codes: 8015, 8033

#DEVICES: 16

1KX8 STATIC RAM

DATA HOLD TIME AFTER WRITE

T_{DHW}

By RM/AT Date 10/80

LOAD: Fig 6

ADDR PAT: DUALWC

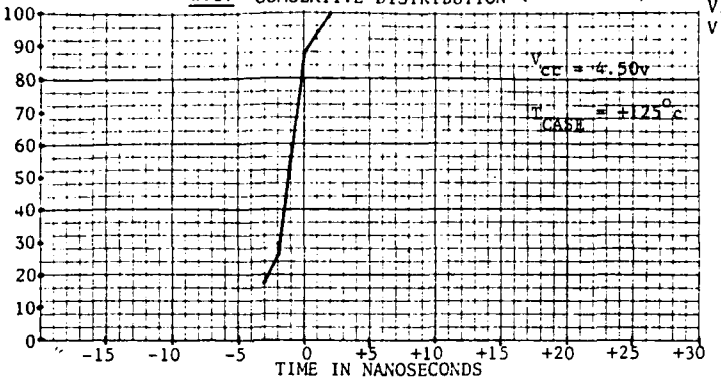
DATA PAT:

VIHC 3.0v

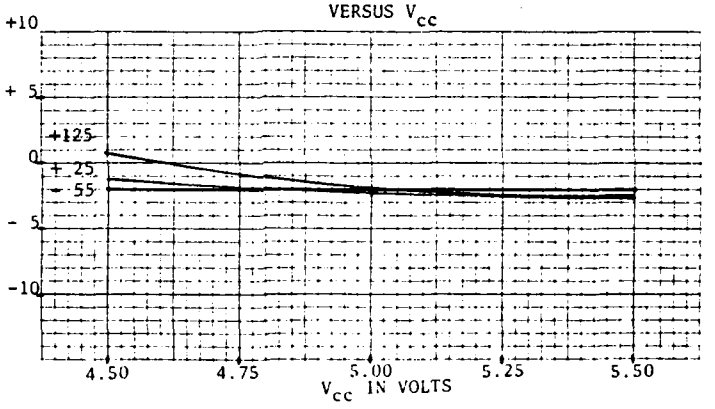
VIH 3.0V

VIL 0.0v

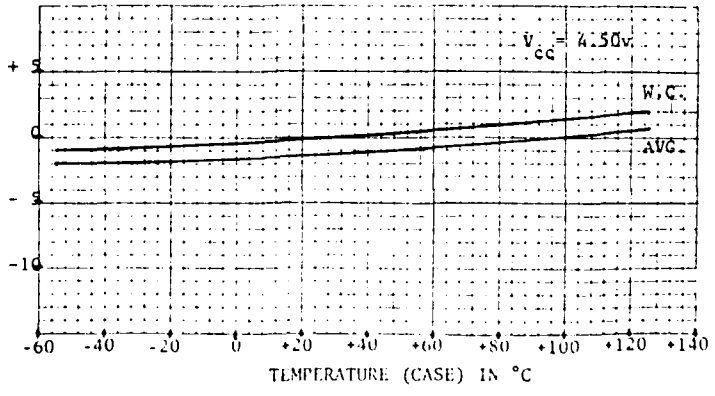
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{DHW} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

P/N: MK4801P-70, MK4801AP-70

REV: J

Date Codes: 8015, 8033

#DEVICES: 16

1KX8 STATIC RAM

WRITE PULSE WIDTH

T_{WD}

By AT/RM Date 10/80

LOAD: Fig. 6

ADDR PAT: DUALWC

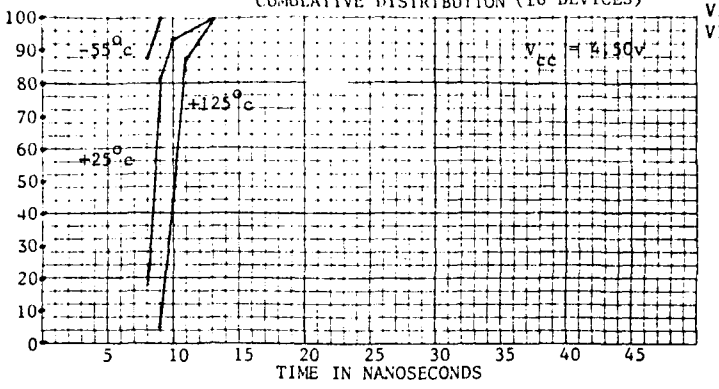
DATA PAT:

VIHC 3.0v

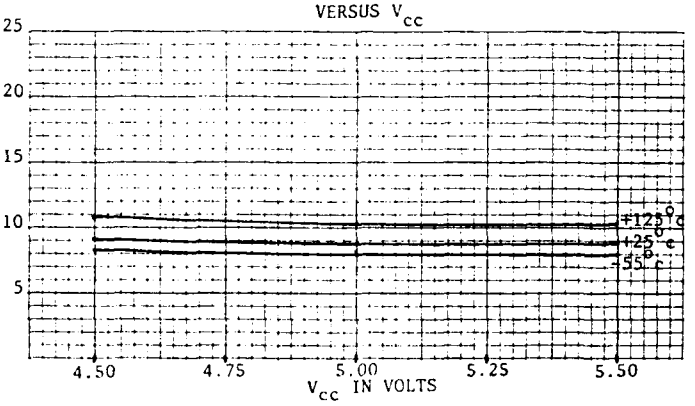
VIH 3.0v

VIL 0.0v

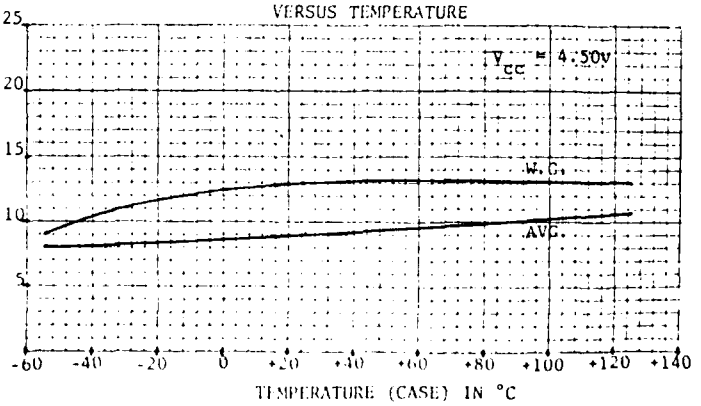
CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{WD} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

P/N: MK4801P70, MK4801AP-70

REV: J

Date Codes: 8015, 8033

#DEVICES: 16

1KX8 STATIC RAM

MINIMUM WRITE ENABLE DATA OFF TIME FOR A LOGIC 0

T_{WEZO} MIN.

By AT/RM Date 10/80

LOAD: fig. 6

ADDR PAT: SEQ. READ

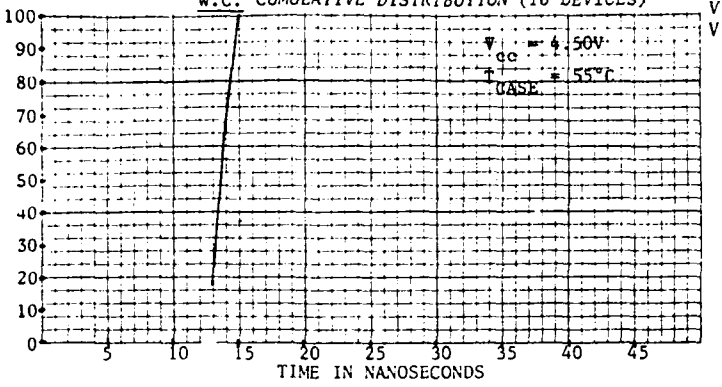
DATA PAT: ALL ZEROS

VIHC 3.0V

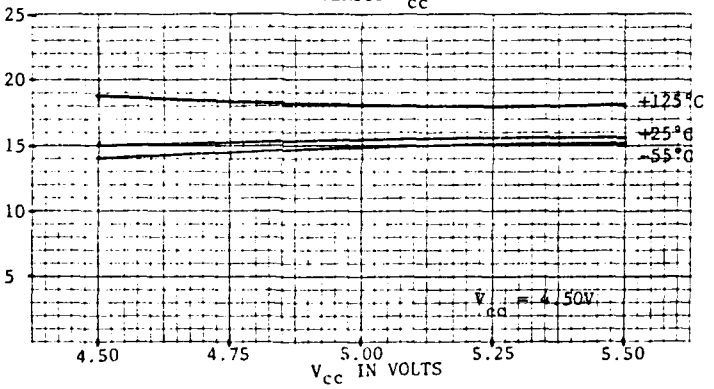
VIH 3.0V

VIL 0.0V

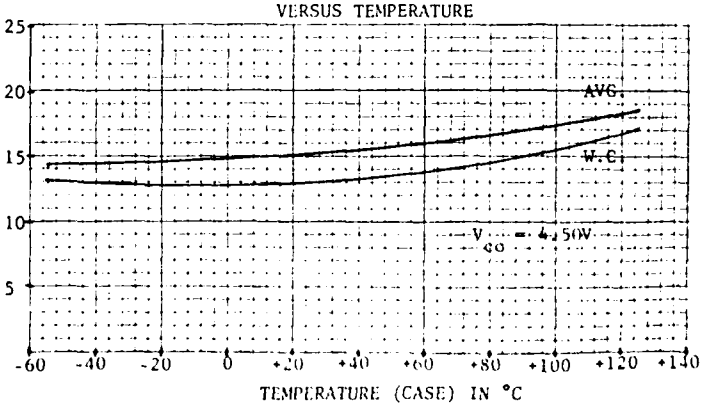
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{WEZO} MIN. VERSUS V_{cc}



VERSUS TEMPERATURE

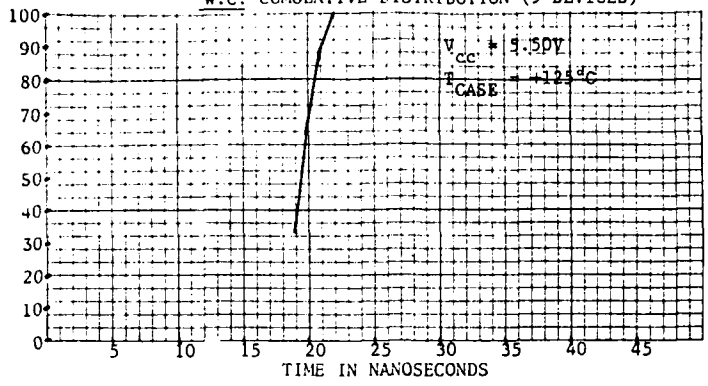


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

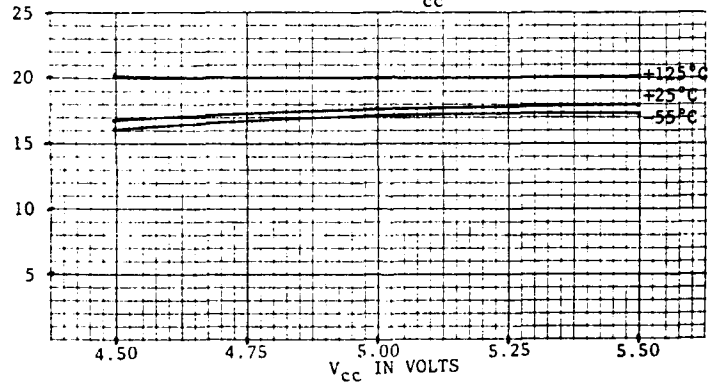
1KX8 STATIC RAM
WRITE ENABLE DATA OFFTIME
FOR A LOGIC 0
T_{WEZO} MAX.

By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROS
VIHC 3.0V
VIH 3.0V
VIL 0.0V

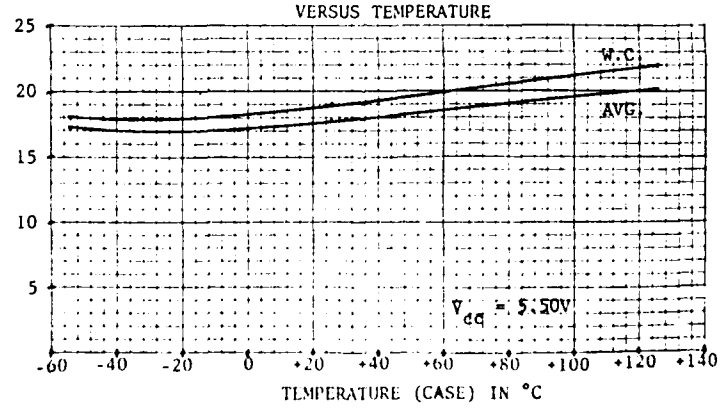
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE T_{WEZO} MAX.
VERSUS V_{cc}



VERSUS TEMPERATURE

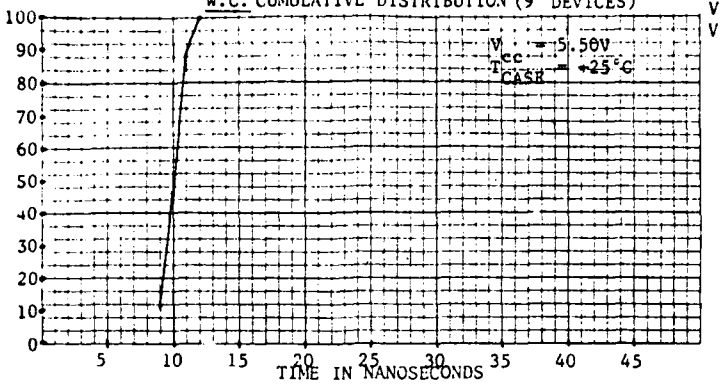


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

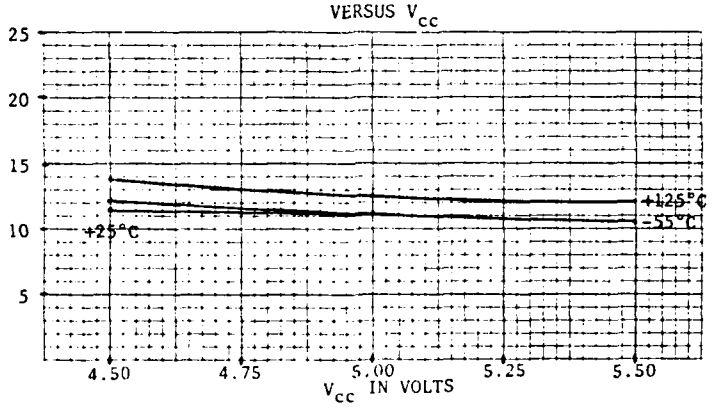
1 KX8 STATIC RAM
MINIMUM WRITE ENABLE DATA OFF TIME
FOR A LOGIC 1
T_{WEZ1} MIN.

By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: SEQ. WRITE
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

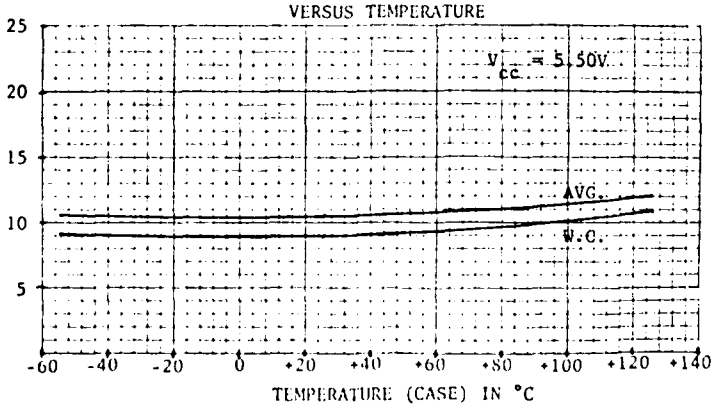
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE T_{WEZ1} MIN.
VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

P/N: MK4801P-70, MK4801AP-70

REV: J

Date Codes: 8015, 8033

#DEVICES: 16

1KX8 STATIC RAM

MAXIMUM WRITE ENABLE DATA OFF TIME FOR A LOGIC 1 T_{WEZ1} MAX.

By AT/RM Date 10/80

LOAD: fig. 6

ADDR PAT: SEQ. READ

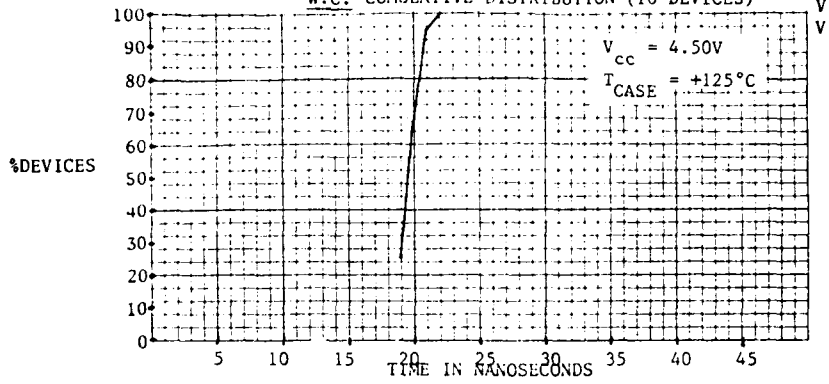
DATA PAT: All ones

VIHC 3.0V

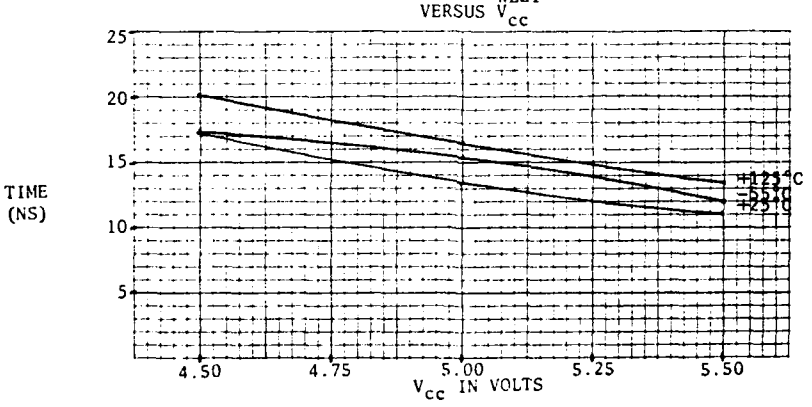
VIH 3.0V

VIL 0.0V

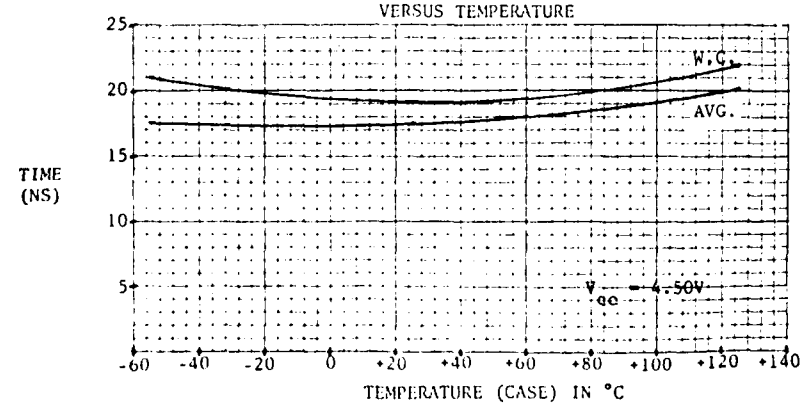
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{WEZ1} MAX. VERSUS V_{cc}



VERSUS TEMPERATURE

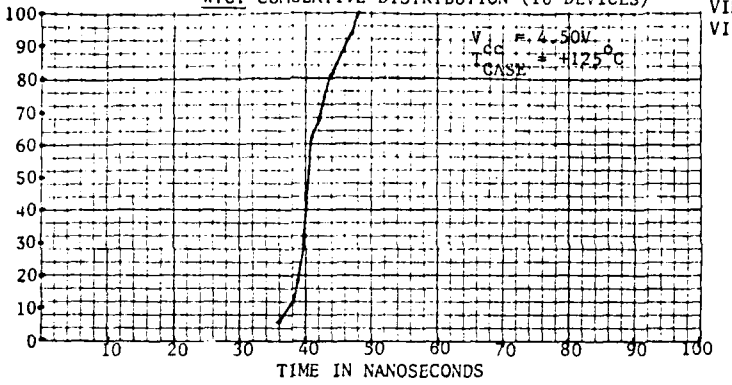


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

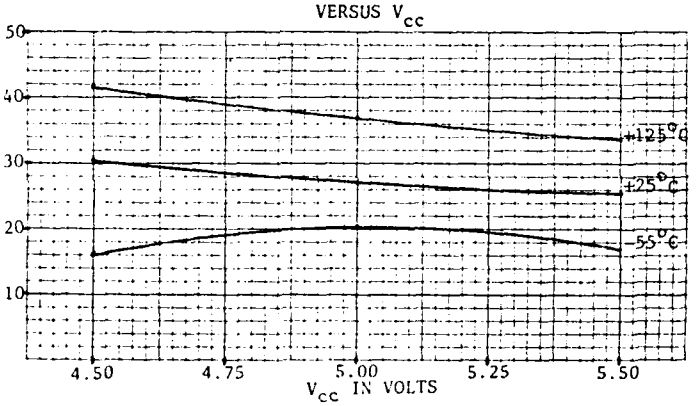
1KX8 STATIC RAM
WRITE PULSE LEAD TIME
T_{WPL}

By AT/KM Date 10/80
LOAD: fig. 6
ADDR PAT: DUALWC
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

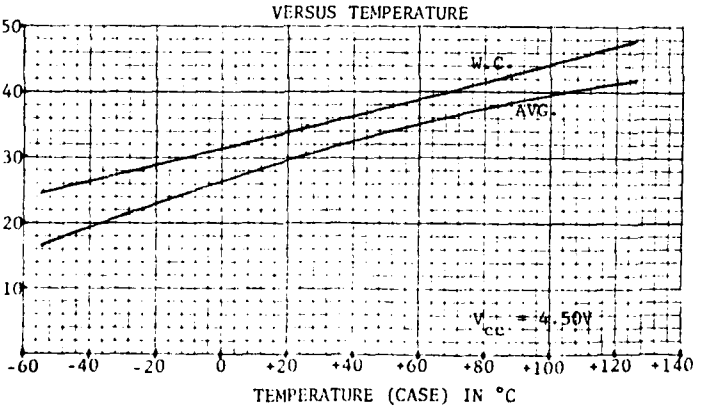
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE T_{WPL}
VERSUS V_{cc}



VERSUS TEMPERATURE

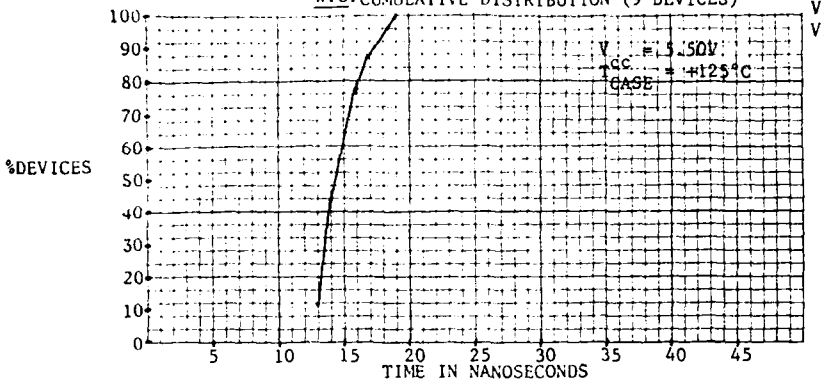


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

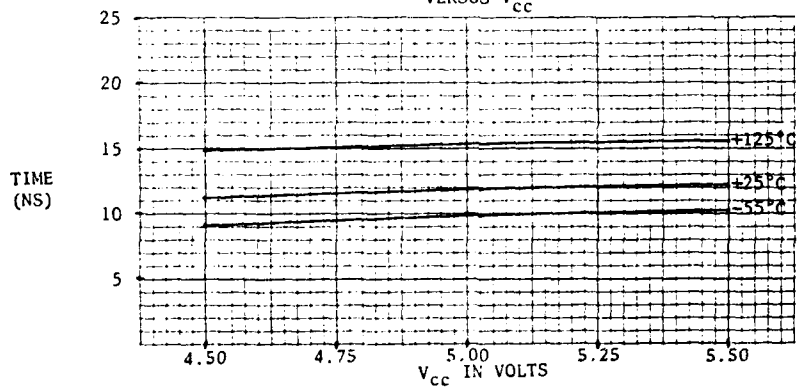
1KX8 STATIC RAM
ADDRESS HOLD TIME AFTER $\overline{WE}$
T_{AHW}

By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: RCGAL
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

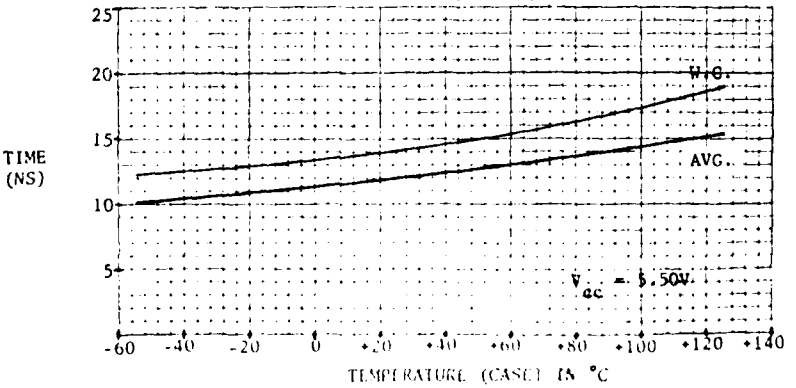
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE T_{AHW} VERSUS V_{cc}



VERSUS TEMPERATURE

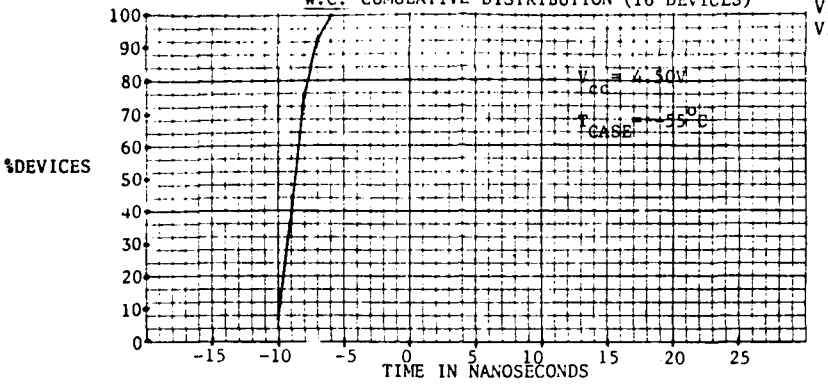


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

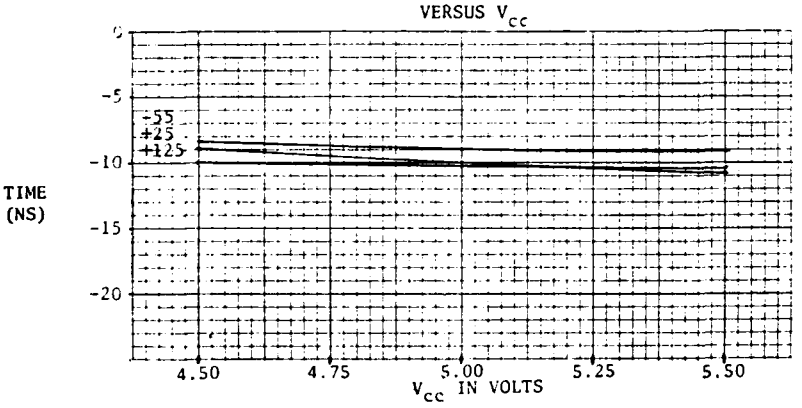
1KX8 STATIC RAM
ADDRESS SETUP TIME BEFORE $\overline{WE}$
t_{ASW}

By AT/RM Date 10/80
LOAD: Fig. 6
ADDR PAT: DUALWC
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

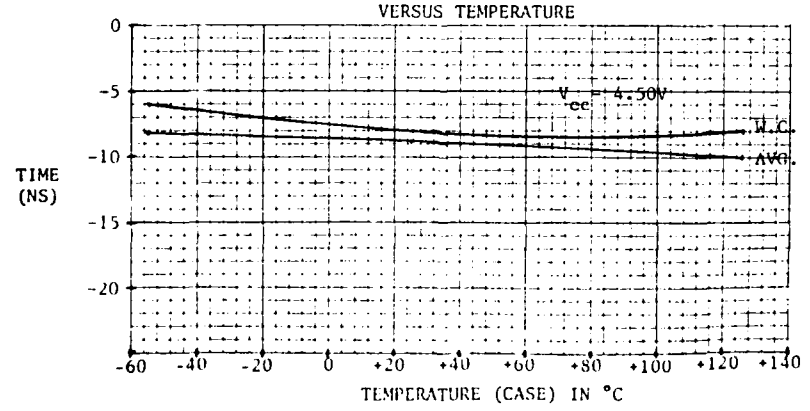
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE t_{ASW} VERSUS V_{cc}



VERSUS TEMPERATURE

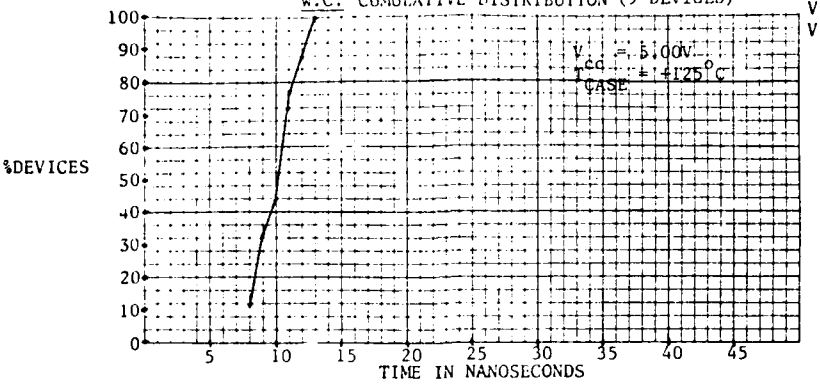


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

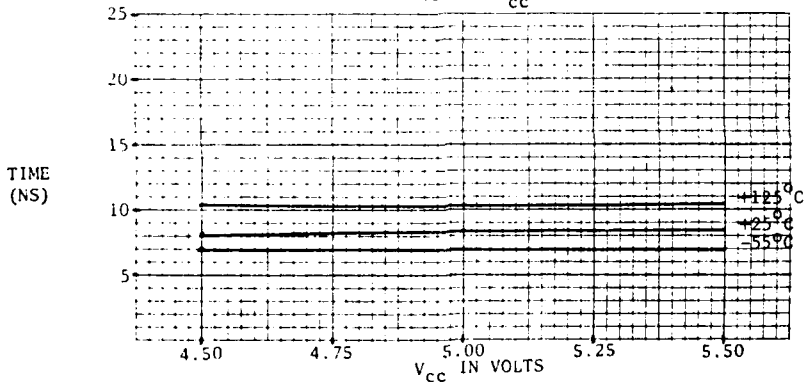
1KX8 STATIC RAM
CHIP ENABLE TO WRITE SETUP TIME
T_{CEW}

By AT/RM Date 10/80
LOAD: fig. 6
ADDR PAT: RCGAL
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

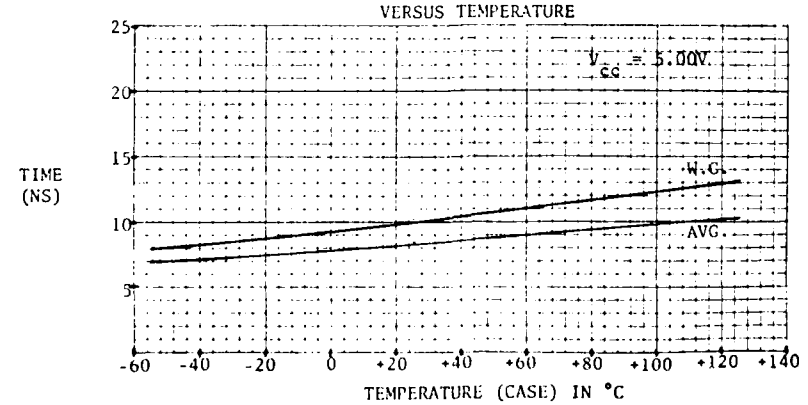
W.C. CUMULATIVE DISTRIBUTION (9 DEVICES)



AVERAGE T_{CEW}
VERSUS V_{cc}



VERSUS TEMPERATURE

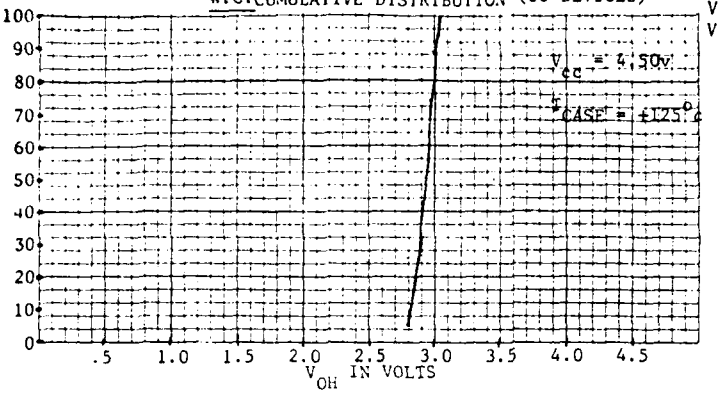


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

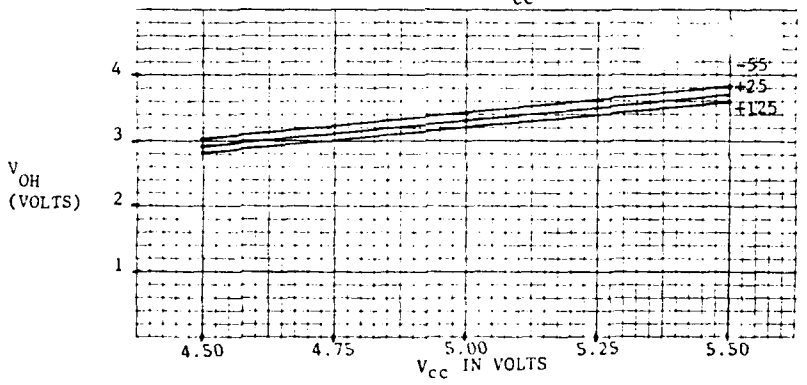
1KX8 STATIC RAM
OUTPUT HIGH VOLTAGE
V_{OH}

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: HOLD XY
DATA PAT: ALL ONES
VIHC 3.0v
VIH 3.0V
VIL 0.0v

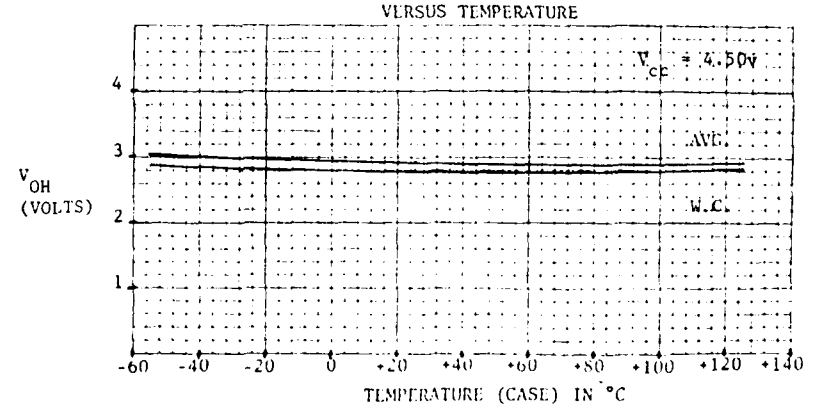
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE V_{OH} VERSUS V_{cc}



VERSUS TEMPERATURE

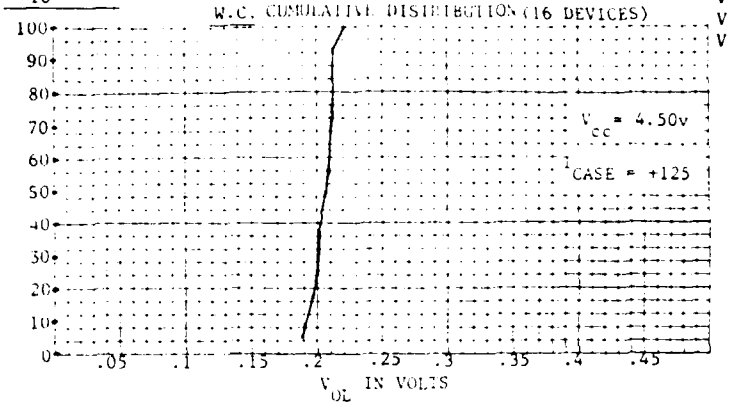


Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015, 8033
#DEVICES: 16

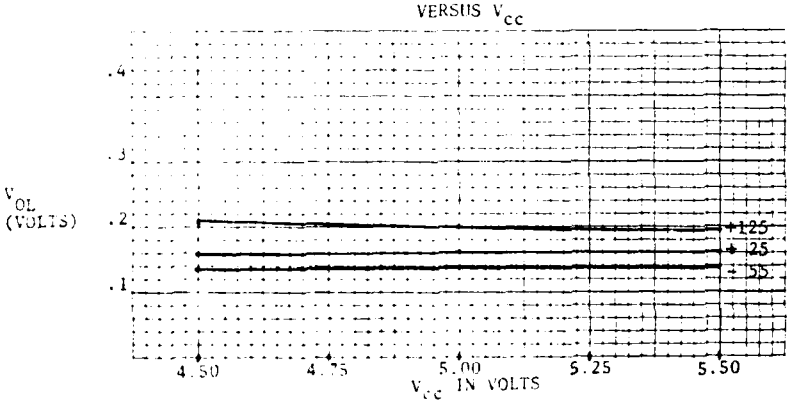
1 KX8 STATIC RAM
OUTPUT LOW VOLTAGE
VOL.

By RM/AT Date 10/80
LOAD: Fig 6
ADDR PAT: HOLD XY
DATA PAT: All ZEROES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

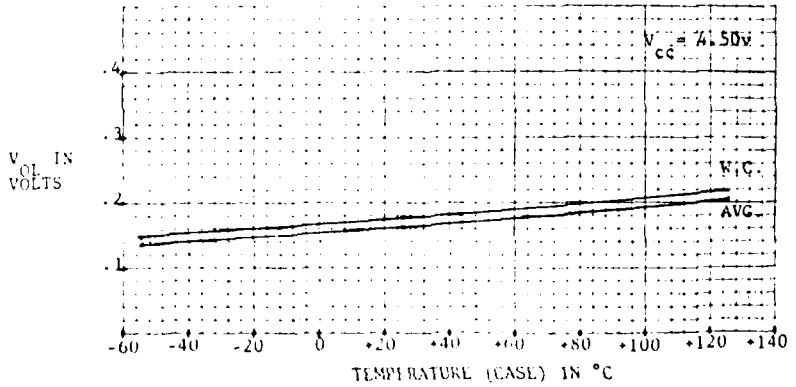
W.C. CUMULATIVE DISTRIBUTION (16 DEVICES)



AVERAGE V_{OL} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

1KX8 STATIC RAM

By AT/RM Date 10/80

P/N: MK4801P-70, MK4801AP-70

REV: J

Date Codes: 8015, 8033

#DEVICES: 16

SUPPLY CURRENT FROM V_{cc}, READ MODE

I_{CC_1}

LOAD: NONE

ADDR PAT: SEQ. READ

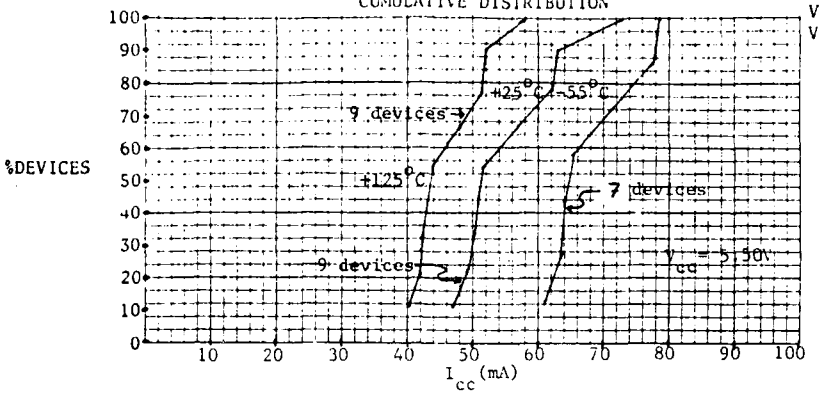
DATA PAT: CHKBD

VIHC 3.0V

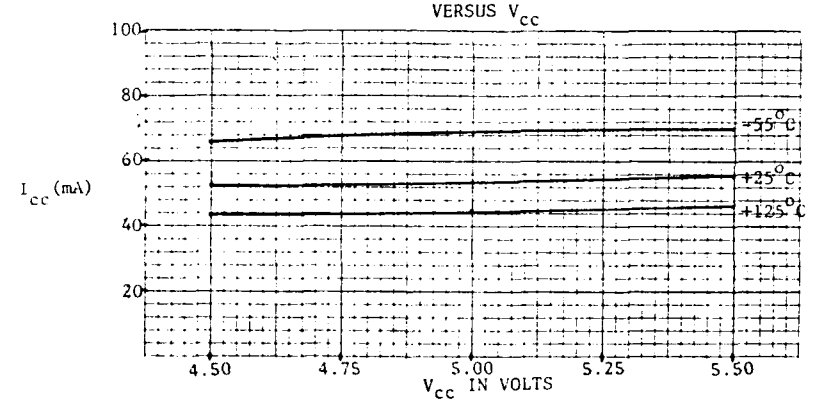
VIH 3.0V

VIL 0.0V

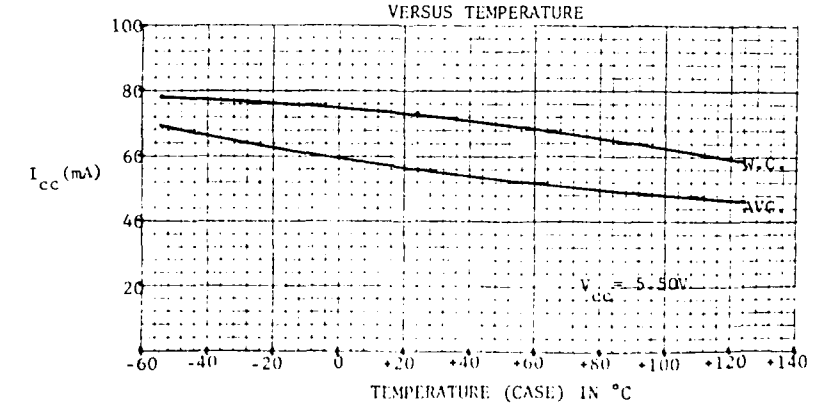
CUMULATIVE DISTRIBUTION



AVERAGE I_{cc} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek

P/N: MK4801P-70, MK4801AP-70

REV: J

Date Codes: 8015, 8033

#DEVICES: 16

1KX8 STATIC RAM

SUPPLY CURRENT FROM V_{cc}, WRITE MODE

I_{cc_2}

By AT/RM Date 10/80

LOAD: NONE

ADDR PAT: SEQ WRITE

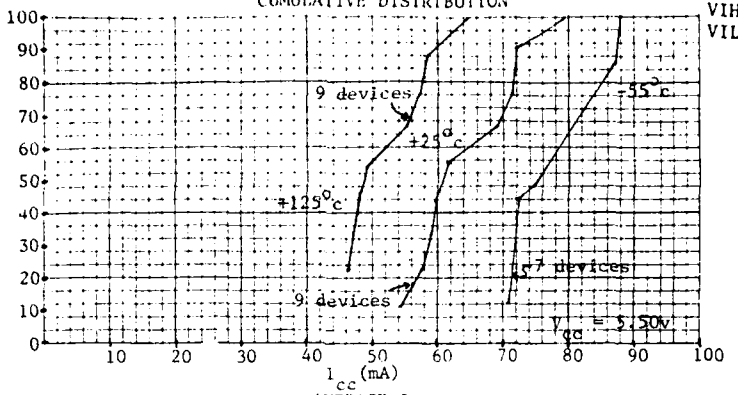
DATA PAT: CHKBD

VIHC 3.0v

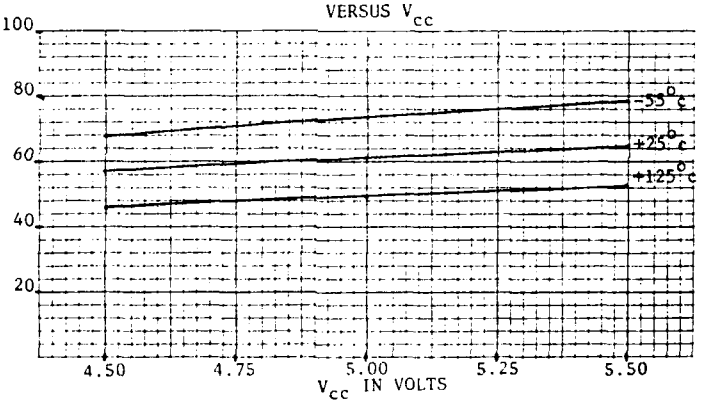
VIH 3.0v

VIL 0.0v

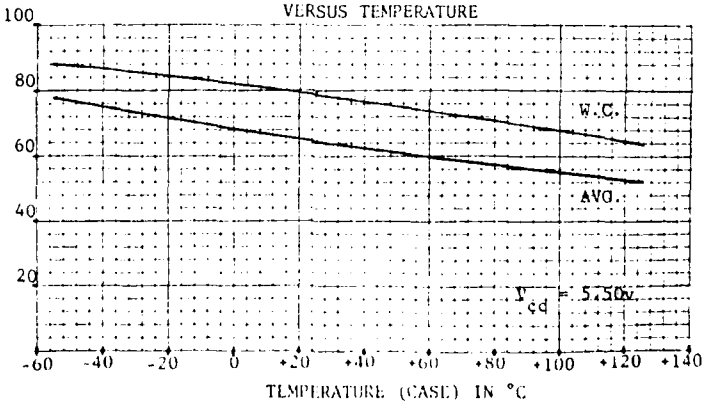
CUMULATIVE DISTRIBUTION



AVERAGE I_{cc} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4801P-70, MK4801AP-70
REV: J
Date Codes: 8015,8033
#DEVICES: 16

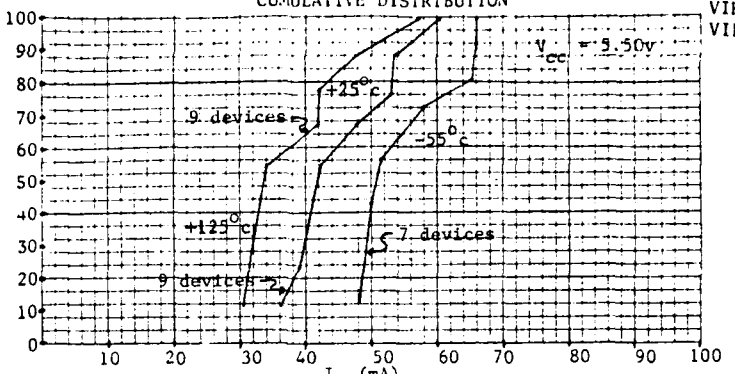
1KX8 STATIC RAM

SUPPLY CURRENT FROM V_{cc}, STANDBY MODE

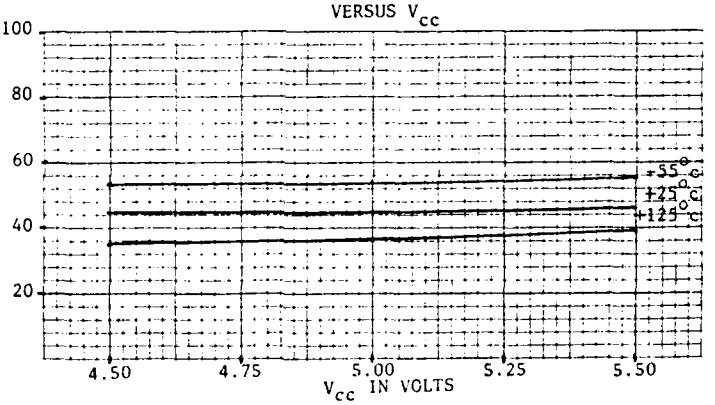
By AT/RM Date 10/80
LOAD: NONE
ADDR PAT: NONE
DATA PAT: NONE
VIHC 3.0v
VIH 3.0v
VIL 0.0v

I_{cc_3}

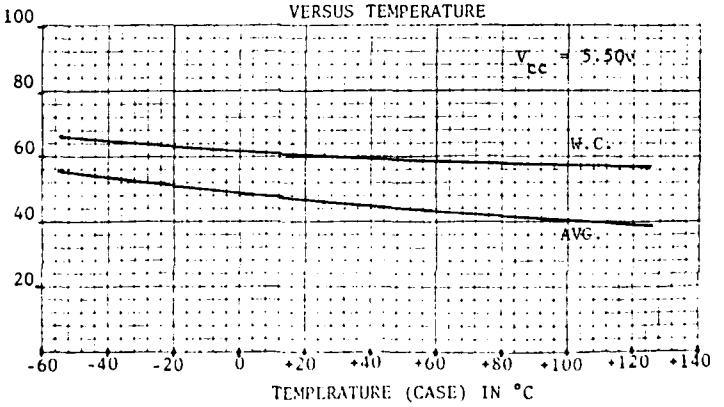
CUMULATIVE DISTRIBUTION



AVERAGE I_{cc} VERSUS V_{cc}



VERSUS TEMPERATURE



APPENDIX II

2KX8 STATIC RAM

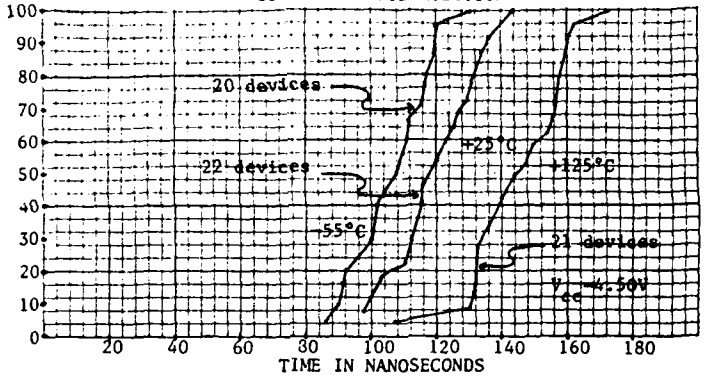
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
RANDOM READ CYCLE TIME

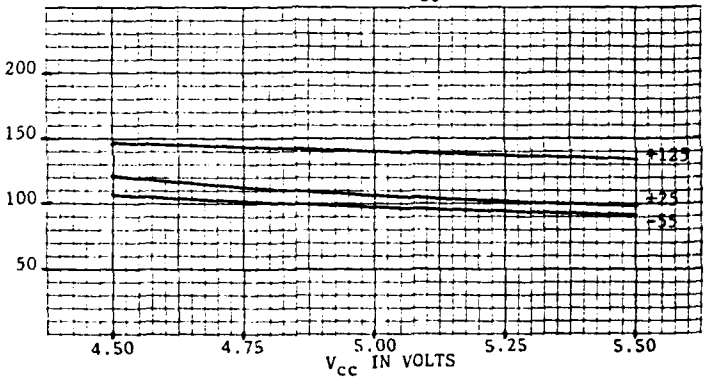
By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: RCGAL
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

T_{RC}

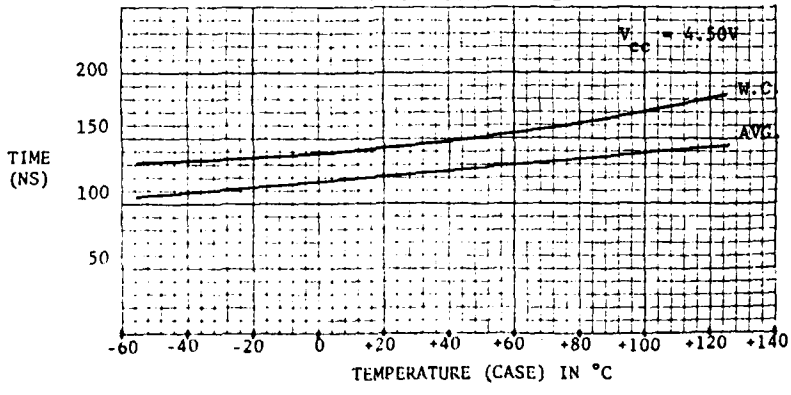
CUMULATIVE DISTRIBUTION



AVERAGE T_{RC}
VERSUS V_{cc}



VERSUS TEMPERATURE



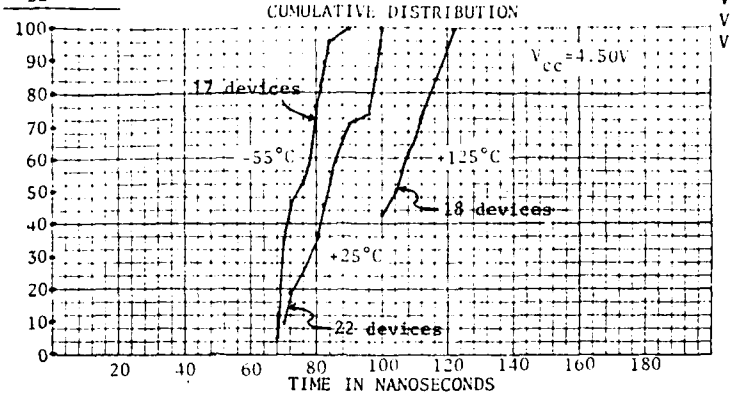
Vendor: Mostek
P/N: MK4802
REV: X
Date Codes: 8022/31/33
#DEVICES: 22

2KX8 STATIC RAM

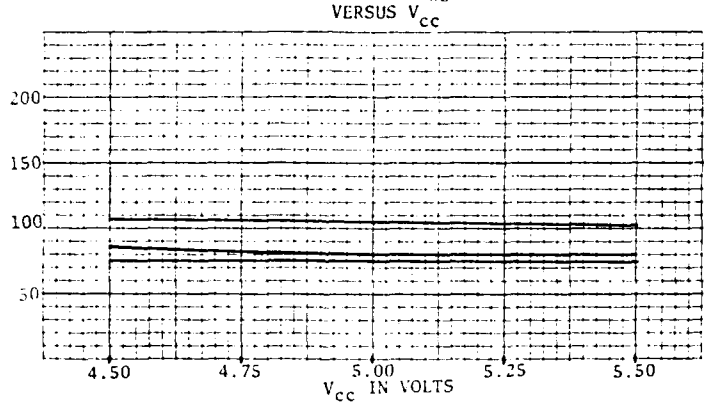
RANDOM WRITE CYCLE TIME
t_{WC}

By AT/RM Date 10/80
LOAD: Fig. 6
ADDR PAT: DUALRC
DATA PAT
VIHC 3.0V
VIH 3.0V
VIL 0.0V

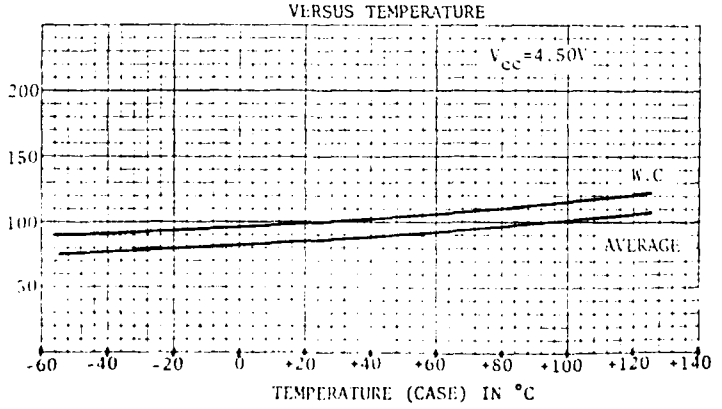
CUMULATIVE DISTRIBUTION



AVERAGE t_{WC}
VERSUS V_{cc}



VERSUS TEMPERATURE

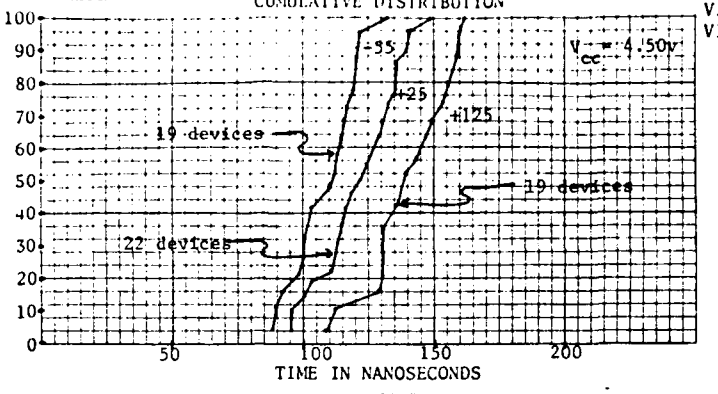


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

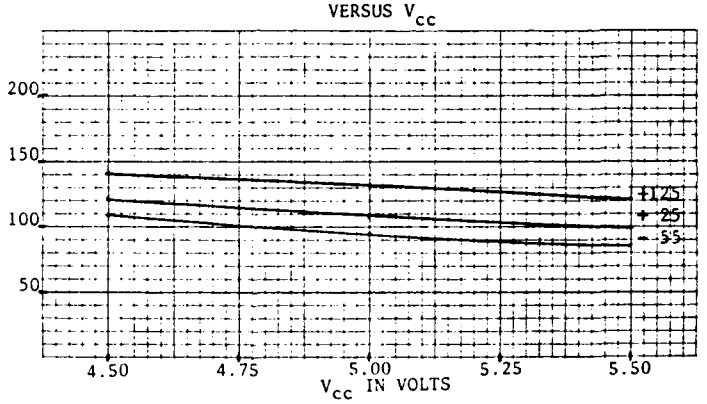
2KX8 STATIC RAM
ADDRESS ACCESS TIME
T_{AA}

By RM/AT Date 10/80
LOAD: FIG 6
ADDR PAT: ADCOMP
DATA PAT:
VIHC 3.0v
VIH 3.0V
VIL 0.0v

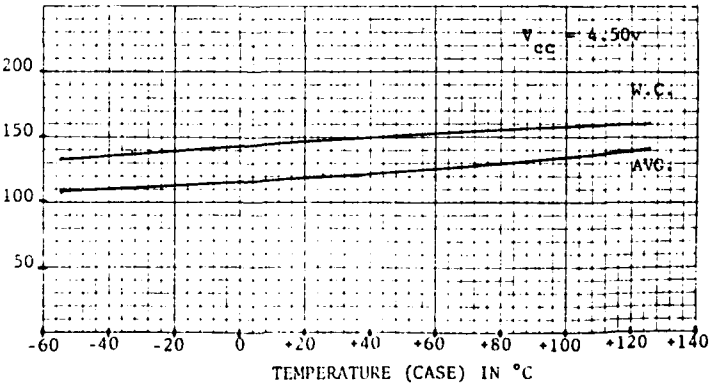
CUMULATIVE DISTRIBUTION



AVERAGE T_{AA}
VERSUS V_{cc}



VERSUS TEMPERATURE



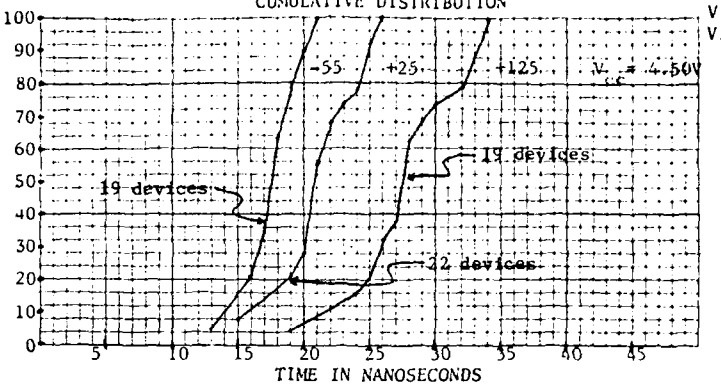
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
CHIP ENABLE ACCESS TIME

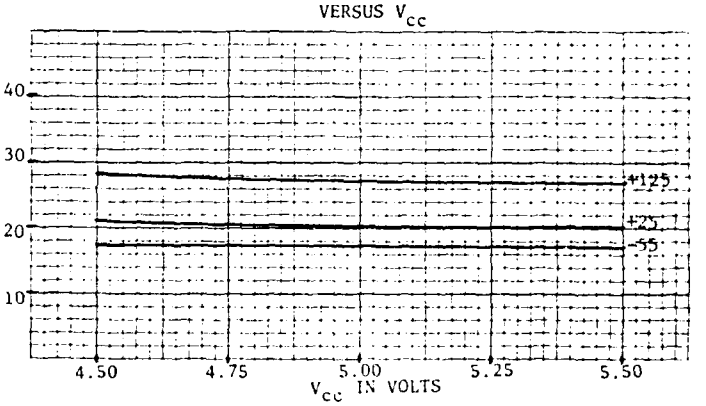
By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: ADCOMP
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

T_{CEA}

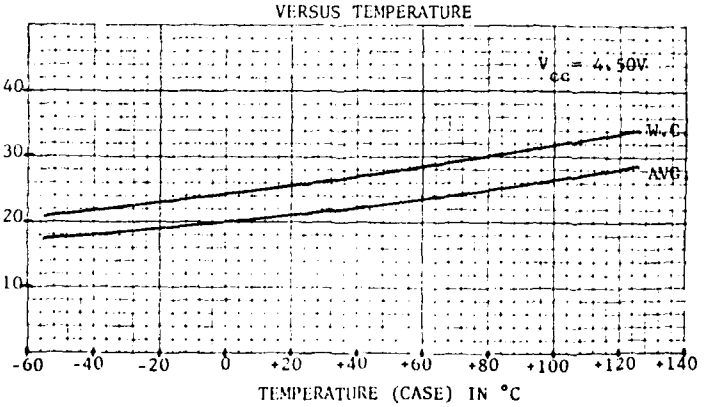
CUMULATIVE DISTRIBUTION



AVERAGE T_{CEA}
VERSUS V_{cc}



VERSUS TEMPERATURE

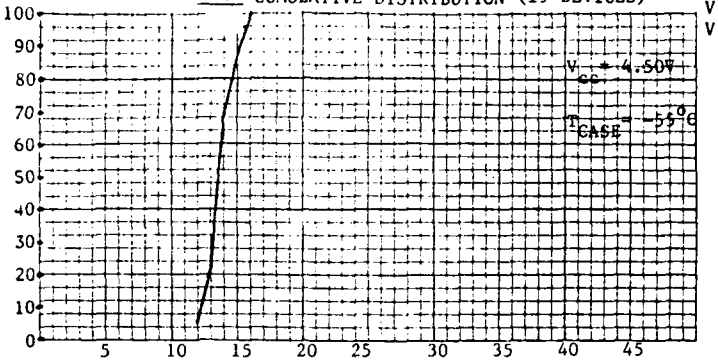


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

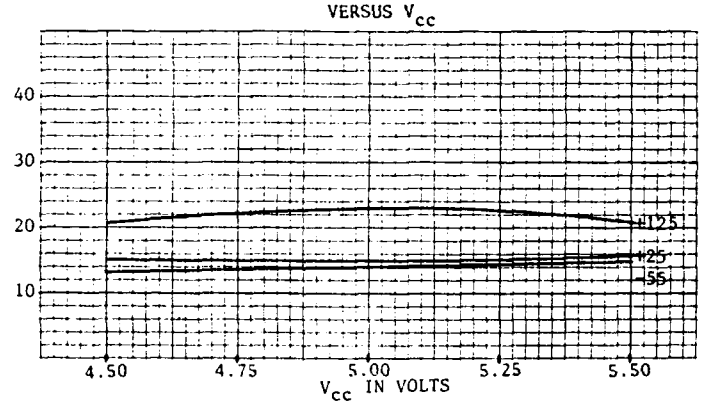
2KX8 STATIC RAM
MINIMUM CHIP ENABLE DATA OFF
TIME FOR A LOGIC 1
$T_{CEZ\emptyset}$ MIN

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROES
VIHC 3.0V
VIH 0.0V
VIL 0.0V

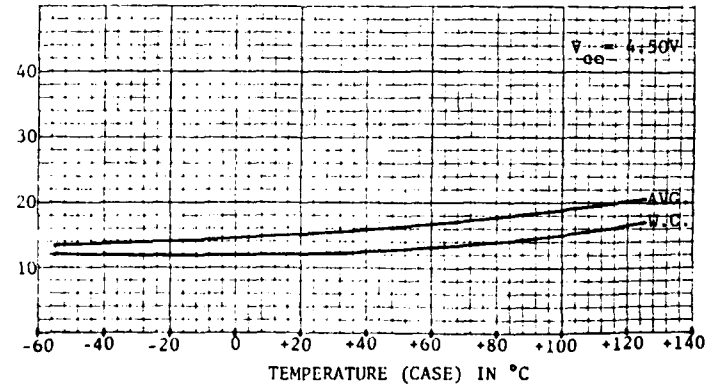
W.C. CUMULATIVE DISTRIBUTION (19 DEVICES)



AVERAGE $T_{CEZ\emptyset}$ MIN.
VERSUS V_{cc}



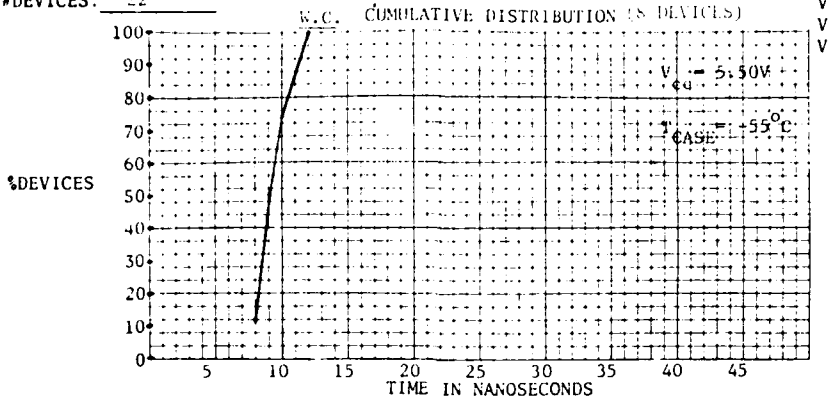
VERSUS TEMPERATURE

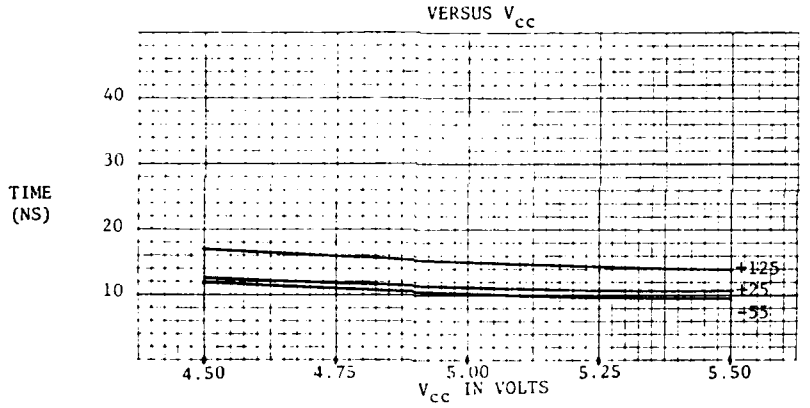


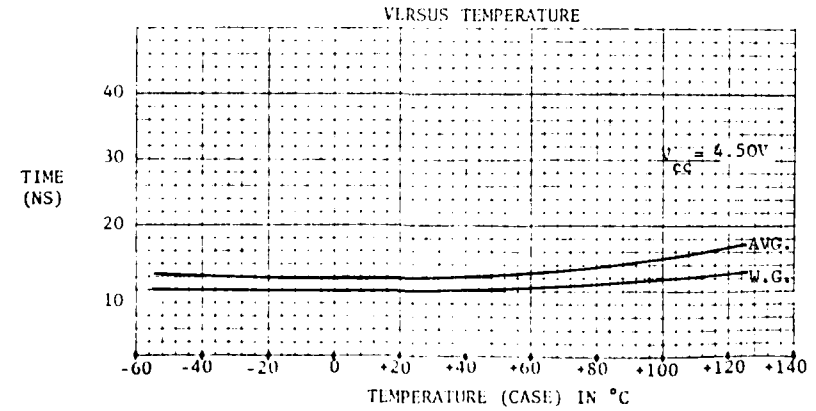
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
MINIMUM CHIP ENABLE TO DATA OFF TIME FOR A LOGIC 1
T_{CEZ1} MIN.

By PW/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V





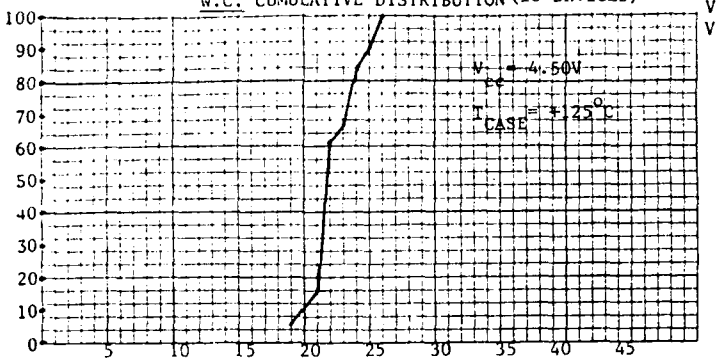


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

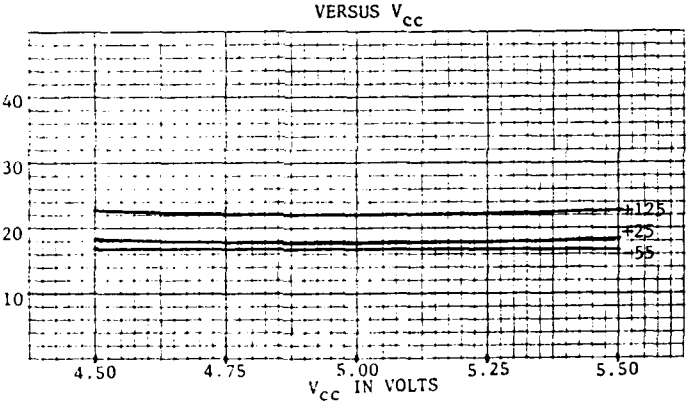
2KX8 STATIC RAM
MAXIMUM CHIP ENABLE DATA OFF
TIME FOR A LOGIC 0
$T_{CEZO\ MAX}$

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

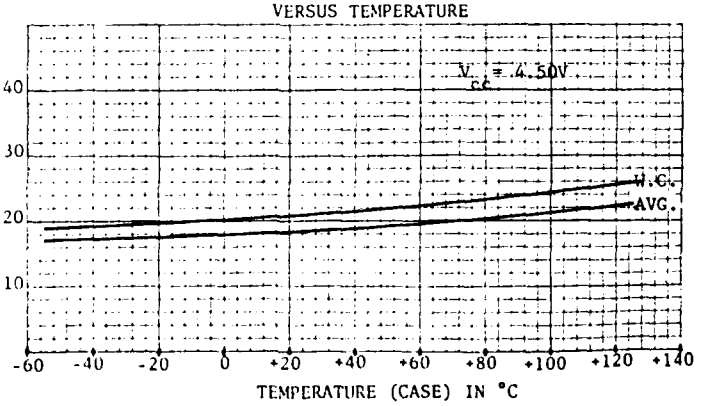
W.C. CUMULATIVE DISTRIBUTION (18 DEVICES)



AVERAGE $T_{CEZO\ MAX.}$ VERSUS V_{cc}



VERSUS TEMPERATURE

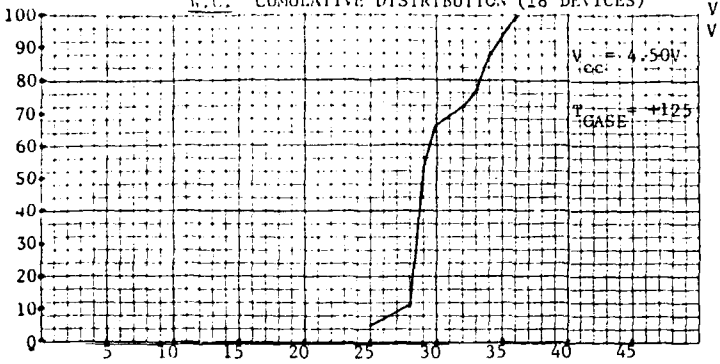


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

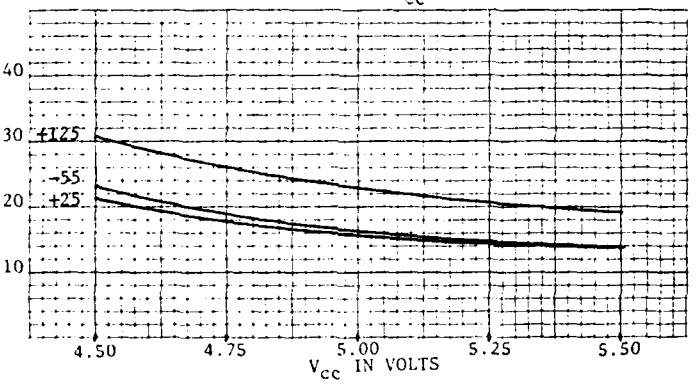
2KX8 STATIC RAM
MAXIMUM CHIP ENABLE TO DATA OFF TIME FOR A LOGIC 1
T_{CEZ1} MAX.

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

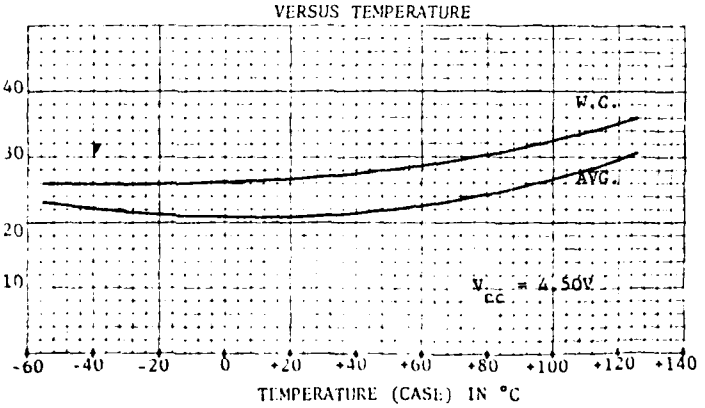
W.C. CUMULATIVE DISTRIBUTION (18 DEVICES)



AVERAGE T_{CEZ1} MAX. VERSUS V_{cc}



VERSUS TEMPERATURE



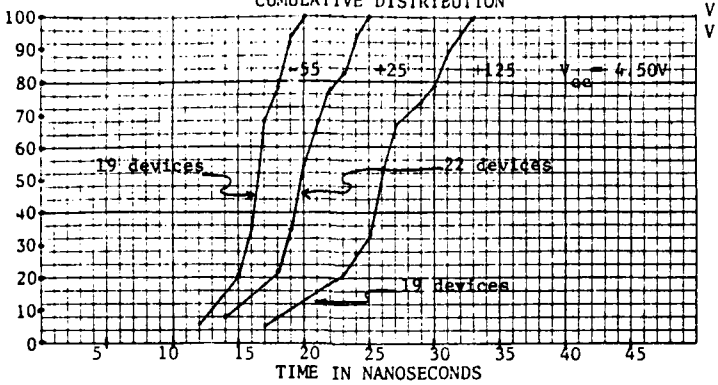
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
OUTPUT ENABLE ACCESS TIME

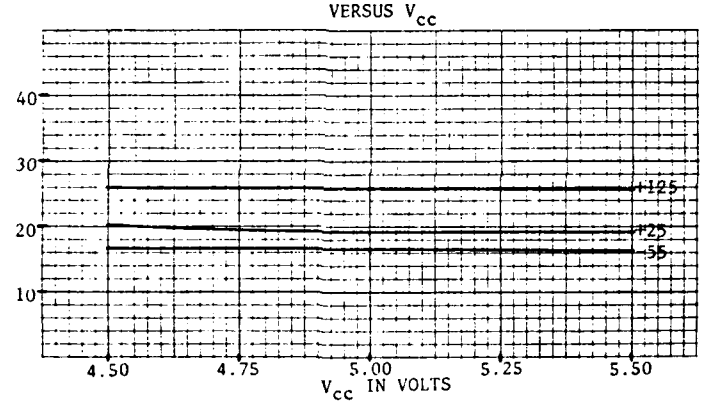
T_{OEA}

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SLDIAG
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

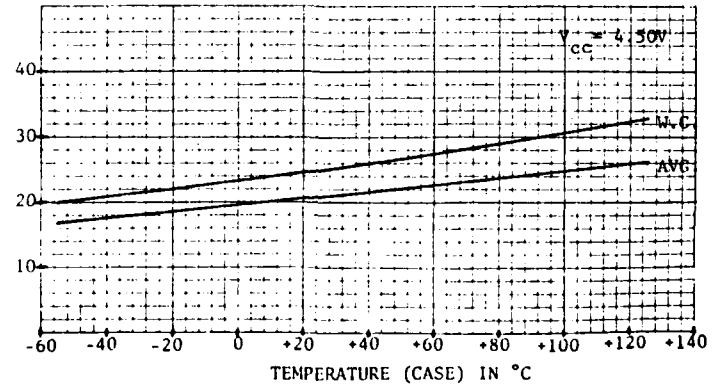
CUMULATIVE DISTRIBUTION



AVERAGE T_{OEA} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

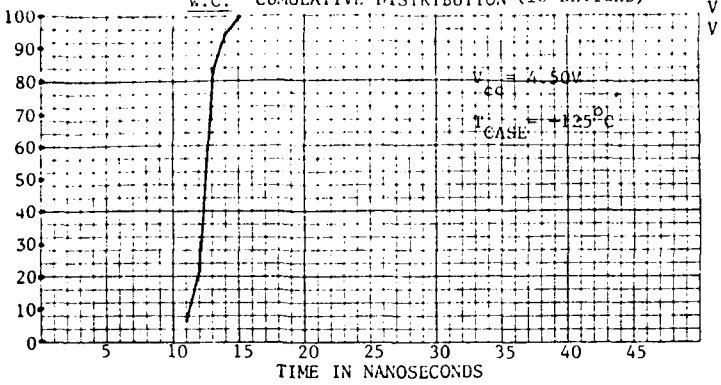
2KX8 STATIC RAM

By RM/AT Date 10/80
LOAD: FIG. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

MINIMUM OUTPUT ENABLE TO DATA OFF TIME FOR A LOGIC 0

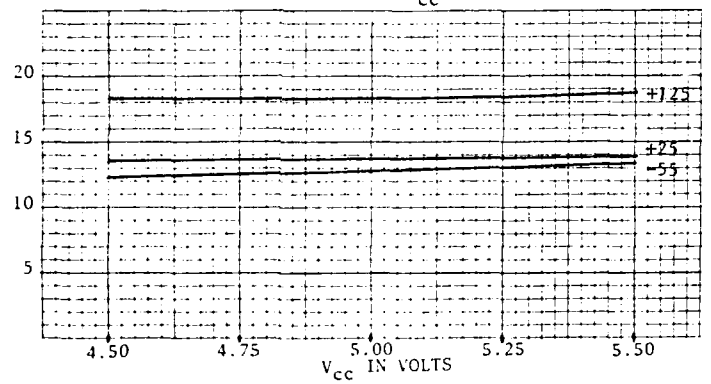
T_{OEZO} MIN.

W.C. CUMULATIVE DISTRIBUTION (18 DEVICES)

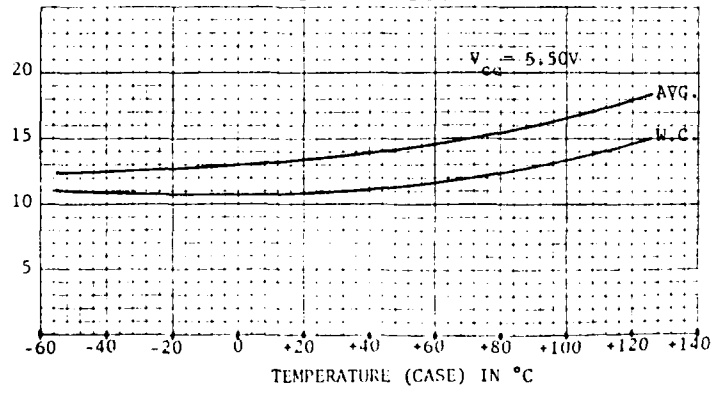


AVERAGE T_{OEZO} MIN.

VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

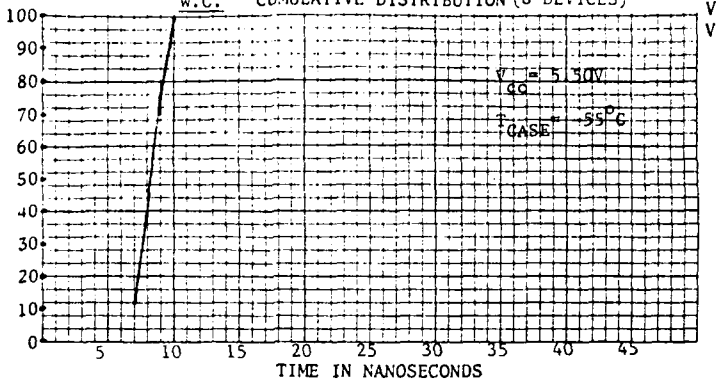
2KX8 STATIC RAM

MINIMUM OUTPUT ENABLE TO DATA OFF TIME FOR A LOGIC 1

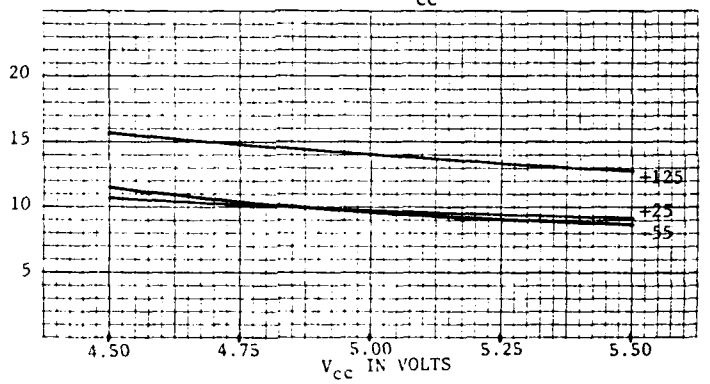
T_{OEZ1} MIN.

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

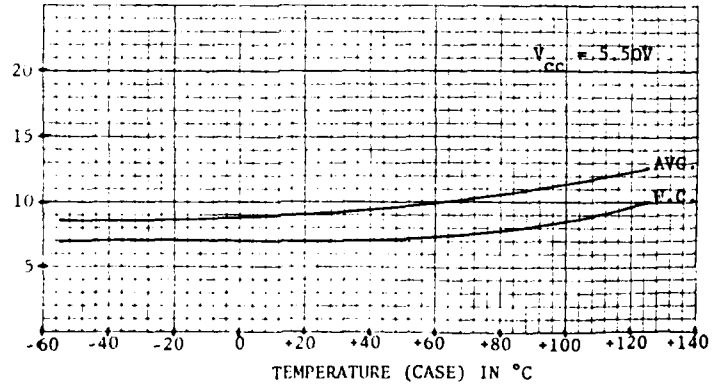
W.C. CUMULATIVE DISTRIBUTION (8 DEVICES)



AVERAGE T_{OEZ1} MIN. VERSUS V_{cc}



VERSUS TEMPERATURE

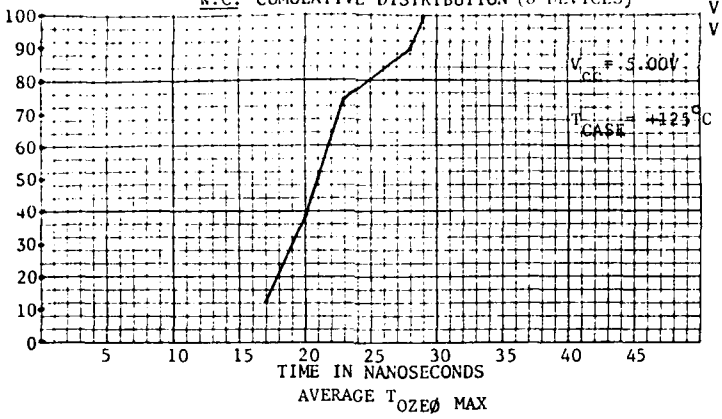


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33731
#DEVICES: 22

2KX8 STATIC RAM
MAXIMUM OUTPUT ENABLE TO DATA OFF
TIME FOR A LOGIC Ø
$T_{OEZØ}$ MAX

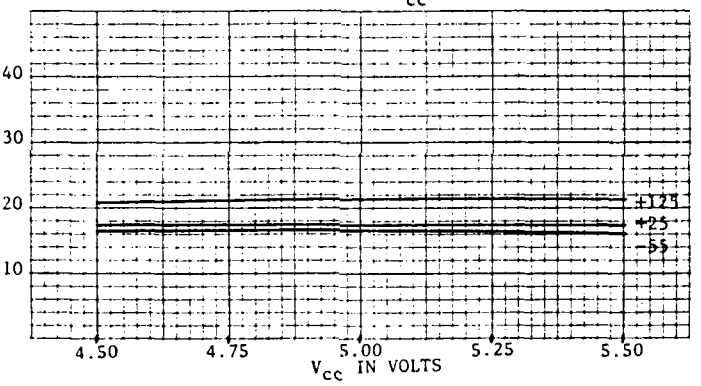
By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

W.C. CUMULATIVE DISTRIBUTION (8 DEVICES)

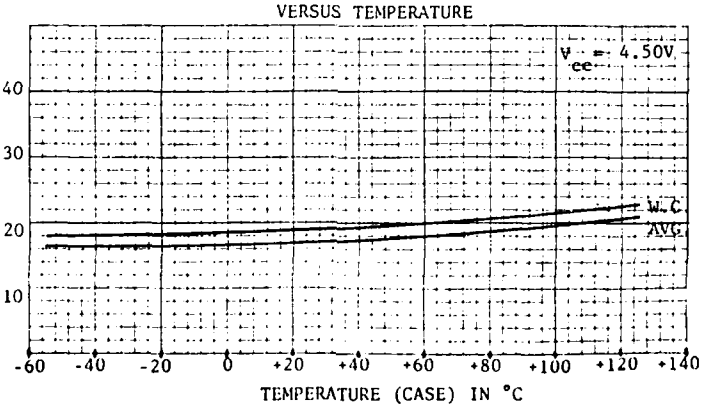


AVERAGE $T_{OZEØ}$ MAX

VERSUS V_{cc}



VERSUS TEMPERATURE

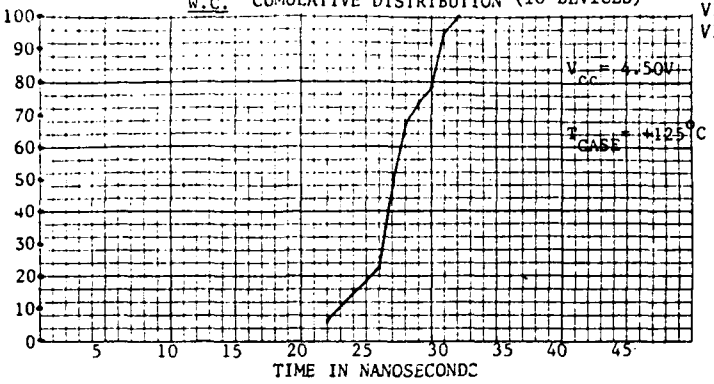


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

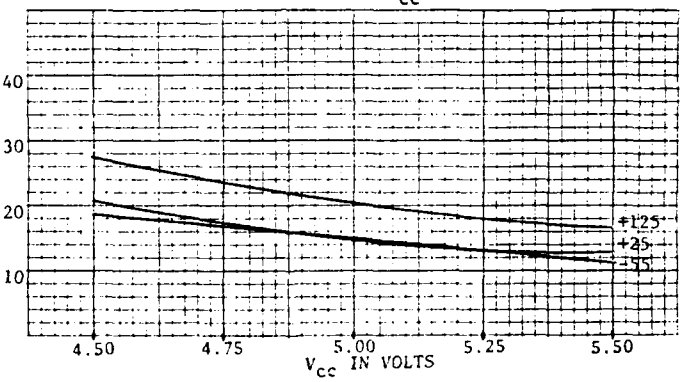
2KX8 STATIC RAM
MAXIMUM OUTPUT ENABLE TO DATA OFF TIME FOR A LOGIC 1
T_{OEZ1} MAX

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

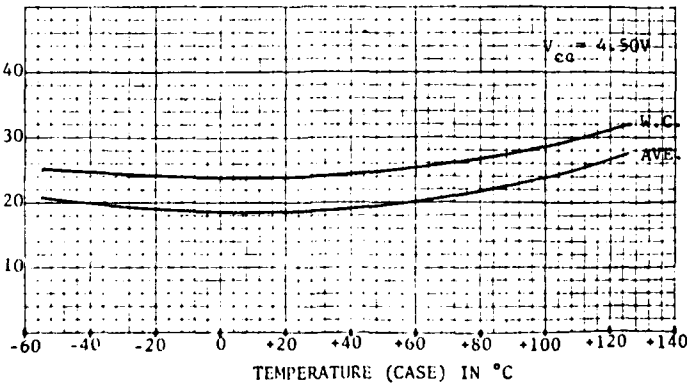
W.C. CUMULATIVE DISTRIBUTION (18 DEVICES)



AVERAGE T_{OEZ1} MAX. VERSUS V_{CC}



VERSUS TEMPERATURE

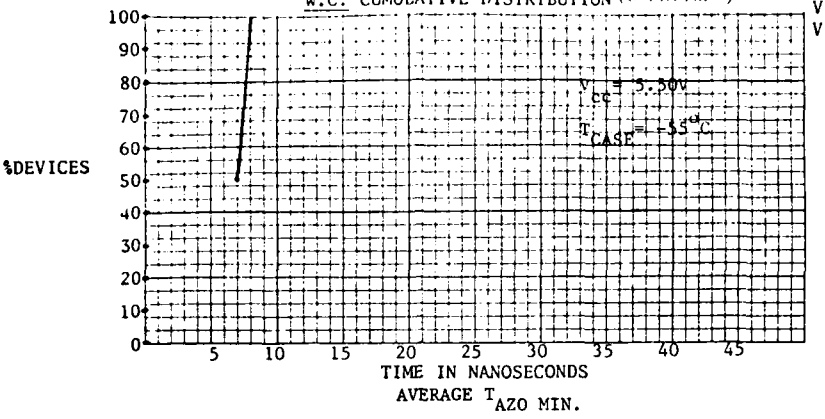


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

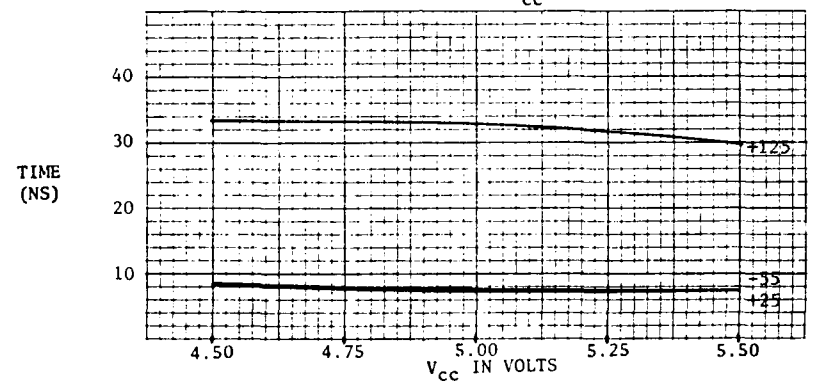
2KX8 STATIC RAM

MINIMUM ADDRESS DATA OFF TIME
FOR A LOGIC 0
T_{AZO} MIN.
W.C. CUMULATIVE DISTRIBUTION (8 DEVICES)

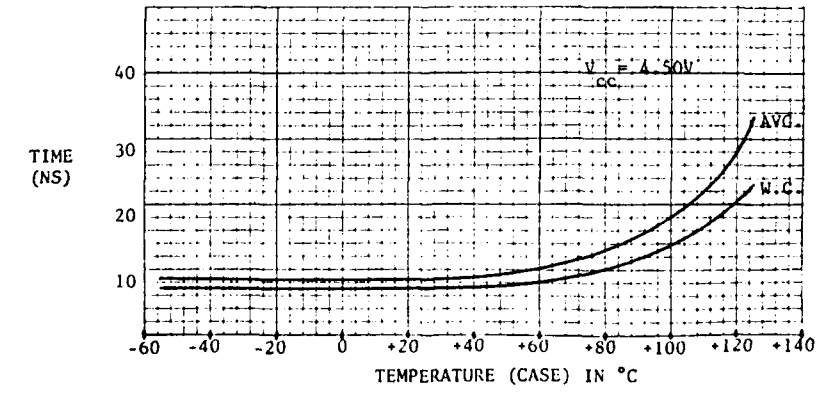
By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROES
VIHC 3.0V
VIH 3.0V
VIL 0.0V



AVERAGE T_{AZO} MIN.
VERSUS V_{cc}



VERSUS TEMPERATURE



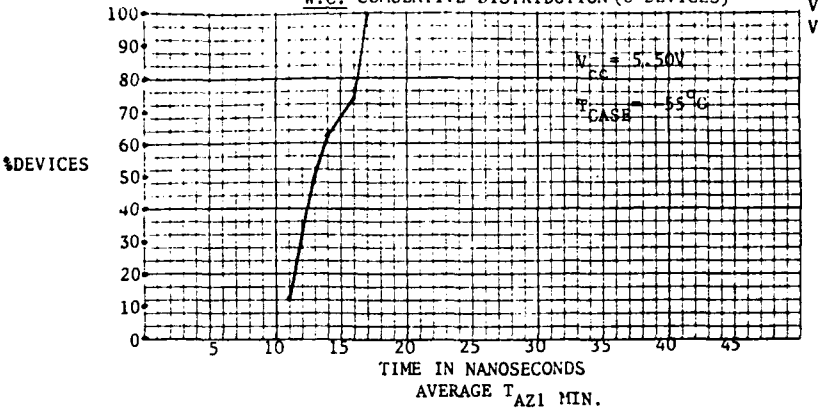
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM

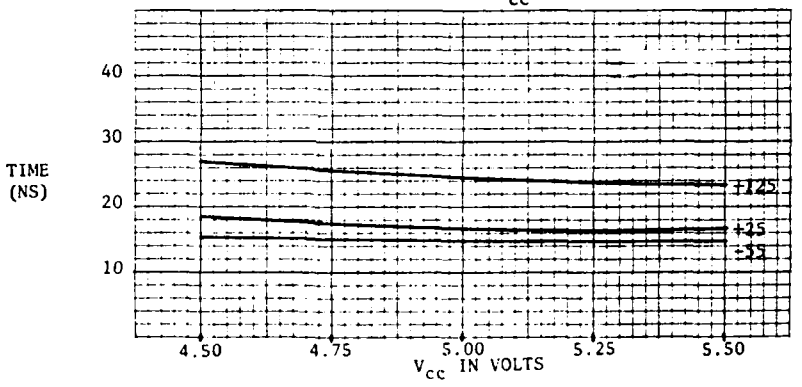
MINIMUM ADDRESS TO DATA-OFF TIME
FOR A LOGIC 1
T_{AZ1} MIN.

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

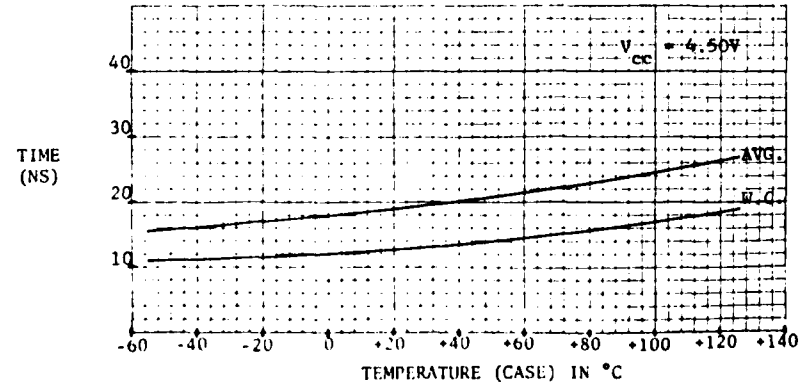
W.C. CUMULATIVE DISTRIBUTION (8 DEVICES)



VERSUS V_{cc}



VERSUS TEMPERATURE



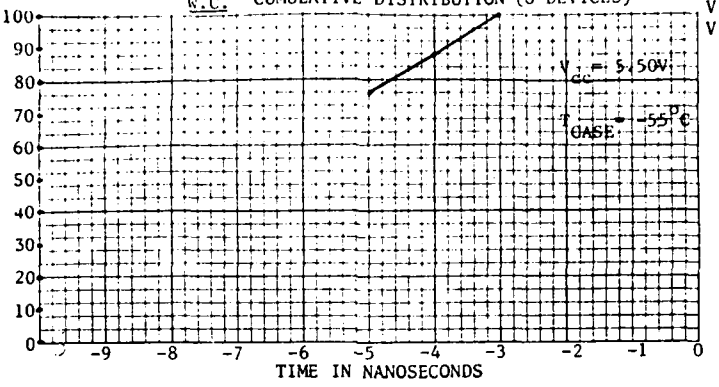
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
ADDRESS SETUP TIME BEFORE $\overline{CE}$

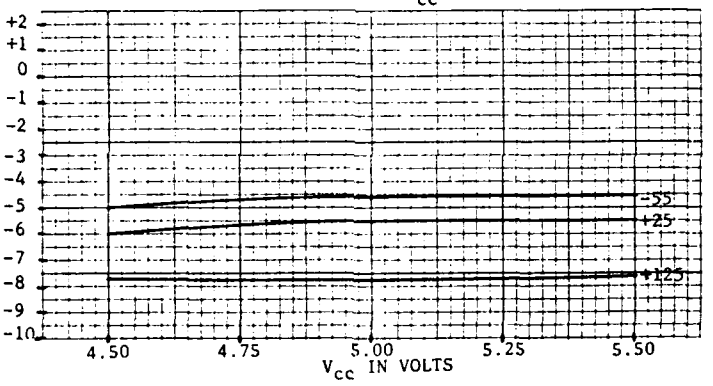
By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: MARCH1
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

T_{ASC}

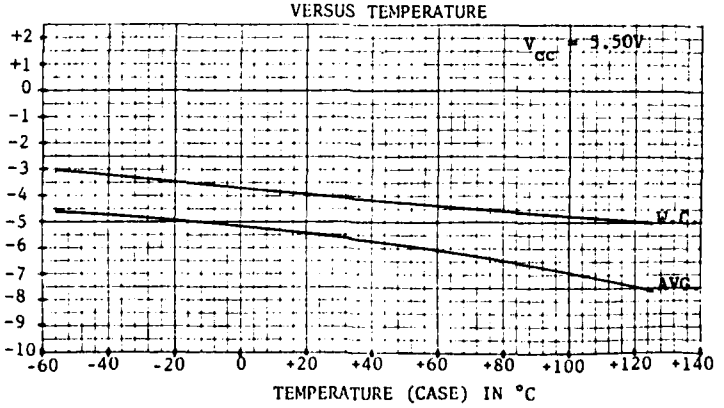
W.C. CUMULATIVE DISTRIBUTION (8 DEVICES)



AVERAGE T_{ASC}
VERSUS V_{cc}



VERSUS TEMPERATURE

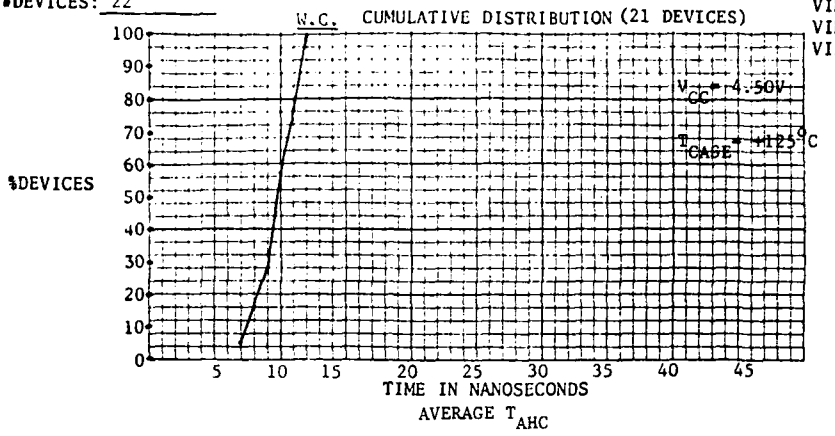


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

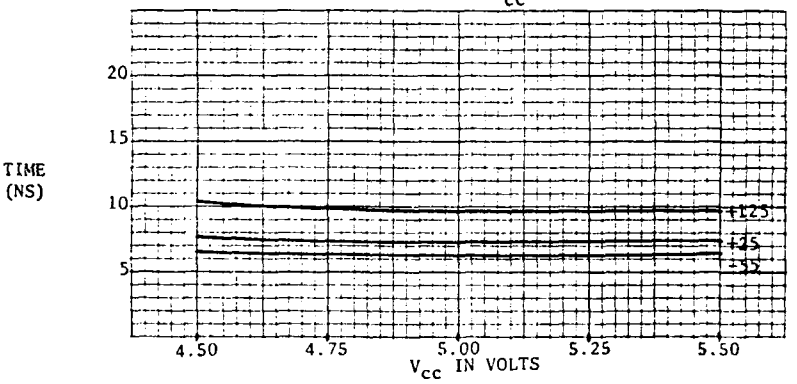
2KX8 STATIC RAM
ADDRESS HOLD TIME AFTER $\overline{CE}$

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: MARCH 1
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

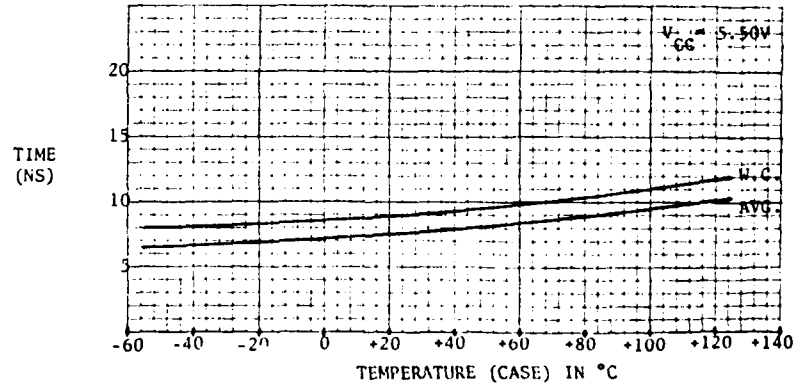
T_{AHC}



AVERAGE T_{AHC} VERSUS V_{CC}



VERSUS TEMPERATURE

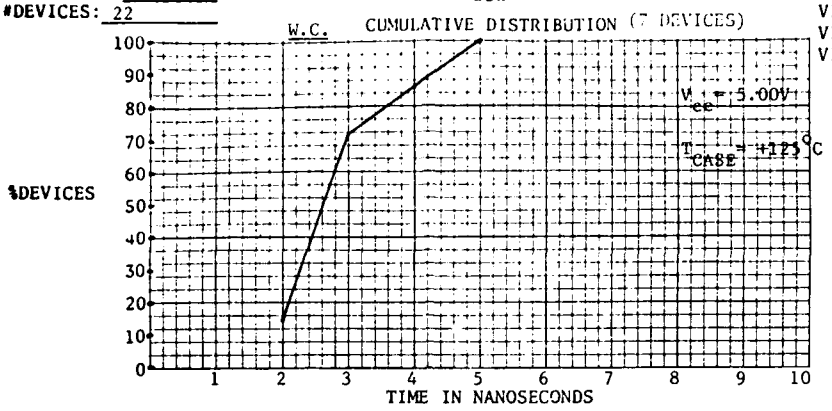


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

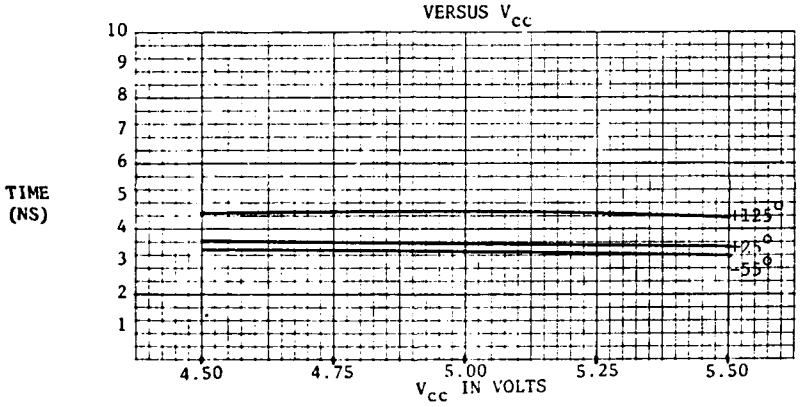
2KX8 STATIC RAM
DATA TO WRITE SETUP TIME

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: RCGAL
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

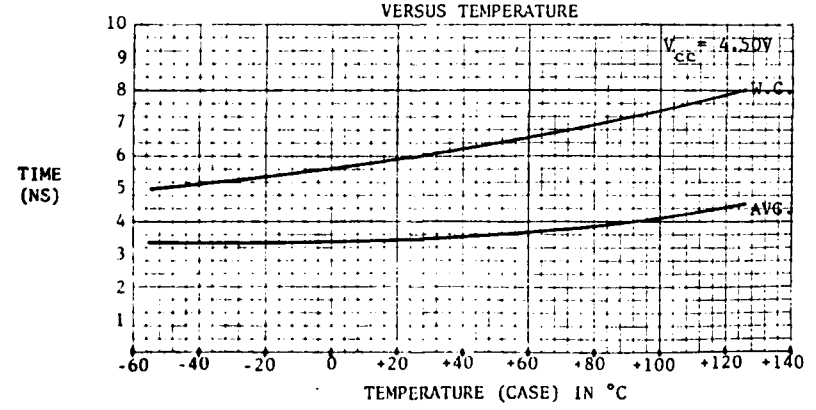
T_{DSW}



AVERAGE T_{DSW}
VERSUS V_{cc}



VERSUS TEMPERATURE



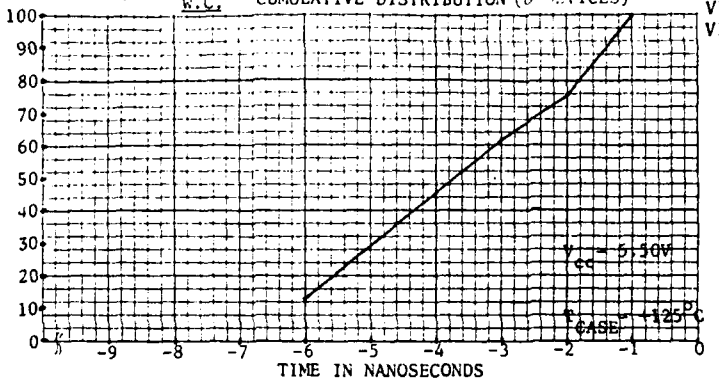
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
DATA HOLD TIME AFTER WRITE

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: MARCH1
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

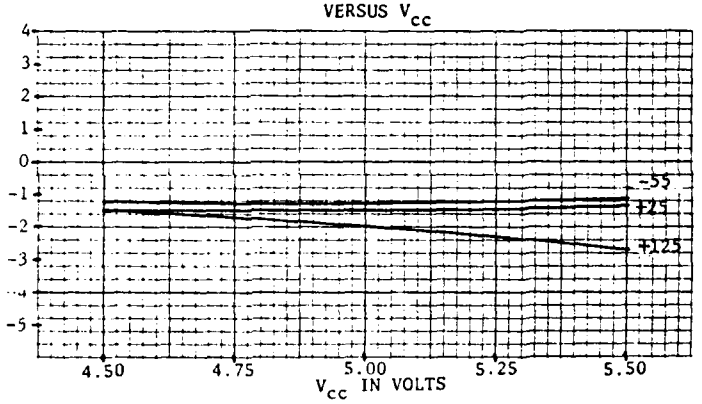
T_{DHW}

W.C. CUMULATIVE DISTRIBUTION (8 DEVICES)



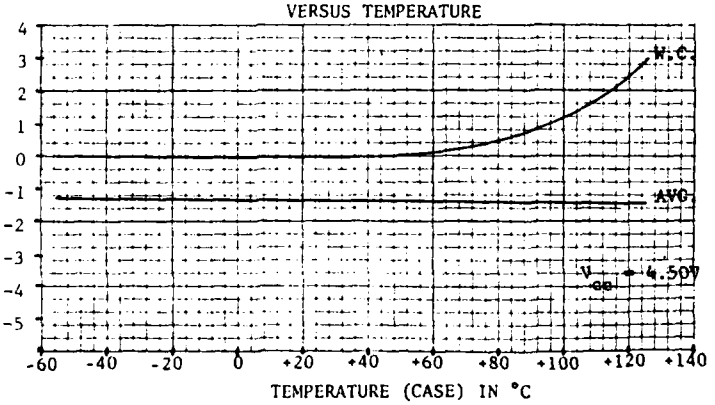
TIME IN NANOSECONDS

AVERAGE T_{DHW} VERSUS V_{cc}



V_{cc} IN VOLTS

VERSUS TEMPERATURE



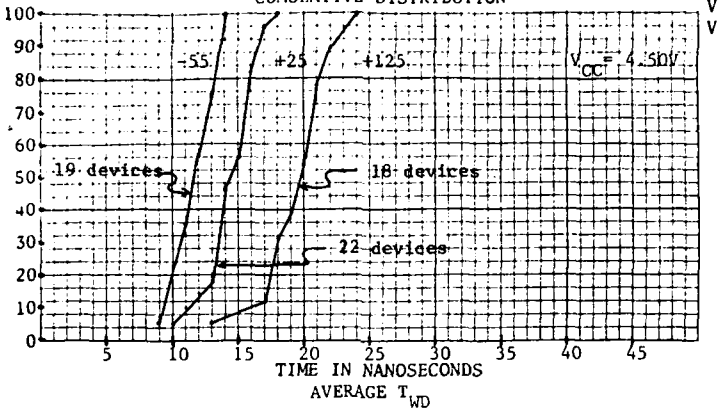
TEMPERATURE (CASE) IN °C

Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

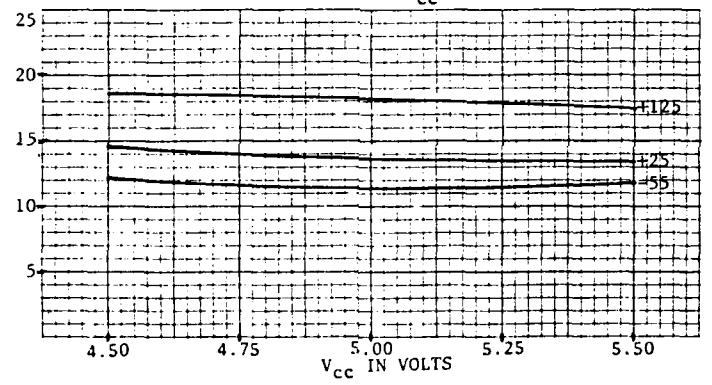
2 KX8 STATIC RAM
WRITE PULSE WIDTH

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: RCGAL
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

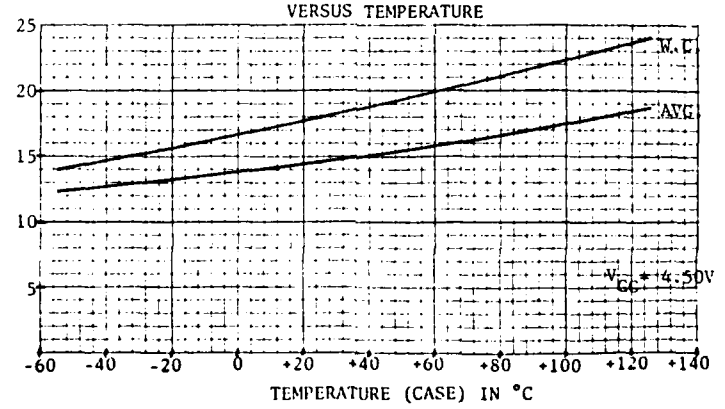
T_{WD}
CUMULATIVE DISTRIBUTION



AVERAGE T_{WD} VERSUS V_{cc}



VERSUS TEMPERATURE

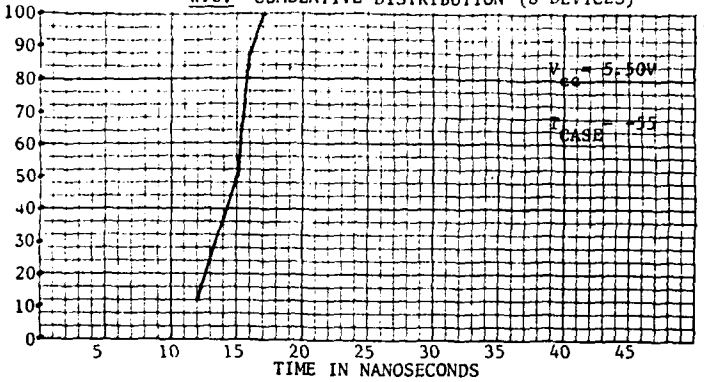


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

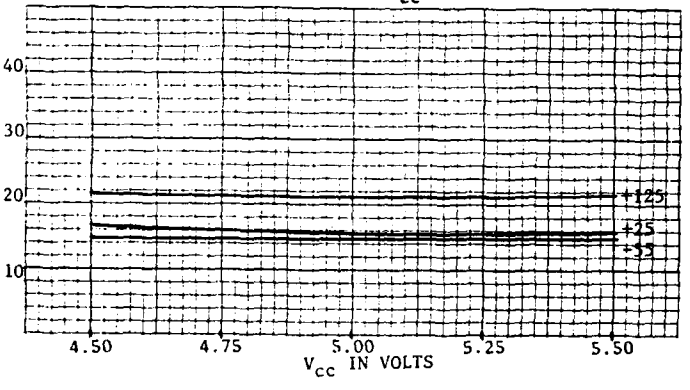
2KX8 STATIC RAM
MINIMUM WRITE ENABLE TO DATA OFF TIME FOR A LOGIC 0
T_{WEZO} MIN.

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

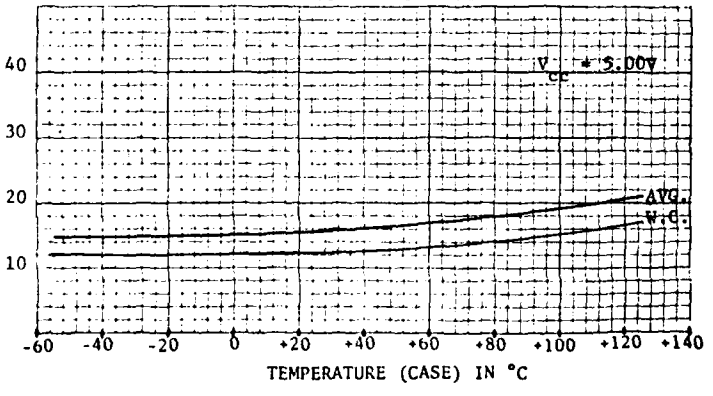
W.C. CUMULATIVE DISTRIBUTION (8 DEVICES)



AVERAGE T_{WEZO} MIN. VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

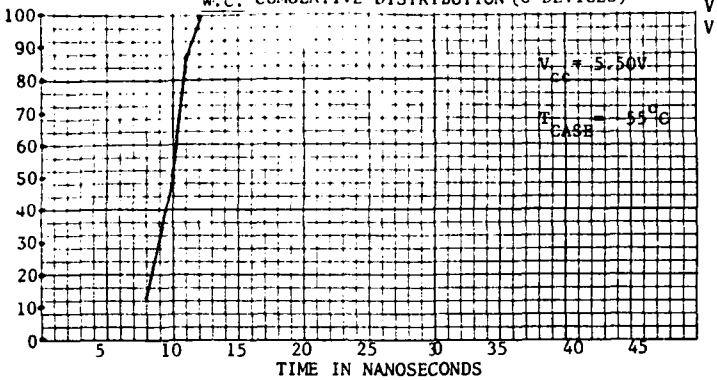
2KX8 STATIC RAM

MINIMUM WRITE ENABLE TO DATA OFF TIME FOR A LOGIC 1

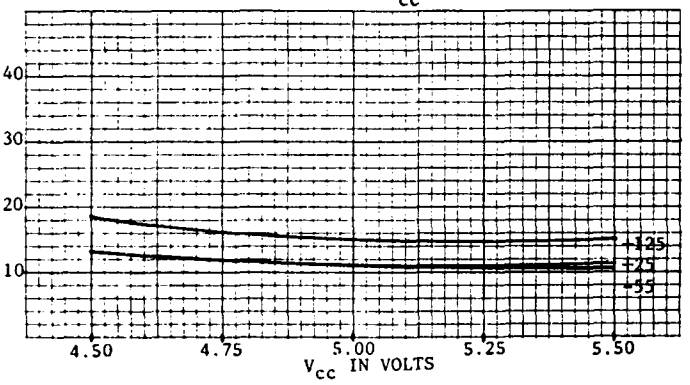
T_{WEZ1} MIN.

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

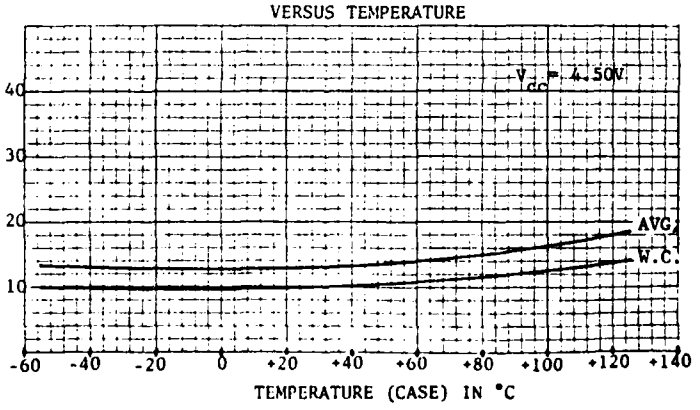
W.C. CUMULATIVE DISTRIBUTION (8 DEVICES)



AVERAGE T_{WEZ1} MIN. VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

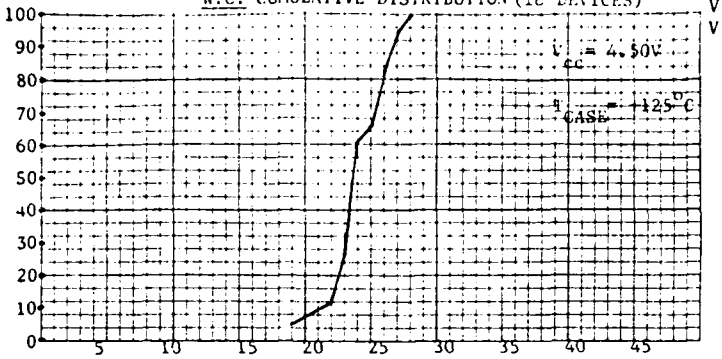
2KX8 STATIC RAM

MAXIMUM WRITE ENABLE TO DATA OFF TIME FOR A LOGIC 0

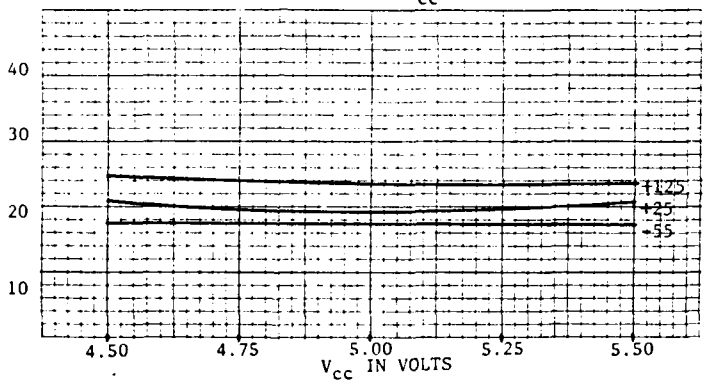
$T_{WEZO\ MAX.}$

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ZEROES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

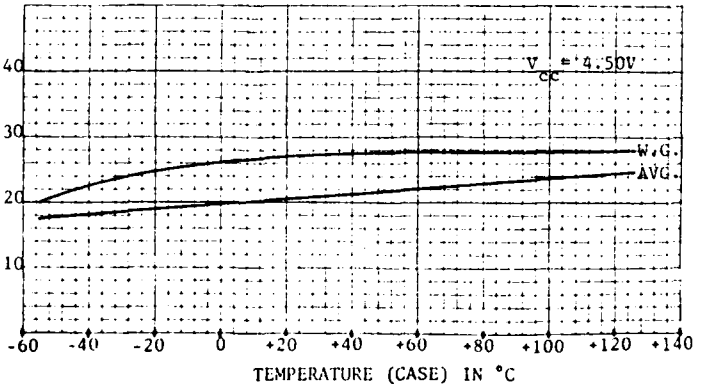
W.C. CUMULATIVE DISTRIBUTION (18 DEVICES)



AVERAGE $T_{WEZO\ MAX.}$ VERSUS V_{cc}



VERSUS TEMPERATURE

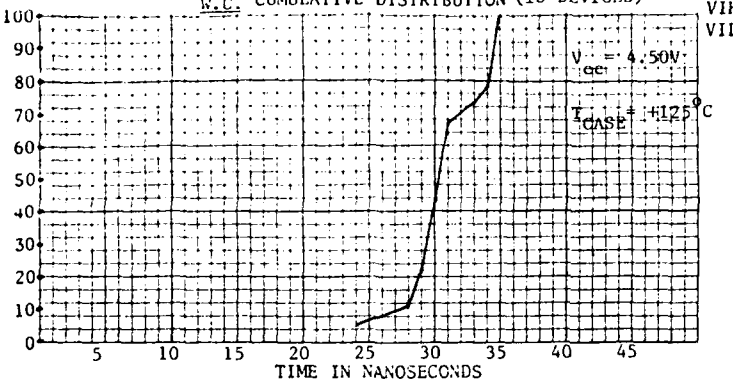


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

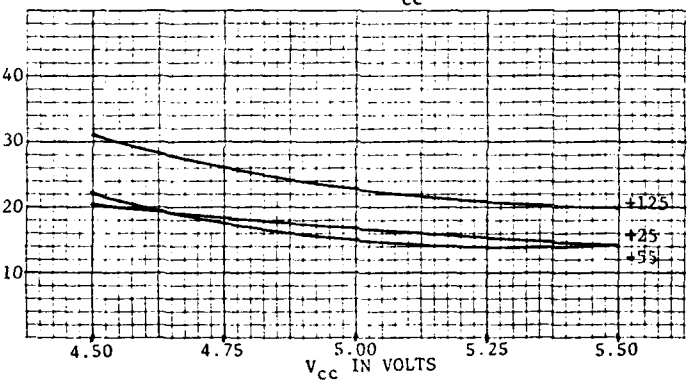
2KX8 STATIC RAM
MAXIMUM WRITE ENABLE TO DATA OFF
TIME FOR A LOGIC 1
T_{WEZ1} MAX.

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: SEQ. READ
DATA PAT: ALL ONES
VIHC 3.0V
VIH 3.0V
VIL 0.0V

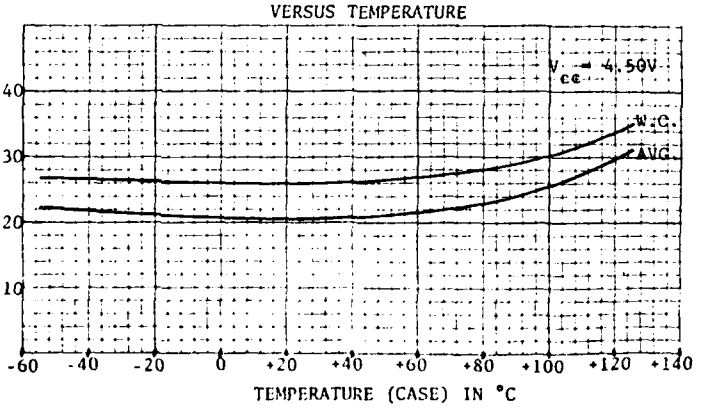
W.C. CUMULATIVE DISTRIBUTION (18 DEVICES)



AVERAGE T_{WEZ1} MAX.
VERSUS V_{cc}



VERSUS TEMPERATURE



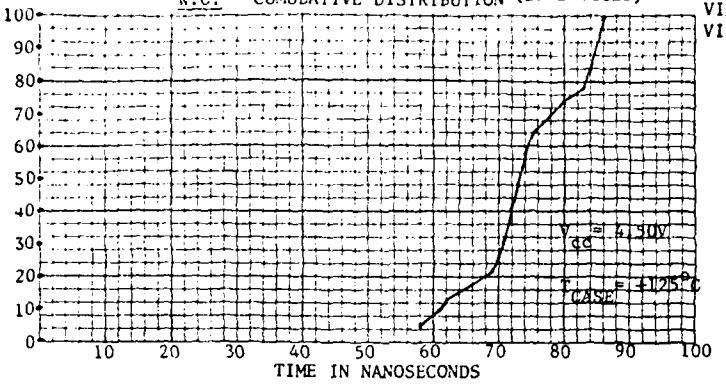
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
WRITE PULSE LEAD TIME

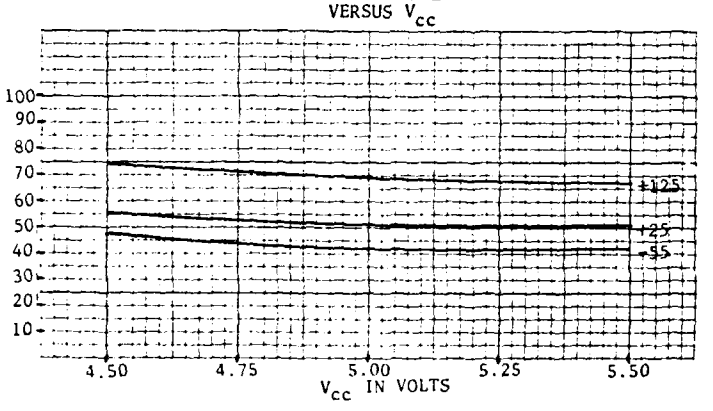
T_{WPL}

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: DUALWC
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

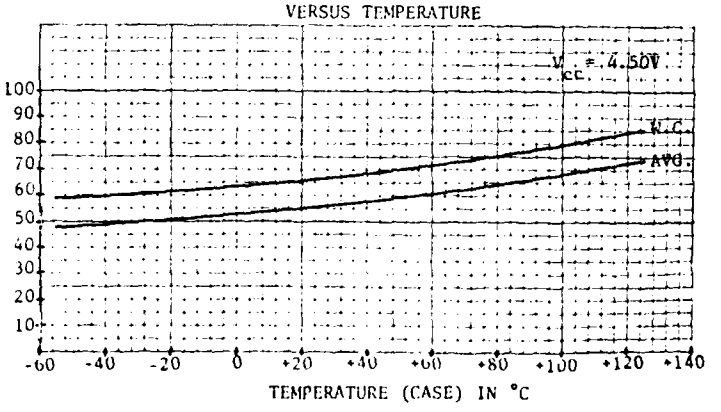
W.C. CUMULATIVE DISTRIBUTION (19 DEVICES)



AVERAGE T_{WPL}
VERSUS V_{cc}



VERSUS TEMPERATURE



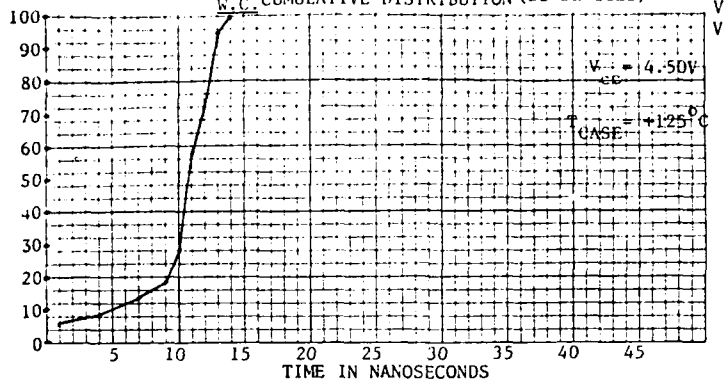
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
ADDRESS HOLD TIME AFTER $\overline{WE}$

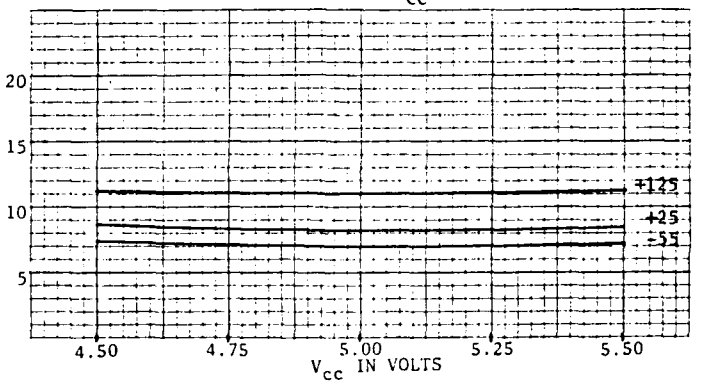
T_{AHW}

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: DUALWC
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

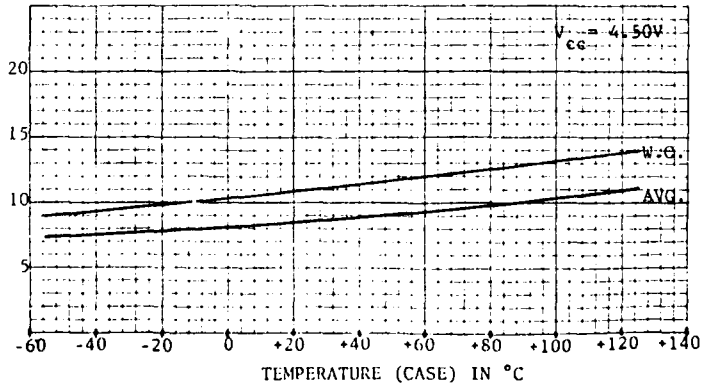
W.C. CUMULATIVE DISTRIBUTION (21 DEVICES)



AVERAGE T_{AHW}
VERSUS V_{cc}



VERSUS TEMPERATURE



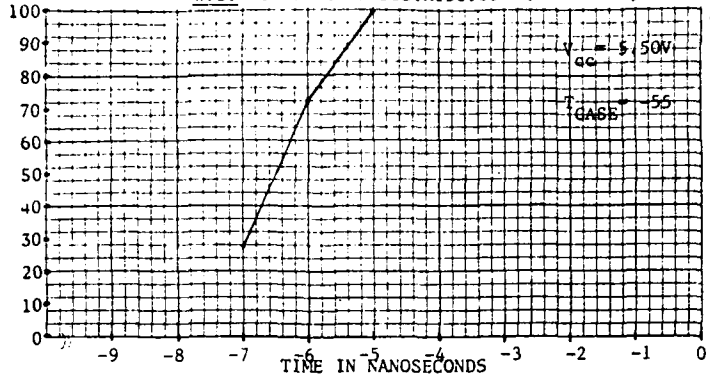
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
ADDRESS SETUP TIME BEFORE $\overline{WE}$

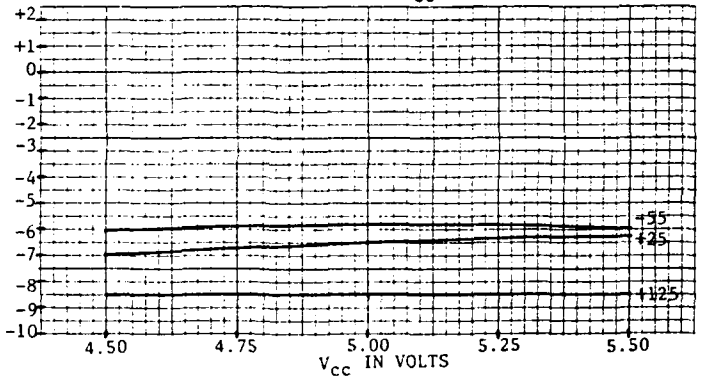
T_{ASW}

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: RCGAL
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

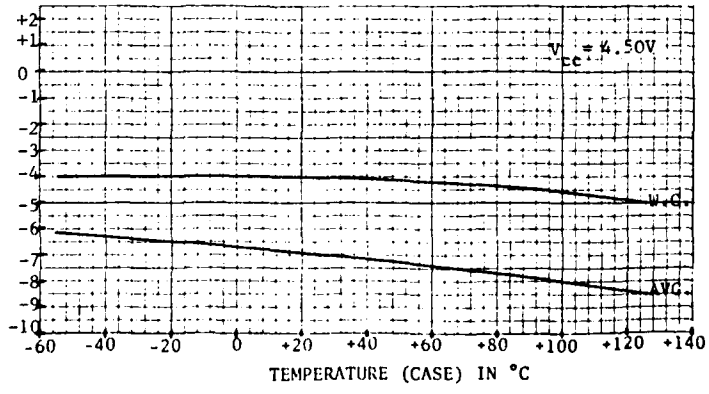
W.C. CUMULATIVE DISTRIBUTION (7 DEVICES)



AVERAGE T_{ASW}
VERSUS V_{cc}



VERSUS TEMPERATURE



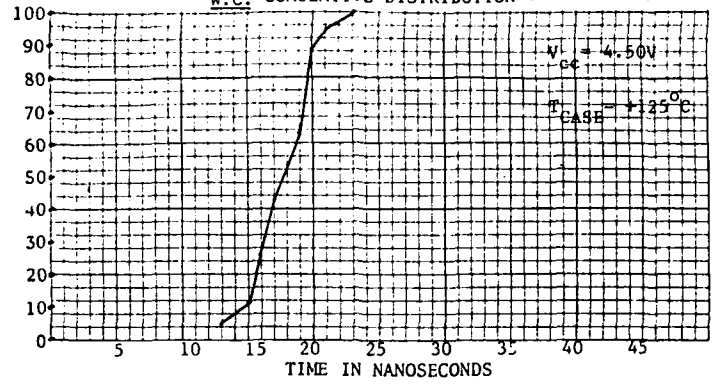
Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

2KX8 STATIC RAM
CHIP ENABLE TO WRITE SETUP TIME

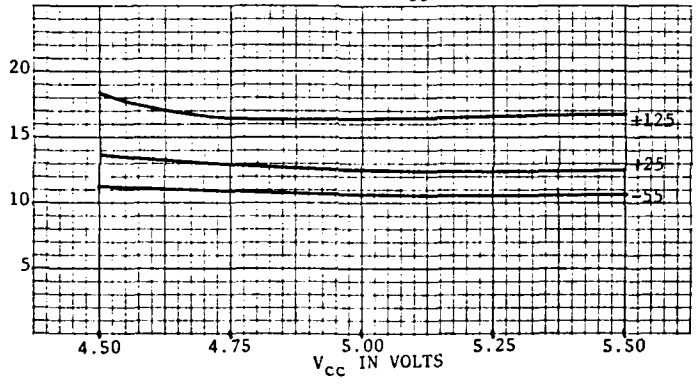
T_{CEW}

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: MARCH1
DATA PAT:
VIHC 3.0V
VIH 3.0V
VIL 0.0V

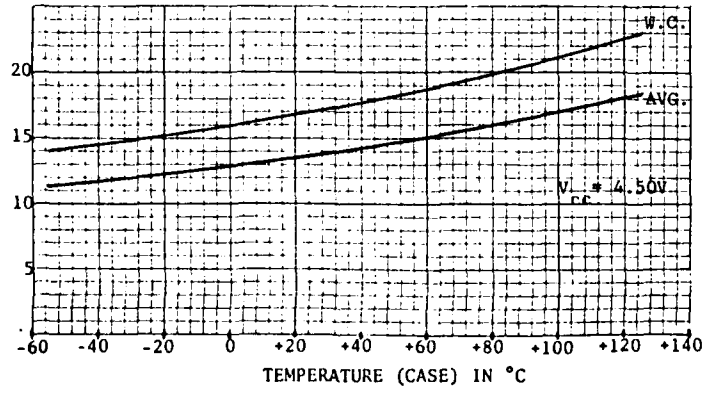
W.C. CUMULATIVE DISTRIBUTION (19 DEVICES)



AVERAGE T_{CEW}
VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N:MK4802P/-1/-3
REV: A
Date Codes:8022/33/31
#DEVICES: 22

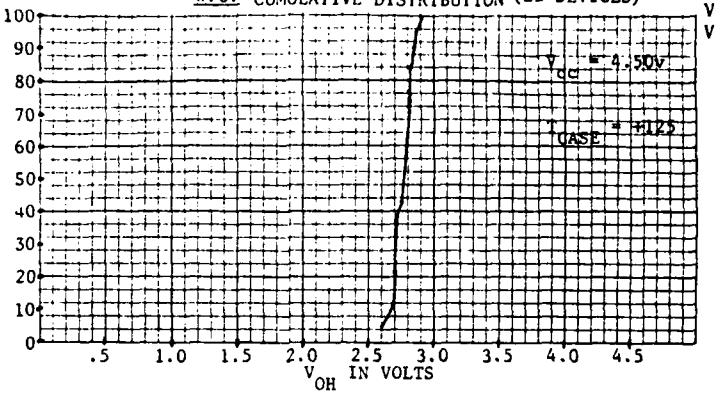
2KX8 STATIC RAM

OUTPUT HIGH VOLTAGE

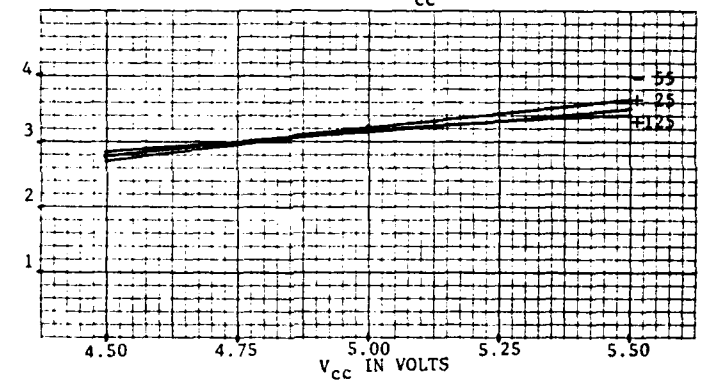
V_{OH}

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: HOLD XY
DATA PAT: ALL ONES
VIHC 3.0v
VIH 3.0V
VIL 0.0v

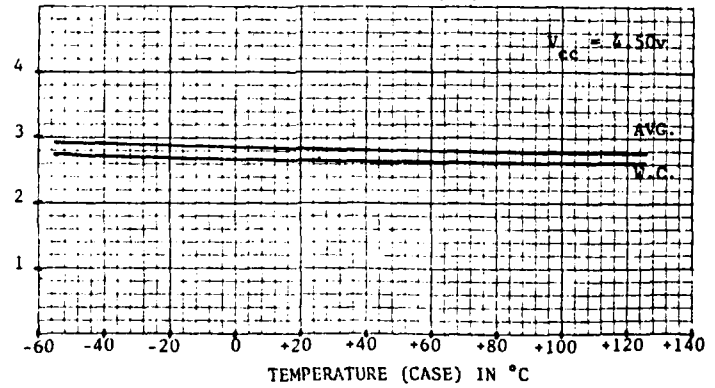
W.C. CUMULATIVE DISTRIBUTION (22 DEVICES)



AVERAGE V_{OH} VERSUS V_{cc}



VERSUS TEMPERATURE

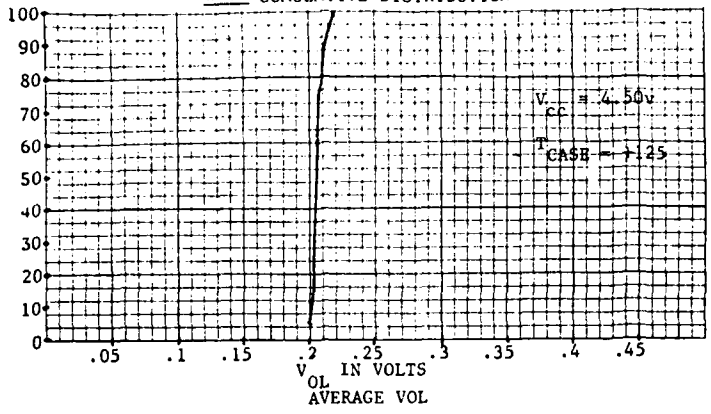


Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/31/33
#DEVICES: 22

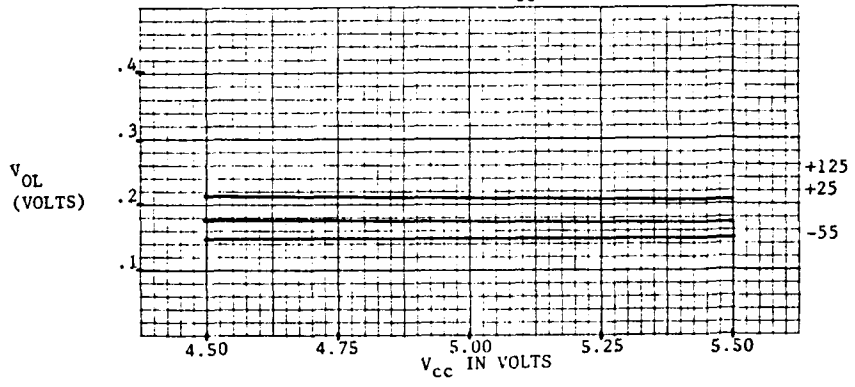
2 KX8 STATIC RAM
OUTPUT LOW VOLTAGE
VOL

By RM/AT Date 10/80
LOAD: Fig. 6
ADDR PAT: HOLD XY
DATA PAT: ALL ZEROES
VIHC 3.0v
VIH 3.0V
VIL 0.0v

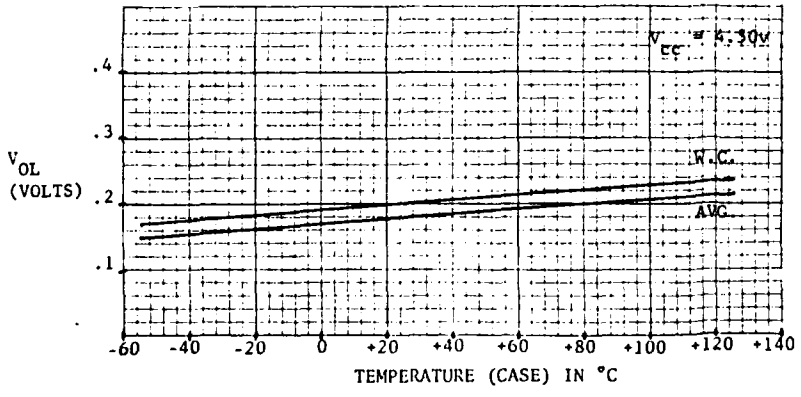
W.C. CUMULATIVE DISTRIBUTION (22 DEVICES)



AVERAGE VOL VERSUS V_{CC}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

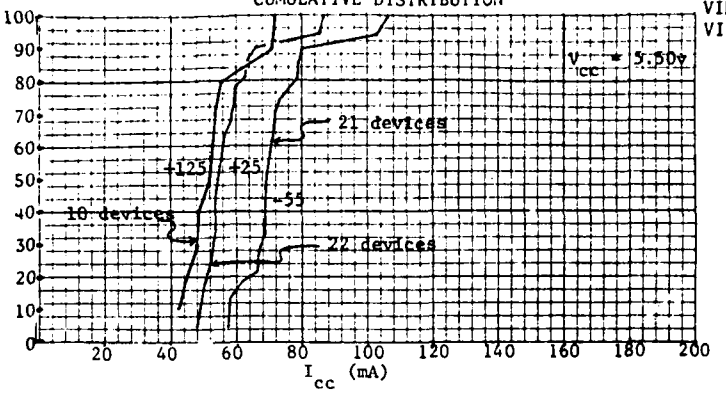
2KX8 STATIC RAM

SUPPLY CURRENT FROM V_{cc}, READ MODE

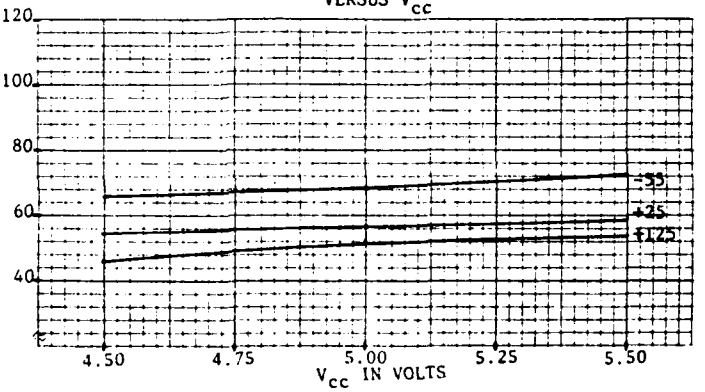
I_{cc_1}

By RM/AT Date 10/80
LOAD: NO LOAD
ADDR PAT: SEQ READ
DATA PAT: CHKBD
VIHC 3.0v
VIH 3.0V
VIL 0.0v

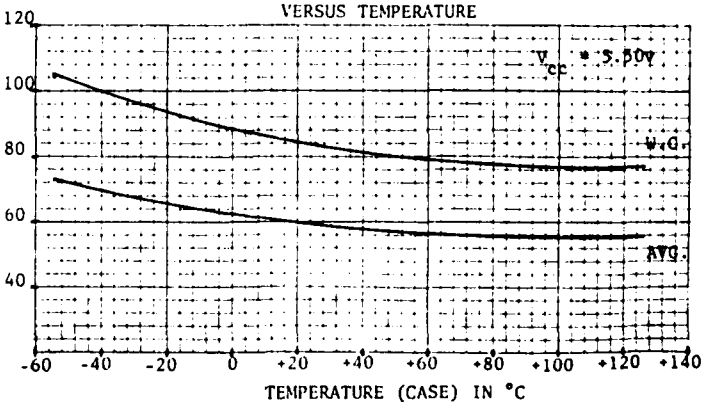
CUMULATIVE DISTRIBUTION



AVERAGE I_{cc_1} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

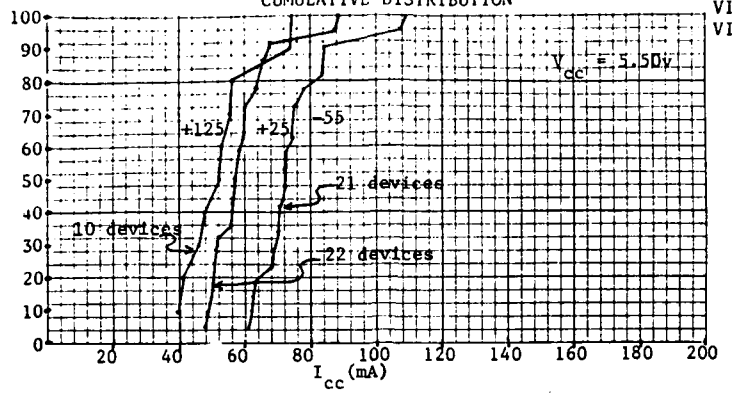
2KX8 STATIC RAM

SUPPLY CURRENT FROM V_{cc}, WRITE MODE

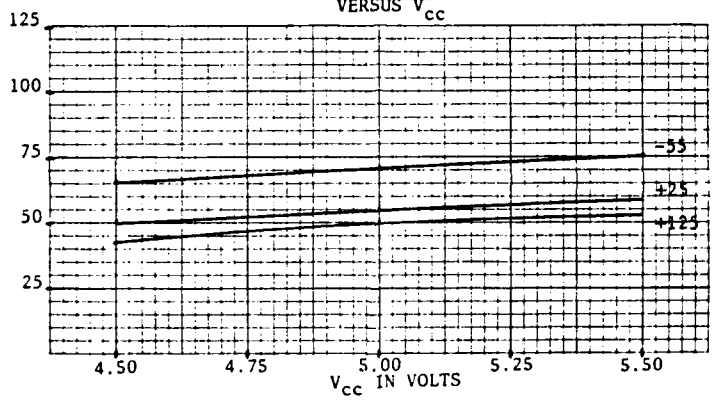
I_{cc_2}

By RM/AT Date 10/80
LOAD: NONE
ADDR PAT: SEQ WRITE
DATA PAT: CHKBD
VIHC 3.0v
VIH 3.0V
VIL 0.0v

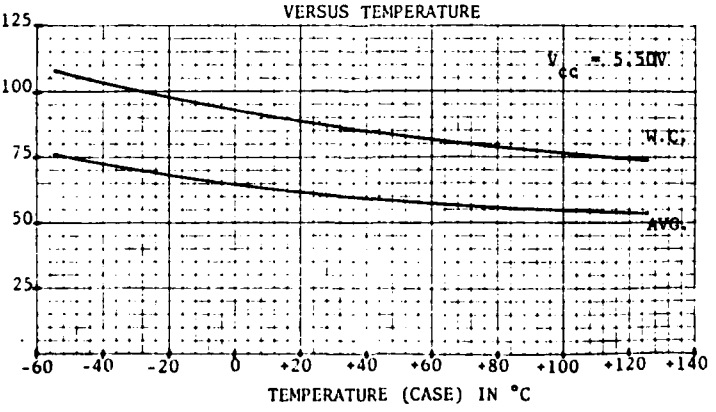
CUMULATIVE DISTRIBUTION



AVERAGE I_{cc_2} VERSUS V_{cc}



VERSUS TEMPERATURE



Vendor: Mostek
P/N: MK4802P/-1/-3
REV: A
Date Codes: 8022/33/31
#DEVICES: 22

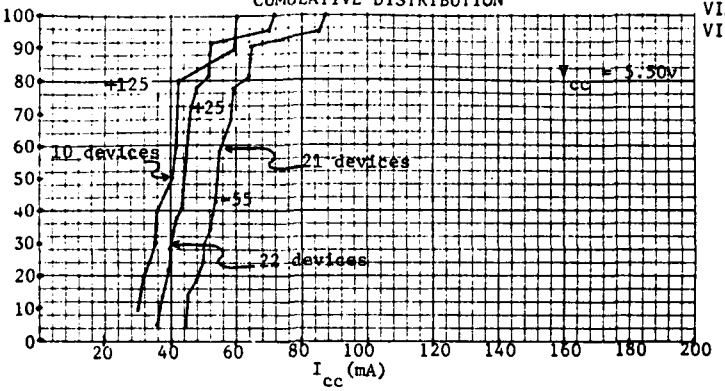
2KX8 STATIC RAM

SUPPLY CURRENT FROM V_{cc}, STANDBY MODE

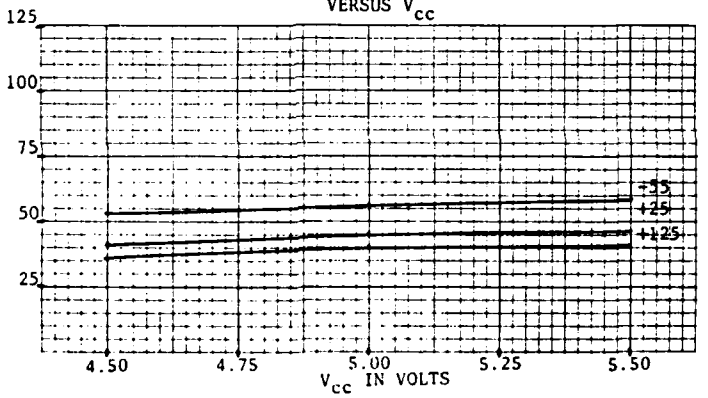
I_{cc_3}

By RM/AT Date 10/80
LOAD: NONE
ADDR PAT: HOLD XY
DATA PAT: ALL ZEROS
VIHC 3.0v
VIH 3.0v
VIL 0.0v

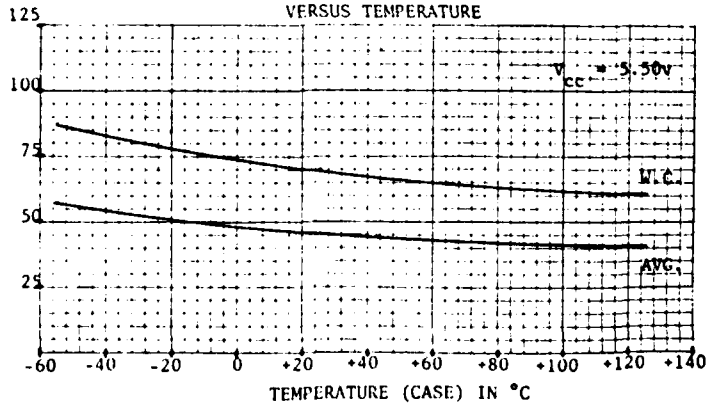
CUMULATIVE DISTRIBUTION



AVERAGE I_{cc_3} VERSUS V_{cc}



VERSUS TEMPERATURE



APPENDIX III

1KX8/2KX8 STATIC RAM

RECOMMENDED PARAMETER LIMITS

1KX8 RAM - Recommended parameter limits

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Output high voltage	V_{OH}	I_{OH} = -1.0 mA V_{CC} = 4.5 V	All	2.4		V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA V_{CC} = 4.5 V	All		0.4	V
Input leakage All inputs	$I_{I(L)(H)}$	V_{IN} = 0 to 5.5 V	All	-10	+10	uA
Output leakage	$I_{O(L)(H)}$	Outputs deselected V_{OUT} = 0.0 to 5.5 V	All	-10	+10	uA
Supply current from V_{CC}	I_{CC1} 1/ 2/	addresses cycling t_{RC} = min (read mode)	01 3/	-	130	mA
	I_{CC2} 1/	addresses cycling t_{wc} = min (write mode)	01 3/	-	140	mA
	I_{CC3}	address stable $\overline{WE}$ = V_{IH}, $\overline{OE}$ & $\overline{CE}$ = V_{IH}	01 3/	-	110	mA
Output short circuit current	I_{OS}	V_{CC} = 5.5V	All	-	160	mA
Pin capacitance (all pins except DQ)	C_I	V_{CC} = 5.0V	All	-	4	pf
Pin capacitance (DQ pins)	C_{DQ}	V_{CC} = 5.0V Outputs deselected	All	-	10	pf

1/ Depends on cycle rate. Limits are for cycle rates listed in conditions column.

2/ Depends on output load. Limits are for one Schottky TTL and 30 pF.

3/ Limits for other device types to be determined.

1KX8 RAM - Recommended parameter limits (Continued)

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Random read cycle time	t_{RC}	See fig. 6,7	01	90	-	NS
Random write cycle time	t_{WC}		01	90	-	NS
Address access time	t_{AA} 3/		01	-	90	NS
Chip enable access time	t_{CEA} 3/		01	-	45	NS
Chip enable data off time	t_{CEZ} 4/		01	5	30	NS
Output enable access time	t_{OEA} 3/		01	-	45	NS
Output enable data off time	t_{OEZ} 4/		01	5	30	NS
Address data off time	t_{AZ} 4/		01	5	-	NS
Address setup time before $\overline{CE}$	t_{ASC}		01	0	-	NS
Address hold time after $\overline{CE}$	t_{AHC}		01	30	-	NS
Data to write setup time	t_{DSW}		01	5	-	NS
Data hold time after write	t_{DHW}		01	10	-	NS
Write pulse duration	t_{WD}		01	40	-	NS
Write enable data off time	t_{WEZ} 4/		01	5	25	NS
Write pulse lead time	t_{WPL}		01	60	-	NS
Address hold time after $\overline{WE}$	t_{AHW}		01	30	-	NS
Address setup time before $\overline{WE}$	t_{ASW}		01	0	-	NS
Chip enable to write setup time	t_{CEW}	↓	01	40	-	NS

3/ Load = One Schottky TTL + 30 pF or equivalent

4/ Disable times are measured from V_{OH} to V_{OH}-75mV, or from V_{OL} to V_{OL}+75mV

1KX8 RAM - Recommended parameter limits (Continued)

Characteristics	Symbol	Conditions	Device type	Limits		Units
				Min	Max	
Random read cycle time	t_{RC}	See fig. 6,7	02	70	-	NS
Random write cycle time	t_{WC}		02	70	-	NS
Address access time	t_{AA} 3/		02	-	70	NS
Chip enable access time	t_{CEA} 3/		02	-	35	NS
Chip enable data off time	t_{CEZ} 4/		02	5	20	NS
Output enable access time	t_{OEA} 3/		02	-	35	NS
Output enable data off time	t_{OEZ} 4/		02	5	20	NS
Address data off time	t_{AZ} 4/		02	5	-	NS
Address setup time before $\overline{CE}$	t_{ASC}		02	0	-	NS
Address hold time after $\overline{CE}$	t_{AHC}		02	20	-	NS
Data to write setup time	t_{DSW}		02	5	-	NS
Data hold time after write	t_{DHW}		02	10	-	NS
Write pulse duration	t_{WD}		02	25	-	NS
Write enable data off time	t_{WEZ} 4/		02	5	15	NS
Write pulse lead time	t_{WPL}		02	45	-	NS
Address hold time after $\overline{WE}$	t_{AHW}		02	20	-	NS
Address setup time before $\overline{WE}$	t_{ASW}		02	0	-	NS
Chip enable to write setup time	t_{CEW}		02	25	-	NS

3/ Load = One Schottky TTL + 30 pF or equivalent

4/ Disable times are measured from V_{OH} to V_{OH}-75mV, or from V_{OL} to V_{OL}+75mV

1KX8 RAM - Recommended parameter limits (Continued)

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Random read cycle time	t_{RC}	See fig. 6,7	03	55	-	NS
Random write cycle time	t_{WC}		03	55	-	NS
Address access time	t_{AA} 3/		03	-	55	NS
Chip enable access time	t_{CEA} 3/		03	-	25	NS
Chip enable data off time	t_{CEZ}		03	5	15	NS
Output enable access time	t_{OEA} 3/		03	-	25	NS
Output enable data off time	t_{OEZ} 4/		03	5	15	NS
Address data off time	t_{AZ} 4/		03	5	-	NS
Address setup time before $\overline{CE}$	t_{ASC}		03	0	-	NS
Address hold time after $\overline{CE}$	t_{AHC}		03	15	-	NS
Data to write setup time	t_{DSW}		03	5	-	NS
Data hold time after write	t_{DHW}		03	10	-	NS
Write pulse duration	t_{WD}		03	20	-	NS
Write enable data off time	t_{WEZ} 4/		03	5	10	NS
Write pulse lead time	t_{WPL}		03	35	-	NS
Address hold time after $\overline{WE}$	t_{AHW}		03	15	-	NS
Address setup time before $\overline{WE}$	t_{ASW}		03	0	-	NS
Chip enable to write setup time	t_{CEW}	↓	03	20	-	NS

3/ Load = One Schottky TTL + 30 pF or equivalent

4/ Disable times are measured from V_{OH} to V_{OH}-75mV, or from V_{OL} to V_{OL}+75mV

2KX8 RAM - Recommended parameter limits

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Output high voltage	V_{OH}	I_{OH} = -1.0 mA V_{CC} = 4.5 V	All	2.4		V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA V_{CC} = 4.5 V	All		0.4	V
Input leakage All inputs	$I_{I(L)(H)}$	V_{IN} = 0 to 7.0 V	All	-10	+10	uA
Output leakage	$I_{O(L)(H)}$	Outputs deselected V_{OUT} = 0.0 to 7.0 V	All	-10	+10	uA
Supply current from V_{CC}	I_{CC1} 1/ 2/	addresses cycling t_{RC} = min (read mode)	01 3/	-	130	mA
	I_{CC2} 1/	addresses cycling t_{wc} = min (write mode)	01 3/	-	140	mA
	I_{CC3}	address stable = V_{IH} $\overline{WE}$ = V_{IH}, $\overline{OE}$ & $\overline{CE}$	01 3/	-	110	mA
Output short circuit current	I_{OS}	V_{CC} = 5.5V	All	-	160	mA
Pin capacitance (all pins except DQ)	C_I	V_{CC} = 5.5V	All	-	4	pf
Pin capacitance (DQ pins)	C_{DQ}	V_{CC} = 5.0V Outputs deselected	All	-	10	pf

1/ Depends on cycle rate. Limits are for cycle rates listed in conditions column.

2/ Depends on output load. Limits are for one Schottky TTL and 30 pF.

3/ Limits for other device types to be determined.

AD-A096 307 IBM FEDERAL SYSTEMS DIV MANASSAS VA F/6 9/2
ELECTRICAL CHARACTERIZATION OF COMPLEX MEMORIES - BYTE WIDE STA--ETC(U)
JAN 81 A H TABER, R A MOYERS F30602-79-C-0162
UNCLASSIFIED RADC-TR-80-401-PT-1 NL

2 OF 2
AD A096307

END
DATE FILMED
4-81
DTIC

2KX8 RAM - Recommended parameter limits (Continued)

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Random read cycle time	t_{RC}	See fig. 6,7	01	200	-	NS
Random write cycle time	t_{WC}		01	200	-	NS
Address access time	t_{AA} 3/		01	-	200	NS
Chip enable access time	t_{CEA} 3/		01	-	100	NS
Chip enable data off time	t_{CEZ} 4/		01	5	35	NS
Output enable access time	t_{OEA} 3/		01	-	100	NS
Output enable data off time	t_{OEZ} 4/		01	5	35	NS
Address data off time	t_{AZ} 4/		01	5	-	NS
Address setup time before $\overline{CE}$	t_{ASC}		01	0	-	NS
Address hold time after $\overline{CE}$	t_{AHC}		01	65	-	NS
Data to write setup time	t_{DSW}		01	20	-	NS
Data hold time after write	t_{DHW}		01	10	-	NS
Write pulse duration	t_{WD}		01	60	-	NS
Write enable data off time	t_{WEZ} 4/		01	5	35	NS
Write pulse lead time	t_{WPL}		01	130	-	NS
Address hold time after $\overline{WE}$	t_{AHW}		01	65	-	NS
Address setup time before $\overline{WE}$	t_{ASW}		01	0	-	NS
Chip enable to write setup time	t_{CEW}	↓	01	60	-	NS

3/ Load = One Schottky TTL + 30 pF or equivalent

4/ Disable times are measured from V_{OH} to V_{OH}-75mV, or from V_{OL} to V_{OL}+75mV

2KX8 RAM - Recommended parameter limits (Continued)

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Random read cycle time	t_{RC}	See fig. 6,7	02	120	-	NS
Random write cycle time	t_{WC}		02	120	-	NS
Address access time	t_{AA} 3/		02	-	120	NS
Chip enable access time	t_{CEA} 3/		02	-	60	NS
Chip enable data off time	t_{CEZ} 4/		02	5	30	NS
Output enable access time	t_{OEA} 3/		02	-	60	NS
Output enable data off time	t_{OEZ} 4/		02	5	30	NS
Address data off time	t_{AZ} 4/		02	5	-	NS
Address setup time before $\overline{CE}$	t_{ASC}		02	0	-	NS
Address hold time after $\overline{CE}$	t_{AHC}		02	40	-	NS
Data to write setup time	t_{DSW}		02	10	-	NS
Data hold time after write	t_{DHW}		02	10	-	NS
Write pulse duration	t_{WD}		02	45	-	NS
Write enable data off time	t_{WEZ} 4/		02	5	30	NS
Write pulse lead time	t_{WPL}		02	65	-	NS
Address hold time after $\overline{WE}$	t_{AHW}		02	40	-	NS
Address setup time before $\overline{WE}$	t_{ASW}		02	0	-	NS
Chip enable to write setup time	t_{CEW}	↓	02	45	-	NS

3/ Load = One Schottky TTL + 30 pF or equivalent

4/ Disable times are measured from V_{OH} to V_{OH}-75mV, or from V_{OL} to V_{OL}+75mV

2KX8 RAM - Recommended parameter limits (Continued)

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Random read cycle time	t_{RC}	See fig. 6,7	03	90	-	NS
Random write cycle time	t_{WC}		03	90	-	NS
Address access time	t_{AA} 3/		03	-	90	NS
Chip enable access time	t_{CEA} 3/		03	-	45	NS
Chip enable data off time	t_{CEZ} 4/		03	5	25	NS
Output enable access time	t_{OEA} 3/		03	-	45	NS
Output enable data off time	t_{OEZ} 4/		03	5	25	NS
Address data off time	t_{AZ}		03	5	-	NS
Address setup time before $\overline{CE}$	t_{ASC}		03	0	-	NS
Address hold time after $\overline{CE}$	t_{AHC}		03	30	-	NS
Data to write setup time	t_{DSW}		03	10	-	NS
Data hold time after write	t_{DHW}		03	10	-	NS
Write pulse duration	t_{WD}		03	30	-	NS
Write enable data off time	t_{WEZ} 4/		03	5	25	NS
Write pulse lead time	t_{WPL}		03	60	-	NS
Address hold time after $\overline{WE}$	t_{AHW}		03	30	-	NS
Address setup time before $\overline{WE}$	t_{ASW}		03	0	-	NS
Chip enable to write setup time	t_{CEW}	↓	03	30	-	NS

3/ Load = One Schottky TTL + 30 pF or equivalent

4/ Disable times are measured from V_{OH} to V_{OH}-75mV, or from V_{OL} to V_{OL}+75mV

2KX8 RAM - Recommended parameter limits (Continued)

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Random read cycle time	t_{RC}	See fig. 6,7	04	70	-	NS
Random write cycle time	t_{WC}		04	70	-	NS
Address access time	t_{AA} 3/		04	-	70	NS
Chip enable access time	t_{CEA} 3/		04	-	35	NS
Chip enable data off time	t_{CEZ} 4/		04		20	NS
Output enable access time	t_{OEA} 3/		04	-	35	NS
Output enable data off time	t_{OEZ} 4/		04		20	NS
Address data off time	t_{AZ} 4/		04	5	-	NS
Address setup time before $\overline{CE}$	t_{ASC}		04	0	-	NS
Address hold time after $\overline{CE}$	t_{AHC}		04	25	-	NS
Data to write setup time	t_{DSW}		04	10	-	NS
Data hold time after write	t_{DHW}		04	10	-	NS
Write pulse duration	t_{WD}		04	25	-	NS
Write enable data off time	t_{WEZ} 4/		04	5	20	NS
Write pulse lead time	t_{WPL}		04	45	-	NS
Address hold time after $\overline{WE}$	t_{AHW}		04	25	-	NS
Address setup time before $\overline{WE}$	t_{ASW}		04	0	-	NS
Chip enable to write setup time	t_{CEW}	↓	04	25	-	NS

3/ Load = One Schottky TTL + 30 pF or equivalent

4/ Disable times are measured from V_{OH} to V_{OH}-75mV, or from V_{OL} to V_{OL}+75mV

2KX8 RAM - Recommended parameter limits (Continued)

Characteristics	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Random read cycle time	t_{RC}	See fig. 2,3	05	55	-	NS
Random write cycle time	t_{WC}		05	55	-	NS
Address access time	t_{AA} 3/		05	-	55	NS
Chip enable access time	t_{CEA} 3/		05	-	30	NS
Chip enable data off time	t_{CEZ} 4/		05	5	15	NS
Output enable access time	t_{OEA} 3/		05	-	30	NS
Output enable data off time	t_{OEZ} 4/		05		15	NS
Address data off time	t_{AZ} 4/		05	5	-	NS
Address setup time before $\overline{CE}$	t_{ASC}		05	0	-	NS
Address hold time after $\overline{CE}$	t_{AHC}		05	20	-	NS
Data to write setup time	t_{DSW}		05	5	-	NS
Data hold time after write	t_{DHW}		05	5	-	NS
Write pulse duration	t_{WD}		05	20	-	NS
Write enable data off time	t_{WEZ} 4/		05	5	15	NS
Write pulse lead time	t_{WPL}		05	35	-	NS
Address hold time after $\overline{WE}$	t_{AHW}		05	20	-	NS
Address setup time before $\overline{WE}$	t_{ASW}		05	0	-	NS
Chip enable to write setup time	t_{CEW}	↓	05	20	-	NS

3/ Load = One Schottky TTL + 30 pF or equivalent

4/ Disable times are measured from V_{OH} TO V_{OH}-75mV, or from V_{OL} to V_{OL}+75mV

APPENDIX IV

1KX8/2KX8 STATIC RAM

TEST ALGORITHMS

8K/16K STATIC RAM

PATTERN 1

ROW/COLUMN GALLOPING PATTERN (RCGAL)

RCGAL is an address pattern sensitivity test resembling the industry standard, GALPAT. Test time is shorter, though, because RCGAL only reads background bits in the same row and column as the test bit, rather than going through the entire array. RCGAL is performed in the following manner:

Step 1 - Write background data
Step 2 - Write complement data at location 0 (test bit)
Step 3 - Perform a series of reads, alternating between the test bit and each bit in the test bit row (X axis)
Step 4 - Perform a series of reads, alternating between the test bit and each bit in the test bit column (Y axis)
Step 5 - Restore the test bit and repeat with a new test bit until each bit in the array has been tested
Step 6 - Repeat steps 1 through 5 with complement data

Test time = $2N(2R + 2C-1)$ cycles

Where: R = # of rows
C = # of columns
N = # of bits (RC)

PATTERN 2

SLIDING DIAGONAL PATTERN (SLDIAG)

SLDIAG is a diagonal addressing pattern sensitivity test using a sequential reading scheme starting at address cell location zero. A test diagonal of complement data is first written into the array against background data and then diagonally read beginning after the test diagonal and wrapping around until the test diagonal is verified. The test diagonal is then restored and the next adjacent diagonal becomes the test diagonal. This procedure is repeated until all diagonals have been exercised as the test diagonal and again for complement data.

Step 1 - Write background data
Step 2 - Read background data
Step 3 - Write a test diagonal of complement data from address cell location XYMIN to XYMAX
Step 4 - Diagonally read the array from the test diagonal +1 looping around the array until the test diagonal has been verified
Step 5 - Restore the test diagonal to background data and write the next test diagonal beginning at address cell location +1.
Step 6 - Repeat steps 4 through 5 until all diagonals have been exercised as the test diagonal.
Step 7 - Repeat steps 1 through 6 with complement data

Test Time = 2NC + 8N + 2R cycles

PATTERN 3

ADDRESS COMPLEMENT (ADCOMP)

ADCOMP is used to test address decoders by reading an address location after writing the complement address location. ADCOMP produces maximum address line noise while testing decoder dynamic response time. The pattern is performed in the following manner:

Step 1 - Write background data
Step 2 - Read minimum address location for background data
Step 3 - Write minimum address location with $\overline{\text{background}}$ data
Step 4 - Read maximum address location for background data
Step 5 - Write maximum address location with $\overline{\text{background}}$ data
Step 6 - Continue steps 2 through 5 incrementing and decrementing from minimum and maximum locations until all locations have been read and written with $\overline{\text{background}}$ data
Step 7 - Repeat steps 2 through 6

Test time = 6N cycles

PATTERN 4

MARCHING PATTERN (MARCH 1)

March 1 is used to test for address uniqueness and multiple selection. March 1 first writes the array with background data, then reads address location zero for data and writes complement data at this same address location. The pattern then reads the previously written cell location for complement data, increments the address location and repeats this procedure until the maximum address location is reached. The entire test is then performed again using complement data as the background data. March 1 is performed in the following manner:

PATTERN 4 (CONT)

MARCHING PATTERN (MARCH 1)

Step 1 - Write background data
Step 2 - Read address location zero for data
Step 3 - Write address location zero with complement data
Step 4 - Read address location zero for complement data
Step 5 - Repeat steps 2 through 4 for each address location (sequentially)
Step 6 - Repeat steps 1 through 5 with complement background data

Test time = 14N cycles

PATTERN 5

DUAL WALKING COLUMNS (DUALWC)

DUALWC is used to test for multiple selection and address uniqueness. This pattern reads the array as two colums of complement data are walked through background data. DUALWC is performed in the following manner:

Step 1 - Write background data
Step 2 - Write complement data along the test columns Y_{min} and $1/2Y_{max}$
Step 3 - Sequentially read the array for valid data
Step 4 - Restore the test columns to background data
Step 5 - Continue steps 2 through 4, incrementing the test columns until all columns have been exercised as the test column.

Test time = $N(3 + \frac{C}{2})$ cycles

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.