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INVESTIGATION AND DESIGN OF ELECTRONIC CIRCUITRY RELATED TO NOI--ETC(U)

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I Electronic Circuitry for Measurement of Charge Decay

1.0 Introduction

The investigation requiring the circuitry of this section involved evaluation of the discharge characteristics of Schottky diode detectors. By means of a mechanical light shutter the detector is periodically illuminated. During the "black out" interval the detector is reverse biased, or charged and the resultant current is a measure of the amount of charge lost during the illuminated time interval. Additionally it was of interest to provide the capability of evaluating the significance of the leakage current in terms of its contribution to the decay characteristics of the detector.

Thus it was decided to provide two charging intervals during the "black out" period separated by a sufficient time interval for evaluation of the leakage current. The detector must be isolated during the entire time of illumination and between the two charge intervals.

The basic instrumentation system is broken into three functions; timing and control, charging and isolation. These will be described in detail in the next three sections.

1.1 Timing and Control

The timing and control circuitry is synchronized with a signal generated by the light shutter. For this particular application it was a 10 volt square wave at a frequency that was dependent upon the speed of light chopping wheel. A two stage amplifier with the

capability of adjusting the amplitude and phase was used as an interface between the synchronizing signal and the input to the timing circuitry.

Three monostable multivibrators connected in cascade are used to generate the necessary gating pulses in the proper sequence. In the initial design three NE555 timers were used to implement this circuitry as indicated in Figure 1.1. In the interest of reducing the complexity of the circuitry and minimizing triggering difficulties the second and final design incorporated an SN74123 and an SN74L122 in place of the NE555's. As indicated in Figure 1.2 this design used fewer IC's and passive components, however, the current requirement was somewhat higher.

The SN74123 is a dual monostable circuit as is the SN74L122. Neither require any special triggering waveform as they operate on either the leading or trailing edge of the input synchronizing pulse. As indicated in Figure 1.2 one half of the SN74123 is used to generate the initial charging time interval control pulse which is nominally 20 μ sec and occurs immediately after the end of the illumination period. At the end of the 20 μ sec pulse the trailing edge is used to trigger the second unit of the SN74123. This unit generates a delay that is variable between 2.5 milliseconds to about 20 milliseconds. The output of this second unit, following the delay, triggers one half of the SN74L122, which generates the second charging time interval control pulse.

An OR gate is used as an interface between the timing circuitry and the charging and isolation circuitry. Originally the output of the OR gate controlled both of these circuits, however, in the final design it was used only for the isolation circuit as can be seen by comparing Figure 1.4 and 1.5. Details of the timing sequence is indicated in Figure 1.3.

1.2 Charging Circuit

In the initial design of the charge circuit the output of OR gate served two purposes as indicated in Figure 1.4. The output served as the input to a control gating circuit for the isolation amplifier and an input to the charging circuit.

The charging circuit consisted of a 531 operational amplifier used in the noninverting mode. The voltage level of the output of the OR gate is amplified to the desired level by the 531 and serves as one input to the isolation amplifier. Thus, the charge amplifier was synchronized with the two charge pulses.

In the final version of this circuit it was found that synchronization of the charging circuit was unnecessary. Instead, the desired charge voltage was fixed at the input of the isolation amplifier, as indicated in Figure 1.5. A 741 operational amplifier with variable gain and internal compensation was found adequate for the charge amplifier. This approach, nonswitching of the charging voltage, resulted in reduced compensation and transient difficulties.

1.3 Isolation Circuit

The basic operation of this circuit makes use of the sample and hold capabilities of an operational-transconductance amplifier, OTA, and a MOS-FET in a closed loop configuration. The OTA is unique in that it is capable of being strobed such that it operates as a normal operational amplifier or is off with zero gain with an output impedance of the order of 10^9 ohms. The MOS-FET used in the source-follower configuration closes the loop and isolates the device under test, DUT, by virtue of its large input impedance. Closed loop operation results in improved transient response and reduced charging time.

The DUT is connected between the OTA output, the gate of the MOS-FET, and ground. When the strobe voltage to the OTA is zero volts the OTA and the MOS-FET operate normally with the input charge voltage applied to the DUT. When the strobe voltage is -15 volts the OTA is turned off and the DUT is isolated from the charge voltage shunted by the output and input impedance of the OTA and MOS-FET respectively.

The decay of the charge of the DUT is obtained at the source of the MOS-FET source-follower without disturbing the DUT. An evaluation of the lost charge can be made by means of a resistance in series with the DUT.

The strobe voltage must have a magnitude of 15 volts, between zero and -15 volts, with a width of 20 μ seconds. This gate voltage is generated by means of a two stage discrete BJT circuit using two PNP's. The input to this gate is the output of the OR gate. This approach was necessary because of the pulse width and the

amplitude which is difficult for normal IC amplifiers.

The final version of this circuit is shown in Figure 1.5. Comparing it with Figure 1.4 it can be seen that aside from minor modifications both versions are essentially the same.

Figures 1.6a, 1.6b and 1.6c are waveforms obtained at the source of the MOS-FET source-follower with a Schottky diode under test for different charge levels. Discharge characteristics for diode while illuminated and when in the dark are significantly different. The reverse biased junction charge decay is the greatest when the diode is illuminated. The smaller decay occurs during black out, the interval between the two charges pulses, and is related to the leakage current.

II Optical Signal and Random Noise Source - Model II

2.0 Introduction

The prototype Optical Signal and Random Noise Source was reported on in report number AFRL-TR-74-0058 dated 1 December 1973. This model had a fixed polarity output, a mechanical vernier for fine control of the noise PMT and no provision for external modulation of the LED optical input to the optical PMT. Subsequent evaluation has revealed certain modifications that were deemed desirable.

2.1 Modifications

In the original model fine control of the noise PMT output was obtained by varying the spacing between the scintillation source and the PMT by mechanical means. This method proved inadequate in that the total variation was insufficient and the minimum output was not adequate.

At first, consideration was given to reducing the output by shielding the 5 μ curie radioactive source. This approach was not taken since a 0.5 μ curie source was available in the same size package as the original source for the same cost. The mechanical vernier was discarded in favor of control by variation of the high voltage similar to the means used for the LED PMT, i.e., switched series resistances.

The output of the noise source was modified so that either polarity signal is available. This modification merely involved the use of an inverting amplifier at the summation mode of the outputs of the two PMT's.

Provision was made for external modulation of the LED. This involved the addition of an internal amplifier similar to the one used at the output of the internal square wave oscillator. The basic details of these modifications are indicated in Figure 2.1.

III Noise Reduction Circuitry

3.0 Introduction

A technique for gamma pulse noise suppression by cancellation was introduced in the report mentioned earlier in Section II. This approach involves isolation of the gamma pulse from the signal, synthesizing a mirror image pulse and finally summing the original signal with the mirror image pulse to obtain a noise free signal.

3.1 Synthesizing the Gamma Mirror Image Pulse

The basic approach of this technique is to differentiate the original signal containing the gamma pulse and thereby remove the signal.

The resultant differentiated signal is then integrated to obtain the original pulse reversed in phase by 180° .

This approach is shown in Figure 3.1. The output from the buffer amplifier is differentiated at the input to the inverting input of the 531 operational amplifier. Positive going signals at the output gate diode D_1 on during the integration time. Diode D_2 suppresses negative going swings at the output.

Difficulty was encountered with this circuit which was related to compensating the 531 operational amplifier. Normally a single capacitance is used between the output and the compensation node. It was found necessary to split the compensation as indicated in Figure 3.1.

The output of the differentiator-integrator is buffered from the summing amplifier by a variable gain noninverting amplifier stage using a 531 operational amplifier.

3.2 Delay and Summing

In the breadboard version it became apparent that it was necessary to delay the original signal prior to summing it and the image pulse. The delay required was of the order of 0.5 μsec . As indicated in Figure 3.1 this delay is inserted between the signal post amplifier and the summing amplifier.

The delay circuit is an MFD filter designed to have a variable zero frequency delay τ_0 . This circuit is a third order Thompson filter of the form described in the report mentioned in Section II, however, 531 amplifiers were used rather than 741's. Variation in τ_0 was accomplished in discrete steps. It was decided to make τ_0 variable in order to compensate for variations that might arise from wiring and component placement of the prototype instrument.

An MFM filter was used between the output of the summing amplifier and the final output of the instrument. The bandwidth of this filter was variable between 5KHz, 10KHz and 15KHz in three discrete steps. The form of this Butterworth filter is the same as the MFD Thompson with the desired characteristics obtained by appropriate matching of the coefficients of the transfer functions. Addition of this filter makes it possible to evaluate either noise output or harmonic content of the signal for which the anticipated fundamental was about 4KHz.

3.3 Summary

In the breadboard version of this circuitry it was found possible to achieve 25 db suppression of the undersirable gamma pulses. These results were obtained using the Optical Signal and Random Noise Source Model II. A somewhat smaller value of suppression was obtained with the final prototype. Evaluation of the final circuitry indicated that the final form of the circuit layout had introduced additional delay, more than had been anticipated, such that optimum suppression was not possible. The suppression obtainable with the early prototype was only about 20 db.

3.4 Conclusions

Evaluation of the gamma noise suppression circuitry suggests two avenues that should be investigated to improve the efficiency of the prototype instrument. One of these is to improve the control of the delay in its early location in the circuitry by improved physical layout, and or choice of improved IC active devices. An alternative

approach which should be investigated is the optimum location of the actual delay circuitry. That is, it may be feasible to place the delay in the circuit prior to differentiation and thereby obtain more flexibility.

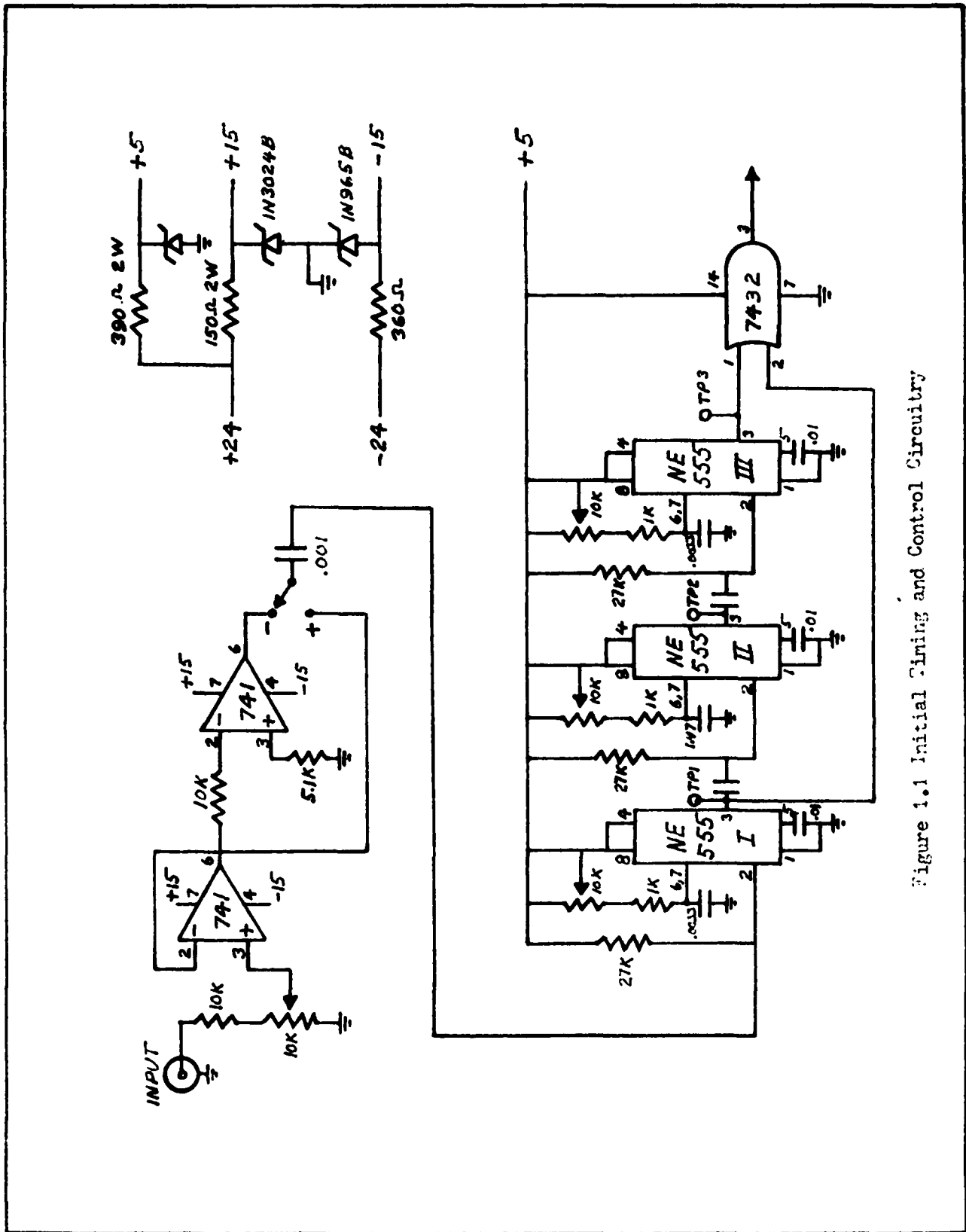


Figure 1.1 Initial Timing and Control Circuitry

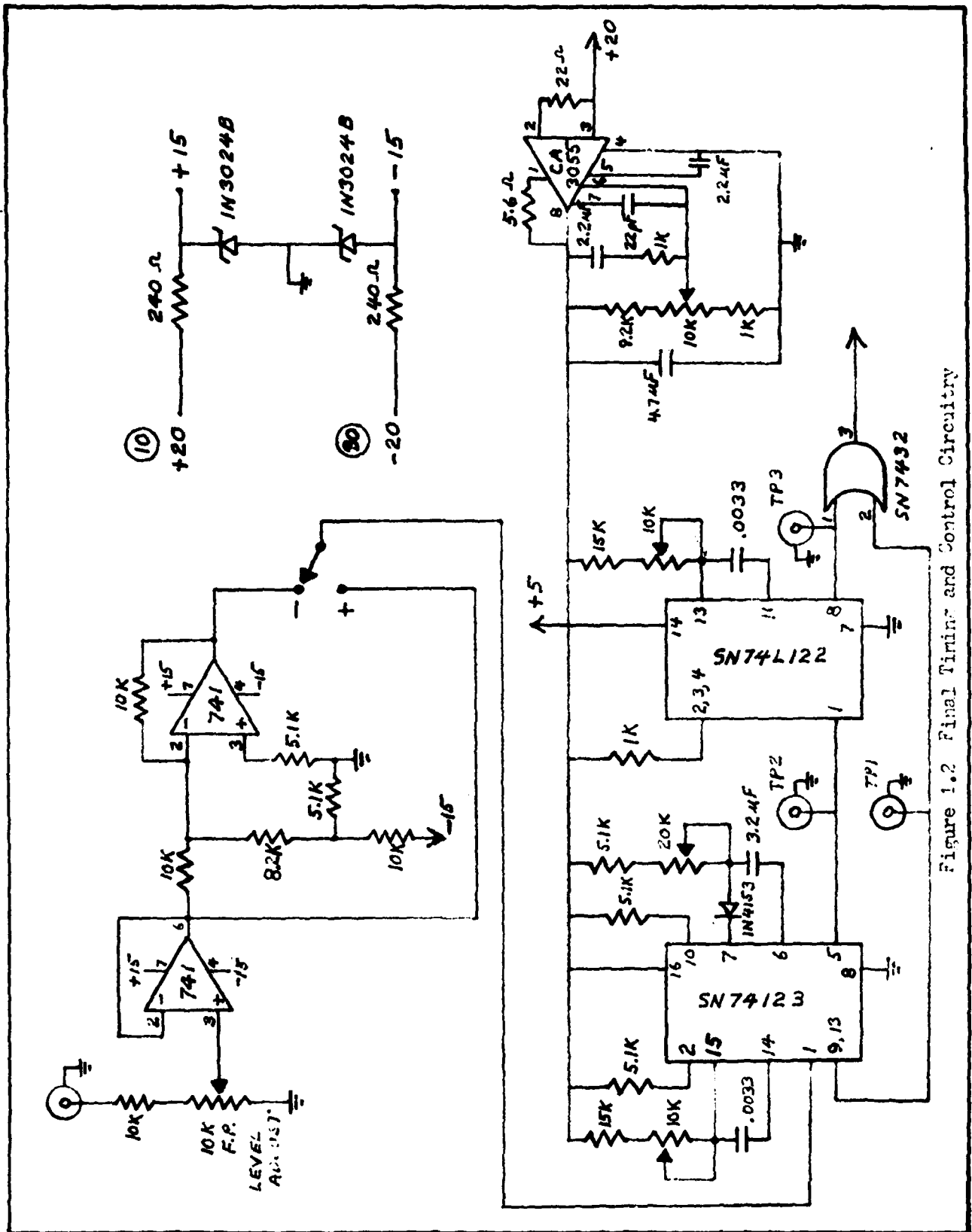


Figure 1.2 Final Timer and Control Circuitry

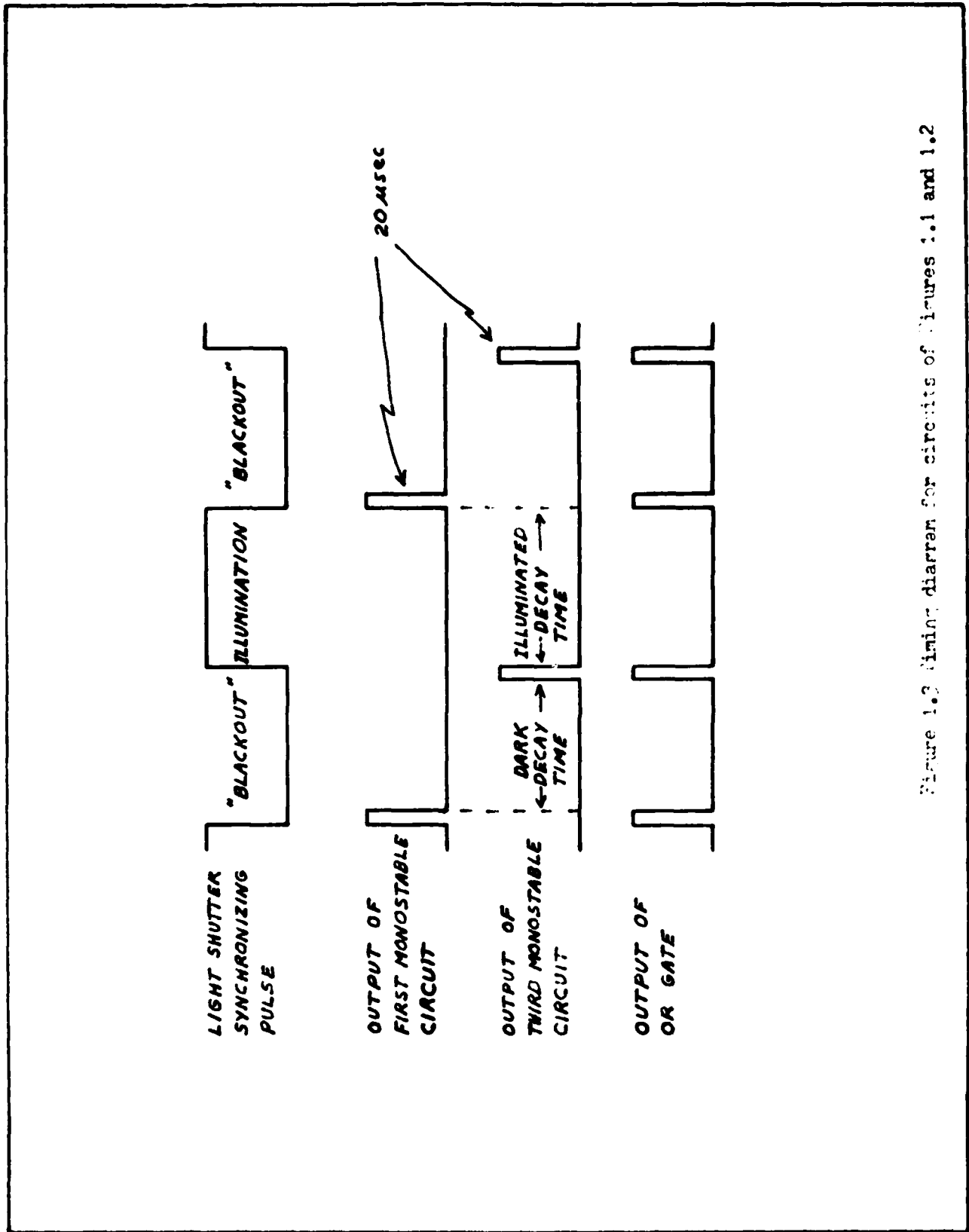


Figure 1.2 Timing diagram for circuits of Figures 1.1 and 1.2

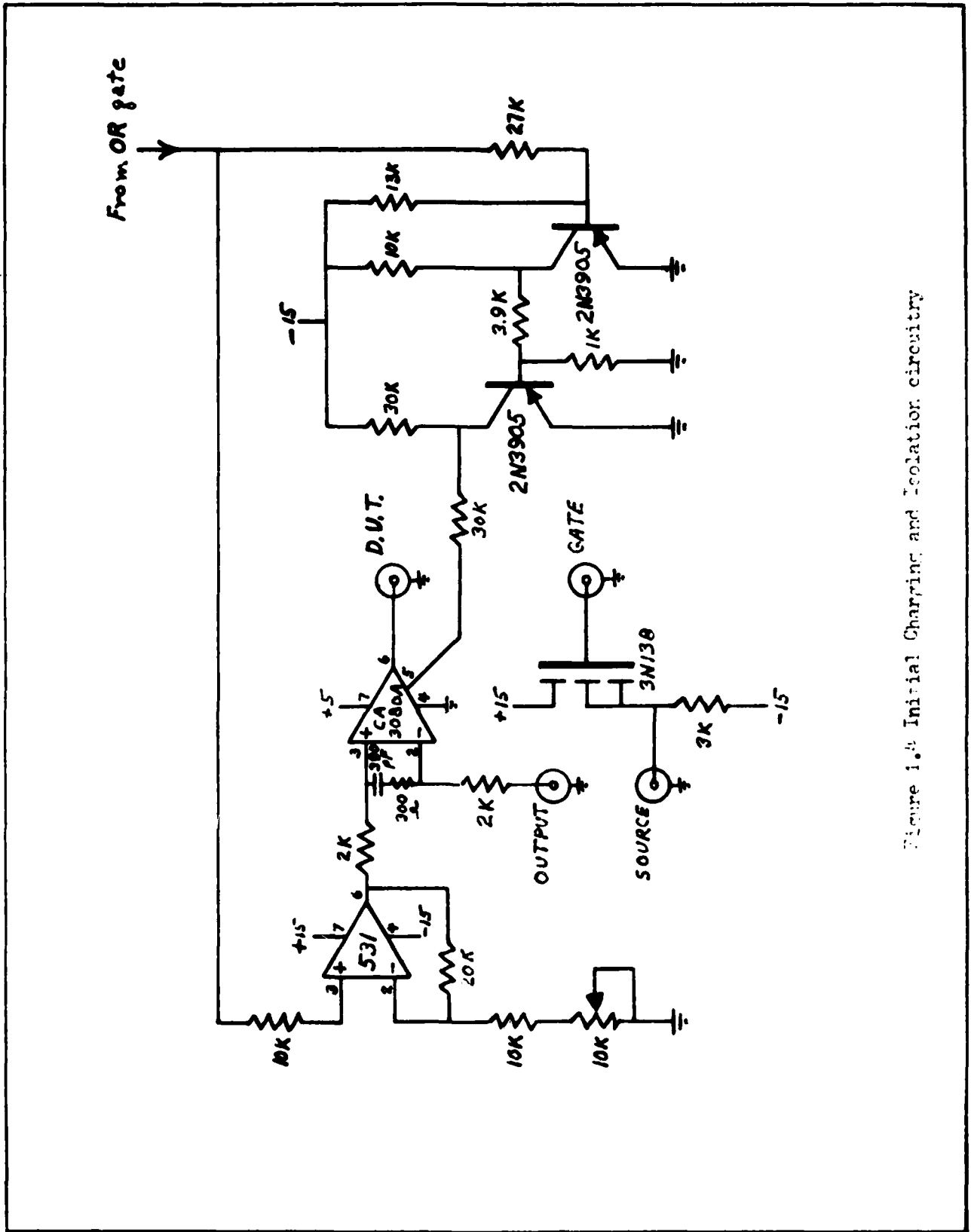


Figure 1.4 Initial Charging and Isolation circuitry

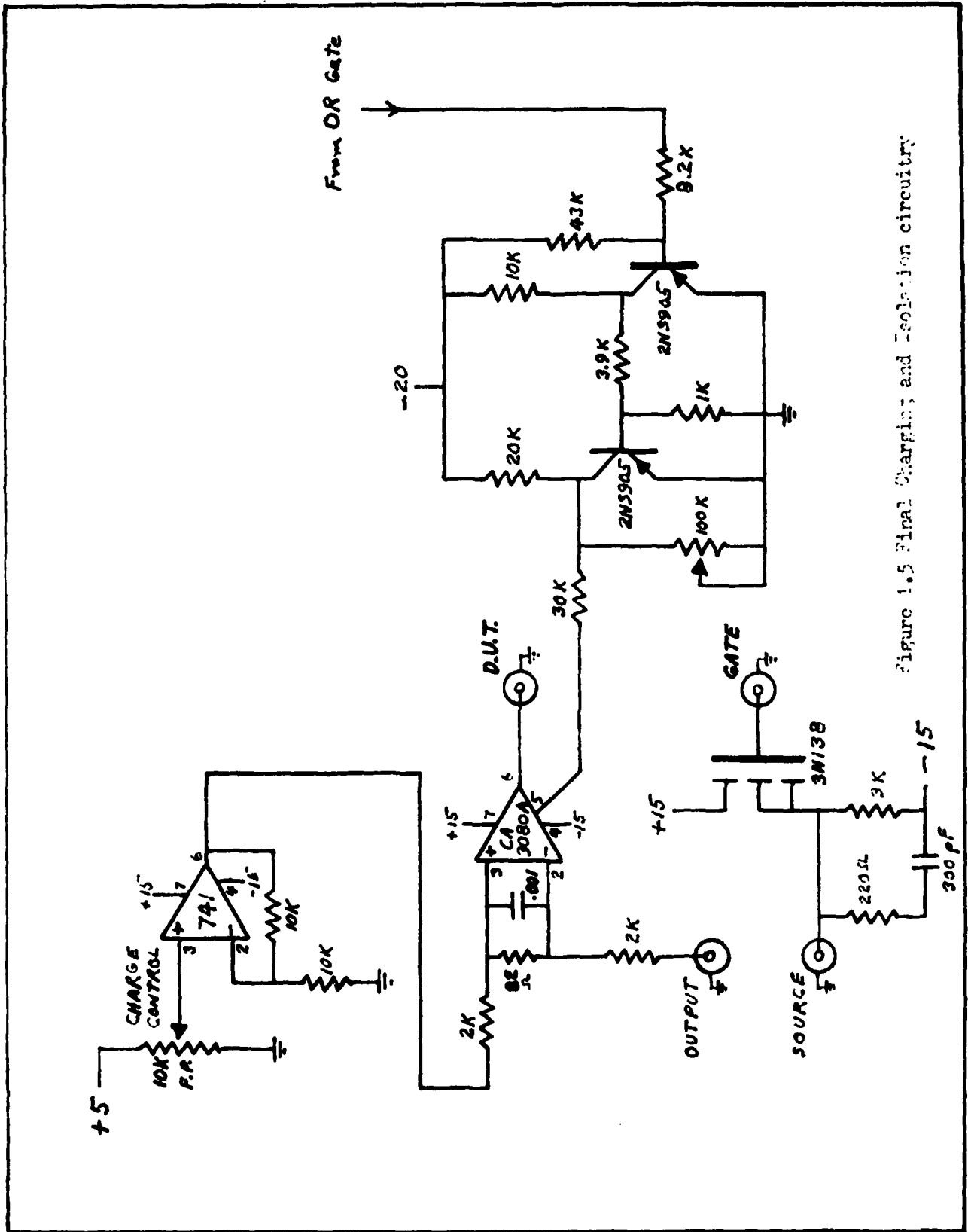


Figure 1.5 Final Charging and Isolation circuitry

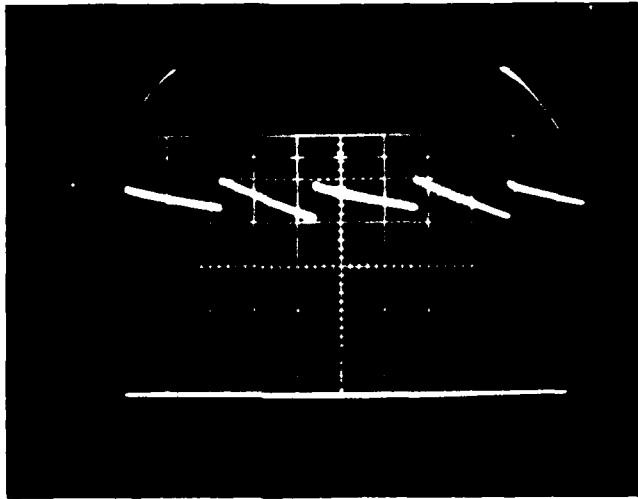


Figure 1.6a

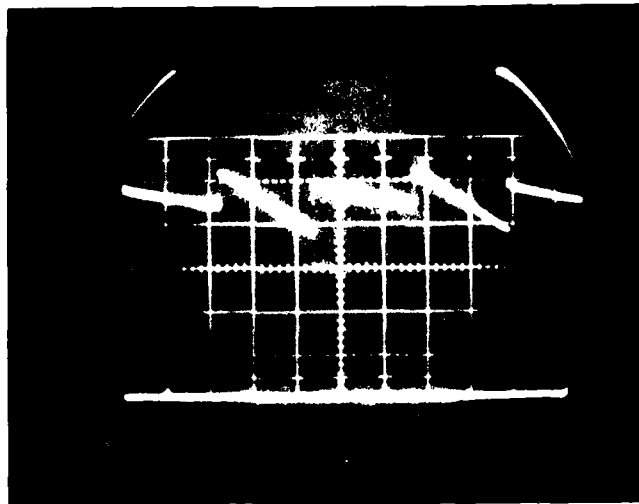


Figure 1.6b



Figure 1.6c

Figure 1.6 Charge decay waveforms for a Schottky diode. The more shallow decay results from the leakage current during black out. The deeper decays result from the decay while the diode is illuminated.

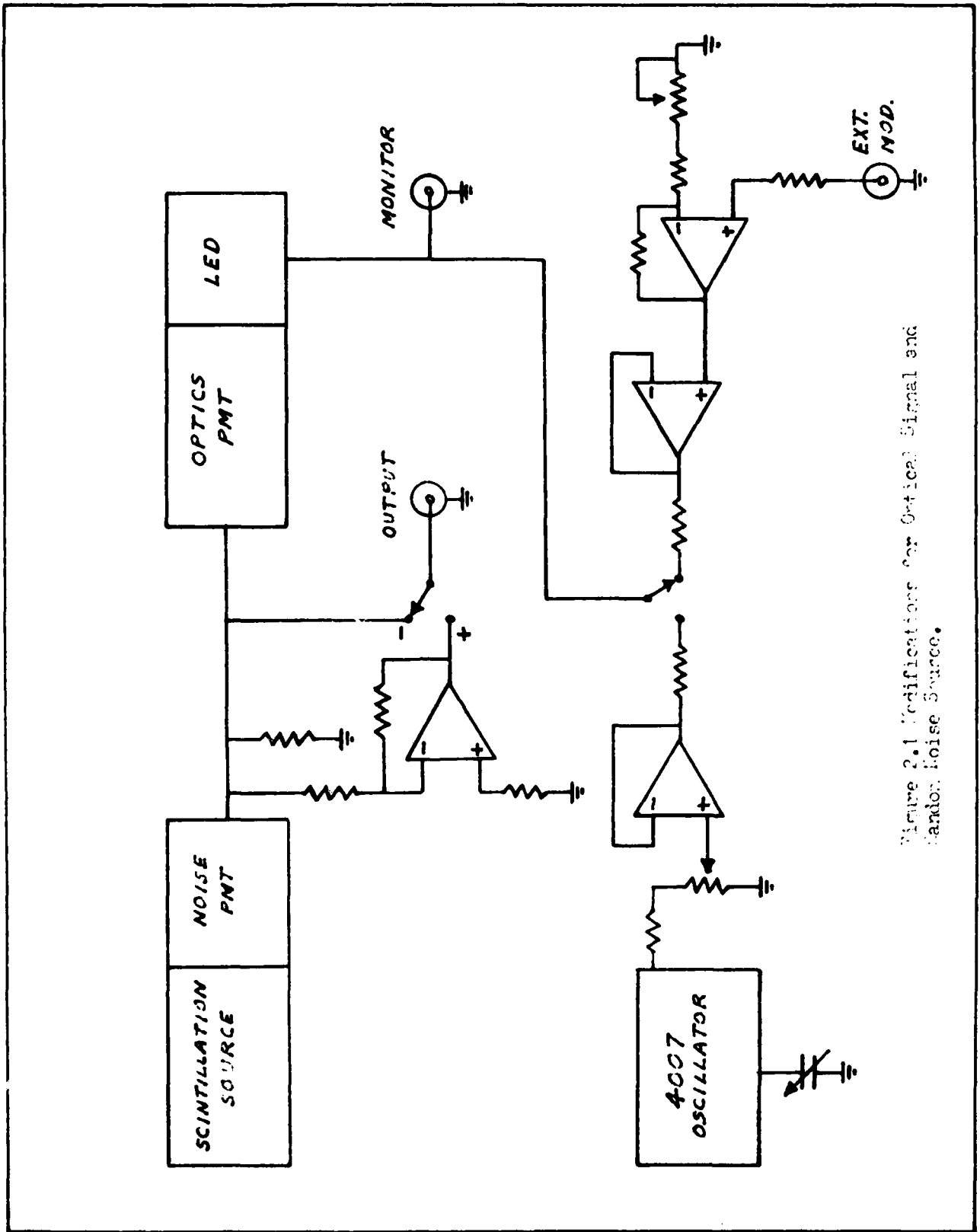


Figure 2.1 Modification for Optical Signal and Random Noise Source.

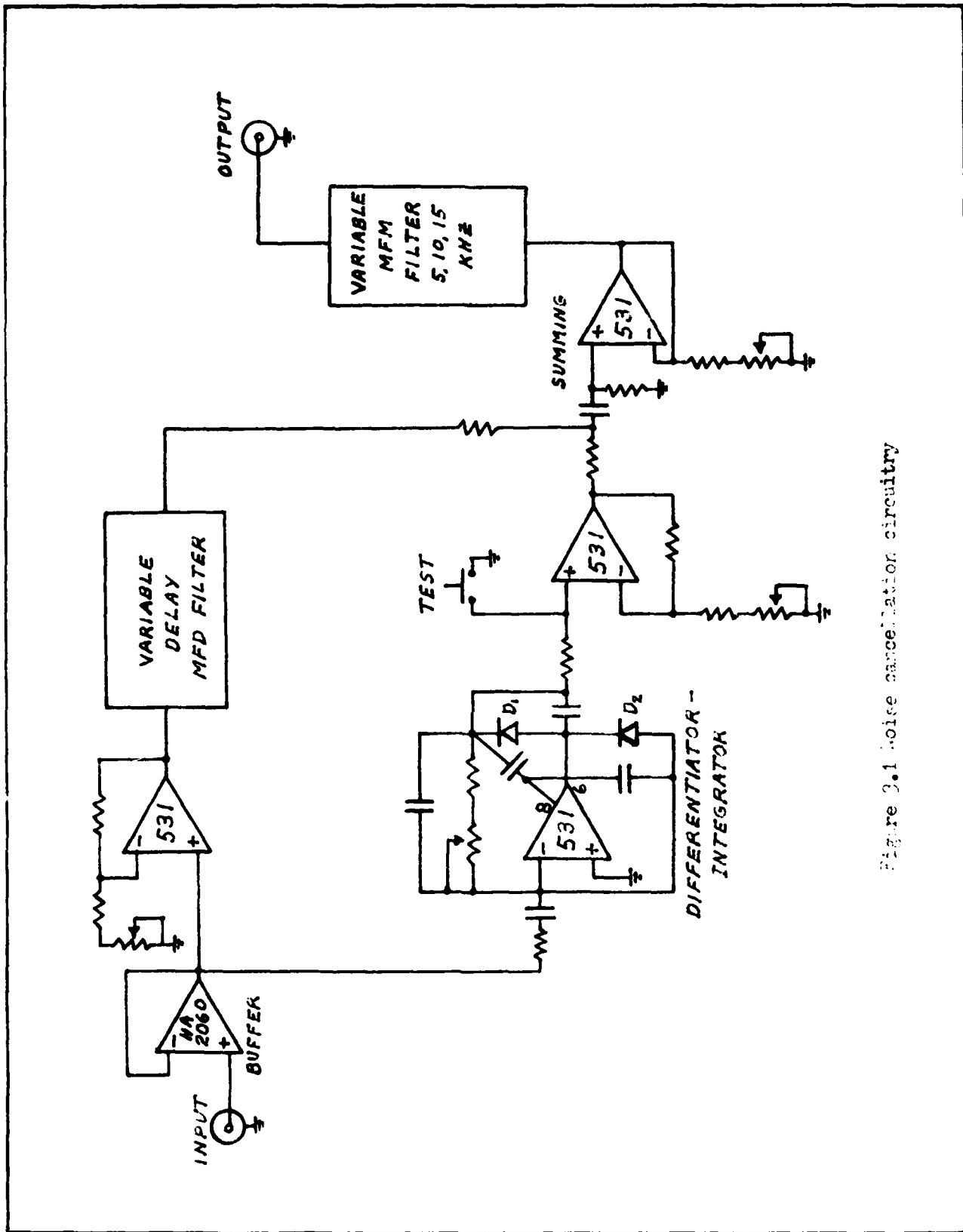


Figure 3.1 noise cancellation circuitry

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