AD-A098 029 NATIONAL BUREAU OF STANDARDS WASHINGTON DC NATIONAL E--ETC F/G 20/12
SEMICONDUCTOR TECHNOLOGY PROGRAM - PROGRESS BRIEFS.(U)
MAR 81 W M BULLIS
UNCLASSIFIED NBSIR-81-2230 NL

END
DATE FILMED
5-81
DTIC

NBSIR 81-2230

Semiconductor Technology Program Progress Briefs

W. Murray Bullis, Editor

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
U.S. Department of Commerce
Washington, DC 20234

March 1981

Prepared for

The Defense Advanced Research Projects Agency
The National Bureau of Standards
The Division of Electric Energy Systems, Department of Energy
The Defense Nuclear Agency
The Charles Stark Draper Laboratory
The Naval Air Systems Command
The Air Force Wright Aeronautical Laboratories
The Army Electronics Technology and Devices Laboratory
The Naval Weapons Support Center
The Solar Energy Research Institute
The Naval Avionics Center
The Lewis Research Center, National Aeronautics & Space Administration
The Office of Naval Research
The Naval Ocean Systems Center

SEMICONDUCTOR TECHNOLOGY PROGRAM

TABLE OF CONTENTS

ABSTRACT - This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Emphasis is placed on silicon and silicon-based devices. Highlighted activities include an analysis of the cross-bridge sheet resistance test structure, observations of laser-induced patterns on semiconductor surfaces, a technique for analysis of data from test structures on process validation wafers, and advances in optical measurements of linewidth on wafers. Brief descriptions of upcoming linewidth measurement seminars and the second moisture measurement workshop are also given. In addition, recent publications and publications in press are listed. The report is not meant to be exhaustive; contacts for obtaining further information are listed.

KEY WORDS - Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

Preface

This report covers results of work during the fiftieth quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce, and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 5. The Defense Nuclear Agency; 6. The C. S. Draper Laboratory; 7. The Naval Air Systems Command; 8. The Air Force Wright Aeronautical Laboratories; 9. The Army Electronics Technology and Devices Laboratory; 10. The Naval Weapons Support Center; 11. The Solar Energy Research Institute; 12. The Naval Avionics Center; 13. The Lewis Research Center, National Aeronautics and Space Administration; 14. The Office of Naval Research; and 15. The Naval Ocean Systems Center.

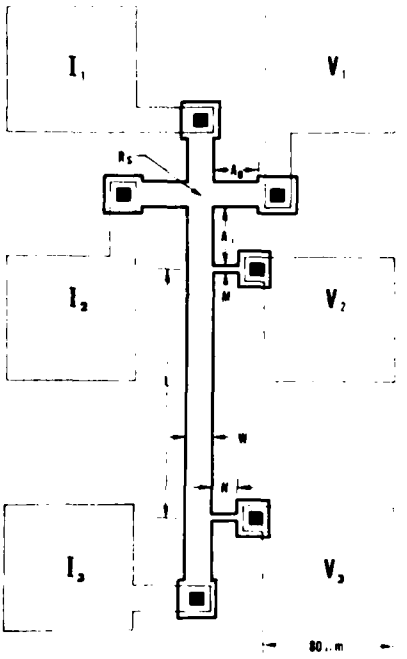
This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported herein are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information, past issues of progress briefs, and a list of publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

Cross-Bridge Sheet Resistors

Analysis of a study of the sensitivity of the channel linewidth as measured by the cross-bridge sheet resistor test structure to three geometrical factors was completed. The three factors are 1) the presence or absence of symmetry tabs on three arms of the cross portion of the structure, 2) the finite width of the bridge voltage taps, and 3) the distance between a voltage tap and the end of the linear portion of the conducting channel of the bridge ("tap-to-corner" distance). The measurements were carried out on nominally 6-, 12-, 18-, and 24-μm wide aluminum and doped region conducting channels fabricated on test pattern NBS-12. Because of overetching effects, the metal channels are somewhat narrower and the doped region channels are somewhat wider than the design dimension; lateral diffusion may also contribute to the widening of the doped region channel.

In the original design of the cross-bridge structure, symmetry tabs and perpendicular contact arms were employed to assure the symmetry of the cross portion of the structure and the applicability of the uncorrected van der Pauw relation. Results of the present study suggest that such refinements are not necessary. A modified design, shown in the accompanying figure, introduces geometry-related inaccuracies of less than 1 percent in the linewidth determination provided that the following relationships are met: tap length (N) greater than tap width (M); tap-to-tap distance (L) greater than 15 times tap width (M); channel width (W) equal to or greater than tap width (M); and tap-to-corner distance (A_1) greater than channel width (W).

It is important to differentiate between factors which affect the accuracy of the measurement and those which affect the resolution of the measurement. The geometrical factors addressed in this study introduce systematic errors in the sheet resistance and linewidth measurements. Process-induced random variations, which contribute to the imprecision of the measurement, are typically smaller; although the result of



Outline drawing of a cross-bridge sheet resistor formed in a doped region conducting channel. Dark lines denote the edges of the doped region, light lines denote the edges of the metallization, and the filled-in areas denote contact windows.

the measurement may differ significantly from the "true" result, the experiment can be designed so that the measurement has great sensitivity and good repeatability. This is particularly important for measurements of linewidth uniformity with an array of cross-bridge resistors; in this case the absolute accuracy of the linewidth measurement is not as important as the precision which determines the achievable resolution. The presence of systematic process-related variations would be expected to degrade the resolution. [Sponsor: 2]

(G. P. Carver and R. L. Mattis, x3541)

Laser-Induced Surface Patterns

One consequence of using radiation from a flashlamp-pumped dye laser as a source for surface heat generation in semiconductor annealing is the formation of nonuniform patterns due to diffraction and interference of the light within the surface region of the semiconductor. This can result in surfaces that are not flat after annealing. One particular case of an uneven surface occurs for laser energy densities near the threshold where the silicon surface appears to melt. "Frozen-in" linear fringe patterns are formed on the silicon surface with fringe spacing close to the wavelength of the incident laser beam. The nature of this fringe pattern is that of an optical grating which is produced by the interaction of an incident laser beam and a generated surface wave trapped in the shallow annealing region. The polarization of the incident beam and the angle of incidence determine the direction of surface wave propagation, the fringe direction, and the fringe spacing. [Sponsor: 2] (D. Horowitz, D. R. Myers,* and P. Roitman, x3625)

Analysis of PVW Data

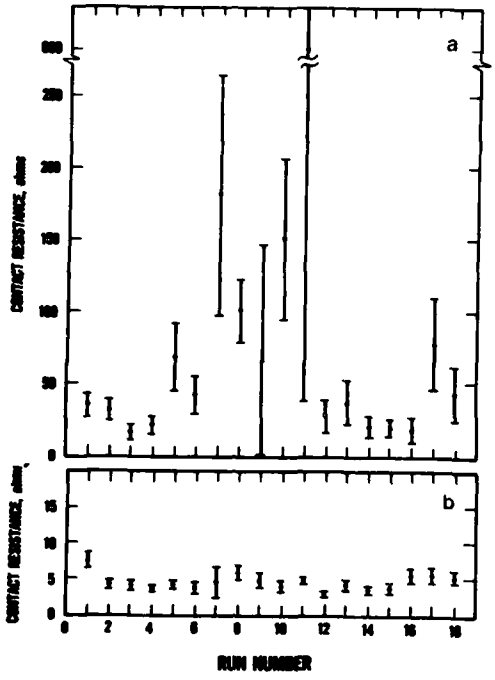
A process validation wafer (PVW) is one which contains test chips over most or all of its surface. The test chips contain a variety of process parameter test structures, each of which is sensitive to one or another material or process parameter. In a developmental integrated circuit process, results from measurements on the process parameter test structures on a PVW which accompanies each process lot can be used to identify which parameters accurately predict or determine the degree of process control; to establish what these parameters are for a given process lot; and to determine how these parameters vary across an integrated circuit die, across a wafer, from wafer to wafer, and from lot to lot. However, in order to be used for correcting or improving the process, the test results must be obtained and interpreted in a timely fashion.

Large amounts of data are obtained from PVWs. In most cases, it is essential to maintain lot identification and chip location information in order to establish statistically significant trends or correlations. It is also necessary to exclude data from defective test structures which do not accurately represent the parameter being measured. The inclusion of data from these structures would result in an incorrect determination and loss of information about systematic trends and analysis of baseline electrical parameters.†

A computer program, STAT2, has been written to analyze data taken on process validation wafers. The program has as its main functions (1) reading of wafer test data from disc files representing a variety of array sizes and formats; (2) identification and exclusion of outliers; (3) calculation of mean, median, and standard deviation of the data points not previously excluded; (4) fitting of the included data values to a

*Present address: Sandia Laboratories, Albuquerque, New Mexico.

†Other types of test structures, e.g., random fault test structures, can be utilized to detect process-induced faults such as metal breaks, oxide or metal-bridging shorts, diffusion pipes, poor contacts, etc. which, if present, could result in a defective process parameter test structure (or product circuit).



Mean and standard deviation of the metal-to-n$^+$ (a) and metal-to-p$^+$ (b) contact resistances for a series of process runs.

plane or quadratic function; (5) creation of a data base by which various sets of wafer data can be automatically compared; and (6) production of wafer maps representing the spatial variation of the data values of selected parameters over the wafer.

A data point can be excluded from the population if it is greater than or less than a specified value, if it is farther than a specified multiple of the sample standard deviation from the sample mean, or if it has been obtained from a peripheral site. Care must be used in applying these procedures so as to not exclude legitimate data points from the population. An algorithm has also been developed which by iteration excludes outliers on a statistical basis by taking into account the number of included data points and the probability that one or more "good" data values might be excluded. For this algorithm, data from properly fabricated test structures are considered to be normally distributed. Test results which deviate slightly from a normal distribution do not adversely affect the analysis.

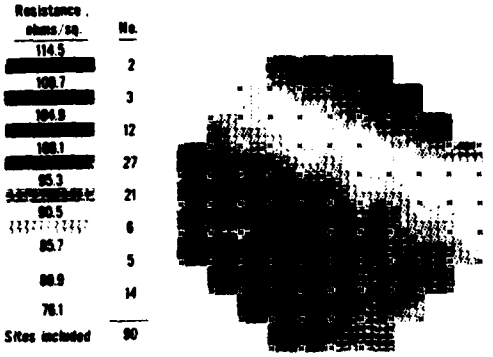
When comparing lot-to-lot variations, trends may sometimes be indicated by the time-variations of the mean and standard deviation of appropriate parameters. For example, the accompanying charts for a series of process runs suggest that problems are being encountered in the control of the metal-to-n^+ contact resistance, but that the metal-to-p^+ contact resistance is under good control.

To establish causes of such trends, it is frequently necessary to determine spatial distribution and point-by-point correlations between different sets of data. A data base can be constructed which can be used to search for such correlations. A representative sample of each data set is stored in disc files. A particular such sample can be selected and other samples in the data base can be compared to it by calculating the correlation coefficient relevant to the two samples. The search can be limited to all data sets from a particular wafer or from a particular device or a particular parameter. An example of the correlations obtained between eight parameters on a wafer from one of the previously mentioned process runs is shown in the accompanying table. These correlations were calculated from a 13-point sample from each data set.

Sample Correlation Coefficients for Selected Process Parameters

	A	B	C	D	E	F	G	
B	-0.80							
C	-0.13	0.11						
D	-0.01	-0.12	0.01					
E	-0.65	0.57	-0.03	-0.13				
F	0.28	-0.30	-0.10	0.76	-0.41			
G	-0.13	0.12	-0.68	-0.61	0.16	-0.50		
H	-0.29	0.01	0.60	-0.07	-0.13	-0.23	-0.27	

A, p-channel threshold voltage, B, n-channel threshold voltage, C, metal-to-p$^+$ contact resistance, D, metal-to-n$^+$ contact resistance, E, p$^+$ sheet resistance, F, n$^+$ sheet resistance, G, metallization linewidth, H, polysilicon sheet resistance



Wafer map of n^+ sheet resistance with eight-level gray scale. Actual measurement locations included in the analysis are denoted by an ×. The range between the highest and lowest measured values is divided into eight equal intervals. For this drawing, the lettering was enhanced to facilitate reproduction.

Note that there is a relatively high correlation coefficient between the n^+ sheet resistance and the metal-to-n^+ contact resistance while there is no correlation between the two contact resistances (which might be expected under normal conditions because all contact windows were opened in the same lithographic process). Based on this data analysis, it was possible to identify serious process difficulties which would not have been detected by other means.

To verify the existence of correlations, wafer maps can be prepared for direct observation. The wafer map capability generates a drawing whose size is selectable by the user and in which parameter values are represented by an eight-level gray scale. Interpolation is used to fill in the space on the map between actual measurement locations shown by an × as illustrated in the accompanying figure. Replacement values, calculated by interpolation or extrapolation, are used to represent excluded data points. A key is provided to give the range of values represented by each gray tone.

In addition to analyzing test results from a PVW, this technique can be used to evaluate test results from a wafer containing test structures distributed over the wafer at periodic locations, for example, on a portion of each product die.

Program STAT2 is presently being modified to make it more portable. Those lines of code which cannot be made portable are being identified by comments. For example, part of the mapping code must be altered to suit the plotter to be used. In addition, a User's Manual is being prepared. Organizations interested in obtaining the FORTRAN code for STAT2 on magnetic tape should request the code in writing from the Electron Devices Division. [Sponsors: 2,5,8]
(L. W. Linholm, R. L. Mattis, and L. J. Till, x3541; R. C. Frisch, x3621; and C. P. Reeve,* x2805)

Optical Linewidth Measurements

A new theoretical approach has been developed leading to more accurate linewidth measurements for lines patterned in thick layers (>200 nm) on integrated circuit wafers. In the past, scalar coherence theory has been successfully applied to the measurement of lines patterned in thin layers with features as small as 0.5 μm. This theory led to coherent edge detection techniques which require correction for the relative phase change at the object edge as well as for object contrast. Although the scalar coherence theory can be applied to opaque objects in transmitted light with relative ease, the problem of dimensional measurement of low-contrast thick objects (such as patterns on oxidized silicon wafers) in reflected illumination is more difficult.

In the scalar coherence theory approach, the object is characterized by its amplitude reflectance and phase. In the measurement of line objects in thin films, the reflectance and phase vary

*NBS Statistical Engineering Division.

steeply with wavelength. As the objects become thicker, the reflectance and phase also vary steeply with angle of incidence. The limitations of the scalar coherence theory approach become apparent as the line objects become thicker, but coherent edge detection techniques may still be applied for a symmetric amplitude impulse response of the imaging system. However, for thick objects, although the optical imaging system remains unchanged, the amplitude Fourier spectrum of the illuminated object, including the apparent contrast and phase, changes with mode of illumination and object thickness.

A formalism to describe thick objects has been developed. This formalism is based on the use of waveguide theory to describe the propagation of an incident plane wave through the thick 3-D layer and the application of scalar theory to treat the imaging of the exiting optical amplitude distribution. A computer program for predicting the optical image profiles of lines patterned in thick layers has been developed to implement this formalism. The program was debugged and is working for 11 by 11 matrices. This corresponds to 1.5-μm lines with a 3-μm period. For this case, as illustrated in the accompanying figure, the image profiles agree quite well for image profiles calculated from scalar coherence theory for patterns in a 90-nm thick layer of silicon dioxide on silicon. For such thin layers, the effective relative reflectance and phase agree with the predictions of the Fresnel equations. As expected, calculations of image profiles of lines in thicker layers (400 and 600 nm) show large differences from scalar coherence calculations in the profiles as well as in the effective reflectance and phase.

In addition, the problem of the design of a wafer standard reference material (SRM) is being reformulated. The wafer SRM must contain a set of linewidths (0.5 μm to 10 μm) for calibration of optical systems for materials, with variations in relative reflectances T_o

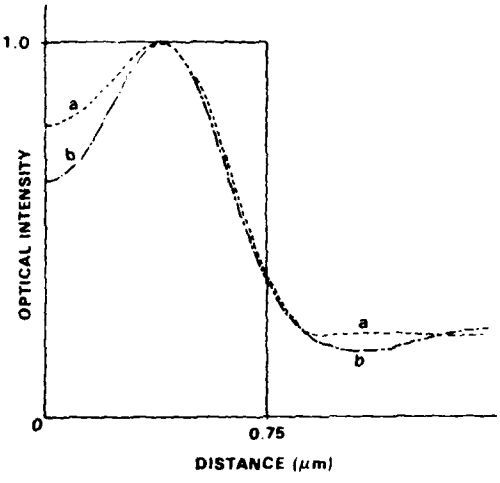


Image profiles of a periodic line object with 1.5-μm wide lines with a 3-μm period in a 90-nm thick layer of silicon dioxide on silicon as calculated by scalar coherence theory (a) and 3-D formalism (b) (wavelength: 530 nm; objective lens N.A.: 0.85; coherence parameter: 0.25).

(ratio of the reflectance of the layer material to that of the substrate) between 0 and 1.0, and phase differences ϕ between 0 and π. Replication of the pattern used for SRM 475 (which contains ten lines of both polarities, approximately evenly spaced over the range) in enough material-film thickness combinations to adequately cover the ranges of T_o and ϕ would result in a prohibitively large number of lines to be measured in certification and use of the SRM. Requiring the repeat measurements necessary for reasonable statistical analysis would further deter many people from using such an SRM. However, if the surface $\Delta(T_o,\phi)$, which describes the calibration error, can be fit with a polynomial of known order, Gauss quadrature techniques can be applied to determine the optimum pairs of values of T_o and ϕ at which linewidths should be measured to most accurately determine the constants in the polynomial. Preliminary results indicate that, for the

case in which the center of the dark band which occurs at the line edge is used as the edge detection criterion, 72 linewidths, 36 of each polarity, are required for calibration of a system for measurements on all wafer materials. Work is continuing to establish the number required for system calibration when a preselected optical threshold is used as the edge detection criterion. [Sponsors: 2,7,8,9]

(D. Nyyssonen, x3621)

Linewidth Measurement Seminars

A 2-1/2-day training seminar on Linewidth Measurements on Integrated Circuit Photomasks and Wafers is being held in Palo Alto, California on March 23-25, 1981, to present up-to-date information on the accurate measurement of linewidths in the 0.5- to 10-μm range. The seminar includes lecture sessions, equipment demonstrations, and group discussions. Emphasis is on optical microscope techniques. It differs from previous NBS linewidth measurement seminars in that equipment demonstrations are being provided instead of the previously included hands-on training with various measurement systems, both manual and automatic. The 75-person capacity of this seminar is expected to be oversubscribed; a similar seminar is tentatively scheduled to be held at NBS/Gaithersburg later this year. [Sponsor: 2] (E. C. Cohen, x3786, and J. M. Jerke, x3621)

Moisture Measurement Workshops

A second workshop on Moisture Measurement Technology for Hermetic Semiconductor Devices was held at NBS/Gaithersburg on November 5-7, 1980. The workshop was designed to facilitate exchange of information among over 130 specialists concerned with moisture measurement problems. Topics in the technical program* covered included mass spectrometry measurement of moisture in device packages; use of *in situ* moisture sensors; moisture measurement during processing and assembly; physics of water vapor transport, sorption, and reactions; moisture characteristics of package materials; and leak detection methods. A proceedings volume including texts of the 37 papers presented at the workshop is being prepared for issuance in the NBS Special Publication 400- series on Semiconductor Measurement Technology later this year. The proceedings of the previous moisture measurement workshop is now being readied for publication in the same series; it will be available in about two months. [Sponsor: 2] (E. C. Cohen, x3786)

Update - Film Thickness Standards

Some delay has been encountered with respect to the planned issuance of thermal oxide thickness standards for ellipsometry measurements. It was originally intended that polished 2-in. diameter silicon wafers with a thermally grown silicon dioxide film nominally 80 nm thick, with the actual thickness measured in accordance with ASTM Method F 576, Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry, be made available as SRM 1524 during 1980. However, it became necessary to postpone the production and certification of this standard reference material (SRM) until the multilaboratory repeatability of Method F 576 can be demonstrated; an industrial round-robin experiment for this purpose was recently begun by ASTM Committee F-1 on Electronics. A prior experiment of this type turned out to be incomplete. In addition, further refinement of the previously conducted experiment on temporal stability of the measured oxide thickness is required to establish the time delay between fabrication of the oxidized wafers and the certification measurements necessary to achieve optimal effective stability of

*The technical program was organized by Dr. Robert Thomas of the Rome Air Development Center.

the SRMs. It is expected that these activities can be completed and the standards made available early in 1982. [Sponsor: 2] (J. R. Ehrstein, x3625)

Erratum - NBS Spec. Publ. 400-61

It has come to our attention that there is an error in the sheet resistance equation on page 9 of NBS Special Publication 400-61, *Semiconductor Measurement Technology:* Metrology for Submicrometer Devices and Circuits (June 1980). The correct form of this equation is:

$$R_s(VDP) = (\pi/\ell n2)\ (\Delta V/I)\ ,$$

where $R_s(VDP)$ is the sheet resistance of a symmetrical, four-terminal van der Pauw cross structure, ΔV is the potential difference between two adjacent taps, and I is the current passed through the other two taps. [Sponsor: 2] (W. M. Bullis, x3786)

Recent Publications . . .

Myers, D. R., Wilson, R. G., and Comas, J., Considerations of Ion Channeling for Semiconductor Microstructure Fabrication, *J. Vac. Sci. Technol.* 16, 1893-1896 (November-December 1979).

*Grunthaner, F. J., Lewis, B. F., Vasquez, R. P., Maserjian, J., and Madhukar, A., Reduced Oxidation States and Radiation-Induced Trap Generation at Si/SiO_2 Interface, *The Physics of MOS Insulators*, G. Lucovsky, S. T. Pantelides, and F. L. Galeener, Eds., pp. 290-295 (Pergamon Press, New York, 1980).

*Wilson, R. G., and Comas, J., Correlation of Atomic Distribution and Implantation Induced Damage Profiles in Be Ion-Implanted Silicon, *Radiat. Eff.* 47, 137-142 (1980).

*Vasquez, R. P., and Grunthaner, F. J., Intensity Analysis of XPS Spectra to Determine Oxide Uniformity: Application to SiO_2/Si Interfaces, *Surface Science* 99, 681-688 (1980).

Ehrstein, J. R., Some Considerations Regarding Film Thickness Standards for the Semiconductor Industry, NBSIR 80-2158 (November 1980).

Forman, R. A., Optical Study of Isotopic Effects in the Sulfur Deep Level in Silicon, *Appl. Phys. Letters* 37, 776-778 (1 November 1980).

*Wilson, R. G., and Weglein, R. D., Acoustic Material Signatures Using the Reflection Acoustic Microscope, *Ultrasonic Mater. Characterization*, H. Berger and M. Linzer, Co-Editors, NBS Spec. Publ. 596 (November 1980), pp. 345-355.

Albers, J. H., Comparison of Spreading Resistance Correction Factor Algorithms Using Model Data, *Solid-State Electronics* 23, 1197-1205 (December 1980).

Blackburn, D. L., and Berning, D. W., An Experimental Study of Reverse-Bias Second Breakdown in Transistors, *Tech. Digest, 1980 Internat. Electron Devices Meeting*, Washington, D.C., December 8-10, 1980, pp. 297-301.

Buehler, M. G., Effect of the Drain-Source Voltage on Dopant Profiles Obtained from the d-c MOSFET Profile Method, *IEEE Trans. Electron Devices* ED-27, 2273-2277 (December 1980).

Carver, G. P., and Buehler, M. G., An Analytical Expression for the Evaluation of Leakage Currents in the Integrated Gated-Diode Electrometer, *IEEE Trans. Electron Devices* ED-27, 2245-2251 (December 1980).

*Grunthaner, F. J., Lewis, B. F., Zamini, N., Maserjian, J., and Madhukar, A., XPS Studies of Structure-Induced Radiation Effects at the Si/SiO_2 Interface, *IEEE Trans. Nucl. Sci.* NS-27, 1640-1646 (December 1980).

Ruthberg, S., A Rapid Cycle Method for Gross Leak Testing with the Helium Leak Detector, *IEEE Trans. Components, Hybrids, and Manufacturing Tech.* CHMT-3, 564-570 (December 1980).

Wilson, C. L., Correction of Differential Capacitance Profiles for Debye Length Effects, *IEEE Trans. Electron Devices* ED-27, 2262-2267 (December 1980).

*Reports of contract research.

Publications in Press . . .

Berning, D. W., The Effect of Magnetic Package Leads on the Measurement of Thermal Resistance of Semiconductor Devices, *IEEE Electron Devices Lett.*

Blackburn, D. L., Power Transistor Switching Characterization, NBSIR 81-2204.

Buehler, M. G., and Perloff, D. S., Microelectronic Test Chips and Associated Parametric Testers: Present and Future, *Semiconductor Silicon/1981* (Electrochemical Society, 1981).

Bullis, W. M., and Nyyssonen, D., Optical Linewidth Measurements on Photomasks and Wafers, chapter in *Microstructure Science and Engineering*, Vol. 3, Norman G. Einspruch, Ed. (Academic Press, New York).

Bullis, W. M., Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), NBSIR 81-2224.

Carver, G. P., and Cullen, W. A., *Semiconductor Measurement Technology:* A Manual Wafer Probe Station for an Integrated Circuit Test System, NBS Spec. Publ. 400-68.

Forman, R. A., Larrabee, R. D., Myers, D. R., Phillips, W. E., and Thurber, W. R., Processing Effects on the Electrical and Optical Properties of Sulfur-Related Defect Centers in Silicon and Similarities to the Oxygen Donor, *Proc. 1980 Annual Meeting of the Materials Research Soc.*, Boston, Massachusetts, November 16-20, 1980.

*Lehovec, K., and Fedotowsky, A., Solar Cell Mathematical Analysis and Computer Simulation, NBS-GCR-80-285.

*Lin, J. F., Li, S. S., Linares, L. C., and Teng, K. W., Theoretical Analysis of Hall Factor and Hall Mobility in p-Type Silicon, *Solid-State Electronics.*

*Linares, L. C., and Li, S. S., An Improved Model for Analyzing Hole Mobility and Resistivity in *p*-Type Silicon Doped with Boron, Gallium, and Indium, *J. Electrochem. Soc.*

Linholm, L. W., Mattis, R. L., Frisch, R. C., and Reeves, C. P., Characterizing and Analyzing Critical Integrated Circuit Process Parameters, *Semiconductor Silicon/1981* (Electrochemical Society, 1981).

Linholm, L. W., *Semiconductor Measurement Technology:* The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control, NBS Spec. Publ. 400-66.

Lowney, J. R., Kahn, A. H., Blue, J. L., and Wilson, C. L., Disappearance of Impurity Levels in Silicon and Germanium Due to Screening, *J. Appl. Phys.*

Mitchell, M. A., and Linholm, L. W., *Semiconductor Measurement Technology:* Test Patterns NBS-28 and NBS-28A: Random Fault Interconnect Step Coverage and Other Structures, NBS Spec. Publ. 400-65.

Ruthberg, S., Graphical Solution for the Back Pressurization Method of Hermetic Test, *IEEE Trans. Components, Hybrids, and Manufacturing Tech.*

Sawyer, D. E., Kessler, H. K., Russell, T. J., Lankford, W. F., and Schafft, H. A., Measurement Techniques for Solar Cells, Annual Report, December 15, 1978 to December 14, 1979, NBSIR 80-2181.

Scace, R. I., Semiconductor Technology for the Non-Technologist, NBSIR 81-2197.

Schafft, H. A., Measurement Development Needs for Photovoltaics and Recommended Responses, NBSIR 80-2126.

*Schwartz, S. A., Helms, C. R., Spicer, W. E., and Taylor, N. J., *Semiconductor Measurement Technology:* The Capabilities and Limitations of Auger Sputter Profiling for Studies of Semiconductors, NBS Spec. Publ. 400-67.

Thurber, W. R., Liu, Y. M., Mattis, R. L., and Filliben, J. J., *Semiconductor Measurement Technology:* The Relationship Between Resistivity and Dopant Density for Phosphorus- and Boron-Doped Silicon, NBS Spec. Publ. 400-64.

Wilson, C. L., and Blue, J. L., Semiconductor Device Simulation, *Proc. Conf. Elliptic Problem Solvers*, Sante Fe, New Mexico, June 30-July 2, 1980.

*Reports of contract research.

NBS-114A (REV. 2-8C)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET (See instructions)	1. PUBLICATION OR REPORT NO. NBSIR-81-2230	2. Performing Organ. Report No.	3. Publication Date March 1981

4. TITLE AND SUBTITLE

Semiconductor Technology Program - Progress Briefs

5. AUTHOR(S)

W. M. Bullis, Editor

6. PERFORMING ORGANIZATION (If joint or other than NBS, see instructions)

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234

7. Contract/Grant No.
See item 10

8. Type of Report & Period Covered
Interim
Oct - Dec 1980

9. SPONSORING ORGANIZATION NAME AND COMPLETE ADDRESS (Street, City, State, ZIP)

ARPA, Arlington, VA 22209; NBS, Washington, DC 20234; Dept. of Energy, Division of Electric Energy Systems, Washington, DC 20545; DNA, Attn: Comp-3, Washington, DC 20305; C. S. Draper Laboratory, Cambridge, MA 02139; NAVAIR, Arlington, VA 20360; AFWAL, Wright-Patterson AFB, OH 45433; Army ETDL, Ft. Monmouth, NJ 07703; NWSC, Crane, IN 47522; SERI, Golden, CO 80401; NAC, Indianapolis, IN 46218; NASA-Lewis Research Center, Cleveland, OH 44135; ONR, Arlington, VA 22217; NOSC, San Diego, CA 92152.

10. SUPPLEMENTARY NOTES

ARPA Order 3882; Dept. of Energy, Interagency Agreement EA-77-A01-6010, Task Order A021-EES; DNA IACRO 81-820, Subtask No. X99QAXVB202; C. S. Draper Laboratory, P.O. DL-H-182632 (Navy contract N 00030-78-C-0100); AFWAL and Army ETDL, FY 117580-N3140; NWSC, P.O. N0016481WR30019; SERI, DS-0-9313; NAC, P.O. N0016380MP00001; NASA-Lewis, C-32818-D, Modification #1; ONR, N00014-80-F-0046; NOSC, MIPR N6600180MP00017.

Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Emphasis is placed on silicon and silicon-based devices. Highlighted activities include an analysis of the cross-bridge sheet resistance test structure, observations of laser-induced patterns on semiconductor surfaces, a technique for analysis of data from test structures on process validation wafers, and advances in optical measurements of linewidth on wafers. Brief descriptions of upcoming linewidth measurement seminars and the second moisture measurement workshop are also given. In addition, recent publications and publications in press are listed. The report is not meant to be exhaustive; contacts for obtaining further information are listed.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

13. AVAILABILITY

[X] Unlimited
[ ] For Official Distribution. Do Not Release to NTIS
[ ] Order From Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.
[X] Order From National Technical Information Service (NTIS), Springfield, VA. 22161

14. NO. OF PRINTED PAGES
11

15. Price

USCOMM-DC 8043-P80

U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, *Secretary*
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Director*


DATE
ILME