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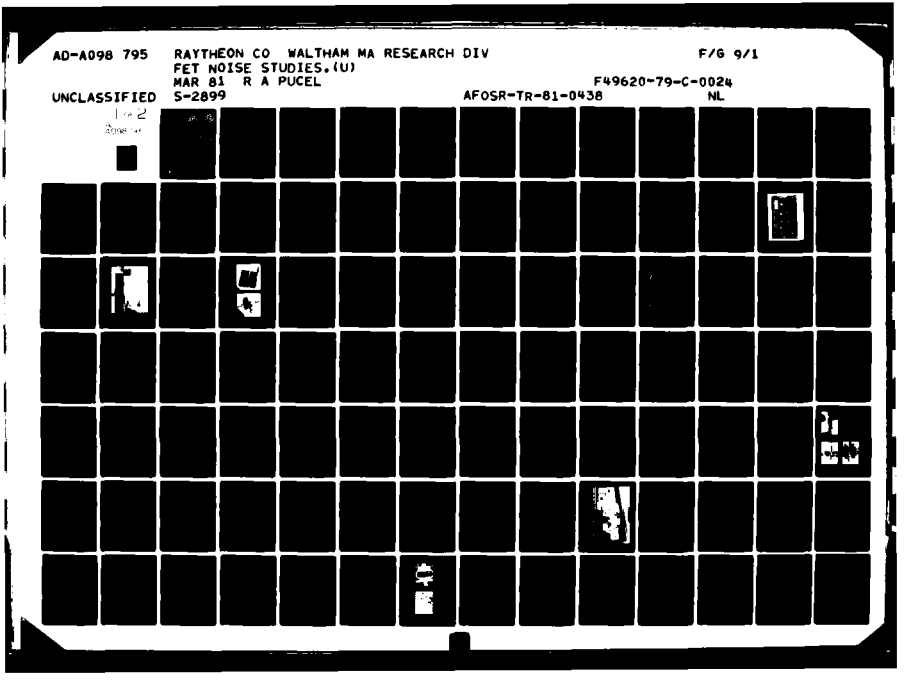

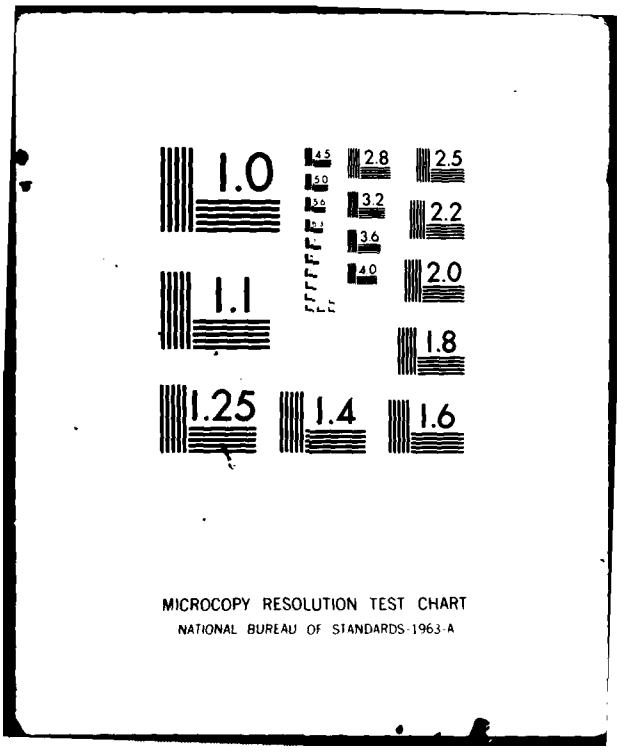
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The GaAs FET oscillator is an alternative device for voltage-controlled oscillator (VCO) applications because of its inherent wide-band electronic tunability, the variety of operating modes possible such as common source, common gate, etc., and the ease of circuit design. However, it has one major drawback, namely, its high near-carrier 1/f noise which makes it unsuitable for many applications, such as radar systems. This report describes the progress made during the report period in

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understanding the physical mechanisms responsible for this noise.

During this period, an extensive experimental study was made of the 1/f noise properties of a variety of oscillators constructed of FET chips fabricated under controlled conditions. Using in-house grown epitaxial wafers, FET's were fabricated from both buffered and unbuffered active layers, with and without epitaxially grown contact layers, and with and without surface passivation.

The experimental results show a good correlation between the trap-generated 1/f baseband noise and the near-carrier 1/f FM noise. The primary sources of the noise are presumed to be either deep traps within the depletion layer under the gate or surface states at the gate-semiconductor interface, probably the latter.

An improvement of the order of 10 dB in the near carrier FM noise level is obtained when a buffer layer separates the active layer from the substrate.

Optical experiments indicated an electron trap level approximately 0.41 eV below the conduction band.

A noise model was devised to explain the modulation process for upconverting baseband 1/f noise to the carrier band by depletion layer modulation.

A large-signal model of the FET is proposed. With the help of this model, the signal performance of an FET in a practical oscillator circuit can be predicted.

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1.0 INTRODUCTION

The performance of the voltage-controlled oscillator (VCO) is critical to the success of many radar systems, especially electronic countermeasure systems. Until recently, the only viable solid-state sources were the bipolar transistor at the lower microwave frequencies (L- to S-bands) and the Gunn and IMPATT diodes at higher frequencies.

In recent years, however, the gallium arsenide field-effect transistor (GaAs FET) has demonstrated its superiority as a low-noise amplifying element at C-band and above. The intrinsic noise mechanisms responsible for its extremely good noise performance are well understood, and have been discussed by workers at this laboratory and elsewhere.[1]

There is thus a growing interest in the use of FETs as wide-band voltage-controlled oscillators. Starting from the early work reported by this laboratory,[2] numerous papers have been published on experimental results obtained with FET oscillators.[3] It is now evident that octave-tuned GaAs FET oscillators, operating up to 20 GHz, with usable power output, are realizable.

The GaAs FET has one major drawback which makes it unacceptable for many radar systems applications, namely, its rather high level of near-carrier ("excess") 1/f noise, especially in the FM spectrum. In all cases where oscillator noise spectra have been reported, unless extreme measures are invoked (such as the use of temperature-compensated high-K dielectric cavities for frequency stabilization) the near-carrier noise level of GaAs FETs has been higher than that for comparable Gunn and avalanche diode oscillators.[2,3,4] Reducing the noise level of the FET oscillator is highly desirable, because this device has many attractive features: its inherent wide-band performance; the variety of its possible operating modes, such as grounded source and grounded gate; and its ease of design.

The need for reduction of the 1/f noise is becoming evident in another important application of FETs, namely microwave monolithic circuits. Here, ultra-broadband monolithic amplifiers ($\simeq$ dc-to-microwave) are exhibiting very poor noise figures at the lower end of the band, principally because of 1/f noise.[5]

If the origin of this excess noise can be identified and either eliminated or reduced, we believe that FETs can become important candidates for low-noise VCOs and mixers and low-frequency monolithic amplifiers. The availability of low-noise devices would open the possibility of constructing low-noise front ends in monolithic form, using FETs as preamplifiers, oscillators, and mixers.

The purpose of the research summarized in this report was to obtain a better understanding of excess noise in a GaAs FET, an understanding from which we might develop the means to reduce this noise to an acceptable level.

The specific objectives of this research were to

1. measure the microwave spectra and baseband spectra of FET oscillators;
2. identify the various noise contributions, with material and device parameters;
3. correlate the observed spectra with the models developed; and
4. develop a large signal model and a noise model of the FET oscillator.

During the period of this research, an extensive experimental study was made of the 1/f noise properties of a variety of oscillators constructed of FET chips fabricated under controlled conditions. Using in-house grown epitaxial wafers, we made FETs from both buffered and unbuffered active layers, with and without epitaxially grown contact layers, and with and without surface passivation. We studied extensively the dependence of the 1/f

noise on temperature, bias operating conditions, optical illumination, and circuit factors.

Our experimental results show a good correlation between the trap-generated 1/f baseband noise and the near-carrier 1/f FM noise. We conclude, tentatively, that the primary source of the noise is either deep traps within the depletion layer under the gate or surface states at the gate-semiconductor interface; we consider the latter more probable.

An outgrowth of this phase of the research was the derivation of a noise model which explains the modulation process by which the low-frequency baseband noise is upconverted to the rf band as near-carrier 1/f noise.

Phase-locking experiments have shown that the classic oscillator noise theory is obeyed by FET oscillators. However, our results indicate that some refinements in the theory are in order.

We have shown that the 1/f noise level is at least an order of magnitude higher than the white noise level for frequencies within a MHz from the carrier, even if the noise figure is as high as 6 dB. This confirms the importance of reducing the 1/f noise mechanism of FET oscillators to capitalize on the low level of thermal noise inherent in MESFETs.

Our research has also demonstrated that the near-carrier FM noise level is reduced by about 10 dB when a buffer layer separates the active layer from the substrate.

Finally, we derived a nonlinear model of the FET by which the signal generating performance of an actual FET oscillator circuit can be predicted. This model agrees well with experimental results.

2.0 THEORY

2.1 Introduction

2.1.1 Nonlinear model of FET oscillator

All existing theories of electronic oscillators, whether they be one-port such as avalanche diodes, or two-port devices with feedback, such as transistors or tube oscillators, reduce the problem of analysis to that of a one-port admittance (or impedance) with a negative real part.[6-8] The general treatment of a two-port oscillator as a nonlinear transducer is a difficult one, and has not been solved;[9] we shall not propose to do so.

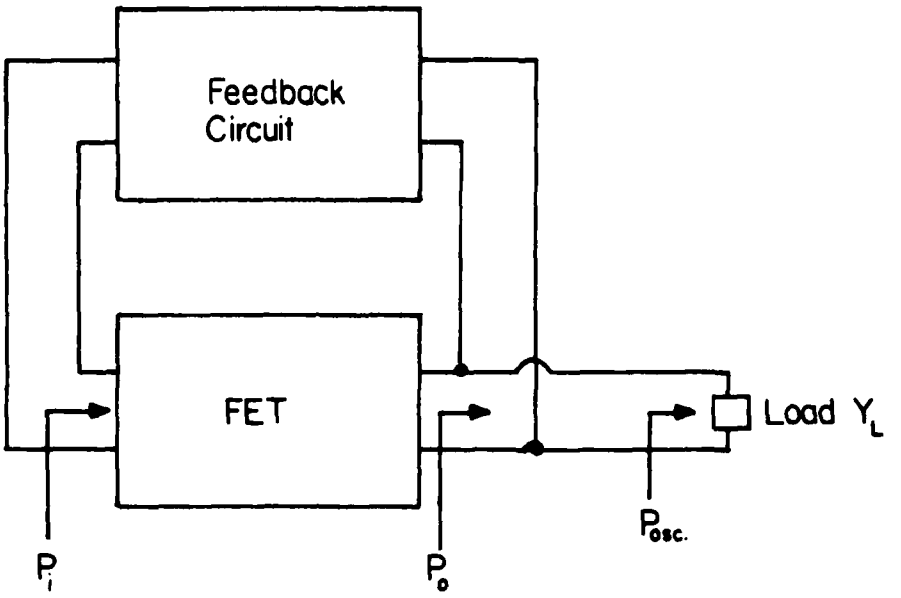
We will treat the FET, with its associated feedback network, as a "black box" which presents a signal-dependent admittance with a negative real part to the load. This representation is shown in Fig. 1(a). The reduced, one-port equivalent circuit, looking from the load terminals, is illustrated in Fig. 1(b). Shown is a nonlinear device admittance Y, a function of signal amplitude A and frequency ω with a negative real part in shunt with the frequency-dependent load Y_L and a conductance G_c representing circuit and feedback losses.

For stable oscillations, the negative real part of the device admittance must be a decreasing function of the signal amplitude A, where A may represent some current or voltage signal. (In the representation of Fig. 1, A represents the node voltage.) A necessary condition for oscillation is that

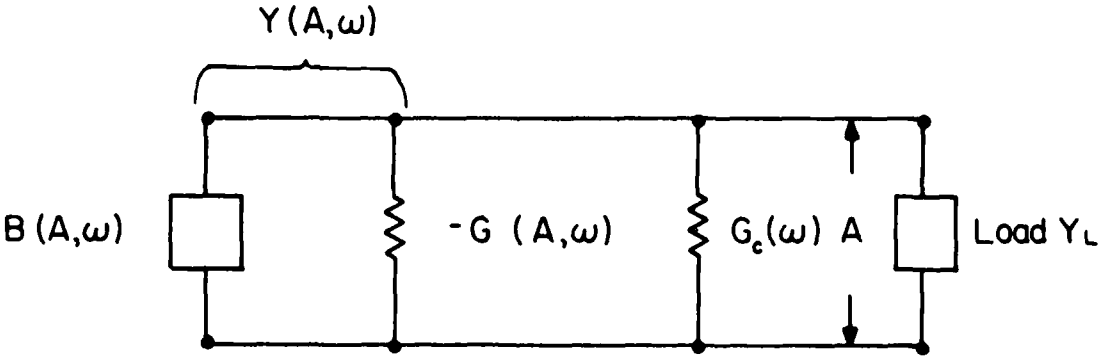
$$G_c(\omega_o) + Y(A_o, \omega_o) + Y_L(\omega_o) = 0 \qquad (1)$$

at some frequency $\omega = \omega_o$, where $A = A_o$ is the resulting oscillation amplitude. This condition establishes the frequency and amplitude of oscillation for any prescribed load. The power delivered to the load will be maximum for some "optimum" load.

For single-state oscillators (one oscillation amplitude and frequency for any prescribed load), it is usually possible to approximate the nonlinear dependence of the device admittance as a power series of the oscillation amplitude. The



(a) Two-Port FET Oscillator with feedback



(b) One-Port Representation of FET Oscillator with losses G_c

Figure 1. Large-Signal Model of FET Oscillator.

simplest representation which leads to stable oscillations is the so-called van der Pol approximation,[6]

$$-G(A,\omega) = \alpha A - \beta A^3 \qquad (2)$$

where G is considered frequency-independent over a narrow band and α and β are properties of the device. Most existing oscillator noise theories are based on this approximation. This cubic approximation also can be applied to the FET oscillator because the oscillator can be considered as a power amplifier in which a portion of the output is fed back to the input to produce a negative input conductance which cancels the input circuit losses and loading, and, hence, leads to sustained oscillations.

The cubic approximation, though convenient analytically, is oversimplified in that it only considers cubic nonlinearities and ignores any nonlinear reactive elements in the active device. Neither of these conditions is satisfied for a microwave FET.

We have developed in Sec. 6.0 a nonlinear model of the FET which overcomes these restrictions and which represents the nonlinear properties of the FET not only at microwave frequencies but also in the dc condition. This model agrees well with dc and rf measurements.

The predominant sources of nonlinearity in the FET, relevant to oscillator analysis, are the transconductance g_m and the source-gate capacitance C_{sg}. Thus, in the representation of Fig. 1, g_m contributes to $-G(A,\omega)$ and C_{sg} contributes to $B(A,\omega)$.

2.1.2 Noise model

2.1.2.1 Background noise

There are two general categories of noise mechanisms in an FET: intrinsic sources, i.e., noise associated with the FET operation itself, and extrinsic noise, i.e., noise generated by sources not essential to FET operation.

The intrinsic sources are thermal noise in the channel and diffusion noise generated at high channel fields in the velocity saturated zone. These noise sources produce a flat (white) spectrum. Avalanche noise, possibly produced at very high drain voltages, also produces white noise. Noise produced by parasitic resistance, one of the extrinsic noise sources, is also flat.

These white noise sources, because they produce spectra which overlap the carrier frequency, are called background sources. This noise interacts directly with the carrier to produce AM and FM noise sidebands. No frequency conversion of the noise spectra takes place. That is to say, the background noise sources, collectively considered as a "small signal", can be represented as a voltage or current source (in the case of Fig. 1, a current source) driving the already established large-signal equivalent circuit. This is the customary way of treating background noise in oscillators.[10-12] Figure 2 represents the equivalent circuit for the background noise. The noise is represented by the current generator i_b.

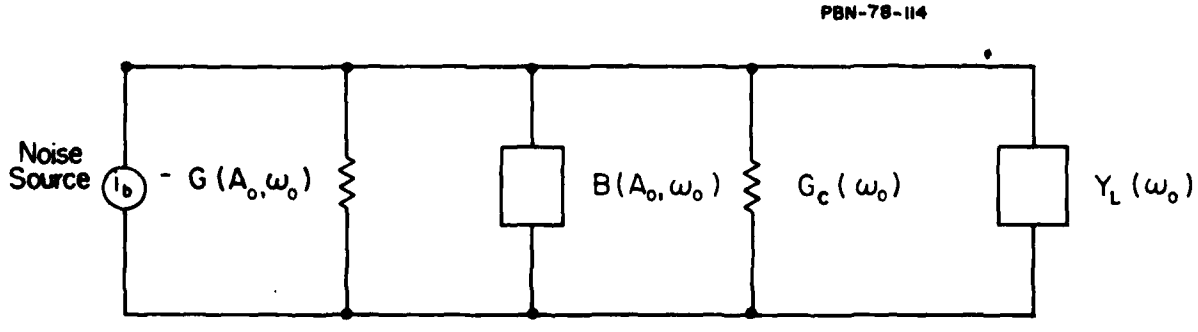


Figure 2. Noise Equivalent Circuit for FET Oscillator.

The major problem in handling background noise in an FET oscillator is to obtain a suitable representation for the noise source amplitude i_b in terms of the physical white noise sources. As a starting point, one may use the background noise model for the FET amplifier, such as developed at this laboratory.[1] Then by taking into account feedback in the oscillator, and averaging the noise sources over an oscillator cycle, if necessary, the background noise contribution

can be computed in the traditional way. Knowing the background noise contribution, one can determine its contribution to the measured oscillator noise or vice versa.

For example, if the spectral density of the available noise power associated with the background current noise source is denoted by N_b, then the rms frequency deviation Δf_{rms}, arising from a band B of this white noise, is given by[10-12]

$$\Delta f_{rms} = \frac{f_o}{Q_L}\sqrt{\frac{N_b B}{P_o}} \qquad (3a)$$

where f_o is the oscillation frequency, Q_L is the loaded Q of the oscillator circuit, and P_o the carrier or oscillator power. The corresponding (double-sideband) noise/carrier ratio at the frequency offset f_m is [11-13]

$$\left(\frac{N}{C}\right)_{FM} \approx \frac{N_b B}{P_o} \quad \frac{1}{(f_m Q_L/f_o)^2} \qquad (f_m > 0) \qquad (3b)$$

This relationship ties in the measured Δf_{rms} (associated with white noise) to the equivalent noise source power N_b, which in turn is linked with the physical sources of noise.

Likewise the AM noise spectra arising from background sources can be related to the double side-band noise-to-carrier ratio by[11-13]

$$\left(\frac{N}{C}\right)_{AM} = \frac{N_b B}{P_o} \quad \frac{1}{1+(f_m Q_L/f_o)^2} \, . \qquad (4)$$

Background noise in an FET oscillator, as we shall show in Sec. 5, is only observable far from the carrier, around 10 MHz removed. It is low compared with other oscillators, such as avalanche and Gunn diodes. It is dominated, near the carrier, by 1/f-like noise, which is to be discussed next.

2.1.2.2 Baseband noise

Turning now to the portion of extrinsic noise which we called "excess noise," we include in this category all sources of noise associated with material defects or introduced by other factors in the device technology. These noise contributions usually can be correlated with traps (electron and/or hole) which are either within the semiconductor, at the interface between the active layer and the substrate, or at the exposed surface (between electrodes or at the electrode-semiconductor interfaces). This trap-related noise originates at the base band and is usually of the form

$$N_e = \frac{AI^{\alpha}}{f^{\beta}} \tag{5}$$

over a finite frequency range,[14-17] where I is the bias current, $\alpha \sim 2$, and $\beta \sim 1\text{-}2$, depending on the distribution and nature of the traps. For example, for a single-level trap distributed uniformly throughout the bulk, one finds $\alpha = 2$, $\beta = 2$, i.e., a base-band contribution falling off with frequency as $1/\omega^2$ and quadratically dependent on bias current. On the other hand, for a set of traps with a uniform distribution of trapping times, Van der Ziel[16] shows that $\beta = 1$, leading to a 1/f spectrum over a finite frequency band. A 1/f spectrum can also be produced by a continuum of states with a uniform distribution of energy levels. The situation often can be approximated by surface states. We shall make use of these models for 1/f noise in Sec. 5.6.

Base-band noise can manifest itself as an rf spectrum only by a modulation or frequency up-conversation or "mixing" process involving the nonlinearity of the device. Therefore, oscillator noise contributed by upconverted base-band noise is often called "modulation noise." Since the frequencies of the noise components are at base band (and hence much lower than the large-signal carrier frequency), base-band noise manifests itself as a slow, random variation of the nonlinear elements of the oscillator — in the case of Fig. 1(b), the real and imaginary parts of the device admittance.

This phenomenological treatment of the 1/f noise, as it pertains to the near-carrier noise spectra of oscillators, is quite successful, and amenable to

analytic treatment.[12,13] Thus if $\langle(\Delta Y)^2\rangle$ is the mean square fluctuation of the device admittance produced by modulation noise,* an "equivalent" modulation noise current source, i_m of mean square value $|A_o|^2 \langle(\Delta Y)^2\rangle$ can be added in shunt with the background noise generator i_b, where A_o is the amplitude of the carrier.[12]

In the special case where the fluctations in -G and B are uncorrelated, the modulation noise contribution can be added very simply to the background noise contribution in Eqs. (3) and (4). In this case the fluctuation in G leads to AM noise and the fluctuation in B leads to FM noise. For example, Eq. (3a) becomes

$$\Delta f_{rms} = \frac{f_o}{Q_L} \sqrt{\frac{(N_b+N_{mb})B}{P_o}} \tag{6}$$

and Eq. (4) becomes

$$\left(\frac{N}{C}\right)_{AM} = \frac{(N_b+N_{mg})B}{P_o} \quad \frac{1}{1+(f_m Q_L/f_o)^2} \tag{7}$$

where N_{mg} is the available noise power associated with the noise modulation of -G and N_{mb} is the available noise power associated with the modulation of B. Both N_{mg} and N_{mb} will exhibit a spectrum corresponding to the form given by Eq. (5).

Equations (6) and (7) are mathematical representations of the background noise and 1/f noise mechanisms as power spectral densities, N_b, N_{mb}, N_{mg}. As such they are useful in that they allow one to compare these noise contributions to some reference, such as thermal source noise, kT. On the other hand, to relate the noise contributions to some specific physical course, one must identify the mechanism by which the noise is generated, and explain how it modulates the carrier.

For example, take the case of 1/f noise. To show how this manifests itself as upconverted AM and FM noise, we follow a simple model of Scherer.[18]

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* *The symbol <> represents a statistical average.*

Let P be some low-frequency device parameter whose fluctuation is suspected of producing near-carrier noise. For example, P may represent drain bias current, gate bias, gate source capacitance, etc. Suppose, in general, that both the oscillator power output and carrier frequency are affected. If $\langle(\Delta P)^2\rangle$ represents the mean-square value of the statistical fluctuation of the parameter measured at base band, in a bandwidth B at some base-band frequency f_m (by the low-frequency noise analyzer), then the corresponding AM and FM noise contributions to the near-carrier spectrum displaced by a frequency f_m from the carrier are, respectively,

$$\left(\frac{N}{C}\right)_{AM} = \frac{|S_{ap}|^2}{4P_c^2}\langle(\Delta P)^2\rangle , \tag{8}$$

$$\Delta f^2_{rms} = |S_{fp}|^2 \langle(\Delta P)^2\rangle \tag{9}$$

where S_{ap} and S_{fp} are amplitude and frequency-sensitivity factors for the parameter P given by

$$S_{ap} = \frac{\partial P_c}{\partial P} , \tag{10a}$$

$$S_{fp} = \frac{\partial f_o}{\partial P} , \tag{10b}$$

As an example of this modulation process, consider the case of surface states or bulk states under the gate electrode. A fluctuation in the occupancy of these states will result in a fluctuation of the depletion layer width, i.e., the gate capacitance. A fluctuation in the gate capacitance gives a fluctuation in the imaginary part of the device susceptance, hence of frequency, as per Eq. (9). The experimental results to be discussed in Sec. 5.3 suggest that a fluctuation process, similar to this, can indeed lead to the FM noise measured in our experiments. The detailed model will be discussed in Sec. 5.6.

3.0 EXPERIMENTAL APPROACH

3.1 Introduction

Baseband and near-carrier noise measurements were made on a 500 micron periphery FET, of a design normally used for low noise purposes. The noise was measured on devices processed in a variety of ways to be described in Sec. 4.0. Substrates from two different vendors were used.

The noise was measured as a function of operating voltages, that is, drain and gate bias, temperature, and optical illumination by white light and a monochromatic source. The baseband noise was measured on both oscillating and non-oscillating devices from approximately 100 Hz to 200 kHz. The rf oscillator noise spectra also were measured from 100 Hz to 200 kHz from the carrier, and in some cases to 10 MHz from the carrier.

3.2 Microwave Noise Measurements

Both amplitude (AM) and phase noise in the vicinity of the carrier were measured. For the rf noise measurements, we have used the direct detection scheme, thus eliminating any problems associated with L.O. frequency jitter and AM noise. This is a serious problem with heterodyne techniques, since the near-carrier noise in the L.O. sets the limiting sensitivity of the system for measurement of noise near the carrier frequency.

Since satisfactory microwave noise analyzers (as contrasted to spectrum analyzers) are not commercially available, a versatile, ultrasensitive direct detection system was designed and built for our laboratory by the Electronic Equipment Group of Raytheon's Microwave and Power Tube Division. This system incorporates features which were designed with near-carrier FET oscillator noise measurements in mind. The system is capable of measuring noise from 50 cycles off the carrier to as far as 10 MHz from the carrier in two, switchable bands. A simplified block diagram is shown in Fig. 3. This system is tunable from 8.5 to 10.5 GHz. Figure 4 is a photograph of the noise analyzer.

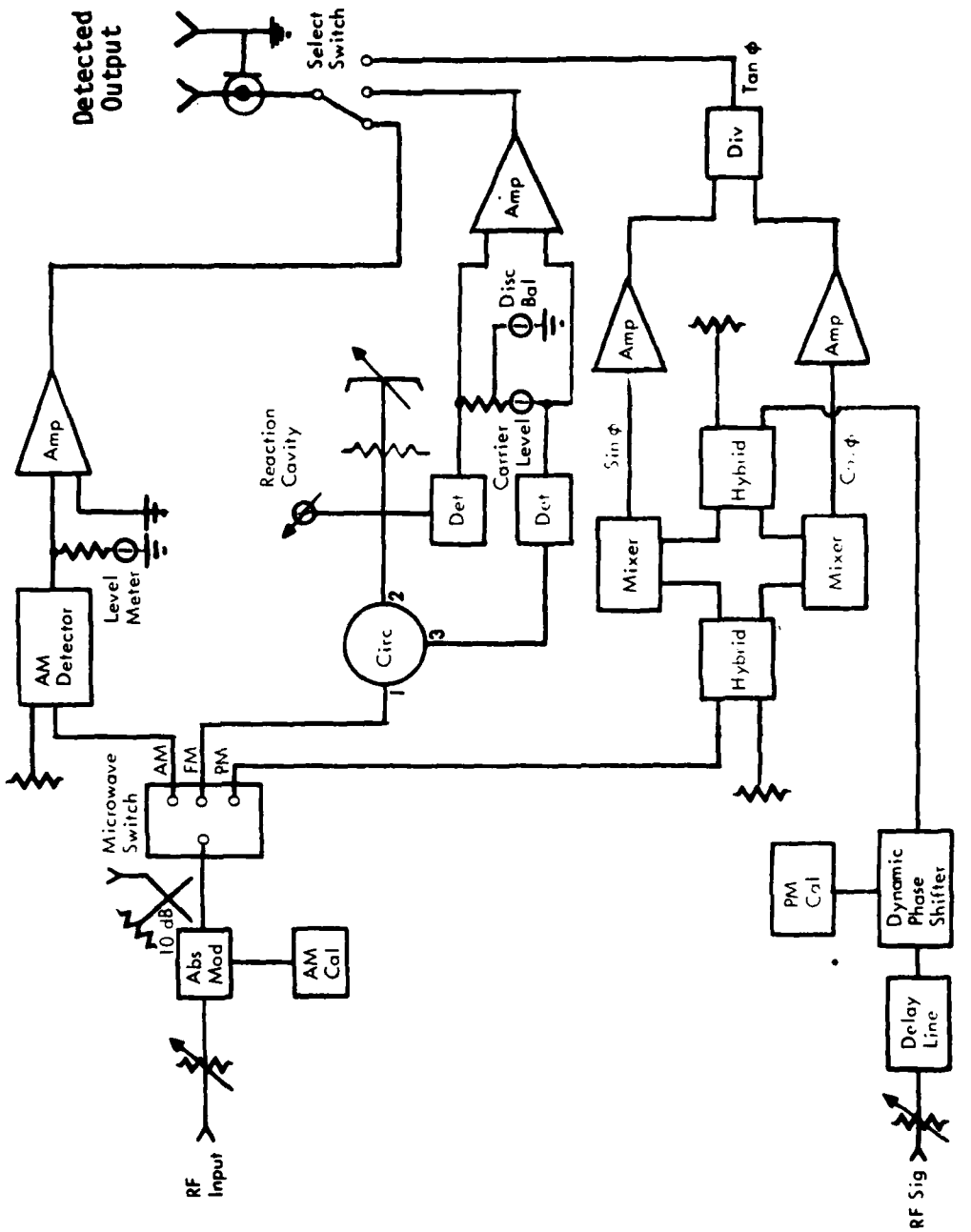


Figure 3. Block Diagram of Noise Analyzer.

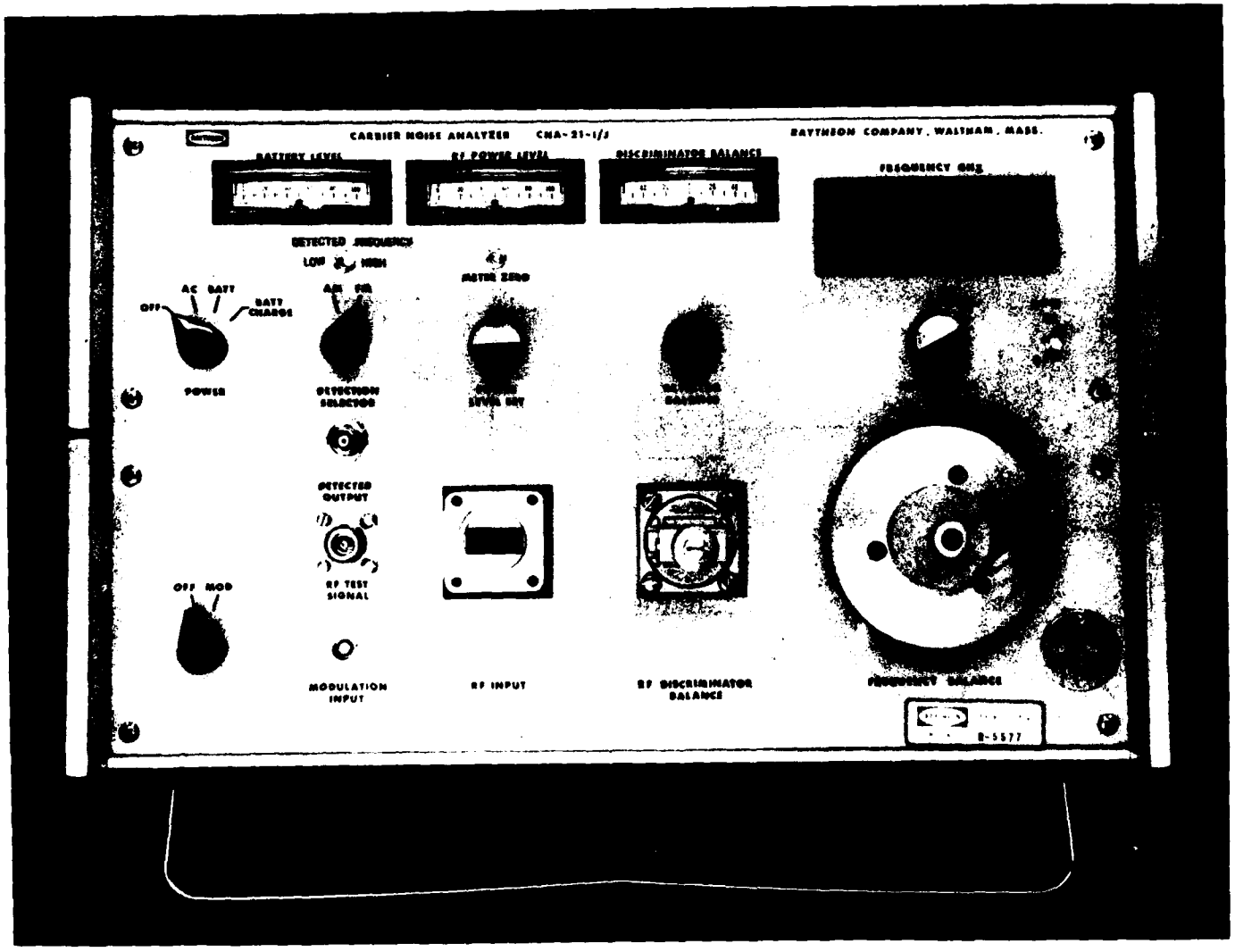


Figure 4. Noise analyzer.

The AM demodulator consists of a balanced mixer matched to operate in the linear region of its diodes for maximum sensitivity. Normal operation for linear detection is 0 to 16 dBm rf input. This sensitivity is more than adequate for testing X-band FET oscillators. For example, with a one-mW input to the system, N/C ratios as low as -150 dB in a 1 Hz bandwidth can be measured.

The FM demodulator (discriminator) is a frequency-sensitive microwave bridge. Unlike other noise measurement techniques employing carrier suppression, this system retains the carrier power. This not only results in lower input rf requirements, but makes the analyzer simpler to operate. Only two adjustments, the rf short and the microwave cavity, are used to balance the discriminator. The analyzer may be battery-operated to eliminate power-supply noise modulation.

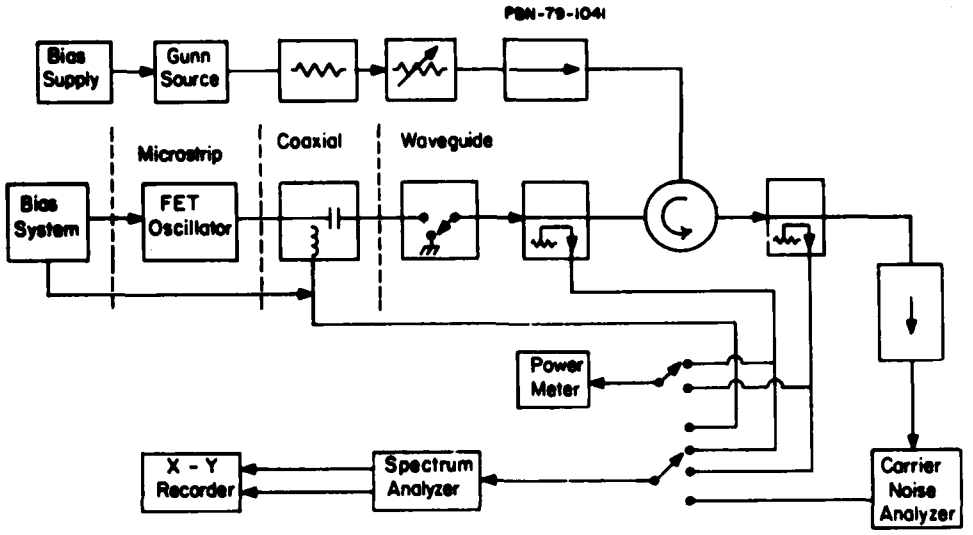
The detected output is passed to a base-band analyzer (not shown). All noise spectra can be traced on an X-Y recorder for a permanent record.

A block diagram showing the details of the microwave measurement set-up appears as Fig. 5(a). The circuit diagram of the set-up is shown in Fig. 5(b). A photograph of the test bench is shown in Fig. 6.

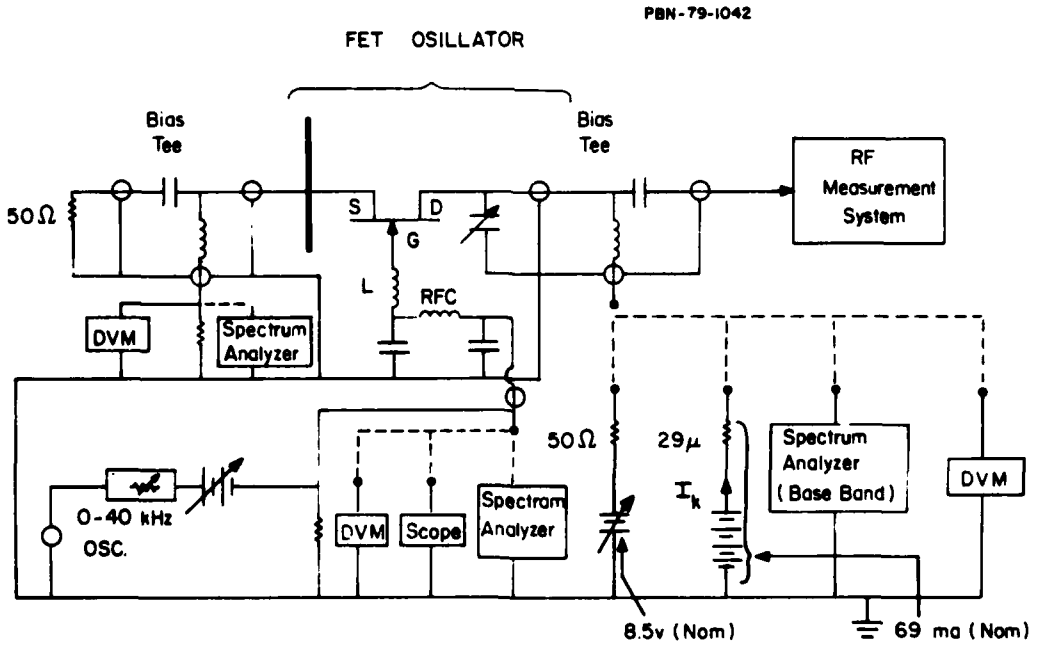
3.3 Baseband Noise Measurements

The baseband noise is measured with a baseband analyzer as a noise voltage drop across a 50-ohm resistor in the drain circuit. This is shown in Fig. 5. The noise voltage can then be converted to a drain current fluctuation. Initially, the sensing resistor was immersed in liquid nitrogen to reduce its own thermal noise contribution when measurements far from the carrier were made. However, this precaution was unnecessary in the near-carrier 1/f range, where the device noise was higher.

The noise analyzer "window" was varied from 10 Hz to 300 Hz and higher, depending on the frequency offset from the carrier and the noise level. At all times, the minimum usable noise window bandwidth was used. Unless stated otherwise, all of the data to be provided later were mathematically normalized to a 1 Hz bandwidth to provide a common basis for comparing noise levels. This



(a) Block Diagram of Oscillator Test Set-Up.



(b) Circuit Diagram of Oscillator Test Set-Up.

Figure 5. Oscillator Test System.

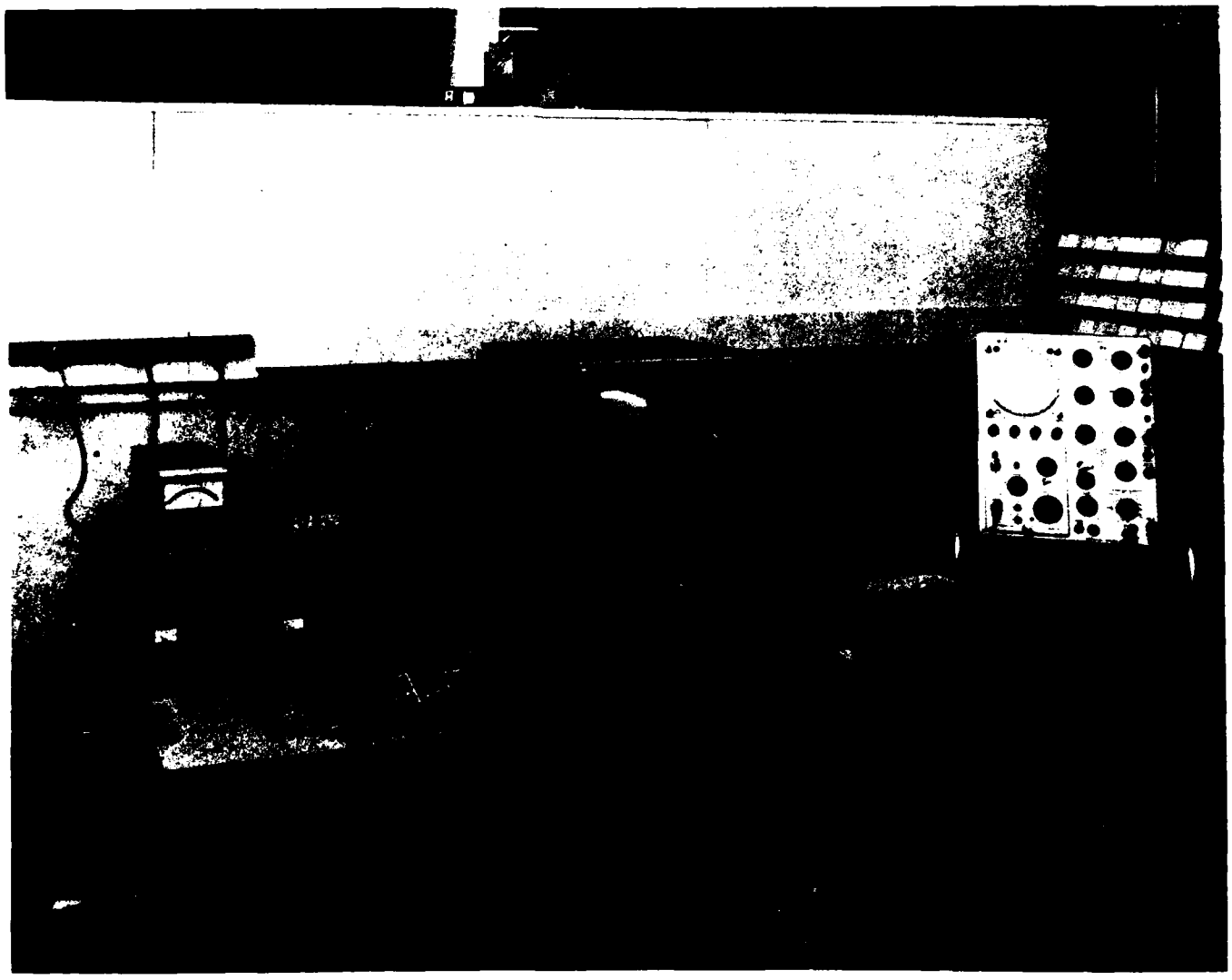


Figure 6. Photograph of Oscillator Test System.

same normalization procedure was used in the rf noise measurements.

The baseband noise was measured in both the oscillating and non-oscillating state. In the first measurements to be described (Sec. 4.2) the measurements were taken on non-oscillating FET's. In later measurements (Sec. 5.2) where quantitative comparisons are made between baseband and rf noise data, the baseband noise was measured under oscillating conditions.

3.4 FET Oscillator Circuit Configuration

A common-gate oscillator was designed for X-band noise studies. The circuit utilizes an inductance in the gate-ground arm for feedback. The circuit was designed to operate with a load approximating that for maximum power output as an amplifier. The necessary inductance value was determined by use of computer-aided techniques (COMPACT). The inductance was in the form of a 1-mil diameter wire which could be "tweaked" for fine tuning.

The oscillator circuit was printed on an alumina substrate. In addition to the rf output port connected to the drain, a coax input port was also used to connect to the source to allow injection of a synchronizing signal and for external cavity tuning and/or stabilization, when desired. The oscillator frequency and power are fine-tuned by appropriate choice of source stubs and drain capacitive tabs already on the substrate, using silver paste. Most measurements were performed on the FET oscillator, while it was oscillating. A photograph of the circuit is shown in Fig. 7(a). The circuit mounted in its holder appears in Fig. 7(b).

The bias scheme has evolved to meet requirements that the supplies, digital multimeters, oscilloscope, and spectrum analyzer may all be interchanged. Bias tees readily pass signals in the baseband frequency range. All rf ports may be used for modulation signal injection at baseband frequencies or for monitoring noise in this frequency range.

The drain circuit bias source may be selected as either constant voltage or constant current. This scheme also allows the determination of apparent g_m under oscillating conditions, as well as frequency and power output.

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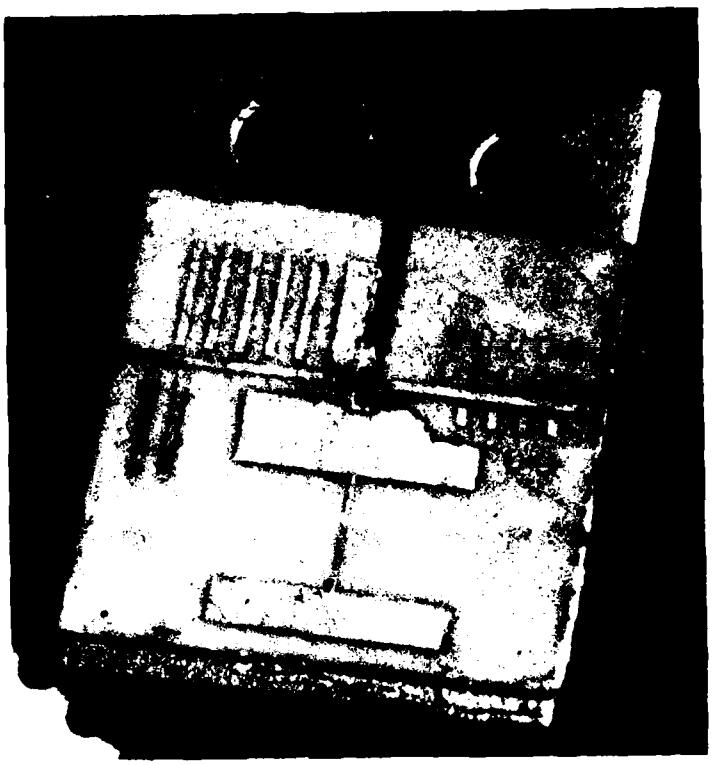

(a) Oscillator Circuit on Alumina Substrate.

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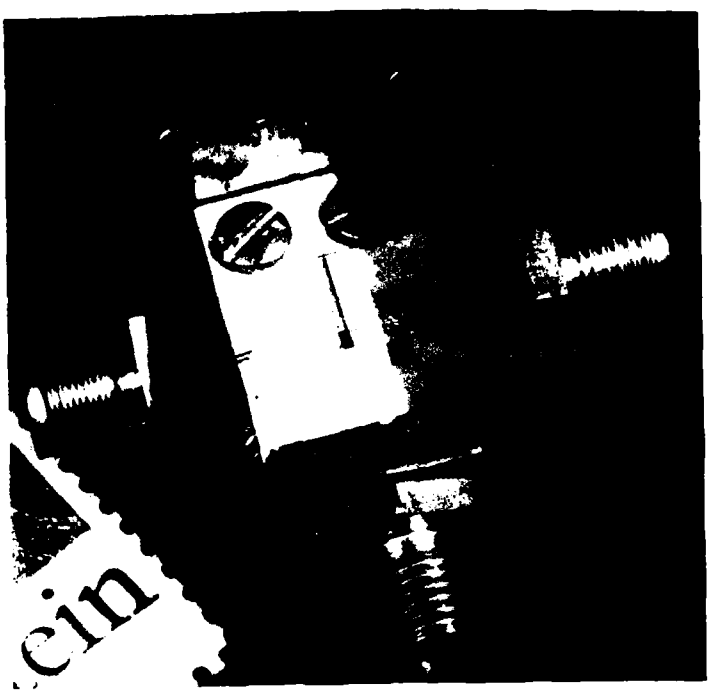


(b) Oscillator Circuit Mounted in Test Jig.

Figure 7. Oscillator Circuit.

4.0 EXPERIMENTAL RESULTS

4.1 Introduction

The first set of wafers processed were two series totalling six wafers, three obtained from Sumitomo, and three from Crystal Specialties. Each set of three wafers was processed simultaneously to minimize unintentional variations in the processing. Epitaxial layers were deposited on the substrates by the vapor phase technique. The "active" or channel layer was doped with silicon to a nominal doping density of 9×10^{16} atoms/cc, which was achieved to within ± 10 percent. One wafer of each set consisted of the following epitaxial layers:

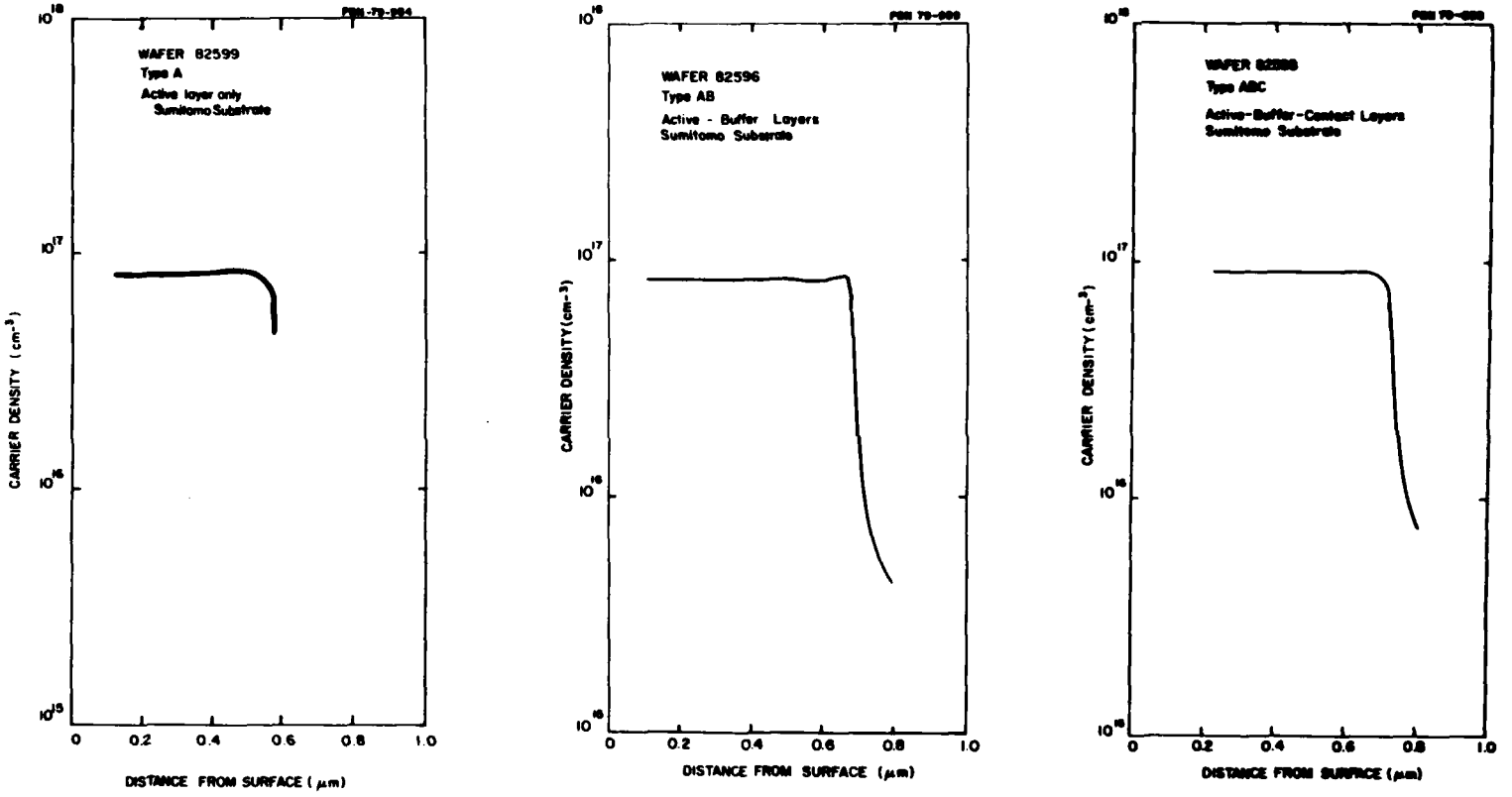
Type "A" wafer: "active" layer only
Type "AB" wafer: "active" plus buffer layers
Type "ABC" wafer: "active" plus buffer layer plus contact layer.

The buffer layers were nominally 2-2.5 μm thick, and "undoped" with an estimated carrier concentration of 5×10^{13} atoms/cc. The contact layers, also silicon doped, had carrier concentrations of 2×10^{19} atoms/cc and were 0.2 μm thick.

Figures 8(a-c) indicate the measured doping profiles for the Sumitomo substrates. Figures 9(a-c) show the doping profiles for the Crystal Specialties substrates.

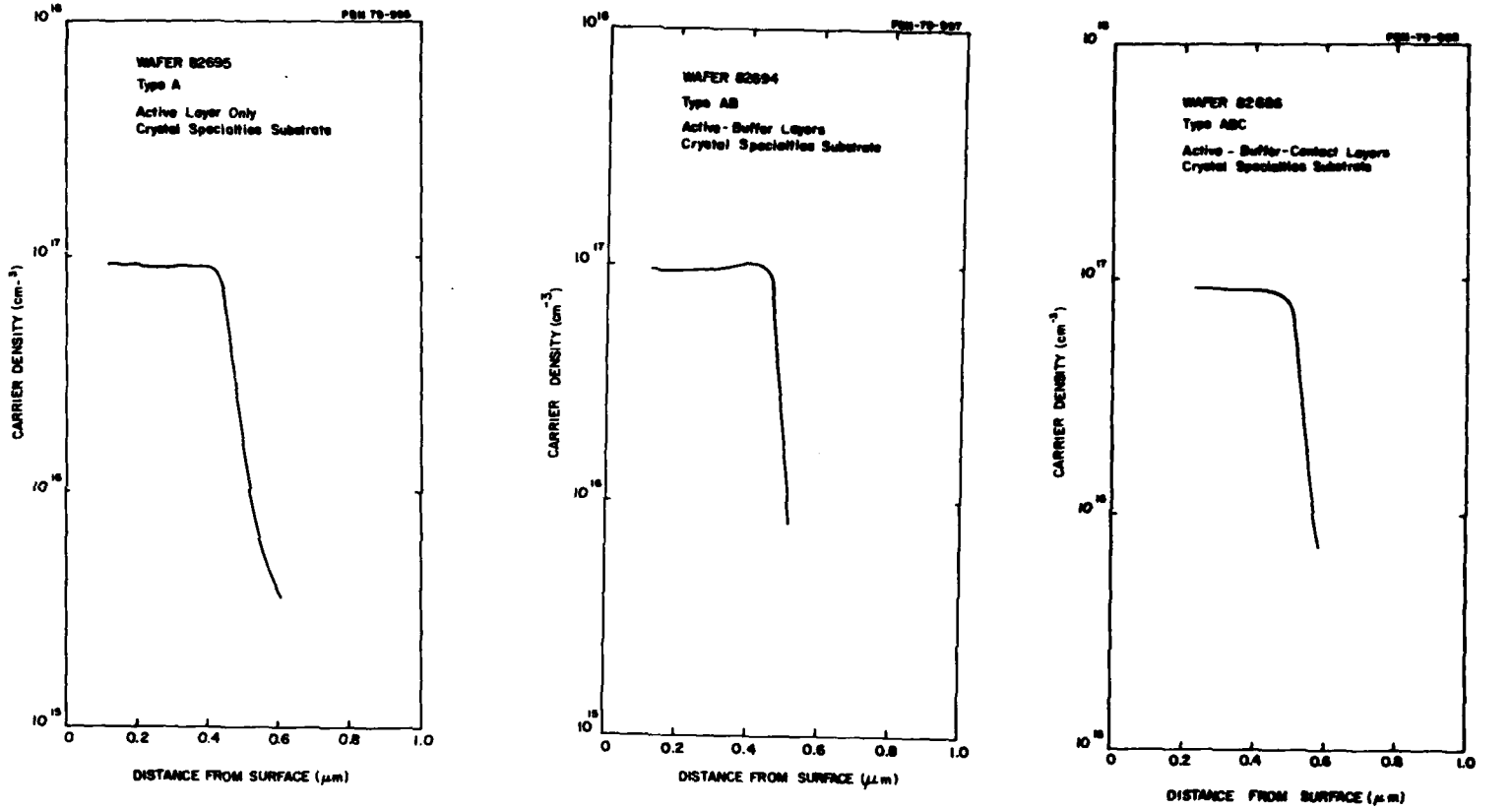
The active layers were grown to between 0.4-0.6 μm thick, then chemically etched down to a thickness which would yield a nominal I_{dss} of 120-150 mA, corresponding to a pinchoff voltage in the 4-4.5 V range. Each wafer was divided into quarters, and processed somewhat differently.

Figure 10 illustrates the scheme used: To test the effect of surface passivation, the left half of each wafer, indicated by the designations, LT (left top) and LB (left bottom) were unpassivated, whereas the right half quarters, RT (right top) and RB (right bottom) were covered with SiO_x which was evaporated to a thickness of 4000 Å. The top half used a shallow gate trench with



(a) Active layer only *(b) Active-buffer layers* *(c) Active-buffer-contact layers*

Figure 8. Doping Profiles on Sumitomo Substrates.



(a) Active Layer Only *(b) Active-Buffer Layers* *(c) Active-Buffer-Contact Layers*

Figure 9. Doping Profiles on Crystal Specialties Substrates.

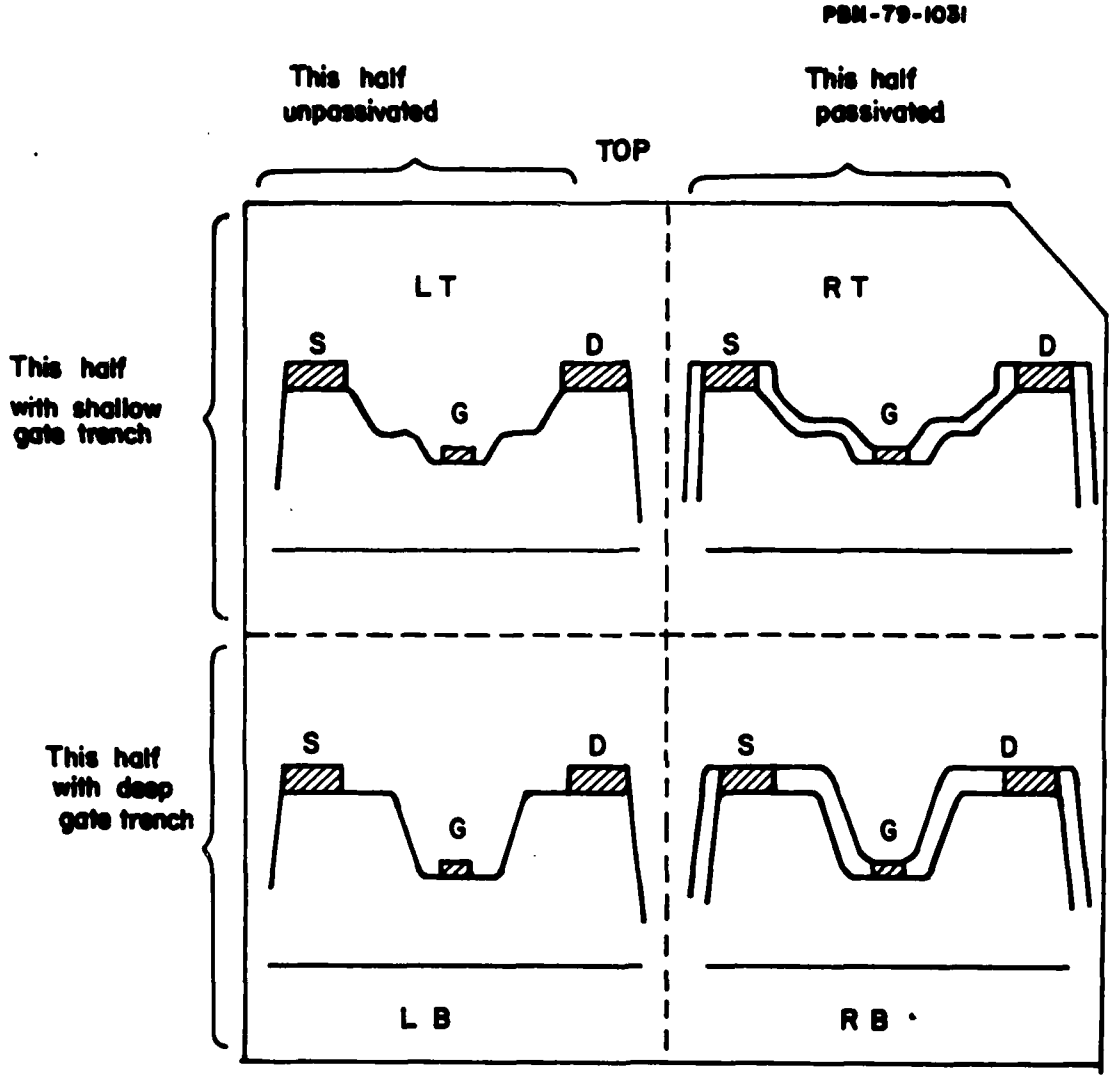


Figure 10. Division of Wafer Into Quarters for Process Variations.

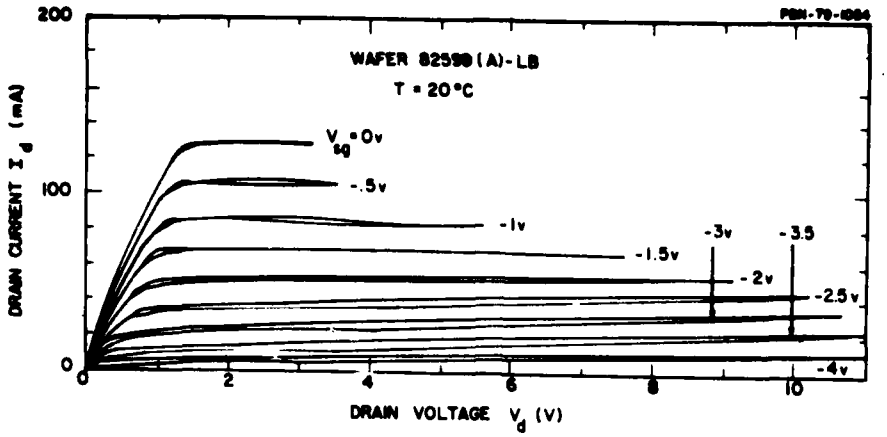
a double shoulder surface. This allowed a recessed gate technology, but still presented an open semiconductor surface near (approximately 2000 Å away from) the channel, to allow us to study the effect of possible surface states. The bottom half was processed with deep gate trenches and with the source-drain contact areas removed the maximum possible distance from the gate channel. Thus in all, there were twelve "variants" for each set of wafers. Except for the deliberate variations introduced above, care was taken to minimize variations in all of the other processing steps needed to fabricate the devices. The chips were tested unpackaged, and were mounted directly into the microstrip circuit holder, with wire bonds to the gate, source, and drain pads.

Figures 11(a-c) and 12(a-b) indicate the uniformity of the I-V characteristics obtained from the devices fabricated on Sumitomo and Crystal Specialties substrates, respectively. Shown are characteristics obtained from each type of wafer, from various quarters of the wafer (as indicated). (No I-V characteristic is shown for the wafer 82686, the type ABC wafer, Crystal Specialties substrate, because of a mishap in the processing.)

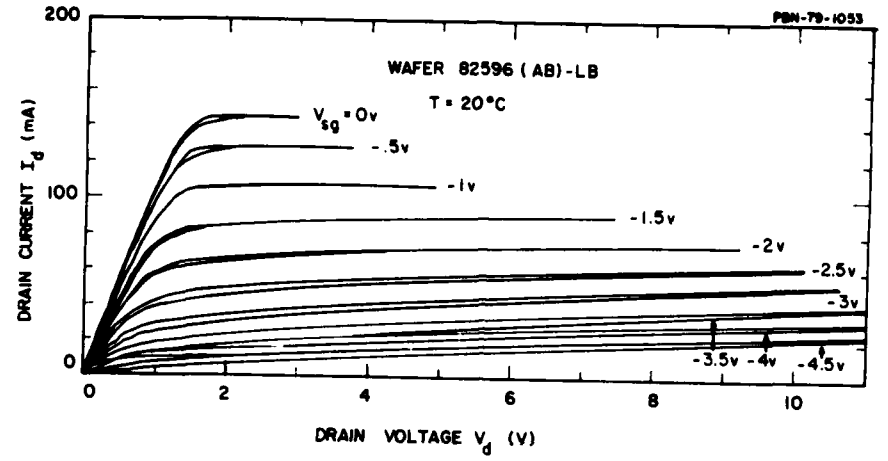
We summarize in Tables I and II the various wafer numbers, type designations, and processing variations discussed above. These tables can be used later, for easy reference, when the experimental results are discussed. In the ensuing discussions we shall refer to the different combinations of layers and processing variants by a designation illustrated by this example: Wafer 82695(A) - LB, that is, Wafer 82695, which has an active layer only, and is from the left-bottom quarter of the wafer.

Our first set of noise measurements, both baseband and rf, were made on one device from each quarter wafer (where possible). The purpose was to obtain an idea which of the various parameters that were varied had an effect on the noise and which did not. From these would be selected certain choices for further detailed studies.

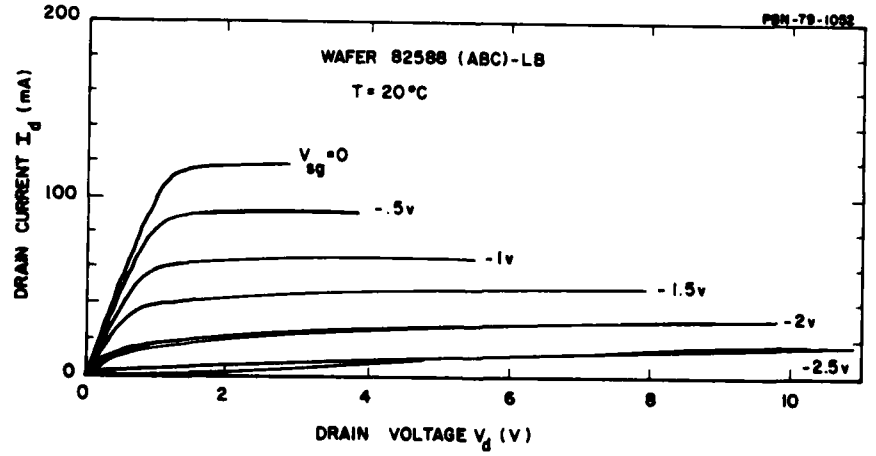
The baseband noise measurements were taken over two frequency bands, from 100 Hz to 1 kHz, and from 1 kHz to 100 kHz. The noise analyzer "window" bandwidths used in the two bands were 10 Hz and 300 Hz, respectively. All



(a) Type A Wafer.

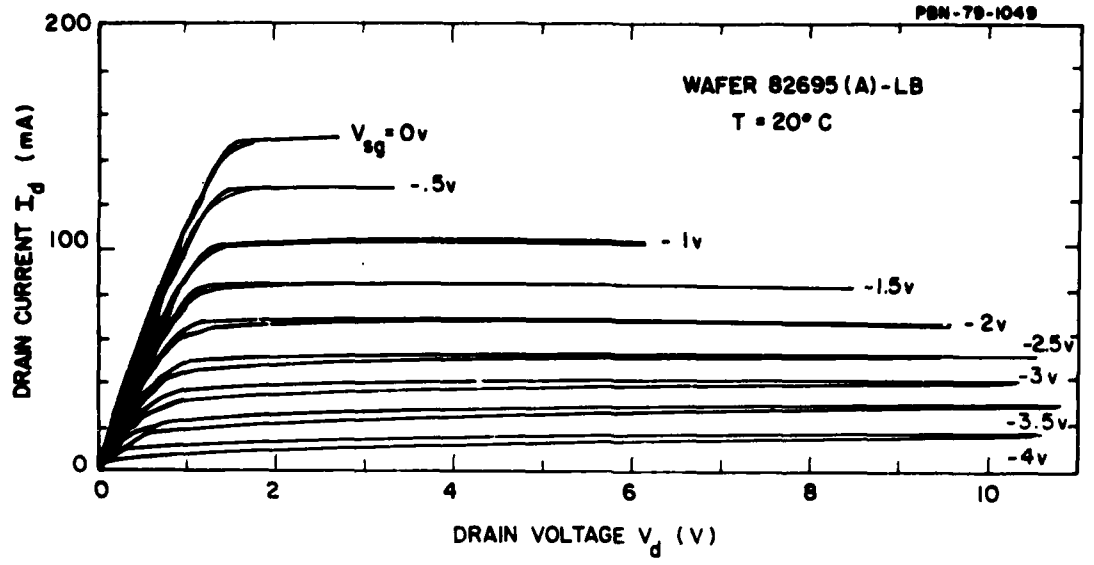


(b) Type AB Wafer.

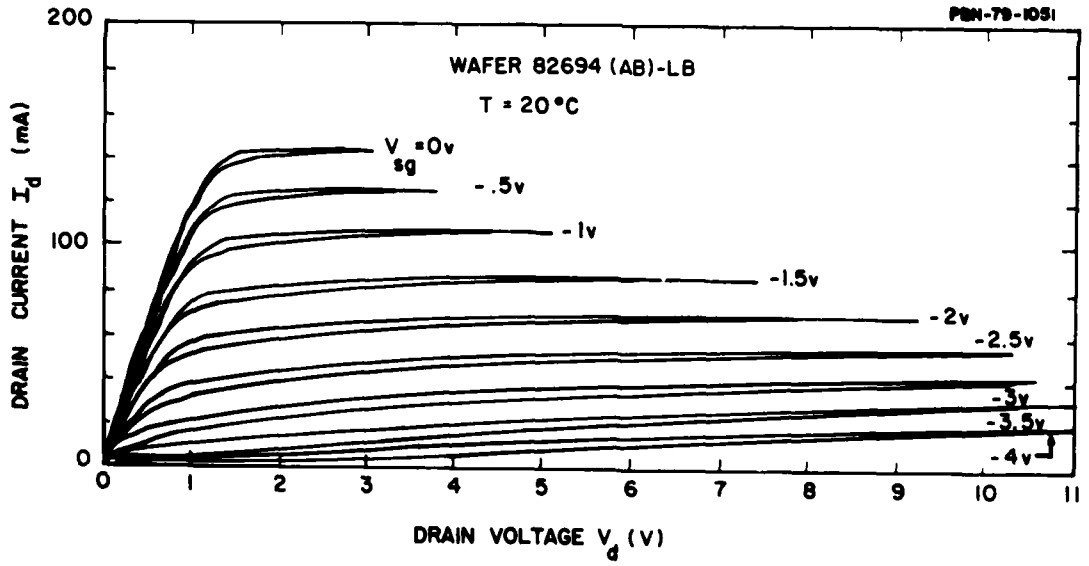


(c) Type ABC Wafer.

Figure 11. I-V Characteristics from Sumitomo Wafers with Different Epitaxial Layer Configurations.



(a) Type A Wafer



(b) Type AB Wafers

Figure 12. I-V Characteristics from Crystal Specialties Wafers with Different Epitaxial Layer Configurations.

TABLE I

EPITAXIAL LAYER CONFIGURATIONS USED IN NOISE STUDIES

Wafer No.	Substrate	Layer Type	Comments
82599	Sumitomo	A	Active layer only
82596	Sumitomo	AB	Active-buffer layers
82588	Sumitomo	ABC	Active-buffer-contact layers
82695	Crystal Specialties	A	Active layer only
82694	Crystal Specialties	AB	Active-buffer layers
82686	Crystal Specialties	ABC	Active-buffer contact layers

TABLE II

PROCESSING VARIANTS FOR FET CHIPS

Processing Designation	Comments
LT	Shallow gate trench w/o surface passivation
LB	Deep gate trench w/o surface passivation
RT	Shallow gate trench with SiO_x surface passivation
RB	Deep gate trench with SiO_x surface passivation

data to be quoted below were based on normalizing the measurements to a common bandwidth of 1 Hz. The noise measured was the noise voltage developed by the drain current passing through a 50-ohm resistor. (The resistor was at first cooled in liquid N_2 to reduce its thermal noise to a negligible value.)* The FET's were in the non-oscillating state. Although in some cases there was a tendency of the devices to oscillate in a spurious manner, extreme precautions were taken to suppress these oscillations. The stability of the resultant I-V characteristics was used as a measure of this, as well as the absence of frequency "spikes" in the low-frequency noise spectra. Both battery operation and well-filtered AC power supply operation were compared, with no noticeable difference in noise spectra. Of course, extreme care was taken to shield the device from outside noise pickup.

Both AM and FM noise spectra were measured in the range 1 kHz to 100 kHz from the carrier. The AM noise-to-carrier (N/C) levels, in general, were 35-40 dB lower than the FM noise.

The baseband noise measurements were taken as a function of gate bias from zero bias to pinchoff, and for two source-drain potentials, 5 V and 9 V. The rf data could be obtained only for a limited range of gate bias values around the half pinch-off value, otherwise oscillations could not be suppressed.

It was not possible to take measurements on more than one device from each quarter, because of the vast amount of data that had to be gathered.

We turn, now, to a discussion of the data obtained with the two sets of wafers.

4.2 Noise Measurement at Room Temperature

4.2.1 Sumitomo substrates

Devices were fabricated from all three wafers, from all but the upper right quarter, RT. A processing mishap prevented many devices from this quarter.

** later found to be unnecessary*

First, some general comments concerning the baseband noise measurements. In all cases, the noise voltage spectra decreased at a faster rate with frequency below 1 kHz than above 1 kHz. The spectra varied at a rate $1/f^{\alpha}$, where f is the noise frequency, with $\alpha \sim 1.5 - 2$ from 100 Hz to 1 kHz, and with $\alpha \sim 0.9 - 1.2$ above 1 kHz. In nearly all cases the noise voltage increased as the gate bias approached pinchoff (as drain current decreased). The noise voltage also increased somewhat with increasing drain bias.

We turn now to the more detailed findings. The inclusion of the buffer layer results in a noise level reduction of from 3 to 6 dB in the range above 1 kHz in all cases, with the higher value applying at the higher drain bias. Little or no improvement was observed at 100 Hz. It appears, therefore, that interface traps do contribute to noise above 1 kHz, and that this contribution is reduced by inclusion of a 2 μm buffer layer. It also appears, in the unbuffered case, that possibly some high field ionization of the exposed interface traps may be occurring at high drain bias voltages.

The inclusion of a contact layer (ABC wafer) appears to have little or no effect on the noise above 1 kHz, although some 5 dB reduction in noise was observed at 100 Hz for the unpassivated, deep trench units. However, too few measurements have been made to generalize this result.

The reduction in noise level above 1 kHz with gate bias varied from zero bias (I_{dss}) to near pinchoff (V_p) appears to be somewhat higher for the unpassivated devices (7-9 dB reduction) than for the passivated devices (0-4 dB), at least for the "deep trench" devices. This is consistent with our findings that passivation reduces the noise level by approximately 0-4 dB, although, again, not enough measurements have been taken to justify a firm generalization of this finding. The improvement with passivation (if any) is most pronounced at $V_g = 0$ V. This is logical, since surface states would have most effect when the conduction channel is nearest the surface.

It appears, however, from our limited results, that there is no perceptible difference in noise level between the shallow trench and deep trench devices,

whether passivated or not. We make the tentative conclusion that it is surface states in the immediate vicinity of the gate that are most probably instrumental in generating noise and that the surface area responsible is essentially the same in both trench designs. Indeed, our results show no significant difference in the noise levels between devices fabricated with a deep gate trench and a shallow gate trench over the entire frequency range.

Turning to the rf measurements, of the twelve combinations tested at baseband, four combinations were selected for detailed rf noise measurements.

The devices tested were the unpassivated set fabricated on the unbuffered wafer (A-type), No. 82599 and the wafer with the buffer layer (AB-type), No. 82596. Both the shallow gate trench and deep gate trench geometries were examined. Because of a "mixup" in instructions in the technology laboratory, the passivated group of devices were fabricated with grounded source contacts ("via" holes) which did not allow us to test them in our common-gate circuitry. The same comment applies to the wafer with the contact layer (ABC type), No. 82588. Despite this problem, the tests made on the remaining device combinations were quite revealing and generally corroborated the findings derived from the baseband noise measurements.

The measurements were quite extensive, because both near carrier AM and FM noise spectra were evaluated from 1 kHz to 100 kHz from the carrier. The noise data were taken as a function of gate bias; generally three or four values ranging from near zero bias to near pinchoff. Here, unlike the baseband noise measurements, little freedom of choice in the gate bias was possible, because the oscillating condition had to be maintained. The measurements were repeated for two other drain biases. Thus, in general, a total of 24 or more noise spectra (AM and FM) were taken for each device combination.

The general findings were as follows. Both the AM and FM noise spectra in the spectral range 1 kHz - 100 kHz varied approximately as 1/f, indicating that the near-carrier noise in this range was indeed a result of baseband noise upconverted to the rf band. The AM noise levels were, in general, approximately 35 - 40 dB lower than the FM noise levels. In most cases, both the AM and FM noise either increased or remained the same as the gate bias was varied

from a slightly negative value ($\simeq$ -1 V) to near pinchoff ($\simeq$ -3 to -3.5 V). The greatest increase in noise level occurred for the unbuffered devices. This is consistent with our baseband noise measurements. The variation in the FM noise with bias was somewhat greater than for the AM noise. The noise levels also increased slightly ($\sim$2 - 4 dB) as the drain voltage was varied from 5 to 9 volts. This result is also consistent with the low frequency measurements.

As for the detailed results, the inclusion of the buffer layer results in a noise level reduction of 10 - 15 dB in the FM noise for the deep trench devices and 6 - 8 dB for the shallow trench devices, with the largest increase occurring near pinchoff. The difference in the FM noise level between the shallow and deep trench designs did not point to a conclusive trend, though the noise level was somewhat lower at most bias conditions for the deep trench designs. This finding, again, is consistent with the baseband measurements.

The reduction in the AM noise level with inclusion of a buffer layer followed the pattern for the FM noise, except that here the improvement in the AM noise was more significant for the shallow trench designs. For example, the noise reduction with buffer layer varied from 4 - 6 dB for the deep trench design, but as much as 13 - 15 dB for the shallow trench design. Furthermore, the absolute level of the AM noise for the shallow trench design was of the order of 4 - 6 dB higher than for the deep trench design. This seems to indicate that surface-state contributed noise might be a larger component of the total noise in the case of AM noise than in the case of FM noise.

4.2.2 Crystal Specialties substrates

In general, the baseband noise spectra decreased at a rate approximately $1/f^{\alpha}$, where f is the frequency, and $\alpha \sim 1 - 1.5$. This is similar to the results obtained with Sumitomo substrates. As with the Sumitomo substrates, the noise increased somewhat with gate bias approaching pinchoff, though in some cases a minimum was achieved at an intermediate bias. The noise spectra increased with increasing drain bias (from V_d = 5 V to V_d = 9 V) by approximately 0 - 4 dB, just as for the Sumitomo substrates. In general, the noise levels were within a few dB of those measured for the Sumitomo substrates for the type AB and ABC

wafers, that is, for those wafers having a buffer layer. However, in the case of the devices fabricated from the unbuffered wafer, the noise level was as much as 7 dB lower than for the Sumitomo substrates. This large difference occurred for low gate bias, V_g = 0 V. At bias voltages approaching pinchoff, the distinction between the two sets of substrates is negligible.

Now for the more detailed findings: The contact layer, as before had little effect on the noise level. Also there appears to be little difference in the noise levels measured for deep trench devices and shallow trench devices. This again confirms the earlier findings with Sumitomo substrates.

Consider the shallow trench devices. The noise level decreased by 2 - 6 dB as the gate bias was varied from 0 V to the pinchoff value. When the drain bias was increased from 5 V to 9 V, the noise increased slightly, approximately 0 - 4 dB, depending on the gate bias, the larger increase occurring for a gate bias near pinchoff. However, we did observe an "anomalous" increase of nearly 20 dB in the noise level at the higher drain bias, near pinchoff for the "ABC" wafer (No. 82686). This may be a spurious result, since it only occurred for the unpassivated "ABC" devices.

We turn now to the deep trench devices. The noise levels here are not significantly different from those of the shallow trench devices, as we also found for the Sumitomo substrates. The variation of noise with gate bias was rather insignificant. Also, here too, a 2 - 5 dB increase in noise level was observed as the drain bias was increased from 5 V to 9 V.

Our general conclusion is that the major difference between the results obtained with Sumitomo and Crystal Specialties substrates is that the noise contributed by the substrate itself in the former case is about 7 dB higher and can be reduced by a buffer layer. On the other hand, the substrate contributed noise in the case of Crystal Specialties is already low enough so that little or no improvement appears to occur with a buffer layer.

4.3 Noise Versus Drain Current and Temperature

4.3.1 Introduction

We measured the baseband noise of selected devices to determine whether the dependence on bias current suggested by Eq. (5) was followed. Generally speaking, 1/f noise shows a mild dependence on temperature. Therefore we also varied the device temperature to test this dependence. We hoped that by these measurements we would gain some insight as to the origin of the traps, i.e. deep level or shallow level, and possibly their physical location, for example, near the active layer-substrate interface, or the bulk or surface regions of the channel.

Based on the results described earlier, we chose to concentrate our studies on two of the twelve possible combinations. These are the devices from the left bottom half of the "active layer only" wafer 82695, and the "active-buffer layer" wafer 82694. See Fig. 10 and Tables I and II. These are both Crystal Specialties substrates. We chose to use unpassivated devices because of the variability of the data obtained with passivated devices, as described earlier.

The choice for deep trench devices was somewhat arbitrary since we did not see any significant difference in noise between the deep and shallow trench devices, as we showed above. We chose to ignore the type ABC wafer (with a highly doped contact layer) since our results showed no dependence on this layer. Thus all data reported here apply to unpassivated, deep trench devices of either the unbuffered type, 82695(A)-LB or buffered type 82694(AB)-LB.

We made detailed measurements of the noise as a function of gate bias from pinchoff to zero bias. We were especially interested in the near-pinchoff condition, since this corresponds to the depletion layer boundary near the interface between the active layer and the buffer layer or the semi-insulating substrate, as the case may be. Our purpose was to obtain diagnostic data to allow us to formulate a simple model of a trap spatial distribution that would account for our measured noise results.

In contrast to most workers, we chose to display the measured noise as a drain noise current fluctuation as a function of drain bias current (rather than

as an equivalent noise voltage fluctuation at the gate). We believe the latter (and more popular method of presentation) is artificial, at best, and obscures the "physics" underlying the noise generation. Furthermore, 1/f noise, phenomenologically speaking, or more precisely trap noise, is a fluctuation of the number of carriers partaking in conduction, and hence as a current fluctuation, rather than a voltage fluctuation. Finally, the channel cross section can be more simply related to the drain current than the gate bias, though this is a minor point.

Suspecting that the trap noise generation might be somewhat different above the knee of the I-V characteristic than below — where the carriers are not in velocity saturation and the fields are very low, we also took baseband noise measurements at a drain bias of approximately one-third the knee voltage.

The mean square noise per unit frequency band associated with traps, or a uniform spatial distribution of traps, generally speaking, varies as

$$\langle i_n^2 \rangle / \text{Hz} = \frac{K(T) I^{\alpha}}{f^{\beta}} , \qquad (11)$$

where α is of the order of two, β the order of unity, and K(T) is a mild function of temperature T.

The results to be described here adhere quite closely to a 1/f dependence from 100 Hz to 100 kHz. However, as shall be seen, the noise current either increases with current, or decreases with current, depending on the bias conditions and temperature. This is at variance with our expectations and suggests that the trap distribution is not at all uniform but, more likely, segregated at narrowly defined physical regions, for example, the interface zone.

The current was varied from near zero (at pinchoff) to I_{dss} at zero gate bias. The drain bias was varied in steps from below the knee of the I-V characteristic, V_d = 0.5, to a value near the knee, V_d = 1.5 V, to values well above the knee, V_d = 5 V, the operating point for our oscillator, to, finally V_d = 9 V, well above the operating point.

The temperature was varied in steps from room temperature to -30°C, -80°C, and -130°C. I_{dss} increased by about 25 percent over this range. Some instabilities set in at -80°C at low drain bias voltages, and presented problems.

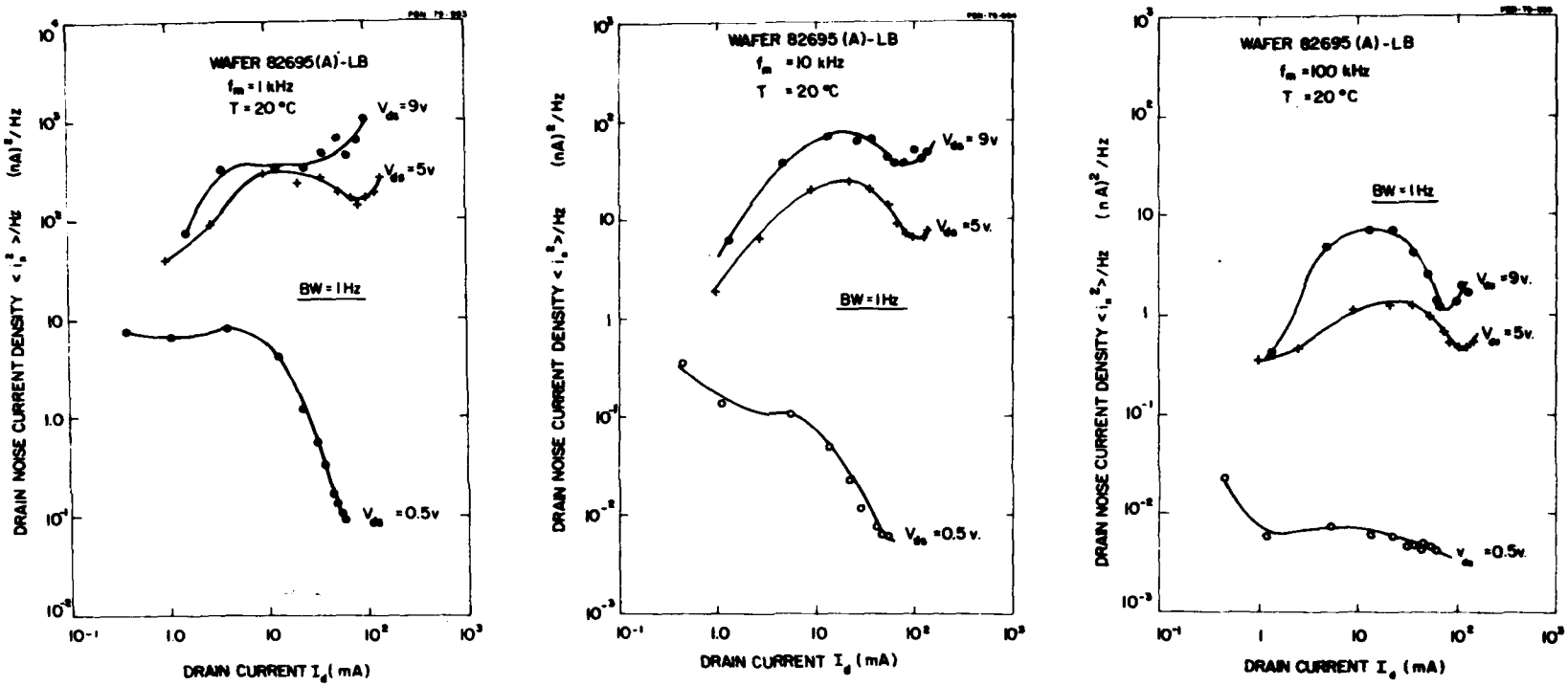
Our noise measurements at room temperature were taken at constant drain bias of 0.5 V, 5 V, and 9 V. At the lower temperatures, 1.5 V was used instead of 0.5 V because of the instability problem. The noise was measured at 1 kHz, 10 kHz, and 100 kHz. For ease of comparison, all noise data were normalized to a one-Hertz bandwidth, though the data were taken over a 10-Hz bandwidth at the lower two frequencies and, in some cases, over a 300-Hz bandwidth at the higher frequency.

We turn to our experimental findings. The first set of results to be discussed apply to the unbuffered device, wafer 82695(A)-LB. The second, less extensive set are for the buffered device, 82694(AB)-LB.

4.3.2 Unbuffered devices

Figure 13 (a-c) are plots of the mean square noise current in the channel as a function of drain bias current at room temperature, T = 20°C, for three baseband frequencies, f_m = 1, 10, 100 kHz. The experimental points correspond to gate bias increments of 0.5 V, starting at 0 V and increasing negatively to pinchoff. Note that the current scale is logarithmic, as is the vertical, noise current (power) density axis. The data shown are for three drain bias voltages, one below the knee, the other two well above the knee.

It is evident from Fig. 13(a) that none of the curves at low drain bias show any power law dependence on current (which would lead to an approximately straight line plot) although the two curves for V_d above the knee show a generally increasing trend with drain current. What is most notable is the rapid, monotonic decrease of noise current for V_d = 0.5 V. Note that, at I_{dss} (60 mA), the noise level is over 30 dB lower than for V_d = 5 V. The "flat" portion below the knee, extending to about 10 mA, corresponds to a channel opening about 8 percent of that at V_g = 0, or about 100 Å. This monotonic drop-off holds true about 10 kHz also. The "flatness" at the higher current for the 100 kHz data was caused by system noise.



(a) f_m = 1 kHz *(b)* f_m = 10 kHz *(c)* f_m = 100 kHz

Figure 13. Baseband Noise as a Function of Drain Bias Current and Voltage for a Type A Wafer (Sumitomo) at Room Temperature.

Turning to the high voltage curves, we note that, although the curves generally increase with increasing drain current, there are distinct peaks at about I_d = 30 mA. These peaks occur for all three frequencies. These peaks correspond to a gate bias $V_g \approx -3.5$ V and a channel opening of $\approx 200 - 250$ Å. It is tentatively postulated that the source of noise at high currents and high drain bias is probably different than at low drain bias, or that some enhancement of trap emission is occurring because of trap barrier lowering by the high channel fields. This does not rule out the possibility that the noise seen at V_d = 0.5 V is also present at V_d = 5 V, but of course, it would be submerged in the higher noise level. Notice that the peaks are more pronounced at V_d = 9 V than at V_d = 5 V.

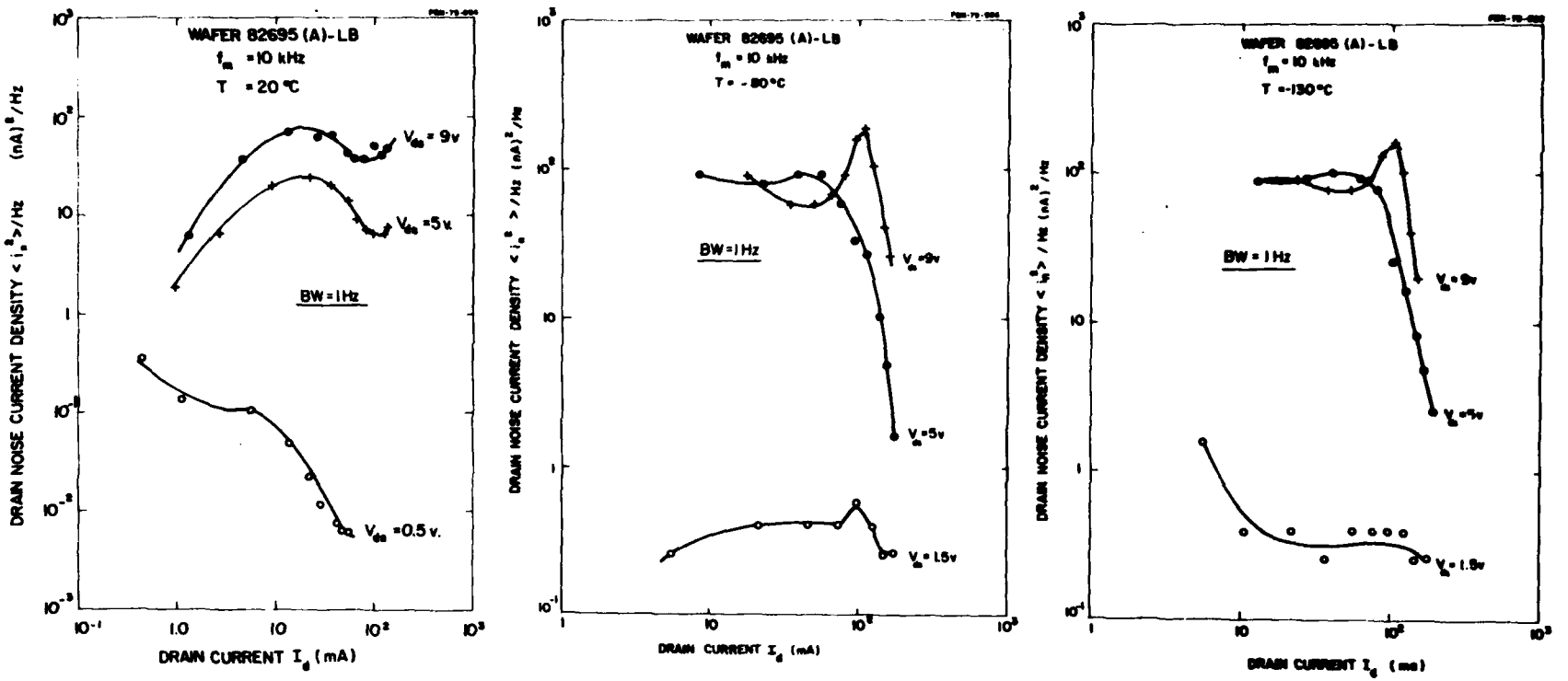
Figures 14(a-c) show how the noise current dependence on drain current changes as the temperature is lowered at 10 kHz. The variations at 1 kHz and 100 kHz were similar. Note that the lowest curve is for V_d = 1.5 V rather than for V_d = 0.5 V, because of the stability problem mentioned earlier.

Generally speaking, the dependence of the noise on temperature is weak and doesn't seem to follow any definite trend with temperature, as at some bias currents it decreases with temperature, and at other bias currents it increases. However, what is notable is that for drain bias voltages above the knee, the noise current does not continue to increase with bias current but decreases rapidly with current above a certain current level. In other words, the rapid monotonic decrease in noise current, with increases of channel current observed for the low drain voltage at room temperature, is exhibited at high drain voltages at the reduced temperatures. This is especially noticeable at T = -130°C. Note the continued presence of the peak region at V_d = 9 V at the reduced temperatures. The rapid drop-off of noise with temperature at high drain voltages and current suggests the presence of deep traps.

We turn to the data for the devices with buffer layers.

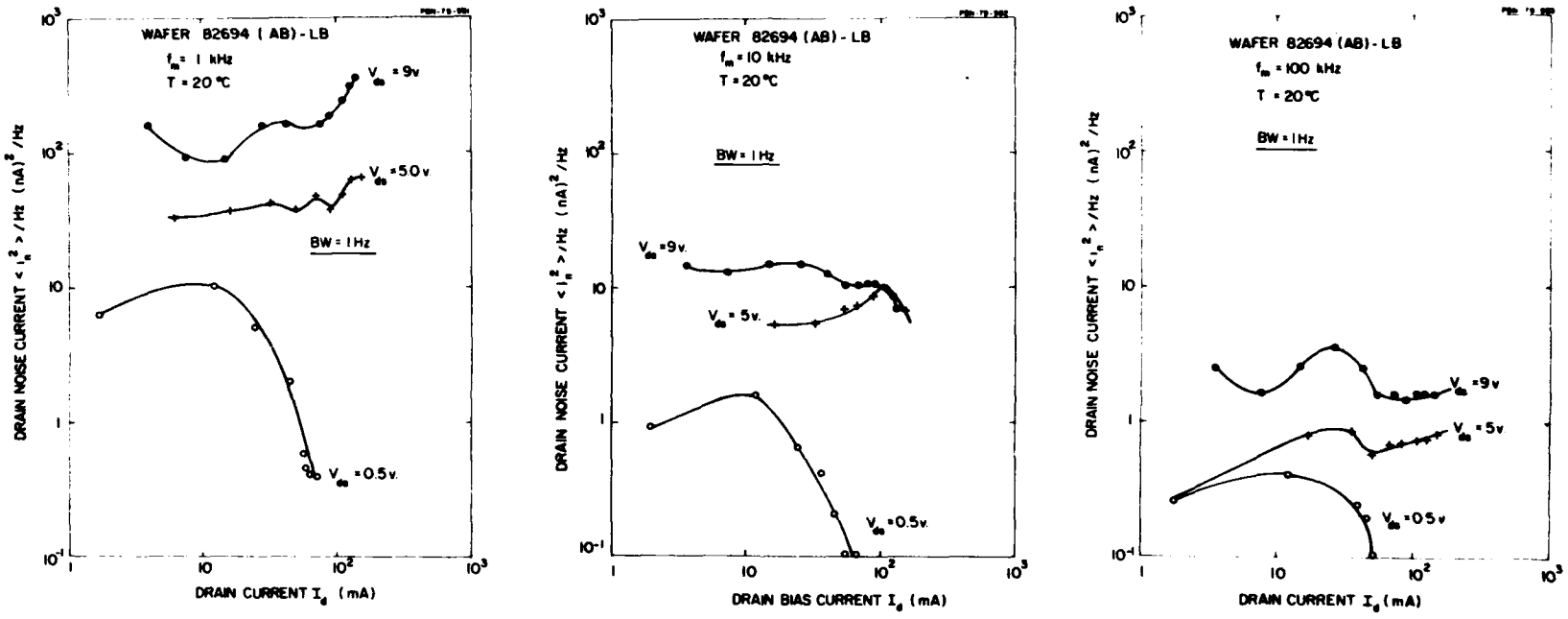
4.3.3 Buffered devices

Figures 15 (a-c) illustrate the noise current level as a function of



(a) T = 20°C *(b) T = -80°C* *(c) T = -130°C*

Figure 14. Baseband Noise as a Function of Drain Bias Current and Voltage for a Type A Wafer (Sumitomo) for Various Temperatures.



(a) f_m = 1 kHz *(b)* f_m = 10 kHz *(c)* f_m = 100 kHz

Figure 15. Baseband Noise as a Function of Drain Bias Current and Voltage for a Type AB Wafer (Crystal Specialties) at Room Temperature.

drain bias current and drain voltage. These should be compared with Fig. 13 for the unbuffered device. Note the general similarity of the curves with respect to the dependence on drain bias current. Though the level of the noise current is lower by a factor of 2 to 3 at the above-knee drain voltages, there does not seem to be a similar relation for below the knee. Here, only limited data were taken at reduced tempratures, namely at T = -130°C. The general similarity of the curves to those for the unbuffered device extends to these lower temperatures also (not shown).

4.3.4 Conclusions

It is evident from all of the data presented in 4.3.2 and 4.3.3 that there are some general trends of the noise data with respect to bias conditions and temperature. The following (tentative) conclusions can be advanced, based on these trends.

(1) Some noise appears to originate from the interface region between the active layer and the semi-insulating substrate or the buffer layer, as the case may be. The below-knee voltage data suggests this. It is likely that, near pinch-off, the source drain current is forced into the substrate, or substrate-buffer layer region, and therefore traps present in the substrate, or those which may have diffused into the buffer layer during the growth process, are active in both the buffered and unbuffered devices.

(2) At room temperature, another much stronger source of noise is active at high drain bias voltages. This source seems to subside at reduced temperatures. This second source seems to peak at current levels corresponding to a very narrow channel height of about 200 Å. Deep traps are suggested. In the next subsection we show how we attempted to "electronically" probe this narrow channel strip to obtain a spatial profile of the trap noise centers in a direction orthogonal to the channel.

4.4 Noise Versus Substrate Bias Voltage

4.4.1 Introduction

The objective of the substrate bias experiments was to deplete a portion of the channel region from the "bottom side." Then by readjusting the gate bias to maintain the drain current constant, one can take a uniform "slice" of channel at different positions within the channel starting from the interface and moving "upward" toward the gate.

The amount of channel depletion that we were able to achieve was limited because of the large drop across the substrate and by substrate-drain avalanche breakdown. Therefore, experiments on channel current modulation could only be carried out near pinchoff where any channel depletion from the substrate side would be a larger fraction of the total channel "height" than at smaller gate bias values. This, of course, limited the amount of spatial probing that we could achieve. It was estimated, on the basis of the I-V characteristics and the current modulation achieved that the spatial probing covered a zone approximately 20 A centered at about 90-100A from the interface between the active layer and the substrate or buffer layer as the case may be. Measurements were made on both buffered and unbuffered devices.

4.4.2 Unbuffered device

Figure 16 shows how the channel current decreases from 10 mA (near pinchoff) to lower values as the substrate-source bias is varied from 0 to -30 V. Notice that the degree of channel height modulation increases with decreasing source-drain bias. The current reduction, even at V_d = 0.5 (below the knee of the I-V characteristic) is only 25 percent. Also shown in Fig. 16 are curves at reduced temperatures. The current variations observed are much less. We have no explanation for this unexpected result at this time, though we suspect the involvement of deep traps.

Figures 17 (a-c) show how the 1/f noise varies as a function of substrate-source bias at f = 1 kHz, 10 kHz, and 100 kHz, respectively, at room temperature.

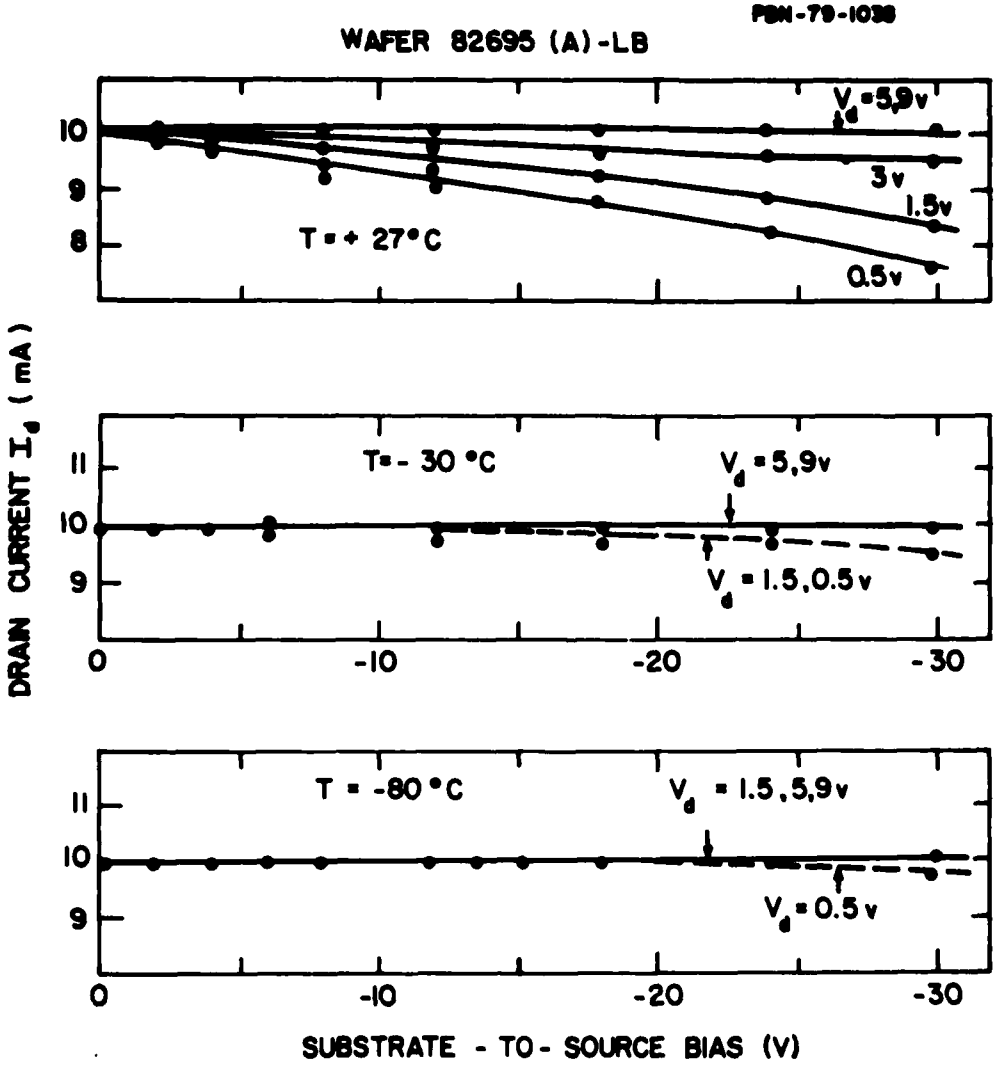
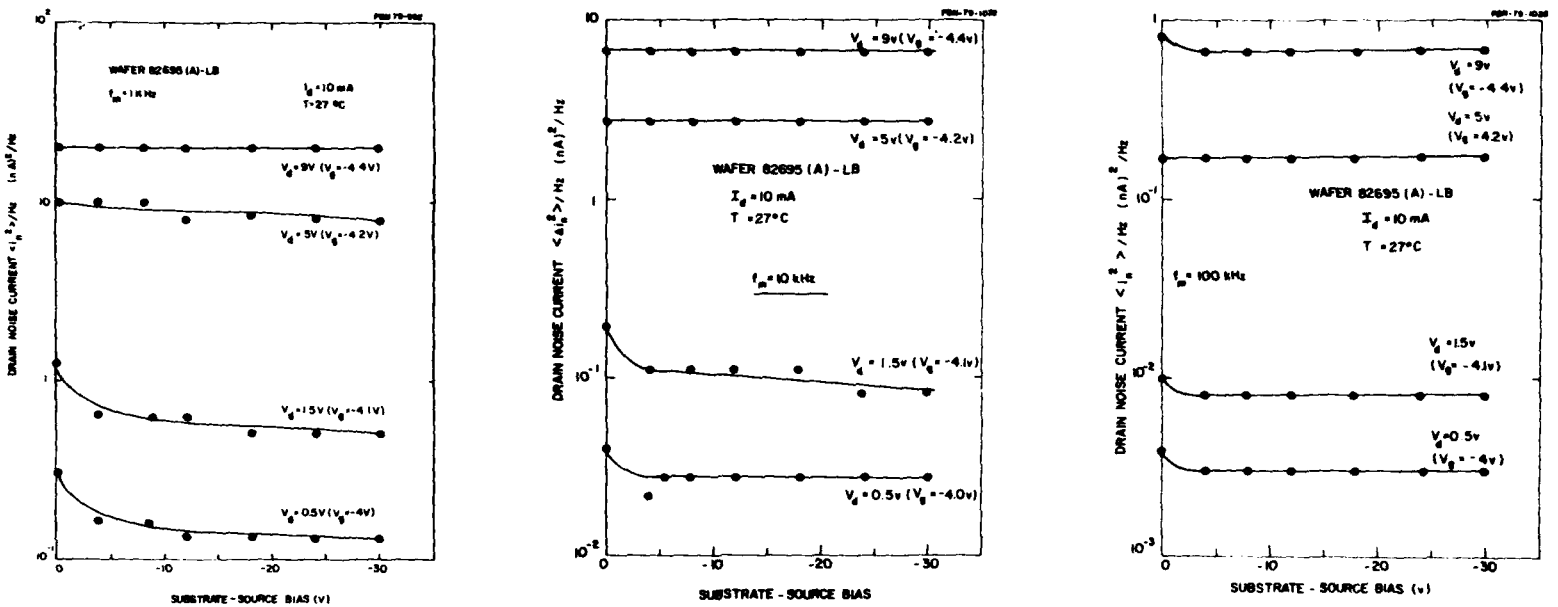


Figure 16. Drain Current as a Function of Substrate Voltage and Drain Bias and Temperature for a Type A Wafer (Sumitomo).



(a) f_m = 1 kHz *(b)* f_m = 10 KHz *(c)* f_m = 100 kHz

Figure 17. Baseband Noise as a Function of Substrate Voltage and Drain Bias at Room Temperature for a Type A Wafer (Sumitomo).

Notice, in particular, for the lower drain voltages an initial decrease in noise as the substrate bias is increased to 5 volts. The initial decrease for f_m= 1 kHz is approximately 3 dB. The decrease is less at f = 10 kHz and 100 kHz. Note the complete absence of an initial drop-off at V_d = 5V.

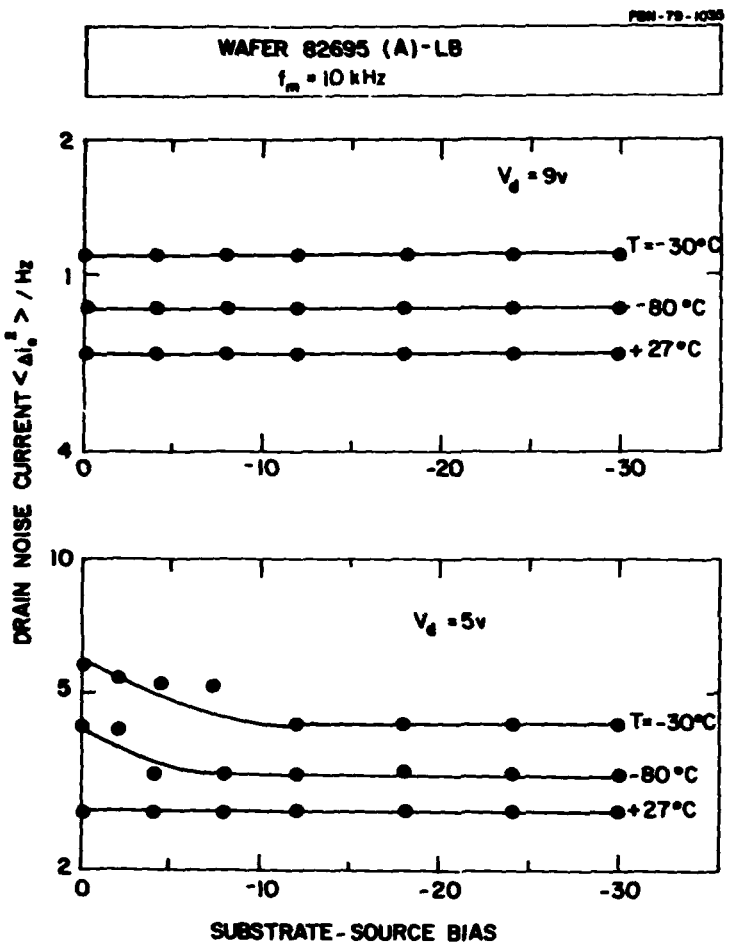
Figure 18 shows how the noise dependence with substrate-source bias varies with temperature. Notice that an initial drop-off in noise with substrate bias now appears for V_d = 5 V at the lower temperatures. Note that at V_d = 1.5 V the curve for T = -80°C falls below the curves for T = -30°C and T = +27°C but then reverts to the original order of curves at the still lower drain voltage, V_d = 0.5 V. Also note that at the lowest drain bias, no initial drop-off in noise with substrate bias occurs for T = -80°C. It is evident that the noise goes through a maximum as a function of temperature near T = -30°C.

4.4.3 Buffered device

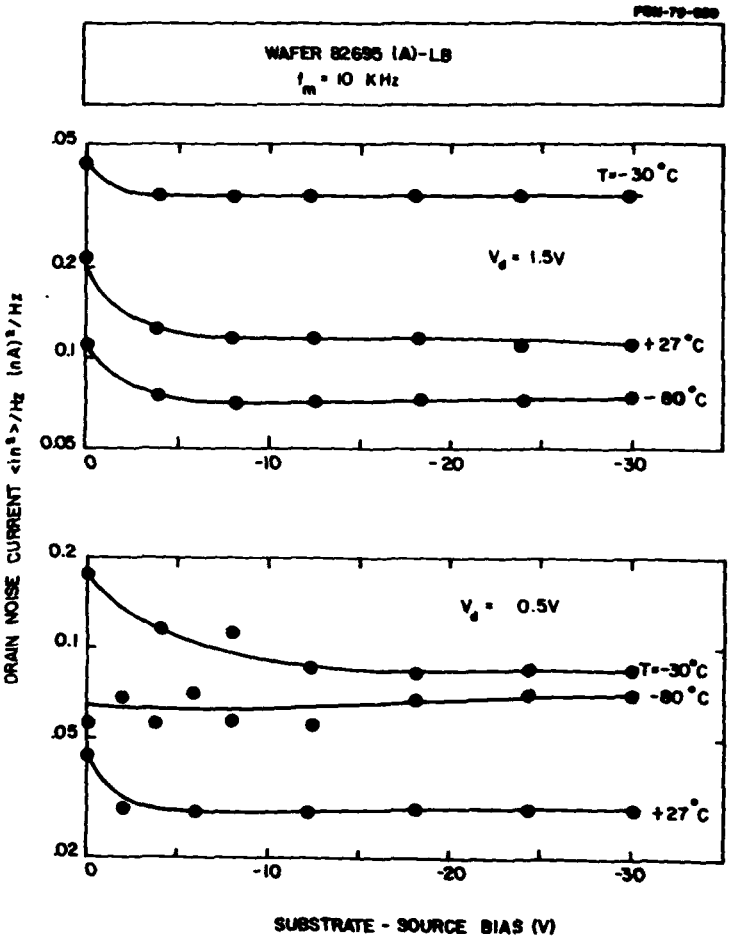
Figure 19 illustrates, for a buffered device from wafer 82694, the substrate-drain current modulation characteristic. Observe the somewhat higher degree of modulation obtained. This is probably caused by carrier depletion in the buffer layer. Note that the V_d = 0.5 V and V_d = 5.0 V curves are reversed in order from that obtained with the unbuffered device. This "anomaly" is not understood. However, the baseband noise data taken at room temperature does not mirror this "disorder". See Fig. 20. The noise curves in Fig. 20 show a monotonically decreasing noise with decreasing drain voltage, just as in the case of the unbuffered device, Fig. 17.

Observe that the data for f_m = 1 kHz show distinct increases in slope at the higher substrate bias voltage. This "threshold" vanishes at 10 kHz and 100 kHz, indicating that the noise fall-off with frequency occurs at a faster rate than 1/f. This would seem to negate an avalanche breakdown process, since this would generate white noise.

We illustrate the frequency fall-off at V_{sub} = OV and V_{sub} = -24 V in Fig. 21, for two values of drain voltages. The rate of drop-off is between



(a) V_d = 9 V, 5 V



(b) V_d = 1.5 V, 0.5 V

Figure 18. Baseband Noise at f_m = 10 kHz as a Function of Substrate Voltage and Drain Bias at Various Temperatures for a Type A Wafer (Sumitomo).

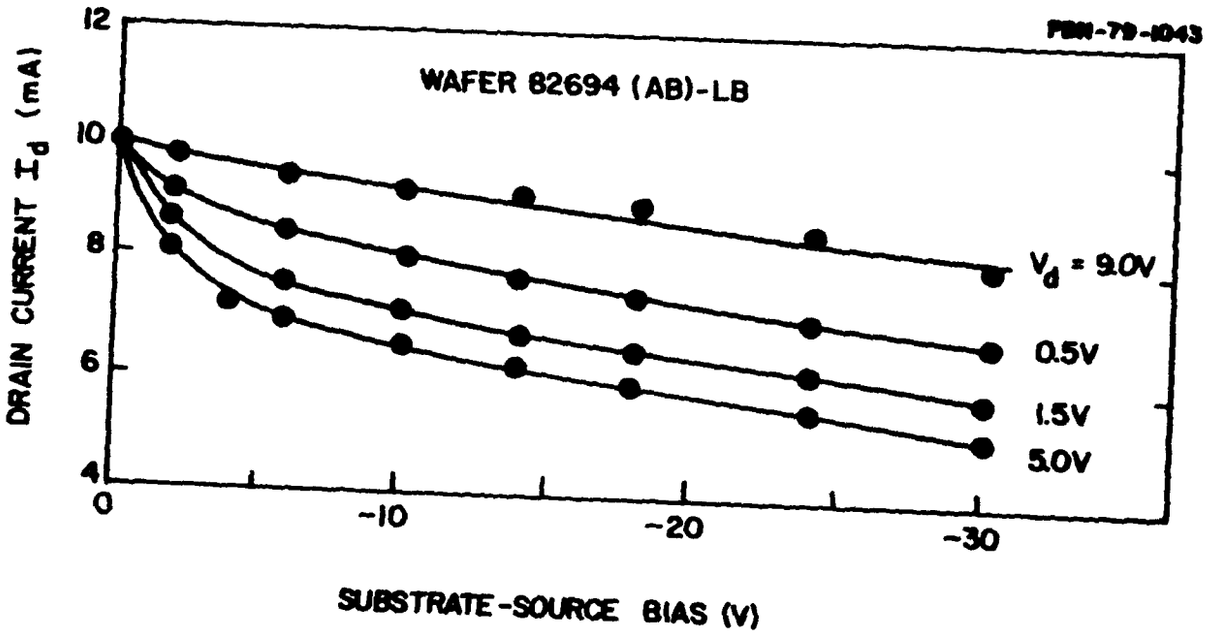


Figure 19. Drain Current as a Function of Substrate Voltage and Drain Bias at Room Temperature for a Type AB Wafer (Crystal Specialties).

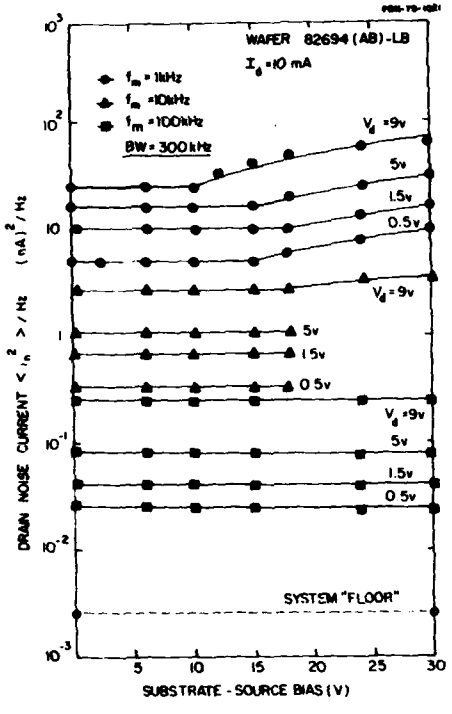


Figure 20. Baseband noise as a function of substrate voltage and drain bias at room temperature for various frequencies for a Type AB wafer (Crystal Specialties).

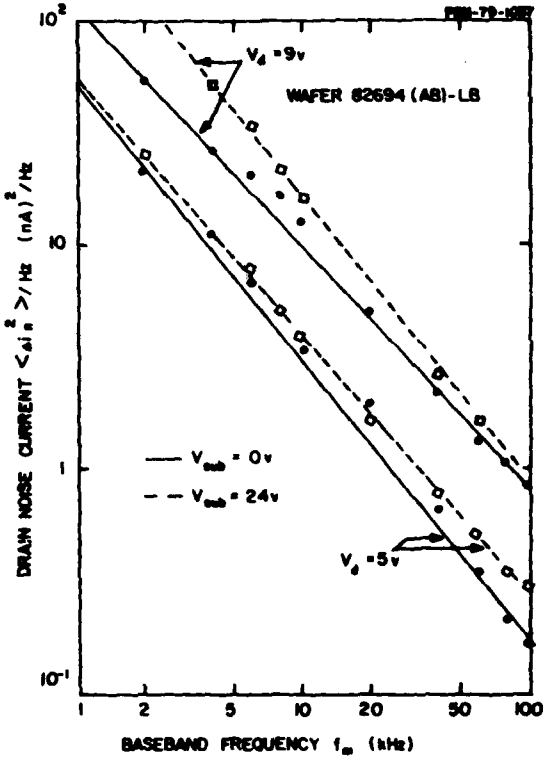


Figure 21. Baseband noise as a function of frequency, drain bias, and substrate voltage for Type AB wafer (Crystal Specialties).

$1/f^{1.4}$ to $1/f^{1.6}$ with a definite trend to a faster rate at V_d = 9 V approaching $1/f^2$. Thus, in the above-threshold region, there is a faster rate of fall-off with frequency than a 1/f rate. We conclude that the threshold condition is not indicative of the onset of avalanche breakdown but some other, as yet undeciphered, threshold phenomenon.

4.4.4 Hysteresis

During our substrate modulation experiments we noticed a hysteresis effect when the substrate bias was changed. This manifested itself as a slow drift in the drain current when a rapid change in substrate bias was made. This hysteresis seemed to be present in both buffered and unbuffered devices. Our observations for a buffered device are shown in Fig. 22. The time intervals between measurements and the sequence in which the data were taken are indicated on the figures. Notice that rather long time intervals are involved. This surely points to deep-trap levels. Since both buffered and unbuffered devices seem to be similar in this regard, and since the space-charge spreading with application of substrate bias occurs into the substrate (predominantly), it appears that this hysteresis is associated with deep traps within the substrate itself.

4.4.5 Conclusions

It should be obvious by now that the measurements of the baseband noise present a rather complex picture of the dependence of the 1/f noise on temperature and biasing conditions. Several tentative noise models have been considered, with traps situated both within the active epi layer, as well as at the epi-substrate or epi-buffer layer interface. From the data obtained at voltages above the "knee" of the I-V characteristic, i.e., V_d = 5.0 V and V_d = 9.0 V, it is suggested that some degree of field ionization of the trap centers takes place. This we believe is a new feature of the 1/f noise in FET's and must be considered for short gate devices because of the high channel fields. Unfortunately, little data is available on field ionization of traps, except in germanium at very low temperatures. The high fields lower the potential barrier in the vicinity of a trap and also may excite a trap by the tunneling mechanism.

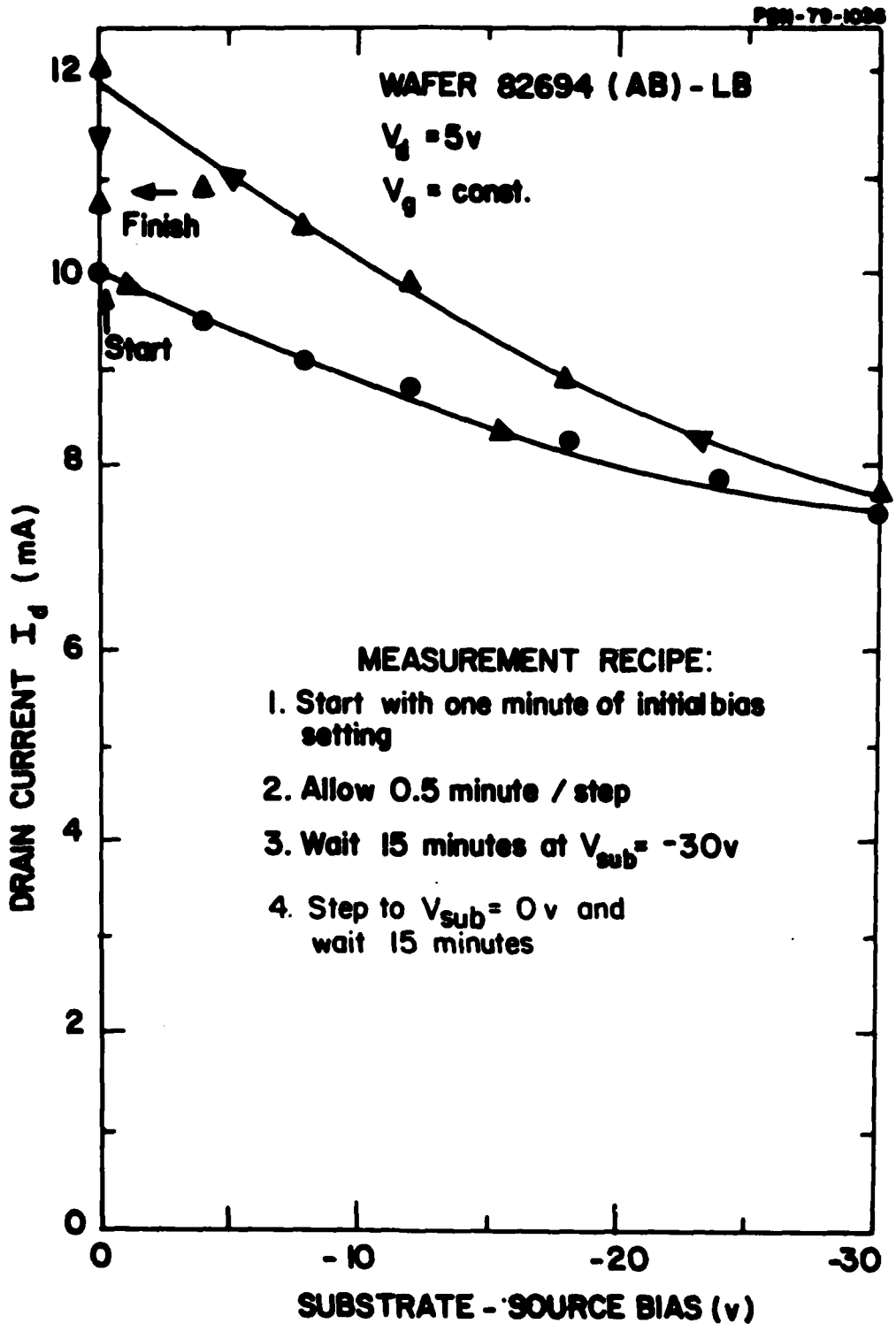


Figure 22. Hysteresis Effects in a Type AB Wafer (Crystal Specialties).

The substrate modulation experiments suggest that, at least for the channel region probed, there does not appear to be a high peaked concentration of trap noise sources. If there were, we should not have obtained such a mild dependence of drain noise on substrate bias.

So far we have only addressed the problem of 1/f noise at the expense of intrinsic (thermal noise) as outlined in Sec. 2.0. We have done this deliberately because we believe that the near carrier noise is the more serious. In Sec. 5.5 we shall present experimental evidence to support this conclusion.

4.5 Baseband Noise Versus Temperature

4.5.1 Introduction

In this section we describe experimental results obtained on FETs which were subjected to a wide temperature range extending from -180° to +70°C (93° K to 343° K). This is a much wider range than that discussed in Sec. 4.3. Both oscillating and non-oscillating FETs were studied. One objective was to determine whether an activation energy is displayed by the noise versus temperature data, for example, by a constant slope in the log (noise) versus 1/T plot. Another, related objective was to look for pronounced peaks in the noise versus temperature data, which would denote distinct trapping levels in the band gap, as observed, for example, in silicon junction FETs.[19] In the process of cycling the FETs over the temperature range, some unexpected but revealing observations were made concerning the effect of stresses on the 1/f noise level.

The FETs were fabricated from a Sumitomo substrate (Wafer 7A87) onto which a buffer and active layer were grown (Type AB). The buffer layer differed from that of the previous devices, which were undoped (not intentionally doped). The present buffer layers were doped with ammonia (NH_3). The thickness was similar to that of the earlier devices. The active layer was silicon doped to $10^{17}/cm^3$ as before. The devices have a recessed gate structure. The exposed unmetallized top surface of the devices was passivated with SiO_x, portions of which are also overcoated with metallization. Figure 23 is an I-V characteristic typical of these devices.

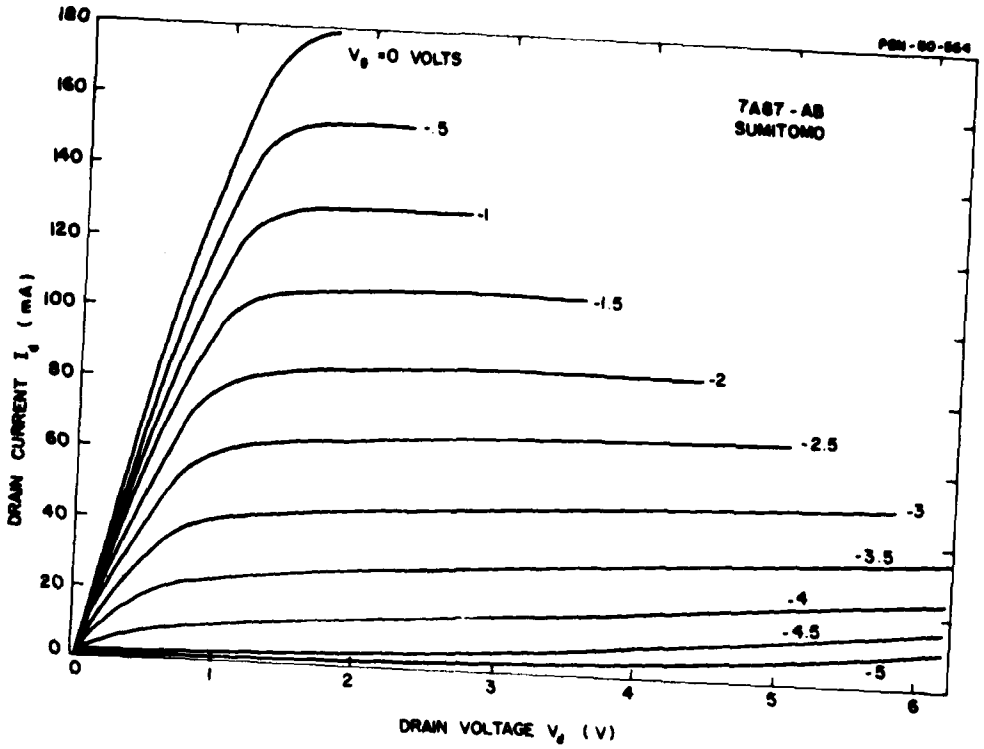


Figure 23. I-V characteristic of FET.

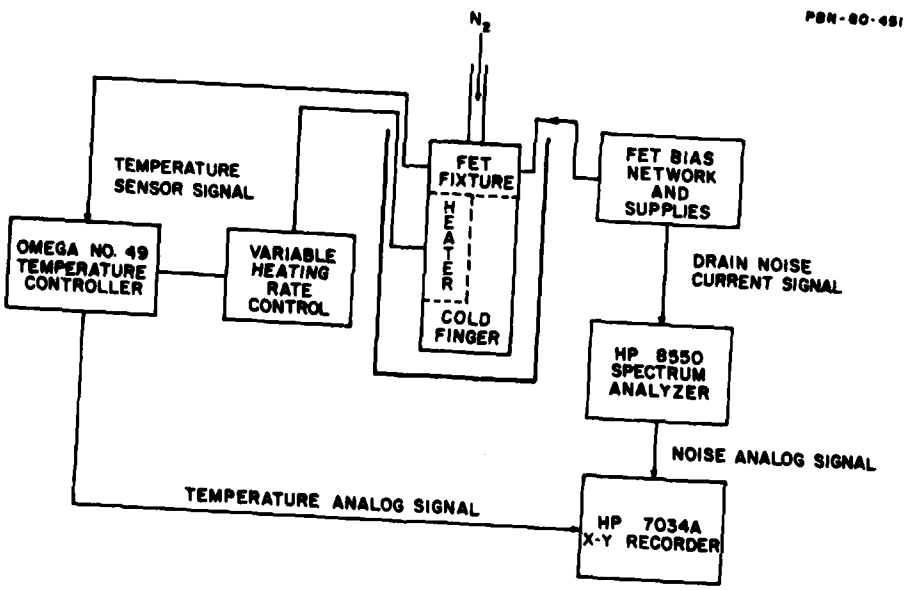


Figure 24. Block diagram set-up for noise versus temperature measurements.

4.5.2 Experimental set-up

The experimental set-up was designed for obtaining noise versus temperature data at a constant baseband frequency or, alternatively, noise versus baseband frequency at a constant temperature. The block diagram in Fig. 24 illustrates the method by which the noise at a single frequency is measured as the temperature is varied. The arrangement for obtaining swept frequency data at a constant temperature is very similar. The device in its fixture was thermally bonded to a cold finger, which also incorporated an integral heater; electrical connections were made to the fixture and the assembly was cooled to near liquid nitrogen temperatures. Nitrogen gas flooded the surface of the device to preclude condensation of water vapor during the temperature cycle.

The power available to the heater was adjusted to provide a nearly constant rate of rise of the temperature of the assembly, approximately five degrees per minute; the temperature controller, acting only in the read-out mode, provided a temperature analog voltage to the x-y recorder. The spectrum analyzer operates as a fixed-frequency noise receiver and also provides a noise-power analog voltage to the x-y recorder.

Swept frequency data at a constant temperature was obtained by allowing the temperature controller to hold the temperature while the spectrum analyzer swept the frequency range of interest. The analyzer provided both noise-power and frequency analog voltages to the recorder. The system allowed temperature measurements from T = -180°C to well above room temperature. The test data was normalized to one Hz bandwidth and replotted against linear temperature, inverse temperature, or baseband frequency, as appropriate.

4.5.3 Oscillating FET

The device was biased at V_{gs} = -3V, V_{ds} = 5V, and oscillated at 10 GHz with a power output of 40 mW (at room temperature).

The noise was measured from T = -180°C to T = +40°C, and over the baseband frequency range from approximately 0.5 kHz to above 200 kHz. At all temperatures the noise displayed a nearly 1/f frequency dependence.

Figure 25 is a plot of drain noise current versus inverse temperature for the temperature range -180°C to +40°C at two baseband frequencies. No distinct linear (constant slope) regions, indicative of an activation energy (trap level), are in evidence.

4.5.4 Non-oscillating, FET

Baseband noise measurements were also taken over the temperature range for the oscillating FET, except that the upper end of the scan was increased to +70°C after some contact problems were solved. The same device was used except that the rf oscillations were suppressed. In addition, the temperature was cycled to determine whether any temperature hysteresis phenomena were present. Temperature cycling under rf oscillation conditions was not tried, because of the vast amount of data reduction which would have been necessary.

Some changes also were made in the noise measurements. To enhance possible "peaks" and "valleys" in the noise data, we replaced the baseband noise analyzer (which measures noise power in decibels) with a noise receiver whose output is in volts. Thus the noise voltage could be recorded directly on an X-Y recorder on a linear scale. In addition, frequency measurements were extended down to 100 Hz. Here a lock-in amplifier proved useful in improving stability during the measurement.

Initially we were plagued by contact problems associated with repeated cycling of the device over the large temperature range. Usually the contacts opened and had to be rebonded. This presented problems in repeating data. To minimize the contact problem, we replaced our wire bonds with gold ribbons to relieve stresses associated with temperature cycling.

Despite these precautions, nonrepeatability of data persisted, though perhaps delayed for a few temperature cycles. The nonrepeatability of the data,

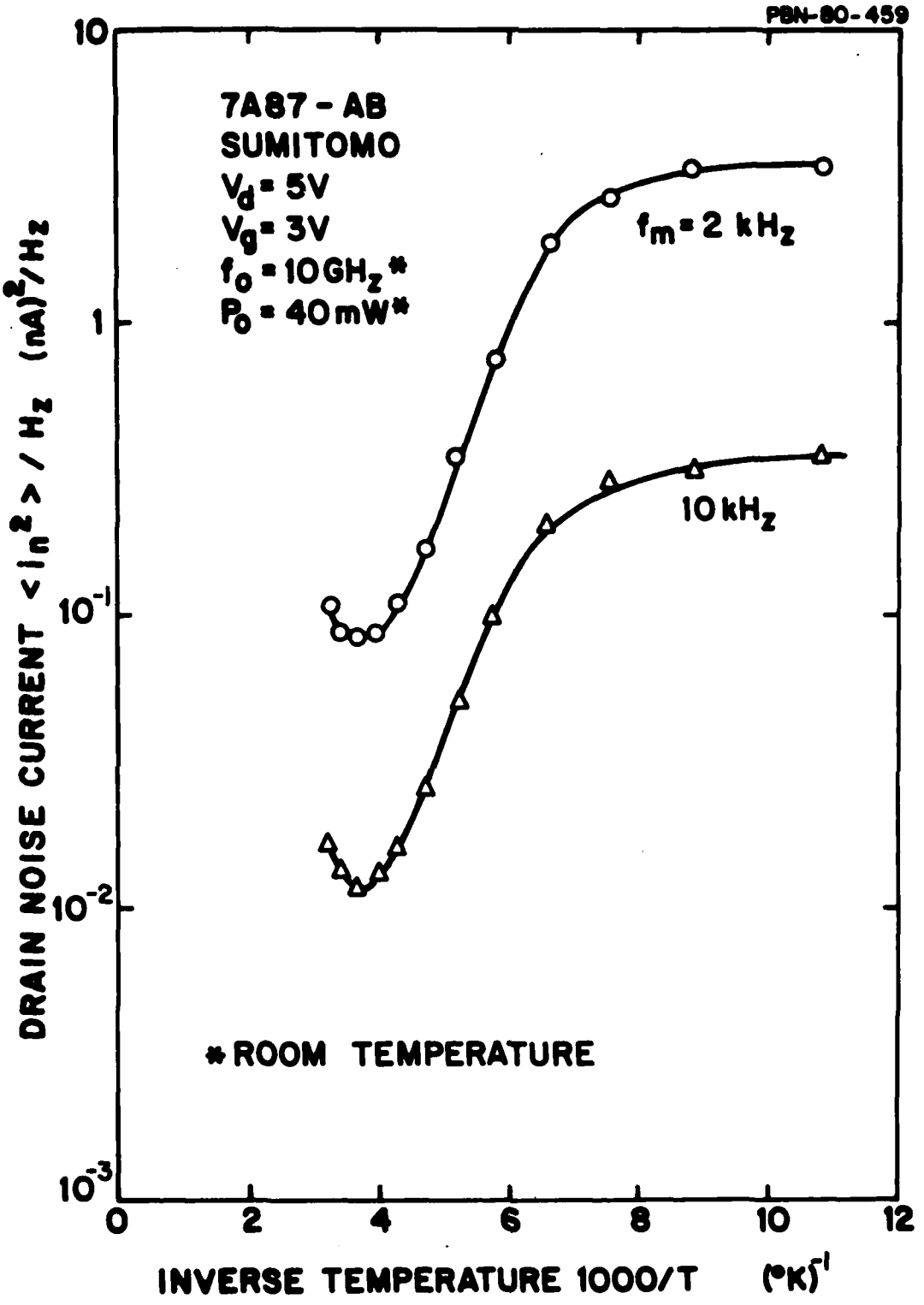


Figure 25. Measured drain current noise versus temperature (inverse scale) for f_m = 2 kHz and f_m = 10 kHz.

however, was of a very special form — namely an increase of the 1/f noise level over the entire baseband frequency range. That is to say, the noise level simply increased while maintaining a near 1/f behavior. The increase was not small — at least an order of magnitude.

Figure 26 shows the measured 1/f noise taken at room temperature before temperature cycling, and then after two cycles down to -180°C. Note that the noise exhibits an almost perfect 1/f behavior. (Actually these curves were taken before the gold ribbons were introduced, but the phenomenon also occurred afterward.)

This behavior certainly could not be explained on the basis of changes in the traps within the GaAs material itself or the device characteristics. Indeed, measurement of the I-V characteristic after cycling did not indicate any unusual features.

Routine examination of the samples after cycling, however, showed unusual deposits on the surface of the chip [see Fig. 27(a).] A SEM photograph showed that the "deposits" were actually small pieces of the metallization [Figs. 27(b) and 27(c).] A close-up view [Fig. 27(c)] shows clearly that cracks have developed in the oxide layer, which caused some of the plating to "snap" off. Thus, the cause of the increase in 1/f noise appears to be related to exposure of the GaAs surface by the cracks and to creation of surface states either because of stresses which may have been created during the temperature cycling by the differential contraction and expansion of the GaAs and oxide or by the ambient, for example, some water vapor which may not have been expelled by the dry nitrogen flow and may have condensed and become trapped in the cracks.

We did manage to obtain some noise data before the nonrepeatability problem set in. Figure 28 illustrates the results. Shown is the noise voltage developed across the 50-Ω sampling resistor in the drain circuit, plotted on a linear scale against sample temperature for four baseband frequencies f_m = 100, 500, 2000, and 10,000 Hz.

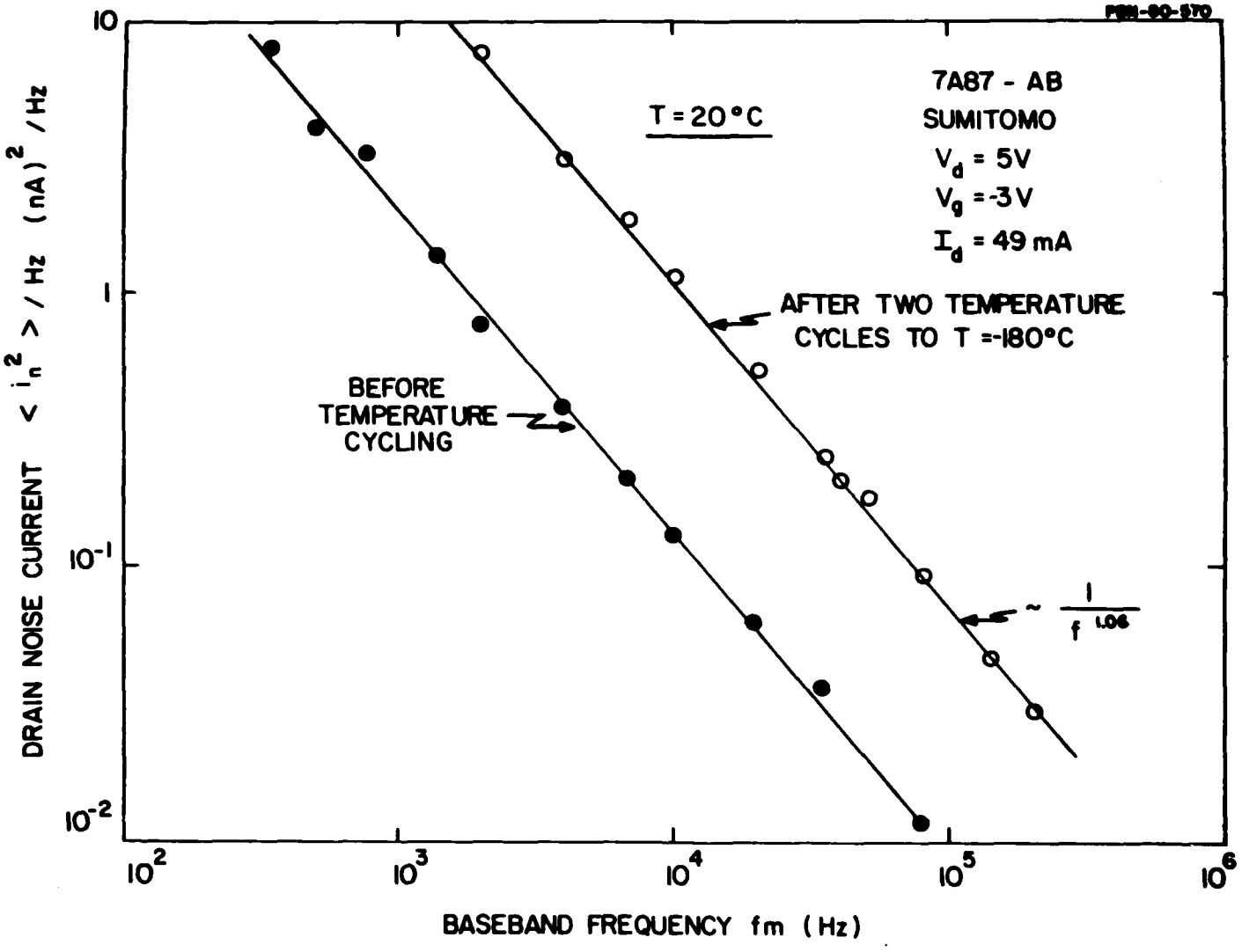


Figure 26. Degradation of baseband noise after two temperature cycles to T = -180°C.

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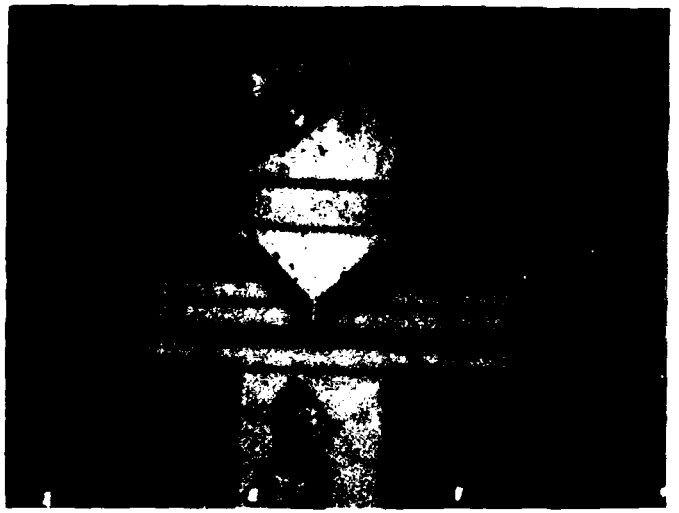
(a)



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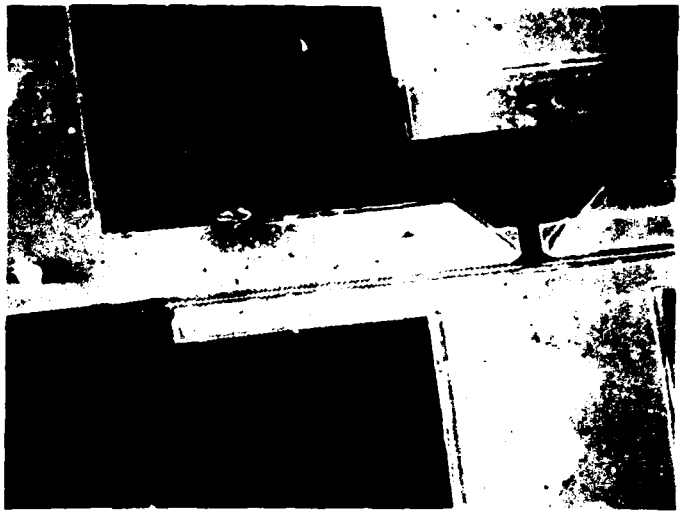
(b)



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(c)

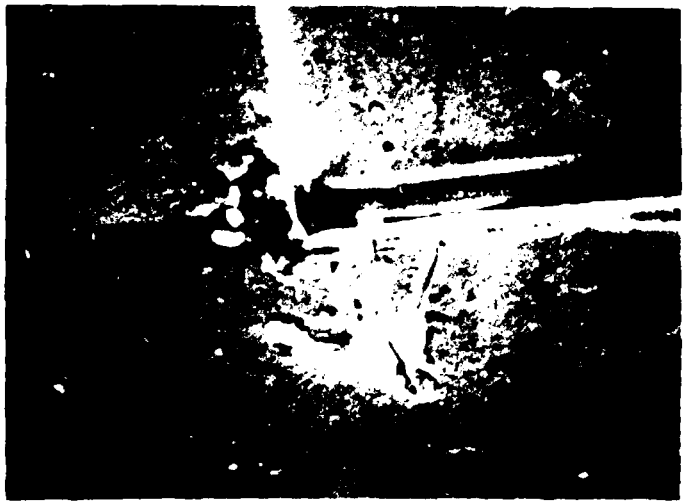


Figure 27. Effect of temperature cycling on SiO_x passivation layer of FET (wafer 7A87). (a) Topside photograph of FET after several temperature cycles to -180°C. (b) A SEM close-up view (200X) of a portion of topside surface of FET after several temperature cycles to T = -180°C. (c) A magnified view (300 X) of crack developed in oxide layer on topside surface of FET after several temperature cycles to T = -180°C.

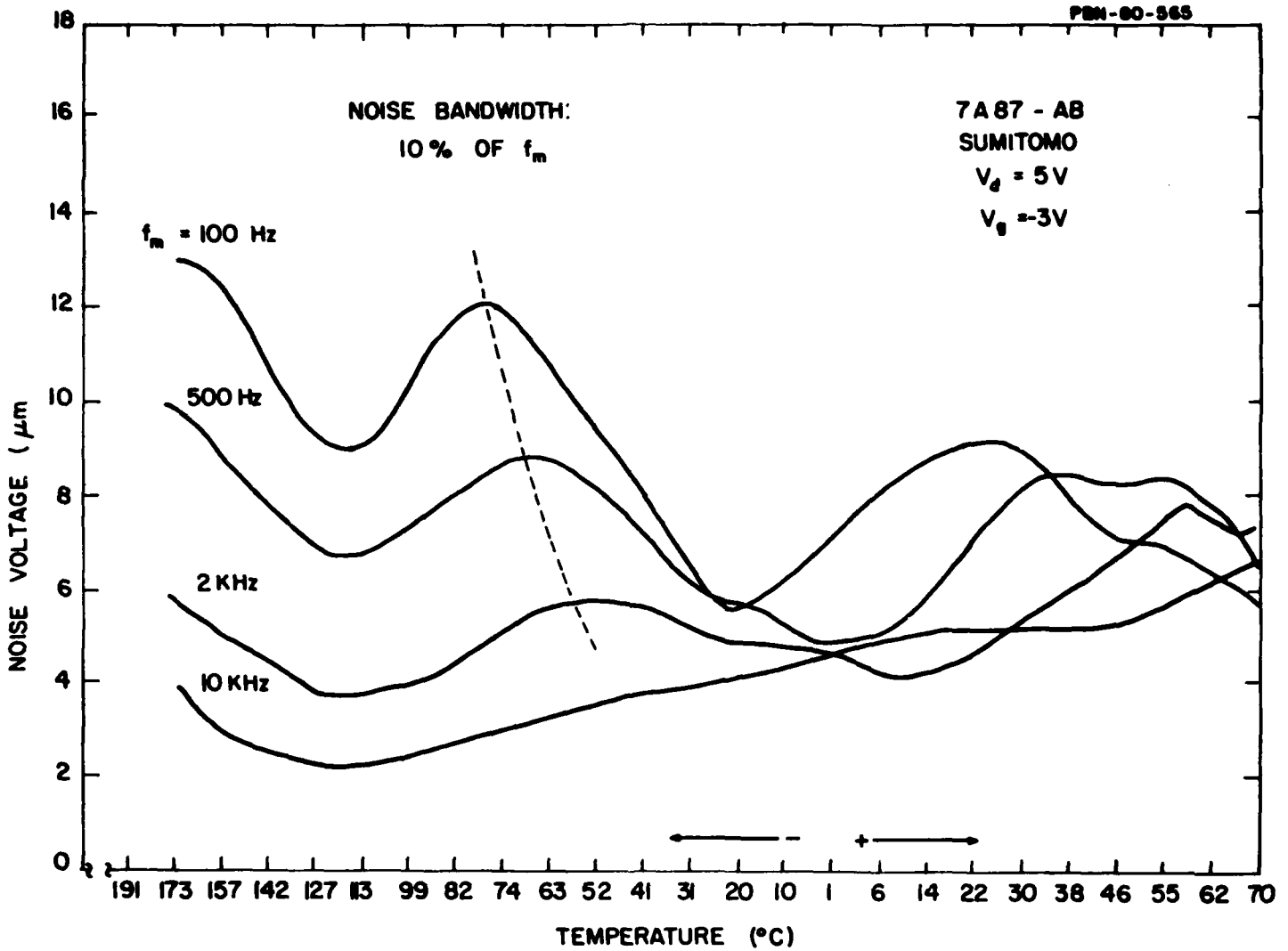


Figure 28. Baseband noise voltage across 50-ohm resistor in drain circuit as a function of device temperature and baseband frequency.

The striking feature of these graphs is the presence of the peaks and their shift to higher temperatures as the baseband frequency is increased. This phenomenon bears a close resemblance to the results reported for silicon junction FETs,[19] except that the peaks which we observed are less pronounced. In the reference cited, it was argued that traps in the depletion layer with a multiplicity of energy levels could account for the temperature dependence depicted in Fig. 28.

We repeated the temperature cycling on a commercial low-noise device manufactured by Raytheon's Special Microwave Devices Operation; this device had no passivation. As expected, negligible hysteresis of the noise data was observed.

4.5.5 Conclusions

No clear-cut evidence of trap levels could be found in the temperature scan data. The large increase in the 1/f noise level associated with "crazing" of the SiO_x passivation after repeated temperature cycling points clearly to stress-induced trap levels resulting from dissimilar expansion coefficients of the GaAs and the passivation layer.

4.6 Baseband Noise as a Function of Operating Bias Conditions

4.6.1 Introduction

The dependence of baseband noise on an extended range of operating bias conditions, that is, gate and drain voltages, was studied with the 7A87 devices. The measurements were confined to room temperature. These measurements cover a wider range of bias conditions than those discussed in Sec. 4.3

We measured the drain current noise as a function of bias voltages and baseband frequency. The noise levels, all normalized to 1 Hz bandwidth, were plotted on the device's I-V characteristic to provide a "map" of noise levels. Thus the noise distribution as a function of operating bias voltages and drain current can be seen at a glance. This was done for the baseband frequencies f_m = 500 Hz, 2 kHz, 10 kHz, 50 kHz and 100 kHz.

4.6.2 Experimental results

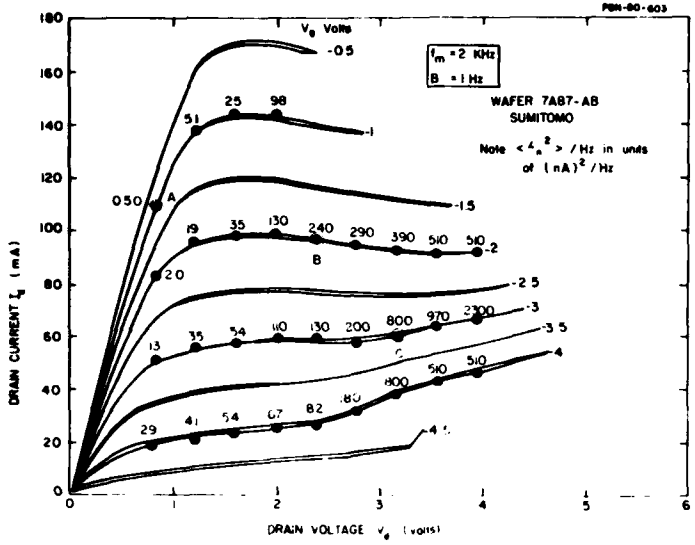
The measured results for f_m = 2 kHz, 10 kHz, and 50 kHz are depicted in Fig. 29. The data for the remaining frequencies fall in between and show the same trend with bias operating conditions. Note that the numbers represent the mean square noise current in units of $(nA)^2$ per Hz bandwidth.

Observe that for all frequencies shown the noise level generally increases in a monotonic fashion as one "travels" along a constant gate bias contour, starting from the origin. In particular, note that even though the current "saturates" above the knee, the noise level continues to increase, that is to say, the noise increases with drain bias. The monotonic increase in noise with drain bias was observed also by Christensson and Lundström[20] with n-channel silicon MOSFETs. These same investigators measured a monotonically decreasing noise level with increasing drain bias for p-channel MOSFETs.

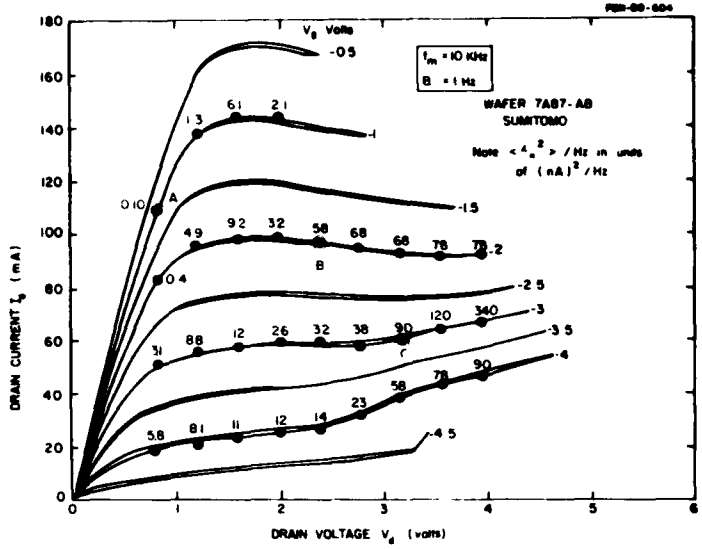
The noise level in our data exhibits a maximum as a function of reverse gate bias in the vicinity of V_g = -2 volts. These trends with gate bias, incidentally, do not agree with the reference cited, where a monotonic decrease with reverse bias occurs for a p-type channel and an increase for an n-type channel.

It is interesting to note that, in the vicinity of the upward "kinks" of the I-V characteristic, the noise level usually exhibits a jump in value. To determine whether a new noise mechanism is involved at the onset of the kinks, we have plotted in Fig. 30 the noise current versus baseband frequency for three bias conditions, (1) point A in Fig. 29 below the knee at V_g = 1.0 V, V_d = 0.8 V; (2) point B, in the current saturation region, at V_g = -2.0 V, V_d = 2.4 V; and (3) point C, in the kink region, V_g = -3.0 V, V_d = 3.2 V.

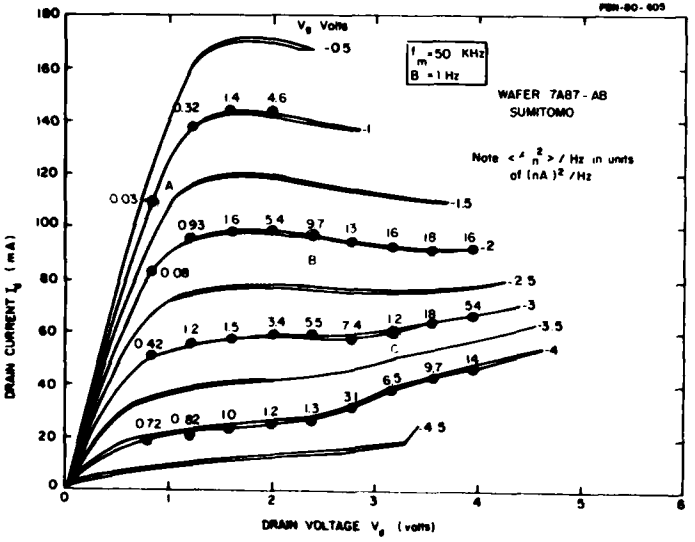
It is obvious that curves A and B follow a 1/f dependence closely, but curve C shows a faster drop-off with frequency. This suggests the possibility of a $1/f^2$ component "mixed in." It is tempting to invoke an avalanche mechanism for this additional noise component. However, avalanching of free carriers



(a) f_m = 2 kHz



(b) f_m = 10 kHz



(c) f_m = 50 kHz

Figure 29. A map of drain noise current as a function of gate and drain bias for three baseband frequencies. (Note: Noise current is normalized to a 1 Hz bandwidth).

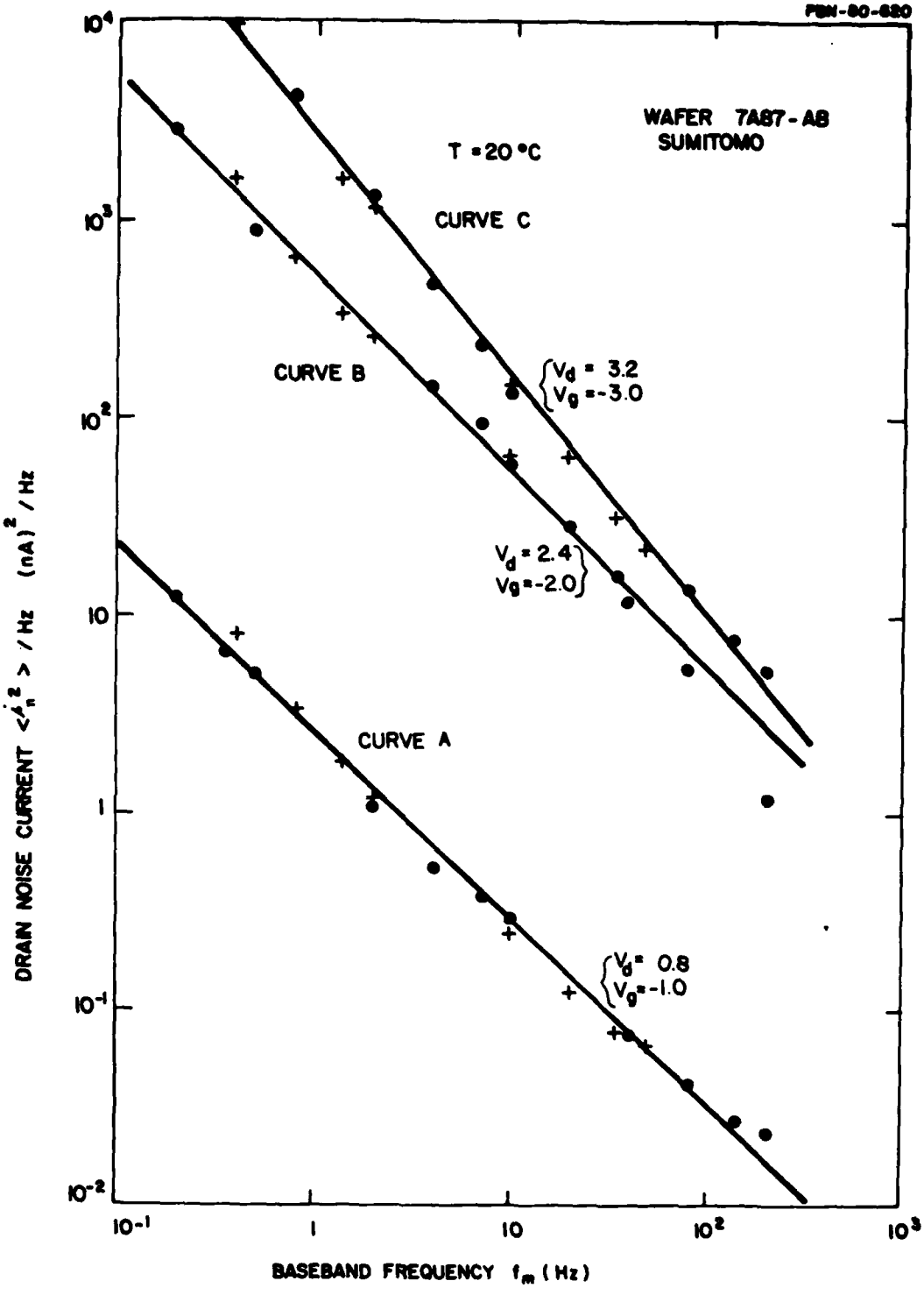


Figure 30. Drain noise current as a function of baseband frequency for three operating conditions, (1) below the knee, Curve A; (2) in the current saturation regim, Curve B; and (3) in the "kink" zone, Curve C.

produces a flat ("white") noise spectrum at low frequencies. On the other hand, if discrete, deep electron traps are present (and the likelihood is high that they are), then high field ionization[21] of these traps by barrier-lowering would lead to a noise spectrum of the form

$$\frac{A(E,T)}{1+\omega^2\tau^2} \tag{12}$$

where A is a function of the electric field E and temperature T among other things. Thus for $\omega\tau >> 1$, where τ is usually of the order of milliseconds, the spectrum would vary as $1/f^2$.

We have some corroborating evidence of the trap ionization mechanism. An (unpassivated) Raytheon commercial design low-noise FET, exhibiting no kinks in the I-V characteristic, was measured, Fig. 31(a). The noise, replotted as a function of frequency, Fig. 31(b), shows a gradual, nearly linear increase in noise with drain bias, Fig. 31(b). The frequency dependence of the noise, though not $1/f^2$, was closer to $1/f^{1.5}$ than to 1/f.

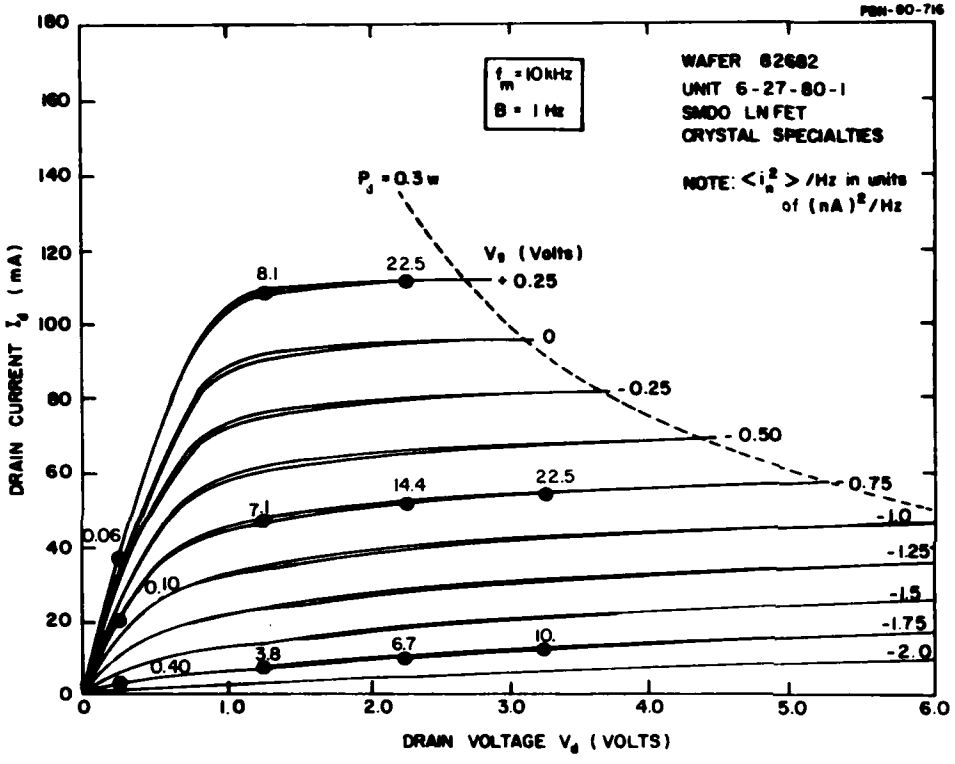
4.6.3 Conclusion

The bias dependence of baseband noise in a GaAs FET is similar to that for a silicon FET. This dependence shows a monotonic increase with drain bias and a maximum with reverse gate bias at approximately half pinch off. At large drain bias voltages, a rapid increase is observed with increasing drain bias, which coincides with an increasing slope in the I-V characteristic, implying that an onset of discrete trap noise generation may be the cause. This conclusion is supported by a trend from a 1/f to a $1/f^2$ frequency dependence of the noise at high drain voltages.

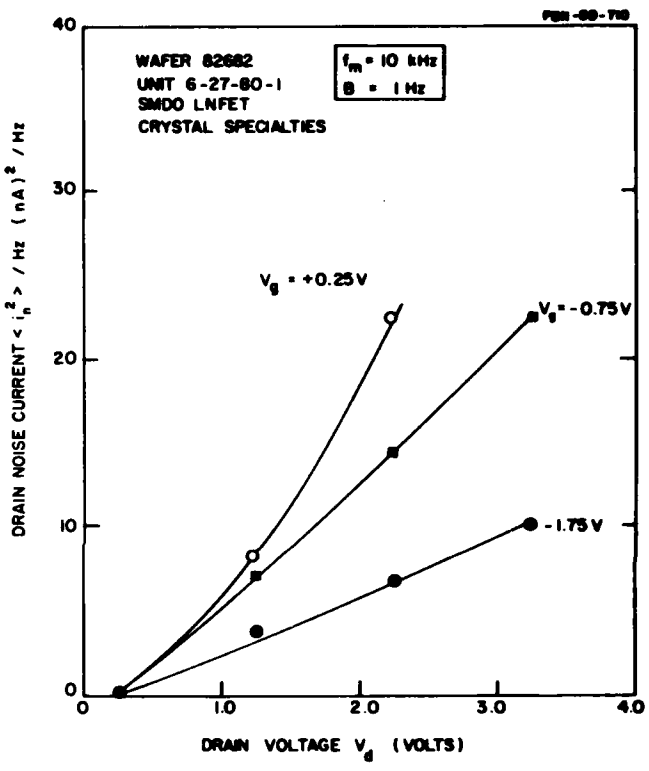
4.7 Baseband Noise as a Function of Optical Excitation

4.7.1 Introduction

We have conducted simple optical experiments with FETs. Our purpose



(a) Map of noise superimposed on I-V characteristics.



(b) Replotted data as a function of drain bias and gate bias.

Figure 31. Drain noise current as a function of operating voltages for a commercial low-noise FET.

was to determine what, if any, effect optical illumination of the FET had on the baseband noise. If traps are present on the surface and within the channel layer, then by optical excitation of them, and the subsequent (random) capture of the electrons by the traps, additional baseband noise would be generated. The optical excitation consisted of exposing the top surface of an FET to a focussed beam of light and monitoring the change in the baseband noise and in the drain current.

Two sources of optical excitation were used. In the first set of experiments the light source used was a tungsten microscope lamp whose (dc) bias current was varied in steps, and, hence, whose intensity could be varied. Since this light covers a broad band of frequencies almost equivalent, in energy spread to the band gap, it at least would indicate the presence of most trapping centers within the band gap. On the basis of our findings, we could then determine whether further experiments with monochromatic light could be used to pin-point the levels of the traps.

The second set of experiments were conducted with a more sophisticated set-up. We converted our optical system to a tunable monochromatic light source and included a telescopic lens system to focus the light on the chip. A block diagram of the system is shown in Fig. 32 and a photograph in Fig. 33. The basic measuring system consists of a microscope illuminator, followed by a two-element collimator consisting of a glass telescope and a CaF_2 lens, then a monochromator and a second CaF_2 lens, the whole providing a collimated beam on the sample. The monochromator consisted of a Perkin-Elmer spectrophotometer having a KBr prism with a resultant tuning range (mechanical) of 0.5 to 20 μm. Intensity was varied by modulating the illuminator power; optical bandwidth control was by a variable slit.

Our initial experiments with the monochromatic light source were limited to the wavelength range 0.55 μm to 2 μm. By removing the glass telescopic lens system, we later extended this range to 6 μm, at some loss of beam intensity.

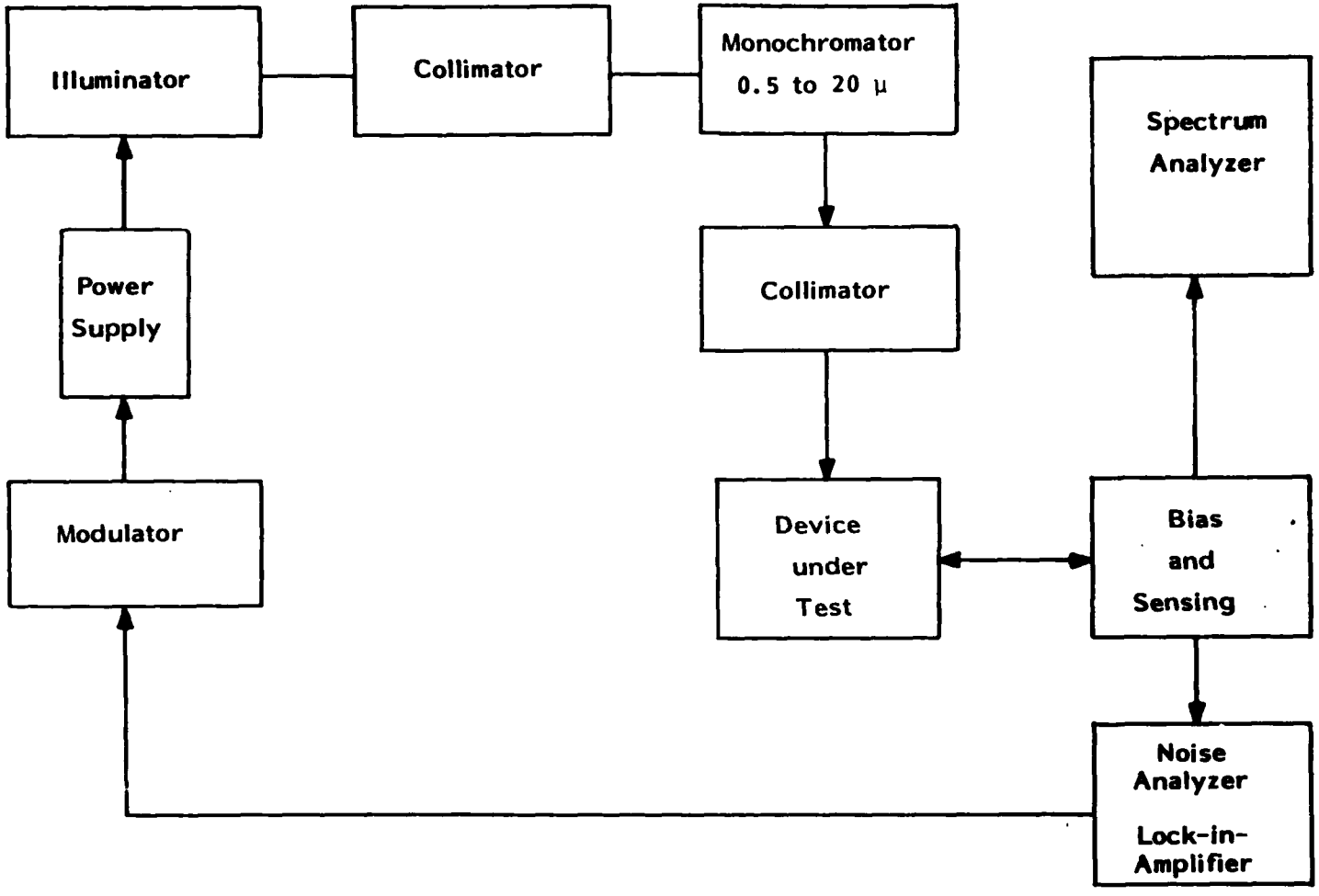


Figure 32. Block diagram of the tunable light monochromatic light source.

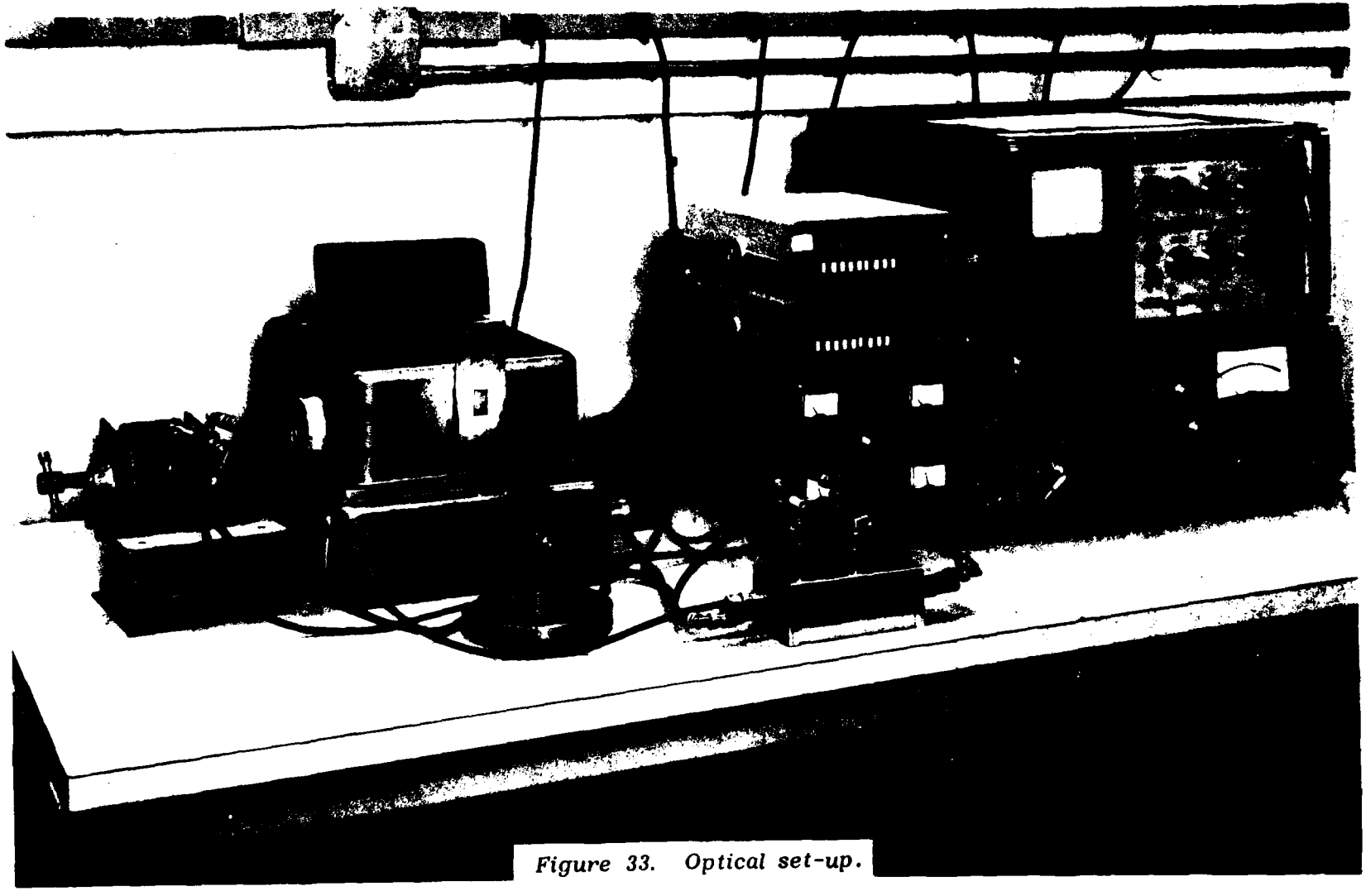


Figure 33. Optical set-up.

Drain current changes with illumination were monitored by dc instrumentation, coupled with a power supply which could be operated in either the constant voltage or constant-current mode. When operated in the constant-voltage mode, drain circuit noise was displayed on a spectrum analyzer and simultaneously processed by a lock-in amplifier operating as a tuned, bandpass, low frequency detector. This lock-in amplifier could be used to integrate all the noise (below 100 kHz) or operated as a synchronous detector wherein it provides a signal to modulate either the illuminator or device power supplies.

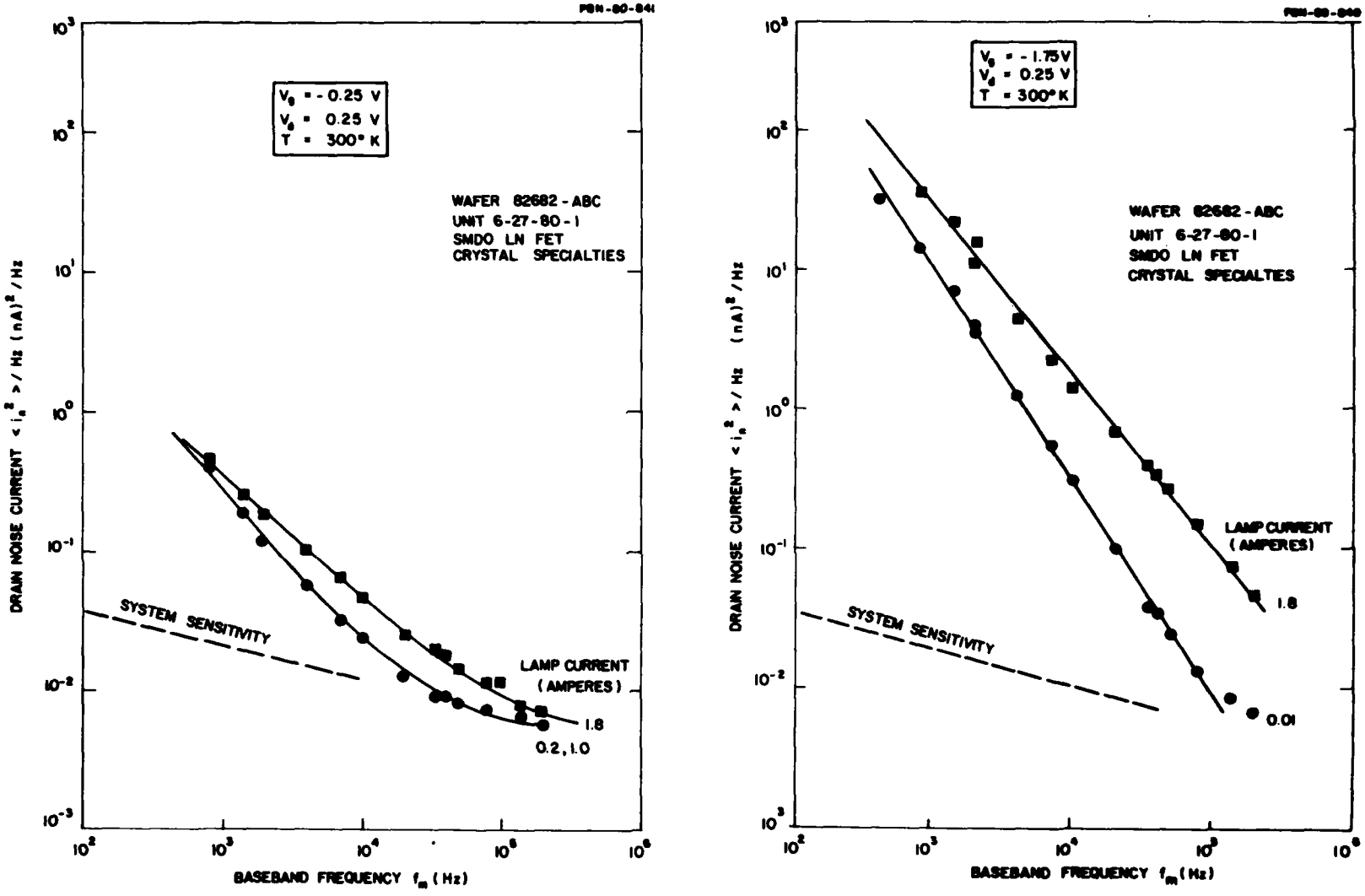
4.7.2 White light excitation

All experiments were performed on a low-noise 500 μm periphery device with a buffer layer and a highly-doped contact layer over the channel layer. The doping level was approximately the same as all previous devices, that is, $10^{17}/cm^3$. The device was unpassivated. The substrate used was obtained from Crystal Specialties. The wafer run was designated 82682-ABC. (This is the commercial design device discussed in Sec. 4.6.2).

The measurements were made at room temperature for several bias conditions, namely, above the "knee," V_d = 3.25 V, and below the knee, V_d = 0.25 V. Two gate bias voltages were used, one corresponding to $I_d \approx I_{dss}$, namely, V_g = -0.75 V, and one near pinchoff, V_g = -1.75 V. [see Fig. 31(a)].

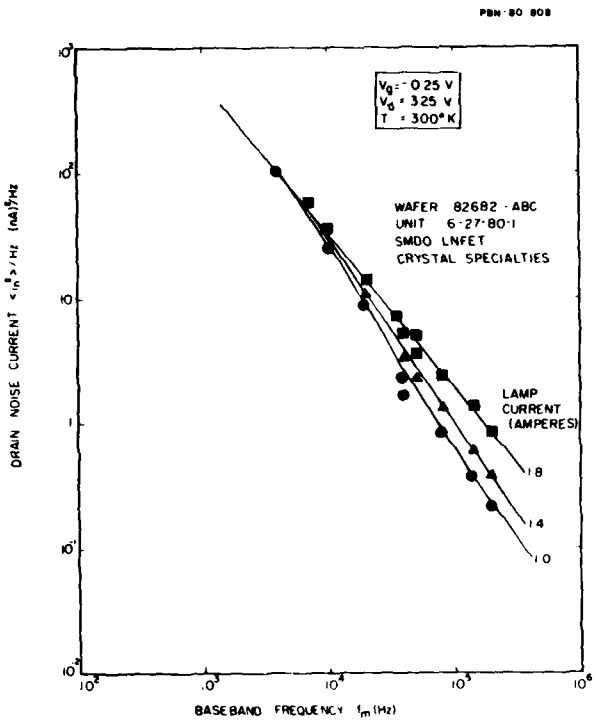
The baseband noise was measured over the range from 100 Hz to 10^6 Hz, for lamp currents of 0.2 - 1.0, 1.4 and 1.8 amperes. The lowest current range corresponds to no perceptible illumination as determined by the naked eye. Figures 34 and 35 display graphically the results obtained for below the knee, V_d = 0.25 V, and above the knee, V_d = 3.25 V, respectively.

Aside from the fact that the noise level is substantially lower below the knee, in all four cases the noise level increased with increased illumination, as expected. This indicates, of course, that some of the traps which are present are being excited sufficiently to release electrons to the conduction band.

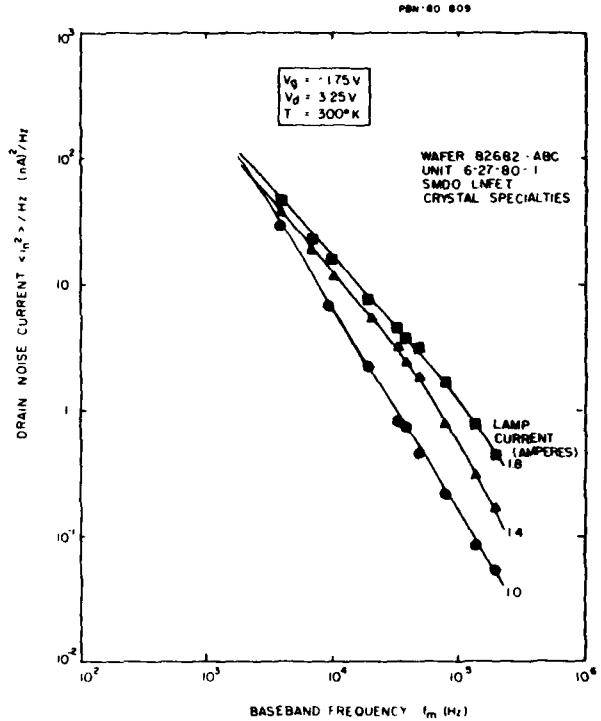


(a) Vg = -0.25 V *(b) Vg = -1.75 V*

Figure 34. Baseband noise current as a function of baseband frequency and (white light) illumination for a drain bias below the knee V_d = 0.25 V and for two gate bias conditions.



(a) $V_g = -0.25$ V



(b) $V_g = -1.75$ V

Figure 35. Baseband noise current as a function of baseband frequency and (white light) illumination for a drain bias above the knee, V_d = 3.25 V, and for two gate bias conditions.

A distinctive feature of the curves above the knee is that the noise increases with illumination only above a certain frequency range centered around 5 kHz. Below this range, the illumination has little or no effect. Furthermore, the noise above this range changes from a near $1/f^2$ dependence on frequency to a slower drop-off rate, but faster than 1/f. The change in slope is more pronounced at the low gate bias.

On the other hand, below the knee, the noise increases with illumination over the entire frequency band and approaches a 1/f dependence more closely. The curvature at the high frequency end for $V_g = -0.75$ V is not representative of the device, but rather of the background limiting noise of the measuring system which dominates because of the low noise level of the device.

What is the reason for the threshold frequency range for Figs. 34(a) and 34(b)? A possible explanation is as follows. When traps are excited within the bulk, surface states attempt to readjust their level with respect to the Fermi level to compensate for the change in bulk trap occupancy (net change). Since surface states are generally slower than bulk states, their compensation will be more effective at low frequencies than at high. That is to say, they will not be able to follow the high frequency components of the random variation of the bulk trap occupancy, hence noise components corresponding to these frequencies will be present upon illumination. Why this compensation does not show up below the knee is not understood.

4.7.3 Monochromatic light excitation

In our initial experiments with this tunable source (before noise measurements were taken), we first observed changes in the dc drain current. In all cases the changes observed were slight dips in the current. In the 0.5 to 2.0 μm wavelength range, these dips occurred at $\lambda = 0.52$ μm, $\lambda = 0.83$ μm, and $\lambda = 1.2$ μm. In units of electron volts, these correspond to 2.38 eV, 1.49 eV, and 1.03 eV, as can be calculated from the expression

$$E = \frac{hc}{\lambda} = \frac{1.239}{\lambda} \text{ (eV)} \qquad (13)$$

where λ is expressed in μm.

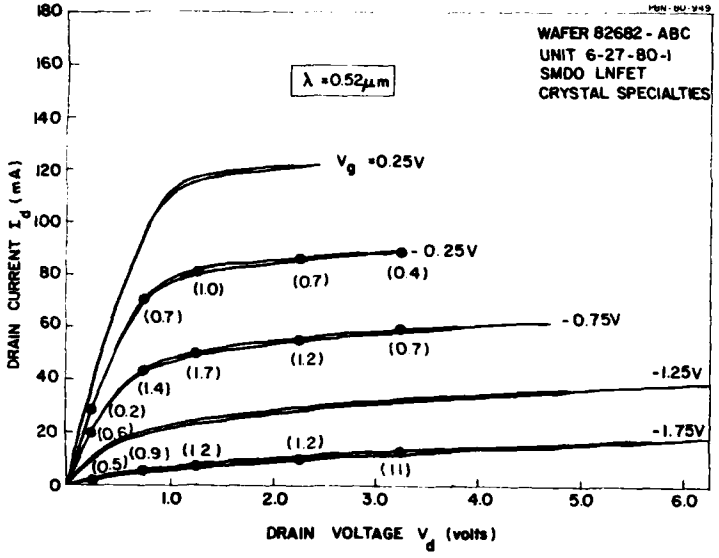
The changes in drain current for these three wavelengths at various gate and drain bias conditions, namely V_g = -0.25, -0.75, and -1.25 V, and V_d = 0.75, 1.25, 2.25, and 3.25 V, are indicated in Fig. 36.

The first thing to notice is that the current dip is of the same order of magnitude in all cases, with variations that follow no particular pattern as the bias conditions are varied. However, the changes are somewhat larger for λ = 0.52, but this might be a result of light intensity variations with wavelength. (No attempt was made to maintain light intensity constant within the optical tuning range.) Because of the relative constancy of the dip with gate bias, it is obvious that the percentage change in drain current is rather large near pinchoff.

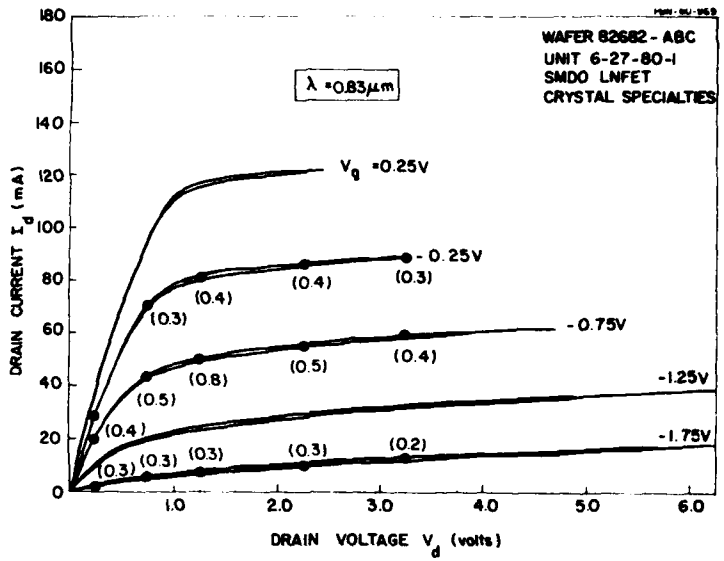
What might these current dips signify? First, it is clear that with the shorter wavelengths, the corresponding energy exceeds the band gap. Thus electron-hole pairs are created, with the electrons elevated to the conduction band. If no traps were present, these additional electron-hole pairs would cause an increase in (channel) drain current, which is not observed. This case is indicated in Fig. 37(a). Suppose, however, that electron traps were present. Clearly, if the electron drops back into a trap, as indicated in Fig. 37(b), this would neutralize the effect of a donor (decrease in doping density) during the time the electron remains trapped, that is, before recombining with a hole. This would cause a decrease in drain current, as observed.

Since the absorption coefficient is extremely high for wavelengths "outside" of the band gap, λ = 0.9 μm (E_g = 1.43 eV), this trapping phenomenon must involve traps near the surface.

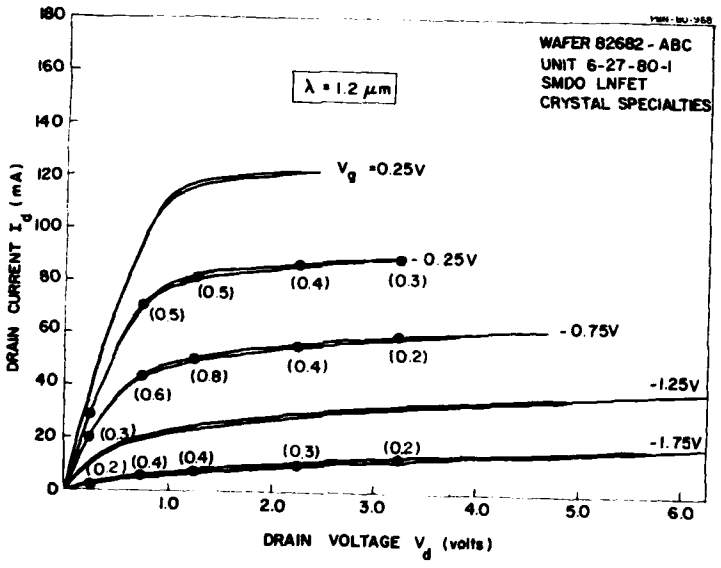
On the other hand, for λ = 1.2 μm, the energy change is less than the band gap. Therefore, light penetration is far into the GaAs material. Also, since λ > 0.9 μm, the current dips again, implying trapping of electrons. However, in this case the transition into the trap from the valence band is direct, as indicated in Fig. 37(c). This implies an electron trap at a level



(a) $\lambda = 0.52\ \mu m$

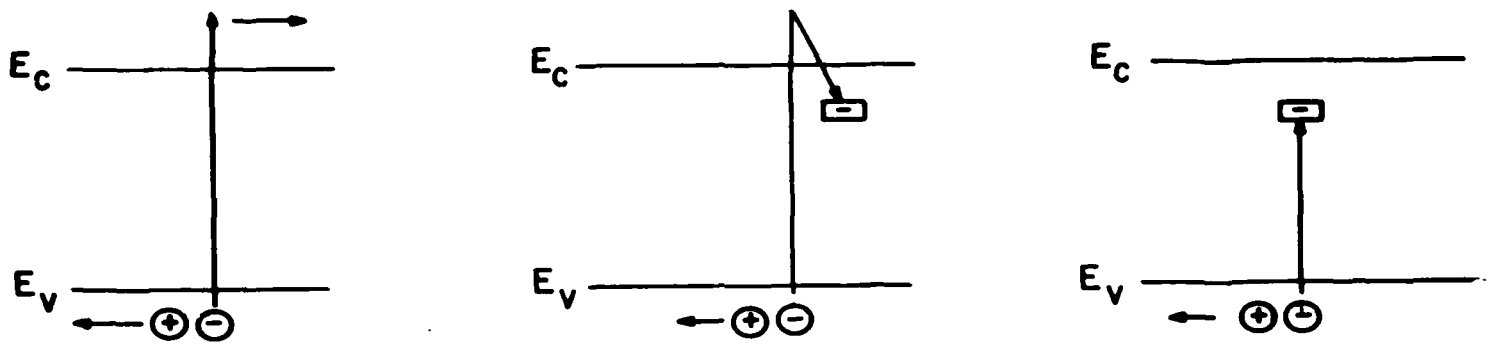


(b) $\lambda = 0.83\ \mu m$



(c) $\lambda = 1.2\ \mu m$

Figure 36. I-V characteristics showing in parentheses the dip in drain current (in milliamperes) when the FET is illuminated by a monochromatic light of the indicated wavelength.



(a) Increase in drain current by optical excitation for $\lambda < \lambda_{gap}$

(b) Decrease in drain current by optical excitation for $\lambda = \lambda_{gap}$

(c) Decrease in drain current by optical excitation for $\lambda > \lambda_{gap}$

Figure 37. Possible mechanism for drain current changes with optical illumination involving electron traps.

E_g - 1.03 = 0.40 eV below the conduction band edge. There are two electron trap levels near this level, the so-called levels EB6 and EI1, as reported by Martin et al.,[22] but not identified by them. An electron trap level near this level (0.41 eV) has been observed by Christou et al.[23] They have classified it as an interface bulk trap which is introduced when a Au-Ta Schottky gate metallization is used on n/n^+ GaAs. However, the present devices use Al gates.

We point out that hole traps cannot be responsible for the current dips, as they would produce a current increase, which is contrary to our observation.

We should mention that once a threshold of illumination has been reached, further increases in light intensity would produce no discernible additional change in drain current. This would indicate that all of the traps involved in that particular transition were filled.

We have examined in more detail the variation in drain current with optical wavelength by biassing the FET at a fixed operating point (above the knee) at V_d = 2.25 V, V_g = -1.75 V, and tuning the wavelength over its full range. The results are shown in the upper half of Fig. 38. Also shown is the variation of the mean square value of the drain noise current measured at f_m = 100 kHz. The bias conditions are near pinchoff, V_g = -1.75 V, V_d = 2.25 V [see Fig. 31(a)].

Some hysteresis was observed in the drain current as the optical wavelength was scanned in opposite directions. As will be noted, the only noise peaks observed are those at λ = 1.28 μm, λ = 0.81 μm, and λ = 0.52 μm. Of these three, only the first corresponds to an electron trap as indicated by the mechanism shown in Fig. 37(c). This corresponds to a trap level of E_t = E_g - 1.239/λ = 1.43 - 1.239/1.28 = 0.46 = eV below the conduction band. This is probably the same level as deduced before, if experimental and graphical errors are taken into account. Because the remaining two wavelengths are less than that corresponding to the band gap, $\lambda < \lambda_g$ = 0.9 μm, the light is absorbed near the surface. Therefore the corresponding noise peaks (rightmost

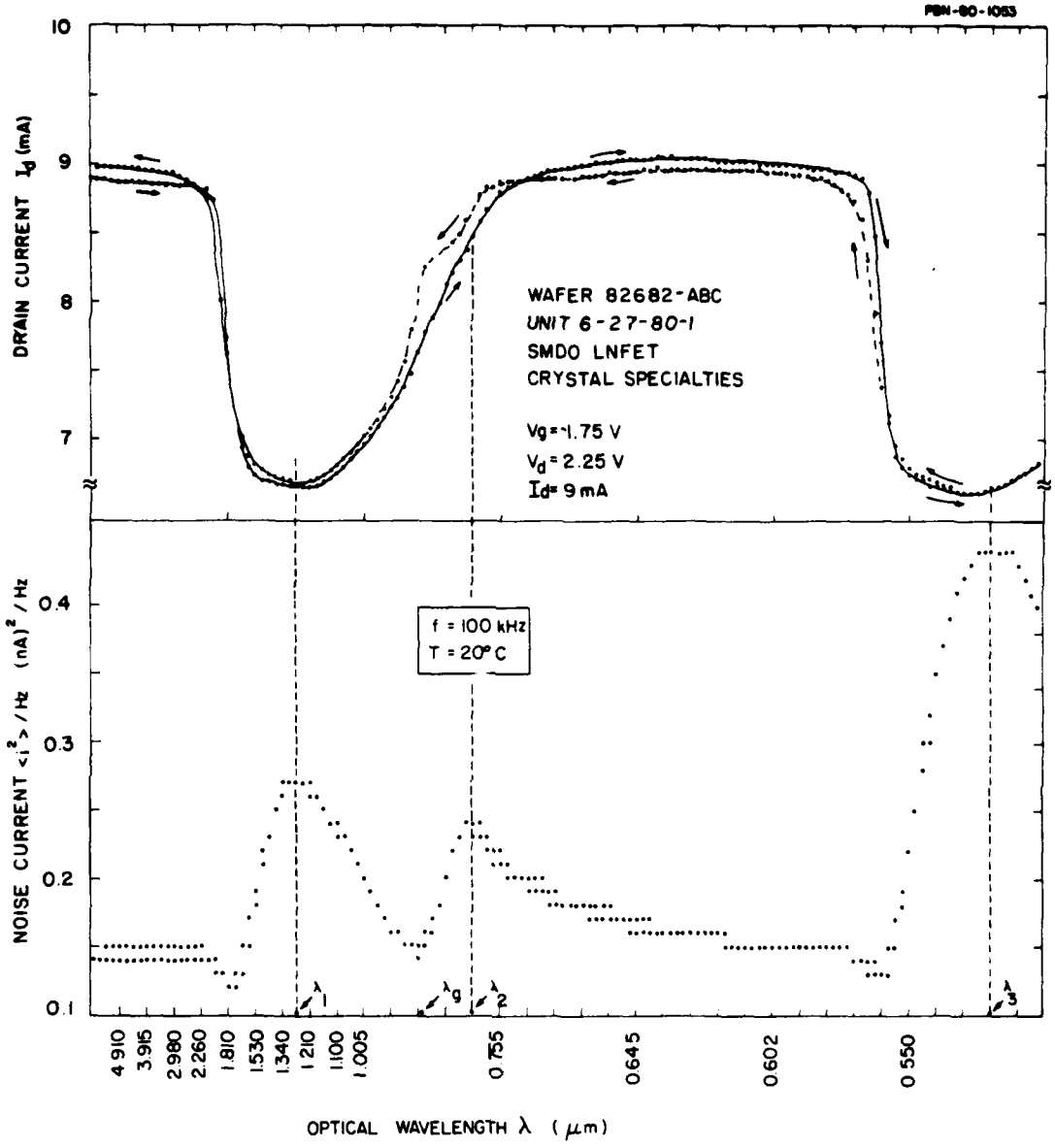


Figure 38. Effect of optical illumination on the drain current and drain noise current of a low-noise FET, for V_g = -1.75 V, V_d = 2.25 V, and baseband frequency f_m = 100 kHz.

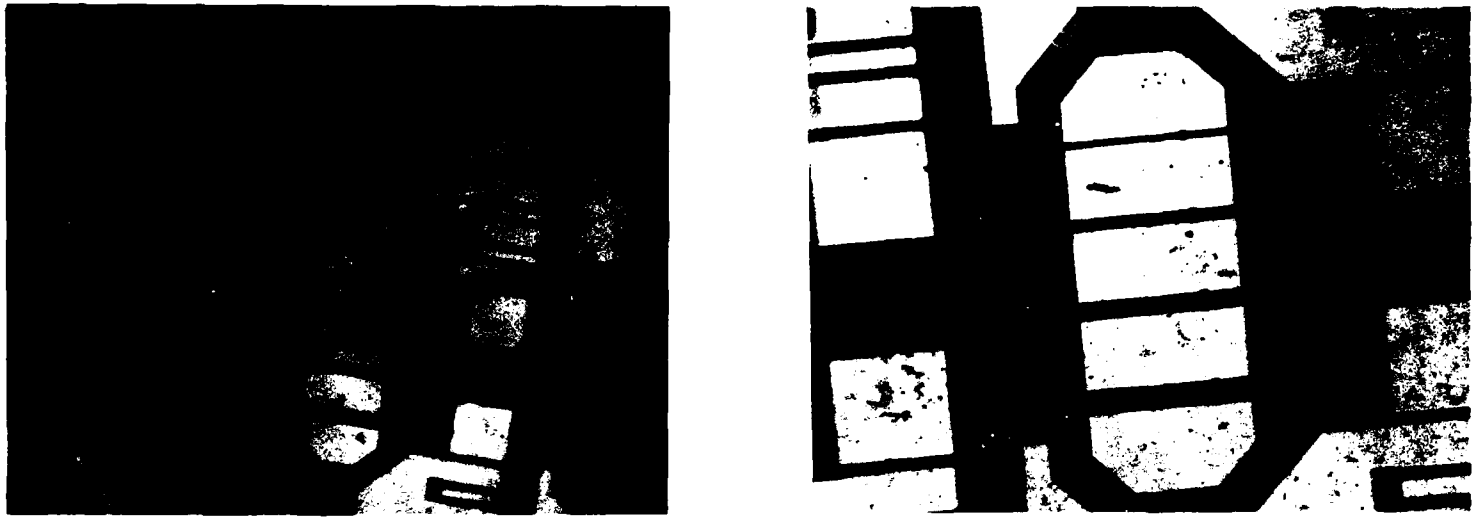
peaks in Fig. 38) must involve surface traps.

No electron traps have been reported by others further than 0.9 eV from the conduction band edge,[22] which would correspond to a noise peak at $\lambda = 1.239/(Eg-0.9) = 1.239/(1.43-0.9) = 2.34$ μm; therefore our scan to $\lambda = 5.0$ μm would seem to be sufficient. Since we have not found any peaks beyond $\lambda = 1.28$ μm, even though a multitude of trap levels in this range have been observed by other methods such as DLTS,[22] it can only be surmised that other trap levels either are not present in our device, or are not excited, or do not produce noise.

There is a possibility that traps in the channel region under the gate are not exposed to the optical illumination. These traps certainly show up in DLTS measurements. To determine whether this is a possibility would require a transparent gate, that is, one with sufficiently thin metallization to allow some light to pass through. The next best thing is a structure which has no gate at all, such as a contact test sample having approximately the spacing of the source-drain pads of an FET.

Figure 39 illustrates such a structure. Figure 39(a) is a microscope photograph of a piece of wafer containing a number of contact test samples used in another program. Figure 39(b) is a close-up of one of the test samples used in our noise experiments. This sample contains a pair of Ni-Au-Ge-Ni-Au contacts separated by 5 μm. To each pad, a one-mil-diameter gold wire is bonded. The opposite end of each wire is bonded to a metallized pad on an underlying alumina substrate.

The contact specimens are fabricated on a GaAs wafer obtained from Crystal Specialties. The epitaxial layer deposited on it consists of three layers, a contact layer doped to 5×10^{17} cm^{-3}, an active layer ($n = 5.5 \times 10^{16} cm^{-3}$), and a buffer layer ($n = 3 \times 10^{14} cm^{-3}$). Note that the doping level of the contact and active layers is somewhat lower than that used in FETs. The dopant used in these layers is silicon, and in the buffer layer, NH_3. The substrate is Cr-doped. The buffer layer is 7 μm thick.



(a) (b)

Figure 39. Photographs of a wafer of contact samples (a), and a single contact sample (b) taken under a microscope. Wafer of samples is mounted on an alumina substrate, and sample under test is wire bonded to pads on alumina substrate.

The I-V characteristic of the sample (actually one similar to the sample tested) is illustrated in Fig. 40(a). The dashed line is a straight line denoting an ohmic contact. Because the test sample was mounted on an alumina substrate, it was not possible to extend the I-V characteristic into the current saturation regime, because of the danger of burnout. One might consider the curve depicted as corresponding to the region below the knee of the FET I-V characteristic for zero gate bias.

The region between the two contacts was exposed to the optical illumination. The operating point was that corresponding to the dot in Fig. 40(a) namely, $V \cong 0.55$ V, $I \cong 20$ mA. Figure 40(b) shows how the noise voltage developed across the sample varies as the optical wavelength is varied. Because of the low noise level, a 2 Hz modulation was superimposed on the optical signal, and a lock-in amplifier was used. Thus the baseband noise measurement frequency was 2 Hz, substantially lower than that normally tested. Notice that the horizontal axis is a linear scale of wavelength.

Observe that no noise peak appears at the wavelengths for which the FET noise exhibited peaks. Indeed, the only definite peak is that at $\lambda = 0.792$ μm, or $E = 1.56$ eV — slightly above the band gap. The minor peaks below this value are not considered real, but merely scatter in the noise data.

What does this mean? It could mean that certain trap levels may be introduced by the technology used for fabricating the gate, possibly in the interface layer between the Schottky gate and the underlying channel region, or on the surface region adjacent to the gate. The experiments of Christou et al.[23] certainly indicate this, but further study relating the method of gate fabrication and 1/f noise is necessary. To carry out such a study, it would be helpful to use a very thin gate metallization (several hundred Angstroms) and a much more intense light source to be able to excite the interfacial (metal-GaAs) trap through the gate electrode.

We repeated some of these experiments with devices fabricated on Sumitomo substrates. One of these devices from wafer 7A87-AB, was described earlier in Sec. 4.5, when temperature experiments were discussed. The second sample

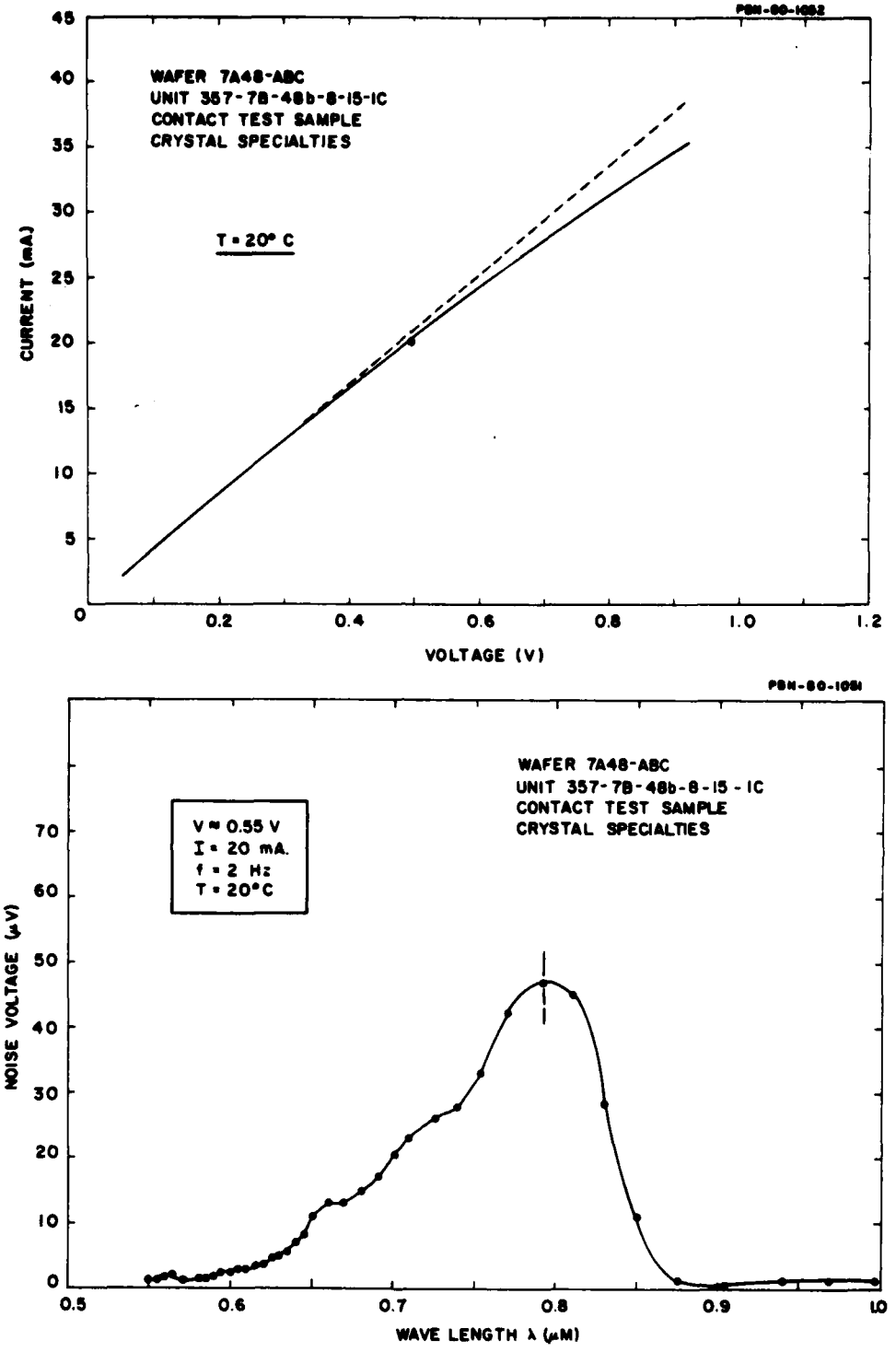


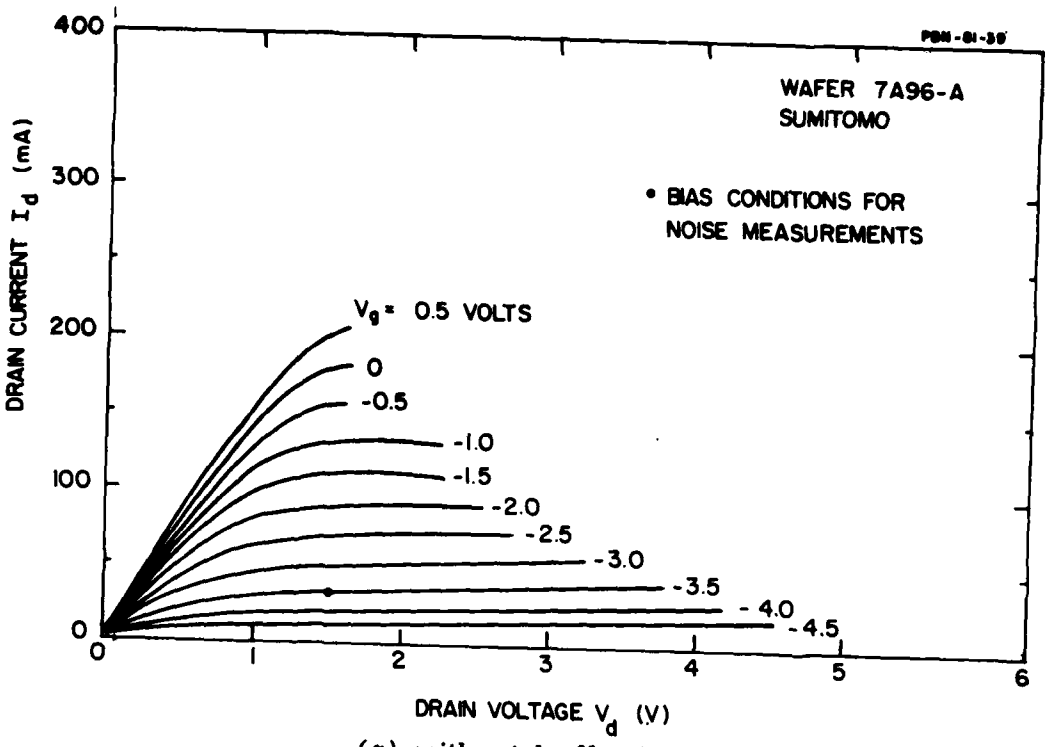
Figure 40. I-V characteristic (a) and noise voltage (b) as a function of optical wavelength for a "gateless" FET (contact sample). In (a) the operating point for noise measurements is indicated by the dot.

was from wafer 7A96-A. This wafer differed from 7A87-AB only in that it lacked a buffer layer. The I-V characteristics of the two devices are shown in Fig. 41.

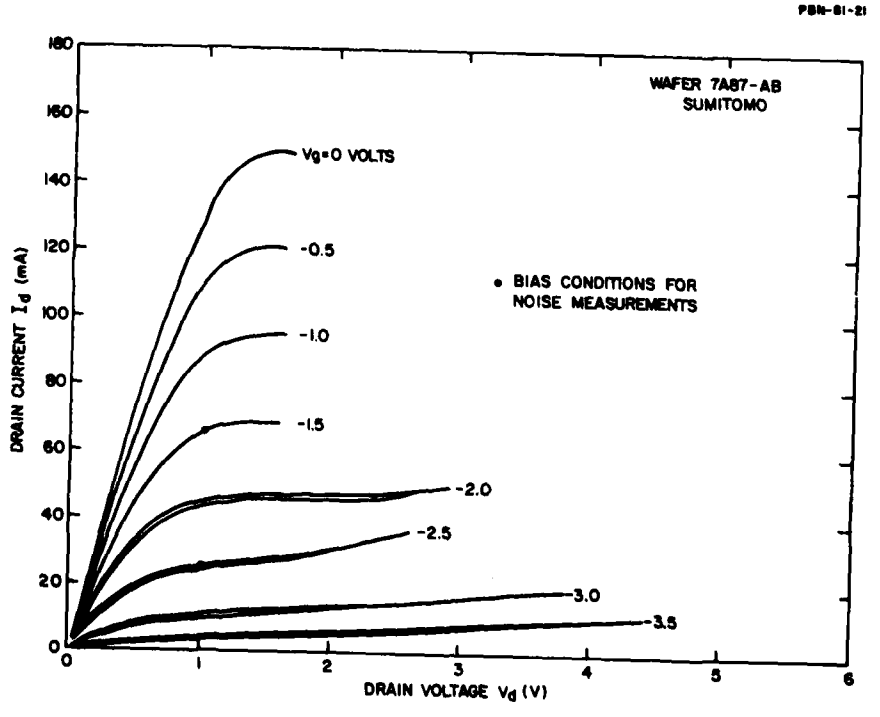
Figures 42(a) and (b) are plots of the noise voltage across a 50-Ω resistor in the drain circuit as a function of the wavelength of the optical excitation for the unbuffered and buffered devices, respectively. Although slight peaks are observed, they are so slight as to be questionable. Certainly variations as large as the previous device are not found. Therefore no conclusions can be reached with respect to trap levels.

4.7.4 Conclusions

The effect of optical illumination on baseband noise has been disappointingly small. Although an electron trap level at approximately 0.41 eV below the conduction band has been noted, the small changes in noise level indicate that if traps are responsible for 1/f noise in FETs, we were not able to excite them. A possibility is that these traps may be associated with the interfacial region under the gate[23] and hence were inaccessible. We therefore recommend that to test this hypothesis one or more of the following approaches should be tried: (1) use a thin gate metallization to allow optical excitation through the gate metal; (2) illuminate the gate from the (unmetallized) back side; (3) vary the gate metallization technology and measure the changes (if any) in the baseband noise level.

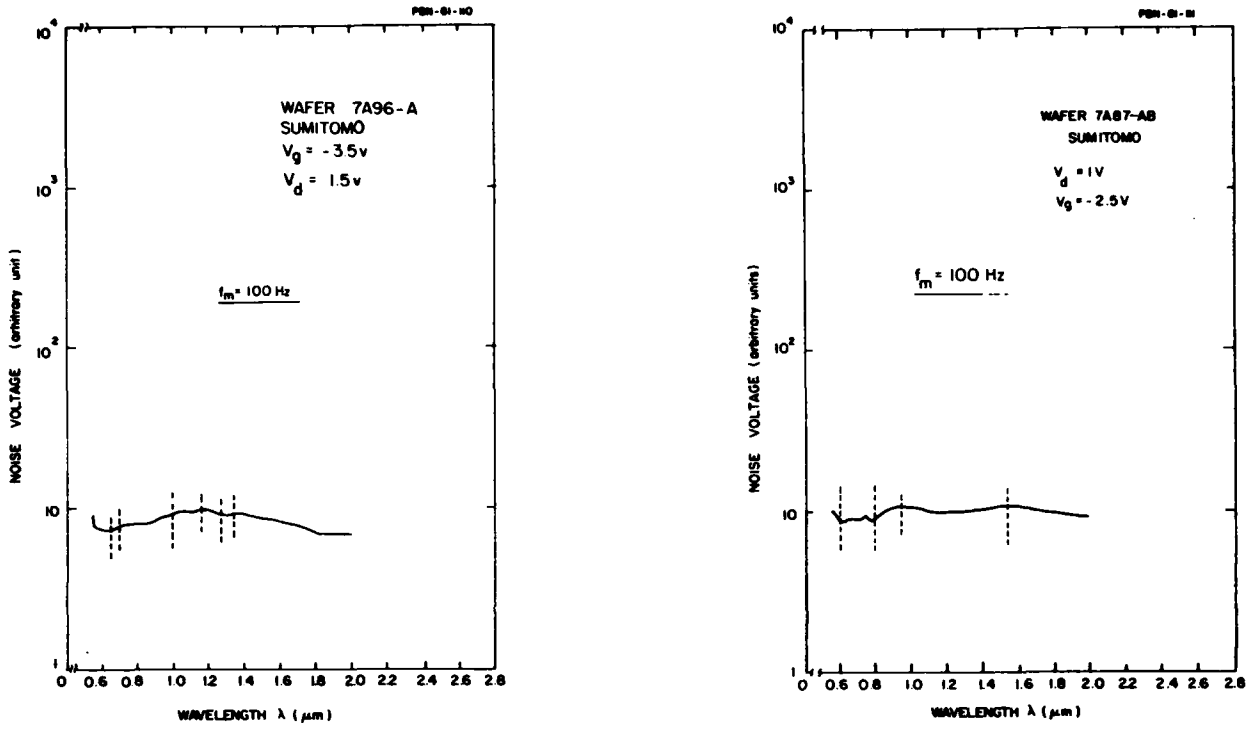


(a) without buffer layer



(b) with buffer layer

Figure 41. I-V characteristics of two 500 μm periphery FETs on Sumitomo substrates.



(a) without buffer layer

(b) with buffer layer

Figure 42. Noise voltage developed across 50 ohm resistor in drain circuit of FET as a function of wavelength of monochromatic illumination source. Measurements taken at baseband frequency of 100 Hz. (DC source for illuminator).

5.0 NOISE SOURCE MODELLING

5.1 Introduction

We shall describe some interesting experimental results which point to depletion layer modulation by traps as the primary mechanism by which baseband noise is translated to the rf band. This mechanism was postulated earlier in Sec. 2.0. The experimental results, in addition to providing more physical insight to the modulation process, also yield quantitative data which is used in the mathematical model of trap noise generation to be discussed below.

5.2 Baseband Upconversion Model

A series of experiments were carried out to determine whether the low-frequency baseband noise (1/f component) manifests itself as a near-carrier 1/f component, and to ascertain the degree or depth of this modulation. For this purpose, we used a simple technique proposed by Scherer[18] which was outlined in Sec. 2.0.

We assume that the modulation of the depletion layer is equivalent to a modulation of the source-gate potential. (Note that in our experiment we use a common gate oscillator.) This depletion layer modulation is proportional to the modulation of the source-gate capacitance, that is

$$\Delta C_{sg} \propto \Delta V_{sg} \tag{14}$$

where Δ denotes a small fluctuation. (From here on, we consider Δ to be a random fluctuation, and we must consider only statistical averages, which we denote by the symbols $< >$.)

We postulate that the measured baseband drain current noise is caused by a fluctuation in the depletion layer, which also causes a random fluctuation is the source-gate capacitance. This randomness in the gate capacitance we believe to be the major cause of the near-carrier FM noise, since it produces a low frequency modulation of the carrier frequency.

Pursuing this model, we may relate the fluctuation in the voltage drop across the depletion layer, ΔV_{sg}, to the fluctuation in the drain current via the transconductance g_m

$$<\Delta^2 i_d(f_m)> = g_m^2 (f_m)<\Delta^2 V_{sg}(f_m)> \qquad (15)$$

where, of course, f_m is the particular frequency component in the noise at baseband. Note that to be general we must ascribe a possible frequency dependence to g_m, although we did not measure any such dependence up to 40 kHz. Equation (15) implies a 1-Hz bandwidth, i.e. B = 1.

By inverting Eq. (15) we may determine the "equivalent" gate noise voltage, v_n

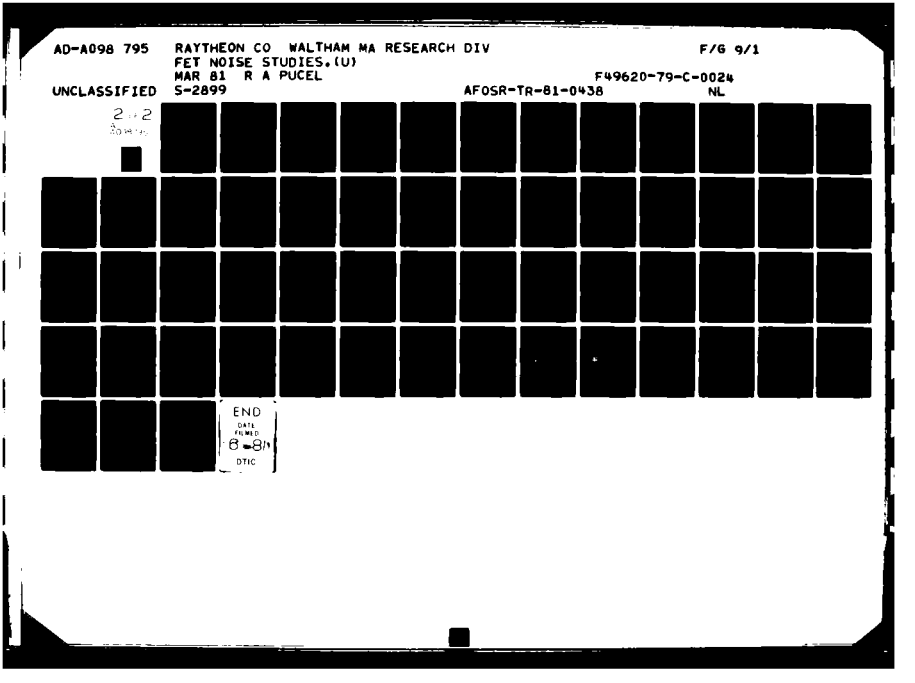
$$v_n = \sqrt{<\Delta^2 V_{sg}(f_m)>} = \sqrt{\frac{<\Delta^2 i_d(f_m)>}{g_m^2 (f_m)}} \qquad (16)$$

Note that many experimenters prefer to represent baseband FET noise in terms of the equivalent gate noise voltage rather than in terms of the more fundamental noise fluctuation of i_d as we do. It must be mentioned that the fluctuation quantities refer to a 1-Hz noise bandwidth. Although experimentally we took our noise data at various noise bandwidths, depending on the width of the spectrum to be measured and how near the carrier we measured, the data was normalized to a 1 Hz bandwidth.

We may relate the statistical RMS average of the gate noise fluctuation, denoted by the left side of Eq. (16) to the near-carrier FM noise, assuming an up-conversion process involving the source-gate capacitance. The "tie-in" is the sensitivity factor Eq. (10),

$$S(f_m) = \frac{\Delta f_o}{\Delta V_{sg}(f_m)} \qquad (17)$$

where $S(f_m)$ denotes the shift in carrier frequency f_o per unit voltage increment between the source-gate terminals at the modulation frequency f_m. Here again, we must, to be general, allow for a possible frequency dependence of S. However,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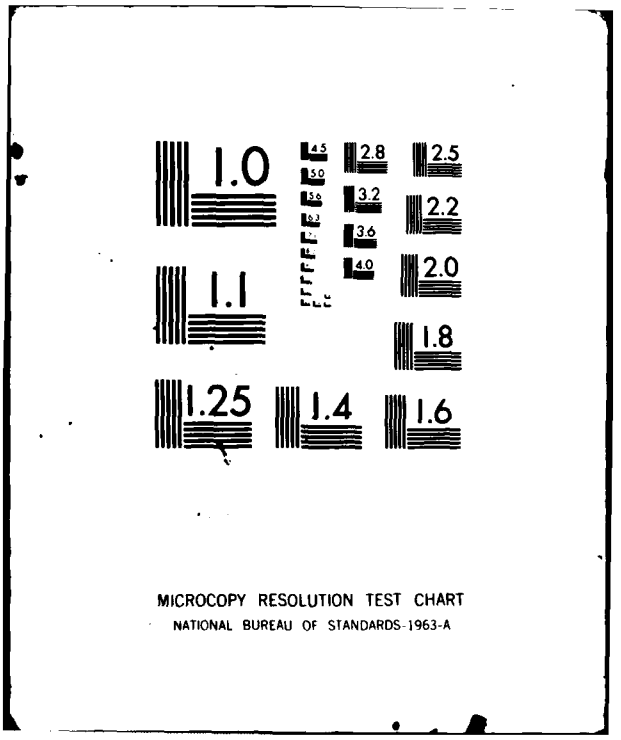
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we did not observe any such dependence up to 40 kHz.

From Eq. (17) we have

$$\Delta f_o = S(f_m)\Delta V_{sg}(f_m) \qquad (18)$$

Treating ΔV_{sg} as random, Eq. (16), and Δf_o as the corresponding noise component in the FM spectrum, we may write, using Eq. (9) and Eq. (16)

$$\langle \Delta^2 f_o(f_m) \rangle = \left| \frac{S(f_m)}{g_m(f_m)} \right|^2 \langle \Delta^2 i_d(f_m) \rangle \qquad (19)$$

which is the desired relation between drain current fluctuation and the near-carrier FM noise.

All four quantities $\langle \Delta^2 f_o(f_m) \rangle$, $S(f_m)$, $g_m(f_m)$, and $\langle \Delta^2 i_d(f_m) \rangle$ can be, and were, measured. Our objective was to test whether the "right-hand side" could account for the entire part of the measured near-carrier FM noise.

5.3 Measurement Conditions

We measured an unbuffered device, wafer series 82695LB-A (see Fig. 10), and a buffered device, wafer series 7A87-AB. Both of these series, which were discussed in previous sections, are fabricated on Sumitomo substrates.

Both AM and FM near-carrier noise were measured, as well as baseband noise, although we will discuss only FM noise in detail. Furthermore, in some cases, the drain of the FET was biased with a low-impedance source (voltage source) and in other cases with a high-impedance source (current source) to study the suppression of current fluctuations by the bias source itself.[18]

The baseband noise and transconductance were made with the device oscillating, since this is the more realistic condition.

5.3.1 Unbuffered device

The transconductance g_m and sensitivity factor S were measured at dc and spot-checked at higher frequencies, for example 40 kHz, with no discernible difference in value. We obtained the values:

$$g_m = 10 \text{ mmhos}$$
$$|S| = 122 \text{ MHz/V}$$

These were obtained at the operating voltages of the oscillator, namely,

$$V_{sg} = -1.4 \text{ V}$$
$$V_{sd} = 5 \text{ V}$$
$$I_d = 70 \text{ mA}$$
$$P_{osc} = 41 \text{ mW}$$

The sensitivity factor obtained from the experimental data is shown in Fig. 43.

The drain current (baseband) spectrum, $\langle \Delta^2 i_d \rangle$, and the near-carrier FM noise $\langle \Delta^2 f \rangle$ are plotted in Fig. 44. Straight-line "fits" to the data (dashed lines) indicate a nearly ideal 1/f dependence. The various sets of data represent measurements over different frequency scan widths and "window" widths of the noise analyzer. However, regardless of the filter bandwidth or window, all of the data was normalized to a 1 Hz bandwidth. Incidentally, f_m denotes either the baseband frequency or the frequency offset from the carrier, as the case may be.

The nearly identical frequency dependence of the two spectra suggests a common noise source — in this case depletion layer modulation by traps. To test this hypothesis, we must demonstrate that the two noise levels are consistent with this hypothesis. For this purpose we use Eq. (19).

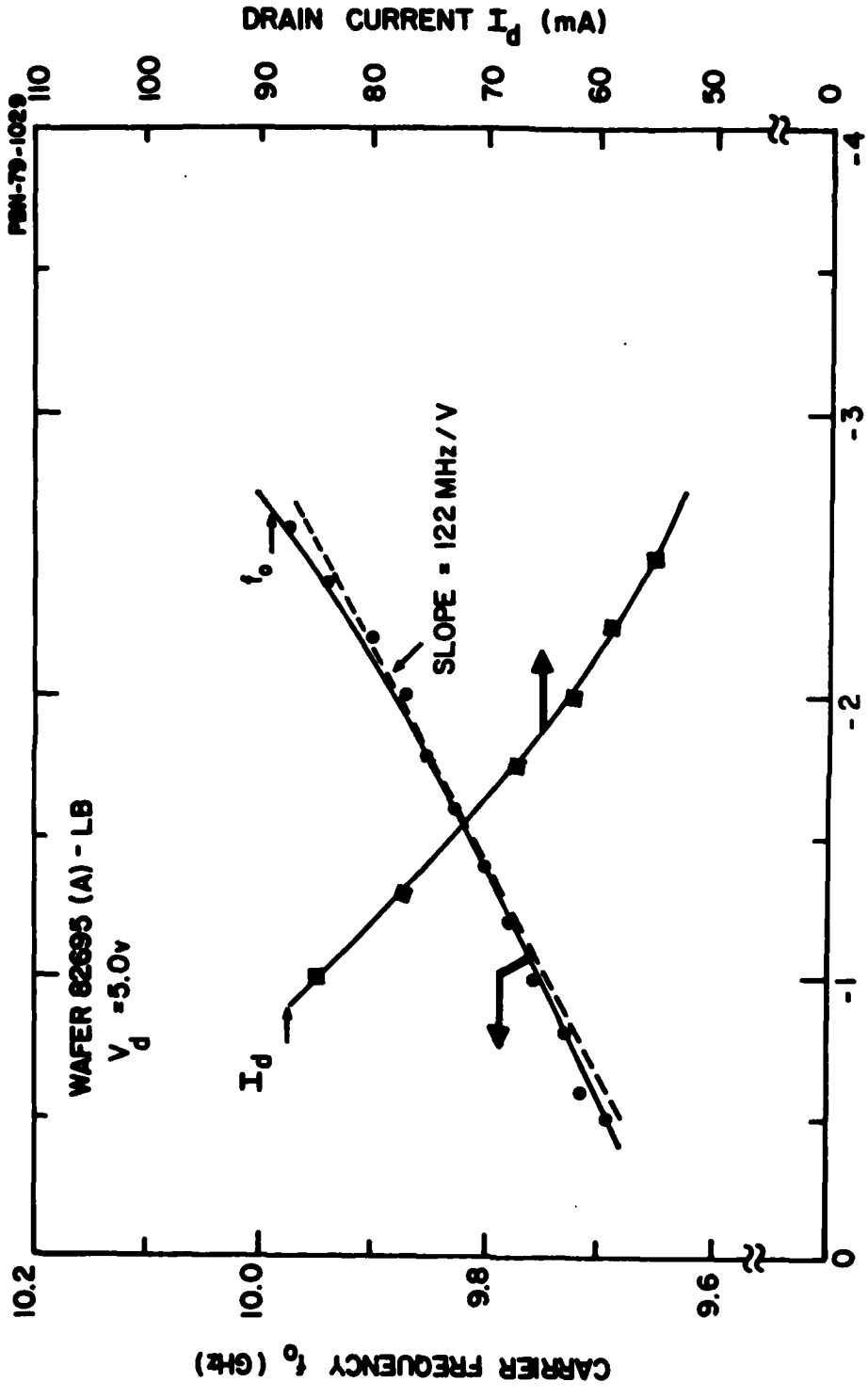


Figure 43. Oscillation Frequency and Drain Current as a Function of Gate Bias.

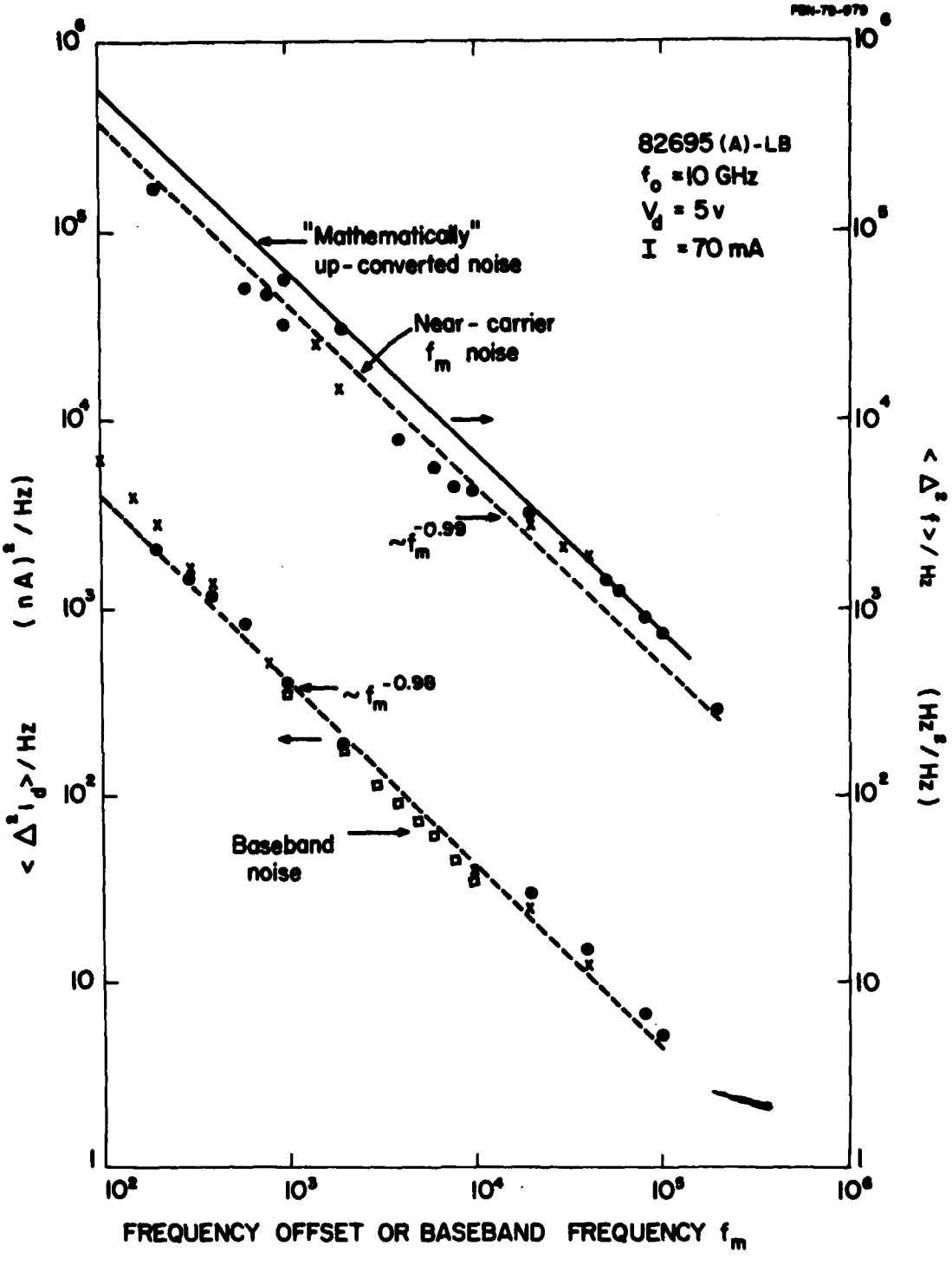


Figure 44. Baseband and FM Noise as a Function of Frequency. (Unbuffered device).

If we represent the straight-line approximation of the baseband noise by the analytic expression

$$<\Delta^2 i_d(f_m)>/Hz = \frac{K_i}{f_m^{0.98}} \qquad (20)$$

where $K_i = 3.9 \times 10^{-13}$ A^2/Hz, and the values for $S(f_m)$ and $g_m(f_m)$ in Eq. (18), we obtain

$$<\Delta^2 f_o(f_m)> = \left(\frac{1.22\times10^8}{10^{-2}}\right)^2 \times \frac{K_i}{f_m^{0.98}} = \frac{5.8\times10^7}{f_m^{0.98}} \qquad (21)$$

This expression is plotted as the solid straight line in Fig. 44. Note that it differs from the straight line approximation to the FM data (dashed) by only 1.5 dB. This close agreement leads us to believe that the baseband drain current fluctuation indeed manifests itself as FM noise via a modulation of the source-gate capacitance, as proposed.

We must rule out any possibility that the 1/f noise is external. For this purpose, we measured the mean square voltage appearing across the gate and source terminals with the FET "off" and "on" (oscillating). With the FET "off," $V_d = 0$, the noise was predominantly "white" from 15 kHz on up. Below 15 kHz, it rose sharply. With the device oscillating, the noise became predominantly 1/f and was some 20 dB higher. The noise was measured up to 200 kHz, using a 3 kHz bandwidth. The noise was measured with a HP baseband noise analyzer having a 75-ohm input impedance.

When the data is normalized to a 1 Hz bandwidth, the results are as shown in Fig. 45 (lower data). The drain current noise referred back to the gate is shown by the upper data. This was obtained from the curve of drain current noise, Fig. 44, with the help of Eq. (16). We see that the residual noise is at least two orders of magnitude below the internal 1/f noise of the FET and poses no problem. Therefore, it is safe to say that we are measuring FM modulation produced by internal 1/f noise.

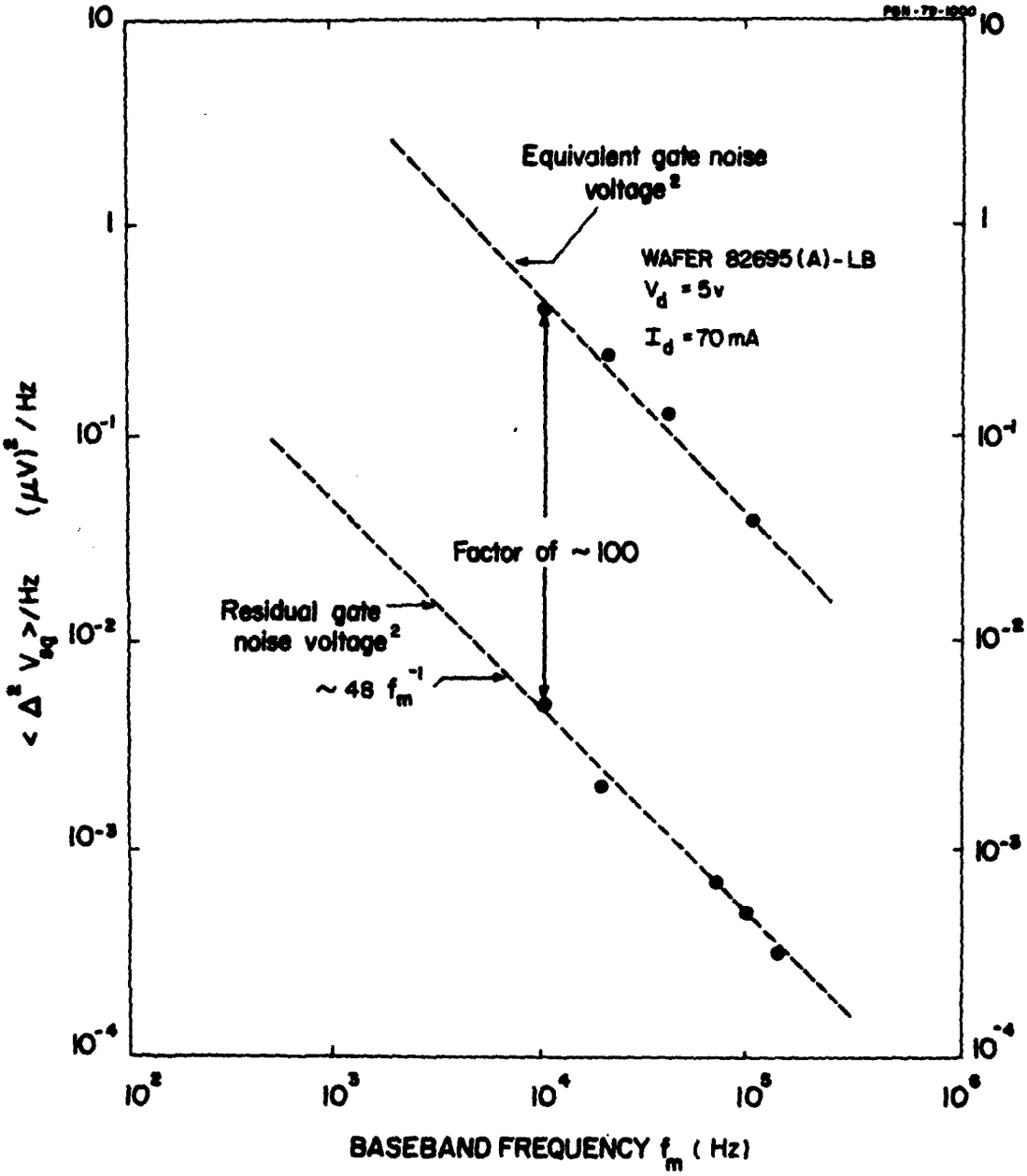


Figure 45. Equivalent Gate Noise Voltage and Residual Gate Noise Voltage as a Function of Frequency.

The AM noise, expressed in terms of the N/C ratio for a 1 Hz bandwidth is plotted in Fig. 46. The fact that the AM noise is nearly 100 dB lower than the FM noise further supports our belief that the noise up-conversion process involves depletion layer modulation, which results in a modulation of the source-gate capacitance. This modulation process would not be expected to result in AM noise.

The relatively high FM noise level is, to some extent, a consequence of the rather low loaded Q-factor. The Q-factor was measured by the technique based on the locking formula*

$$Q_L = \frac{2f_o}{\Delta f_L}\sqrt{\frac{1}{P_o/P_i - 1}} \qquad (22)$$

where Δf_L is the total locking bandwidth, P_o the carrier power, and P_i the synchronizing power. From experiment, $P_i/P_o = -27$ dB, $f_o = 9.8$ GHz, and $\Delta f_L = 30$ MHz. Thus

$$Q_L = \frac{2\times 9.8\times 10^9}{3\times 10^7}\sqrt{\frac{1}{501-1}} = 29.2$$

In Sec. 5.4 we shall examine in more detail the dependence of near-carrier noise on circuit Q.

5.3.2 Buffered device

The noise was measured under two drain biasing conditions: (1) the constant drain voltage or "voltage stabilized" condition and (2) the constant drain current or "current stabilized" condition. Significant similarities and departures from the previous results were noted.

5.3.2.1 Constant voltage case

We consider, first, the constant-voltage case. Figure 47(a) shows a plot of the measured baseband and FM noise as a function of baseband frequency

*The phase-locking technique for measuring the loaded Q-factor is described in Sec. 5.4.

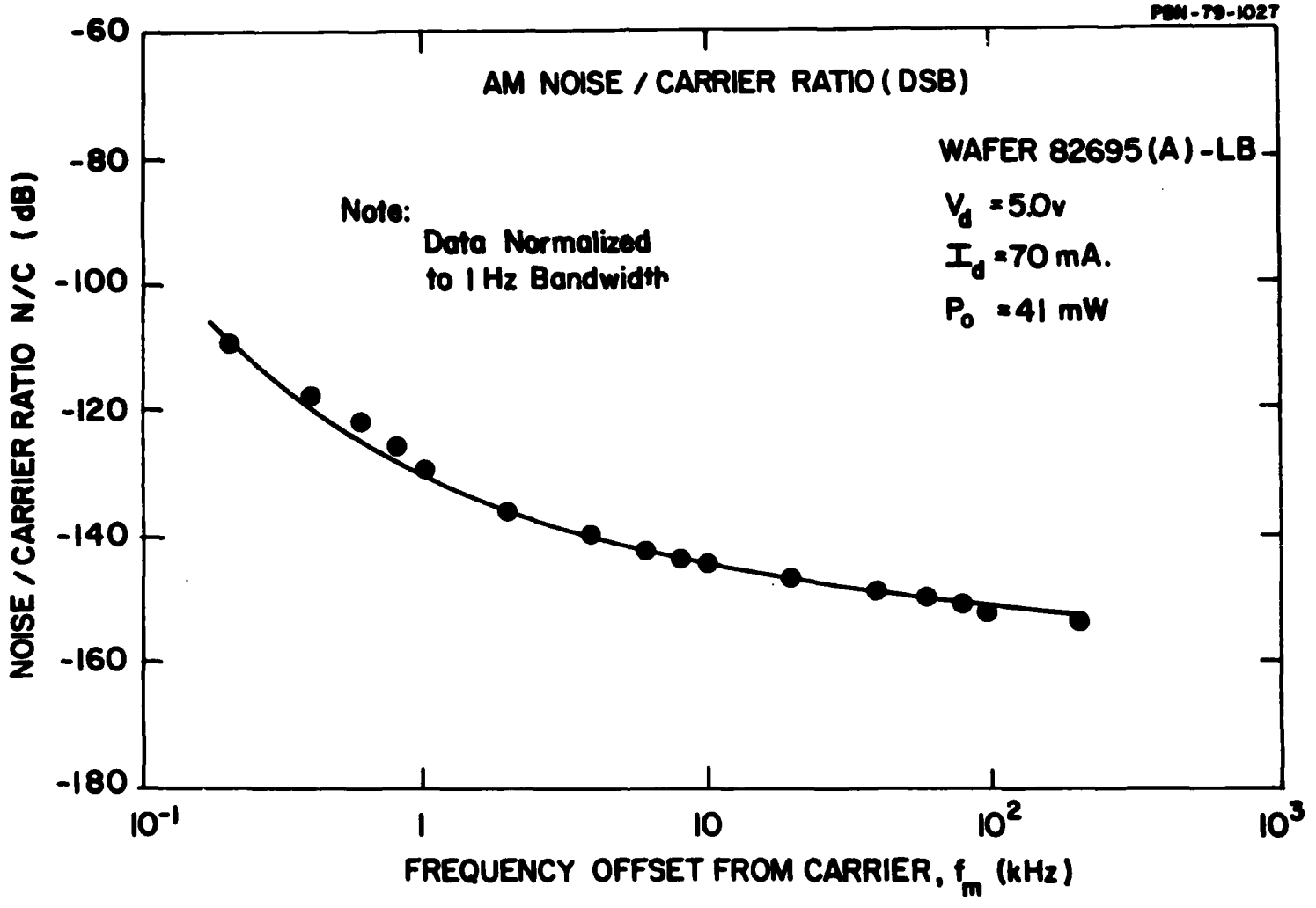
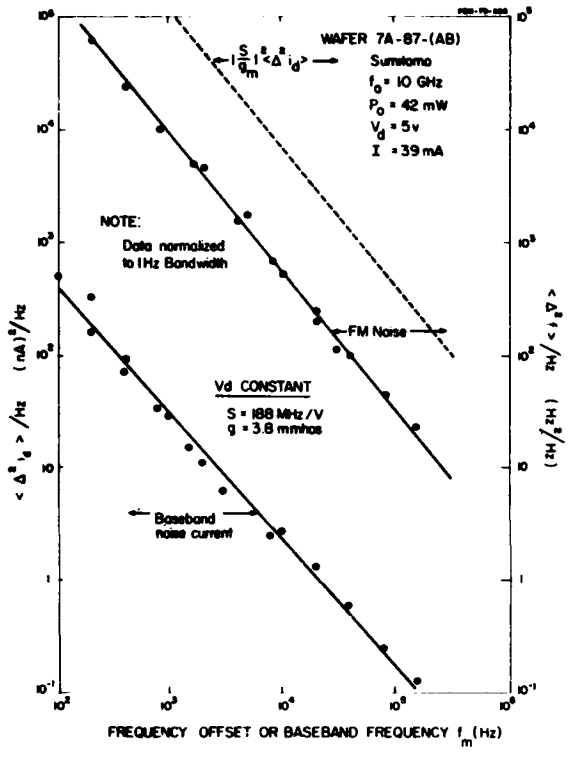
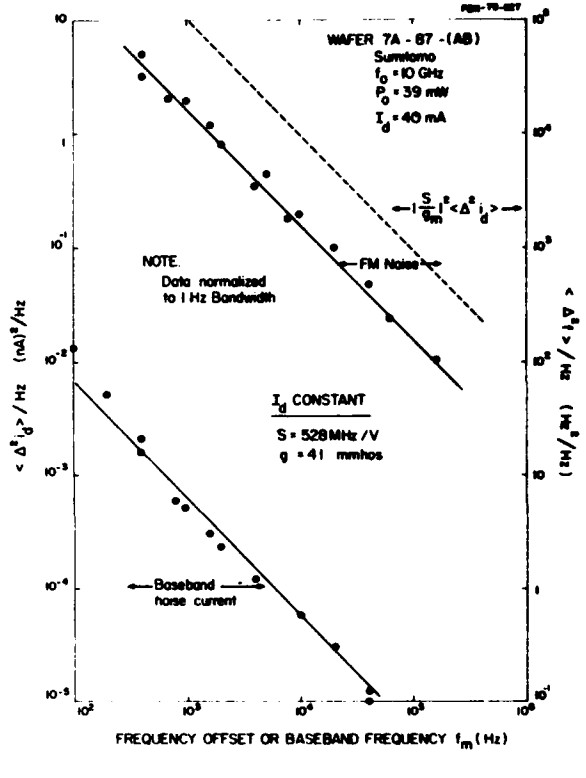


Figure 46. AM Noise-To-Carrier Ratio as a Function of Offset Frequency.



(a) Constant Drain Voltage



(b) Constant Drain Current

Figure 47. Baseband and FM noise as a function of frequency for a buffered device.

or frequency offset from the carrier, as the case may be. We note, as for the non-buffered case, that the noise is nearly 1/f in nature up to and beyond 100 kHz. Observe, however, that both the baseband and FM noise are over 10 dB lower than for the nonbuffered case.

As before, we calculate the FM noise to be expected if we assume all baseband noise manifests itself as a depletion layer modulation by the mechanism described in Eq. (19) where $S = \Delta f_o / \Delta V_g$ is the frequency-sensitivity factor denoting the carrier frequency shift with respect to gate bias and g_m is the transconductance measured under oscillating conditions. The measured sensitivity factor and g_m are

$$|S| = 188 \text{ MHz/V}$$

$$g_m = 3.8 \text{ mmhos}$$

Note that S is somewhat higher in magnitude here than in the previous case (122 MHz/V) and g_m is somewhat lower. The lower g_m can be explained by the gate bias condition, which is near pinch-off. The bias dependence of g_m is illustrated in Fig. 48. The mathematically upconverted FM noise is also shown in Fig. 47(a)[dotted line]. Note that this "predicted" noise is over 10 dB higher than the measured FM noise, indicating that not all baseband noise is upconverted by the depletion layer modulation process. This is a significant result, in light of the fact that the overall noise levels, both baseband and FM, are themselves some 10 dB lower than for the nonbuffered case (Fig. 44), which showed good agreement between the predicted and measured FM noise.

5.3.2.2 Constant-current case

Turning to the constant-current bias case [see Fig. 47(b)], we find as expected that the baseband noise has been suppressed severely, by approximately 45 dB. However, the measured FM noise is not significantly different from the constant voltage case, being some 1.5 dB higher at f_m = 10 kHz! (The difference varies with f_m, since both bias cases do not give the same frequency dependence of the noise.) The sensitivity factor is over twice that for

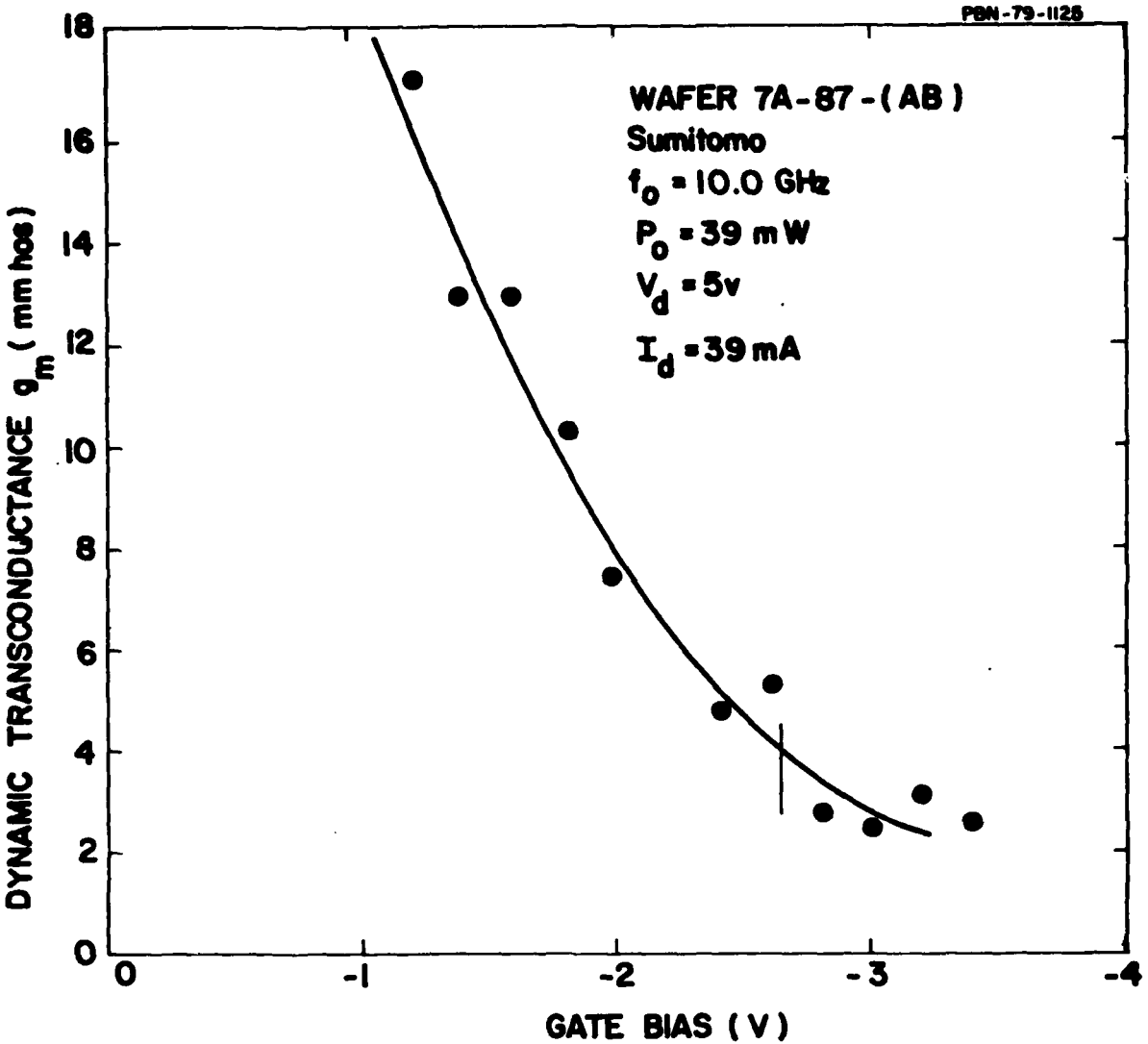


Figure 48. Dynamic transconductance as a function of gate-source bias (constant drain voltage).

the constant drain voltage case, and the g_m is lower. The measured values are

$$|S| = 528 \text{ MHz/V}$$

$$g_m = 41 \text{ micromhos}$$

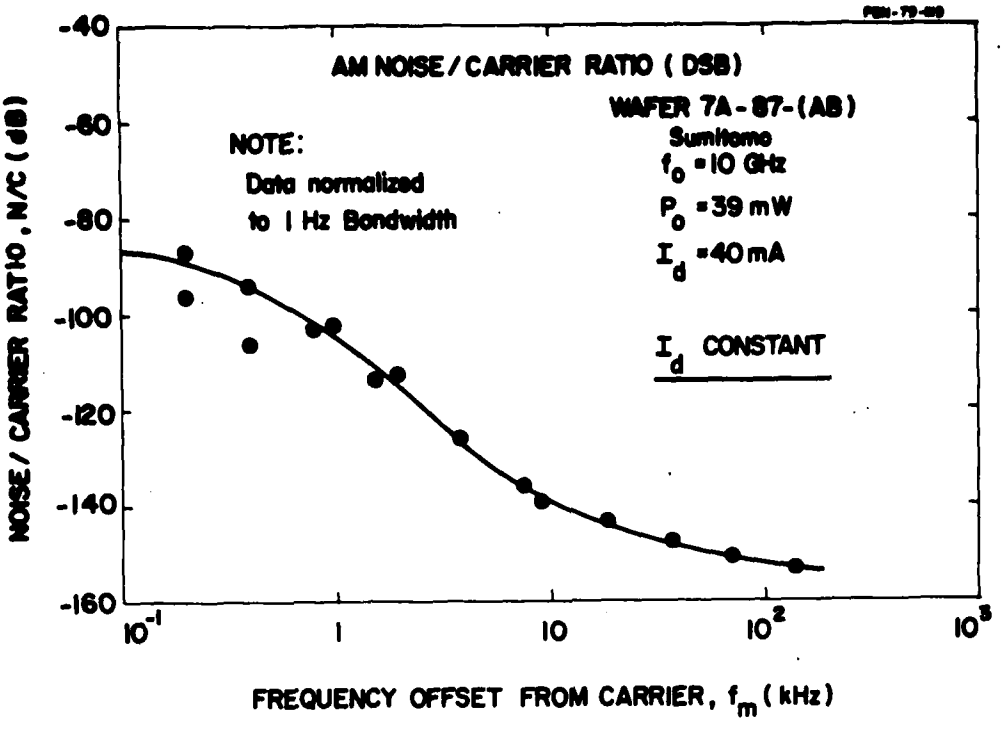
where for S we have corrected for the frequency shift with drain bias. The predicted FM noise is shown by the dotted line in Fig. 47(b). The predicted noise like the measured FM noise is nearly identical to that for the constant voltage case.

The measured AM noise for the constant current and constant voltage cases is illustrated in Figs. 49(a) and 49(b). Note that there is no significant difference in the noise levels.

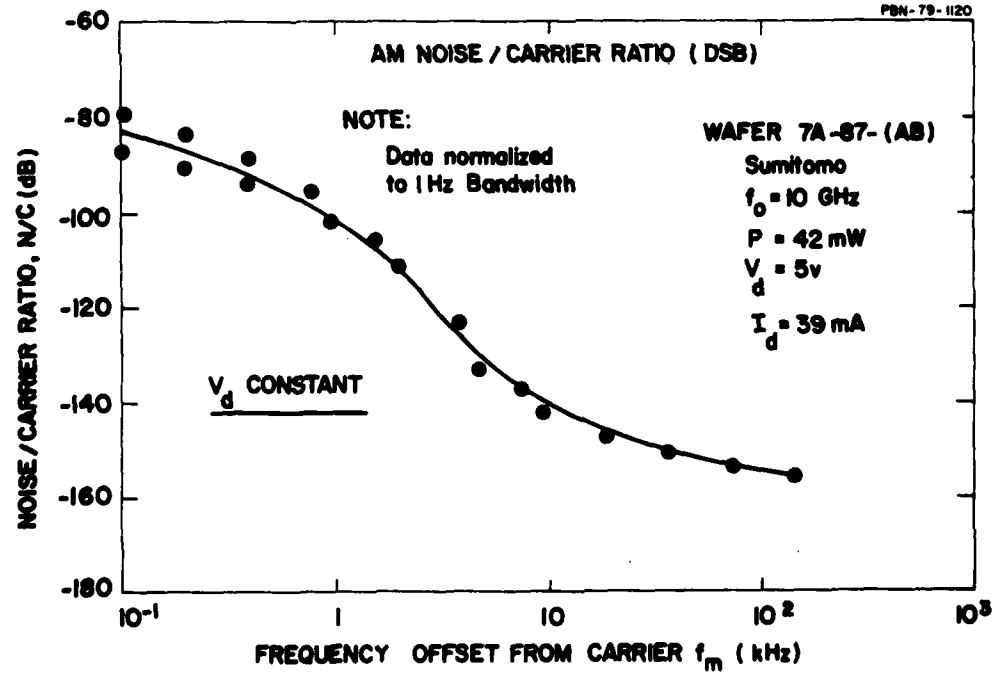
5.3.3 Conclusions

What does this all mean? First, in comparison to a device without a buffer layer, the measured baseband and near carrier 1/f noise are lower, by about 10 dB, for a buffered device. Second, for an unbuffered device, the measured near carrier 1/f noise can be accounted for completely by the depletion layer modulation model. For a buffered device, however, this model predicts too high a near-carrier noise. Finally, biasing the drain with a current source rather than a voltage source suppresses the baseband noise severely (over 40 dB) but has little or no effect on the near-carrier noise.

In the following sections we shall report on experiments relating the effect of circuit Q-factor and phase-locking on near-carrier noise reduction. These experiments will also shed more light on the experimental results just described.



(a) Constant Drain Current



(b) Constant Drain Voltage

Figure 49. AM noise-to-carrier ratio as a function of offset frequency for a buffered device.

5.4 Effect of Circuit Q on Near-Carrier Noise

5.4.1 Introduction

The experiments that were carried out were designed to study the effect of circuit Q on the FM noise for the case of constant drain voltage and constant drain current bias modes. Our objective was to determine whether the classical oscillator models apply to the FET, especially in the 1/f region. The loaded Q was varied by attaching a waveguide cavity or a wavemeter to the oscillator circuit and adjusting the coupling of the load by a probe inserted into the cavity. By this means it was possible to increase the loaded Q to 2000, which is about two orders of magnitude above the Q realized by the integrated circuit alone (without the waveguide cavity attached).

The loaded Q was determined by pulling the oscillator frequency with a synchronizing source and determining the range over which synchronization is maintained as a function of locking gain, G_L. The test arrangement is shown in Fig. 50. The synchronizing signal was injected into the drain terminal of the FET oscillator via a circulator (recall that we are using a grounded-gate oscillator). The injected locking signal was varied from 10 dB below the oscillator carrier power to as low as 50 dB below the carrier. The synchronizing signal was an ultra-low-noise solid-state (Gunn) oscillator.

The locking gain is defined in the usual manner as the oscillator power P_o divided by the incident power P_i from the synchronizing source. Thus

$$G_L = \frac{P_o}{P_i} \tag{23}$$

the locking gain was varied over a 40-50 dB range by varying the incident synchronizing power.

5.4.2 Determination of the loaded Q-factor of the oscillator

It is necessary to establish a means of determining the Q-factor of the oscillator circuit under oscillating conditions before one can test the validity

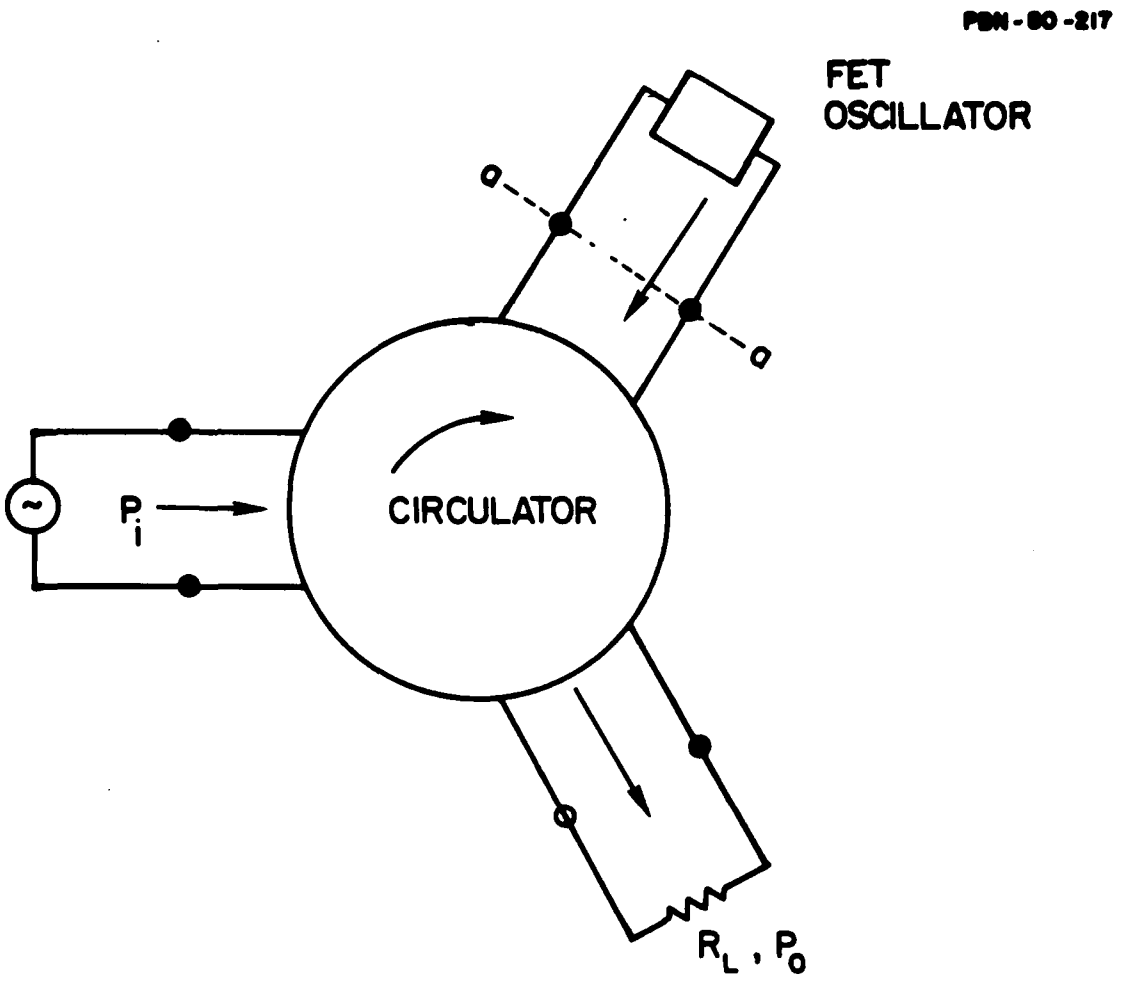


Figure 50. Test arrangement for measuring Q-factors and FM noise reduction under phase-locked conditions.

of the classical oscillator relation between the loaded Q, Q_L and the FM noise level for FET oscillators.

This relationship can be determined by the phase-locking scheme illustrated in Fig. 50. The technique for determining Q_L is to vary the FET carrier frequency by "pulling" it from its free-running value f_o to either "side" of this value by adjusting the frequency of the synchronizing source until "lock" is "broken". The total pulling frequency interval we define as f_L, the locking range. The loaded Q is given by the relation

$$Q_L = \frac{2f_o}{f_L}\sqrt{\frac{1}{G_L^{-1}}} \qquad (24)$$

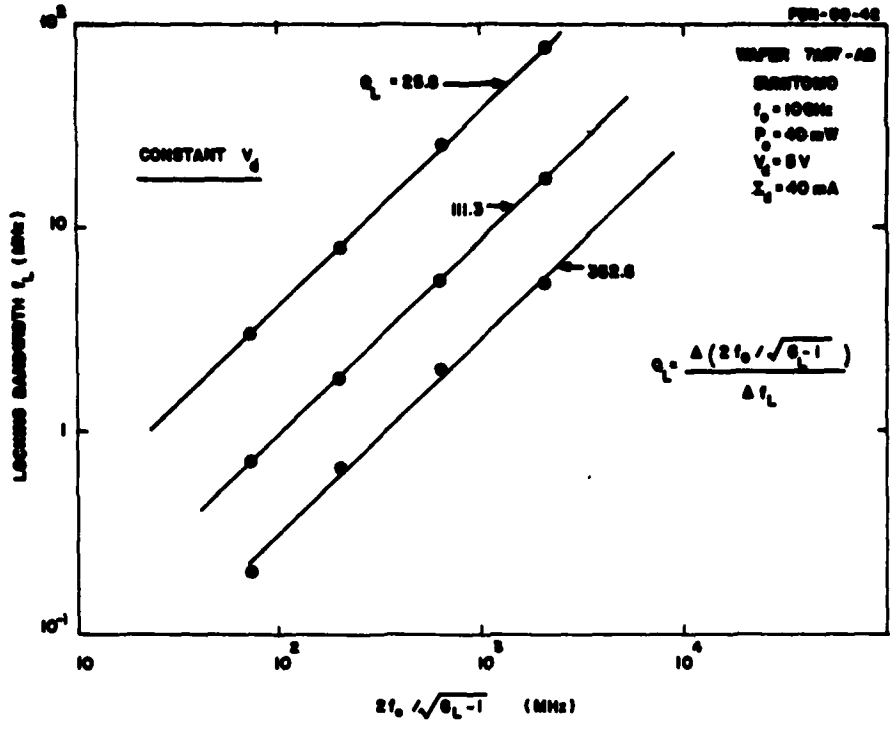
If one varies the locking gain in steps and measures the corresponding locking bandwidth, then a plot of f_L against the quantity $2f_o/\sqrt{G_L^{-1}}$ on a linear scale should yield a straight line whose slope is equal to $1/Q_L$. However, because of the large range of locking bandwidth involved, it is more convenient to plot this relation on log-log paper. In this case a straight line with a 45° slope is obtained. The loaded Q can be determined by the intersection of the line with the vertical axis. Such a plot is shown in Fig. 51(a) for several loaded Q factors. The loaded Q-factor was varied from the intrinsic MIC Q value, $Q_L \approx 25$, to values approaching that of the wavemeter $Q_L \simeq 2000$ by varying the coupling to the load by means of a slide screw tuner.

Alternatively, one may plot the quantity $2f_o/(f_L\sqrt{G_L^{-1}})$ against G_L on linear paper as shown in Fig. 51(b). The best horizontal line fit to the data, extrapolated to the vertical axis, yields the loaded Q. We used both methods.

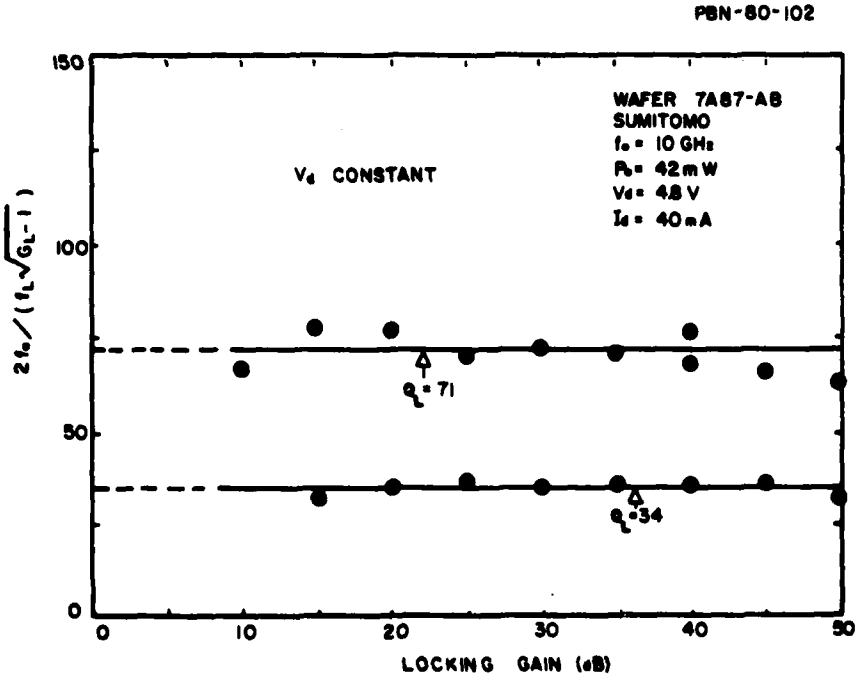
It is evident from Fig. 51 that because the expected straight-line relationship is obtained, the classic synchronizing relation (24) does indeed hold for the FET oscillator. Thus we may proceed to the noise relationships.

5.4.3 Near-carrier noise as a function of loaded Q-factor

The first relationship we wish to test is that relating the FM noise-to-carrier ratio to the loaded Q and the noise spectrum, Eq. (3b), which is repeated



(a)



(b)

Figure 51. Two methods for determining the loaded Q of an FET oscillator by the phase-locked technique.

here as Eq. 25 for convenience.

$$\left(\frac{N}{C}\right)_{FM} \approx \frac{N_{bm}}{P_c} \frac{1}{(f_m Q_L/f_o)^2} \qquad (f_m > 0) \qquad (25)$$

Here the noise spectral density N_{bm} represents the frequency dependence of the baseband (1/f) noise.

Figure 52(a) illustrates the FM noise-to-carrier ratio as a function of frequency offset from the carrier for the FET oscillator under constant drain voltage bias conditions. Note that the noise decreases by approximately 30 dB per decade of frequency change, that is, as $1/f_m^3$ indicative of "1/f" noise, as predicted by Eq. (25). It is obvious that a measurable 1/f component extends beyond 1 MHz from the carrier. Notice that the N/C ratio varies as $1/Q_L^2$ over the entire Q range, as predicted by this classic equation.

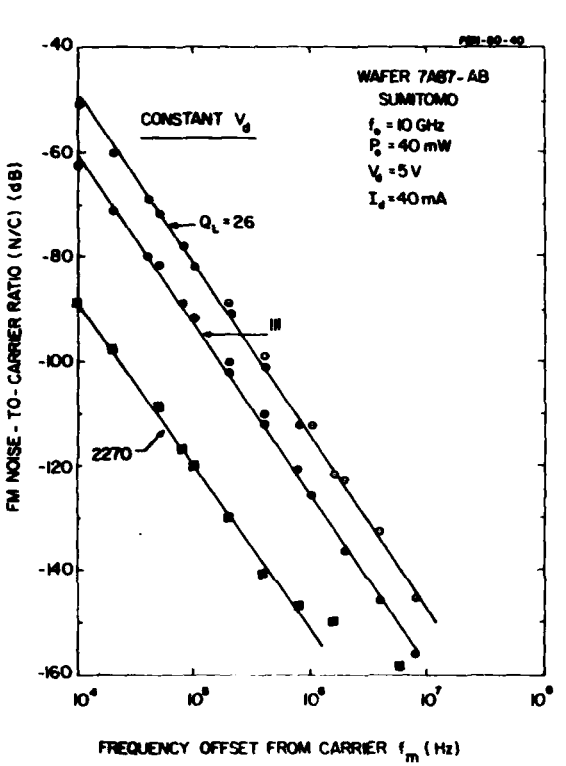
Figure 52(b) illustrates the mean square frequency deviation corresponding to the data in Fig. 52(a). Here, of course, $<\Delta^2 f>$ decreases at a rate of 10 dB per decade, corresponding to 1/f noise, that is, as predicted by theory (Eq. (6).

$$\Delta^2 f_{rms} = \left(\frac{f_o}{Q_L}\right)^2 \frac{N_{mb} B}{P_c} \quad , \qquad (26)$$

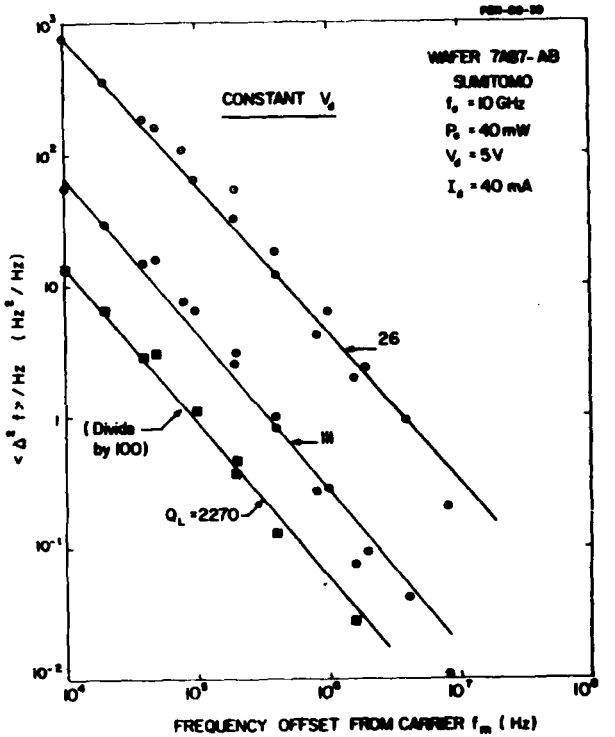
where N_{mb} is the 1/f noise spectrum responsible for the noise. Note that again the noise level varies as $1/Q_L^2$.

The baseband noise was also measured, but under oscillating conditions. In principle, the baseband noise level, according to classical oscillator theory, should not be affected by the loaded (rf) Q-factor. We tested this prediction both for the case where the FET drain was biased with a constant voltage and constant current source, respectively. The results are shown in Fig. 53.

A small (but inconclusive) variation of the baseband noise level for the constant voltage case can be seen. However, the dependence on Q_L for the

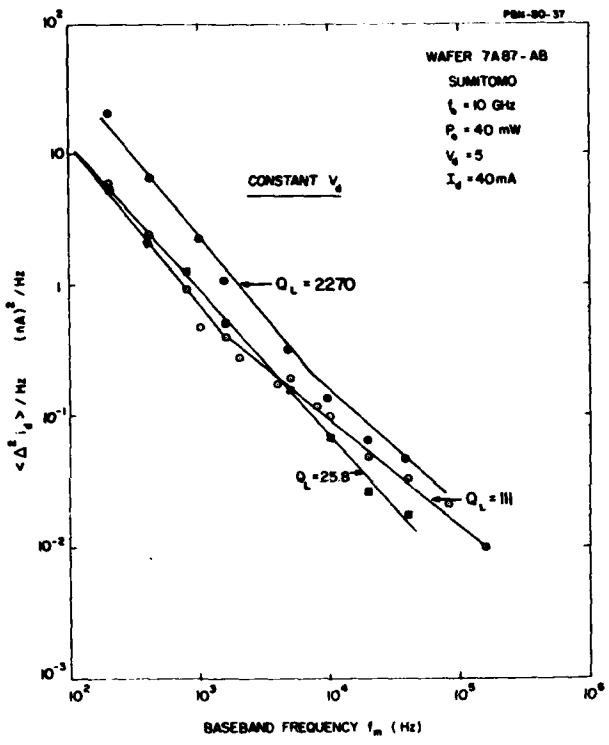


(a) N/C ratio

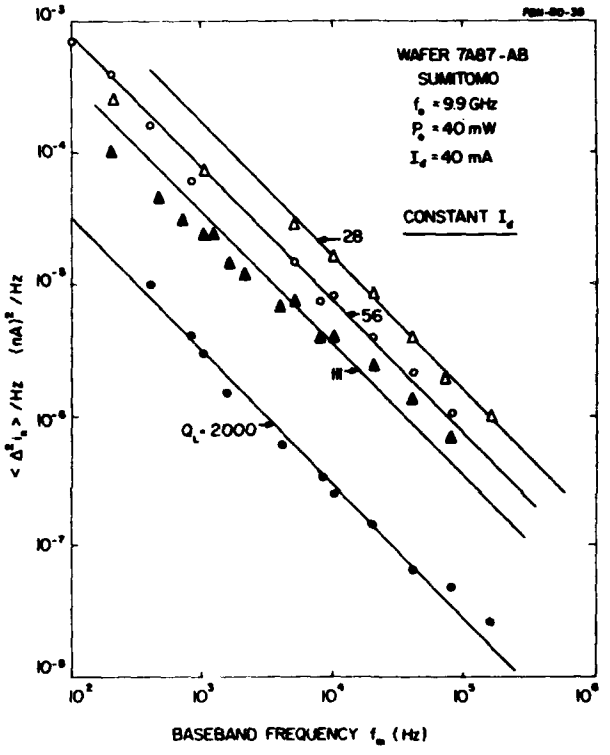


(b) Mean-square frequency deviation

Figure 52. FM noise properties of an FET oscillator as a function of frequency offset and loaded Q under constant drain bias conditions for a buffered device.



(a) Constant Drain Bias Voltage



(b) Constant Drain Bias Current

Figure 53. Baseband noise measured under oscillating conditions as a function of baseband frequency and the loaded Q of the oscillator circuit.

constant current case is very large. This was unexpected. Although there was some scatter in the data for this case, a definite 1/f dependence is maintained for all Q values. What is very interesting is the fact that the baseband noise seems to vary nearly inversely with the loaded Q-factor, Q_L, as indicated in Fig. 54.

Present oscillator theories do not predict any rf interaction with the baseband noise sources except in a modulation upward in frequency, that is, from baseband to rf — but not in the reverse direction. However, there is no reason that the interaction should not work both ways. For example, a (nonlinear) diode can function as a modulator as well as a demodulator. It just seems that, in the case of the oscillator, the down-conversion process has been neglected.

We propose the following tentative explanation of our baseband dependence on Q factor. First, near-carrier noise sidebands are demodulated back into baseband components. The higher the Q factor, the lower the sideband level, and hence the smaller the baseband component resulting from the demodulation process. This demodulated component, it appears, adds to the initial baseband noise.

Consider the voltage-controlled case first. Assuming that the demodulated component is small compared with the original baseband noise, little difference would be observed in the baseband noise as Q is varied.

Let us turn now to the current-controlled case. As we see from Fig. 53, the initial baseband noise level (i.e., for Q = 2000) is about four orders of magnitude lower than for the voltage controlled case, so low, in fact that the down-converted component is now comparable to the originating noise source. As the Q is lowered, more and more down-converted noise is added because of the increasing level of the sideband, hence the results of Fig. 53(b). The lower level of the baseband noise, therefore, can only be determined by removing the down-converted component altogether, that is, by "killing" the oscillation.

Our theory may also explain why the "mathematically" up-converted FM noise for the current-controlled case, as reported previously, is always substantially higher than that measured [Fig. 47(b)]. That is because the baseband noise level used in the computation was not the originating noise level, but was mostly the down-converted component, which was higher.

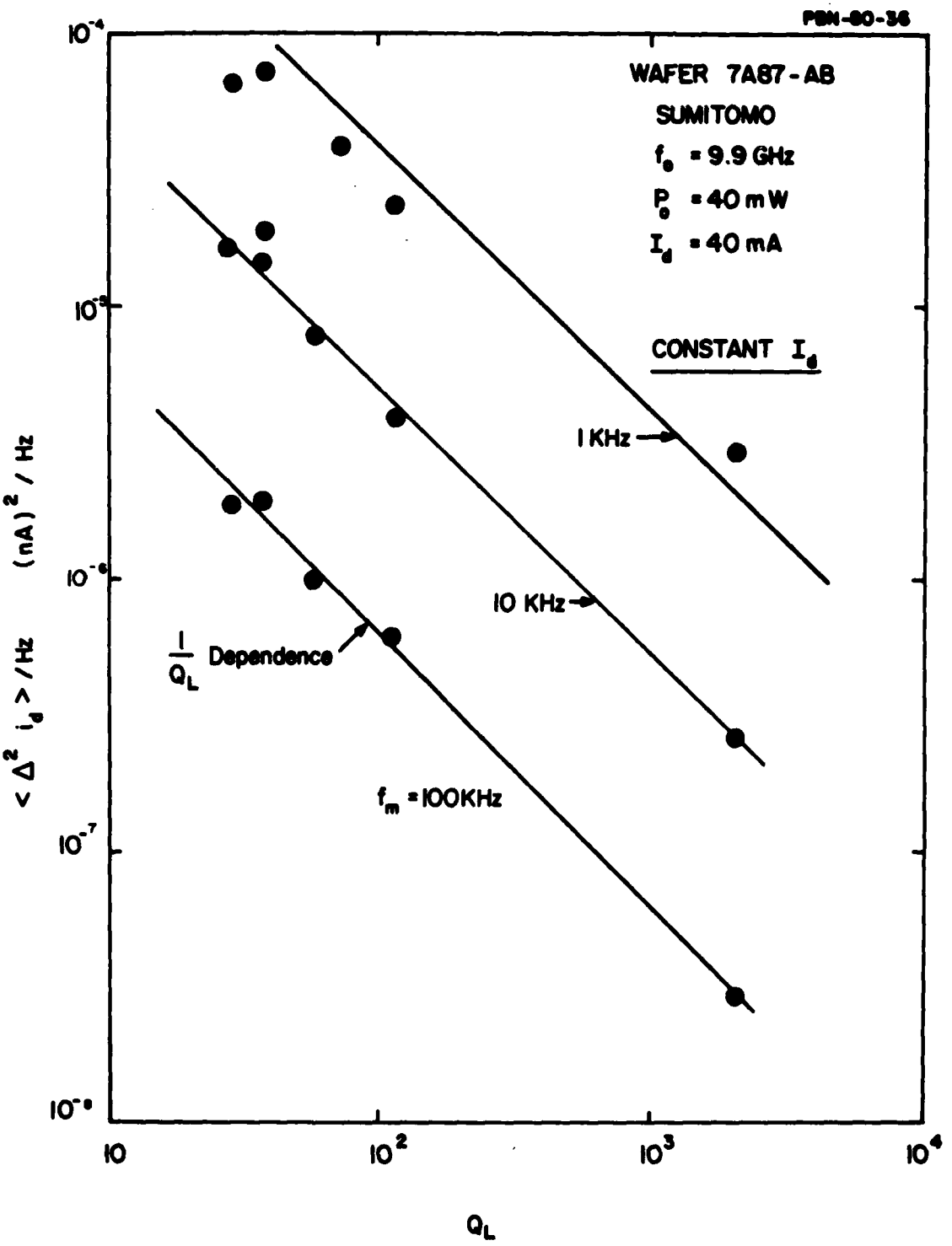


Figure 54. Baseband noise current as a function of loaded Q at three baseband frequencies (constant I_d case).

We are stressing this model because it may shed more insight into the up-conversion process and hence into the mechanism by which baseband trap noise contaminates the carrier.

5.4.4 Conclusions

We have found that the FM noise dependence on Q factor appears to follow the existing simple oscillator noise theory derived for one-port and two-port oscillators. What is new is the strong effect of cavity Q on baseband noise. Clearly, this effect, if it exists in other oscillators, has not been reported. It may, indeed, be connected to the physical mechanisms by which baseband noise gets upconverted to rf and, hence, may be peculiar to FETs. In any case, this phenomenon bears further study, especially from a theoretical standpoint.

Our experiments also show that, were it not for the low Q factors associated with integrated circuits, the FM noise level could be reduced to rather respectable levels when the Q factor is of the order of several thousand. To achieve such high Q's, one is required to use external cavity stabilization (waveguide or coaxial); alternatively some internal stabilization with, for instance, high-K dielectric cavities, or synchronization with an external low-noise oscillator as in the scheme illustrated in Fig. 50 would achieve the same purpose. We report on our experiments on FM noise reduction by phase synchronization below.

5.5 Noise Reduction by Phase Locking

We report here on FM noise measurements for the case of phase locking. The oscillator noise was measured with various levels of power injected into the FET oscillator from a stable, low-noise source, in this case, a commercial Gunn oscillator. The measurements are significant only for those noise frequencies off the carrier for which the FET oscillator noise exceeds the synchronizing source noise. As our data will show, this means frequency offsets in the range of $f_m \gtrsim 10^5$ Hz, depending on the external Q of the oscillator and the locking gain. The FM noise characteristic of the Gunn oscillator is shown in Fig. 55, in which

the double-sideband noise-to-carrier ratio is plotted as a function of frequency offset from the carrier.

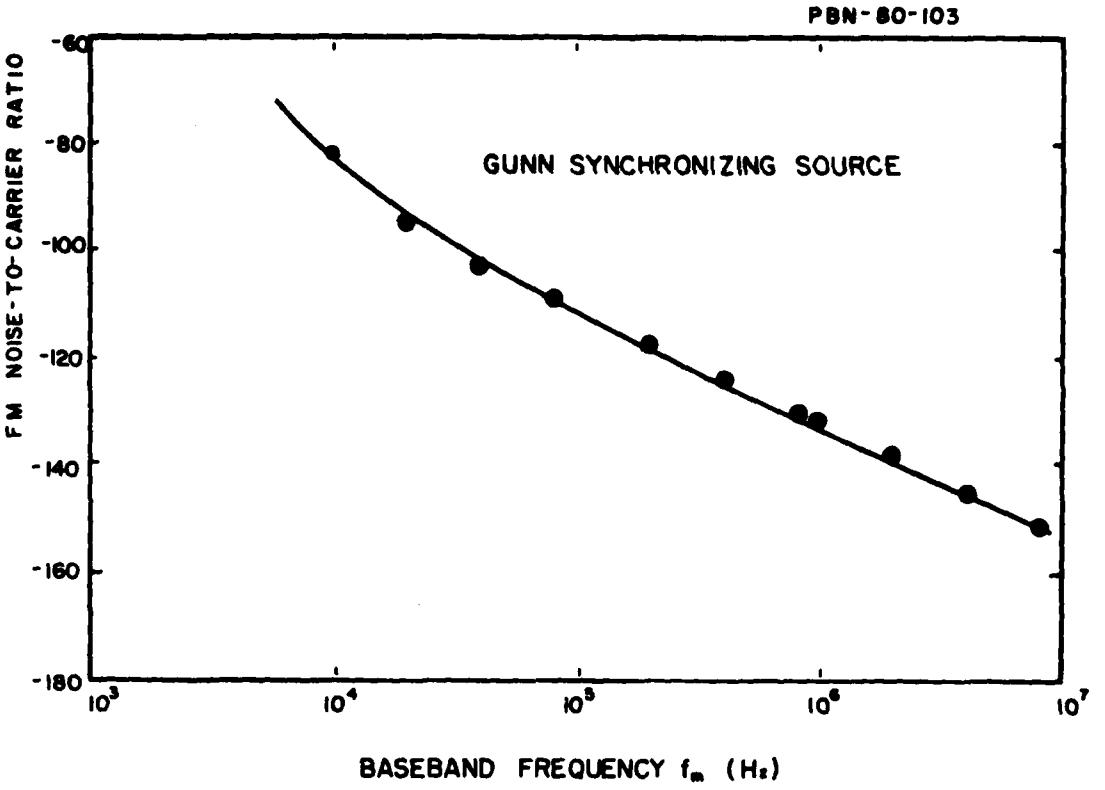


Figure 55. FM noise-to-carrier ratio of synchronizing Gunn source as a function of frequency offset from carrier.

Under phase-locked conditions the FM noise of an oscillator is reduced if the oscillator is synchronized to a "quieter" source. In theory, based on the classical oscillator noise model,[24] the noise-to-carrier ratio is given by the expression

$$\frac{N}{C}_{DSB} = \left(\frac{f_o}{Q_L}\right)^2 \frac{N_b B/P_o}{f_m^2 + (f_L/2)^2} \tag{27}$$

where N_b denotes the spectral density of the available noise power associated with the background noise source in the vicinity of the FET carrier frequency. In our experiments we have normalized the noise data to a noise bandwidth of 1 Hz.

Note in Eq. 27 that for frequency offsets $f_m << f_L/2$ the noise-to-carrier ratio becomes

$$\left(\frac{N}{C}\right)_{DSB} = \left(\frac{2f_o}{Q_L f_L}\right)^2 \frac{N_b B}{P_o} \qquad (f_m << f_L/2) \qquad (28)$$

This can be rewritten in a more convenient form for our purposes by substituting the expression (24) for Q_L. We obtain

$$\left(\frac{N}{C}\right)_{DSB} = (G_L - 1) \frac{N_b B}{P_o} \qquad (f_m << f_L/2) \qquad (29)$$

from which we obtain

$$N_b = \frac{P_o}{B} \frac{1}{(G_L - 1)} \left(\frac{N}{C}\right)_{DSB} \qquad (f_m << f_L/2) \qquad (30)$$

This last relation allows us to determine the spectral noise density of the background noise source in terms of experimental quantities.

The condition $f_m << f_L/2$ ensures that the data is taken well within the locking range. However, one cannot reduce f_m too low, because the noise level of the synchronizing source may dominate. Experimentally, we find a fairly narrow "window" to work in, constrained to $10^5 \leq f_m \leq 10^6$ Hz.

Note from Eq. (27) that outside the locking range, that is, for $f_m >> f_L/2$, the noise level returns to the free-running case. Observe that the locking range is $f_L/2$ rather than f_L, because after detection the upper and lower noise sideband spectra overlap.

We note that, in principle, N_b does not depend on the loaded Q, because it is a property of the FET alone. In general, N_b will consist of a sum of two terms, a white noise component N, independent of frequency offset, and a component N_{mb} representing upconverted baseband noise, which depends on f_m. That is

$$N_b = N + N_{mb}(f_m) \qquad (31)$$

The frequency dependence can easily be spotted by an inspection of the noise-to-carrier ratio plot in the locking region. If there is a nonzero slope to N/C, a frequency dependence exists. If the frequency dependence represents upconverted 1/f noise, then this dependence is mirrored in the N/C plot. Such is the case for our experimental data.

Figures 56(a) and 56(b) are graphs of the noise-to-carrier ratio for two loaded Q values, $Q_L = 34$ and $Q_L = 71$, for the case of constant drain bias. Figure 56(c) is a plot for the constant drain current case for $Q_L = 31$. Note the distinct 1/f slope. The upturn at low values of f_m indicate the predominance of synchronizing source noise.

In principle, the curves in the locking region should be spaced by 10-dB intervals, but they are not. Instead they average to a spacing nearer 8 dB. The reason for this is not known.

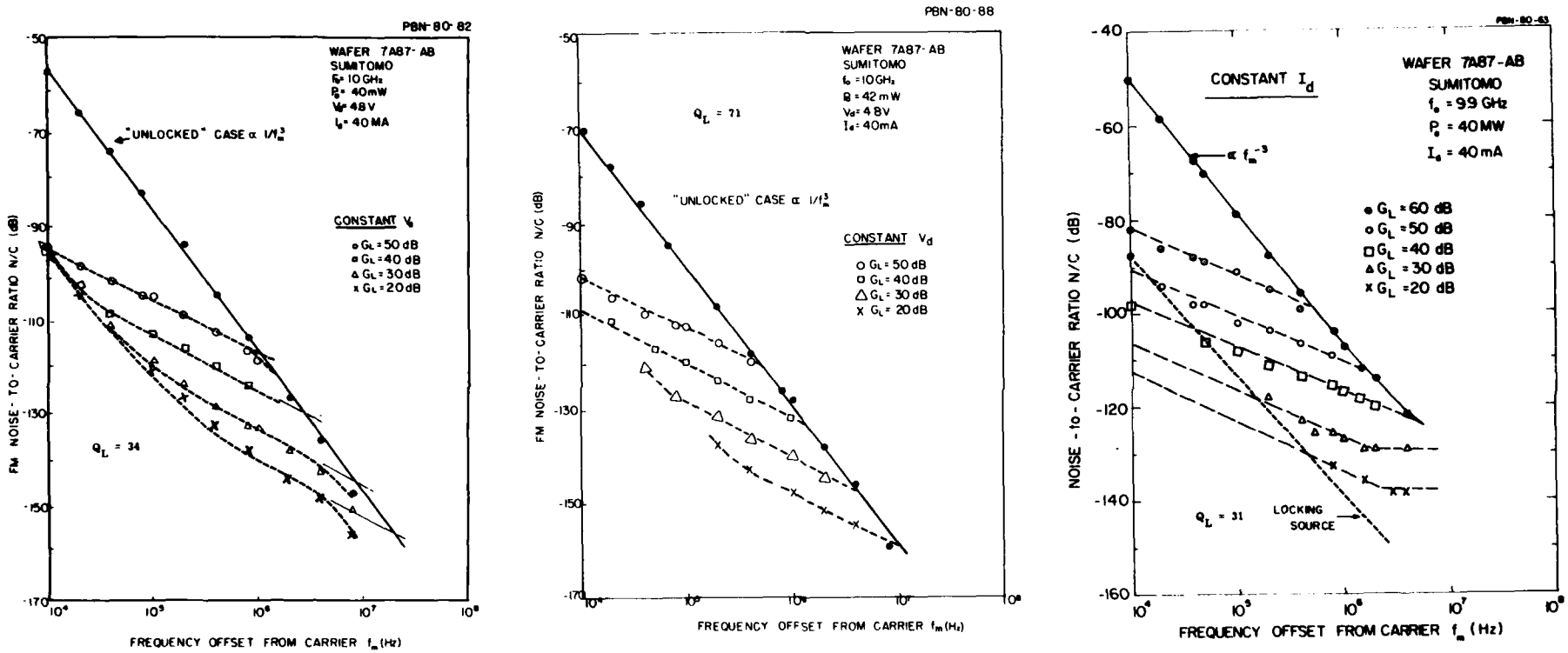
The fact that N/C varies as $1/f_m$ in the locking range suggests that, below about $f_m < 10$ MHz, the white noise component is negligible. We shall assume this for the time being and show later that it is valid. Thus we may write

$$N_m = \frac{f_m}{B} \frac{P_o}{G_L - 1} \left(\frac{N}{C}\right)_{DSB} \qquad (f_m < f_L/2) \qquad (32)$$

where we have assumed for the modulation component of the noise the form

$$N_{mb}\ (f_m) = \frac{N_m}{f_m} \qquad (33)$$

By reading N/C-values from the graphs of Fig. 56, and by plotting the quantity on the right side of Eq. 32, labelling it N'_b, one should obtain a value for N_m ($\approx N'_b$) which, in principle, is a constant. Such a plot is shown in Fig. 57. Note that the graphs are not horizontal but rather show a dependence on G_L. In addition, the values vary somewhat with Q_L, a phenomenon which the simple, classical theory does not predict. It is possible that the "first order" theory must be modified. The curves in Fig. 57 were determined for f_m values in the range $(2\text{-}5) \times 10^5$ Hz - well away from the synchronization source noise.



(a) Constant V_d (Q_L = 34)

(b) Constant V_d (Q_L = 71)

(c) Constant I_d (Q_L = 31)

Figure 56. FM noise as a function of frequency offset from the carrier with locking gain as a parameter.

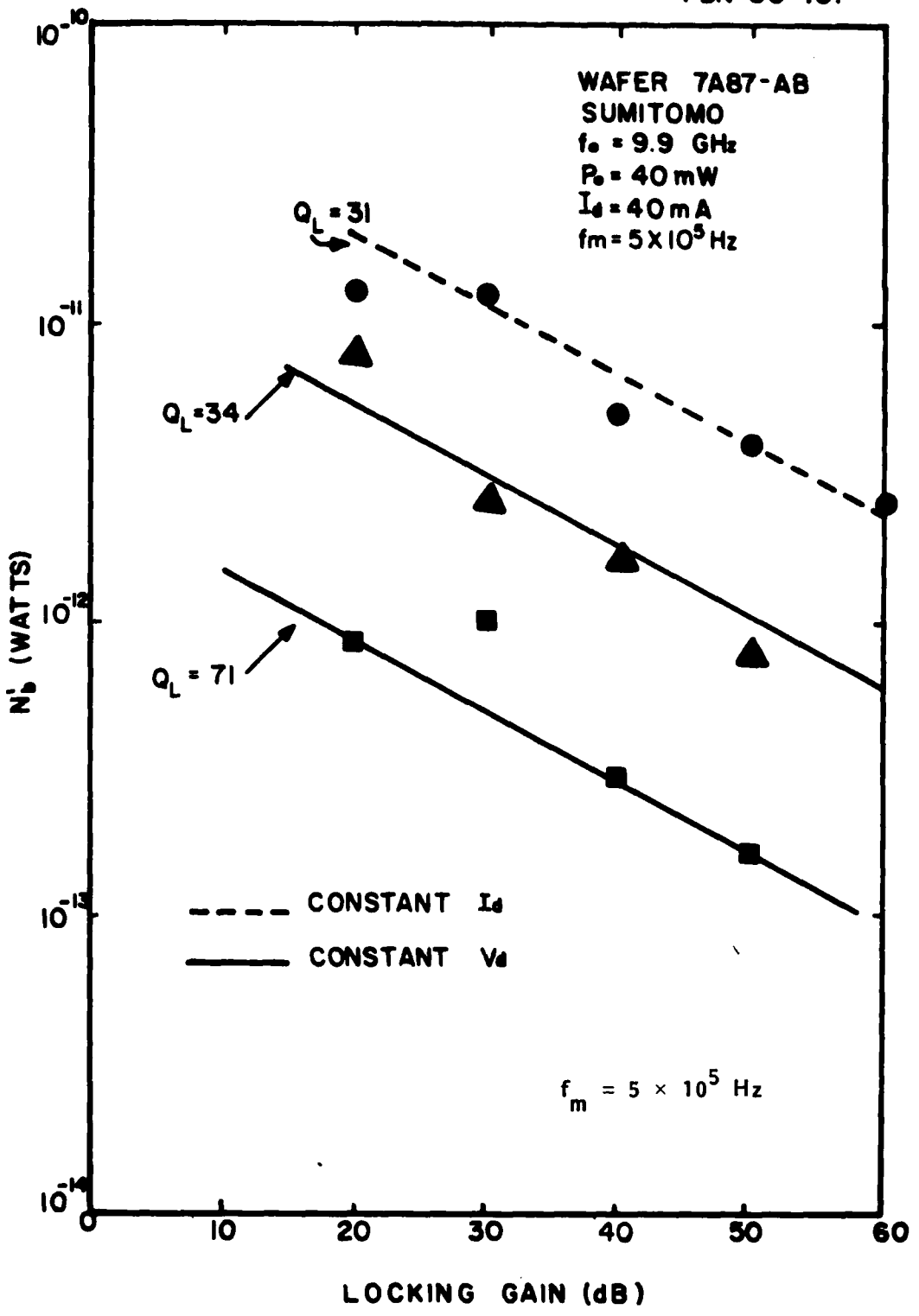


Figure 57. Graphical data used to determine the 1/f background noise level coefficient.

What is important in all of this is that we have obtained, finally, a quantitative estimate of the background spectral density level of the upconverted 1/f noise in FET oscillators. We believe this is a "first."

It is of interest to test our assumption that the white noise background can be neglected in the locking region. For this purpose, we evaluate N_{mb} and compare it with an estimated value of N. Let $f_m \approx 5 \times 10^5$ Hz. Then from Fig. 57 with $10^{-13} < N_b' \lesssim 10^{-11}$, we obtain

$$2 \times 10^{-19} < N_{mb} \lesssim 2 \times 10^{-17} \text{ watts/Hz (or joules)}$$

where we have let $N_{mb} = N_b'/f_m$.

Letting $N \approx MkT$, where M is an estimated noise measure of the FET used as an amplifier ($M \approx F$, the noise figure), assuming $F \lesssim 6$ dB, and using $k = 1.38 \times 10^{-23}$ joules, and T = 300°K, we find

$$N \approx 1.6 \times 10^{-20} \text{ joules.}$$

This is still over one order of magnitude lower than the 1/f noise and, hence, justifies our assumption. The predominance of 1/f noise emphasizes the importance of reducing this noise in FET oscillators.

5.5.1 Conclusions

Phase-locking experiments have shown that the classical oscillator noise theory is obeyed by FET oscillators. Our results indicate, however, that some refinements in the theory are in order.

We have succeeded in estimating the spectral density of the 1/f background source. Thus, a quantitative basis for modelling the upconversion coupling mechanism is established.

The 1/f noise level, we have shown, is at least an order of magnitude higher than the white noise level for frequencies within a MHz from the carrier,

even if the noise figure is as high as 6 dB. This confirms the importance of reducing the 1/f noise mechanism of FET oscillators to capitalize on the low level of thermal noise inherent in MESFETs.

5.6 Tentative Theoretical Model of Noise Sources in an FET Depletion Region

Our experimental measurements suggest that FM noise can be correlated with fluctuations in the capacitance of the depletion region. In order to evaluate possible noise sources, we consider the one dimensional FET model introduced by Sah[25] as shown in Fig. 58(a). Fluctuations in the width of the depletion region W manifest themselves as changes in the source-gate capacitance. We consider two possible sources of noise, Shockley-Hall-Read bulk traps and traps at the surface layer of the Schottky-barrier gate.

5.6.1 SHR bulk traps

In the depletion region, the concentration of carriers is so low that changes in the trap occupany occur only due to emission processes. Since the emission of a hole is equivalent to the absorption of an electron from the valence band, the rate of change of the number of filled traps in the depletion region is

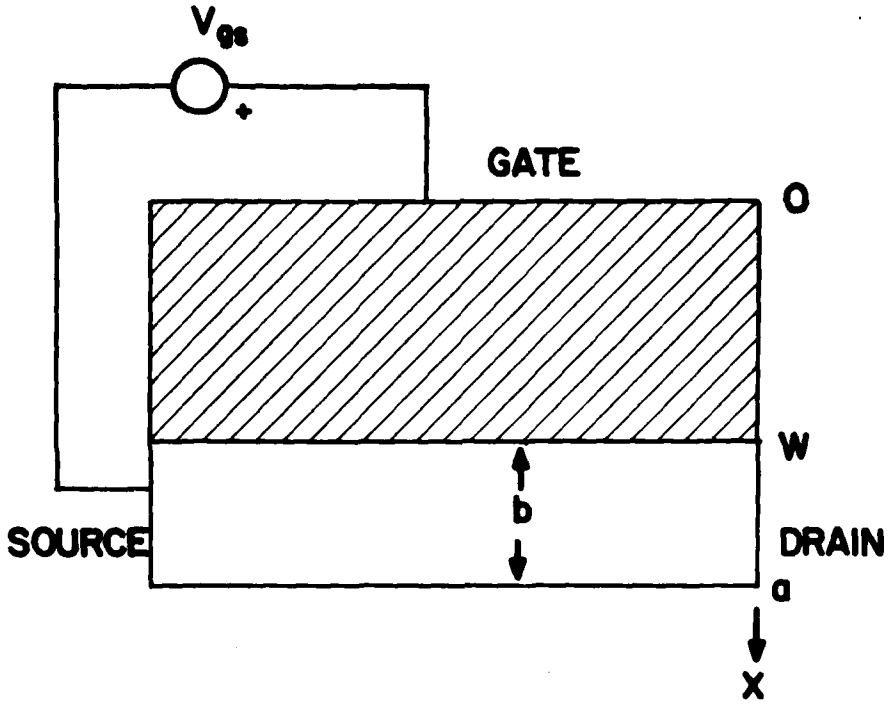
$$\frac{\partial f_t}{\partial t} = e_p(1-f_t)-e_n f_t \qquad (34)$$

where f_t is the fraction of filled traps.

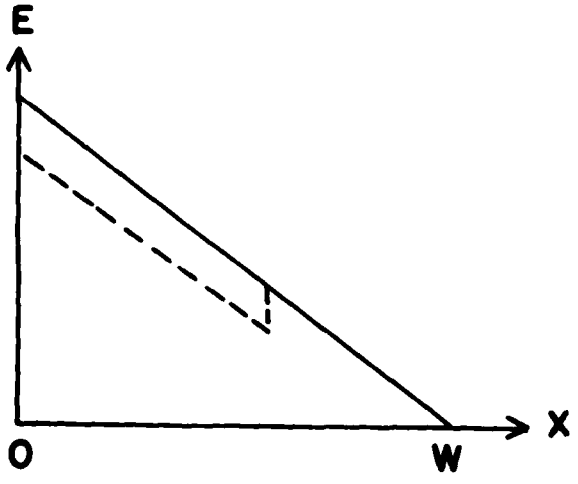
Since the source-gate voltage is related to the capacitance by the equation

$$V_{gs} + \phi_b = \frac{q}{\varepsilon} \int_o^W x\, N_d(x)dx \qquad (35)$$

where ϕ_b is the built-in potential, we can relate a fluctuation in the gate-source capacitance to an equivalent noise fluctuation. In the depletion layer, $N_d(x)$ can be considered as a constant doping N_d less the fluctuation in the number of filled traps, i.e.,



(a) One-Dimensional Model of Gate Depletion Zone of FET



(b) Depletion Field Distribution Showing Perturbation Caused by Trap Fluctuation.

Figure 58. FET Model Relevant to Analysis of Noise from Bulk Traps.

$$\delta V_{gs} = \frac{q}{\varepsilon} [W N_d(W) \delta W + x_1 \delta n_t \Delta x_1]$$

where $\Delta x_1 \delta n_t$ is the change in the concentration of filled traps in the volume element $A\Delta x_1$, where A is the area of the gate. Following Sah, we consider the depth W fixed. The electric field perturbation is shown in Fig. 58(b). Sah shows that the noise voltage fluctuation in a frequency interval Δf satisfies

$$v_n^2 = \frac{4\Delta f \tau_t}{1+\omega^2\tau_t^2} \left(\frac{q}{\varepsilon}\right)^2 \frac{N_t W^3}{3A} f_t(1-f_t) \qquad (36)$$

where N_t is the concentration of traps which have been assumed to be uniformly distributed across the depletion zone. The other variables in Eq. (36) are τ_t = trap decay time, A = gate area, and ε = the dielectric constant for GaAs.

The equilibrium occupation factor $f_t = e_p/(e_p+e_n)$ so that to have a large magnitude for Eq. (36) we need to have e_p approximately equal to e_n. As a possible example, Lang and Logan[26] have discussed the chromium trap level which has an energy level 0.61 eV below the conduction band and is approximately 2/3 filled with electrons at equilibrium. In this case the product $f_t(1-f_t)$ has the value 0.22 compared to its maximum value of 0.25.

For a fluctuation of δn_t, the time dependence will follow an exponential decay according to Eq. (34) where

$$\tau_t = (e_n+e_p)^{-1} \qquad (37)$$

The emission times can be written as

$$e_{na} = \gamma_n \sigma_{na} T^2 \exp [-(E_c-E_t)/kT] \qquad (38)$$

where $\gamma_n = 2.28 \times 10^{20} cm^2/sec - {}^\circ K^2$ and σ_{na} is an effective cross section.[22] Values for trap levels have been measured with E_c-E_t around 0.72 eV and σ_{na} around $10^{-14} cm^2$, so that decay times around 1 ms corresponding to noise frequencies near 1 kHz are reasonable.

The experimental measurements show that the noise fluctuations decrease as 1/f which does not agree with Eq. (36) for a single trap level. However, McWhorter has shown that if the trap density is spread out over a range of decay times, Eq. (36) can explain 1/f noise. This requires the number of traps in a volume ΔV with decay times between τ and $\tau+d\tau$ to be

$$\frac{N_t}{\ell n(\tau_2/\tau_1)} \frac{d\tau}{\tau} \Delta V \quad , \tag{39}$$

so that $N_t \Delta V$ is the total number of traps in ΔV and the distribution extends from τ_1 to τ_2 but vanishes outside this interval. Then, applying the Wiener-Khinchin theorem to Eq. (39), we obtain

$$v_n^2 = \frac{N_t}{\ell n(\tau_2/\tau_1)} \left(\frac{q}{\varepsilon}\right)^2 \frac{W^3}{3A} f_t(1-f_t) \frac{\Delta f}{f} \tag{40}$$

where we have assumed that $\omega t_2 >> 1$ and $\omega\tau_1 << 1$ so that

$$\int \frac{d\tau}{1+\omega^2\tau^2} \cong \frac{1}{4f} \quad .$$

For a numerical evaluation of Eq. (40) we take $f_t = 2/3$, $\tau_2/\tau_1 = 10^6$, $W = 0.27$ μm and the gate area as 1 μm × 500 μm, corresponding to our experimental FET. Then the fluctuation in the gate-source voltage would be

$$v_n^2 = 4.4 \times 10^{-25} N_t \Delta f/f \quad . \tag{41}$$

From the experimental measurements, it was found that

$$v_n^2 = \langle \Delta^2 V_{sg} \rangle = \langle \Delta^2 f_o \rangle / |S|^2$$

where $|S|$ was measured as 122 MHz/V and $\langle \Delta^2 f_o \rangle = 5.8 \times 10^7 / f_m^{0.98}$,

$$v_n^2 = 3.9 \times 10^{-9} \frac{\Delta f}{f^{0.98}} \quad . \tag{42}$$

The expressions (41) and (42) would only be in agreement if N_t were $8.9 \times 10^{15} cm^{-3}$.

In earlier measurements in this laboratory bulk trap densities in GaAs, of $2 \times 10^{14} cm^{-3}$ were measured in low doped $2 \times 10^{15} cm^{-3}$ GaAs "Fat FET's." When the same measurements were repeated with the 10^{17} doping used in GaAs, bulk traps were not detected which suggested that the trap density did not increase as the doping level increased, since the trap signature is proportional to the ratio N_t/N_d. Thus the measured source-gate noise is about an order of magnitude larger than would be predicted on the basis of the above analysis.

The decay times should be on the order of $1/\tau_1 \cong 1$ Hz and $1/\tau_2 \cong 1$ MHz. On the basis of Eq. (38) and a cross section of $10^{-14} cm^2$ this would correspond to $E_c - E_t$ ranging from 0.65 eV to 0.30 eV.

5.6.2 Surface traps

An alternate source for the fluctuation in source-gate capacitance is the fluctuation of surface trap occupancy. Figure 59 is a schematic diagram of the surface trap energy levels. This model is essentially that proposed by Crowley and Sze[28] to explain the built-in voltage at a Schottky barrier, except that they considered the applied reverse bias to be zero.

The model in Fig. 59 illustrates surface states in the semiconductor being physically separated from the metal by an insulating oxide of thickness δ. The electric charge Q_m per unit area is produced at the surface of the gate metal. Electrons can tunnel through the oxide to fill the semiconductor surface states up to the Fermi level of the metal. This model is discussed in more detail by Holway and Adlerstein[27] who found that DLTS measurements attributed to these surface traps were considerably stronger than the signatures from bulk traps.

In the diagram of Fig. 59 if we neglect terms of order kT/e compared with the work potential, the built-in potential is equal to the barrier height,

$$\phi_b = \phi_m - \chi - \Delta \quad , \tag{43}$$

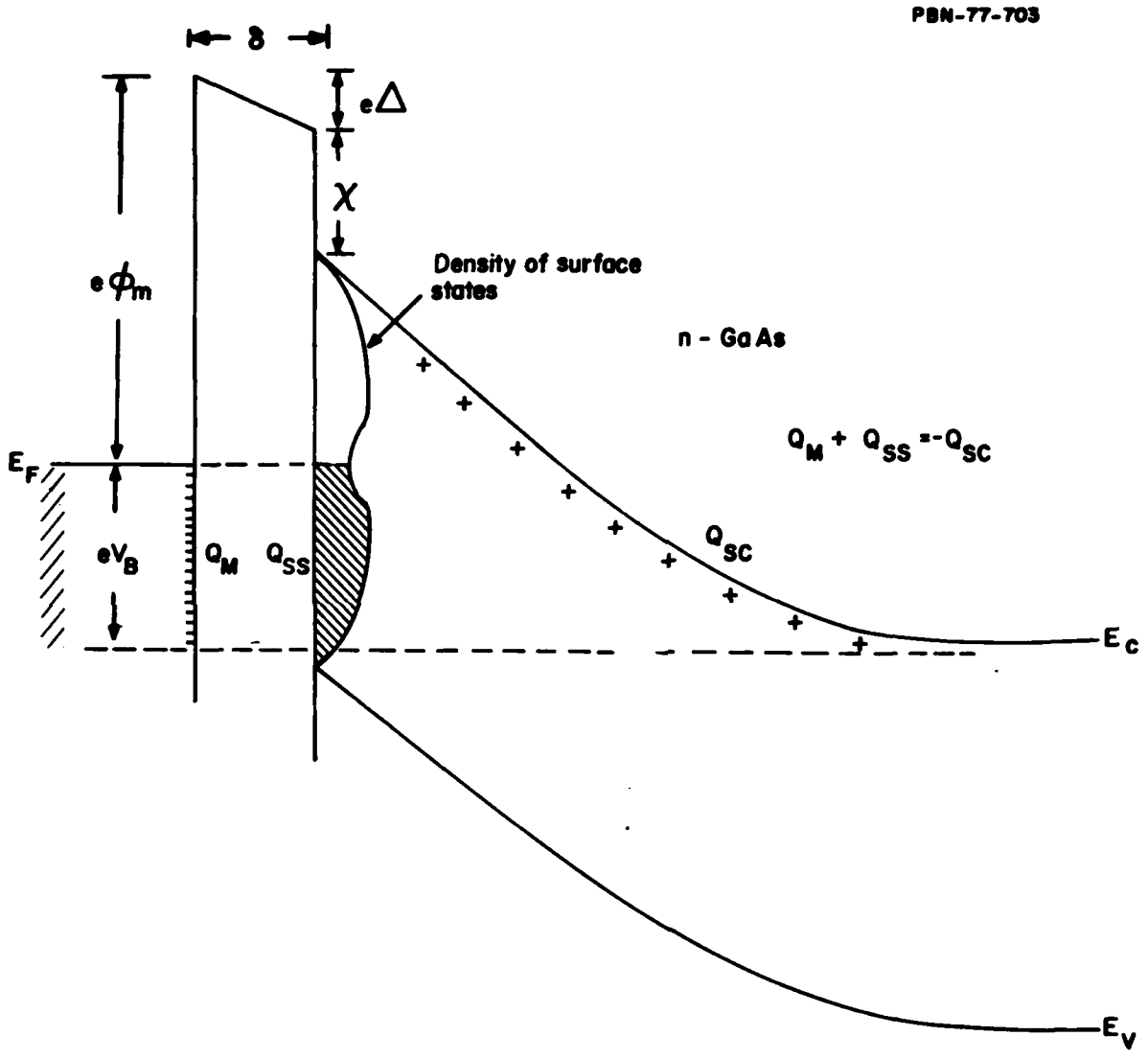


Figure 59. FET Model Relevant to Analysis of Noise from Surface Traps.

where ϕ_m is the metal work function, χ is the electron affinity of the semiconductor (in volts) and Δ is the potential drop across the insulation with a dielectric constant ε_i. The equations determining the charge densities become

$$Q_m + Q_{ss} + Q_{sc} = 0 \tag{44}$$

$$Q_{sc} = \sqrt{2\varepsilon q N_d (V_B + \phi_b)} \tag{45}$$

$$\Delta = -(\delta/\varepsilon_i) Q_m \tag{46}$$

and

$$Q_{ss} = -qD_s(E_{gap} - q\phi_o - q\phi_b) \tag{47}$$

where V_B is the applied barrier (gate-source) potential, D_s is the density of quantum states per unit area, $q\phi_o$ is the neutral point in the energy spectrum of the surface states, Q_{sc} is the charge density per unit area in the depletion region with doping N_d. Q_m is the charge density per unit area at the surface of the metal and Q_{ss} is the charge density per unit area in the surface states. Equations (44-47) are discussed by Holway and Adlerstein[27] but the same equations are given by Crowley and Sze[28] except that the applied bias V_B equals zero in their formulation.

Now suppose a fluctuation δQ_{ss} occurs in the surface state charge. The charges Q_m and Q_{sc} will adjust to satisfy Eqs. (43-46) in times short compared to a microsecond, but the equilibrium equation (47) will not be satisfied until enough time has passed for tunnelling through the insulating oxide layer. The experiments carried out earlier suggested that the times were on the order of 1-100 ms and that these relaxation times vary depending upon the position in the energy gap.

The change δQ_{ss} causes change δQ_m, δQ_{sc}, $\delta\Delta$ and $\delta\phi_b$ which can be found from Eqs. (43-46). To keep the length W fixed it will be necessary to induce a fluctuation δV_B in the applied gate-source potential which just compensates the change $\delta\phi_b$ in Eq. (45). The result is

$$\delta V_B = -\delta\phi_b = \left(\frac{\delta}{\varepsilon_i}\right) \delta Q_{ss} \quad . \tag{48}$$

On the other hand, if we keep V_B (the applied gate bias) fixed and let the depletion width vary, we find

$$\delta\phi_b = -\frac{\delta Q_{ss}}{\left(\varepsilon_i/\delta + \sqrt{\frac{\varepsilon q N_d}{2(V_B+\phi_b)}}\right)} \quad . \tag{49}$$

The tunnelling time through a barrier of thickness ℓ is

$$\tau = \tau_o \exp(\alpha\ell) \tag{50}$$

where α depends on barrier height but is a number on the order of $10^8 cm^{-1}$. Let n_T be the number of traps per unit area and n_t be the number of trapped electrons. Then according to van der Ziel[29] the variance in the number of filled traps per unit area is

$$\langle \Delta n_t^2 \rangle = n_T \lambda(1-\lambda) \tag{51}$$

where λ is the probability that a trap is occupied. Since only those traps near the Fermi level are effective, then

$$\lambda \cong 1/2$$

and

$$\langle \Delta n_t^2 \rangle = 1/4\ n_T \tag{52}$$

so that

$$S_{n_t} = n_T A \frac{\tau}{1+\omega^2\tau^2} \tag{53}$$

where S_{n_t} is the spectral density of the probability.

Now assume that ℓ in Eq. (50) is the average distance of the trap from the interface and that the probability distribution is uniformly distributed in ℓ from ℓ_1 to ℓ_2 and zero otherwise. Then, integration of Eq. (53) over the distribution gives

$$S_{n_t} = \frac{n_T A}{\omega \ell n(\tau_2/\tau_1)} \left[\arctan(\omega\tau_2) - \arctan(\omega\tau_1)\right] , \qquad (54)$$

where τ_1 and τ_2 corresponds to ℓ_1 and ℓ_2 from Eq. 50. Then from Eq. (48), if $\tau_2/\tau_1 = 10^6$, corresponding to $10^2 \leq f_m \leq 10^5$ and taking $\omega\tau_1 << 1 << \omega\tau_2$, Eq. (54) implies

$$v_n^2 = \left(\frac{\delta}{\varepsilon_i}\right)^2 S_{n_t} \qquad (55a)$$

$$= \left(\frac{\delta}{\varepsilon_i}\right)^2 \frac{n_T q^2}{4fA\ell n(\tau_2/\tau_1)} \qquad (55b)$$

With $A = 5 \times 10^{-6}\text{cm}^2$, $\delta = 40$ Å and $\varepsilon_i = 8.85 \times 10^{-14}$,

$$v_n^2 = 2 \times 10^{-21} n_T \frac{\Delta f}{f} . \qquad (55c)$$

Equation (55c) will be in agreement with the experimental measurement of Eq. (42) if the surface density of traps is

$$n_t = 2 \times 10^{12}\text{cm}^{-2} .$$

This magnitude for the surface trap density seems reasonable. The earlier DLTS experiments[27] showed surface trap signatures which were more than an order of magnitude larger than the signature of bulk traps. Although we still consider the surface trap model of noise tentative, the model appears to be worth further analytical investigation.

5.6.3 Conclusions

Experimental results indicate that depletion layer (capacitance) modulation by traps appears to be the primary source of near carrier noise in GaAs FET's. Theory indicates that of the two possible sources, bulk or surface traps, surface traps appear to be more reasonable, based on the required density to produce the observed noise, and from independent studies of traps by DLTS experiments. Interface traps, from limited substrate modulation experiments, do not seem to be important sources of 1/f noise. Further experimental studies, however, are necessary to establish this conclusion on a firmer basis.

6.0 NONLINEAR OSCILLATOR MODEL

6.1 Introduction

One of the objectives of this contract was to develop a nonlinear (large-signal) model of the FET oscillator which can be used with practical circuitry to predict such performance parameters as frequency of oscillation, power output, and efficiency. For this purpose a nonlinear model based on the frequency domain, rather than on the time domain, was preferable. During this reporting period, such an analysis, based on the work of Y. Tajima[30] of our laboratory, was initiated.

The validity of this model was established by its success in predicting the large-signal (oscillating) performance of an FET imbedded in an actual circuit.

The circuit employed for this study was that used in our rf noise studies. The schematic for this circuit is shown in Fig. 60. An FET is located in the middle of a microstrip circuit, wherein the FET gate is connected to an rf choke by means of a wire inductance, while the source is bonded to a long stripline which is terminated by another rf choke. The dc drain bias is fed through a bias tee at the drain port. The gate bias is applied through the gate choke. The source choke is connected to ground for the dc return. RF output power is obtained from the drain port via a matching circuit. The circuits connected to the source and gate terminals function together as a resonator and a feedback circuit, respectively.

This oscillator circuit for purposes of analysis can be divided into two parts at the plane where the drain is connected to the output matching circuit. The admittances at this plane "looking" to the right and left are denoted by $Y_{\ell d}$ and Y_a. The admittance $Y_{\ell d}$ represents the load and its matching circuit. The admittance Y_a includes the FET and its source and gate terminations. The oscillator condition is determined by the equation

$$Y_a(A, \omega) + Y_{\ell d}(\omega) = 0 \tag{56}$$

where A represents the rf voltage amplitude dependence of Y_a. The frequency dependence is represented by ω. The amplitude dependence of Y_a, of course, stems from the nonlinear behavior of the FET. The frequency behavior of the linear admittance $Y_{\ell d}$ is easy to establish, given the circuit configuration. However, the amplitude and frequency dependence of $Y_a(A, \omega)$ is more difficult to determine.

The first step of this study is to establish the nonlinear behavior of $Y_a(A, \omega)$ and to obtain the correlation between $Y_a(A, \omega)$ and the FET equivalent circuit. To do this, the FET in Fig. 60(a) is represented in terms of its equivalent circuit, as shown in Fig. 60(b).

Under large-signal operation, the element values of the FET equivalent circuit, shown in Fig. 60(b), vary with time because at large driving levels they become dependent on terminal voltages. We may consider two of the terminal voltages to be independent and choose the set V_{gs} and V_{ds}, V_{gs} being the voltage across the gate capacitance and V_{ds} that across the drain conductance. If we restrict our interest to the signal frequency and ignore the effects due to higher harmonic components, these voltages can be written as

$$\begin{aligned} V_{gs} &= V_{gso} + v_{gs} \cos(\omega t + \phi) \\ V_{ds} &= V_{dso} + v_{ds} \cos \omega t \end{aligned} \tag{57}$$

where V_{gso} and V_{dso} are the dc bias voltages, v_{gs} and v_{ds} the amplitudes of signal frequency components, and ϕ the phase difference between the gate and drain voltages. The equivalent circuit for the signal frequency can now be expressed as a function of the following parameters, which are independent of time: V_{gso}, V_{dso}, v_{gs}, v_{ds}, ω, and ϕ.

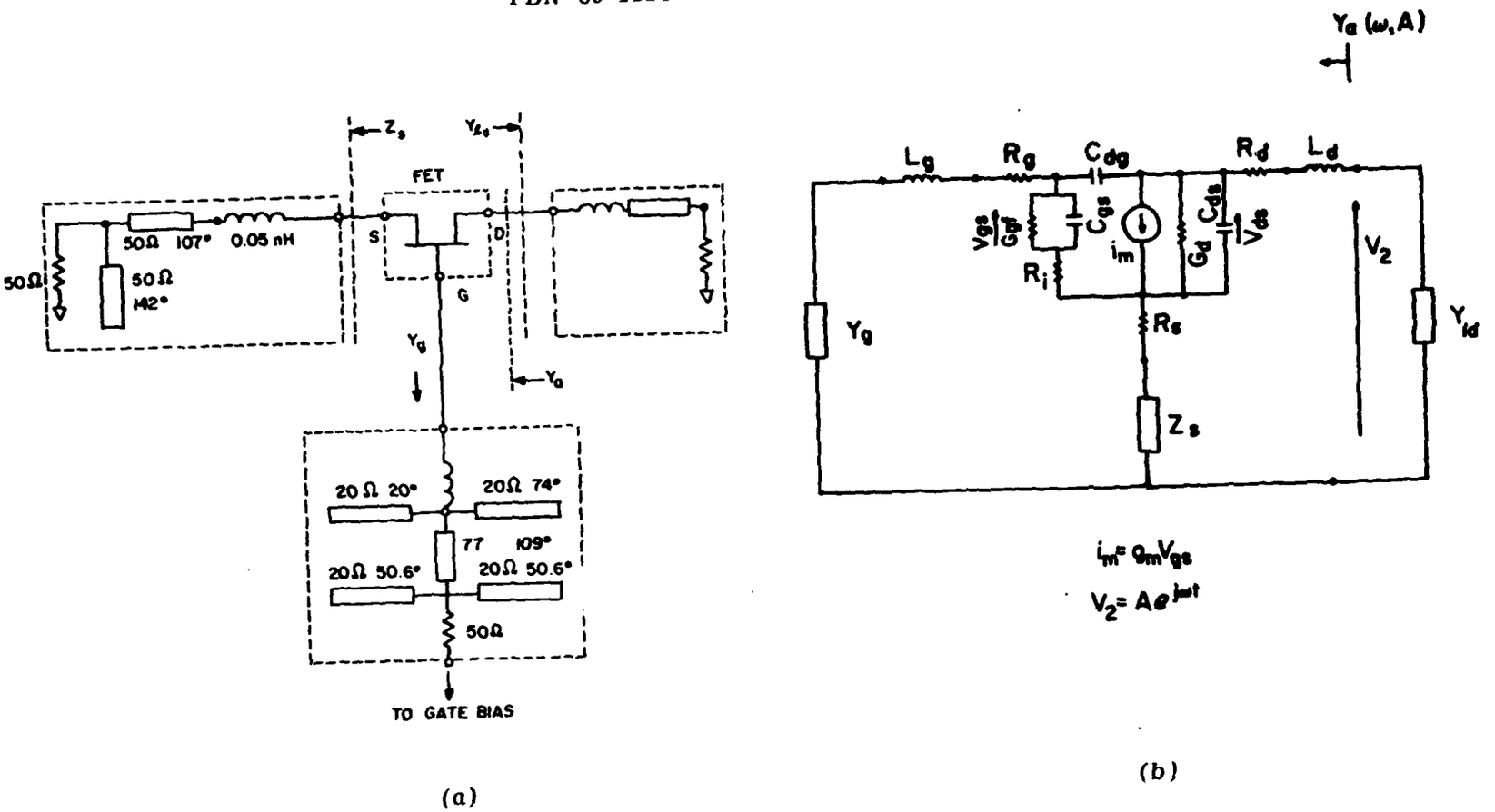


Figure 60. Schematic of oscillator circuit and equivalent circuit of FET used in oscillator analysis.

In order to avoid unnecessary complexity of calculations, we limit the nonlinear behavior to five elements, gate forward conductance G_{gf}, gate capacitance C_{gs}, gate charging resistance R_i, transconductance g_m, and drain conductance G_d. This is justifiable. Here, G_{gf} represents the effect of the forward rectified current across the gate junction under large-signal operation. No voltage dependence was assumed for the parasitic elements, that is, the lead inductances (L_g, L_d, L_s) and contact resistances (R_g, R_d, R_s). Also ignored was the small voltage dependence of the drain channel capacitance C_{ds} and feedback capacitance C_{dg} because of their small values.

6.1.1 Expressions for g_m and G_d

Transconductance g_m and drain conductance G_d are defined as

$$g_m = \left(\frac{i_{ds}}{v_{gs}} \right)_{v_{ds}=0} \qquad G_d = \left(\frac{i_{ds}}{v_{ds}} \right)_{v_{gs}=0} \tag{58}$$

where i_{ds} is the rf drain current amplitude. The instantaneous drain current can be written in terms of g_m and G_d as

$$I_{ds}(t) = I_{dso} + g_m v_{gs} \cos(\omega t + \phi) + G_d v_{ds} \cos \omega t \tag{59}$$

where I_{dso} is the dc drain current. In this expression linear superposition of the dc and rf currents is assumed.

Now, if we have a function which can simulate the nonlinear dependence of the drain current I_{ds} on V_{gs} and V_{ds}, as

$$I_{ds} = I_{ds}(V_{gs}, V_{ds}) \quad , \tag{60}$$

then, under large-signal conditions, the instantaneous current $I_{ds}(t)$ can be obtained by inserting Eq. 57 into Eq. 60. By multiplying $\sin\omega t$ by Eq. 60 and integrating over a complete period, g_m is obtained as

$$g_m = -\frac{\omega}{\pi v_{gs} \sin\phi} \int_0^{\frac{2\pi}{\omega}} I_{ds} \sin \omega t \quad dt \quad . \tag{61}$$

Similarly, G_d is obtained as

$$G_d = \frac{\omega}{\pi v_{ds} \sin\phi} \int_0^{\frac{2\pi}{\omega}} I_{ds} \sin(\omega t + \phi) \quad dt \; . \tag{62}$$

Equations 61 and 62 are now functions of rf amplitudes v_{gs} and v_{ds}, as well as of bias voltages V_{gso} and V_{dso}. We turn now to a more detailed discussion of the nonlinear relation, Eq. 60.

The functional relation $I_{ds}(V_{gs}, V_{ds})$ was established empirically by simulating the dc I-V characteristics by a nonlinear function. We chose the one below, though others might work just as well. Thus,

$$I_{ds}(V_{ds}, V_{gs}) = I_{d1} \cdot I_{d2} \tag{63}$$

$$I_{d1} = \frac{1}{k}\left[1 + \frac{V'_{gs}}{V_p} - \frac{1}{m} + \frac{1}{m}\exp\left\{-m\left(1 + \frac{V'_{gs}}{V_p}\right)\right\}\right]$$

$$I_{d2} = I_{dsp}\left[1 - \exp\left\{\frac{-V_{ds}}{V_{dss}} - a\left(\frac{V_{ds}}{V_{dss}}\right)^2 - b\left(\frac{V_{ds}}{V_{dss}}\right)^3\right\}\right]$$

$$k = 1 - \frac{1}{m}\{1 - \exp(-m)\}$$

$$V_p = V_{po} + pV_{ds} + V_\phi$$

$$V'_{gs} = V_{gs} - V_\phi$$

where V_{po} (> 0) is the pinchoff voltage at $V_{ds} \approx 0$,
V_{dss} is the drain current saturation voltage,
V_{ϕ} is the built-in potential of the Schottky barrier,
I_{dsp} is the drain current when $V_{gs} = V_{\phi}$,

and a, b, m, and p are fitting factors that can be varied from device to device.

6.1.2 Nonlinear expressions for C_{gs}, G_{gf}, and R_i

Although the gate junction is also a function of V_{gs} and V_{ds}, we assume here that it can be approximated by a Schottky barrier diode between gate and source, with V_{gs} as the sole voltage parameter. Gate capacitance C'_{gs} and forward gate current i_{gf} can be found from Schottky barrier theory as

$$C'_{gs} = \frac{C'_{gso}}{\sqrt{1-V_{gs}/V_{\phi}}} \qquad (-V_p \leq V_{gs}) \tag{64a}$$

or

$$C'_{gs} = \frac{C'_{gso}}{\sqrt{1+V_p/V_{\phi}}} \qquad (-V_p \geq V_{gs}) \tag{64b}$$

$$i_{gf} = i_s(\exp \alpha V_{gs} - 1) \tag{65}$$

where C'_{gso} is the zero bias gate capacitance, i_s the saturation current of the Schottky barrier, and $\alpha = q/nkT$.

When V_{gs} varies according to Eq. 57 the effective gate capacitance C_{gs} and gate forward conductance G_{gf} for the signal frequency are obtained from Eqs. 57, 64, and 65 as

$$C_{gs} = \frac{1}{\pi V_{gs}} \int_0^{2\pi} \left(\int^{V_{gs}} C'_{gs}\, dv \right) \cos \omega t \; d(\omega t) \qquad (66)$$

$$G_{gf} = 2i_s \exp(\alpha V_{gso}) \frac{I_1(\alpha V_{gs})}{V_{gs}} \qquad (67)$$

where $I_1(x)$ is the modified Bessel function of the first order.

The gate charging resistance R_i was assumed to vary in such a way that the charging time constant was invariant with bias.[1]

$$R_i \cdot C_{gs} = \tau_i \text{ (constant)} \qquad (68)$$

Thus, all nonlinear element values of the equivalent circuit can be expressed in terms on the terminal rf amplitudes and their relatiye phase. One may now determine more precisely the admittance $Y_a(A,\omega)$, or $Y_a(v_{gs},v_{ds},\omega)$. by an iteration method such as the following.

First, starting values for v_{gs} and the equivalent circuit parameters are assumed. For the latter, small-signal values based on measured S-parameters are suitable. With these parameters specified, the output voltage v_{ds} and its phase can be calculated in a straightforward manner. With the resultant value of v_{ds}, ϕ, and the initially assumed V_{gs}, the "first cut" evaluation of the equivalent circuit elements can be made with the help of Eqs. 61, 62, and 66-68. The above procedure is then repeated, each time, using the most recently evaluated values of v_{ds}, ϕ, and v_{gs}, until convergence is obtained. The process converges when successive iterations reproduce the equivalent circuit parameters to within some specified error. Once convergence is achieved, such oscillator properties as power output and efficiency can be calculated.

6.2 Analytic Simulation of I-V Characteristics

The analysis begins by applying the analytic expressions (Eq. 63) to the set of measured I-V characteristics shown in Fig. 61(a). The fitting

parameters a, b, m, and p in these equations were determined, and the simulated I-V characteristics calculated. Figure 61(b) is the result of this simulation. Note the excellent agreement (of course, the hysteresis shown in Fig. 61(a) cannot be represented).

6.3 Equivalent Circuit Derivation

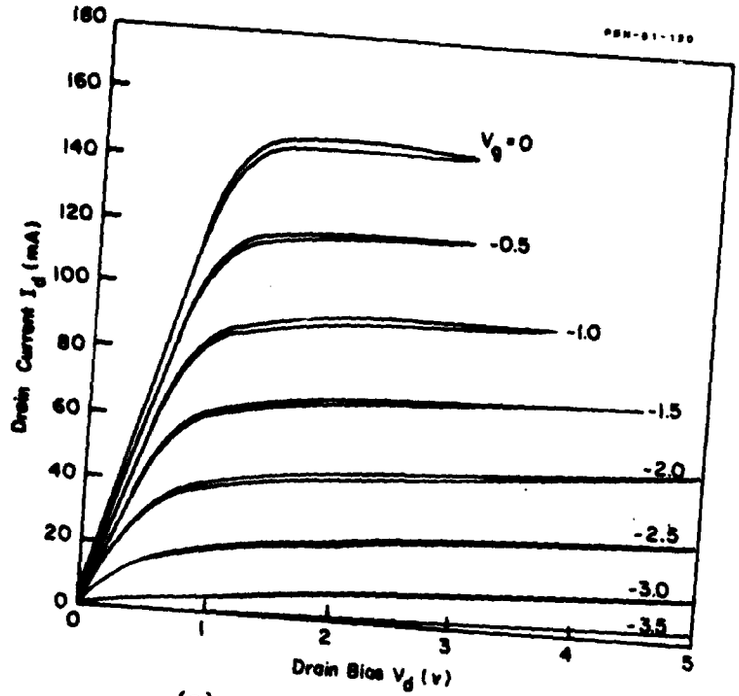
Next, the small-signal S-parameters were measured over a broad frequency range (2-12 GHz) at the operating bias conditions for the oscillator. These were used to determine the equivalent circuit element values, Fig. 62. These element values were determined by using the COMPACT computer-aided design program which optimizes the equivalent circuit element values to provide a "good" fit to the measured S-parameters.

Figure 63 illustrates the excellent agreement between measured S-parameters and those calculated from the equivalent circuit. This establishes confidence in the equivalent circuit element values.

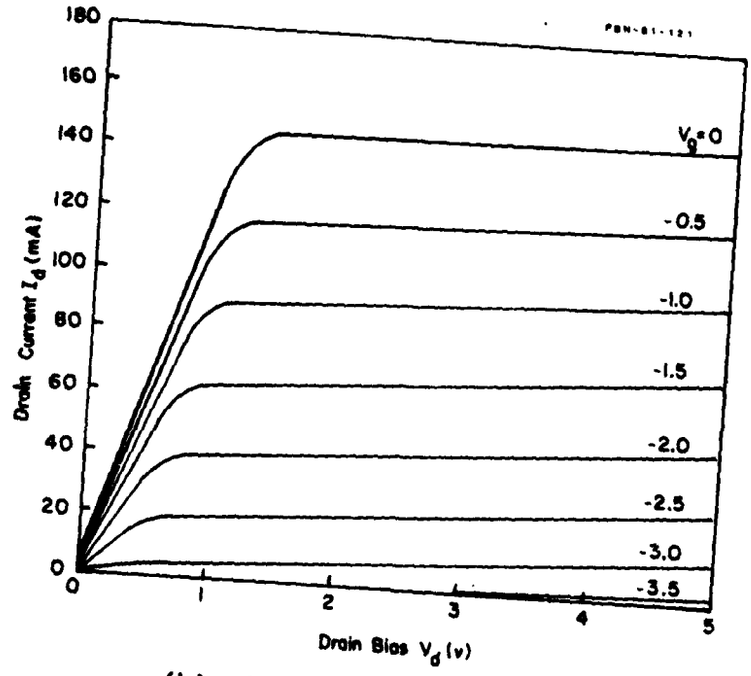
The equivalent circuit elements are used for two purposes: (1) to determine what range of circuit terminations are necessary to initiate oscillations, i.e., establish instability; and (2) to establish initial conditions for the nonlinear analysis.

6.4 Determination of Oscillation Conditions

The oscillation conditions, that is, the load conditions at the drain terminals necessary for oscillations to start, are delineated by the shaded regions in Fig. 64. Shown is a plot of $-Y_a/Y_o$, where $Y_o = 0.02$ mhos is the characteristic line admittance. This plot was obtained for the conditions where the source and gate terminals were terminated by the oscillator circuit elements established earlier, Fig. 60(a). The unstable regions where oscillation is possible was determined by the Nyquist criterion. It shows that oscillation is most likely to occur close to 10 GHz, but with greater mismatch, oscillation could also occur at lower



(a) measured I-V characteristic



(b) simulated I-V characteristic

Figure 61. Measured and simulated I-V characteristic used in nonlinear oscillator analyzer.

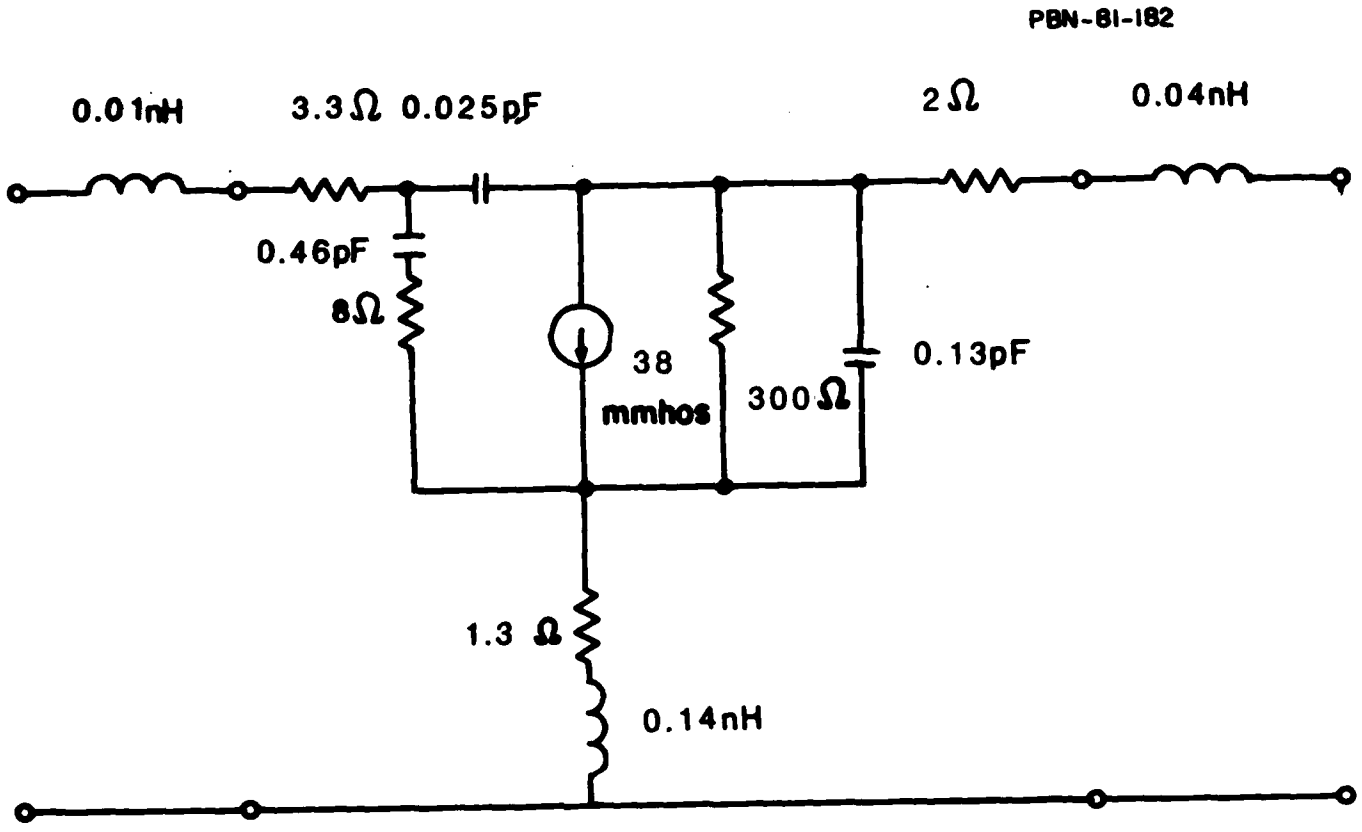


Figure 62. Equivalent circuit of FET based on measured S-parameters.

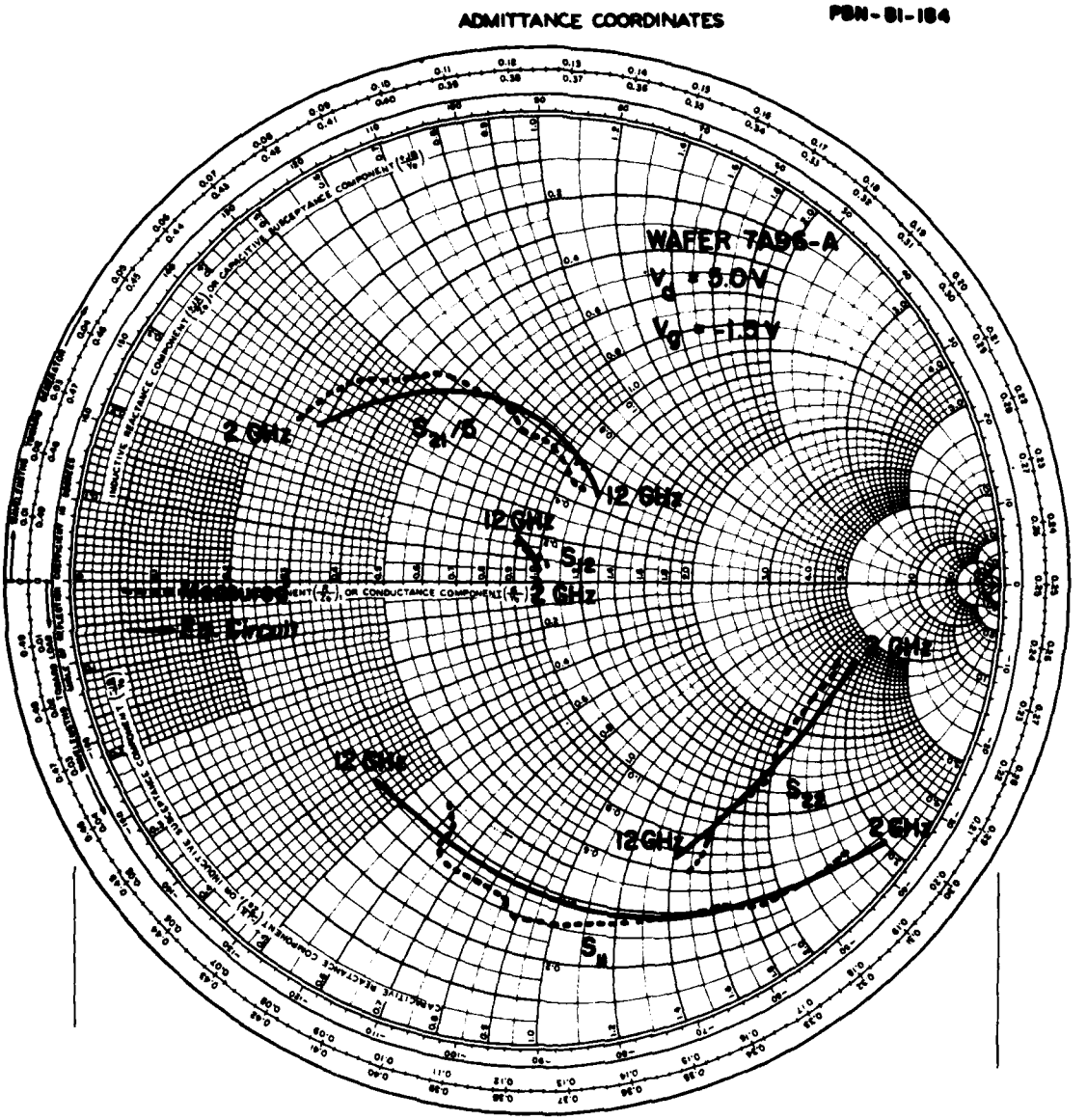


Figure 63. Comparison of measured S-parameters and calculated S-parameters based on equivalent circuit.

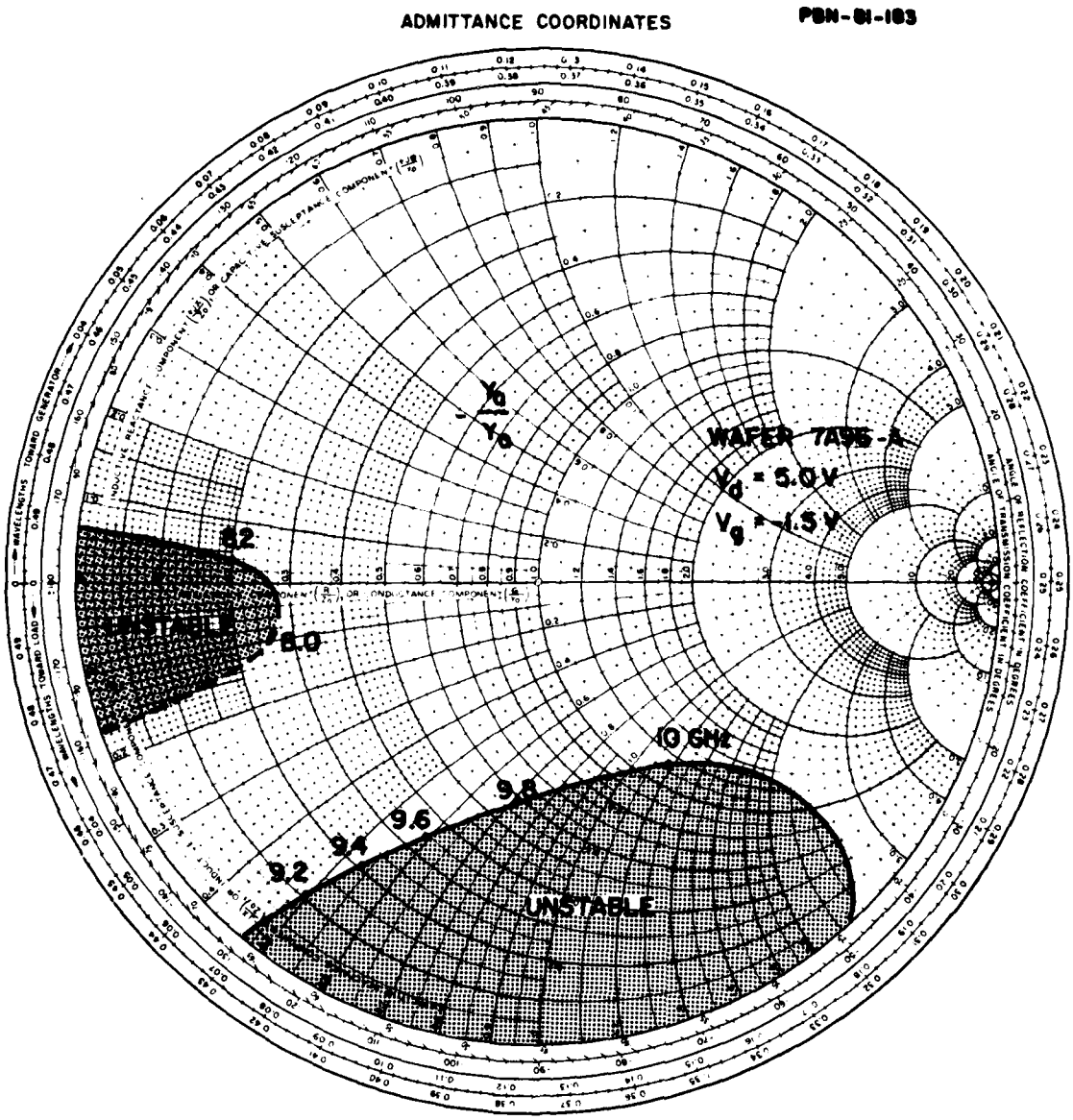


Figure 64. Domains of load admittance (dotted areas) which support oscillations in FET circuit. Reference plane for load is that marked "Y_a" in Fig. 60(a).

frequencies, 6-8 GHz. Past measurements with similar FETs have shown a tendency to hop in frequency as the circuit was tuned.

6.5 Nonlinear Analysis

Having established the oscillation conditions, we now apply the equivalent circuit elements and the nonlinear equations from the dc I-V simulation to determine the oscillator properties under steady-state oscillation conditions for the permissible range of load terminating conditions.

The result of the nonlinear analysis is shown in Fig. 65. Shown are closed constant output power contours (in dBm) as a function of load (drain) terminating conditions. Also shown are intersecting loci of constant frequency contours. For example, the 10 GHz contour shows the predicted power output at various terminating admittance levels. The power levels indicated are in the range obtained experimentally as shown by the measured data.

6.6 Conclusion

A large signal model of the FET has been derived. This model has been applied to an FET embedded in an actual oscillator circuit, and the predicted performance has been shown to be consistent with experimental results.

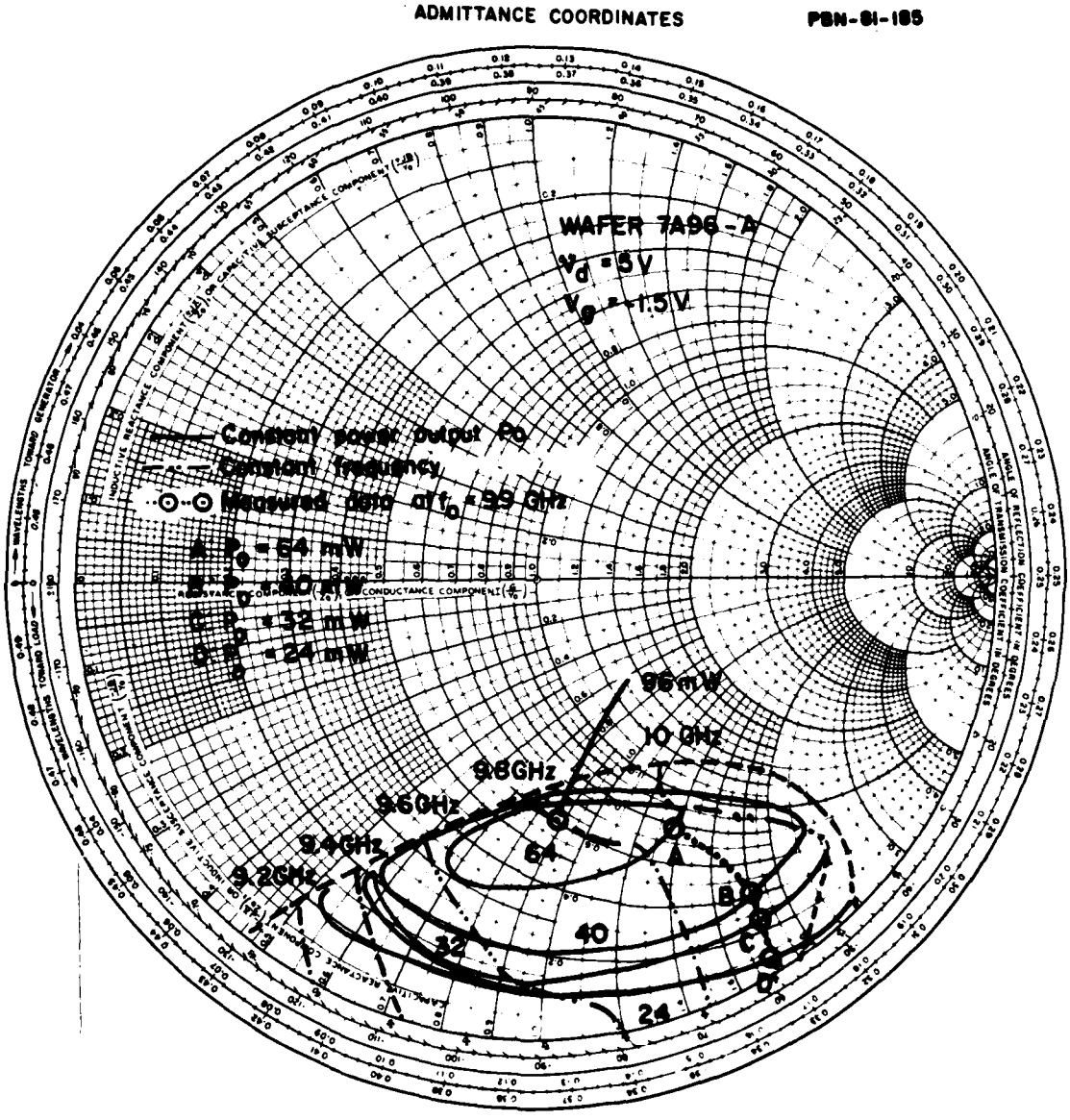


Figure 65. Calculated constant frequency and power output contours for FET oscillator circuit. These contours represent load admittance conditions at the drain which are necessary to yield the stated power output at the given frequency. Also shown are measured oscillator data.

7.0 SUMMARY AND CONCLUSIONS

An extensive experimental study has been made of the 1/f noise properties of FET oscillators constructed of chips fabricated under a variety of controlled conditions. With use of in-house grown epitaxial layers, FETs were fabricated from both buffered and unbuffered active layers, with and without epitaxially grown contact layers, and with and without surface passivation. Substrates from Sumitomo and Crystal Specialties were used.

Our results show that the contact layer has no effect on the 1/f noise. The results with surface-passivated (SiO_x) chips were too variable to allow conclusions. The inclusion of the buffer layers produced a somewhat larger reduction in baseband noise for the Sumitomo devices than for the Crystal Specialties devices. The improvement in rf FM noise followed the trend for the baseband noise and was about 10 dB for the buffered devices.

The noise increases with drain bias and exhibits a pronounced increase at about 9 V at room temperature. Although we have not identified the source of this threshold-like condition, it does not appear to be avalanche breakdown. We suspect field ionization of traps. The noise exhibits a maximum with reverse gate bias at about half pinchoff. This behavior is similar to that of silicon FETs.

The 1/f noise as a function of temperature over the range 90°K to 300°K decreases monotonically and then begins to increase above this range. However, no evidence of an activation energy emerges from the data.

When the surface of the FET is exposed to optical illumination over the wavelength range covering the bandgap, the variation in 1/f noise is disappointingly small. However, this result may reflect the fact that the gate metal-GaAs interface region was not accessible. On the basis of DLTS measurements made by other workers, we expect this region to contain traps. We recommend that this region be studied by optical exposure through a thinned-down gate electrode and by variation of the gate metallization technology.

A good correlation has been obtained between the 1/f baseband noise and the measured 1/f near-carrier FM noise. Our analysis indicates that traps either in the depletion layer of the gate region or in surface states under the gate are responsible. Our theoretical model for these two possible mechanisms favors the surface states.

Measurements of the near-carrier 1/f noise show that the dependence with loaded Q follows the classical oscillator formulas. Large reductions in near-carrier noise with phase-locking techniques also were shown to obey the classical formulas. Some deviations, however, have been noted.

Our experiments show that were it not for the low Q-factors associated with integrated circuits, the FM noise level could be reduced to a rather respectable level when the Q-factor is of the order of 2000. To achieve such high Q-factors requires stabilization by high-Q cavities such as waveguide or high-K dielectric resonators.

A large-signal model of the FET has been derived which, when applied to an FET imbedded in an actual integrated circuit, predicts oscillator performance consistent with experimental results.

8.0 PROFESSIONAL PERSONNEL ASSOCIATED WITH THE RESEARCH EFFORT

The following staff members were associated with this effort.

1. Mr. Robert W. Bierig
2. Mr. Jack Curtis, Sr.
3. Mr. Raymond Ellis
4. Professor Hermann Haus (Consultant)
5. Dr. Lowell H. Holway, Jr.
6. Mr. William Labossier
7. Mr. Paul Ng
8. Dr. Robert A. Pucel
9. Dr. Hermann Statz
10. Dr. Yusuke Tajima
11. Mr. Robert Thomas
12. Miss Beverly Wrona

9.0 WRITTEN PUBLICATIONS IN TECHNICAL JOURNALS

No publications were published in connection with this effort.

10.0 INTERACTIONS

There were no talks or consultations connected with this effort.

11.0 NEW DISCOVERIES, INVENTIONS, OR PATENT DISCLOSURES AND SPECIFIC APPLICATIONS STEMMING FROM THE RESEARCH EFFORT

There were none.

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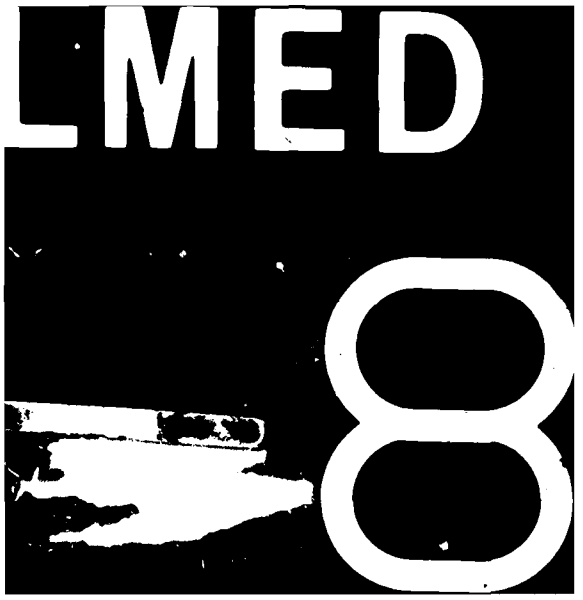
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