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MONOLITHIC INTEGRATION OF MICROWAVE GAAS POWER FETS. (U)
JAN 81 V SOKOLOV, R E WILLIAMS

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MONOLITHIC INTEGRATION OF MICROWAVE GaAs POWER FETs

Texas Instruments Incorporated
Central Research Laboratories
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Dallas, Texas 75265

January 1981

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gain compression point of 1.3 W at 9.0 GHz. The paraphase amplifier has demonstrated active balun action from 6.5 to 9.0 GHz. The gain is +3 dB for each antiphase output at 8.0 GHz and tracks within ± 0.75 dB over the 6.5 to 9.0 GHz frequency range. Phase tracking of the 180° characteristic is within $\pm 20^\circ$. Preliminary results for the 1.2 mm gatewidth FIPP devices indicate higher small signal gains than for conventional FETs with comparable gate width. Narrow-band small signal gains up to 12 dB have been obtained at 10 GHz.

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SECTION I INTRODUCTION

This report covers the progress made during the third year of a continuing research program for the monolithic integration of microwave GaAs power field effect transistors (FETs) under Contract No. N00014-77-C-0657. The objective of this program is to demonstrate the feasibility of monolithic GaAs microwave integrated amplifier circuits using power FETs in X-band. This report covers the period 1 October 1979 to 30 November 1980.

During the first 2 years of the program, a two-stage push-pull monolithic FET power amplifier with a small signal gain of 13 dB and an output 1 dB gain compression point of 1.1 W (saturated output power is 1.3 W) was developed. Work was also begun on the development of the monolithic paraphase amplifier that will drive the two-stage push-pull amplifier. Although paraphase chips were fabricated, only preliminary rf results were obtained. The results indicated that a small signal gain existed for these devices. Work was also initiated on the development of a fully integrated push-pull device. Mask sets were designed and submitted for fabrication.

Among the accomplishments of the past year are the following:

- Further amplifier results were obtained for the monolithic two-stage push-pull chip. At 9.0 GHz, a saturated output power of 1.4 W with 19-percent power-added efficiency and 12.4 dB gain was obtained. The small signal gain is 16 dB and the 1-dB gain compression point occurs at 1.3 W.
- The paraphase amplifier chip and the test fixtures were improved and new results were obtained. From 6.5 to 9.0 GHz, the two outputs from the differential FET pair have gains that track within ± 0.75 dB and are at the 3 dB level at mid-band (note that a passive balun would show a 3 dB loss). The phase tracking of the 180 degree characteristic is accurate to about ± 20 degrees over the same frequency range.
- A new "air-bridge" capacitor was conceived and implemented on monolithic circuits.
- Evaporated solder was used on the backs of monolithic chips to improve mounting.
- A fully integrated push-pull device exhibited 13 dB small signal gain at 9 GHz.

The remainder of this report presents details of these accomplishments.

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SECTION II

FABRICATION AND PROCESSING

Except for the specific items discussed below, GaAs monolithic slice processing parallels that of discrete GaAs devices. Both epitaxial and ion-implanted material have been used for fabrication. Device isolation is achieved either by etching mesas or by destroying the conductivity of the slice using a proton or boron implant. Source-drain regions are fabricated using alloyed AuGe/Ni. The source-drain pattern includes alignment marks to be used by the e-beam machine for gate definition (all other levels are defined using photolithography). Silicon nitride is used beneath the alignment marks so they will not alloy. The gate stripes are defined using e-beam lithography. The gates are then recessed and metallized using TiPtAu. The gates are nominally $0.7\text{ }\mu\text{m}$ long and $6,000\text{ }\text{\AA}$ thick.

The next level is a current spreading layer consisting of TiAu. Any gate pads or other features, such as transmission lines connecting to the gates, are formed at this step. The inductor patterns are also defined in this step using a separate mask (this requires a double-exposure of the resist). Next, silicon nitride is plasma deposited over the slice and capacitors are formed.

Contact areas and source pad areas are opened in the nitride and plated. Air-bridges are then formed to interconnect source pads. The slice is lapped to $100\text{ }\mu\text{m}$, metallized on the back, and scribed.

A. CAPACITOR FORMATION

During this year, the monolithic capacitor geometry was changed from that illustrated in Figure 1a to that of Figure 1b. The former geometry had been used to eliminate the yield problems that resulted from crossovers across an abrupt step when the top capacitor plate is connected to another metalization. This geometry has worked well. However, its disadvantage is that it produces a structure that really is two capacitors in series. This results in a capacitance half that of each component, or a quarter of the value that would result from a single capacitor using the same total area. Hence, it would be desirable to use single capacitors if a high yield crossover technique existed. We chose to use the plated-air-bridge procedure to realize this connection. Instead of connecting two source pads, the bridge connects the top capacitor plate and the lower level metal (Figure 1b).

This capacitor geometry was first implemented on the paraphase amplifier after changing two masks. Figure 2 shows one such chip. The two larger dark bars are the plated air-bridges used to interconnect the sources of the FETs. The four smaller dark bars are similar plated areas that connect a capacitor top plate to adjacent metalization. Their function is to assure a good connection without relying on a thin metalization step-over. The actual top plates are difficult to distinguish in the figure because their metalization (TiPt) is the same as the ground plane that serves as the lower capacitor plate. A number of capacitors on the first slice were probed and all were found to be functional. As expected, capacitance values are twice those of the double capacitors formerly fabricated. Values of 7.5 to 12.5 pF were measured for the various size capacitors. Since the operation of the paraphase amplifier requires good rf-bypass capacitors (4 places), these larger value capacitors improved the paraphase amplifier performance.

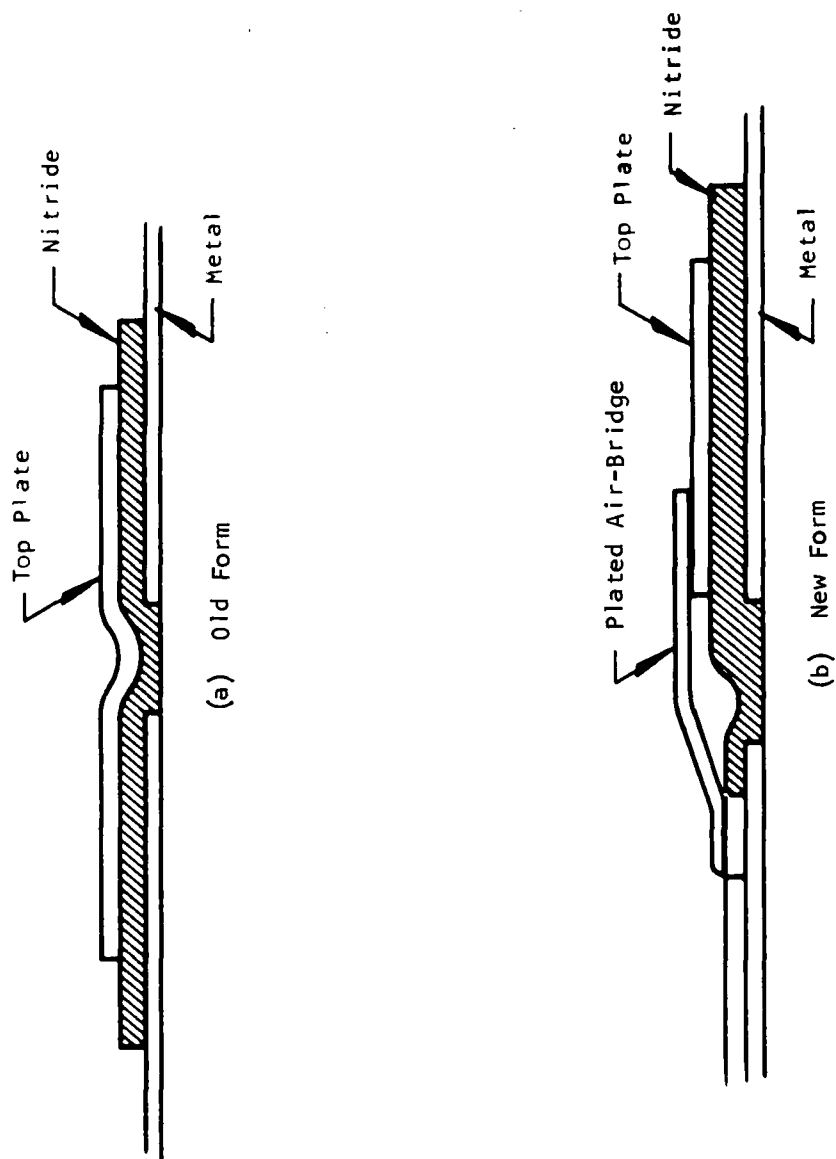


Figure 1 Monolithic Capacitor Geometries

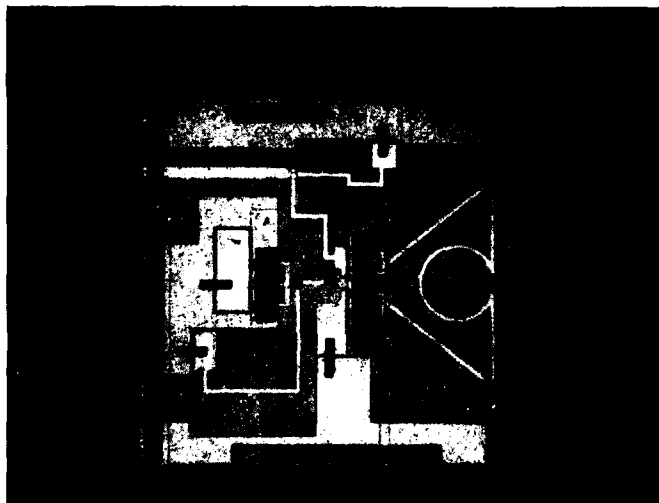


Figure 2. Paraphase Amplifier Chip Incorporating the New Form of Capacitor (see text)
 The four small, dark rectangles compose the step-over connection
 between the capacitor top plate and adjacent metalization

B. SOLDERING TECHNIQUES

Improved methods of soldering thin, large-area GaAs chips to metal headers were needed. Use of a low temperature solder, AgSn, greatly reduced cracking problems associated with thermal stresses. Nevertheless, it was still difficult to solder large-area, thin GaAs chips and be assured of a uniform thin solder joint (for thermal dissipation) having no voids. Smaller, less fragile discrete devices can be "scrubbed in" to assure good solder joints, but manipulation of larger, monolithic chips must be kept to a minimum to reduce the chance of damage.

A soldering procedure was investigated that has shown good results. A thin layer of AgSn solder is evaporated onto the back of the slice before scribing, and a thicker layer is evaporated onto the gold-plated copper mounting blocks. The chip is placed on the block and heated until the solder melts. A final, gentle adjustment of chip position can then be made. No flux is used during this process (other processes required flux). Initial experience with this new technique has shown that when a chip is soldered onto a surface larger than the chip, the solder tends to swell when melted and flows under the chip. Thus, the chip must be pushed down gently or (probably better) thinner solder must be used on the block. When the chip is soldered onto a surface the same size as the chip (our case), this swelling effect only serves to fill in any fillet that may be present because of nonflatness of the block at the extreme edge.

C. DUAL-GATE PUSH-PULL STAGE

Two processing modifications have been planned for use in fabricating the dual-gate push-pull amplifier stage. The first is the use of e-beam alignment marks that are defined with the current spreading layer instead of with the source-drain layer. This requires forming the layer before e-beam gate definition.

A disadvantage of the procedure is that this level must be well aligned to the source-drain level. However, this is not especially difficult for power slices, which have a reasonably wide source-drain spacing. The advantage is that no nitride need be placed under the alignment marks, as is done in the conventional procedure. This saves a full step and will probably also result in better quality alignment marks since they are not subjected to alloy temperature.

The second modification is the fabrication of the inductors on top of the silicon nitride in the same step as the top capacitor plates. This will save one mask level. Any required crossovers at a nitride edge will be implemented using air-bridges.

SECTION III

PUSH-PULL AMPLIFIERS

A. TWO-STAGE PUSH-PULL AMPLIFIER

A new slice (79B2-24In) of push-pull devices (a single chip is shown in Figure 3) has been processed and rf-evaluated. Monolithic amplifiers from this slice have yielded the best cw performance yet seen for these devices. Figure 4 shows the gain compression curve for this amplifier. At full saturation, an output power of 1.38 W with 12.4 dB gain was obtained. The small signal gain is 16 dB with a 1 dB gain compression point of 1.27 W. Overall power added efficiency is 17 percent for the entire amplifier and 19 percent referred to the chip (i.e., taking into account 0.4 dB loss through each hybrid ring). Figure 5 is a cross section through this device, showing the good quality of the solder joint. Since the thickness of the GaAs chip is approximately 100 μm , it is seen from the photo that the solder joint is about 30 μm and contains no voids. (Compare this photo with Figure 16 in the second Annual Report for this contract, which shows the solder joint for a poorly mounted device.) As expected, the bandwidth performance was similar to that of the previous monolithic chips (see previous Annual Report), namely a 1 dB bandwidth of about 1.4 GHz centered at 9.0 GHz. Devices of this type and performance are expected to be used together with the paraphase amplifier chips for the development of multistage monolithic push-pull amplifiers capable of up to 1.5 W output power and driven from conventional unbalanced (i.e., not push-pull) sources.

B. PARAPHASE AMPLIFIER CHIP

Several design iterations both in the monolithic chip and test fixture were used to improve the evaluation accuracy and performance of the paraphase amplifier. The main difficulty in the test fixture was the maintenance of good ground continuity between fixture and the top ground metallization on the GaAs chip. The performance of the paraphase chip was dramatically improved by the incorporation of the new type of capacitor that essentially doubled the value of the bypass capacitors used in the paraphase chip design. Before this change, difficulty was encountered in realizing bypass capacitors with values greater than about 3 or 4 pF. With the adoption of the new capacitor design, capacitance values from 7 to 12 pF were realized. The latter values represent sufficient capacity for most bypass applications at X-band.

New rf performance results for the paraphase amplifier were obtained. Figure 6 shows small-signal results from 6.5 to 9.0 GHz. Figure 6c shows the test fixture used to obtain the gain and phase characteristics shown in Figure 6a and 6b. By mechanically switching from the right output to the left using bonding ribbon as shown on the output alumina circuit in Figure 6c, each output half could be measured individually. The other half is terminated with 50 ohms by a chip capacitor also located on the output alumina circuit. Figure 6a shows the gain characteristic from 6.5 to 9.0 GHz for the two outputs. It is seen that the gain tracks within ± 0.75 dB over this frequency range and is +3 dB at 8 GHz. Figure 6b shows that the phase tracking of the 180-degree characteristic is accurate to about ± 20 degrees over the same frequency range. These are the best results yet obtained for the paraphase chips in terms of output symmetry and bandwidth and are due primarily to the improved capacitor construction. Figure 7 shows the large-signal characteristics. Figure 7a shows the 180-degree hybrid ring used at the output to recombine the two antiphase signals. Figure 7b shows the large-signal gain and return loss. At an input level of 18 dBm, a 4 dB gain is achieved at 8 GHz, corresponding to an output power of about 160 mW. Figure 7c shows the detail of the chip/test fixture interface. Gold ribbon mesh is used to connect the top ground metallization to the chip carrier. Although these results are encouraging, further work is required to extend the mid-band frequency to 9.5 GHz, as was originally intended.

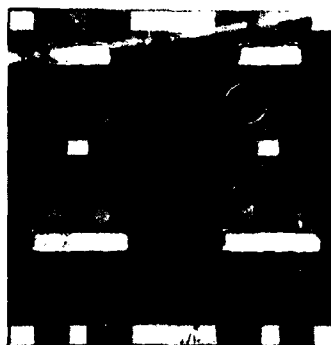


Figure 3. The Two-Stage Monolithic Push-Pull Power Amplifier Chip. Chip size: 2×2 mm

C. PUSH-PULL DUAL-GATE POWER FET

It is well known that at least under small signal conditions the dual-gate FET device provides higher gain than its single-gate counterpart. As much as 18 dB gain at 10 GHz has been achieved with dual-gate FETs, in contrast with 10- or 11-dB gain for single-gate devices.¹ Recent work at another laboratory has resulted in a discrete dual-gate power FET with a gate width of 1.6 mm, operating at 5 GHz. A power output of 1/3 W with 9.7 dB-gain has been achieved with this device.²

In a high gain monolithic amplifier, several stages of amplification may be required. Obviously, by increasing the gain of each stage, fewer stages are required and the size of the monolithic amplifier chip can be minimized. With this as a primary motivation, the development of a push-pull dual gate power FET has begun under the present program.

Initial work is involved with the design of a 2.4 mm gate width push-pull pair (each half is a 1.2 mm device) suitable for X-band operation. The performance goal for this device will be a power output of at least 1.2 W with 8 to 10 dB gain at 9.5 GHz. Monolithic fabrication techniques such as air-bridge interconnections and the use of overlay silicon nitride capacitors for second gate rf grounding are employed to minimize reactive parasitics. The air-bridges are necessary to interconnect the second gates as well as to interconnect the source pads. Since 150- μ m long gate channels are used, a total of eight channels needs to be paralleled and interconnected.

Figure 8 shows the initial chip layout for the pair of 1.2 mm dual-gate FETs. The chip size is 1.5×1.8 mm. The input impedance matching circuit is designed on the basis of the equivalent input circuit of a 1.2 mm single-gate FET. This equivalent circuit and the input impedance matching are shown in Figure 9 together with the Smith Chart plot of the resultant impedance locus. Only half of the push-pull circuit is shown; therefore, any shunt inductance in Figure 9 is doubled in value for implementation in the push-pull configuration and any shunt capacitance is halved. Simple 50-ohm microstrip lines are used for the output circuit. Since the output impedance of a dual-gate FET is significantly changed from its single-gate counterpart, the output matching will need to be incorporated after the first devices are characterized. It is believed that a simple shunt inductor followed by a series inductance could be implemented for the output impedance matching configuration. For initial evaluation, the 50 ohm output lines will aid in characterizing the device output impedance.

¹Charles A. Liechti, "Performance of Dual-Gate GaAs MESFET's as Gain Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Trans. Microwave Theory Tech.*, MTT-23, 461 (1975).

²J.L. Vorhaus, "GaAs Dual Gate Power FET," Seventh Biennial Conference on Active Microwave semiconductor Devices and Circuits, Cornell University, August 1979.

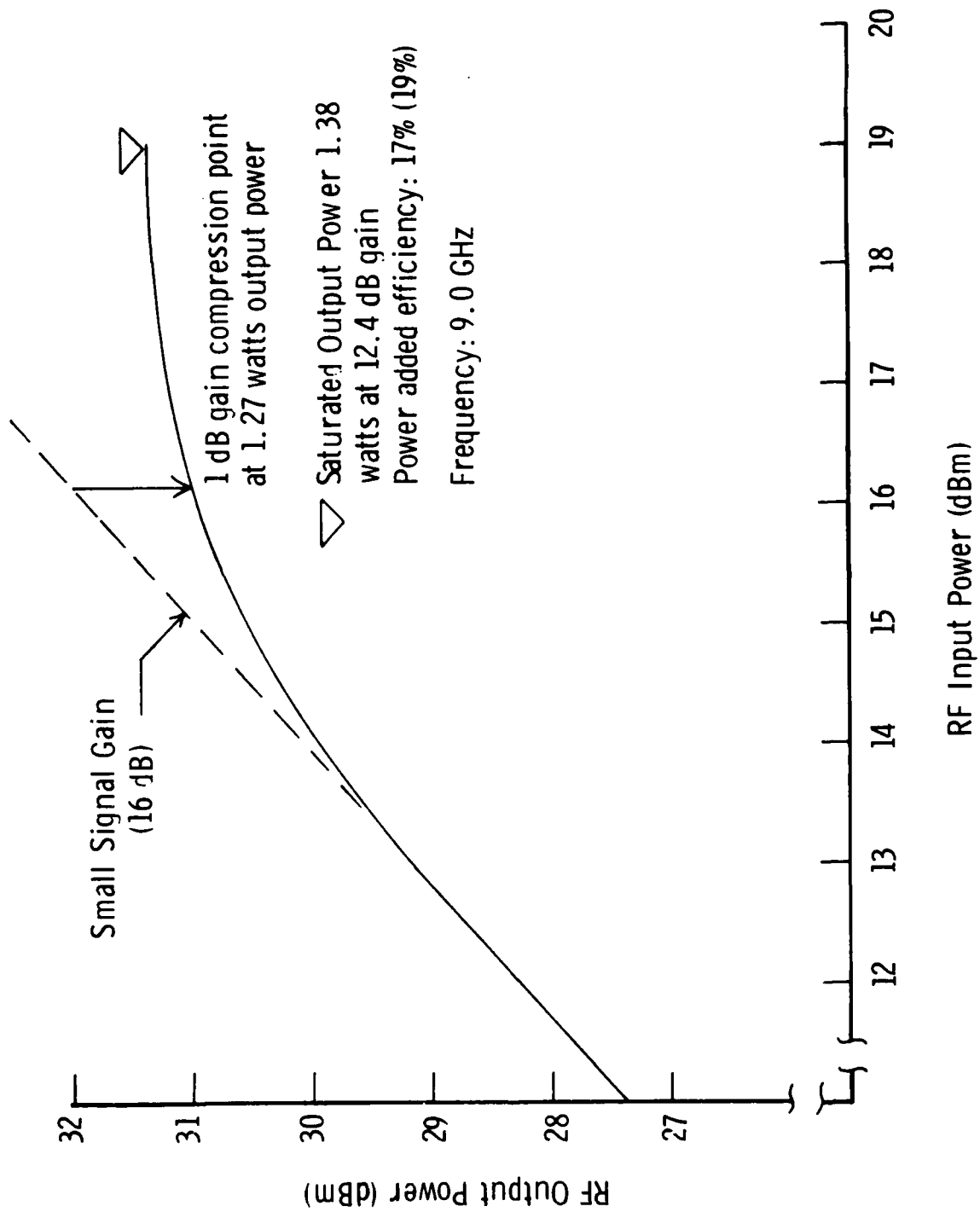


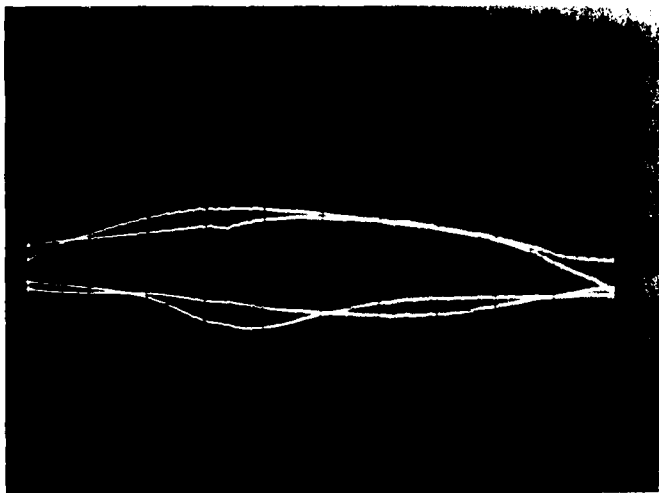
Figure 4 Gain Compression Characteristics for Monolithic Two-Stage Push-Pull Amplifier



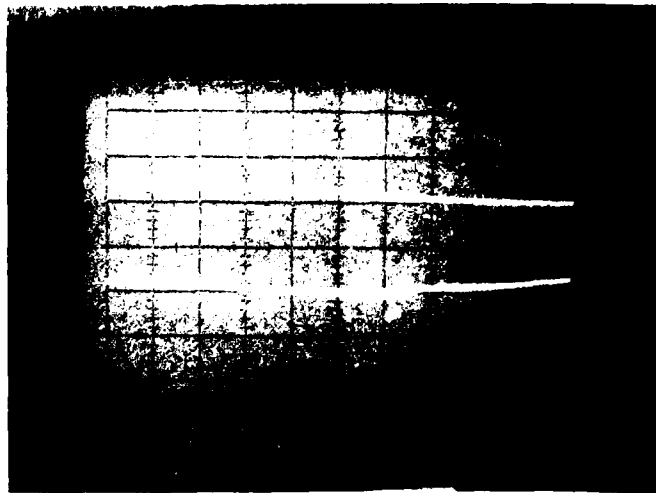
← 0.1 mm GaAs
← Solder Joint
← Copper Carrier

Figure 5. Cross Section of 1.4 W Monolithic Amplifier

Figure 10 shows the detail of a single dual-gate FET with 1.2 mm of total gate width. Air-bridges are used to interconnect the source pads and the drain pads. The second gate FET is shorted to ground by 10 pF bypass capacitors. These capacitors are of the silicon nitride overlay type and are located close to each device. The mask set is so designed that each dual-gate FET can be cleaved out of the slice for characterization purposes. Note that the actual mask design is slightly modified from the layouts shown in Figures 8 and 10. Nevertheless, the latter is representative and shows the salient features of the actual chip design. Presently, several slices of push-pull dual-gate devices are completing processing.

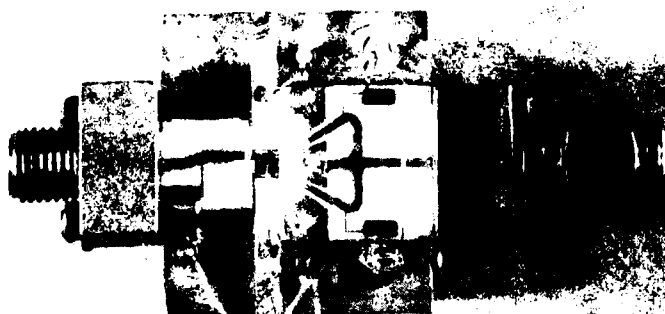


(a) Gain Characteristic
5 dB/div
Return Loss 10 dB/div



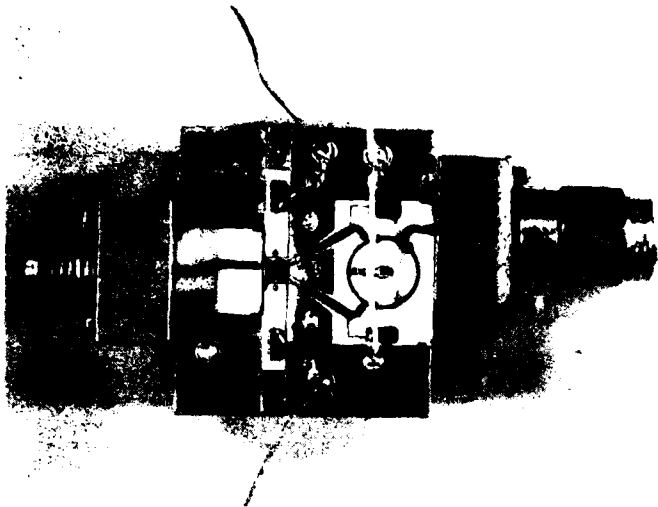
(b) Phase Characteristic
90 degree/div

Frequency 6.5 to 9 GHz
Paraphase Amplifier Results

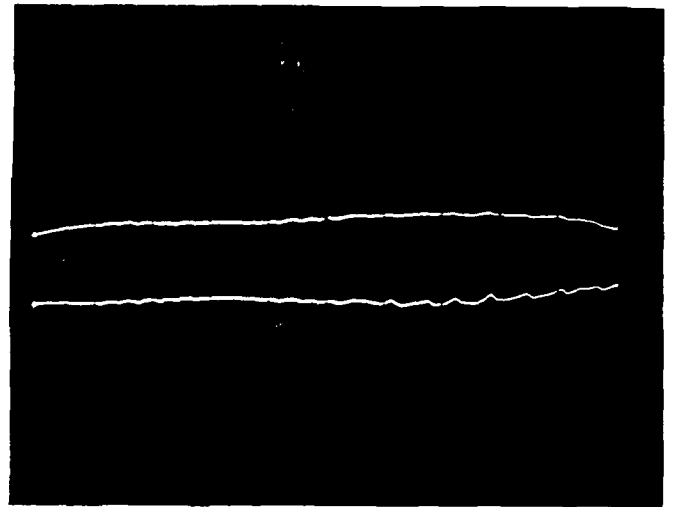


(c) Test Fixture

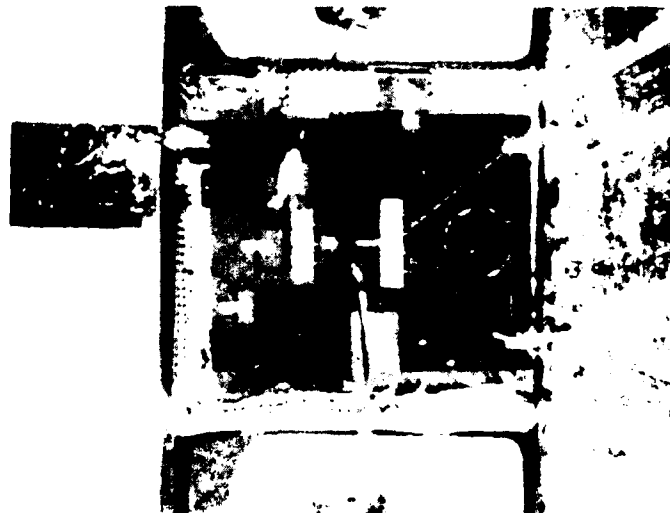
Figure 6 Small-Signal Characteristics for Paraphase Amplifier Chip



(a) Test Fixture



(b) Output Power, 5 dB/div
Return Loss, 10 dB/div
7 to 9 GHz



(c) Chip/Test Fixture
Detail

Figure 7 Large-Signal Characteristics for Paraphase Amplifier
Chip

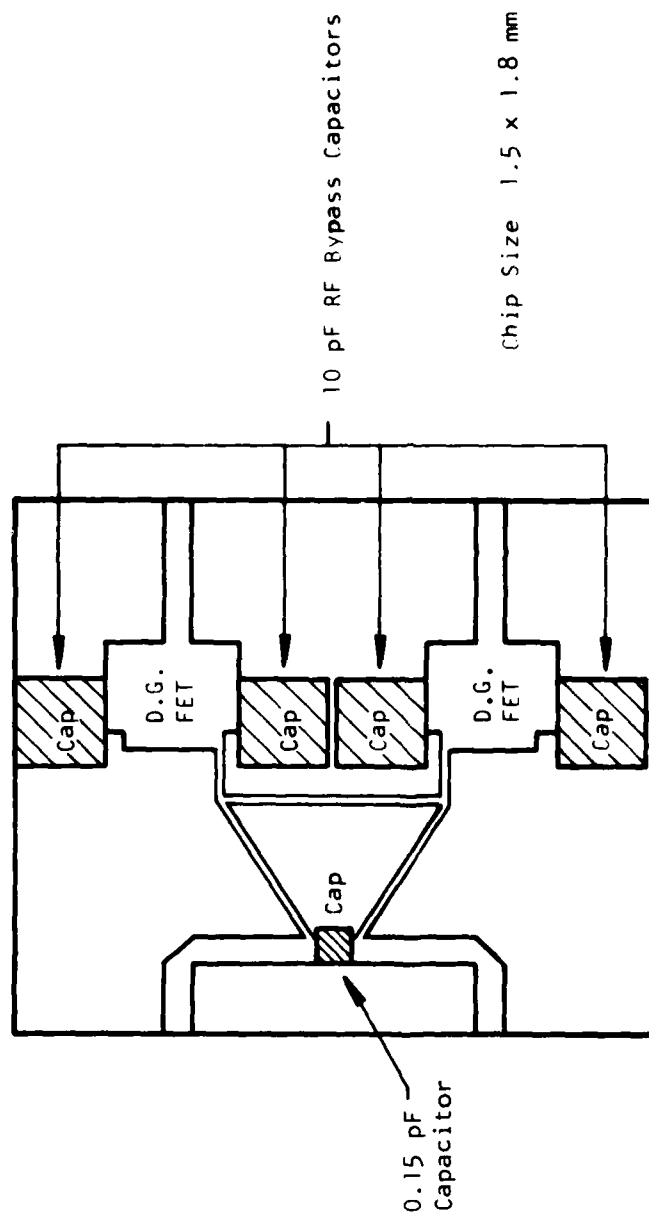
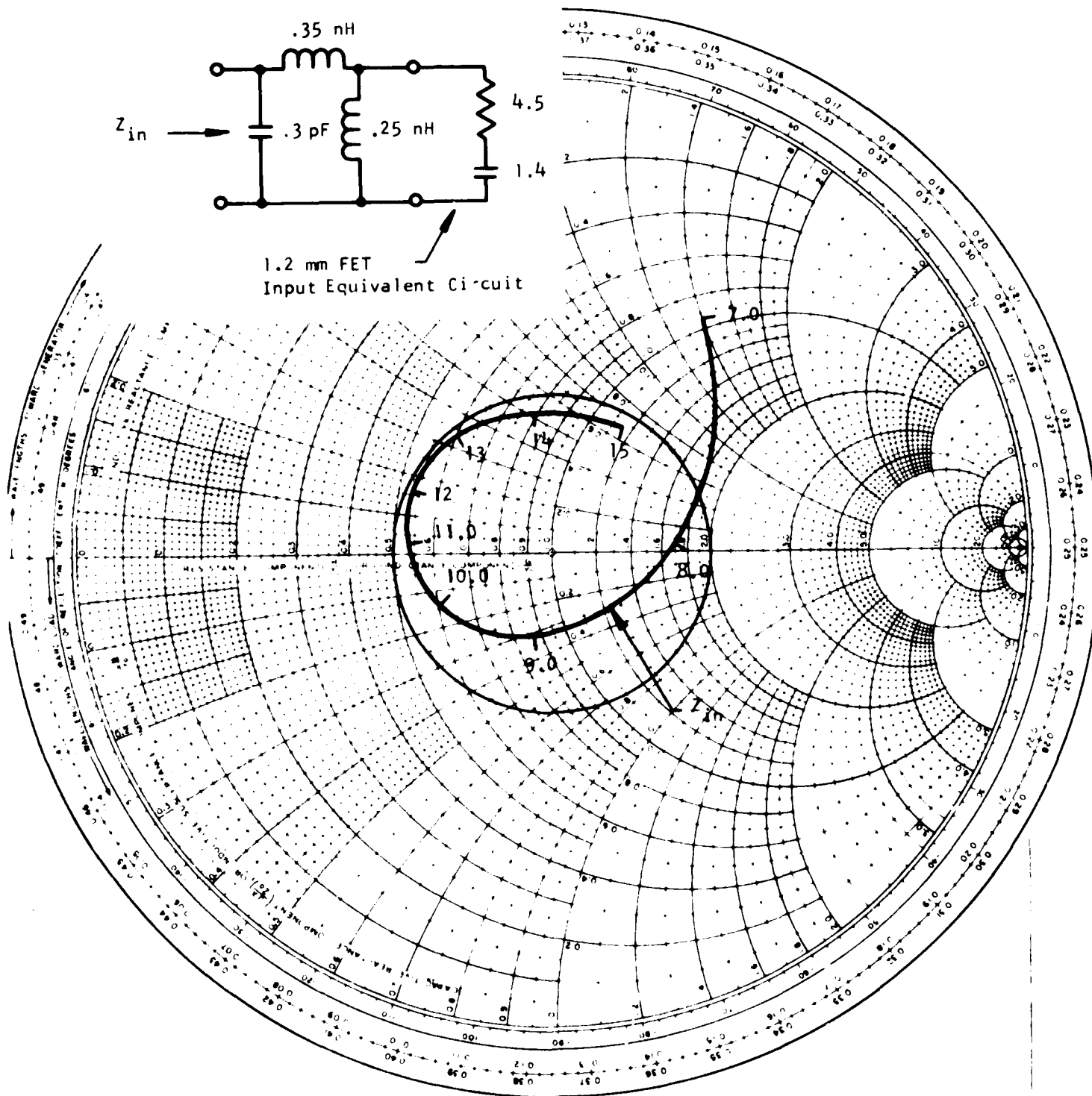
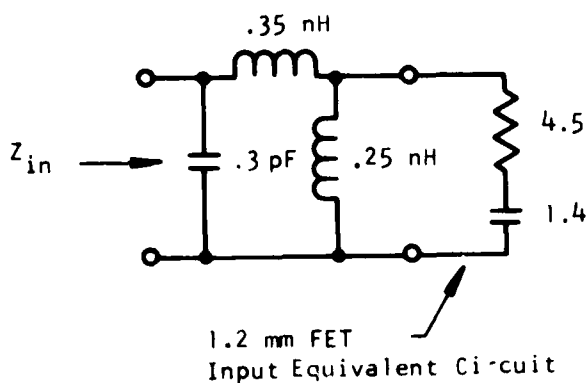


Figure 8 Initial Chip Layout for a Pair of 1.2 mm Dual-Gate FETs with Partial On-Chip Impedance Matching

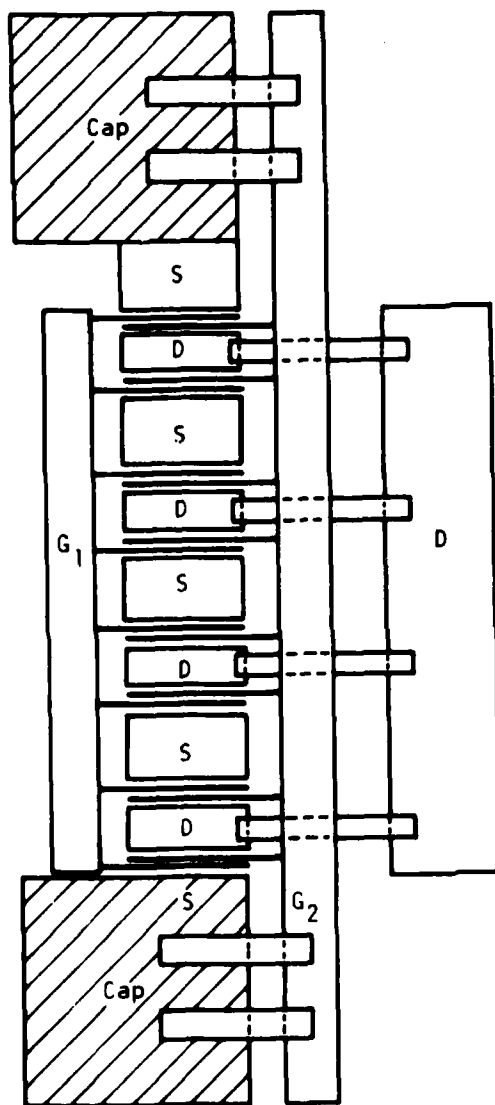
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SMITH CHART FORM 5301-7560-N	GENERAL RADIO COMPANY, WEST CONCORD, MASSACHUSETTS	DATE

IMPEDANCE OR ADMITTANCE COORDINATES



RADIALLY SCALED PARAMETERS

Figure 9 Equivalent Circuit for Dual-Gate Input Impedance Matching
(Based on Single-Gate 1.2 mm Gate Width FET)



Note: Air-bridge source interconnect is not shown for clarity

Figure 10 A Dual-Gate FET with Integral RF-Bypass Capacitors for RF-Shorting the Second Gate

SECTION IV

FULLY INTEGRATED PUSH-PULL (DISCRETE) DEVICES

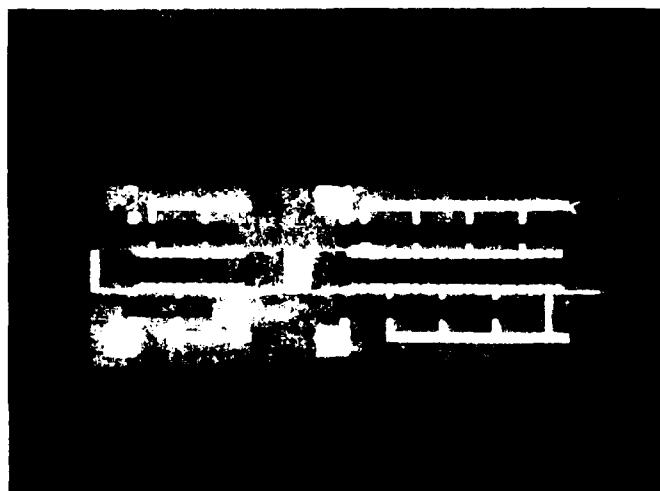
During this report year, the fully integrated push-pull (FIPP) devices (see second Annual Report) were designed, fabricated, and tested. These devices are made so that gate fingers on either side of each source pad operate 180 degrees out of phase (push-pull). Thus, rf currents need not flow to true ground, but only to the virtual ground between the gate fingers. Source impedance is therefore minimized. Each device has two input gate pads and two output drain pads. Air-bridges interconnect the gates of each phase and interconnect the sources (for dc bias only). Photographs of the completed devices are shown in Figure 11. The figure shows two chips, one containing a 4,800 μm device, the other containing a 1,200 and a 2,400 μm device. These are scribed apart manually for testing. (Manual scribing can be done easily using a blade and a low power microscope.) Because of the maximum size of an e-beam field (assuming $>0.5\text{-}\mu\text{m}$ placement accuracy), the size of the 4,800 μm device, and the desire to include a test bar, placement of the 2,400 and 1,200 μm devices on the same chip was necessary to allow fabrication of devices of all three sizes using the same mask set.

Initially, several 1,200- μm discrete push-pull devices and one 2,400- μm device were tested using 180-degree hybrid rings. These devices were from the first completed slice. Since these devices do not incorporate on-chip impedance matching, external matching on the hybrid rings was used. Figure 12a shows the small signal gain versus frequency for the 1.2 mm FIPP device. Input and output matching circuits are identical to those used on the first stage of the monolithic two-stage push-pull amplifier developed earlier under this contract. As seen in Figure 12a, a small signal gain of 8.5 dB (including circuit losses about 0.8 dB) is achieved at 9.5 GHz. Note that the bandwidth includes the inherent bandwidth of the 180-degree hybrid rings (approximately 8.8 to 11.2 GHz). For large signal operation, an output power of 0.5 W with 7.2 dB gain was measured for several 1,200- μm devices. Slightly higher power (28 dBm) occurs at lower gain.

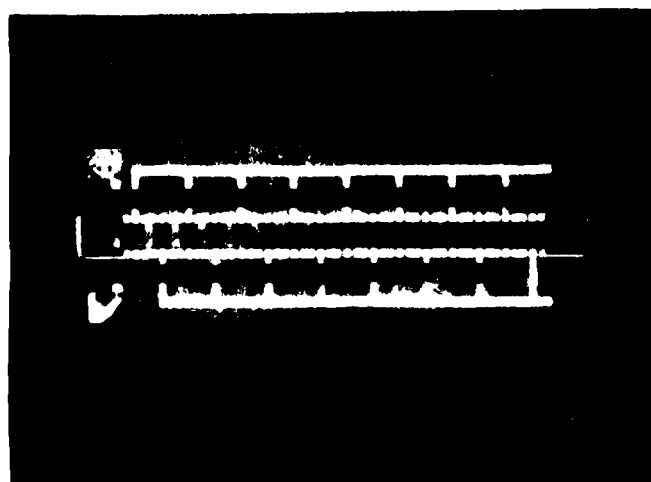
Figure 12b shows the small signal gain of the first 2.4 mm FIPP FET device tested. Again, external impedance matching with a shunt chip capacitor was used. These preliminary tests used a narrowband matching scheme for convenience. At 9.5 GHz, a small signal gain of 6.5 dB is observed. The large signal output power of this first 2.4 mm FIPP FET was 0.5 W.

Devices from a subsequent slice were examined. Below full saturation, these 1,200 μm FIPP devices have exhibited gain and power performance approximately equal to discrete devices from the best slices. Since many slices of discrete devices have been evaluated, these initial results from only three FIPP slices are encouraging. Small signal gains as high as 13.7 dB have been observed for the 1,200 μm devices. A typical gain compression characteristic is presented in Figure 13.

However, performance of the 2,400- μm devices was discouraging. Although this device should have produced nearly 3 dB more output power than the 1,200 μm device (at twice the input power), its performance was only 1.3 dB higher. The reason for this degraded performance is most likely due to unequal phasing of the individual transistor cells. This is due to the length of the device and the finite propagation time required for the input and output signals to travel along the gate and drain buses (electrical length of device is about 45 degrees based on a microstrip line on GaAs). This phasing problem results in poorer cell combining efficiency. Although the orientation of the device with respect to the input and output circuits was chosen to be at right angles to the conventional FET layout (to minimize the number of crossovers), changes in the present layout and orientation of the FIPP FET that reflect an improved

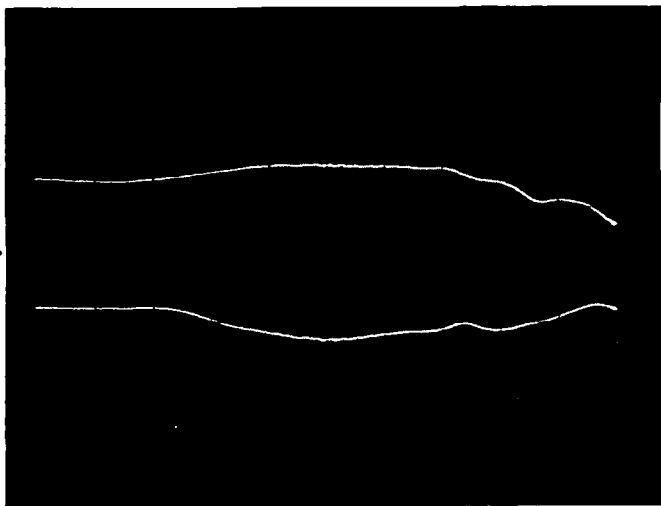


(a) A 1200 μm and a
2400 μm device

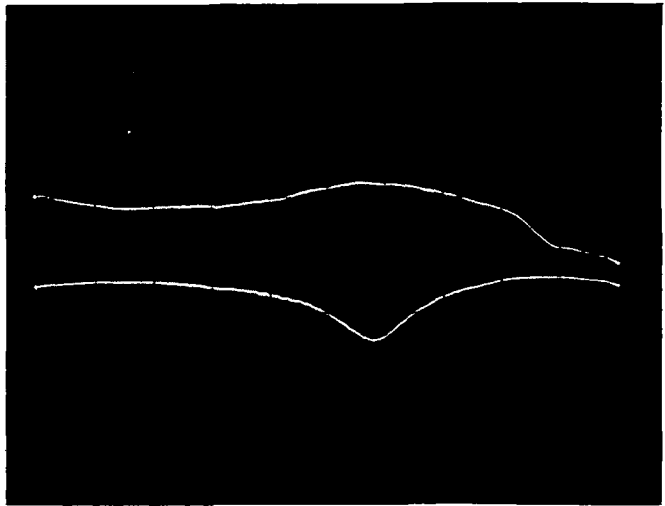


(b) a 4800 μm device

Figure 1. Push-Pull FETs.
Same size (both photos)
magnified 1250x.



(a) 1.2 mm Gate Width



(b) 2.4 mm Gate Width

Vertical: Top Trace (Gain): 5 dB/div
 Lower Trace (Return Loss): 10 dB/div
 Horizontal: 250 MHz/div - Range 8 to 10.5 GHz
 Reference: Center Graticule Line, both Traces

Figure 12 Small Signal Gain vs Frequency for Fully Integrated Push-Pull Amplifiers

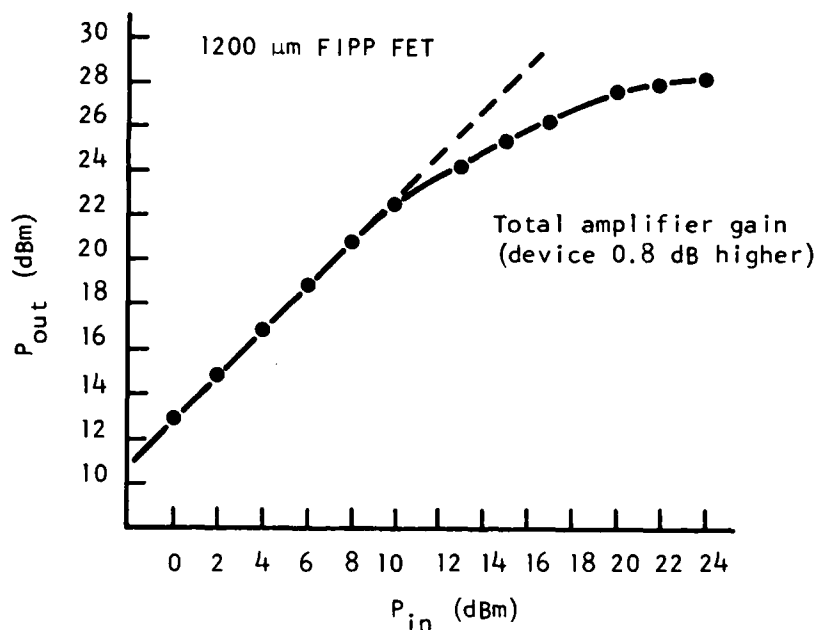


Figure 13 9 GHz Performance of a FIPP Device. The hybrid rings of the test circuit are included in this data.

"feed" symmetry for the input and output signals may improve the combining efficiency. Such design changes are under consideration.

Because of the encouraging results obtained on the smaller 1,200 μm gate width FIPP FETs at least in terms of small signal gain, work will continue to improve its performance and to extend the potential advantages of the FIPP approach to larger gate width FETs.

SECTION V

PLANS FOR FUTURE WORK

The work to be continued under this program is aimed at achieving an X-band monolithic 5 W amplifier, with a gain of at least 20 dB. Some of the building blocks for this amplifier have been identified and are being developed, while others are in the initial design stages. A block diagram of the proposed amplifier configuration is shown in Figure 14. The amplifier consists of three basic parts: the paraphase amplifier, a high gain push-pull dual-gate driver amplifier, and a final push-pull power output stage that has a total gate width of 9.6 mm. Work on the paraphase and dual-gate driver amplifiers is continuing under the present program. Plans have been formulated for development of the power output stage. The following subsections summarize the basic activities to be pursued for the development of the 5 W amplifier.

A. ANALYSIS AND REFINEMENT OF PARAPHASE AMPLIFIER

The feasibility of the monolithic paraphase amplifier has been successfully demonstrated. However, additional improvement in performance is necessary. Further theoretical analysis and possibly device mask redesign will be required to fully optimize the paraphase amplifier. Fabrication, testing, and characterization of these monolithic paraphase amplifiers will provide the necessary data base for interfacing this circuit with the other active components of the final 5 W monolithic amplifier.

B. DEVELOPMENT AND EVALUATION OF THE DUAL-GATE PUSH-PULL DRIVER AMPLIFIER

The dual-gate power amplifier is under development. Its potential advantage is to provide higher gain than a conventional single-gate amplifier having comparable gate width. The design plan is to fabricate a pair of dual-gate, 1.2 mm gate width FETs on a single chip, including on-chip impedance matching. Provision is made for cleaving out the dual-gate devices for individual characterization without the complication of the on-chip matching networks. After fabrication and evaluation of this first chip design, a second design iteration and device mask set will be used to optimize the dual-gate driver amplifier for integration into the final 5 W monolithic amplifier.

Note that if the dual-gate push-pull driver amplifier does not prove more advantageous than a conventional push-pull pair, the latter will be implemented into the design of the final 5 W monolithic amplifier. As shown in Figure 14, a 10 dB gain 1 W amplifier is required for the driver stage. This amplifier can be realized with an optimized design of the original two-stage, push-pull amplifier developed for this program. The two-stage single-gate push-pull amplifier yields a minimum 10 dB gain at the 1 W power output level.

C. DEVELOPMENT AND OPTIMIZATION OF THE HIGH-POWER, 5-W, SINGLE-STAGE AMPLIFIER

From discrete device experience, it is known that a pair of 4.8 mm gate width FETs operated in the push-pull mode will be required to obtain the 5 W power output goal. To take advantage of interstage matching, the input impedance to the 5 W power stage will be designed to conjugately impedance-match the output impedance of the driver amplifier (<50 ohms). The advantage to this approach is that less impedance transformation is required in the interstage networks and, consequently, lower loss occurs. This

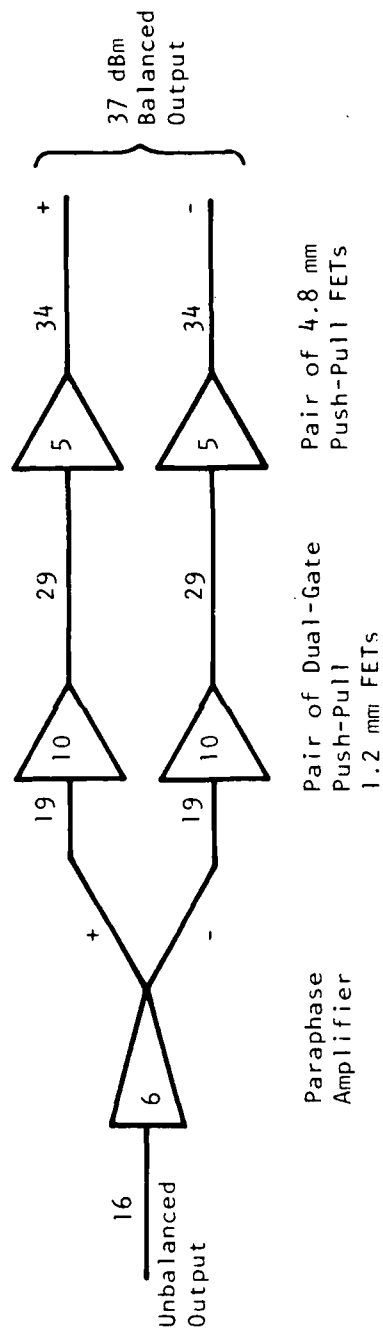


Figure 14 Preliminary Design for 5 W Monolithic Amplifier.
(Numbers outside triangles are in dBm; numbers inside triangles are in dB).

is an important consideration in a monolithic circuit, since it is generally more difficult to realize low-loss, monolithically fabricated, passive components than it is to realize the corresponding components using conventional MIC technology. The disadvantage is that testing of the individual amplifiers must be done using appropriate transformers that interface the amplifier under test with a conventional 50-ohm system. Figure 15 shows a possible layout for this monolithic chip. Lumped element impedance matching is used to conserve GaAs chip area. A two-section matching network will most likely be used to increase bandwidth. Chip dimensions of about 3 mm $\times$ 2 mm are required for the power output stage.

D. INTEGRATION OF ALL AMPLIFIERS ON ONE CHIP

A final mask design must be generated and the devices fabricated for the 5 W monolithic amplifier. This chip will incorporate the paraphase, the driver, and the power amplifiers as shown in the block diagram of Figure 14. To test the monolithic amplifier chips, an output passive balun will be used.

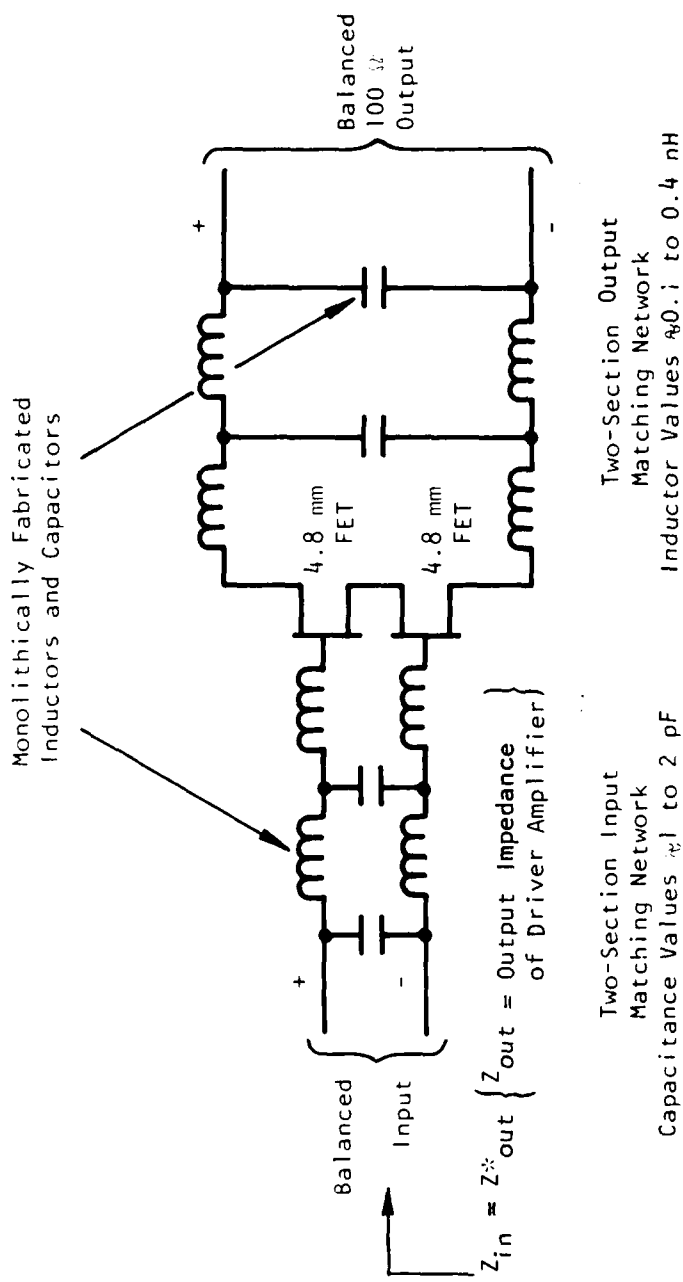


Figure 15 Possible Configuration for a Monolithic 5 W, Single-Stage Push-Pull Amplifier with On-Chip Impedance Matching

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