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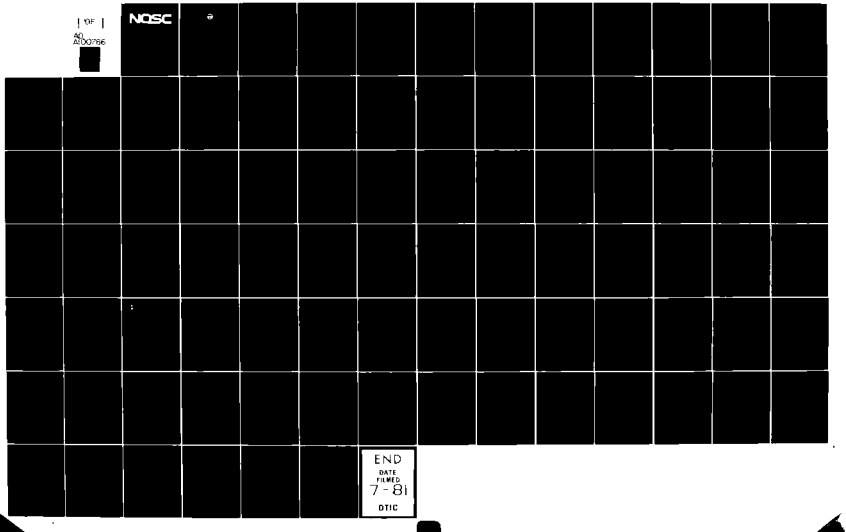

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FIBER OPTIC DATA BUS FOR MARINE CORPS COMMAND-CONTROL SYSTEMS

A. Schaefer, D. Butts and J. Wildermuth

February 1981

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A five-terminal data bus operating at 1 Mbps was built, tested and evaluated using state-of-the-art fiber optic components. The data bus utilized a modified MIL-STD-1553B protocol and was operated with a central controller and also a distributed bus control algorithm. Problems associated with the USMC Command-Control data bus were identified.

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SUMMARY

OBJECTIVE

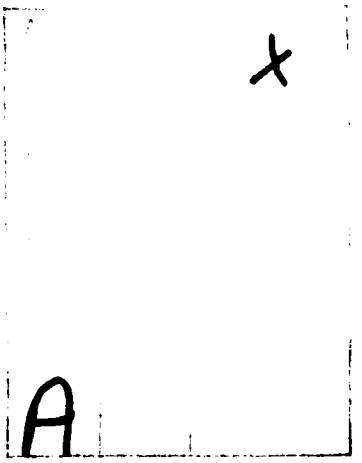
To verify the fiber optic data bus design identified in the FY78 system analysis and feasibility study by building and demonstrating operation in the laboratory. In addition, to identify problems and reduce the risk associated with the development of a tactical USMC Command-Control data bus.

RESULTS

A five-terminal data bus operating at 1 Mbps was built, tested and evaluated using state-of-the-art fiber optic components. The data bus utilized a passive 16- by 16-port transmissive star coupler to interconnect typical equipments used in a tactical shelter system. The bus system was operated with a central controller and also with a distributed bus control algorithm.

RECOMMENDATIONS

The requirements developed herein for fiber optic components should be included in the objectives of pertinent manufacturing technology programs. A fail-safe active fiber optic T-coupler which will allow multidrop bus architectures to be extended beyond present technology limitations should be developed. The data rate of the bus should be increased to 20 Mbps. Further development of distributed control algorithms should be pursued using the data bus test bed. The interconnection of buses, as in multiple shelter applications, with active repeaters should be developed and demonstrated.



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I. INTRODUCTION

The effort described in this report was carried out under the USMC Command-Control Technology Direct Development Funding Program (Task Area Plan No. ZF21.203.080). The objective was to construct and evaluate a fiber optic data bus in the laboratory based upon the conclusions reached in NOSC Technical Report 342, Marine Corps Command and Control Fiber Optic Data Bus Feasibility Study.* This data bus represents an optimum design determined by typical Marine Integrated Fire and Air Support System (MIFASS) requirements, existing data bus architectures and protocols, and state-of-the-art fiber optic components. The MIFASS requirements were selected as typical for post-1980 USMC Command-Control data bus requirements.

II. BACKGROUND

Military data bus technology has been developed to fulfill platform operational requirements for increased maneuverability, survivability, reliability, and maintainability. The data bus utilizes a common transmission path for signal transfer within an electronic system. The application of fiber optics to the data bus offers significant advantages over systems utilizing metallic conductors. The fiber optic transmission medium neither causes nor picks up EMI or RFI, has high bandwidth, excellent isolation, light weight, small volume, and low transmission loss. This project seeks to exploit fiber optics technology for the benefit of the USMC Command-Control System.

III. APPROACH

A system analysis to develop an optimum system design based on typical requirements, existing data bus architectures and protocols, and state-of-the-art fiber optic components was performed in FY78 and is described in NOSC Technical Report 342. During FY79 the fiber optic component requirements for the data bus system were identified,aand procurement or in-house fabrication of these components was begun. In FY80 a fiber optic data bus test bed was established which permitted equipments to be interconnected in a representative Marine Corps Command-Control configuration. Evaluation of alternative fiber optic components was accomplished together with data bus system testing. A five-terminal fiber optic data bus was demonstrated.

IV. DATA BUS DESCRIPTION

The fiber optic "data bus system" is a collection of functional elements including fiber optic cables, couplers, connectors, transmitters, and receivers associated together to provide for the distribution of information between or among components of a larger system. The data bus system includes everything between access ports, which provide for the connection of the external equipments to the data bus. The interface provided at these access ports is directly compatible with the associated equipments.

* Marine Corps Command and Control Fiber Optic Data Bus Feasibility Study, NOSC TR 342, 1 November 1978, by A Schaefer.

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The "data bus" refers exclusively to the medium shared by the users which is used to spatially distribute signals within the data bus system. The data bus serves only to provide a path for the signals and does not change their nature, as by nonlinear processing.

The bus terminal units are the devices which act as interfaces between the data bus and the access ports to the bus. These units provide for all functions required to effect information transfer via the bus, such as encoding, formatting, timing, synchronization, and modulation/demodulation of a carrier appropriate to the data bus medium. Included in the bus terminal units for the fiber optic data bus system are the fiber optic transmitter and receiver and the bus interface unit (BIU). The fiber optic transmitter and receiver convert between electrical and optical signals. The bus interface unit performs the queuing functions necessary to allow information to be passed on the bus serially, that is, from one terminal unit at a time to one or more receiving terminals.

A generalized block diagram for a fiber optic data bus appears in figure 1. This illustration is an example of a system employing a transmissive star coupler for signal distribution and a central bus controller. Other configurations are possible.

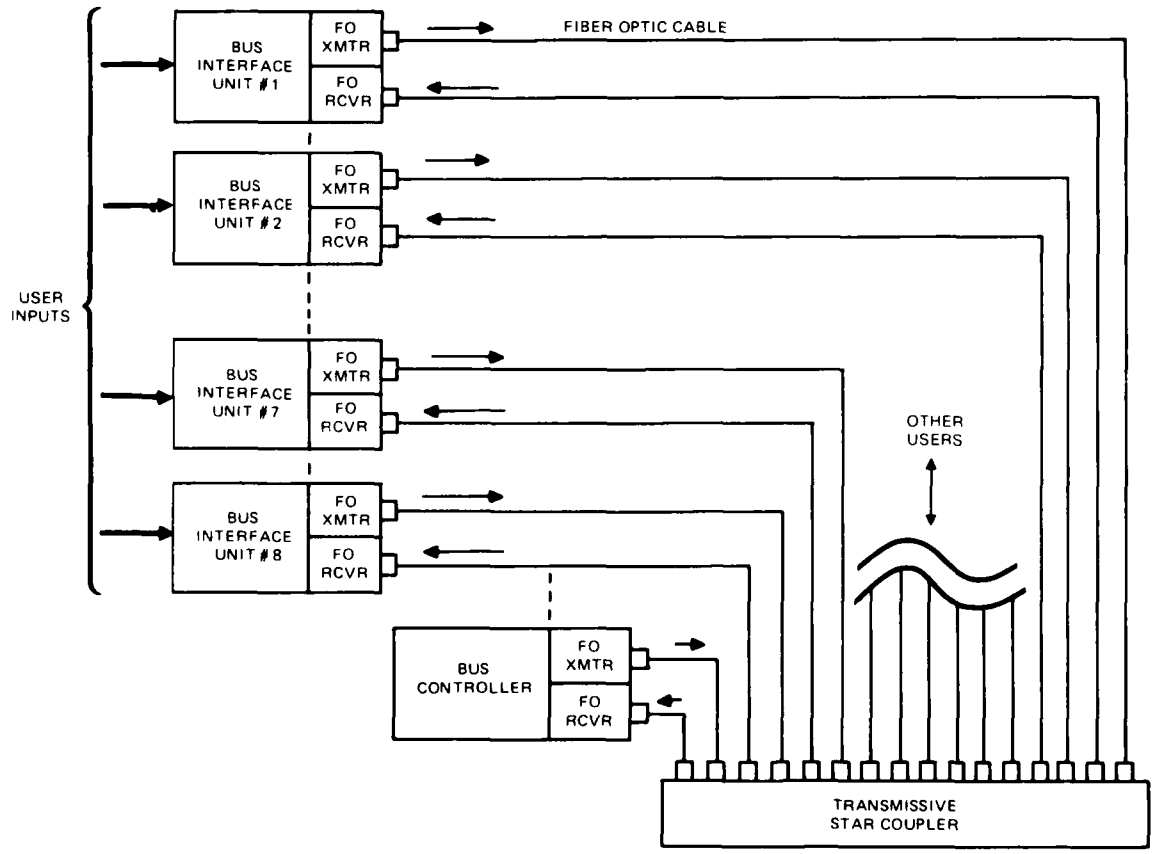


Figure 1. Generalized block diagram for a fiber optic data bus.

A block diagram for the Marine Corps Command Control data bus discussed in this report can be found in figure 2. The requirements for this data bus were derived from the MIFASS requirements which are considered typical for the post 1980 era. A summary of these requirements follows:

1. Interconnect a maximum of 256 terminals within a command post; 32 terminals within a single shelter.

2. Accommodate user data rates up to 32 kbps.

3. Composite bus data rate of 10 Mbps.

4. Low error rates terminal to terminal.

5. Fail-safe bus control.

The data bus discussed herein has demonstrated the following characteristics:

1. Five terminals interconnected, with 16 terminal connections possible.

2. Accommodates user data rates of 110 bps, 4800 bps, and 1 Mbps.

3. Composite bus data rate of 1 Mbps.

4. Terminal-to-terminal bit error rates of a few bit errors in 10^9 bits transmitted.

5. Microprocessor bus interface unit utilizing a MIL-STD-1553B protocol with a central controller and with a fail-safe distributed controller.

V. COMPONENT TECHNOLOGY

A. GENERAL

This discussion of the data bus system is divided into five component areas: fiber cable, fiber optic connectors, multiple-access couplers, fiber optic transmitters/receivers and bus interface units.

The fiber cable used for interconnections was chosen to match the fiber used to construct the coupler. The development of fiber cable is leading the development of other fiber optic components and is considered to be a very low-risk item.

The fiber optic connector is considered to be a high-risk component. A large number of manufacturers are engaged in production of fiber optic connectors. Expensive and/or extensive tooling and elaborate termination procedures are factors which make field termination impractical for some connectors and affected the choice of connectors for evaluation. The connector types used on each of the two star couplers were evaluated. The results are discussed in detail in Section V.C.

The most critical component was the transmissive star coupler. Only a few manufacturers could be identified that had produced developmental star couplers. This program was limited to the purchase of only two couplers for evaluation because of their high cost. A number of star couplers procured under other programs were also available. Star coupler technology is discussed in detail in Section V.D.

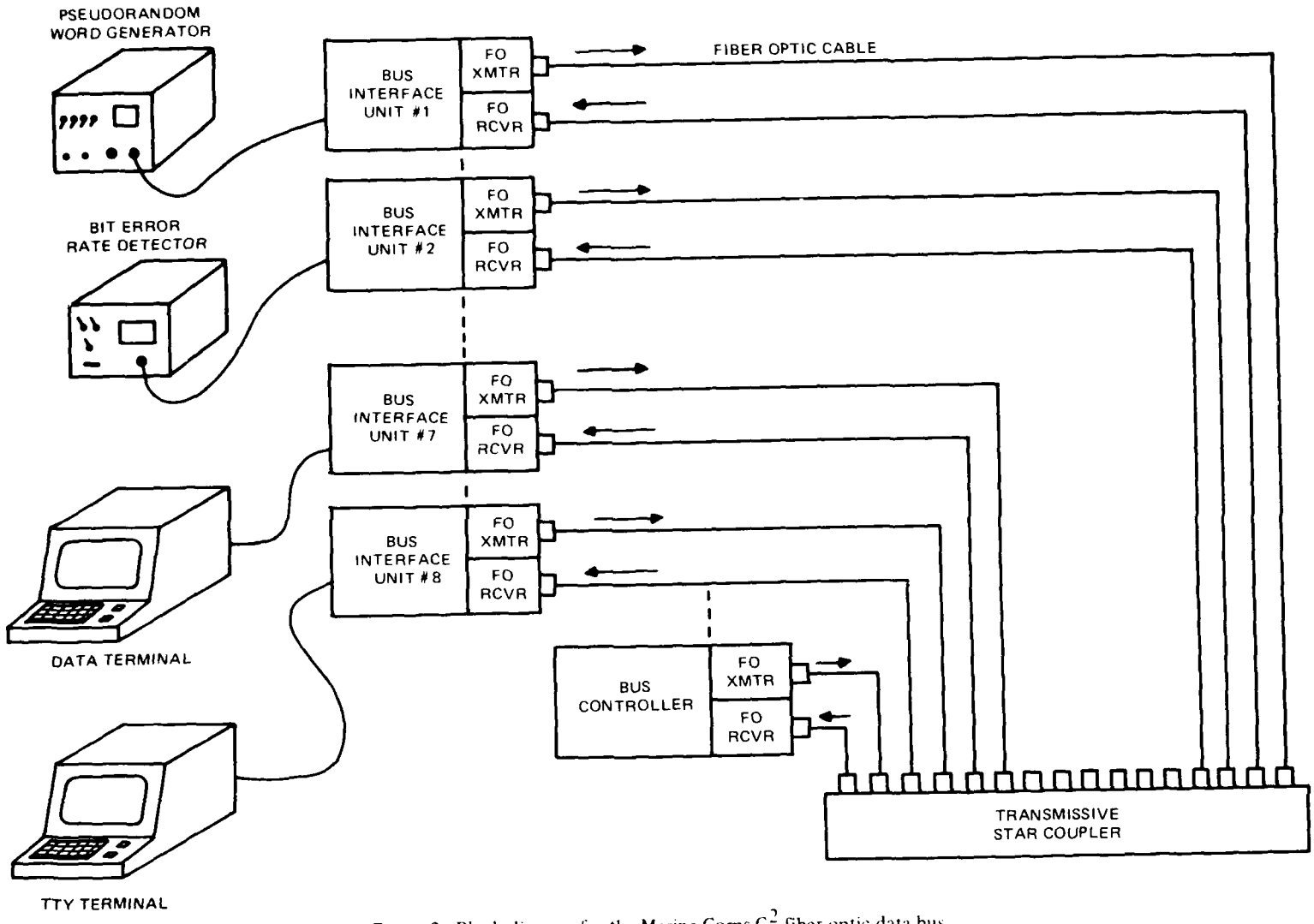


Figure 2. Block diagram for the Marine Corps C^2 fiber optic data bus.

The requirements, as determined by the system analysis, for fiber optic transmitters/receivers for use in the bus system were compared with advertised specifications for commercially available units. A satisfactory correlation was not obtained, so in-house design and fabrication of these units was undertaken. The results of this effort are discussed in detail in Section V.E.

In order to dynamically test the fiber optic data bus, a bus controller and a number of bus interface units (BIU) were required. An Intel SDK-86 microcomputer was selected to perform both functions. This selection was based on availability, applicability, and familiarity with Intel programming and debugging. The Intel microcomputer was programmed to provide a distributed control protocol for the data bus. The distributed control bus modification was accomplished by reprogramming the microcomputer PROMs. A complete description of the BIU is given in Section V.F.

B. FIBER OPTIC CABLE

1. General

The Marine Corps Command and Control Shelter data bus application requires a cable that is based on single-fiber technology, that is lightweight, small, strong, flexible and that has low optical transmission loss. These requirements were established in the data bus feasibility study.

2. Essential Characteristics

a. Attenuation. The attenuation characteristics of graded-index fibers are usually specified between 600 and 1300 nm. The attenuation-versus-wavelength curve contains several local minima which can be exploited when choosing the operating wavelengths of light-emitting diodes and photodiodes for fiber optic systems. The system analysis established the feasibility of a data bus system using fibers with an attenuation of 20 dB/km. The state of the art is well under 10 dB/km between 800 and 900 nm. The short lengths required assure minimum risk for this fiber cable characteristic.

b. Strength. The MIFASS specification requires that the non-shelterized command center cable not sustain any damage as a consequence of being tread upon by a 250-lb person wearing combat boots. Cable manufacturers are applying the technology of high-strength ruggedized wire cable to fiber optic cable. High-strength fiber cable can be made with a nonmetallic strength member so that it is entirely nonmetallic.

The strength requirements are less stringent where the data bus is inside a rigid shelter, with the result that an internal strength member may not be required. A very small, lightweight cable can be used for the in-shelter application.

c. **Temperature.** The MIFASS temperature requirements are:

Operating	-28°C to +65°C
Non-operating	-62°C to +71°C

Cables whose performance exceeds these temperature specifications are available from a number of manufacturers, including Times Wire and Cable and Galileo. These cables are fabricated from glass-clad fibers. Transmission loss of currently available plastic-clad fibers increases at very low temperatures. The choice of cable, however, should not be based solely on the current situation, since fiber technology is changing rapidly. Our knowledge of fiber characteristics is continually growing and being revised. The effects of temperature on fiber performance is an example. There is relatively little information available in this area. Continued evaluation of fiber performance is recommended to determine suitability for this application.

d. **Radiation Hardening.** Optical communication systems for military applications will be required to withstand exposure to nuclear environments. The MIFASS specification contains nuclear environment requirements. Optical losses several orders of magnitude greater than the intrinsic fiber loss can be induced by relatively low levels of radiation. Induced optical attenuation due to radiation varies greatly as a function of fiber type, manufacturer, dose rate, total dose, temperatures, etc. Some plastic-clad silica fibers recover fully in 10 μs to 1 min after a moderate radiation dose. All-glass fibers vary in their total absorption and recovery time depending on their precise chemical composition. Much work has been done in this area by E. J. Friebele et al of the Naval Research Laboratory and is described in the November-December 1979 issue of *Optical Engineering*. There is no quick answer as to which fiber is best for deployment in a nuclear environment. In choosing a fiber, it is necessary to completely specify the nuclear environment and the operating conditions that the fiber will encounter.

3. Summary

A cable that meets the attenuation, strength, and temperature requirements is available. No specific advantageous differences were observed between a 100- and a 200-μm-core-diameter fiber. Additional development is necessary in the area of cable standardization, temperature range of PCS fiber, and radiation hardening.

C. FIBER OPTIC CONNECTORS

The lack of suitable single-fiber optical connectors is the major roadblock to widespread military use of single-fiber systems.

1. Essential Characteristics

The essential characteristics which must be considered in selection of a fiber optic connector are discussed below.

a. Connector Insertion Loss. The connector insertion loss is the relative optical power loss, expressed in decibels, due to the introduction of a mated connector pair in series with a fiber optic cable. Factors influencing insertion loss include lateral and angular misalignment of the fiber core, fiber-to-fiber end separation, and Fresnel reflection losses.

b. Repeatability. The connector repeatability is the variation of connector insertion loss over a number of mating/unmating/mating cycles. Most fiber optic connector manufacturers do not specify this parameter. A 0.5-dB variation is considered very good for today's technology.

c. Alignment Methods. Fiber alignment consists of two steps. The first step is to mechanically secure the fiber end within the connector and to prepare the face of the fiber so that it is optically flat. The quality of this step is a function of the connector design and the skill of the technician doing the assembly. The second step is the alignment of the fiber ends within the mated connector. The quality of this step is primarily a function of the design. A common realization of these processes is by means of metal ferrules attached to the fiber ends and a precision bore adapter for alignment. One connector which was evaluated used a watch jewel to center the fiber within a ferrule and a precision bore adapter to align the mating fiber ferrules. The second connector evaluated used four steel pins to center the fiber accurately in the ferrule and a plastic alignment sleeve to align the ferrules.

d. Field Installation. Some fiber optic connectors must be factory installed. Other connectors can be field installed but require special tools. In terminating a fiber cable, the end of the fiber must be cleaved or polished. Polishing usually reduces connector loss but may not be convenient to do in the field. The fiber optic connector required for the Marine Corps data bus application must be capable of being installed in the field without bulky tooling and must exhibit a low repeatable insertion loss.

e. Single- vs Multi-Channel Connectors. The majority of fiber optic connectors being manufactured are of the single-channel type. The connectors evaluated were of the single-channel type, but the design concepts have been applied to multi-channel connectors. The data bus requirements for system setup time and march-order time dictate use of multi-channel connectors. The optimum configuration for data bus applications requires dual-channel connectors at the transmitter/receiver end of the cable and 16- or 32-pin connectors at the star coupler. Some connector manufacturers are producing multi-channel connectors, and some star couplers have been fabricated using multi-channel connectors.

2. Test Description

a. Connectors Tested. Two fiber optic connectors were evaluated. The Amphenol 906 series (Pt. No. 906-113-5000) is the connector utilized by the Olektron Corp. on their star coupler. The ITT Cannon FOT series connector was utilized by ITT E/O Products Division on their star coupler. Test cables with mating connectors were fabricated to test each coupler and to interconnect the data bus system. These cables provided a vehicle for evaluating the fiber optic connectors. Ten cables were terminated with Amphenol connectors at each end and three cables were terminated with the ITT Cannon connectors. Interchanging and reversing the cable ends allowed a satisfactory number of samples of connector data to be obtained. The connectors were tested for insertion loss, repeatability, and rotational variation.

b. Test Setup. An optical multimeter, Photodyne Model 22XL, was used to measure optical power. This instrument indicates directly in dBm or dBu. A reference reading was taken with the optical transmitter connected directly to the optical multimeter via two short test cables. The second test cable was inserted in the link in order to strip the cladding radiant power. A second reading was taken with three test cables in series between the optical transmitter and the optical multimeter. The reference reading was subtracted from the second reading. The result is the insertion loss of one connector plus the loss in a short piece of fiber, which is negligible. The connectors were subjected to a repeatability test by mating and unmating five times and recording the insertion loss. Neither connector tested is keyed, and the insertion loss may vary slightly with rotation. The connectors were rotated ±180 deg, and the insertion loss variations were recorded.

3. Test Results

The optical fiber used in the test cables should be identical to the fiber used internal to the star coupler. The Olektron star coupler utilized Galite 3000-LC fiber, which is a large-diameter glass-core/glass-clad fiber (200 μm core diameter, 245 μm clad diameter). The Galite fiber was too fragile to use as a test cable, so Valtec DC-PC08-02 cable, a plastic-clad 200-μm-diameter silica fiber, was substituted. An Amphenol connector was required to mate with those on the Olektron coupler, but a type specifically intended for the Valtec cable was not available. Valtec advised the use of the Amphenol connectors for Galileo 3000-LC fiber. These were on hand and had taken nearly 6 months to procure. Various techniques were evaluated to terminate the Valtec fiber with the Amphenol connector. The method used on most of the cables resulted in excessive insertion loss, about 4 dB, although some cables had losses close to 1 dB. These problems and the adaptations required prevent a fair appraisal of the Amphenol connector.

The data on the ITT Cannon connector are based on a very small number of readings and are not, therefore, conclusive. The evaluation of these connectors yielded the test data and revealed the design deficiencies indicated below:

AMPHENOL 906 SERIES CONNECTOR:

(Terminated with fiber not specified for this connector)

- Insertion loss varied from 1.2 dB to 4.3 dB.
- Repeatability varied ≤ 0.5 dB (unmating/mating 5 times).
- Rotational variation 0.5 dB maximum (through ±180 deg).
- Delrin plastic alignment sleeve came out of many connectors during unmating. Insertion loss increases without the alignment sleeve. This sleeve is very small and can easily be lost once it is removed from the connector body.

ITT CANNON FOT SERIES CONNECTOR:

(Data based on testing of three terminated fibers)

- Insertion loss varied from 1.0 dB to 1.6 dB.
- Repeatability varied ≤ 0.6 dB (unmating/mating 5 times).
- Rotational variation 1.0 dB maximum (through ±180 deg).
- Rubber O-ring frequently came out during unmating. The receptacle must be disassembled to replace the O-ring. It is very small and can be lost easily once removed from the receptacle.
- Polished fiber ends are in direct contact under spring tension within the connector. Potential for scratching and chipping these ends is high.
- Heavy spring in one connector wore out after mating and unmating approximately 360 times during testing of a star coupler.
- The connector is made for use with uncabled fiber.

4. Summary

The evaluation attempted to identify a connector concept which could be the basis for an operational design. The Marine Corps Command and Control application requires a low-loss, ruggedized, environmentally sound fiber optic connector. The connectors tested were intended for controlled environments and cannot be expected to meet the Marine Corps mechanical and environmental requirements. Both connectors have serious design problems. The Amphenol and the ITT Cannon fiber optic connectors tested are both subject to the loss of small internal components while being unmated, and both require the fiber ends to be protected to maintain acceptable performance levels. These design problems must be corrected before either connector can be considered for the data bus application.

D. MULTIPLE-ACCESS COUPLERS

The FY78 analysis determined that a data bus architecture utilizing passive transmissive star couplers would best satisfy the requirements of the Marine Corps Tactical Command-Control system. Passive reflective stars or active tee couplers could also be used to build an acceptable system. This development effort, however, concentrated on the passive single-fiber transmissive star coupler.

A transmissive star coupler is an optical power divider. Light entering one of the input port fibers is distributed equally to all of the output fibers. See figure 3.

1. Essential Parameters

There is no standard terminology for star coupler performance parameters. Many manufacturers do not adequately define the parameters they use, and most employ definitions unique to themselves. Definitions used in this report appear on the following pages.

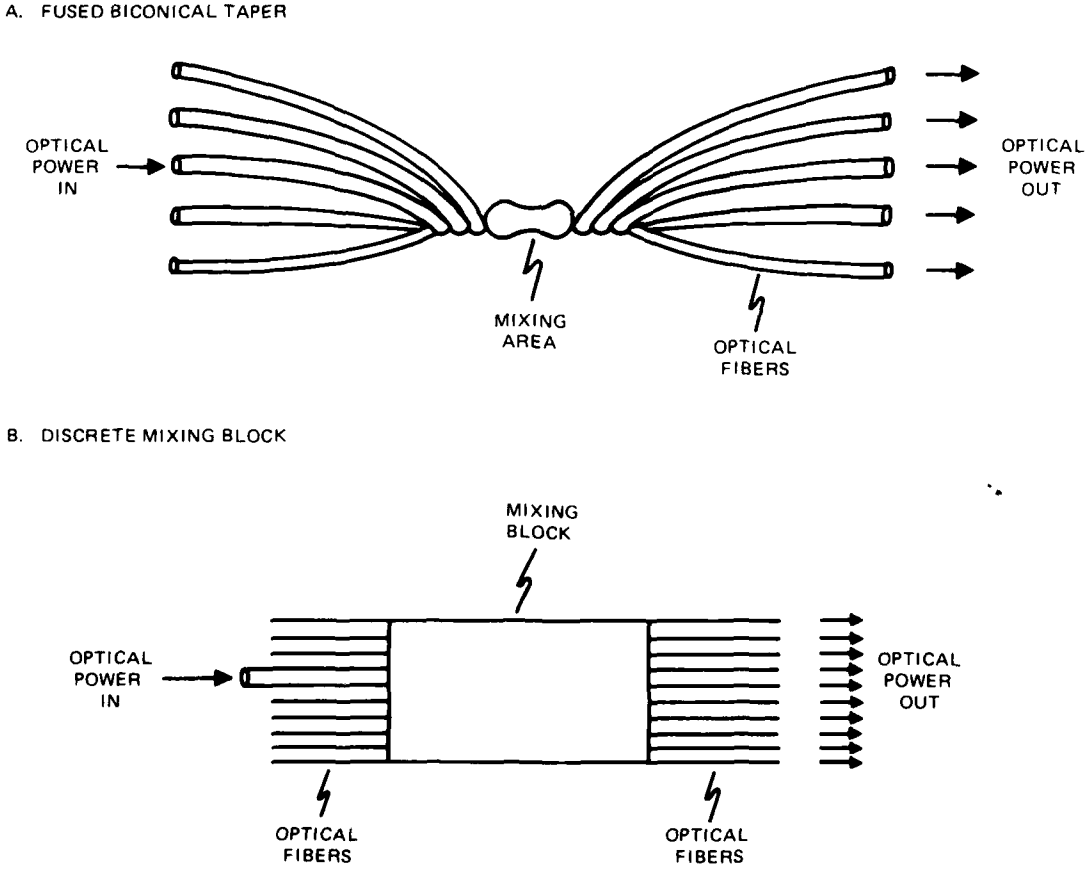


Figure 3. Transmissive star coupler construction.

a. Number of Ports. A transmissive star coupler requires an input port and an output port for each terminal to be serviced. Some manufacturers refer to a star coupler with 16 input ports and 16 output ports as a 32-port coupler. Others refer to it as a 16-port coupler. A standard nomenclature such as "16- x 16-port transmissive star coupler" should be adopted.

b. Insertion Loss. Insertion loss is usually defined as:

$$-10 \log \frac{P_{test}}{P_{ref}} \quad \text{(see figure 4A)}$$

Most manufacturers of star couplers do not include the connector loss as part of the insertion loss. A designer requires a total coupler insertion loss, which includes the connector loss. One manufacturer uses an excellent method to specify this parameter, an insertion loss matrix. The matrix specifies the limitations on insertion loss for every output port of the coupler.

c. **Excess Loss.** This internal optical power loss includes all losses due to internal reflections, scattering, absorption, packing fraction, and fiber misalignment. This parameter is defined as:

$$-10 \log \frac{\Sigma P_{out}}{P_{in}} \quad \text{(see figure 4B)}$$

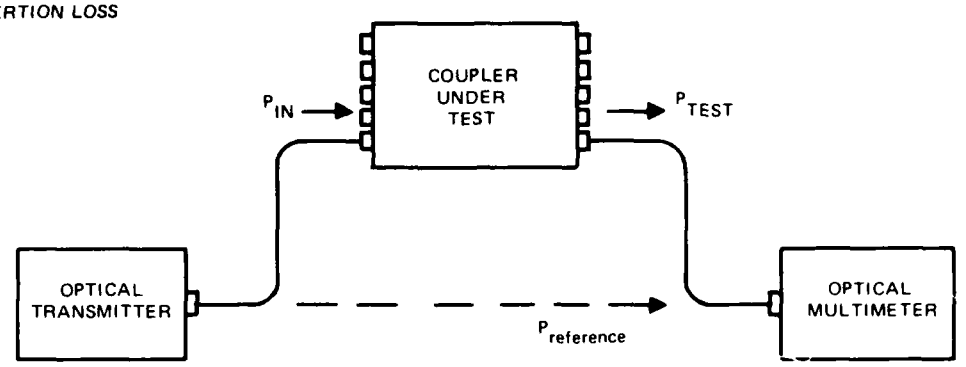
The magnitude of this characteristic is a good indicator of the quality of the coupler. Excess loss need not be specified by the user. Specification of total coupler insertion loss is more relevant from a system design standpoint.

d. Optical Signal Range. This parameter is usually defined as:

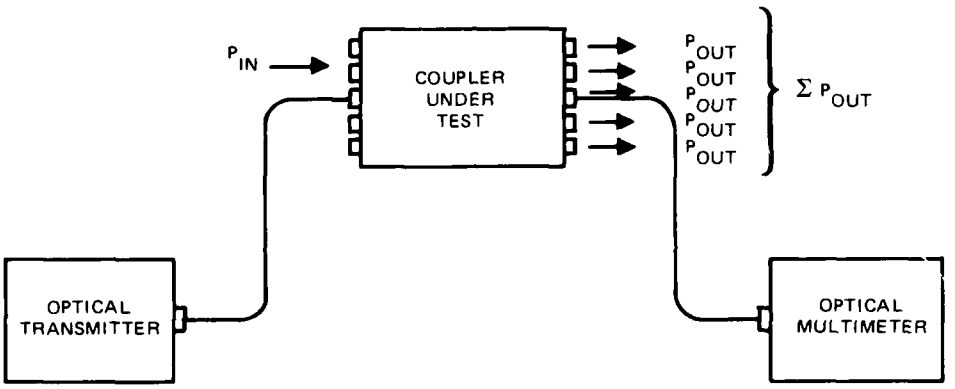
$$10 \log \frac{\text{Maximum } P_{out}}{\text{Minimum } P_{out}} \quad \text{(see figure 4C)}$$

The optical signal range of a coupler indicates how uniformly power is distributed among the output ports. The magnitude may affect the dynamic range requirement of the associated fiber optic receivers. Specification of average optical signal range has been used to make the performance of a coupler appear better than it actually is. Average optical signal range is of little value in designing a system.

A. INSERTION LOSS



B. EXCESS LOSS



C. OPTICAL SIGNAL RANGE

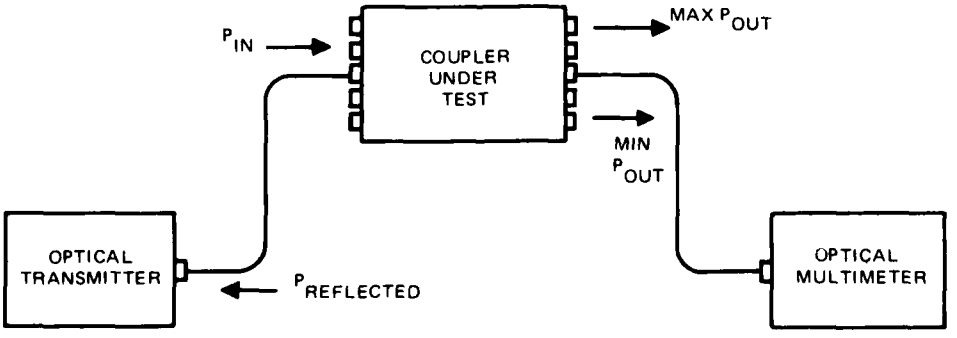


Figure 4. Star coupler test parameters.

e. **Directivity**. This parameter is usually defined as:

$$-10 \log \frac{P_{reflected}}{P_{in}} \quad \text{(see figure 4C)}$$

The specification of this parameter is not essential for the particular configuration chosen for the data bus since the optical power reflected back into the transmitter LED will not degrade the bus system, although it is wasted power.

2. Test Description

a. **Couplers Tested**. Two transmissive star couplers were purchased for evaluation. A 16- x 16-port coupler using a glass core (200 μm), glass-clad (245 μm) fiber and Amphenol 906 series connectors was purchased from the Olektron Corp. for $1600. A 19- x 19-port coupler using a glass core (100 μm), glass-clad (140 μm) fiber and ITT Cannon Model FOT connectors was purchased from ITT/Electro Optics Product Division for $6176. ITT also offered couplers using plastic-clad silica fibers, pigtail-terminated couplers, and a number of alternate connectors, including the Hughes multi-channel and Leeds single-channel connectors. A Spectronics 16- x 16-port transmissive star coupler purchased and tested under another project approximately 2 years ago was also available. Test results for all three couplers are compared here.

b. **Test Setup**. It is difficult to test separately for each of the various parameters which make up total coupler insertion loss. The following will describe the evaluation of coupler insertion loss.

The test setup for both the Olektron and the ITT coupler is shown in figure 5. Test cables were made from fibers and connectors compatible with those used to fabricate the coupler under test. The additional test cable was inserted in the test link to strip the cladding radiant power.

A reference reading, in dBm, was taken with the optical transmitter connected directly to the optical multimeter. This reference was subtracted from each subsequent reading. The difference represents the internal coupler losses plus two connector losses. Output powers were measured and recorded for each output port with the transmitter test lead connected to each input port in turn in order to map the complete (16 x 16 or 19 x 19) insertion loss matrix.

3. Test Results

a. **Test Data**. Appendix A contains insertion loss measurement data for both the ITT and Olektron couplers. A histogram of the data for each coupler is presented in figure 6. Variations in manufacturing and loss from connector to connector resulted in the spreading in the histogram. The insertion losses are summarized below:

ITT Coupler	19 ± 7 dB
Olektron Coupler	19 ± 5 dB
Spectronics Coupler	23 ± 8 dB

An estimate of the magnitude of coupler insertion loss components follows:

Power division	12 dB
Excess loss	5 dB
Connector (2) loss	2 dB
Total insertion loss	19 dB

The means of the measured values are very close to the estimated value of insertion loss. The rather large variation for each coupler is an area that needs improvement.

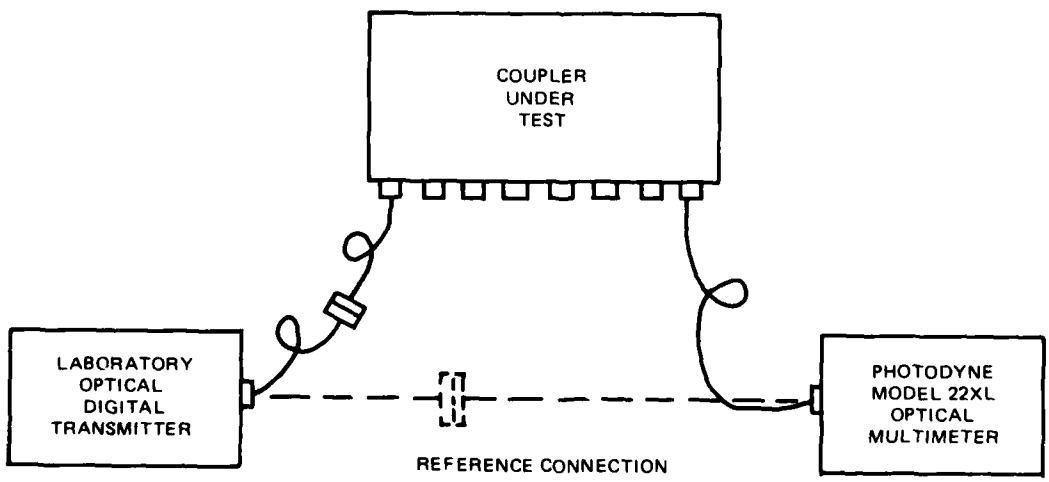


Figure 5. Star coupler test setup.

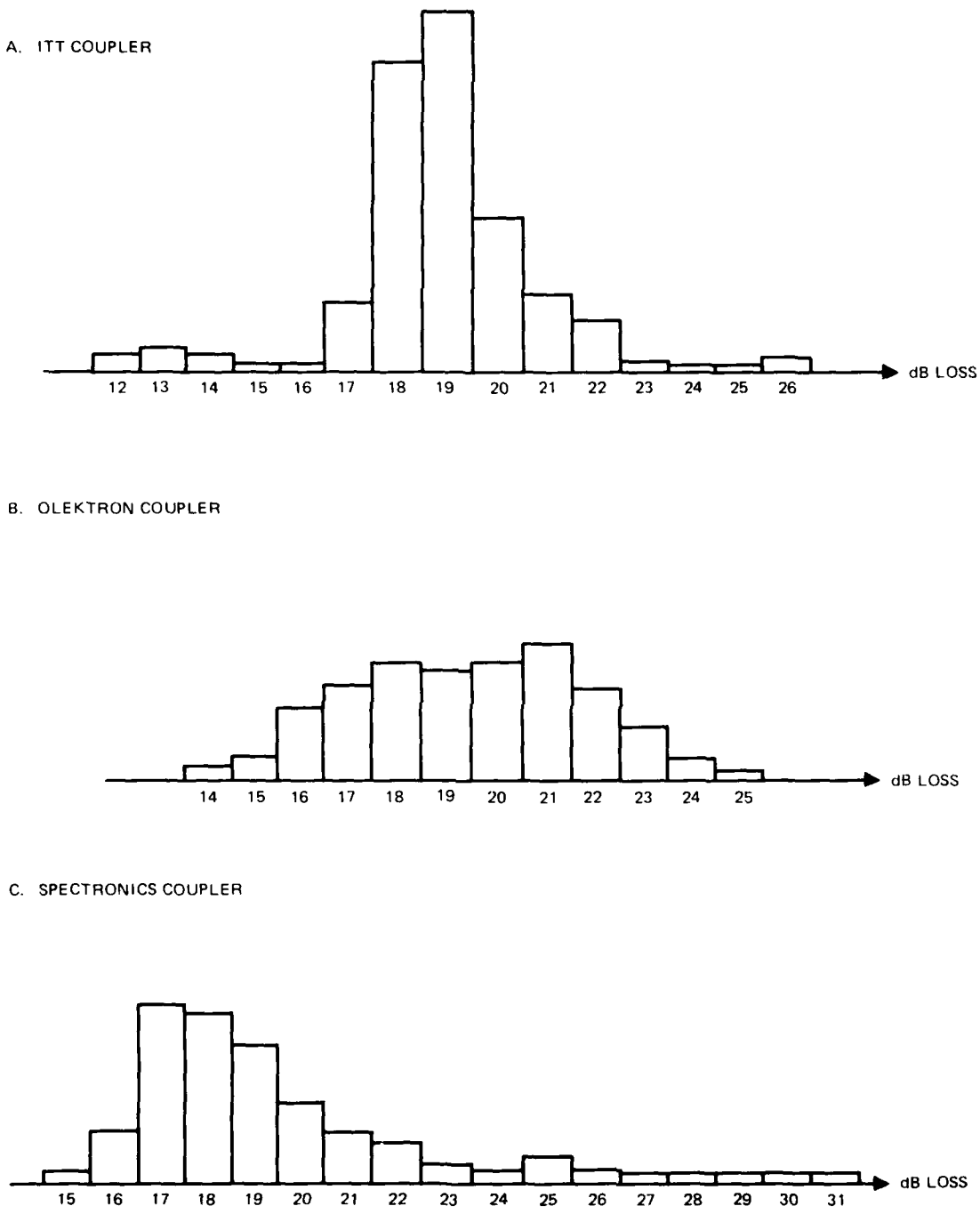


Figure 6. Histogram of star coupler insertion loss.

b. Coupler State-of-the-Art Characteristics. The following paragraphs discuss the current state of the art of the transmissive star coupler based upon testing, study, and analysis of the units described above.

(1) FABRICATION METHOD – Two methods of coupler fabrication are being employed, the discrete mixing block method and the fused biconical taper method. See figure 3. The mixing block method employs fibers attached to opposite sides of a mixing block. Fibers are heated while twisted and under tension to produce a fused biconical taper. Mixing occurs within the fused region of the fibers. The simplicity of the fused biconical taper method suggests that it might be employed to produce more reliable devices at lower cost. The input-output port-pairs that are in line tend to have significantly less insertion loss than other pairs, which is not a desirable characteristic. The diagonal row in the ITT coupler data in Appendix A illustrates this characteristic. The difference is approximately 5 dB in that case.

(2) NUMBER OF PORTS – Transmissive star couplers are being fabricated with up to 19 x 19 ports. The number of ports is currently limited by manufacturing difficulties. Couplers with 32 ports and greater are technologically feasible and should become available shortly.

(3) FIBER/CONNECTOR LOSS – Spectronics Corp. and ITT used a 100-μm-core-diameter glass-core/glass-clad fiber to fabricate their couplers, while Olektron Corp. used a 200-μm-core-diameter glass-core/glass-clad fiber. There was no discernible advantage attributable solely to fiber core size. The optical signal loss of the fiber within the star coupler is negligible because of the very short length used. Vendor claims for single-fiber connector loss range from 0.7 to 2 dB. Measured losses for connectors used in the evaluations ranged from 1 to 4 dB. Our experience indicates that the connector loss realized in practice is highly dependent upon the skill of the technician terminating the fiber. The variation in connector loss contributes to the dynamic range requirement of the optical receiver. A connector design objective should be to minimize this loss variation in the assembled device. The fiber optic connector was discussed in Section V.C.

(4) EXCESS LOSS – Excess loss for all three couplers tested was between 3 and 6 dB. This parameter can be reduced greatly since the theoretical excess loss of a coupler is less than 1 dB.

(5) INSERTION LOSS/OPTICAL SIGNAL RANGE – Test results were as follows:

	Insertion loss, dB	Optical signal range, dB
ITT	19	14
Olektron	19	11
Spectronics	23	16

The 19-dB insertion loss for the couplers tested is acceptable. The large optical signal range needs to be reduced. The unequal division of optical power in a

coupler can be attributed to design and manufacturing deficiencies. The connector loss also contributes to the optical signal range.

4. Summary

The 16- x 16- and 19- x 19-port transmissive star couplers are practical components for limited use in a number of operational fiber optic data bus systems. Repeaters permit an unlimited number of users for bus systems having cascaded passive couplers. The excess loss and optical signal range of the coupler are parameters where improvements would simplify overall system design. These coupler loss mechanisms require improved designs and manufacturing techniques for improved performance.

E. FIBER OPTIC TRANSMITTER/RECEIVER

1. General

Transmitter and receiver units provide the electro-optic interfaces for the data bus. The performance objective for these units is to produce the effect that would be seen if the input to any transmitter were at the output of a receiver. The accuracy of reproduction can be measured by comparing the state (high or low) and location of the transitions of the received signal with those of the transmitted signal.

There are many approaches that might have been taken to accomplish the objective; the one used is based on a relatively simple concept. The transmitter produces an optical output which is an analog of the binary electrical input waveform. The receiver converts the optical signal back to electrical form.

The initial objectives for the data bus system included a 10-Mbps data transmission rate. The transmitter was designed and constructed to that objective. Subsequently the data rate was reduced to 1 Mbps to facilitate the construction of the bus. This reduction allowed an LSI integrated circuit to be used to format the data and a microprocessor to be used as the bus controller and to provide interfaces between the terminal equipments and the bus. The alternative of developing these functions would have increased the effort required to many times the available tasking. The design of the 10-Mbps receiver was in progress when this change occurred. A decision was made to set aside the work on this design in favor of one dedicated to the 1-Mbps application. This was judged to be the best approach to meeting the timetable for having an operating system.

2. Transmitter

The transmitter output level needs only to be sufficient for the receiver to differentiate between the high and low states. The transmitter consists of circuits to provide the required input compatibility and a switch to turn the LED on and off. The relative temporal locations of input transitions between high and low states must be preserved in the optical output signal to help minimize errors. Propagation delays in the transmitter for both transitions must therefore be considered carefully and equalized.

The transmitter appears in schematic form in figure 7. The input is TTL compatible. Circuit propagation delays have been minimized so that relative spacing of successive transitions is retained in the LED current. The output transistor is used as a current source to assure that the waveform of the LED current is not affected by either LED nonlinearities or associated series reactances.

The required output from the transmitter, based on the NOSC TR 342 analysis, was 100 μW (-10 dBm). It is more reasonable, however, to plan on 50 μW (-13 dBm) being available. Propagation delays are not usually significant, but the associated pulse-width distortion is. This distortion should not exceed 10% of a bit time, which is 5 ns for a 10-Mbps data rate.

Rise and fall times of the transmitter output are of secondary importance compared with the difference in propagation delays. It is desirable, however, from the point of view of the receiver design, that the peak-to-peak amplitude of the received signal not change as a function of the data pattern. This can be accomplished by assuring that each transition is completed, within some acceptable error (say, 10%), in one bit period. Each component of the link contributes to slowing this transition. The contribution of the transmitter can be minimized by making it appreciably faster than the receiver. This is a relatively easy approach. A factor of about three faster will result in a 10% contribution to the overall transition times. A 10-Mbps-data-rate manchester-encoded signal would then require transition times of 5 ns or less.

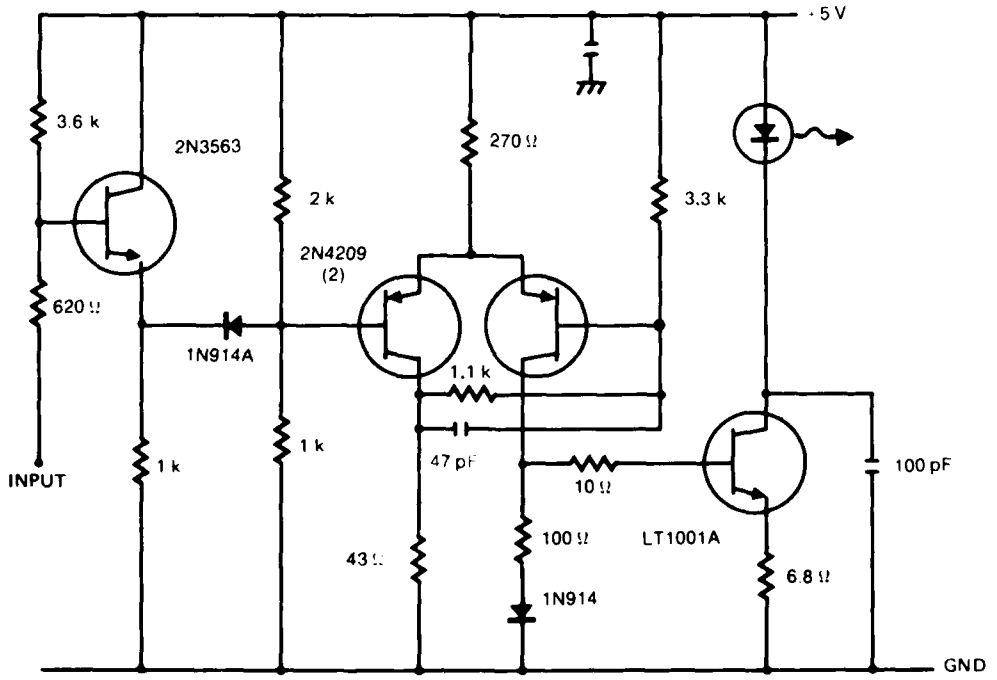


Figure 7. Digital transmitter (non-inverting).

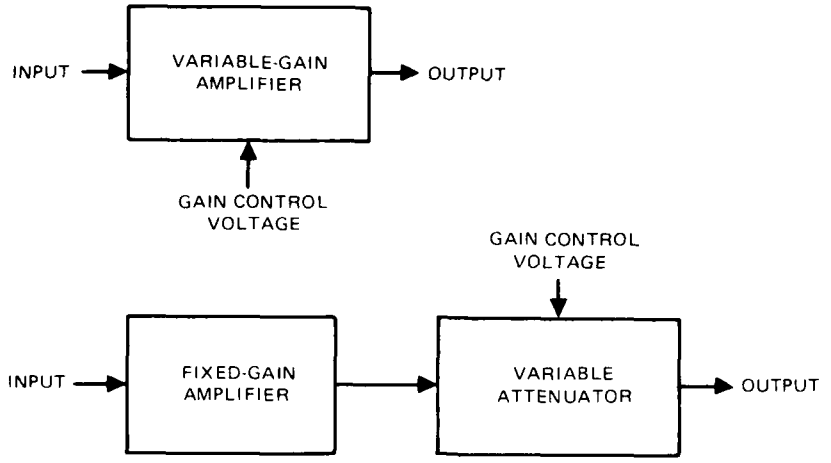
3. Receiver

Receiver characteristics which determine the efficacy of the data bus system include the range of signal levels over which acceptable operation is obtained, the level of signal quality, and the response to signal bursts of varying strengths and temporal spacings. Signal range is defined by the lowest and highest signal levels which bound a continuous range of signal levels over which an acceptable quality of signal transmission is maintained. Signal quality is measured in terms of an error rate for data entered and received at any bus terminal.

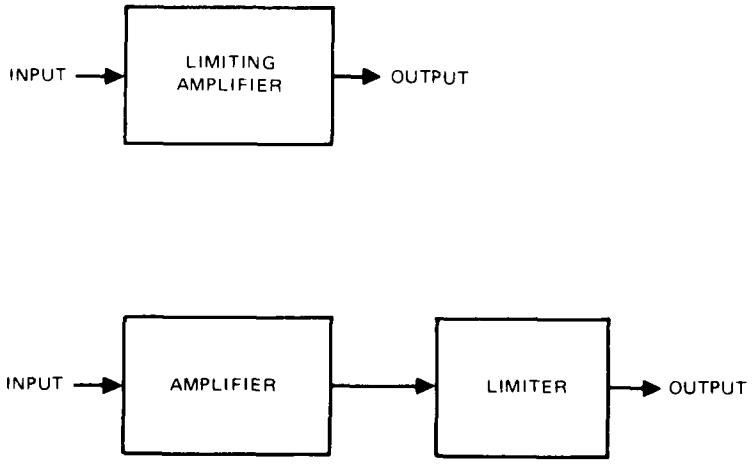
An important objective in the data bus receiver was to accommodate as large a difference in received signal levels as possible and to minimize the effect of previous transmissions on the current transmission. Electronic circuits do not respond instantaneously to a stimulus. Delays exist both in responding to and recovering from a stimulus. The largest signal which the receiver can respond to in a controlled fashion is ultimately determined by the available power supply voltages. The minimum detectable signal is determined by electronic noise originating in the input circuit of the receiver and transients initiated by preceding signals. This signal range problem is not entirely novel or unique to fiber optics applications, and some general approaches have evolved in responding to it. There are two fundamental approaches: either the receiver response to changes in the average level is made insignificant in relation to its response to the signal, or the signal waveform is made so that the average component is greatly reduced. The former approach was taken. The illustrations in figure 8 depict some approaches to increase the input level at which a receiver will overload. In figure 8A a variable-gain stage is shown. The gain of the stage can be controlled either directly or through a cascaded controlled-attenuator stage. The *limiting* amplifier is another approach. This type of amplifier has high gain for low-level signals and essentially *zero gain* for signals above the limiting level. This limiting function can also be accomplished in a stage separate from the amplifier. When subject to a high-level input signal, the amplifier gain must change before the amplifier overloads. The variable-gain amplifier requires a control signal to change its gain. The generation of this signal is itself encumbered by overload problems and signal delays. Limiting amplifiers do not require a control signal but produce severe waveform distortion.

Limiters which are primarily constrained in signal handling capability by the available power supply voltages can easily be built. Such capability can be far in excess of what would be required in this application. A diode limiter was evaluated and this performance confirmed. The approach chosen for this task was to design a wide-range receiver incorporating such a limiter.

The overall block diagram for the receiver appears in figure 9. The basic objective of the receiver processing is to recover only that portion of the incoming signal waveform that lies about the midpoint between its peak excursions. This particular portion has the property of preserving the original locations of the signal transitions. The receiver is direct coupled. The input stage converts the optical input signal to an electrical signal. The optical signal is unipolar, radiant intensity increasing from the quiescent or no-signal condition. Consequently, the resulting electrical signal is also unipolar. The signal is filtered to provide high attenuation above the cutoff frequency (2.2 MHz for a 1-Mbps-data-rate Manchester-encoded signal). The output signal from the filter buffer amplifier is split into two parallel paths. In one of these paths a peak detector captures and



A. VARIABLE GAIN



B. LIMITING

Figure 8. Methods to delay amplifier overload.

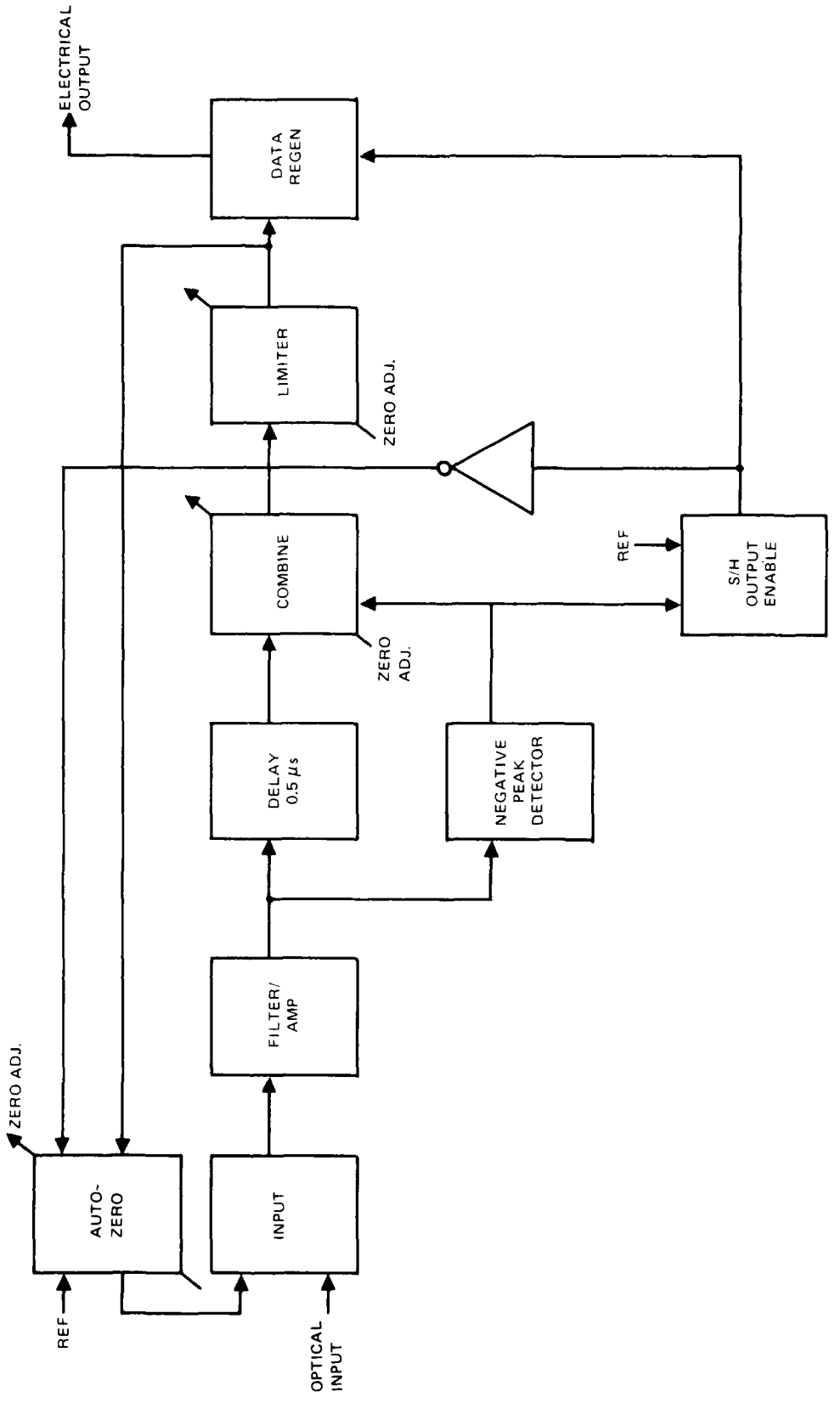


Figure 9. Receiver block diagram.

briefly holds the signal peak level. The other path passes through a delay line to allow the peak detector time to perform its function. Outputs from the peak detector and the delay line are combined, so the resulting signal excursions above and below ground are equal. A limiter stage greatly amplifies that portion of the combiner output waveform which is near ground level.

This amplified and limited signal is applied to a comparator to regenerate the original data. Gain is kept low in the analog portion of the receiver to achieve the greatest dynamic range. The dynamic range is determined by the ratio of peak output to noise levels. The data regenerator provides the bridge between the analog portions of the receiver and the digital output. Two comparators make up the regenerator. One comparator receives the output from the limiter, a fixed reference voltage at a level above the noise peaks, and an enable voltage. This comparator produces the digital data output signal. The other comparator receives an output from the negative peak detector and a fixed reference voltage and provides an output enabling the first comparator when the optical input exceeds a level determined by the reference. This reference represents a minimum input signal level required to assure that the output data error rate does not exceed a maximum limit. The enabling signal also disables the sample-and-hold circuit.

The ultimate sensitivity of the receiver is determined in part by the dc offsets of the various stages in the analog portion of the receiver. These offsets affect the accuracy with which the processed signal at the data regenerator input is centered about ground and, consequently, the location of the transitions in the output data.

An auto-zero circuit is used to reduce the offset at the input to the regenerator. The voltage at the limiter output is applied to a sample/hold amplifier. The output enabling signal from the regenerator is inverted and also applied to the sample/hold amplifier so that the limiter output is sampled whenever there is no input signal to the receiver. The output from the sample/hold amplifier is fed back to the input stage in the proper polarity to reduce the offset at the limiter output. This process also stabilizes the interstage offsets, thereby reducing error in the detected peak level.

The receiver includes a dc-to-dc converter, which provides bias to the photodiode. A single transistor-tuned collector-oscillator converts the available dc current to sinusoidal variations through the primary of a transformer. The transformer secondary steps up the voltage. This voltage is rectified and filtered to provide the high-voltage dc output. A second transistor regulates the output voltage. A sinusoidal oscillator is used to avoid the production of strong high-frequency signals, as would be the case with a switching-type converter. Such signals could couple to the receiver amplifier and compromise its performance.

The assumptions of NOSC TR 342 led to the following requirements for the receiver. The sensitivity expected of the receiver was -42 dBm for an error rate of 1×10^{-9}. The corresponding electrical signal-to-noise power ratio for this error rate is 18.5 dB when Gaussian noise is assumed. Therefore, the optical noise equivalent power (NEP) requirement for the receiver is -42 dB - 9.3 dB = -51.3 dBm or 7.4 nW. The port-to-port loss allowed for the demonstration data bus was 25 dB with a ±3-dB variation. This loss, in association with the -13-dBm output from the transmitter, suggests that the signal at the receiver would range from -41 dBm to -35 dBm. It was suspected that a much greater range would actually be found in the system once assembled, and the design objective

for the receiver was the maximum that could be achieved. The minimum response time given in MIL-STD-1553B is 4 μs. The receiver would have to fully recover from an input at the maximum level within 4 μs to properly respond to a following signal at the minimum level and with the minimum spacing. The maximum pulse-width distortion was to be minimized; a 10% change would be acceptable.

4. Construction

The transmitter and receiver are contained within the same enclosure. The circuitry for both is on two printed circuit boards which plug into each other. The receiver resides on one large board, while the transmitter and dc-to-dc converter are on another, smaller board. Power and electrical signal ports are accessible through a single multi-pin connector. Single-fiber optical connectors are used for transmitter output and receiver input. The LED and photodiode both have fiber pigtails to enhance coupling efficiency and to allow these components to be located on the printed circuit boards in electrically advantageous positions.

5. Performance – Transmitter

A variety of LEDs were used in the units constructed for the demonstration system. This is reflected in the performance data. Performance of the transmitters constructed is summarized below:

Serial	LED Type	P_O, μW(dBm)	T_r, ns	T_f, ns	Bias, ns
0	LDL 160	118 (-9.3)	17	20	4 spacing
1	LDL 611	118 (-9.3)	11	12	4 marking
2	C30133	35 (-14.6)	4	10	3 marking
3	LDL 160	92 (-10.4)	17	17	3 marking
4	Hitachi	152 (-8.2)	15	14	1.5 marking
5	Hitachi	58 (-12.4)	--	--	--

Notes: P_O is the high-level optical output power;
T_r is the rise time of the optical output;
T_f is the fall time of the optical output;
Bias is the difference between the width of the electrical input pulse and the optical output pulse as measured at the 50% point.

The emission wavelengths of all the above LEDs ranged from 800 to 850 nm. The one unit with the LED selected for this application, an RCA C30133, showed the lowest power and the fastest transition times for the group. The measured output power for this device is notably less than what had been projected for the optimum system, -10 dBm (100 μW). The small-quantity cost for the LEDs employed in the transmitter ranged

from $200 for the RCA C30133 to more than $300 each. These prices reflect a limited market and are expected to fall to $50 or less when production quantities become larger.

6. Performance – Receiver

The specification of a receiver for use in a specific data bus need only state the sensitivity (minimum input signal level at and above which there is a continuous range of signal levels where a maximum acceptable error rate is not exceeded) and the signal range (the extent of a continuous range above the minimum input signal level for which the error rate does not exceed the maximum acceptable value).

If there is no specific data bus clearly intended, then more performance parameters will be required to describe the receiver performance. A suggested listing of such parameters appears below:

Noise equivalent power (NEP)	–	maximum average value at a specified wavelength
Sensitivity	–	as described above, at a specified wavelength, measured using a specified data pattern and transmission format
Signal range	–	minimum continuous range of input signal levels at a specified wavelength above the level at which sensitivity is specified for which all specified performance parameters are valid
Word spacing	–	minimum allowable spacing between successive received data words, each having any level within the signal range for which all performance parameters apply
Signal data rate range	–	data rate range of input signals for which all performance parameters apply
Edge jitter	–	maximum average jitter to be expected over signal range
Δ propagation delay	–	maximum expected difference between low-to-high and high-to-low transitions over the signal range
Input compatibility	–	fiber optic connector and cable types required
Output compatibility	–	description of electrical interface (including connectors), impedance or similar characteristic, and levels
Special requirements	–	peculiar signal characteristics required for proper operation

Some attempt was made to determine [illegible] general receiver parameters; however the complexity and extent of the [illegible] surements placed a severe limitation on what could actually be accomplished.

The performance of the receiver input stage was ascertained by measurement independent of the remaining stages. NEP for the operating bandwidth was calculated to lie between 0.9 and 1.8 nW. Measured values ranged from 1.3 to 1.7 nW.

Receiver overload occurs first in the filter amplifier at about 24 μW (-16.2 dBm).

The receiver outputs must be enabled to have data available. Measured input powers required for this ranged from 40 to 170 nW. These levels represent signal levels on the order of 20 mV at the comparator input, which is commensurate with the input offsets. This data bus requires that the receiver be enabled for an input signal level of 25 nW to eliminate the need to select receivers and transmitters for particular coupler paths.

Recovery of quiescent conditions following an input varies, depending upon the strength of that input from about 1 μs for a 55-nW input to 25 μs for a 20-μW input. Although MIL-STD-1553 B requires that recovery take place in 4 μs or less, the demonstration bus employs a modified protocol which requires that this time be 25 μs or less.

Pulse-width variations were found to not exceed 60 ns from 60 nW to 15 μW. When overload occurs pulse-width distortion becomes gross, being many times a bit width.

F. BUS INTERFACE UNIT

1. General

The Bus Interface Unit (BIU) provides the hardware and software needed to interface between the terminal equipment (CRT, Teletype, etc.) and the data bus. The BIU provides the necessary timing, formatting, and encoding needed for the orderly transfer of data on the bus as required by the bus protocol. The protocol used is a modified command/response version of MIL-STD-1553B. The protocol is discussed more thoroughly in Section V.F.2. Initially the system was configured with a central controller controlling all activity on the bus. The controller would identify the terminals that were to communicate, and the terminals would respond if they had data to send. Another version of the protocol that was used involved the elimination of the central controller. The single central bus controller configuration has a serious survivability problem. Failure of the bus controller would result in failure of all terminals to communicate. To prevent this type of catastrophic failure, a modified configuration was designed which distributed the bus controller function among all the terminals on the bus and eliminated the central bus controller. This modification was accomplished entirely in BIU software. The distributed bus controller program is contained wholly in one pair of erasable PROMs. In this version each terminal was capable of being a controller. Once a terminal acquired the bus it would transmit its data, then request another terminal to take control of the bus. It would release control of the bus when another terminal accepted the request. Descriptions of the central and the distributed controller software are in Section V.F.5.

2. Protocol

a. Central Controller. The controller orchestrates bus activity. It determines which terminal can transmit on the bus and when. Each terminal is identified by one or two addresses, a transmitter address and/or a receiver address. The addresses were assigned so that receiver addresses are even and transmitter addresses are odd. A transmitter sends data to an address that is one higher than its own. The controller increments through the addresses, offering the bus to each transmitter terminal in turn. A receiver command word is transmitted, followed by a transmitter command word. If the terminal addressed to transmit has data, it will transmit a receive command word followed by the data words. A terminal that has transmitted data requires a status word from the receiving terminal acknowledging that the data have been received correctly. If such a status word is not received, the terminal will retransmit the data the next time it gains access to the bus. If the terminal addressed by the controller to transmit does not respond within 30 μs or there are no signals on the bus for more than 30 μs, the controller continues to offer the bus to the next address.

b. Distributed Controller. In the distributed controller protocol, the bus controller function is passed from terminal to terminal. The bus controller offers control to the other terminals by issuing transmit commands to each in turn. The controller allows 25 μs for a response, after which it proceeds to the next address in numerical order. Transfers of control are normally accomplished by responding to a transmit command from the controller. If the terminal addressed has data to transmit, it assumes control of the bus. The controller transfers data by issuing a receive command followed by the data. The controller allows about 20 μs to receive a status word from the receiving terminal, acknowledging receipt of the data before proceeding. If the status word is not received, the data are retained and another transfer attempt is made when the terminal is again addressed in a transmit command. If the data are successfully transferred on the first attempt after control is assumed, the address register for the transmit command is set to zero. It is not set for any other condition. This process is continued by the controlling terminal until it relinquishes control. A second way for a terminal to gain control occurs when there is no activity on the bus. Each terminal senses the lack of activity and will assume control of the bus if this condition persists for a length of time proportional to its address. This proportioning avoids conflict among the terminals. The controlling terminal drops control of the bus if another terminal accepts control or if its input requires service.

3. Word Formats

A modified version of MIL-STD-1553B is used. Figure 10 shows the format for the words that are transmitted over the system. The first three bit times comprise the sync. The sync is an illegal Manchester code that can be identified by the decoder as the start of a word. The phase of the sync identifies the word as a command/status word or a data word. Figure 10 shows the sync phase for these words. The 16 bit times following the sync can contain addresses, data and/or status information.

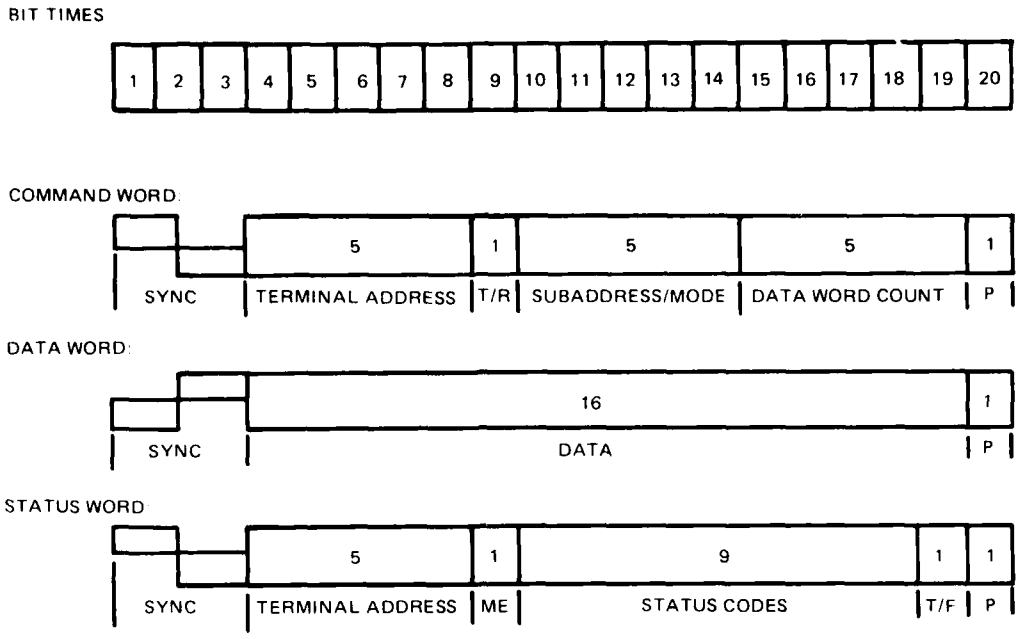


Figure 10. Word Formats.

A command word contains the address of the terminal that is to receive the word in the next five bit times (4-8). Bit time 9 indicates whether this word is a transmitter request (high) or a receive request (low). Bit times 10 through 19 are not used in either the command word or the status word for the central controller program. The distributed controller program uses bit times 10 through 14 of the command word for the address of the controlling terminal and bit times 15 through 19 to indicate the number of data words to be transmitted. A data word uses bit times 4 through 19 for data. The last bit, 20, is the parity bit for all word types. The least significant bit of data and addresses contained in these words is transmitted first.

4. Hardware Description

a. General. The hardware for the BIU consists of an Intel Corp. SDK-86 microcomputer board with circuits added to provide a serial interface to the fiber optic transmitter/receiver unit.

The SDK-86 was chosen for a number of reasons. The SDK-86 provides a 16-bit microprocessor, 2k bytes of RAM, 8k bytes of PROM, a serial input/output (I/O), 48 lines of parallel I/O, and a breadboarding area. The 8086 microprocessor used on the board is capable of operating with a 5-Mhz clock. The high clock rate of this microprocessor and its ability to handle 16-bit-wide data were attractive in this application. The availability of the SDK-86 and an Intel microprocessor development system to aid in programming and debugging the 8086 microprocessor provided additional incentive for using the SDK-86. While the SDK-86 is not the optimum system to provide the BIU function, its use saved time that would have been required for hardware and software design and debugging.

Block diagrams of the interface circuits between the SDK-86 board and the fiber optic transmitter/receiver unit are shown in figures 11 and 12. Figure 11 shows the section dealing with transmission of data and figure 12 shows the receiving section. Schematics of the circuits are in Appendix B.

A Harris Corporation HD-15530 Manchester encoder–decoder integrated circuit is shared by both the transmit and receive sections. The data sheet for this device is included in Appendix B.

b. Transmit Section (See figure 11). This portion of the interface converts the parallel data from the microcomputer to serial data, determines a parity bit for the data, encodes the data, and provides a proper sync signal. The microcomputer provides the data to be transmitted in 16-bit-wide blocks. These data are loaded into the parallel-to-serial (P/S) converter for transfer to the Manchester encoder. The Manchester encoder formats the data for transmission on the bus by adding the proper sync signal identifying it as a command or data word and calculating and adding a parity bit as well as Manchester-encoding the data. Data transfer into the P/S converter occurs when the TRNS ENABLE line is set high by the microcomputer. The encoder provides a gated clock signal to the P/S converter to shift the data out of the converter and into the encoder. The SYNC SELECT line is set high for a command word and low for a data word. Switch-selectable terminal address data are provided to the microcomputer via an 8-bit input port.

c. Receive Section (See figure 12). The receive section of the interface decodes the Manchester-encoded signal, checks for errors, and converts the serial data to parallel data. The Manchester decoder decodes the incoming signal, checks for code and parity errors, and examines the sync signal to determine whether it is a data word or a command word. The CMD/DATA and TAKE DATA lines are both set as the data are being decoded. The TAKE DATA line is set high. The CMD/DATA is set high for a command word and low for a data word. A clock signal from the decoder gated by the TAKE DATA signal clocks the decoded data into the serial-to-parallel (S/P) converter. If no errors are detected in the word, the VALID WORD line goes high, latching the data into the parallel outputs of the converter. The VALID WORD, TAKE DATA, and CMD/DATA lines are connected to the microcomputer's input ports to indicate that valid input data are present.

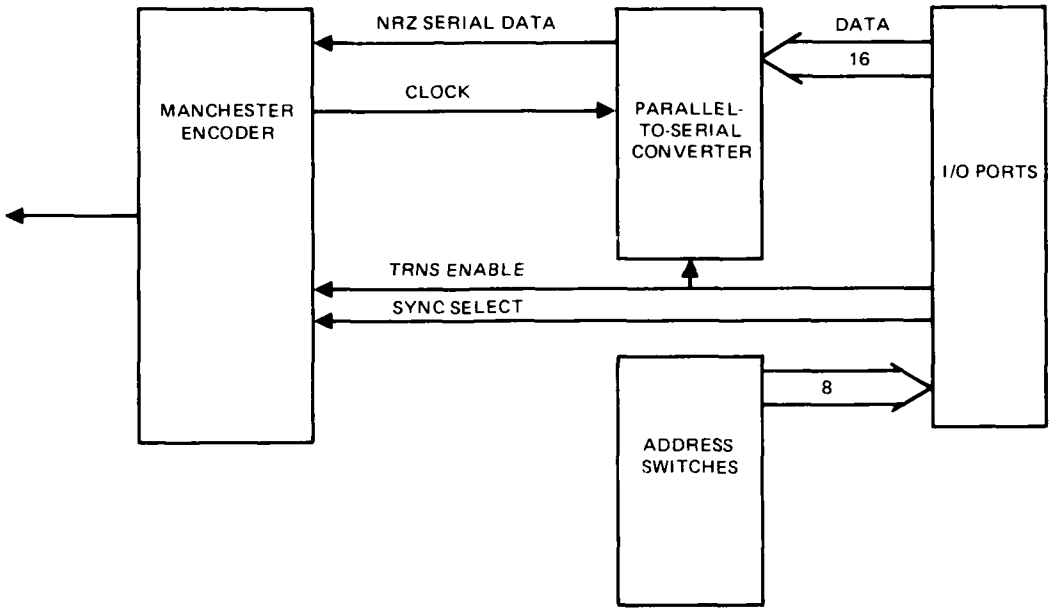


Figure 11. BIU transmit block diagram.

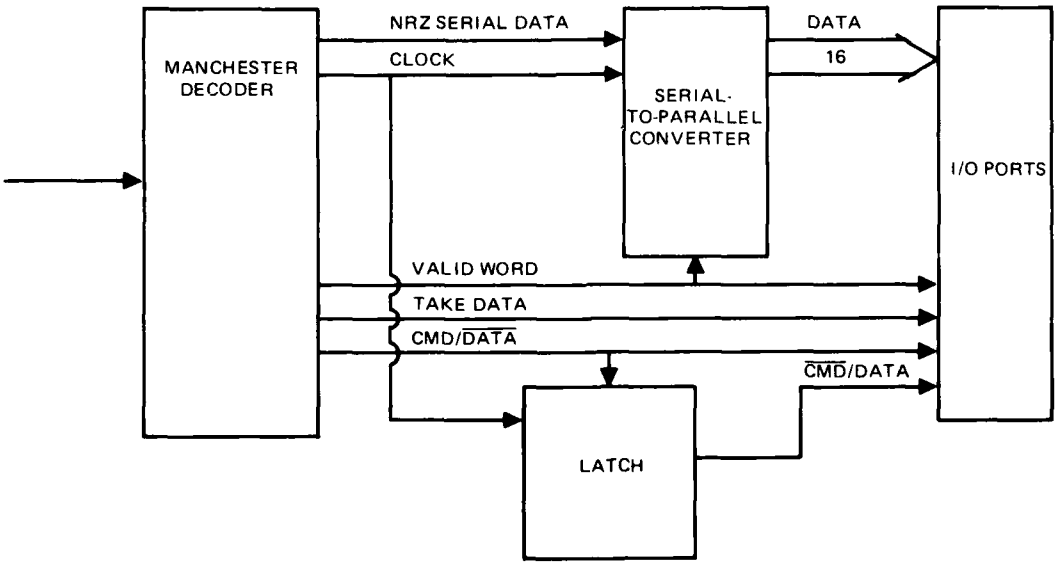


Figure 12. BIU receive block diagram.

5. Programming

a. General. Programming determines the function performed by a BIU. A BIU may be programmed as a controller or as an interface between the terminal equipment and the bus. Control can be centralized or it can be distributed. These programming instructions are contained in erasable programmable read-only memories (EPROMs) on the SDK-86 board.

Programs for the 8086 microprocessor were developed using an Intel MDS-800 Microcomputer Development System (MDS). The development system facilitates program development by simulating the operation of the 8086 and providing an interface to the human programmer. The keyboard allows the programmer to enter and alter the program via structured English-language and numerical commands. A video display presents the simulated 8086 performance in these same terms. This process is the opposite of working with the actual unit, where changes would be made in hardware and performance assessment would require specialized equipment and tedious waveform interpretation.

To aid in program development, the development system allows a program to be broken into blocks which can be worked on independently. These blocks are referred to as modules. Modules used in the BIUs are discussed below.

b. Terminals. The terminal BIUs are capable of receiving and transmitting up to 32 words of data per transmission. The software for this task consists of three program modules. The main program module (RT1) controls the interface with the Harris encoder-decoder. It determines when data on the bus are meant for the terminal and when it is time to transmit on the bus. The INSUB1 program module provides the instructions to input and store the data from the terminal. It also provides a very limited text editing capability so that typing errors may be corrected before the information is sent. The OUT1 program module contains the instructions to output the data to the terminal. INSUB1 and OUT1 can be changed for different types of terminals without having to change the main program. Flow charts for these programs are shown in figures 13, 14 and 15. Program listings are included in Appendix C.

c. Central Controller. The central controller program, CONTR, is contained in one module. The flow chart is shown in figure 16. An assembly language listing of the controller software can be found in Appendix C.

d. Distributed Controller. The distributed bus controller program is contained in three modules. The DBC2 module controls the BIU's interface to the data bus. The other two programs INSUB2 and OUT2 control the handling of data from the terminal.

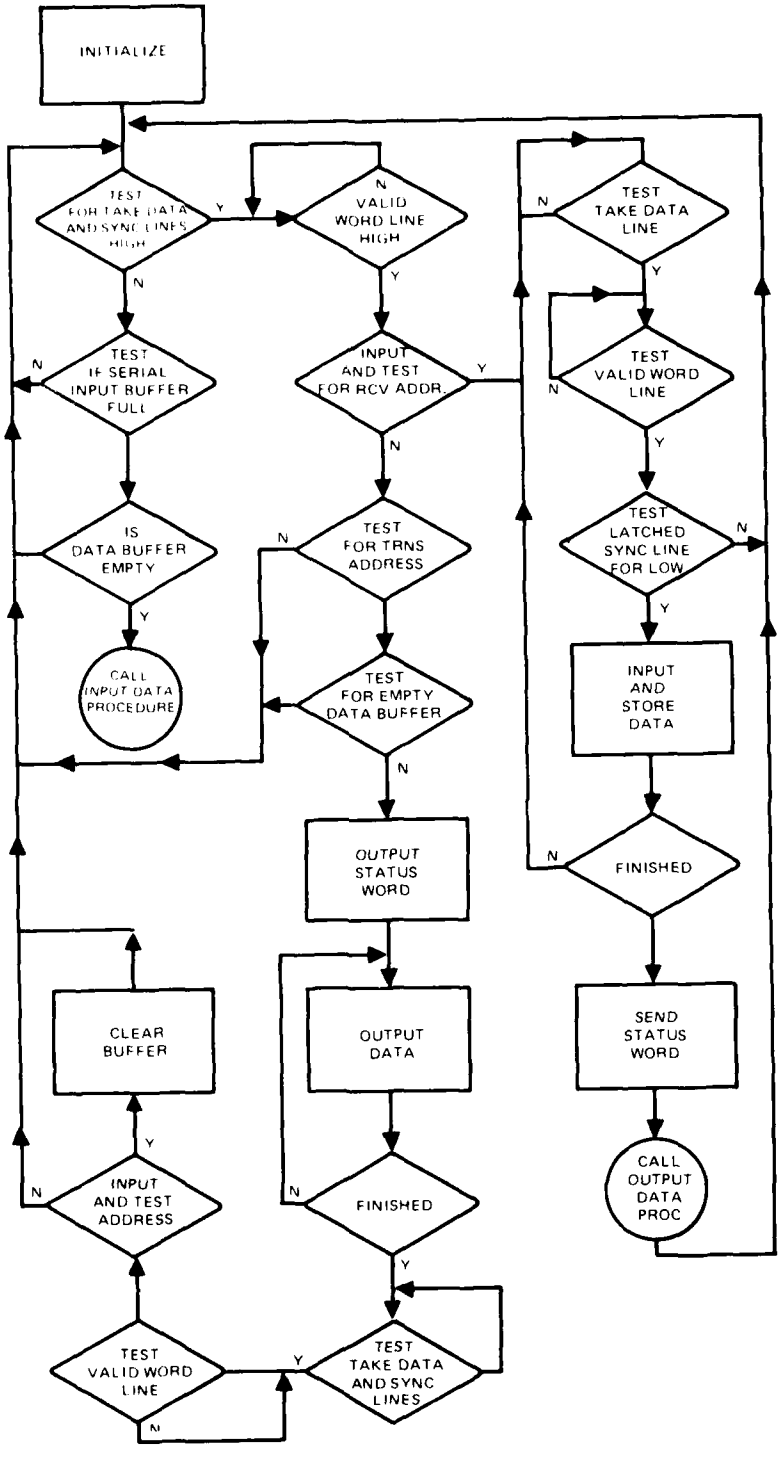


Figure 13. Flow chart for RT1 program module.

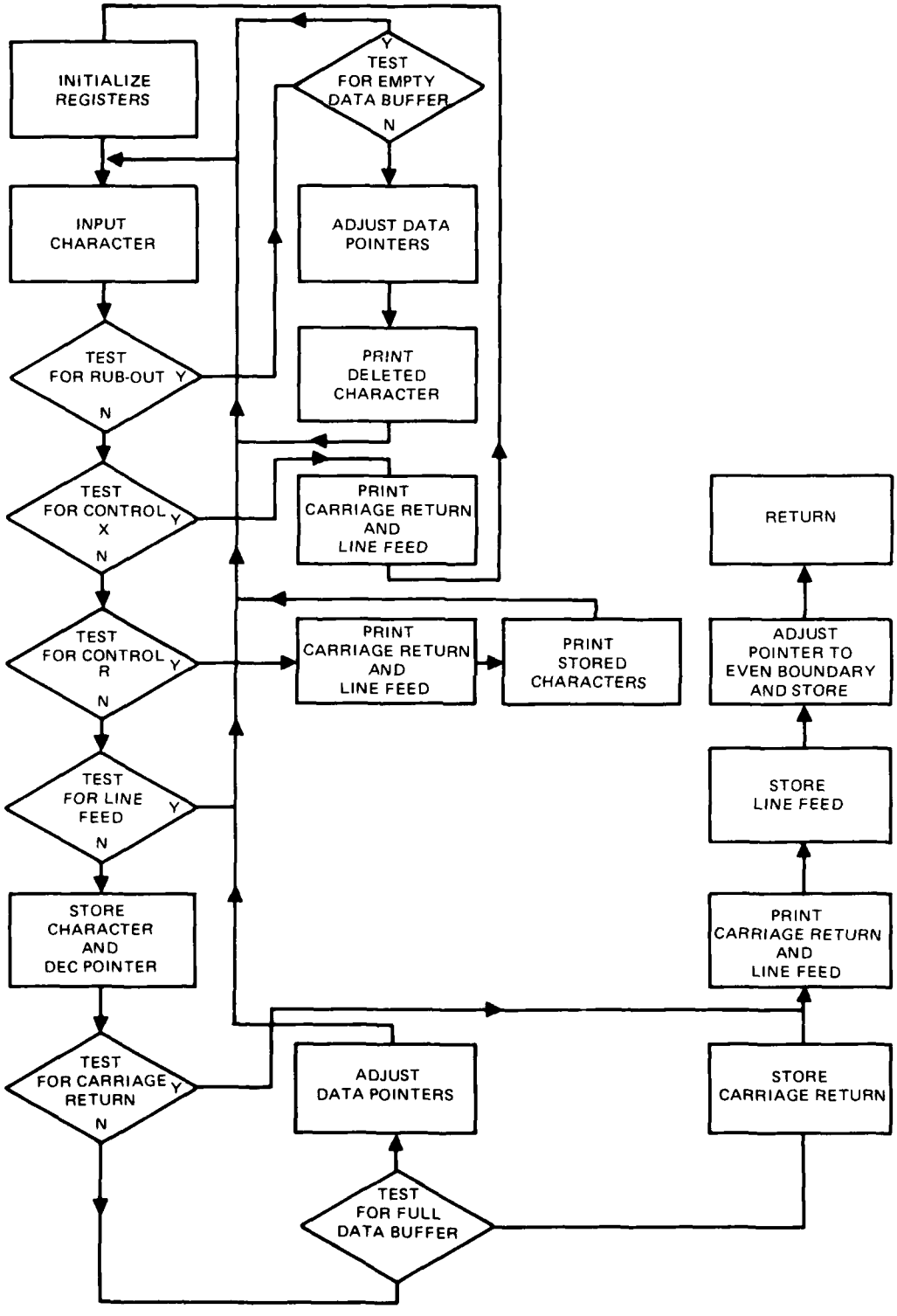


Figure 14. Flow chart for INSUB1 program module.

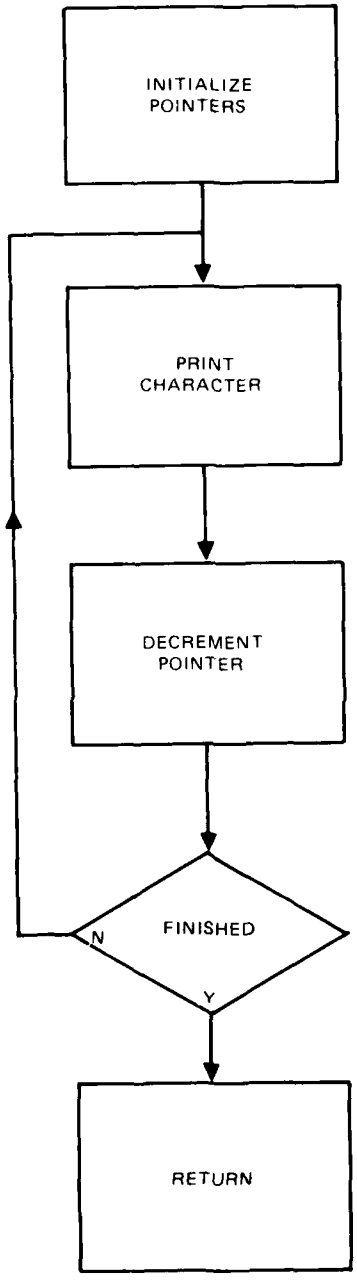


Figure 15. Flow chart for OUT1 program module.

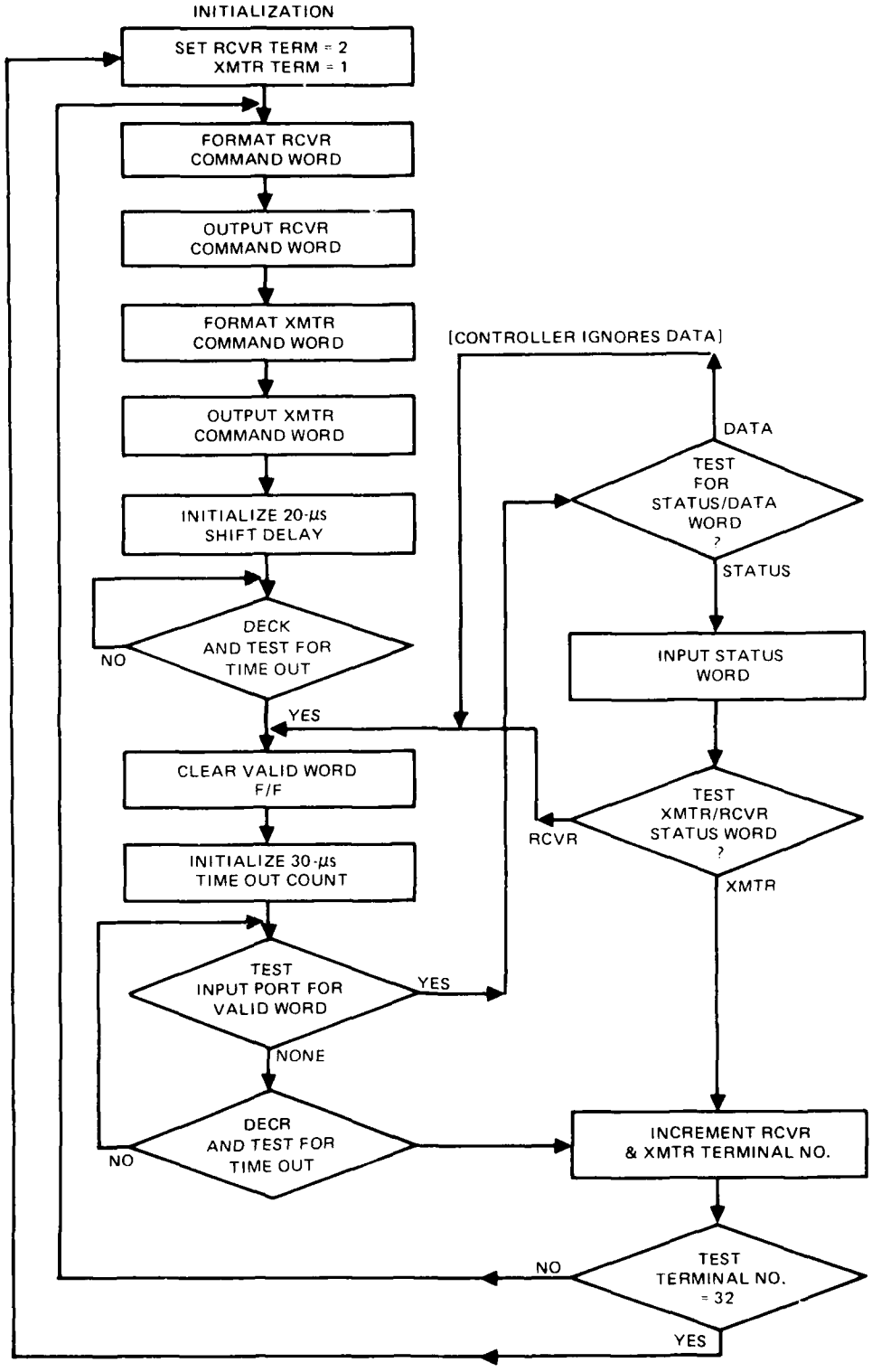


Figure 16. System bus controller program flow chart.

The INSUB2 program module is the same as the INSUB1 program described above in item b, except for some additional instructions to select the terminal to receive the data. When a control T is entered on the keyboard, a message is printed requesting the address of the receiving terminal. The address is checked for errors and stored for use by the main program modules. All messages are sent to the indicated terminal until another control T is typed to change the stored address.

The OUT2 program module is similar to the OUT1 module described in item b, except that a statement is printed preceding the received message that indicates which terminal is transmitting the data.

Figure 17 shows the flow chart for the DBC2 program. Listings for DBC2, INSUB2, and OUT2 are in Appendix C.

b. Discussion

The BIUs were built to test the fiber optic data bus under dynamic bus conditions. The current system was designed to control serial data transfers at a 1-Mbps rate. This system has worked quite well at this data rate, but it cannot be made to work at the 10-Mbps rate. The Harris HD-15530 integrated circuit, which performs most of the interfacing functions, will not operate at more than 4 Mbps. ILC Data Device Corporation has recently announced that early in 1981, it will make available devices to perform these interfacing functions at 10 Mbps. Since the SDK-86 cannot execute instructions in the short times necessary to satisfy the requirements of a 10-Mbps data bus, a dedicated microcomputer board will have to be designed using either a bipolar or an ECL microprocessor. A new microcomputer will require the development of new software. A new microprocessor development system may be needed to facilitate the new design. The microprocessor requirement may be met by American Micro Devices (AMD) AM29116, a 16-bit bipolar device expected to be available in early 1981. Software for programming the AM29116 compatible with our present development system has been promised by the manufacturer. Other options include the 2900 series bit-slice microprocessor and a discrete interface design. These options would require more development time.

VI. LINK-LEVEL TESTS

A. LINK DESCRIPTION AND POWER BUDGET

A link, in the sense used here, includes a fiber optic transmitter, an associated receiver, and anything serving to carry a signal between these two points. This intervening medium is generally lossy and includes connector losses, cable loss, and both the power division and excess losses of a coupler. This is a model for all possible point-to-point connections that might be made through the data bus. The factors determining link effectiveness include the output power from the transmitter, total loss between transmitter and receiver, and receiver sensitivity. The distribution of these gains and losses constitutes a power budget. A graph of possible signal power levels appears in figure 18. The primary link loss in the data bus occurs in the star coupler. The port-to-port loss for a star coupler should, in the ideal sense, be independent of the ports

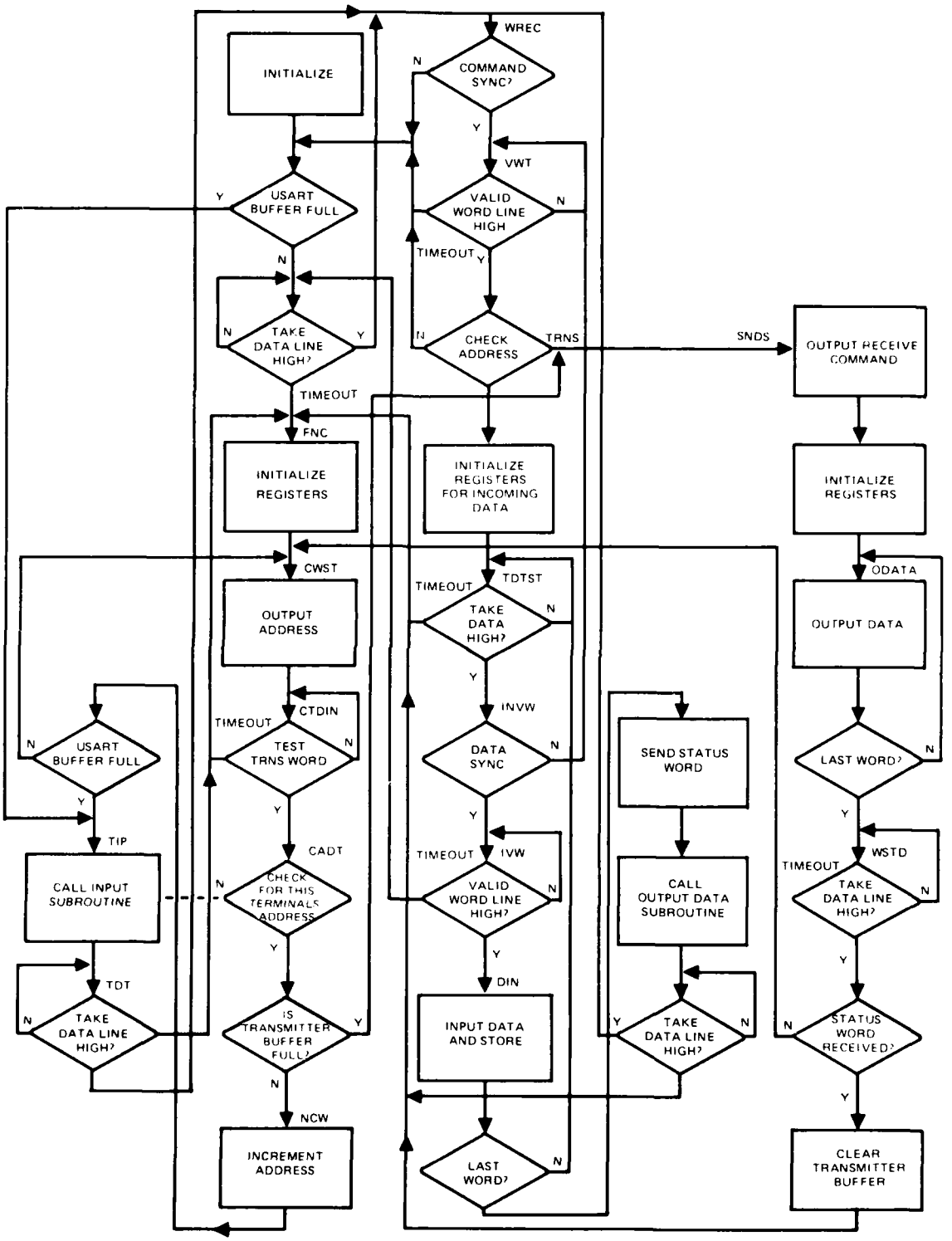


Figure 17. Flow chart for DBC2 program module.

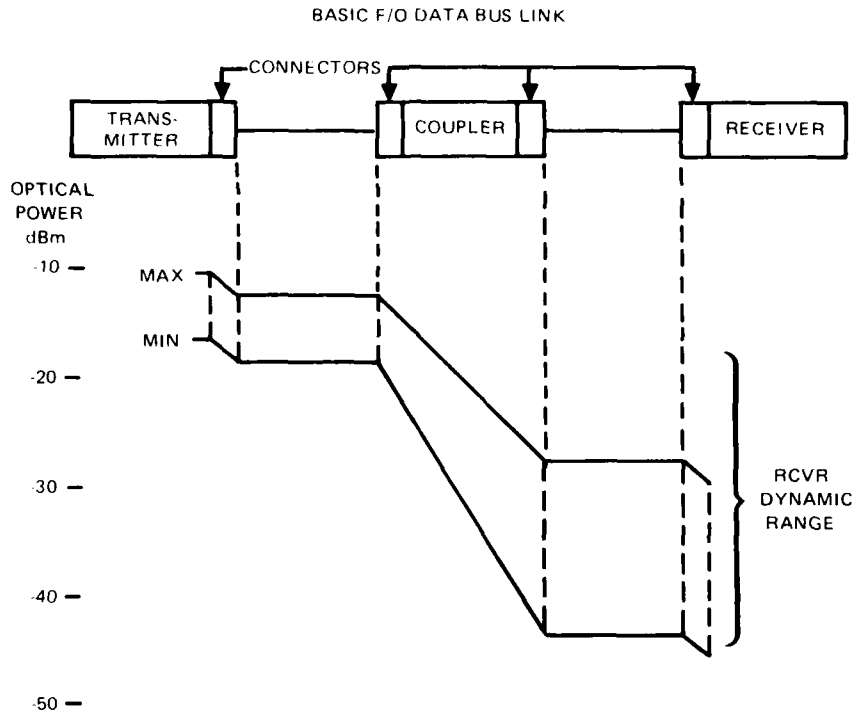


Figure 18. Power budget graph.

chosen; however, evaluation of three actual couplers has indicated differences of 11 to 16 dB. A secondary contributor to link loss variations are the connectors. The total effect of all connectors in a link is no greater than 2 dB for each properly assembled termination. An objective in assessing a power budget is to provide a signal at the receiver of adequate strength to assure a minimum signal quality. The operating signal range for the bus extends from approximately -41 dBm to -16 dBm. The outputs from the various bus transmitters range from -14.6 to -8.2 dBm. Star coupler losses for the Olektron coupler and associated connectors ranged from 14.9 to 25 dB. In the actual data bus there is an additional 4 dB of connector loss which must be added to the coupler loss when considering total link loss.

B. DESCRIPTION OF TESTS

The performance of a simple fiber optic bus link from transmitter input through the star coupler to the receiver output can be evaluated in terms of error rate as measured by a Bit Error Rate Tester (BERT). This permits a relatively simple test procedure to be used and yields a single number for comparison purposes.

The characterization of link performance based on error rate should reflect the operating conditions which yielded the associated test results. An actual description of all the pertinent conditions would be extensive since it requires elaborating on the general specifications of the system under test. Most of these details are fixed, however, and since

they impart little pertinent information, are generally not stated. The salient characteristics are the variables, and of those the most relevant is power, or the change in power. Performance characterization, therefore, is usefully expressed by relating error rate to signal power. This required that a reliable procedure be developed for measuring power and that the assumed fixed parameters do not change.

Problems encountered in the process of developing this test prompted changes in procedures and/or receiver design. Variations in receiver performance, largely a consequence of the use of direct coupling, caused considerable uncertainty in what was to be a fixed parameter. These variations were due to such things as photodiode leakage, power supply rejection, component matching and selection, drift, offsets, and zeroing. These problems have been satisfactorily resolved for a laboratory environment. The measurement and variation of optical signal power was another matter. Although the power available from the cable to the receiver could be measured when the transmitter output was "high," the exact amount reaching the photodiode under signal conditions could not be ascertained. This was found to be due primarily to the alignment of the fiber pigtail in its connector, which produced mating variations. Alignment of the fiber with respect to the photodiode affected unit-to-unit variations. The power level could not be significantly adjusted, readily or reliably. Therefore, only a gross assessment of power could be accomplished, which was inadequate for characterizing performance.

The receiver auto-zero circuit requires that the input signal be a "low" periodically and long enough to allow this circuit to compensate for offset and drift at the limiter output. The timing requirements depend upon signal strengths and time since the last zeroing. An example is 25 μs of "dead" time every 0.65 ms for a 10-μW signal.

Data transmitted over the bus are Manchester encoded and sent in "bursts." Each burst consists of from 1 to 32 "words" of 20 information bits per word. The BERT does not provide output data in this way. A test adapter was constructed based on the Harris Corp. HD-15530 Manchester Encoder-Decoder integrated circuit. This adapter, acting as an interface between the BERT and the fiber optic link, provides the necessary functions so that data can be transmitted in a burst format. The adapter has been used with a Hewlett-Packard model 3780A BERT and a Tau-Tron PTS-107 BERT. A problem with maintaining word synchronization has been observed with both instruments. Synchronization appears to be lost under conditions where it would be sustained if data transmission were continuous. Error rates of from 0.1 to 3.6 x 10^{-9} were indicated when the HP3780A BERT was used. Power levels for these measurements are estimated to have been 100 nW.

C. SUMMARY

The attempt at evaluating link performance emphasized that the simple model was not valid for a receiver operating over a wide range of conditions when the effects of certain combinations of signal parameters degraded performance more than others. These performance limitations, revealed during testing, had to be remedied before proceeding. It was found that evaluation of the receivers requires accurate simulation of data bus signals, that simplified test signals are not adequate to reveal many performance peculiarities. The test signal now used for preliminary evaluations is a gated square wave, and link analysis

is done with pseudorandom data formatted and encoded with a Harris HD-15530. These signals do not provide for changing signal levels of successive bursts. This would be the next level of refinement.

A variable optical signal attenuator would significantly facilitate the acquisition of useful performance data. Once the attenuator is installed in the signal path, none of the optical connectors need be disturbed to take measurements at a variety of power levels. A curve of BER versus attenuation can then be constructed with the accumulated data, and it is a relatively simple matter to establish a reference for an adequate assessment of absolute signal power. Such an attenuator was not available but is on order.

The transmitter design gave no problems, but the choice to utilize direct coupling in the receiver resulted in a significant number. Good performance in overload was substantiated, but associated dc instabilities were difficult to remedy. An alternative approach to the receiver design, such as the one shown in figure 19, should be investigated. This approach was explored in a preliminary fashion using some circuits from the data bus receiver. The resulting receiver is significantly simpler.

Figure 19 is an example of a waveform-dependent approach to the design of the data bus receiver. It is a realization of an approach suggested in "Fiber Optic Stores Interface System Design Analysis Report," November 1979. Vought Corporation, Contract N66001-78-C-0331, by P.M. Cunningham, K.L. Hartfield, and M.R. Posey. Such an approach exploits particular characteristics of the signal waveform unique to the application. In this case the Manchester-encoded NRZ waveform of the MIL-STD-1553 burst transmissions found in the demonstration bus described in this report is used. The circuit following the input modifies the waveform to one having no dc component and equal positive and negative excursions. This signal can be capacitively coupled without significant distortion occurring. Limiting amplifiers can be employed to delay overload. The resulting signal will have certain waveform peculiarities which can be eliminated by the output circuits shown.

VII. SYSTEM-LEVEL TEST

A. GENERAL

The evaluation of system performance is a complex matter involving the capacity of the system to handle information, the delay factors associated with the data communication process, the accuracy or freedom from errors, and the availability of the system to perform its intended function. The demonstration system is a model with five terminals, including the controller. The dynamic operation of the bus involves the interplay between the controller and the terminals and among the terminals themselves. The response of the fiber optic units to varying signal patterns and strengths, of the BIUs to input data rates and patterns, and the overall system to errors in a component part are all factors in the intricate relationship represented by the bus.

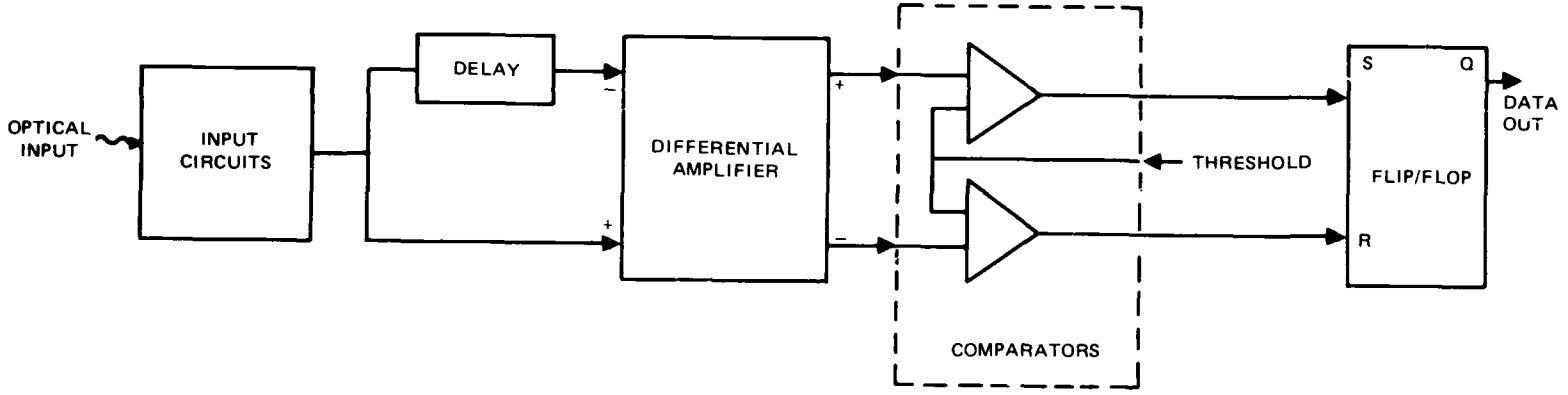


Figure 19. A waveform-dependent approach to delaying receiver overload.

There are many variables, therefore, affecting bus operation. An evaluation based on the determination of all the pertinent variables and assessing the relative importance of each would completely characterize bus operation but would also be an unacceptably lengthy and detailed process. A simpler and more rapid procedure for evaluating performance was required to facilitate comparing the relative performance of various bus configurations, components, procedures, etc. The method chosen, however, had to be capable of producing repeatable results. The BERT is a test instrument which can be used to rapidly measure the quality of a digital link. The BERT provides pseudorandom data to the link being tested, and the output from the link is applied to the same or another, identical, instrument. Input and output patterns are compared and differences (errors) detected. The error rate, the ratio of the number of errors to the total number of data bits transferred, is calculated and displayed. This instrument was chosen as the means for evaluating the data bus. The test results must not be interpreted on an absolute basis, because a direct comparison with any other system would not be valid. Operational differences between systems, especially, contribute to the lack of validity. The definition of an error, for example, can vary from one system to another.

B. TEST DESCRIPTION

The interconnection of the system components for the system-level test is shown in figure 20. The single-fiber bus system was evaluated using a Hewlett-Packard model 3780A BERT. The 3780A was not designed specifically for a burst measurement capability, but this function can be realized by controlling clock signals provided to the instrument. The bus terminals were interconnected via a wire bus in the process of working out the problems associated with interfacing the BERT to the bus. When satisfactory operation was obtained, the indicated error rate was 2×10^{-8}. The wire bus was then replaced by the fiber optic bus. The teletype and video terminals were set up to transmit whenever the bus was offered to them to better simulate an operational bus.

Continuous error rate testing was carried out in the laboratory for about 1 month. Data were transmitted in burst fashion in blocks of 512 bits. Approximately 20 hours were required to accumulate 10^{10} bits.

C. TEST RESULTS

The system often operated for hours without a single error. Occasionally loss of synchronization was observed. The following ten readings were typical of the measured error rates for a test length of 10^{10} bits each.

1. 0.0×10^{-9}
2. 0.1×10^{-9}
3. 0.6×10^{-9}
4. 2.3×10^{-9}
5. 2.4×10^{-9}
6. 3.9×10^{-9}

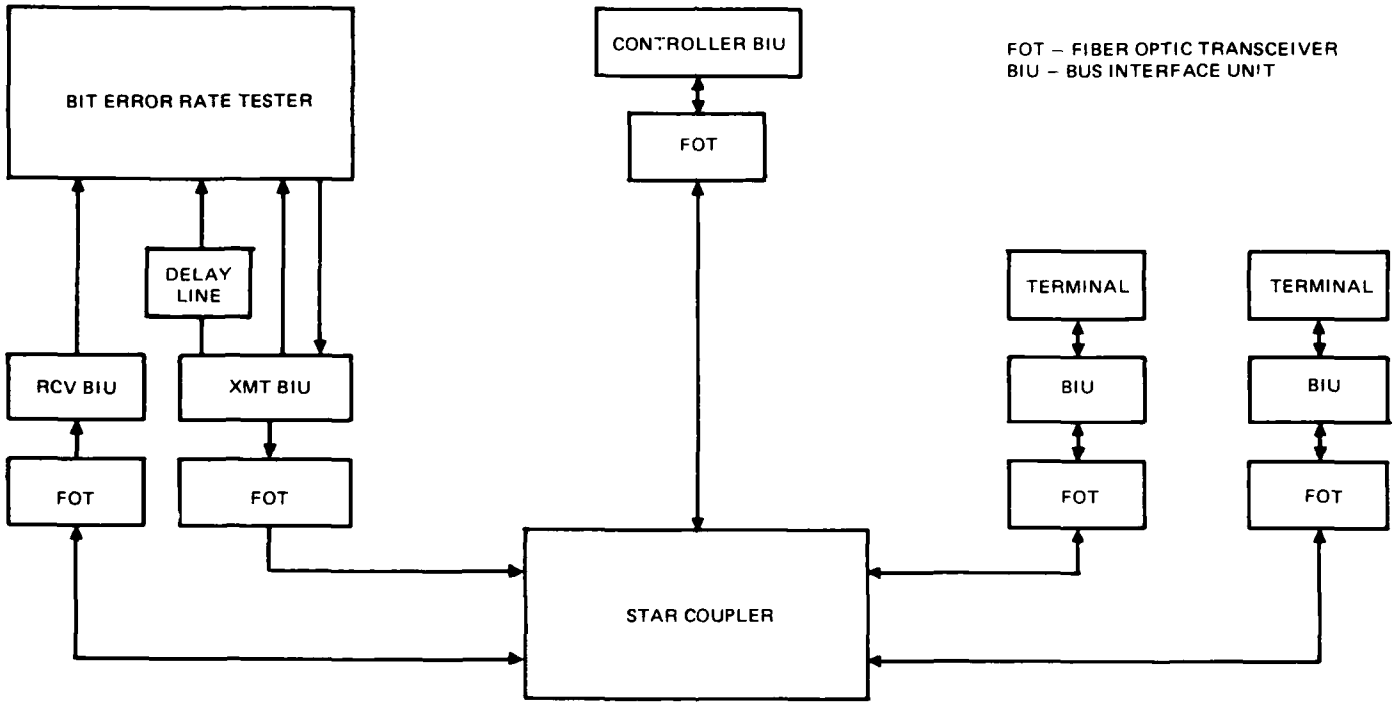


Figure 20. Single-fiber bus system evaluation configuration.

7. 4.1×10^{-9}

8. 6.8×10^{-9}

9. 9.0×10^{-9}

10. 1.3×10^{-8}

These readings do not indicate when the errors occurred. A number of tests of 10 minutes duration were run. These tests showed the errors to occur in bursts. The data indicate that the majority of errors occurred during the daytime. The system was virtually error-free at night. These results indicate that errors may have been caused by power line transients. Only minimal precautions were taken to protect against interference from this source.

The tests demonstrated the ability of the data bus system to accommodate terminals at low, medium, and high data rates. The teletypewriter operates at 110 bps, the data terminal at 4800 bps, and the BERT at the maximum bus rate of 1 Mbps.

VIII. SUMMARY AND CONCLUSIONS

An FY78 system analysis and feasibility study identified a baseline fiber optic data bus design for a tactical Marine Corps Command-Control system application. During FY79 fiber optic data bus components necessary to implement this baseline system were identified, secured, and evaluated. These components included fiber optic transmitters, fiber optic receivers, star couplers, fiber optic connectors, fiber cable, and a microprocessor to perform the bus-interface-unit function. Problems associated with the use of each component were identified.

During FY80 a five-terminal data bus operating at a clock rate of 1 Mbps was built, tested, and evaluated using state-of-the-art fiber optic components. The laboratory data bus utilized a passive 16- x 16-port transmissive star coupler to interconnect typical equipment used in a tactical Marine Corps shelter system. Data bus operation was demonstrated with both a central and a distributed bus controller. Testing of terminal-to-terminal data transfer over the operational data bus showed bit error rates between 1 error in 10^8 and 0 errors in 10^9 bits.

IX. RECOMMENDATIONS

The primary goal of this multi-year effort has been to identify problems and reduce the risk associated with the development of a tactical Marine Corps Command-Control data bus for the post 1980 era. It is recommended that the fiber optic component requirements be transitioned into the Manufacturing Technology Program, where fully compliant MIL-SPEC components will be developed. The Manufacturing Technology Program is intended to bridge the gap between R&D and production and ultimately reduce acquisition costs of defense procurements.

It is further recommended that additional efforts be initiated in the following related areas:

- Develop a 20-Mbps fiber optic data bus receiver.
- Develop an active repeater for use in cascading transmissive star couplers as a means of interconnecting buses in multiple-shelter applications.
- Develop a high-speed bus interface unit to accommodate a 20-Mbps transmission data rate.
- Investigate and implement alternate fail-safe data bus distributed control protocols.
- Develop and demonstrate a digital voice terminal interface to the fiber optic data bus.
- Develop a fail-safe active fiber optic T-coupler to permit utilization of multidrop architectures beyond limitations imposed by present T-coupler technology.

The fiber optic data bus test bed established in FY79 and FY80 allows many of the follow-on efforts listed above to be accomplished with minimum additional costs.

APPENDIX A

STAR COUPLER INSERTION LOSS TEST DATA

Table A-1. Insertion loss data (dB) for Olektron Corp. star coupler.

Input Ports \ Output Ports	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	20.3	21.2	21.0	16.6	19.5	20.0	23.0	18.0	20.8	20.8	21.5	18.4	21.1	20.8	16.3	18.0
2	21.0	19.9	23.3	18.4	20.2	17.8	21.4	19.8	21.1	19.6	21.5	18.5	23.0	19.8	16.7	16.7
3	21.9	22.5	22.0	17.6	20.1	19.4	18.5	17.6	22.1	21.6	22.3	18.4	22.2	21.1	16.5	17.0
4	21.0	20.0	23.5	20.0	21.3	17.1	21.3	21.3	18.3	18.2	20.2	19.5	23.0	20.4	16.8	16.9
5	22.1	15.9	22.2	21.1	17.6	17.9	19.0	16.6	14.9	20.8	22.7	23.4	22.4	18.4	21.3	18.0
6	19.8	19.4	23.5	21.0	21.7	17.3	21.5	21.0	17.3	17.0	18.4	20.9	22.1	20.6	17.9	16.9
7	18.6	18.1	19.8	17.6	21.4	21.7	17.6	22.3	19.8	21.1	20.3	19.6	18.3	21.4	19.3	20.5
8	21.4	16.5	24.7	17.6	17.5	20.5	18.7	16.3	17.3	19.6	20.4	22.2	24.0	19.6	20.7	19.5
9	18.3	17.9	24.6	22.2	16.3	22.5	23.2	15.2	17.4	20.6	20.6	19.5	22.0	18.6	17.5	21.5
10	20.4	17.1	24.9	19.6	15.1	22.3	20.9	15.4	15.9	18.0	17.3	20.4	23.8	19.0	19.4	20.8
11	19.1	21.0	22.8	22.9	21.5	18.0	22.2	22.0	22.4	18.2	18.1	23.4	21.2	23.4	20.8	18.5
12	20.2	16.7	20.0	21.9	16.9	19.9	22.3	16.5	16.8	20.2	22.7	21.5	18.5	16.2	19.4	19.5
13	17.8	21.4	19.6	20.4	18.1	17.6	19.4	19.9	23.3	17.5	16.9	22.0	17.9	23.3	20.9	19.5
14	21.3	18.8	18.5	17.4	21.5	21.5	16.8	22.9	21.4	22.4	21.3	18.4	18.9	23.9	18.3	20.5
15	19.3	23.5	19.4	19.5	25.0	21.3	18.2	22.8	22.7	21.2	19.3	20.6	17.4	18.5	20.6	21.4
16	17.0	21.0	18.6	18.9	19.2	18.4	17.9	18.8	20.6	16.9	16.4	20.6	17.5	18.9	20.0	19.7

Table A-2. Insertion loss data (dB) for ITT Corp. star coupler.

Input Ports \ Output Ports	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1	14.9	21.1	20.2	19.5	20.0	20.4	21.1	21.0	21.0	21.3	22.4	21.9	20.5	20.9	21.8	22.2	20.8	21.0	22.6
2	19.8	13.8	19.3	18.7	19.7	19.5	20.2	21.2	18.1	19.0	19.8	19.8	18.5	18.9	19.8	19.5	19.0	18.9	22.5
3	19.2	18.8	13.2	17.5	17.6	18.7	19.2	19.6	18.1	18.2	18.9	18.6	17.3	18.1	19.5	18.8	18.0	18.1	19.6
4	19.5	19.0	18.9	12.6	17.8	18.8	19.0	19.7	18.1	18.0	19.1	19.2	17.7	18.3	19.3	18.6	18.3	18.8	19.9
5	19.7	20.1	19.2	18.4	19.1	19.6	20.2	20.1	19.0	19.0	19.7	19.7	18.3	19.3	19.5	19.0	18.9	19.4	20.4
6	22.9	22.2	22.0	21.1	23.0	19.4	22.5	22.7	23.7	22.8	26.9	22.3	21.7	21.9	22.7	22.5	22.4	22.6	24.3
7	19.9	19.5	19.1	17.8	18.7	19.3	13.8	19.6	19.2	19.0	19.2	19.1	18.5	18.4	19.0	18.6	18.4	19.1	20.0
8	18.9	18.7	18.1	17.1	18.5	18.6	18.9	13.7	18.7	17.7	18.5	18.7	17.5	17.8	18.7	18.0	18.2	18.5	19.7
9	20.1	19.6	19.0	18.4	18.9	19.7	19.7	19.2	14.2	19.4	19.5	19.6	18.7	18.6	19.2	19.0	18.6	19.2	20.1
10	19.8	19.6	18.8	18.1	19.1	19.5	19.8	19.5	19.6	14.0	19.3	19.4	18.0	18.7	19.6	19.2	18.8	19.5	20.5
11	20.0	19.6	18.8	18.6	18.4	19.6	19.7	19.7	19.7	19.5	13.8	19.2	18.2	18.9	19.1	18.7	18.7	19.5	20.2
12	21.6	21.4	20.8	20.5	20.5	21.6	21.5	21.5	21.1	20.7	21.2	14.5	20.1	20.5	21.4	20.7	20.8	21.2	22.9
13	19.3	19.0	18.8	17.6	18.3	18.7	19.1	19.0	18.8	18.8	19.1	19.1	12.2	18.0	19.2	18.1	17.7	18.7	19.5
14	20.6	20.2	19.7	18.7	19.6	19.9	20.8	20.2	19.8	20.3	20.3	19.6	19.0	13.1	19.7	19.6	19.2	19.6	20.6
15	20.2	19.8	19.5	18.6	19.5	19.8	20.2	20.4	20.2	20.0	20.8	19.6	18.6	19.1	14.0	19.1	19.6	19.5	21.0
16	19.0	18.5	18.1	17.1	18.2	18.2	18.8	19.1	18.9	18.5	18.5	18.5	17.7	17.6	18.4	12.6	17.7	17.8	19.5
17	18.8	18.4	17.9	17.0	18.0	18.0	18.5	18.4	18.5	18.7	18.4	18.1	16.9	17.7	18.3	17.5	12.1	17.6	19.0
18	20.1	20.1	19.7	18.7	19.6	19.8	20.4	20.4	20.1	19.9	19.8	20.6	18.8	19.1	20.1	19.7	19.3	13.3	21.7
19	19.6	21.5	18.9	18.0	18.3	19.5	19.8	20.2	18.8	18.5	25.8	19.4	18.0	18.6	19.6	26.4	18.6	19.2	13.9

APPENDIX B

BIU INPUT/OUTPUT SCHEMATICS

HD-15530 ENCODER/DECODER

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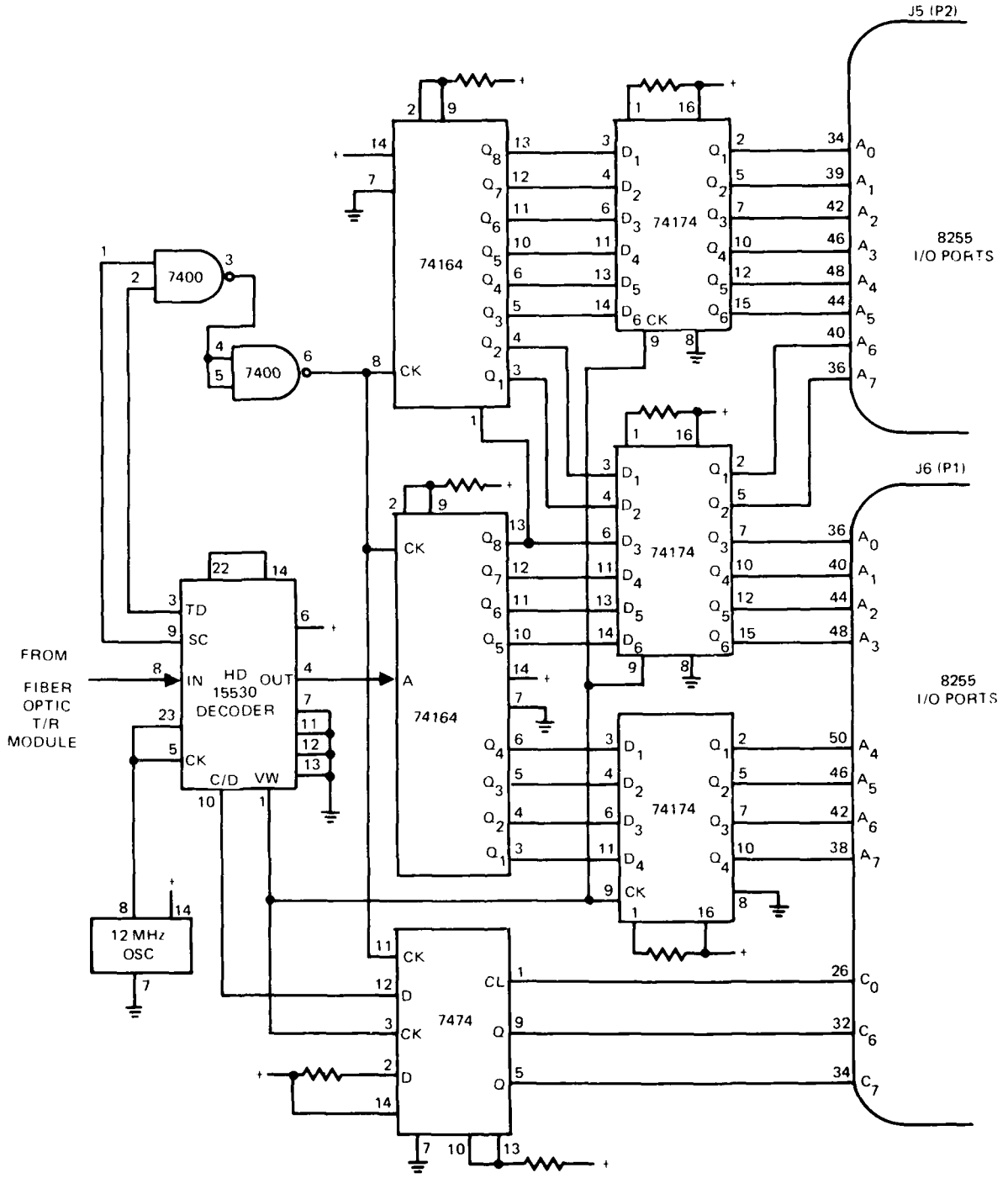


Figure B-1. Schematic of BIU data input circuit.

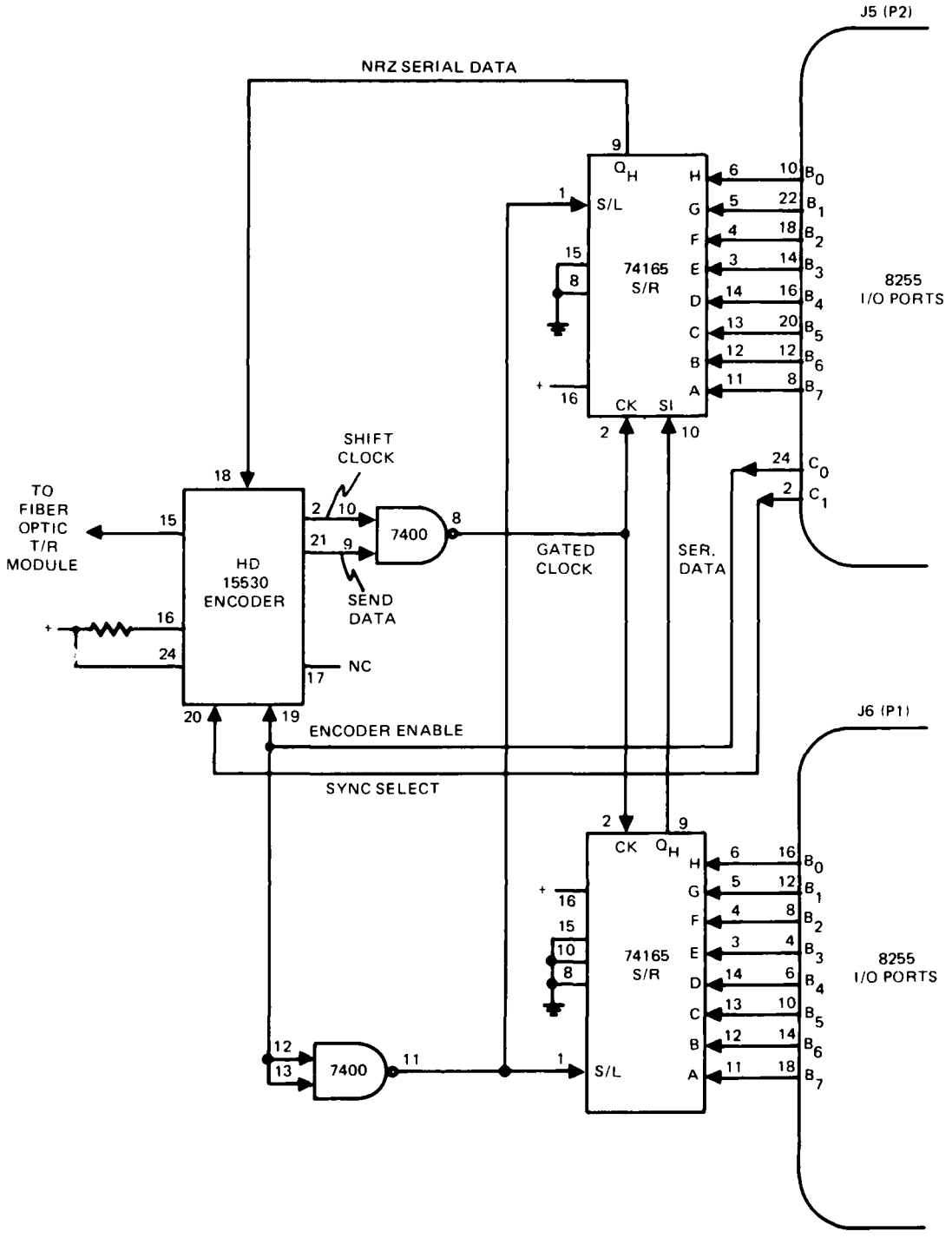


Figure B-2. Schematic of BIU data output circuit.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-15530

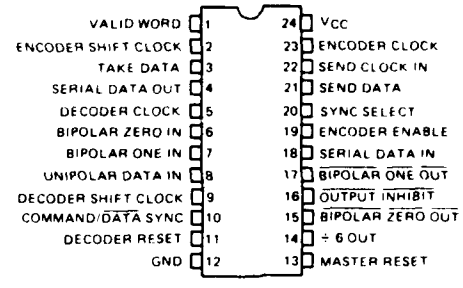
CMOS Manchester Encoder-Decoder

APRIL 1978

Features

- SUPPORT OF MIL-STD-1553
- 1.25 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE

Pinout



Description

The Harris HD-15530 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset function.

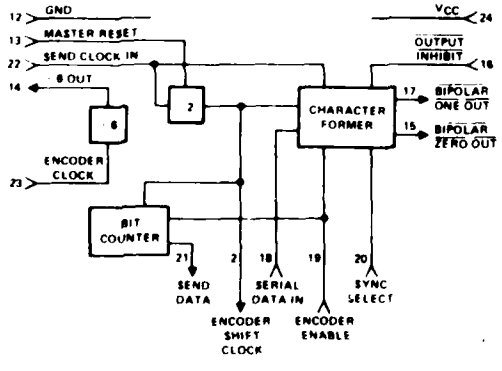
This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

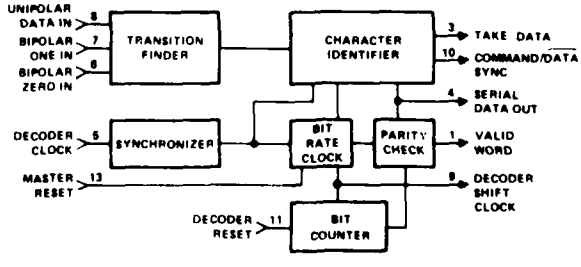
The HD-15530 could also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable or fiber optic cable throughout the building.

Block Diagrams

ENCODER



DECODER



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APPENDIX C

PROGRAM MODULE LISTINGS

```
MCS-86 ASSEMBLER     PT1


ISIS-II MCS-86 ASSEMBLER V1.0 ASSEMBLY OF MODULE PT1
OBJECT MODULE PLACED IN  F1 PT1 OBJ
ASSEMBLER INVOKED BY:  ASM86  F1 PT1.ASM DB EP

LOC  OBJ                      LINE    SOURCE

                                 1            ;UPDATE 1: DEL 79
                                 2;
----                             3    STACK_SEG       SEGMENT
                                 4            ASSUME NOTHING
0000 [20                         5            DW      20 DUP(?)
      ????
     ]
0028                             6    STACK_TOP       LABEL   WORD
----                             7    STACK_SEG       ENDS
----                             8    RTDATA  SEGMENT COMMON
                                 9            ASSUME NOTHING
0000 [52                        10    TDATA   DW      52 DUP(0)
      0000
     ]
0068 [52                        11    RDATA   DW      52 DUP(0)
      0000
     ]
00D0 ????                       12    BVOL    DW      ?
00D2 1E00                       13    CLMS    DW      30
----                            14    RTDATA  ENDS
                                15
                                16
----                            17    RTPROG  SEGMENT PUBLIC

                                18
                                19            ASSUME  CS:RTPROG, DS:RTDATA, SS:STACK_SE
  FFF8                          20    INPORT  EQU     0FFF8H
                                21
  FFFA                          22    OUTPORT EQU     0FFFAH
  FFFE                          23    CONPORT EQU     0FFFEH
  FFFD                          24    CTLO    EQU     0FFFDH
  FFFC                          25    COMND   EQU     0FFFCH
  FFFB                          26    SPORT   EQU     0FFFBH
                                27
  0002                          28    RXRDY   EQU     2H
  0007                          29    STATUS_1        EQU     7
  0001                          30    DATA_OUT_1      EQU     1
                                31
                                32    EXTRN   OUTPUT_DATA1     NEAR
                                33    EXTRN   INPUT_DATA1      NEAR
                                34
0000 B8----           R         35    START   MOV     AX,RTDATA
0003 8ED8                       36            MOV     DS,AX   ;INITIALIZE DATA SEGMENT
0005 B8----           R         37            MOV     AX,STACK_SEG
0008 8ED0                       38            MOV     SS,AX
000A BC2800                     39            MOV     SP,OFFSET STACK_TOP
000D C706D20064100              40            MOV     CLMS,100        ;SET COLUMN WIDTH
0013 B84600                     41            MOV     AX, 70
0016 2906D200                   42            SUB     CLMS,AX
001A C706D0000C500              43            MOV     BVOL,101
```

```
MCS-86 ASSEMBLER    PT1


LOC  OBJ                  LINE   SOURCE

                            44           ;INITIALIZE USART
0020 BAF2FF                 45           MOV     DX,0FFF2H       ;USART CONTROL ADD
0023 B065                   46           MOV     AL,65H  ;RESET
0025 EE                     47           OUT     DX,AL
0026 90                     48           NOP
0027 B025                   49           MOV     AL,25H  ;CMD
0029 EE                     50           OUT     DX,AL
002A 90                     51           NOP
002B B065                   52           MOV     AL,65H  ;RESET
002D EE                     53           OUT     DX,AL
002E 90                     54           NOP
002F B0CF                   55           MOV     AL,0CFH ;MODE SET
0031 EE                     56           OUT     DX,AL
0032 90                     57           NOP
0033 B025                   58           MOV     AL,25H  ;CMD SET
0035 EE                     59           OUT     DX,AL
0036 B0FF                   60           MOV     AL,0FFH ;USART SETTLING DELAY
0038 B178                   61           MOV     CL,78H
003A D2E9                   62   SDELAY  SHR     CL,CL
003C 90                     63           NOP
003D FEC8                   64           DEC     AL
003F 75F9                   65           JNZ     SDELAY
0041 BAFEFF                 66           MOV     DX,CONPORT      ;CONTROL PORT ADD
0044 B89998                 67           MOV     AX,9899H        ;CONTROL WORD
0047 EF                     68           OUT     DX,AX   ;INITIALIZE PORTS
0048 BAFCFF                 69           MOV     DX,C2ADD
004B EC                     70           IN      AL,DX   ;INPUT TERMINAL ADDRESSES
004C 8AD8                   71           MOV     BL,AL   ;REC ADDS
004E 8AF8                   72           MOV     BH,AL   ;TRNS ADDS
0050 81E30FF0               73           AND     BX,0F00FH       ;MASK UNWANTED BI
0054 F9                     74           STC
0055 B105                   75           MOV     CL,5H
0057 D2D7                   76           RCL     BH,CL   ;ROTORATE TO PROPER POSITI
0059 F9                     77           STC
005A D0D7                   78           RCL     BH,1
005C F8                     79           CLC
005D D0DC                   80           RCL     BL,1
005F BAFDFF                 81   IPTEST  MOV     DX,C1IO
0062 EC                     82           IN      AL,DX   ;INPUT HAND SHAKE LINE
0063 2430                   83           AND     AL,30H  ;MASK
0065 3C30                   84           CMP     AL,30H  ;TEST FOR TD AND CMD TRUE
0067 7414                   85           JE      SHORT   VWTEST
0069 BAF2FF                 86           MOV     DX,SPORT
006C EC                     87           IN      AL,DX   ;INPUT SERIAL PORT
                            88                           ;STATUS WORD
006D A802                   89           TEST    AL,RXRDY        ;CHECK FOR
                            90                           ;FULL BUFFER
006F 74EE                   91           JZ      IPTEST
0071 833ED00065             92           CMP     BVOL,101
0076 75E7                   93           JNE     IPTEST
0078 E80000         E       94           CALL    INPUT_DATA1
007B EBE2                   95           JMP     IPTEST
007D EC                     96   VWTEST  IN      AL,DX
007E D0E0                   97           SHL     AL,1
0080 72FB                   98           JNB     VWTEST
```

```
MCS-86 ASSEMBLER    PT1


LOC  OBJ                  LINE   SOURCE

0082 BAF8FF                 99   CMDIN   MOV     DX,INPORT       ;INPUT ADDS
0085 ED                    100           IN      AX,DX    ;INPUT CMD WORD
0086 24 1F                 101           AND     AL,1FH
0088 3A [                  102           CMP     AL,BL    ;CHECK ADDS
008A 74 [                  103           JZ      RCV      ;IF CORRECT JUMP
008C 3A07                  104           CMP     AL,BH    ;CHECK FOR TRNS ADDS
008E 750F                  105           JNE     IPTEST
0090 833E0000065           106           CMP     BVOL,101        ;CHECK FOR FULL B
0095 7408                  107           JE      IPTEST
                           108
0097 8AC7                  109   SNDST   MOV     AL,BH    ;PUT STATUS WORD IN ACC
0099 241F                  110           AND     AL,1FH   ;DELETE TRNS BIT
009B FEC0                  111           INC     AL       ;SET RCV ADDS
009D BAFAFF                112           MOV     DX,OUTPORT
00A0 EF                    113           OUT     DX,AX    ;OUTPUT STATUS WORD
00A1 BAFDFF                114           MOV     DX,C11D
00A4 B002                  115           MOV     AL,STATUS_1
00A6 EE                    116           OUT     DX,AL    ;SET ENCODER ENABLE
00A7 FEC8                  117           DEC     AL
00A9 EE                    118           OUT     DX,AL    ;RESET ENABLE
00AA BF6400                119           MOV     DI,100   ;SET DATA INDEX
00AD BAFAFF                120   DOUT    MOV     DX,OUTPORT      ;OUTPUT PORT ADDS
00B0 8B05                  121           MOV     AX,[DATA[DI]
00B2 EF                    122           OUT     DX,AX
00B3 B90600                123           MOV     CX,6     ;SET DELAY
00B6 E2FE                  124   NEXT    LOOP    NEXT     ;DELAY
00B8 BAFDFF                125           MOV     DX,C11D
00BB B001                  126           MOV     AL,DATA_OUT_1
                           127
                           128                   ;SET DATA ENCODER ENABLE
00BD EE                    129           OUT     DX,AL
00BE FEC8                  130           DEC     AL
00C0 EE                    131           OUT     DX,AL    ;RESET DATA ENCODER ENABLE
00C1 4F                    132           DEC     DI
00C2 4F                    133           DEC     DI
00C3 [B3E[000              134           CMP     DI,BVOL
00C7 72E4                  135           JAE     DOUT     ;GET MORE DATA
00C9 BAFDFF                136           MOV     DX,C11D
00CC EC                    137   IN1     IN      AL,DX
00CD 2430                  138           AND     AL,30H
00CF 3C30                  139           CMP     AL,30H
00D1 75F9                  140           JNE     IN1
00D3 EC                    141   IN2     IN      AL,DX
00D4 D0E0                  142           SHL     AL,1
00D6 72FB                  143           JNB     IN2
00D8 BAF8FF                144           MOV     DX,INPORT
00DB EC                    145           IN      AL,DX
00DC 3AC7                  146           CMP     AL,BH
00DE 754D                  147           JNE     JUMP
00E0 C706[0006500          148           MOV     BVOL,101        ;RESET BUFFER
00E6 E976FF                149           JMP     IPTEST
00E9 BF6400                150   RCV     MOV     DI,100
00EC BAFDFF                151   DIN1    MOV     DX,C11D ;SET IO LINE
00EF EC                    152           IN      AL,DX
00F0 A810                  153           TEST    AL,10H
```

```
MCS-86 ASSEMBLER     RT1


LOC  OBJ                  LINE   SOURCE

                           154            JZ      DIN1
00F2 74F8                  155    DIN2    IN      AL,DX    ;INPUT VALID WORD LINE
00F4 EC                    156            SHL     AL,1     ;
00F5 D0E0                  157            JNB     DIN2
00F7 72FB                  158            SHL     AL,1
00F9 D0E0                  159            JB      CMDIN
00FB 7285                  160            MOV     DX,INPORT
00FD BAF8FF                161    INPUT   IN      AX,DX    ;INPUT DATA
0100 FD                    162            MOV PDATA[DI],AX        ;STORE DATA
0101 894568                163            CMP     AL,0AH
0104 3C0A                  164            JZ      SHORT   SEND
0106 740B                  165            CMP     AH,0AH
0108 80FC0A                166            JZ      SHORT   SEND1
010B 7405                  167            SUB     DI,2
010D 83EF02                168            JMP     DIN1    ;GET MORE DATA IF NEEDED
0110 EBDA                  169    SEND1   INC     DI
0112 47                    170    SEND    MOV     DX,OUTPORT
0113 BAFAFF                171            MOV     AL,BL
0116 8AC3                  172            OR      AL,20H
0118 0C20                  173            DEC     AL
011A FEC8                  174            XOR     AH,AH
011C 72E1                  175            OUT     DX,AX    ;SEND STATUS WORD
011E EF                    176            MOV     DX,C11O
011F BAFCFF                177            MOV     AL,STATUS_1
0122 B003                  178            OUT     DX,AL    ;ENABLE ENCODER
0124 FE                    179            DEC     AL
0125 FEC8                  180            OUT     DX,AL    ;RESET ENABLE LINE
0127 EE                    181            MOV     SI,DI
0128 8BF7                  182            CALL    OUTPUT_DATA1    ;OUTPUT DATA
012A E800000          E    183    JUMP    JMP     IPTEST   ;START OVER
012D E92FFF                184    PTPROG  ENDS
----                       185            END     START
  0000
```

```
ISIS-II MCS-86 ASSEMBLER V1.0 ASSEMBLY OF MODULE INSUB1
OBJECT MODULE PLACED IN :F1:INSUB1.OBJ
ASSEMBLER INVOKED BY: ASM86 :F1:INSUB1.ASM DB EP

LOC  OBJ                  LINE   SOURCE

                             1          ;UPDATE 12 DEC 79
                             2
                             3   PUBLIC  INPUT_DATA1
                             4   RTDATA  SEGMENT COMMON
0000 [104                    5   DATA    DB      104 DUP(0)
     00
     ]
0068 [52                     6           DW      52 DUP(?)
     ????
     ]
0000 ????                    7   BVOL    DW      ?
0002 ????                    8   CLMS    DW      ?
----                         9   RTDATA  ENDS
                            10
                            11
----                        12   RTPROG  SEGMENT PUBLIC
                            13           ASSUME  CS:RTPROG, DS:RTDATA
                            14
  0018                      15   CONX    EQU     18H
  0012                      16   CONR    EQU     12H
  000A                      17   LF      EQU     0AH
  007F                      18   RUB_OUT EQU     7FH
                            19
0000                        20   INPUT_DATA1     PROC
0000 53                     21           PUSH    BX
0001 BF6500                 22   START   MOV     DI,101
                            23
0004 C605000                24           MOV     DATA[DI],0      ;CLEAR BYTE
0007 B90800                 25   INDATA  MOV     CX,308H
000A FED1                   26           CALL    CX
000C 3C7F                   27           CMP     AL,RUB_OUT
000E 741B                   28           JZ      SHORT   ERROR
0010 3C18                   29           CMP     AL,CONX
0012 7430                   30           JE      SHORT   DLINE   ;DELETE LINE
0014 3C12                   31           CMP     AL,CONR
0016 7430                   32           JE      SHORT   RLINE   ;REPRINT LINE
0018 3C0A                   33           CMP     AL,0AH  ;CHECK FOR LINE FEED
001A 74ER                   34           JE      INDATA  ;DON'T STORE LF
001C 8805                   35   STORE   MOV     DATA[DI],AL
001E 3C0D                   36           CMP     AL,0DH  ;CHECK FOR CR
0020 744D                   37           JZ      CR_LF   ;IF CR PRINT CR LF
0022 3BBED200               38           CMP     DI,CLMS ;CHECK FOR FULL BUFFER
0026 7443                   39           JE      BFULL
0028 4F                     40           DEC     DI
0029 EBDC                   41           JMP     INDATA
002B 83FF65                 42   ERROR   CMP     DI,101
002E 74D1                   43           JE      START
0030 47                     44           INC     DI
0031 BAF2FF                 45           MOV     DX,0FFF2H
```

```
MCS-86 ASSEMBLER     INSUB1


LOC  OBJ                  LINE   SOURCE

                            46   CHECK:   IN      AL,DX
                            47            TEST    AL,1H
                            48            JZ      CHECK
                            49
                            50            MOV     DX,0FFF0H
                            51            MOV     AL,DATA[DI]
                            52            OUT     DX,AL
                            53            JMP     INDATA
                            54   DLINE    MOV     CX,492H
                            55            CALL    CX          ;CR LF SUBROUTINE
                            56            JMP     START
                            57   RLINE    MOV     CX,492H
                            58            CALL    CX          ;CR LF SUBROUTINE
                            59            MOV     BVOL, DI
                            60            MOV     DI,101   ;INITIALICE POINTER
                            61   CHK:     MOV     DX,0FFF2H
                            62            IN      AL,DX
                            63            TEST    AL,1H
                            64            JZ      CHK
                            65            MOV     DX,0FFF0H
                            66            MOV     AL,DATA[DI]
                            67            OUT     DX,AL
                            68            DEC     DI
                            69            CMP     DI,BVOL
                            70            JA      CHK
                            71            JMP     INDATA
                            72
                            73
0068 4F                     74   BFULL    DEC     DI
0069 C60500                 75            MOV     DATA[DI],0DH
006C B89204                 76   CR_LF    MOV     CX,492H
006F FFD1                   77            CALL    CX
0071 4F                     78            DEC     DI
0072 C60500A                79            MOV     DATA[DI],0AH
                            80
0075 F7C70100               81            TEST    DI,1
0079 7401                   82            JZ      SHORT   EVEN
007B 4F                     83            DEC     DI
007C 893E0000               84   EVEN     MOV     BVOL,DI
0080 5B                     85            POP     BX
0081 C3                     86            RET
                            87   INPUT_DATA1      ENDP
                            88   RTPPOG   ENDS
                            89            END

----
```

```
MCS-86 ASSEMBLER    OUT1


ISIS-II MCS-86 ASSEMBLER V1.0 ASSEMBLY OF MODULE OUT1
OBJECT MODULE PLACED IN  F1 OUT1 OBJ
ASSEMBLER INVOKED BY: ASM86  F1 OUT1 ASM DB EP

LOC  OBJ                    LINE    SOURCE

                               1            ;UPDATE 13 DEC 79
                               2
                               3            PUBLIC  OUTPUT_DATA1
----                           4    RTDATA  SEGMENT COMMON
0000 (104                      5            DB      104 DUP(?)
     ??
     )
0068 (104                      6    DATA    DB      104 DUP(?)
     ??
     )
00D0 ????                      7    BVOL    DW      ?
00D2 4600                      8    CLMS    DW      70
----                           9    RTDATA  ENDS
----                          10    RTPROG  SEGMENT PUBLIC
                              11            ASSUME  CS:RTPROG,      DS:RTDATA
                              12
0000                          13    OUTPUT_DATA1    PROC    NEAR
                              14
                              15
0000 4E                       16    START   DEC     SI
0001 BF6500                   17            MOV     DI,101  ;SET POINTER
0004 BAF2FF                   18    CHECK   MOV     DX,0FFF2H       ;SET DATA READY AD
0007 EC                       19            IN      AL,DX   ;INPUT DATA READY LINE
0008 A801                     20            TEST    AL,1H   ;TEST DATA READY LINE
000A 74F8                     21            JZ      CHECK
000C BAF0FF                   22            MOV     DX,0FFF0H       ;SET OUTPUT ADDS
000F 8A4568                   23            MOV     AL,BYTE PTR DATA[DI]    ;OUTPUT DA
0012 EE                       24            OUT     DX,AL   ;OUTPUT DATA
0013 4F                       25            DEC     DI
0014 3BFE                     26            CMP     DI,SI
0016 75EC                     27            JNZ     CHECK
0018 C3                       28            RET
                              29    OUTPUT_DATA1    ENDP
----                          30    RTPROG  ENDS
                              31            END
```

```
MCS-86 ASSEMBLER    DBC2


ISIS-II MCS-86 ASSEMBLER V1.0 ASSEMBLY OF MODULE DBC2
OBJECT MODULE PLACED IN  F4:DBC2.OBJ
ASSEMBLER INVOKED BY:  ASM86  F4:DBC2.ASM DB EP

LOC  OBJ                    LINE   SOURCE

                               1           $UPDATE  1 JUNE 1980
                               2
----                           3   STACK_SEG       SEGMENT
                               4           ASSUME NOTHING
0000 (20                       5           DW      20 DUP(?)
     ????
     )
0028                           6   STACK_TOP       LABEL   WORD
----                           7   STACK_SEG       ENDS
                               8
----                           9   RTCDATA SEGMENT COMMON
                              10
                              11           ASSUME  NOTHING
                              12
0000 (32                      13   TDATA   DW      32 DUP(?)
     ????
     )
0040 (32                      14   RDATA   DW      32 DUP(?)
     ????
     )
0080 ????                     15   RCMD    DW      ?
0082 ????                     16   BVOL    DW      ?
0084 ????                     17   CADDS   DW      ?
                              18
----                          19   RTCDATA ENDS
                              20
----                          21   RTCPROG SEGMENT WORD PUBLIC
                              22   EXTRN   TRED BYTE
                              23           ASSUME  CS:RTCPROG, DS:RTCDATA, SS:STACK_
                              24           ASSUME  ES:SEG TRED
                              25
  FFF8                        26   INPORT  EQU     0FFF8H
  FFFA                        27   OUTPORT EQU     0FFFAH
  FFFE                        28   CONPORT EQU     0FFFEH
  FFFD                        29   C1IO    EQU     0FFFDH
  FFFC                        30   C2ADD   EQU     0FFFCH
  FFF2                        31   SPORT   EQU     0FFF2H
  0002                        32   RXRCV   EQU     2H
  0003                        33   STAT_1  EQU     3
  0001                        34   DATA_1  EQU     1
  003E                        35   PRMT    EQU     3EH     ;>
  0010                        36   TDB     EQU     10H
  0020                        37   SYB     EQU     20H
  0080                        38   VWB     EQU     80H
  001F                        39   AMASK   EQU     1FH
  0020                        40   TRNSB   EQU     20H
                              41
                              42   EXTRN   OUTPUT_DATA2      NEAR
                              43   EXTRN   INPUT_DATA2       NEAR
```

```
MCS-86 ASSEMBLER     DBC2


LOC  OBJ                  LINE   SOURCE

                           44    EXTRN   DTEST             NEAR
                           45
0000 B8----          R     46    START   MOV     AX, RTCDATA
0003 8ED8                  47            MOV     DS, AX  ;INITIALIZE DATA SEGMENT
0005 B8----          R     48            MOV     AX,SEG TREO
0008 8EC0                  49            MOV     ES,AX
000A B8----          R     50            MOV     AX, STACK_SEG
000D 8ED0                  51            MOV     SS, AX  ;INITIALIZE STACK SEGMENT
000F BC2800                52            MOV     SP, OFFSET STACK_TOP
0012 C706870000000         53            MOV     BVOL, 0
                           54
                           55            ;INITIALIZE USART ROUTINE
                           56
0018 BAF2FF                57            MOV     DX, SPORT
001B B065                  58            MOV     AL, 65H ;RESET
001D EE                    59            OUT     DX, AL
001E 90                    60            NOP
001F B025                  61            MOV     AL, 25H ;CMD
0021 EE                    62            OUT     DX, AL
0022 90                    63            NOP
0023 B065                  64            MOV     AL, 65H ;RESET
0025 EE                    65            OUT     DX, AL
0026 90                    66            NOP
0027 B0CF                  67            MOV     AL, 0CFH          ;MODE SET
0029 EE                    68            OUT     DX, AL
002A 90                    69            NOP
002B B025                  70            MOV     AL, 25H ;CMD SET
002D EE                    71            OUT     DX, AL
002E B0FF                  72            MOV     AL, 0FFH ;USART SETTLING DELAY
0030 B178                  73            MOV     CL, 78H
0032 D2E9                  74    SDELAY  SHR     CL, CL
0034 90                    75            NOP
0035 FEC8                  76            DEC     AL
0037 75F9                  77            JNZ     SDELAY
                           78
0039 BAFEFF                79            MOV     DX, CONPORT
003C B89999                80            MOV     AX,9999H          ;CONTROL WORD
003F EF                    81            OUT     DX, AX  ;INITIALIZE PARALLEL PORT
                           82
0040 BAFCFF                83            MOV     DX, CPADD
0043 EC                    84            IN      AL, DX  ;INPUT TERMINAL ADDRESS
0044 241F                  85            AND     AL, AMASK         ;MASK UNUSED BITS
0046 8AD8                  86            MOV     BL, AL  ;STORE IN BL REG
0048 8AFB                  87            MOV     BH, BL  ;SETUP TIMEOUT DELAY BASED
004A D0E7                  88            SAL     BH, 1   ;ON THE TERMINAL ADDRESS
004C D0E7                  89            SAL     BH, 1 ;THE 2 SHIFTS MULT BY 4
004E 80C70A                90            ADD     BH,0AH  ;ADD 10 TO THE DELAY
0051 E80000          E     91            CALL    DTEST
0054 B0CF                  92            MOV     AL,PRMT ;OUTPUT PROMPT
0056 EE                    93            OUT     DX,AL
                           94
0057 8B3E8200              95    MBFULL  MOV     DI,BVOL
005B 83FF00                96    SPT1    CMP     DI,0
005E 7508                  97            JNE     DSET
0060 BAF2FF                98            MOV     DX,SPORT
```

```
MCS-86 ASSEMBLER    DBC2


LOC  OBJ                  LINE   SOURCE

0062 EC                    99            IN      AL,DX
0064 A802                 100            TEST    AL,RXRCV        ;TEST SERIAL PORT
0066 7560                 101            JNZ     TIP
                          102
0068 8ACF                 103    DSET    MOV     CL, BH  ;INITIALIZE TIMEOUT
006A BAFDFF               104            MOV     DX, C1IO ;HANDSHAKE LINE ADDS
006D EC                   105    MINP    IN      AL, DX  ;INPUT HANDSHAKE LINES
006E A810                 106            TEST    AL, TDB ;TEST TAKE DATA LINE
0070 7575                 107            JNZ     WREC    ;JMP IF A ONE
0072 FEC9                 108            DEC     CL
0074 75F7                 109            JNZ     MINP ;JMP IF TIMEOUT NOT FINISHED
0076 33F6                 110    FNF     XOR     SI, SI  ;FIND NEW CONTROLER
0078 8BC6                 111    CWST    MOV     AX, SI
007A 0C20                 112            OR      AL, 20H ;SET TRNS BIT
007C BAFAFF               113            MOV     DX, OUTPORT
007F EF                   114            OUT     DX, AX  ;OUTPUT COMMAND WORD
0080 BAFDFF               115            MOV     DX, C1IO
0083 B007                 116            MOV     AL, STAT_1
0085 EE                   117            OUT     DX, AL  ;ENABLE TRNS
0086 FEC8                 118            DEC     AL
0088 EE                   119            OUT     DX, AL  ;RESET ENABLE
0089 B102                 120            MOV     CL,2    ;SET TIMER
008B EC                   121    CTDIN   IN      AL,DX   ;INPUT AND TEST
008C A810                 122            TEST    AL,TDB  ;OWN WORD
008E 7506                 123            JNZ     TSYNC
0090 FEC9                 124            DEC     CL
0092 75F7                 125            JNZ     CTDIN
0094 EB05                 126            JMP     SPT1
0096 A820                 127    TSYNC   TEST    AL,SYB  ;TEST SYNC BIT
0098 7401                 128            JZ      SPT1    ;JUMP IF LOW (DATA)
009A B104                 129            MOV     CL,4    ;SET TIMER
009C EC                   130    CWWT    IN      AL,DX
009D A880                 131            TEST    AL,VWB  ;TEST FOR VALID WORD HIGH
009F 750F                 132            JNZ     CRDT
00A1 FEC9                 133            DEC     CL
00A3 75F7                 134            JNZ     CWWT
00A5 EB0A                 135            JMP     SPT1
00A7 8BC6                 136    CRDT    MOV     AX,SI
00A9 241F                 137            AND     AL,AMASK
00AB 3AC3                 138            CMP     AL,BL
00AD 7508                 139            JNE     ST
00AF 83FF00               140            CMP     DI,0
00B2 740F                 141            JE      NCW
00B4 E9C700               142            JMP     SNDS
00B7 B106                 143    ST      MOV     CL,6
00B9 EC                   144    TDIN1   IN      AL,DX
00BA A810                 145            TEST    AL,TDB  ;TEST FOR TAKE DATA HIGH
00BC 7529                 146            JNZ     WREC
                          147
00BE FEC9                 148            DEC     CL
00C0 75F7                 149            JNZ     TDIN1
00C2 46                   150    NCW     INC     SI      ;INCRAMENT ADDS
00C3 81E61F00             151            AND     SI, AMASK       ;MASK UNWANTED BI
00C7 83FF00               152            CMP     DI,0
00CA 75AC                 153            JNE     CWST
```

```
MCS-86 ASSEMBLER    DBC2


LOC  OBJ                  LINE   SOURCE

00CC BAF2FF                154            MOV     DX, SPORT
00CF EC                    155            IN      AL, DX
00D0 A802                  156            TEST    AL, RXRCV
00D2 74A4                  157            JZ      CWST
                           158
00D4 E80000          E     159    TIP     CALL    INPUT_DATA2 ;INPUT DATA FROM
                           160                            ;TERMINAL
                           161
00D7 B1FF                  162            MOV     CL,0FFH ;SET TIMER
00D9 BAFDFF                163            MOV     DX, C11O
00DC EC                    164    TDT     IN      AL, DX
00DD A810                  165            TEST    AL, TDB
00DF 7506                  166            JNZ     WREC
00E1 FEC9                  167            DEC     CL
00E3 75F7                  168            JNZ     TDT
00E5 EB5F                  169            JMP     FNC
                           170
00E7 A820                  171    WREC    TEST    AL, SYB ;TEST CMD/DATA LINE
00E9 740B                  172            JZ      JSPT1   ;IF LOW LOOP FOR TAKE DATA
00EB B105                  173            MOV     CL,5    ;SET TIMEOUT FOR VALID WOR
00ED EC                    174    VWT     IN      AL, DX
00EE A880                  175            TEST    AL, VWB ;TEST FOR VALID WORD HIGH
00F0 7507                  176            JNZ     ADDT
00F2 FEC9                  177            DEC     CL
00F4 75F7                  178            JNZ     VWT
00F6 E96JFF                179    JSPT1   JMP     SPT1
                           180
00F9 BAF8FF                181    ADDT    MOV     DX,INPORT
00FC ED                    182            IN      AX,DX   ;INPUT CMD WORD
00FD 8BF0                  183            MOV     SI,AX
00FF 251FF8                184            AND     AX,0F81FH
0102 3AC7                  185            CMP     AL,BL
0104 75F0                  186            JNE     JSPT1
0106 F7C6?000              187            TEST    SI,TRNSB
010A 7526                  188            JNZ     BTEST
010C D0EC                  189            SHR     AH,1    ;THIS SEQUENCE TELLS THE
010E D0EC                  190            SHR     AH,1    ;HOW MANY DATA WORDS WILL
0110 8AC4                  191            MOV     AL, AH  ;BE COMING
0112 32E4                  192            XOR     AH, AH
0114 8BF8                  193            MOV     DI, AX
0116 B9E800                194            MOV     BP, 62  ;INITIALZE REGISTERS
0119 2BEF                  195            SUB     BP, DI  ;FOR MEMORY STORAGE
011B 8AC5                  196    TDDV    MOV     CL, BH  ;SETUP TIMEOUT
011D BAFDFF                197            MOV     DX,C11O
0120 EC                    198    TDTST   IN      AL, DX
0121 A810                  199            TEST    AL, TDB
0123 7515                  200            JNZ     INVW
0125 FEC9                  201            DEC     CL
0127 75F7                  202            JNZ     TDTST
0129 8BCE8200              203            MOV     DI,BVCL
012D E946FF                204            JMP     FNC
0130 EB85                  205    JWREC   JMP     WREC
                           206
0132 83FF00                207    BTEST   CMP     DI,0
0135 7547                  208            JNE     SNDS
```

```
MCS-86 ASSEMBLER    DBC2


LOC  OBJ                  LINE   SOURCE

0137 E921FF                209            JMP     SPT1
013A A820                  210    INVW    TEST    AL, SYB
013C 75AF                  211            JNZ     VWT     ;IF SYNC BIT HIGH JUMP
013E B106                  212            MOV     CL, 6   ;SET TIMEOUT
0140 EC                    213    IVW:    IN      AL, DX
0141 A880                  214            TEST    AL, VWB ;TEST VALID WORD LINE
0143 7507                  215            JNZ     DIN     ;JUMP IF HIGH
0145 FEC9                  216            DEC     CL
0147 75F7                  217            JNZ     IVW
0149 E91CFF                218            JMP     DSET
014C BAF8FF                219    DIN     MOV     DX, INPORT
014F ED                    220            IN      AX, DX
0150 8E894340              221            MOV     RDATA[BP][DI], AX       ;STORE DA
0154 83EF02                222            SUB     DI, 2
0157 79C2                  223            JNS     TDDV    ;JMP IF DI NOT NEG
0159 8AC3                  224            MOV     AL,BL   ;SEND STATUS WORD
015B 32E4                  225            XOR     AH,AH
015D BAFAFF                226            MOV     DX,OUTPORT
0160 EF                    227            OUT     DX, AX  ;OUTPUT STATUS WORD
0161 BAFDFF                228            MOV     DX, C11O
0164 B003                  229            MOV     AL, STAT_1      ;ENABLE TRNS
0166 FE                    230            OUT     DX, AL
0167 FEC8                  231            DEC     AL
0169 EE                    232            OUT     DX, AL  ;RESET ENABLE
016A E80000          E     233            CALL    OUTPUT_DATA2
016D BAFDFF                234            MOV     DX,C11O
0170 B1FF                  235            MOV     CL,0FFH ;SET TIMEOUT
0172 EC                    236    TD1     IN      AL,DX
0173 A810                  237            TEST    AL,TDB
0175 75B9                  238            JNZ     IWREC
0177 FEC9                  239            DEC     CL
0179 75F7                  240            JNZ     TD1
017B E9F8FE                241            JMP     ENC
                           242
017E A18000                243    SNDS    MOV     AX, RCMD ;LOAD AC WITH REC
0181 BAFAFF                244            MOV     DX, OUTPORT ;COMMAND WORD
0184 EF                    245            OUT     DX,AX
0185 B002                  246            MOV     AL, STAT_1
0187 BAFDFF                247            MOV     DX, C11O
018A EE                    248            OUT     DX, AL
018B FEC8                  249            DEC     AL
018D FE                    250            OUT     DX, AL
018E BDE800                251            MOV     BP, 62
0191 2BEF                  252            SUB     BP, DI
0193 B90500                253            MOV     CX,5
0196 E2FE                  254    RDLY    LOOP    RDLY
0198 BAFAFF                255    ODATA   MOV     DX, OUTPORT
019B 3E8B03                256            MOV     AX, TDATA[BP][DI] ;MOVE DATA TO A
019E EF                    257            OUT     DX, AX
019F BAFDFF                258            MOV     DX,C11O
01A2 B001                  259            MOV     AL, DATA_1
01A4 EE                    260            OUT     DX,AL
01A5 FEC8                  261            DEC     AL
01A7 EE                    262            OUT     DX, AL
01A8 B90600                263            MOV     CX, 6   ;DELAY FOR DATA WORD
```

```
MCS-86 ASSEMBLER     DBC2


LOC  OBJ                  LINE   SOURCE

01AB E2FE                  264   DDY      LOOP     DDY
01AD 83EF02                265              SUB      DI, 2
01B0 75E6                  266              JNZ      ODATA
01B2 B106                  267   DLY2     MOV      CL, 6
01B4 EC                    268   WSTD     IN       AL, DX   ;LOOKING FOR STATUS WORD
01B5 A810                  269              TEST     AL, TDB  ;TEST TAKE DATA BIT
01B7 7508                  270              JNZ      SMT
01B9 FEC9                  271              DEC      CL
01BB 75F7                  272              JNZ      WSTD
01BD 46                    273   JCWST    INC      SI
01BE 893E8200              274              MOV      DI,BVOL
01C2 E9B3FE                275              JMP      CWST
01C5 A820                  276   SMT      TEST     AL, SYB  ;TEST SYNC BIT
01C7 74E9                  277              JZ       DLY2     ;JMP IF LOW
01C9 B90400                278              MOV      CX, 4
01CC EC                    279   SYW      IN       AL, DX
01CD A880                  280              TEST     AL,VWB   ;TEST VALID WORD BIT
01CF 7507                  281              JNZ              SAT      ;JMP IF HIGH
01D1 FEC9                  282              DEC      CL
01D3 75F7                  283              JNZ      SYW
01D5 E97EFE                284              JMP      MBFULL
01D8 BAF8FF                285   SAT      MOV      DX, INPORT
01DB 8B0E8000              286              MOV      CX,RCMD
01DF 80E11F                287              AND      CL,AMASK
01E2 ED                    288              IN       AX, DX
01E3 3AC1                  289              CMP      AL, CL
01E5 7506                  290              JNE      JCWST
01E7 C7068200000000        291              MOV      BVOL, 0
01ED E80000          E     292              CALL     QTEST
01F0 B0CE                  293              MOV      AL,PRMT  ;SEND PROMPT
01F2 EE                    294              OUT      DX,AL
01F3 33FF                  295              XOR      DI,DI
01F5 E97EFE                296   JENC     JMP      ENC
----                       297   RTCPROG  ENDS
  00000                    298              END      START
```

```
MCS-86 ASSEMBLER    INSUB2


ISIS-II MCS-86 ASSEMBLER V1 0 ASSEMBLY OF MODULE INSUB2
OBJECT MODULE PLACED IN  F1 INSUB2 OBJ
ASSEMBLER INVOKED BY  ASM86  F1 INSUB2 ASM EPDB

LOC  OBJ                    LINE   SOURCE

                              1          ;UPDATE 19 MAR 1980
                              2
----                          3   RTCDATA SEGMENT COMMON
                              4          ASSUME  DS:RTCDATA
                              5
0000 (64                      6   DATA    DB      64 DUP(?
     ??
     )
0040 (32                      7          DW      32 DUP(?)
     ????
     )
0080 ????                     8   RCMD    DW      ?
0082 ????                     9   BVOL    DW      ?
0084 ????                    10   CADDS   DW      ?
                             11
----                         12   RTCDATA ENDS
                             13
----                         14   STRING_SEG      SEGMENT WORD PUBLIC
                             15   PUBLIC  TRED
                             16          ASSUME  ES:STRING_SEG
0000 5445524D494E41          17   TRED    DB      'TERMINAL ADDRESS - '
     4C204144445245
     535320D20
0012 5445524D494E41          18   ERMES   DB      'TERMINAL ADDRESSES ARE FROM 0 TO
     4C204144445245
     535345532041
     452046524F4D20
     3020544F203331
                             19
----                         20   STRING_SEG ENDS
                             21
----                         22   RTCPROG SEGMENT WORD PUBLIC
                             23   PUBLIC  INPUT_DATA2
                             24   EXTRN   OTEST    NEAR
                             25          ASSUME  CS:RTCPROG, DS:RTCDATA
                             26          ASSUME  ES:STRING_SEG
                             27
  0018                       28   CONC    EQU     18H
  0012                       29   CONP    EQU     12H
  000A                       30   LF      EQU     0AH
  007F                       31   RUB_OUT EQU     7FH
  0014                       32   CT      EQU     14H
  0308                       33   LINP    EQU     308H
  000D                       34   CR      EQU     0DH
  0492                       35   SCR     EQU     492H
  0030                       36   ASC0    EQU     30H
                             37
                             38
0000                         39   INPUT_DATA2     PROC
```

```
MCS-86 ASSEMBLER    INSUB2


LOC  OBJ                  LINE   SOURCE

                           40
0000 53                    41             PUSH    BX
0001 56                    42             PUSH    SI
0002 812680000FF07         43             AND     PCMD,7FFH ;CLEAR DATA NO FROM STO
0008 BF3F00                44   RB        MOV     DI,63
000B C60500                45   NFB       MOV     DATA[DI],0        ;CLEAR FIRST MEM
000E B90803                46   INDATA    MOV     CX,LINP ;LETTER INPUT ROUTINE
0011 FFD1                  47             CALL    CX
0013 3C14                  48             CMP     AL,CT     ;TEST FOR CONTROL T
0015 741B                  49             JE      JTADDS
0017 3C7F                  50             CMP     AL,RUB_OUT        ;TEST FOR RUBOUT
0019 741A                  51             JE      ERROR
001B 3C18                  52             CMP     AL,CONX ;TEST FOR CONTROL X
001D 7424                  53             JE      DLINE
001F 3C12                  54             CMP     AL,CONR ;TEST FOR CONTROL R
0021 7427                  55             JE      RLINE
0023 3C0A                  56             CMP     AL,LF     ;TEST FOR LINE FEED
0025 74E7                  57             JE      INDATA  ;IGNORE LINE FEED
0027 8805                  58   STORE     MOV     DATA[DI],AL
0029 3C0D                  59             CMP     AL,CR     ;TEST FOR CARRAGE RETURN
002B 743B                  60             JE      CR_LF
002D 4F                    61             DEC     DI
002E 7415                  62             JZ      BFULL     ;JUMP IF BUFFER FULL
0030 EBDC                  63             JMP     INDATA
0032 F806040               64   JTADDS    JMP     TADDS
0035 83FF3F                65   ERROR     CMP     DI,63     ;TEST FOR EMPTY BUFFER
0038 74D1                  66             JE      NFB
003A 47                    67             INC     DI
003B E80000          E     68             CALL    OTEST
003E 8A05                  69             MOV     AL,DATA[DI]
0040 EE                    70             OUT     DX,AL
0041 EBCB                  71             JMP     INDATA
                           72
0043 B99204                73   DLINE     MOV     CX,SCR
0046 FFD1                  74             CALL    CX ;CARRAGE RETURN LINE FEED ROUT
0048 EBBE                  75             JMP     RB
004A B99204                76   RLINE     MOV     CX,SCR
004D FFD1                  77             CALL    CX
004F 893E8200              78             MOV     BVOL,DI
0053 BF3F00                79             MOV     DI,63
0056 E80000          E     80   CK3       CALL    OTEST
0059 8A05                  81             MOV     AL,DATA[DI]
005B EE                    82             OUT     DX,AL     ;OUTPUT MESSAGE
005C 4F                    83             DEC     DI
005D 3B3E8200              84             CMP     DI,BVOL
0061 77F3                  85             JA      CK3
0063 EBA9                  86             JMP     INDATA
0065 C6050D                87   BFULL     MOV     DATA[DI],CR ;STORE CARRAGE RETURN
0068 B99204                88   CR_LF     MOV     CX,SCR
006B FFD1                  89             CALL    CX
006D F7C70100              90             TEST    DI,1 ;TEST FOR EVEN OR ODD NUMBER
0071 7404                  91             JZ      EVEN
0073 4F                    92             DEC     DI
0074 C60500                93             MOV     DATA[DI],0 ;STORE 0 IN UNUSED LOC
0077 BD4000                94   EVEN.     MOV     BP,64
```

```
MCS-86 ASSEMBLER     INSUB2


LOC  OBJ                  LINE   SOURCE

007A 2BEF                   95            SUB     BP,DI    ;THIS ROUTINE STORES THE
007C 892E8200               96            MOV     BVOL,BP  ;DATA BYTES STORED
0080 8BFD                   97            MOV     DI,BP
0082 8B05                   98            MOV     AX,BP    ;THIS ROUTINE STORES THE
0084 2D0200                 99            SUB     AX,2     ;NUMBER OF WORDS TO BE TR
0087 243E                  100            AND     AL,3EH   ;0 IS ONE WORD 3EH IS
0089 B102                  101            MOV     CL,2     ;12 WORDS
008B D2E0                  102            SHL     AL,CL
008D 080681100             103            OR      BYTE PTR RCMD+1,AL
0091 5E                    104            POP     SI
0092 5B                    105            POP     BX
0093 C3                    106            RET
0094 33F6                  107    TADDS   XOR     SI,SI
0096 8AC3                  108            MOV     AL,BL
0098 32E4                  109            XOR     AH,AH
009A B106                  110            MOV     CL,6
009C D3E0                  111            SHL     AX,CL
009E A38000                112            MOV     RCMD,AX
00A1 B99204                113            MOV     CX,SCP
00A4 FFD1                  114            CALL    CX
00A6 E80000          E     115    OUT     CALL    OTEST
00A9 268A840000      R     116            MOV     AL,ES TRED[SI]  ;SEND TERMINAL
                           117                                    ;ADDRESS REQUEST
00AE FE                    118            OUT     DX,AL
00AF 46                    119            INC     SI
00B0 83FE13                120            CMP     SI,19
00B3 72F1                  121            JB      OUT
00B5 33DB                  122            XOR     BX,BX
00B7 B90800                123    AIN     MOV     CX,LINP
00BA FFD1                  124            CALL    CX
00BC 3C0D                  125            CMP     AL,CR    ;TEST FOR CARRAGE RETURN
00BE 740E                  126            JE      FIN
00C0 2C30                  127            SUB     AL,ASC0  ;CONVERT TO BCD
00C2 7BD0                  128            JS      TADDS    ;IF LESS THAN 0 PRINT
                           129                             ;MESSAGE AGAIN
00C4 3C09                  130            CMP     AL,9     ;IF GREATER THAN 9
00C6 77DC                  131            JA      TADDS    ;JUMP
00C8 8AFB                  132            MOV     BH,BL    ;MOVE NUMBER IN BL TO BH
00CA 8AD8                  133            MOV     BL,AL    ;STORE NEW NUMBER IN BL
00CC EBE9                  134            JMP     AIN
00CE B99204                135    FIN     MOV     CX,SCP   ;SEND CARRAGE RETURN AND
00D1 FFD1                  136            CALL    CX       ;LINE FEED
00D3 B80A00                137            MOV     AX,10    ;THIS ROUTINE CONVERTS
00D6 F6E7                  138            MUL     BH       ;THE BCD NUMBER STORED
                           139                             ;IN BX AND CONVERTS IT
00D8 02C3                  140            ADD     AL,BL    ;TO A BINARY NUMBER
00DA 3C1F                  141            CMP     AL,31    ;TEST FOR BAD ADDRESS
00DC 7707                  142            JA      BADN
00DE 09068000              143            OR      RCMD,AX  ;STORE ADDRESS
00E2 E929FF                144            JMP     INDATA
00E5 B99204                145    BADN    MOV     CX,SCP   ;SEND CARRAGE RETURN AND
00E8 FFD1                  146            CALL    CX       ;LINE FEED
00EA 33F6                  147            XOR     SI,SI
00EC E80000          E     148    OTS     CALL    OTEST
00EF 268A841300      R     149            MOV     AL,ES ERMES[SI]
```

```
MCS-86 ASSEMBLER     INSUB2


LOC  OBJ                  LINE    SOURCE

00F4 EE                    150             OUT     DX,AL    ;OUTPUT MESSAGE
00F5 46                    151             INC     SI
00F6 803F24                152             CMP     SI,'$'   ;TEST FOR END OF MESSAGE
00F9 75F1                  153             JB      OTS
00FB EB97                  154             JMP     TADDS
                           155
                           156     INPUT_DATA2     ENDP
                           157
----                       158             RTCPROG ENDS
                           159             END
```

```
MCS-86 ASSEMBLER    OUT2


ISIS-II MCS-86 ASSEMBLER V1 0 ASSEMBLY OF MODULE OUT2
OBJECT MODULE PLACED IN  F1:OUT2 OBJ
ASSEMBLER INVOKED BY:  ASM86  F1:OUT2 ASM EP DB

LOC  OBJ                    LINE   SOURCE

                              1           ;UPDATE 19 MAR  1980
                              2
                              3
----                          4   RTCDATA SEGMENT COMMON
                              5
0000 (32                      6           DW      32 DUP(?)
     ????
     )
0040 (64                      7   DATA    DB      64 DUP(?)
     ??
     )
0080 ????                     8   RCMD    DW      ?
0082 ????                     9   BVOL    DW      ?
0084 ????                    10   CADDS   DW      ?
                             11
----                         12   RTCDATA ENDS
                             13
----                         14   STRING_SEG      SEGMENT WORD PUBLIC
                             15           ASSUME  ES:STRING_SEG
                             16
0000 4D455353414745          17   TSRNG   DB      'MESSAGE FROM TERMINAL '
     2046524F4D2054
     45524D494E414C
     20
                             18
----                         19   STRING_SEG      ENDS
                             20
----                         21   RTCPROG SEGMENT WORD PUBLIC
  001F                       22   AMASK   EQU     1FH
                             23
                             24   PUBLIC  OUTPUT_DATA2
                             25   PUBLIC  OTEST
                             26           ASSUME  CS:RTCPROG, DS:RTCDATA
                             27           ASSUME  ES:STRING_SEG
0000                         28   OTEST   PROC    NEAR
0000 BAF2FF                  29           MOV     DX,0FFF2H
0003 EC                      30   CH1     IN      AL,DX
0004 A801                    31           TEST    AL,1
0006 74FB                    32           JZ      CH1
0008 BAF0FF                  33           MOV     DX,0FFF0H
000B C3                      34           RET
                             35   OTEST   ENDP
                             36
                             37
000C                         38   OUTPUT_DATA2    PROC    NEAR
                             39
  0492                       40   SCR     EQU     492H
                             41
000C B106                    42           MOV     CL,6
```

```
MCS-86 ASSEMBLER     OUT2


LOC  OBJ                  LINE   SOURCE

000E D3EE                   43            SHR     SI,CL
0010 81E61F00               44            AND     SI,AMASK
0014 893E8400               45            MOV     CADDS,SI
0018 33F6                   46            XOR     SI,SI
001A 53                     47            PUSH    BX
001B BF3F00                 48            MOV     DI,63
001E 2BFD                   49            SUB     DI,BP     ;INIT REGISTERS FOR DATA
0020 E8DDFF                 50    CH2:    CALL    OTEST
0023 268A840000       R     51            MOV     AL,ES:TSRNG[SI]
0028 FE                     52            OUT     DX,AL     ;OUTPUT MESSAGE
0029 46                     53            INC     SI
002A 83FE16                 54            CMP     SI,22     ;TEST FOR END OF MESSAGE
002D 72F1                   55            JB      CH2
002F 33C0                   56            XOR     AX,AX     ;CLEAR ALL FLAGS
0031 A18400                 57            MOV     AX,CADDS
0034 27                     58            DAA
0035 8AE0                   59            MOV     AH,AL
0037 240F                   60            AND     AL,0FH    ;MASK LOWER BCD NUMBER
0039 B104                   61            MOV     CL,4
003B D2E8                   62            SHR     AL,CL
003D 053030                 63            ADD     AX,3030H          ;ADJUST TO ASCII
0040 8BD8                   64            MOV     BX,AX
0042 3C30                   65            CMP     AL,30H    ;CHECK FOR 0 IN HIGH DIGI
0044 7406                   66            JE      P2D
0046 8AC7                   67            MOV     AL,BL
0048 E8B5FF                 68            CALL    OTEST
004B EE                     69            OUT     DX,AL     ;PRINT HIGH DIGIT
004C E8B1FF                 70    P2D:    CALL    OTEST
004F 8AC7                   71            MOV     AL,BH
0051 EE                     72            OUT     DX,AL     ;PRINT LOW DIGIT
0052 B99204                 73            MOV     CX,SCR
0055 FFD1                   74            CALL    CX
0057 E8A6FF                 75    CH6:    CALL    OTEST
005A 3E8A1340               76            MOV     AL,DATA[BP][DI]
005E EE                     77            OUT     DX,AL     ;OUTPUT DATA TO TERMINAL
005F 4F                     78            DEC     DI
0060 79F5                   79            JNS     CH6       ;JUMP IF DI GREATER THAN
0062 E898FF                 80            CALL    OTEST
                            81
0065 B00A                   82            MOV     AL,0AH
0067 EE                     83            OUT     DX,AL
0068 8B3E8200               84            MOV     DI,BVOL
006C 83FF00                 85            CMP     DI,0
006F 7506                   86            JNE     RN
0071 E88CFF                 87            CALL    OTEST
0074 B03E                   88            MOV     AL,3EH    ;>
0076 EE                     89    OUT:    DX,AL     ;SEND PROMPT
0077 58                     90    RN:     POP     BX
0078 C3                     91            RET
                            92
----                        93    OUTPUT_DATA2    ENDP
                            94    RTCPROG ENDS
                            95            END
```

```
MCS-86 ASSEMBLER    CONTR


ISIS-II MCS-86 ASSEMBLER V1.0 ASSEMBLY OF MODULE CONTR
OBJECT MODULE PLACED IN  F1 CONTR OBJ
ASSEMBLER INVOKED BY  ASM86  F1 CONTR SRC

LOC  OBJ                    LINE   SOURCE

                               1           ;UPDATE 30 AUG 79
                               2
----                           3   STACK_SEG       SEGMENT
                               4           ASSUME NOTHING
0000 (20                       5           DW      20 DUP(?)
     ????
     )

0028                           6   STACK_TOP       LABEL   WORD
----                           7   STACK_SEG       ENDS
                               8
----                           9   BUS     SEGMENT
                              10           ASSUME CS:BUS, DS:BUS, ES:BUS
                              11
0000 B8----            R      12   START   MOV     AX,STACK_SEG
0003 8ED0                     13           MOV     SS,AX
0005 BC2800                   14           MOV     SP,OFFSET STACK_TOP
0008 0E                       15           PUSH    CS
0009 1F                       16           POP     DS
000A 0E                       17           PUSH    CS
000B 07                       18           POP     ES
000C BAFEFF                   19           MOV     DX,0FFFEH       ;INITIALIZE I/O P
000F B89898                   20           MOV     AX,9898H
0012 EF                       21           OUT     DX,AX
0013 BAFCFF                   22   BEGIN:  MOV     DX,0FFFCH       ;CLEAR VALID WORD
0016 B000                     23           MOV     AL,00
0018 EE                       24           OUT     DX,AL   ;ACK
0019 FEC0                     25           INC     AL
001B EE                       26           OUT     DX,AL   ;CLEAR ACK
001C 33C0                     27           XOR     AX,AX
                              28
                              29
001E B302                     30           MOV     BL,2    ;INIT RCVR TERM NO
0020 B701                     31           MOV     BH,1    ;INIT XMTR TERM NO
                              32
0022 8AC3                     33   GENREC: MOV     AL,BL   ;FORMATE RCVR COMMAND WORD
0024 BAFAFF                   34           MOV     DX,0FFFAH       ;OUTPUT RECV COMM
0027 EF                       35           OUT     DX,AX
0028 BAFCFF                   36           MOV     DX,0FFFCH       ;SET OUTPUT ENABLE
002B B003                     37           MOV     AL,3
002D FE                       38           OUT     DX,AL   ;NOTE       BETWEEN OUTPUT
                              39
002E B000                     40           MOV     AL,00       ;CLEAR OUTPUT ENABLE
0030 EE                       41           OUT     DX,AL
                              42
0031 B90500                   43           MOV     CX,5
0034 49                       44   DELAY   DEC     CX
0035 75FD                     45           JNZ     DELAY
                              46
0037 8AC7                     47   GENXMT  MOV     AL,BH   ;FORMAT XMTR COMM WORD
```

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MCS-86 ASSEMBLER     CONTR


LOC  OBJ                  LINE   SOURCE

0039 B420                   48            ADD     AL,32   ;ADD XMIT BIT
003B BAFAFF                 49            MOV     DX,0FFFAH       ;OUTPUT XMTR COMM
003E EF                     50            OUT     DX,AX
003F BAFCFF                 51            MOV     DX,0FFFCH       ;SET OUTPUT ENABLI
0042 B007                   52            MOV     AL,7
0044 EE                     53            OUT     DX,AL
                            54
0045 B000                   55            MOV     AL,00
0047 EE                     56            OUT     DX,AL
                            57
0048 B90900                 58            MOV     CX,9    ;INIT 20US SHIFT DELAY
004B 49                     59    SHIFTD: DEC     CX
004C 75FD                   60            JNZ     SHIFTD  ;CX=9*1060P=21 2US DELAY
                            61
                            62    ;CLEAR VALID WORD SET BY OWN TRANS
004E BAFEFF                 63    TIMEOUT:MOV     DX,0FFFEH
0051 B000                   64            MOV     AL,00
0053 EE                     65            OUT     DX,AL   ;ACK
0054 FEC0                   66            INC     AL
0056 EE                     67            OUT     DX,AL   ;CLEAR ACK
                            68
0057 B90100                 69            MOV     CX,1    ;INIT TIMEOUT COUNT
                            70
005A BAFEFF                 71    INPUT:  MOV     DX,0FFFEH       ;LOOK FOR VALID WI
005D EF                     72            IN      AL,DX
005E D0E0                   73            SHL     AL,1    ;CARRY FLAG SET IF VALID I
0060 7217                   74            JB      SHORT COMDAT    ;JUMP IF CF=1
                            75
0062 49                     76            DEC     CX
0063 75F5                   77            JNZ     INPUT   ;32US TEST
                            78
0065 FEC3                   79    INCR:   INC     BL      ;INCR RCVR TERM NO  TWICE
0067 FEC3                   80            INC     BL
                            81
0069 FEC7                   82            INC     BH      ;INCR XMTR TERM NO  TWICE
006B FEC7                   83            INC     BH
006D 8AC3                   84            MOV     AL,BL
006F 2C20                   85            SUB     AL,20H  ;UNMASK THE 32 BIT
0071 74A0                   86            JZ      BEGIN   ;REG COUNT=32
0073 EBAD                   87            JMP     GENREC  ;ISSUE NEW BUS OFFER
                            88
0075 D0E0                   89    COMDAT: SHL     AL,1    ;COMM/DATA WORD TEST
0077 73D5                   90            JNB     TIMEOUT ;JUMP IF CF=0 (DATA)
                            91
0079 BAF8FF                 92    STWD:   MOV     DX,0FFF8H       ;INPUT STATUS WORI
007C ED                     93            IN      AX,DX
007D 8AD7                   94            MOV     DL,BH
007F 2AC2                   95            SUB     AL,DL   ;COMPARE STATUS TERM TO
                            96                            ;STORED XMTR TERM NO.
                            97
0081 74E2                   98            JZ      INCR    ;DATA EXCHANGE IS COMPL
0083 EBC9                   99            JMP     TIMEOUT
----                       100    BUS     ENDS
  0000                     101            END     START
```

APPENDIX D

RECEIVER SCHEMATICS

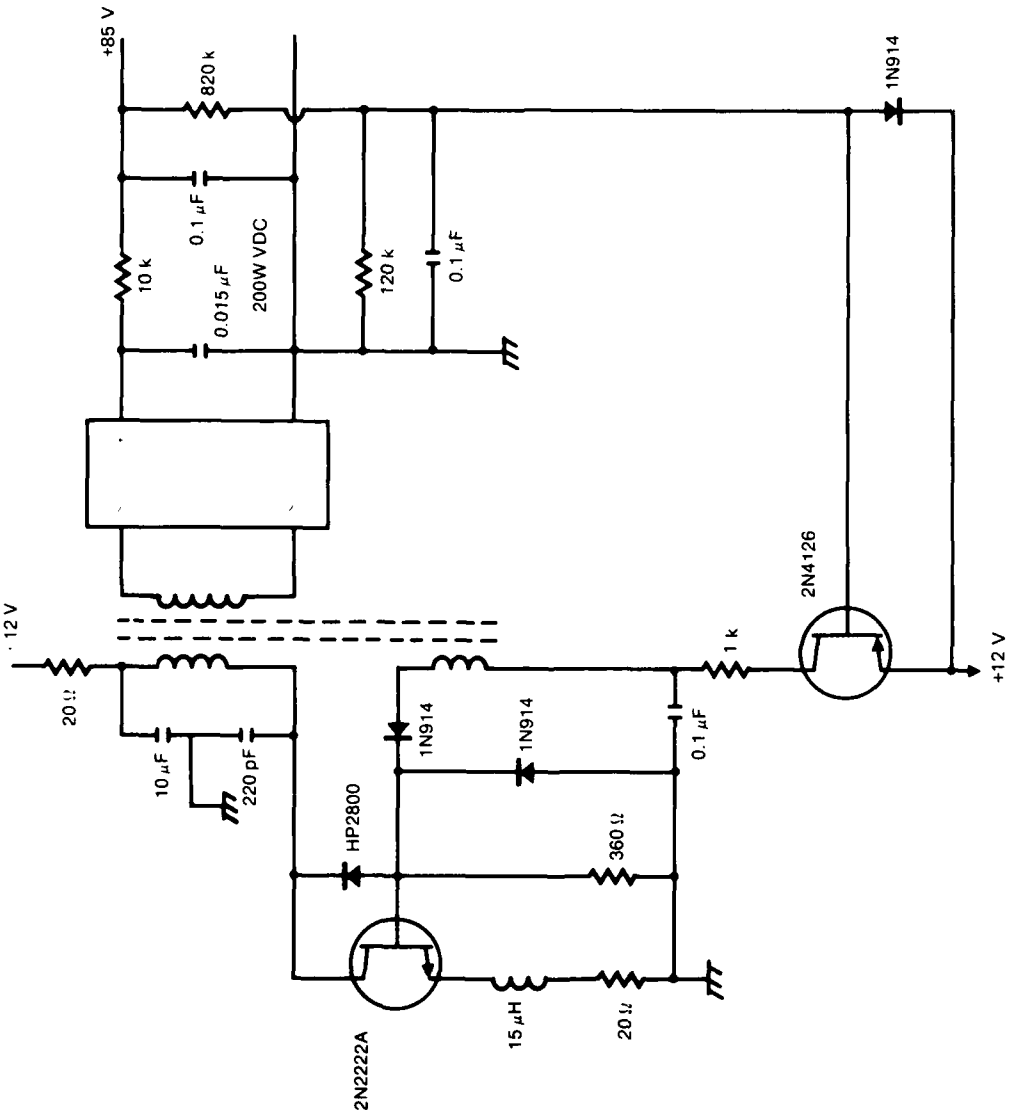

Figure D-1. DC-to-DC converter.

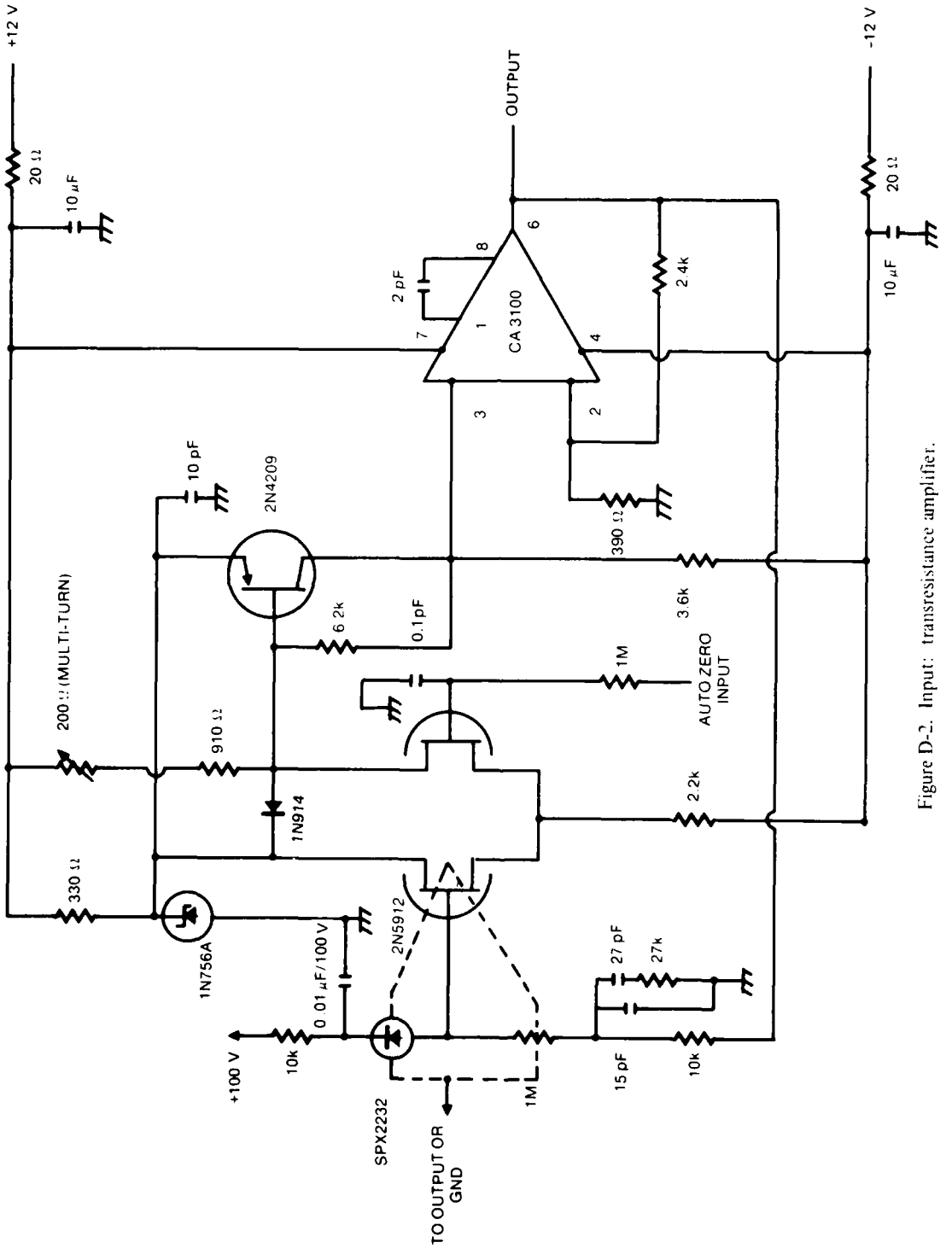

Figure D-2. Input: transresistance amplifier.

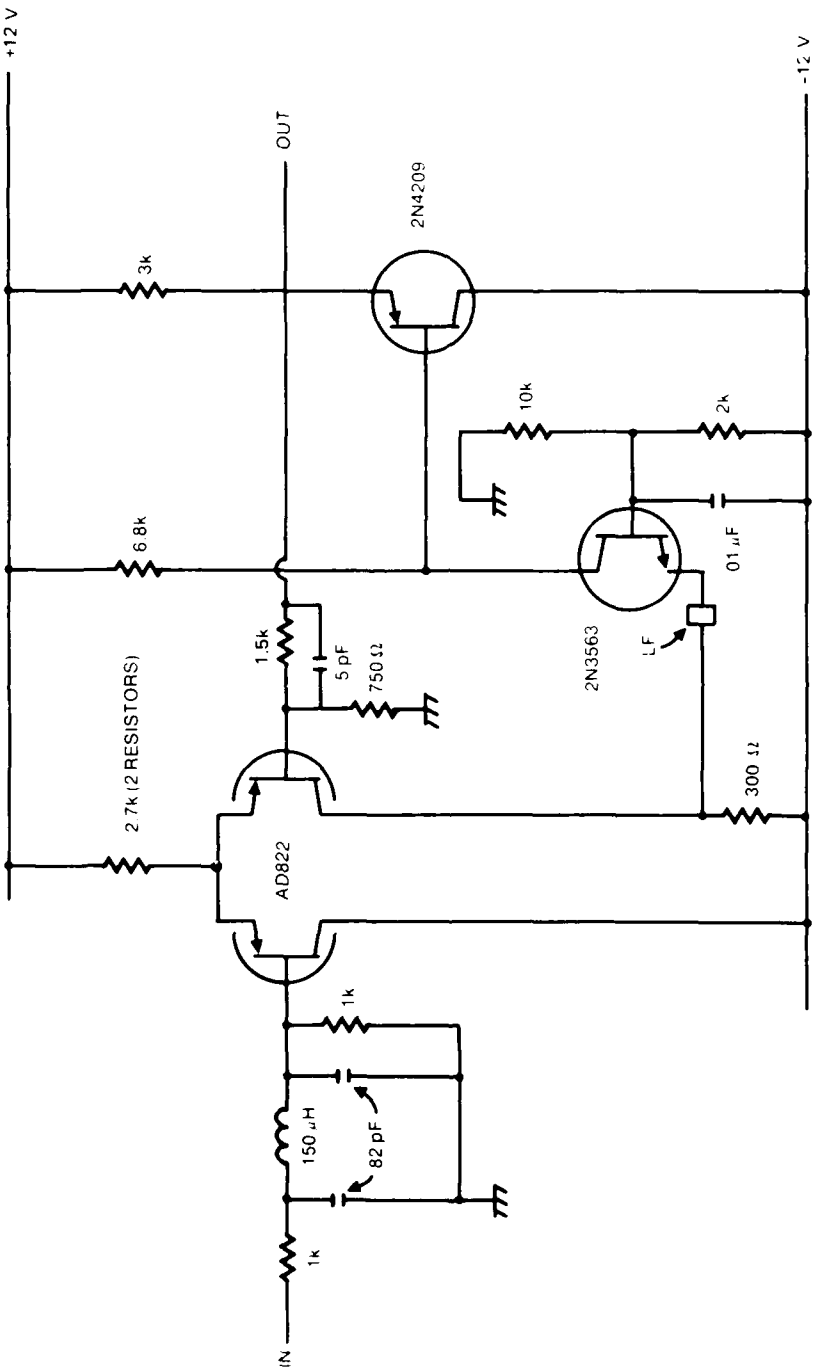

Figure D-3. Filter and amplifier.

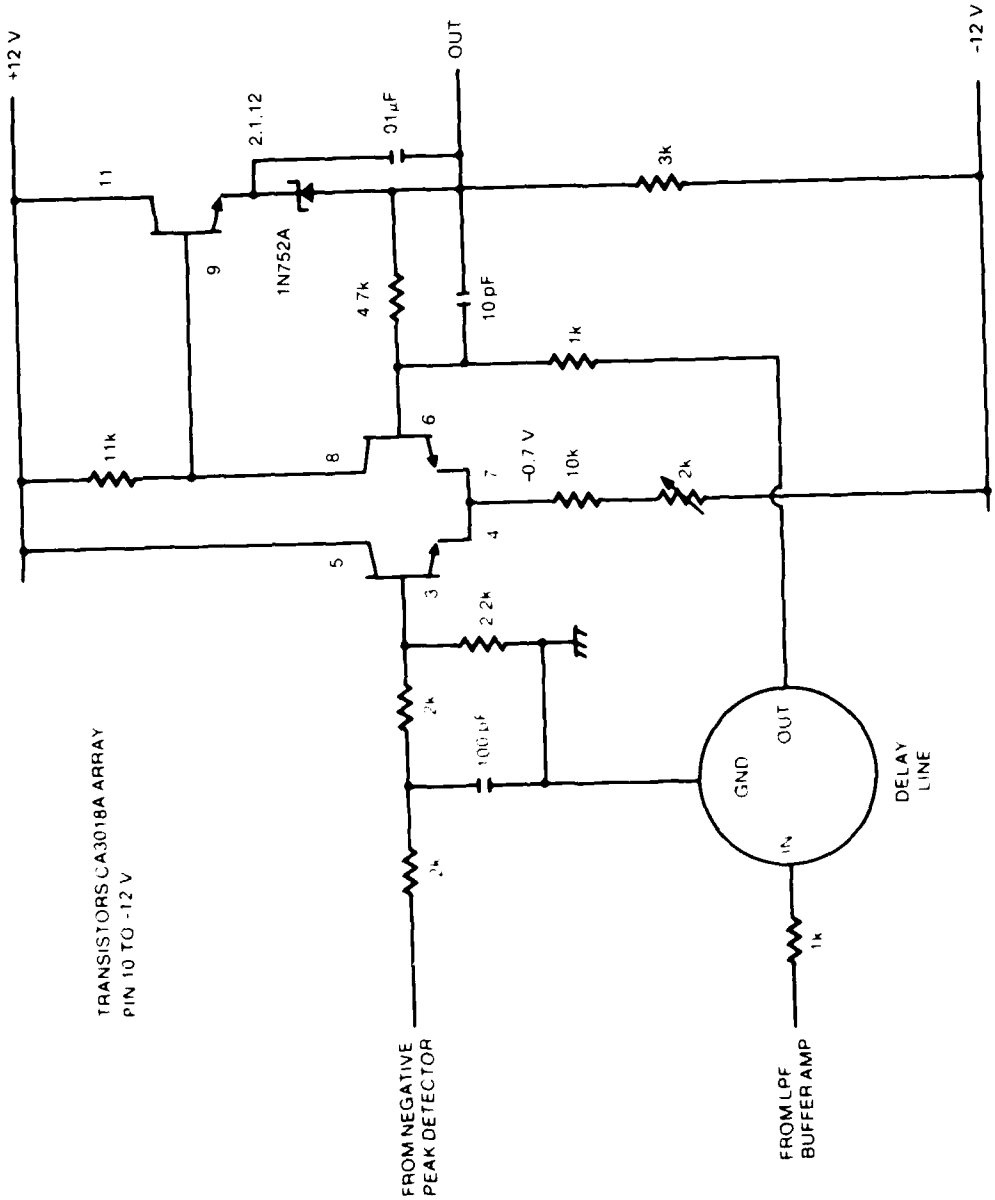

Figure D-4 Delay line and combining amplifier.

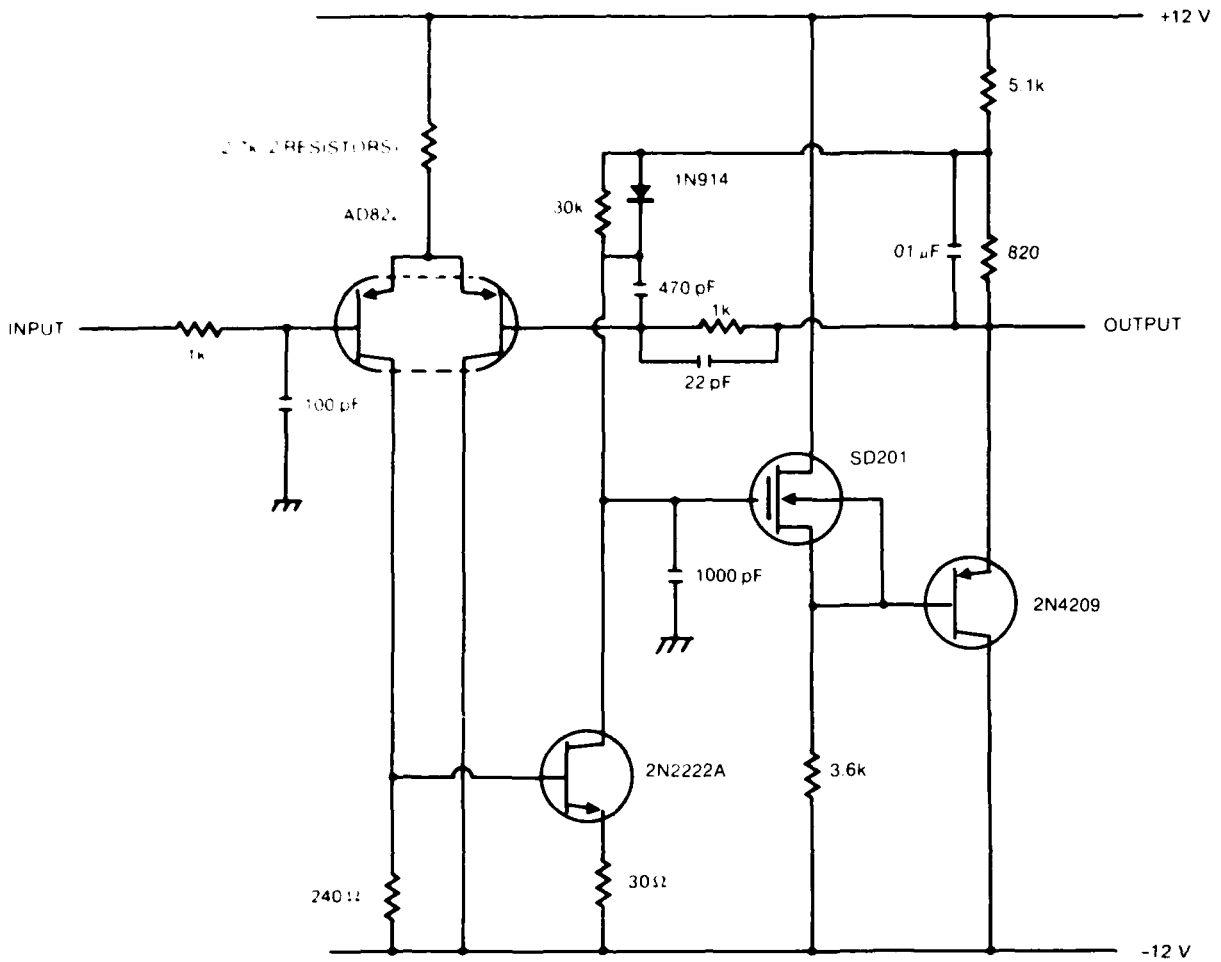

Figure D-5. Negative peak detector.

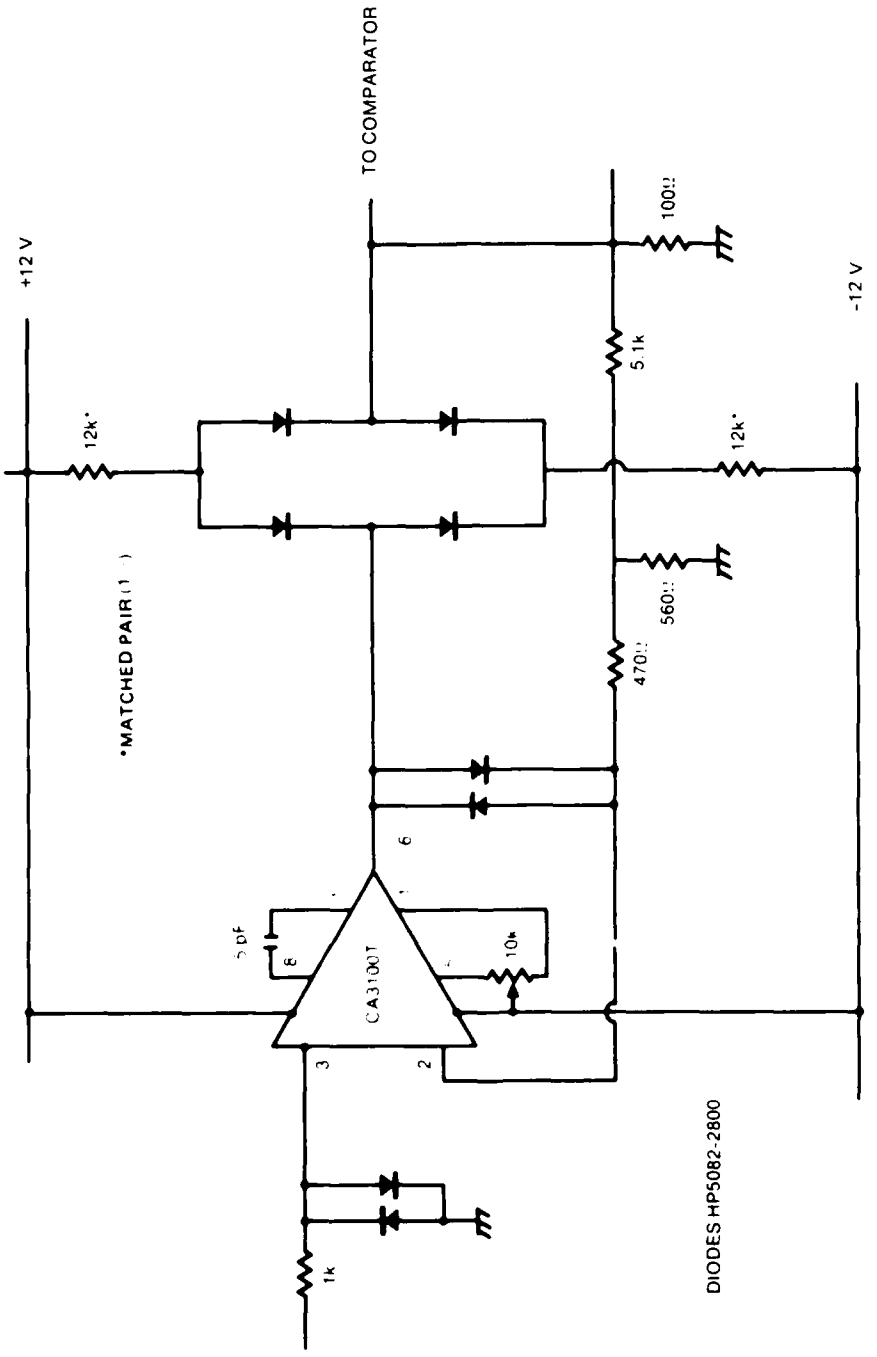

Figure D-6. Limiting amplifier.

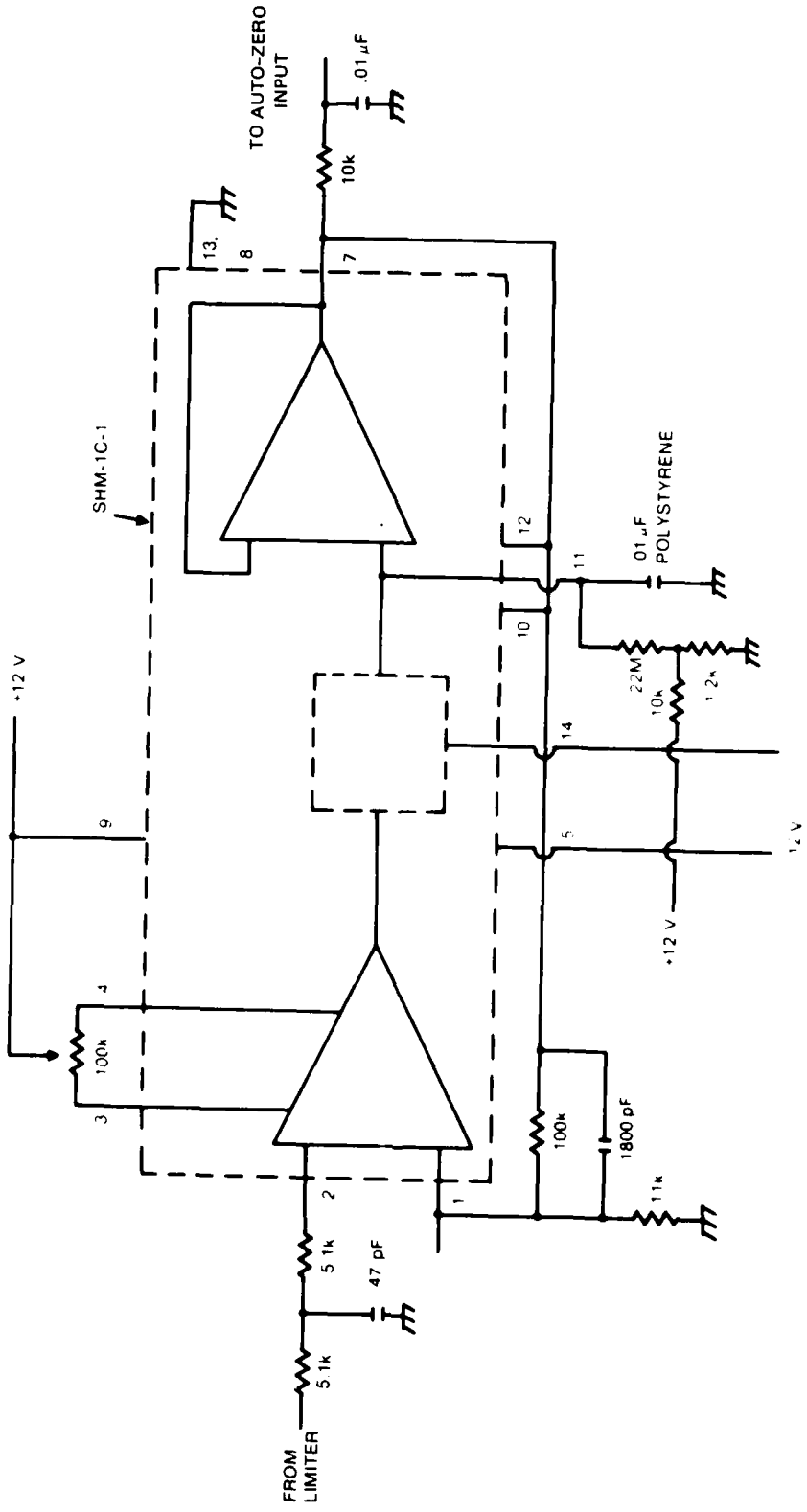

Figure D-7. Sample-and-hold circuit.

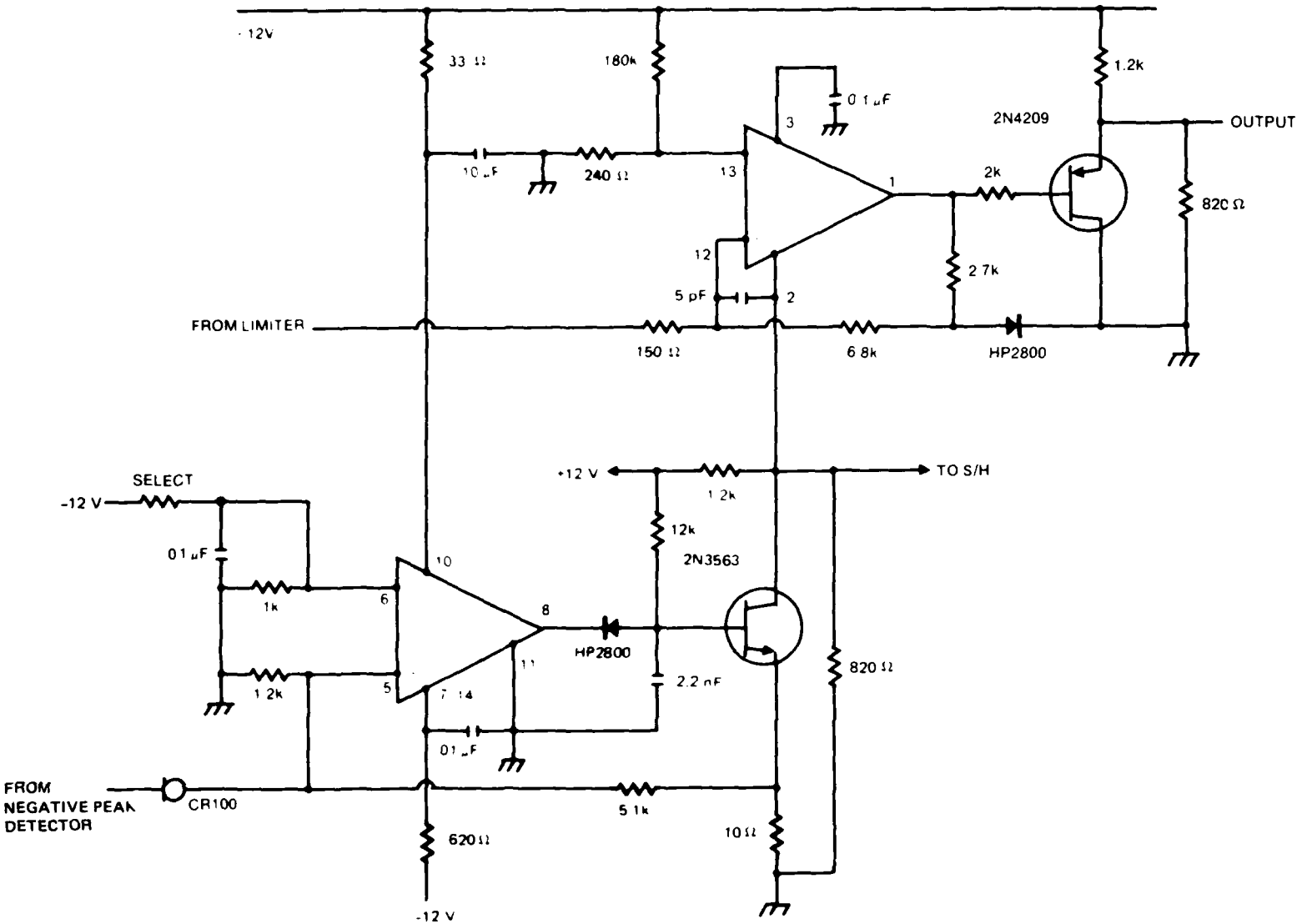

Figure D-8. Data regenerator and output.

END

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