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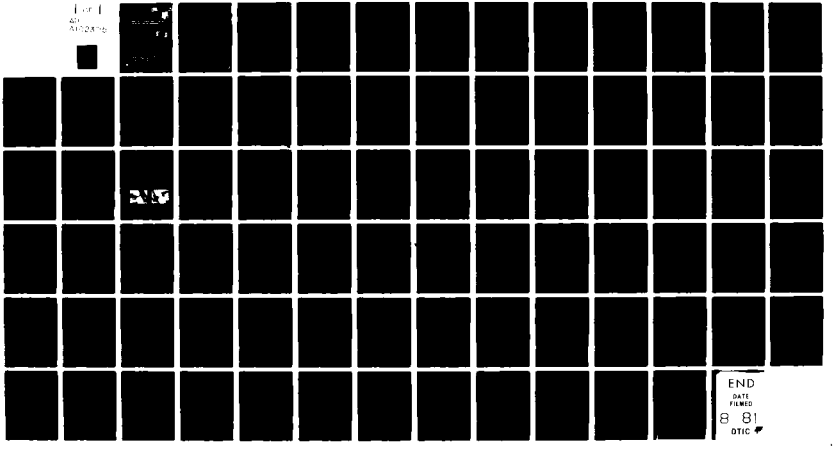

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Final Technical Report
June 1981

ELECTRICAL CHARACTERIZATION OF MICROPROCESSOR MEMORIES

Hughes Aircraft Company

Ted Y. Fujimoto

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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APPROVED: Allen P. Converse

ALLEN P. CONVERSE
Project Engineer

APPROVED: David C. Luke

DAVID C. LUKE, Colonel, USAF
Chief, Reliability & Compatibility Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

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With the advent of microprocessors, considerable design activity has occurred in the development of semiconductor memories as an integral part of the family with the microprocessors. These memories tend to be organized in byte fashion or some submultiple or multiple of the 8 bits. Selected memories of this type have been evaluated and MIL-M-38510 detail specifications written for those devices deemed appropriate. Evaluation consisted of normal DC and AC parameter limit testing, functional tests

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and electrical characterization studies. The characterization studies included Schmoo plots of selected parameters that were considered critical, including AC timing requirements.

The following types of memories were evaluated: Static RAMS, ROM, Fused PROM, Programmable Array Logic, Field Programmable Logic Arrays, Ultraviolet Erasable PROMS, and Electrically Erasable ROMS.

Ten detail specifications were written for the foregoing types of parts as follows: Static RAMS - 1) 2147, 2147H, 2114, 2148; 2) 6810; 3) 27S07A, 27S03A; 4) ROM - S6831B; 5) PAL - 10H8, 12H6, 14H4, 16H2; 6) FPLA - 82S100, 93458; 7) UV/EPROM - 2716; 8) TMS 2532; 9) 6654; 10) EAROM - 2810, 7810.

SUMMARY

This report presents the results of a study to select and electrically characterize semiconductor memories that are compatible with microprocessors and are suitable for military applications. An assessment of factors that effect the reliability of memories was made, and drafts of MIL-M-38510 detail specifications (slash sheets) for specific devices were generated.

To meet the project goals the following objectives were defined: (1) develop and refine a test philosophy for complex microprocessor oriented memories that can be used for preparing MIL-M-38510 detail specifications, (2) establish the type and sequence of electrical tests to be performed on each of the different types of memories, (3) perform electrical characterization, DC, AC and functional testing to assure reliable performance over the military temperature ranges, (4) generate drafts of MIL-M-38510 detail specifications, and any special test methods that should be included in MIL-STD-883.

The selection of memories for this program was based on mutual agreement between RADC and Hughes Aircraft Company. The selection process included contacts with the suppliers to determine the availability of the parts, and the supplier's willingness to submit his product for military qualification. The process yielded the following types of memories for evaluation; (1) static RAMs both bipolar and MOS, (2) fusible PROMs (Programmable ROMs), (3) UV/EPROM (Ultra Violet/Erasible PROM), (4) EAROMs (Electrically Alterable ROMs), (5) FPLAs (Field Programmable Logic Arrays), and (6) PALs (Programmable Array Logic).

The general selection methodology employed for this program started with a tentative list of desirable memories mutually agreed upon by RADC and Hughes. Contact was then made with the supplier. The availability and temperature range capability of the parts were determined, as well as the willingness of the supplier to support their parts in a military program. The vendor's part specification was reviewed, and since most of the parts were state-of-the-art devices, the available technical literature describing the class of memory under investigation was studied. Any existing military specifications that were similar to the selected part were used as a general guideline for tests and for writing new specifications. The actual tests, selection of test patterns, and electrical characterization of the memories were dependent upon the type of memory. Test patterns used for the RAMs were quite extensive, since both writing and reading were under direct high speed computer control. Programmed ROMs, PROMs, UV/EPROMs had restricted writing characteristics, and therefore the tests were limited to read only. The EAROMs were similar to the RAMs, and required complex testing and an extensive detail specification.

All of the memories with written specifications were divided into three distinct groups: Group I – static RAMs; Group II – ROM, Fused PROM, PAL, FPLA, and Group III – UV/EPROM, EAROM. Group I, static RAMs were volatile and were sufficiently different from the other devices to be studied separately. The Group II memories were all non-volatile memories, once they were fuse programmed. The Group III memories were semi-volatile and stored their contents as an electrical charge in the gate region of the memory cell FET.

All of the tests were performed on the Fairchild Sentry 610, an automatic computer controlled tester, which provided extensive electrical characterization data, such as Schmoo plots. The appendix in this report shows typical DC, AC, functional test results and Schmoo plots of the electrical characterization of most of the memory parameters of the static RAM device 2148.

Most of the programming of memories, when required, was accomplished on commercial equipment recommended by the manufacturers. UV (Ultra Violet) erasing for UV EPROMs was accomplished on in-house equipment including the programming. The MNOS device was programmed, erased and read on the Sentry tester.

Ten detail specifications for MIL-M-38510 were written. A complete list of the 26 parts tested including the ten specifications are listed in Table 3-1 of this report. It should be noted that the 26 parts tested included alternate sources of the same part and different dash number versions. In addition, some parts did not meet specification requirements, and hence were eliminated. Other parts with existing specifications such as the 93470 (MIL-M-38510/233) and M3636 (MIL-M-38510/210) were evaluated for specific test conditions only as requested by RADC.

The following is a summary of evaluation results by groups. Group I static RAMs were in general quite satisfactory. The 2148 and 2147H parts appear to be marginal for V_{IH} inputs, and may suffer yield problems. The Group II devices, the M3636 fused PROM cannot meet ±10% Vcc at -55°C. The new PAL devices suffer low programming yields at the present time, otherwise the electrical test results are satisfactory. Both sources for the FPLA devices are satisfactory, and can meet the new specification.

In the Group III devices, the UV/EPROM 2716 from both sources are satisfactory. The MM2716 can easily meet the electrical requirements at 125 °C, but its extended memory retension capability is unknown. The M2716 from vendor E is limited to 100 °C. The TMS2532, a 32K UV/EPROM, is electrically good to +125 °C, however its memory retention capability is unknown. The EAROMs from both suppliers were satisfactory.

It appears that some form of standardization is needed to define input/output levels for MOS microprocessor memories. In particular, standardization is needed if MOS microprocessor memories are to be compatible only with other MOS devices or TTL circuits, or both. The memory suppliers are generally inconsistent in their V_{IH} and V_{IL} requirements. Some memories will accept standard TTL output devices, but others will not, and the V_{IH} levels can only be met by adding pull up resistors to the inputs.

PREFACE

The test and evaluation program described in this report was performed by the Components Department of the Ground Systems Group of the Hughes Aircraft Company, Fullerton during the period between June 1978 and September 1980. The work was performed for the USAF Rome Air Development Center under contract number F30602-78-C-0221. Mr. Allen P. Converse of the RADC Reliability Assurance Section provided the technical direction.

Special acknowledgement is made to the following personnel from the Sentry Engineering Group who wrote all the ATE test software and performed all of the electrical measurements: Mark I. Growe, Howard A. Baumer, Gordon P. Chin, and Dan B. Buker. The Document Services Group prepared all the MIL-M-38510 detail specifications in particular Lillian Y. Arakaki who performed and coordinated most of this effort. Mr. Jim E. Thomas was the Program Manager and Ted Y. Fujimoto was the Technical Director.

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Section 1

INTRODUCTION

1.1 Purpose of Program

This report presents the results of electrically testing and characterizing a number of selected, state-of-the-art, microprocessor oriented memories for military applications. The information acquired was utilized to write drafts of MIL-M-38510 detail specifications. Included in this list of memory types were static RAMs, both bipolar and MOS, Fusible PROMs, UV Erasable PROMs, Electrically Alterable ROMs (EAROMs), Field Programmable Logic Arrays (FPLAs), and Programmable Array Logic (PAL).

The objectives of this effort were to:

- Develop and refine a test philosophy for memories that can be used for preparing MIL-M-38510 specifications.
- Establish the type and sequence of electrical tests to be performed on the selected memories.
- Electrically characterize, DC, AC, and functional tests for memories to assure reliable performance over military temperature ranges.
- Generate MIL-M-38510 detail specifications and any special electrical test methods for inclusion in MIL-STD-883.

1.2 Background

Complex memory devices such as the 4044 (4KX1) static RAM and the 6831, a 4096 bit ROM are presently being used in military, microprocessor-based systems. Other memory devices, such as the 2716, (2048 by 8 bit), ultraviolet erasable PROM, are scheduled to be used in military applications. As these more complex devices are used in increasing numbers, the need for reliability assurance through proper test methods and electrical characterization has become essential.

1.3 Primary Tasks

The primary tasks of this program were to determine those semiconductor memories that are being used in on-going military projects, including those

being used in developmental and production programs, and those being designed into new systems; to determine the willingness of the suppliers to support their product in military programs, to obtain samples, test and characterize the devices, and finally, to write the drafts of MIL-M-38510 slash sheets for those devices determined to be acceptable. In addition, if any special test procedures were generated that could be incorporated in MIL-STD-883, they would also be submitted.

1.4 Scope of Program

Early in the program, Rome Air Development Center (RADC) indicated that dynamic random access memories (RAMs), need not be included in the tests since these types of parts were being evaluated on another RADC program. The initial parts selected by RADC and Hughes Aircraft Company included 8 types of parts from 5 different suppliers. These parts are listed below.

Device	Supplier	Description
2114	E	1Kx4 Static MOS RAM
2147	E	4Kx1 Static MOS RAM
2716	E	2Kx8 UV/PROM (-55^{o} to +100^{o}C)
4044	N	4Kx1 Static MOS RAM
40L45	N	1Kx4 Static MOS RAM
82S100	M	16x48x8 FPLA, T.S., Bipolar
82S101	M	16x48x8 FPLA, O.C., Bipolar
93459	C	16x48x8 FPLA, T.S., Bipolar
93458	C	16x48x8 FPLA, O.C., Bipolar

The vendor code for the suppliers is included in Section 3.0 of this report.

The parts selection process included availability, military contractor usage, and whether full military temperature requirements were met. They had to be hermetically sealed, and "burn-in" was not required. In addition, the test program did not require qualification testing or formal failure analysis procedures. The primary requisites were to fully evaluate the selected devices and to determine if the devices could undergo a rigorous electrical characterization program using an automatic computer controlled tester.

During the next 10 months, six additional devices were added:

Device	Supplier	Description
9114	A	Equiv. to 2114
93470/93471	C	Bipolar 4Kx1 RAM
5114	L	1Kx4 CMOS/SOS RAM

Device	Supplier	Description
281.	D	2Kx4 EAROM, PMOS
7810	K	2Kx4 EAROM, PMOS
4104	G	4Kx1 Quasi Static MOS RAM

Subsequently, twenty five (25) new part numbers consisting of 13 part categories were introduced as new potential candidates for evaluation. Later the list was reduced to the following sixteen items.

Device	Supplier	Description
2532	N	4Kx8 UV Erasable PROMs (0^{o} to 70^{o}C)
2716	J	2Kx8 UV Erasable PROMs (-55^{o} to $+125^{o}$C)
6654	F	512x8 CMOS UV Erasable PROMs
3636	E	2Kx8 Fused PROM, Bipolar
6831B	B	2Kx8 ROM, MOS
6810	B	128x8 Static RAM, MOS
2147H	E	4Kx1 Static RAM, MOS
2148	E	1Kx4 Static RAM, MOS
27SO7A (29701)	A	16x4 Static RAM, Bipolar
27SO7	A	16x4 Static RAM, Bipolar
27SO3A	A	16x4 Static RAM, Bipolar
27SO3	A	16x4 Static RAM, Bipolar
10H8	I	PAL, Bipolar
12H6	I	PAL, Bipolar
14H4	I	PAL, Bipolar
16H2	I	PAL, Bipolar

Section 2

MEMORY TESTING AND CHARACTERIZATION

In general, a test philosophy was established to aid in drafting the detail slash sheet of the general MIL-M-38510, microcircuit specification. The starting point was generally the vendor's specification for the memory device. The vendor's specification were anything from one page to several pages, and the quality of the specification ranged from inadequate to satisfactory. The manufacturer usually had to be contacted regarding their willingness to qualify their device as a military product, and to cooperate in producing additional device information.

Another general guideline was the utilization of existing military specifications that are similar to the product being evaluated. This was particularly helpful in trying to standardize the tests as much as possible, as well as establishing the specification format.

DC and AC (switching) parameter testing is a mature and well understood procedure, and is easily handled by most general purpose computer controlled testers available on the market. It was in the area of functional testing and test pattern sensitivity that proved most troublesome, and required the greatest device analysis leading to establishment of the appropriate test specifications.

Those devices that did not have parameters defined at military temperature limits were tested over the military temperature extremes, unless the vendor indicates that the product was not designed for the wide temperature operation. Using statistical analysis and Schmoo plots, new functional limits were assigned at the military temperature extremes.

The majority of the parts were tested on the Fairchild Sentry 610 tester. The only exception was the 2716 UV/PROM which was tested and characterized using the Tektronix S-3260. Since the Tektronix S-3260 was previously used for characterizing the 8K UV/EPROM 2708, the test program was easily modified to run the 16K UV/EPROM. Memory programming and erasing characteristics were accomplished at the Fullerton facility

The basic Sentry test program included functional tests and characterization plots, AC parametric measurements, and DC parametric measurements. Memory pattern sensitivity tests were accomplished under functional tests.

The memories selected for this program can be separated into three distinct groups based upon the internal memory cell structure and principle of operation, for example, Group I consisted of Static RAMs while Group II consisted of ROMs, Fused PROMs, PALs, FPLAs, and Group III was composed of UV/EPROMs, and EAROMs.

Group I static RAMs are sufficiently different in memory structure and timing requirements to dictate their grouping separately from the other memory devices. The cells can be easily written into by electrical signals in situ, as well as being easily read. This type of memory is volatile.

Group II memories differ from others in that the memory cell structure is dependent on an interconnecting link or lack of it, as determined by the customer's special programming techniques. The programming is accomplished at the factory with a final process mask for ROMs. While with PROMs, the customers utilizing special device programmers blow open internal fuses. This type of memory is nonvolatile and nonreprogrammable.

Group III memories depend upon storing memory programs within the device gate areas by electrical charge methods. The charges are stored in a semipermanent state in a nonvolatile manner. Erasure is by ultraviolet light or electrical means.

2.1 Group I Static RAMs

Static Random Access Memories (RAM) are defined as high speed memories that rely on the Flip-Flop (FF) configuration as the basic memory cell. The cross coupled flip-flop keeps the cell in a relatively stable state due to it's internal latching feedback network. The stability of the latching flip-flop cell depends upon ratio of current flow in the on-transistor versus the leakage current of the off-transistor. A conservative cell design means higher on-current flow, but a resulting higher power dissipation in the basic cell. Current designers and some of the new low-power cell designs, using giga ohm polysilicon load resistors, have reduced the current flow to less than 1 nano ampere. Since the on transistor current flow may now be approaching the leakage current of the off-transistor at high temperature, the stability of the latching network can become marginal and is in danger of being easily upset by noise or abnormal leakage at the off-transistor node. Because of the low current flow, static memories are becoming susceptible to alpha particle soft failures. The static RAM's evaluated in this program (except for the 4104) have relatively conservative FF cell designs using transistor currents in the range of 1 microampere. Since the true or false state of the FF is the basic memory cell information, the FF will always be in a stable state, except during the transition time. This is illustrated in Figure 2-1 for the schematics of a FF memory cell.

The advantages of using static RAMs are high speed, simple interface circuitry, lower susceptibility to glitch problems, absence of pattern sensitivity problems, reduced support circuitry, relatively little electrical disturbances, and no requirements for refresh circuitry.

The main disadvantages of the RAMs are: they require larger die compared to dynamic memories of equal bit capacity, require more power than dynamic memories, and are more expensive per bit then dynamic RAM's. The main

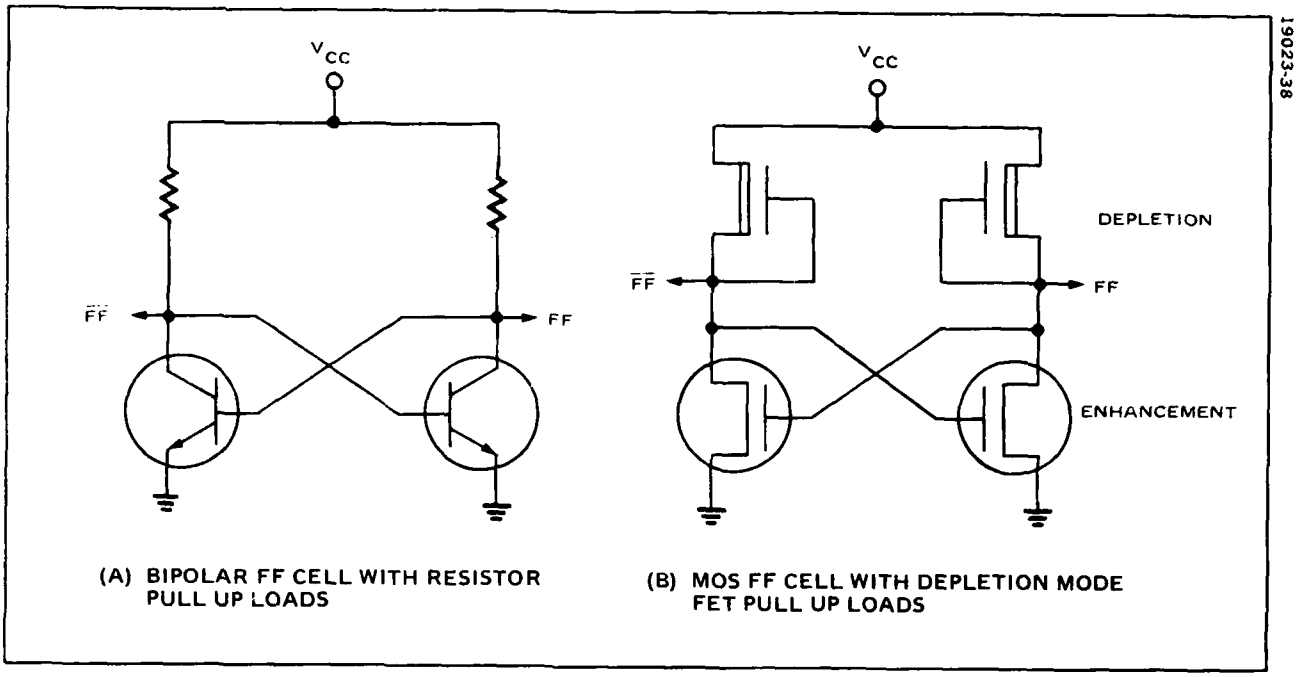

Figure 2-1. Basic Static RAM Cells. The FF is always in a stable state except during transition time.

reason that static RAMs are larger and require more power than dynamic RAMs is because the design structure of the static circuits requires more transistors per bit when compared to dynamic circuits. Historically, dynamic circuits evolved because static circuits required too much power and used too many transistors. Smaller, lower power memories were needed so dynamic circuits and dynamic memory cells became the answers. A static-memory cell flip-flop requires at least four transistors or two transistors and two resistors. In addition, one of the transistors is always conducting current. A dynamic memory cell requires only one transistor and one capacitor, and draws current only to charge and discharge capacitances during the clock transition time. Thus, both power and chip size is reduced for dynamic RAMs over equivalent bit memory size static RAMs. Smaller chip size semiconductor devices are generally lower in cost due to the greater number of chips that can be placed on any given silicon wafer.

The test philosophy adopted for all memories included initially testing the device to all vendor specifications, as well as standard military requirements. In addition, since the device pattern sensitivities were usually unknown and device topology was not always available, basic test patterns already available from the Sentry hardware pattern generator were utilized. The same approach was taken in memory characterization to do Schmoo plotting. Critical device parameter safety margins were investigated as thoroughly as possible, resulting in some plots that have redundant information.

Functional Tests. Initial functional tests were performed on RAMs to determine that the device was in good working order prior to spending further characterization test operations on the device.

With all limits and conditions as specified in the manufacturer's data sheets, the device was tested under minimum, nominal, and maximum voltage conditions. The functional tests checked memory pattern sensitivities, cell integrity, address decoding, sense amplifier capabilities, write amplifier characteristics, etc, as completely as possible. Depending upon the type of memory, RAM, ROM, EPROM, EAROM, FPLA, etc, the order of performing the major characterization tasks is quite different, unlike the RAMs, writing and reading for the PROM's cannot be done simultaneously. RAMs are normally alterable during operation, but PROMs can be both programmed in the field or factory, temporarily or permanently, electrically or mask programmed. Thus, each of these different applications determines the order and method in which the major tests are performed.

The test patterns selected concentrated upon checking total memory cell integrity, address decoding, sense amplifier capabilities, write recovery capabilities, and simple intercell noise sensitivity tests. The initial functional test patterns selected for static RAM's were: all "ones" and all "zeros" patterns for determining cell integrity, checkerboard pattern and its complement to test intercell reactions, check for shorts, diagonal patterns to check slow sense amplifier recovery and address decoding, and march pattern and its complement to check the functionalism of the cells and sense amplifier recovery. N^2 and $N^{3/2}$ patterns such as Galpat, Ping Pong, Walking 1/0, Galwrec, etc, are not normally required. However, during initial qualification of a device for MIL-M-38510 requirements or for periodic checking, these test patterns would be utilized. Therefore, all static RAMs were tested using Galpat (N^2) to check worst case access times, and the diagonal GALWREC ($N^{3/2}$) to check for write recovery characteristics.

DC and AC Parametric Tests. All DC and AC parametric tests were performed using the vendor parameter specifications to normal military temperature limits of -55 °C to +125 °C. If specification limits were not defined at military temperature, then tests were run to the military temperature extremes and parameter values were determined. If the vendor indicated that the devices should not be utilized beyond their stated temperature ranges, these requests were taken into consideration. Although the samples were small, sufficient information was obtained to establish reasonable test limits. AC parametric tests such as switching parameters or propagation delays were usually checked using functional test conditions. Write parameters were also checked during functional test conditions because of the test time efficiency achieved. The comparators of the tester were adjusted to the level defined by the customer or the normal military requirements for all switching tests. For functional tests, the sampling comparators were usually set at the device threshold or mid-points of the input/output voltage swing.

Characterization Tests. These tests were conducted to determine the critical parameters of the devices supplied by a vendor or vendors. The devices were forced to operate over a much wider range of conditions, and the go/no-go results at each set of conditions were plotted or tabulated for quick visual examinations in graphic "SCHMOO" plots displays showing the margins of safe operation. In most cases, all conditions were held constant except for two parameters which were varied on the x-y graphic display table showing pass areas as "x" and fail areas as ".". Sample schmoo plots are shown in the appendix for the 2148, 4K static RAMs. For these Schmoo plots, the sampling strobes were kept as narrow as practical, approximately 20 nanoseconds wide.

2.1.1 RAM Test Results Static

2147, 2114. The initial tests of vendor E's 2114 and 2147 devices indicated that the devices passed all functional, DC and AC parameter requirements. The characterization tests indicated that the measured parameters have adequate margins of safety. Some problems did occur in the order of measurements on the Sentry tester. During the -55 °C tests, a polyurethane foam is used as an insulator and sealer for the thermostream test cavity. During the tests, the foam gradually hardened and pushed against the load jumper wires on the (performance) board eventually breaking some wires, and electrically damaging some of the parts. In addition, the -55 °C test caused considerable condensation problems. Even though dry nitrogen is used for the -55 °C test, care had to be taken to prevent moisture condensation from obscuring low level current leakage tests. As a result, this test was reprogrammed to be performed last.

The 2147 is the first of the NMOS static RAM that uses a device scaling process[1] to achieve very small physical dimensions. The memory is arranged in a 4096 by 1 bit array. It uses FET device technology based on 6 micron gate length, 1200 Å gate thickness and 2 micron diffusion depth. It also uses depletion mode FETs as the static cell flip-flop loads, and has its own internal substrate voltage bias generator.

2147H-1, 2147H-2, 2148. Shortly after the 2147 devices were tested, the 2147H and the 2148 were introduced, and made available by vendor E. The supplier also indicated that the 2114 and 2147 will no longer be made since the new devices will replace them. These new devices are scaled down devices of the 2147, promoting smaller FET's resulting in higher speeds. The gate lengths were reduced to 3.5 microns, and the gate oxides thicknesses to under 700 Å. To maintain device reliability and yield, neither of the basic circuit technology or device design was changed. Only the device dimensions were scaled down according to specific design rules.

When evaluated to the vendor specifications, in particular if an input pulse of 0 to 3.0 Volts was specified and the temperature range limited to 0 to 70 °C, the parts met their own specifications. However, the validity of using such a high input pulse for generating device switching parameter characteristics is open to question, since TTL outputs (which might be used as a drive source) are generally specified at 0.8V to 2.4 Volts when fully loaded. If TTL outputs drive only MOS inputs, then V_{OH} of 3.0 Volts can be easily generated by TTL outputs.

The 2147H-1 and 2147H-2, and the 2148 electrical characteristics were checked over the military temperature range of -55 °C to +125 °C. Figure 2-2, show the average address access time measurements of the 2147H and the 2148, respectively. When the vendor's recommended input pulse was utilized, access times for the 2147H-1 and 2147H-2 were satisfactory as shown in Figure 2-2. When V_{IH} was reduced towards 2.0 Volts, the chip select access times became marginal. Figures 2-3 and 2-4 show the input pulse characteristics of the two

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[1] Dennard, R. H., et al, "Design of Ion-Implanted MOSFET's With Very Small Physical Dimensions," IEEE S. F. Solid State Circuits, p 31-37, Oct 1974.

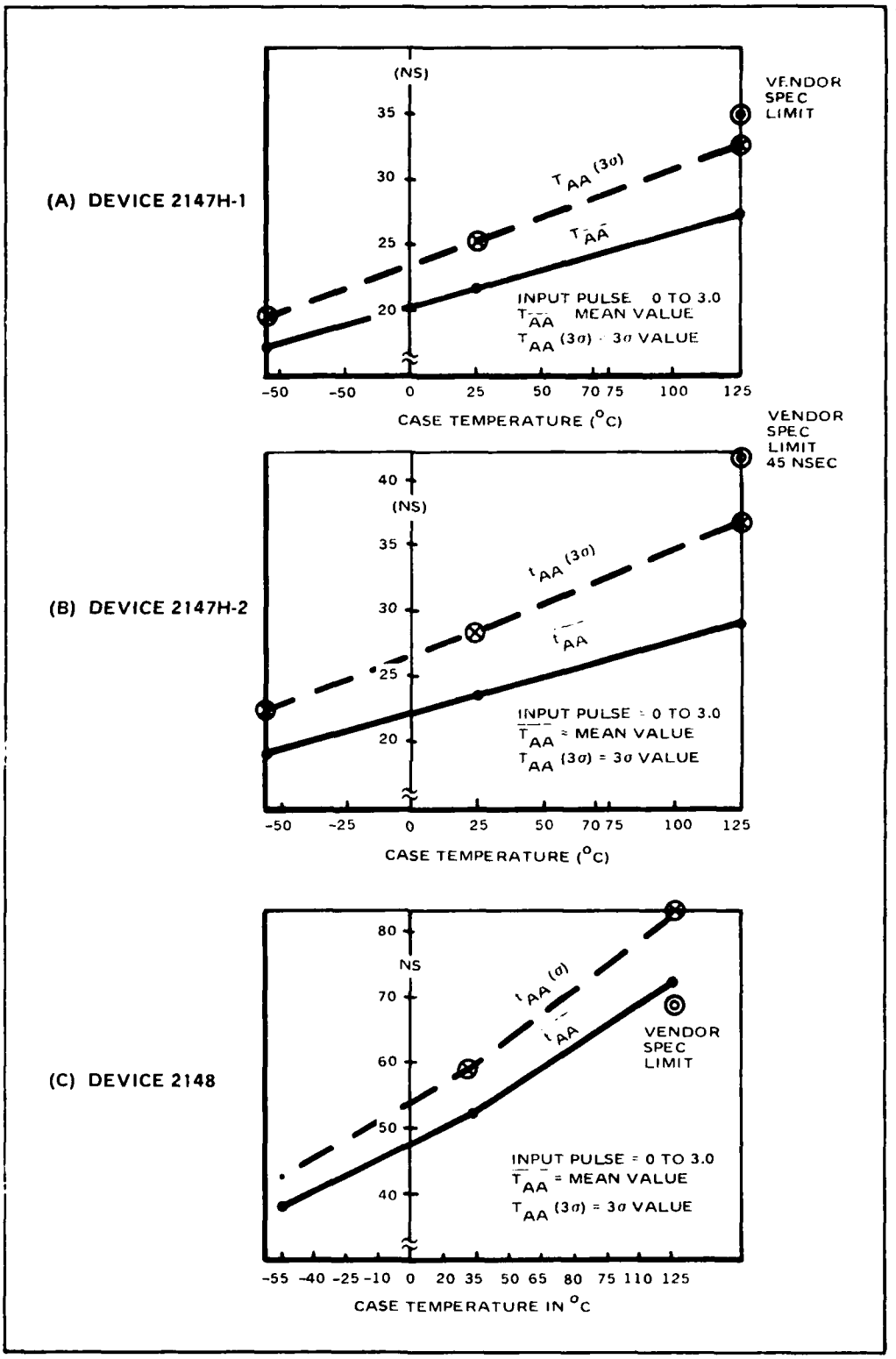


Figure 2-2. Address Access Time vs Temperature. When the vendor's recommended input pulses were used, the access times were satisfactory except for the 2148.

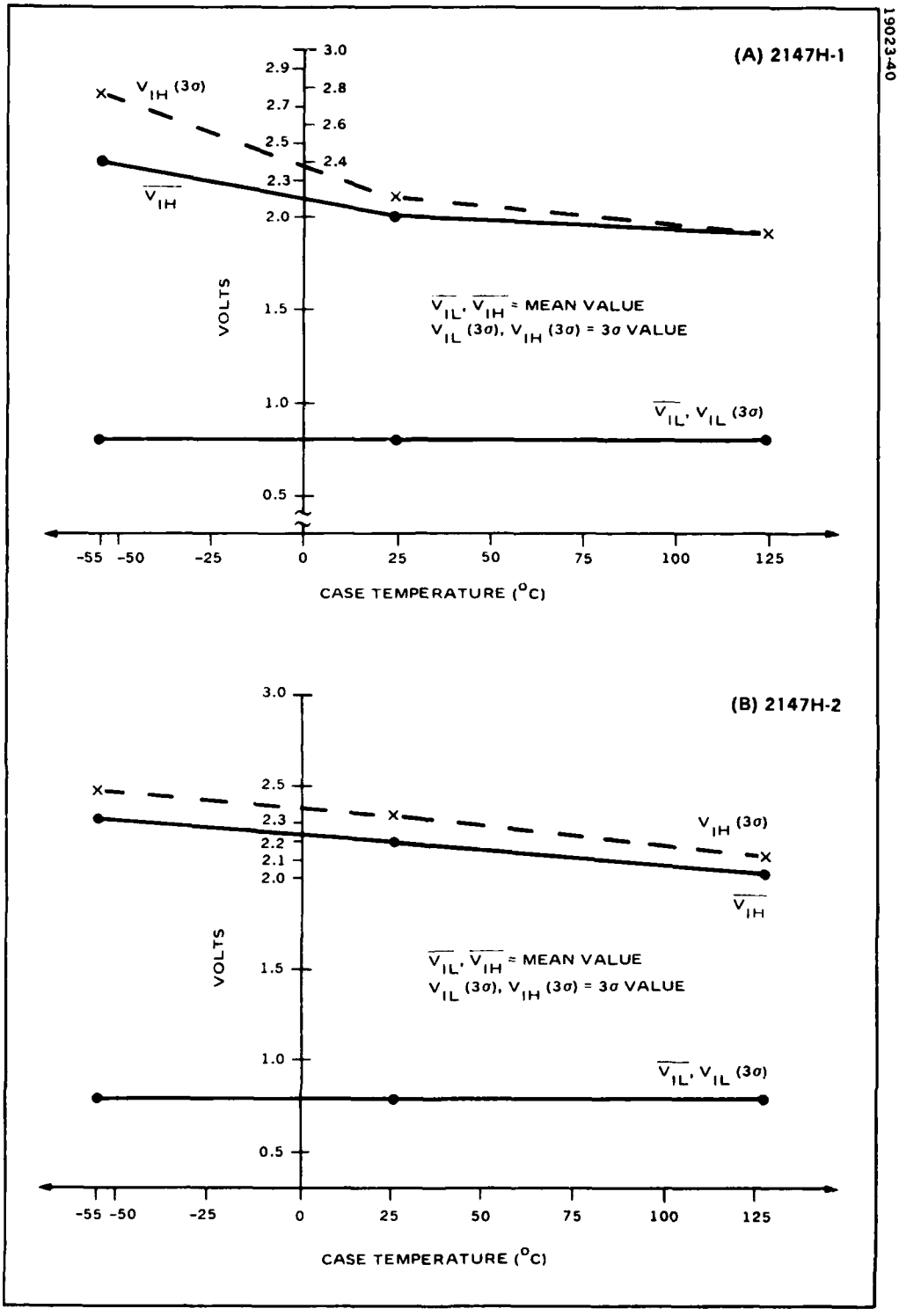


Figure 2-3. AC Pulse Input vs Temperature. Tests at -55°C indicated that both devices exceed to V_{IH} specification limit of 2.0 volts.

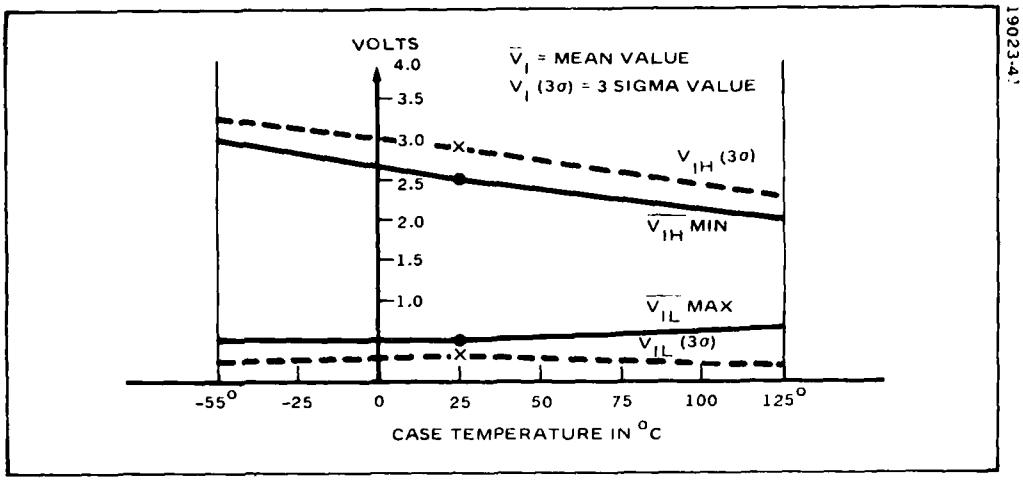


Figure 2-4. 2148 AC Pulse Input vs Temperature. The vendor has discontinued device 2114, and they will be replaced by this device.

types of devices and verify the AC V_{IH} requirements at -55°C. The detail specification for MIL-M-38510 requires that for the functional tests, all inputs must be set to V_{IH} of 2.0 Volts. Vendor E has indicated that yields on the 2147H-1 and 2147H-2 are very poor, and therefore will not be available. In addition, the 2148H is now available, although it was not indicated if the 2148 will be replaced immediately with the H version or if the 2148 will be maintained in production.

Due to the marginal capabilities at the lower input pulses, and the small sample size of the test, it was decided to increase access time limits. At +125°C, the access times for 2147H-1 and 2147H-2 were increased 5 nanoseconds each to 40 and 50 nanoseconds, respectively. For the 2148, the access times were increased to 90 nanoseconds to allow operation at +125 °C temperature. The 3 sigma limits shown in the graphs are shown only for relative information since the distribution is based on a small sample (15) and usually only from one lot.

9114. Vendor A version of the 2114 was evaluated through all electrical characterization, DC and AC tests, and functional tests similar to the 2147 and 2148. This device met all electrical requirements according to the test analysis. Two minor differences were noted in the detail specifications of the 9114 versus the 2114. The 9114 has output leakage I_{OZ} that exceeds the 2114 specification limit. The output short circuit current (I_{OS}) limit is less than the 2114 specification limits. A review of the electrical characterization data indicated that I_{OZ} is not a problem, and the 9114 can easily meet the 2114 specification limit with plenty of safety margin. The 9114 output short circuit current, worst case measurement data was 30 mA maximum compared to the 2114 limit of 40 mA, so therefore, this parameter normally is not a problem either.

4044, 40L45. Initial testing of the NMOS 4044, (4Kx1) and 40L45 (1Kx4) devices indicated that it could not meet certain of the vendor's own parameter limits. In particular, these devices could not meet the V_{OH} at 1 mA requirement. In addition, vendor support was not encouraging; therefore, all testing of these devices was curtailed until the vendor could supply improved parts.

6810. These static memories (128x8) belong to the 6800 microprocessor family. Two suppliers parts were evaluated, vendors B and H. Both vendors parts met all requirements at the military temperature range of -55°C to +125°C except for small differences in noncritical parameters as shown in Table 2-1. When two or more vendors supplied devices to meet the requirements for one particular memory part type, the first step was to compare their respective device specifications and note any differences. Both devices were then electrically measured and characterized at all three military temperatures. The measured data was reviewed and compared against their own specifications as well as the other specification limits. The final parameter limits chosen for the draft of a military specification were based on the results of a review of the measured parameters, of each device, the vendors specification limits, and a reasonable certainty that the vendors can or cannot meet the specification limits. The final specification limit must be a reasonable value depending upon the parameter being measured. The discrepancies noted on each vendor's device specifications are listed in Table 2-1. For each of the parameters listed in the table, the final

TABLE 2-1 SPECIFICATION DIFFERENCES IN CERTAIN ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Vendor		Units
		B	H	
Max Input Current (A_n, R/W, CS_n, $\overline{CS}_n$) V_{in} = 0 to 5.5V	I_{in}	10	2.5	uA
Max Supply Current (25°C)	I_{CC}	70	100	mA
Output Capacitance (25°C)	C_{out}	10	12.5	pF
Max Enable Access Time	t_{acs}	200	230	nSec

values for the specification were chosen based on the result of carefully reviewing all measured data and selecting limits that would accommodate both suppliers. All functional and switching requirements met the worst case conditions, V_{IH} at 2.0 Volts, and V_{IL} at 0.8 Volts.

27S07A (29701), 27S07, 27S03A, 27S03. These high speed memories utilize both Schottky diode clamped and emitter coupled logic circuits. The memory is organized as a fully decoded 16 word by 4 bit per word static RAM. The 27S07A is a noninverting tri-state output, while the 27S03A is an inverting tri-state output RAM. The other two devices are slightly slower versions of the first two. All DC and AC tests were satisfactory. There were no particular sensitivities to test patterns noted during functional tests. The address access times at +125°C temperature did not have sufficient margins, therefore, the limit was increased 5 ns to 30 ns.

Input pulse requirements for V_{IH} typically measured 2.2 and 2.4 volts at -55°C for the 27S07A and 27S03A respectively. The sample size was small, 11 each, and from a single lot, therefore, these measurements may not represent the normal population. However, if these samples represent the true production

runs, then a serious yield problem would exist for the manufacturer at a V_{IH} minimum of 2.0 volts. All DC and AC tests were satisfactory. In the functional tests, the worst V_{IH} was 2.4 Volts at -55°C. This may lead to a yield problem if production parts cannot meet an AC input pulse of 2.0 Volts.

4104. Tests of these quasi-static devices were satisfactory. It should be noted that although the memory is made of true flip-flop static cells, the supporting peripherial circuits are dynamic. The chip select input is a clock, and occurs in a periodic manner to keep the internal circuits operational, including the data output. The output will not hold its V_{OH} level indefinitely, hence requiring the chip select signal to be cycled periodically.

93470, 93471. These high speed TTL bipolar static memories are organized 4096x1. The two devices are identical except for the one bit output stage. The 93470 is open collector while the 93471 has a tri-state output. The devices have full decoding on chip, with separate data input and data output lines.

These bipolar 4Kx1 static RAM's were tested primarily to determine if a cold start problem exists at low temperatures. The necessary Sentry DC, AC parametric and functional test programs were created and a sample of eleven 93471 devices were fully characterized at 25°C, +125°C and -55°C using standard test procedures. At 25°C and +125°C temperature levels all devices met specification requirements. At -55°C none of the devices would meet the functional tests or the V_{OH} requirements.

A second test was performed using a different test procedure in which the power was kept on the devices in the stand by mode and after waiting for 1.5 minutes, the temperature was reduced to -30°C. A complete set of measurements was taken. All parts met the specification requirements for DC and AC parameters and functional tests. The temperature was again reduced to -55°C, and the power to the device was left connected. After a 30 second wait period the devices were tested again. All of the parts failed functional tests again, in particular, at V_{cc} of 4.5 Volts.

Figures 2-5 through 2-8 show that at -55°C, the data input is unable to be written into or read out of the memory when V_{cc} supply voltage goes below +5.0 Volts.

2.2 Group II ROM

The Read Only Memory (ROM) is one of the simplest of semi-conductor memories in terms of memory cell structure. The ROM is mask programmed to customer requirements at the factory. The memory cell consists of one transistor per cell, and the coding consists of disconnecting or leaving the cell transistor connected to the appropriate address lines.

Due to the relative simplicity of the memory cell and the fact that the cell becomes active when addressed, the ROM is a highly stable memory device and relatively insensitive to most capacitivity coupled noise disturbances. The primary objective of functional test patterns for the cell area was to check the cells for integrity, opens, adjacent cell shorts, and speed. In addition to the cell area, standard test patterns were run to check address decoding, sense amplifier recovery, input-output operation and other special circuits. A GALPAT type, read-only test pattern was used to check all of the foregoing test requirements for devices already programmed to a known code.

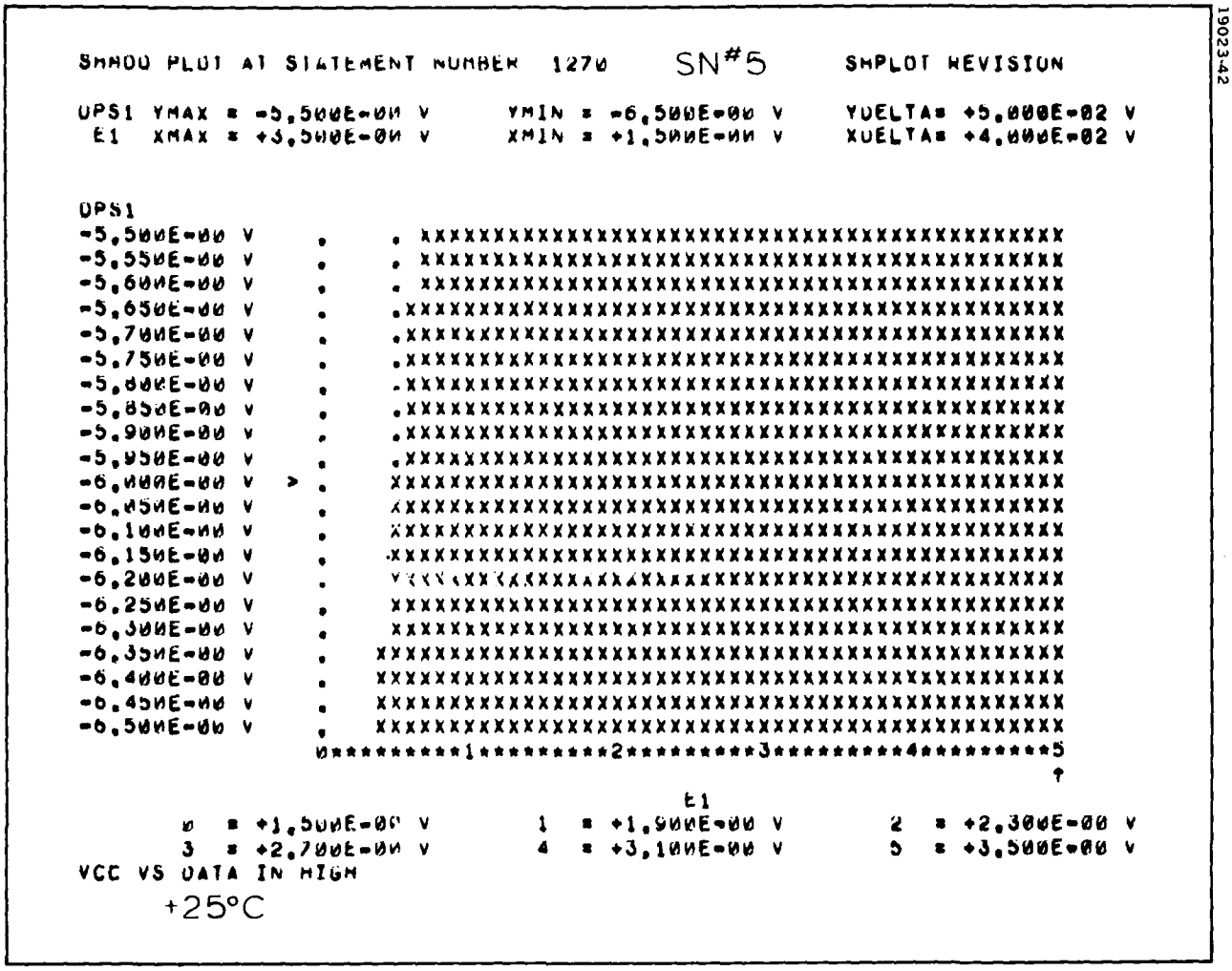


Figure 2-5. Device 93471 V_{cc} vs Data Input High at 25°C. The device passed this test at +25°C, but failed at -55°C.

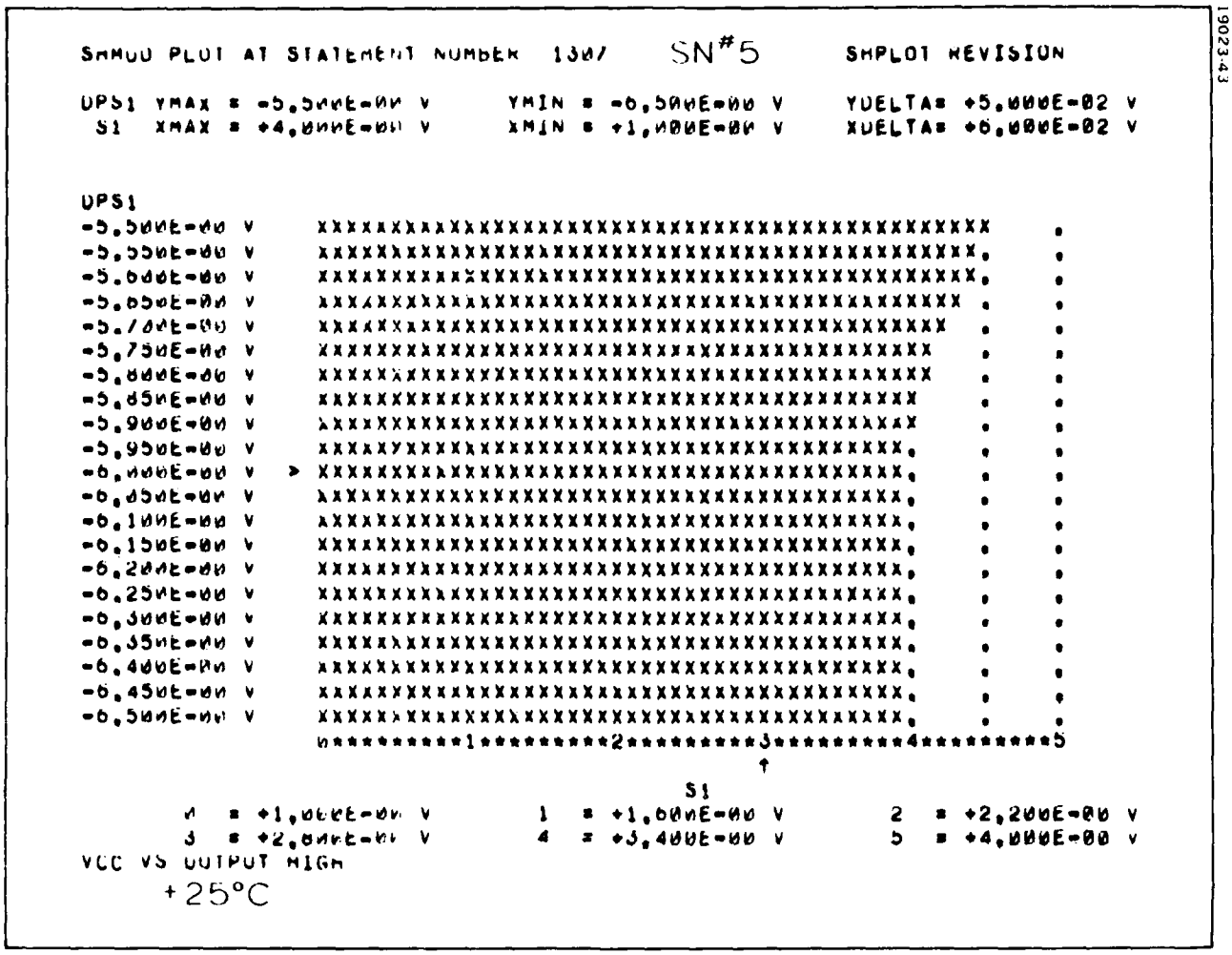


Figure 2-6. Device 93471 V_{cc} vs Data Output High at 25°C. Again this unit met specification requirements at 25°C.

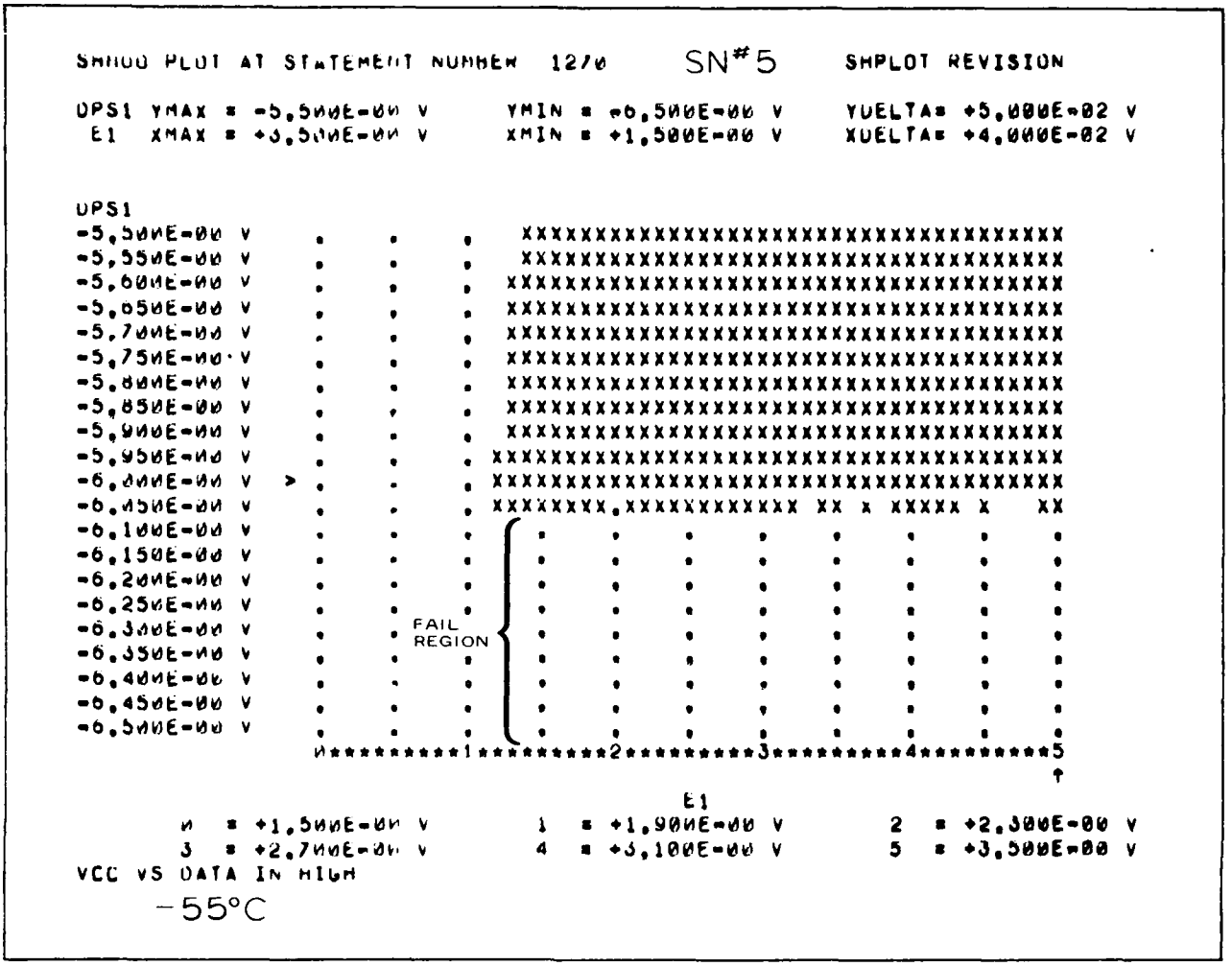


Figure 2-7. Device 93471 V_{cc} vs Data Input High at -55°C. The unit failed this test at -55°C when V_{cc} was below 5 volts.

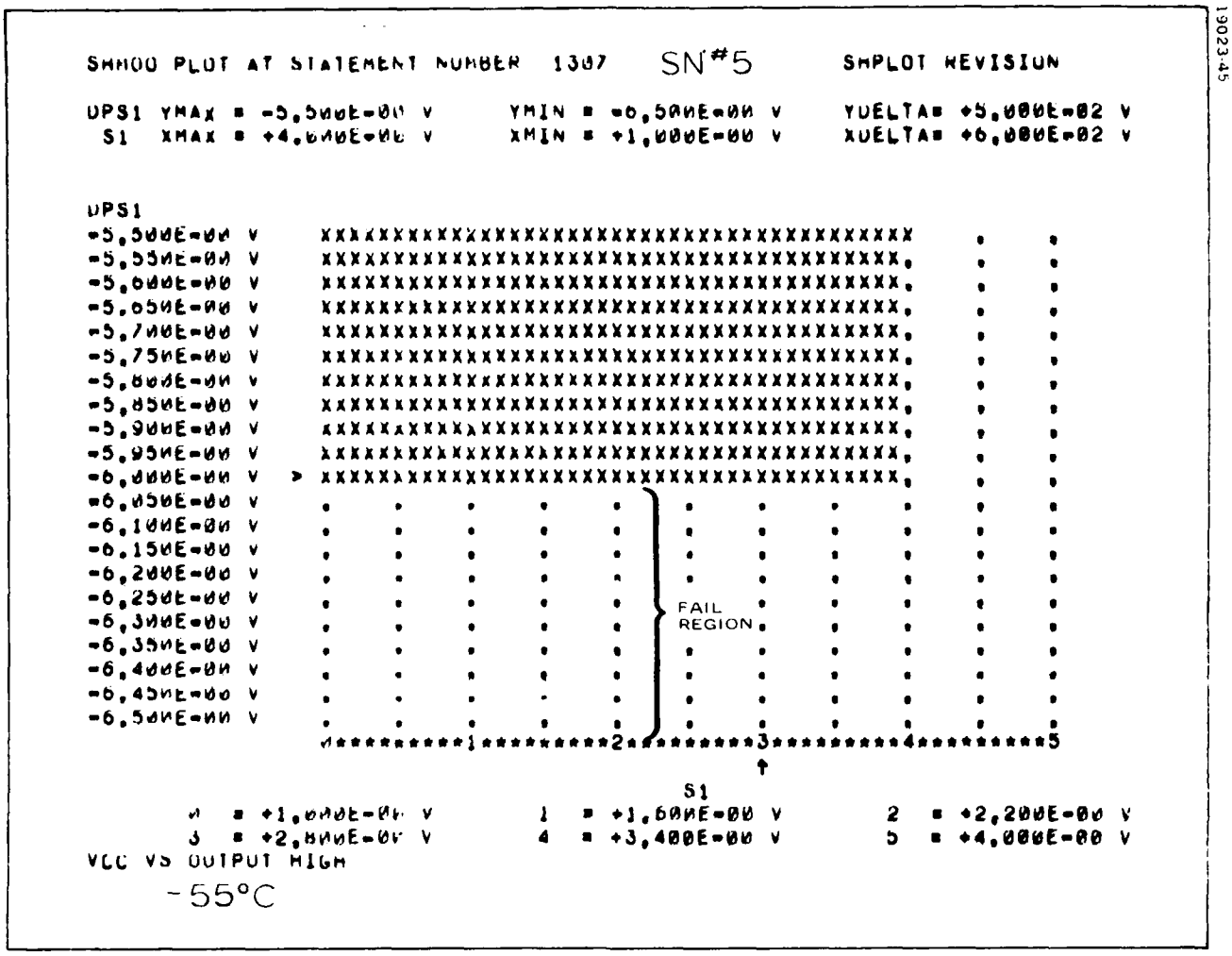


Figure 2-8. Device 93471 V_{cc} vs Data Output High at -55°C. This test was also a failure when V_{cc} was below 5 volts.

S6831B. The S6831B from vendor B is an alternate source for the 68316B ROM which is part of the 6800 microprocessor family. The 68316B from vendor H was not evaluated since the parts were not available at the time. The S6831B is a 2048x8 bit, static NMOS ROM that is mask programmable, and is pin compatible with the 2708 and 2716 EPROM's. The parts were programmed to a standard pattern used by the manufacturer for evaluation samples.

The device met all device parameter limits at the military temperature ranges. It should be noted that the DC V_{IH} is 2.0 Volts but the AC tests were specified with an input pulse of 2.4 Volts to 0.8 Volts. Electrical characterization of vendor B devices indicate that it can easily meet input pulse requirements of 2.0 and 0.8 volts for V_{IH} and V_{IL}, respectively.

2.3 Group II Fused PROM

The fuse Programmable Read Only Memory (PROM) is probably the simplest memory in its cell structure, compared to the mask programmed ROM. Each memory cell is again a simple transistor that is connected through a fuse to power or ground. The fuses are generally nichrome, titanium-tungsten, or polysilicon that can be blown open by an electrical power surge. Since the programming of the fuses can be done through the device package leads, the customer can easily choose his own program pattern using appropriate commercially available programming equipment. Most of the better programming equipments are capable of producing fuse programming yields of around 90% or better.

In order to check the fuse blowing characteristics of the devices at the factory, the PROM designers have resorted to establishing test fuses laid out internally within the memory cell area. The test fuses are usually laid out as an extra column and as an extra bit in each row. These test fuses are accessible from the outside package leads and the fuses are blown to see if the device is acceptable. A good test fuse blowing capability should assure the manufacturer and the customer that over 90% yield of good devices can be expected when the customer programs his PROM's.

The special leads used for electrically programming the PROMs are usually a dual-state device input. It is a normally functioning input or output pin when standard voltages are used, but for special test fuse programming, the input is stepped up to a higher voltage. Internal zener diodes bypass the normal circuits to activate the proper address decoding, and select the test fuses to be blown open.

Most memory devices that require fuse programming have stringent program pulse requirements. In addition, the electrical program pulse requirements are different for each vendor's device. The leading edge of the current pulse, amplitude, pulse width, number of pulse cycles are precisely defined in order to produce good, reliable opens in the fuses. Since the Sentry ATE is not designed to create or handle these unusual programming pulses, no attempt was made to use the Sentry for programming any of the devices. Commercial PROM programming equipment, or the suppliers factory programmer, was used to assure reasonable yields from the samples available for testing.

The quality of the programming performed by the commercial programming equipment will be reflected in the electrical test results performed by the user. It is important that a comprehensive electrical test at temperature extremes be performed to validate the programming operation. Outside of rigorous electrical tests, no attempts were made to evaluate the reliability consideration of the programming function by various programming equipment.

Prior to programming PROM's, all memory cells are checked to see if all the fuses are intact by addressing each cell while monitoring the outputs. All outputs for unprogrammed devices shall be either in the high state or low state depending upon the polarity chosen by the supplier. Any output that is not in the correct state at any address, most likely indicates an open fuse and is rejectable.

M3636. Vendor E's PROM M3636 is a polysilicon fused 2048x8 bit bipolar device that is supposed to be a military application device. Unfortunately, the devices that were tested had a limited range in V_{CC} of ±5%. All of the devices failed functional tests, or did not meet specifications at -55 °C if the V_{CC} range was set at -10% (+4.5 volts).

2.4 Group II PALs

Vendor I, recently introduced the fuse Programmable Logic Arrays (PAL's) family of AND-OR gates arranged in various functional organizations. The AND gates have programmable titanium-tungsten fuses, whereas the OR gates are fixed. This is the inverse of the PROM where the PROM has fixed "AND" gates but programmable "OR" gates. The PAL family utilizes Schottky TTL process and bipolar transistor devices. Figure 2-9 shows the basic cell structure of two "AND" array cells and a SEM photograph of details of the unprogrammed and programmed fuse. Unprogrammed PALs must have all of the fuses checked to make sure that none of them are blown or open. A fuse verification program has been implemented on the Sentry for a nonprogrammed PAL.

Functional test patterns were created for each part type to test every input transition completely separate from other input interactions. Each input was independently toggled from a 1 level to a 0 level, and a 0 level to a 1 level for every possible steady state condition of the relating inputs. A steady state condition for a given input occurs when there is a nonchanging 1 or 0 level at that input when another relating input changes, e.g., for a 2 input device, inputs A and B, input A can have two steady states when input B toggles, a 1 or a 0. For a 3 input device, inputs A, B, C, inputs A and B can have four steady states when input C toggles, 00, 01, 10, and 11. A relating input is an input that is in the same logic equation for a particular output. See Table 2-2 for the logic equations programmed into the devices for testing purposes.

All of the PAL devices were programmed at a local distributor using a DATA I/O Model 19 system. A programming yield of 39/61, (64%) indicates the relative immaturity of both the parts, and/or programming equipment. The PAL devices that were submitted worked over the required military temperature range. The parts are programmed with modern PROM programmers, and the blown fuse patterns verified by the programming equipment.

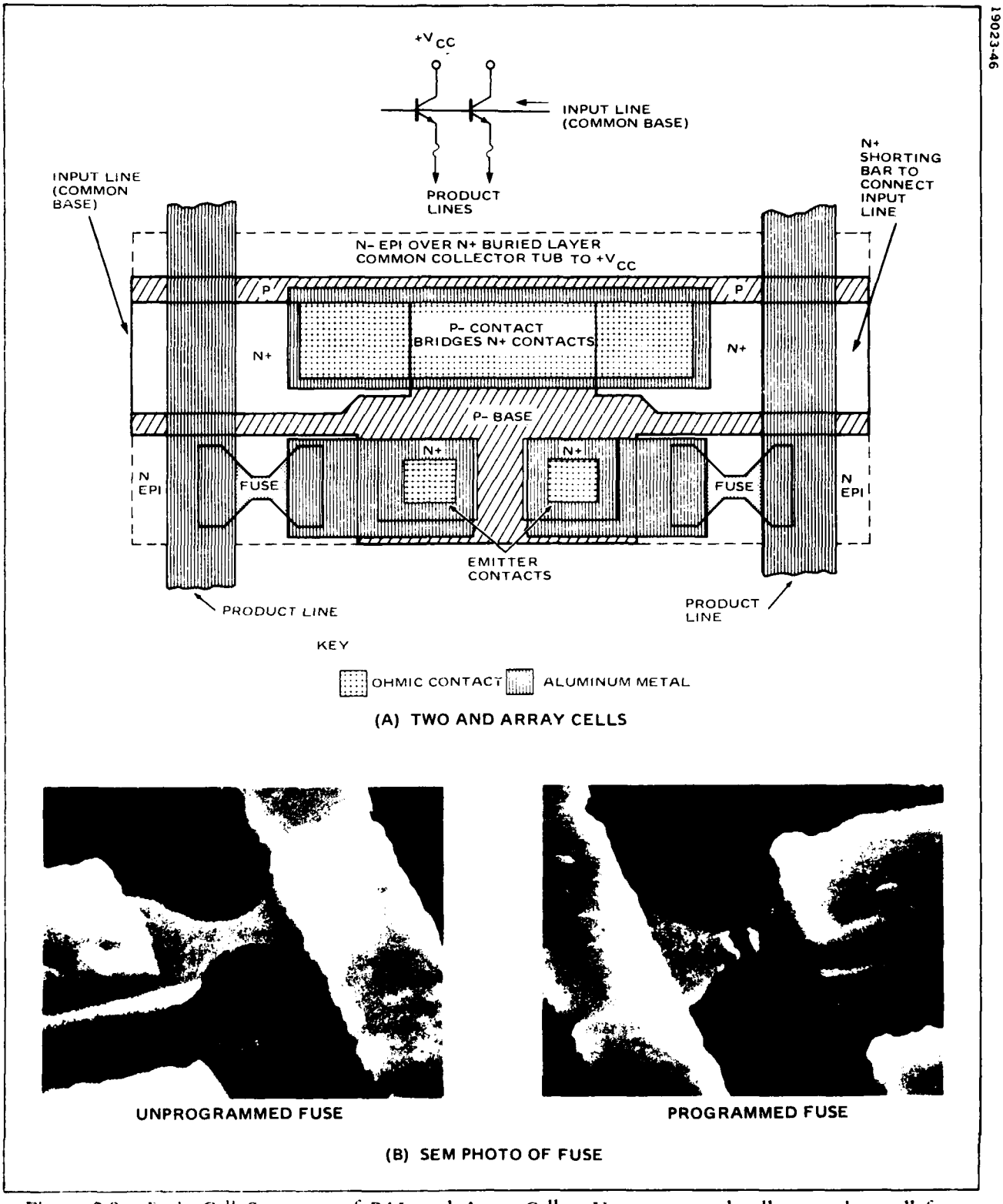


Figure 2-9. Basic Cell Structure of PAL and Array Cells. Unprogrammed cells must have all fuses checked to verify that none of them are blown or open. (Photo courtesy of MMI.)

TABLE 2-2 PART PROGRAMMING DATA

PAL10H8: 11 of 17 programmed, 10 correctly.	Output Pins - Input Pins 19 = 3 18 = 4 x 5 17 = 6 + 7 16 = 8 + 9 15 = "1" 14 = "0" 13 = "0" 12 = "0"
PAL12H6: 11 of 17 programmed, 11 correctly.	Output Pins - Input Pins 18 = 19 17 = 1 x 2 16 = 3 + 4 15 = (7 x 8) + (7 x 8); 7 ⊕ 8 14 = 9 + 11 + 12
PAL14H4: 7 of 13 programmed, 7 correctly.	Output Pins - Input Pins 17 = (2 x 4) + (2 x 8) 16 = (2 x 5) + (2 x 9) 15 = (2 x 6) + 2 14 = "0"
PAL16H2: 10 of 14 programmed, 6 correctly.	Output Pins - Input Pins 16 = (1x2x3) + (1x2x5) + (1x2x7) + (1x2x9) 15 = (1x2x4) + (1x2x6) + (1x2x8) + (1x2x1)

A good full ATE functional test of the programmed devices will satisfy verification of the fuse blowing as far as functionality of the programming sequence. The programming equipment verified that all unused fuses were intact, blown fuses were open and it differentiated between blown fuses and positions where no fuses exist (phantom fuses). The PALs with phantom fuses appear to the programming equipment as a partially programmed 512x4 PROM. Since all 2048 addresses are checked, the programming format also provided the expected pattern for verifying nonexistent fuse nodes. The logic equations defined the expected functional fuse patterns to be blown by the programming equipment. The advantage of a direct verification of the exact inside fuse pattern supplied knowledge on the remaining usable fuses. By knowing the remaining fuses it is possible to edit or modify the device if needed. It would be advantageous for an ATE functional verification to develop this fuse verification procedure.

Test Results. Two of the 10H8 parts had propagation times slightly out of specification at -55 °C. All of the other parameters were satisfactory. Two of the 12H6 devices failed V_{OL} at -55 °C. The same two devices showed that in the Schmoo plots involving V_{cc}, they would not function when near 4.5 volts. All 14H4 parts passed all the requirements. Two of the 16H2 parts had transient oscillation (ringing) of V_{OL} at -55 °C and +125 °C while one device showed the V_{OL} oscillation at +25 °C. The oscillation is shown in a typical Schmoo plot of device number 10 at -55 °C in Figure 2-10.

2.5 Group II. FPLA

Vendors M and C produce the bipolar Field Programmable Logic Array (FPLA) devices containing 48 AND terms (product terms) and 8 OR terms (sum terms). Each OR term controls an output function which can be programmed either true active high, or true active low. The true state of each output function is activated by a logical combination of 16 input variables, or their complements, up to 48 terms.

The FPLA is more complex than the PAL simply because it is a more general programmable logic array compared to the PAL. In fact, the FPLA is a combination of the PROM and PAL, but fully programmable at the AND gates, the OR gates, or even a choice of input/output polarity levels. The FPLA uses programmable nichrome fuses. Similar to the PROMs and PALs, the FPLA has internal test fuses to verify the fusibility of the fuses. The nonprogrammed devices can have all the fuses checked and, unlike the PALs, the vendors have provided a method of checking the status of each fuse in the set, separately from the programming equipment. This means of fuse verification outside of functional testing is extremely valuable in readily checking unused gates for programming additional functions.

82S100, 82S101. The only difference between the two FPLA types is that the former has tri-state outputs, while the latter has open collector outputs. These devices are rated to the military temperature range -55 °C to +125 °C. These parts, like the PROMs, are shipped in an unprogrammed state. In order to test the devices, 82S100 and 82S101 were programmed at the manufacturer's local field office using their programming equipment. A total of 19 of the 21 parts were correctly programmed for a 90% yield. Electrical programming of these devices is complex, since the output polarity-verify sequence, the AND matrix program-verify sequence and the OR matrix program-verify sequence are each unique and require different wave shapes and amplitudes as shown in Figure 2-11.

Of the 19 programmed parts, the majority met all electrical requirements of the specifications at the military temperature ranges. Four parts failed functional tests at -55 °C, primarily due to output transient ringing problems. Considerable time and effort was expended to make certain that the test equipment was not causing the ringing problem.

93459, 93458. As an alternate source for the FPLA, Vendor C uses an isoplanar device technology which makes these devices faster than Vendor M. However, the leakages are higher for the Vendor C devices. The detail slash sheet specifications reflect appropriate parameter limits to allow both vendor devices to meet all the requirements.

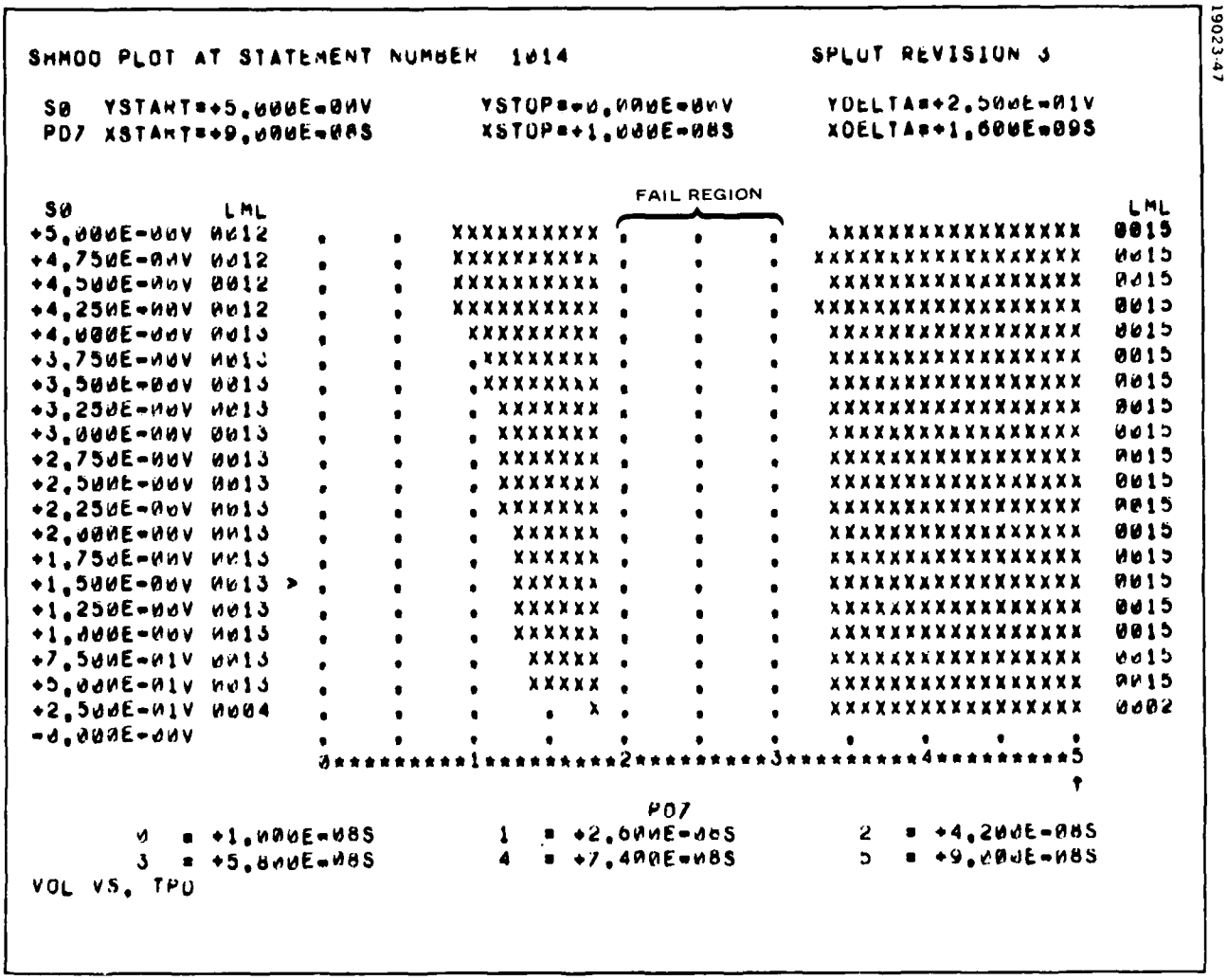
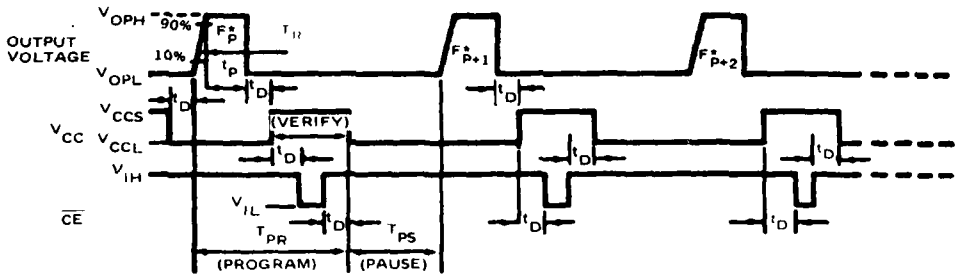
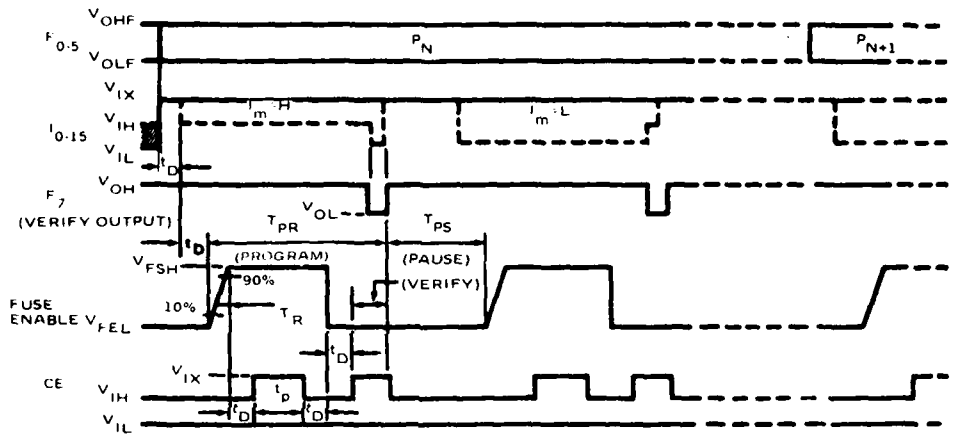


Figure 2-10. V_{OL} vs Propagation Delay of PAL 16H2 S.N. 7 at 25°C

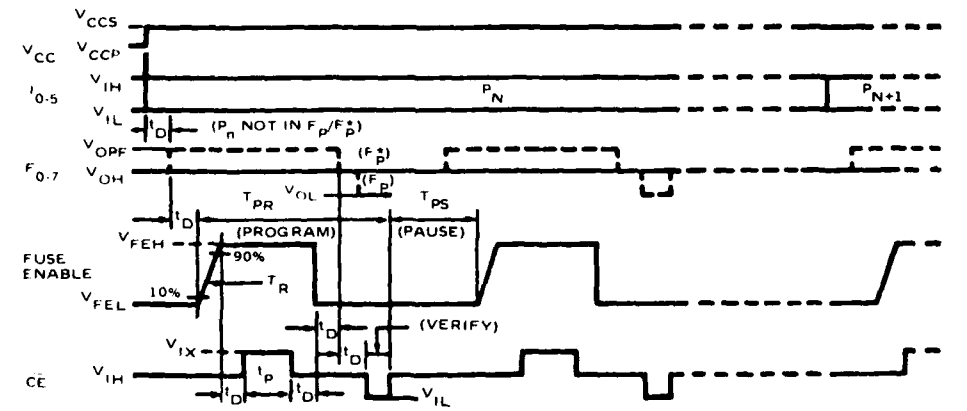


(A) OUTPUT POLARITY PROGRAM — VERIFY SEQUENCE

$V_{CC} = V_{CCP}$



(B) AND MATRIX PROGRAM — VERIFY SEQUENCE



(C) OR MATRIX PROGRAM — VERIFY SEQUENCE

Figure 2-11. FPLA Programming Waveforms. Each of these waveforms are unique for the function which makes electrical programming complex.

Considerable difficulty was encountered in trying to locate programming equipment to program these devices. Several devices were unsuccessfully programmed using a distributor's DATA I/O programmer, and new parts had to be procured, to replace them. These devices were finally taken to the supplier's plant, and programmed using factory equipment. All (20) parts were correctly programmed. Subsequent electrical tests indicated that these parts can easily be a second source product. There was only one part that was rejected, for not meeting the V_{OL} requirement.

2.6 Group III UV/EPROM

This third group of memories is distinguished by the fact that the PROM programming is accomplished by electrically storing a charge in the region of the FET gates of MOS devices. The Ultraviolet Erasable PROM (UV/EPROM) has a memory cell structurally configured with a single FET. However, the FET uses an unusual construction where a polysilicon gate floats above the FET between the source and drain. By using an avalanche technique, the electron charge is emitted from the drain region to the gate above, and the charges are trapped, since there are no electrical connections to the dielectrically isolated gate. The N channel FET now acts like a normal FET switch when proper gate voltages are applied and the gate threshold voltage V_t is overcome. For all practical purposes, the floating gate will maintain its charge for most quasi-permanent applications. Although the MNOS memory devices have a minimum, unpowered, data-retention specification of 10 years, no such specifications exist for UV/EPROMs. All indications point to the fact that UV/EPROMs will retain data at least as long as MNOS devices, but suppliers have not committed themselves to any kind of data retention tests. Therefore, it cannot be stated unequivocally that these memories will store data permanently.

To erase the memory, the entire memory cell area is exposed to ultraviolet light which discharges the floating gates to the substrate. The erasing is performed off-line, or out of the equipment, with the device placed under an ultraviolet source.

A rudimentary examination was made of the ultraviolet erasing equipment that was utilized during in-house operations. There appears to be a sufficient safety factor in the specified erasing time for this operation, and erasing should not be a problem if the operational rules are followed. The UV/EPROMs are placed in a holder that slides to within 0.722 inches from the ultraviolet lamp source. The exposure time recommended for this particular equipment (Ultraviolet Products Inc., Mineral Lamp Model S52-T) is a minimum of 20 minutes. In an effort to determine how much guard band was used, a minimum exposure time of four minutes was achieved on five M2716 devices. The programmed pattern was a checkerboard.

M2716. Evaluation of Vendor E's 2048x8 UV/EPROM indicated that it can meet all of its specifications. However, the upper temperature limit was set at 100 °C by the vendor. The parts will not meet specifications beyond 100 °C. All the parts were programmed and erased satisfactorily using an in-house DATA I/O programmer. The worst case DC V_{IH} and V_{IL} was 2.0 volts and 0.8 volts, respectively. The AC parameters were tested with V_{IH} and V_{IL} at 2.0 volts and 0.45 volts, respectively, as specified by the supplier.

MM2716. Vendor J's UV/EPROM claimed capabilities to +125 °C. Subsequent testing and electrical characterization revealed that the device met all electrical specification parameters at the +125 °C limit. Since extended life testing to determine data retention capabilities at 125 °C was not attempted, further evaluation in this area remains to be investigated. All parts erased and programmed satisfactorily. The worst case DC V_{IH} and V_{IL} was 2.0 volts and 0.8 volts. The AC parameters were tested with V_{IH} and V_{IL} at 2.2 volts and 0.45 volts, respectively, as specified by the supplier.

It should be noted that when specifying the input signals required for AC parameters and functional testing, most vendors use higher pulses than the specified DC V_{IH} and V_{IL} levels. The rationale is that when making switching parameters and propagation measurements, they want to make certain that clean input pulse signals are utilized.

TMS2532. A 4Kx8 UV/EPROM from Vendor N was evaluated. This device was tested through the full military temperature range. Erasing and programming was satisfactory. Electrical tests, characterizations and functional tests did not reveal any unusual traits, and the device met all specifications. The DC and AC V_{IH} and V_{OL} were specified at 2.2 volts and 0.65 volts. It should be noted that the vendor did not use the more standard 2.0 volts and 0.8 volts for V_{IH} and V_{IL}. It should be pointed out that not all suppliers of MOS devices are trying to meet the worst case output drive capabilities of TTL circuits.

IM6654. This was the only CMOS part evaluated, and it features a 512x8 memory organization. UV erasing and subsequent electrical programming was satisfactory. DC and AC parameter tests, electrical characterizations and functional testing was performed. All parts satisfactorily met the specification limits. It should be noted however that the DC V_{IH} is specified at 2.5 volts and 2.7 volts for address inputs. Again, it must be pointed out that MOS and CMOS suppliers are not making a very determined effort to be compatible with TTL drivers.

2.7 Group III EAROM

The Electrically Alterable Read Only Memory (EAROM) depends upon storing electronic charge in the gate region of the MOS FET. Both vendors D and K supply the EAROMs as a P channel device with a non volatile FET memory cell transistor made of a Metal Nitride Oxide Silicon (MNOS) sandwich, as shown in Figure 2-12. The MNOS FET is located between two normal MOS devices as shown in Figure 2-13. The electronic charge is stored at the interface between the nitride-silicon dioxide sandwich under the metal gate. When a high electric field is produced from the gate to substrate, electron charges tunnel through a very thin silicon dioxide to the nitride interface where they are trapped. When there are sufficient charges at the gate interface to reach a designed threshold point V_t, the memory FET then acts like a normal FET switch similar to the UV/EPROM memory cell. Erasing is accomplished electrically by reversing the polarity of the gate to substrate voltage, and using a high electric field.

The MNOS FET is constructed in a trigate fashion (see Figure 2-13) with two normal MOS FETS on either side to prevent the memory FET from becoming a depletion mode transistor. The normal MOS FET will cut off and isolate the

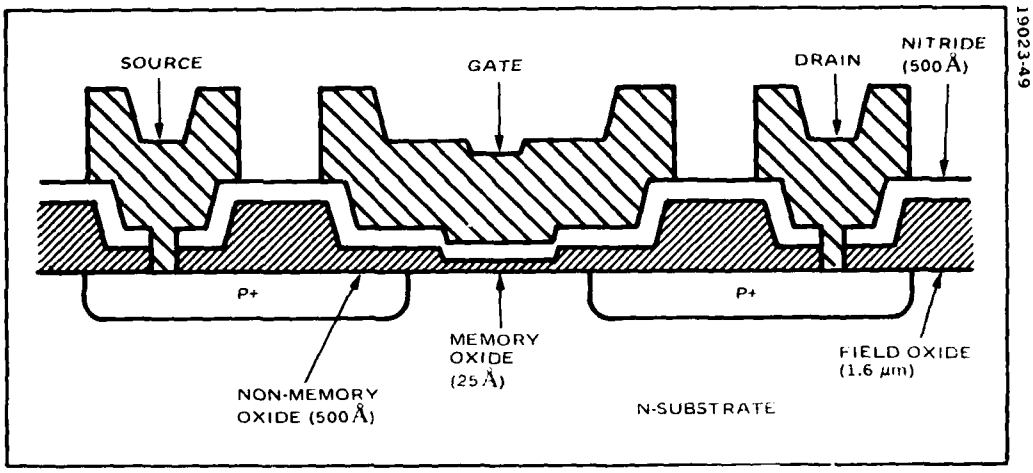


Figure 2-12. Tri-Gate MNOS Transistor

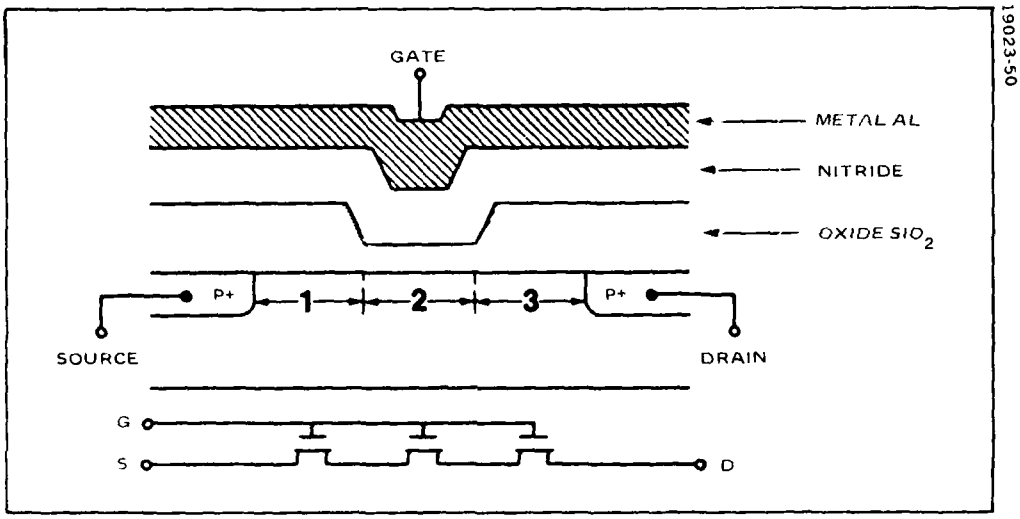


Figure 2-13. MNOS Tri-Gate Structure

memory FET when the gate voltage goes positive, thus preventing the memory FET from being charged in the positive direction above ground when the memory is being erased.

Using a single trigate FET for the basic memory cell, the output is read differentially by comparing against a reference MOS FET externally biased with the signal V_R. Figure 2-14 shows this read operation. The area within the dotted line indicates the memory cell area which is diode isolated from the rest of the chip, so that erase drive can be accomplished.

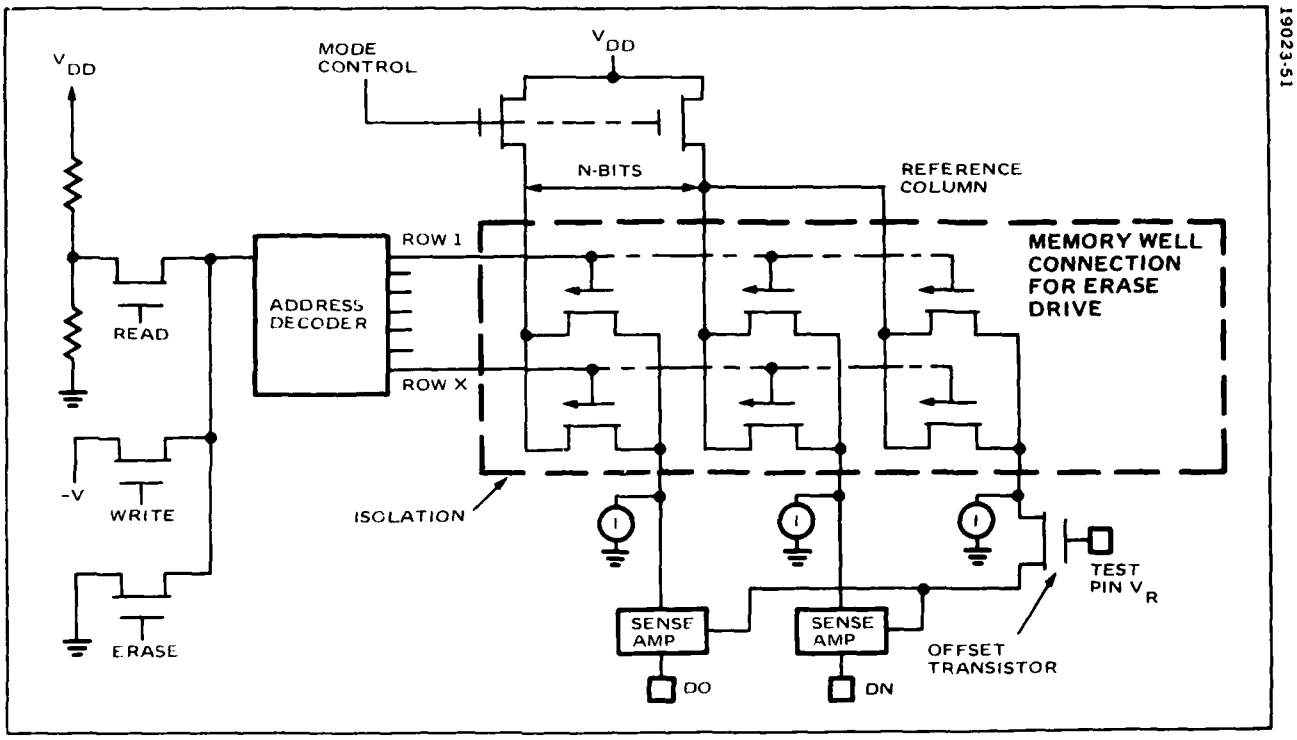


Figure 2-14. MNOS Memory Read Diagram

Due to the necessity to reverse the memory FET gate voltage polarity, this type of memory is physically and electrically complex. This memory is comparatively less dense than other memories, because wider line and diffusion spacings were utilized. The wider spacing is necessary to support the higher voltages (30V) that is necessary for this particular process. Also these MNOS devices have some unique general characteristics that should be briefly reviewed in order to appreciate the rather involved detailed part specification that resulted.

- Unpowered data storage time – 10 years minimum.
- Read access time – 1.5 microseconds maximum.
- Write time – 10 millisecond minimum.
- Erase time – 100 millisecond minimum.
- 2×10^{11} minimum read access (N_{RA}) before reprogramming.
- 10^4 minimum write cycles (N_W).
- V_R – Reference voltage for memory cells that allow differential read out to the sense amplifier input.
- Voltages – ±5.0 volts, -14.0 volts, -24.0 volts.

Data storage time in an unpowered state is specified to last for 10 years minimum at nominal temperature. To verify this nonvolatility, an accelerated life test should be run at high temperature in an unpowered condition.

Read access time, write time and erase times are self explanatory except that write time is accomplished with a series of pulses that total a minimum write period of 10 milliseconds.

There is a slight degradation of the memory cells threshold voltages when a cell is read. Therefore, a minimum of 2×10^{11} read accesses are specified before reprogramming is necessary. The read disturb life test is performed to verify that the devices are capable of the minimum N_{RA} read accesses. The reference voltage V_R can be adjusted to determine the 1 and 0 limits of the memory cells. If the 1 and 0 margin becomes too narrow, the device needs to be reprogrammed. The 1 and 0 voltage values at the critical threshold points can be plotted on semilog paper showing the memory cell V_t degradation slope as a function of the number of read cycles. The foregoing action of varying the V_R voltage to determine a memory cell threshold voltage is also called the threshold test.

N_W is the number of erase-write (program) cycles that can be performed before permanent degradation of the memory FET's occurs. Again, the V_R can be used as a tool and the memory FET's thresholds or V_t plotted on the same semilog paper showing the degradation slope as a function of number of the programming cycles.

Due to the fact that these parts are P channel devices, the required voltages are all negative. The +5.0 Volts is used on the substrate to allow TTL output compatibility.

Considering the high complexity of these device, Vendor D's product is relatively mature, and the yields appear to be under reasonable control. Vendor K is relatively new in producing this particular product, and is apparently having more difficulty in meeting the requirements. All tests for erasing, writing and reading were accomplished on the Sentry tester.

2810. Tests and characterization of Vendor D's 2048x4 bit memory device were satisfactory. All tests were run at the specified military temperatures of -55 °C to +125 °C. Bulk erasing and selective writing by 4 bit words were performed using the Sentry tester.

Since these devices require a V_{IH} input signal of 3.0 volts minimum, external pull up resistors must be used if TTL devices are used for inputs. TTL drivers can only guarantee worst case minimum output voltage capability of 2.4 volts. V_{IL} = 0.8 volts maximum. AC input requirements are the same as DC inputs. The data output is TTL compatible, but is not a true static output, and cannot hold its output levels indefinitely. The ϕ clock must be activated within 40 microseconds to hold the device static output level. This output is similar to the 4104 quasi-static RAM.

7810. Vendor K is an alternate source to Vendor D on this 2810 part. However, the parts were not as consistent in meeting all the parameter requirements. This is probably due to the fact that the vendor had just started delivering sample devices to interested customers, and the parts were relatively new. However, of the sample parts (11 of 15) showed enough functional and device parameter yield capability that by the time these devices are ready for qualification testing and evaluation, supplier K's production process should have device yields under reasonable control.

Section 3

MIL-M-38510 DETAIL SPECIFICATIONS

Table 3-1 lists all of the memory devices that were evaluated by this contract, including the ones in which actual drafts of the detail specifications were written. It should be noted that a slash sheet was written for the IM6654 CMOS UV/EPROM, but a number was not assigned at this time. A total of ten detail specifications for MIL-M-38510 were written.

In Table 3-1, the first four parts were utilized to create 5 dash numbers within the basic 238 slash sheet categorized by memory organization and speed of memory access time. The 4104 was fully tested and characterized, but it was not requested that a specification be written. The S6810 and MC6810 RAMs represent two sources for the same type of device. The 27S07A and 27S03A represent a noninverting and an inverting output as two separate dash numbers for the 260 slash sheet. The 93470, 93471 bipolar RAMs were specially tested as requested by RADC. The "cold start" problem below -30 °C was investigated for RADC. The 4044 and 40L45 could not meet their own specification, therefore were eliminated from the programs. The S6831B ROM was successfully evaluated by using an evaluation mask programmed device from the supplier. The M3636 bipolar PROM was fully evaluated as per RADC request, but no specification was written since one already exists.

The next group of four PAL devices are part of a family of programmable logic array devices of which four dash numbers were created. The two FPLA devices are alternate sources for the slash 502 specification. The M2716 and MM2716 devices are alternate sources for the slash 221 specification. The TMS2532 device is a single source part for the slash 222 specification. As mentioned earlier, no detail specification number has been assigned to the IM6654 part. The ER2810 and 7810 devices are alternate sources for the slash 225 specification.

No special test methods were written for MIL-STD-883. One possible candidate for inclusion might be the memory retention test for nonvolatile memories. The so called UV/EPROMs, EAROMs, and the new EEROMs are all nonvolatile memories. However, the term nonvolatile for these semiconductor devices is a qualified term because all three devices cannot hold charges in the gate regions indefinitely when compared with magnetic memories. Memory retention capabilities can be broken down at the present time as a function of: (1) unpowered, static data retention, (2) data retention after a number of read cycles, (3) data retention after a number of erase-write cycles, or (4) a

TABLE 3-1. LISTING OF SEMICONDUCTOR MEMORIES CHARACTERIZED

Part Number	Part Description	Draft of MIL-M-38510 Detail Spec	Supplier
2147, M2147	4Kx1 MOS Static RAM	/238	E
2147H-1, 2147H-2	4Kx1 MOS Static RAM	/238	E
2114, M2114	1Kx4 MOS Static RAM	/238	E
2148	1Kx4 MOS Static RAM	/238	E
4104	4Kx1 MOS Static RAM	-	G
S6810	128x8 MOS Static RAM	/402	B
MC6810	128x8 MOS Static RAM	/402	H
27S07A (29701)	16x4 ECL Static RAM	/260	A
27S03A	16x4 ECL Static RAM	/260	A
93470, 93471	4Kx1 Bi-Polar Static RAM	/233 2/	C
4044	4Kx1 MOS Static RAM	-	N
40L45	1Kx4 MOS Static RAM	-	N
S6831B (68316E)	2Kx8 MOS Static ROM	/403	B
M3636	2Kx8 Bi-Polar PROM	/210 2/	E
PAL 10H8	10x8 PAL	/503	I
PAL12H6	12x6 PAL	/503	I
PAL14H4	14x4 PAL	/503	I
PAL16H2	16x2 PAL	/503	I
82S100, 82S101	16x48x8 FPAL	/502	M
93459, 93458	16x48x8 FPAL	/502	C
M2716	2Kx8 MOS UV/EPROM	/221	E
MM2716	2Kx8 MOS UV/EPROM	/221	J
TMS2532	4Kx8 MOS UV/EPROM	/222	N
IM6654	512x8 CMOS UV/EPROM	1/	F
ER2810	1Kx4 MNOS EAROM	/225	D
7810	2Kx4 MNOS EAROM	/225	K

Vendor Code

Code	Vendor
A	AMD
B	AMI
C	FAIRCHILD
D	G.I.
E	INTEL
F	INTERSIL
G	MOSTEK
H	MOTOROLA
I	MMI
J	NATIONAL SEMI.
K	NITRON
L	RCA
M	SIGNETICS
N	TI

1/ Detail specification not assigned yet.
2/ Not written in this study.

combination of all three. It is not clear at this time if one test method can be written to satisfy all three operational conditions for all three device types. This will require further investigation of test methods.

Section 4

CONCLUSIONS AND RECOMMENDATIONS

The majority of parts evaluated were satisfactory, and those which were not were obviously incapable of meeting the specified requirements.

One potential problem became evident, after evaluating most of the vendor furnished memory specifications. There is an apparent nonstandardization trend on input/output parameters. When microcircuits were originally introduced several years ago, there was a strong effort to standardize the input and output requirements so that healthy noise margins could be predicted. DTL and TTL microcircuits were particularly well defined on DC noise margins. However, with the advent of MOS LSI microcircuits and memories, the input/output level requirements started to become ambiguous due to conflicting needs and capabilities.

Most periphery support circuits for microprocessors and MOS memories have been TTL circuits. MOS circuits have had difficulty responding to the low level output voltages levels of TTL, particularly when the TTL driver is fully DC loaded (V_{IH} = 2.0 volts). Many of the suppliers have designed their MOS circuits for higher input voltages, and even higher voltages for pulsed inputs for functional and switching parameter measurements.

It is recommended at this time, that a study be undertaken to determine if input and output DC voltage levels and pulse inputs can be standardized. Such a study would also investigate what the near future portrays for input/output requirements when MOS threshold levels go lower, and supply voltage falls below 5.0 volts to 3.0 or 1.5 volts.

Appendix A

SELECTED SENTRY ATE TEST PRINTOUTS

DISCUSSION ON SENTRY TEST PRINTOUTS ON 2148 STATIC RAM

SENTRY ATE test data printouts of functional, AC parameters, Schmoo plots and DC parameters for the 2148 Static RAM serial number 9 are shown in the following pages. These measured data and characterization plots at the military temperature extremes of -55 °C and +125 °C are typical of the tests conducted and the data gathered for each of the 26 devices tested during the conduct of these tests.

Figure A-1 shows the basic timing diagram used for the Schmoo plots in the appendix. Most of the plots have self explanatory headings, however, there are two terms that needs further definition, delay and width. Delay means that the signal moves both leading and trailing edges simultaneously delayed in time. The term width means that the signal moves only the trailing edge. The ATE timing starts at 100 ns, and the printout of timing plots shows this number. The timing diagram shows that real time "0" starts at 120 nSec of the ATE timing diagram. This adjustment for real time must be made when reading timing plots in the horizontal scale.

Figures A-2 and A-3 show the results of functional and AC parameter tests at -55° C and +125° C respectively. Figures A-4 through A-35 show examples of Schmoo plots of various device parameters as a function of time or V_{CC}, and temperature. Figure A-36 and A-37 show the results of DC parameter tests at -55° C and +125° C respectively.

The test data and Schmoo plots for this particular sample part (2148) have been included in this appendix because they show a failure at high temperature for access time T_{AA} and T_{ACSI} in Figure A-3. The failures occur because the original test limit was set for the vendor specification limit of 70 ns, and measurements indicate 72.3 ns and 71.5 ns respectively. This access time failure can also be seen in the Schmoo plot in Figure A-15. It shows the plot of address access time (strobe) in the horizontal time scale, and every thing left of 200 ns equivalent to 80 ns real time, is a failure. In this particular example, the access time limit T_{AA} was marked at 90 ns instead of 70 ns. The final mil specification limit was also set at 90 ns for this access time parameter.

The hand encircled data points in the plots were inserted to visually indicate where the specification limits occur in relation to the plotted data.

The Schmoo plots (Figures A-24 through A-35), showing the supply voltage V_{CC} on the left vertical scale, must be converted to obtain the correct voltage by adding +11.0 volts. For example, in Figure A-24, the top of the left vertical column should read +11.0 volts - 5.5 volts = +5.5V. The bottom of the scale should read +11.0 volts - 6.5 volts = +4.5 volts.

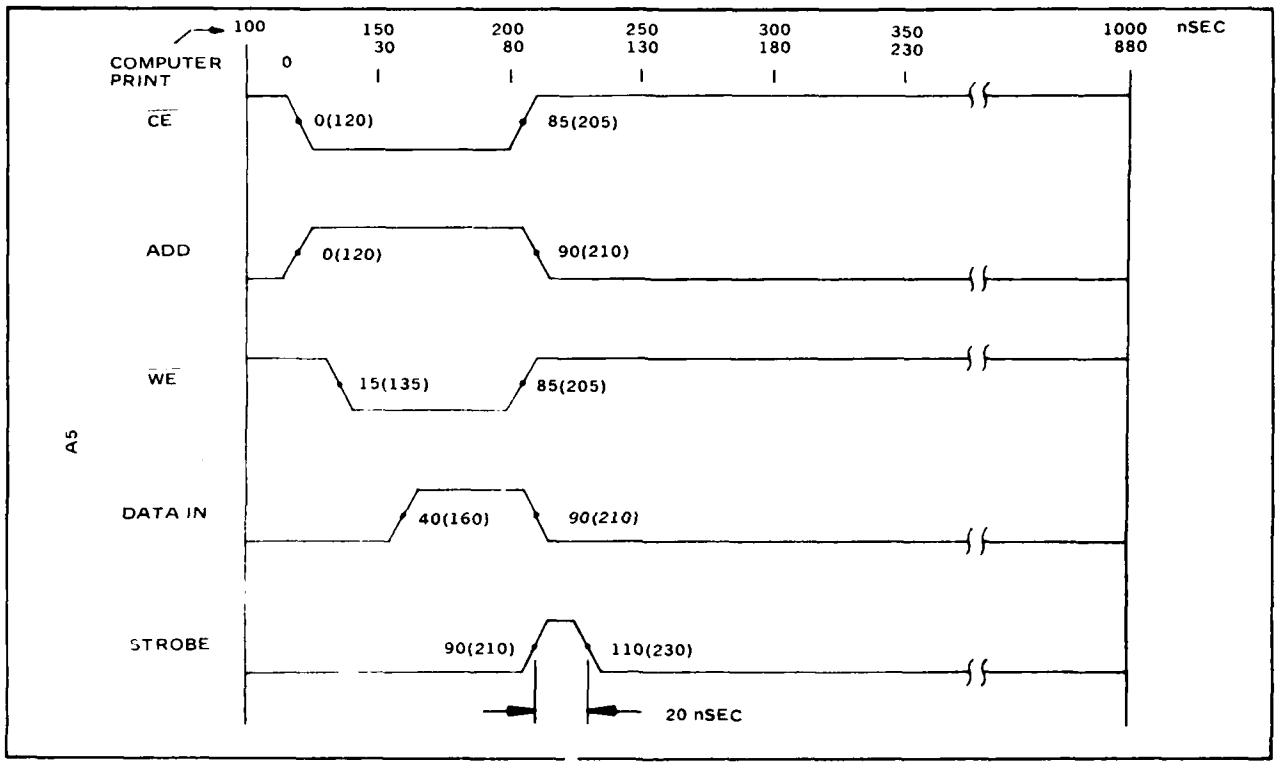


Figure A-1. Basic Shmoo Plot Timing Waveform for 2148. A delay moves both leading and trailing edges while a variable pulsewidth moves trailing edges only.

```
STATIC       TEST PLAN  21481        SN        9

          2148                                  TAA - ADDRESS ACCESS TIME
          DATE :  3/25/88                        PIN  1=  +3.824E-08
          -55 DEGREES C
          SERIAL #  9                           TACS1 - CHIP SELECT ACCESS TIME
                                                 PIN  1=  +4.216E-08
          FUNCTIONAL TEST
           PASSED ZEROS                         TACS2 - CHIP SELECT ACCESS TIME
           PASSED ONES                           PIN  1=  +4.216E-08
           PASSED CHECK
           PASSED NCHECK
           PASSED DIAG
           PASSED NDIAG
           PASSED MARCH
           PASSED NMARCH
           PASSED PING-PONG
           PASSED NPING-PONG
           PASSED N3/2 PATTERN
          *** PASSED ALL PATTERNS ***
```

19023-2

Figure A-2. Functional and AC Parameter Tests at -55°C

```
STATIC       TEST PLAN  21481        SN        9

          2148
          DATE :  3/25/88
          125 DEGREES C
          SERIAL #  9

          FUNCTIONAL TEST          TAA - ADDRESS ACCESS TIME
           PASSED ZEROS             PIN  1=  +7.232E-08  S/B<   +7.000E-08 FAIL
           PASSED ONES
           PASSED CHECK            TACS1 - CHIP SELECT ACCESS TIME
           PASSED NCHECK            PIN  1=  +7.152E-08  S/B<   +7.000E-08 FAIL
           PASSED DIAG
           PASSED NDIAG            TACS2 - CHIP SELECT ACCESS TIME
           PASSED MARCH             PIN  1=  +6.904E-08
           PASSED NMARCH
           PASSED PING-PONG
           PASSED NPING-PONG
           PASSED N3/2 PATTERN
          *** PASSED ALL PATTERNS ***
```

19023-3

Figure A-3. Functional and AC Tests at +125°C

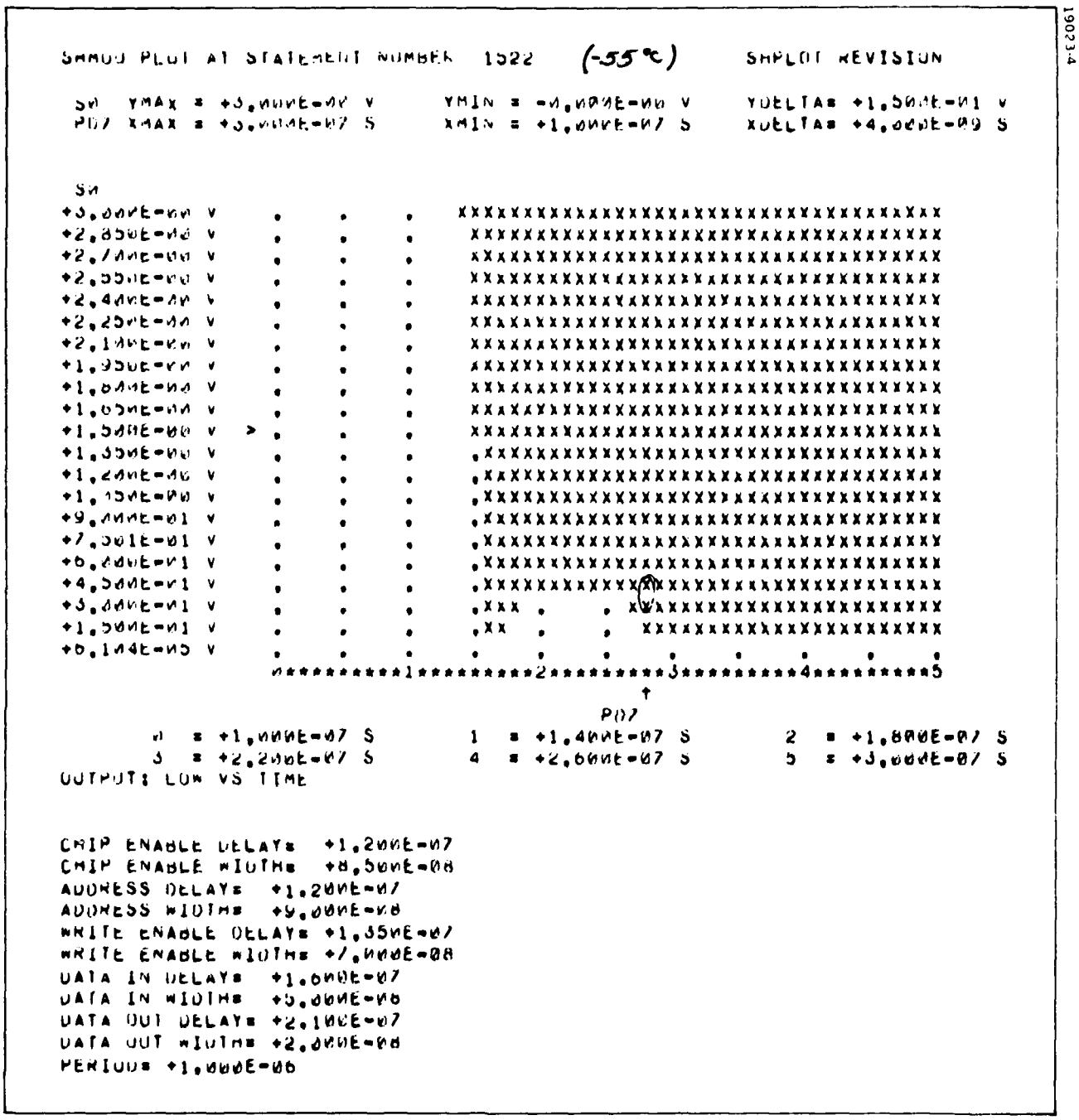


Figure A-4. Sentry Shmoo Plot of Device 2148 – Output Low vs Time at -55°C

```
SHMOO PLOT AT STATEMENT NUMBER  1522   (+125°C)      SHPLOT REVISION

 S0  YMAX = +3,000E-00 V      YMIN = -0,000E-00 V     YDELTA= +1,500E-01 V
 PD7 XMAX = +3,000E-07 S      XMIN = +1,000E-07 S     XDELTA= +4,000E-09 S


 S0
+3,000E-00 V     .     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXX
+2,850E-00 V     .     .     .     .     . XXXXXXXXXXXXXXXXXXXXXXXXXX
+2,700E-00 V     .     .     .     .     . XXXXXXXXXXXXXXXXXXXXXXXXXX
+2,550E-00 V     .     .     .     .     . XXXXXXXXXXXXXXXXXXXXXXXXXX
+2,400E-00 V     .     .     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXX
+2,250E-00 V     .     .     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXX
+2,100E-00 V     .     .     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXX
+1,950E-00 V     .     .     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXX
+1,800E-00 V     .     .     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXX
+1,650E-00 V     .     .     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXX
+1,500E-00 V   > .     .     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXX
+1,350E-00 V     .     .     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXX
+1,200E-00 V     .     .     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXX
+1,050E-00 V     .     .     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXX
+9,000E-01 V     .     .     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXX
+7,501E-01 V     .     .     .     .     .    XXXXXXXXXXXXXXXXXXXXXXX
+6,000E-01 V     .     .     .     .     .    XXXXXXXXXXXXXXXXXXXXXXX
+4,500E-01 V     .     .     .     .     .    XXXXXXXXXXXXXXXXXXXXXXX
+3,000E-01 V     .     .     .     .     .    XXXXXXXXXXXXXXXXXXXXXXX
+1,500E-01 V     .     .     .     .     .    .XXXXXXXXXXXXXXXXXXXXXXX
+6,104E-05 V     .     .     .     .     .    .XXXXXXXXXXXXXXXXXXXXXXX
               0*********1*********2*********3*********4*********5
                                      ↑
                                     PD7
       0  = +1,000E-07 S        1  = +1,400E-07 S        2  = +1,800E-07 S
       3  = +2,200E-07 S        4  = +2,600E-07 S        5  = +3,000E-07 S
OUTPUT: LOW VS TIME


CHIP ENABLE DELAY=  +1,200E-07
CHIP ENABLE WIDTH=  +8,500E-08
ADDRESS DELAY=  +1,200E-07
ADDRESS WIDTH=  +9,000E-08
WRITE ENABLE DELAY= +1,350E-07
WRITE ENABLE WIDTH= +7,000E-08
DATA IN DELAY=  +1,600E-07
DATA IN WIDTH=  +5,000E-08
DATA OUT DELAY= +2,100E-07
DATA OUT WIDTH= +2,000E-08
PERIOD= +1,000E-06
```

Figure A-5. Sentry Shmoo Plot of Device 2148 – Output Low vs Time at +125°C

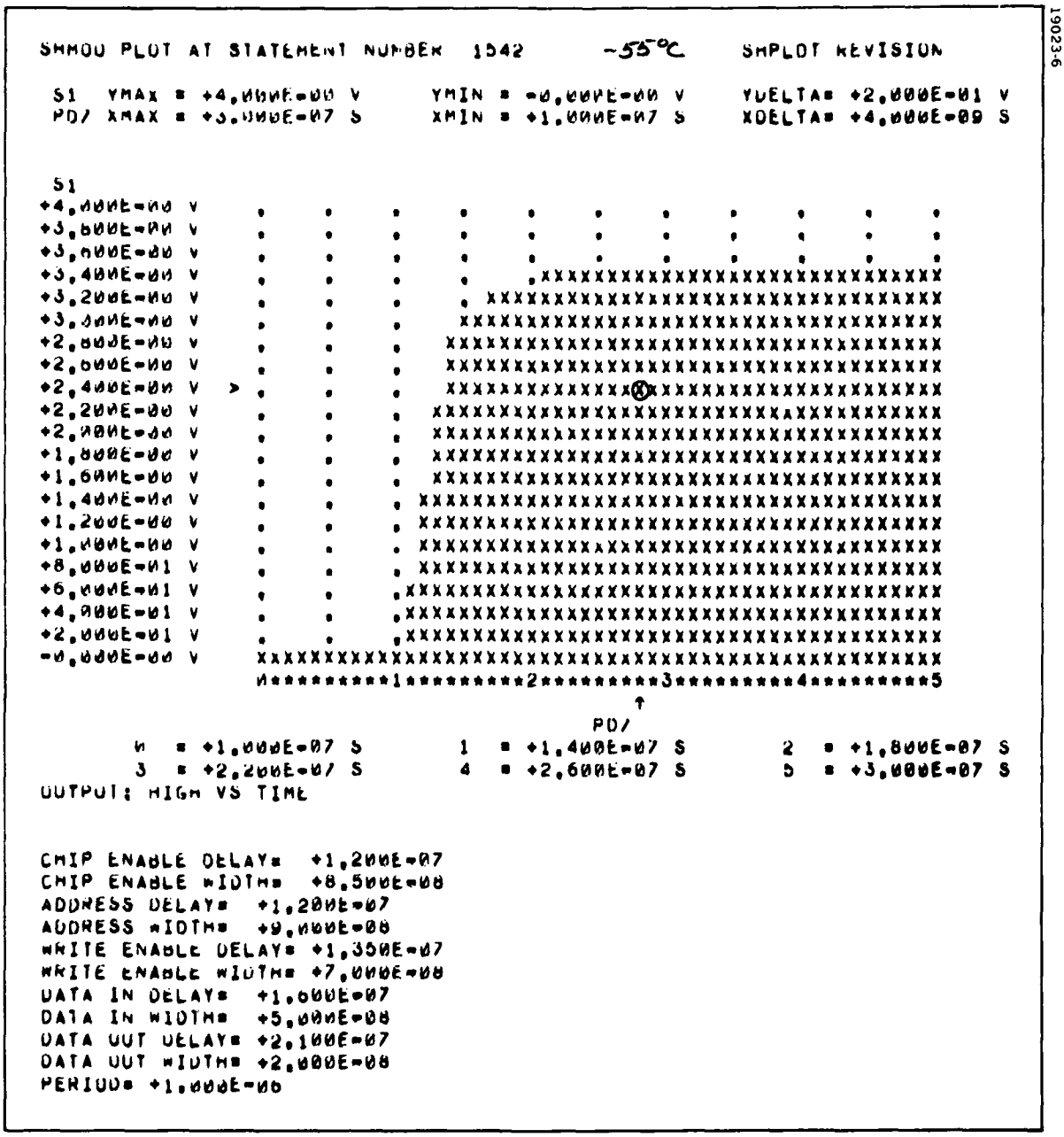


Figure A-6. Sentry Shmoo Plot of Device 2148 – Output High vs Time at -55°C

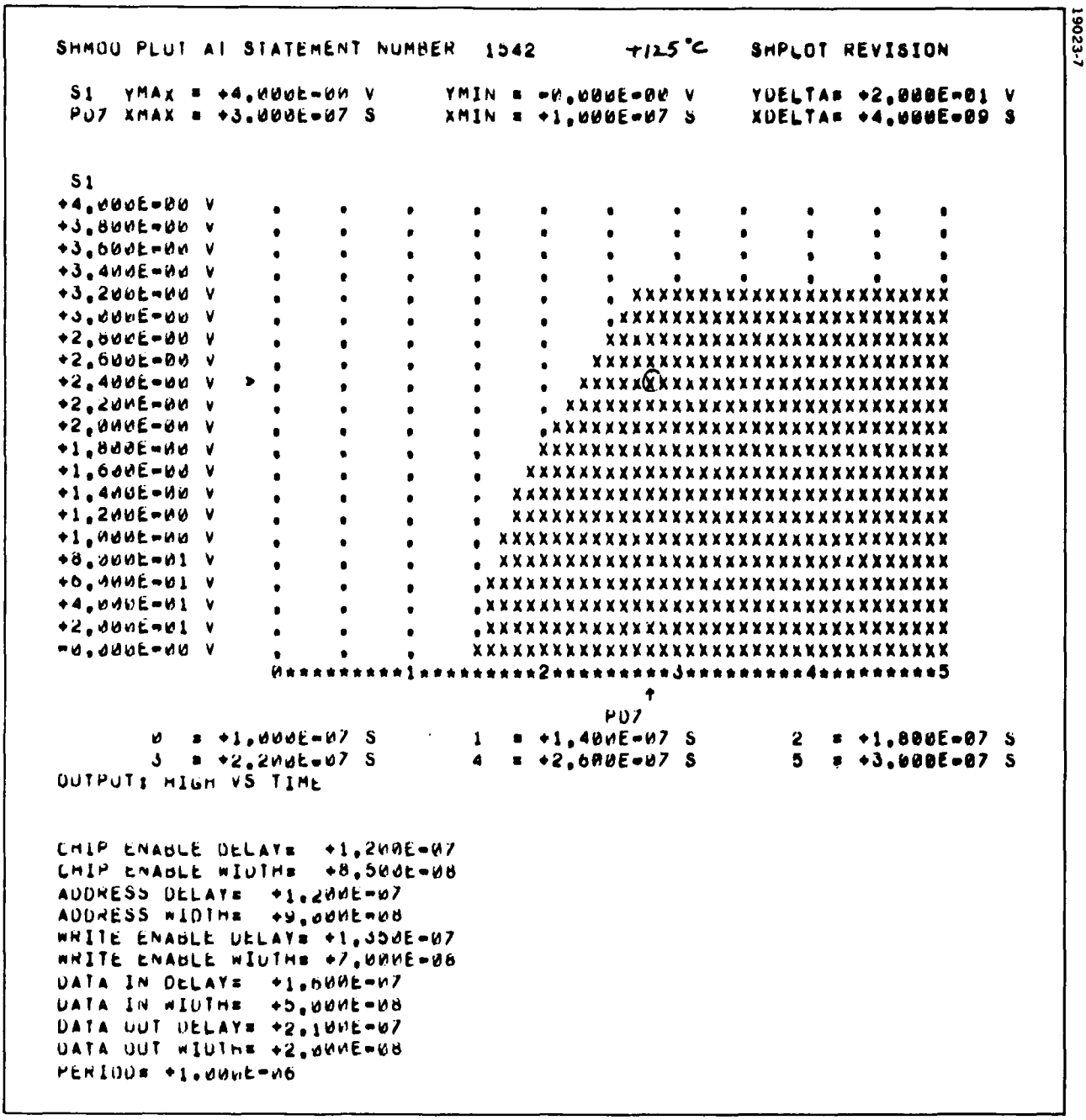


Figure A-7. Sentry Shmoo Plot of Device 2148 – Output High vs Time at +125°C

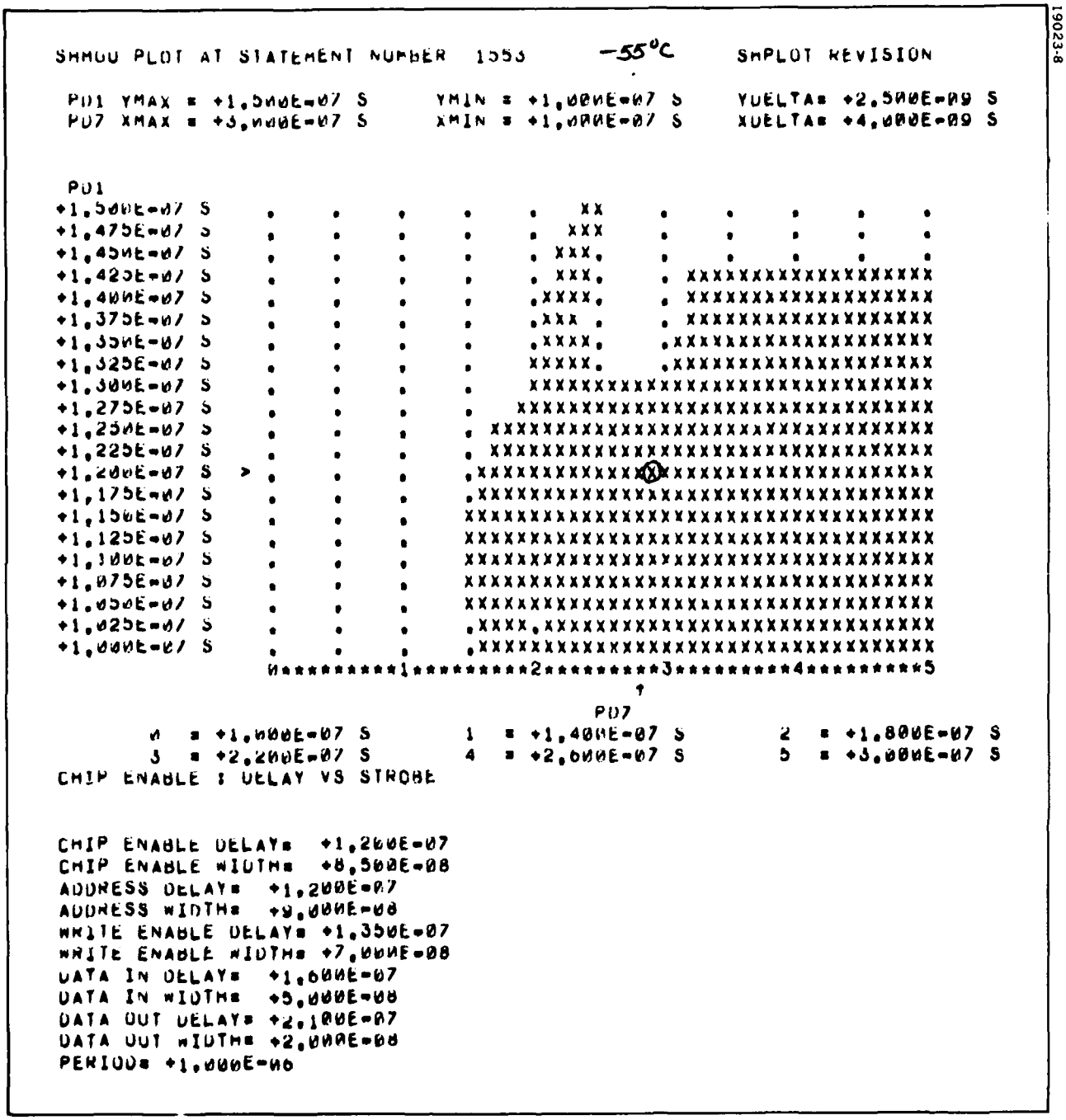


Figure A-8. Sentry Shmoo Plot of Device 2148 – CE Delay vs Read at -55°C

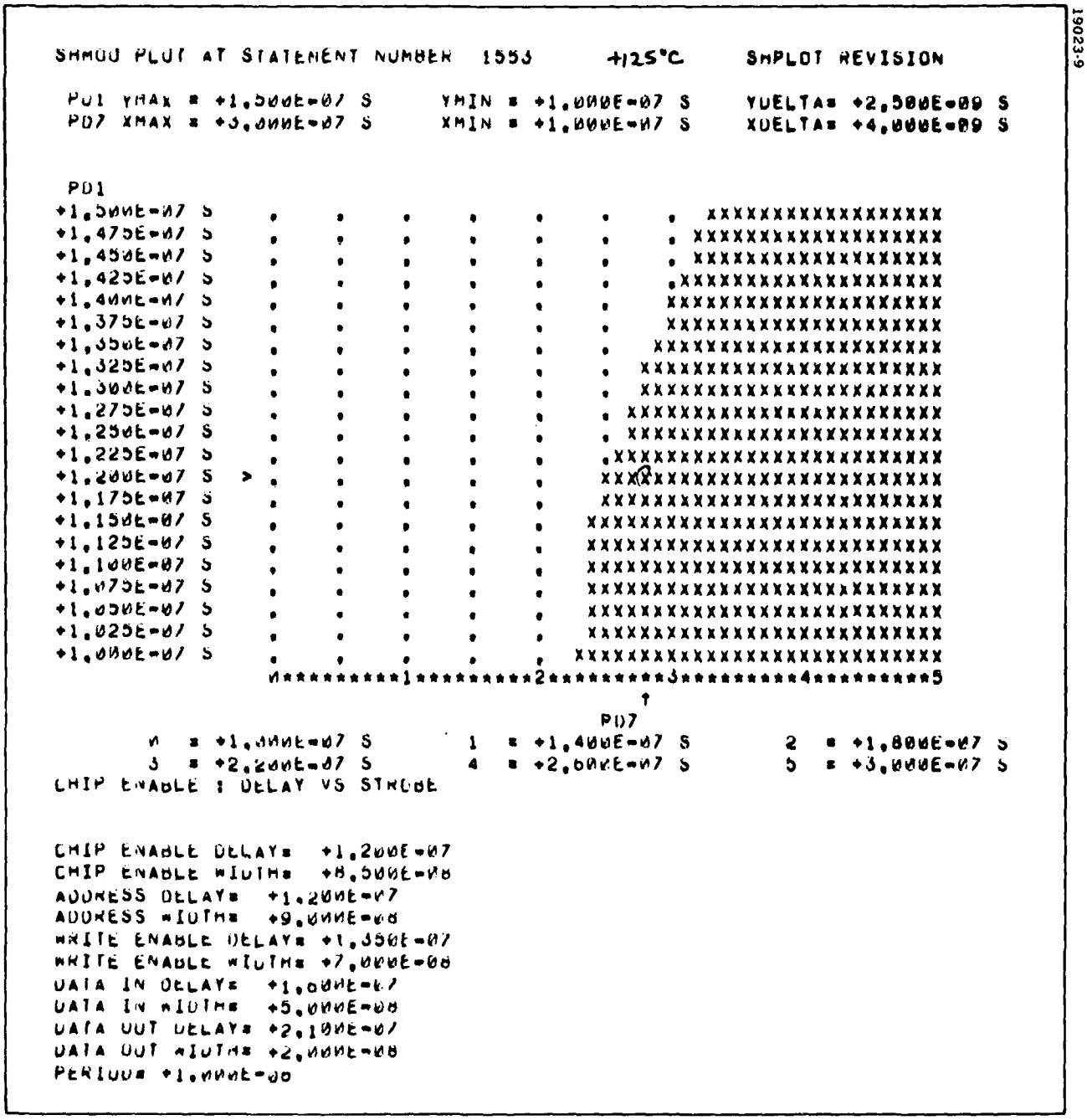


Figure A-9. Sentry Shmoo Plot of Device 2148 – CE Delay vs Read at +125°C

```
SHMOO PLOT AT STATEMENT NUMBER  1556        -55°C    SHPLOT REVISION

 PW1 YMAX = +1.500E-07 S      YMIN = +5.000E-08 S     YDELTA= +5.000E-09 S
 P07 XMAX = +3.000E-07 S      XMIN = +1.000E-07 S     XDELTA= +4.000E-09 S


 PW1
+1.500E-07 S     .    .    .    . XX .    . XX .    .    .    .    .
+1.450E-07 S     .    .    .    . XX .    .XXX .    .    .    .    .
+1.400E-07 S     .    .    .    . XX .    .XXX .    .    .    .    .
+1.350E-07 S     .    .    .    .XXX .    .XXX .    .    .    .    .
+1.300E-07 S     .    .    .    . XX .    .XXX .    .    .    .    .
+1.250E-07 S     .    .    .    . XX .    .XXX .    .    .    .    .
+1.200E-07 S     .    .    .    . XX .    XXXX .    .    .    .    .
+1.150E-07 S     .    .    .    . XX .    XXXX .    .    .    .    .
+1.100E-07 S     .    .    .    .XXX .    XXXX .    .    .    .    .
+1.050E-07 S     .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.000E-07 S     .    .    .    . XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+9.500E-08 S     .    .    .    . XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+9.000E-08 S     .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+8.500E-08 S  >  .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+8.000E-08 S     .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+7.500E-08 S     .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+7.000E-08 S     .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+6.500E-08 S     .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+6.000E-08 S     .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+5.500E-08 S     .    .    .    .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+5.000E-08 S     .    .    .    .    .    .    .    .    .    .    .
                 0*********1*********2*********3*********4*********5
                                       ↑
                                      P07
       0  = +1.000E-07 S        1  = +1.400E-07 S        2  = +1.800E-07 S
       3  = +2.200E-07 S        4  = +2.600E-07 S        5  = +3.000E-07 S
CHIP ENABLE : WIDTH VS STROBE


CHIP ENABLE DELAY=  +1.200E-07
CHIP ENABLE WIDTH=  +8.500E-08
ADDRESS DELAY=  +1.200E-07
ADDRESS WIDTH=  +9.000E-08
WRITE ENABLE DELAY= +1.350E-07
WRITE ENABLE WIDTH= +7.000E-08
DATA IN DELAY=  +1.600E-07
DATA IN WIDTH=  +5.000E-08
DATA OUT DELAY= +2.100E-07
DATA OUT WIDTH= +2.000E-08
PERIOD= +1.000E-06
```

Figure A-10. Sentry Shmoo Plot of Device 2148 – CE Width vs Read at -55°C

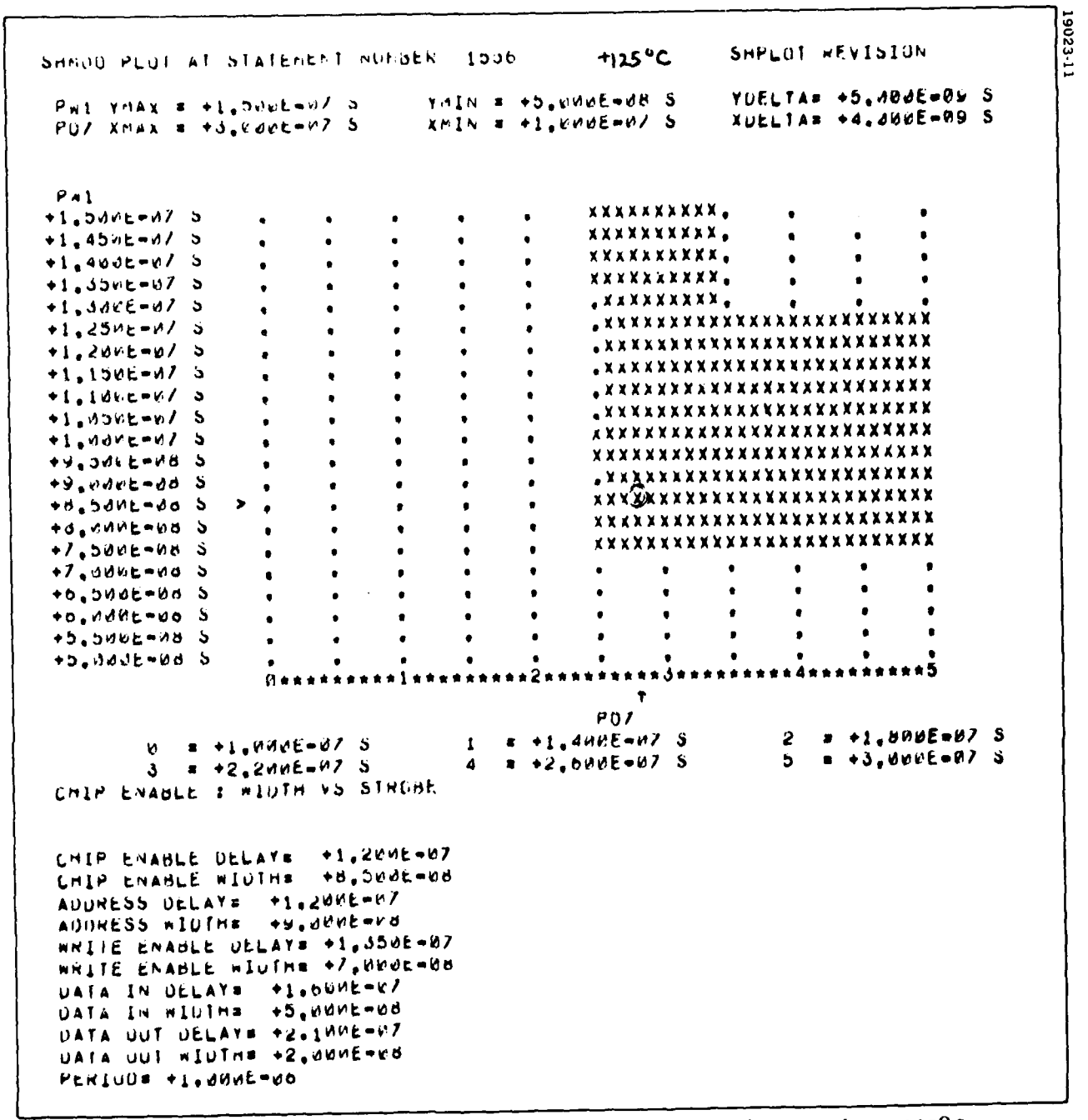


Figure A-11. Sentry Shmoo Plot of Device 2148 – CE Width vs Read at +125°C

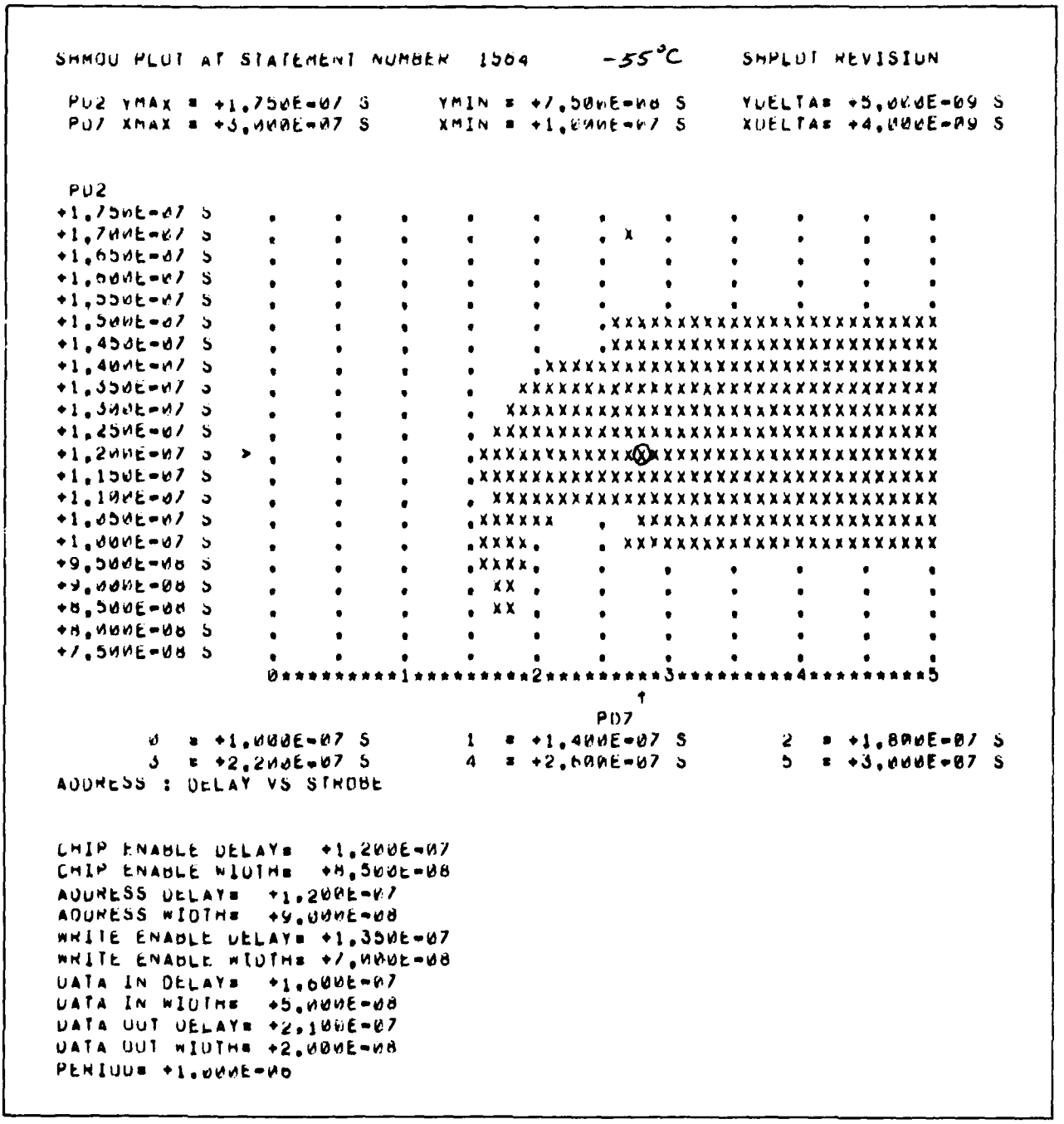


Figure A-12. Sentry Shmoo Plot of Device 2148 – Address Delay vs Read at -55°C

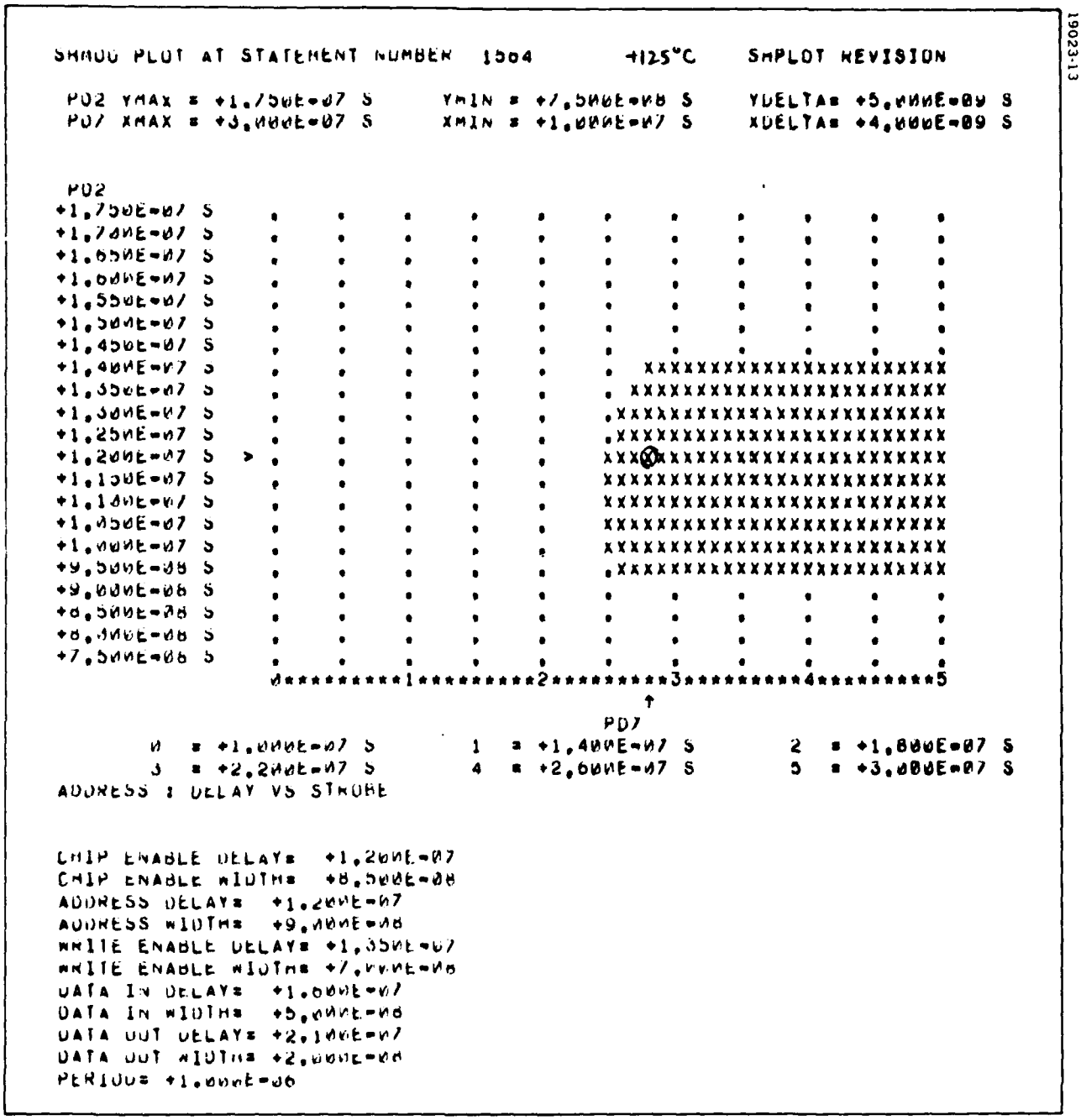


Figure A-13. Sentry Shmoo Plot of Device 2148 – Address Delay vs Read at +125°C

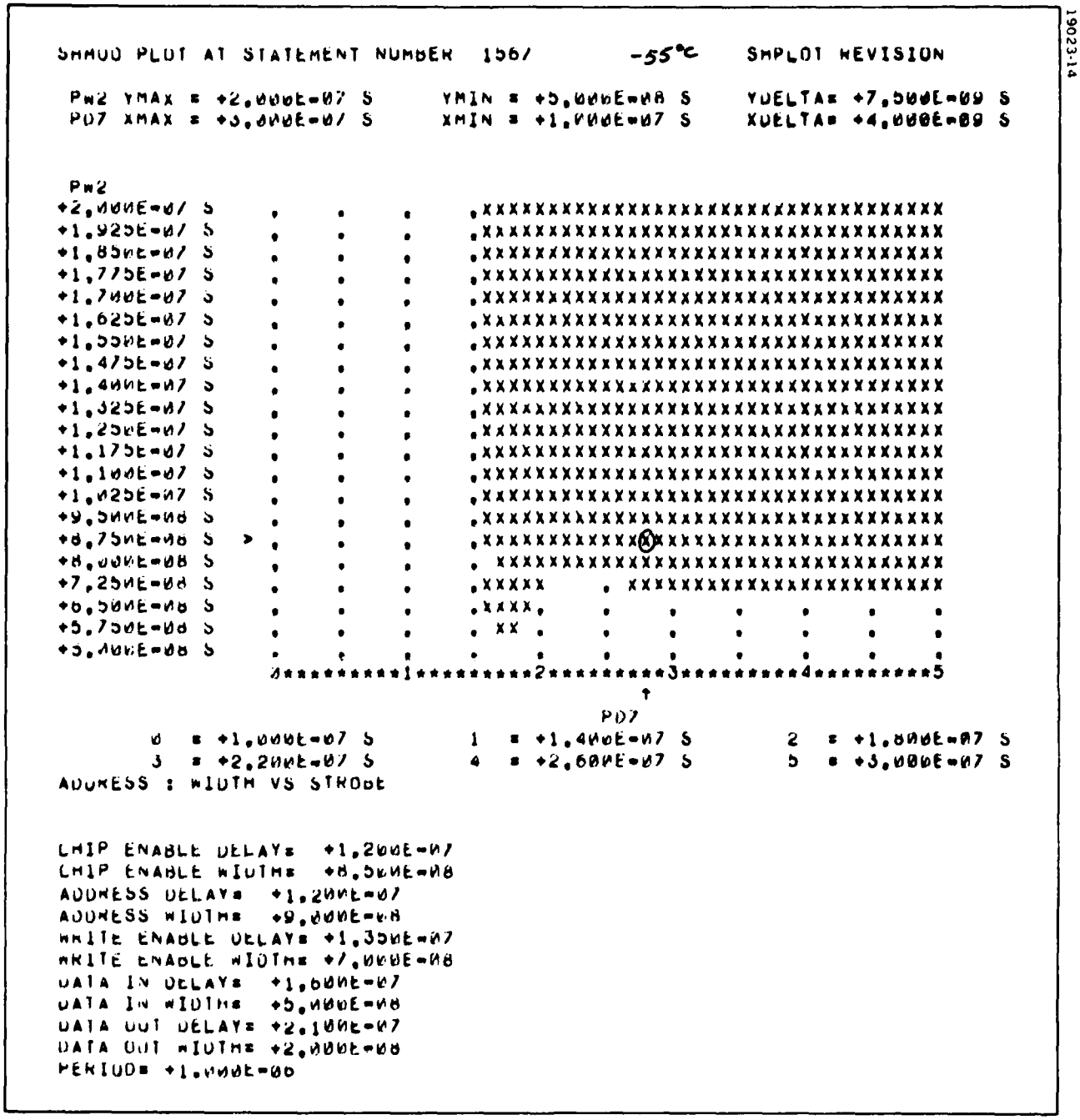


Figure A-14. Sentry Shmoo Plot of Device 2148 – Address Width vs Read at -55°C

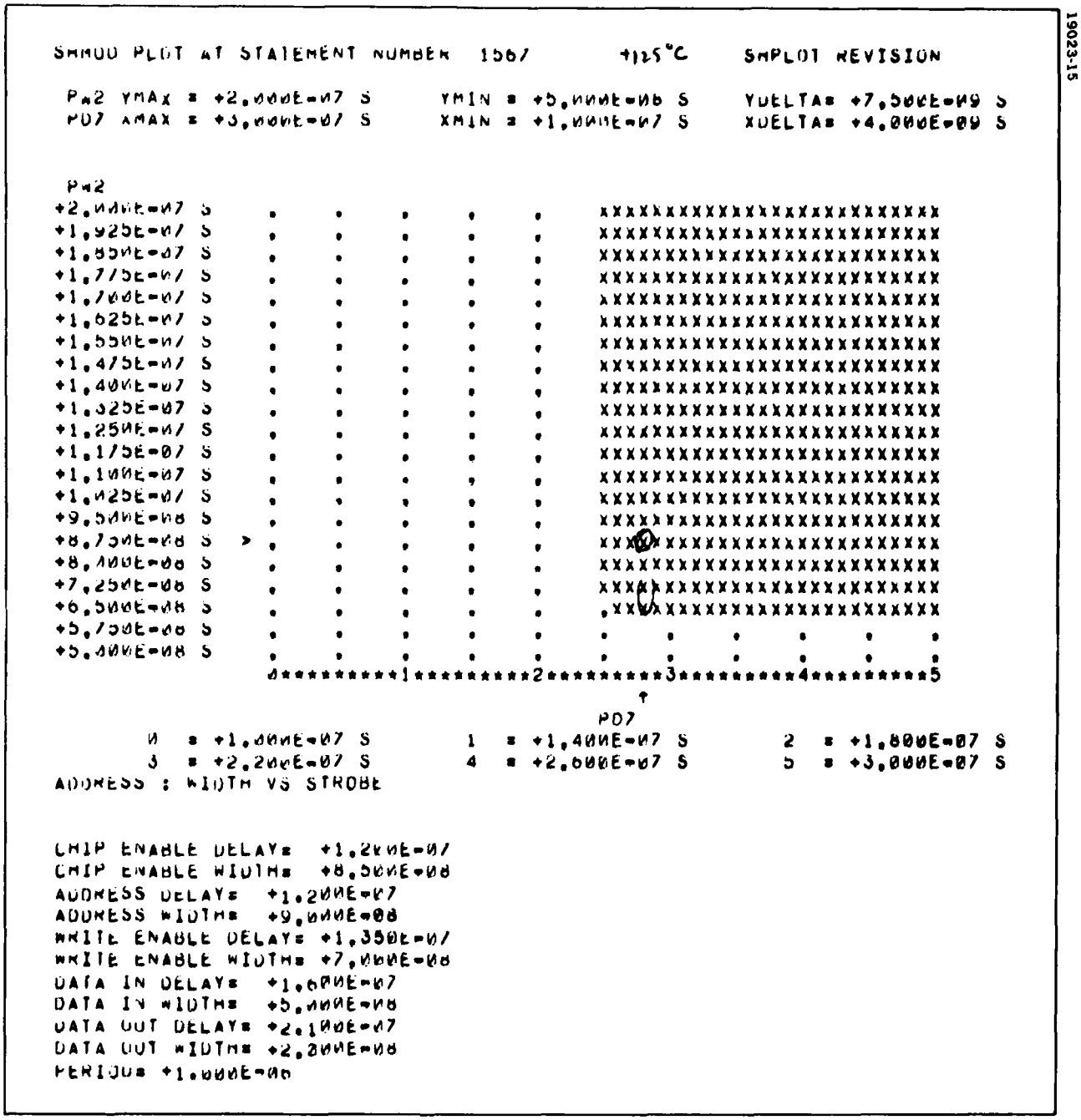


Figure A-15. Sentry Shmoo Plot of Device 2148 – Address Width vs Read at +125°C

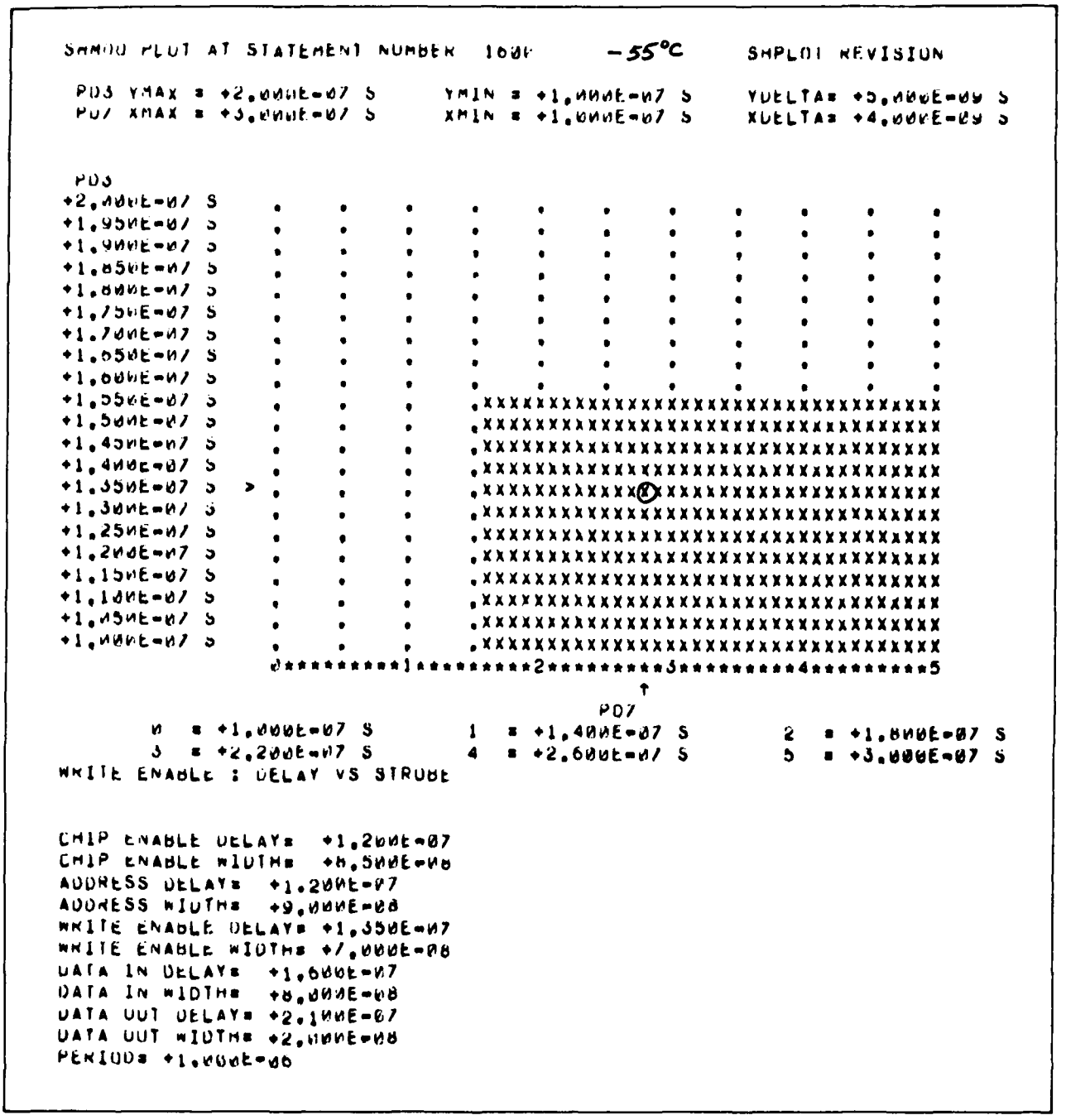


Figure A-16. Sentry Shmoo Plot of Device 2148 – WE Delay vs Read at -55°C

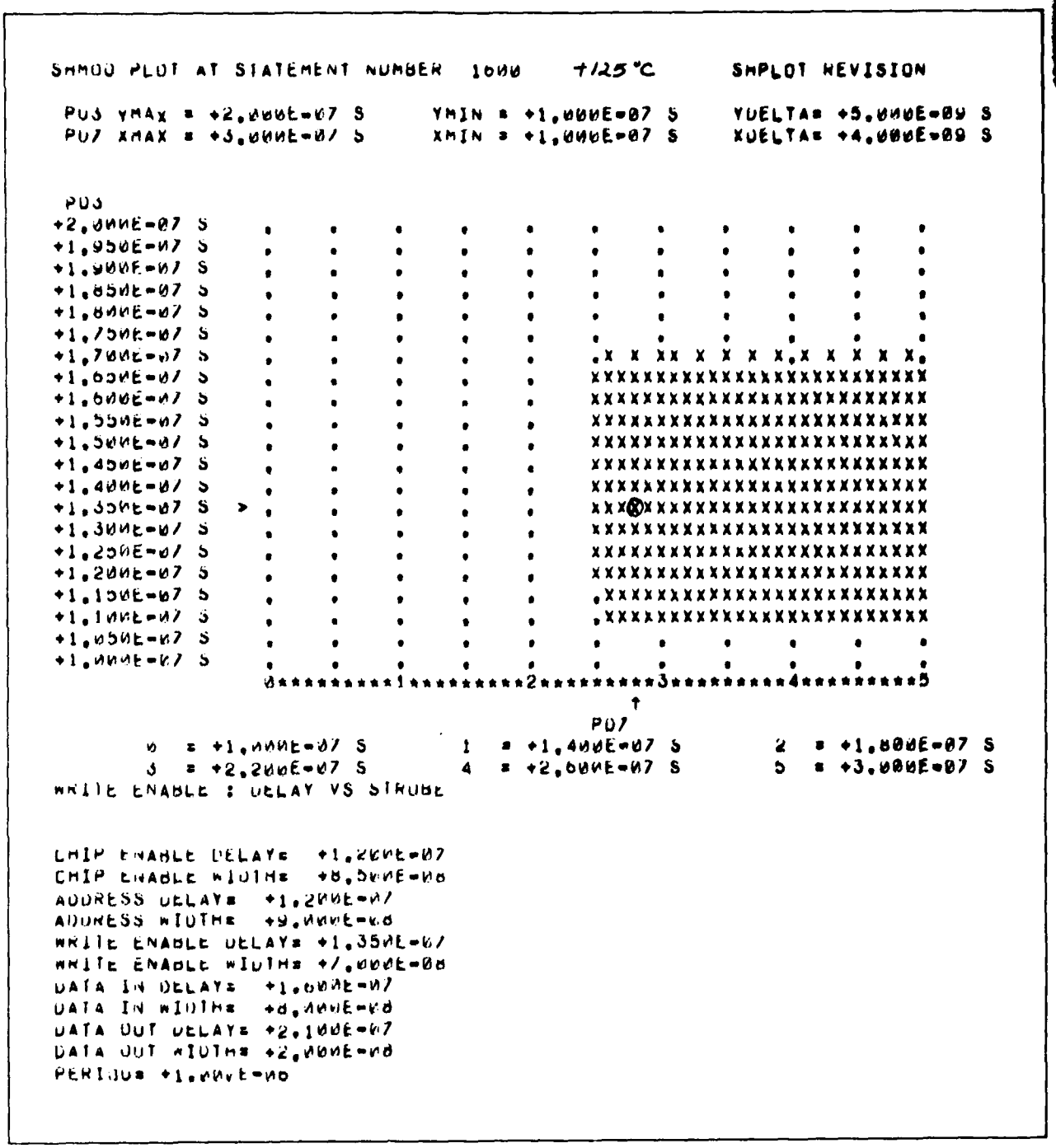


Figure A-17. Sentry Shmoo Plot of Device 2148 – WE Delay vs Read at +125°C

```
SHMOO PLOT AT STATEMENT NUMBER  1603          -55°C     SHPLOT REVISION

 PW3 YMAX = +1.500E-07 S      YMIN = +5.000E-08 S     YDELTA= +5.000E-09 S
 PD7 XMAX = +3.000E-07 S      XMIN = +1.000E-07 S     XDELTA= +4.000E-09 S


 PW3
+1.500E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.450E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.400E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.350E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.300E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.250E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.200E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.150E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.100E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.050E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+1.000E-07 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+9.500E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+9.000E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+8.500E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+8.000E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+7.500E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+7.000E-08 S  >  .     .     .     .XXXXXXXXXXXX0XXXXXXXXXXXXXXXXXXXX
+6.500E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+6.000E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+5.500E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
+5.000E-08 S     .     .     .     .XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
               0*********1*********2*********3*********4*********5
                                          ↑
                                         PD7
      0  = +1.000E-07 S        1  = +1.400E-07 S        2  = +1.800E-07 S
      3  = +2.200E-07 S        4  = +2.600E-07 S        5  = +3.000E-07 S
WRITE ENABLE : WIDTH VS STROBE


CHIP ENABLE DELAY=  +1.200E-07
CHIP ENABLE WIDTH=  +8.500E-08
ADDRESS DELAY=  +1.200E-07
ADDRESS WIDTH=  +9.000E-08
WRITE ENABLE DELAY= +1.350E-07
WRITE ENABLE WIDTH= +7.000E-08
DATA IN DELAY=  +1.800E-07
DATA IN WIDTH=  +8.000E-08
DATA OUT DELAY= +2.100E-07
DATA OUT WIDTH= +2.000E-08
PERIOD= +1.000E-06
```

Figure A-18. Sentry Shmoo Plot of Device 2148 – WE Width vs Read at -55°C

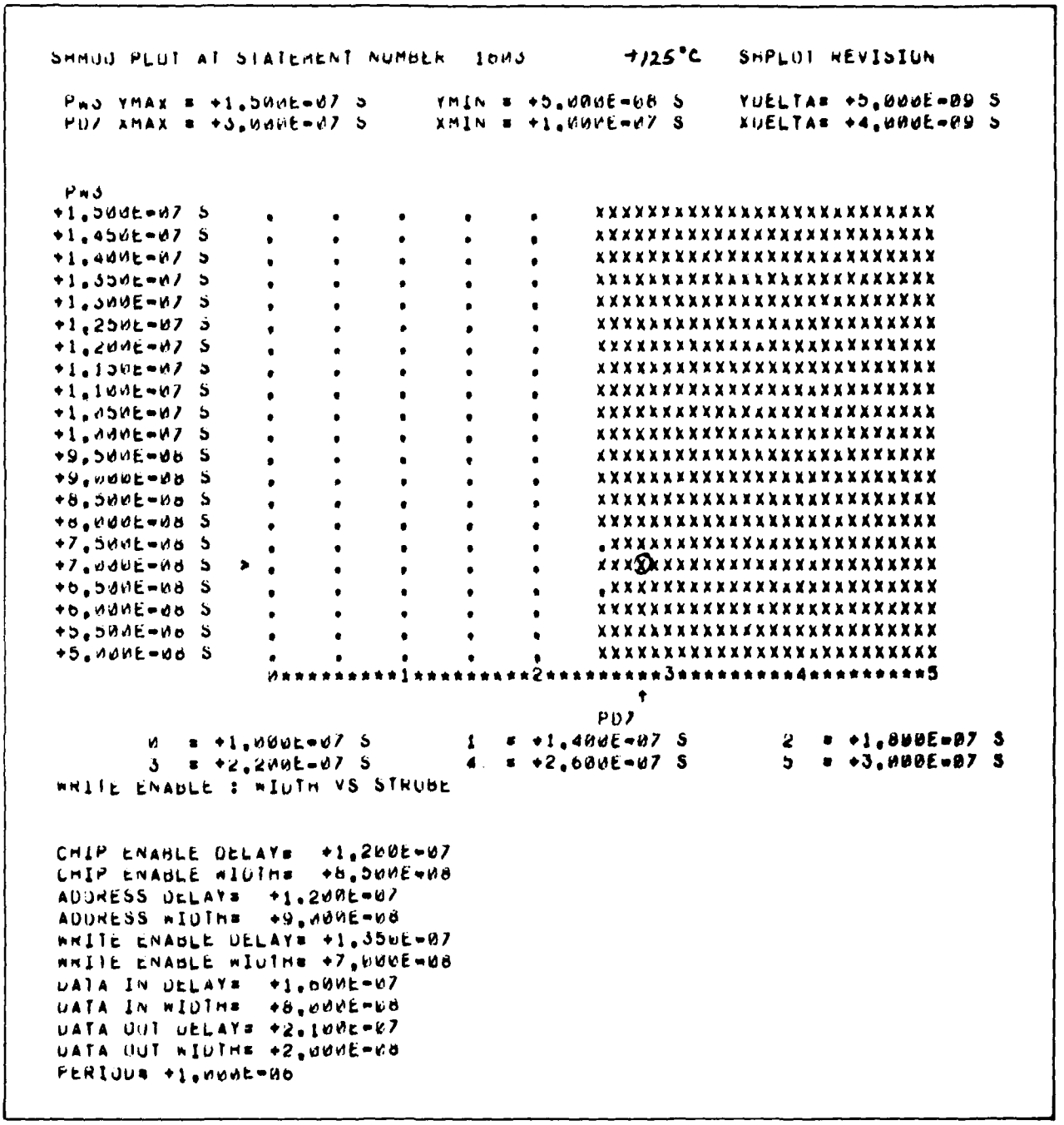


Figure A-19. Sentry Shmoo Plot of Device 2148 – WE Width vs Read at +125°C

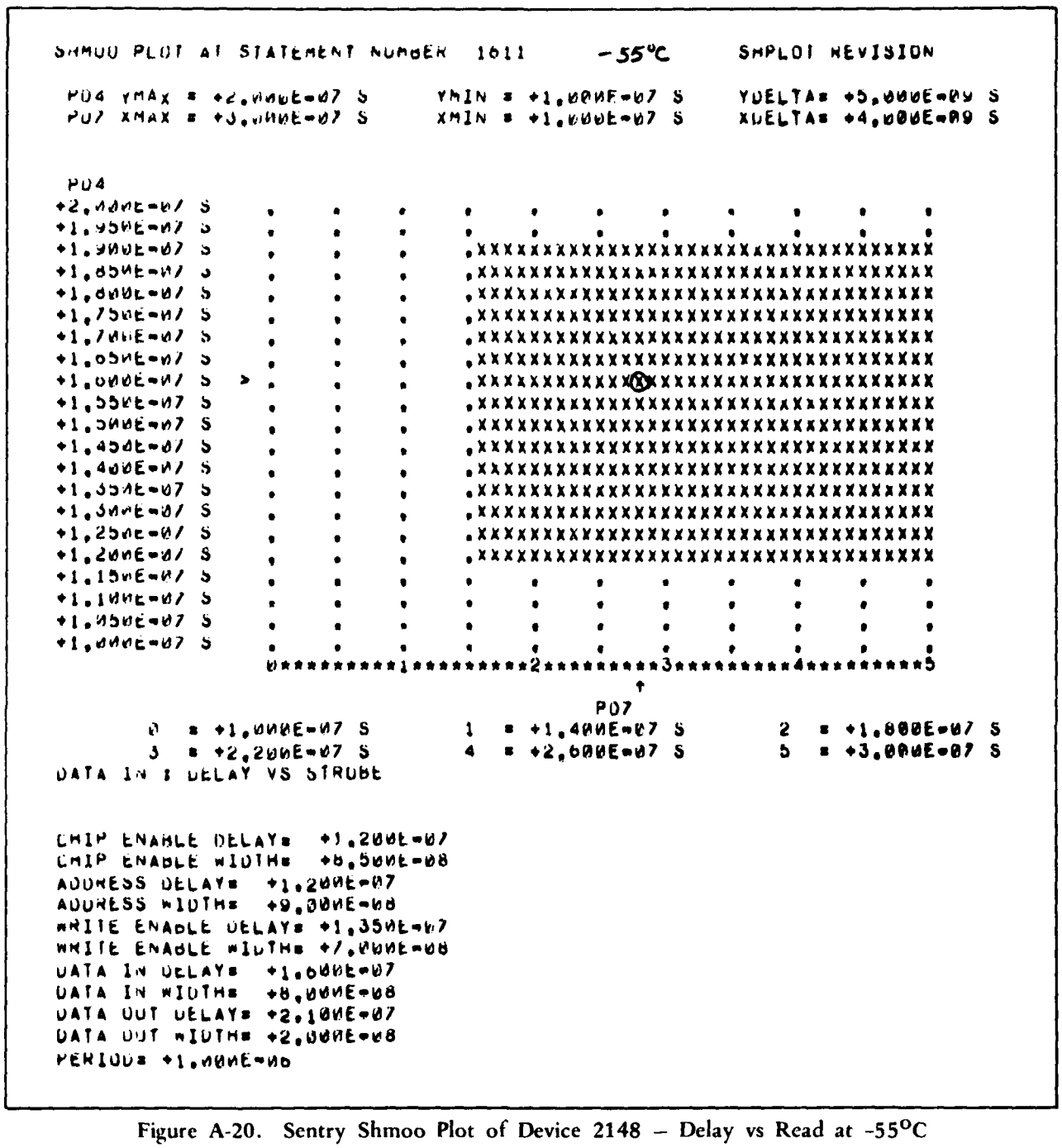


Figure A-20. Sentry Shmoo Plot of Device 2148 – Delay vs Read at -55°C

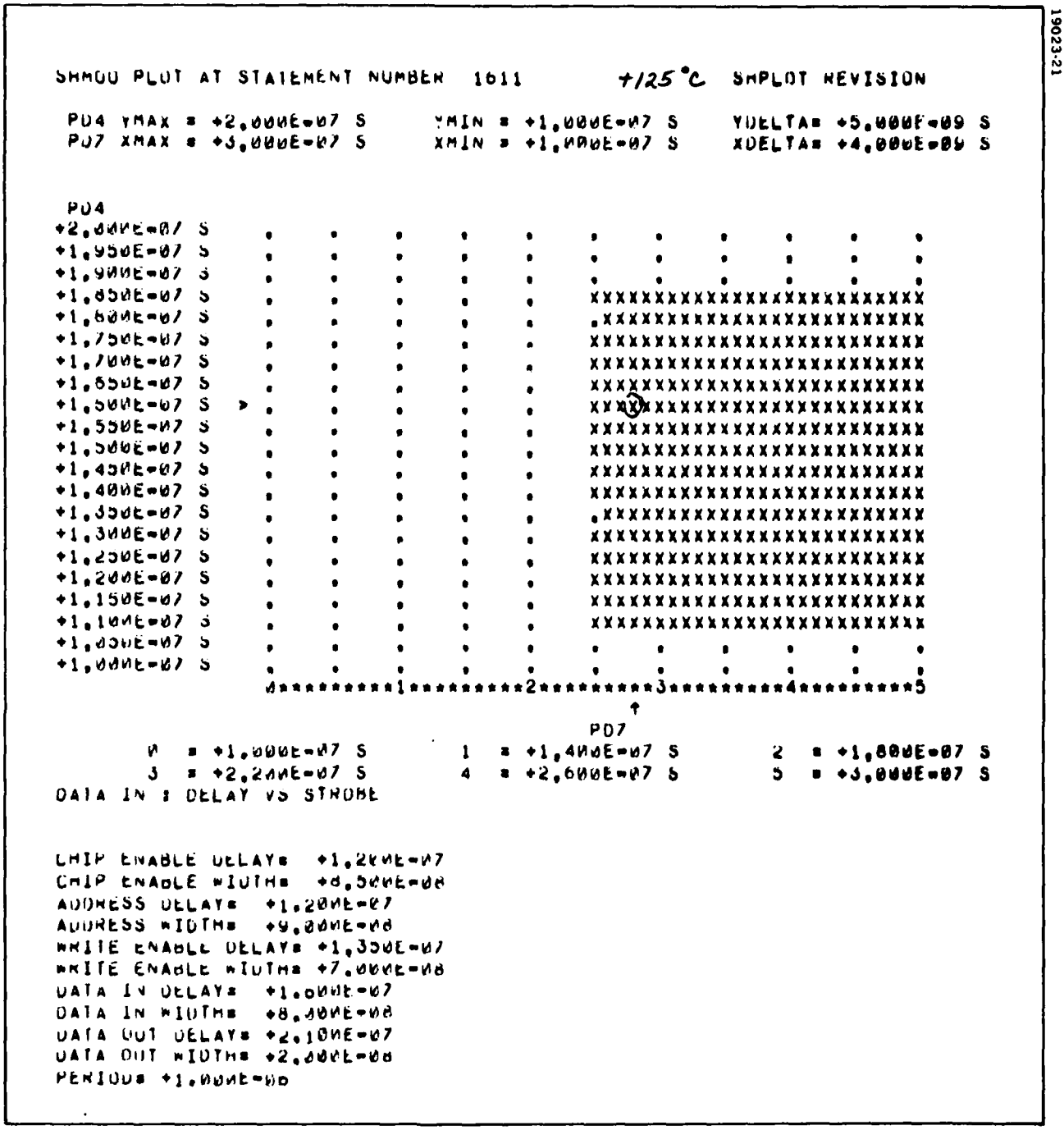


Figure A-21. Sentry Shmoo Plot of Device 2148 – Delay vs Read at +125°C

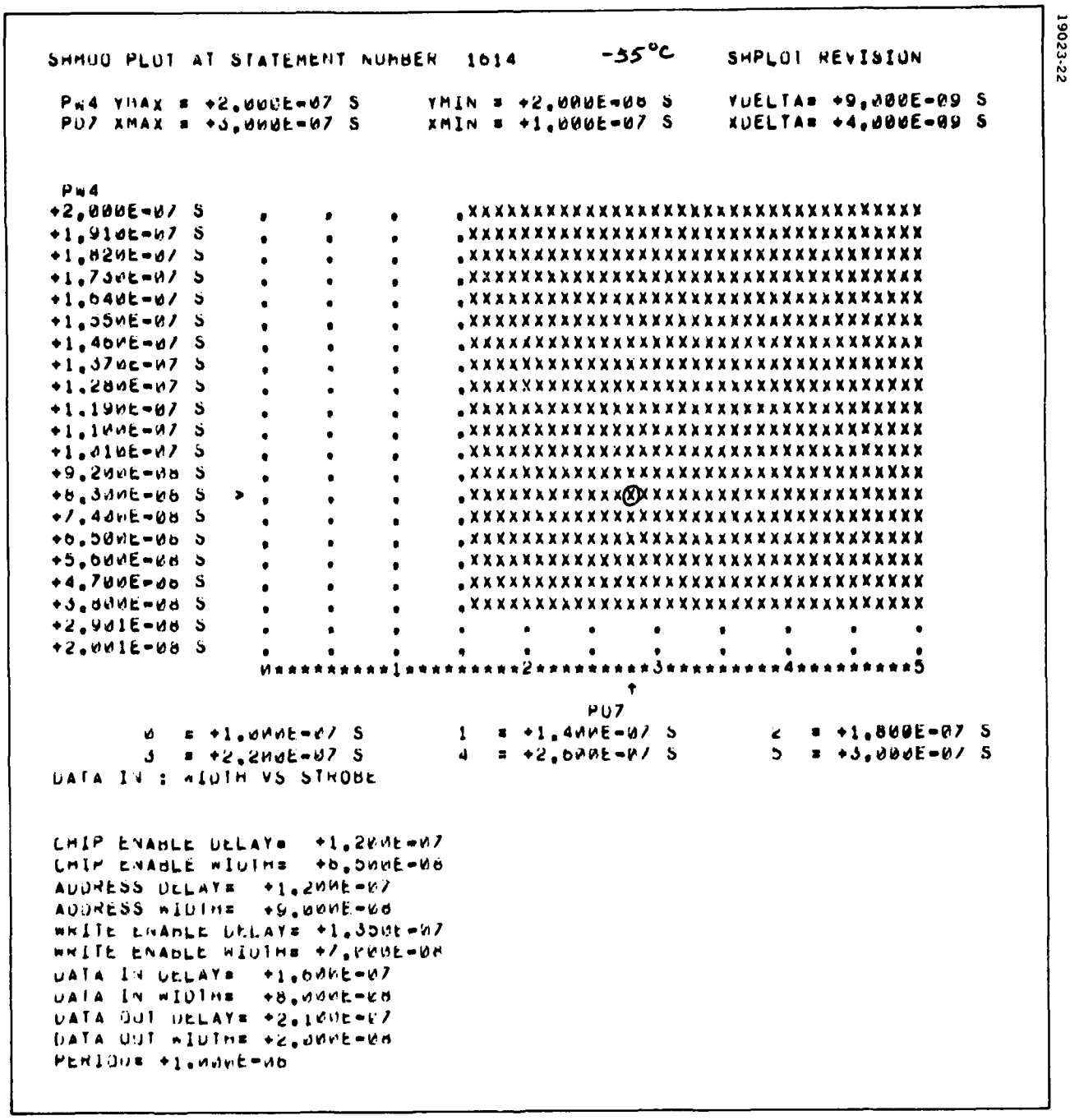


Figure A-22. Sentry Shmoo Plot of Device 2148 – Width vs Read at -55°C

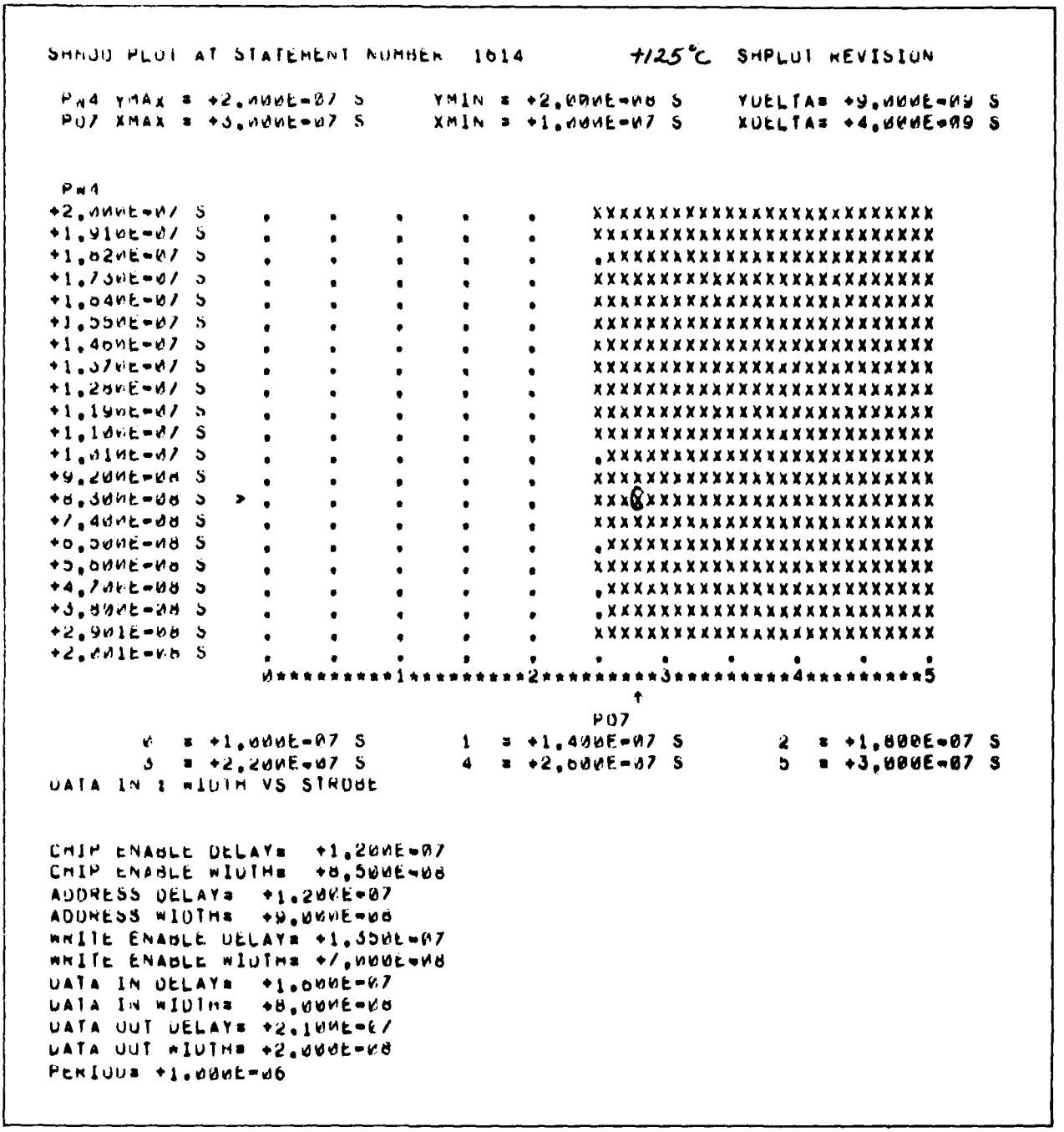


Figure A-23. Sentry Shmoo Plot of Device 2148 – Width vs Read at +125°C

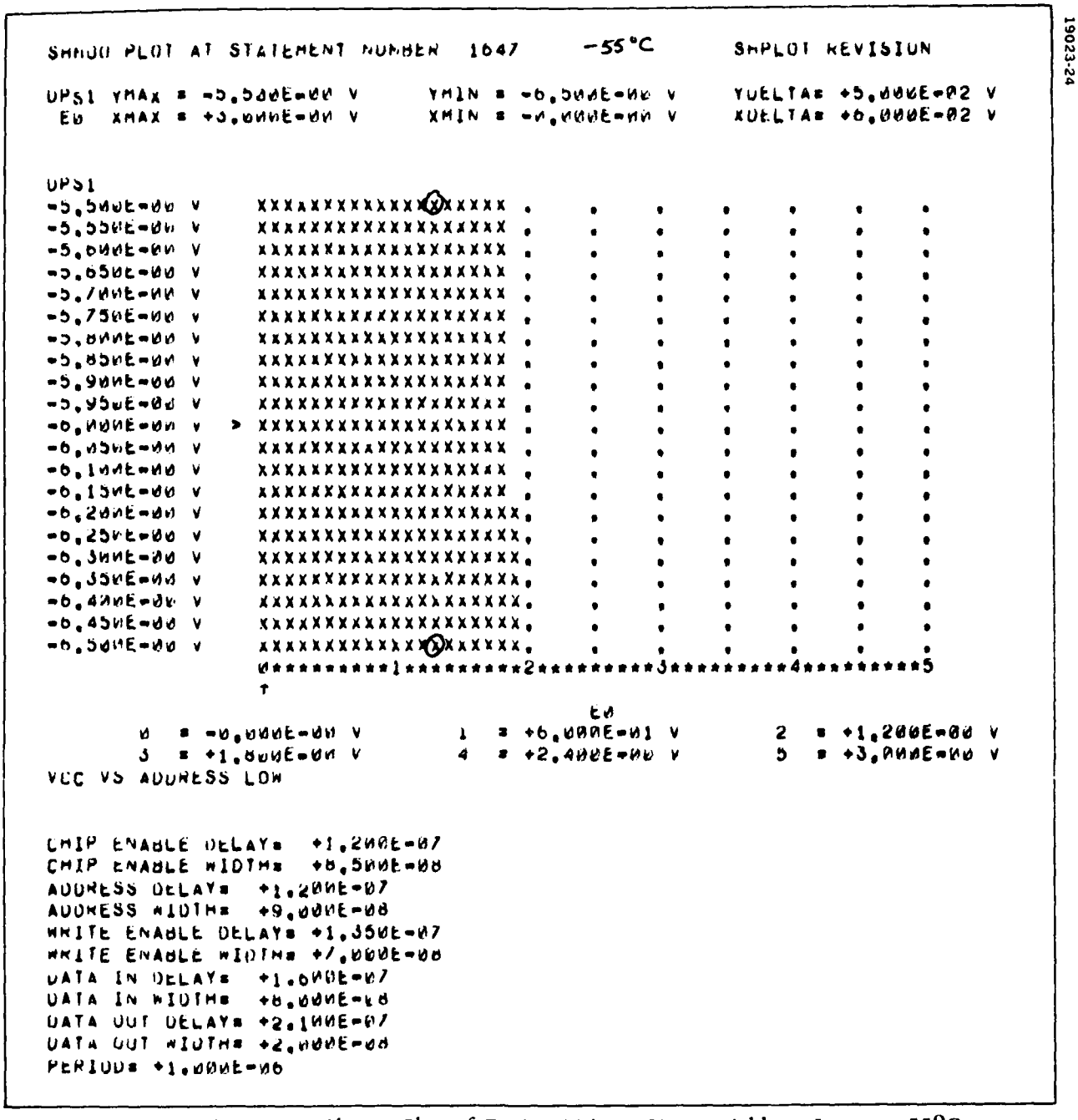


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Figure A-24. Sentry Shmoo Plot of Device 2148 – V_{CC} vs Address Low at -55°C

```
SHMOO PLOT AT STATEMENT NUMBER  1647          +125°C    SHPLOT REVISION

UPS1 YMAX = -5,500E-00 V      YMIN = -6,500E-00 V     YDELTA= +5,000E-02 V
 E0  XMAX = +3,000E-00 V      XMIN = -0,000E-00 V     XDELTA= +6,000E-02 V


UPS1
-5,500E-00 V   >> XXXXXXXXXXXXXXXXXX . . . . . .
-5,550E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-5,600E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-5,650E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-5,700E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-5,750E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-5,800E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-5,850E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-5,900E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-5,950E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,000E-00 V   >  XXXXXXXXXXXXXXXXXX . . . . . .
-6,050E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,100E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,150E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,200E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,250E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,300E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,350E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,400E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,450E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
-6,500E-00 V      XXXXXXXXXXXXXXXXXX . . . . . .
                  0*********1*********2*********3*********4*********5
                  ↑
                                      E0
        0  = -0,000E-00 V        1  = +6,000E-01 V        2  = +1,200E-00 V
        3  = +1,800E-00 V        4  = +2,400E-00 V        5  = +3,000E-00 V
VCC VS ADDRESS LOW


CHIP ENABLE DELAY=  +1,200E-07
CHIP ENABLE WIDTH=  +8,500E-08
ADDRESS DELAY=  +1,200E-07
ADDRESS WIDTH=  +9,000E-08
WRITE ENABLE DELAY= +1,350E-07
WRITE ENABLE WIDTH= +7,000E-08
DATA IN DELAY=  +1,000E-07
DATA IN WIDTH=  +6,000E-08
DATA OUT DELAY= +2,100E-07
DATA OUT WIDTH= +2,000E-08
PERIOD= +1,000E-06
```

Figure A-25. Sentry Shmoo Plot of Device 2148 – V_{CC} vs Address Low at +125°C

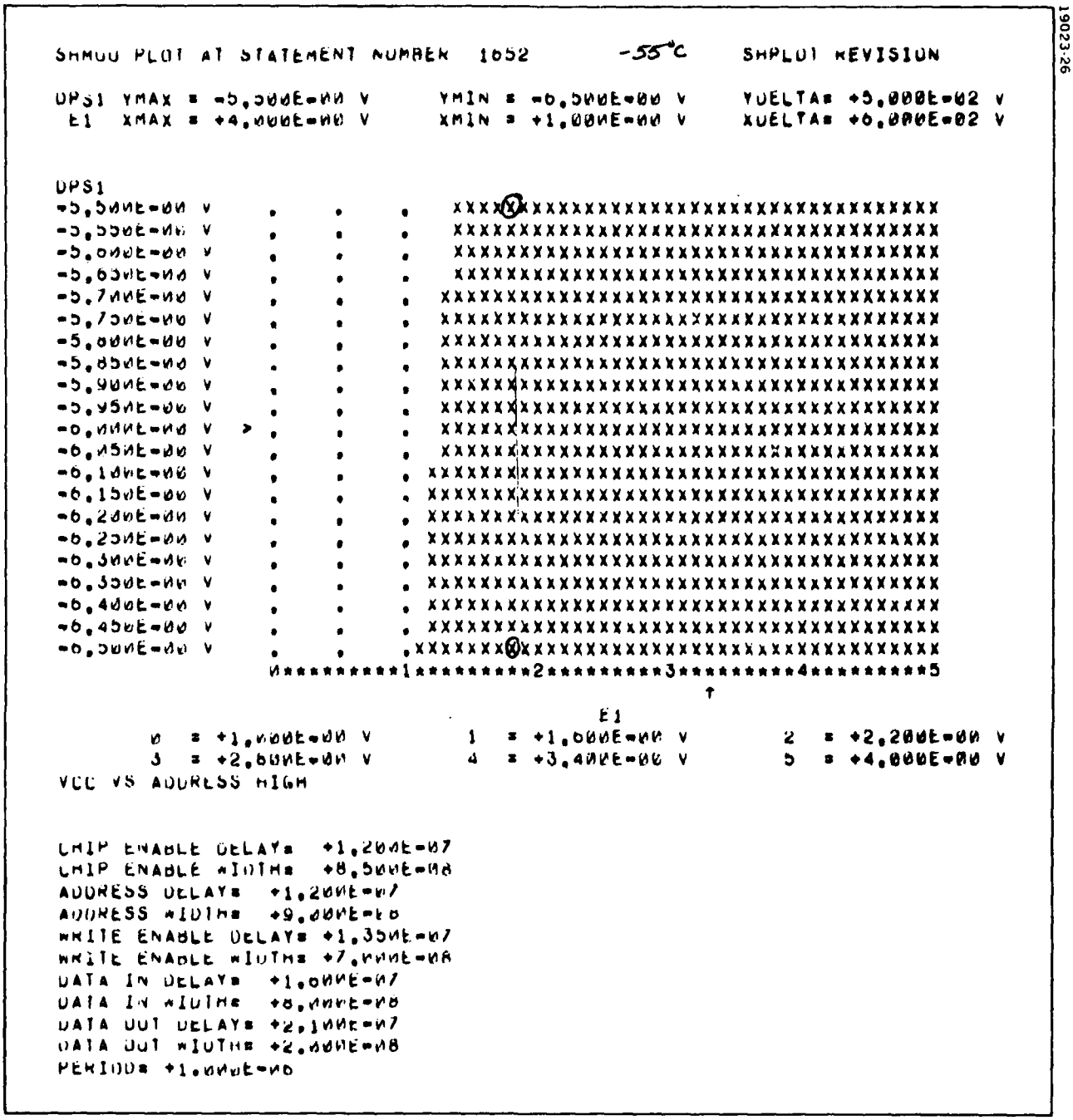

Figure A-26. Sentry Shmoo Plot of Device 2148 – V_{cc} vs Address High at -55°C

```
SHMOO PLOT AT STATEMENT NUMBER  1052        +125°C     SHPLOT REVISION

UPS1 YMAX = -5,500E-00 V      YMIN = -6,500E-00 V     YDELTA= +5,000E-02 V
 E1  XMAX = +4,000E-06 V      XMIN = +1,000E-06 V     XDELTA= +6,000E-02 V


UPS1
-5,500E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,550E-00 V      .     .    XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,600E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,650E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,700E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,750E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,800E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,850E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,900E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,950E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,000E-00 V   >  .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,050E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,100E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,150E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,200E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,250E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,300E-00 V      .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,350E-00 V      .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,400E-00 V      .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,450E-00 V      .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,500E-00 V      .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
                  0*********1*********2*********3*********4*********5
                                        E1
      0  = +1,000E-00 V        1  = +1,600E-00 V        2  = +2,200E-00 V
      3  = +2,800E-00 V        4  = +3,400E-06 V        5  = +4,000E-00 V
VCC VS ADDRESS HIGH


CHIP ENABLE DELAY=  +1,200E-07
CHIP ENABLE WIDTH=  +8,500E-08
ADDRESS DELAY=  +1,200E-07
ADDRESS WIDTH=  +9,000E-08
WRITE ENABLE DELAY= +1,350E-07
WRITE ENABLE WIDTH= +7,000E-08
DATA IN DELAY=  +1,600E-07
DATA IN WIDTH=  +6,000E-08
DATA OUT DELAY= +2,100E-07
DATA OUT WIDTH= +2,000E-06
PERIOD= +1,000E-06
```

Figure A-27. Sentry Shmoo Plot of Device 2148 -- V_{CC} vs Address High at +125°C

```
SHMOO PLOT AT STATEMENT NUMBER  1003        -55°C      SHPLOT REVISION

UPS1 YMAX = +5,500E-00 V      YMIN = -6,500E-00 V      YDELTA= +5,000E-02 V
 E0  XMAX = +3,000E-00 V      XMIN = -0,000E-01 V      XDELTA= +6,000E-02 V


UPS1
-5,500E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,550E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,600E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,650E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,700E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,750E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,800E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,850E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,900E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-5,950E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,000E-00 V   > XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,050E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,100E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,150E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,200E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,250E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,300E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,350E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,400E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,450E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
-6,500E-00 V     XXXXXXXXXXXXXXXXXXXXX     .     .     .     .     .     .
                 0*********1*********2*********3*********4*********5
                 ↑
                                          E0
       0  = -0,000E-00 V       1  = +6,000E-01 V       2  = +1,200E-00 V
       3  = +1,800E-00 V       4  = +2,400E-00 V       5  = +3,000E-00 V
VCC VS DATA IN LOW


CHIP ENABLE DELAY=  +1,200E-07
CHIP ENABLE WIDTH=  +8,500E-08
ADDRESS DELAY=  +1,200E-07
ADDRESS WIDTH=  +9,000E-08
WRITE ENABLE DELAY= +1,350E-07
WRITE ENABLE WIDTH= +7,000E-08
DATA IN DELAY=  +1,000E-07
DATA IN WIDTH=  +8,000E-08
DATA OUT DELAY= +2,100E-07
DATA OUT WIDTH= +2,000E-08
PERIOD= +1,000E-00
```

Figure A-28. Sentry Shmoo Plot of Device 2148 – V_{CC} vs Data In Low at -55°C

```
SHMOO PLOT AT STATEMENT NUMBER  1063        +125°C     SMPLOT REVISION

DPS1 YMAX = -5,500E-00 V      YMIN = -6,500E-00 V     YDELTA= +5,000E-02 V
 E0  XMAX = +3,000E-00 V      XMIN = -0,000E-00 V     XDELTA= +6,000E-02 V


DPS1
-5,500E-00 V     XXXXXXXXXXXXXXXXX   .     .     .     .     .     .     .
-5,550E-00 V     XXXXXXXXXXXXXXXXX   .     .     .     .     .     .     .
-5,600E-00 V     XXXXXXXXXXXXXXXXX   .     .     .     .     .     .     .
-5,650E-00 V     XXXXXXXXXXXXXXXXX   .     .     .     .     .     .     .
-5,700E-00 V     XXXXXXXXXXXXXXXXX   .     .     .     .     .     .     .
-5,750E-00 V     XXXXXXXXXXXXXXXXX   .     .     .     .     .     .     .
-5,800E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-5,850E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-5,900E-00 V     XXXXXXXXXXXXXXXXX   .     .     .     .     .     .     .
-5,950E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,000E-00 V   > XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,050E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,100E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,150E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,200E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,250E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,300E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,350E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,400E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,450E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
-6,500E-00 V     XXXXXXXXXXXXXXXX    .     .     .     .     .     .     .
                 0*********1*********2*********3*********4*********5
                 ↑
                                      E0
        W  = -0,000E-00 V        1  = +0,000E-01 V        2  = +1,200E-00 V
        3  = +1,800E-00 V        4  = +2,400E-00 V        5  = +3,000E-00 V
VCC VS DATA IN LOW


CHIP ENABLE DELAY=  +1,200E-07
CHIP ENABLE WIDTH=  +8,500E-08
ADDRESS DELAY=  +1,200E-07
ADDRESS WIDTH=  +9,000E-08
WRITE ENABLE DELAY= +1,350E-07
WRITE ENABLE WIDTH= +7,000E-08
DATA IN DELAY=  +1,000E-07
DATA IN WIDTH=  +0,000E-08
DATA OUT DELAY= +2,100E-07
DATA OUT WIDTH= +2,000E-08
PERIOD= +1,000E-06
```

Figure A-29. Sentry Shmoo Plot of Device 2148 – V_{cc} vs Data In Low at +125°C

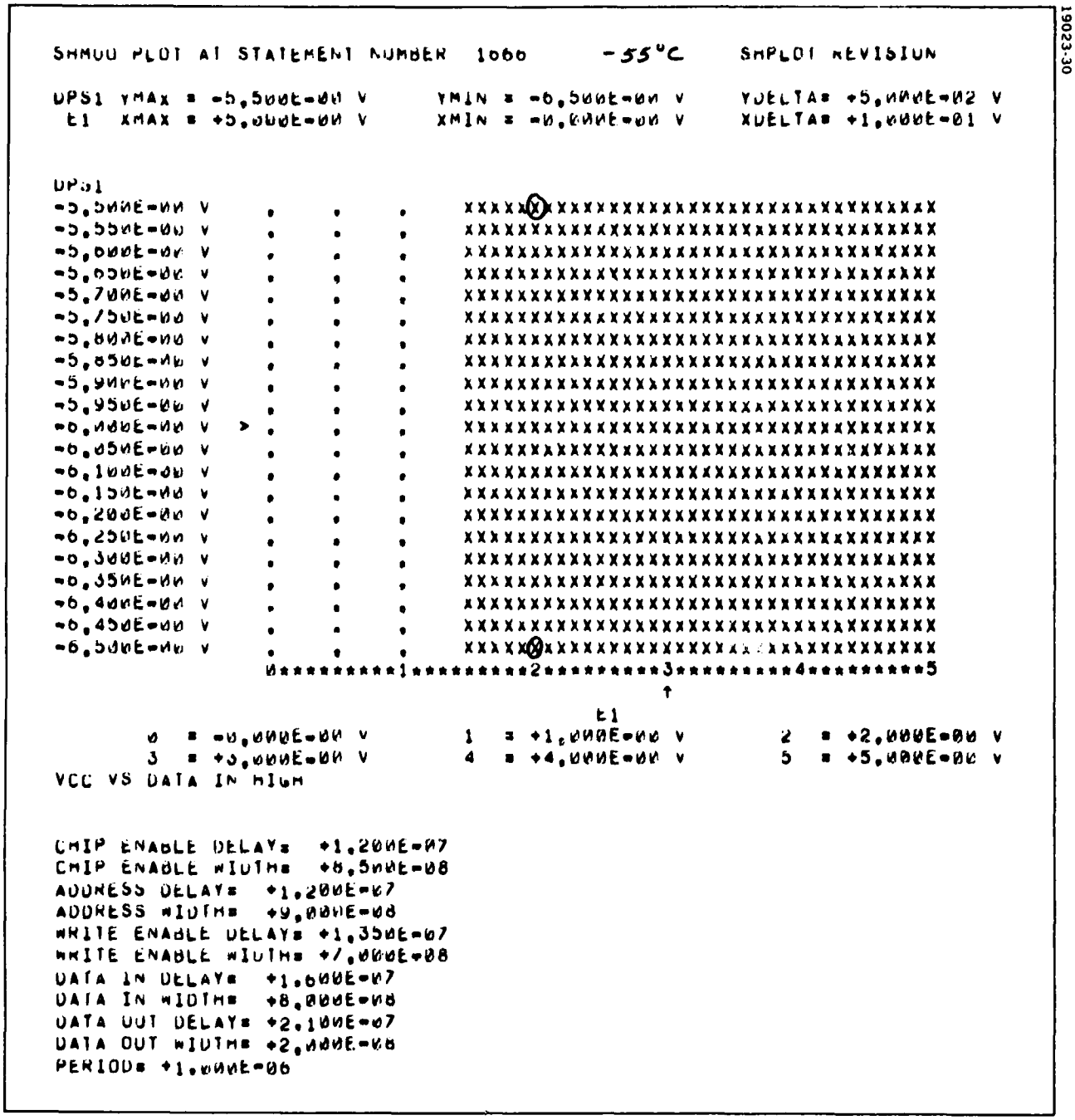

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Figure A-30. Sentry Shmoo Plot of Device 2148 – V_{CC} vs Data In High at -55°C

```
SHMOO PLOT AT STATEMENT NUMBER  1000      +125°C        SHPLOT REVISION

DPS1 YMAX = -5,500E-00 V      YMIN = -6,50ME-00 V     YDELTA= +5,000E-02 V
 E1  XMAX = +5,000E-00 V      XMIN = -0,000E-00 V     XDELTA= +1,000E-01 V


DPS1
-5,50ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,55ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,000E-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,05ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,70ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,75OE-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,80ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,85ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,900E-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-5,95OE-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,00ME-00 V  >  .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,05ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,10ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,15OE-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,20ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,25ME-00 V     .     .     .   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,300E-00 V     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,35ME-00 V     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,40ME-00 V     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,45ME-00 V     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-6,50ME-00 V     .     .     .  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
                 *********1*********2*********3*********4*********5
                                        ↑
                                       E1
      0  = -0,00ME-00 V        1  = +1,00ME-00 V        2  = +2,000E-00 V
      3  = +3,000E-00 V        4  = +4,00ME-00 V        5  = +5,000E-00 V
VCC VS DATA IN HIGH


CHIP ENABLE DELAY=  +1,200E-07
CHIP ENABLE WIDTH=  +8,500E-08
ADDRESS DELAY=  +1,20ME-07
ADDRESS WIDTH=  +9,000E-08
WRITE ENABLE DELAY= +1,35ME-07
WRITE ENABLE WIDTH= +7,00OE-08
DATA IN DELAY=  +1,000E-07
DATA IN WIDTH=  +8,00ME-08
DATA OUT DELAY= +2,10ME-07
DATA OUT WIDTH= +2,00ME-08
PERIOD= +1,000E-06
```

Figure A-31. Sentry Shmoo Plot of Device 2148 – V_{CC} vs Data In High at +125°C

```
SHMOO PLOT AT STATEMENT NUMBER  1701        -55°C      SHPLOT REVISION

DPS1 YMAX = -5.500E-00 V      YMIN = -0.500E-00 V     YDELTA= +5.000E-02 V
 EB1 XMAX = +5.000E-00 V      XMIN = -0.000E-00 V     XDELTA= +1.000E-01 V


DPS1
-5.500E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.550E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.600E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.650E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.700E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.750E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.800E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.850E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.900E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-5.950E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.000E-00 V   > XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.050E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.100E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.150E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.200E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.250E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.300E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.350E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.400E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.450E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
-6.500E-00 V     XXXXXXXXXXXXX  .    .    .    .    .    .    .    .
                 0*********1*********2*********3*********4*********5
                 ↑
                                        EB1
      0  = -0.000E-00 V        1  = +1.000E-00 V        2  = +2.000E-00 V
      3  = +3.000E-00 V        4  = +4.000E-00 V        5  = +5.000E-00 V
VCC VS /WE HIGH


CHIP ENABLE DELAY=  +1.200E-07
CHIP ENABLE WIDTH=  +8.500E-08
ADDRESS DELAY=  +1.200E-07
ADDRESS WIDTH=  +9.000E-08
WRITE ENABLE DELAY= +1.350E-07
WRITE ENABLE WIDTH= +7.000E-08
DATA IN DELAY=  +1.600E-07
DATA IN WIDTH=  +8.000E-08
DATA OUT DELAY= +2.100E-07
DATA OUT WIDTH= +2.000E-08
PERIOD= +1.000E-06
```

Figure A-32. Sentry Shmoo Plot of Device 2148 – V_{CC} vs WE High at -55°C

```
SHMOO PLOT AT STATEMENT NUMBER  1701          +125°C      SHPLOT REVISION

UPS1 YMAX = -5,500E-00 V      YMIN = -6,500E-00 V     YDELTA= +5,000E-02 V
 EB1 XMAX = +5,000E-00 V      XMIN = -0,000E-00 V     XDELTA= +1,000E-01 V


UPS1
-5,500E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,550E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,600E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,650E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,700E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,750E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,800E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,850E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,900E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-5,950E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-6,000E-00 V   > XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-6,050E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-6,100E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-6,150E-00 V     XXXXXXXXXXX   .  .  .  .  .  .  .  .  .
-6,200E-00 V     XXXXXXXXXXXX  .  .  .  .  .  .  .  .  .
-6,250E-00 V     XXXXXXXXXXX   .  .  .  .  .  .  .  .  .
-6,300E-00 V     XXXXXXXXXXX   .  .  .  .  .  .  .  .  .
-6,350E-00 V     XXXXXXXXXXX   .  .  .  .  .  .  .  .  .
-6,400E-00 V     XXXXXXXXXXX   .  .  .  .  .  .  .  .  .
-6,450E-00 V     XXXXXXXXXXX   .  .  .  .  .  .  .  .  .
-6,500E-00 V     XXXXXXXXXXX   .  .  .  .  .  .  .  .  .
                 0*********1*********2*********3*********4*********5
                 ↑
                                        EB1
        0  = -0,000E-00 V        1  = +1,000E-00 V        2  = +2,000E-00 V
        3  = +3,000E-00 V        4  = +4,000E-00 V        5  = +5,000E-00 V
VCC VS /WE HIGH


CHIP ENABLE DELAY=  +1,200E-07
CHIP ENABLE WIDTH=  +6,500E-08
ADDRESS DELAY=  +1,200E-07
ADDRESS WIDTH=  +9,000E-08
WRITE ENABLE DELAY= +1,350E-07
WRITE ENABLE WIDTH= +7,000E-08
DATA IN DELAY=  +1,000E-07
DATA IN WIDTH=  +6,000E-08
DATA OUT DELAY= +2,100E-07
DATA OUT WIDTH= +2,000E-08
PERIOD= +1,000E-06
```

Figure A-33. Sentry Shmoo Plot of Device 2148 – V_{CC} vs WE High at +125°C

```
SHMOO PLOT AT STATEMENT NUMBER  1/12      -55°C     SMPLOT REVISION

DPS1 YMAX = -5,500E-00 V      YMIN = -6,500E-00 V     YDELTA= +5,000E-02 V
 S1  XMAX = +4,000E-00 V      XMIN = +2,000E-00 V     XDELTA= +4,000E-02 V


DPS1
-5,500E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,550E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,600E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,650E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,700E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,750E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,800E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,850E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,900E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-5,950E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-6,000E-00 V  >  XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-6,050E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-6,100E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-6,150E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-6,200E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-6,250E-00 V     XXXXXXXXXXXXXXXXXXXXXXX . . . . . .
-6,300E-00 V     XXXXXXXXXXXXXXXXXXXXXX  . . . . . .
-6,350E-00 V     XXXXXXXXXXXXXXXXXXXXXX  . . . . . .
-6,400E-00 V     XXXXXXXXXXXXXXXXXXXXXX  . . . . . .
-6,450E-00 V     XXXXXXXXXXXXXXXXXXXXXX  . . . . . .
-6,500E-00 V     XXXXXXXXXXXXXXXXXXXXXX  . . . . . .
                 0*********1*********2*********3*********4*********5
                           ↑
                                    S1
       0  = +2,000E-00 V        1  = +2,400E-00 V        2  = +2,800E-00 V
       3  = +3,200E-00 V        4  = +3,600E-00 V        5  = +4,000E-00 V
VCC VS OUTPUT HIGH


CHIP ENABLE DELAY=  +1,200E-07
CHIP ENABLE WIDTH=  +8,500E-08
ADDRESS DELAY=  +1,200E-07
ADDRESS WIDTH=  +9,000E-08
WRITE ENABLE DELAY= +1,350E-07
WRITE ENABLE WIDTH= +7,000E-08
DATA IN DELAY=  +1,600E-07
DATA IN WIDTH=  +8,000E-08
DATA OUT DELAY= +2,100E-07
DATA OUT WIDTH= +2,000E-08
PERIOD= +1,000E-06
```

Figure A-34. Sentry Shmoo Plot of Device 2148 – V_{CC} vs Output High at -55°C

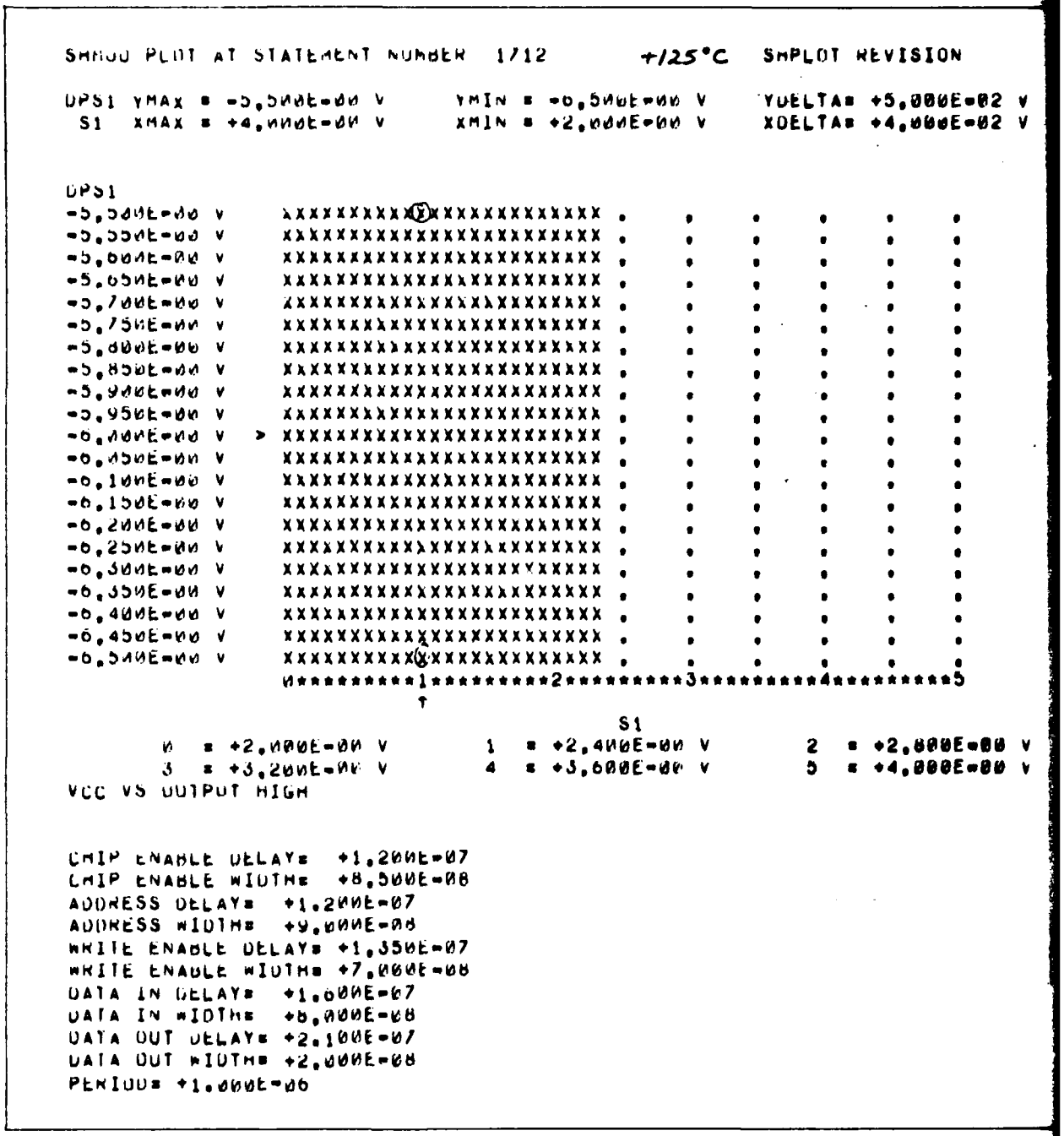

Figure A-35. Sentry Shmoo Plot of Device 2148 – V_{cc} vs Output High at +125°C

```
ILI1 TEST
 PIN  1=  -1.000E-07
 PIN  2=  -1.000E-07
 PIN  3=      0
 PIN  4=  -1.000E-07
 PIN  5=  -1.000E-07
 PIN  6=      0
 PIN  7=  -1.000E-07
 PIN  8=  -1.000E-07
 PIN 10=      0
 PIN 11=  -2.600E-06
 PIN 12=  -1.800E-06
 PIN 13=  -4.500E-06
 PIN 14=  -5.000E-06
 PIN 15=  -1.000E-07
 PIN 16=  -2.000E-07
 PIN 17=  -1.000E-07

ILI2 TEST
 PIN  1=  -1.000E-07
 PIN  2=  -1.000E-07
 PIN  3=      0
 PIN  4=      0
 PIN  5=      0
 PIN  6=      0
 PIN  7=  -1.000E-07
 PIN  8=  -1.000E-07
 PIN 10=  -1.000E-07
 PIN 11=  -1.000E-06
 PIN 12=  -9.000E-07
 PIN 13=  -2.400E-06
 PIN 14=  -2.000E-06
 PIN 15=  -1.000E-07
 PIN 16=  -1.000E-07
 PIN 17=  -1.000E-07

IOS TEST AT VCCMAX
 PIN 11=  -1.500E-01   S/B>   -1.500E-01  AND <  +1.500E-01    PAIL
 PIN 12=  -1.400E-01
 PIN 13=  -1.420E-01
 PIN 14=  -1.400E-01
```

```
ILO1 TEST                                          -55°C
 PIN 11=  -2.800E-06
 PIN 12=  -3.700E-06
 PIN 13=  -6.100E-06
 PIN 14=  -6.100E-06

ILO2 TEST
 PIN 11=  -1.400E-06
 PIN 12=  -2.100E-06
 PIN 13=  -3.400E-06
 PIN 14=  -3.200E-06

ICC TEST
 PIN 16=  +7.800E-02

VOL TEST
 PIN 11=  +1.720E-01
 PIN 12=  +1.900E-01
 PIN 13=  +1.820E-01
 PIN 14=  +1.800E-01

VOH TEST
 PIN 11=  +3.390E+00
 PIN 12=  +4.140E+00
 PIN 13=  +4.230E+00
 PIN 14=  +4.150E+00

ISB1&2 TEST                                        -55°C
 PIN 16=  +1.270E-02
 PIN 16=  +1.140E-02

IPU TEST
 PIN 16=  +1.150E-02
```

Figure A-36. Sentry Test Results of Device 2148 – DC Parameter Test at -55°C

```
ILI1 TEST
 PIN  1=      0
 PIN  2=      0
 PIN  3=      0
 PIN  4=      0
 PIN  5=      0
 PIN  6=      0
 PIN  7=      0
 PIN  8=      0
 PIN 10=  +1.000E-06
 PIN 11=  +7.000E-07
 PIN 12=  +2.000E-07
 PIN 13=  +1.000E-07
 PIN 14=      0
 PIN 15=      0
 PIN 16=      0
 PIN 17=      0

ILI2 TEST
 PIN  1=      0
 PIN  2=      0
 PIN  3=      0
 PIN  4=      0
 PIN  5=      0
 PIN  6=      0
 PIN  7=      0
 PIN  8=      0
 PIN 10=  +1.900E-06
 PIN 11=  +8.000E-07
 PIN 12=  +2.000E-07
 PIN 13=  +2.000E-07
 PIN 14=      0
 PIN 15=      0
 PIN 16=      0
 PIN 17=      0

ILO1 TEST
 PIN 11=  +6.000E-07
 PIN 12=  +2.000E-07
 PIN 13=  +1.000E-07
 PIN 14=      0

ILO2 TEST
 PIN 11=  +8.000E-07
 PIN 12=  +2.000E-07
 PIN 13=  +2.000E-07
 PIN 14=      0

ICL TEST
 PIN 16=  +4.600E-02

ISB1&2 TEST
 PIN 16=  +1.420E-02
 PIN 18=  +1.350E-02

IPD TEST
 PIN 18=  +1.600E-02

IOS TEST AT VCCMAX
 PIN 11=  -8.200E-02
 PIN 12=  -7.800E-02
 PIN 13=  -7.400E-02
 PIN 14=  -7.800E-02

VOL TEST
 PIN 11=  +3.160E-01
 PIN 12=  +3.320E-01
 PIN 13=  +3.240E-01
 PIN 14=  +3.560E-01

VOH TEST
 PIN 11=  +2.960E-00
 PIN 12=  +2.950E-00
 PIN 13=  +2.990E-00
 PIN 14=  +2.940E-00
```

Figure A-37. Sentry Test Results of Device 2148 – DC Parameter Tests at +125°C

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