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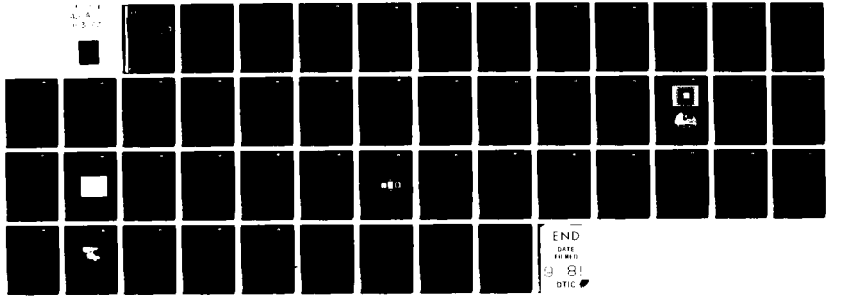

LEVEL II

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Research and Development Technical Report

DELET-TR-78-2996-2

HIGH CONTRAST ELECTROLUMINESCENT NUMERIC READOUT DEVICE

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The Microelectronics Research and Development Center of Rockwell International has completed the program encompassing the design, fabrication, and characterization of a High Contrast Electroluminescent Readout Device. The device consists of EL seven-segment numeric displays incorporating a high contrast background layer. The device also contains within its sealed package, logic and drive circuitry to operate the displays from a computer output data stream, having conventional 5-volt logic and ECD input. The package design also allows stacking the displays end to end, resulting in a multi-digit

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computer-type terminal display.

The displays delivered during this program contain internal decode and drive circuitry not heretofore available in EL displays. The ten-pin dual in-line packages with high contrast thin film EL emitter have excellent legibility in normal ambient and good legibility in high ambient light levels. Since the EL thin film emission results by a tunneling mechanism, the display is not temperature sensitive and operates over a wide temperature range, easily meeting military temperature requirements. This report describes the design, development and fabrication of the high-contrast EL displays and details the characteristics and performance of the displays as compared to program objectives.

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1.0 SUMMARY

The Microelectronics Research and Development Center of Rockwell International has completed the program encompassing the design, fabrication, and characterization of a High Contrast Electroluminescent Readout Device. The device consists of EL seven-segment numeric displays incorporating a high contrast background layer. The device also contains within its sealed package, logic and drive circuitry to operate the displays from a computer output data stream, having conventional 5-volt logic and BCD input. The package design also allows stacking the displays end to end, resulting in a multi-digit computer-type terminal display.

The displays delivered during this program contain internal decode and drive circuitry not heretofore available in EL displays. The ten-pin dual in-line packages with high contrast thin film EL emitter have excellent legibility in normal ambient and good legibility in high ambient light levels. Since the EL thin film emission results by a tunneling mechanism, the display is not temperature sensitive and operates over a wide temperature range, easily meeting military temperature requirements. This report describes the design, development and fabrication of the high-contrast EL displays and details the characteristics and performance of the displays as compared to program objectives.

2.0 PROGRAM AIMS AND OBJECTIVES

The objective of this program is to design and fabricate a quantity of numeric EL display devices containing two-digits consisting of seven segments and a decimal point. Four (4) exploratory development models have been fabricated each consisting of a ten-digit display made up of five of the two-digit numeric devices. Drive circuitry and decoding logic are included in the devices to allow operation directly from computer level logic inputs at TTL voltage levels. The display medium is a transparent AC thin film electroluminescent type with a high-contrast background layer for viewing in high-light ambients. The operational characteristics of the devices are designed as to allow a uniform electronic dimming of the display to outputs in the order of the 10^{-3} ft-L for compatability with night vision applications. The display is capable of sufficient contrast to be viewed in an ambient illumination of 10,000 ft-c without contrast enhancement techniques. The devices are capable of operation for 3,000 hours at a luminance level that satisfies the condition of visibility under high-ambient illumination described above. Also, the devices shall operate without the loss of significant light emitting areas due to any failure or degradation mechanism during the 3,000 hour/lifetime.

3.0 DEVICE DESIGN AND FABRICATION

3.1 Thin Film Emitter Structure

The design of the thin film emitter must consider the properties and effects of several variables. To achieve the optimum film performance, a careful balance of the physical, optical and electrical parameters is of vital importance. Figure 3.1 shows a cross section of a high contrast thin film EL structure. The multilayer thin film structure is deposited on a borosilicate glass substrate as shown. The Zn S:Mn EL emitter is sandwiched between layers of the Y_2O_3 dielectric to provide adequate voltage protection for driving the display.

The drive signal (typically 5kHz) is applied between the transparent conductor (backplane) and the segments of the numeric display. The backplane is common to all segments, while the segments and decimal points each have individual electrodes so they can be driven separately by digital logic as described later in this report.

3.2 High Contrast Design

Figure 3.2 shows a profile view of the high contrast numeric display. The design utilizes the common backplane as the transparent front electrode which is deposited directly on the glass substrate through which the display is observed. A low-reflectance insulator is deposited in the unused areas of the display. This material is chosen to have a refractive index approximately equal to the glass substrate so that Fresnel reflections are minimized.

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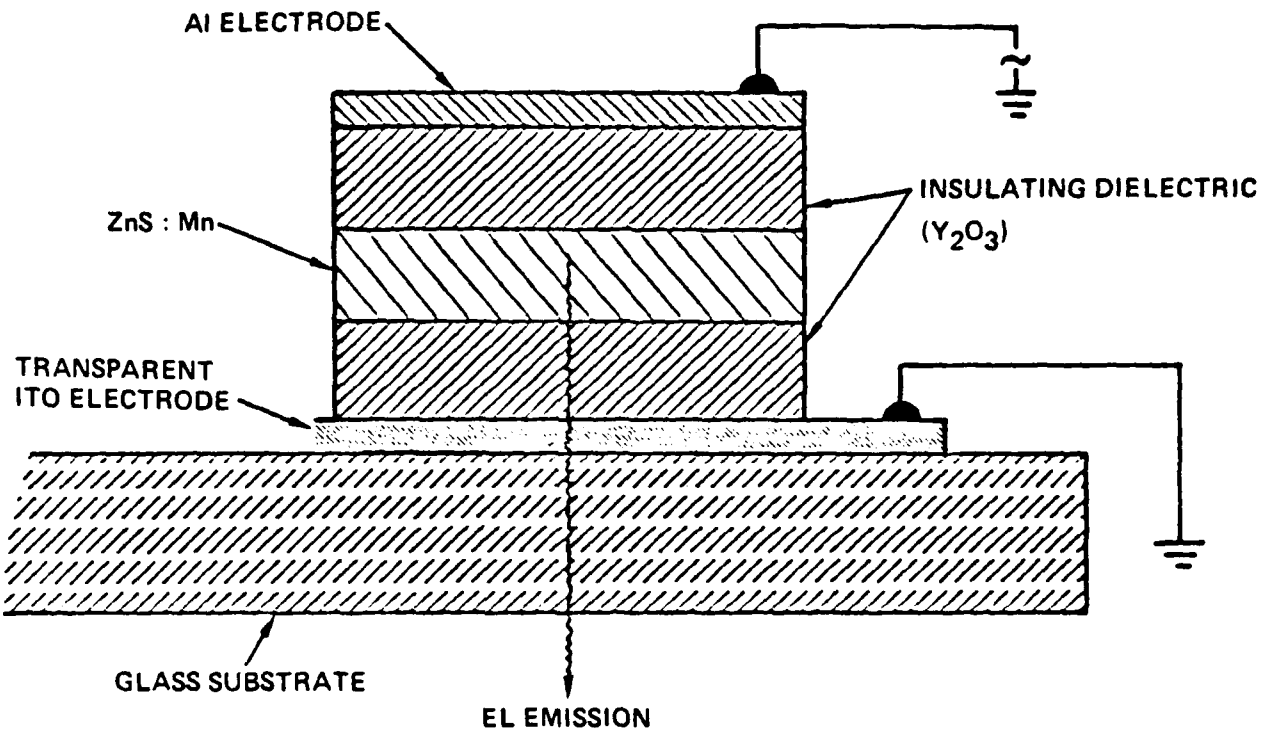

Fig. 3.1 Thin Film Emitter Structure.

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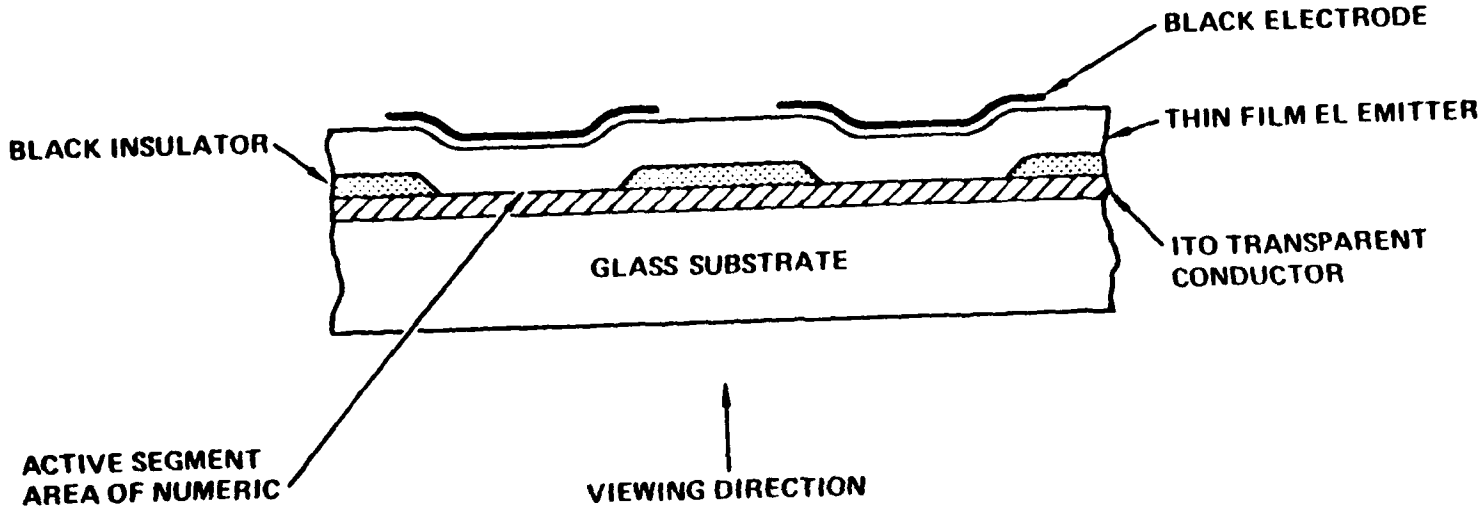


Fig. 3.2 Profile View of High Contrast Numeric Display..

The active segment areas utilize a light scattering and absorbing material as the segment electrode. This electrode material is processed to have an effective refractive index approximately equal to the Y_2O_3 rear dielectric to minimize Fresnel reflections. Since, in the active segment areas, the display consists of a combination of several thin film layers on the borosilicate glass substrate, this thin film multilayer must be carefully designed not only with regard to electro-optical performance but also with respect to the various optical reflections that can arise throughout the visible spectrum. Viewability of the display at angles significantly away from normal incidence must also be considered in the design.

3.2.1 Specular Reflection Components of A Multilayer High Contrast EL Emitter

Figure 3.3 schematically illustrates the specular reflection components from the multi-layer TFEL emitter. In this case it is assumed that the reflection at the glass-air interface is minimized by an external anti-reflection coating; therefore the front surface reflection is not shown in Fig. 3.3. It is also assumed tnat the black backing is a perfect absorber so $R_4=0$. Therefore, in order to minimize the major reflection R_1 at the glass ITO interface, the magnitude and phase of successive reflection components R_2 and R_3 are adjusted by means of thickness control of d_2 and d_3 to exactly cancel R_1. The ITO and first Y_2O_3 are lumped as a single layer since the index of refraction for each are similar.

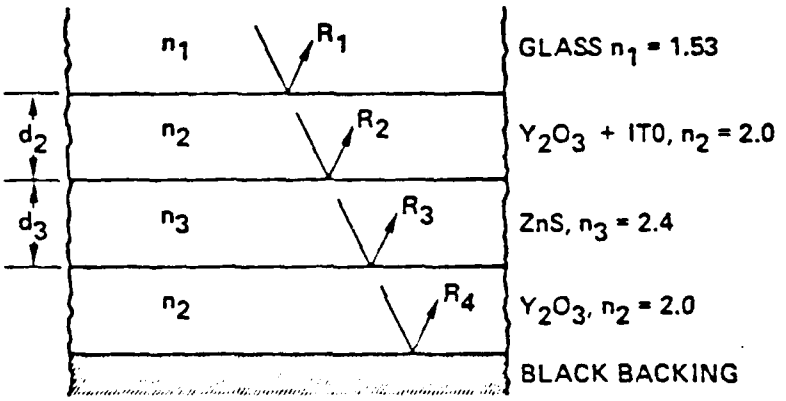


Fig. 3.3 Specular Reflection Components from Multilayer TFEL Emitter.

The following discussion develops an expression for optimum thicknesses of d_2 and d_3.

Using Ruoard's Method[1] one can calculate the reflectivity of a multi-layer system by a recursive procedure. In the present case the reflection R_1 (glass-ITO interface) can be expressed in terms of the Fresnel co-efficiencs (r) and the accumulated phase in each layer as follows:

$$R_1 = \frac{r_1 + s_2 R_2}{1 + r_1 s_2 R_2} \quad ; \quad r_1 = \frac{n_1 - n_2}{n_1 + n_2} \quad , \tag{1a}$$

$$s_2 = e^{4\pi i n_2 d_2/\lambda}$$

$$R_2 = \frac{r_2 + s_3 R_3}{1 + r_2 s_3 R_3} \quad ; \quad r_2 = \frac{n_2 - n_3}{n_2 + n_3} = -R_3 \quad , \tag{1b}$$

$$s_3 = e^{4\pi i n_3 d_3/\lambda}$$

The coefficient R_i represents the total reflectivity contributed by all the layers below the i^{th} layer.

The requirement that R_1 vanish reduces to:

$$R_1 = \frac{r_1 + s_2 R_2}{1 + r_1 s_2 R_s} = 0 \tag{2}$$

or

$$r_1 + s_2 \left[\frac{(1-s_3) r_2}{1 - s_3 r_2^2}\right] = 0$$

$$r_1(1-s_3 r_2^2) + s_2(1-s_3) r_2 = 0 \tag{3}$$

[1] OS Heavens Optical Properties of Thin Solid Films, Dover Publications, 1965.

assuming $s_3 r_2^2 \ll 1$

$$\frac{r_1}{r_2} \approx -s_2(1-s_3) = -e^{i\phi_2}\left(1-e^{i\phi_3}\right) \tag{4}$$

$$= -e^{i\phi_2}\left|1 - \cos\phi_3 - i\sin\phi_3\right|$$

$$= -2e^{i\phi_2}\left[\sin^2\frac{\phi_3}{2} - i\sin\frac{\phi_3}{2}\cos\frac{\phi_3}{2}\right]$$

$$= 2ie^{i\phi_2}\sin\frac{\phi_3}{2}\left[\cos\frac{\phi_3}{2} + i\sin\frac{\phi_3}{2}\right]$$

$$= 2e^{i\frac{\pi}{2}}e^{i\phi_2}e^{i\frac{\phi_3}{2}}$$

Since r_1/r_2 is real, in order to satisy the equation it is necessary that the right-hand side be a real number; this means that the total phase $(\frac{\pi}{2} + \phi_2 + \frac{\phi_3}{2})$ must be an integer multiple of π. When it is an even multiple, one has

$$\frac{r_1}{r_2} = 2\sin\frac{\phi_3}{2}\text{ , which has solutions} \tag{5}$$

$$\phi_3 = 2\left[2n\pi + \sin^{-1}\left(\frac{r_1}{2r_2}\right)\right]\text{ , or} \tag{6a}$$

$$\phi_3 = 2\left[(2n+1)\pi - \sin^{-1}\left(\frac{r_1}{2r_2}\right)\right]\text{ .} \tag{6b}$$

When the phase is an odd multiple of π, one has

$$\frac{r_1}{r_2} = -2 \sin \frac{\phi_3}{2} \text{ , which has solutions} \tag{7}$$

$$\phi_3 = 2\left[2n\pi - \sin^{-1}\left(\frac{r_1}{2r_2}\right)\right] \text{ , or} \tag{8a}$$

$$\phi_3 = 2\left[(2n+1)\pi + \sin^{-1}\left(\frac{r_1}{2r_2}\right)\right] . \tag{8b}$$

In the present case $n_1 = 1.53$, $n_2 = 2.0$, and $n_3 = 2.4$, so that $\sin^{-1}(r_1/2r_2) = 0.82$ radian. We seek a solution wherein the ZnS layer is roughly 4000Å thick and the composite ITO-Y_2O_3 layer is about 2800Å thick, as determined by other device constraints. Taking $d_3 \approx 4000$Å and an operating wavelength $\lambda \approx 5800$Å gives $\phi_3 = 20.48$ radians, corresponding to $d_3 = 3940$Å.

This choice forces the total phase to be an odd multiple of π, which gives the relation

$$\phi_2 = (2m + 1)\pi - \frac{\pi}{2} - 10.24 \tag{9}$$

On the otherhand, we seek a solution near $d_2 = 2800$Å, for which $\phi_2 = 12.2$ radians. The closest one can come is $m = 3$, which gives $\phi_2 = 10.18$ radians, corresponding to $d_2 = 2348$Å.

The above analysis considers the emission wavelength, 5800 Å. For reflected ambient light all wavelengths of the visible spectrum should be considered, weighed by the photopic response of the eye and the spectral radiance of the sun to obtain a realistic estimate of contrast performance. The improvement on contrast of a relatively monochromatic emitter in a broad sunlight ambient is difficult to estimate.

3.3 High Contrast Display Performance

Since the optimum design must consider the entire spectrum, a computer model was implemented to predict display reflection characteristics. Figure 3.4 shows the reflection vs. wavelengtn calculated for an EL film having the following structure:

N(0) = 1.53 - (Borosilicate Glass Substrate)

N(1) = 2.00, T(1) = 207 nM - (ITO + Y_2O_3)

N(2) = 2.36, T(2) = 400 nM - (ZnS)

N(3) = 2.00, T(3) = 207 nM (Y_2O_3)

N(4) = 1.53 (Black Backing)

The transparent indium-tin oxide are combined as N(1) since they have essentially equal refractive indices. As mentioned earlier, the front surface of the glass substrate is assumed to be coated with a low reflectance material; therefore, reflections from this surface would not significantly alter total reflectance data.

Referring to Figure 3.4 the reflectance vs. wavelength varies from 10.3% peak in the blue region of the spectrum to the relatively low levels less than 0.2% at 520nM and 580nM in the green and yellow regions. The reflectance then increases to a 6% peak in the red spectral region at 630nM.

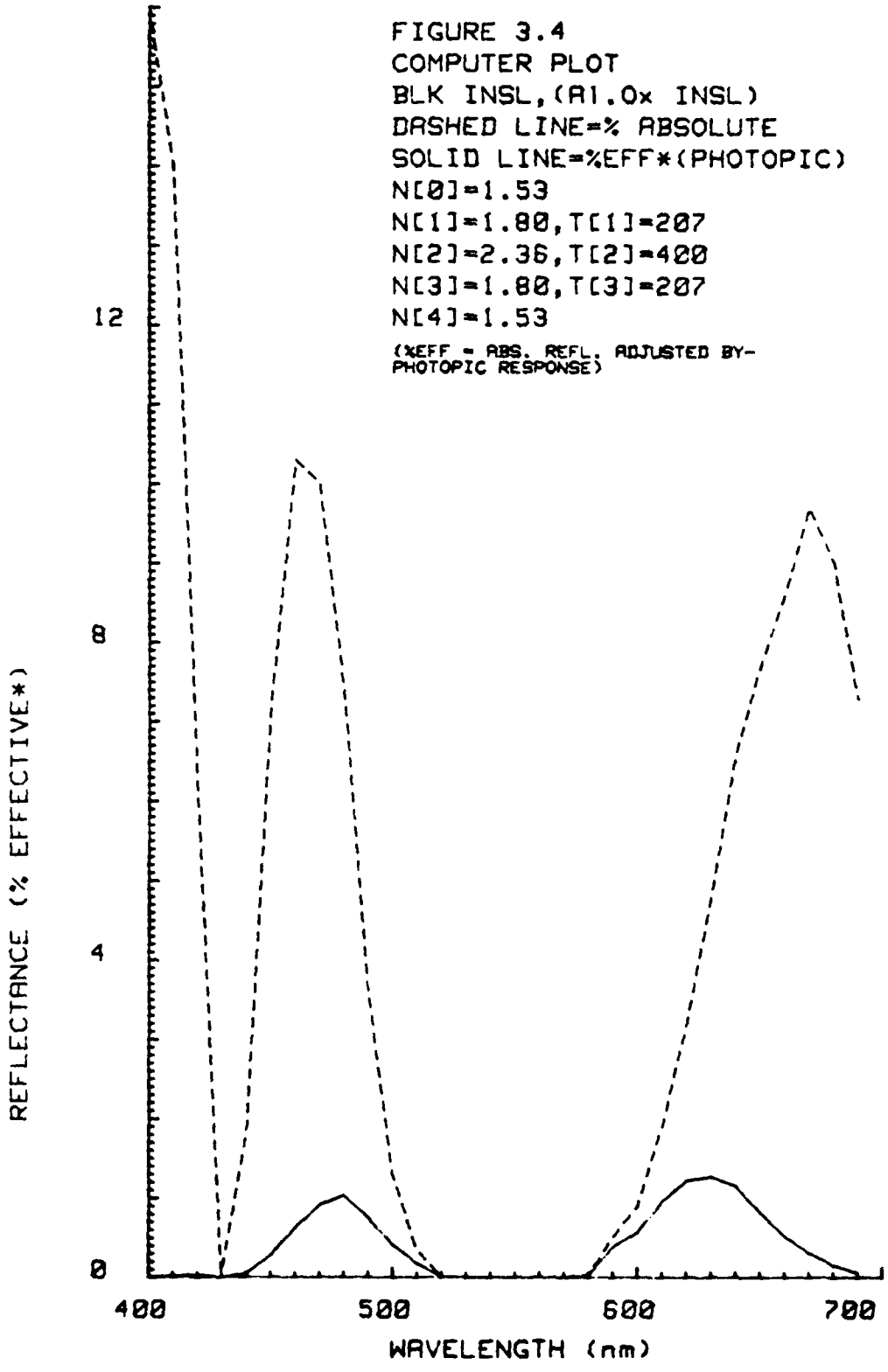


FIGURE 3.4
COMPUTER PLOT
BLK INSL,(A1.0x INSL)
DASHED LINE=% ABSOLUTE
SOLID LINE=%EFF*(PHOTOPIC)
N[0]=1.53
N[1]=1.80,T[1]=207
N[2]=2.36,T[2]=400
N[3]=1.80,T[3]=207
N[4]=1.53
(%EFF = ABS. REFL. ADJUSTED BY-PHOTOPIC RESPONSE)
12
8
4
0
REFLECTANCE (% EFFECTIVE*)
400
500
600
700
WAVELENGTH (nm)

The thin film display is designed to minimize reflections in the 500 to 600 nanometer area where photopic response is the highest. Despite the relatively high absolute reflections in the blue and red portions of the spectrum, the effective reflections (effective reflection is defined as the absolute reflection adjusted by the photopic response) average only 0.5% and peak at only 1% as can be seen in the solid line data in Fig. 3.4. The reflectance between 500 and 600 nanometers has been reduced essentially to zero by optically turning the combined multi-layer thin films to an interference mode.

Figure 3.5 shows reflectance data measured from an actual sample EL display. The dashed line shows the effective reflectance of the active segment area as a function of wavelength. The peak reflectance is slightly greater than 1% with the average reflectance measured at 0.43%. The reflectance of the non-segment area matches very closely that of the active area as shown by the solid line of Figure 3.5. For the non-segment area, the peak reflectance is only 0.83% with the average reflectance of only 0.40%. The close match of the active segment and inactive non-segment areas is of paramount importance in achieving good contrast in high-ambient light levels, where even small differences in reflection characteristics will be noticeable in the display. By achieving extremely low reflectance in both the active and non-active display areas, the difference in the amount of light, as well as the total light reflected, is minimized resulting in a display which maintains excellent contrast and legibility even in high-ambient illumination.

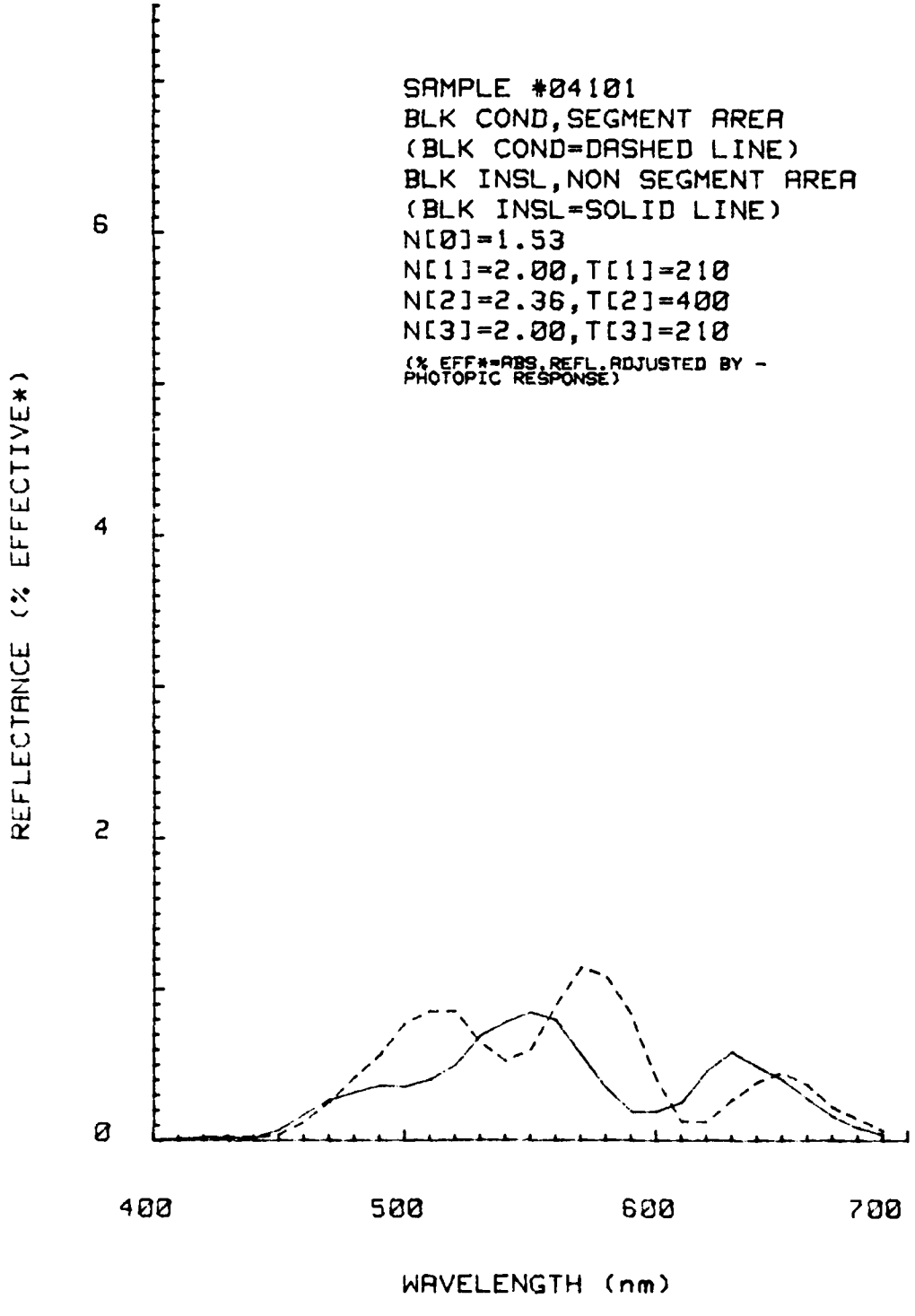


Figure 3.5 Reflectance vs. Wavelength for Sample #04101 EL Display

A sample display was placed in an integrating sphere and operated in a 10,000 ft-candle ambient, illuminated by a 2840° Kelvin light source. The display contrast was measured under the extreme ambient of the integrating sphere with the results tabulated below:

EL DISPLAY	BRIGHTNESS (FT-LAMBERTS)	REFLECTANCE % (DIFFUSE)	DISPLAY CONTRAST @ 10,000 Ft-CANDLES
Sample A	250	0.43	5.81
Sample B	250	0.43	5.81

Contrast was defined as $\frac{B_S - B_B}{B_B}$

where B_S = Source Brightness

B_B = Background Brightness

A plot of the contrast performance of the high contrast EL numeric display, a function of ambient light level, is shown in Figure 3.6.

To evaluate the display structure and determine what factors influence contrast, including the use of neutral density filters and other means, a more detailed definition of the contrast definition is applied:

where:

C = Contrast Ratio

B_P = Brightness of Phosphor EL at Inside Surface

ρ_F = Reflectance at Front Surface

ρ_S = Reflectance at Glass-TFEL Interface

τ = Transmittance of Glass/Neutral Density Filter

I = Incident Illumination in Ft-Lamberts

B_B = Total Effective Background Brightness

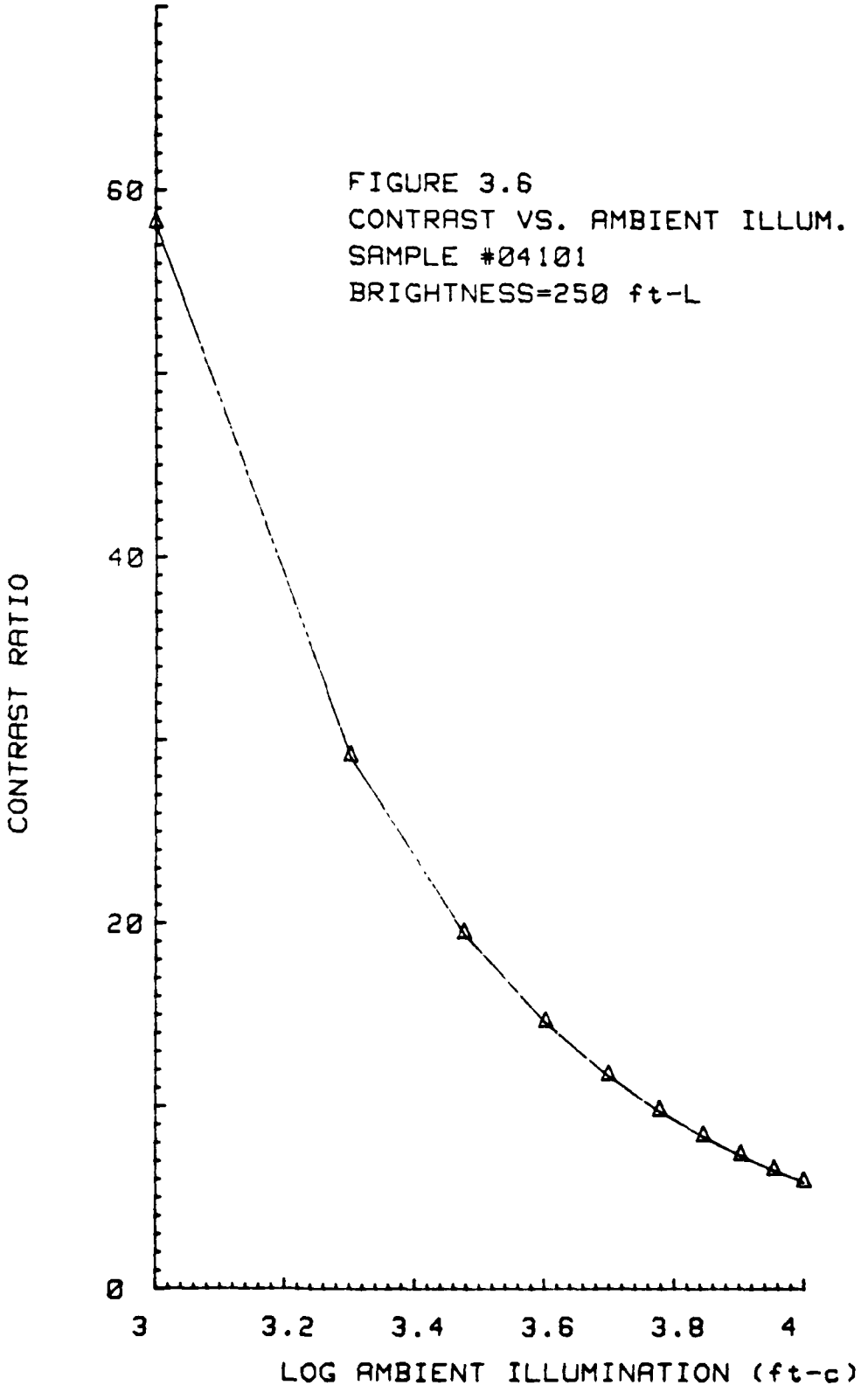


FIGURE 3.6
CONTRAST VS. AMBIENT ILLUM.
SAMPLE #04101
BRIGHTNESS=250 ft-L

$$C = \frac{B_S - B_B}{B_B} = \frac{B_S}{B_B} - 1$$

$$C = \frac{B_\rho \tau + I(\rho_F) + I[(1-\rho_F)(\tau^2 \rho_S)]}{I(\rho_F) + I[(1-\rho_F)(\tau^2 \rho_S)] + B_\rho \tau^3 \rho_Z} - 1$$

Analysis of various techniques for further contrast enhancement showed that neutral density filtering offers relatively little improvement when the black backing material has a diffuse reflectivity less than 0.5%. The attenuation of light output offsets any advantage the neutral density filter may have; contrast improvement is much more effective in the low reflectivity black backing material. Figure 3.7 shows contrast vs. illumination for various amounts of neutral density filtering, τ.

3.4 Decoder/Driver Integrated Circuit Design

Within the cost scope of this development program, a three-chip integrated circuit design was implemented utilizing a custom CMOS logic chip and two custom high-voltage DMOS drivers. The custom CMOS logic chip shown in Figure 3.8 contains all the necessary functions to interface with the two high-voltage drivers from BCD input signals. Figure 3.9 shows the signal input/output diagram of the logic IC. BCD logic signals are input with either digit 1 (EN1) or digit 2 (EN2), the signals are decoded and the segments are latched to either an "on" or "off" condition until new BCD information is received. The logic signals are coupled to the high-voltage driver chips as shown in Figure 3.10.

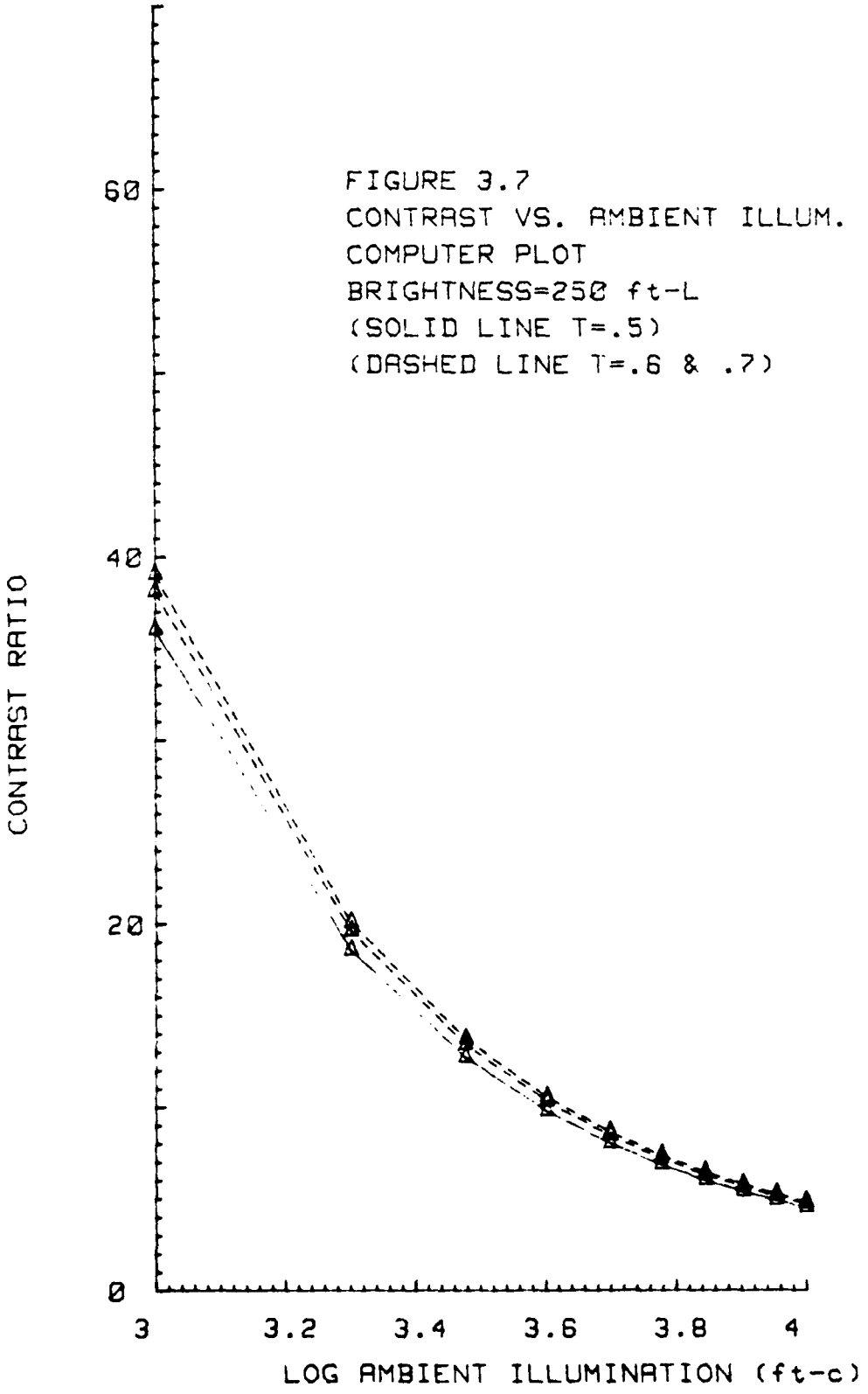
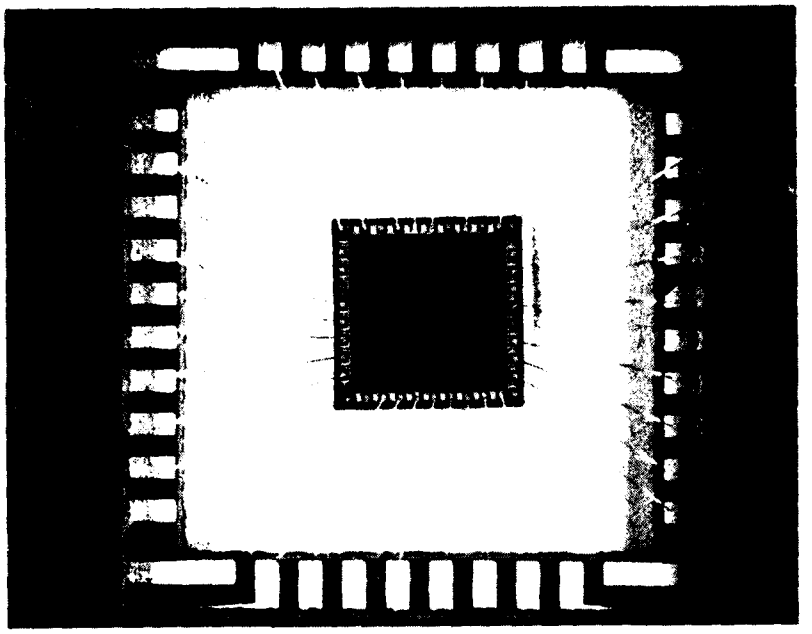


FIGURE 3.7
CONTRAST VS. AMBIENT ILLUM.
COMPUTER PLOT
BRIGHTNESS=250 ft-L
(SOLID LINE T=.5)
(DASHED LINE T=.6 & .7)



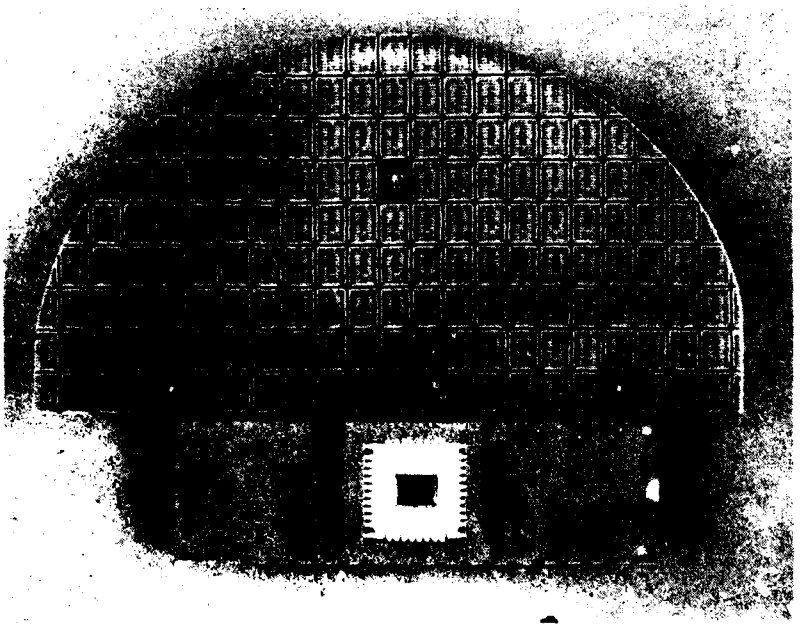
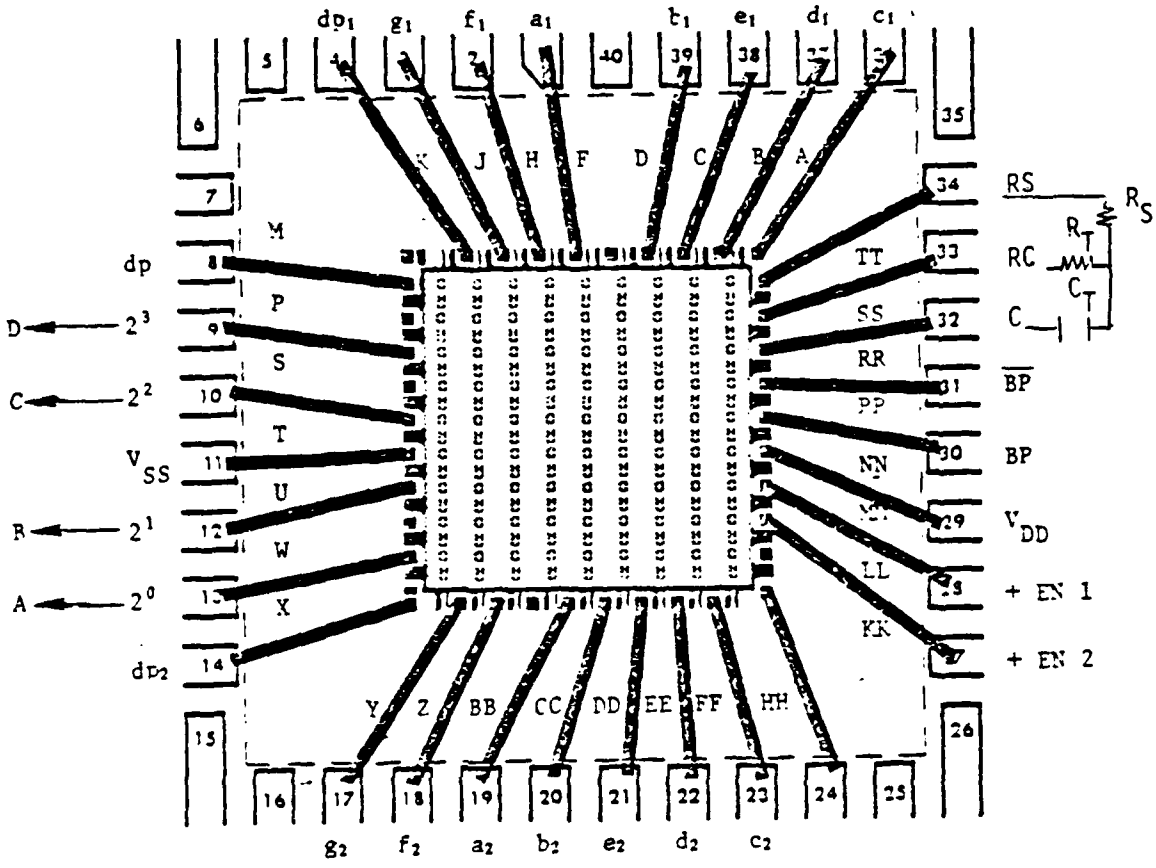


Fig. 3.8 Custom CMOS Integrated Logic Chip.



DATE: 29 August 1979 INITIALS: CAA/PCA

MARKING DIAGRAM

DIE NUMBER: RI 154
DIE SIZE: 136 x 136
SPECIAL INSTRUCTIONS: Special - Not for production

Figure 3.9 Logic Chip Input/Output Diagram

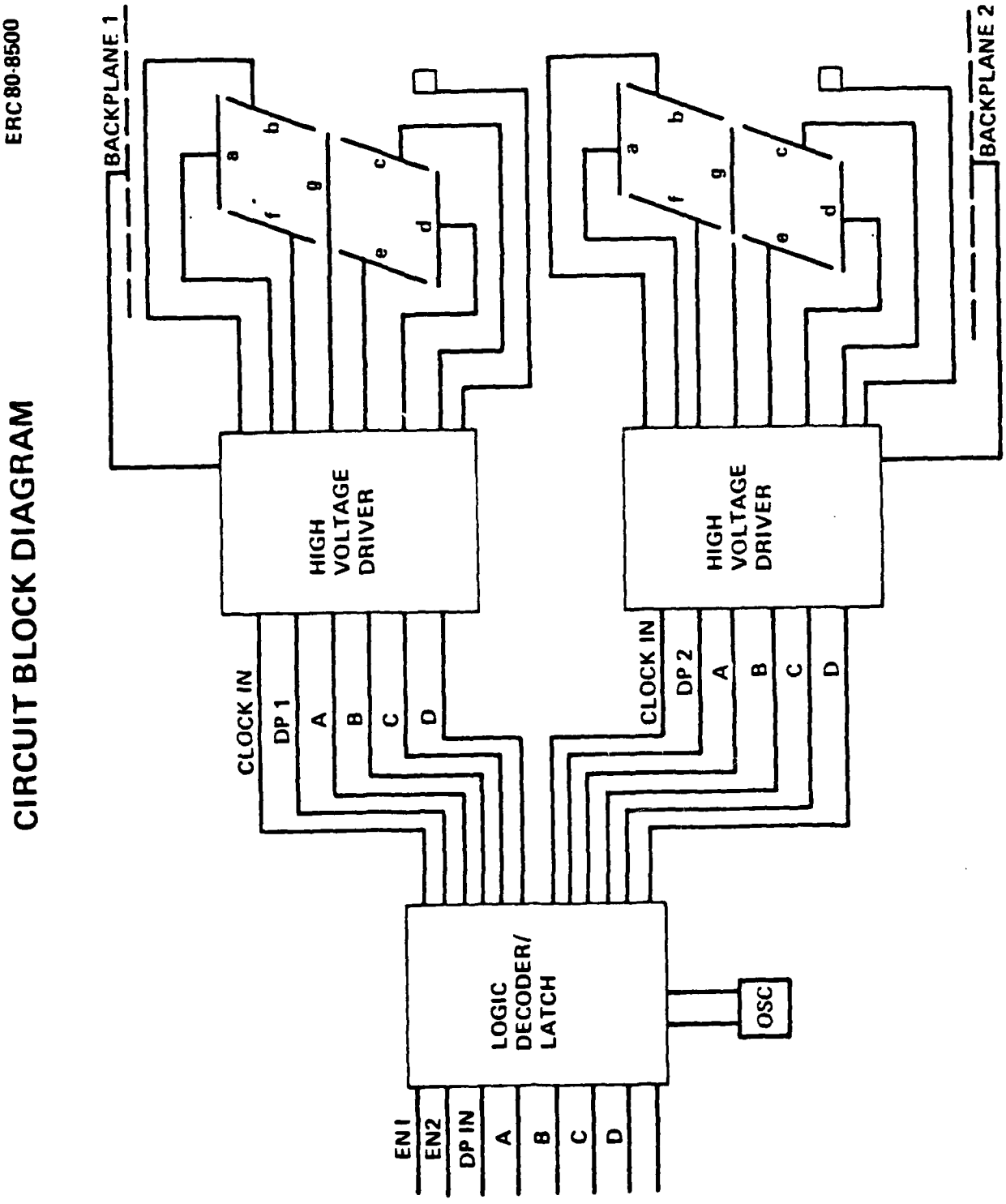


Fig. 3.10 Circuit Block Diagram.

3.4.1 High Voltage Driver Chip Design

The custom high-voltage driver chips used in this design consist of DMOS processed P-channel and N-channel FET arrays shown in Figure 3.11. The P-channel and N-channel chips are connected in a complimentary pair configuration as shown in Figure 3.12. The complimentary configuration allows efficient switching between high-voltage and ground levels without the need for pull-up resistors, thus substantially reducing power consumption.

3.4.2 Alternate Circuit Design

Unfortunately, the development of these high-voltage drivers has been seriously delayed, necessitating the use of an alternate circuit design. The alternate two-digit TFEL decoder/driver circuit using conventional available CMOS CD4042 latch circuits in conjunction with DS8880 bipolar decoder driver chips is shown in Figure 3.13. This design accomplishes the latch function in the CMOS CD4042 chip.

The BCD to seven-segment decode function is in the bipolar driver chip which has an 80-volt switching level capability and requires the use of 100K pull-up resistors. The design results in increased power consumption over the original design; however, it is uncertain even at this writing when the DMOS FET drivers will be completed.

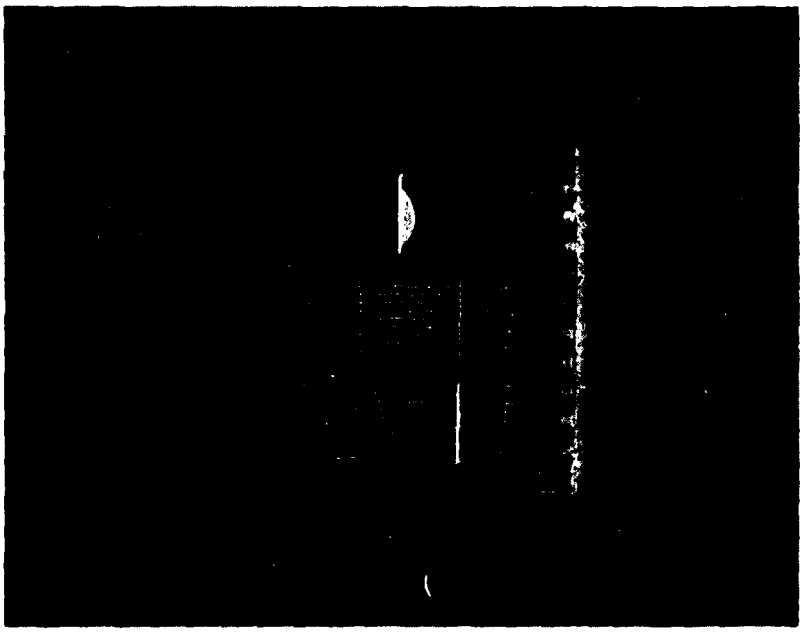


Fig. 3.11 High Voltage Driver Chip Assembly.

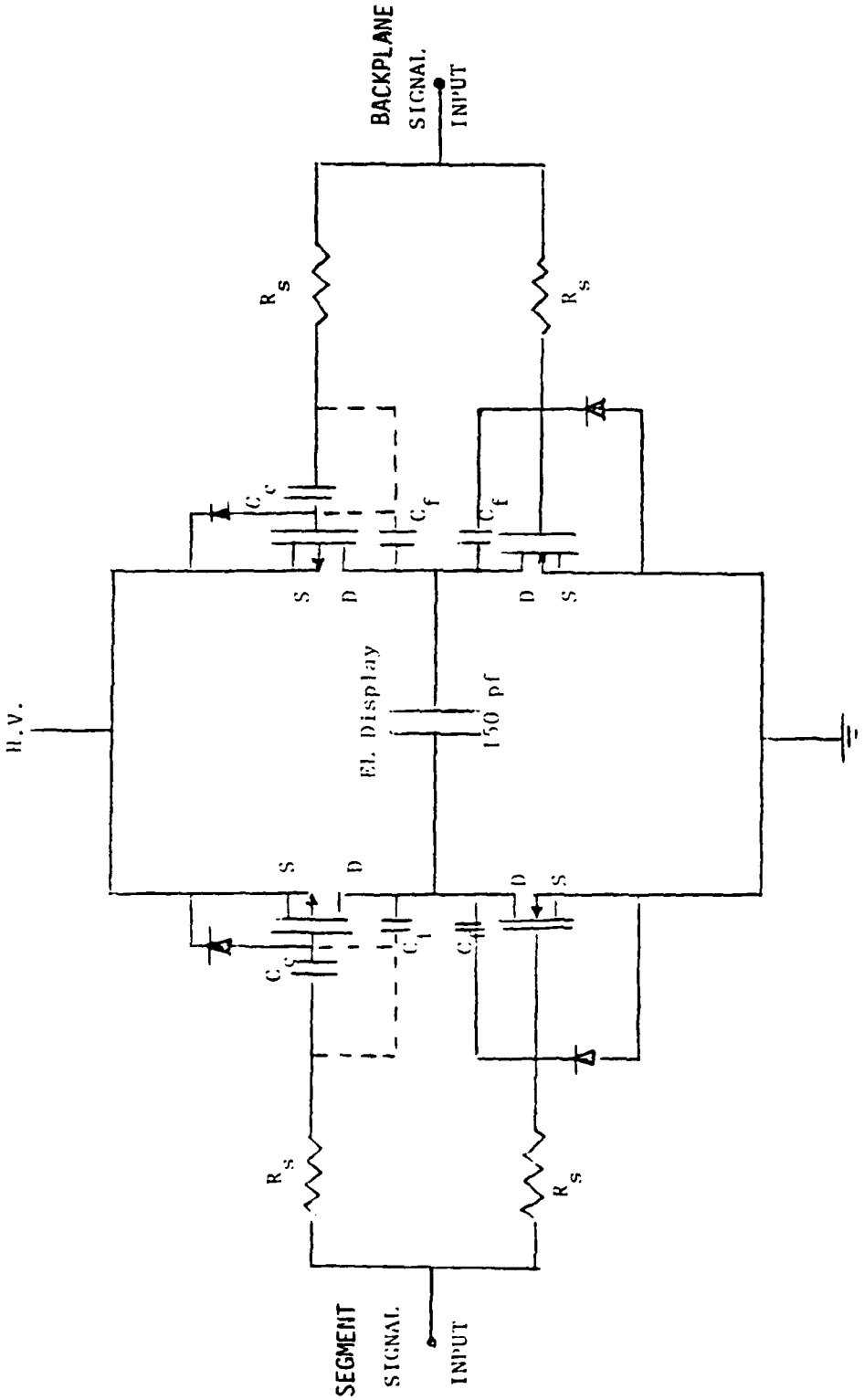


Fig. 3.12 High Driver Circuit Design.

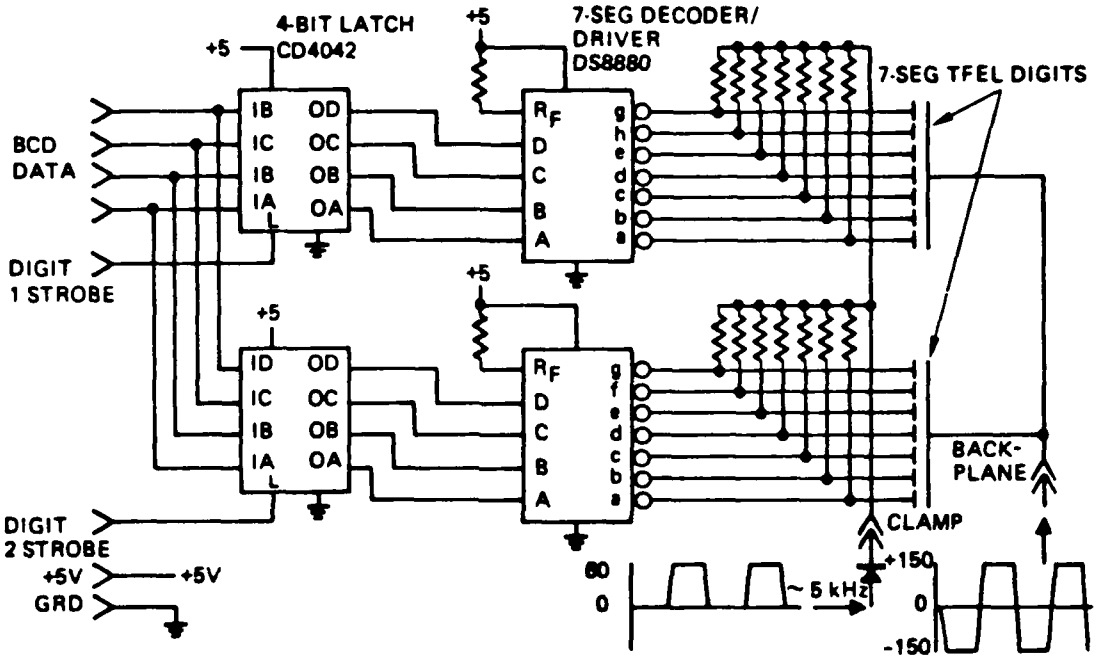


Figure 3.13 Alternate Two-Digit Circuit Design

4.0 EL DISPLAY DESIGN FABRICATION AND ASSEMBLY

4.1 Hermetic Seal and Package Design

The hermetic packaging of TFEL displays required development of new techniques, since truly hermetic EL thin-film displays have not yet been fabricated. Perhaps the most unique requirement is a vertical interconnection between the hybrid driver circuitry and the EL display which is deposited on the integral front window of the package. Figure 4.1 shows a cross sectional view of the hermetic seal design. The hybrid circuit utilizes convention thick-film circuitry with standard die attach and wire bonding methods.

Since the number of units to be fabricated was small, a seal design resulting in moderate tooling cost was used. A ceramic sidewall frame was frit-sealed to the ceramic substrate to form the package cavity. The top surface of the sidewall frame was metalized, fired and then braze sealed to the 7059 glass substrate on which the thin-film EL structure was deposited. A separate channel using thick film conductors was used to accomplish the vertical interconnect between display and drive circuitry. The channel was installed prior to sealing so that the top surface of the thick film conductors formed the interconnect to the display when the package was sealed. This method resulted in reliable connections with a high yield and excellent reliability.

Figure 4.2 is a photograph of the component parts of the display showing the component parts as follows:

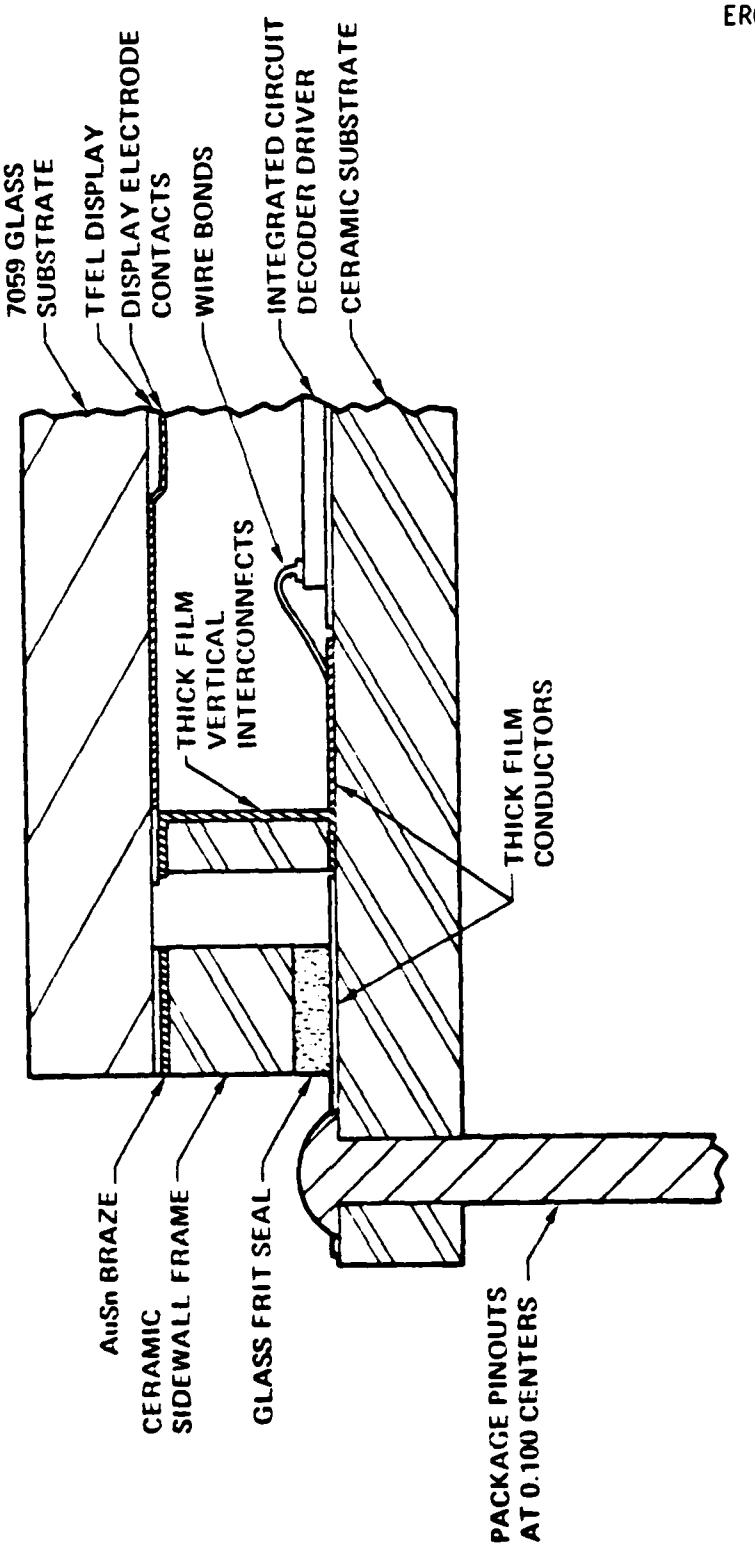


Fig. 4.1 EL Hermetic Package Design.

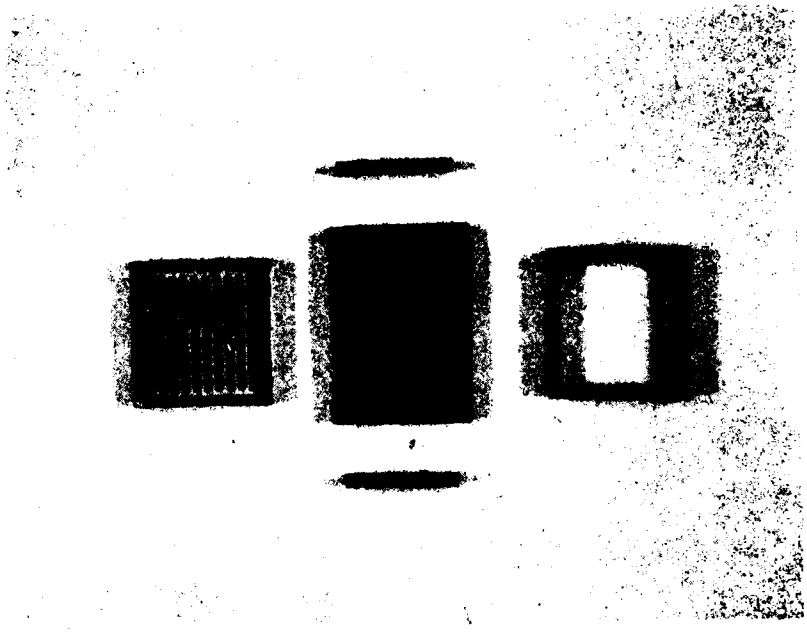


Fig. 4.2 Hermetic Package - Component Parts.

1. 7059 glass substrate (phosphor);
2. Alumina ceramic substrate (hybrid circuit);
3. Vertical interconnect channels;
4. Ceramic sidewall frame.

An exhaust/seal port was also designed into the ceramic substrate to establish a controlled atmosphere in the package after the main seal. The final seal of the exhaust port is a high temperature solder seal. The package can esaily withstand -55^{o}C to +125^{o}C environment.

5.0 DISPLAY ELECTRO-OPTICAL CHARACTERISTICS

5.1 Brightness and Efficiency Performance

All TFEL displays are evaluated for luminous output, impedance, power dissipation and efficiency. A select sampling are placed on test for evaluation of operating life and maintanence characteristics. The devices are driven with a constant 5KHz sinusoidal voltage with periodic measurement of characteristics.

Figure 5.1 shows the brightness vs. voltage characteristic for a typical high-contrast numeric display driven at 5KHz. The high contrast TFEL structure has similar threshhold voltage to the more common metal electroded structure, but does not benefit from the reflective properties of the metal electrode structure. Typical peak brightness for the high-contrast cells range from 350 to 500 ft-lamberts with the peak at 372 ft-lamberts for the curve shown. The total cell thickness is controlled to minimize reflections, as described earlier.

Figure 5.2 shows the efficiency and power dissipation for a typical segment again driven at a 5KHz frequency. The data is from the same sample as the brightness data so that typical brightness efficiency and power dissipation may be compared. For comparison at a brightness of 150 ft-L, the segment voltage is 111 volts, the power dissipation is 4.5 milliwatts and the efficiency is .45 lumens per watt. Because of the larger package required to house the interim circuitry, the segment areas are larger than will be used in later production versions where the power dissipation is expected to be about 2.5 milliwatts per segment. Power dissipation per digit would be reduced from the present 22.5 milliwatts to 12.5 milliwatts.

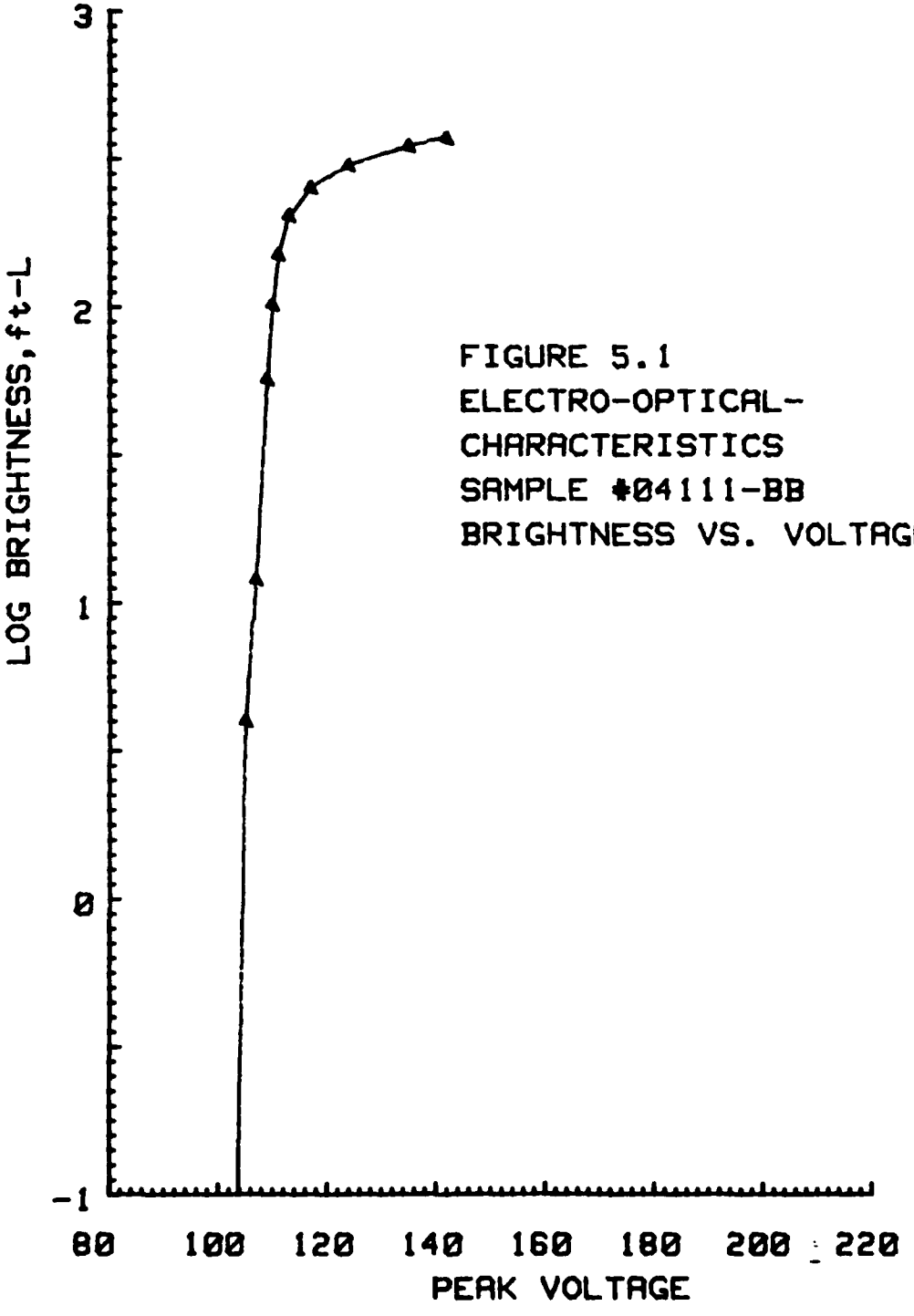


FIGURE 5.1
ELECTRO-OPTICAL-
CHARACTERISTICS
SAMPLE #04111-BB
BRIGHTNESS VS. VOLTAGE

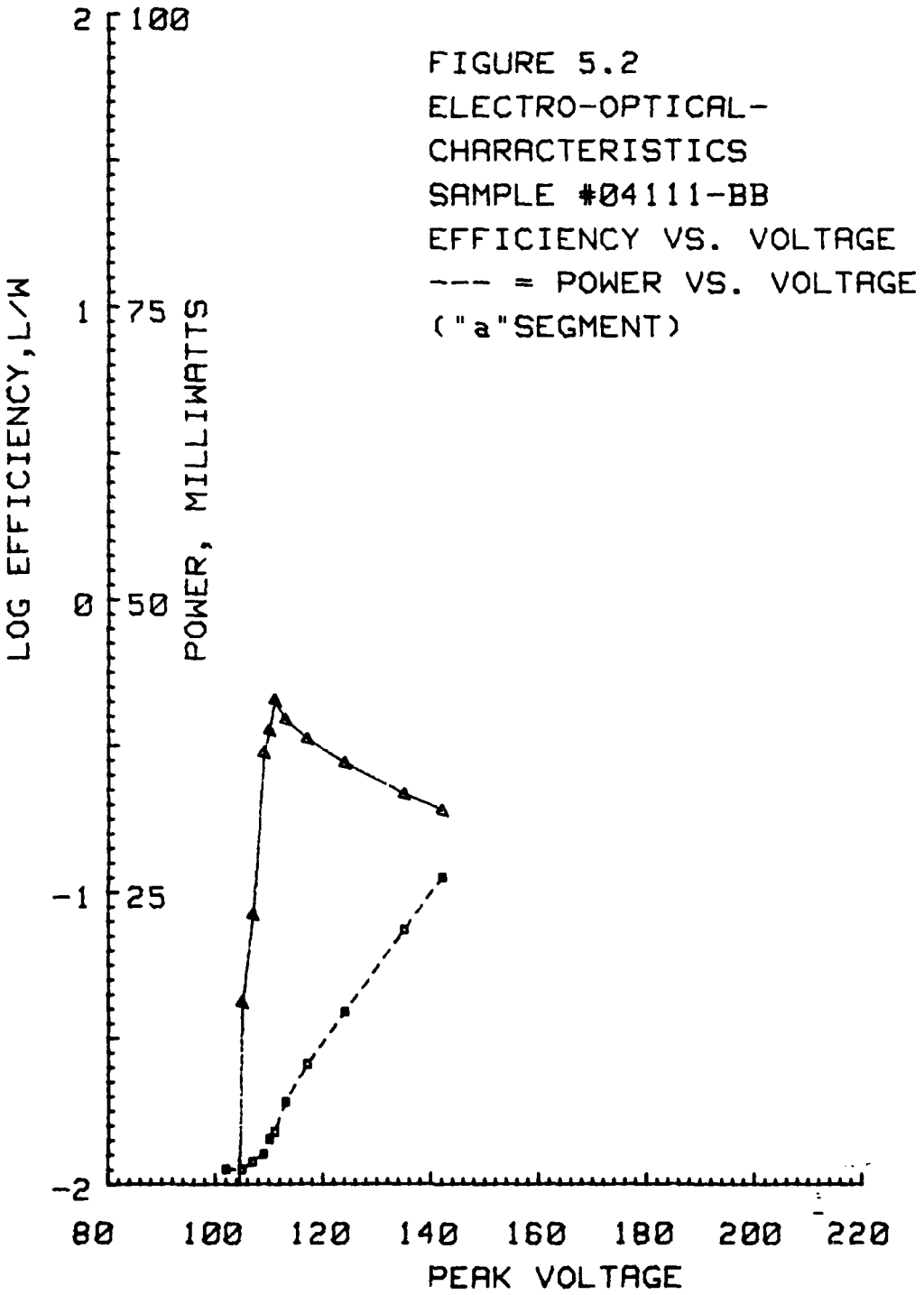


Figure 5.2 Efficiency and Power Dissipation

5.2 Display Contrast vs. Ambient Illumination

Figure 5.3 shows display contrast vs. illumination for a typical display operating at 250 ft-L. The data was taken in an integrating sphere, as described earlier. Contrast was measured as defined in Section 3 in an integrating sphere. The contrast ratio was 290:1 at 200 ft-c; 58:1 at 1,000 ft-c; and 5.8:1 at 10,000 ft-c. The displays were judged easily legible by several observers at 10,000 ft-c. The goal of 3:1 contrast at 10,000 ft-c was exceeded by almost 2 to 1. A photo of the 2-digit numeric is shown in Figure 5.5.

5.3 Operating Life and Maintanence Characteristics

Operating life was conducted under constant voltage continuous drive 5KHz excitation at 100 ft-L initial brightness. As is typical in TFEL displays, the brightness declines slightly during the first 100 hours of operating and then remains relatively stable. Figure 5.4 shows the operating life characteristics for 2 high-contrast numeric displays. In Sample #01161, the brightness declines to 97% of the original brightness after 100 hours and remained at this level out to 1500 hours. Sample #41101-BB declined to 82% after 1500 hours of operation.

While the mechanism of the decay is not clearly understood, this type of decay curve appears to be typical of decay characteristics with displays having been tested for up to 30,000 hours with very little decay after 100 hours of operation.

The high contrast TFEL displays have excellent life and reliability characteristics. Design of the devices with an open circuit pinhole failure mechanism minimizes the possibility of any catastrophic failures.

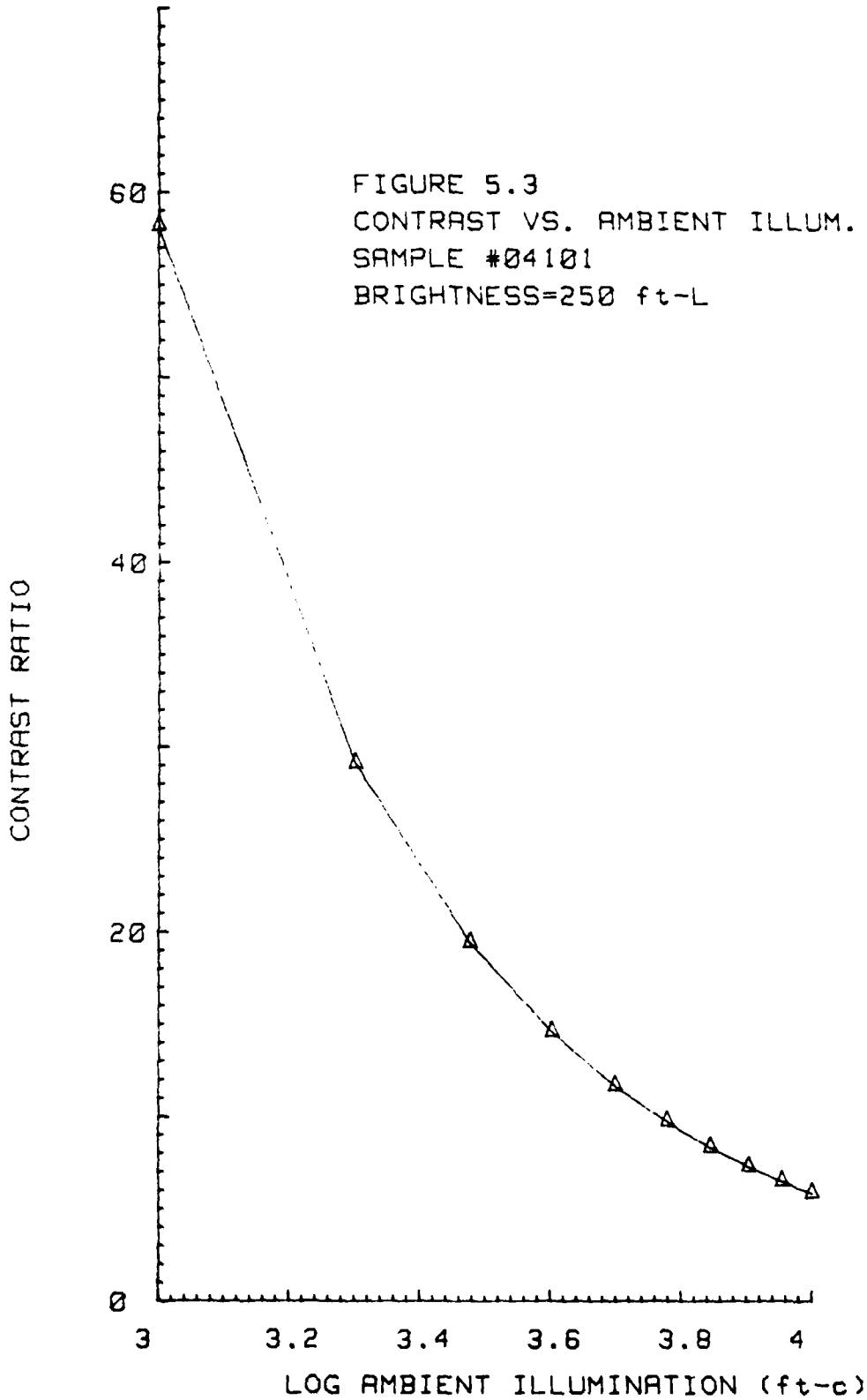


Figure 5.3 Display Contrast vs. Ambient Illumination

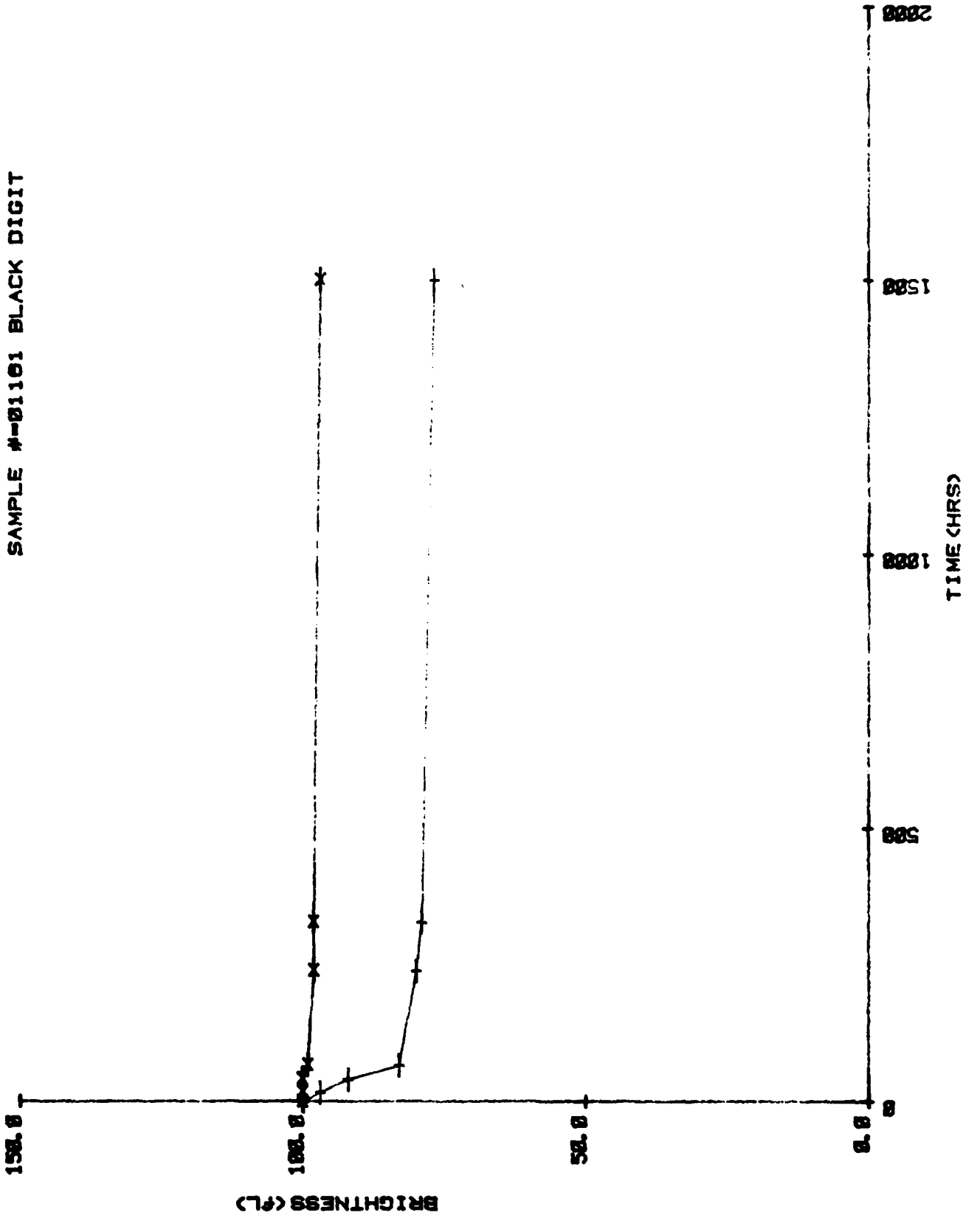


Figure 5.4 Operating Life & Maintenance Characteristics

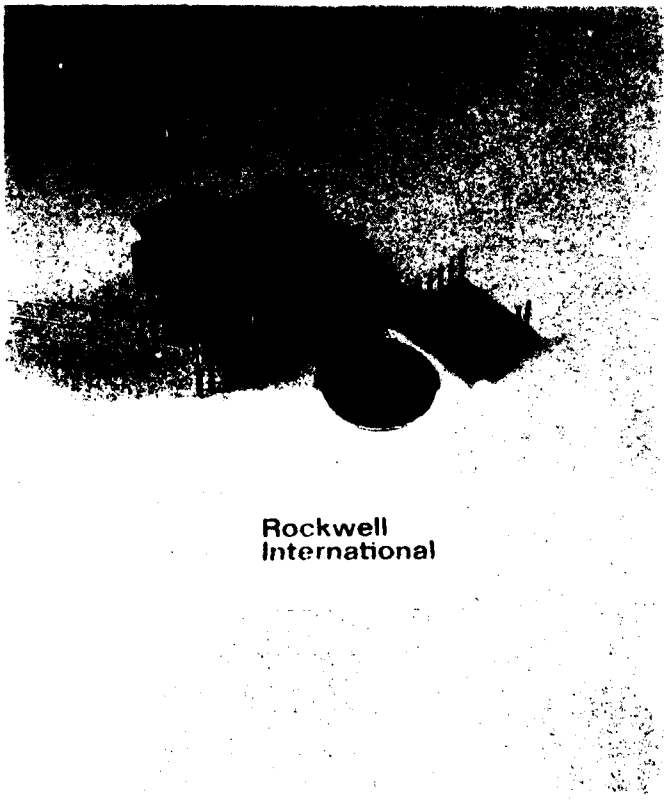


Fig. 5.5 Operating EL 2-digit Numeric Display.

6.0 CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER DEVELOPMENT

6.1 Conclusions

The program to develop high-contrast EL numeric displays was completed with the delivery of 20 two-digit EL numerics with integral decoder/driver circuitry. The displays are capable of viewing in high-ambient direct-sunlight conditions. The displays are driven directly with low-level BCD logic signals and have latched inputs which retain signal information until new information is received. The latched circuitry allows multiplexing multiple digits on a single input circuit using "digit select" (enable) lines to select digit to which new input signals are transmitted.

This program was significantly delayed by the unavailability of high-voltage driver chips as discussed in the previous section on high-voltage driver design. When it became apparent that further delays would be encountered, an alternate circuit design, using available lower-voltage driver chips, was implemented. While this design produced usable displays, driver-power consumption was higher than original designs, due to the necessity of utilizing bipolar driver chips rather than DMOS FET drivers which continue to be unavailable at this writing. The FET performance of the test chips indicate that the driver power of the bipolar types (50 milliwatts per segment) could be reduced to less than two milliwatts per segment. The actual EL segment dissipation of three milliwatts per segment would result in an overall power consumption of 40 milliwatts per digit, including logic, driver and segment power. Total package power for a two-digit package would be reduced to less than 100 milliwatts, as compared to the present 420 milliwatts.

6.2 Recommendations for Further Development

The circuit design originally proposed contained a logic decoder chip and two high voltage driver chips as previously discussed. With recent developments in DMOS FET driver technology, an approach using a single DMOS P-channel FET integrated circuit including on-board decoder logic should definitely be undertaken in any future refinements or further manufacturing methods and technology programs for EL numeric displays.

Such a design would further reduce power requirements, simplify the design and allow packaging of multiple digits in arrays of 2, 4 or 8 digits, simply by use of larger logic arrays. For example, a single chip IC would drive four digits, including decimal points. The only additional circuitry required is a single NMOS FET to drive the back-plane electrode. Use of the single chip design reduces the input leads to eight pins even for a four-digit display, a significant simplification. Reducing the size and number of integrated circuits also simplifies circuit complexity wire bonding, and interconnection requirements making feasible smaller more compact displays for applications requiring more digits in a smaller format and space.

An alternative, using the single chip approach, is the implementation of 16-segment alphanumeric two-digit displays using the same type of single chip approach with a single NMOS FET backplane driver.

Rockwell also recognizes the importance of achieving a reliable continuous insulating high contrast layer and is continuing research efforts in this area. Despite excellent contrast ratio and surface reflection data obtained in presently delivered samples, the capability of a continuous black layer to completely reject all background reflection patterns is a powerful advantage and virtually mandatory requirement for the ultimate high-contrast display. While Rockwell has achieved continuously black high-contrast layers, reliability of these structures must be improved by further material research and process development to attain a continuous high-contrast layer comparable in reliability to our present conventional EL structures.

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