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A104000

LEVEL III

Research and Development Technical Report

AD A104001

A FAST TURN AROUND FACILITY
FOR VERY LARGE SCALE INTEGRATION (VLSI)

A SEMI-ANNUAL TECHNICAL STATUS REPORT
January 1, 1981 to June 30, 1981

DARPA Contract No. MDA 903-80-C-0432
ARPA Order No. 4012

Sponsored by:
Defense Advanced Research Projects Agency

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Office Of Naval Research
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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

19 REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM	
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER	
18) DELET-TR-80-0432-2	AD-A204 002		
4. TITLE (and Subtitle)		5. TYPE OF REPORT & PERIOD COVERED	
6) A Fast Turn-Around Facility for Very Large Scale Integration (VLSI).		Interim Report No. 2 1/1/81 - 6/30/81	
		6. PERFORMING ORG. REPORT NUMBER	
		8. CONTRACT OR GRANT NUMBER(s)	
7. AUTHOR(s) James D./Meindl, James D./Plummer, Robert W./Dutton, R. Fabian/Pease, J./Beaudouin, D. Dameron, L. Gerzberg, K. Saraswat, J. Shott, T. Walker		13) MDA 903-80-C-0432 DARPA Order-4012	
9. PERFORMING ORGANIZATION NAME AND ADDRESS		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS	
Stanford Electronics Laboratories Stanford University Stanford, CA 94305		DARPA Order No. 4012	
11. CONTROLLING OFFICE NAME AND ADDRESS		12. REPORT DATE	
9) Interim rept. no. 2, 1 Jan-30 Jun 81,		11) July, 1981 12) 48	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		13. NUMBER OF PAGES	
Office of Naval Research Stanford Branch Stanford University			
		15. SECURITY CLASS. (of this report)	
		UNCLASSIFIED	
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE	
16. DISTRIBUTION STATEMENT (of this Report)			
APPROVED FOR PUBLIC RELEASE DISTRIBUTION UNLIMITED			
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)			
18. SUPPLEMENTARY NOTES			
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)			
Integrated Circuit Fabrication; VLSI Wafer Fabrication. 10000 - 6,000,000			
20. ABSTRACT (Continue on reverse side if necessary and identify by block number)			
In order to appreciate the critical hardware and software problems associated with the definition and design of very large scale integrated circuits or integrated systems including 10^4 - 10^6 transistors in a single silicon chip, incisive experiments conducted with actual operating chips are indispensable. The objective of this project is to establish, within a university research environment, a facility for the rapid execution of mask generation, wafer fabrication, and functional testing of user-generated custom I.C. designs.			

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19. KEY WORDS (Continued)

20 ABSTRACT (Continued)

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Research Project

A FAST TURN-AROUND FACILITY
FOR VERY LARGE SCALE INTEGRATION (VLSI)

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Defense Advanced Research Projects Agency

ARPA Order No. 4012

Under Contract No. MDA 903-80-C-0432
issued by Department of Army, Defense
Supply Service - Washington
Washington, D.C. 20310

Effective Date July 1, 1980

Expiration Date September 30, 1983

Performance Period January 1, 1981 - June 30, 1981

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INTRODUCTION

This document is the second semi-annual report for the Stanford University Fast Turn Around Facility project DARPA Contract No.: MDA 903-80-C-0432 covering the period January 1, 1981 to June 30, 1981.

SUMMARY

1/1/81 to 6/30/81

SUMMARY

This document describes activity in the DARPA sponsored Fast Turn Around Facility for VLSI Project during the period January 1, 1981 to June 30, 1981. The principal goal of the FTAF is to provide fast turn-around fabrication of silicon integrated circuits for the local VLSI design community. The Stanford Integrated Circuits Laboratory (with close cooperation from Stanford's Information Systems Laboratory and Computer Systems Laboratory) has been actively pursuing many of the practical aspects of producing small numbers of custom designed integrated circuits with a short turn around time. This report will focus on many of the facilities, equipment, and fabrication issues which affect our ability to fabricate and test these custom designed chips.

The FTAF Project is organized into the following four major activities:

- FTAF Wafer Fabrication
- Electron Beam Lithography
- Electrical Wafer Testing
- VLSI Device Research

More detailed descriptions of each of these four areas appear as individual sections later in this report. However this summary will describe the important activities and results in each of the four areas that have occurred during the past six months.

The principal activity of the FTAF wafer fabrication group has been the fabrication of a set of MPC (multi project chip) wafers containing 32 student designed projects from the Mead-Conway based class taught by John Newkirk and Rob Mathews at Stanford. The complexity of this mask set was simply too great for our present David Mann 1600 optical pattern generator, so we were

obliged to look to the outside for mask making assistance. In this case the CIF files of the design projects were sent to ISI where they were packed into die types, their standard test stripe was added, and a MEBES format tape was prepared. This set of projects was packed into seven different die types, each measuring 7.34 mm by 7.86 mm with a minimum feature size of 5 microns ($\lambda = 2.5$ micron). Amdahl Corporation agreed to prepare the chrome master plates using their ETEC MEBES machine. Because these wafers would be fabricated using contact printing equipment, we had contact plates made at Micro Fab to eliminate the risk of destroying the E-beam written masters. We received the contact plates from Micro Fab and began processing a lot of six 50 mm wafers on February 12, 1981. The process used to fabricate these wafers was described in a previous semi-annual report (July 1, 1980 - December 31, 1980): a six mask enhancement/depletion process. Wafer fabrication was completed on February 16, 1981, and we began to deliver packaged devices on February 26, 1981. The testing results of these devices have been reported elsewhere by Newkirk and Mathews.

During this time period we undertook a joint fabrication project with Dr. Gordon Kino and Jonathan B. Green of the Ginzton Laboratory at Stanford. Together we designed a novel ZnO on Silicon device which consists of a 700 element diode array, a pair of interlaced 350 element shift registers to read signals into and out of the diode array, a piezoelectric ZnO layer, and the appropriate transducers to transmit/receive surface acoustic waves along the ZnO. We feel that this project was significant for the following three reasons:

- (1) It demonstrated the coupling of two DARPA funded projects to produce a new device with greater capabilities than would have been achieved without this close interaction.
- (2) It demonstrated the ability of the FTAF to respond quickly to the system needs of a "user" group: The desired acoustic frequencies required a very narrow diode spacing (10 microns center-to-center) which in turn required a shift register with a very small pitch.

The layout of this tightly packed shift register called for the use of "buried contacts" in the NMOS process (at the cost of an additional masking step) -- the ZnO on Silicon device was the first circuit built by the FTAF to incorporate buried contacts into the process, although it appears that they are sufficiently desirable to offer them to all designers soon.

- (3) It demonstrated that the defect density in the Stanford University IC Lab is decreasing: The yield of electrically functional shift registers was roughly 20 - 25% on a die measuring 3 mm by 9 mm and containing over 4000 buried contacts per die.

In April, 1981, the Integrated Circuits Lab was shut down for a lengthy period for a series of major renovations and equipment modifications. The most major of the renovations is the replacement of the entire fume exhaust/ make-up air system at a cost of \$2,000,000. The new system (which is being paid for by Stanford University) will (1) provide sufficient exhaust capability to greatly enhance our ability to SAFELY work with the toxic gases and chemicals commonly encountered in integrated circuit fabrication and (2) provide sufficient HEPA filtered make-up air to keep the laboratory under positive pressure and thus reduce the concentration of airborne particles in the fabrication areas.

While a lengthy shut down of this type is obviously unpleasant, we strongly feel that these major renovations are a necessity if we are to achieve the objectives of the current DARPA FTAF contract.

During this extended shut-down period we are purchasing and installing new pieces of process equipment, modifying existing equipment where needed, and renovating the existing facility to enhance our ability to reliably and controllably produce larger circuits. Among the major changes underway are:

- (1) Purchase and installation of a new bank of furnaces including tubes which will be devoted to the low pressure chemical vapor deposition (LPCVD) of silicon nitride and phosphorus doped, low temperature silicon dioxide. The new furnace systems will produce thin films with greater uniformity and fewer "pinhole" defects than previously available in our laboratory.

- (2) Replace and/or modify equipment to allow us to process full 75 mm (3 inch) wafers. Among the areas being changed are wafer cleaning stations, photoresist application and exposure, and the ion implantation wafer chamber. These improvements will increase yield by eliminating the silicon dust which is produced by the processing of partial wafers.
- (3) Prepare the site for the arrival of the ETEC electron beam lithography system and associated plate/wafer processing equipment. The temperature, humidity, vibration, and particle count requirements of this area are exceedingly stringent.

Activity in the area of wafer testing has focused on the installation and initial check-out of the Tektronix S3260 general purpose digital tester. Several "demonstration chips" have been fully exercised on the test system. Present effort is being devoted to the task of installing a UNIX operating system and the appropriate interface so that the S3260 will be compatible with and can communicate with the remainder of the design and simulation software environment. Bridging the "communication gap" between design and test seems to be an important first step in the overall attempt to design more testable circuits.

In the area of VLSI device research, we have recently completed the fabrication of buried-channel MOS transistors and depleted-base bipolar transistors with minimum feature sizes as small as 1 micron using the Canon FPA 141 projection alignment system. Detailed summaries of these activities appear in the later sections of this report. We have also recently completed the fabrication of enhancement and depletion NMOS transistors with gate oxide thicknesses of 200, 400, and 600 Angstroms and channel lengths as small as 1 micron. The purpose of fabricating these "scaled" devices is to study the short channel properties of NMOS circuits so that we may optimize the next generation process schedule to be compatible with these reduced feature sizes. As was pointed out in the last semi-annual report, the present NMOS

process is suitable for channel lengths of 2-3 microns; however, feature sizes smaller than this (e.g. 1 micron in Stage 3) will require a revised process schedule. These initial experiments in fabricating and measuring scaled devices should greatly increase our understanding of the underlying device physics of short-channel MOS transistors, and thereby greatly enhance our ability to produce small geometry circuits in the FTAF during the later stages of this project.

In conclusion, during the past six months we have made significant improvements in our ability to produce complex NMOS integrated circuits with a short turn-around time as reflected by the MPC wafers produced for the local Mead-Conway design course and by the ZnO on Silicon addressed diode array which was fabricated for Dr. Gordon Kino and Jonathan B. Green of the Ginzton Laboratory. At present, we are in the midst of an EXTENSIVE set of facilities and equipment changes; however, each of these changes should greatly enhance our ability to quickly produce small volumes of high quality custom integrated circuits. Much of our current activity reflects the view that the Fast Turn-Around Facility refers to more than just the time difference from "masks-in" to "wafers-out"; it also includes the rapid incorporation of advances in device physics, materials properties, and technology into a deliverable "production" technology and the close coupling of design, simulation, fabrication, and testing so software design tools develop in concert with technological advances and so technological advances are responsive to the needs of the system designer.

Our activities during the past six months reflect the fact that we are striving to provide a state-of-the-art technology for the user community and are committed to establishing an appropriate set of user-interfaces to the design community. User groups may be Mead-Conway based design courses, Dr.

Gordon Kino in the Ginzton Lab, or ultimately, a DARPA system designer - in any case the successful coupling of a sophisticated technology to a broad user base requires a smooth set of design-simulation fabrication-testing interfaces. In particular, we feel that, at the present, the transmission of geometrical information from designer to processor is a smoother transition than the situation found during the test and characterization of a fabricated chip - we will devote much of our attention to the problems of efficiently testing a new circuit or system.

FTAF WAFER FABRICATION

1/1/81 to 6/30/81

Fast Turn - Around Facility (FTAF)

at Stanford University

Interim Progress Report - May 1, 1981

Submitted By J. D. Shott and J. D. Meindl

This report will provide a brief overview of recent activities of the Fast Turn-Around Facility at Stanford University and will concentrate on various aspects of wafer fabrication. In particular, testing results of multi-project chips produced by the FTAF will be described by John Newkirk and Rob Mathews.

The description of recent activities of the Fast Turn-Around Facility will be partitioned into the following five categories:

Stanford/FTAF MPC Wafer Fabrication

Surface Acoustic Wave on Silicon I.C. (SAWFET)

Small Geometry Devices

Electron Beam Lithography

Facility Improvements and Renovations

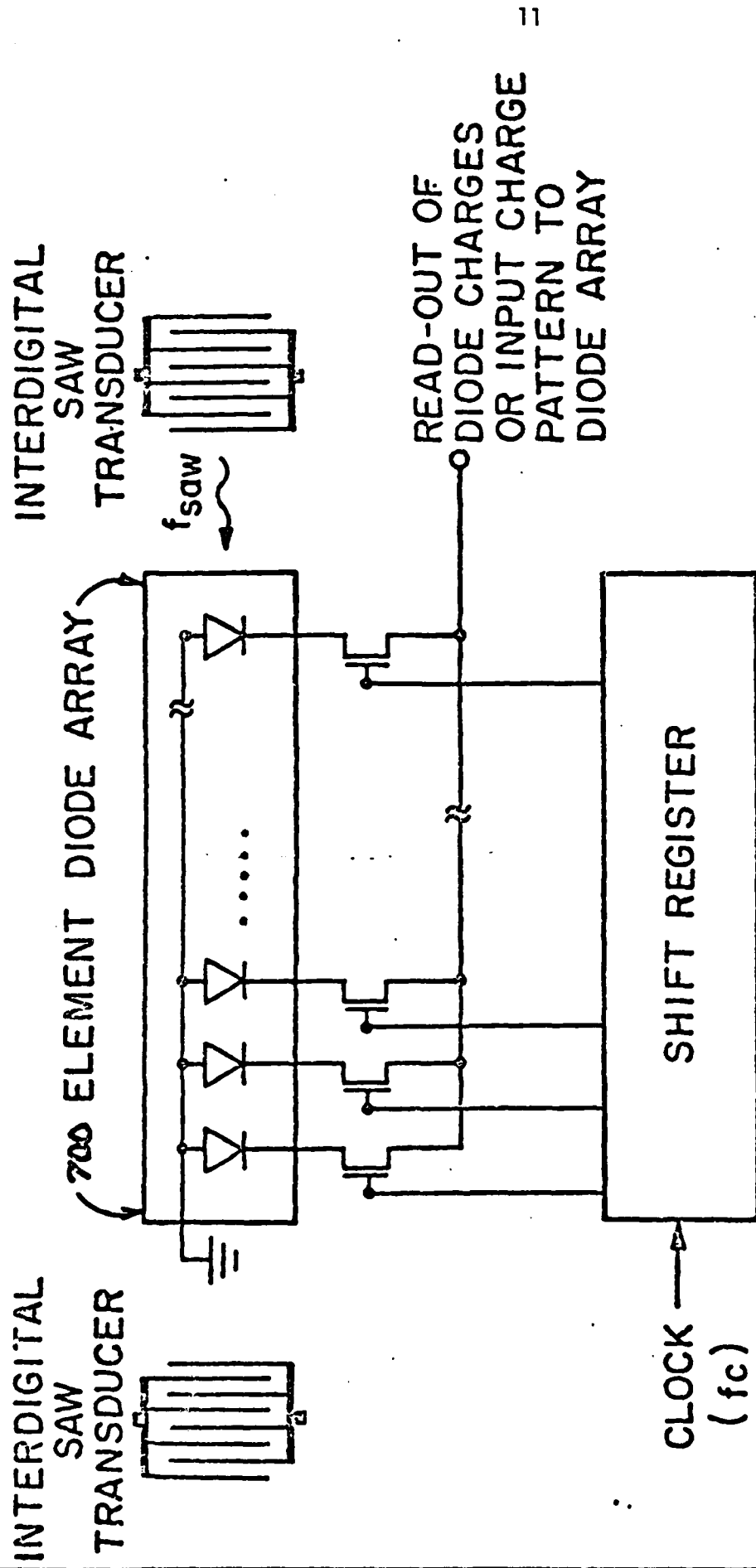
Stanford/FTAF MPC Wafer Fabrication

Early in 1981 we undertook the fabrication of a set of MPC wafers containing 32 student-designed projects from the Mead-Conway based class taught by Newkirk and Mathews at Stanford. Because of the large number of designs, pattern generation using our in-house mask making equipment was ruled out. As a result, CIF files were sent to ISI where they were packed into die types, a test stripe was added, and a MEBES format tape was prepared. The projects were packed into seven different die types, each measuring 7.34 mm by 7.86 mm ($\lambda = 2.5 \mu\text{m}$).

On January 13, 1981 we took these ISI prepared tapes to Amdahl, who had agreed to prepare the E-Beam written 1X master plates, and then on to Micro-Fab for preparation of contact plates. On February 12, 1981, we received contact plates from Micro-Fab and began processing a 6-wafer lot of 2" wafers containing 3 copies of each of the 7 die types per wafer. On February 17, 1981, we completed wafer fabrication and verified that enhancement and depletion test transistors functioned properly ($V_{TE} \approx 0.9$ V, $V_{TD} \approx -3.3$ V). On February 26, 1981 we began delivering packaged devices. Newkirk and Mathews will describe the detailed testing results of the projects in their report.

Surface Acoustic Wave on Silicon I. C. (SAWFET)

We recently completed the design, fabrication, and preliminary testing of a novel surface acoustic wave on silicon integrated circuit (SAWFET). This project was initiated by Jonathan Green and Prof. Gordon Kino of the Ginzton Labs at Stanford under DARPA sponsorship. As shown in Fig. 1, this integrated circuit combines NMOS signal processing with ZnO surface acoustic wave technology on the same chip. The NMOS portion of the circuit consists of a 700-element linear diode array (which provides signal storage) and a shift register which is used to address the diode array. Piezoelectric ZnO is sputtered over the diode array, and interdigital launch/receive SAW transducers are placed on either end of the diode array. Because of SAW center frequency requirements and the desire to provide as many diode storage sites as possible (and thereby allow more powerful signal processing capabilities) the diode pitch was chosen to be 10μ , the minimum allowed with $\lambda = 2.5$ micron. This, in turn, places very severe layout requirements on the shift register used to address this array. In particular, we found it highly desirable to use area-efficient buried contacts rather than the more conventional butting



SCHEMATIC OF SAW/FET DEVICE

Figure 1

contacts throughout the shift register design. The completed SAWFET chip measures 3.0 mm x 9.0 mm and contains over 4,000 buried contacts. Preliminary electrical testing of diode array and shift register yielded 5 out of 27 fully functional chips. We feel that the SAWFET provides a good demonstration of our ability to produce buried contacts and are prepared to offer it as an optional design feature for the next set of MPC wafers.

Small Geometry Devices

It is well known that the electrical properties of NMOS enhancement/depletion transistors do not scale ideally with minimum feature size, particularly as the minimum feature size becomes less than 3.0 μm ($\lambda = 1.5$ micron). To be fully prepared for the impact of non-ideal device scaling at the system level, we must first begin by understanding these phenomena at the device level by examining small geometry enhancement/depletion NMOS transistors and/or by investigating alternative technologies which may offer superior performance at small geometries.

We have recently fabricated, and are in the process of characterizing, a set of enhancement/depletion NMOS test devices with gate lengths and channel widths ranging down to ≈ 1.0 micron and gate oxide thicknesses as thin as 20 nm. These devices were produced with a Canon 4:1 reducing projection alignment system and conventional positive photo resist (Shipley AZ1470J).

Alternative small geometry devices which are under study in our laboratory include buried channel MOS devices and the depleted-base bipolar transistor (also known as the static induction transistor). Both of these types of devices have been fabricated with minimum feature sizes as small as $\approx 1.0 \mu\text{m}$. The buried channel MOS transistor is particularly attractive because it potentially offers reduced small geometry effects while maintaining the comparative design simplicity of conventional NMOS structures.

Electron Beam Lithography

Although optical lithography can be used to produce test devices with minimum features as small as one micron, requirements for greater linewidth control, registration accuracy, and throughput make electron lithography a desirable alternative to optical techniques for the fabrication of large circuits. Initially electron lithography will be used for the preparation of chrome IX masks and later to directly write patterns on the wafers.

A MEBES system has been purchased from ETEC and has passed factory acceptance. At present the system has demonstrated a minimum spot size of $.25\text{ }\mu\text{m}$, a butting tolerance of $\leq 0.125\text{ }\mu\text{m}$, and a layer-to layer registration accuracy of $\leq 0.25\text{ }\mu\text{m}$ when directly writing a pattern on top of a previously patterned wafer that has been purposely mis-aligned by as much as 3° .

At present FTAF staff members are undergoing training at ETEC, and site preparations, as described in the next section, are under way at Stanford.

Facilities and Equipment

The fabrication of larger circuits with smaller feature sizes calls for greater process control and reduced defect densities. As a result, much of our current effort is aimed at installing process equipment and renovating the process facility to achieve tighter process control and lower defect densities.

We are currently replacing the existing laboratory fume exhaust system with a higher performance air handling system which will allow us to more safely handle the toxic substances required in wafer fabrication and, by providing filtered make-up air under positive pressure, will substantially reduce defects due to airborne particulate contamination. At the same time, we are beginning the extensive site preparation required for the electron beam lithography system. These preparations include the installation of a

seismic pad for vibration isolation, installation of precise temperature and humidity control, and installation of the resist processing equipment to develop and etch electron-written patterns on masks or on wafers. Finally, we are specifying, purchasing, and installing a number of pieces of equipment which will increase process control or reduce the defect densities in the FTAF. In particular we are investigating additional plasma etching equipment so that we may more precisely define the aluminum metallization on our wafers.

In conclusion, the Integrated Circuits Lab (with close cooperation from Stanford's ISL and CSL) has been pursuing many of the practical aspects of producing small numbers of custom designed integrated circuits with a short turn-around time. In particular, we are aggressively pursuing facilities, equipment, and process issues which affect defect densities and device yields. Furthermore, by working closely with local system designers we are attempting to more smoothly bridge the design-fabrication and fabrication-testing interfaces. Finally, by closely coupling our activities to systems activities we are striving to make our technological advances more responsive to particular systems requirements.

PLASMA ETCHING ACTIVITIES

Dry etching has been recognized as an essential tool for the pattern delineation of VLSI fabrication. Such activity to support the Fast Turn Around Fabrication was initiated last August. This section of the report discusses the progress in these activities in the period from October 1980 to April 1981.

I. Installation of the system

The first plasma etcher, model AMNPS-1 from Plasma Therm, was successfully installed last August. The system is planar-type etcher, with the maximum capacity of six 4-inch wafers in one cycle. A typical etching cycle takes approximately 30 min. from loading to the removal of wafers after etching. The etch rate varies with materials to be etched as well as the operating condition. However, the operating conditions can be easily adjusted so that the etch rate is maintained between 100 to 1000 Å/min. The system can be operated in two modes: normal plasma etching and reactive ion etching modes. The latter mode gives better anisotropic etching, but at the expense of chemical selectivity. (The RIE mode operates at much lower pressure, which is near the marginal pumping capability of the vacuum system. RIE mode etching has not yet been investigated.)

The system accepts three processing gases and three purging gases. In supporting the most critical etching steps in NMOS process, i.e., polysilicon, nitride, oxide and p-glass, the processing gases presently installed are O_2 , CF_4 , C_2F_6 , C_3F_8 and $CClF_3$. CF_4/H_2 has also been acquired for the etching of oxide.

A sequential programmer has been added to the system to facilitate operation. This allows fully automated etch cycle from pump down to venting of the chamber.

II. System performance characterization

The performance of plasma etching mode has been characterized. In such characterization, fine line masks with minimum linewidth of $1.25\ \mu\text{m}$ are used. Both the Alpha-step thickness monitor and a scanning electron microscope are used to determine the etched depths and etching profiles. Only the average etch rate can be measured by dividing the etch depth by the etching time.

The most characterization work done for the system is the etching of polysilicon, since such replacement by dry etching is the most crucial step in many fabrication processes. It has at least two advantages: (a) simplification of process and, (b) better control of etching profiles. Extensive etching characteristics using CF_4/O_2 gas mixtures has been studied and its performance is summarized below:

(1) The worst undercut is approximately 100% of etched depth in all experimental conditions tested. With the proper choice of etching condition, the under cut can be controlled to be less than 20% of the etched depth.

(2) Etching uniformity is generally within 5% across the wafer. However, near the wafer edge, the etch rate can be 10% larger than that of the center, and is worse at high power density. This non-uniformity is believed to be caused by the local non-uniform distribution of the electrical field. The non-uniformity can be reduced by using a larger loading wafer underneath the etched wafer.

(3) The loading effect persists for all wafer areas. It also depends on the wafer location. Wafers closely placed show more loading effect than wafers well separated. It is advisable to load the wafers separated with equal distance from each other in the etcher.

(4) Etching at high power levels (above 300 watts) does not necessarily increase the etch rate, rather the etching becomes less uniform across the wafer.

(5) With 2% O_2 in CF_4 , the typical oxide etch rate is 10 Å/min at 50 watts and 100 mtorr, compared to more than 500 Å/min for polysilicon. The chemical selectivity is excellent.

(6) Small percentage of oxygen typically increases the polysilicon etch rate by several times.

(7) N^+ polysilicon etches faster than undoped polysilicon. The dependence of etch rate as a function of doping concentration has not yet been investigated.

(8) Etch rate increases as the pressure is raised from less than 100 mtorr to about 400 mtorr. Further pressure increase has a negative effect on the etch rate. The best pressure for etching is between 100 and 300 mtorr.

A typical etched structure of 1.25 μm lines of polysilicon running across a 0.5 μm height vertical oxide step is shown in Fig. 1. The photoresist has not yet been stripped. The polysilicon was etched by CF_4 at 100 watts and 150 mtorr for 20 minutes. The oxide step in this particular structure was created by previous etching of Si wafer before oxidation by using $CClF_3/C_2F_6$ mixture. Excellent anisotropic etching profile with negligible undercut was achieved. Fig. 2 shows the same structure but with the photoresist stripped. The continuity of polysilicon line across the oxide step is excellent.

IV. Summary

The first stage of dry etching activities has been successfully implemented. The etching characteristics for polysilicon have been characterized. Anisotropic etching with good chemical selectivity of polysilicon over oxide has been achieved. Polysilicon lines as narrow as

1.25 μm can be etched without having the problem of residuals at step. NMOS as well as CCD devices have successfully been fabricated using this dry etching capability.

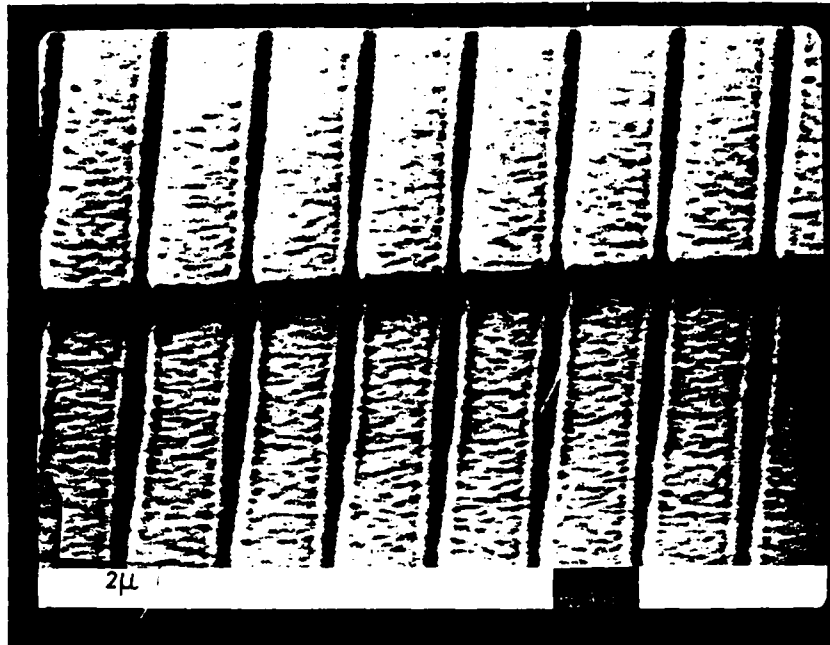


Figure 1

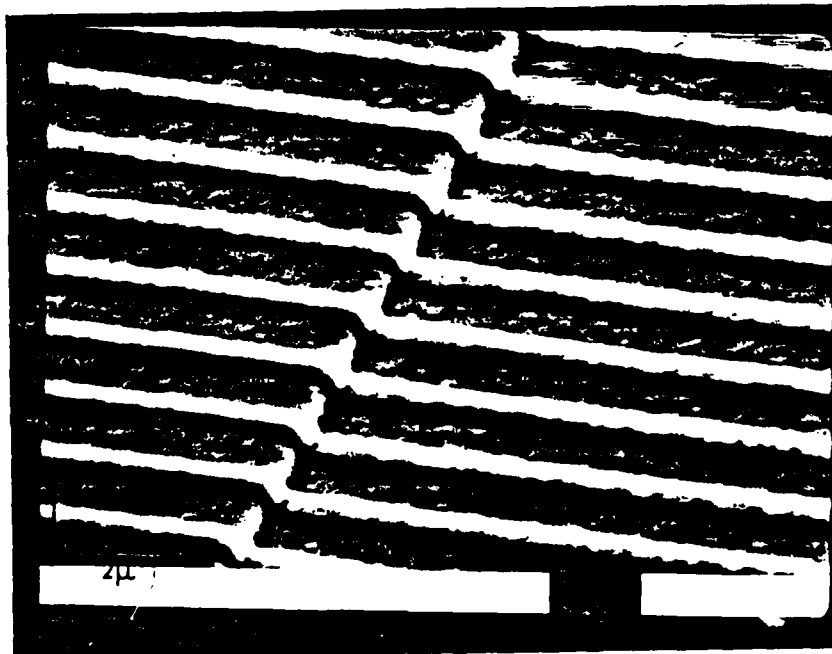


Figure 2

MULTILAYER INTERCONNECTION TECHNOLOGY

Krishna C. Saraswat

Within the last couple of decades tremendous progress has taken place in the area of microelectronics. With the advances in technology, the integrated circuit chip size, complexity and device packing density is continuously increasing. Many of these advancements can be attributed to improved fabrication technology. New developments in lithographic and etching techniques have resulted in reduction in the minimum feature size used in the integrated circuits. At the same time improvements in materials technology have allowed integration of more and more devices on the same chip, resulting in increased area. The reduction in the size of the device geometry has resulted in faster devices. According to the theory of scaling, the speed of an MOS transistor is inversely proportional to its channel length. As a first order approximation therefore, this should proportionally increase the circuit speed. Indeed for smaller circuits it does happen. However, for larger area circuits the time delays associated with the interconnections can play a significant role in determining the performance of the circuit. As the minimum feature size is made smaller, the area of cross section of the interconnection also reduces. At the same time, for state of the art technology, the chip area increases causing the length of the interconnections to increase. The net effect of this Scaling of Interconnections is reflected into an appreciable RC time delay. For very large chips with extremely small geometries, the time delay associated with interconnections could become an appreciable portion of the total time delay and hence the circuit performance could no longer be decided by the device performance.

The time delay associated with the interconnections is dependent upon two factors; the resistance of the interconnections and the capacitance controlled by the dielectric media. Generally silicon dioxide is used as the dielectric. The success of silicon in microelectronics can be largely attributed to excellent properties of Si/SiO₂ interface and ease of thermal oxidation of silicon to produce a passivating layer of SiO₂. Therefore as far as the dielectric material is concerned, our choice is somewhat limited to SiO₂. Fortunately for interconnections a variety of materials have been used which can be broadly classified into three categories: (1) metals, (2) polycrystalline silicon and (3) metal silicides. Historically, metals like aluminum and gold have been used in bipolar and MOS integrated circuits. With the advent of silicon gate MOS technology, polysilicon has been extensively used to form the electrodes and interconnections. However, its high resistivity is beginning to limit the performance of the larger area circuits. Refractory metals such as tungsten (W), molybdenum (Mo), titanium (Ti) and tantalum (Ta) and their silicides are receiving increased attention as a replacement/compliment of polysilicon. The silicides have several advantages over the refractory metals because of their superior thermal oxidation characteristics and ability to withstand chemicals normally encountered during the fabrication process. Table I gives a comparison of the properties of various materials which can be used for this application. A big variation of resistivity is available in this case, e.g., the resistivities of heavily doped polysilicon and aluminum are 5×10^{-4} and 2.25×10^{-6} ohm/cm, respectively. Obviously the proper choice of the material within the constraints placed by the fabrication technology, as shown in Table I, can result in minimization of the delay time.

Our proposal is to use a combination of metals, silicides and polysilicon to develop a multilayer interconnection technology. In our initial work, the

effect of increase in chip area and decrease in the minimum feature size on the performance of the circuit has been investigated. A theory of Scaling of Interconnections has been developed. From the information available in the literature, empirical equations have been developed to predict the various elements of the technology, i.e., minimum feature size, maximum chip area, maximum interconnection length, etc., at a given point in time. Time delays associated with interconnections made of different materials have been calculated. Utilizing the theory of scaling of interconnections and scaling of MOS transistors the delay times associated with interconnections and devices have been compared.

From this analysis it is shown that polysilicon can severely deteriorate the circuit performance. In future technologies a combination of metals and silicides will have to be used in a multilayer interconnection technology.

Table I

<u>MATERIALS</u>		<u>THIN FILM RESISTIVITY OHM/CM</u>	<u>MELTING POINT (°C)</u>	<u>CHEMICAL COMPATIBILITY</u>	<u>THERMAL OXIDATION</u>
Metals	Poly-Si	5×10^{-4}	1410	YES	YES
	{ Al	2.2×10^{-6}	660	NO	NO
	{ W	5.5×10^{-6}	3410	NO	NO
	{ Mo	5×10^{-6}	2610	NO	NO
Silicides	{ WSi ₂	3×10^{-5}	2165	YES	YES
	{ MoSi ₂	4×10^{-5}	2050	YES	YES
	{ TaSi ₂	3.5×10^{-5}	2170	YES	YES
	{ TiSi ₂	1.5×10^{-5}	1540	NO	YES

ELECTRON BEAM LITHOGRAPHY

1/1/81 to 6/30/81

MEBES

1/1/81 - 6/30/81

ELECTRON BEAM PATTERN GENERATION

In early January, factory acceptance tests for our MEBES #29 were started. These included both ETEC and Stanford test patterns and the multi project chip levels on both masks and 75 mm wafers. These tests were successfully completed by the end of February 1981. In the direct write mode the demonstrated registration accuracy was within the 3-sigma limit of 0.25 micrometer.

Detailed technical specifications for the joint Stanford - ETEC direct write development contract were agreed upon in April. These include the installation of a LaB₆ gun with 1/8 μ spot size, improved direct write software and hardware, and improved machine specifications to go with the 1/8 μ capability. The actual retrofits will be after the machine is delivered to Stanford. Factory training in the machine operation, hardware, and software was also carried out in April.

We are working on the design and implementation of a multi-level resist structure for E-Beam direct writing. The multi-level structure includes a thick resist on the wafer to planarize its surface and a thin E-Beam resist on top for high resolution. The pattern written and developed in the E-Beam resist has to then be transferred to the underlying thick resist for processing.

We have arrived on specific layouts for the E-Beam facility. Talks have been going on with subcontractors and ETEC to see what actually can be done.

This installation of the system is presently being delayed both because of the construction in the Stanford IC Lab and because the site for MEBES, which is within the IC Lab but has separate air handling, is not ready.

Outline Requirements for Stanford Electron Beam Pattern Generator

This instrument must be capable of

(1) Routine generation of Cr-on-glass, 4" x 4" reticles with 1 μm address structure at a rate of 1 (or more) per hour.

(2) Routine generation of Cr-on-glass, 4 cm x 4 cm reticles with 0.5 μm address structure. Time per mask to be 1 hour or less.

(3) Routine generation of 4" x 4", chromium-on-glass 1:1 masks with 0.25 μm address size at a rate of 0.5 $\text{cm}^2 \text{ min}^{-1}$. Writing beam diameter (defined as that diameter whose circle contains 75% of the total beam current) to be 0.25 μm or less. Butting errors to be 0.15 μm or less (3-sigma value on a population of sites across each of several masks).

Linewidth control to be 0.15 μm (3-sigma chosen in the same way).

Defect density (on defects 0.5 μm diameter or larger) 1 cm^{-2} .

Die size to be 10 x 10 mm^2 (or smaller).

(4) Direct Writing Capability on 3" and 4" diameter silicon wafers:

20 MHz (or more) stepping rate

Address and beam diameter down to 0.125 μm

Current at 0.125 μm diameter and 20 kV: 5nA or more

Butting error to be $\leq 0.1 \mu\text{m}$ (3-sigma)

Registration error to be $\leq 0.1 \mu\text{m}$ (3-sigma between any 2 levels of a NMOS SIC)

Linewidth control to be $\leq 0.1 \mu\text{m}$ on isolated features exposed in 0.25 μm thick positive photoresist (or equivalent resist).

Some form of exploiting a low density of exposed area (e.g., by vector scanning or by modifying a uniform raster scanning rate) is desirable.

Eventual provision for some form of correction for proximity effects is

also desirable.

(5) Measuring in-plane distortion of Si wafers, X-ray masks and other substrates to an absolute spatial accuracy of 0.1 μm .

Specific acceptance tests are to be drawn up jointly as part of a contract for purchase of such an instrument.

Stanford MEBES (#29)

Test Pattern Plate - System Integration Complete

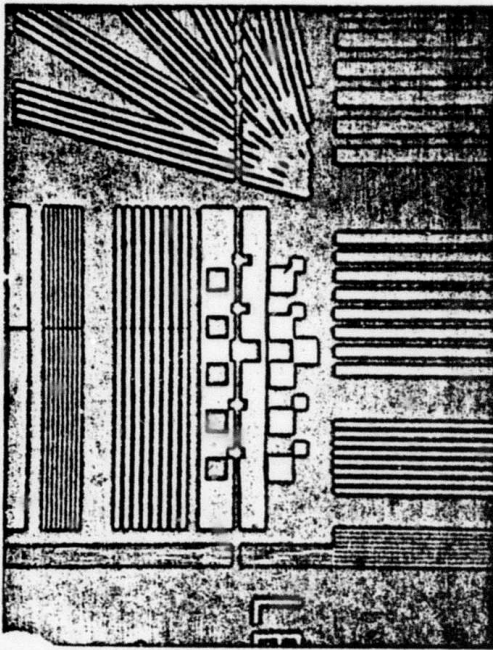
11/24/80	.5 and .25 micron spot size processed	PBS L/E
11/24/80	.5 and .125 micron spot size written processed	11/25/80

Stanford SIC Plate

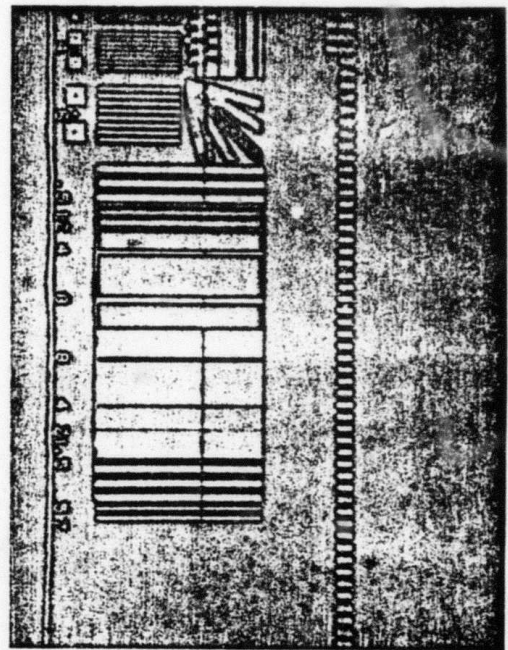
1. - PBS - Test grade, developed 25 seconds.
 - Six levels of 1/2 um, four levels of 1/8 um Bell patterns. Level numbers are contained within each pattern. 1-6 1/2
2-5 1/8
 - 1/2 um patterns are written at 40 nA.
 - 1/8 um patterns are written at 1.4 nA, levels 4 and 5 are double exposed.
2. Observed defects: (ETEC)
 - Y DAC is failing to track errors below 1/4 um causing sinusoid along write scan boundary.
 - Intermittent X data displacement. Likely cause is 16 um error bit being gated on at Stage Interface.
 - Butting error due to deflection system not being aligned.
 - 1/8 um levels 4 and 5 double exposures do not coincide due to failure to register between exposures.

Comments (Stanford)

1. Some extra and missing features, mostly y lines, some x lines.
 - missing or extra intermittent bits exposed.
2. 1/8 micron patterns marked as "0.25 um"
3. Zig-zag edges of alternate ends of lines in grid.
4. Offset in Y up to 4 microns - in butting errors
In one case there was a tilt along a Y fault.
5. Plate over-developed.



0.5 micron



0.125 micron

→ 20 addresses

6 PBS lifted from plate in region between patterns?

FTAF WAFER TESTING

1/1/81 to 6/30/81

FTAF Testing Accomplishments 1/1/81 - 6/30/81

- 1) First version of ICTEST language is implemented for the LSI II based and minimal testers and runs on the VAX. It is now interfaced to logic simulation software.
- 2) Several circuits have been tested on the S3260 to increase understanding of and familiarity with the machine. These included parametric and performance tests on both TTL and NMOS logic. Process performance parameters were determined.
- 3) Work has begun on conversion of the S3260 software to run under the UNIX operating system. Only ~5% has been done. Selected test subroutines have been converted for evaluation purposes and automatic conversion software developed.
- 4) Measured process performance parameters on several runs from IC Lab to support process development of NMOS.

Next Year

- 1) Complete S3260 conversion to UNIX.
- 2) Link S3260 with ICTEST on VAX for unified testing.
- 3) Will design new test patterns for process development.
- 4) Will design new test patterns for yield measurement of the NMOS process steps.
- 5) Will interface automatic wafer prober to S3260 for automatic wafer tests for process and die yield.

VLSI DEVICE RESEARCH

1/1/81 to 6/30/81

FTAF

James R. Pfiester

An investigation to determine optimum threshold voltages and the minimum power supply voltage for an enhancement-depletion load inverter has been initiated. The depletion threshold is determined by speed-power considerations while the enhancement thresholds are set by noise margins. The minimum power supply voltage is dictated by dynamic leakage due to subthreshold conduction. Assuming large geometry and room temperature conditions, optimal parameters are determined as a function of the body effect coefficient. This technique is generalized such that a class of circuits may be analyzed for specific leakage and noise margin specifications. The establishment of the large geometry parameters is essential for scaling limits for VLSI as these parameters become modified for small geometry and temperature effects.

Devices and Circuits in Laser Re-crystallized Polycrystalline Silicon

Harinder Singh

0. This work has been done in active and close collaboration with Dr. Dirk Bartelink of the Xerox Palo Alto Research Center. It covers the preparation of device quality laser-recrystallized (LR) polysilicon, studies of the integrity of the oxides thermally grown on the LR poly, and the fabrication of devices/circuits in the LR poly.

1. Polysilicon has been recrystallized on two types of substrates: i) on oxidized bulk single-crystal silicon wafers, and ii) on quartz substrates. This was done with a CW Argon laser (at PARC) and is facilitated by using a thin nitride encapsulation on the poly. Quartz substrates are found to crack during the laser operation, probably due to thermal stresses as the molten poly re-crystallizes. This creates cracks in the poly film and renders it unusable for device fabrication. One approach around this problem is to use thin stripes or islands of poly on the quartz so as to relieve the stress. This problem has been addressed by co-workers at PARC. The poly on oxidized bulk wafers does not suffer from this problem and is therefore more directly suitable for device fabrication. It has grain sizes on the order of 5 to 10 microns and appears to be an adequate vehicle for studies of device characteristics in large grain polysilicon.

2. Leakage currents and breakdown voltages are of concern when we use thermal oxides of LR poly as gate dielectrics or as insulators in multilevel polysilicon structures for VLSI. The presence of asperities on the surface of a poly film is central to this issue, and their reduction by LR is the objective. Our experiments indicate breakdown field strength of 2-5 MV/cm,

which is encouraging even though it is an order of magnitude below the value for single-crystal silicon. Leakage currents on LR poly are 3-4 orders of magnitude lower than on un-LR poly, suggesting that the LR has helped reduce the magnitude of the asperities in the starting material. Asperity reduction/accentuation is sensitive to the regime, duration and temperature of oxidation, in addition to the conditions for LR, and is likely to stay as a concern for some time.

3. (a) P-type boron doped LR poly was used for all the fabrication, and the devices made were capacitors, n-channel enhancement transistors and p-channel "deep-depletion" transistors. The devices are all currently under investigation. The operation of enh/enh n-channel inverters has been verified. The capacitors are expected to yield information about both the interfaces of the poly layer, back-gate bias effects, and effective free-carrier densities/lifetimes for comparison with single-crystal material. The capacitors also give data about the gate dielectrics. The n-channel enhancement transistors and the inverters have been made by a simplified NMOS process to establish basic compatability with the standard NMOS processes. The "deep-depletion" transistors have been made with a very simple 2-level process and are basically just TFTs; the literature on SOS and compound semiconductors has historically dubbed them as "deep-depletion" devices. They use the bulk of the thin film poly as the channel, and are thus different from depletion transistors as made in conventional silicon technology.

(b) We have made these deep-depletion transistors without the use of implanted or diffused junctions for the source or the drain. The gate-oxidation is followed directly by contact lithography (mask level 1) and metal evaporation. The second level defines the metal, and we find fairly good depletion transistor characteristics. The aluminum serves to make the

S/D contacts and "junctions" to the p-type poly, so in the conventional sense this is a junction-less process. It yields very quick turn-around for studies of conduction properties of large-grain poly, and we have not observed any adverse effects of omitting a p^+ diffusion plug under the contacts; however, an investigation could be carried out to look for them. A further advantage of these junction-less depletion transistors is their promise of simple load devices for an NMOS process, and simple CMOS thin-film processing with little more trouble than NMOS.

BURIED-CHANNEL MOSFETs

(Thao Nguyen)

During the past six months, activities on the device research of small-geometry Buried-Channel MOSFETs (BC-MOSFETs) have been fabrication of both standard surface-channel and buried-channel NMOS test chips with minimum dimension down to $1\frac{1}{4}$ μm and modeling of the threshold voltage of short-channel MOSFETs using analytical techniques as well as two-dimensional numerical analysis.

A test chip has been designed to study the small-geometry effects of both surface and buried channel devices. It includes:

- MOSFETs with various gate lengths to study short channel effects. The dimensions are $W = 20$ μm and $L = 20, 10, 7.5, 5, 4, 3, 2,$ and 1.25 μm . This portion of the test chip is shown in Fig. 1.
- MOSFETs with various channel widths to study the narrow width effect. The dimensions are $L = 20$ μm and $W = 20, 10, 7.5, 4, 3, 2,$ and 1.25 μm . This portion of the test chip is shown in Fig. 2.
- Large and small MOSFETs having dimensions $W = L = 100$ and $W = L = 2.5$ μm to study small-geometry effects.
- Enclosed MOSFETs with $W = 480$ μm and $L = 5$ and 2.5 μm to study the effects of the absence of the channel width.
- Various process structures to evaluate the process parameters such as polysilicon gate capacitors, a diode, sheet resistance structures for source/drain and poly sheet resistance.

This test chip has been fabricated using a modified self-aligned polysilicon gate process with the following patterning steps:

- Device well definition
- Field-implant definition

- Contact-plug definition
- Polysilicon gate definition
- Contact hole definition
- Metal definition

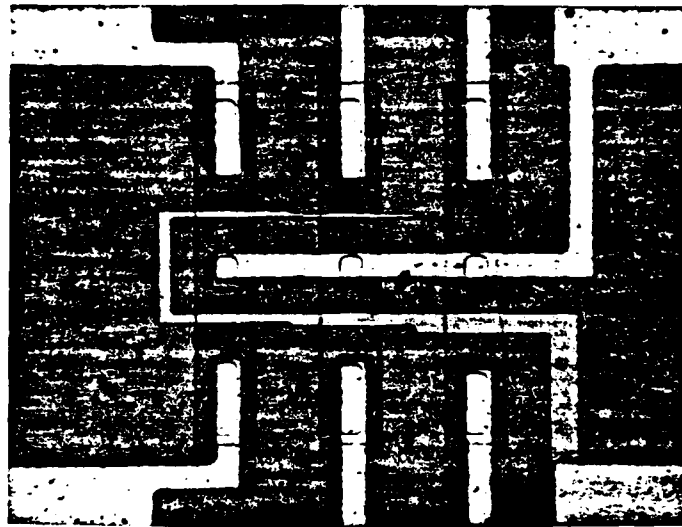
The fabrication process employed in implantation for every doping step and optical projection mask aligning and wet chemical etching for patterning. Preliminary measurements on test devices showed satisfactory results except that the threshold voltage on some BC MOSFET wafers appeared to be slightly negative. Careful characterization of these test devices is currently underway.

The device modeling efforts have been focused on the development of analytical models for threshold voltage shift in small geometry BC MOSFETs. In the past, simple models for the short channel and narrow width effects have been derived based on a concept similar to Yau's charge-sharing model, but they have many limitations and probably insufficient accuracy for small geometry devices. An attempt has been made to develop advanced threshold models that bear physical insight and have reasonable accuracy. Standard surface channel MOSFETs (SC MOSFETs) have been the subject of study thus far because they are simpler and because it is expected that a SC MOSFET model can be extended to BC MOSFETs. Physical insights in small geometry devices have been obtained through extensive use of the GEMINI program. This program is a two-dimensional Poisson solver with very flexible input/output capability and it has proved to be a very useful tool in studying the device physics.

Several analytical models for the threshold voltage of SC MOSFETs have been developed based on different sets of approximations and assumptions, but they all share the same principle features. V_{TH} is linearly dependent

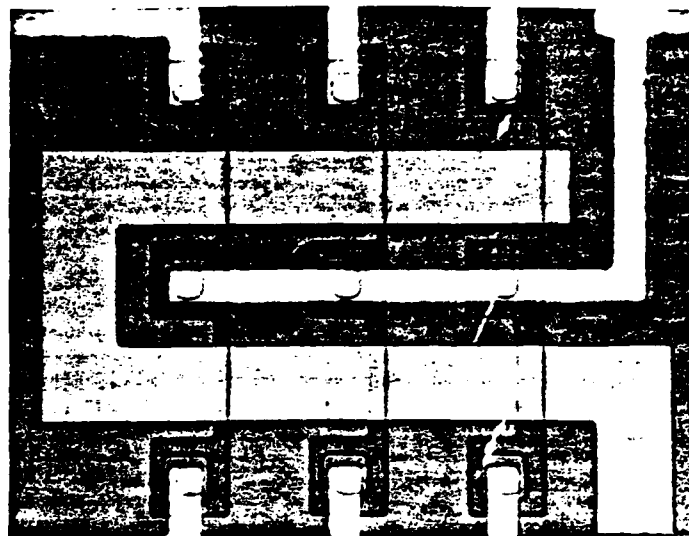
on the drain voltage and inversely proportional to the square of the channel length. The validity of these models is currently under evaluation.

Future work will involve device characterization and modeling of threshold voltage. The test chip will be fully measured to provide an experimental basis for the theoretical study. The activities on modeling will be continued to complete the threshold model for SC MOSFETs and to extend this model to BC MOSFETs. Finally a comparison on small geometry effects of both SC and BC MOSFETs will be made on both theoretical and experimental grounds.



BCMOST LENS 40 x 1.6

Fig. 1. Portion of test chip containing devices with channel lengths down to 1.25μ .



BCMOST LENS 40x2

Fig. 2. Portion of test chip containing devices with channel widths down to 1.25μ .

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MILESTONES - DARPA FTA PROJECT

A. DEPLETED BASE BIPOLAR STRUCTURES (SIT)

<u>To Date</u>	<u>Projected for next year</u>
1. Applied 2D Computer Modeling and Analytic Techniques to develop Physical Understanding of Device Operation.	1. Complete the development of physical models describing device behavior.
2. Developed simple analytic expressions describing I-V characteristics.	2. Evaluate the usefulness of this structure as a process monitoring tool because of its extreme sensitivity to linewidth variations.
3. Experimentally fabricated structures with linewidths of 1-5 μ with increments of 0.25 μ .	3. Compare quantitatively the VLSI potential of conventional bipolar and depleted bipolar devices.
4. Characterized experimental structures and found their behavior to be well modeled by the models developed in (1) and (2).	
5. Found this device to be very sensitive to geometry (linewidth) variations which render it an unlikely candidate for VLSI circuits. This is in contrast to claims which have been made for this device in the literature.	

B. BURIED CHANNEL MOSFETS

<u>To date</u>	<u>Projected for Next year</u>
1. Applied 2D Computer Modeling and analytic techniques to develop physical understanding of small geometry effects in MOS devices.	1. Finish experimental characterization of small geometry surface and buried channel devices.
2. Developed a detailed physical model for the origin of short channel effects on MOS threshold voltage.	2. Extend physical model for the origin of short channel effects in surface channel devices to buried channel structures.
3. Experimentally fabricated surface and buried channel devices with channel lengths and widths from 1-10 μ with increments as small as 0.25 μ .	3. Compare experimentally and theoretically the VLSI potential of surface and buried channel structures.
4. Evaluating these devices at present to understand their electrical characteristics.	