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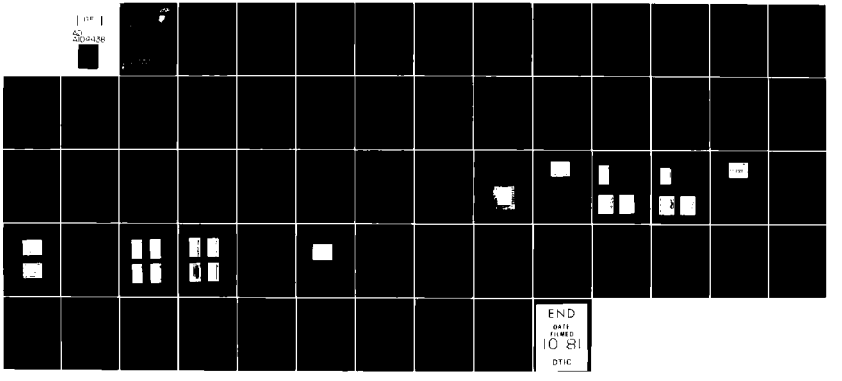

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Final Technical Report
July 1981

BINARY/ANALOG CCD CORRELATOR DEVELOPMENT

Texas Instruments Inc.

R. A. Haken

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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The architecture, design and performance of a general purpose, 1,024-stage, programmable transversal filter implemented in CCD/NMOS technology is described. The device features programmability of the reference signal, the filter length and weighting coefficient resolution. Off-ship circuitry is minimized by incorporating both analog and digital support circuitry, on-chip. This results in a monolithic analog signal processing system that has the flexibility to be operated in nine pro-

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grammable configurations, from 1,024-stages by 1-bit, to 128-stages by 8-bits. The versatility of the device makes it suitable for a wide range of applications, from matched filtering with chirp signals and very long binary sequences, to image correlation and adaptive filtering.

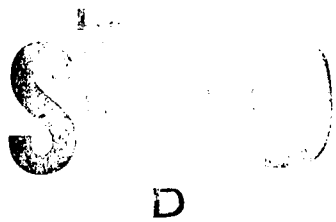


TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

PREFACE

This report was prepared by Texas Instruments Incorporated, Dallas, Texas, under Air Force Contract No. F19628-78-C-0122. The work under this contract was administered and funded by Electronic Systems Division, Air Force Systems Command, Hanscom AFB, MA. Dr. F.D. Shepherd, Jr., of the office of Deputy for Electronic Technology (RADC ESE), Hanscom AFB, MA, was the contract monitor.

At Texas Instruments, the work was performed in the System Components Laboratory under the direction of Dr. L.T. Claiborne, Director of the System Components Laboratory. In addition to the author, personnel who made major contributions to the work include: C.R. Hewes, R.C. Pettengill, L.R. Hite, D. Mayer, W.J. Westfall, J.A. Lott, C. Hoffman and D.M. Doyle.

This is the Final Technical Report for the contract. It was submitted by the author in January 1981.

SECTION I
INTRODUCTION

The charge-transfer transversal filter with split-electrode weighting is well recognized as a useful tool for a number of sampled-data filtering applications.[1-4] However, these devices are limited to dedicated applications since their weighting coefficients are fixed during IC fabrication. For applications that require rapid updating of the weighting coefficients, such as adaptive filtering and matched filtering in spread spectrum communication systems, a device with electronically programmable tap weights is essential.[5-10] Of the present programmable techniques, the most attractive for these types of applications is the binary/analog approach.[7-10]

The objective of this program is to design, fabricate and evaluate a general-purpose, 1,024-stage, electronically programmable binary/analog transversal filter. The device is implemented in CCD/NMOS technology and features programmability of the reference signal, the filter length and weighting coefficient resolution. Off-chip circuitry is minimized by incorporating both analog and digital support circuitry, such as clock logic, drivers, amplifiers and microprocessor interface circuitry, on-chip. This results in a monolithic analog signal processing system that has the flexibility to be operated in nine programmable configurations, from 1,024-stages by 1-bit, to 128-stages by 8-bits. The versatility of the device makes it suitable for a wide range of applications, from matched filtering with chirp signals and long binary sequences, to image correlation and programmable filtering.

Section I of this report describes the operation of the binary/analog transveral filter and the architecture required to realize a general-purpose device. Section II contains a technical discussion of the key circuits for implementing the programmable filter. In Section III, the performance characteristics of the device are discussed. The report concludes with a summary and discussion in Section IV.

[1] D.D. Buss, D.R. Collins, W.H. Bailey and C.R. Reeves, "Transversal Filtering Using Charge-Transfer Devices," *IEEE J. Solid State Circuits*, Vol. **SC-8** (April 1973), pp. 138—146.

[2] R.D. Baertsch, W.E. Engeler, H.S. Goldberg, C.M. Puckette and J.J. Tiemann, "The Design and Operation of Practical Charge-Transfer Transversal Filters," *IEEE J. Solid-State Circuits*, Vol. **SC-11** (February 1976), pp. 65—74.

[3] R.W. Brodersen, C.R. Hewes and D.D. Buss, "A 500-Stage CCD Transversal Filter for Spectral Analysis," *IEEE J. Solid State Circuits*, Vol. **SC-11** (1976), p. 75.

[4] C.R. Hewes, R.W. Brodersen and D.D. Buss, "Applications of CCD and Switched Capacitor Filter Technology," *Proc. IEEE*, Vol. **67** (October 1979), pp. 1403—1415.

[5] P. Bosshart, "An Integrated Analog Correlator Using Charge-Coupled Devices," *Proc. IEEE ISSCC* (1976), pp. 198—199.

[6] P.B. Denyer, J. Mavor and J.W. Arthur, "Miniature Programmable Transversal Filter Using CCD MOS Technology," *Proc. IEE*, Vol. **67** (December 1979), pp. 42—50.

[7] J.J. Tiemann, W.E. Engeler, R.D. Baertsch, "A Surface-Charge Correlator," *IEEE J. Solid-State Circuits*, Vol. **SC-9** (December 1974), pp. 403—409.

[8] D.V. Gandolfo, J.R. Tower, J.J. Pridgen and S.C. Munroe, "Analog-Binary CCD Correlator: A VLSI Signal Processor," *IEEE J. Solid State Circuits*, Vol. **SC-14** (April 1979), pp. 518—525.

[9] J.G. Magill, D.M. Grieco, R.H. Dyck and P.C.Y. Chen, "Charge-Coupled Device Pseudo-Noise Matched Filter Design," *Proc. IEE*, Vol. **67** (January 1979), pp. 50—60.

[10] V.M. Chiang, B.E. Burke, D.E. Smythe, D.J. Silversmith and R.W. Mountain, "A High Speed CCD Digitally Programmable Transversal Filter," *Proc. Int. Conf. on CCD Applications*, CCD 1979 (Edinburgh, Scotland), pp. 230—238.

A. BINARY/ANALOG TRANSVERSAL FILTER OPERATION

Electronic programmability is achieved in the binary/analog approach by decomposing each one of the weighting coefficients into a binary representation that can be loaded into a static shift register, as illustrated in Figure 1. For M-bit accuracy of each weighting coefficient, M parallel CCD binary/analog filters are required, so that h_n is represented with M-bit accuracy by:

$$h_n = \sum_{k=0}^{M-1} h_n^k \, 2^{-k} \tag{1}$$

The most significant bit h_n^0 of each weighting coefficient is loaded into the static shift register, shown as elongated rectangles in the filter at the top of the figure. The second most significant bit h_n^1 of each coefficient is loaded into the second coefficient store, and the least significant bit, h^{M-1}, is loaded into the coefficient store shown at the bottom of the figure. The analog signal must be weighted by the appropriate factor of 2^{-n-1} at either the input or output of each filter. In Figure 1, the weighting is performed at the input to the filters, with the analog signal applied without attenuation to the top filter (most significant bit) and attenuated by a factor of two at the input of the second filter (second most significant bit). At the input to the bottom filter (least significant bit), it is attenuated by a factor of 2^{M-1}.

The choice of whether input or output signal weighting is employed, or a mixture of both, depends on the application. Input signal weighting is simpler to implement because capacitor ratio techniques can be used, whereas output weighting requires amplifiers with accurately controlled gain. However, output signal weighting is desirable in some applications because of a dynamic range limitation associated with the input weighting configuration. For a general-purpose filter it is desirable to perform a mixture of both input and output weighting to strike a balance between dynamic range, the number of integrators required, and logic simplicity. A more detailed discussion of output versus input signal weighting appears in Appendix A.

The total weighting coefficient for any one of the M parallel CCD bits is determined by the sum of the coefficients in the M parallel static shift register bits. Consequently, when the outputs of each filter are summed together as shown in Figure 1, the result is:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \sum_{n=1}^{N} h_n^0 \, z^{-n} + 2^{-1} \sum_{n=1}^{N} h_n^1 \, z^{-n} + \ldots + 2^{-(M-1)} \sum_{n=1}^{N} h_n^{M-1} \, z^{-n} \tag{2}$$

$$= \sum_{n=1}^{N} \left[\sum_{k=0}^{M-1} (h_n^k \, 2^{-k}) \right] z^{-n} \tag{3}$$

$$= \sum_{n=1}^{N} h_n \, z^{-n} \tag{4}$$

Programmability of the CCD weighting coefficients is achieved by using the coefficient code in the static shift register to determine the relative timing of charge transfer in a four-phase CCD register. This is described in detail in Subsection II.C. In essence, the coefficient code in each of the static shift register cells determines when the charge in the corresponding CCD bit transfers to the electrode that is connected to the integrator. If the charge is transferred early, the charge packet is sampled underneath the sense electrode and contributes to the integrator output during that cycle. If the charge is transferred late, after the

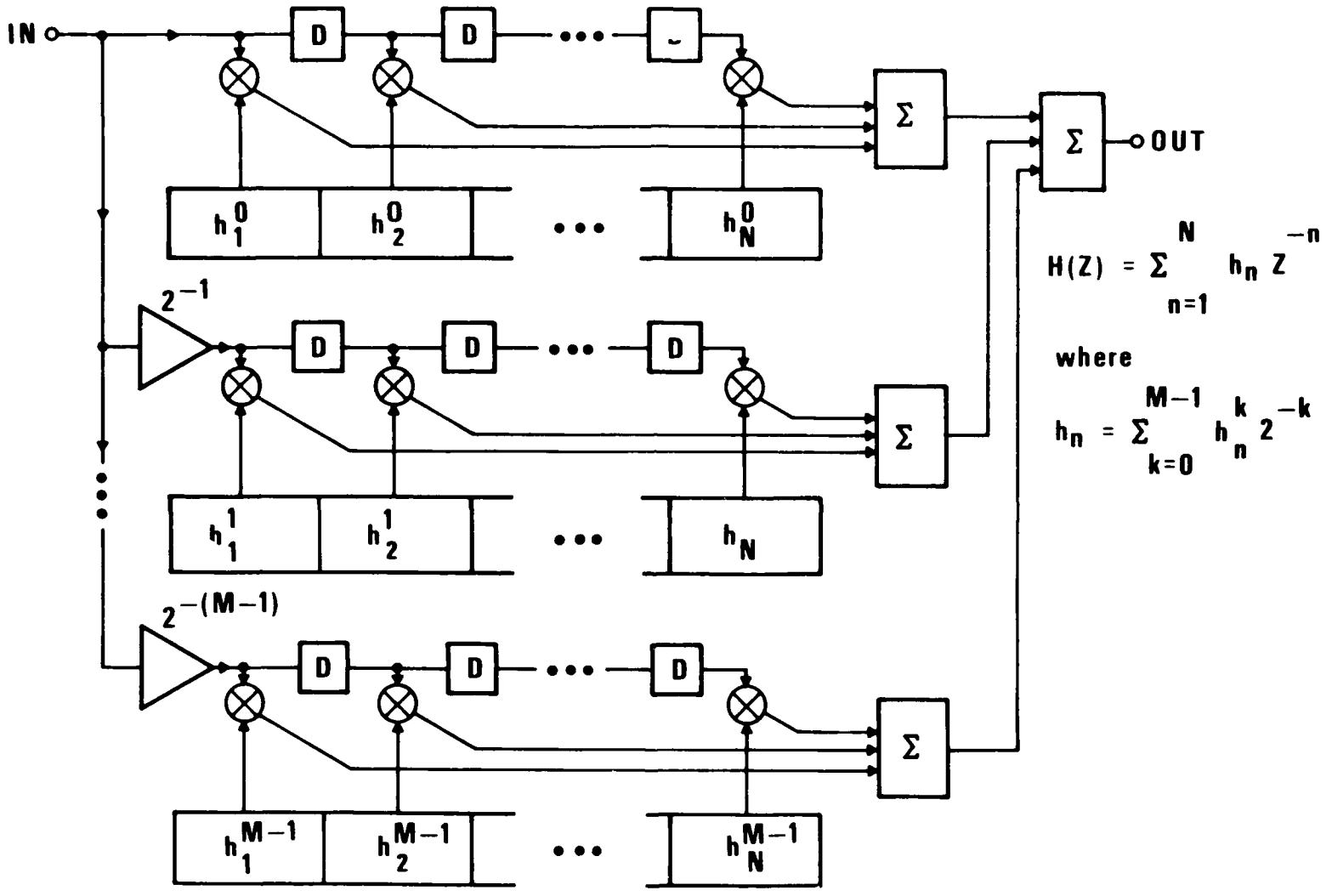


Figure 1. Block Diagram of the Binary/Analog Transversal Filter

integrator sampling period has finished, the charge does not contribute to the output. During the sampling period, the output signal is given by

$$Q_{out}(n) = \sum_{i=1}^{N} h_i Q_{SE}(n-i) \tag{5}$$

As described thus far, the device can only handle unipolar signals. For a signal of either sign to be used, it must be added to a fat zero, which also improves the charge transfer efficiency. The actual CCD input is then $Q_{sig} + Q_{fz}$ and the output from a single binary/analog filter is given by:

$$Q_{out}(n) = \sum_{i=1}^{N} h_i Q_{fz}(n-i) + h_i Q_{SE}(n-i) \tag{6}$$

The first term represents a code dependent offset and must be eliminated. The second term is the desired signal. To eliminate the first term, a parallel filter must be added in which the input signal is inverted, i.e., the input to the second CCD becomes $Q_{fz} - Q_{sig}$. The output of the parallel filter is then given by:

$$Q_{out}(n) = \sum_{i=1}^{N} h_i Q_{fz}(n-i) - h_i Q_{SE}(n-i) \tag{7}$$

When the two CCD outputs are connected to a differential current integrator (DCI), the undersired terms cancel, resulting in the DCI output being given by:

$$Q_{out}(n) = \sum_{i=1}^{N} 2h_i Q_{sig}(n-i) \tag{8}$$

The elimination of code dependent offset is a primary requirement of any programmable filter. The effect manifests itself as a change in the output dc level with filter code, and can drastically reduce the dynamic range of the device unless the offset is manually compensated. In the approach described here, the offset is only contributed to by variations between the sizes of the fat zeros and sampling electrodes in the adjacent +ve and -ve CCD channels. The use of plasma etching can restrict these local variations to less than 1 percent, resulting in worst case offsets of <100 mV (see Subsection III.C). Furthermore, because multiplication of the signal by the weighting coefficients occurs in the CCD, there is no fixed pattern noise resulting from transistor multiplier threshold variations.

The salient features of the binary/analog approach to programmable correlators are:

One-bit programmable filters in which h_n can be 1 or 0.

Capability to expand to M-bit accuracy by combining M binary/analog correlators in parallel with the appropriate gain.

Capability to program the filters to the desired length (N = 32, 64, 138, etc.) and to cascade filters to achieve longer filters.

Weighting coefficient accuracy sufficient to give 8-bit resolution of weighting coefficients (i.e., weighting coefficient accuracy of 0.2 percent, $\frac{1}{2}$ LSB).

Minimization of off-chip circuitry. All clock drivers, amplifiers, static shift registers, etc., can be on-chip.

Capability to use a microprocessor to read data out of memory into the code registers.

Elimination of the code-dependent output dc level problem. A code-independent dc level is essential for spread spectrum and ECM applications.

B. ARCHITECTURE OF THE GENERAL-PURPOSE TRANSVERSAL FILTER

The architecture of the general-purpose electronically programmable 1,024-stage binary analog transversal filter is shown in the simplified block diagram of Figure 2. The architecture is arranged so that the 1,024-stage device is folded into eight 128-stage sections with the output of each section fed by a unity gain amplifier to the input of the next 128-stage device. This provides a convenient point to insert an alternative input signal, together with the necessary logic for selecting the filter configuration desired.

To achieve multiple-bit accuracy, some of the signal weighting is performed at the input and some at the output. The rectangles labeled X1 and $X^1/_2$ indicate that the input signal is passed with unity gain and with 50-percent attenuation. The input selection switches to the filters determine whether the attenuated or unattenuated signal is applied to the filter input. The remainder of the signal weighting is performed at the output of the filters.

The convolution outputs of the filters (output at the top of each filter) go to the differential current integrators and summing amplifiers labeled Σ. By summing the outputs in pairs, the number of DCI amplifiers required is only four; the DCI outputs are summed through two switched, weighted summation stages that determine the mode of operation.

The flexibility of the architecture chosen to realize the general-purpose transversal filter chip is illustrated by the nine possible operating configurations described below and summarized in Table 1.

1. Single Mode

[illegible] B_{IT}

In this mode, the input is applied to $V^{in}(1)$, and the output is taken from $V^{out}(7)$. The inputs to each filter are switched to the lower position so that the serial output from the preceding filter is applied to the input. The switches on the outputs all select the unity gain amplifiers.

[illegible] B_{ITS}

In this mode of operation, the input is applied to $V^{in}(1)$, and the output is taken from $V^{out}(7)$. The X1 input is applied to filter 1, and $X^1/_2$ input is applied to filter 2. The inputs of all other filters are switched to the central position such that the unattenuated (X1) signal passes from filter 1 to filter 3 to filter 5 to filter 7, and the attenuated ($X^1/_2$) signal passes from filter 2 to filter 4 to filter 6 to filter 8. The output amplifiers are all switched to the unity gain setting and summed to provide the output at $V^{out}(7)$.

[illegible] B_{ITS}

Only the 4-bit and 8-bit modes use output amplifier settings at other than unity gain. The connections for this mode of operation are illustrated in Figure 2. The same input is applied to both $V^{in}(1)$ and $V^{in}(3)$. The top four filters perform a 256-stage by 2-bit convolution with the most significant bit (MSB) and the second significant bit (2SB), and the bottom four filters perform a 256-stage by 2-bit convolution with the third significant bit (3SB) and the least significant bit (LSB). The outputs $V^{out}(5)$ and $V^{out}(6)$ are then summed together with $V^{out}(6)$ being summed through the $X^1/_4$ amplifier to provide the 4-bit weighted output at $V^{out}(7)$.

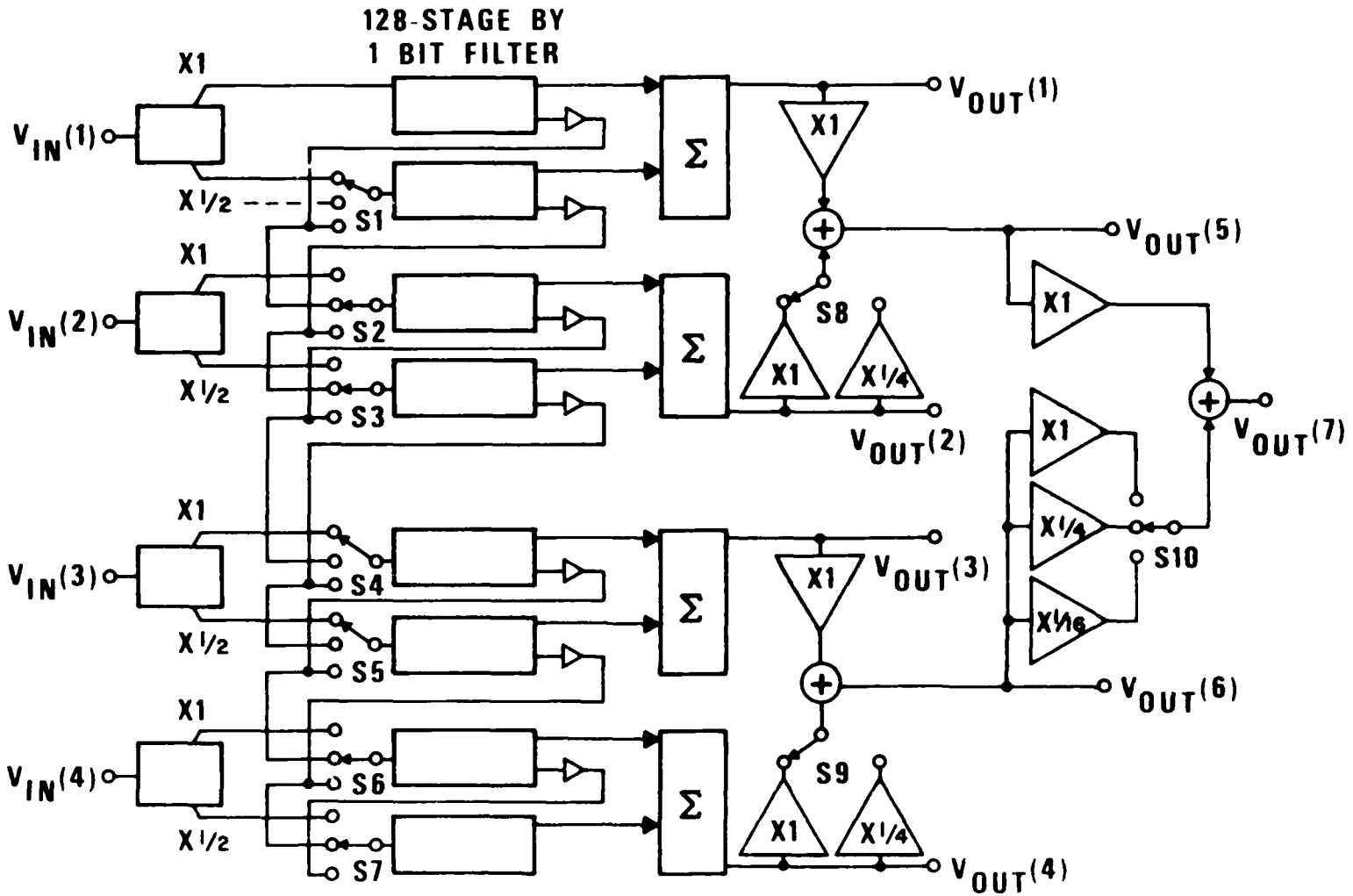


Figure 2. Analog Signal Flowgraph of the 1,024-Stage Binary Analog Transversal Filter (Shown connected as a 256-stage by 4-bit filter.)

TABLE I. FILTER CONFIGURATIONS AVAILABLE WITH THE 1,024-STAGE GENERAL-PURPOSE PROGRAMMABLE TRANSVERSAL FILTER

Filter Configuration	Weighting Coefficients	Number of Filters/Device	Mode Code A	B	C	D
1,024-stage by 1 bit	+1, 0	1	1	0	0	0
512-stage by 2 bits	+1, 0, −1, −2	1	0	1	0	0
256-stage by 4 bits	+7 to −8	1	1	1	0	0
128-stage by 8 bits	+127 to −128	1	0	0	1	0
512-stage by 1 bit	+1, 0	2	1	0	1	0
256-stage by 2 bits	+1, 0, −1, −2	2	0	1	1	0
128-stage by 4 bits	+7 to −8	2	1	1	1	0
256-stage by 1 bit	+1, 0	4	0	0	0	1
128-stage by 2 bits	+1, 0, −1, −2	4	1	0	0	1

d. 128-Stage by 8 Bits

In this mode of operation, the input is applied simultaneously to $V^{in}(1)$, $V^{in}(2)$, $V^{in}(3)$, and $V^{in}(4)$. The top four filters perform a 128-stage by 4-bit convolution with the MSB, 2SB, 3SB, and 4SB; the bottom four filters perform a 128-stage by 4-bit convolution with the 5SB, 6SB, 7SB, and LSB. The output $V^{out}(6)$ is then summed through the $X^1/_{16}$ amplifier, together with $V^{out}(5)$, to provide the 8-bit convolution at $V^{out}(7)$.

2. Dual Mode

a. 512-Stage by 1 Bit

In this mode, the two inputs are applied to $V^{in}(1)$ and $V^{in}(3)$, and the outputs are taken from $V^{out}(5)$ and $V^{out}(6)$. Operation is similar to the 1,024-stage by 1 bit, except that the switch at the input to the fifth filter is in the upper position so that $V^{in}(3)$ is applied to the input. The outputs $V^{out}(5)$ and $V^{out}(6)$ are taken separately instead of being summed to give $V^{out}(7)$.

b. 256-Stage by 2 Bits

In this mode, operation is similar to the 512-stage by 2-bit mode, except that inputs are made at $V^{in}(1)$ and $V^{in}(3)$, and outputs are taken at $V^{out}(5)$ and $V^{out}(6)$.

c. 128-Stage by 4 Bits

In this mode of operation, the top four filters perform one 128-stage by 4-bit convolution and the bottom four perform another. Input 1 is applied simultaneously to $V^{in}(1)$ and $V^{in}(2)$, and input 2 is applied simultaneously to $V^{in}(3)$ and $V^{in}(4)$. $V^{out}(2)$ and $V^{out}(4)$ are summed through the $X^1/_4$ amplifier to $V^{out}(1)$ and $V^{out}(3)$ to provide the two outputs at $V^{out}(5)$ and $V^{out}(6)$.

3. Quad Mode

a. 256-Stage by 1 Bit

In this mode, the four inputs are applied to $V^{in}(1)$, $V^{in}(2)$, $V^{in}(3)$, and $V^{in}(4)$; and the four outputs are taken at $V^{out}(1)$, $V^{out}(2)$, $V^{out}(3)$, and $V^{out}(4)$. Filters 1, 3, 5, and 7 select the X1 input (upper position); and filters 2, 4, 6, and 8 select the output from the previous filter (lower position).

b. 128-Stage by 2 Bits

In this mode, the pairs of filters operate separately. Inputs are made at $V^{in}(1)$, $V^{in}(2)$, $V^{in}(3)$, and $V^{in}(4)$; outputs are taken at $V^{out}(1)$, $V^{out}(2)$, $V^{out}(3)$, and $V^{out}(4)$.

C. CONSTITUENT CELLS

The architecture of the general-purpose binary/analog transversal filter can be broken down into the following principal on-chip cells.

Sixteen 128-stage four-phase CCDs.

Eight 128-bit static binary shift registers for storing the reference signal.

Switching circuitry for selecting the filter configuration and operating mode: either single, dual or quad

Scaling circuitry for providing the X1, $\overline{X1}$ and $X^1/_2$, $\overline{X^1/_2}$ analog signal inputs.

Fourteen unity gain charge amplifiers (CVAMPs) for linking the output of one 128-stage CCD to the input of the next.

Seven DCIs summing amplifiers.

Microprocessor interface circuitry for loading the reference signal from memory into the static shift registers

Clock generation and drive circuits.

SECTION II

GENERAL-PURPOSE TRANSVERSAL FILTER DESIGN

A. FILTER LENGTH, WEIGHTING COEFFICIENT RESOLUTION AND MODE SELECTION CIRCUITRY

To externally select any one of the nine filter configurations, a 4-bit input word is required that, therefore, necessitates an on-chip 4-bit to nine-line decode circuit. Table I shows the input word required to select any one of the nine filter configurations. The outputs from the decode circuitry are fed to the input and output switches, S1 to S10 in Figure 2. The filter configuration can be selected manually or, for applications that require rapid change, by microprocessor.

In addition to the switching circuitry for selecting the length and weighting coefficient resolution of the filters, input and output mode switches are required to interconnect the various inputs and outputs for the single, dual, and quad modes of operation. This results in four analog input and output lines. On-chip logic is also included to invert the input signal to the MSB whenever a multi-bit resolution filter mode is selected. This enables positive and negative weighting coefficients to be realized when 2's complement arithmetic is used.

B. ANALOG INPUT SIGNAL SCALING AND INVERSION

In the block diagram of Figure 2, the scaling circuitry located ahead of the correlators generates X1 and $X^1/_2$ versions of the input signal. Since each 128-stage by 1-bit filter actually comprises a differential channel, the scaling circuitry must also provide $\overline{X1}$ and $\overline{X^1/_2}$ signals. To match the signal gains to 8 bits, a circuit using a capacitor ratio technique is employed. This circuit, together with the controlling waveforms, is shown in Figure 3.

The continuous time analog input signal is converted to a sampled data signal by the sample-and-hold circuitry of M1 and C1. The holding capacitor is buffered from the load by a unity gain operational amplifier whose output is connected to the inverting and scaling circuitry. The input signal and its complement are generated by the action of the switches M2 to M5. These signals are scaled by the identical capacitors C2 and C3, the scaling ratio being independent of stray capacitance. When the bottom plate of C3 is wired to ground, the signal generated is half that compared with when C2 and C3 are wired in parallel. The gain of the positive and negative channels is closely matched by ensuring symmetrical layout and introducing a large, but equal, stray capacitance. This is accomplished by using the first layer of polysilicon for the top plate of C3 and for the right plate of C2. The source followers act to buffer the capacitance sensitive nodes from the unequal loading of the input lines to the CCDs. A fat zero charge is generated by translating the input signal onto a bias provided by V_{f2}.

C. PROGRAMMABLE WEIGHTING USING A FOUR-PHASE CCD

Programmable weighting is implemented by selectively controlling the time of charge transfer from one well to the next. Figure 4 shows a section of a four-phase CCD, with plots of surface potential at various times during charge transfer, and the driving waveforms. The four-electrode CCD has two clocked electrodes, ϕ_1 and ϕ_2, and a dc biased barrier electrode, ϕ_3, which serves to reduce clock feedthrough from ϕ_2 to the sense electrodes, ϕ_4. The ϕ_4 electrodes are in common on the output summing bus, which is tied to an integrator that maintains it at an intermediate dc bias level.

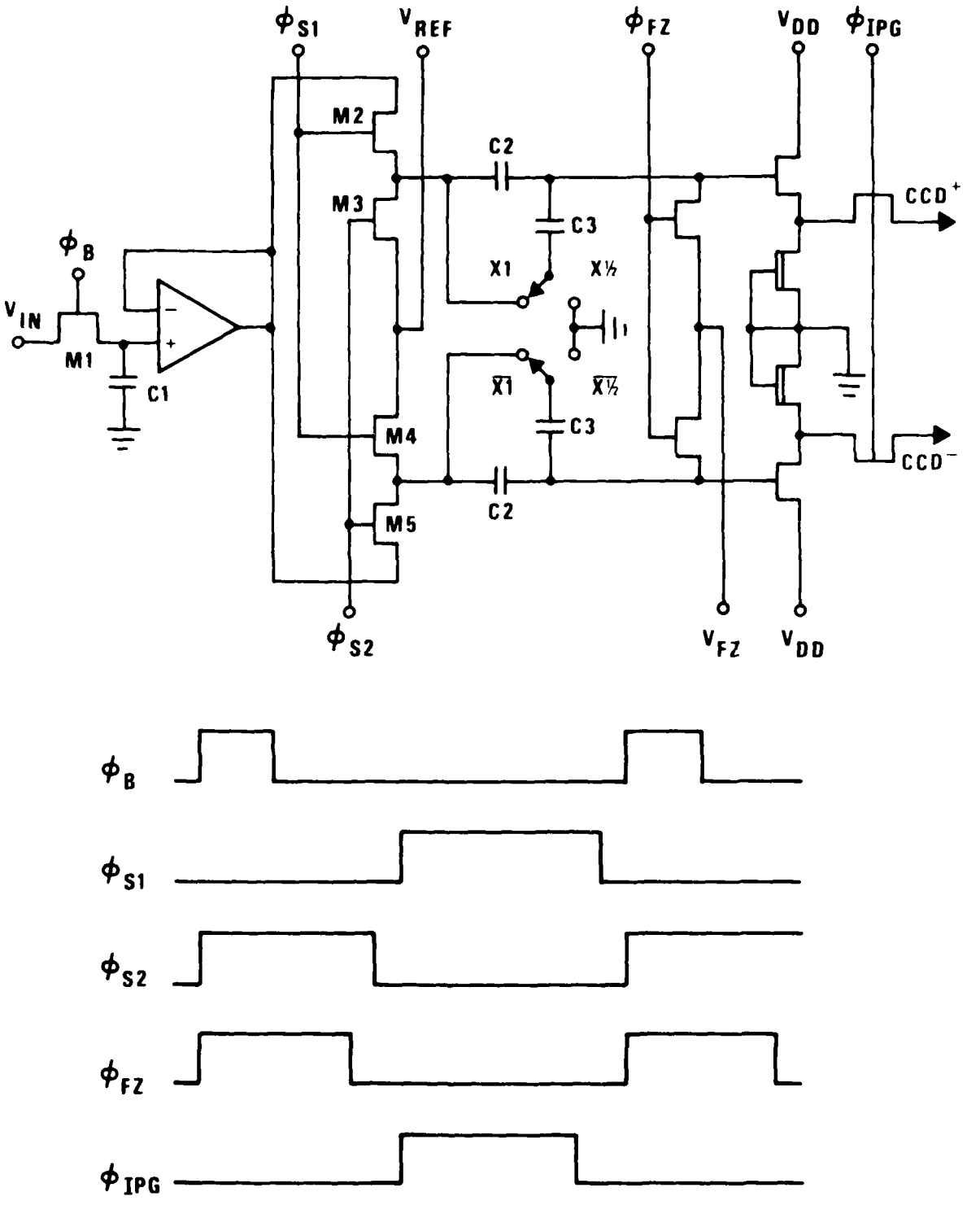


Figure 3. Input Signal Scaling and Inverting Circuitry

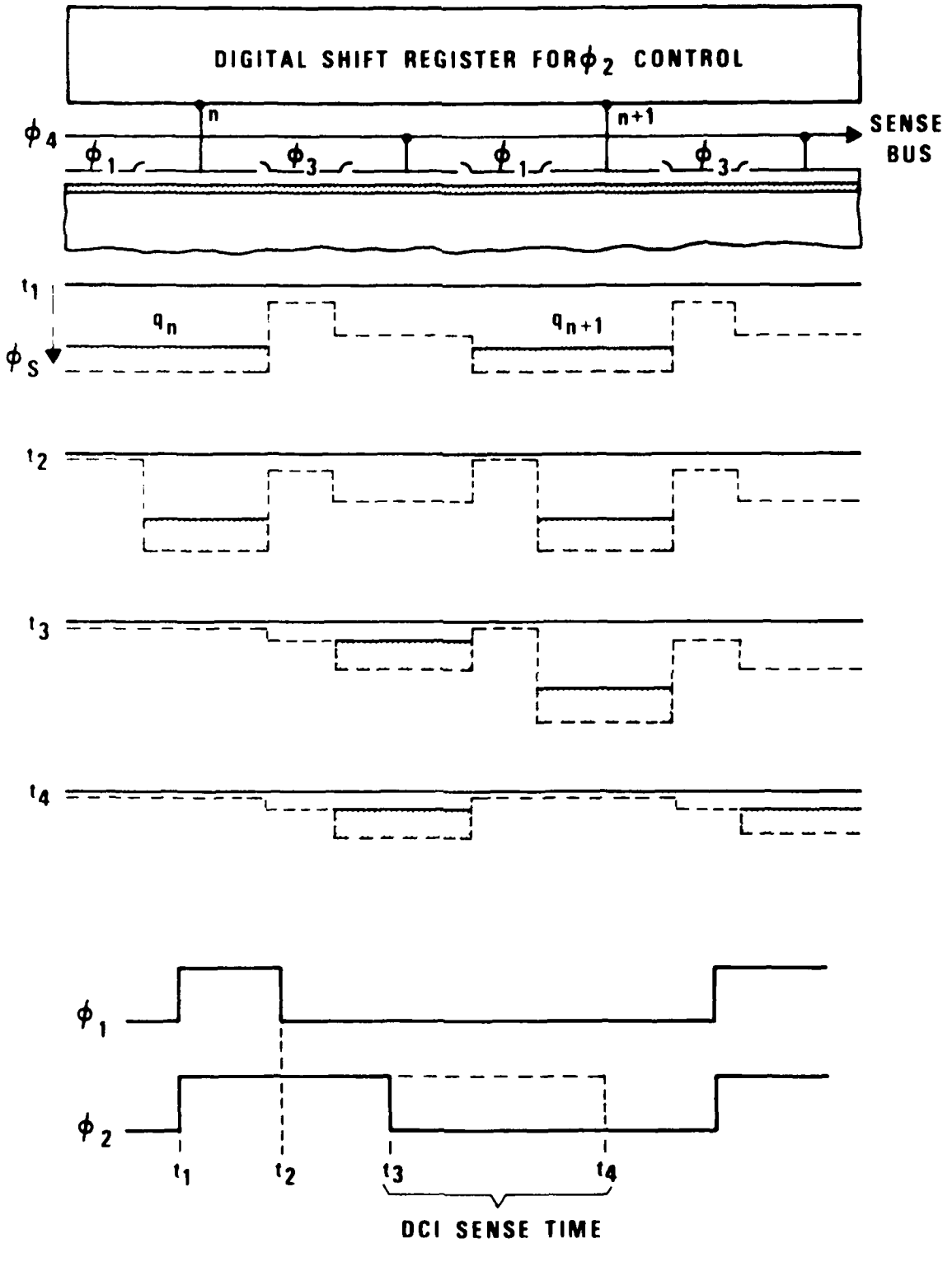


Figure 4. Programmable Weighting Using a Four-Phase CCD

At time t_1, the charge packets are shared between the ϕ_1 and ϕ_2 electrodes. At time t_2, the ϕ_1 clock is turned off, leaving the charge under the ϕ_2 storage and control electrodes. At time t_3, the ϕ_2 electrode corresponding to q_n is turned off, thereby transferring q_n under the sense electrode ϕ_4. Meanwhile, other charge packets such as $q_n + 1$ (depending on the code in the digital shift register) have been left unchanged, as those ϕ_2 electrodes have not been clocked to the off state. At time t_4, the ϕ_2 electrodes that were held on at t_3 are turned off, resulting in all the remaining charge packets being transferred to the ϕ_4 electrodes. The weighting on any one sample in the filter is therefore determined by how many of the M parallel CCD charge packets were transferred to the ϕ_4 sampling electrodes at t_3. If all M parallel bits were transferred at t_3, the weighting coefficient would be 1; if none, the weighting would be zero. Hence, the output of the integrator between t_3 and t_4 is proportional to the sum of the charge packets that were transferred because of the corresponding ϕ_2 electrodes being turned off. The integrator is reset between t_4 and t_1; then the cycle repeats.

The scheme eliminates the requirement for conventional MOS multipliers, as multiplication of the analog signal by the binary weighting coefficients occurs in the CCD. This eliminates a major source of fixed pattern noise associated with other approaches[6,8,9] and should result in improved weighting coefficient resolution. As noted in Section I, each section of the filter has two CCD channels that are operated in parallel, both being controlled by the same digital shift register. The input signal and its complement are applied to the two CCD channels, while the output sense buses (ϕ_4) are differentially summed by the DCI. Thus, the bias charge, or fat zero, does not produce an output from the DCI, and there is no code dependent offset.

D. DIGITAL SHIFT REGISTER AND MICROPROCESSOR INTERFACE

Figure 5 shows the circuit diagram of one stage of the static digital shift register, together with the controlling and output waveforms. The shift register holds the reference signal/code that determines the time of charge transfer from ϕ_2 to ϕ_4 and is operated by three nonoverlapping clocks, ϕ_A, ϕ_B, and ϕ_C. To control whether the shift register is connected serially for loading or whether each bit is continuously recirculated within the same stage in the storage mode, ϕ_B is routed to the gate of either M1 or M8. If a digital 1 is loaded into the shift register stage, a long pulse, ϕ_{2L}, results, so that no sampling occurs under the ϕ_4 electrode in the corresponding CCD cell. If the bit is a 0, a short pulse, ϕ_{2S}, occurs, with the result that the charge packet is sampled.

Operation of the digital shift register can be explained by letting the load/hold control circuitry route the ϕ_B pulse to the gate of M1 and letting the load input go high. When ϕ_B goes on, the input turns M2 on, so that when ϕ_B turns off, the source of M3 discharges to ground through M2. The next event is when ϕ_C goes on; this sets the output of the shift register to zero and, hence, the corresponding CCD ϕ_2 electrode. When ϕ_A goes on, the gate of M5 is connected to the drain of M2 through M4 and is, therefore, set to 0. At the same time, the output of the shift register tracks ϕ_A through M6. When ϕ_A goes off, the shift register output is left floating high because M5 is turned off. Consequently, a long ϕ_2 pulse is generated; only when ϕ_C comes on will the output be reset to 0. Now let the control circuitry route the next ϕ_B pulse to the gate of hold transistor M8. When M8 is clocked, the high output of the shift register is routed to the gate of M2; thus, the previous cycle is repeated, resulting in the generation of another long ϕ_2 pulse.

If the input to M1 had been a 0 rather than a 1, then when ϕ_B went off, the drain of M2 would have been left floating high. Therefore, when ϕ_A went on, the gate of M5 would have been set to 1, resulting in the source of M6 being discharged through M5 when ϕ_A turned off. This would have caused a short ϕ_2 pulse to be generated.

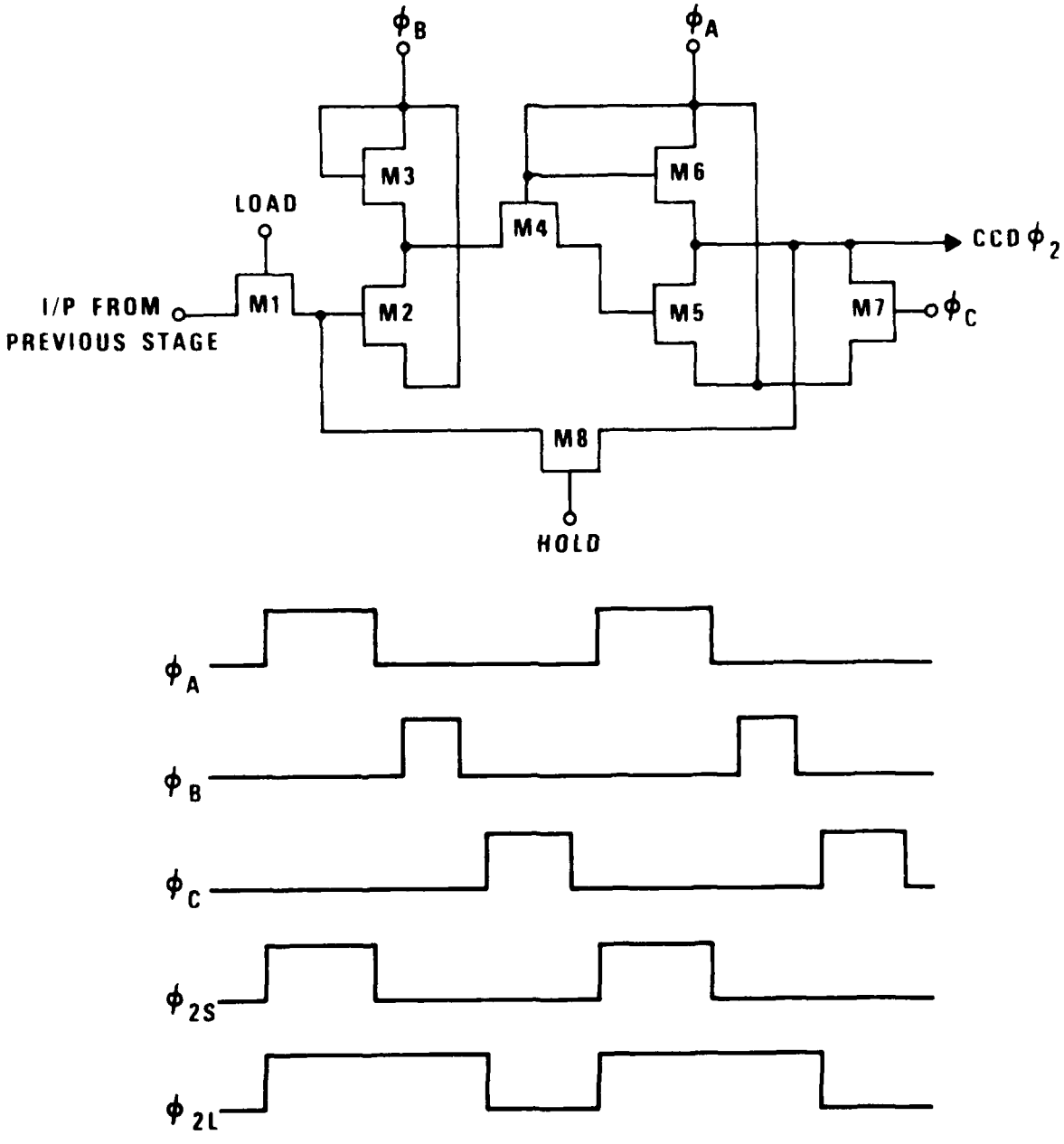


Figure 5. Digital Shift Register Circuit With Controlling and Output Waveforms

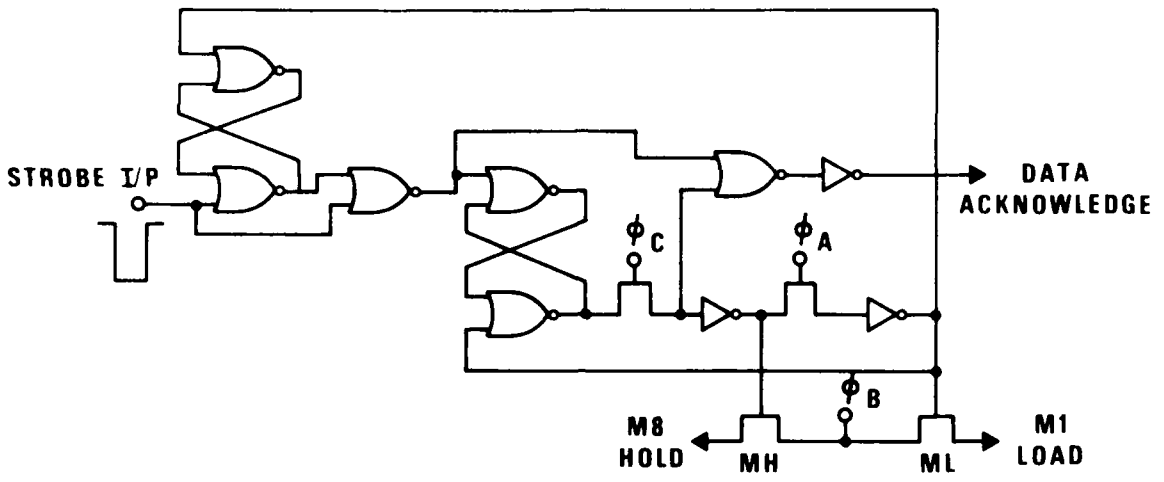


Figure 6. Microprocessor Interface Circuitry

The circuitry of Figure 6 allows microprocessor loading of the shift register by routing the ϕ_B pulse to the load transistors whenever an asynchronous strobe pulse is received from the microprocessor. During clock cycles when no strobe pulses occur, i.e., the microprocessor is not ready to send new tap weight data, the ϕ_B pulse is routed to the hold transistors, thereby recirculating the old data.

E. CHARGE TRANSFER BETWEEN CCD REGISTERS

The architecture of the general-purpose transversal filter requires the output of each 128-stage CCD register to be folded back along its length to the input of the next stage. This constraint requires the output charge of each CCD register to be converted to a voltage by a unity gain charge amplifier. The amplifier output is fed to the input of the following CCD where a voltage-to-charge conversion is performed. This conversion must result in the input charge packet being identical in size to the charge packet transferred to the output of the preceding CCD. An additional constraint is that the transfer of charge between CCDs must take place during one clock period without the loss of a correlation sample. The scheme described in the following subsections meets these requirements.

1. Clocking Scheme

Figures 7a and 7b show the output and input sections of the CCDs with plots of surface potential at various times during the charge transfer cycle. Figure 7c shows the waveforms required to control the transfer of charge between the CCD registers.

At time t_1, all the clocks are off, and the charge packets are located under the sampling electrodes ϕ_4. At time t_2, ϕ_1, ϕ_2, and ϕ_2' are turned on; hence, charge is transferred to ϕ_1 and ϕ_2 or at the output ϕ_1 and ϕ_2'. At t_3, ϕ_1 is turned off, thereby transferring all the charge to ϕ_2 or ϕ_2'. At t_4, the input gate of the

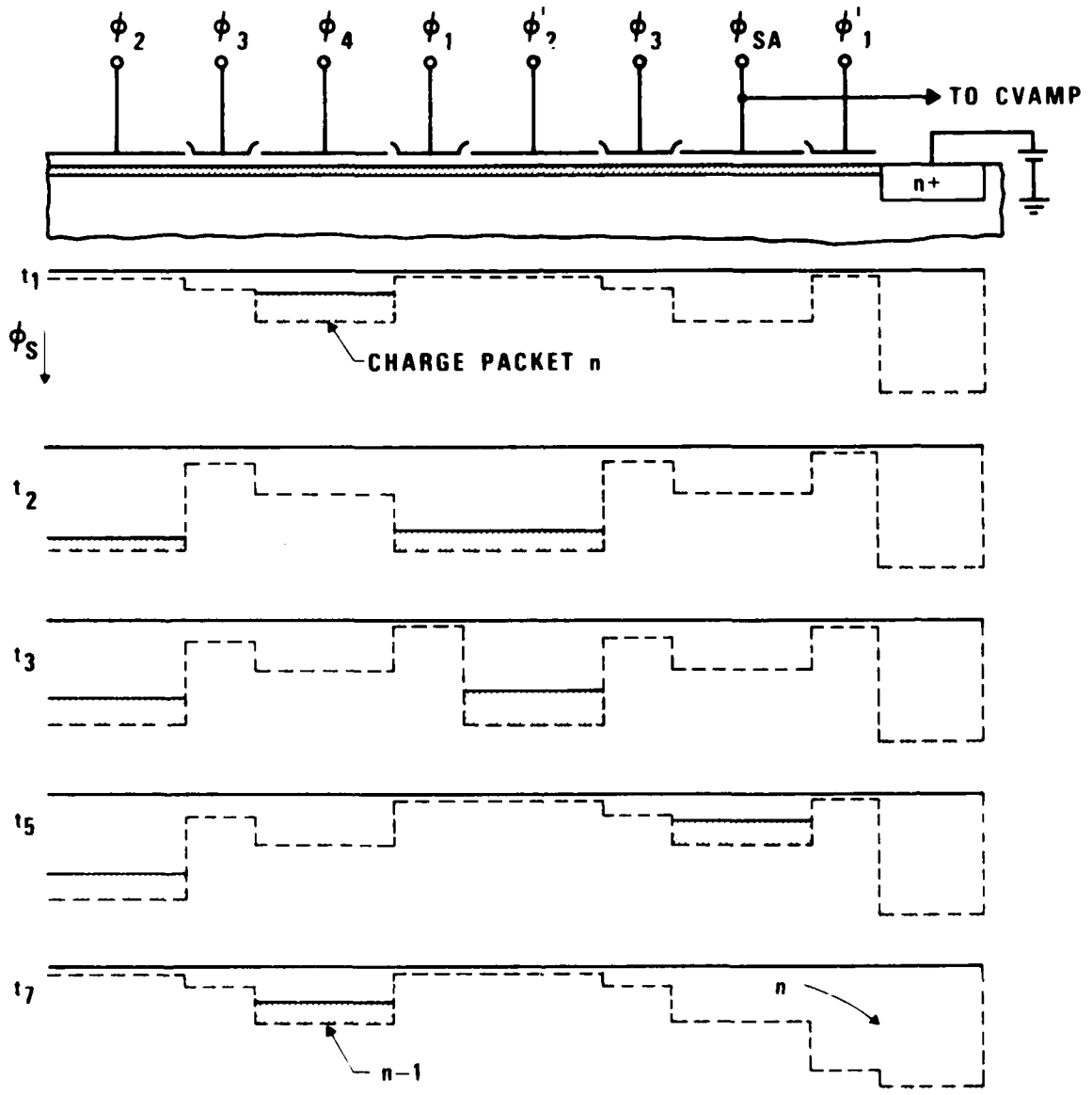


Figure 7a. CCD Output Stage Showing Surface Potential Variations
During Charge Transfer Between CCD Registers

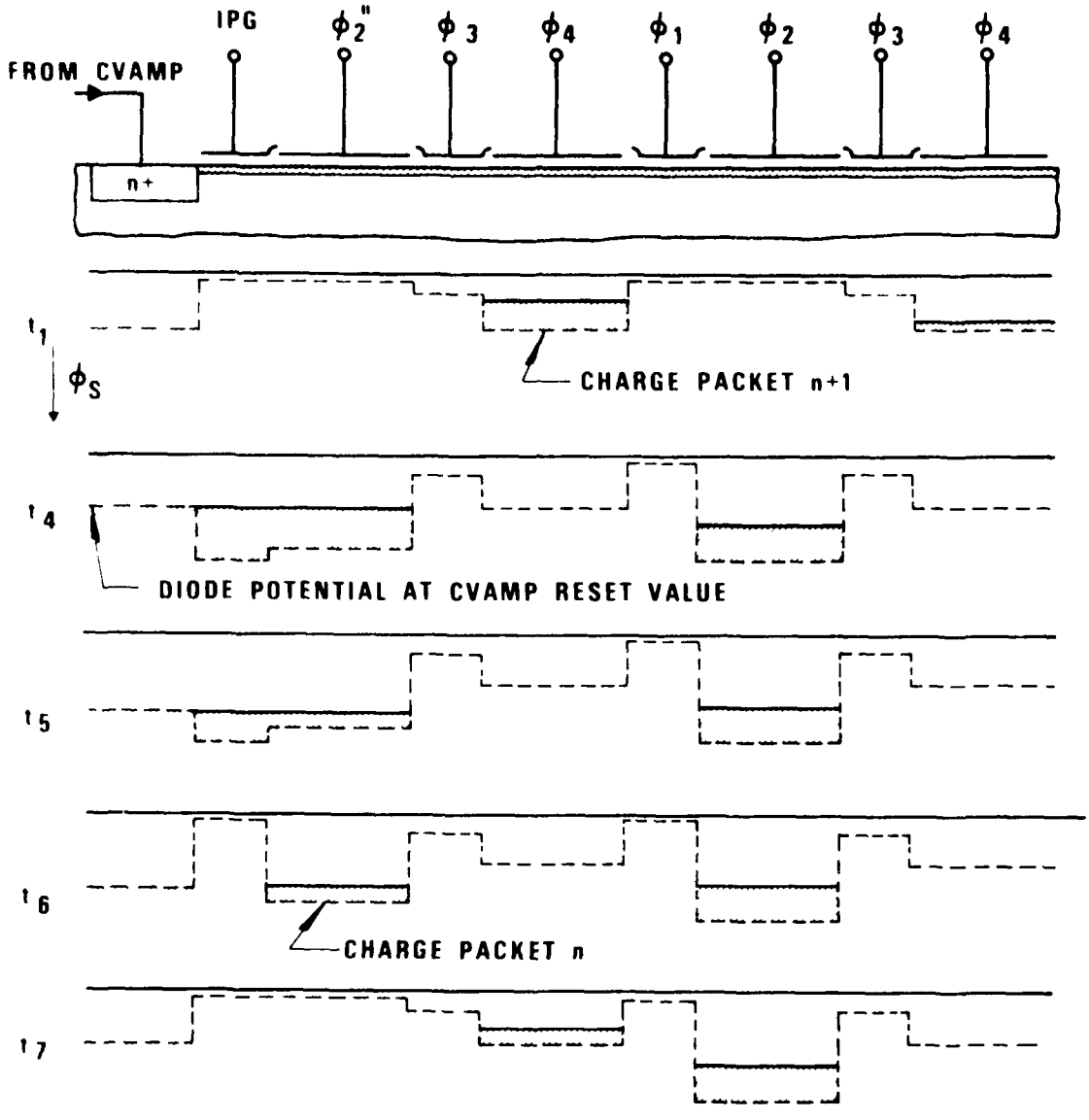


Figure 7b. CCD Input Stage Showing Surface Potential Variations During Charge Transfer Between CCD Registers

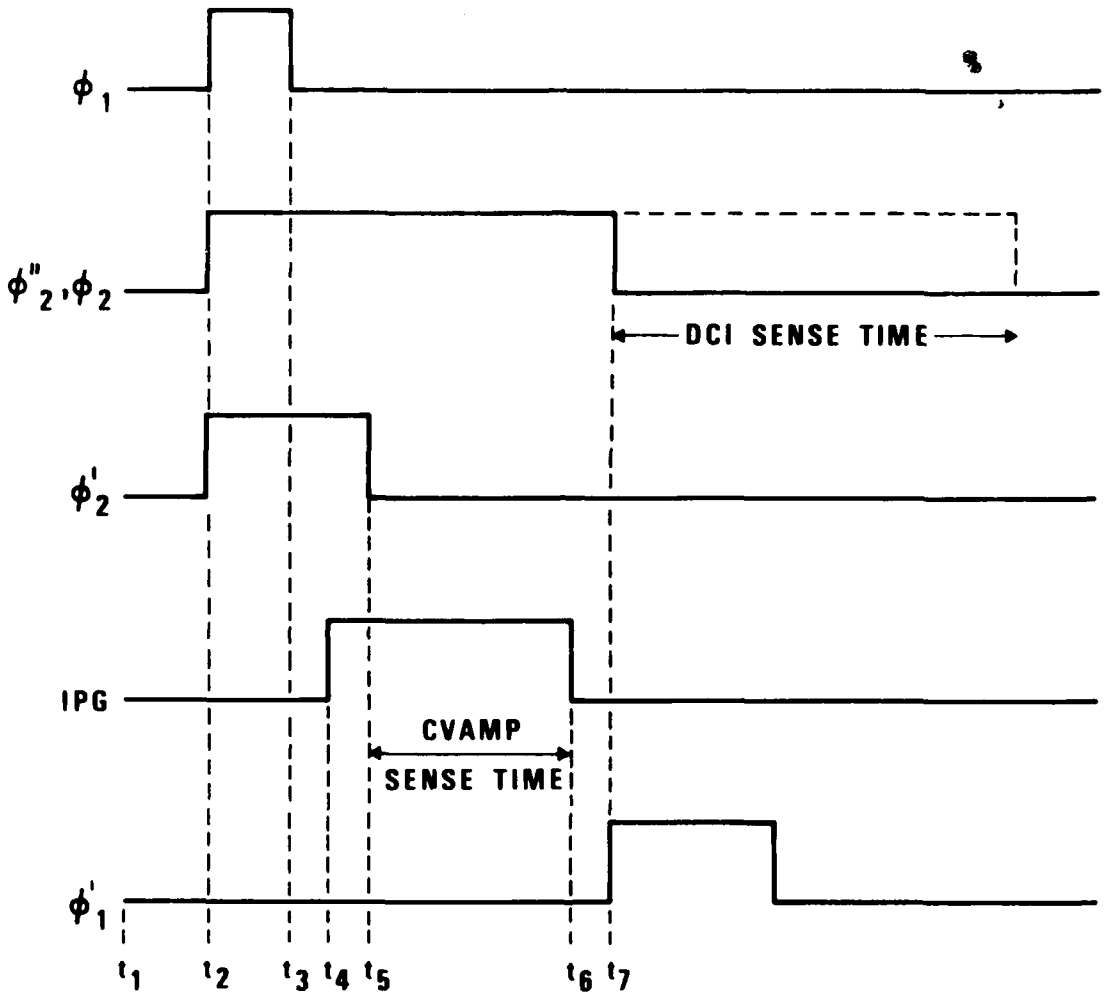


Figure 7c. Clocking Scheme for Transferring Charge Between CCD Shift Registers

next CCD is turned on, and at t_6, ϕ_2' is turned off. This transfers the charge packet n to the sampling electrode ϕ_{SA} that is connected to the unity gain amplifier. The amplifier converts the charge under ϕ_{SA} to a voltage, which sets the input diode potential of the following CCD, and therefore, the amount of charge that is stored under ϕ''_2. The same clock driving ϕ''_2 drives all the other ϕ_2 electrodes, but has independent amplitude control, thereby allowing the fat zero reference level to be adjusted.

At t_6, the input gate is turned off. The CVAMP has between t_6 and t_8 to settle, which at a clock rate of 1 MHz is approximately 370 ns. At t_7, ϕ_1' is turned on so that the charge packet that was located under ϕ_{SA} is dumped into the reverse-biased diode at the end of the CCD register. At the same time, the ϕ_2 clocks, including ϕ_2'', are selectively turned off, depending on the reference code in the digital shift register, and sampling under the first ϕ_4 electrode in each CCD is performed as normal. Figure 7b shows charge packet n being sampled under the first ϕ_4 electrode and charge packet n + 1 not being sampled. After ϕ_1' is turned off, the CVAMP, and hence the input diode potential, is reset.

The clocking scheme results in the last cell of each 128-stage CCD being split between itself and the adjacent CCD in the serial chain. Furthermore, the transfer scheme is inverting, which requires the outputs from the differential CCD channels to be interchanged when they are connected to the inputs of the following CCD pair.

2. Charge-to-Voltage Amplifier

A key part of the circuitry for successful transfer of charge between CCD shift-registers is a unity gain charge amplifier. Since the general-purpose filter requires 14 such amplifiers, primary requirements are low power consumption and small silicon area. In addition, for operation at 1 MHz with a 3 V signal swing, the amplifier must settle to 1 percent in approximately 350 ns. High open loop gain is not required, as any inaccuracy in the closed loop unity gain mode can be compensated by adjustment of the feedback capacitor C_f.

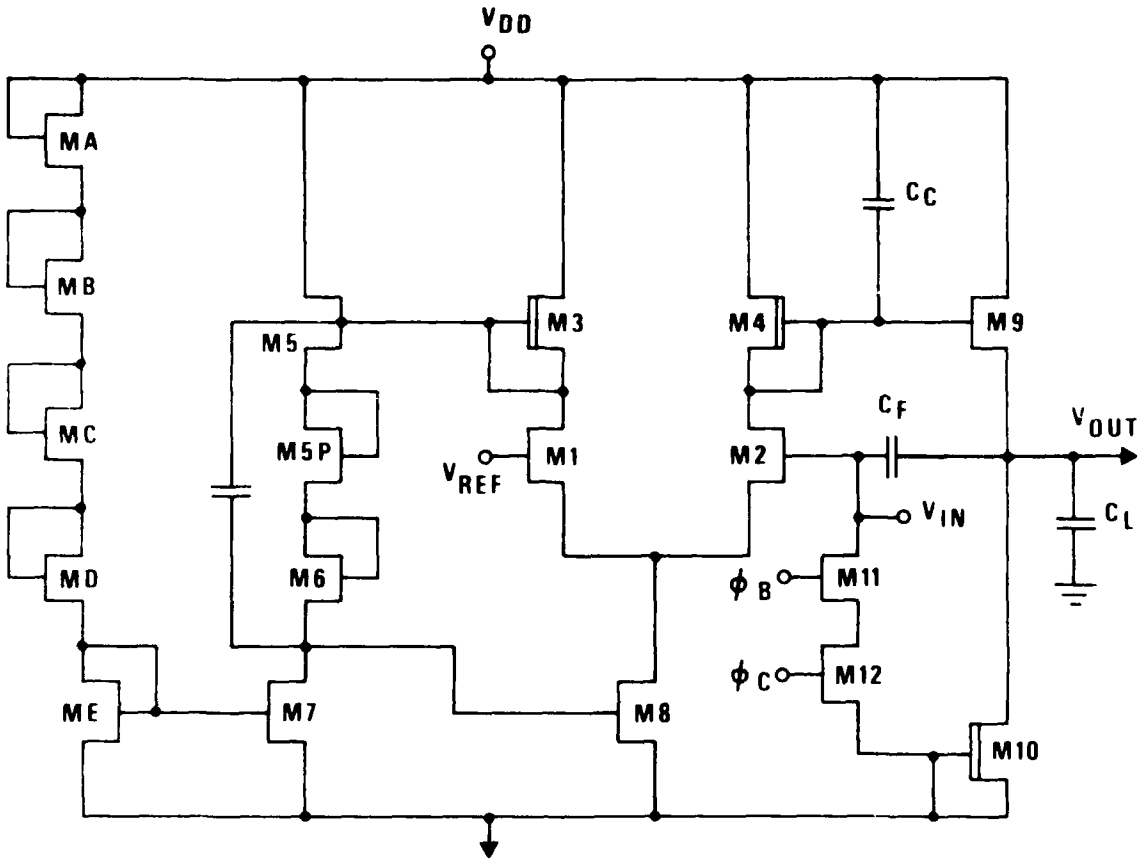
An NMOS amplifier circuit that fulfills the above requirements is shown with its characteristics in Figure 8. The amplifier is composed of a single differential gain stage and a differential to single-ended conversion stage. The feedback path between M1 and M8 also provides for improved common mode rejection. The output is taken via a source-follower stage that is designed to drive a load capacitance of up to 5 pF. Open loop unity gain frequency compensation is provided by C_c, which also limits the amplifier slew rate. The amplifier occupies an area of 0.05 mm^2 that includes both reset transistors and the closed loop gain adjustment capacitor C_f.

F. OUTPUT SENSING CIRCUIT

Current sensing, rather than voltage, is employed so that a linear transfer characteristic is realized when the diode cutoff or surface potential setting input method is used.[1] Furthermore, because the CCD sensing electrode is maintained at a constant potential, a higher charge handling capacity, and hence dynamic range, can be realized than with voltage sensing.

The circuit of Figure 9 illustrates how current sensing is performed on the filter chip. The technique requires the use of a DCT to sense the signal image charge on the ϕ_4 lines differentially and provide a voltage output, given by

$$V_{out}(n) = -\frac{C_{in}}{C_f}\sum_{i=1}^{N} h_i V_{in}(n-i) \qquad (9)$$



CHARGE AMPLIFIER CHARACTERISTICS	
POWER	6 mW
OPEN LOOP GAIN	40
UNITY GAIN BANDWIDTH	11 MHz
SLEW RATE	20 v/μs
PHASE MARGIN	50°
LOAD	5 pF
SILICON AREA	0.05 mm^2

Figure 8. Charge Amplifier Circuit and Characteristics

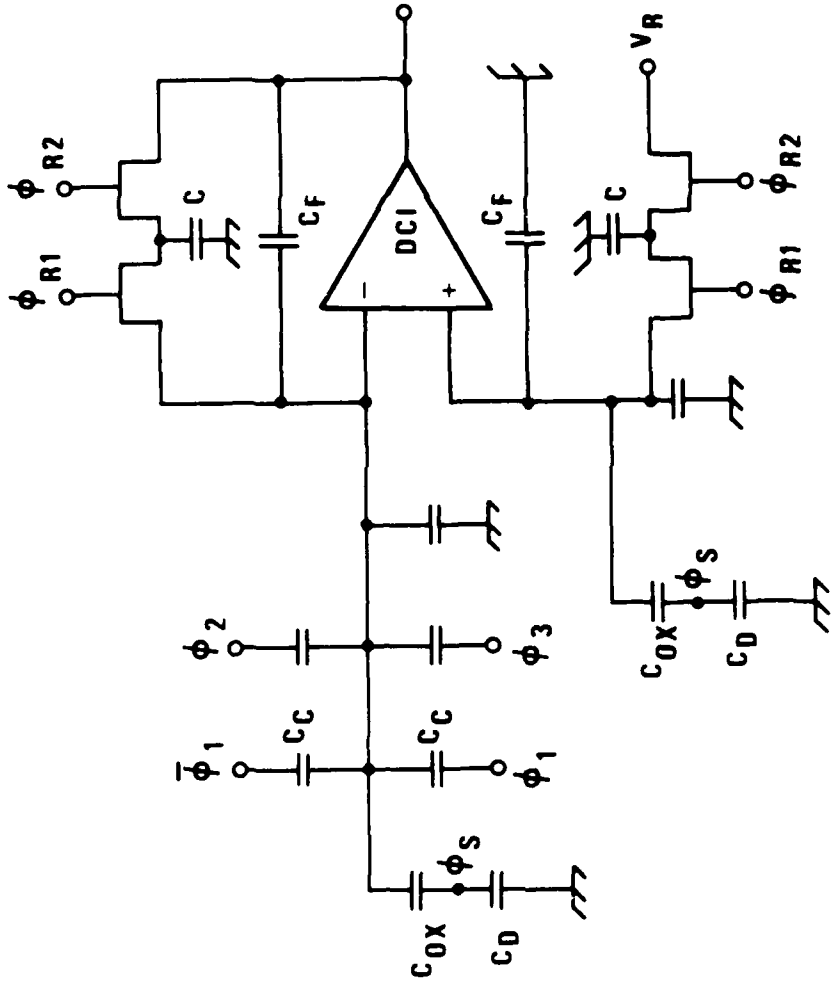


Figure 9. DCI Circuit With Parasitics

where C_{in} is the capacitance of the input metering well of the CCD, C_f is the capacitance of the feedback capacitor, and h_i are the filter weighting coefficients. The CCD ϕ_4 electrodes are maintained at a fixed dc potential by the two switched capacitor resistors,[11,12] represented by the minimum size capacitor C and the two MOSFET switches gated on by two nonoverlapping clock pulses, ϕ_{R1} and ϕ_{R2}. The use of the switched capacitor resistors avoids the reset noise that would be introduced if the resistors were replaced by simple switches. In addition, the operational amplifier used does not have to be compensated for unity gain internally because it is not reset. Much higher bandwidth is possible in this mode of operation.

The filter chip includes four of these output sensing circuits with each DCI connected to the ϕ_4 summing buses from two differential CCD pairs, resulting in a total CCD oxide capacitance on both amplifier inputs of approximately 85 pF. To strike a balance between the size of feedback capacitance C_f and processing gain, the DCIs have been designed to deliver a full 8 V output when 25 percent of the taps are 1's, 64 stages, with maximum signal present in the CCD. This requires a 10.7 pF feedback capacitor giving a total signal gain of 2, or a gain per tap of 0.03.

The ϕ_4 clock feedthrough is cancelled by a complementary clock and cancellation capacitance C_c. To eliminate the fat zero signal, the amplifier common mode rejection must be greater than 60 dB. The parasitic capacitances associated with each input to the DCI necessitates phase-compensation for a closed loop gain of 0.03. To achieve good gain stability, the open loop gain must be greater than 1,000. Operation at 1 MHz data rate requires that the amplifier settle in approximately 350 ns.

A schematic of the DCI amplifier is given in Figure 10. The bias string M14 and M18 is matched to the level shifters M5 to M8 and M10 to M13, so that the quiescent operating point is well controlled. The input differential pair M1 and M2 operates at a current of 65 μA, each giving a gain of 26 in the first stage. The voltage at the drain of M1 is fed back to the tail current source M9 by the source follower M5 to provide increased common mode rejection and to perform a differential to single-ended conversion in the first stage. The source follower level shifter M10 to M13 provides the correct dc voltage to the second stage. Phase shift through this level shifter is minimized by the high frequency feed forward capacitor, C_{FSO}.

The second stage gain of 43 is realized with an enhanced gain stage, M19 to M22. About 130 μA flow through both the cascode transistor M20 and the current source M21. M27 buffers the second stage from both the output buffer load and a portion of the low frequency compensating capacitor, CCF, to increase the bandwidth of the second stage.

The output is a source follower operating at 300 μA of current to drive a load of 15 pF. Additional current for pulldown is provided by the diode M15, which also controls the operating point of the second stage during negative output slewing.

The unity gain crossover frequency is 31 MHz and the zero phase margin frequency is 18 MHz. The performance of the amplifier is summarized in Table 2.

G. FILTER CLOCKING

The filter chip requires a total of 13 clocks to perform the variety of functions previously described. All these clocks are derived on-chip from a single master clock input that operates at four times the system frequency. All clock drivers are included on-chip and are designed to operate at a maximum system frequency of 1 MHz. Figure 11 shows the complete timing diagram for the filter chip.

[11] J.J. Caves, M.V. Copeland, C.F. Rahim and S.D. Rosenbaum, "Sampled Analog Filtering Using Switched Capacitors as Resistor Equivalents," *IEEE J. Solid-State Circuits*, Vol. **SC-12** (December 1977), pp. 592—599.

[12] B.J. Hosticka, R.W. Brodersen and P.R. Gray, "MOS Sampled Data Recursive Filters Using Switched Capacitor Integrators," *IEEE J. Solid State Circuits*, Vol. **SC-12** (1977), p. 600.

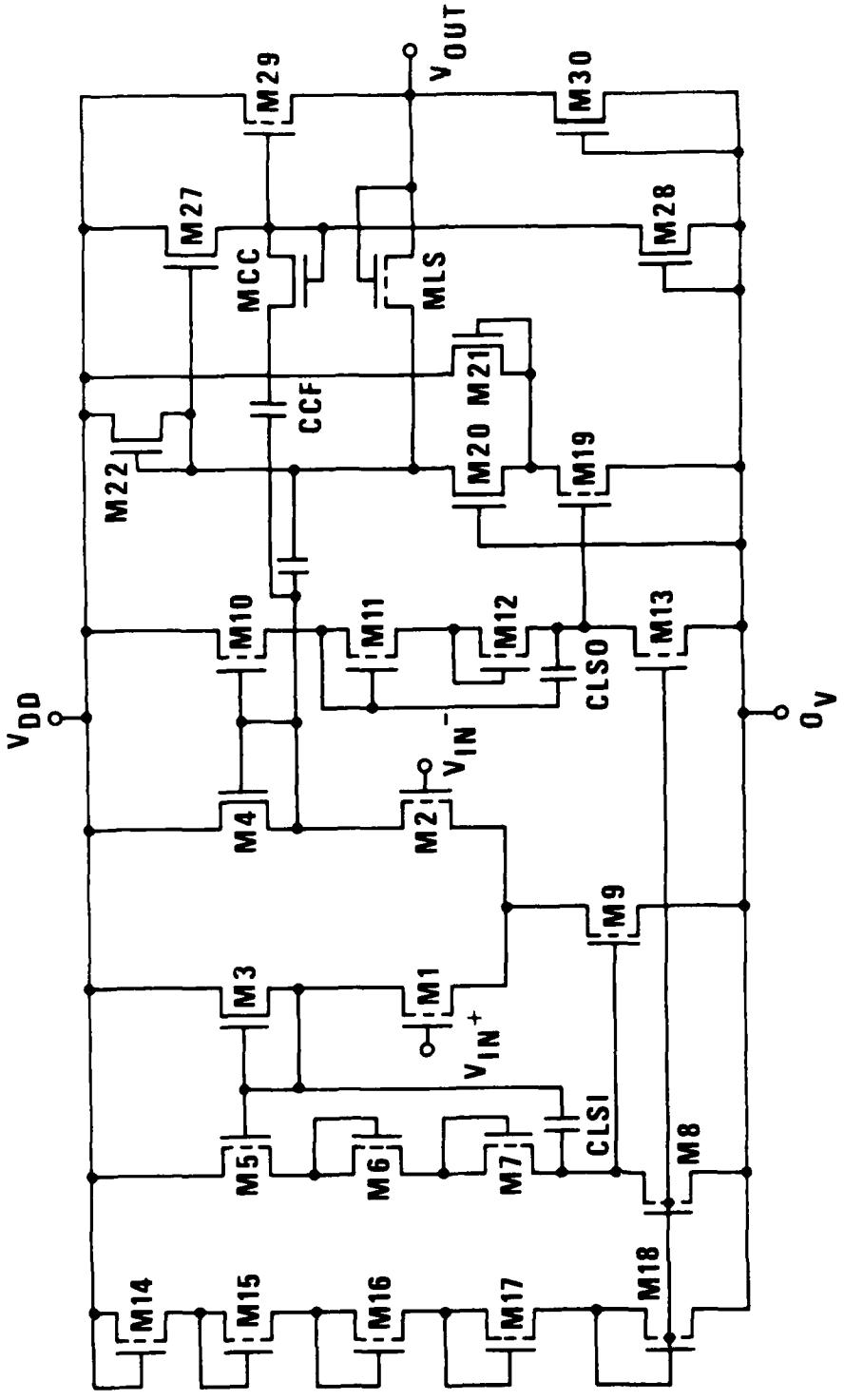


Figure 10. DCI Amplifier Schematic

TABLE 2. DCT CHARACTERISTICS

Operating Voltages	$V_{DD} = 15$ V $V_{BB} = -5$ V
Power dissipation	16 mW
Open loop gain	1,058
Output resistance	544 ohms
Closed loop gain (15 pF load)	6.7
Bandwidth (Gain = 6.7)	4.7 MHz
Phase margin	78 degrees
Gain margin	2.73

The master clock is fed to a generator that produces two nonoverlapping waveforms, M1 and M2, and two delayed versions of these waveforms, by approximately 40 ns, M1D and M2D. The M1 and M2 clocks, operate a shift register divider that generates four nonoverlapping clocks Q1 to Q4. These signals, M1 to Q4, are combined to trigger the clock driver circuits that generate all the other clock waveforms shown in Figure 11.

The basic clock driver circuit is shown in Figure 12 and has been built in five different sizes to drive the various loading capacitances, ranging from 10 to 720 pF. All the driver circuits were designed to have rise and fall times of 20 ns. Power dissipation of the 13 drivers plus the circuitry for generating the waveforms is approximately 550 mW at 1 MHz with a 15 V clock swing.

The driver circuit requires two nonoverlapping signals at its inputs labeled PU and PD for pullup and pulldown, respectively. Transistor M5 is used to charge the bootstrap capacitor formed by transistor M8 whose source and drain are tied together to form a capacitor. Transistor M7 pulls up the bottom plate of the bootstrap capacitor, which provides a large gate overdrive on transistor M10, allowing the clock driver to pull the output node to V_{DD}. Delay of the input pulse applied to node PU is provided by transistors M1 and M3 before it reaches the gate of M7 and M11. This delay causes M7 and M11 to remain on during the initial part of the rise of the driver output, thus achieving a larger charge on the bootstrap capacitor and ultimately a faster transition. The clock driver turnoff pulse applied to node PD discharges the bootstrap capacitor through M6 and after a small delay, pulls up the gates of M7 and M11 causing the output to be pulled low. The circuit is completely dynamic and draws no dc power, yet it provides a low output impedance that minimizes interactions between the various clock circuits.

Figure 13 shows how the various timing signals, M1 to Q4, are combined to the inputs of the clock drivers to provide the pullup and pulldown signals for the drivers. One example of the logic is the ϕ_1 driver for the CCD clock. The pullup signal to the driver is obtained by gating M1D with Q1 on the gate of a series MOSFET. The pulldown command is obtained by using the M2 clock. Note that in all cases the logic ensures that the pullup and pulldown signals are never on simultaneously.

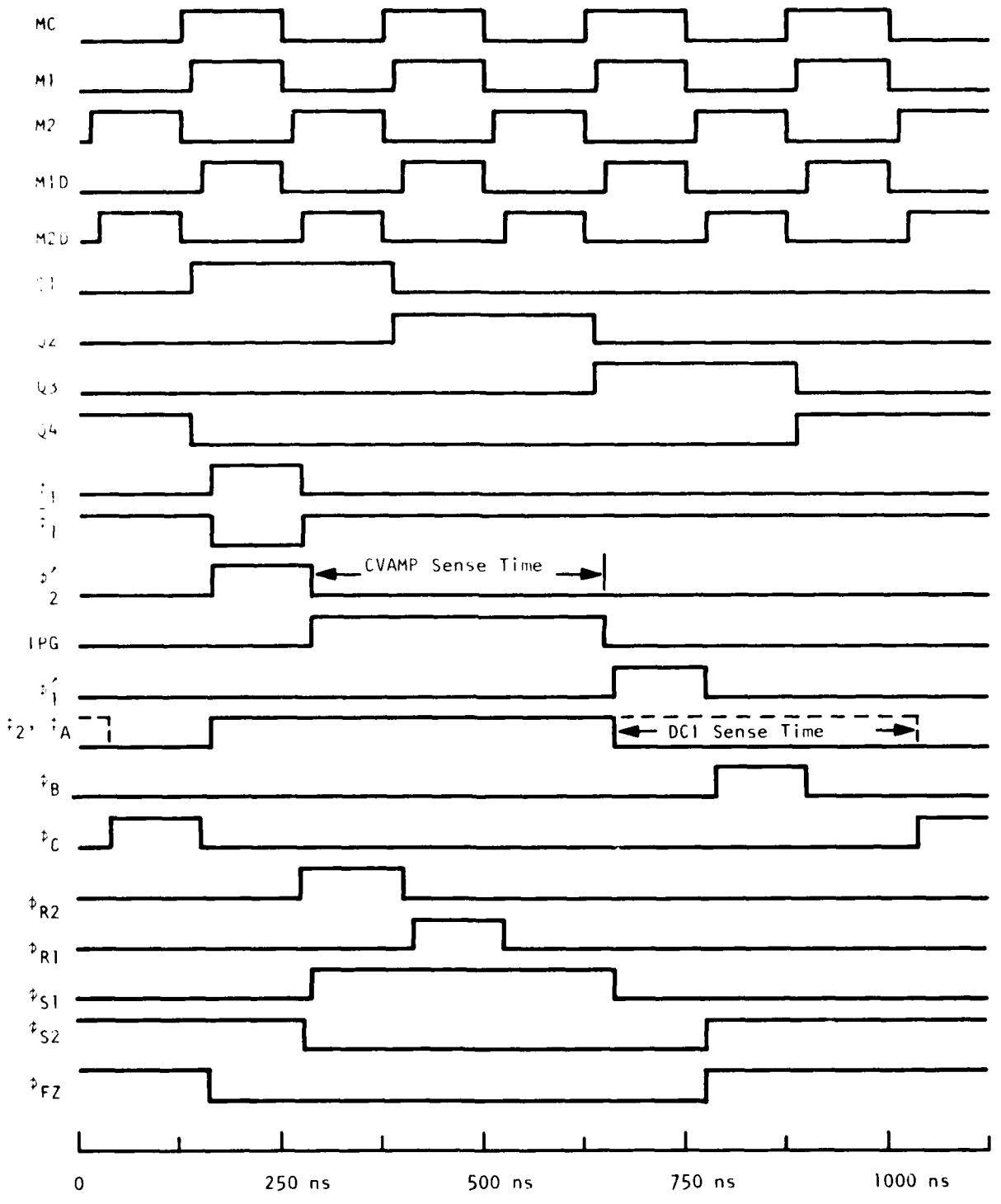


Figure 11. Filter Timing Diagram at a System Frequency of 1 MHz

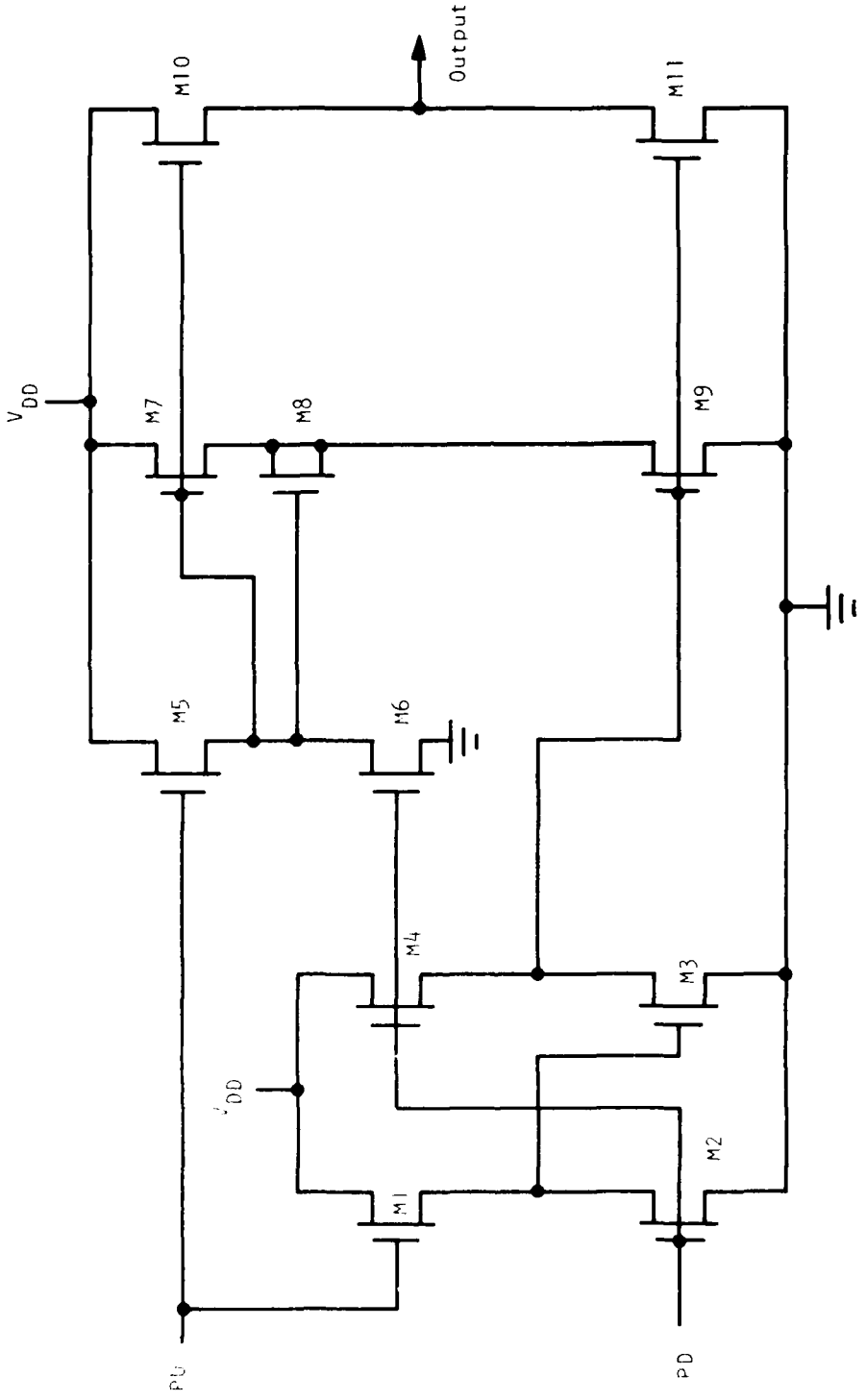


Figure 12. Clock Driver Circuit

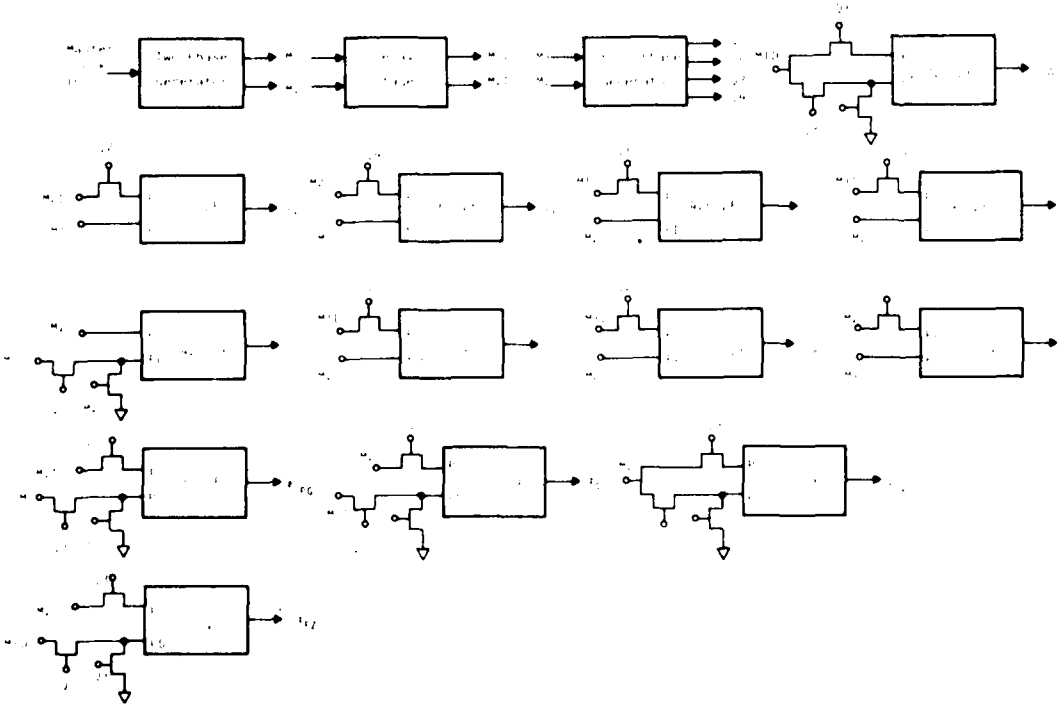


Figure 13. Derivation of Clock Signals With Drive Capacitances

SECTION III
FILTER IMPLEMENTATION AND PERFORMANCE

The device was fabricated using e-beam generated masks and a standard NMOS two-level polysilicon process with an 800Å gate oxide and a minimum feature size of 5 μm. A photomicrograph of the chip identifying the various circuits is shown in Figure 14. The chip comprises approximately 9K enhancement and depletion NMOS transistors, and 2,048 surface channel CCD stages. The chip measures approximately 7.1 by 7.4 mm (52.5 mm^2 or 80K mil^2), and at 1 MHz dissipates approximately 900 mW.

A. WEIGHTING COEFFICIENT RESOLUTION

The weighting coefficient resolution of the programmable transversal filter is illustrated by the filter impulse response of Figure 15. In this figure, the device is operated in the 128-stage by 8-bit mode with a range of the tap weights from −64 to +63. The transition from 00000000 (decimal '0') to 11111111 (decimal '−1') occurs at the center of the photograph. The lack of a discontinuity of slope here, and at other bit transitions, verifies the 8-bit code resolution. The weighting coefficient resolution of the filter is further illustrated by the filter responses of Figures 16 and 17. In each case, a 128-stage filter was designed using the Parks and McClellan[18] finite impulse response filter design program. Figure 16 shows the experimental and computed responses of a 128-stage by 8-bit filter designed to have a bandpass at 0.2 F_c with stopbands from zero to 0.18 F_c and from 0.22 F_c to 0.5 F_c. At a clock frequency of 147 kHz, the passband is at 29.4 kHz with the stopband edges at 26.5 kHz and 32.4 kHz. With ideal weighting coefficients, the stopbands would have uniform peak ripple at −53 dB. However, rounding to 8 bits results in a nonuniform stopband ripple as shown in the theoretical response. It can be observed that there is good agreement between the theoretical and experimental responses, with a stopband attenuation of approximately 50 dB, corresponding to a weighting coefficient accuracy of approximately 8 bits or 0.4 percent. If the tap weight accuracy was much less than this, the stopband attenuation would be less than that predicted by theory and the sidelobes in the experimental response would not follow those of the theoretical response so closely.

Figure 17 shows the experimental and theoretical filter responses for a 128-stage by 8-bit lowpass filter with a passband from zero to 0.1 F_c and a stopband from 0.12 F_c to 0.5 F_c. Again, there is close agreement between the observed and theoretical responses with a stopband attenuation of approximately 40 dB.

B. DYNAMIC RANGE

In a programmable filter, the dynamic range of each filter configuration varies according to the average power of the filter impulse response. Consequently, the most meaningful way to define the dynamic range of a programmable filter is to refer to the dynamic range per tap. This figure can then be used in conjunction with the value of the peak signal in the filter passband, to determine the dynamic range of that particular filter configuration.

The dynamic range per tap is most conveniently measured by using the impulse response to determine the maximum signal-to-noise ratio, measured over the Nyquist bandwidth (zero to $F_c/2$) with a linearity of 1 percent or 40 dB. Although each tap contributes noise and only one tap provides the signal, the resulting signal-to-noise measurement is a measure of the peak signal per tap to the dominant noise source of the DCI output circuitry. A wideband RMS voltmeter was used to measure the noise in conjunction with a lowpass filter having a cutoff frequency of $F_c/2$. The dynamic range per tap was

[18] J.H. McClellan, T.W. Parks and L.R. Rabiner, "A Computer Program for Designing Optimum FIR Linear Phase Digital Filters," *IEEE Trans. Audio Electroacoustics*, Vol. AU-21 (1973), pp. 506—526.

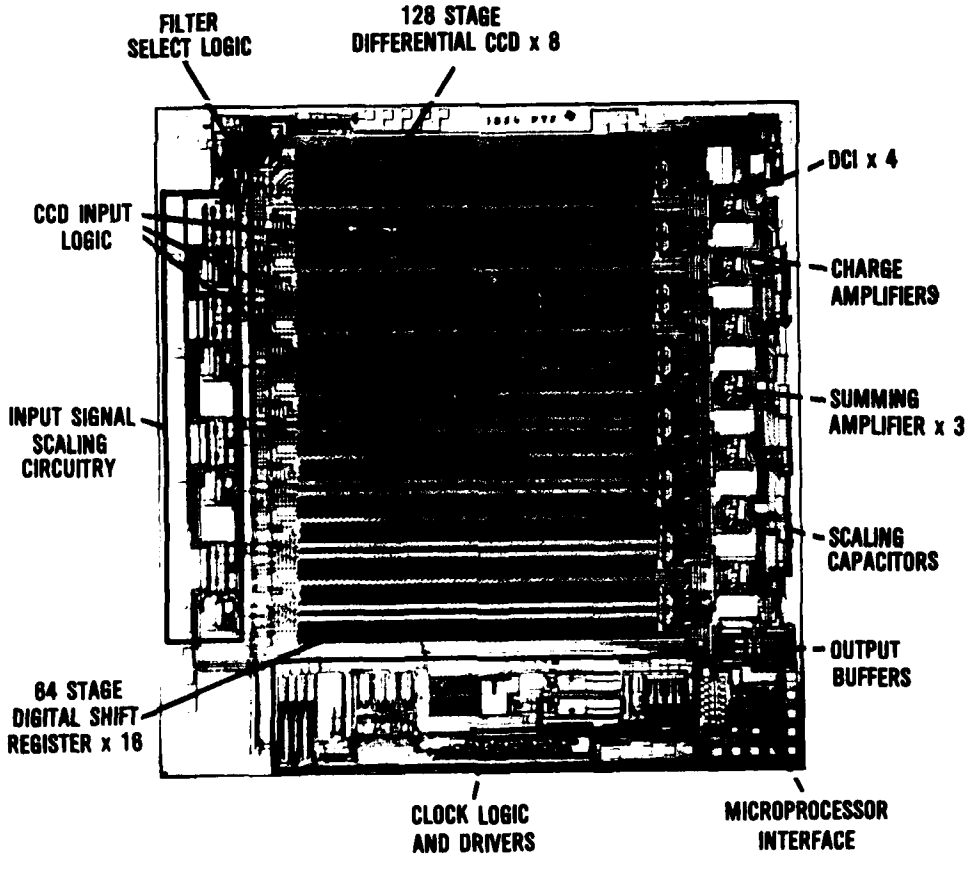


FIGURE 14. PHOTOMICROGRAPH OF THE 1,024-STAGE PROGRAMMABLE TRANSVERSAL FILTER

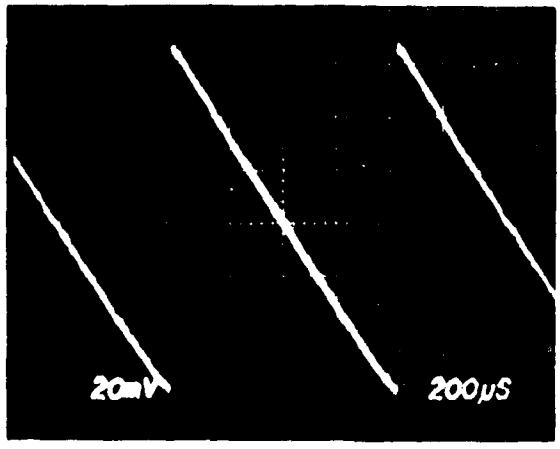


Figure 15. Filter Impulse Response for a Range of the Tap Weights From −64 to +63

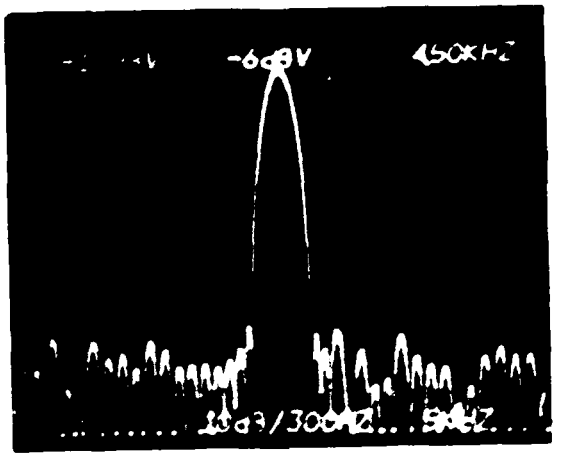
determined to be approximately 35 dB, corresponding to a peak RMS signal per tap of 44 mV and an RMS noise voltage of 2 $\mu V/\sqrt{Hz}$, or 1 mV measured over a 50 kHz bandwidth, F. 2. The processing gain per tap corresponds to 0.025 compared with a calculated value of 0.03.

From a knowledge of the dynamic range per tap and the peak signal in the passband, calculated using the filter design program, the dynamic range of the bandpass *filter* is 60 dB and the lowpass is 48 dB. These figures have been confirmed by direct measurements on the filters. The maximum dynamic range of the programmable filter is realized when a square-wave sequence is correlated with a square wave of tap weights. In this case, the output DCI can be saturated and a dynamic range of 78 dB realized.

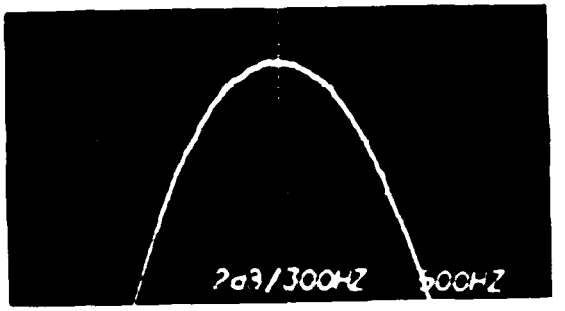
C. CODE DEPENDENT OFFSET

As discussed in Section I, a primary requirement of any programmable filter is the elimination of code dependent offset. The approach described in this report for implementing the programmable transversal filter ensures that the only contribution to the offset is from variations in fat zero charge and sampling electrode capacitance. Therefore, a useful test to determine the dependence of the output dc level to code changes is to inject a fat zero charge and change the code from all 0's to all 1's.

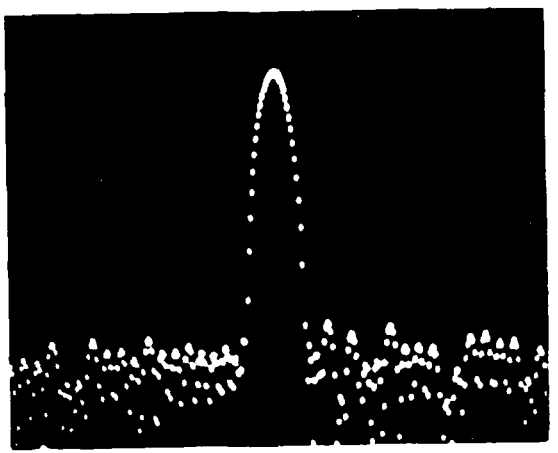
With a code of all 0's, none of the fat zeros are sampled under the ϕ_4 electrodes, and therefore, the output dc level is determined only by the biasing conditions of the DCIs. With a code of all 1's, every fat zero is sampled and any imbalance between the +ve and −ve CCD channels will be reflected as an offset in the output dc level. Figure 18 shows the results of this test performed on a device operated in the 512-stage by 1-bit mode. The two center traces are at a scale of 50 mV/division and are the dc levels at the output of the device for all 0's and all 1's code. Thus, for a code change from all 1's to all 0's, there is a code dependent offset of approximately 50 mV. Several other codes were loaded into the device with none of them causing the output dc level to change by more than 50 mV from the all 0's reference level. These results indicate not only good matching between the +ve and −ve CCD channels, but also good gain matching between the charge amplifiers at the end of each 128-stage CCD register. In the 512-stage mode, each charge packet passes through three such amplifiers. The remaining trace in Figure 18 is at 1V division and represents correlation of a square wave with the all 1's code, causing the DCI output to clip.



Experimental Response



Passband, Experimental Response
2 dB/div.



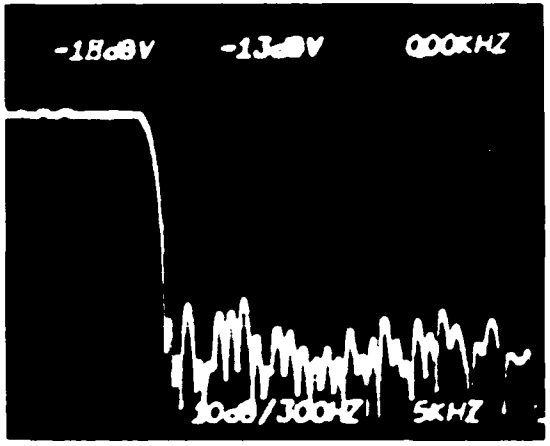
Computed Response

Performance

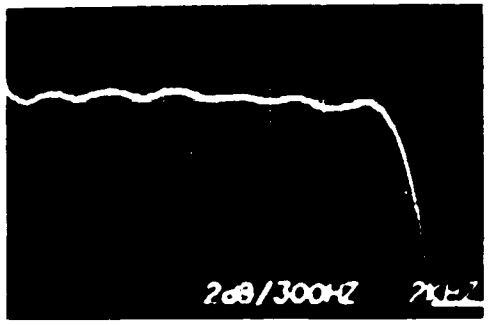
Center Frequency = $F_c/5$, at F_c = 147 kHz
CF = 29.4 kHz

- Stopbands at 26.5 kHz, 32.4 kHz
- 3 dB Bandwidth = 1.18 kHz
- 3 dB Stopband Transition = 2.35 kHz
- Stopband Attenuation ~ 50 dB
- Dynamic Range = 60 dB, Measured Over Nyquist Sampling Frequency with 1- Harmonic Distortion

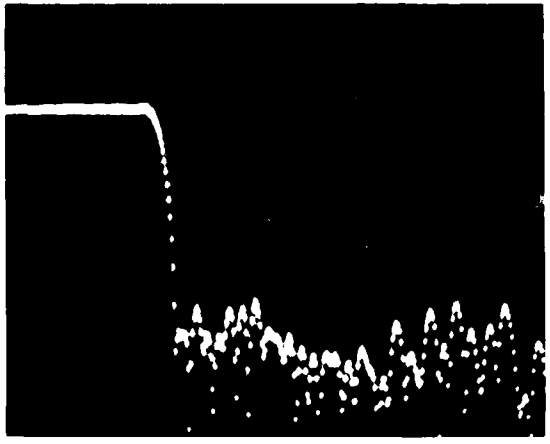
Figure 16. Experimental and Computed Responses for a Narrow Bandpass Filter (Vertical scale is 10 dB division; horizontal scale is 10 kHz division)



Experimental Response



Passband, Experimental Response
2 dB/Div.

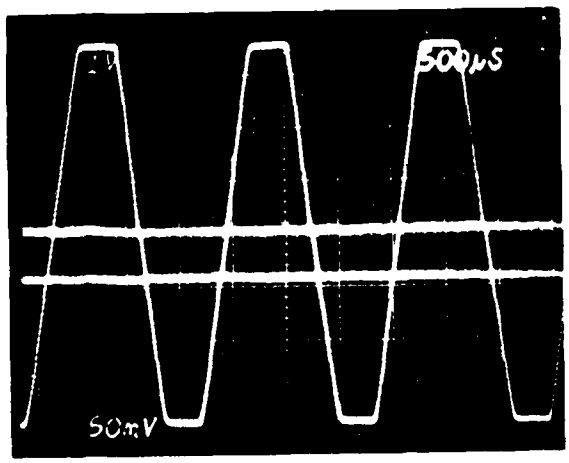


Computed Response

Performance

- Passband Edge = 0.1 F_c = 14.7 kHz
- Passband to Stopband Transition = 2.9 kHz (.1 - .12 F_c)
- Stopband Attenuation ∿ 40 dB
- Passband Ripple ∿ 0.4 dB, Theoretical = 0.3 dB
- Dynamic Range = 48 dB, Measured over Nyquist Sampling Frequency with 1% Harmonic Distortion

Figure 17. Experimental and Computed Responses for a Lowpass Filter (Vertical scale is 10 dB/division; horizontal scale is 10 kHz division)



- Device Operated in the 512-Stage by 1-Bit mode
- Center Two Traces Are the Dc Output Levels of the Device for a Code Change from all 0^S (Upper) to all 1^S, with No Ac Input Signal and No Output Level Adjustment. Vertical Scale is 50 mV/Div.
- Third Trace Is Device Output for a Code of All 1^S, Correlated with a Square Wave. Vertical Scale is 1 V/Div.

Figure 18. Illustration of Code Dependent Offset

D. CHARGE TRANSFER BETWEEN REGISTERS

The performance of the serial charge-to-voltage-to-charge-conversion circuitry, used in six of the nine filter configurations, is illustrated in Figures 19 and 20. Figure 19 shows the dc transfer characteristic of two cascaded 128-stage delay lines incorporating two conversion stages. The characteristic illustrates the inverting nature of the conversion scheme and clearly shows a dc gain close to unity; dc unity gain is vital for realizing the full ac operating range of cascaded filters, approximately 3.5 V peak-to-peak.

Figure 20a shows the device output after the input signal has passed through a single 128-stage filter with one charge-to-voltage conversion; the through gain is approximately 0.98. Figure 20b shows the device operated in the 1,024-stage by 1-bit mode where each charge packet has undergone eight conversions. Here, the total through gain is approximately 0.6, corresponding to a conversion gain stage of 0.93. However, in addition to signal attenuation due to serial conversion, this figure includes significant MTI degradation resulting from charge transfer inefficiency (CTI). For 1,024 stages, a CTI of 4×10^{-4} transfer produces an n product of 1.23. The effect of nonunity gain charge conversion is a reduction in dynamic range; however, for the values of conversion gain measured, within approximately 2 percent of unity, this is a second order effect compared to CTI.

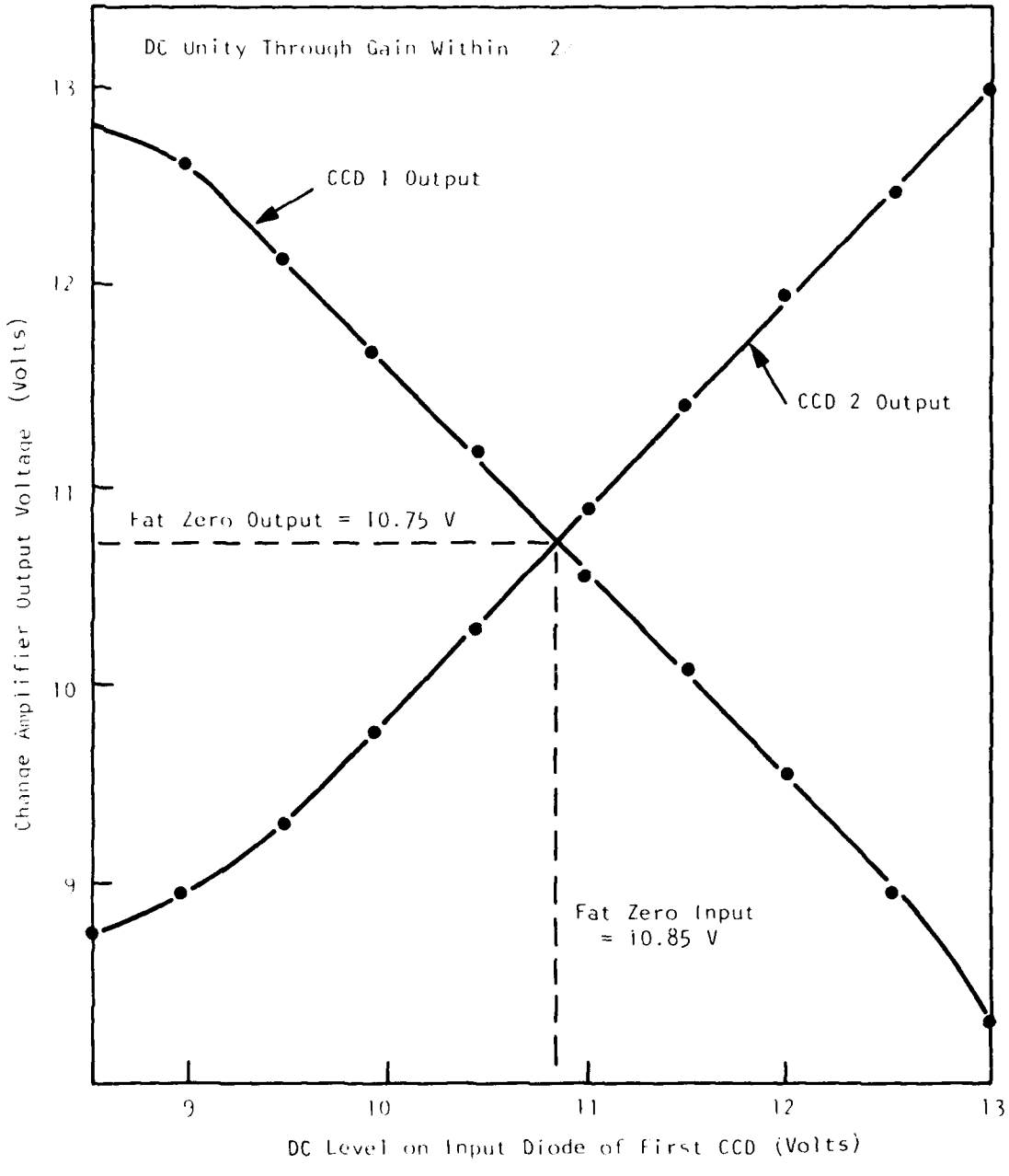
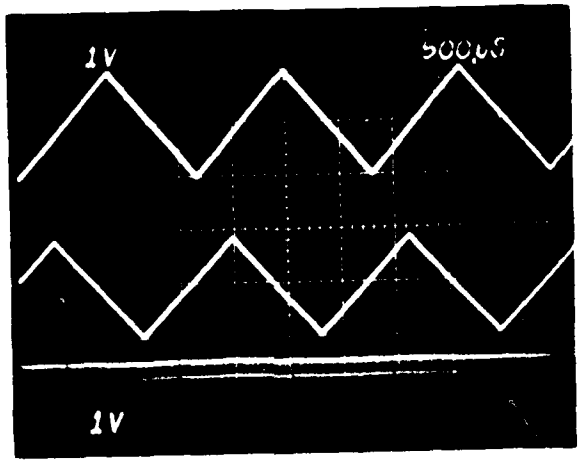
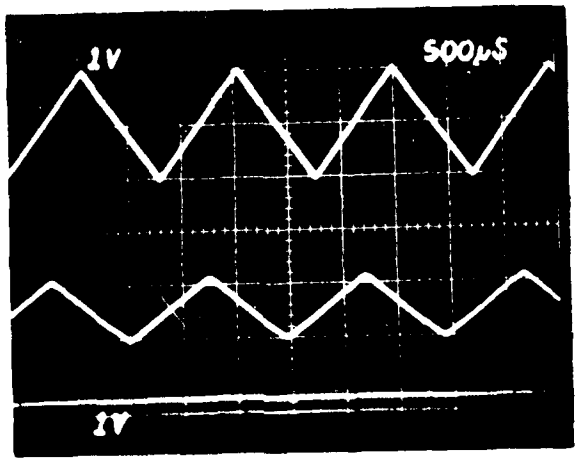


Figure 19. DC Transfer Characteristic of Two Cascaded 128-Stage Delay Lines



(a)
Four Conversions, 22 CCD Stages



(b)
Eight Conversions, 1024 CCD Stages

Figure 20. Serial Voltage-Charge-Voltage Conversion

E. MATCHED FILTERING

An important class of applications that the general-purpose transversal filter is well suited to is correlation detection or matched filtering. In these applications, the waveform to be detected is the time reversal of the filters impulse response. The waveforms for correlation may be either pseudonoise (PN) sequences, in which case the weighting coefficients are +1, 0 or −1; or chirp waveforms where multibit resolution of the tap weights is required. Previously reported binary/analog correlators[8,9] have only been suitable for realizing PN sequence matched filters since they only possess single-bit accuracy. The programmable resolution feature of the binary/analog filter described in this report makes it suitable for matched filter applications with both PN sequences* and chirp waveforms. An important application of binary sequence matched filtering is in spread spectrum communication systems. These systems provide secure communications such as in the Global Positioning Satellite (GPS) system. The GPS system requires very long PN sequences, up to 1,024 stages, to obtain large time-bandwidth products to produce high processing gains required for worldwide, high resolution, navigation, using weak signals transmitted from satellites. Chirp waveform matched filtering has important applications in radar and sonar systems. The chirp waveform is used such that the transmitted signal energy is time compressed into a single output peak, the degree of compression being directly proportional to the time-bandwidth product of the chirp.

Figure 21 illustrates the device operated in the 1,024-stage by 1-bit mode and matched to an arbitrarily generated binary sequence. Figure 21a is the experimental response and Figure 21b is the computed response taking charge transfer inefficiency (CTI) into account, see Subsection III.E. In this mode, and with the device operating at 1 MHz, the filter performs over 10^9 1-bit multiply-and-add operations every second. Sequential digital implementation would require a multiplier having an internal clock rate of over 1 GHz.

Figures 22a to 22d show cosine chirp matched filter responses when the device is operated in the 256-stage by 4-bit mode. Figure 22a shows the impulse response of the cosine down-chirp filter, and Figure 22b illustrates the response of the filter when matched to a cosine up-chirp input signal. Figure 22c shows the theoretical characteristic assuming perfect CTE. The experimental response when the weighting coefficients have been corrected to account for CTI is shown in Figure 22d.

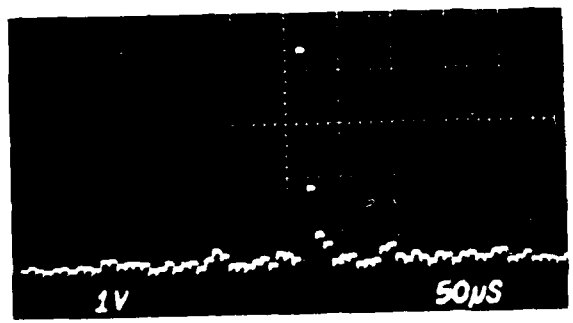
F. CHARGE TRANSFER INEFFICIENCY EFFECTS

The effect of charge transfer inefficiency is most noticeable in matched filtering applications, causing a reduction in the correlation peak-to-sidelobe ratio; as illustrated by the 1,024-stage binary sequence responses of Figure 21. Figure 21b is the computed response taking into account the measured CTI of 1.2×10^{-3} stage. This response was computed by using the value of CTI to calculate the distorted tap weight coefficients, Equation 10, and then using these weighting coefficients to perform the convolution sum digitally.

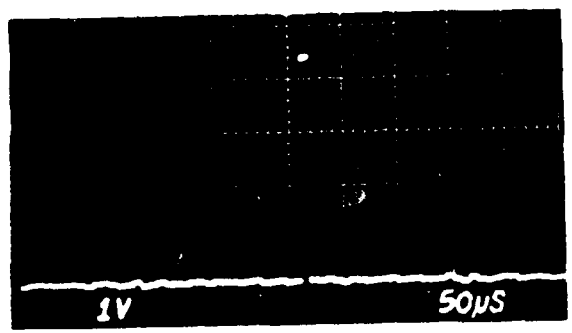
$$h_n' = h_n (1 - \epsilon)^n + \sum_{j=0}^{n-1} h_j \frac{n!}{j!(n-j)!} \epsilon^{n-j} (1 - \epsilon)^j \qquad (10)$$

A comparison of Figures 21a and 21b indicate close agreement between the experimental and theoretical responses. Figure 21c is the computed response for a device with perfect CTE. This clearly shows the deleterious effect of CTI on such a long surface channel matched filter.

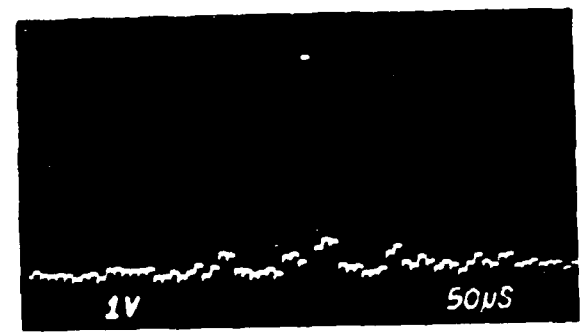
*To realize a matched filter with bipolar tap weights, the device must be operated in the 2-bit mode, since single-bit operation results in coefficients of +1 and 0. For example, a 512-stage PN sequence matched filter is realized by operating the device in mode 2: 512-stages by 2 bits.



Computed Response Accounting for CTI

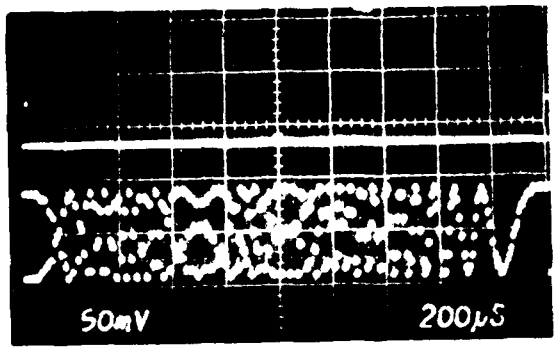


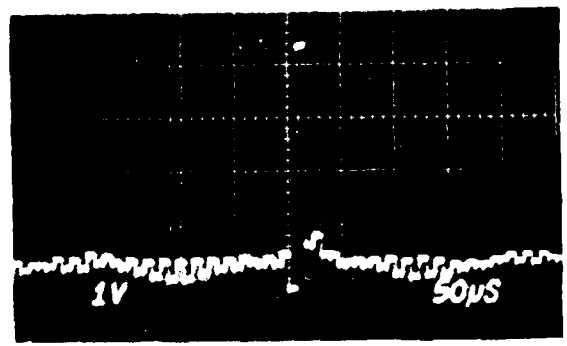
Computed Response for Zero CTI

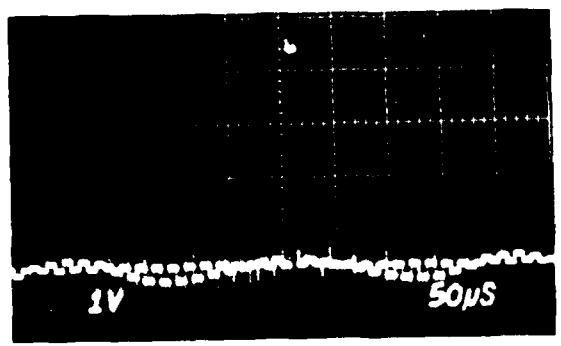


Experimental Response with Modified Weighting Coefficients

Figure 21. 1,024-Stage Binary Sequence Matched Filter Responses







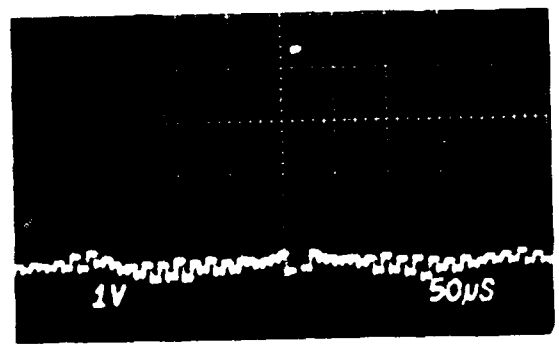


Figure 22. Operation as a 256 Stage to 4-Bit Chirp Matched Filter

As CTI effectively alters the value of the filter weighting coefficients, it can be compensated by programming the device with modified tap weights that invert the dispersion caused by CTI.[4] These modified tap weights can be calculated using Equation 11.

$$h''_n = \frac{h_n - \sum_{j=0}^{n-1} h''_j \frac{n!}{j!(n-j)!} \varepsilon^{n-j}(1-\varepsilon)^j}{(1-\varepsilon)^n} \qquad (11)$$

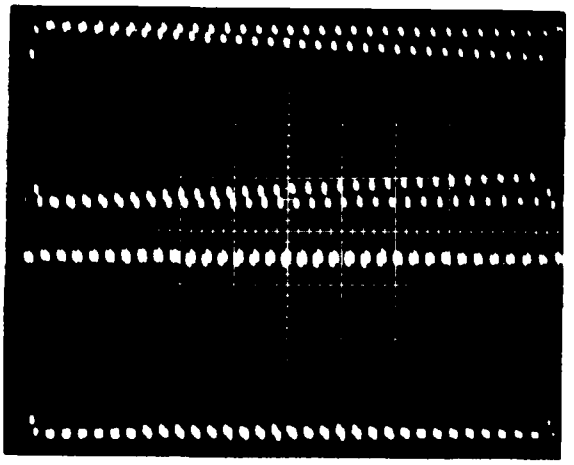
This technique is illustrated in Figure 23 where the top trace shows the device impulse response for a code that alternates between pairs of +1 and −1 coefficients, with no correction for CTI. The effect of CTI is to distort the response, a distortion that gets progressively worse as the charge packet traverses down the CCD. The bottom trace is the impulse response of the filter with weighting coefficients that account for the signal dispersion caused by CTI. The filter response is now virtually ideal.

Clearly, this technique is most effective when filters with multibit resolution are implemented. For example, the corrected response of the 256-stage by 4-bit chirp matched filter, Figure 22d, is close to the computed response of Figure 22c, which assumes perfect CTE. However, even in applications where the device is used as a binary sequence matched filter, correction for CTI can improve the correlation response. This is illustrated in Figure 21d where the device is used as a 1,024-stage binary sequence correlator with corrected tap weights. Although this response differs from the ideal response of Figure 21c, the correlation peak-to-sidelobe ratio is clearly improved over the uncorrected response of Figure 21a.

The ability to invert the dispersion caused by CTI in a programmable transversal filter has important implications. Since the length of a chirp or binary sequence correlator is not seriously limited by CTI, very long filters can be designed to realize high time-bandwidth products, and hence large compression factors.

Electronic programmability of transversal filters not only permits modification of the weighting coefficients to account for CTI, but with the use of a microprocessor, allows any ideal response to be realized. In such a system, a microprocessor would compare the filter response with that of the desired response and apply the necessary correction factor to the weighting coefficients. This is the principle of adaptive filtering, but can also be used to compensate for filter inaccuracies.

[4] D. D. Buss and W. H. Bailey, "Applications of Charge Transfer Devices to Communication," *Proc. Int. Conf. on CCD Applications*, CCD 1973, p. 83—93.



- Device Operated in the 128-Stage by 8-Bit Mode
- Top Trace Is the Device Impulse Response for a Code That Alternates Between Pairs of +1 and -1 Coefficients, No Correction for CTI
- Lower Trace Is Response When the Coefficients Have Been Corrected for CTI

Figure 23. Illustration of Weighting Coefficient Correction for CTI Effects

SECTION IV
CONCLUSIONS AND DISCUSSION

This report has described the architecture, design and performance of a general-purpose, 1,024-stage, electronically programmable transversal filter. This powerful, yet versatile, monolithic analog signal processing system has been realized through innovative techniques for performing programmable weighting and digital analog multiplication, together with the integration of a high level of both analog and digital support circuitry. The versatility of the device/system has been illustrated by its application in frequency filtering, where short, multibit resolution filters are required, and by its use in binary sequence matched filtering, where very long, single-bit precision correlators are necessary.

In the early 1980s, military signal processing systems will require chip performance in excess of 10^{11} gate Hertz; this figure corresponds to the goals of the VHSIC program. For certain applications, programmable transversal filters, under digital control, realize these goals today. For example, the device described in this report has a signal processing figure of merit of 2×10^{11} gate-Hertz. Although in the future, digital VLSI will undoubtly have a significant impact on signal processing there remain a number of applications where monolithic analog techniques possess an inherent advantage over digital methods, both in terms of throughput speed and number of functions per chip. Such applications are structured signal processing operations, such as scalar product operations, multipoint Fourier transforms and matched filters. These classes of functions are not well suited to digital methods, since they require groups of fast multiplications. Digital techniques require the use of dedicated fast parallel multiplier networks or serial processing. The former leads to increased system complexity and power dissipation, while the latter prevents real-time analysis, a vital feature in antijam communications. By combining digital and analog devices in a single processor, these problems are eliminated while high throughput and minimial system complexity is achieved. For example, when the device described in this report is used in conjunction with a Z80A microprocessor, the throughput of a 128-stage by 8-bit finite impulse response filter can be increased 10,000 times over the Z80A alone, while system complexity and power requirements increase no more than 15 percent.

In the future, as VLSI techniques develop, it can be expected that the sampling rates of electronically programmable transversal filters will increase, probably to the order of 10 to 15 MHz. However, to maintain a general-purpose architecture at the higher throughput rates, a number of new approaches will be required. For example, to achieve satisfactory charge transfer efficiency, ≥0.9995, buried channel CCDs, BCCDs, will be required. This rules out the use of the transversal output architecture since the nondestructive charge sensing techniques are nonlinear with BCCD structures; i.e., multibit weighting coefficient resolution could not be realized. Furthermore, it is unlikely that on-chip differential amplifiers could be designed to settle quickly enough at the higher sampling rates. The same is true of the circuitry used for the serial charge-to-voltage conversion. A more attractive approach is the programmable binary tree transversal input filter, since high-speed two-phase BCCDs can be used in conjunction with surface channel inputs for high linearity. The major disadvantage with this scheme is the increase in active area compared to the transversal output architecture. Higher speeds will undoubtly require some form of reverse CMOS process to reduce power dissipation. However, even with CMOS, it is unlikely that on-chip buffers will be feasible. Another problem area is signal acquisition at the output of the filter. Acquisition of the signal must take place within a maximum of half a clock cycle; at a 15 MHz sampling rate this is approximately 30 ns. To achieve this sampling rate, a sophisticated off-chip sample-and-hold circuit, or flash converter will be required. Both these approaches are expensive and will dramatically increase the power requirements of the system.

The realization of the next generation of general-purpose, electronically programmable transversal filters requires the solution of a number of complex and interrelated circuit problems. If these problems can be solved, the result will be a sophisticated analog signal processing system that for a number of applications will possess inherent advantages over an all digital VLSI approach.

SECTION V
REFERENCES

1. D.D. Buss, D.R. Collins, W.H. Bailey and C.R. Reeves, "Transversal Filtering Using Charge-Transfer Devices," *IEEE J. Solid-State Circuits*, Vol. SC-8 (April 1973), pp. 138—146.

2. R.D. Baertsch, W.E. Engeler, H.S. Goldberg, C.M. Puckette and J.J. Tiemann, "The Design and Operation of Practical Charge-Transfer Transversal Filters," *IEEE J. Solid-State Circuits*, Vol. SC-11 (February 1976), pp. 65—74.

3. R.W. Brodersen, C.R. Hewes and D.D. Buss, "A 500-Stage CCD Transversal Filter for Spectral Analysis," *IEEE J. Solid-State Circuits*, Vol. SC-11 (1976), p. 75.

4. C.R. Hewes, R.W. Brodersen and D.D. Buss, "Applications of CCD and Switched Capacitor Filter Technology," *Proc. IEEE*, Vol. 67 (October 1979), pp. 1403—1415.

5. P. Bosshart, "An Integrated Analog Correlator Using Charge-Coupled Devices," *Proc. IEEE ISSCC* (1976), pp. 198—199.

6. P.B. Denyer, J. Mavor and J.W. Arthur, "Miniature Programmable Transversal Filter Using CCD/MOS Technology," *Proc. IEEE*, Vol. 67 (December 1979), pp. 42—50.

7. J.J. Tiemann, W.E. Engeler, R.D. Baertsch, "A Surface-Charge Correlator," *IEEE J. Solid-State Circuits*, Vol. SC-9 (December 1974), pp. 403—409.

8. D.A. Gandolfo, J.R. Tower, J.I. Pridgen and S.C. Munroe, "Analog-Binary CCD Correlator: A VLSI Signal Processor," *IEEE, J. Solid-State Circuits*, Vol. SC-14 (April 1979), pp. 518—525.

9. E.G. Magill, D.M. Grieco, R.H. Dyck and P.C.Y. Chen, "Charge-Coupled Device Pseudo-Noise Matched Filter Design," *Proc. IEEE*, Vol. 67 (January 1979), pp. 50—60.

10. A.M. Chiang, B.E. Burke, D.L. Smythe, D.J. Silversmith and R.W. Mountain, "A High Speed CCD Digitally Programmable Transversal Filer," *Proc. Int. Conf. on CCD Applications*, CCD 1979 (Edinburgh, Scotland), pp. 230—235.

11. J.T. Caves, M.A. Copeland, C.F. Rahim and S.D. Rosenbaum, "Sampled Analog Filtering Using Switched Capacitors as Resistor Equivalents," *IEEE J. Solid-State Circuits*, Vol. SC-12 (December 1977), pp. 592—599.

12. B.J. Hosticka, R.W. Brodersen and P.R. Gray, "MOS Sampled Data Recursive Filters Using Switched Capacitor Integrators," *IEEE J. Solid-State Circuits*, Vol. SC-12 (1977), p. 600.

13. J.H. McClellan, T.W. Parks and L.R. Rabiner, "A Computer Program for Designing Optimum FIR Linear Phase Digital Filters," *IEEE Trans. Audio Electroacousitcs*, Vol. AU-21 (1973), pp. 506—526.

14. D.D. Buss and W.H. Bailey, "Applications of Charge Transfer Devices to Communication," *Proc. Int. Conf. on CCD Applications*, CCD 1973, p. 83—93.

APPENDIX A
OUTPUT VERSUS INPUT SIGNAL WEIGHTING

As was mentioned in Section I, input signal weighting is simpler to implement than output weighting, but suffers from a dynamic range limitation, which can be estimated as follows:

- With input weighting, the signals into the eight filters are weighted by factors of 1, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{32}$, $\frac{1}{64}$ and $\frac{1}{128}$.
- Compared with the signal in the MSB filter, the total signal into all eight filters is increased by a factor of $1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} \approx 2$.
- Assuming the noise in each filter is fixed, the noise power increases by a factor of 8 over that of the MSB filter.
- The signal increases by $20 \log_{10} 2 = 6$ dB, whereas the noise increases by $10 \log_{10} 8 = 9$ dB with the result that the dynamic range is degraded by 3 dB over that of a single filter. This is not particularly serious, but it represents a 12 dB degradation over the dynamic range that would be achieved with eight filters in parallel, all operating with unattenuated signal, because the dynamic range of eight filters in parallel is 9 dB greater than that of a single filter.

To avoid this dynamic range degradation, the analog signal should be applied unattenuated to the filter input, and the weighting should be after convolution. This would require eight DCIs, however. To have the flexibility of operating the device as a quad 256-stage by 1-bit filter or as a quad 128-stage by 2-bit filter, it is necessary to have four DCIs, but not eight.

The compromise architecture (Figure 2 of the Final Report) uses four DCIs by performing some weighting (X_1, X_2) ahead of the filters. This results in a dynamic range that is 0.5 dB greater than that of a single filter, but 2.5 dB less than the dynamic range that would result if the signal was applied unattenuated to all filters. The dynamic range degradation of the configuration of Figure 2 is not significant and does not justify the additional circuit complexity (eight DCIs instead of four) required to perform all the weighting on the output.

APPENDIX B
FILTER PIN-OUT AND OPERATING POTENTIALS

The filter chip is bonded in a ceramic 64-pin DIP and at 1 MHz dissipates approximately 1 W with the case temperature reaching approximately 40°C. All pins labeled N/C should be returned to either analog or digital ground (AG/DG), as shown in Table B-1. A total of five external bias levels are required; these should be decoupled at the device pins and made variable for maximum flexibility.

Table B-2 shows the various input and output signal connections as a function of the filter configuration. For example, if the device is in the dual 128-stage by 4-bit mode, one input signal is connected to pins 11 and 13 while the other signal is connected to pins 15 and 17. The output signal, corresponding to the two separate filters, appears on pins 44 and 42, respectively.

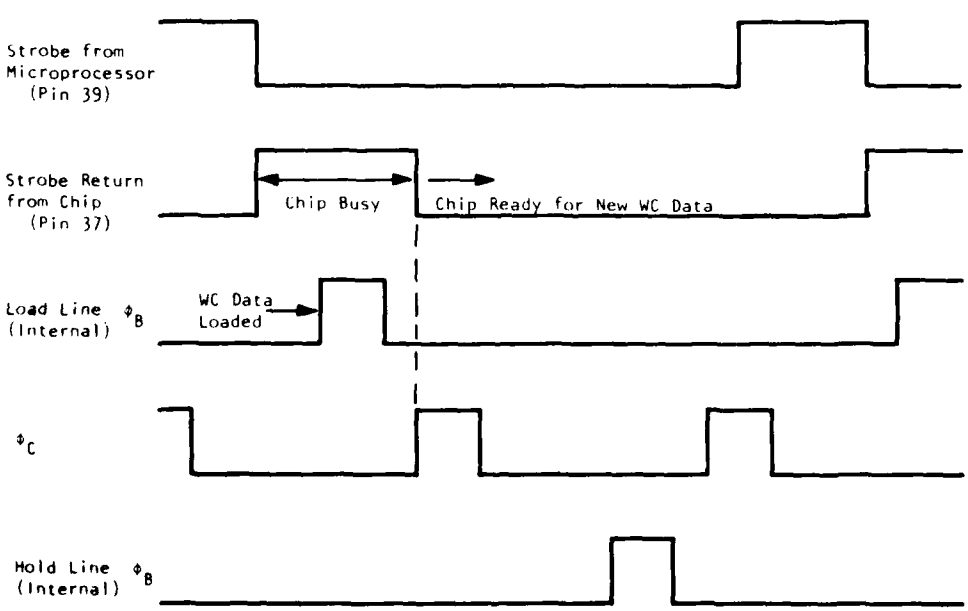


Figure B-1. Chip/Microprocessor Handshaking for Weighting Coefficient Data Loading

TABLE B-1. FILTER PIN-OUT AND OPERATING POTENTIALS

Pin	Function	Operating Voltage
1	Substrate bias	−5 V
2	Mode code, input D	0 ,+5 V
3	Mode code, input C	0 ,+5 V
4	Mode code, input B	0 ,+5 V
5	Mode code, input A	0 ,+5 V
6	Mode code latch strobe	0 ,+5 V[1]
7	N C	AG
8	N C	AG
9	Analog V_{DD}	+15 V
10	N C	AG
11	Analog input S1	0 ,+5 V on +5 V bias
12	N C	AG
13	Analog input S2	0 ,+5 V on +5 V bias
14	N C	AG
15	Analog input S3	0 ,+5 V on +5 V bias
16	N C	AG
17	Analog input S4	0 ,+5 V on +5 V bias
18	N C	AG
19	Flat zero level, V_{FZ}	0 ,+15 V, dc bias, ~12 V
20	N C	AG
21	V_{HOLD}	0 ,+15 V, dc bias, ~7 V
22	N C	AG
23	ϕ_3	0 ,+5 V, dc bias, ~2 V
24	N C	AG
25	ϕ'_3	0 ,+15 V, dc bias, ~13 V
26	N C	AG
27	Analog G_{SD}	O_V
28	N C	AG
29	Master clock	0 ,+5 V
30	N C	AG
31	Digital G_{SD}	O_V
32	ϕ_1 output	Clock output from chip, 0 ,+15 V
33	ϕ_2 output	Clock output from chip, 0 ,+15 V
34	ϕ_3 output	Clock output from chip, 0 ,+15 V
35	Digital V_{DD}	+15 V
36	N C	DG
37	Output strobe to microprocessor	0 ,+5 V output[2]
38	MOS to TTL interface V_{DD}	+5 V
39	Input strobe from microprocessor	0 ,+5 V input[2]
40	CCD 8 serial output	0 ,+4 V output on 7 V dc bias[3]
41	N C	AG
42	Filter B output	0 ,8V output on 7 V dc bias
43	N C	AG

TABLE B-1. FILTER PIN-OUT AND OPERATING POTENTIALS (Continued)

Pin	Function	Operating Voltage
44	Filter A output	0 -8V output on 7 V dc bias
45	N C	AG
46	CCD 8 serial output	0 -+4 V output on 7 V dc bias[3]
47	Digital reference code 1/P 8, LSB	0 -+5 V input[4]
48	Digital reference code 1/P 7	0 -+5 V input
49	Digital reference code 1/P 6	0 -+5 V input
50	N C	AG
51	Digital reference code 1/P 5	0 -+5 V input
52	Digital reference code 1/P 4	0 -+5 V input
53	Digital reference code 1/P 3	0 -+5 V input
54	N C	AG
55	Digital reference code 1/P 2	0 -+5 V input
56	N C	AG
57	Filter D output	0 -8 V output on 7 Vdc bias
58	N C	AG
59	Filter C output	0 -8 V output on 7 Vdc bias
60	N C	AG
61	Analog V_{DD}	+15 V
62	Analog G_{SD}	0 V
63	V_{REFI}	0 -+15 V, dc bias, ~7 V.
64	Digital reference code 1/P 1, MSB	0 -+5 V input.

[1] The filter includes latches for holding the mode code. For manual selection of the filter, mode pin 6 should be kept at +5 V. When using a microprocessor for mode control, the data on pins 2 to 5 must be valid until after the strobe pulse on pin 6 has gone low, 0 V.

[2] The on-chip microprocessor interface is triggered by a negative-going edge (5 -0 V) on the input, pin 39. As soon as this edge occurs, the return from the chip, pin 37, goes high, representing a busy signal. When this line returns to a low, the digital reference code present on pins 47, 48, 49, 51, 52, 53, 55 and 64 has been loaded into the shift registers. The chip microprocessor handshaking is shown in Figure B-1.

[3] The signals on pins 40 and 46 are the complementary serial outputs from the last two delay lines.

[4] The digital reference code is inverting. A code of 1 causes a long ϕ_2 pulse, corresponding to a weighting coefficient of 0. A code of 0 causes a short ϕ_2 pulse, corresponding to a weighting coefficient of 1.

TABLE B-2. INPUT AND OUTPUT SIGNAL CONNECTIONS AS A FUNCTION OF FILTER CONFIGURATION

	Analog Input Signal					Filter Output			
Signal Name	**S1**	**S2**	**S3**	**S4**		**A**	**B**	**C**	**D**
Pin Number	**11**	**13**	**15**	**17**		**44**	**42**	**59**	**57**
Filter Configuration					***Interconnect***				
1 × 1,024-stage by 1 bit	✓					S1			
1 × 512-stage by 2 bits	✓					S1			
1 × 256-stage by 4 bits	✓		✓		11 with 15	S1			
1 × 128-stage by 8 bits	✓	✓	✓	✓	All inputs	S1 to S4			
2 × 512-stage by 1 bit	✓		✓		11 and 15 are separate inputs	S1	S3		
2 × 256-stage by 2 bits	✓		✓			S1	S3		
2 × 128-stage by 4 bits	✓	✓	✓	✓	11 with 13, 15 with 17	S1 and S2	S3 and S4		
4 × 256-stage by 1 bit	✓	✓	✓	✓	All inputs separate	S3	S4	S1	S2
4 × 128-stage by 2 bits	✓	✓	✓	✓		S3	S4	S1	S2

APPENDIX C
EVALUATION CIRCUITRY

The evaluation circuitry comprises two boards, one analog the other digital, as shown in Figures C-1 and C-2, respectively. The test equipment can be operated in two different modes, either in a standalone mode or in conjunction with a minicomputer system. In the standalone mode, the filter can be operated in two configurations, 512 stages by 2 bits and 128 stages by 8 bits, with weighting coefficients loaded into the device from onboard EPROMs. When the circuitry is interfaced with a minicomputer, the device can be operated in all nine modes.

The analog circuitry of Figure C-1 consists of a network of switched unity gain buffers that provide analog input signal level shifting. The SD5000 FET switches SW1 to SW9 control the routing of the analog input signals to the chip (Table C-1) according to the mode of operation selected by panel switches or a microprocessor command. The outputs from the chip (A, B, C, D, CCD8', CCD8) are buffered by unity gain amplifiers Z12 to Z17. Switch ST1 in conjunction with SD5000 FET switches permits selection of a sampled and held version of any one of the A to D outputs. The sample-and-hold circuitry, located on the digital board, allows adjustment of the output dc level and the sample pulse width and position. In addition to the sample-and-hold circuitry, the digital board includes circuits for timing and synchronization, weighting coefficient loading, and binary sequence loading (Figure C-2). The clock generation circuitry consists of a one-shot, Z1, whose output is divided by 2; this is used as the chip master clock. A divided by 4 version of the master clock, locked to ϕ_H, is used to synchronize the binary sequence loading circuit.

A. STANDALONE OPERATION

To use the test circuitry in the standalone configuration, the mode of operation switch, ST3, should be set to internal and the filter select switches set to either the 128-stage by 8-bit mode or the 512-stage by 2-bit mode. The weighting coefficients for the appropriate filter configuration are loaded into the device from the EPROM, Z10, when the load button is depressed. The binary sequence data, used for the analog signal input in the 512-stage by 2-bit mode, is stored in the EPROM Z6, and is addressed as long as switch ST3 is in the internal position. This data is fed to the input of the filter via switch ST2. When the device is operated in the 128-stage by 8-bit mode, switch ST2 should be in the external position and a signal applied to any one of the analog inputs S1 to S4. The onboard EPROMs contain codes for a 128-stage by 8-bit narrow bandpass filter, as detailed in page 31 of this report, and a 511-stage M-sequence code for use in the 512-stage by 2-bit mode.

B. COMPUTER-CONTROLLED OPERATION

The test equipment can be interfaced with a computer by means of the connectors J1 and J2. J1 is connected to bits 0 to 7 and to the computer interrupt line, pin 5. J2 is connected to bits 8 to 15. These lines perform the following functions:

Bits 0 to 7, weighting coefficient data

Bits 0 to 3, filter mode select

Bits 0 to 9, binary sequence RAM address with bit 10 for the strobe

Bit 9, serial binary sequence data to RAM, Z11

Bit 10, load address command

Bit 12, write enable for RAM

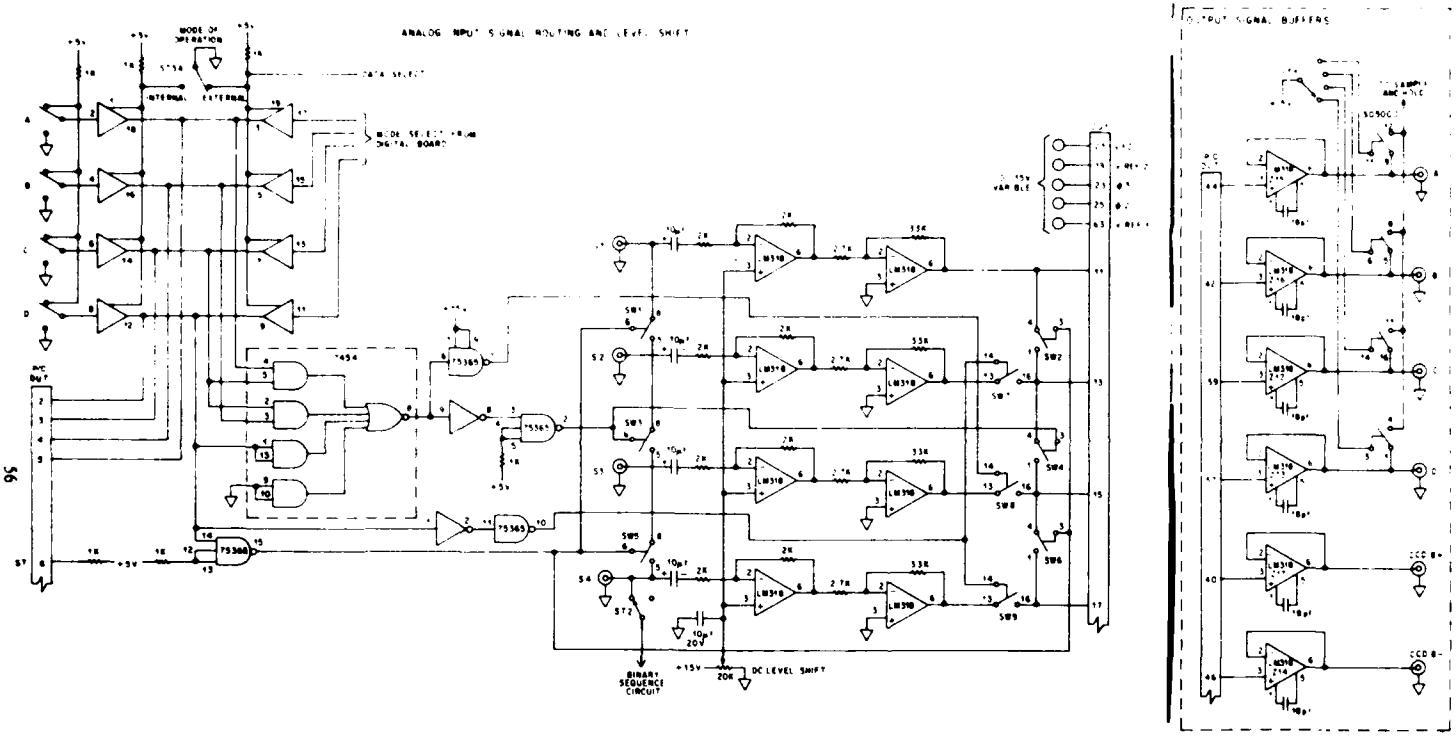


Figure C-1. Evaluation Circuitry-Analog Board

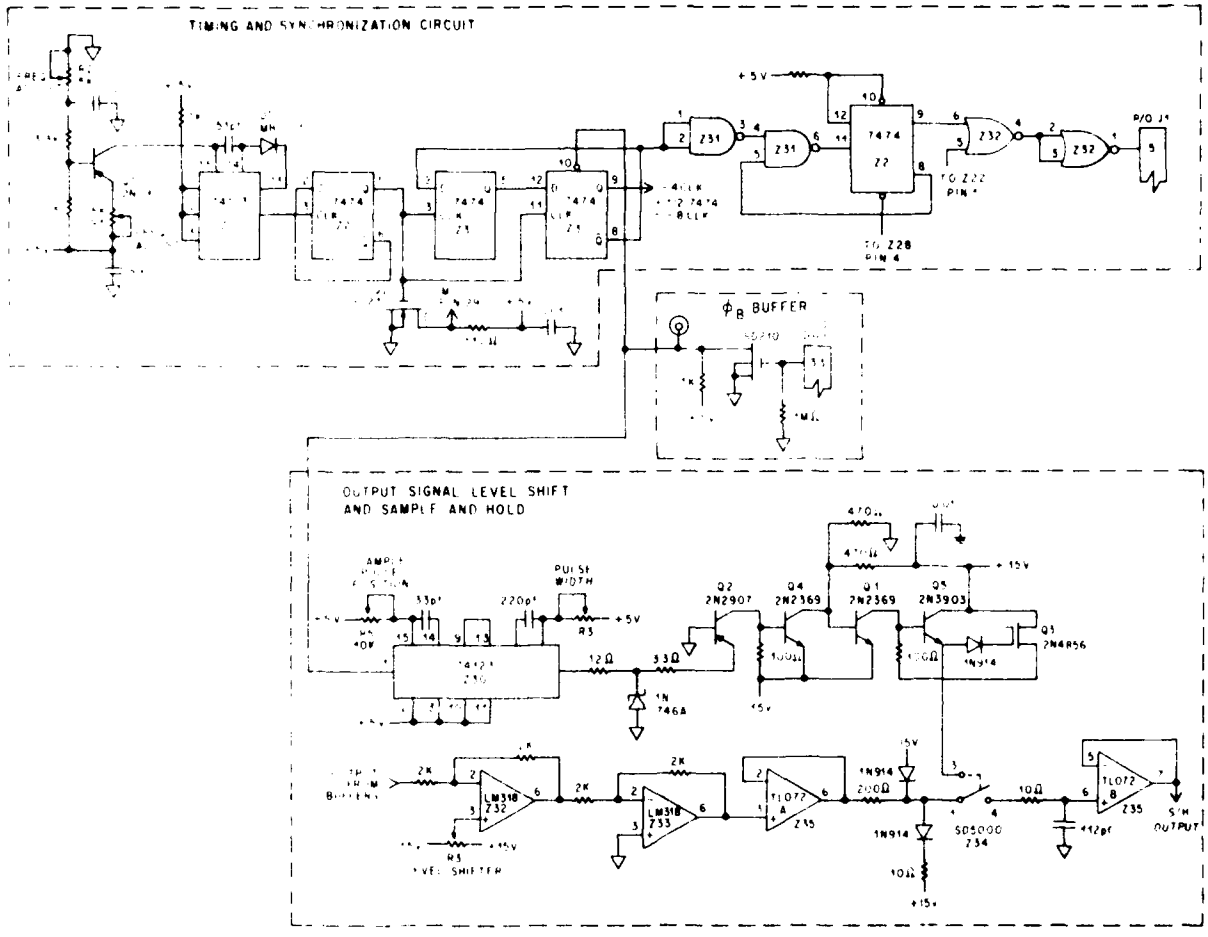


Figure C-2. Evaluation Circuitry-Digital Board

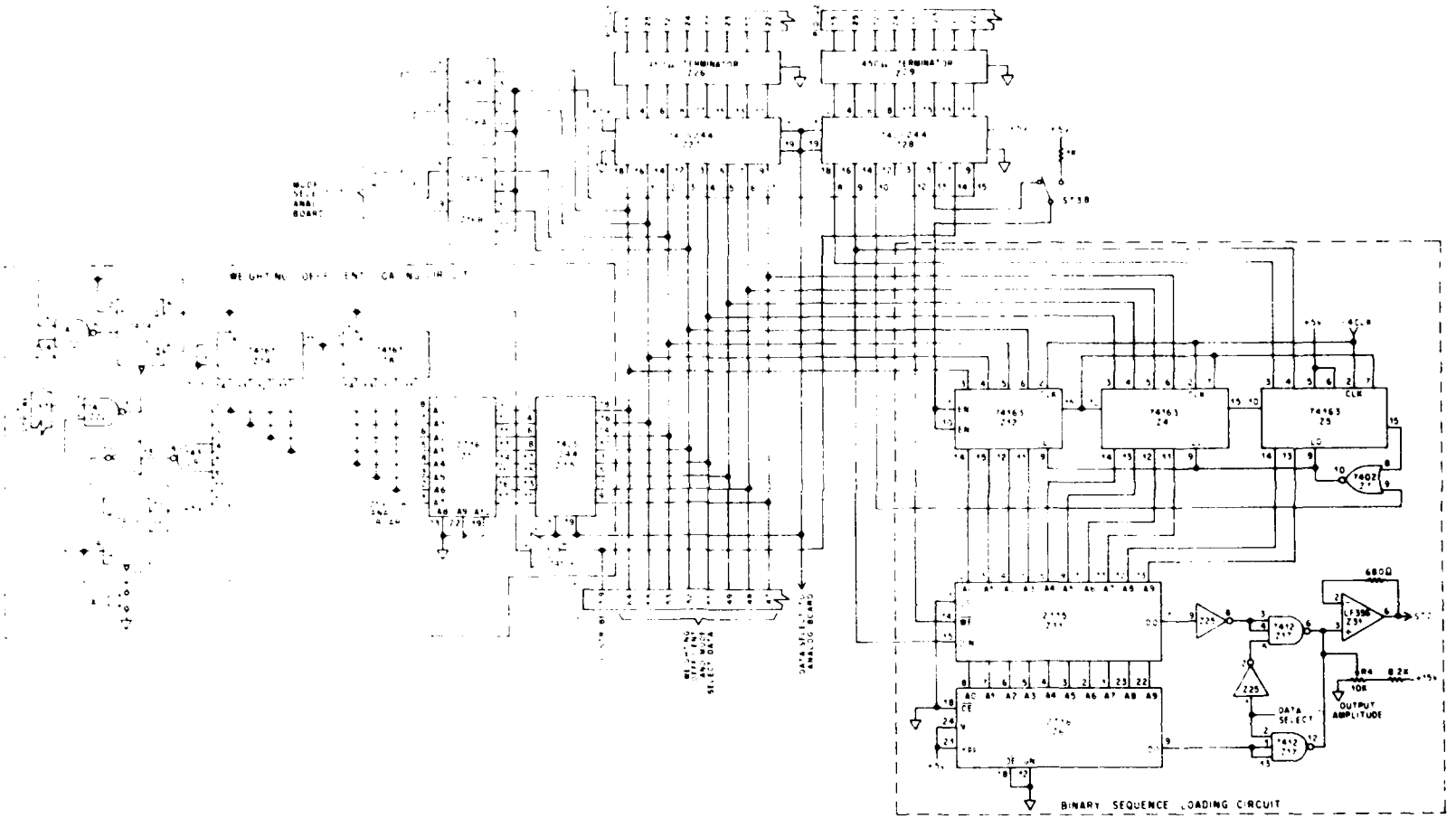


Figure C-2. Evaluation Circuitry-Digital Board

(Continued)

TABLE C-1. TRUTH TABLE FOR OFF-CHIP INPUT LOGIC

Filter Configuration	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
1 × 1,024-stage by 1 bit	1	D/C	1	D/C	1	D/C	0	0	0
1 × 512-stage by 2 bits	1	D/C	1	D/C	1	D/C	0	0	0
1 × 256-stage by 4 bits	1	1	1	1	1	1	0	0	0
1 × 128-stage by 8 bits	1	1	1	1	1	1	0	0	0
2 × 512-stage by 1 bit	1	D/C	0	0	1	D/C	0	1	0
2 × 256-stage by 2 bits	1	D/C	0	0	1	D/C	0	1	0
2 × 128-stage by 1 bit	1	1	0	0	1	1	0	1	0
4 × 256-stage by 1 bit	0	0	0	0	0	0	1	1	1
4 × 128-stage by 2 bits	0	0	0	0	0	0	1	1	1

1 = switch closed
0 = switch open
D/C = don't care

Bit 13, enable RAM address counter

Bit 14, input strobe to DUT

Bit 15, mode select strobe.

The following paragraphs detail the sequence of events for operating the test circuitry in conjunction with a computer.

1. Load Filter Mode Code

Set the mode data on bits 0 to 3 with bit 15 low. Strobe bit 15 high, then low. The positive transition of the strobe loads the data into the latches.

2. Load Weighting Coefficient Data

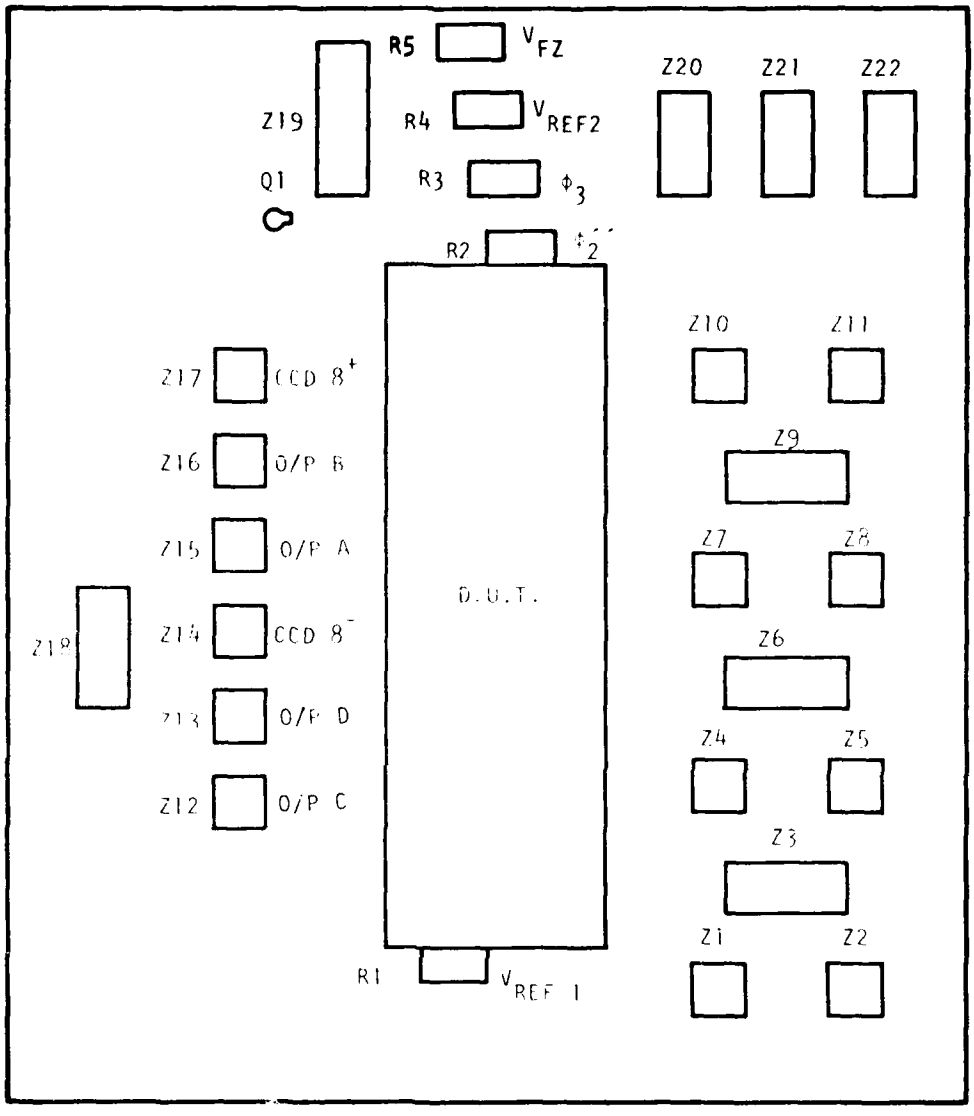
Set input strobe, bit 14, high and then place data on bits 0 to 7. Take input strobe low and monitor the interrupt line on pin 5 J1. When the line goes high, the DUT has recognized the data (Figure B-1); when the line returns to a low state, the DUT has accepted the data and is ready for the next word. This process repeats a total of 128 times.

3. Load Binary Sequence RAM

Set RAM address on bits 0 to 9 and set bit 10 high; this loads the data into the counter. Place the first data bit on bit 9 and then strobe bit 12 low and then back to a high. This loads the data bit on bit 9 into the RAM. This process is repeated until the binary sequence data is loaded. The binary sequence is read out continuously by setting bit 13 high. Note, the binary sequence RAM can only be used with the device operated in single-bit precision modes; i.e., 1,204 × 1 bit, dual 512 × 1 bit and quad 256 × 1 bit.

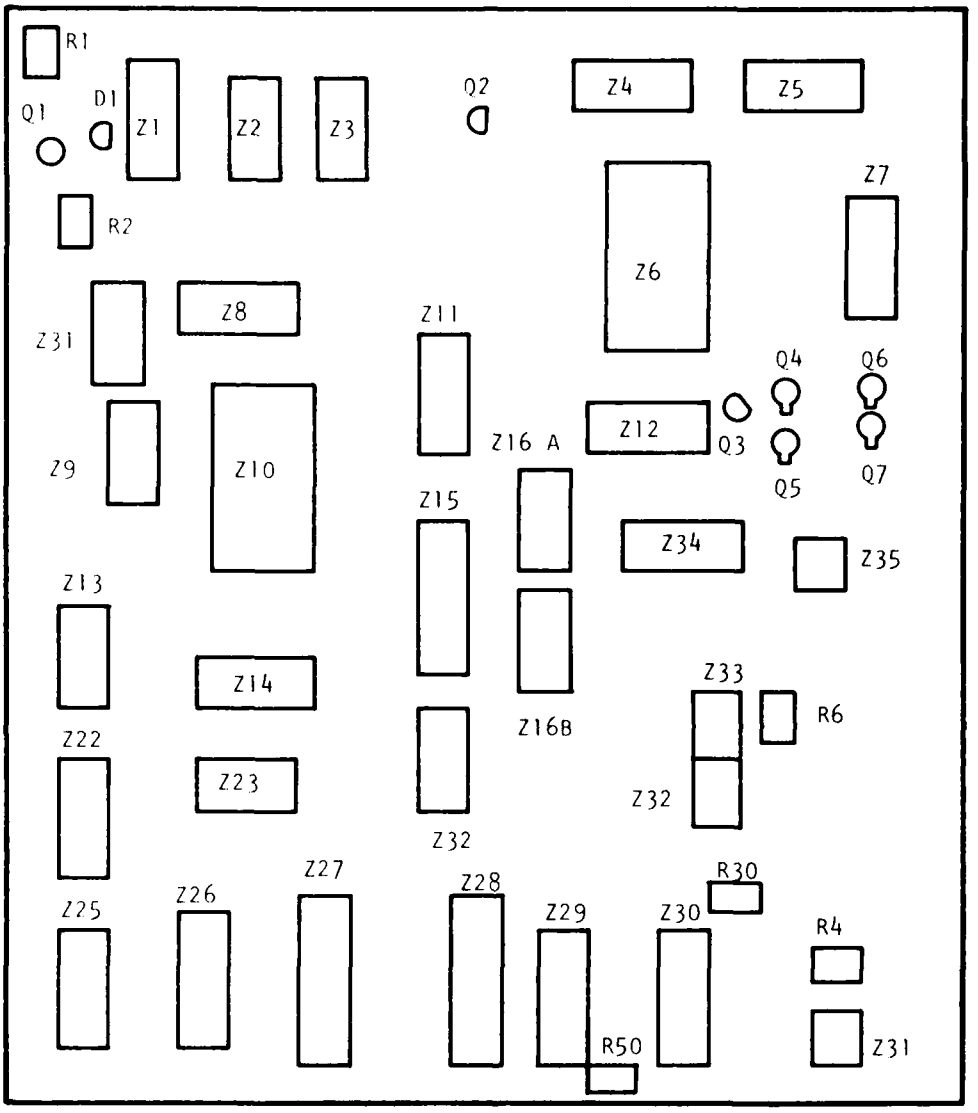
C. BOARD LAYOUTS AND POWER REQUIREMENTS

Figures C-3 and C-4 show the component layouts of the analog and digital boards, identifying the various dc bias level controls.



Z1, Z2, Z4, Z5, Z7
Z8, Z10, Z11, Z12, Z13
Z14, Z15, Z16, Z17 - LM318
Z3, Z6, Z9, Z18 - SD5000
Z19 - 74LS244
Z20 - 7454
Z21 - 7404
Z22 - 75365

Figure C-3. Analog Board Layout



Z1, Z24 - 74123
Z2, Z3, Z13 - 7474
Z4, Z5, Z8]- 74163
Z12, Z14]
Z6, Z10 - 2516
Z7 - 7402
Z9 - 7430
Z11 - 2115
Z15, Z27, Z28 - 74LS244
Z16 - 74174
Z17 - 7412
Z18 - LM318
Z22 - 7400
Z23 - 74126
Z25 - 7404
Z26, Z29 - 470 Ω Resistor PAC
Z30 - 74123
Z31 - LF356
Z32, Z33 - LM318

Figure C-4. Digital Board Layout

The test equipment requires the following power supplies.

+15 V, 100 mA, filter analog circuitry

+15 V, 100 mA, filter digital circuitry

+15 V, 200 mA, test box circuitry

−15 V, 200 mA, test box circuitry

+5 V, 900 mA, test box circuitry

−5 V, 100 mA, filter circuitry.

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