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PRACTICAL STUDY OF SILICON MICROWAVE TRANSISTORS.(U)
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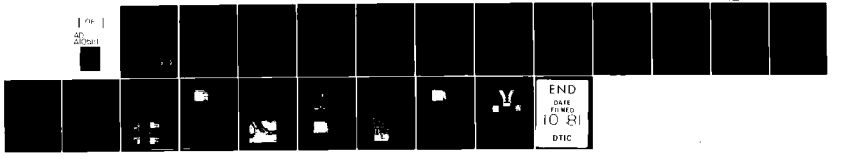

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FINAL REPORT

PRACTICAL STUDY OF SILICON MICROWAVE TRANSISTORS

N00173-78-C-0435

May 15, 1978 - October 31, 1979

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I. INTRODUCTION

The objective of the work performed under this grant was to study the technology and usefulness of silicon-on-sapphire material for fabrication of Schottky-barrier field-effect transistors suitable for use in the lower microwave frequency range.

During the grant period, three technologies for the fabrication of SOS MESFET's (SOSFET's) and their integration in microwave subsystems were developed. Work is continuing on the most promising of these technologies. Each technology was found to have a singular advantage in either fabrication simplicity, potential for large drain-gate breakdown voltage (and therefore for high power devices) or maximum operating frequency. All technologies developed are based on standard silicon IC processing techniques, making use of self-alignment and lateral diffusion to reduce demands on photolithography, and allow for easy integration of standard microwave IC lumped elements on insulating substrates.

This work was stimulated by a theoretical prediction of good microwave performance by these devices (1) and by the evolving need for large quantities of very low-cost transmit/receive modules operating in the lower microwave frequency range for such systems as strategic and tactical phased array radars.

II. PROCESSING TECHNOLOGY

Three means of fabricating SOSFET's were explored:

i) A three-mask short-channel process on thinned SOS doped during growth to 1E17 donors/cm^3

ii) A recessed-gate process using an ion-implanted channel.

iii) A planar process using an ion-implanted channel that exploits lateral diffusion to achieve short channel lengths.

i) Uniformly Doped SOS Process. This process is simple enough to allow anyone with relatively simple facilities to make MESFET's with reasonably good electrical characteristics. An outline of the process for this device is given in Figure 1. The starting material was 300nm thick (100) silicon doped during growth with phosphorus to a level of 5-10E16/cm^3. This material was supplied by the Union Carbide Co., Electronic Materials Division. The silicon was thinned to 200nm by briefly etching in a solution of nitric acid:acetic acid: HF::90:7:3. Undiluted Az1350J positive photoresist was spun on to a thickness of 1.6 microns and the image of the MESA mask was projected onto the wafer using a Kasper 10:1 reduction aligner, although contact alignment also is feasible. After etching the mesa with the same solution as that used for thinning, the 1 micron x 200 micron by 250 nm thick aluminum GATE was defined using liftoff. The gate was sintered in H_2 at 500C for 7 minutes. Finally, AuSb ohmic

source and drain CONTACTS, separated by 5 microns, were defined, again using liftoff. A final sinter was done in H_2 at 280C for 7 minutes; this low temperature was necessary to avoid gold ball-up.

Figure 2 shows the general layout of all of the MESFET's to be discussed. The DC drain characteristics of the uniformly doped SOS device are shown in Fig. 3 for 100 micron gate width (i.e., single gate operation). The observed transconductance was 42 ms/cm at V_g = 0V, V_{ds} = 5V and the observed pinchoff voltage was -3.0V. The reverse bias gate leakage at -12V was 10 microamperes; forward bias current as 400 mV was also 10 microamperes. The gate capacitance C_{gs} of this device was calculated(2) to be approximately .075pf which results in a cutoff frequency $f_t = g_m/2\ C_{gs}$ = 900MHz. This value of f_t is considerably lower than that predicted by an exact two-dimensional device simulation for a one micron gate device (1). The discrepancy is attributable to the large source-drain spacing, which led to large source and drain parasitic resistances, and to a relatively small low-field mobility (about 250 cm^2/V-sec) in the thin SOS layer, which led to a low transconductance.

ii) Recessed Channel SOS Process. This four-mask process was developed to explore technologies to increase drain breakdown voltage for power devices; and to reduce channel impact ionization for low-noise devices. An outline of the technology for this process is shown in Figure 4. The channel was formed

by implantation into a 500nm layer of intrinsic SOS. The implant profile kept the electron transport away from both the silicon surface and silicon:sapphire interface. 150nm of undoped SiO_x film (Silicafilm) was spun on the SOS at 3000 rpm and densified for 15 minutes at 750C in nitrogen. A source and drain DIFFUSION photolithography step opened windows in the oxide after which 100nm of phosphorus-doped (C_o=5E20/cm^3) glass was spun on the wafer. The diffusion was done at 900C for 10 minutes in nitrogen. A SIMS analysis of the diffusion profile is compared to a SUPREM simulation for bulk silicon in Figure 5. The measured phosphorus profile imples that the diffusion coefficient is much larger in SOS than in bulk silicon; in addition, this coefficient varies markedly with depth. The effective source-drain spacing, after diffusion, was about four microns. After the diffusion, the oxide was etched off the wafer. The channel RECESS mask image was then exposed in photoresist that had been dipped in toluene for two minutes prior to development. The toluene hardens the surface of the resist, resulting in sharper lift-off edges, as will be explained below.

The wafer was then ion milled in argon at 500V accelerator potential for 8 minutes to give a 150nm recess in the silicon. 60nm of wet oxide was grown over the entire surface after the photoresist had been stripped, to both remove the milling damage and keep the channel surface clean during the following step.

The oxide over the milled region turned out about 16nm thicker than that over the intrinsic silicon. It should be noted that it was not possible to form a good Schottky barrier gate on untreated ion-milled silicon as the milling introduced a large density of surface states which prevented the channel from being totally depleted before reverse-bias breakdown.

The phosphorus channel implant was performed at 160KeV with a dose of 1.5E12/cm^2 followed by an activation anneal at 750C for 30 minutes. Figure 5 also shows the implanted channel profile as predicted by SUPREM. A MESA photolithography and etch step defined an oxide mask against anisotropic silicon etching in 85% hydrazine at 70C for about 4 minutes. After the oxide was removed, the source, drain and gate aluminum METALLISATION was defined by lift off. The wafer was sintered at 500C for 7 minutes in hydorgen. A micrograph of the finished device is shown in Figure 6.

During development of this device the lift-off technique for the Al gate was improved by a two-minute dip of the exposed but undeveloped photoresist (Shipley AZ1350J) in toluene. Figure 7 shows gate images in AZ1350J both without (a) and with (b) a two-minute dip in toluene prior to development. The image in resist that was soaked prior to development has a sharper edge near the resist surface, giving a clean lift off. The resultant gate length, however, is larger than that obtained when no soaking occurs.

Figure 8 shows the drain characteristics of the recessed channel transistor. The g_m at V_g = 0V, V_{ds} = 5V was 130 mS/cm

and, with no parasitic source-drain leakage, the pinch off voltage would be -1.5V. The f_t was calculated to be about 2.7GHz.

The increased process complexity of the recessed channel device may not be necessary in all cases. Therefore, an ion-implanted/diffused planar process was developed.

iii) Planar SOS Process. This three mask process yielded the best observed g_m of the three processes described. An outline of the process used for this device is shown in Figure 9. Undoped SiO_x was spun on the wafer, after which the source and drain DIFFUSION windows were opened in the oxide using ion milling to preserve the required source-drain spacing. Doping of the source and drain was done at 900C for 10 minutes using spun on phosphorus doped SiO_x. The SiO_x was then removed and 60 nm of wet oxide was grown at 900C. A phosphorus channel implant (same parameters as in ii) was followed by an activation anneal. The MESA was then ion milled with a photoresist mask produced by defocussing the image projected onto the photoresist; the slopes of the developed photoresist edges could be varied by varying the degree of defocus. The photoresist edge was transferred to the mesa by a 16 minute ion mill at 500V accelerator potential. The source, gain and drain METALLISATION was defined using lift-off of aluminum and the wafer was then sintered at 500C for 7 minutes.

A gate length of 700 nm was achieved using lift-off of 250 nm of aluminum and 1.6 micron of AZ1350J photoresist.

The exposure time of the projection aligner was adjusted such that after development, the gate length at the surface of the photoresist was 600nm to 700 nm at the silicon surface, although it was 1.2 microns at the photoresist surface. It was noticed that for a 15 minute sinter at 500C in hydrogen there was appreciable diffusion of silicon into the aluminum. This phenomenon, which is correctable by proper pad spacing, is shown in Figure 10 where the large area gate pad forms a sink for silicon atoms.

The drain characteristics of the planar-process transistor is shown in Figure 11. The g_m for the planar MESFET was 230 mS/cm giving a calculated f_t of almost 5 GHz. The pinch-off voltage was -3.85V.

III. SUMMARY OF RESULTS

Device results obtained are summarized in Figure 12. We have not yet achieved the results predicted by CUPID, perhaps because of the following differences between our devices and those simulated:

1) The intrinsic SOS regions below our devices (ii) was not perfectly insulating.
2) Our device channels (ii and iii) were not uniformly doped.
3) Most important, the total source-drain distances in our devices were larger than those in the simulation.

IV. ADDITIONAL TECHNOLOGICAL POINTS

1) Effect of mesa on gate width. The Al gate was found to neck down at the point where it crossed the mesa edge, as a result of the combination of edge and proximity of source and drain patterns.

This effect was often serious enough to cause open gates. Several phenomena were identified with these problems, and were corrected.

(a) After development it appeared from an optical microscope examination that the photoresist had excessively necked down. However, a SEM examination of the same region revealed that the necking down was less severe indicating some form of shadowing in the critical region when the photoresist was viewed using the optical microscope.

(b) Edge diffraction - it was thought that the sharp transition from gate to gate pad diffracted light near that point. However, necking down was seen even when that region is enlarged smoothly.

(c) When the SD contacts (which are on the same mask as the G metal) are terminated such that the gate electrode must run for several μm without being close to the SD areas, problems were experienced with the gate thinning down outside the region of SD area influence. In order to improve the uniformity of the interaction between the SD areas and the gate during exposure, an asymmetrical SGD pattern was developed. This pattern also had a very gradual transition from gate metal to gate pad.

(i) Excessive lateral diffusion occasionally resulted in gate-drain and gate-source short circuits. It was found that the effective lateral diffusion of phosphorus after 15 min at 940°C was around 0.8 to 1.0 μm and the sheet resistivity was 23 $\Omega\square^{-1}$. The diffusion temperature was decreased to 875°C giving a sheet resistance ranging from 80 - 120$\Omega\square^{-1}$ and an effective lateral diffusion of 0.3 - 0.5 μm.

We have also used ion implanted source and drain contacts to reduce the lateral diffusion problem. Phosphorus was implanted at 80 keV into 500 Å oxide covered SOS with a dose of 1.5 to 5.0 x 10^{15} cm^{-2}.

(i) Mask rotation and alignment errors. The original pattern of Figure 2 was sensitive to small rotational misalignment or to lateral misalignment which would result in the gate between S_1 and D being closer to the source (for example) i.e., offset gate in favorable direction; but in this case the gate between S_2 and D would then be closer to the drain where the offset is very unfavorable.

This unsatisfactory situation has been solved by using the transistor topology shown in Figure 13, where any misalignment has the same effect on the gate relative to both sources and drains. However, the rotational problem in Fig.13 is more severe, i.e., the rotational error between the diffusion mask and the metal mask needs to be less, than in Fig. 2. Elimination of rotational error has been achieved by using the shift mask principle in which the diffusion and the metal masks are combined. In this situation, the whole pattern of Fig. 13 is diffused into the SOS. A MESA mask then selects the wanted diffused silicon, the rest being etched away. The original mask used in the selective diffusion is now moved up a distance Δ with respect to its original position so that the gate lies between the diffused SD regions, and the photoresist is exposed. As the same mask is used for both diffusion and metallization, rotation error can be drastically reduced and only two plates are now needed to make the SOS MESFETs. It has also been possible, using an extension of the shift mask idea, to use only 2 plates to make transistors whose SD spacing can be chosen to be 3, 4 or 5 μm depending only on the amount of shift.

The new transistor structure is relatively insensitive to both photomask preparation errors (eg, rotation in the step and repeat) and to processing linear misalignment. Rotational misalignment between diffusion and metal images has been reduced to a negligible proportions. In addition, the overall topology is more versatile and allows several different transistors to be made from the same mask set, which itself consists of only 2 plates.

V. EXTENSIONS OF THIS WORK

Work is currently under way on:

1) Platinum metallisation - gold will be deposited on platinum in contact pad areas for gold wire bonding.

2) SOSFET with V_T = 2.0V, with drain gate breakdown voltage of 7.5V with either Al or P_t gate.

3) MESFET on laser annealed poly Si uniformly doped to 5×10^{16} cm^{-3}, 5000 Å thick.

4) Comparison between diffused and implanted source and drain regions with respect to contact resistance, sideways diffusion and oxide masking.

5) Consideration of processing steps to be used with electron-beam-fabricated MESFETs.

VI. CONCLUSIONS

Several technologies have been used for the fabrication of SOS MESFET's for use in the lower microwave frequency ranges. These technologies result in devices with performance suitable for many applications in this range, and can benefit from the body of experience acquired in the mass-production of lower-frequency integrated circuits. The sapphire substrate upon which these devices are constructed is an ideal low-loss medium for the support of microstrip or coplanar lines for distributed circuits, and is an equally good medium for the support of lumped elements, e.g., loop inductors and interdigitated or MOM capacitors.

The relative cheapness of the SOS material compared to that, say, of epitaxial GaAs on semi-insulating substrates, should be considered when evolving IC's for use in the lower microwave frequency range. Many of the benefits of GaAs for microwave IC's lie with the availability of such a substrate, but the advantage is not exclusively to GaAs once the availability of sapphire, or other insulating materials upon which Si can be grown or deposited (e.g., SiO_2) is recognized.

VII. ADDITIONAL INFORMATION

1) A paper was presented describing our work on uniformly doped SOSFET's at the SiMESFET Workshop, Boulder, CO, June 1979.

2) A paper was presented describing our work on planar-process SOSFET's at the International Electron Devices Meeting, Washington, DC, Dec. 1979.

3) During the course of this contract two trips were made to Naval Research Laboratory, Washington, DC, for technical discussions.

REFERENCES

(1) T. Wada and Jeffrey Frey, "Physical Basis of Short-Channel MESFET Operation", IEEE Trans. ED-26, 476 (1979).

(2) R.A. Pucel, et al., "Signal and Noise Properties of Gallium Arsenide Microwave Field-Effect Transistors", Advances in Electron. Electron Phys. 38, 195 (1975).

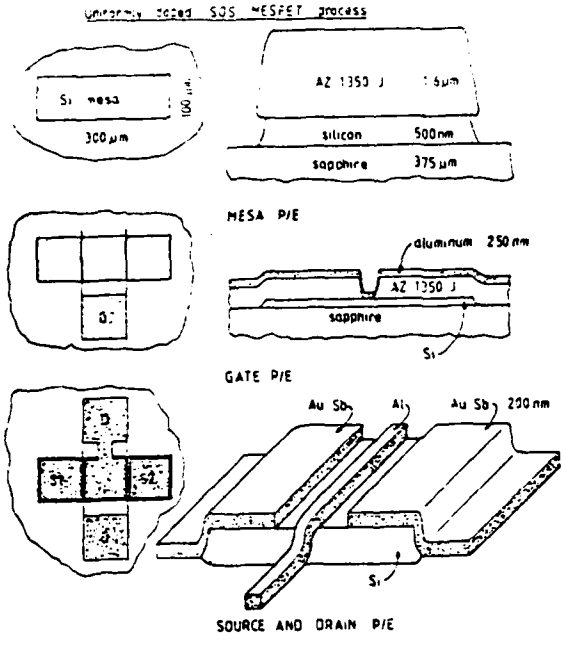


Fig. 1. Outline of of uniformly doped SOSFET process.

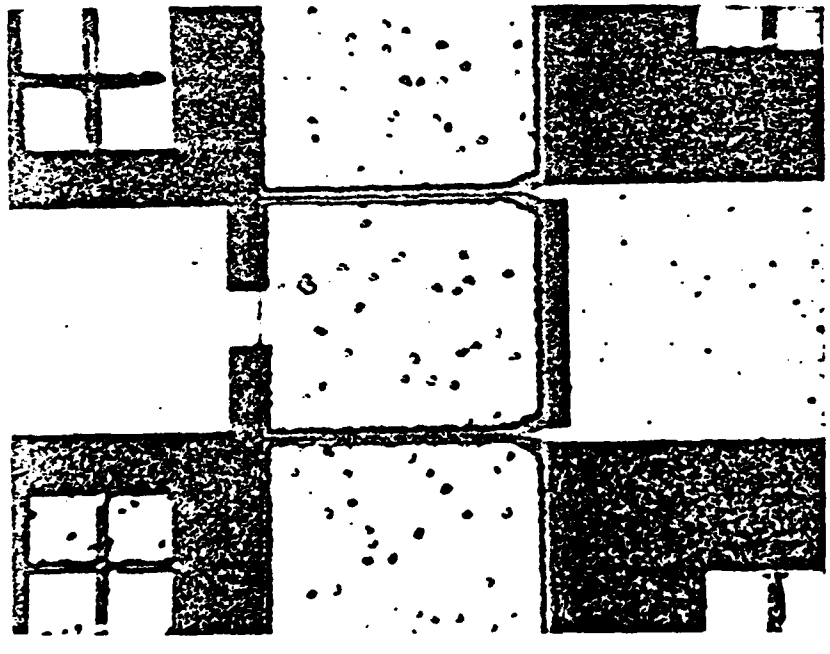


Fig. 2. General lay-out of all the MESFETs discussed.

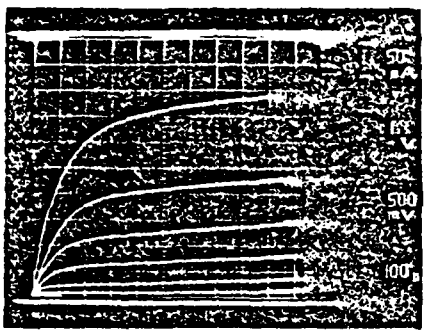


Fig. 3. D.C. drain characteristics for uniformly doped-process FET.

D.C. DRAIN CHARACTERISTICS FOR UNIFORMLY DOPED-PROCESS FET.

- G_M = 42mS cm^{-1} AT V_G = 0V, V_{DS} = 5V.
- PINCH OFF VOLTAGE = - 3.0V.
- F_T PREDICTED = 900 MHz.

Recessed channel SOS MESFET

- source and drain DIFFUSION 900°C 15mn $C_0 = 3E20cm^{-3}$
- CHANNEL RECESS ion mill in argon 200 nm
- channel implant 1,5E12cm^{-3} phosphorus at 150KeV
- MESA P/E using anisotropic etchant
- METALLISATION 250nm Al

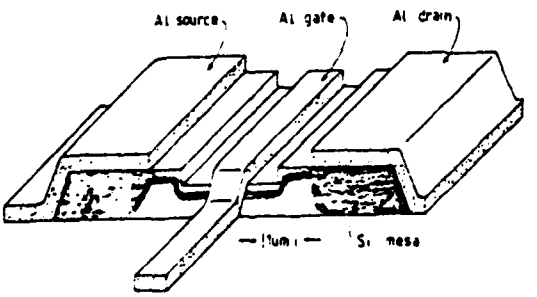
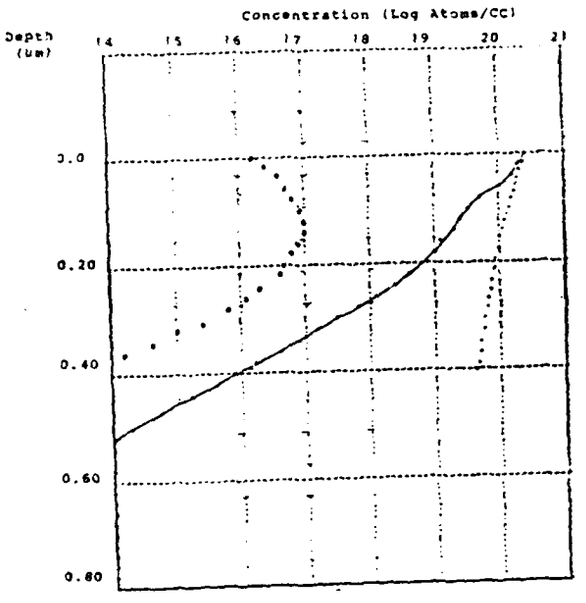


Fig. 4. Recessed-channel FET.



DOPANT CONCENTRATION PROFILES

Fig. 5. Source-Drain Diffusion Profile.

solid line = SUPREM simulation

small dots = SIMS measurement

(Large Dots = SUPREM simulation of channel implant)

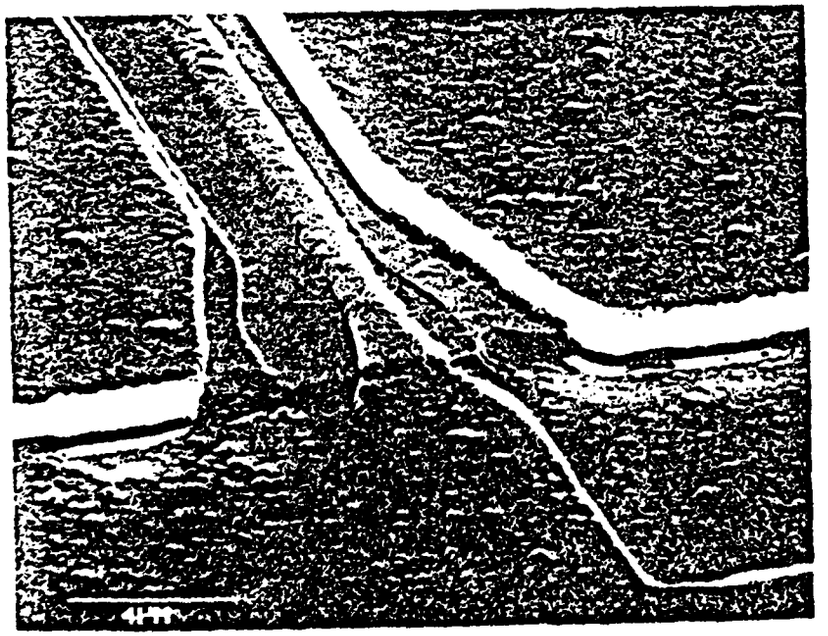
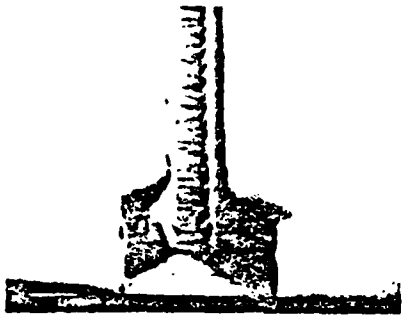
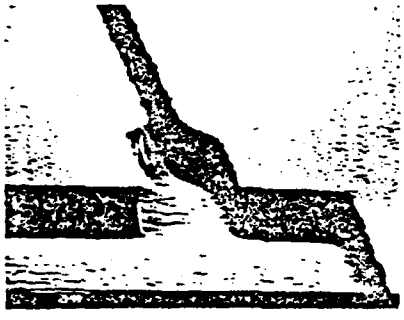


Fig. 6. Recessed channel SOS MESFET.

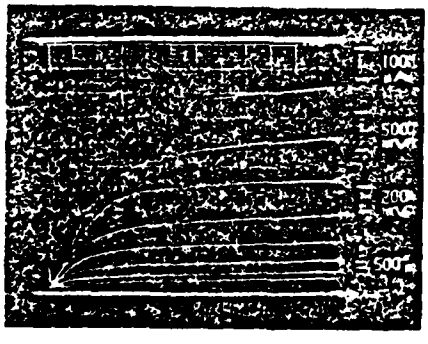


DEVELOPED GATE PATTERN IN AZ1350J



AS ABOVE BUT WITH A 2 MINUTE DIP IN TOLUENE PRIOR TO DEVELOPMENT.

Fig. 7. (a) Developed Gate Pattern in AZ1350J; (b) As above but with a 2 minute dip in toluene prior to development.



D. C. DRAIN CHARACTERISTICS FOR RECESSED-CHANNEL-PROCESS FET.

- g_m = 130 mS/m AT V_G = 0V, V_{DS} = 5V.
- PINCH OFF VOLTAGE = - 1.5V
- f_T PREDICTED = 2.7 GHz.

Fig. 8. D.C. drain characteristics for recessed-channel-process FET.

Planar SOS MESFET

- o source and drain DIFFUSION or high dose IMPLANT
- o MESA ion milled in argon at 500V 500nm
- o channel implant $1.5E12cm^{-2}$ phosphorus at 120 to 160Kev
- o METALLISATION 250nm Al [illegible] gate

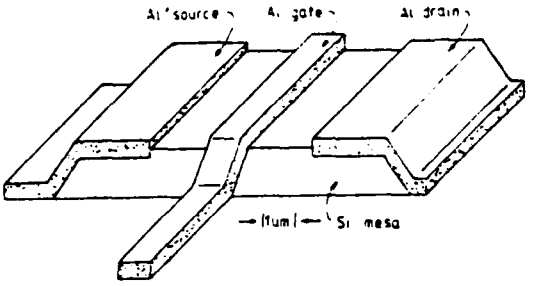
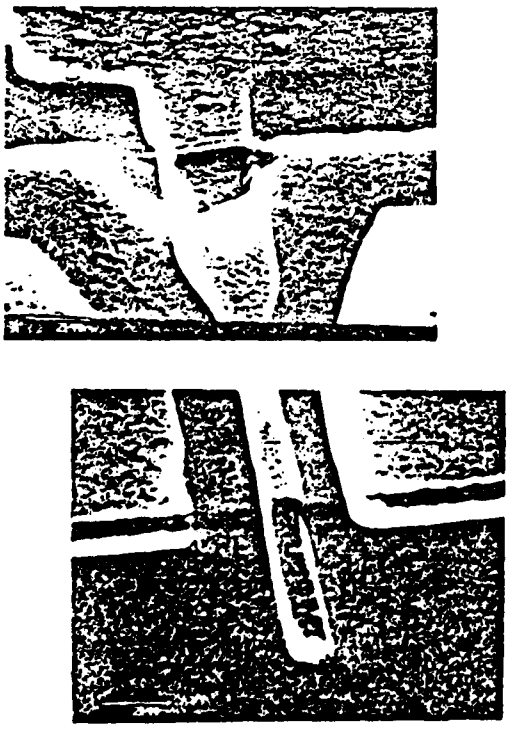


Fig. 9. Planar SOS MESFET.



Diffusion of silicon into aluminum

Fig. 10. Diffusion of silicon into aluminum.

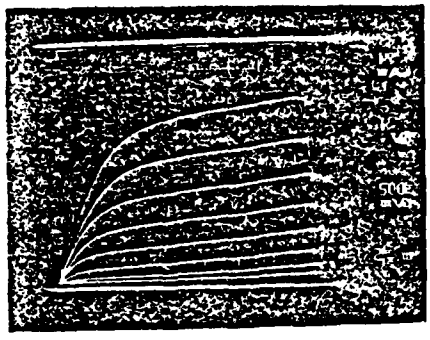


Fig. 11. D.C. drain characteristics for planar-process FET.

D.C. DRAIN CHARACTERISTICS FOR PLANAR-PROCESS-FET

- G_M = 230 mS/cm AT V_G = 0V, V_{DS} = 5V.
- PINCH OFF VOLTAGE = - 3.8V.
- F_T PREDICTED = 4.3 GHz.

SUMMARY

D.C. RESULTS FOR SOS MESFET

	V_P	G_M PER CM GATE WIDTH	PREDICTED F_T
UNIFORMLY DOPED	-3.0 V	42 mS	900 MHz
RECESSED CHANNEL	-1.5 V	130 mS	2.7 GHz
PLANAR	-3.8 V	230 mS	4.8 GHz
CUPID SIMULATION		315 mS	6.2 GHz

Fig. 12. D.C. results for SOS MESFET.

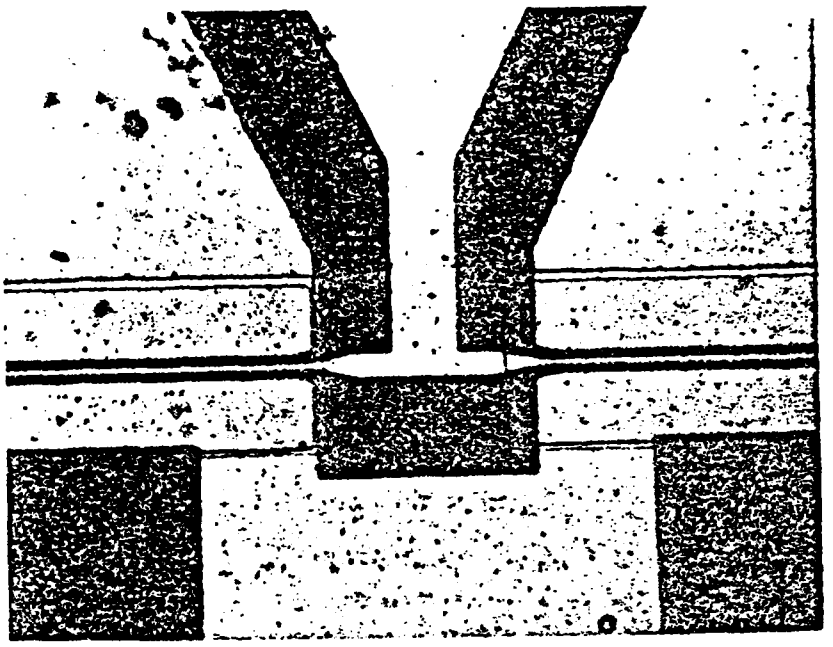
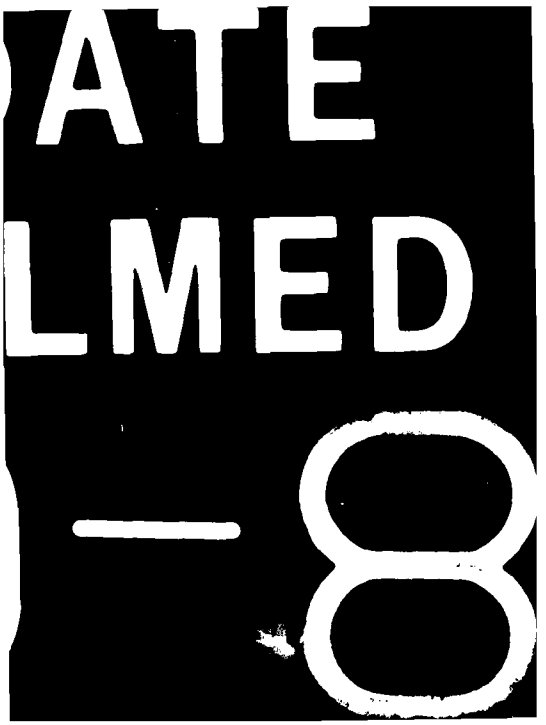


Fig. 13. New improved transistor topology.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