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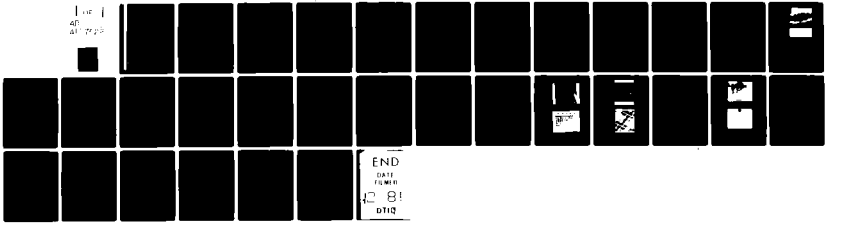

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INTEGRATED BALANCED FETs FOR BROADBAND MILLIMETER WAVE AMPLIFIERS

FINAL REPORT

August 1981

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by

S. Bandy, C. Nishimoto, P. Stonestrom, Y. Chai and C. Hooper

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Using electron-beam exposure and MBE GaAs, balanced FETs were designed and fabricated. While the devices exhibited excellent dc characteristics, their single-sided rf performance was not up to expectations, for reasons yet to be determined. This report is an interim account of a program being continued under a different contract number (N00014-81-C-0270).

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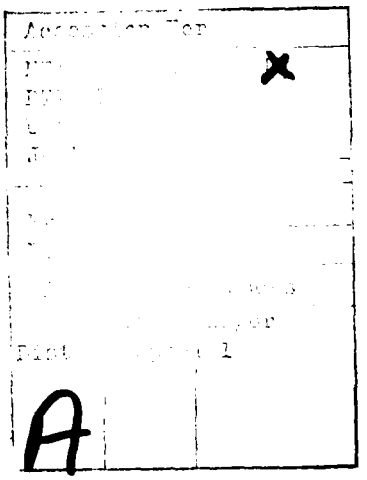
FOREWORD

The work reported here was supported by the Office of Naval Research, Washington, DC, under Contract No. N00014-80-C-0391 and managed by Mr. Max Yoder. The program was aimed at developing GaAs FETs with improved rf performance by using a balanced push-pull design.

The work was carried out in the Varian Corporate Research Solid State Laboratory. The authors wish to thank M. Pustorino and S. Lombardi for technical assistance. Valuable discussions with M. Yoder and R. L. Bell are gratefully acknowledged.



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I. INTRODUCTION

The high-frequency performance of microwave FETs is determined not only by transit time effects, but by parasitic resistive and reactive elements. In particular, parasitic source resistance has a degenerative effect on gain, as well as degrading noise figure. Reactive elements give rise to resonances in the gain/frequency curves which can be useful for peaking the gain at particular frequencies, but basically lead to narrow band performance. Beyond the peak, gain falls off more rapidly than the basic 6-dB/octave of the basic FET, deteriorating the gain significantly at the very highest frequencies. In addition, these extra resonances may make it difficult for the circuit designer to realize broadband performance in practical FET amplifiers. Such effects are observed as a result of source inductance and gate/drain (feedback) capacitance. These elements can be used to peak the gain at some intermediate but usually uncontrolled frequency. However, beyond the peak, the gain falls more rapidly than in their absence.

From these points of view, it is desirable to eliminate such parasitics. If needed for particular peaking functions, they can be reintroduced in a less expensive and more controllable manner by lithographic methods on the chip.

These requirements suggest the use of integrated push-pull pairs of FETs with common source electrodes, shown schematically in Fig. 1, which have the following advantages for very high-frequency operation:

(1) virtual elimination of source lead inductance for the fundamental component of the signal,

(2) some reduction in effective source resistance. A very large effect here will generally not be feasible, since the fundamental current exchanged between the two halves of the pair

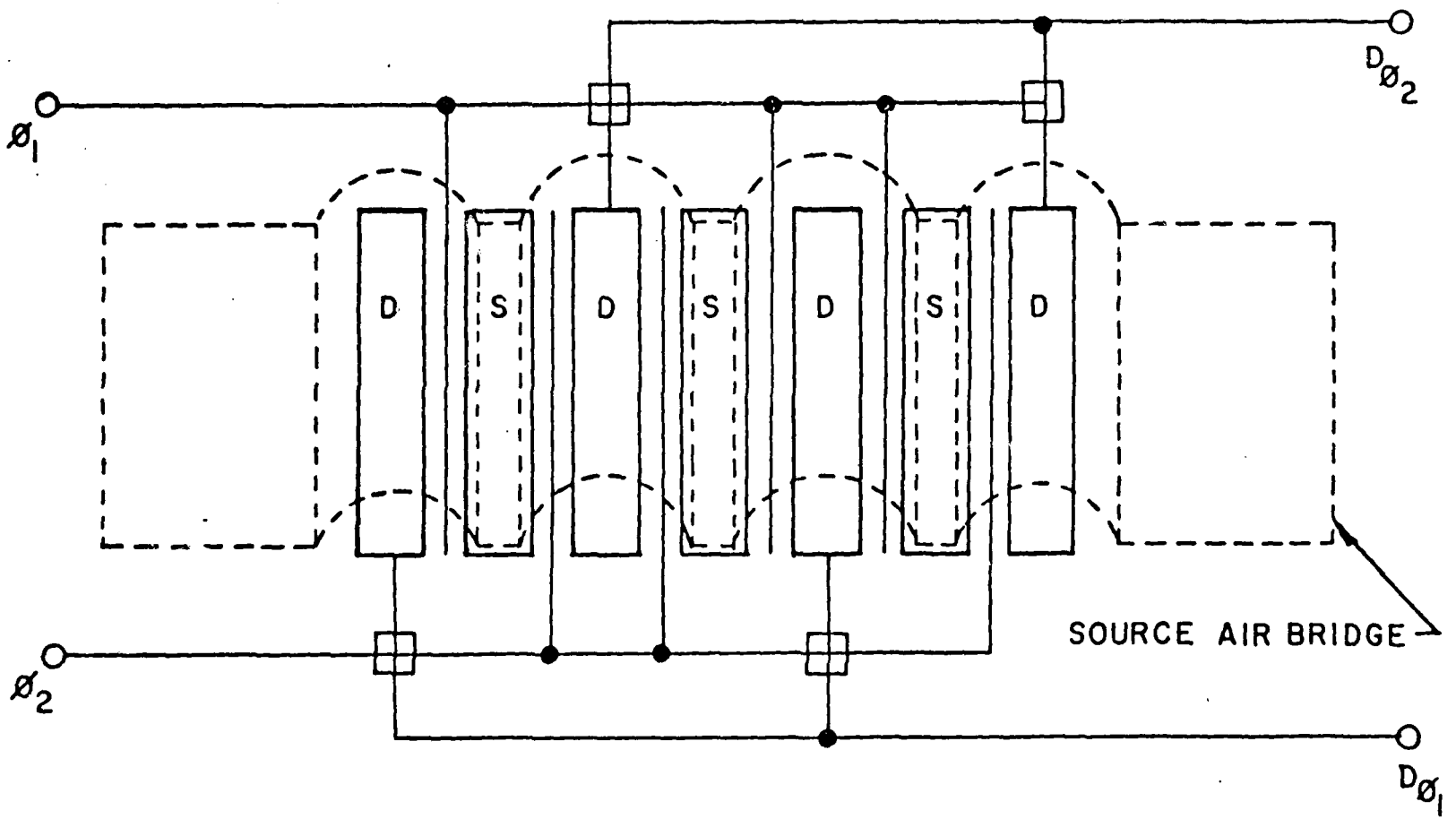


FIG. 1. SCHEMATIC LAYOUT

still flows through the source-to-gate region of the channel, which accounts for most of the source resistance in the current MBE/EB FET design under ONR Contract N00014-77-C-0655. The n^+/metallization contact resistance and the metallization resistance itself may be bypassed by this exchange current, leading to some improvement in gain (and in noise figure through coherent cancellation of the noise effects in the common parts of the resistance).

(3) the possibility of neutralization (or even overcompensation, if desired) of the feedback capacitance C_{gd}, by intentional capacitive feedback to the gates from the drain lines of the opposite phase devices. Again, by eliminating rapidly-varying reactive terms in the gain expression, this should extend the upper frequency limits of useful operation, as well as easing problems for the broadband circuit designer.

(4) a convenient geometry for reducing gate resistance by paralleling large numbers of short gate fingers.

The basic high-frequency capability of the FET, however, still resides in the transit time reductions afforded by the short physical length of the gate, combined with the possible short-gate velocity overshoot effects leading to increased transconductance. These are attainable through use of advanced fabrication techniques such as electron beam lithography, molecular beam epitaxy, etc., in use at Varian under Contract N00014-77-C-0655.

The goal of this contract, then, is to design, fabricate, and evaluate balanced FETs utilizing the features previously itemized and shown schematically in Fig. 1. The same total device gate width of 150 microns is used as for the dual-gate structure used under Contract N00014-77-C-0655, shown in Fig. 2. The same material parameters and

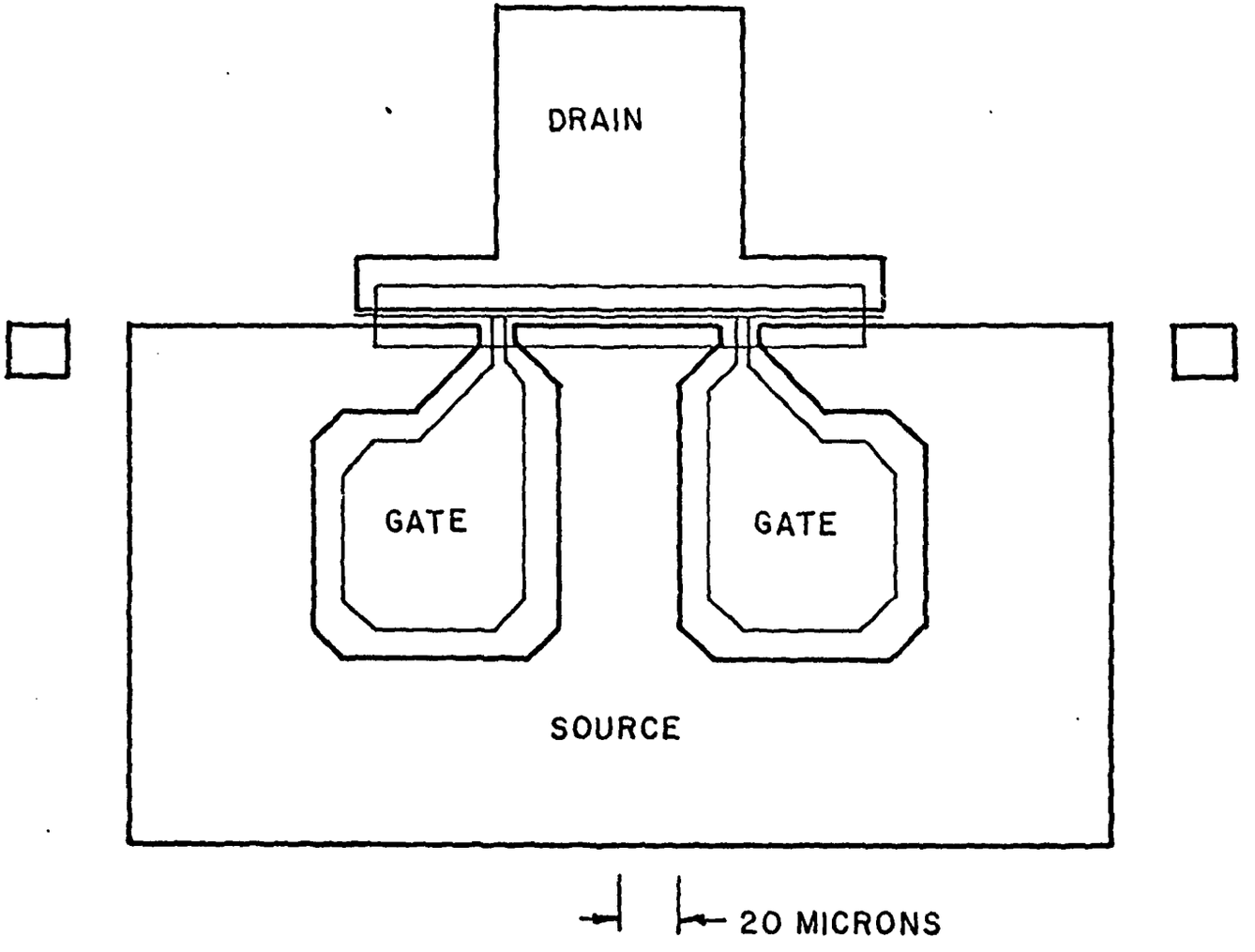


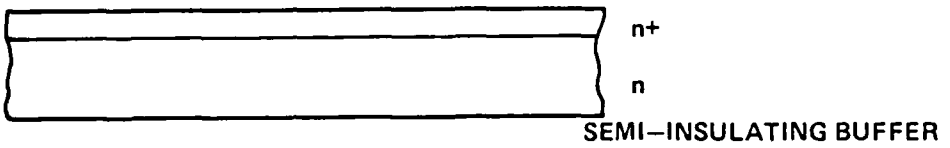
Fig. 2 Dual gate pad geometry.

fabrication process are used, including electron-beam exposure of the gates to achieve sub-half-micron gate lengths. This provides a basis of comparison with which to evaluate the merits of balanced operation.

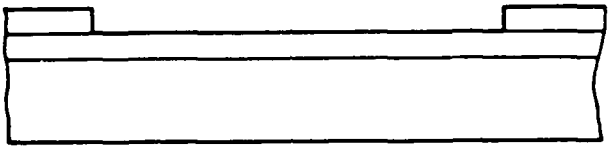
II. FABRICATION PROCESS

This section briefly outlines the material parameters and fabrication process used for the devices fabricated under this program and under Contract N00014-77-C-0655. MBE material is used, having a one-micron buffer layer, a 1200 Å thick n-type active layer doped 3.5 x $10^{17}cm^{-3}$ with Si, and an n^+ contact layer doped greater than $10^{19}cm^{-3}$ with SnTe. These parameters are nominal, with the MBE growth being done at 581°C.

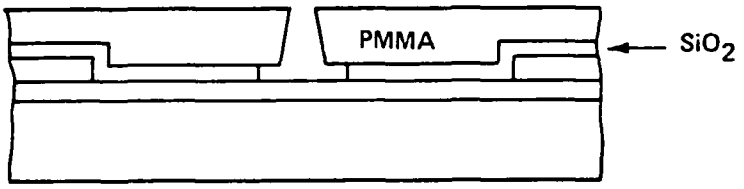
Figure 3 shows the fabrication process. The gate is exposed with a computer-controlled electron beam using an ETEC Autoscan SEM. The gate is self-aligned in the channel between two n^+ contacts by use of the channel etch; Fig. 4 shows that the gate can be placed extremely close (within 1000 Å) to the source n^+ region, providing a low source resistance. Figure 4 also shows the typically triangular cross-section of the gate metallization, due to the resist opening gradually being closed up by metal buildup on the edges of the resist mask defining the gate electrode during the gate metal deposition. This problem appears to be basic to the fabrication of such small gate lengths,[1,2] and causes the FET gate resistance in conventional FET designs to dominate the input resistance and thereby raise the device noise figure. The paralleling of the gates by the balanced scheme of Fig. 1 will help alleviate this problem by shortening the effective length of the gate fingers.



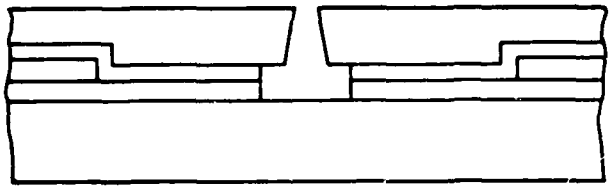
(a) STARTING MATERIAL



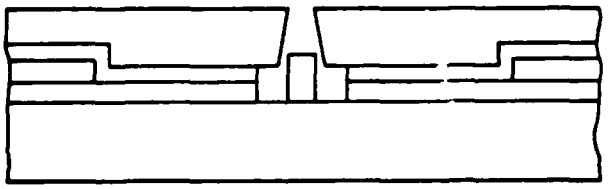
(b) OHMIC CONTACTS



(c) GATE DEFINITION

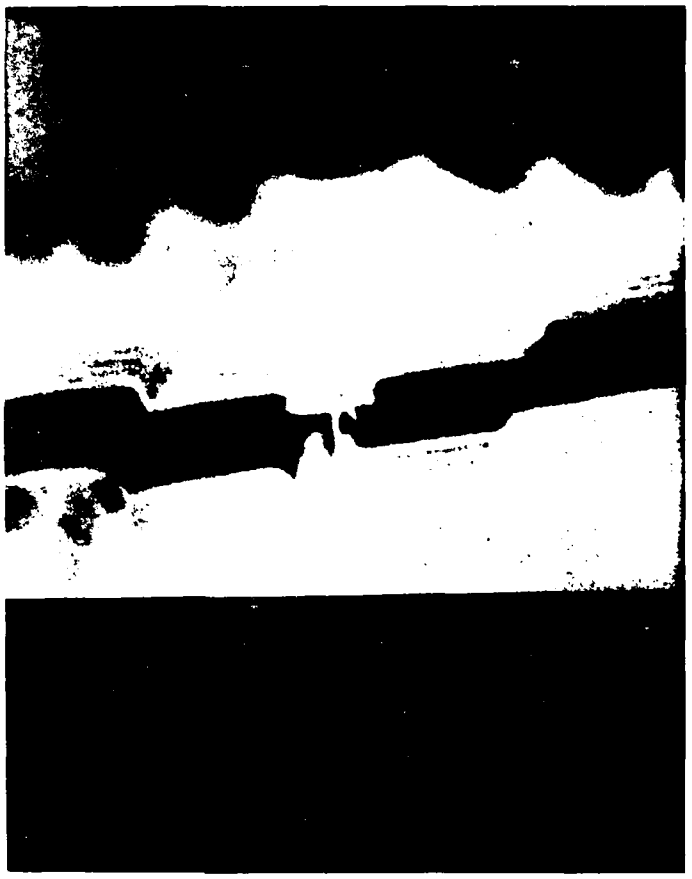


(d) ANODIC ETCH



(e) GATE DEPOSITION

Fig. 3 Gate anodization process.



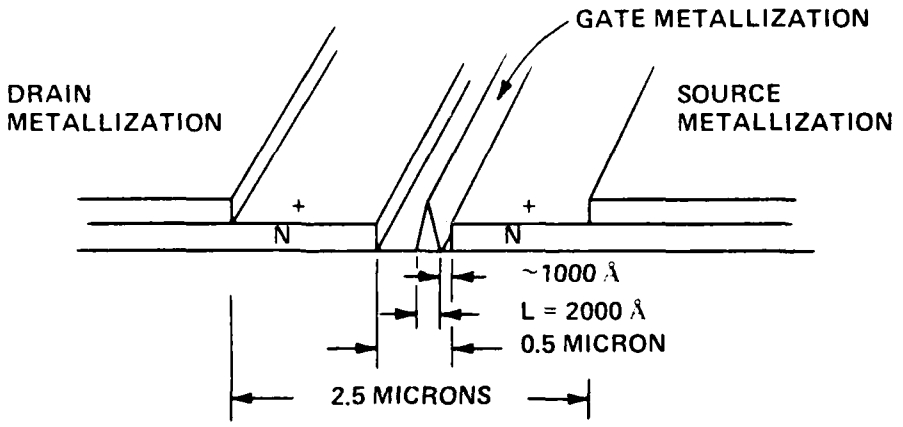


Fig. 4 Cross section of gate channel area.

III. BALANCED FET DESIGN

A. Design Considerations

Figure 1 shows the schematic layout of the low-noise FET device to be designed, fabricated, and evaluated under this contract. This design should permit elimination of the parasitic source inductance, L_s, and minimization of the parasitics r_g (gate resistance), R_s (source resistance), and C_{gd} (drain-to-gate feedback capacitance).

Gate Resistance, r_g: If R is the total end-to-end gate resistance of the gate stripe, then if broken up into N segments and paralleled,

$$r_g = \frac{R}{3N^2} \quad . \tag{1}$$

Under ONR Contract N00014-77-C-0655, a dual gate pad structure is used to give N = 4, but gate resistance remains a problem because of the high value of R due to the small gate length (0.25-micron or less) and to closure of the gate aperture in the resist by sideways metal buildup on the top of the resist edge, previously described. The structure of Fig. 1 will allow N to be as high as 10, say, thus effecting a decrease in r_g of about a factor of 6. With the structure used for the dual gate pad device, a value of N larger than 4 would be difficult without having to go to multiple source pads.

Source Inductance, L_s: The reduction in gate resistance accomplished by the structure in Fig. 1 is done at the expense of multiple source pads, which in turn means stitch bonding and an increase in L_s. However, the push-pull design of Fig. 1 should virtually eliminate L_s for the fundamental component of the signal. Appendix A shows the role that L_s plays in the noise figure. For purposes of computation, r_g = 1 ohm, R_s = 2 ohms, $g_m L_s / C_{gs}$ = 5 ohms (typical for the dual gate pad

structure, L = 0.2 micron, Z = 150 microns, $N_D = 3.5 \times 10^{17} cm^{-3}$ and a = .07 micron; Equation (A-1) gives 2.69 dB for NF_m at 24 GHz. With L_s = 0, these same parameters give 2.04 dB at 24 GHz, indicating the significant impact that L_s can have on the noise figure at the higher frequencies (at 8 GHz, L_s has little effect on NF_m). Multiple sources will result in a larger value of L_s than used in this example, making it even more imperative to use the balanced push-pull scheme of Fig. 1.

Source Resistance, R_s: Referring to Fig. 5, after some analysis,

$$R_1 = R_n + \left(\frac{\rho_c}{ZL_T}\right) \frac{\left(e^{\ell_s/L_T} - 1\right)^2}{e^{2\ell_s/L_T} - 1} \qquad (2)$$

$$R_2 = \left(\frac{\rho_c}{ZL_T}\right) \frac{2e^{\ell_s/L_T}}{e^{2\ell_s/L_T} - 1} \quad , \qquad (3)$$

where

$$L_T = \sqrt{\rho_c/\rho_s} \qquad (4)$$

is the transfer length, ρ_c is the specific contact resistance and ρ_s is the sheet resistance of the n layer. When operating push-pull, only R_1 affects the high-frequency performance, so it is desirable to minimize it. R_n and ρ_c can be minimized by going to an n^+ layer, and lowered even further using Cornell's As-doped Ge layer.[6] The last term in R_1 can be minimized with $\ell_s << L_T$. However, for $\rho = 10^{-6}$ ohm-cm^2 and ρ_s = 125 ohms/square for a $2.5 \times 10^{18} cm^{-3}$ doped n^+ layer, as used under Contract N00014-77-C-0655, L_T = 0.9 micron. For air-bridged pads, ℓ_s probably cannot be smaller than about 10 microns or so, unless a scheme like that shown in Fig. 6 is used. Lowering ℓ_s, ρ_c and ρ_s always reduces R_1, so increasing ρ_c to make $\ell_s < L_T$ will result in a higher value of R_1.

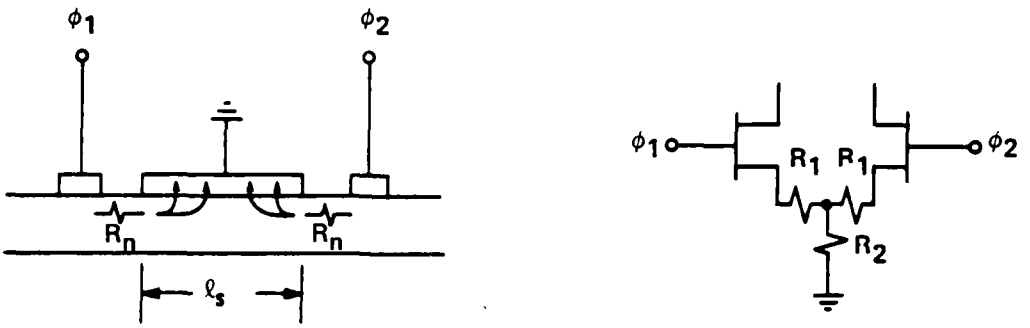


Fig. 5 Push-pull source resistance.

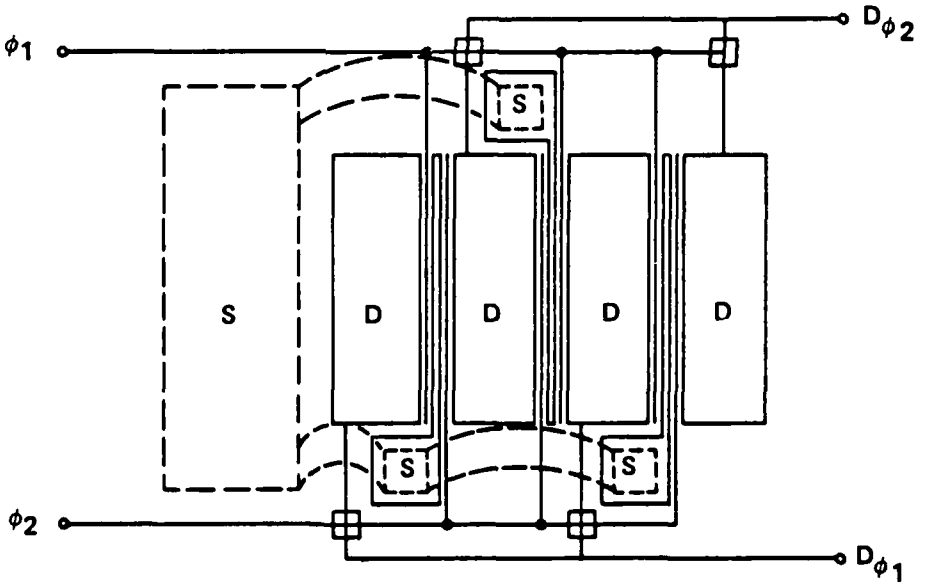


Fig. 6 Push-pull scheme to reduce source dimension.

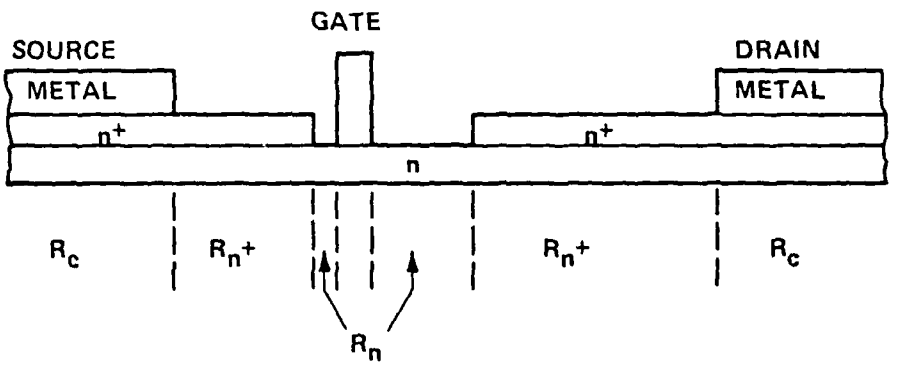


Fig. 7 Source resistance breakdown into component values.

Referring to Fig. 7 for the device fabricated under Contract N00014-77-C-0655, using Z = 150 microns, $\rho_c = 10^{-6}$ ohm/cm^2, $N_D = 2.5 \times 10^{18}$cm^{-3} for the 1000 Å thick n^+ layer, and $N_D = 3.5 \times 10^{17}$cm^{-3} for the 700 Å thick n layer, then for $\ell_s >> L_T$

$$R_n = 0.48 \text{ ohm} \qquad R_{n^+} = 0.833 \text{ ohm} \qquad R_c = 0.747 \text{ ohm}$$

using a 1000 Å n^+-gate spacing and a one-micron n^+ length. Consequently, going to the more difficult scheme of Fig. 6 in order to reduce R_c will do little to reduce the overall value of the source resistance. This means that the push-pull scheme of Fig. 1 will probably do little to lower R_s.

Feedback Capacitance, C_{gd}: The crossovers shown in Fig. 1 offer the possibility of neutralization (or even over-compensation, if desired) of the feedback capacitance C_{gd} by intentional capacitance feedback to the gates from the drain lines of the opposite phase devices. This will compensate the Miller effect of C_{gd}, provided the sum of the crossover capacitances for a particular phase is equal to the total value of C_{gd} for all the devices driven by that phase. This should extend the upper frequency limits of useful operation.

B. Mask Design

Figure 8 shows the design for the balanced FET in completed form. The mask layers shown are the source-drain, gate, crossover oxide, and air bridge layers. In the interest of clarity, the mesa, overlay, air-bridge contact, and oxide protection layers are not shown. The following explains some of the pertinent details of this mask set.

To maintain a comparison with the devices fabricated under ONR Contract N00014-77-C-0655, the total active device width is Z = 150 microns.

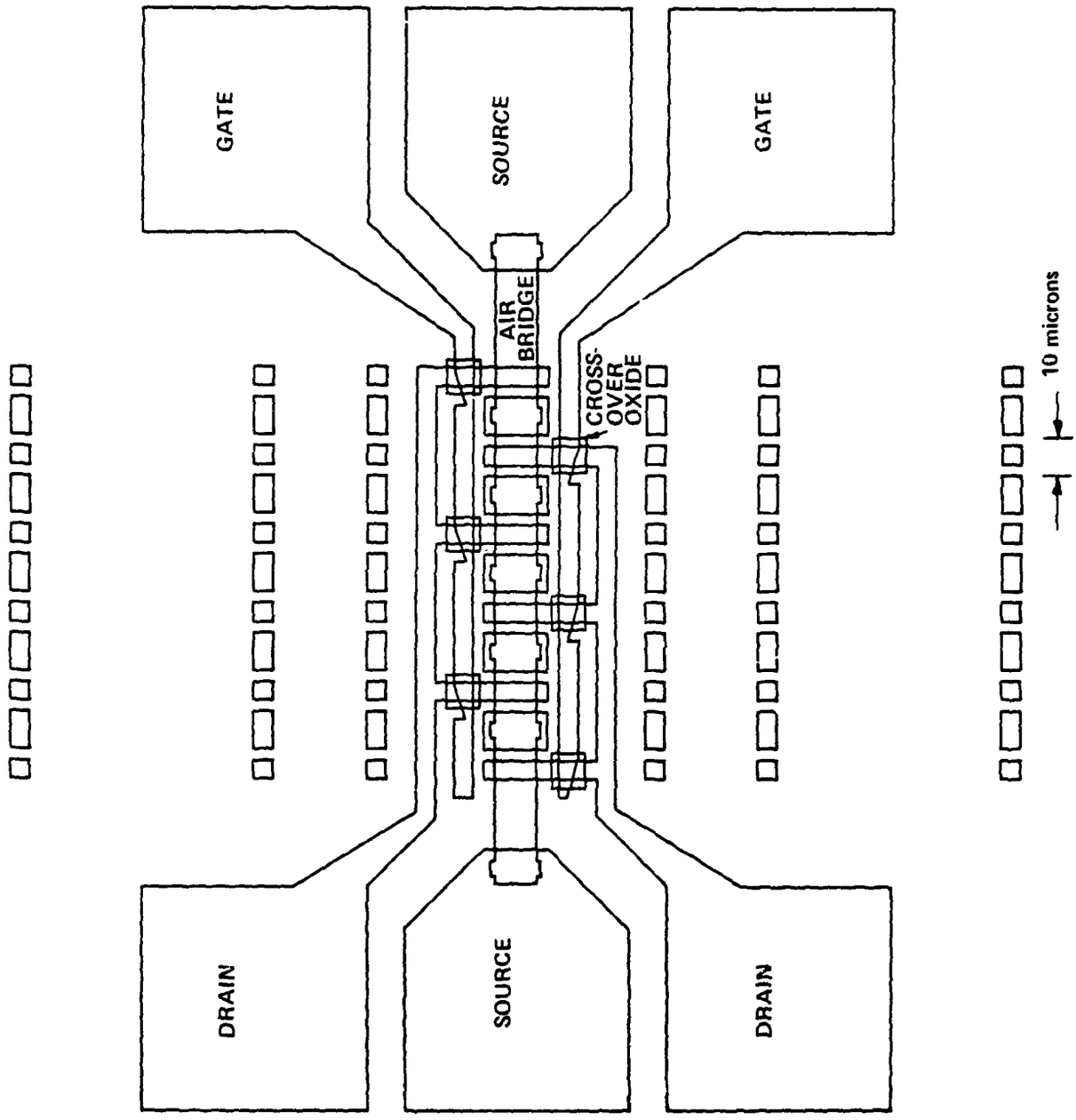


Fig. 8 Design for balanced FET.

Ten gate fingers are used, each having an active length of 15 microns. The 0655 contract devices had finger lengths of 37.5 microns, so a substantial decrease in gate resistance should be realized. Fifteen gate fingers having 10-micron active lengths could have been used, but this would result in quite a lopsided aspect ratio, and the ratio of the active-to-inactive finger lengths (the inactive length being the distance from the mesa edge to the gate bus, being about 4 microns for the design of Fig. 8) would become quite sizeable. The gates are to be written by electron beam exposure (and are not shown in Fig. 8), and gate tabs may be added tc the software to reduce the inactive length.

The bonding pad layout affords easy mating with coplanar waveguide inputs and outputs. It was tempting to put both the gate and drain signal of the opposite phase on the same pair of coplanar waveguide lines to enhance the coupling to cancel the feedback effect of C_{gd}, but the coupling is very complex and includes inductive coupling, so it was decided that it would be better to have the negative feedback coupling of adjacent gate (and drain) pairs.

Based on the results from the 0655 contract, around .0024 pF is needed per gate-drain crossover to cancel C_{gd}. This is accomplished with CVD SiO_2, and the serrated gate bus allows a 2:1 adjustment to compensate for uncertainties in both the nominal 2000 Å oxide thickness and the dielectric constant.

The design allows for a one-micron mesa undercut (typical for devices on the 0655 contract) and places the gate bus as close to the mesa as possible to minimize the parasitic resistance of the inactive part of the gate finger. The source-drain spacing is increased from the 2.4-micron value on the 0655 contract to 2.8 microns to reduce PMMA resist buildup in the channel and aid the gate exposure. The array of squares and rectangles in the field are for purposes of alignment in writing the gates in the SEM.

IV. DEVICE FABRICATION

As previously mentioned, it is anticipated that source resistance will still be a problem in spite of the balanced operation. In anticipation of this, n^+-on-n layers were grown by MBE for purposes of evaluating the n layer, n^+ layer, and contact resistance portions of the source resistance. A technique was devised where ohmic contacts were put down on the material and the material was thinned in steps and the saturated current was recorded for each step. This technique determined when the n layer was reached, which was then profiled in the conventional manner (the ohmic contacts were on one edge of the wafer). The current profile for the n^+ layer was then differentiated with respect to distance and matched to the n-layer profile to obtain the doping profile for the n^+ layer, which cannot be profiled by conventional techniques because of Schottky-barrier leakage. This technique assumes that the saturated velocity is independent of doping, which seems to be the case according to Ref. 7. By employing this technique and using it as feedback to the MBE growth, layers to be used for balanced FET fabrication were obtained with $n = 3.5 \times 10^{17} cm^{-3}$ and n^+ in excess of $10^{19} cm^{-3}$. 150-micron wide ohmic contacts spaced 2.5 microns apart on this material (no channel etch) were measured to have 2.5 ohms resistance.

During the report period, the software for electron lithography of the gates was written, and during the course of its development, it was determined that the alignment mark configuration for the E-beam exposure was inadequate in that it was difficult to determine which of the three pairs of alignment marks were actually being observed in the narrow observation windows. This problem has been resolved by using the drain pads for alignment.

The mask set was fabricated by Master Images and evaluated as being satisfactory. The desired channel spacing was 2.8 microns, but was measured to be around 2.3 microns, which falls slightly outside the

specified tolerance of ±0.4 micron (a tighter spec of ±0.25 micron was desired, but the mask vendor would accept only ±0.4 micron as the minimum). The purpose for the longer channel is that the ohmic contact metallization and the overlay can be done at the same time with the same resist liftoff. Such a procedure for a spacing of 2.4 microns or less gives a "Grand Canyon" effect, which in turn prevents a good gate resist profile and hence a good E-beam gate exposure from being obtained. The FETs fabricated under Contract N00014-77-C-0655 have a 2.4-micron channel spacing, necessitating a separate resist step for the overlay metallization, which is set back from the channel edge by about 2 microns. Since the smaller channel spacing should not preclude obtaining good working devices, the mask set was accepted.

The 2000 Å CVD SiO_2 deposition for the dielectric for the feedback capacitance cancellation was done at 350°C for 2.7 minutes, and was found to cause the edges of the ohmic contact to become more irregular than they ordinarily are after alloy. Whether or not this will consistently be the case is not known. Although SiO_2 at the same temperature is used to facilitate the gate formation for the FETs under Contract N00014-77-C-0655, the time of about 0.8 min. is much less. Figures 9 and 10 show different magnifications of the channel regions after the gates have been formed by electron-beam exposure and evaporated.

Figures 11 and 12 show different magnifications of the completed device after formation of the air bridge which connects all of the sources together. Many of the air bridges partially lifted off (an O_2 plasma descum before the air bridge metallization should cure this) and many devices did not have all of their gates connected to the gate bus, owing to the difficulty in obtaining the proper alignment in the SEM.

Fig. 9 Balanced FET channel region.

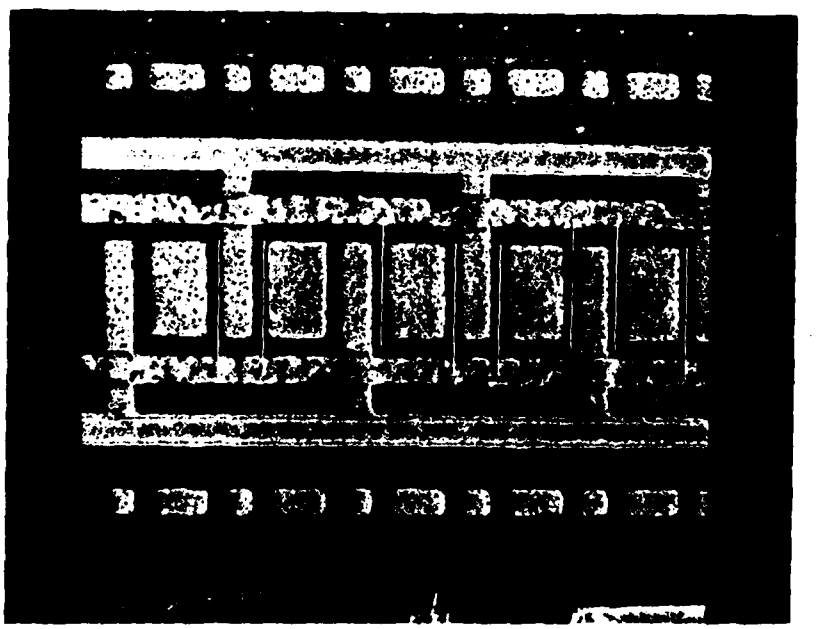


Fig. 10 Balanced FET channel region.

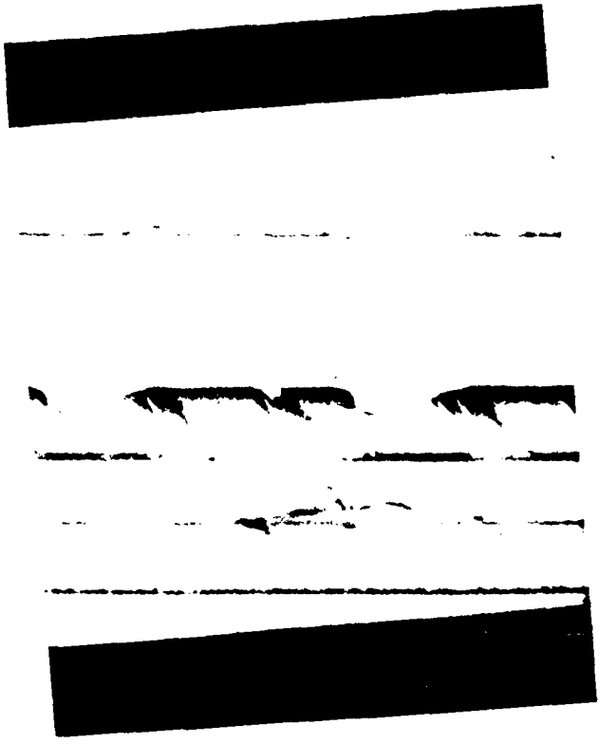


Fig. 11 Completed balanced FET with air bridge.

Fig. 12 Completed balanced FET with air bridge.

V. DEVICE CHARACTERIZATION

Figures 13 and 14 show the drain characteristics for two of the devices. The g_m's are 28-30 mmhos, and are the same as for the FETs of Contract N00014-77-C-0655, which have the same total active Z = 150 μm device width and are fabricated on identical MBE material, since the purpose of this balanced FET design is to match the dc characteristics of the FETs of Contract N00014-77-C-0655, but to outperform them at rf frequencies by virtue of lower gate resistance, source inductance, and feedback capacitance in the balanced mode.

Rf measurements were made on several of the devices by connecting both drain and gate pads together and operating the FET as a 3-terminal device rather than in the balanced mode (we have not yet developed the circuitry to provide balanced signals and balanced matching). Table I gives the results of measurements made at 8 GHz.

TABLE I

Balanced FET Performance in Single-Ended Mode at 8 GHz

Device	NF_m (dB)	G_a (dB)
BALFET 2-2	3.5	3.6
BALFET 2-3	3.1	4.5
BALFET 3-1 (common drain)	2.66	10.2
BALFET 3-2	3.6	3.2

These resutls are rather poor in light of the $NF_m \doteq$ 1-1.5 dB, $G_a \doteq$ 12-14 dB values obtained for the FETs on Contract N00014-77-C-0655. Slightly poorer performance could be expected when operated single-endedly due to the increased feedback capacitance (ideally, it should be double so that

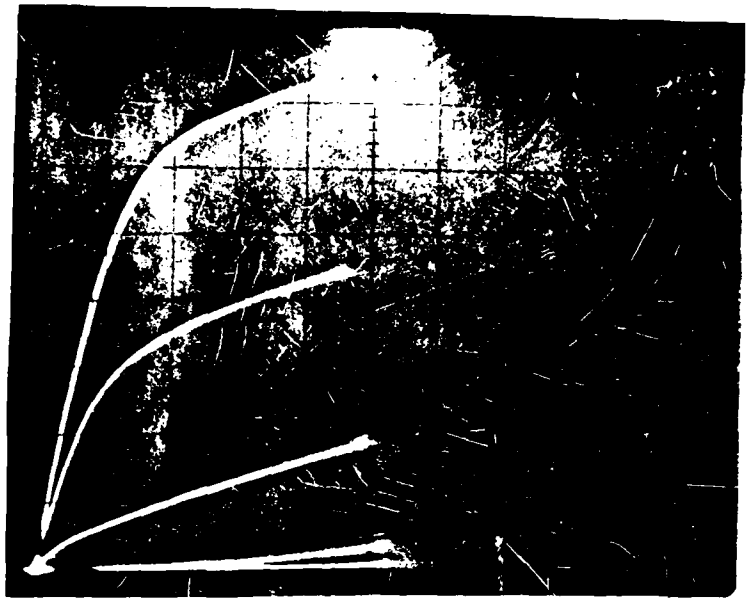


Fig. 13 Typical balanced FET drain characteristic.
(5 mA/div, 0.5 V/div, -0.5V/step)

Fig. 14 Typical balanced FET drain characteristic.
(10 mA/div, 0.5V/div, -0.5V/step)

when operated in the balanced mode, it will be zero) and higher source inductance (due to the air bridge needed for the paralleling of the ten segments, which also should be effectively zero when operated in the balanced mode), but not to the degree of the data in Table I. S-parameter measurements will be made on the devices to determine the cause. Perhaps the feedback capacitance of the gate-drain crossovers is much higher than expected. S-parameters should also reveal why the results were so much better for the common drain connection.

VI. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

During this period, a balanced FET mask set was designed and devices fabricated to match the dc characteristics of the sub-half-micron gate FETs of ONR Contract N00014-77-C-0655, but to outperform them at rf frequencies by virtue of lower gate resistance, source inductance, feedback capaciatance, and possible source resistance when operated in the balanced or push-pull mode. Late in the period, several device runs were made which cosmetically looked good and which indeed matched the excellent dc characteristics (g_m's of 28-30 mmhos for Z = 150 microns) obtained for single-ended FETs of the same width made on the same material. However, when operated single-endedly at 8 GHz, the performance of the balanced FETs was rather poor. S-parameter measurements need to be made on the fabricated devices to determine the cause. Perhaps the feedback capacitance of the gate-drain crossovers is much higher than expected.

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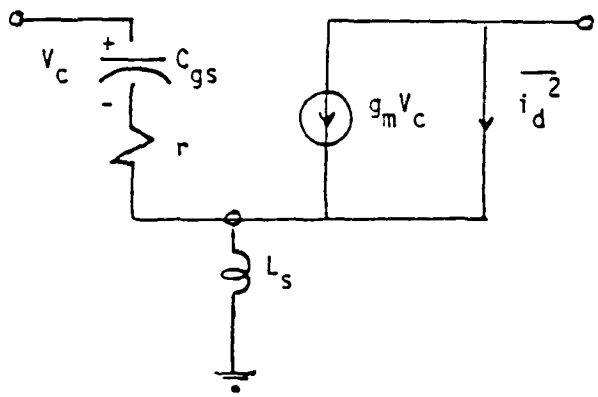
APPENDIX A: NOISE FIGURE COMPUTATION

For the FET model



with $r = r_g + R_s + r_o \cong r_g + R_s$, the minimum noise figure is given by:

$$NF_m = 1 + 2r_{11}\omega^2 C_{gs}^2 R_{eq} + 2(r\omega^2 C_{gs}^2 R_{eq} + r_{11}^2 \omega^4 C_{gs}^4 R_{eq}^2)^{1/2} \qquad (2)$$

where

$$r_{11} = r + \frac{g_m L_s}{C_{gs}} = \text{real part of } z_{11}$$

$$r_{eq} = \frac{\overline{i_d^2}}{4kTB\, g_m^2} .$$

Podell[3] has found empirically for one-micron gate length FETs that,

$$R_{eq} \cong \frac{1.25}{g_m} .$$

Using this in Eq. (1) along with parameter values at 8 GHz for run EB 26 results in

$$NF = 1 + 2\omega C_{gs} \sqrt{r R_{eq}} \qquad (3)$$

which is nearly identical to that of Fukui[4] (Eq. 1). Since BTL and others find Fukui's equation to be an accurate description of the noise of their devices, it will be used to compute R_{eq}. Setting Eq. (3) equal to Eq. (1) results in

$$R_{eq} = \frac{[.04\, L^{5/6}\, (N_D/a)^{1/6}\, Z^{1/2}]^2}{4\pi\, C_{gs}^{\,2} \times 10^{-6}} \quad , \qquad (4)$$

enabling Eq. (2) to be used at the higher frequencies where Eq. (1) is no longer valid.

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