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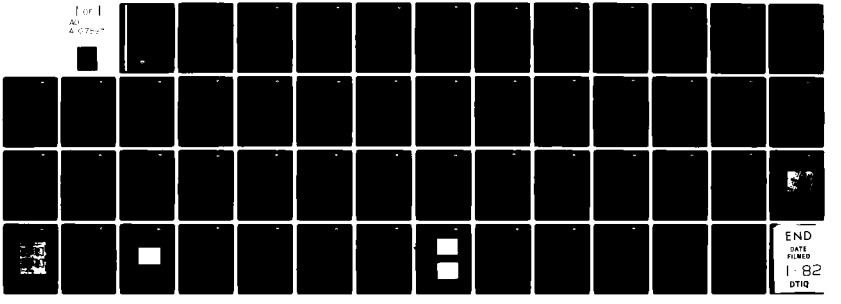

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High resistivity epitaxial layers of $Al_xGa_{1-x}As$ have been produced by molecular beam epitaxy. These layers have been incorporated, as a buffer layer, in the fabrication of GaAs MESFETs and the results are discussed. Device analysis includes an assortment of low frequency and DC measurements as well as RF measurements.

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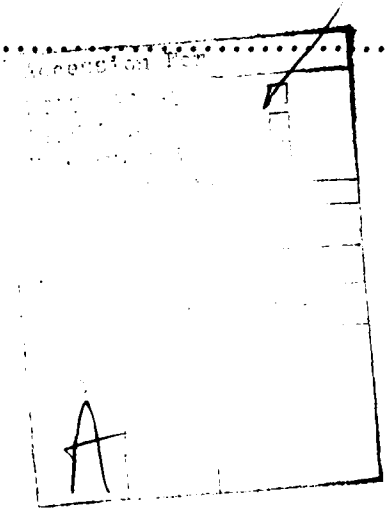
TABLE OF CONTENTS

		Page
1.0	INTRODUCTION	1
2.0	TECHNICAL DISCUSSION	2
2.1	Molecular Beam Growth Technology for Transistor Applications	2
2.1.1	Basic Structures Grown	2
2.1.2	Techniques for Achieving 1) Abrupt Impurity Profiles, 2) High-Resistivity AlGaAs, 3) Other Things Related to Growths and Program	2
2.2	Heterostructure Field Effect Transistors	10
2.2.1	Theory of Operation	10
2.2.2	Analysis Techniques	11
3.0	CHARACTERIZATION AND RESULTS	23
3.1	Material Results	23
3.1.1	Sn Predeposition	23
3.1.2	Deep Levels in AlGaAs	23
3.1.3	MIS Structures by MBE	29
3.2	Device Results and Performance	32
3.2.1	Device Fabrication	32
3.2.2	Low Frequency Device Analysis	38
3.2.3	RF Performance	43
4.0	CONCLUSION	45
5.0	REFERENCES	46



LIST OF FIGURES

		Page
Fig. 1	Comparison of n-GaAs on (a) S.I. AlGaAs and (b) S.I. GaAs.....	12
Fig. 2	Comparison of n-GaAs on (a) S.I. AlGaAs and (b) S.I. GaAs under conditions of static reverse bias.....	13
Fig. 3	High-frequency equivalent circuit of an FET.....	15
Fig. 4	Ohmic contact resistance measurement.....	16
Fig. 5	Test set for measurement of FET admittance.....	18
Fig. 6	Noise figure and gain test set.....	21
Fig. 7	C-V profile of Sn predeposition.....	25
Fig. 8	PITS spectrum of MBE AlGaAs.....	26
Fig. 9	Comparison of Free Carrier Concentration and Metallurgical Thickness for MBE GaAs.....	28
Fig. 10	Schematic of MIS structure.....	31
Fig. 11	C-V of MIS structure (dark).....	32
Fig. 12	C-V, G-V of MIS structure (light).....	34
Fig. 13	Carrier confinement field effect transistors.....	36
Fig. 14	Characterization test pattern.....	37
Fig. 15	I-V of MBE FET featuring current fluctuation.....	39
Fig. 16	Ohmic contact resistance of MBE GaAs on AlGaAs.....	40
Fig. 17	Drift mobility test set data.....	41
Fig. 18	Drift mobility of an ion-implanted layer.....	42
Fig. 19	I-V comparison of MBE layers.....	44

1.0 INTRODUCTION

GaAs FET technology has reached a status where conventional devices are in production[1] and new material approaches are being investigated for potentially higher performance devices. The current confinement properties of an epitaxial heterostructure layer is one such approach. Reduced noise figures and higher operating frequencies are envisaged for devices where the conduction channel is controlled both from the active layer surface and the active layer-buffer layer interface. Molecular beam epitaxy is an attractive technology where thin, highly doped compound semiconductors can be grown. The heterostructure layers considered in this research project are n-type GaAs on high resistivity AlGaAs buffer layers. Rockwell International Electronics Research Center, Thousand Oaks, has long been involved in the fabrication and characterization of GaAs microwave transistors.[2] Progress in this technology has produced a well established one micrometer gate length device. It is this transistor structure which has been used to gather device results for MBE layers grown for this program.

Section 2.0 begins with a discussion of molecular beam epitaxy growth techniques for high performance device applications. This section continues with a discussion of low noise FET analyses used for device characterization and evaluation. Section 3.0 presents the experimental results and their interpretations. A summary of the results is given in Section 4.0.

2.0 TECHNICAL DISCUSSION

2.1 Molecular Beam Growth Technology for Transistor Application

The research conducted using molecular beam epitaxy (MBE) techniques for this contract can be divided into two broad categories: (1) investigation of GaAs and AlGaAs epilayer properties to determine their suitability for high frequency device applications, and (2) preparation of wafers suitable for tests of MIS structures and AlGaAs buffer FET structures. Under (1), undoped and doped n-type GaAs with Ge and Sn were grown to determine background impurity content and mobilities at doping levels suitable for FET active layers. AlGaAs has been grown, undoped, under our standard UHV conditions, in the presence of an O_2 ambient, and with a H_2 ambient, to determine the deep level content and resistivity of this material for insulating layers in MIS structures or as a buffer layer for a Schottky gate MESFET structure. Under (2), several MIS structures using semi-insulating or oxidized AlGaAs layers, and a number of AlGaAs-buffer layers were grown for FET fabrication.

2.1.1 Basic Structures Grown

A list of the layers grown specifically for this project is given in Table 1. Knowledge gained in the growth of MBE material through other projects were useful in determining doping parameters, growth rates, etc. Many layers grown in general (not specifically earmarked for any project) to calibrate dopant source performance, background doping, and other MBE system parameters are not included in this list.

2.1.2 Growth Techniques for Device Applications

In order to produce FET devices with useful characteristics, several critical parameters must be optimized. The epilayer thickness and doping density must be selected so that active layer pinch-off is achieved before gate current becomes large. Therefore, a doping density of 1-2 $\times 10^{17}/cm^3$ and active layer thickness of about 3000Å were chosen. Tests were made on each

Layer	Composition	Thickness (μm)	Doping	Comments
106	GaAs	1.7	----	Background calibration
108	GaAs	2.8	----	Background calibration
110	GaAs	3.6	----	Background calibration
111	GaAs	2.3	----	Background calibration
112	$Al_{0.15}Ga_{0.85}As$		----	For ρ, SIMS
113	$Al_{0.3}Ga_{0.7}As$		----	For ρ, SIMS
114	GaAs	1.7	----	Background calibration
119B	GaAs	2.0	----	PITS sample
137	$Al_{0.09}Ga_{0.91}As$		----	For ρ, SIMS
138	$Al_{0.11}Ga_{0.89}As$		----	For ρ, SIMS
208	$Al_{0.17}Ga_{0.83}As$	2.000	----	3 active layer thicknesses
	GaAs	0.350	Ge	
	GaAs	0.100	Ge	
	GaAs	0.100	Ge	
209	$Al_{0.23}Ga_{0.77}As$	2.000	----	
	GaAs	0.270	Ge	
*210	$Al_{0.3}Ga_{0.7}As$	2.000	----	Growth in 10^{-6} torr H_2
	GaAs	0.250	Ge	
	GaAs	0.100	Ge	
	GaAs	0.100	Ge	
211	$Al_{0.29}Ga_{0.71}As$	2.300	----	Growth in 10^{-6} torr H_2
212	$Al_{0.3}Ga_{0.7}As$	2.000	----	Growth in 5×10^{-7} torr O_2
	GaAs	0.250	Ge	3 active layer thicknesses
	GaAs	0.100	Ge	
	GaAs	0.100	Ge	
*213	$Al_{0.3}Ga_{0.7}As$	2.000	----	Growth in 5×10^{-7} torr O_2
	GaAs	0.350	Ge	

Layer	Composition	Thickness (μm)	Doping	Comments
*261	$Al_{0.4}Ga_{0.6}As$	1.000	----	Growth in 10^{-6} torr O_2
	GaAs	0.250-0.350	Bkgnd ~10^{17}/cm^3	Graded active layer thickness
262	$Al_{0.40}Ga_{0.60}As$	1.000	----	Growth in 10^{-6} torr O_2
	$Al_{0.05}Ga_{0.95}As$	0.044	----	Graded buffer-active interface
	GaAs	0.250-0.350	Bkgnd 10^{17}/cm^3	Graded Active layer
*283	GaAs	0.500	----	No O_2 background
	$Al_{0.30}Ga_{0.70}As$	1.350	----	Sn predeposition to tailor
	GaAs	0.005	Sn	doping profile
	Sn/As		Sn predeposition	
	GaAs	0.250	Sn	
*284	GaAs	0.500	----	O_2 background during AlGaAs
	$Al_{0.20}Ga_{0.80}As$	1.000	----	growth
	GaAs	0.005	Sn	
	Sn/As		Sn predeposition	
	GaAs	0.250		
*285	GaAs	0.500	----	No O_2 background
	$Al_{0.36}Ga_{0.64}As$	1.000	----	
	GaAs	0.005		
	Sn/As		Sn predeposition	
	GaAs	0.250	----	
*286	GaAs	0.500	----	O_2 background during AlGaAs
	$Al_{0.40}Ga_{0.60}As$	1.000	----	growth
	GaAs	0.005	----	Higher Al content
	Sn/As		Sn predeposition	
	GaAs	0.250	----	
*287	GaAs	0.005	----	Sn predeposition with As flux
	Sn/As		Sn predeposition	Growth directly on S.I. GaAs,
	GaAs	0.250	----	for comparison
302	GaAs	1.000	Sn	MIS structure, graded GaAs-
	$Al_{0.0}Ga_{0.3}As$	0.050	----	AlGaAs interface
	$Al_{0.50}Ga_{0.50}As$	0.200	----	In situ metallization
	Al	0.200	----	
303	GaAs	1.000	Sn	MIS structure
	$Al_{0.2}Ga_{1.0}As$	0.050	----	AlAs oxidized at 200°C in
	AlAs	0.200	----	pure O_2

Layer	Composition	Thickness (μm)	Doping	Comments
319	GaAs	1.000	----	MIS structure
	$Al_{0.5}Ga_{0.0}As$	0.050		Graded AlAs thickness
	AlAs	0.050-0.500	---- Graded	AlAs oxidized at 250°C in O_2
342	GaAs	0.500	----	342-360: series of $Al_{0.5}Ga_{0.5}As$ buffer runs with attempt to optimize active layer thickness and doping. Several substrate temperatures used during growth $Al_{0.5}Ga_{0.5}As$ to investigate effect of growth temperature on deep levels
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.005	----	
	Sn/As		Sn predeposition	
	GaAs	0.300	Sn	
343	GaAs	0.500	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.005	----	
	Sn/As		Sn predeposition	
	GaAs	0.300	Sn	
351	GaAs	0.500	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	Sn/As		Sn predeposition	
	GaAs	0.250	Sn	
352	GaAs	0.500	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	Sn/As		Sn predeposition	
	GaAs	0.250	Sn	
353	GaAs	0.500	----	
	GaAs	0.166	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.005	----	
	Sn/As		Sn predeposition	
	GaAs	0.250	Sn	
354	GaAs	0.500	----	
	GaAs	0.166	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.350	Sn	
	GaAs	0.650 (n^+ only)	Sn	

	Composition	Thickness (μm)	Doping	Comments
355	GaAs	0.500	----	n^+ contact layer added
	$Al_{0.50}Ga_{0.50}As$	1.250	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.150	Sn	
	GaAs	0.150 (n^+ only)	Sn	
356	GaAs	0.500	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.350	Sn	
*357	GaAs	0.500	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.350	Sn	
*358	GaAs	0.500	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.350	Sn	
*359	GaAs	0.500	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.350	Sn	
*360	GaAs	0.500	----	n^{++} contact layer added
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.350	Sn	
	GaAs	0.050	Sn	
	GaAs	0.005	Sn	
	Sn/As			
389	GaAs	1.000	----	Check of no predeposition
	$Al_{0.50}Ga_{0.50}As$	0.200	----	
	GaAs	0.005	----	
	GaAs	0.250	----	
	GaAs	0.500	----	

er	Composition	Thickness (μm)	Doping	Comments
*421	$Al_{0.50}Ga_{0.50}As$	2.000	----	Growths 421-424 had undoped $Al_{0.5}Ga_{0.5}As$ buffer layers grown at 640°C, no underlying MBE GaAs layer, and doping profiles optimized by Sn predeposition
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.300	Sn	
*422	$Al_{0.50}Ga_{0.50}As$	2.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.250	Sn	
*423	$Al_{0.50}Ga_{0.50}As$	2.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.250	Sn	
*424	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	$Al_{0.50}Ga_{0.50}As$	1.000	----	
	GaAs	0.010	----	
	Sn/As		Sn predeposition	
	GaAs	0.250	Sn	

* Slices used for device fabrication

fer to insure that complete pinch-off occurred at 3-5 volts applied bias. For better device linearity, doping profiles were adjusted so that the carrier concentration was slightly higher near the active layer-buffer interface, decreasing nearly linearly toward the wafer surface.

One of the most important considerations is the saturated drift velocity of carriers in the active layer near the active layer-buffer interface. This will be influenced by the doping in the active layer, the mobility in the active layer, and the extent to which energetic carriers in the GaAs active layer interact with deep levels in the AlGaAs buffer. In general, it is important to achieve the highest mobility possible near this interface, and use AlGaAs with the lowest possible density of deep levels, traps, etc.

The choice of n-type dopant for the GaAs active layer was influenced by the desire to obtain an appropriate abrupt profile at the active layer-buffer interface. The n-type dopants available to us during this project were Ge and Sn. SnTe was also introduced into the MBE chamber for use as an n-type dopant, but was removed and never actively used because of a coincidental abrupt increase in n-type background doping (later determined to have been most probably due to Ge, not the SnTe). Sn doping yields high n-type mobilities and is not sensitive to the details of MBE growth, such as As/Ga ratio. However, Sn doping suffers from a surface segregation phenomenon which makes abrupt changes in doping level difficult to achieve. Therefore, initial experiments were done with Ge doping (Table 1, 208 to 262). Ge produces n-type GaAs under the usual As-rich MBE growth conditions, and can be used to create extremely abrupt junctions. However, Ge is amphoteric, and the degree of compensation of a Ge-doped MBE epilayer therefore depends on growth details such as substrate temperature and the ratio of As flux to Ga flux. Extremely high As/Ga ratios must be used to reduce compensation in n-type material, and the resulting mobilities are generally lower than those obtained using Sn. Therefore, although abrupt profiles could be obtained with Ge, it was soon abandoned because of difficulties in obtaining reproducibly high mobilities.

The method used to obtain abrupt profiles with Sn doping was to build up a surface accumulation of Sn prior to growth of the active layer. This Sn then will ride along on or near the growing GaAs surface and will be incorporated into the growing layer at a rate determined by substrate temperature, growth rate, and Sn surface coverage. This is a well-known MBE process and has been discussed extensively by Wood.[3] By choosing an appropriate Sn predeposition flux and time, it was possible to tailor the doping profile of the active layer (Table 1, 283-287, 342-360, 421-424). Results obtained by this method are discussed in Section 3.1. Since the surface of AlGaAs is much more reactive than that of GaAs, in general the AlGaAs buffer layers were covered with 50Å of epitaxial GaAs before beginning the 10 min to 20 min Sn predepositions. Typically, the As flux used during GaAs growth remained on during the Sn predeposition, with the Ga source being shuttered off.

Growth of high quality AlGaAs by MBE requires a good deal of effort and is not completely understood. Neither is the role of oxygen in semi-insulating AlGaAs well understood. Our approach to growth of buffer layers was to attempt to grow the highest purity AlGaAs possible at the time, then to add O_2 (or H_2) to look for differences in the material behavior. The MBE chamber vacuum background composition, Al and Ga source designs, and Al starting material all can affect the AlGaAs quality. Improvements were made in all these areas over the course of the experiment. A 10°K cryogenic pump was added to the MBE chamber to pump background gasses, particularly CO. This pump was also useful in pumping out O_2 or H_2 admitted to the growth chambers purposely. Sources were redesigned to minimize the possibility that contaminants originating on the hot heater windings could impinge on the substrate. Starting material handling and source degassing procedures were also improved to decrease the possibility of contamination.

In addition to vacuum and source considerations, the growth conditions to AlGaAs can have large effects on material quality. For growth of the best MBE AlGaAs laser material, substrate temperatures of 640°C and above have been used in conjunction with relatively low As/Ga ratios. Therefore, in the

stages of this program we grew many of the AlGaAs buffer layers at or near 640°C. The combination of the improved vacuum, redesigned sources and improved growth procedures resulted in dramatic increases in mobilities of n-type AlGaAs. Undoped AlGaAs remained semi-insulating, however. The addition of H_2 to the growth chamber had no measurable effect on the AlGaAs properties.

2.2 Heterostructure Field Effect Transistors

The concept of a heterostructure interface between an active layer and a buffer layer can have very promising properties when related to the performance of depletion mode, field effect devices. Because of the heterostructure nature at an interface, the wide bandgap buffer layer can partially deplete the narrower bandgap active layer and produce carrier confinement in the active layer away from the interface. This is the case for an AlGaAs buffer layer onto which a GaAs active layer is grown although the details of the interface suggest certain limitations on the degree of carrier confinement and the subsequent performance advantage of this material system.

2.2.1 Theory of Operation

Since $Al_xGa_{1-x}As$ has a larger bandgap than does GaAs, it is anticipated that if the Fermi level can be pinned at mid-gap, either by introducing deep impurity levels or by growing "intrinsic" material, the room temperature resistivity of $Al_xGa_{1-x}As$ should exceed that of semi-insulating GaAs. Because of the good lattice match between GaAs and $Al_xGa_{1-x}As$ one does not anticipate any significant density of interface states in this system as theoretical calculations by Schulman and McGill[4] and by Pickett, Louie and Cohen[5] have confirmed. Therefore, interface states are not expected to pin the Fermi level at mid-gap. The energy gap discontinuity ΔEg between $Al_xGa_{1-x}As$ and GaAs is distributed at the interface partly in the valance band ΔE_v and partly in the conduction band ΔE_c so that $\Delta Eg = \Delta E_v + \Delta Ec$. For x = 0.2 to 0.5, $\Delta E_v = 0.15\ \Delta Eg$ and $\Delta E_c = 0.85\ \Delta Eg$ where ΔEg is the discontinuity in the direct

bandgaps[6,7] This discontinuity is caused by the natural tendency for the transition of the electron affinities, χ, of both materials to be continuous across the interface.[8] The presence of such band discontinuities can lead to carrier confinement in either or both of the materials of the heterojunction.

The major effort of this project is to study the device characteristics and advantages, if any, of the wide bandgap, semi-insulating AlGaAs to n-type GaAs heterostructure. In Fig. 1 the energy band diagrams of both n-GaAs on S.I.-AlGaAs and n-GaAs on S.I.-GaAs are shown under conditions of thermal equilibrium. It can be seen that although AlGaAs has a wider bandgap than GaAs, the structure on semi-insulating GaAs introduces a somewhat larger self-depletion width into the active layer than that of the AlGaAs buffer layer. The Debye length for free carriers in GaAs ($n = 1.5 \times 10^{17}$ cm^{-3}) is approximately 160Å.

The question to be investigated is the effect of the interface under operational conditions. As the Schottky gate is pulled to a negative potential, electrons are depleted and the remaining carriers are confined somewhere away from both the surface and the interface in both cases (Fig. 2). Energetic electrons which reach the interface are in some sense eventually scattered back into the channel. The anticipated advantage of the AlGaAs buffer layer is that the abrupt potential barrier will significantly reduce the number of carriers which penetrate into the semi-insulating region and subsequently re-enter the channel with a phase delay.

The practical trade-offs to be encountered are the relative trap densities at the interface for the two structures and, for carriers which enter the semi-insulating region, the effect on phase delay related to the degraded mobility in AlGaAs as compared to that of GaAs.

2.2.2 Analysis Techniques

In the development of most any microelectronic device a well prepared characterization procedure must follow device fabrication. Given a set of final device performance parameters, the task of pinpointing the reasons for

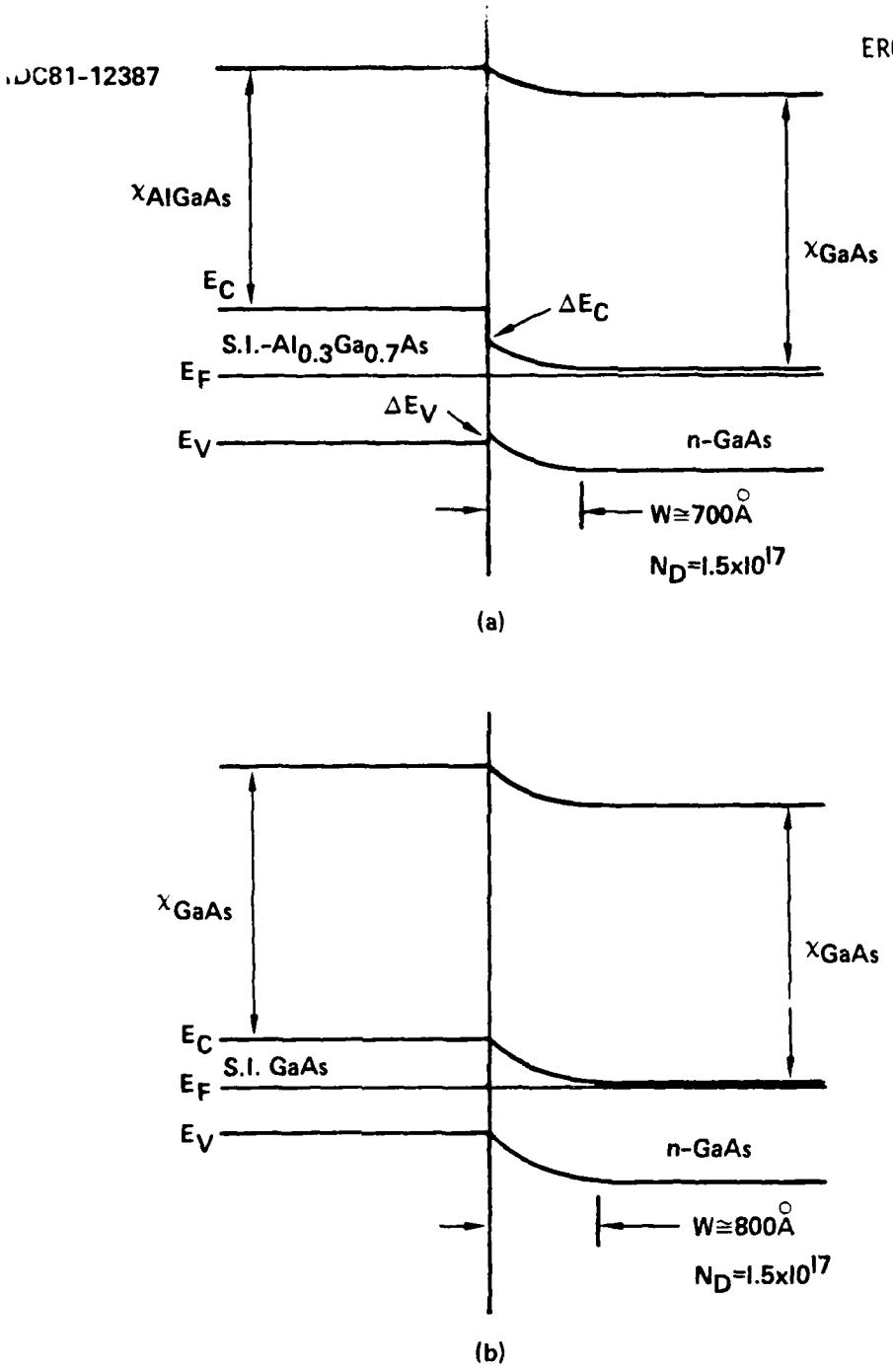


Fig. . Comparison of n-GaAs on (a) S.I. AlGaAs and (b) S.I. GaAs.

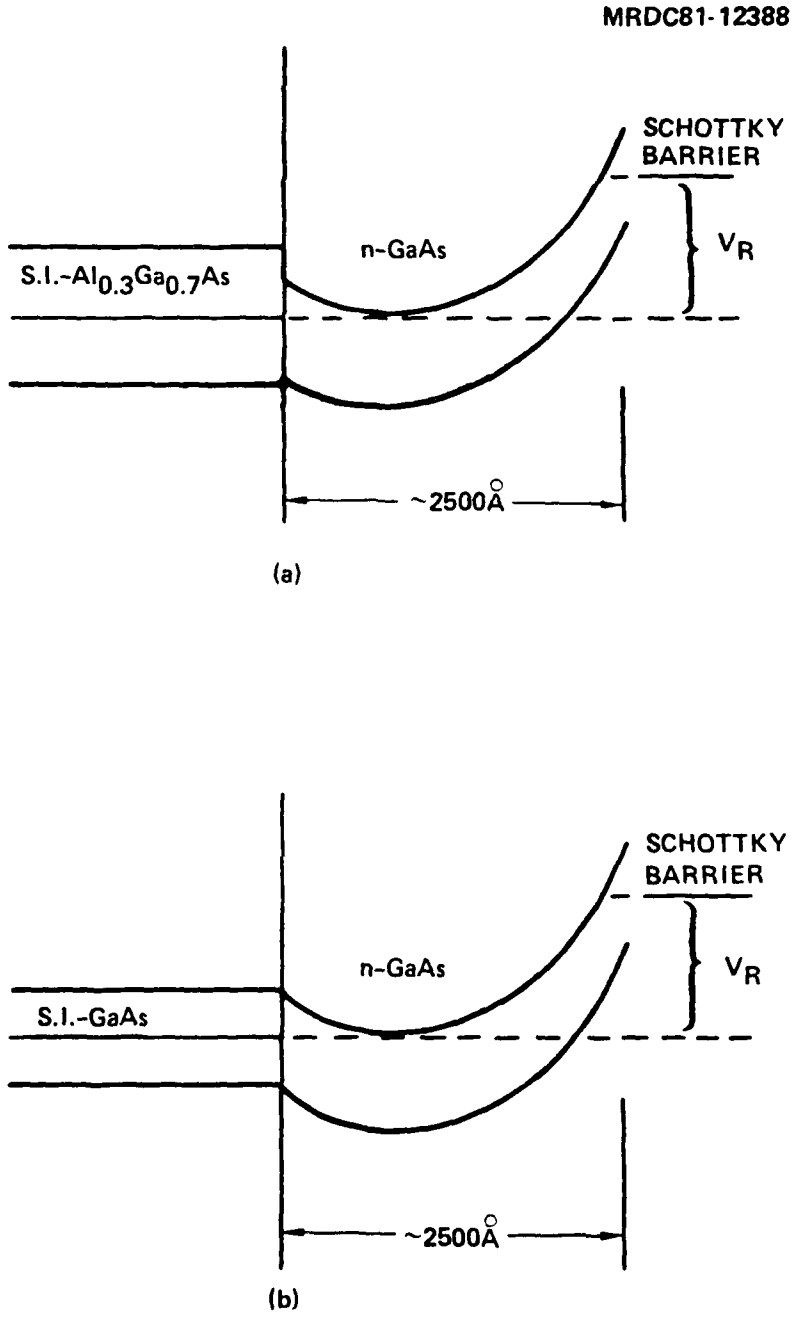


Fig. 2 Comparison of n-GaAs on (a) S.I. AlGaAs and (b) S.I. GaAs under conditions of static reverse bias.

...ies or poor performance can be tedious if not impossible. There are several analytical tools and techniques available which allow the independent measurement of most factors which together determine the final performance of GaAs field effect transistors.

The high frequency equivalent circuit of an FET is shown in Fig. 3. Also shown is the geometric region responsible for each element of the equivalent circuit. The principal elements of interest are the ohmic contact resistance, the gate resistance, the modulated and unmodulated channel resistances, and the depletion capacitance. Directly and indirectly these elements give rise to determinations of device noise and gain, transconductance, device pinchoff, drift mobility, and other parameters.

2.2.2.1 DC Analysis

The effect of ohmic contact resistance on the performance of FETs is well documented.[9] Ohmic contacts play a significant role in FET noise performance and gain.

Contact resistance is then one of the most obvious and important parameters to keep track of in the fabrication of FET devices. Resistances for contacts on thin conductive layers can be measured by a variable gap method.[10] As shown in Fig. 4 the contact resistance is determined by measuring the resistance between a series of adjacent ohmic contact pads. These resistances are then plotted with respect to pad separation distance and the least squares fit intercept is twice the effective contact resistance. The geometry independent effective contact resistance for planar structures, in units of Ω-mm, is then obtained by multiplying the intercept resistance by the pad width in millimeters.

Desirable information concerning the active layer can be obtained from measurements of depletion capacitance vs. voltage and transconductance vs. voltage. These measurements, performed on a long gate FET, provide free carrier concentration profiles and drift mobility profiles. The importance of C-V and N-D profiles has been previously shown.[11,12] As far as mobility is

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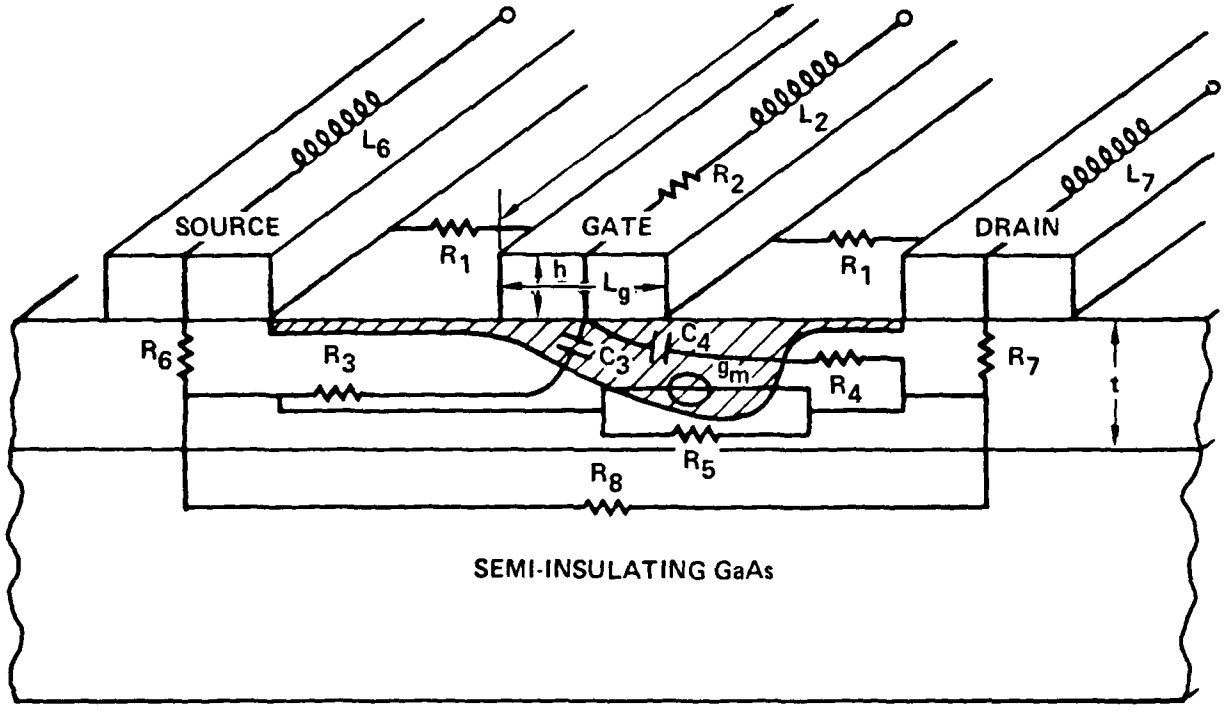

CROSS-SECTION OF AN FET

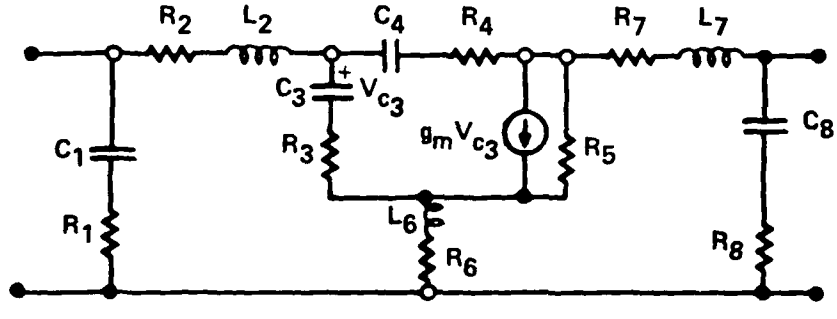

Fig. 3 High-frequency equivalent circuit of an FET.

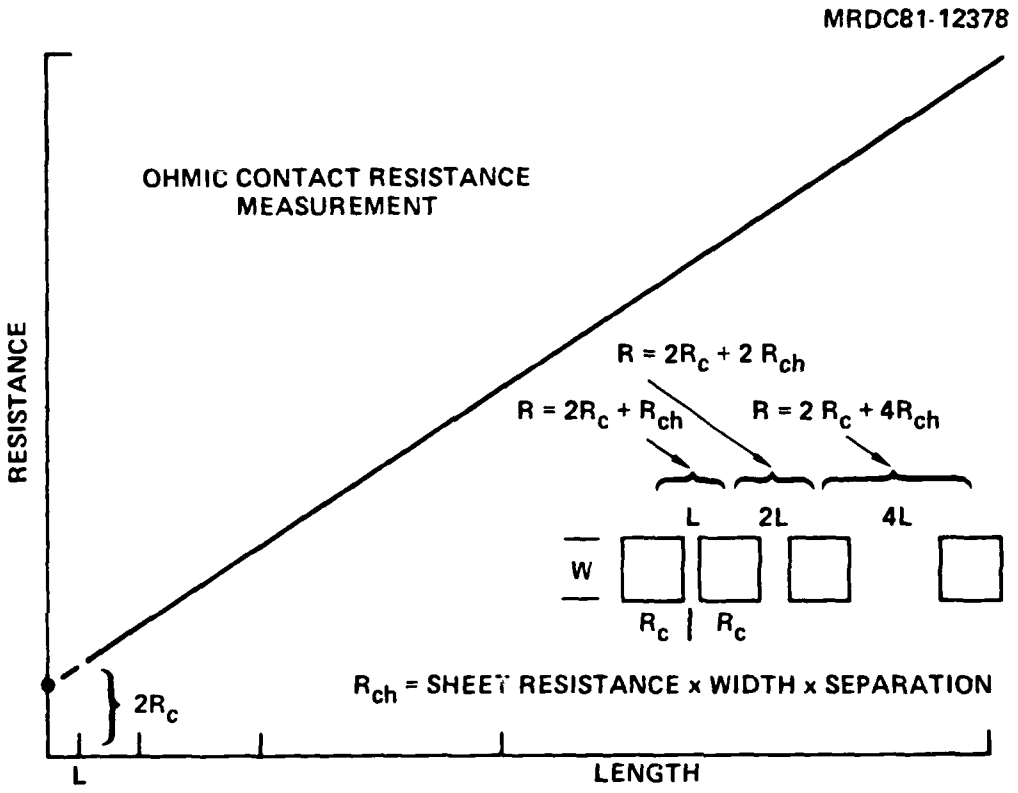

Fig. 4 Ohmic contact resistance measurement.

erned, although the average Hall mobility is a figure of merit for active layers and can pinpoint some processing induced problem, it does not bear a strong relationship to the operational properties of a FET. On the other hand drift mobility is a much more meaningful parameter in analyzing device performance.

The drift mobility in the linear region of a FET is given by

$$\mu_d = \frac{g_m L_G^2}{C_g V_D} (1 - R_p G_{ch})^{-2} \quad (1)$$

where L_G is the gate length of a long gate FET and V_D is the drain bias. The quantity in the brackets is a correction factor important near zero gate bias. Ohmic contact resistance and the sheet resistance of the active layer between the gate-drain and gate-source region is given as R_p. This value can be determined from ohmic contact resistance data. The channel conductance (G_{ch}), transconductance (g_m), and depletion capacitance (C_g) can all be measured by phase sensitive detection techniques. Shown in Fig. 5 is a block diagram of the instrumentation and circuitry. Appropriate switching of the sources and terminations provides the capability of direct measurement of equivalent parallel capacitance and conductance. This technique measures differential rather than static parameters. That is,

$$C = \frac{dQ}{dv} \text{ and } G = \frac{dI}{dv} \quad (2)$$

with the assumption that the dependence of capacitance and conductance on voltage is only slowly varying.

It is known that if a function and its derivatives are regular in some continuous region of ordinary points, that function can be written as a Taylor series expanded about a point in that region. Specifically, the considerations are the cases of charge on a capacitor and current in a conductor as functions of the voltage applied across those elements. The voltage V is the sum of a constant or slowly varying part and the series of a time varying

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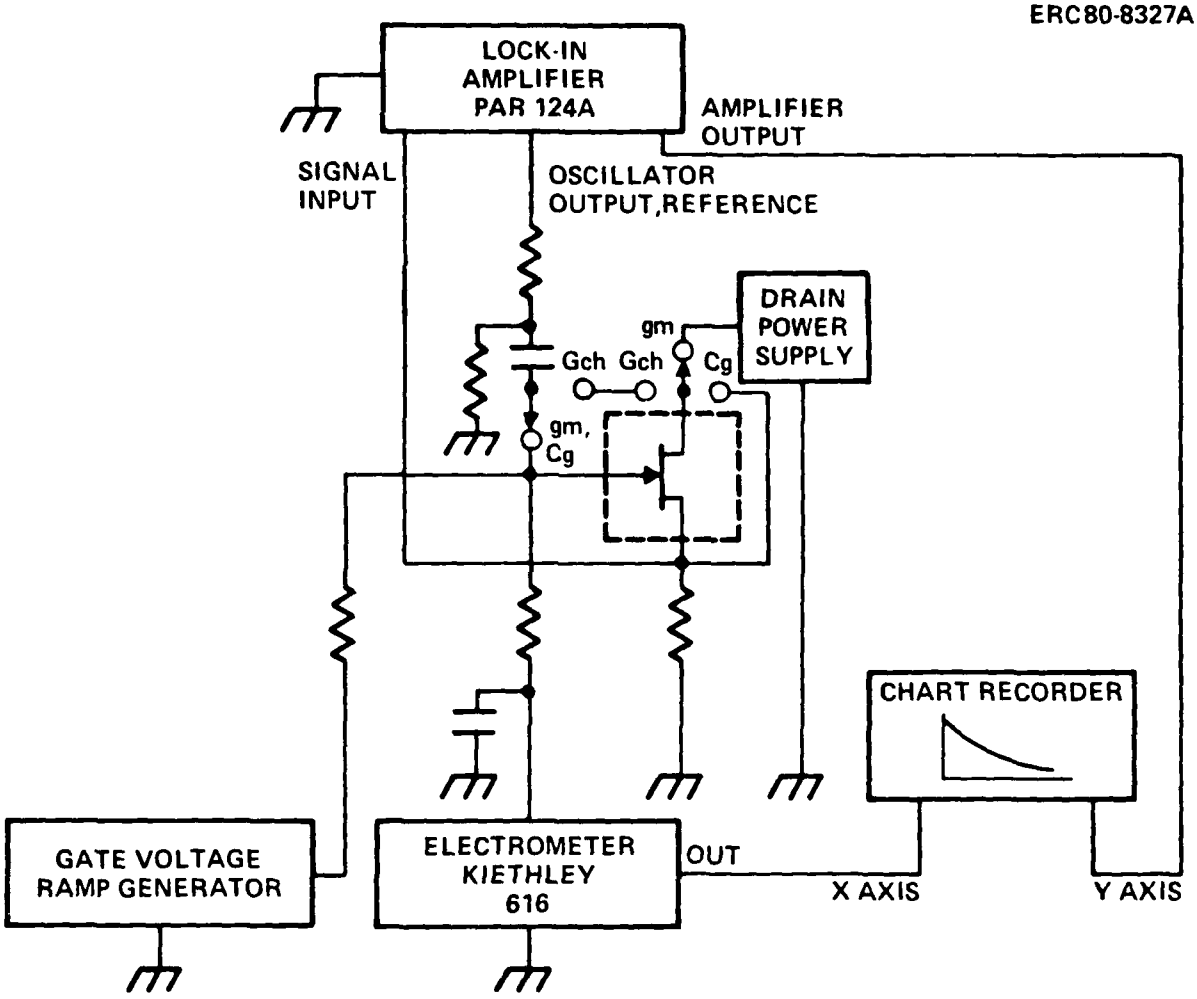

TEST SET FOR MEASUREMENT OF FET ADMITTANCE

Fig. 5 Test set for measurement of FET admittance.

soidal and harmonics with possible phase shifts,

$$v = v_o + v_\omega \sin \omega t + v_{2\omega} \sin (2\omega t + \theta) + \ldots \tag{3}$$

By expressing Q in terms of the common Taylor series,

$$Q = Q(v_o) + \Delta v \left.\frac{dQ}{dv}\right|_{v_o} + \frac{1}{2} (\Delta v)^2 \left.\frac{d^2Q}{dv^2}\right|_{v_o} + \ldots \tag{4}$$

and acknowledging that Δv represents the time varying terms in the given voltage the result is,

$$Q = Q(v_o) + v_\omega \sin(\omega t) \left.\frac{dQ}{dv}\right|_{v_o} + \frac{v\omega\ v_{2\omega}}{2} \cos (\omega t + \theta) \left.\frac{d^2Q}{dv^2}\right|_{v_o}$$

$$+ v_{2\omega} \sin(2\omega t + \theta) \left.\frac{dQ}{dv}\right|_{v_o} - \frac{v\omega^2}{4} \cos(2\omega t) \left.\frac{d^2Q}{dv^2}\right| + \ldots \tag{5}$$

closer inspection reveals that with proper signal purity Eq. (5) is directly proportional to differential capacitance at the signal frequency. The time derivative of this equation gives rise to the displacement current associated with a capacitor. That is,

$$i_\omega = \omega v_\omega \cos \omega t\ C\Big|_{v_o} \tag{6}$$

For the analysis of channel conductance, at any given gate voltage

$$i = i(v_o)\Big|_{v_G} + \Delta v \left.\frac{di}{dv_d}\right|_{v_o,\ v_G} + \ldots \tag{7}$$

Here the drain current is given as i and the drain voltage has a constant part v_o and a time varying part Δv. The drain current at the signal frequency is given by

$$i_\omega = v_\omega \sin(\omega t)\ G_{ch}\Big|_{v_o, v_G} \tag{8}$$

In this measurement v_o is normally zero or held fixed and v_G slowly varies.

Transconductance is analyzed similarly such that for any given drain voltage v_D,

$$i = i(v_o)\Big|_{v_D} + \Delta v \frac{di}{dv_G}\Big|_{v_o, v_D} + \ldots \tag{9}$$

In this case the drain current i is evaluated from the series with the gate voltage assuming a constant or slowing varying part v_o and a time varying sinusoidal part Δv. The drain voltage v_d is normally held constant at a small value placing the transistor in the linear region. The drain current at the signal frequency is given by

$$i_\omega = v_\omega \sin(\omega t)\ g_m\Big|_{v_o, v_D} \tag{10}$$

2.2.2.2 *RF Analysis*

The most important performance parameters of low-noise transistors are the minimum noise figure and the associated gain. Accordingly, strong emphasis has been placed on developing low-loss test circuits with wide tuning flexibility and on refining the test procedures. The test set developed for this purpose is shown in Fig. 6. A broad-band coaxial switch (1) is used to apply a low level signal for measuring gain or the output of a modulated noise source for determining the noise figure. A circulator (2) is inserted in front of the test circuit to prevent VSWR variations between the hot and cold states of the noise source from interferring with the noise measurement. A crystal detector terminates the third port of the circulator to facilitate input tuning for obtaining maximum gain. The input tuner is adjusted for minimum reading on the automatic noise-figure indicator in establishing the minimum noise figure, while the output is tuned for maximum gain reading on the output-power meter. A high-gain low-noise amplifier (3) is employed to

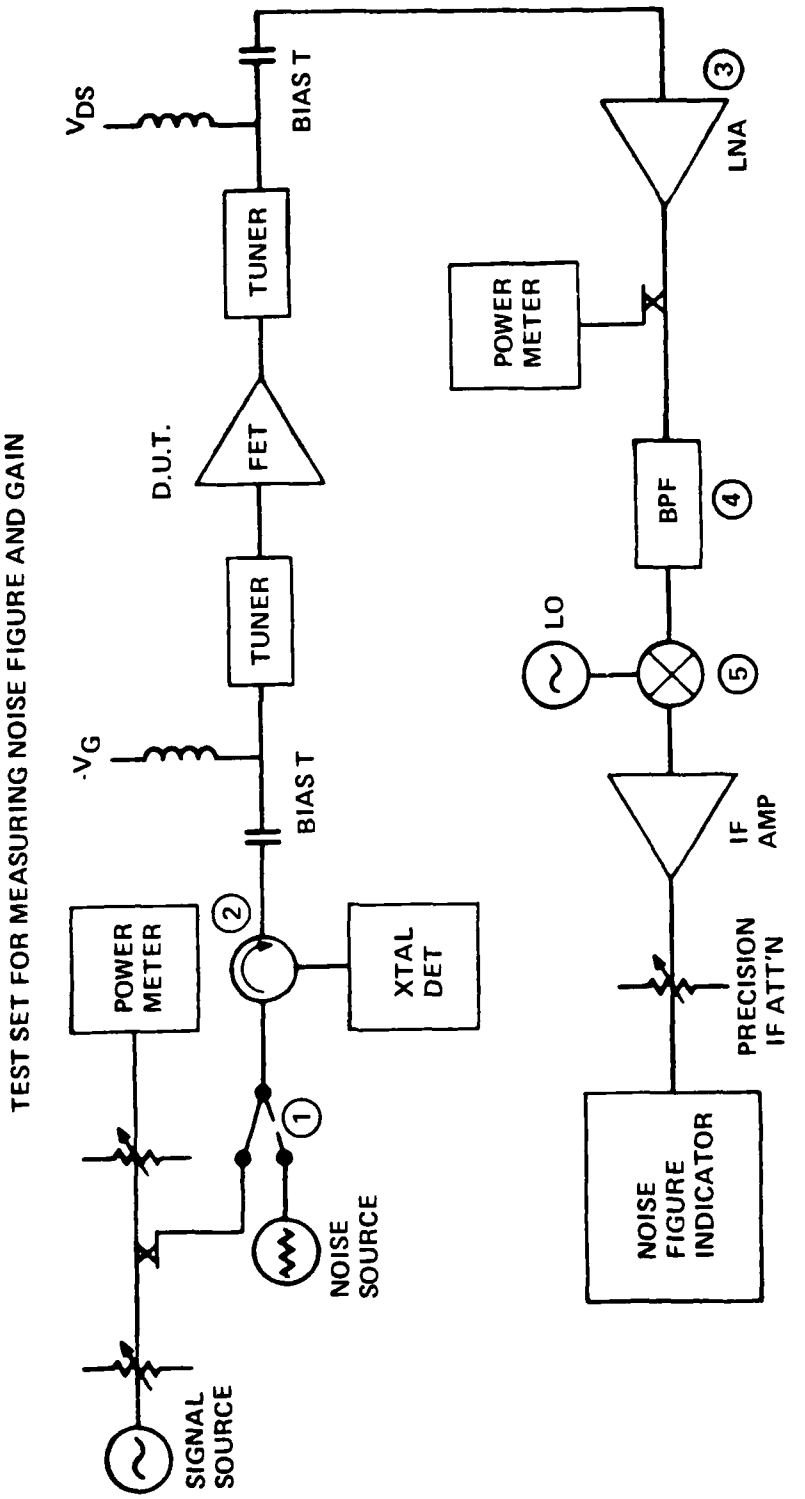

Fig. 6 Noise figure and gain test set.

minimize the noise contribution of the measurement system. Uncertainties due to gain variations vs. frequency are eliminated by inserting a bandpass filter (4) in front of the mixer (5) which passes the signal frequency and provides greater than 40-dB rejection of the image frequency. A calibrated precision IF attenuator is inserted in front of the noise-figure indicator to permit noise measurements by the Y-factor method. This option serves to eliminate errors associated with nonlinearities and inaccurate tracking in the noise-figure indicator.

Three differennt low noise front ends (3,4,5) can be used to cover the frequency range from 4 to 15 GHz. The resulting system noise, referred to the device under test, is about 3 dB in the lower part of the frequency range and increases to about 4.5 dB in the upper part. A test fixture covering 4 to 10 GHz has been designed for evaluating packaged transistors and it has been possible to keep the circuit losses in the range of 0.4 to 0.8 dB by integrating the tuners with the test fixture.

3.0 CHARACTERIZATION AND RESULTS

3.1 Material Result

The major experiments and materials results are summarized in Table 2.

3.1.1 Sn Predeposition for Doping Profile Tailoring

With the use of Sn to obtain higher n-type GaAs mobilities arose the necessity to use Sn predeposition to tailor the doping profile. A number of experiments were conducted to determine the appropriate Sn flux, predeposition time, and substrate temperature to arrive at an appropriate profile. Figure 7 shows a C-V profile of two layers grown under similar conditions, one with Sn predeposition and one without. Without Sn predeposition, over 2000Å of GaAs growth occurred before 10^{17} concentration doping was achieved.

3.1.2 Deep Levels in AlGaAs

The problem of producing high purity AlGaAs with a low density of deep levels is difficult and has apparently now been solved satisfactorily. Doping experiments conducted with n-type AlGaAs indicated that compensating acceptors are present. Whether these are due to impurities or native defects remains a topic of considerable discussion among III-V materials people. During the course of this project, our AlGaAs quality has increased from material which could not be doped n-type with less than $10^{18}/cm^3$ donors (for 10% Al), to material exhibiting mobilities within 30% of the best n-type $Al_{0.3}Ga_{0.7}As$ mobilities reported in the literature. There obviously is room for further improvement; however, it is not known to what extent the remaining compensating acceptors and/or deep levels affect the performance of the AlGaAs buffer devices. Our early measurements made with photoinduced transient spectroscopy indicated a nearly continuous spectrum of traps in MBE AlGaAs, which is shown in Fig. 8. Most improvements in our AlGaAs material have occurred since this time, so the significance of these early results is questionable.

Table 2

Summary of Material Results

Growth Nos.	Experiment	Result Summary
106, 108, 110-114, 199B, 137, 138	GaAs, AlGaAs ρ, μ	GaAs background ~1 × 10^{16} n-type AlGaAs (undoped) high ρ SI.
208-213, 261, 262	Ge-doped active layer growth in H_2	Difficult to achieve appropriate doping and mobility with Ge. No noticeable GaAs mobility improvement or change in AlGaAs Properties
261, 262	Growth of AlGaAs	High ρ AlGaAs, no noticeable difference from material w/o O_2 background
283-287	Sn predeposition, O_2 background vs no O_2 for AlGaAs	Achieved suitable Sn profiles with predeposition; no noticeable effect due to O_2 background during AlGaAs growth
302, 303, 319	MIS structures using $Al_{0.5}Ga_{0.15}As$, AlAs (oxidized)	C-V showed large amount of leakage properties
342, 343, 351-360, 389	Optimization of active thickness and doping using Sn predeposition	Achieved suitable profile, but electrically active layer depth (by C-V profiling) less than metallurgical layer thickness.
	Variation of substrate temperature of $Al_{0.5}Ga_{0.15}As$ buffer growth	No changes noticed
421-424	Attempt to use best conditions, no underlying GaAs buffer to reduce output shunt	

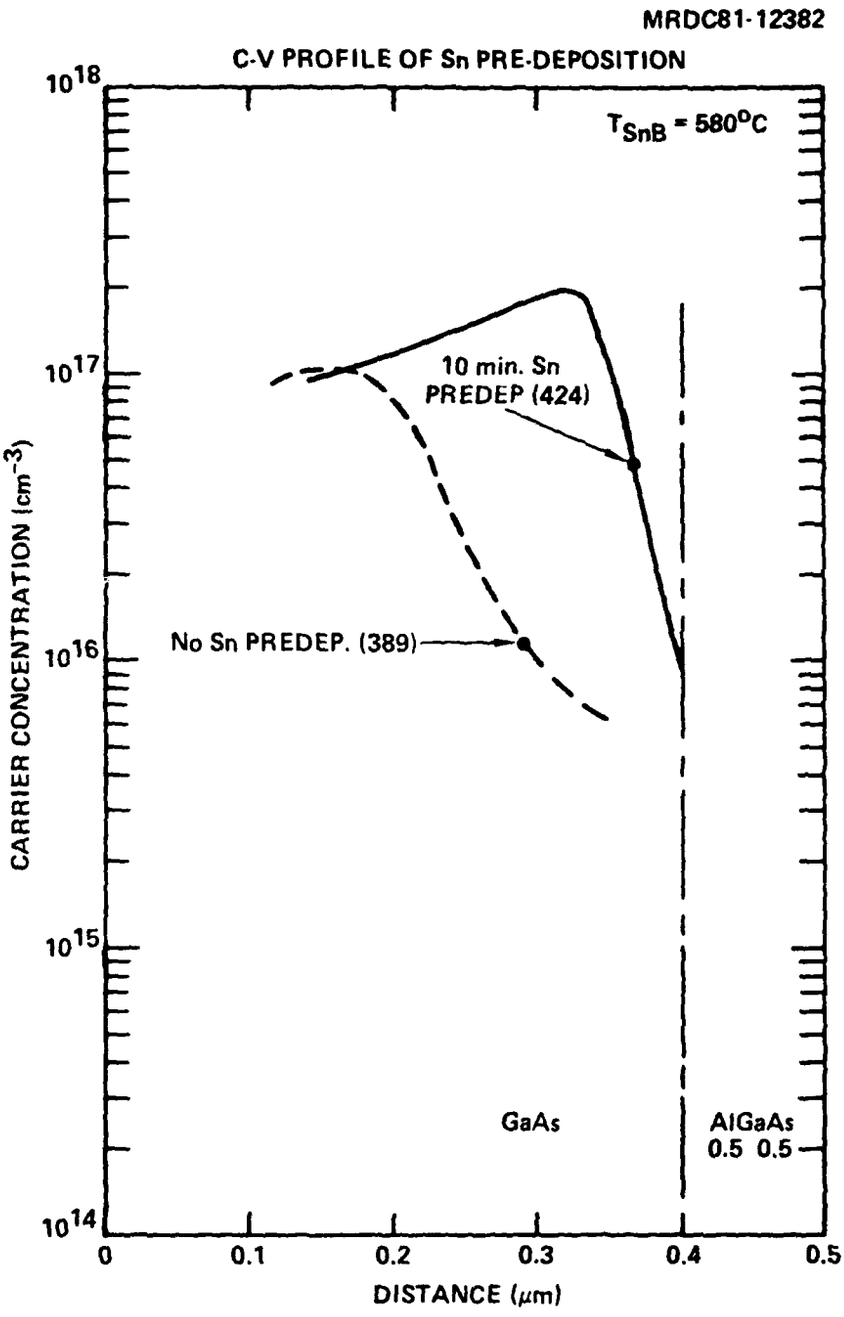

Fig. 7 C-V profile of Sn predeposition.

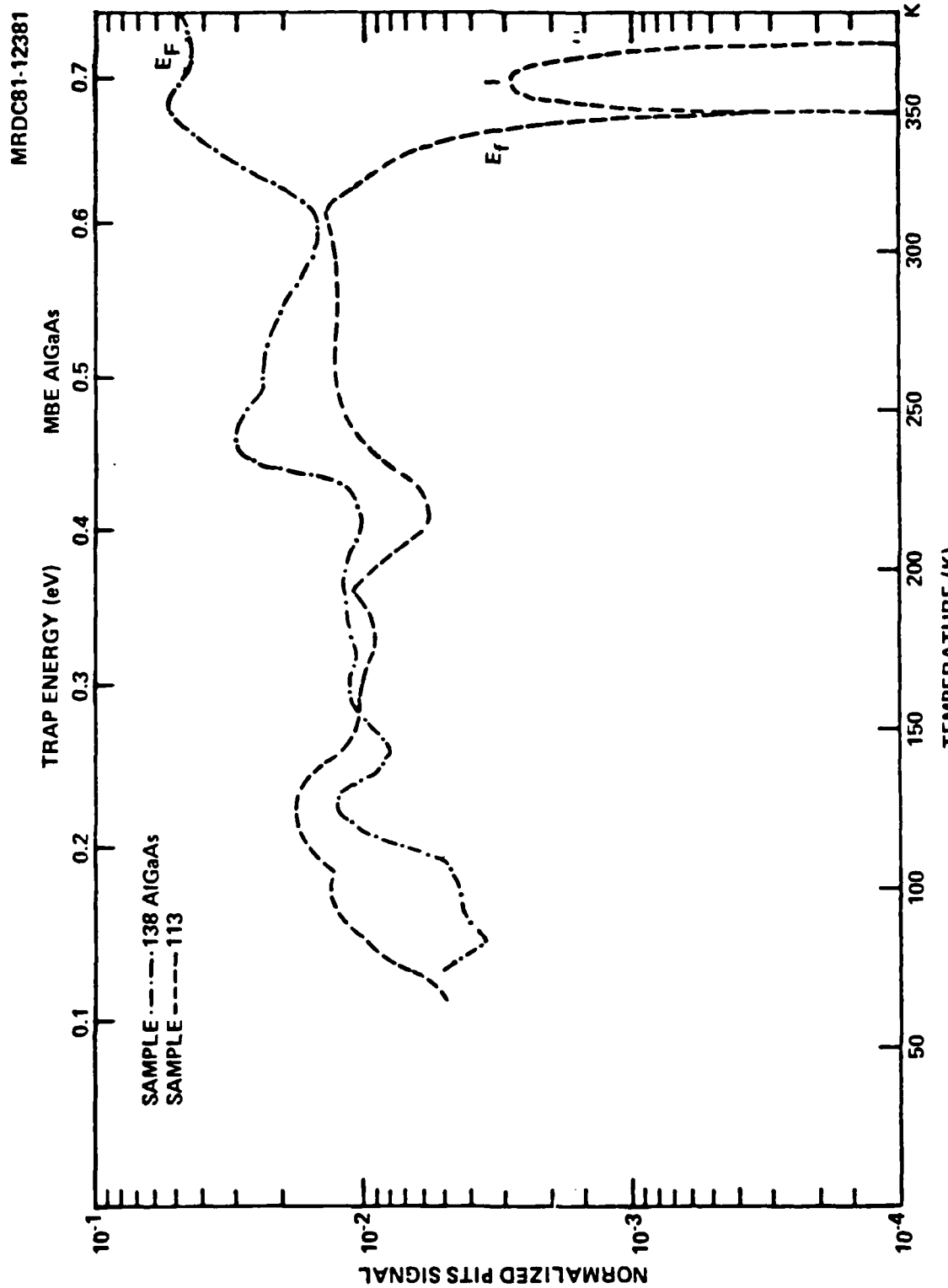

Fig. 8 PITS spectrum of MBE AlGaAs.

Many fewer traps are expected as evidenced from the n-type doping experiments mentioned above.

This project has pointed out a number of areas for further investigation. From a materials standpoint, the major unresolved question is related to the transport of majority carriers near the GaAs-AlGaAs heterojunction. Several layers yielded GaAs material with a thickness, deduced from C-V measurements, that were considerably less than the as-grown metallurgical thickness. For growths using Sn as the n-type dopant, most of these difficulties occurred due to the well-known surface segregation effects. The predeposition of Sn on the AlGaAs buffer (covered by 50Å of GaAs) before growth of the GaAs was used to overcome this effect, which normally would leave a very lightly doped region at the interface. The amount of Sn needed to accomplish this, however, was more than expected based on calculations and experience with GaAs-GaAs interfaces. Additionally, even with Ge, which produces abrupt doping profiles, the thickness of the doped layer was found to be less than the thickness of the GaAs grown (see Fig. 9). Although it is possible that variations in As/Ga flux ratios or substrate temperature could have produced this type of effect occassionally, the regularity with which it was observed suggests less trivial causes. For future experiments, Si would be a preferred type dopant.

In the period since the experimental portion of this project was considered and the writing of this report, considerable effort has been expended at our laboratory and elsewhere in understanding AlGaAs-GaAs heterojunctions and the effect of AlGaAs material properties on these heterojunctions. Several points pertinent to this project are worth mentioning. In the growth of high mobility structures, in which doped AlGaAs is grown over undoped GaAs, high mobilities are achieved, whereas for the opposite growth direction, achieving high mobilities is much more difficult.[13] There has been considerable speculation (unpublished) over the possibility of diffusion of something out of the AlGaAs into the GaAs grown over it, or of the role of interface roughening at the GaAs-AlGaAs interface. Substrate temperature appears to

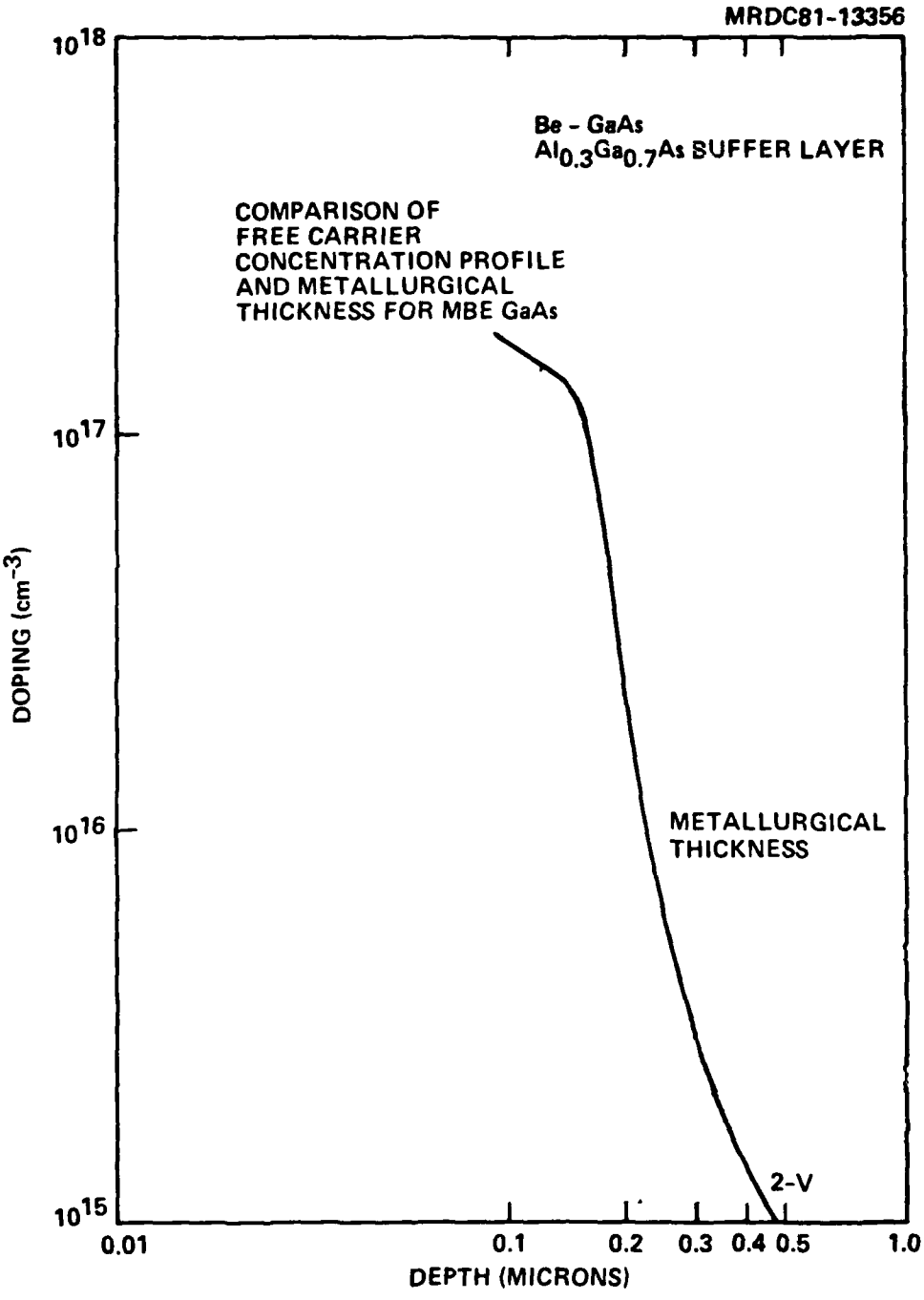

Fig. 9 Comparison of free carrier concentration and metallurgical thickness for MBE GaAs.

play a very large role in determining the suitability of AlGaAs for various device applications. Investigation of the effect of substrate temperature on channel mobility, especially near pinchoff, would be a suitable topic for further investigation. It should be pointed out that the question of growth direction-dependent properties of AlGaAs-GaAs heterojunctions[14] and high mobility structures has not been resolved, and bears directly on the AlGaAs buffer FET design.

The role of impurities or undesired electronic deep levels in the AlGaAs buffer also deserves a more detailed theoretical and experimental investigation. At high source-drain bias, hot carriers may be injected into the AlGaAs buffer layer. Trapping effects with long lifetimes have been observed in these buffers, and are undoubtedly related to impurity-produced deep levels.

3.1.3 MIS Structures by MBE

Several attempts to produce MIS structures by MBE have been made. These experiments consisted of growing n-type GaAs covered with either semi-insulating O_2-doped AlGaAs or oxidized AlAs.[15] C-V profiling was done at several frequencies to determine whether inversion of the GaAs at the insulator interface could be achieved. In neither case was inversion achieved. Deep depletion resulted, accompanied by trapping of injected carriers and photocapacitive effects which lead to hysteresis in C-V characteristics.

The most successful MIS test structure grown by MBE was MBA-319 which consists of a GaAs n^+ substrate, 1 μm n-type (5×10^{16}) GaAs buffer layer, 500Å of undoped $Al_xGa_{1-x}As$ graded from x = 0.5 to x = 1.0, and a layer of AlAs. The AlAs layer was masked by moving a shutter across the face of the wafer at a linear rate. This gave an AlAs layer thickness that ranged from 0.05 μm at one end of the wafer to 0.5 μm at the other end.

Following growth, the wafer was rapidly transferred at 400°C to the MBE chamber airlock. Pure, dry O_2 was admitted to the airlock at a pressure of about 133 Pa (1 torr) to oxidize the AlAs layer. The wafer and holder were

allowed to cool from 400°C in the O_2. The wafer surface was smooth and specular, with no indication of bubbling or cracking. The wafer was then removed to a separate evaporator where 25 μm diameter Au dots 0.2 μm thick were deposited through a shadow mask. The In metal by which the wafer was attached to the MBE substrate holder served as an ohmic back contact. A schematic diagram of the resulting structure is shown in Fig. 10.

Several measurements were made on this structure. Capacitance measurements were made as a function of applied bias (C-V) at 1 MHz, 100 kHz, and 10 kHz, with and without illumination with white light. Conductance was also measured as a function of applied bias (G-V) at 10 kHz and 100 kHz. Breakdown voltages were also measured at several points on the wafer.

Breakdown voltages in forward bias (GaAs in accumulation) ranged from about 7 V to 23 V, for oxidized AlAs layer thicknesses ranging from 850Å to 4000Å. This corresponds to an average electric field at breakdown of 5.7 to 8.2×10^5 V/cm.

Capacitance-voltage curves taken in the dark at 1 MHz and 10 kHz are shown in Fig. 11. There is relatively little difference in the curves for the two frequencies between accumulation and deep depletion, which indicates that few traps or interface states are present which respond with time constants characterized by this frequency range. We do not understand the origin of the increase in capacitance with forward bias past flatband (accumulation), although similar phenomena have been reported with O_2-doped AlGaAs MBE semi-insulating layers.[16]

The shape of the C-V curve, as seen in Fig. 11, indicates that inversion has not been achieved in the GaAs. Inversion, at the measurement frequencies used here, would lead to a C-V curve shown by the dotted line in Fig. 11. The leveling off of capacitance in deep depletion (-20 V bias) seen in Fig. 11 is due to variation in layer doping at the buffer-substrate interface.

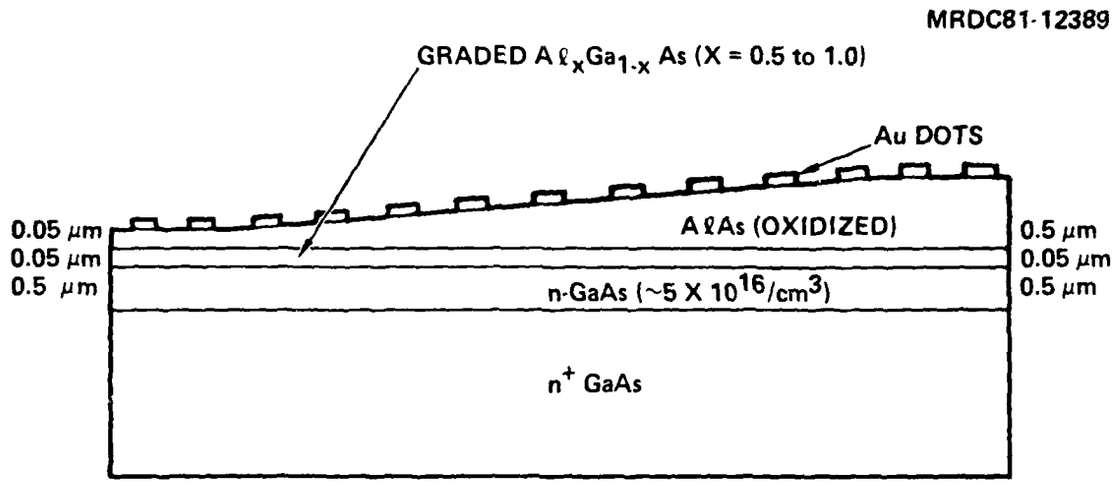

Fig. 10 Schematic of MIS structure.

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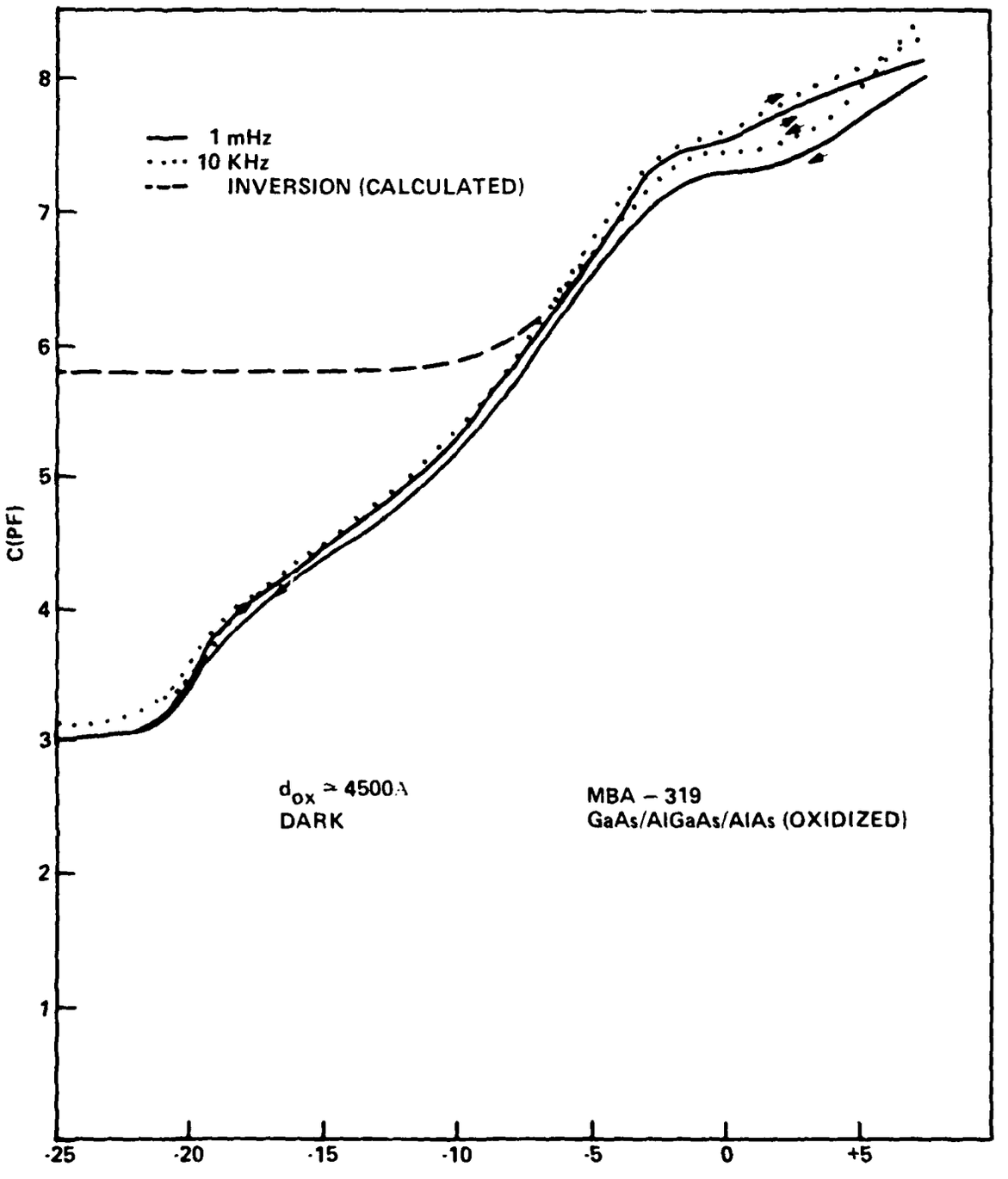

Fig. 11 C-V of MIS structure (dark).

Lack of inversion in these structures could be caused by leakage of holes into and across the AlGaAs and AlAs(O) barrier. This has been suggested to be the cause of very similar C-V curves seen with O_2-doped AlGaAs barrier MIS structures made by MBE.[16] Very high generation/recombination rates caused by interface states at either the GaAs-AlGaAs or AlGaAs-AlAs(O) interfaces could also pin the Fermi level and prevent inversion.

When these layers are exposed to light, differences between 1 MHz and 10 kHz C-V curves become more pronounced, as seen in Fig. 12. Structure also appears in the 10 kHz C-V curve and in the G-V curves at 100 kHz and 10 kHz. The flatband voltage also shifts for both curves. The incident light is therefore changing the population of traps or interface states which communicate rapidly with free carriers in the GaAs. The centering of the conductance spike near the flatband bias suggests it is associated with the AlGaAs region, although it has yet not been determined whether GaAs/AlGaAs interface states, bulk AlGaAs traps, or AlGaAs/AlAs(O) interface states are involved.

Several conclusions may be reached from these initial experiments. First, in situ oxidation of AlAs is capable of producing smooth, tightly adherent insulating layers with good breakdown strength. C-V curves show accumulation and deep depletion, although inversion is not achieved. The frequency dependence of the C-V and G-V curves indicates that the number of interface states is probably small, although more detailed measurements will be needed to determine numerical values. It is not known at this point whether lack of inversion is due to the GaAs-AlGaAs interface, AlGaAs material, or AlGaAs-AlAs(O) interface, or perhaps to some as yet unidentified mechanism.

3.2 Device Results and Performance

3.2.1 Device Fabrication

For this project, device fabrication followed an established low noise FET processing procedure incorporating contact printing mask alignment with changes to accommodate the heterojunction layers. Briefly, the process

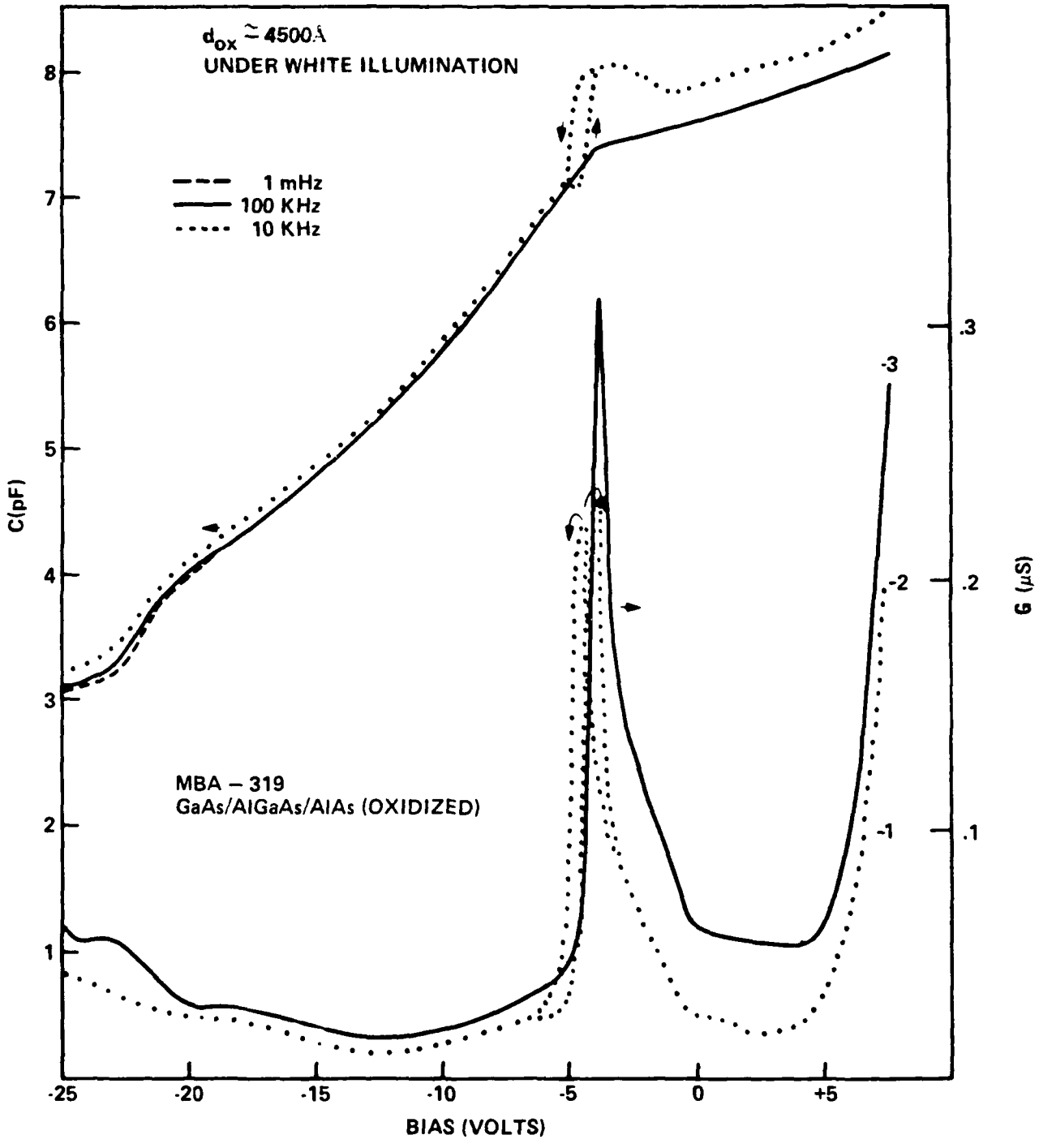

Fig. 12 C-V, G-V of MIS structure (light).

utilizes mesa isolation of the active areas. Experiments were conducted with the heterostructure layers where the isolation etch stopped at the AlGaAs buffer layer and also where the isolation etch proceeded clear to the semi-insulating GaAs substrate. On comparison, there has been no experimental evidence of a difference in device performance. A 5% solution of sodium hypochlorite (NaOCl) followed by a 20:1 solution of H_2O_2:NH_4OH was used as the stop etch whereas a 10:1:1 solution of H_2O:H_2O_2:NH_4OH was used as the standard isolation etch. The ohmic contact system (for the source and drain) is an Au-Ge layer of eutectic composition covered with a thin layer of Pt which is alloyed at 450°C. The Schottky barrier gate metallization system is a Ti/Pt/Au combination having a total thickness of approximately 0.5 μm. The device layout exhibits a nominal gate length of 1 μm and a gate width of 300 μm within a source to drain spacing of 3.5 μm. Figure 13 is a micrograph of the transistors and in Fig. 14 the test circuitry. Included in the processing were control slices of both ion implanted and vapor phase epitaxy layers of GaAs. This maintained verification that the fabrication process could produce high performance devices.

Of the slices mentioned in Table 1, several were specifically grown for device fabrication. These followed design rules recommended by computer analysis. Twenty-five slices were processed in all. Initially, the problems confronted were wafer flatness and removal of an indium residue used in a substrate attachment scheme for MBE layer growth. The flatness problem was eliminated by proper substrate selection and the growth process did not subsequently alter the initial condition. Removal of the indium in the first few slices was accomplished by etching in warm HCl with the wafer surface protected with photoresist. The wafer surface was sufficiently protected but the substrate backside was badly pitted and very thin in places due to irregular etching. As a result of this procedure the wafers were subject to breakage and alignment difficulties were increased by not being able to hold the wafers with chuck vacuum. The final solution was found by wet lapping with a silicon carbide abrasive to a final wafer thickness of approximately twelve mils. This thinning, about eight mils, removed virtually all of the residue. The final slices presented very few problems for standard processing.

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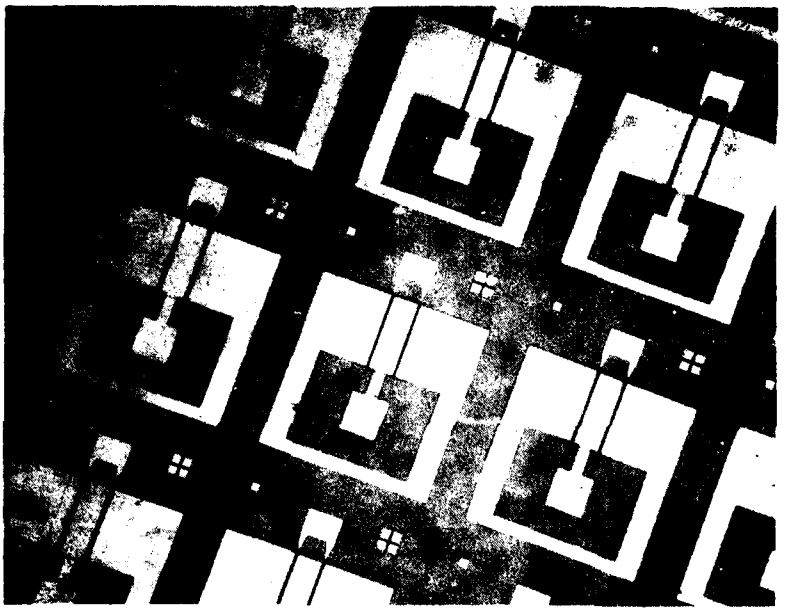

Fig. 13 Carrier confinement field effect transistors.

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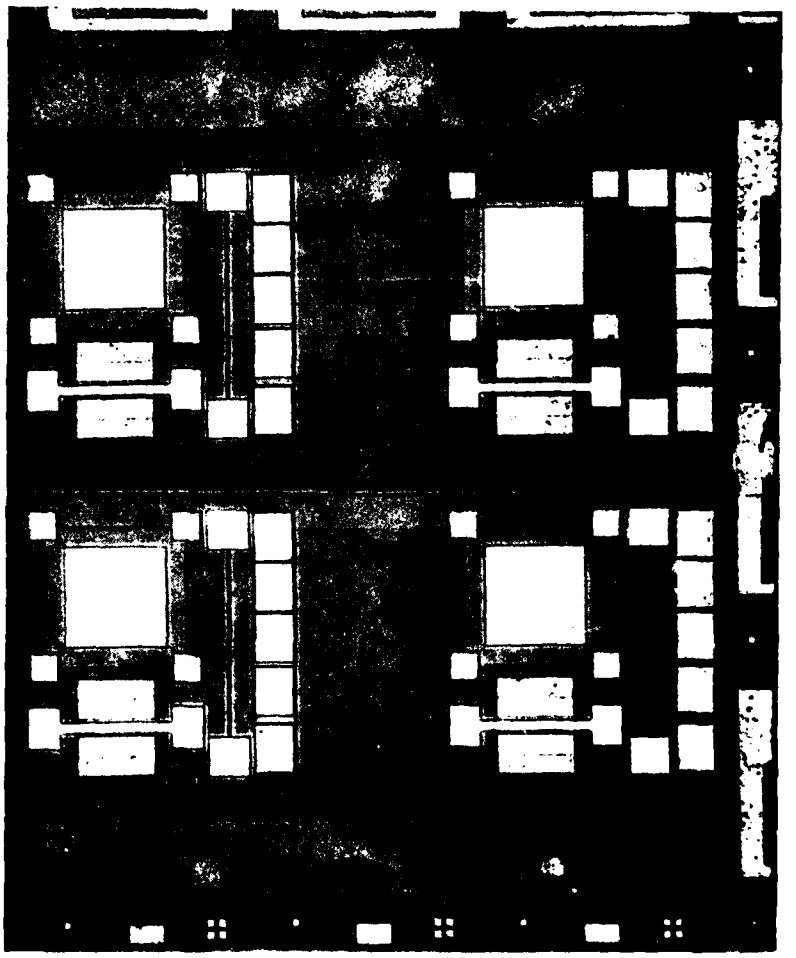

Fig. 14 Characterization test pattern.

3.2.2 Low Frequency Device Analysis

All of the MBE slices, after processing, suffered from a very low frequency or long time constant (500 msec to 3 sec) fluctuation in drain current and transconductance as shown in Fig. 15. This was observed in low frequency (curve tracer, lock-in measurements as well as strictly d.c. measurements. Compensation circuitry was used to prevent obvious oscillation but this type of effort did not alter the current fluctuation. The aperiodic fluctuations displayed 20% to 40% changes in current and even larger changes in transconductance.

The fabrication process produced exceptional ohmic contacts on most of the layers. This is shown in Fig. 16. Here the effective contact resistance as discussed earlier is determined to be 0.5 Ω-mm. This calculation uses the 75 μm width of the ohmic contact test pattern. The error bars simply show the different sheet resistivities of the several layers, yet all have nearly the same ohmic contact resistance. This sheet resistance is found by multiplying the slope in Fig. 16 by the test pattern width. The results indicate sheet resistances of approximately 675 ohms per square. This value is commensurate with that expected and necessary for the device goals.

Measurements of drift mobility were quite successful on the ion-implanted and vapor phase epitaxy devices. The unstable nature of the MBE devices, as previously mentioned, prevented detail analysis of such things as drift mobility, although this parameter can be approximated from curve tracer data. Figure 17 shows data as recorded from the test setup shown in Fig. 18. In this figure an ion-implanted device was analyzed; note its close agreement with the Hall mobility, but more importantly, note the increase in mobility toward the semi-insulating region of the structure. These measurements must be done in the linear region of a FET and care must be taken not to overdrive the device. In our experiments the small signal drive was 10 mV rms and the drain bias was 50 mV.

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Fig. 15 I-V of MBE heterostructure FET showing drain current and transconductance fluctuation.

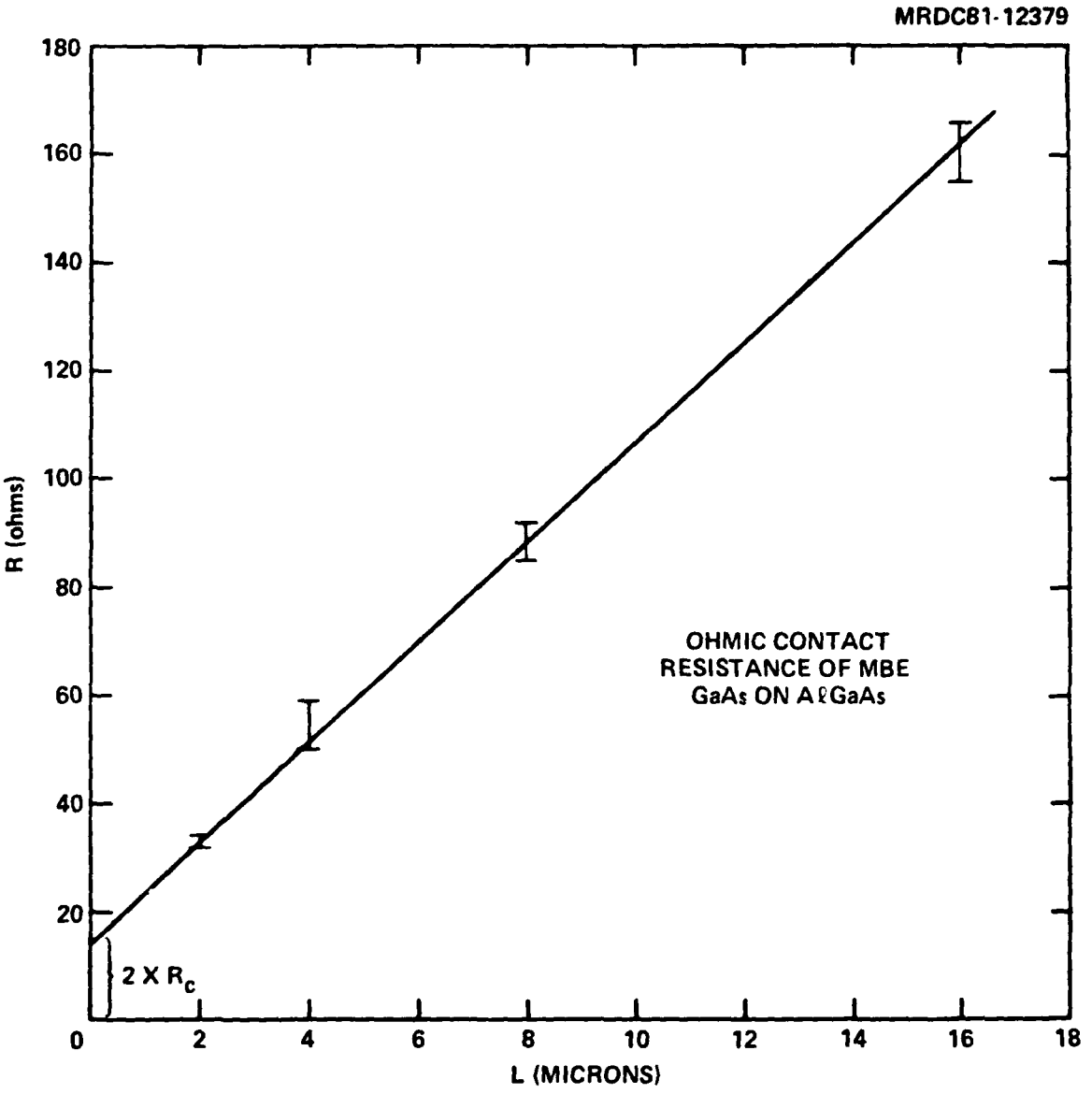

Fig. 16 Ohmic contact resistance of MBE GaAs on AlGaAs.

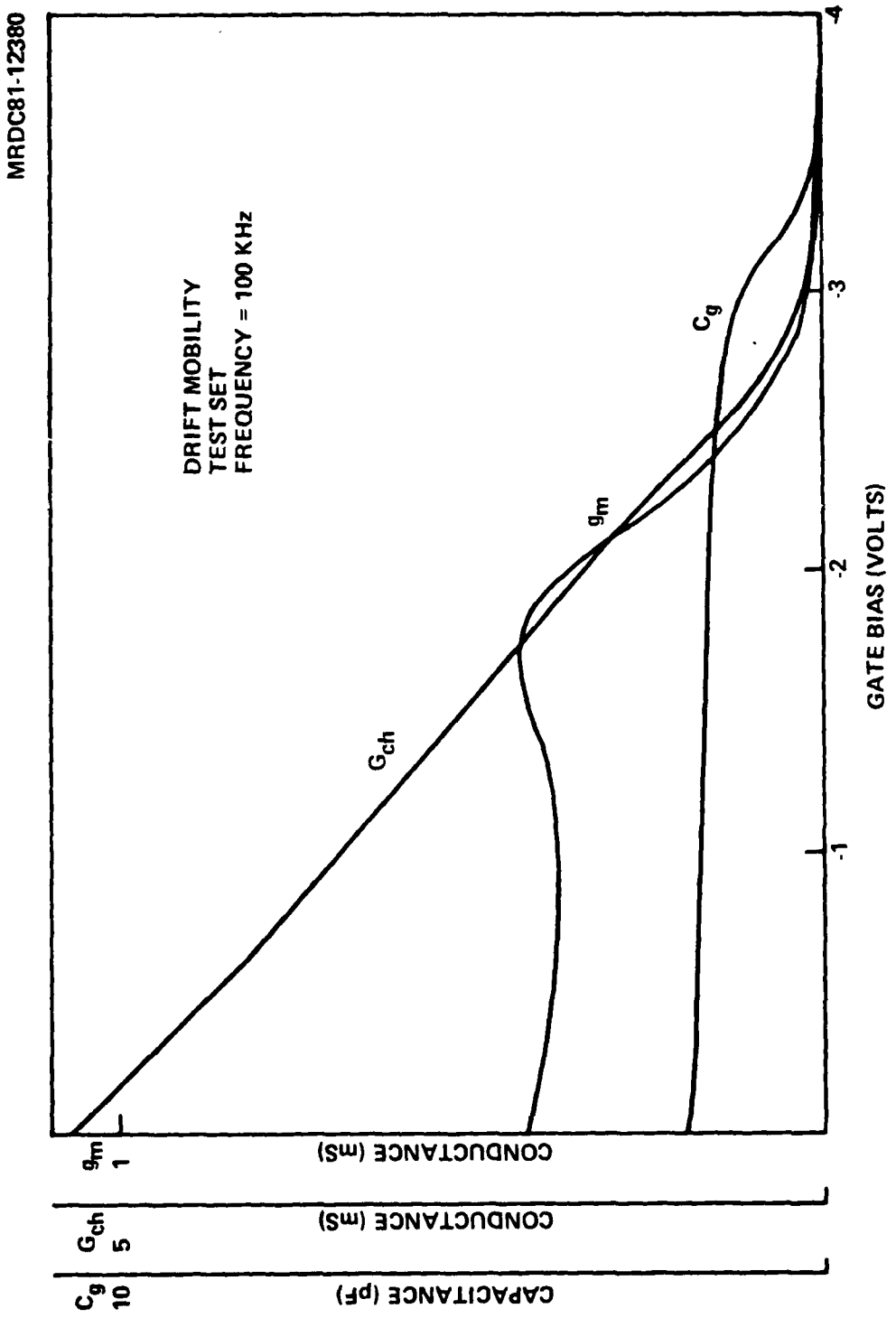

Fig. 17 Drift mobility test set data.

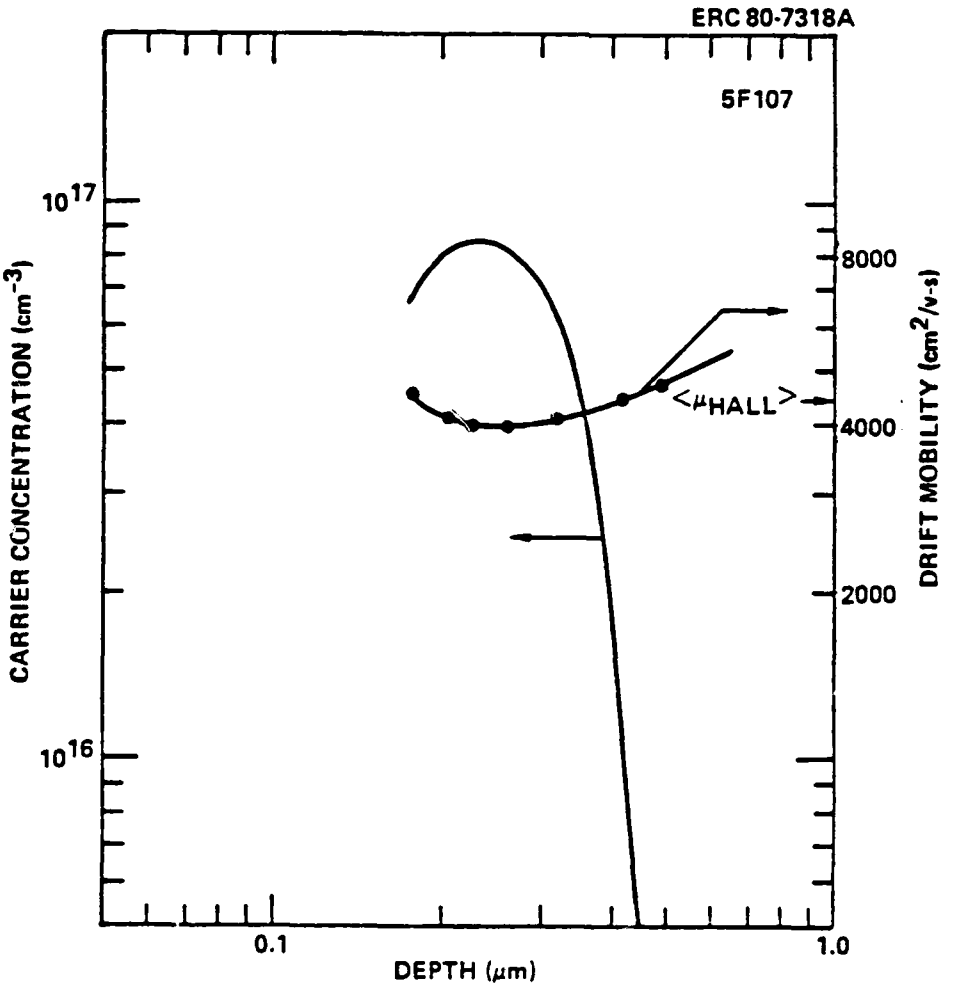

Fig. 18 Drift mobility of an ion-implanted layer.

3.2.3 RF Performance

Vapor-phase epitaxy and ion implanted devices measured at 6.2 GHz have produced noise figure/associated gain values of 1.75 dB/10.0 dB. The initial measurements of the MBE heterostructure devices produced only 5.2 dB/2.0 dB on several devices. At first study these results were thought to be due primarily to a high output conductance or very low gain in spite of the transient or fluctuating nature of the basic device current. This high output conductance was traced to an initial deposition of GaAs on the substrate before the AlGaAs and subsequent active layer of GaAs (see Table 1, layer 283 to 289). Removal of this growth step indeed produced much harder saturation as shown by curve tracer analysis in Fig. 19 but the aperiodic fluctuation of the current continued as well as the poor performance at high frequency.

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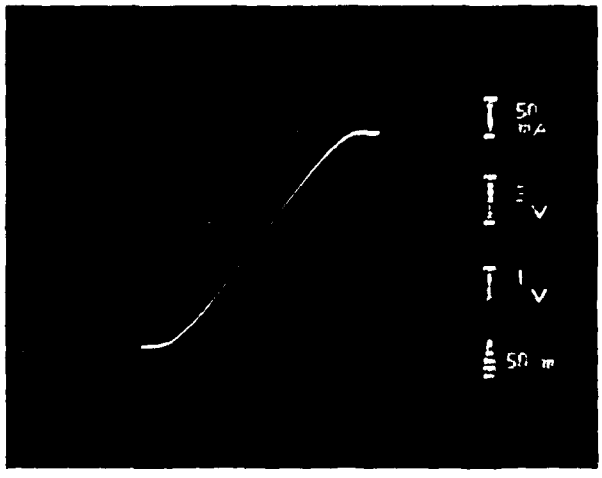
MBE 358

LNF 1980-1



MBE 421

Fig. 19 I-V comparison of MBE layers.

4.0 CONCLUSION

At the present stage of evaluation, AlGaAs buffer layers grown by molecular beam epitaxy have shown some superior properties over those produced by LPE or VPE methods. Although this has been shown, the fabrication of a high performance heterostructure device has experienced severe difficulty. Techniques have been developed to successfully produce devices of at least the correct d.c. specifications but the electrical performance is constrained by an effect which causes current and transconductance fluctuations.

The advantage attributed to current confinement by an AlGaAs/GaAs heterostructure may suffer from traps at the interface whose most serious effect occurs near full depletion. This counteracts precisely the device conditon of optimum noise performace for small signal FETs. As was discussed in Section 2 the actual confinement due to the heterostructure is comparable to that of a GaAs/GaAs homostructure. Although the hard potential barrier may prevent penetration of carriers into the buffer layer for the heterostructure, the homostructure has fabrication quality advantages. It must be noted that other structures utilizing the band discontinuity of AlGaAs to GaAs (superlattice, modulation doping) has quite obvious performance advantages over the established homostructure of GaAs active layer to GaAs buffer layer devices.

Recent work in MBE growth of AlGaAs suggests that the effect of lower substrate temperatures during growth needs further investigation. This parameter may play a major role in the device fluctuation behavior observed in this program.

5.0 REFERENCES

1. J. S. Barrera, "GaAs FETs Promise Much As they Come of Age," Microwaves, Vol. 19, No. 2, pp. 67-8 (Feb. 1980).
2. J. A. Higgins, R. L. Kuvas, F. H. Eisen, and D. R. Ch'en, IEEE Trans. on Elect. Dev. ED-15, 587 (June 1978).
3. C. E. C. Wood and B. A. Joyce, J. Appl. Phys. 49, 4854 (1978).
4. S. N. Schulman and T. C. McGill, "Band Structure of AlAs-GaAs (100) (Dec. 1977).
5. W. E. Pickett, S. G. Louie, M. L. Cohen, "Self-consistent Calculations of Interface States and Electronic Structure of the (110) Interfaces of Ge-GaAs and AlAs-GaAs," Phys. Rev. B, Vol. 17, No. 2, p. 815 Jan. 1978).
6. R. Dingle, W. Wiegmann, and C. H. Henry, "Quantum States of Confined Carriers in Very Thin Al_xGa_{1-x}-$Al_xGa_{1-x}As$ Heterostructures," Phys. Rev. Lett., Vol. 33, No. 14, p. 827 (Sept. 1974)
7. R. Dingle, A. C. Gossand, and W. Wiegmann, "Direct Observation of Superlattice Formation in a Semiconductor Heterostructure," Phys. Rev. Lett., Vol. 34, No. 21, p. 1327 (May 1975).
8. A. G. Milnes and D. L. Feucht, "Heterojunctions and Metal-Semiconductor Junctions," Academic Press, New York, p. 3 (1972).
9. R. A. Pucel, H. A. Haus and H. Statz, "Signal and Noise Properties of GaAs Microwave Transistors," Advances in Electronics and Electron Physics, Vol. 38, Academic Press, New York, 1975.
10. H. H. Berger, "Contact Resistance and Contact Resistivity," J. Electrochemical Society, Vol. 119, pp. 507-514, April 1972.
11. J. A. Higgins, R. L. Kuvas, F. H. Eisen, and D. R. Ch'en, IEEE Trans. on Elect. Dev. ED-15, 587 (June 1978).
12. R. A. Pucel, H.A. Haus and H. Statz, "Signal and Noise Properties of GaAs Microwave Transistors," Advances in Electronics and Electron Physics, Vol. 38, Academic Press, New York, 1975.
13. H. Morkoc, L. C. Withkowski, T. J. Drummond, C. M. Stanchak, B. G. Streetman, and A. Y. Cho, to be published

14. J. R. Waldrop, S. P. Kowalczyk, R. W. Grant, E. A. Kraut, and D. L. Miner, Proceedings of Physics of Compound Semiconductor Inerfaces ____ 8, 1981, to appear in J. Vac. Sci. Tech.

15. W. T. Tsang, M. Olmstead and R. P. H. Chang, Appl. Phys. Lett. 34, 408 (1979).

16. H. C. Casey, Jr., A. Y. Cho, D. V. Lang, E. H. Nicollian and P. W. Foy, J. Appl. Phys. 50, 3484 (1979).

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Code 922
271 Catalina Blvd.
San Diego, CA 92152

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F124 A, P.O. Box 73
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Enclosure (2)

Commandant
Marine Corps
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Washington, DC 20380 — 1

Communications Transistor Corp.
Dr. W. Weisenberger
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San Carlos, CA 94070 — 1

Microwave Associates
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Advisory Group on Electron Devices
201 Varick Street, 11th Floor
New York, NY 10014 — 1

Professor L. Eastman
Phillips Hall
Cornell University
Ithaca, NY 14853 — 1

Professors Hauser and Littlejohn
Department of Electrical Engr.
North Carolina State University
Raleigh, NC 27607 — 1

Professors Rosenbaum & Wolfe
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Washington University
St. Louis, MO 63130 — 1

W. H. Perkins
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