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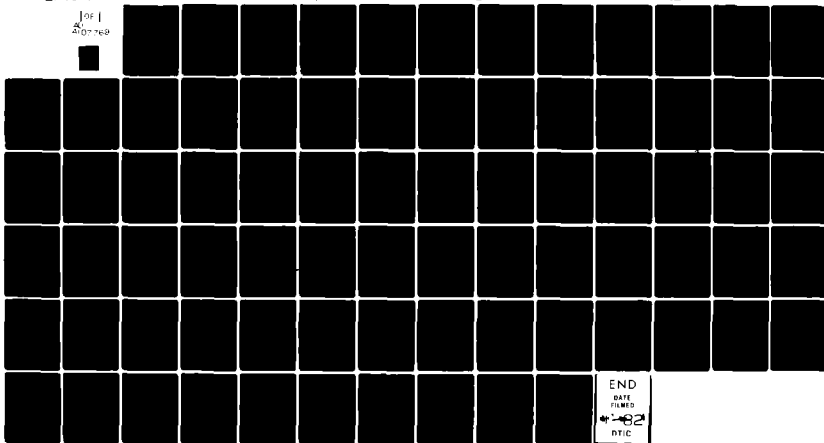
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This report discusses the implementation of the reject and selective reject
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M6800 microprocessor. Flow charts and a portion of the code are included.

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USE OF A MICROPROCESSOR
TO IMPLEMENT AN ADCCP PROTOCOL
WITH REJECT & SELECTIVE REJECT
(Federal Standard 1003)

AUGUST, 1981

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FOREWORD

Among the responsibilities assigned to the Office of the Manager, National Communications System, is the management of the Federal Telecommunication Standards Program which is an element of the overall GSA Federal Standardization Program. Under this program, the NCS, with the assistance of the Federal Telecommunication Standards Committee, identifies, develops, and coordinates proposed Federal Standards which either contribute to the interoperability of functionally similar Federal telecommunication systems or to the achievement of a compatible and efficient interface between computer and telecommunication systems. In developing and coordinating these standards a considerable amount of effort is expended in initiating and pursuing joint standards development efforts with appropriate technical committees of the Electronic Industries Association, the American National Standards Institute, the International Organization for Standardization, and the International Telegraph and Telephone Consultative Committee of the International Telecommunication Union. This Technical Information Bulletin (TIB), one of a series, is a companion document to NCS TIB 80-7 (which incorporates all substantive material contained in NCS TIB 80-2), and has been prepared to inform interested Federal activities of the progress of these efforts. Any comments, inputs, or statements of requirements which could assist in the advancement of this work are welcome and should be addressed to:

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USE OF A MICROPROCESSOR TO
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WITH REJECT & SELECTIVE REJECT
(FEDERAL STD. 1003)

August , 1981

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TABLE OF CONTENTS

1.0	Introduction.	1-1
2.0	System Design Consideratons	2-1
3.0	REJ/SREJ Implementation	3-1
4.0	Detailed Software Design.	4-1
4.1	Data Structures	4-3
4.2	Subroutine/Function Descriptions.	4-6
4.3	Detailed Flow Charts.	4-29
5.0	Microprocessor Coding and Testing	5-1
6.0	Discussion of Feasibility	6-1
7.0	References.	7-1

APPENDICES

A.	Operating System	A-1
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1.0 INTRODUCTION

This document summarizes the work performed by Delta Information Systems, Inc. for the Office of Technology and Standards of the National Communications System, an organization of the U. S. Government, under Purchase Order DCA100-80-M-0221. The Office of Technology and Standards, headed by National Communications System Assistant Manager Marshall L. Cain, is responsible for the management of the Federal Telecommunications Standards Program, which develops telecommunication standards whose use is mandatory by all Federal agencies. The objective of this program is to develop a block diagram, flow charts, and computer programming for the Reject and Selective Reject functions of the unbalanced normal, unbalanced asynchronous, and balanced asynchronous class of procedures in accordance with Federal Standard 1003. The purpose of this effort is to determine the feasibility of using the M6800 or similar microprocessor to implement this type of protocol, and to obtain an estimate of memory and processor resources that would be required. The Office of Technology and Standards will use the information to advise other Federal agencies who implement the standard and, when merged with the results of other studies, to evaluate the operational and economic impact of incorporating various options in Federal Standard 1003.

The effort necessarily has focussed on the software required to implement the protocol itself, and is by no means a total hardware/software system design that would be

required to develop a complete system. Complete system development is, of course, beyond the scope of this program.

A discussion of the method of implementation of Reject and Selective Reject is included in Section 2. Flow charts describing the software that makes up the protocol included in Section 4. These flow charts describe the protocol software processes in sufficient detail that code may be written with no major design decisions. The flow charts at this level are very hardware dependent.

A small portion of the code for the 6800 microprocessor has been written and is included in Section 5.0. The code was introduced into a 6800 microcomputer, provided by Delta Information Systems. The code in the computer was then tested to insure its validity. Finally Section 6.0 contains a discussion of the feasibility of using the 6800 to implement the ADCCP protocol. It is estimated that approximately 1300 instructions are needed to implement the three classes of procedures in a logically configurable station (primary, secondary, or combined) with the Selective Reject option (1200 instructions with the Reject option), and that approximately 250 instructions are required for the operating system. Data transmission rates of up to 19.2 kilibit/sec. appear feasible for the configuration being considered.

2.0 SYSTEM DESIGN CONSIDERATIONS

The block diagram in Figure 2-1 shows a link with one primary/combined and one secondary/combined station communicating with each other by sending information in both directions. That is, either station may be a source or sink of data or both. Two-way simultaneous transmission is assumed. Although many secondary stations may communicate with one primary station, the objectives of this program can be met with no loss of generality, by assuming the existence of only one secondary station.

Each station, primary, secondary, or combined is made up of a microcomputer, an LSI interface to the link, and a user which supplies and uses the data to be communicated. The primary and secondary stations are physically very similar; operationally, of course, the primary must supervise and control a number of secondary stations, and thus it requires a larger data structure and somewhat more complicated code.

For the purpose of this program, the microcomputer can be assumed to be very basic--microprocessor, memory (RAM and ROM), interface chips, clock, etc. A design choice that has significant impact on the outcome of this program is the choice of the LSI interface. The purpose of the LSI interface is to convert the parallel data from the CPU to a continuous serial data stream for transmission. Simultaneously, it must convert received serial data to parallel data for the CPU. In addition, it must generate and verify the frame check

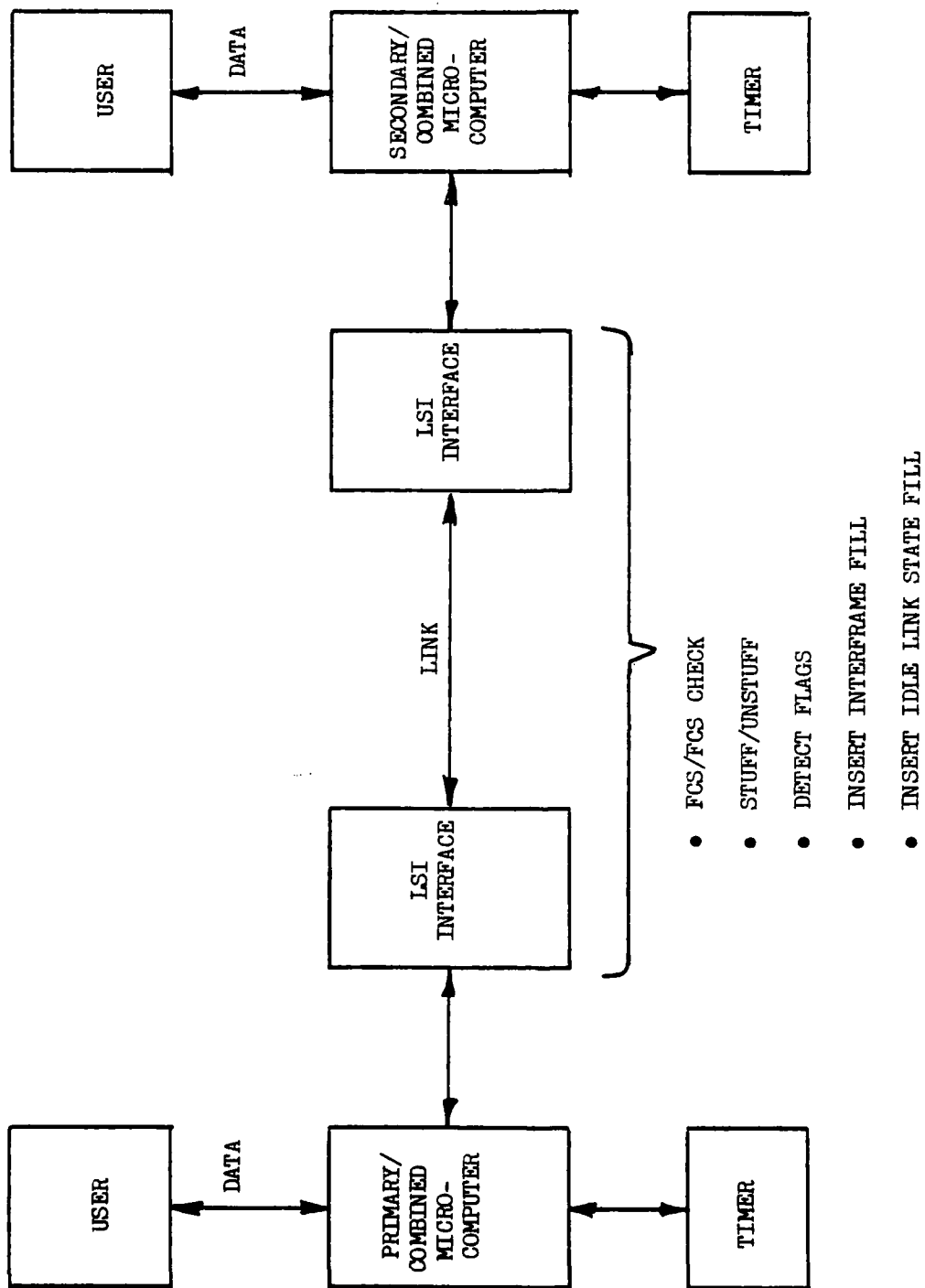


Figure 2-1 System Block Diagram

sequence (FCS), stuff and delete 0's to distinguish FLAG or ABORT from data, insert and detect FLAG or ABORT, and insert interframe fill or idle link fill. Other functions may also be performed by this interface.

Two different LSI chip specifications have been examined as possible candidates for the interface function in this particular study. These chips, which represent different approaches to the interface problem, are the F6856 and the WD2501. (Refer to a previous report (1) for a copy of their preliminary data sheets and a brief comparison).

At least three other similar protocol chips have become candidates since the beginning of this effort. These are the Solid State Scientific SND5025, the Signetic 2652 and the Zilog SIO.

The F6856 chip was selected for this program by mutual consent of the contractor and the government. The interface to the communications lines requires additional logic such as a Federal Standard 1031 (Electronic Industries Association Recommended Standard 449) interface chip and a modem, but the choice of these has little impact on this program.

The data transmitted over the link, must also be transmitted to the user. The interface/protocol required between the microcomputer and the user is also part of the system design. However, for this program, the protocol has not been defined. The interface, including the buffers to hold the data, is defined and described in Section 4.0.

3.0 REJ/SREJ IMPLEMENTATION

The objective of this program is to add the Reject (REJ) and the Selective Reject (SREJ) functions to the design of the ADCCP according to the Federal Standard 1003 and to estimate the memory and processor resources that these functions require. The REJ and SREJ protocols may be used in a number of ways: pure REJ, pure SREJ, and various combinations⁽²⁾ of these two including a look-ahead SREJ/REJ. For the pure REJ protocol, the receiver of information frames uses the REJ supervisory frame to request the sender of information frames to back up to an earlier point and begin retransmission. On the other hand, SREJ requests a single previous information frame followed by the continuation of the send sequence. REJ and SREJ may be used together in various combinations depending on whether the lost frame is single or multiple and if an exception condition exists when a new loss is detected.

The addition of REJ and SREJ to the ADCCP protocol also adds some complexity (especially for SREJ). This is due to the somewhat redundant nature of the reject protocols with respect to the checkpointing and timeout mechanisms. Although the reject mechanism is more efficient, checkpointing must be operational as a backup in case the REJ or SREJ frames or the retransmitted information frames are lost due to errors. Care must be taken to ensure that the checkpointing mechanism works with the reject frames while preventing redundant retransmission.

Only the pure REJ and pure SREJ have been included in the design, because these are adequate to allow memory requirements and speed to be estimated. However, the software design has been reorganized to provide for pure REJ, pure SREJ, or a combination of these options for error recovery. This has been accomplished by the inclusion of a recovery module in the subroutine that receives information frames. As described in more detail farther along in the report, this module is programmed for the desired recovery option. If a more complex recovery option is desired such as a look-ahead REJ/SREJ option, most of the software for this option will reside in the recovery module and the other modules will suffer little change.

4.0 DETAILED SOFTWARE DESIGN

In this section the software design is presented in sufficient detail to allow the objectives of this program to be met: that is, the feasibility of using the 6800 and an estimate of memory and throughput can be obtained. The design covers the major aspects of a logically configurable station; functions that allow the station to operate as a primary, secondary, a combined station in unbalanced normal, unbalanced asynchronous or balanced modes are included. Operation as a secondary/combined station is emphasized, since FED-STD-1003 does not cover many of the primary/combined station procedures for managing the link. These are left to the system designer. The software design includes a description of a minimal operating system to handle concurrent processes, major data structures, major software routines, and a set of detailed flow charts.

The detailed flow chart, together with associated data structures, describes the protocol software processes in sufficient detail so that code may be generated with no major design decisions. The flow chart at this level is hardware dependent, and must take into consideration the time constraints imposed by the concurrent software processes associated with the implementation of the protocol.

The protocol is made up of four major concurrent software processes, each of which is an example of the classic producer/

consumer problem. In this problem, one process produces items and then deposits them into a buffer. A second process consumes the items by taking them from the buffer. The processes must be coordinated so that the consumer does not run ahead of the producer, and that the producer does not write over records before the consumer has had a chance to read them. For the protocol problem, two concurrent processes are involved in communicating data between the LSI interface and the microprocessor; the LSI chip deposits bytes in its buffer as the producer, and the MPU reads this data as the consumer. Conversely, the microprocessor writes data into a buffer as the producer, to be read by the LSI chip as the consumer and transmitted over the link. A similar pair of processes serves to implement the interface between the microprocessor and the higher level user. For this effort, emphasis is placed on the interface between the MPU and the LSI protocol chip. This requires two main processes to be running at the same time--transmit and receive. The operating system that manages these processes is presented in Appendix A.

The purpose of this phase of the program is to add the REJ and SREJ functions to the design and estimate the memory and processor resources that these functions require. In order to accommodate REJ and SREJ in a modular fashion, the routines that receive I frames and that transmit I and supervisory frames have been reorganized and supplemented. For example, the receive I subroutine now includes a recovery module

that can be used for REJECT, or SREJECT, or neither depending on which of three software routines are included. Note that either pure REJ or pure SREJ is included and not a combination of the two. The combination could be added as a fourth recovery technique, although for the purpose of measuring memory and processor resources the pure REJ and SREJ provide an adequate vehicle. If neither REJ or SREJ are employed the error recovery defaults to the checkpointing mechanism.

In addition to the receive I frame routine, the process that transmits I and supervisory frames was modified to enable REJ and SREJ transmission and retransmission when appropriate. The ability to reset the send variable as a result of receiving REJ was provided as well as the ability to transmit a selected I frame as a result of receiving SREJ. Two new routines were added to act on a received REJ or SREJ.

4.1 DATA STRUCTURES

This section outlines the data structures, including variables, arrays, buffers, etc. in order to more easily understand the detailed flow charts that follow and to estimate the amount of random access memory (RAM) that is required to implement the protocol. Main state variables are as follows:

STATION TYPE - PRIMARY, SECONDARY, OR COMBINED
(mutually exclusive)

OPERATIONAL STATE - has 3 values, mutually exclusive:

LDS - Logically disconnected state

ITS - Information transfer state

FRMR - Frame reject state (for secondary/combined)

Logically disconnected state has two mutually exclusive modes:

NDM - normal disconnected mode

ADM - asynchronous disconnected mode

Information transfer state has three mutually exclusive modes:

NRM - normal respond mode

ARM - asynchronous respond mode

ABM - asynchronous balanced mode

Other major variables are:

REMOTE BUSY - true if RNR received

 false if RR received or P/F bit

 set in received I-frame

STATION BUSY - true if not prepared to receive

 information; false otherwise

SNDREJ/ SNDSREJ - flag

REJ/SREJ ACTIONED - state variable

SENT REJ/SREJ - state variable

P-BIT - Poll bit

F-BIT - final bit

S - Send Variable (next I-frame to be transmitted)

R - Receive Variable (expected sequence number
 of next received I-frame)

N(S) - Send Sequence Number (I-frame sequence
 number)

N(R) - Receive Sequence Number (station trans-
 mitting N(R) has correctly received all
 I-frames up to and including N(R)-1)

Operating System variables include:

RDAI LG - Receive data available event variable

TBMT - Transmitter buffer empty event variable

RUNNING	}	Pointers to beginning of each queue
BLOCK		
READY		

PCB - Each process control block contains:

condition code register

accumulator A

accumulator B

index register (upper and lower)

program counter (upper and lower)

pointer to next PCB

priority

A number of buffers are required for such things as the received control word, transmitted control word, frame type, etc. Next, consider the data buffer required to transmit/receive information between CPU and USER. Assume that a separate buffer is required for transmit and receive, and that each buffer can hold up to eight I-frames of data. These buffers are accessed via tables shown in Figure 4-6. Each frame to be transmitted via the LSI chip has a starting address for the data and length in bytes of the data part of the frame. If the frame was transmitted with the poll/final bit set, this is recorded. The "acknowledge" variable is used to indicate whether a frame has been deposited by the USER for transmission, whether it has been transmitted, and finally, whether it has been acknowledged by the receiving station. In the example shown,

six frames have been deposited by the USER for transmission, three have been transmitted ending with a final bit (SECONDARY-NRM), and the first frame has been acknowledged. Three frames remain to be transmitted. The received look-up table performs a similar function for data received from the LSI chip. Each frame is assembled byte-by-byte and the frame length is incremented. When the frame has been correctly received (valid FCS and N(S)) the frame is tagged as verified and may be read by the user.

The buffers and associated variables required for LSI Interface chip operation are shown in Figures 4-2, 4-3, and 4-4. The Mode Control Register (MCR) contains control information common to both receiver and transmitter. The SAR contains the secondary station address. The TCR is loaded by the MPU to control the transmitter, and the TDB contains the byte to be transmitted. The Receiver Status Register (RSR) is read by the MPU to determine the status of the byte received in the Received Data Buffer (RDB). The RCR contains control information for the receiver and the TSR supplies transmitter status. Refer to previous report for a detailed description of receiver/transmitter operation and flow charts for the F6856 LSI interface chips.

4.2 SUBROUTINE/FUNCTION DESCRIPTIONS

This section describes the functions of software modules that make up the protocol. Figure 4-5 contains a table of all the significant software modules organized by station types (primary, secondary, or common to both) and by whether the module is associated primarily with a transmit

TPACK

FRAME NUMBER	STARTING ADDRESS	FRAME LENGTH	FINAL BIT SET	ACKNOWLEDGEMENT
0	ADDR0	1028	0	1
1	ADDR1	1028	0	0
2	ADDR2	512	F	0
3	ADDR3	512		-1
4	ADDR4	512		-1
5	ADDR5	512		-1
6				8
7				8

TRANSMITTER LOOK-UP
TABLE

RPACK

FRAME NUMBER	STARTING ADDRESS	FRAME LENGTH	FRAME VERIFIED
0			
1			
2			
3			
4			
5			
6			
7			

RECEIVER LOOK-UP
TABLE

Figure 4-1 Transmitter/Receiver Look-up Table

100 SAR (WRITE ONLY)

101 MCR (WRITE ONLY)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSCA			PROTOCOL SELECT			LRSS	CC	NRZI	LOOP	EC	SECONDARY ADDRESS				

DEFAULT: 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1

BOP PRIMARY 1 CONT. NRZI CRC '1's
BYTE

SET: 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0

BOP SECONDARY NORMAL MODE

STATION SECONDARY ADDRESS

010 TDB (WRITE ONLY)

011 TCR (WRITE ONLY)

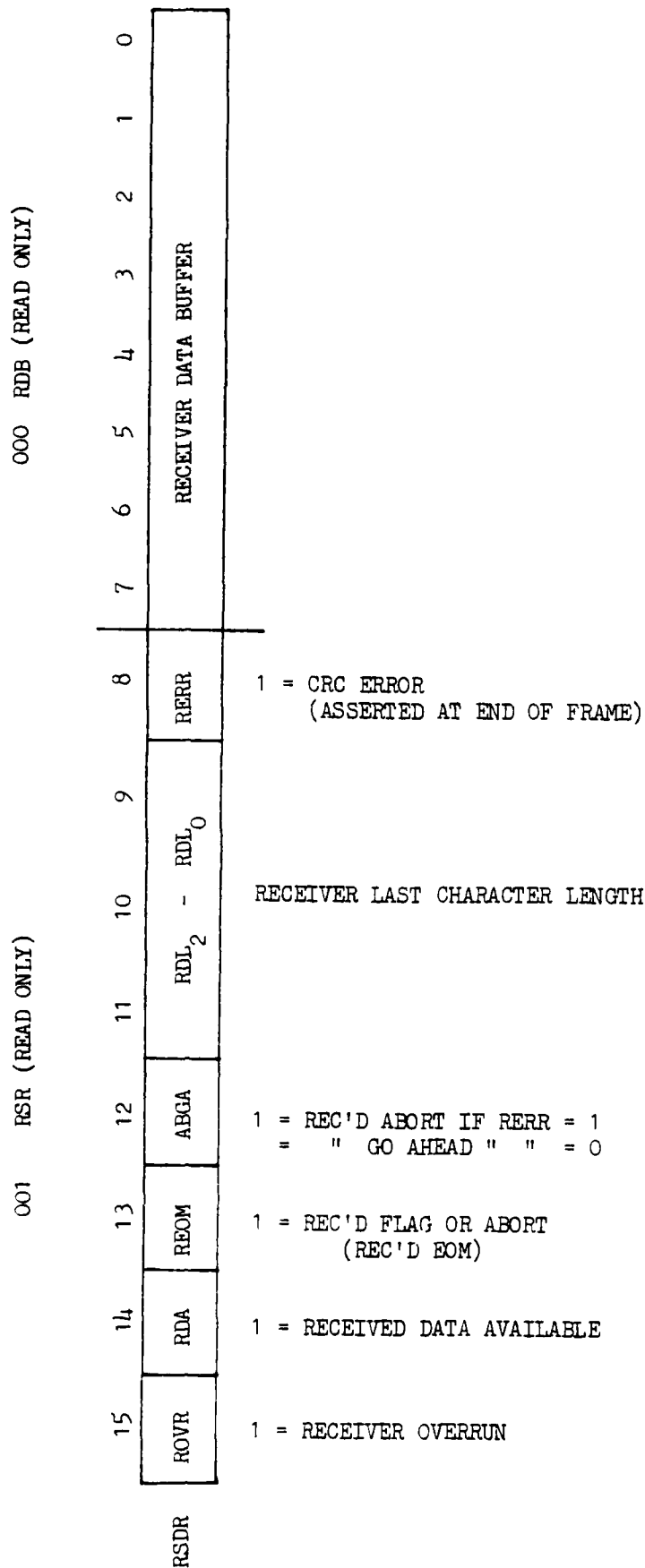
TCDR	SOM	TACG	GATD	EOM	RTS	TCL ₂ - TCL ₀	TRANSMITTER DATA BUFFER
------	-----	------	------	-----	-----	-------------------------------------	-------------------------

(DEFAULT=0's)

1= START OF MESSAGE
1= ABORT
0= FLAGS TRANS. BETW. FRAMES
1= CONT. OF TDB IS LAST BYTE OF MESSAGE
1= REQUEST TO SEND
0 0 0 8-BIT TRANS. CHAR. LENGTH

MUST BE RELOADED EACH TIME TCR IS
UPDATED UNTIL AFTER EOM BIT HAS BEEN SENT

Figure 4-2 Mode Control, Secondary Address, Transmitter Control, and Transmitter Data Registers



ALL BITS OF RSR EXCEPT RDA ARE RESET ON READ; RDA IS RESET WHEN RDB IS READ
DATA IS PASSED TO RDB ONLY ON ADDRESS MATCH

Figure 4-3 Receiver Status Register and Receive Data Buffer

SECONDARY/COMBINED

<u>RECEIVE FUNCTIONS</u>	<u>TRANSMIT FUNCTIONS</u>
SNRM	
SARM	TR-UA
SABM	TR-DM
DISC	
RESET	
FRMREJ	TR-FRMR

PRIMARY/COMBINED

<u>RECEIVE FUNCTIONS</u>	<u>TRANSMIT FUNCTIONS</u>
	TR-SNRM
UA	TR-SARM
DM	TR-SABM
	TR-DISC
FRMR	TR-RSET

BOTH

<u>RECEIVE FUNCTIONS</u>	<u>TRANSMIT FUNCTIONS</u>	<u>OPERATING SYSTEM</u>
RCV	SENDI	WAIT
I	SNDRR	SIGNAL
RR	SNDRNR	INTERRUPT SERVICE
RNR	SENDRJ	IDLE
CHKPNT		DUMMY
RCNTRL		
GETBYT	SNDBYT	
REJ		
SREJ		

INIT

Figure 4-5 Software Modules
4-11

or receive process. Those modules contained in the operating system have been discussed previously. Some of the modules are the main routines for processes, namely INIT, RCV, SENDI, and IDLE. INIT is the initialization process, RCV, is the process that receives and processes the address and control bytes of the received frame, SENDI is the main transmitting process, and IDLE is a simple process that runs when all other processes are blocked. DUMMY is a process that is never run, but serves as a place for the IDLE process to point to and has the lowest priority. Those modules that are associated only with either the primary/combined or secondary/combined stations are mostly mode-setting or mode acknowledging functions and are relatively simple.

GETBYT is a macro that reads the receive buffer if data is available and stores the data in a location specified in the macro agreement. Interrupts are disabled for the duration of the macro to prevent flags or data from changing while reading. If no data is available, the process is blocked via WAIT. The SNDBYT macro loads the transmitter buffer with operation similar to that in GETBYT.

FRMREJ changes the state of the secondary/combined station to frame reject, assembles the FRMR information field, and activates the FRMR transmit process called TR-FRMR. This process terminates any other transmit process except TR-DM, or TR-UA, sends the FRMR frame, and then terminates itself. The FRMR routine receives a FRMR frame (implies a primary/combined station) and takes appropriate mode setting action.

The main routines for transmitting and receiving I and supervisory frames, including RR, RNR, REJ and SREJ, are described in the following pages.

SENDI process - Transmits I and all supervisory frames

REFERENCES: P/F received
Information transfer mode
SENT SREJ state variable
P/F PREVIOUS State variable
STATION BUSY state variable
REMOTE BUSY state variable
SREJ ACTIONED state variable

MODIFIES: SNDSREJ flag
SENDRJ return
S - send variable
TIME OUT

CALLS: SENDRJ
SNDRR
SNDNRN

EXIT: NONE

FUNCTION: The function of the SENDI process is to transmit I frames and to transmit supervisory frames as required. The process begins with a determination of whether or not to retransmit a previously transmitted SREJECT. If not, a REJECT or SREJECT may be transmitted depending on the SNDREJ/SNDSREJ

flag. Then, if data is available for transmission and the remote station is not busy, the loop for transmitting I frames is entered at NEXTI. If SREJ has been actioned, the requested frame is set up for retransmission. Next, if P and NRM the F bit is set. SREJ is retransmitted as required. Next the complete I frame is transmitted byte by byte and the send variable (S) is incremented. If the remote station is found to be busy RR or RNR is transmitted as appropriate. If more frames are available for transmission the loop is repeated from NEXTI. If not, the process is repeated from SENDI.

SNDRR Subroutine - Sends Receive Ready

REFERENCES: P/F received

Information transfer mode

SENTSREJ state variable

P/F PREVIOUS state variable

STATION BUSY state variable

R - receive variable

MODIFIES: SNDSREJ state variable

TIMEOUT

CALLS: SENDRJ

EXIT: NORMAL RETURN

FUNCITON: This routine is used to send Receive Ready and also to send SREJECT if appropriate. First, a decision is made whether or not to retransmit a previously sent SREJ. If not, the SENDRJ subroutine is called to send REJ or SREJ depending on the SNDREJ and SNDSREJ flags and the STATION BUSY state variable. Finally, RECEIVE READY is transmitted (or not) depending on the P/F bit and the information transfer state.

SNDRNR Subroutine - Sends Receive Not Ready

REFERENCES: P/F received
Information transfer mode
R - receive variable

MODIFIES: TIMEOUT

EXIT: NORMAL RETURN

FUNCTION: This routine sends Receive Not Ready depending on the P/F bit and the information transfer state. Functionally it is similar to SNDRR, except that there is no provision to send SREJ because RNR Implies that the station is busy.

SENDRJ Subroutine - Transmit REJECT or SREJECT routine

REFERENCES: STATION BUSY state variable
SNDREJ/SNDSREJ flag
R - receive variable

MODIFIES: SNDREJ/SNDSREJ flag
Timeout

EXIT: NORMAL RETURN

FUNCTION: After determining that STATION BUSY is false,
and that either SNDREJ or SNDSREJ is true, a
supervisory command/response of REJ or SREJ is
transmitted, as appropriate. The SNDREJ/
SNDSREJ flag is set false before returning.

I Module - Receive I frame routine

REFERENCES: OPERATIONAL STATE Variable
FRMR - frame reject state variable
LENGTH - number of bytes in information field
P/F received
N(S) received
R - receive variable
REJ/SREJ SENT state variable

MODIFIES: LENGTH
R
REJ/SREJ SENT
SNDREJ/SNDSREJ flag

EXIT: RCV
FRMRI

FUNCTION: This routine is used to make the appropriate checks on the I-frame control field and to read the information field byte-by-byte. First, a check is made to ensure that the receiver is either in information transfer state (ITS) or frame reject state (FRMR). If so, the information field is read in a byte at a time. Next, tests are made for a good frame check sequence (FCS),

no FRMR, and an I-frame information field of the correct length. If all of these tests pass, the send sequence number (N(S)) received is compared with the receive variable (R) and appropriate action taken depending on whether or not there is an error and on the method of error recovery. One of the three methods of error recovery that are presented may be used at a given time. These include REJECT recovery, SREJECT recovery, and checkpoint recovery.

SREJECT recovery is used to request that a specific frame be retransmitted. Following frames are buffered until the requested frame is received and then the receive variable is advanced accordingly. REJECT is similar except that all frames following the frame in error must be retransmitted. If neither REJECT nor SREJECT is employed, the checkpointing mechanism must be relied on to perform error recovery: the receiver simply ignores the frame, and the transmitter must discover the error via N(R) and the P-F checkpoint cycle.

RR/RNR Module - Receive Ready/Receive not Ready

REFERENCES: FRMR - frame reject state variable

MODIFIES: REMOTE BUSY - state variable

CALLS: CHKPNT

EXIT: RCV
FRMRI

FUNCTION After the frame has been validated the CHKPNT routine is called to update the acknowledgement of frames through N(R)-1. If not in frame reject state the REMOTE BUSY state variable is cleared or set depending on whether a receive ready (RR) or receive not ready (RNR) was received.

SREJ Module - Receive SREJECT routine

REFERENCES: N(R) received

P/F received

FRMR - frame reject state variable

REJ/SREJ ACTIONED state variable

CHECKPOINT RETRANS. state variable

P/F (old) value set when SREJ actioned

N(R) (old)

MODIFIES: Ss - specific send variable

REJ/SREJ ACTIONED State variable

REMOTE BUSY state variable

CALLS: CHKPNT

EXIT: RCV

FRMRI

FUNCTION: The SREJ function is similar to the REJ function. After the frame has been validated, a test is made to determine if REJ or SREJ are currently being actioned. If REJ is being actioned, operation is identical to that of the REJ subroutine (no error recovery is performed). If SREJ is being actioned, the P/F and N(R) of the original are compared to the P/F and

N(R) of the current SREJ. If the original P/F is equal to zero for a secondary or primary/combined station, the next SREJ is not actioned if the P/F=1 and N(R) has the same value and numbering cycle as the first SREJ. If no REJ/SREJ is being actioned and no checkpoint retransmission is in progress a reject exception condition is established. The P/F bit and N(R) are recorded for possible later use as discussed above. The single frame to be retransmitted is made known to the transmit subroutine and the CHPNT routine is called to update the acknowledgement of frames through N(R)-1.

REJ Module - Receive REJECT routine

REFERENCES: N(R) received

P/F received

FRMR - frame reject state variable

REJ/SREJ ACTIONED state variable

CHECKPOINT RETRANS. state variable

MODIFIES: S - send variable

TPAK-variables and status bits

REJ/SREJ ACTIONED state variable

REMOTE BUSY state variable

CALLS: CHKPNT

EXIT: RCV

FRMRI

FUNCTION: After the REJ frame has been validated (no FCS error and not in FRMR state) a test is made to determine if a REJECT or SREJECT command/response is currently being actioned. If not, and if the frame indicated in the N(R) is not being retransmitted due to the checkpointing mechanism, a reject exception condition is established. The send variable, S, is made equal to the N(R) received and the pointers in the

transmit buffer are adjusted accordingly. The
CHKPNT routine is called to update the acknowl-
edgement of frame through $N(R)-1$.

CHKPNT Subroutine - Checkpoint recovery routine

REFERENCES: N(R) received
 P/F received
 FRMR - frame reject state variable
 Information transfer state variable
 REJ/SREJ ACTIONED - state variable

MODIFIES: S - send variable
 TPACK variables add status bits
 REJ/SREJ ACTIONED state variable

EXIT: NORMAL RETURN
 FRMREJ
 FRMR1

FUNCTION: The N(R) received is check for validity. An invalid N(R) is defined as a number that points to an I-frame that has been transmitted previously and acknowledged, or to an I-frame that has not been transmitted and is not the next sequential I-frame pending transmission. If the N(R) is invalid, FRMREJ is called. Otherise the acknowledgement of frames through N(R)-1 is updated via the adjustment of pointers and variables in TPACK. If the poll (or final) bit is set, a check is made to determine if N(R)-1 points to

the frame transmitted previously with the final (or poll) bit set. If not, the send variable (S) is reset to the earliest outstanding frame preceding the frame with the final (poll) bit set, as long as this frame is not being transmitted due to REJ or SREJ.

RCNTRL Subroutine - Unpacks control field

REFERENCES: CNTFLD - input control field
COMTAB - command table
VALTAB - command validity table
FRTAB - frame type table
STATE - station type and mode

MODIFIES: POLLP - provisional poll/final bit
NRP - provisional N(R)
NSP - provisional N(S)
FTYPE - frame type

EXIT: NORMAL RETURN

FUNCTION: A provisional P/F bit is extracted from the control field. Next, the frame type is determined by matching the masked control field against a table of implemented commands and responses. The I frame is expected first, followed by the supervisory and the unnumbered frames. If no table entry matches the frame type, the command/response is marked invalid. Otherwise the frame type is checked against current station type and mode. If valid, the provisional N(R) and N(S) are extracted and the frame type is returned.

4.3 DETAILED FLOW CHARTS

The detailed flow charts are shown in Figures 4-6 through 4-26. Note that Figure 4-13, Receive I Subroutine, contains three optional recovery routines depending on the method to be used for error recovery. The three routines provide for a pure REJECT recovery, or a pure SREJECT recovery, or neither of these two (checkpoint recovery by default).

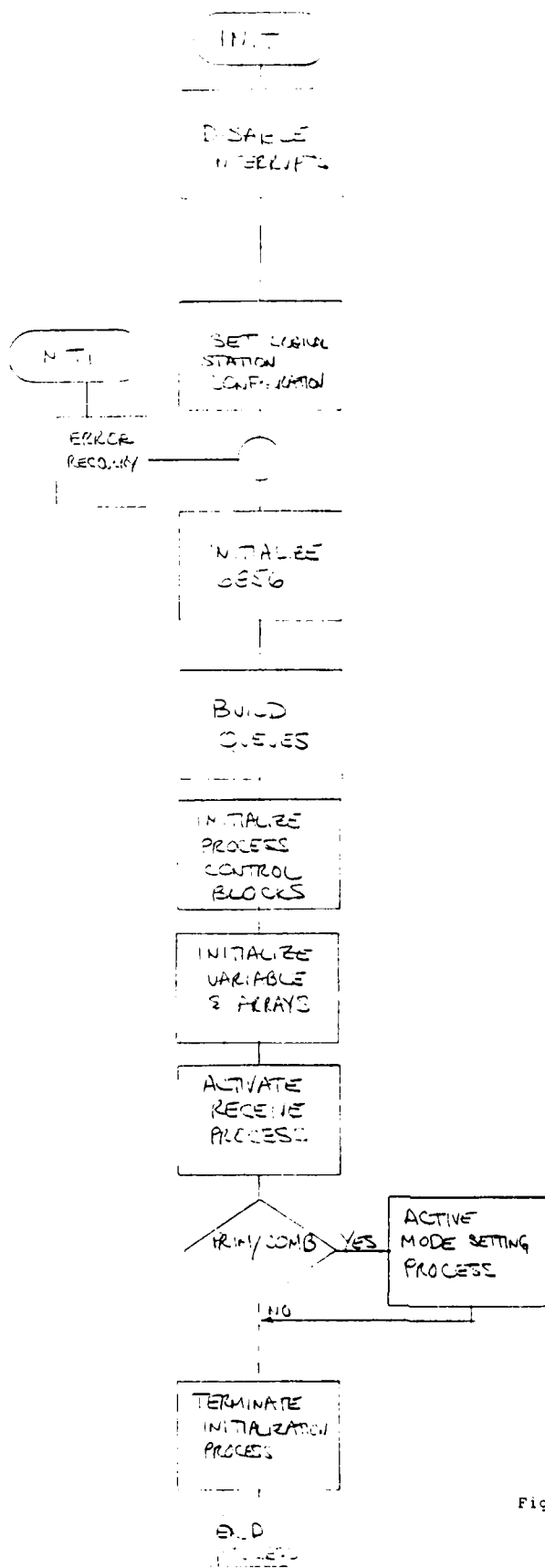


Figure 4-6 INIT Process

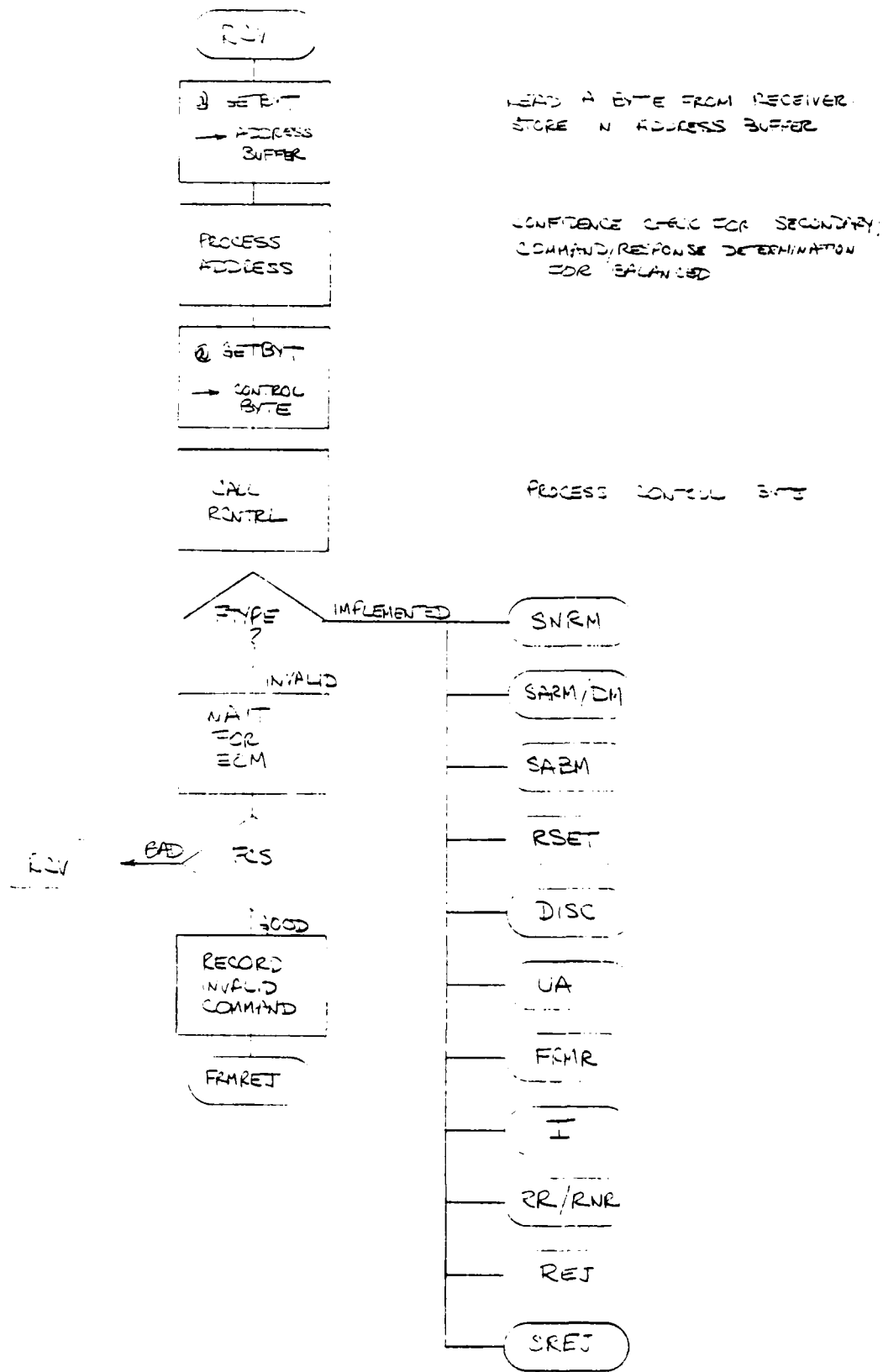


Figure 4-7 RCV Process
4-31

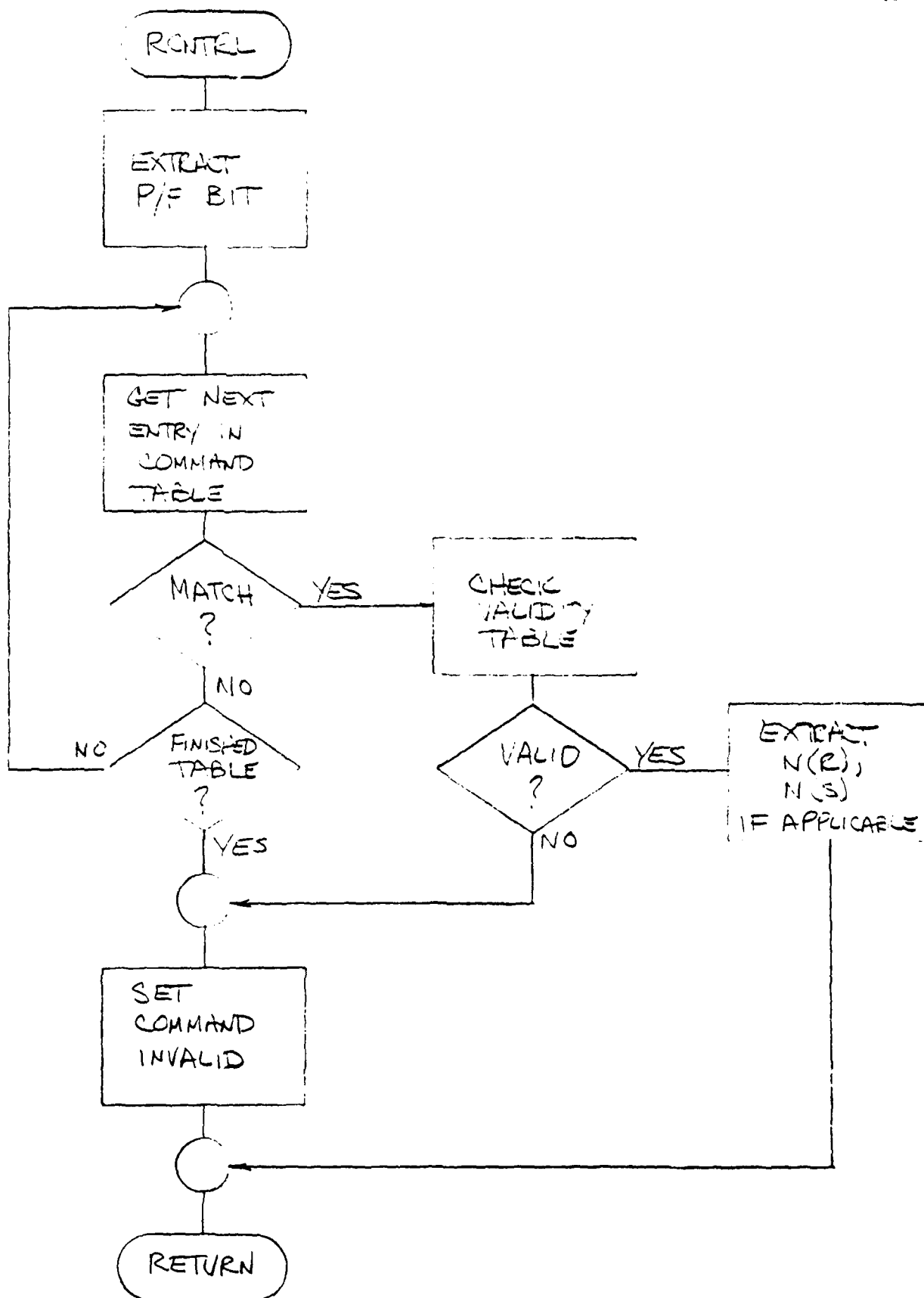


Figure 4-8 RCNTRL Subroutine

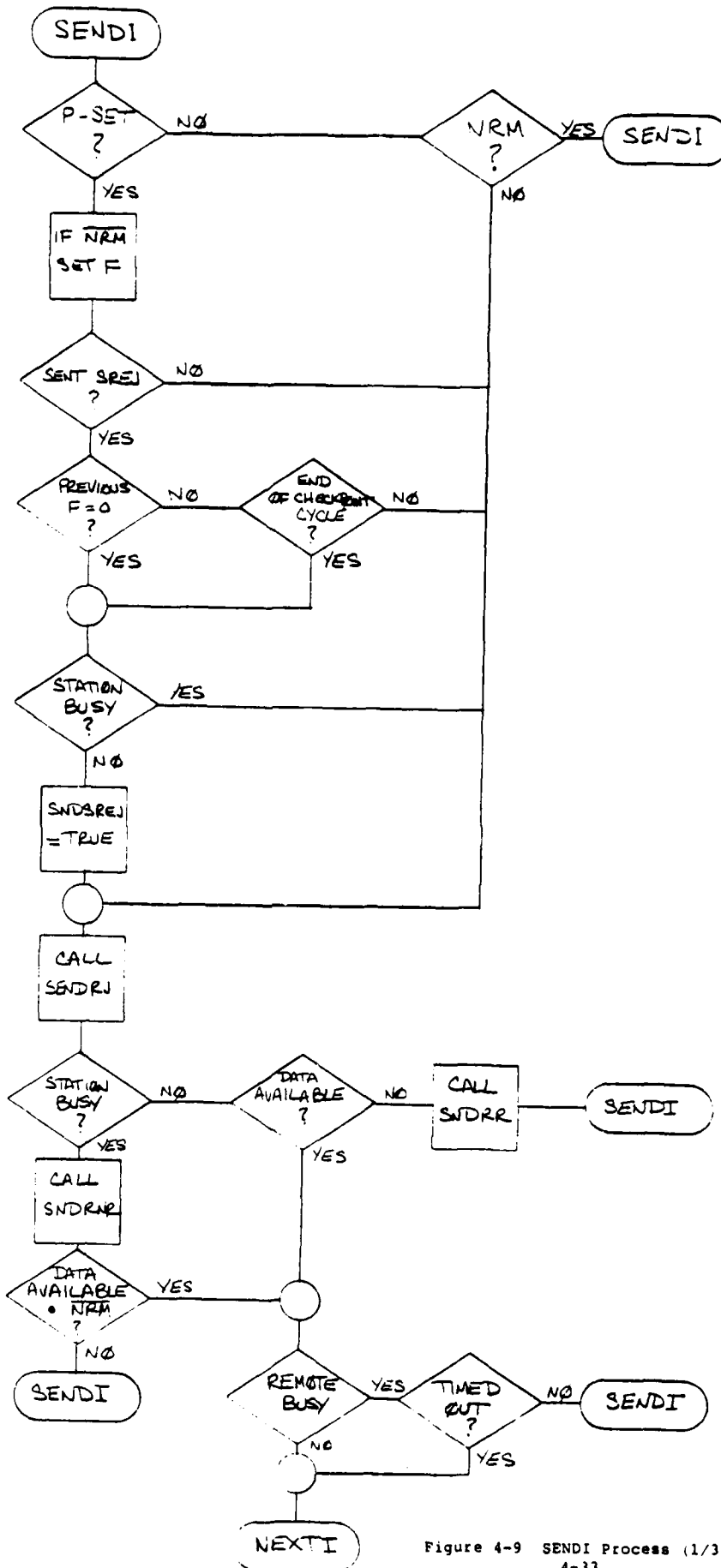


Figure 4-9 SENDI Process (1/3)
4-33

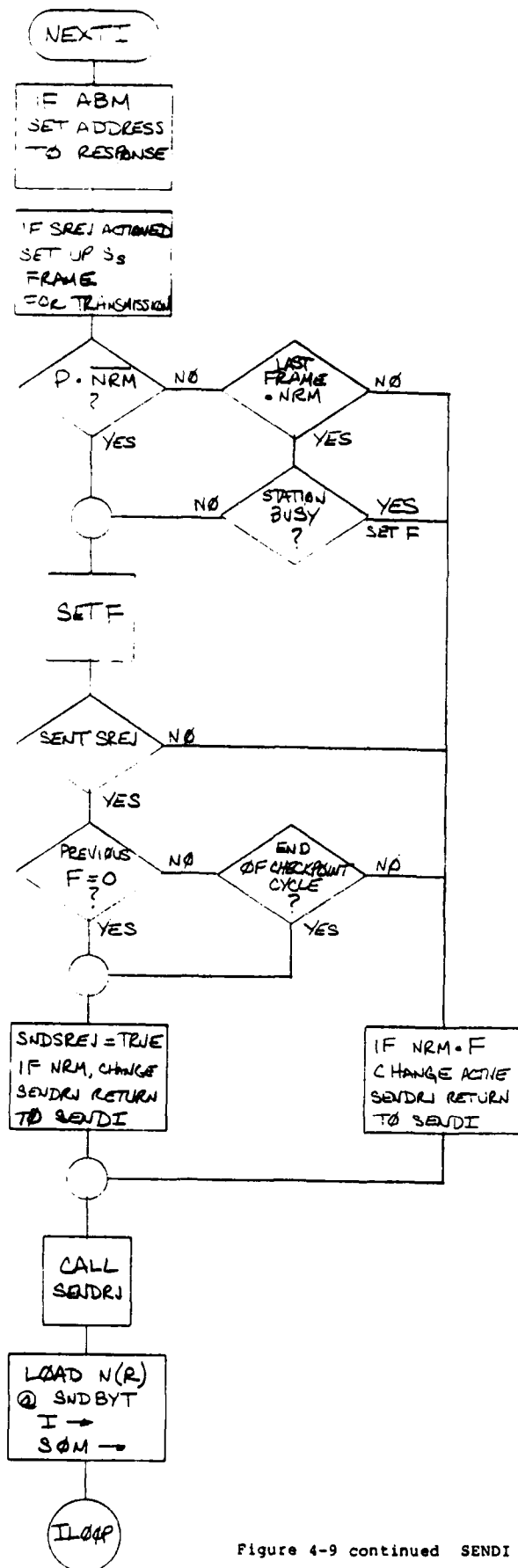


Figure 4-9 continued SENDI Process (2/3)

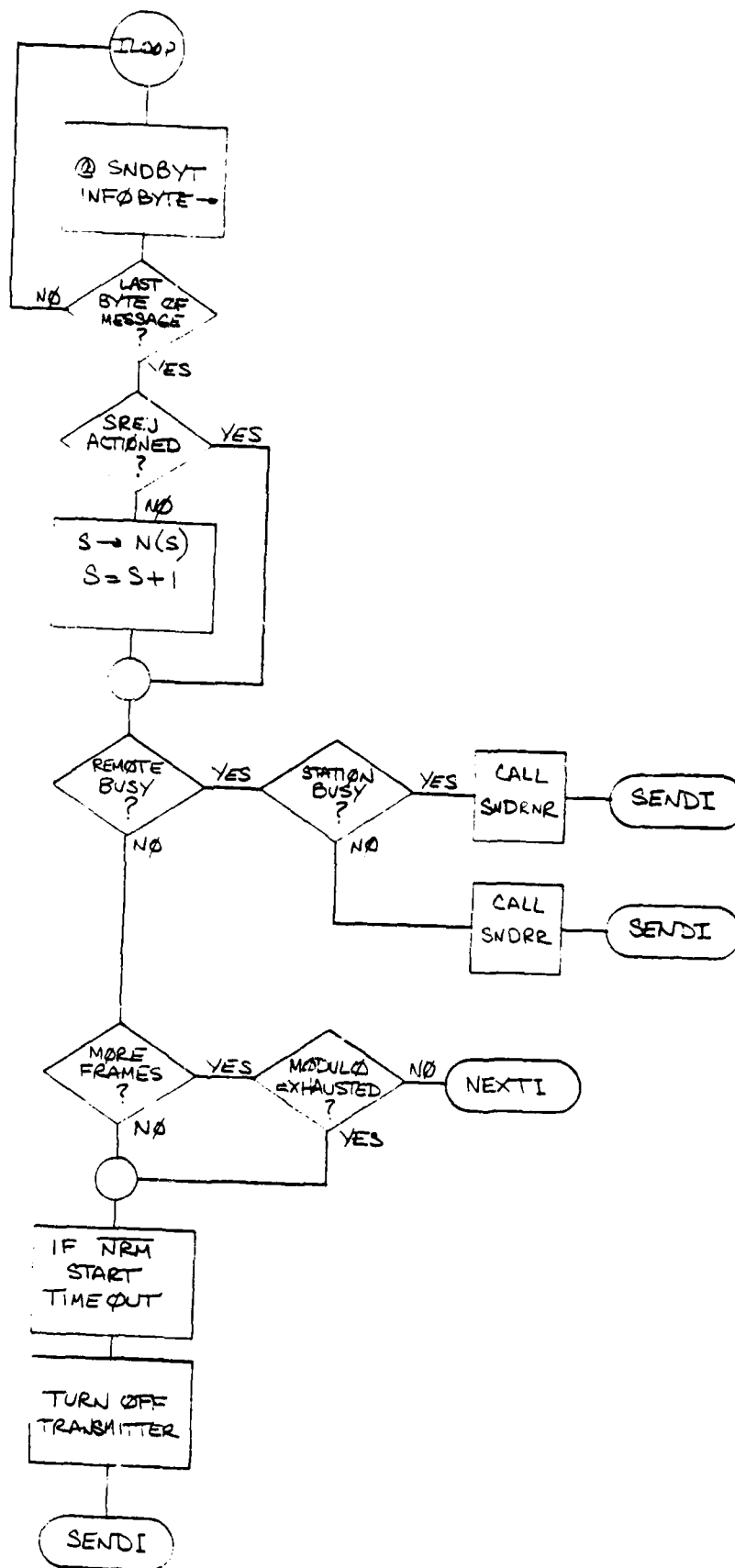


Figure 4-9 continued SENDI Process (3/3)

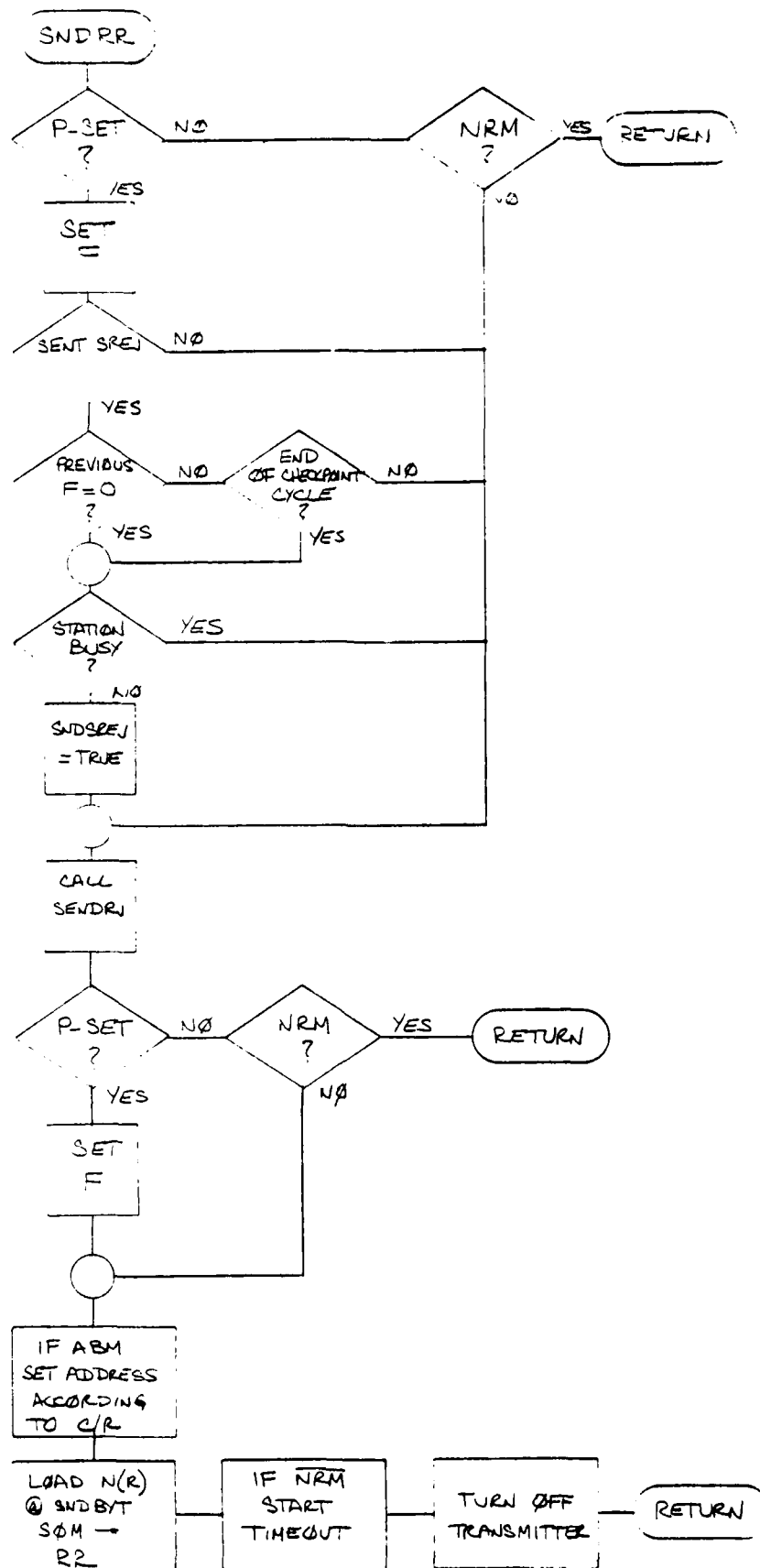


Figure 4-10 SNDRR Subroutine

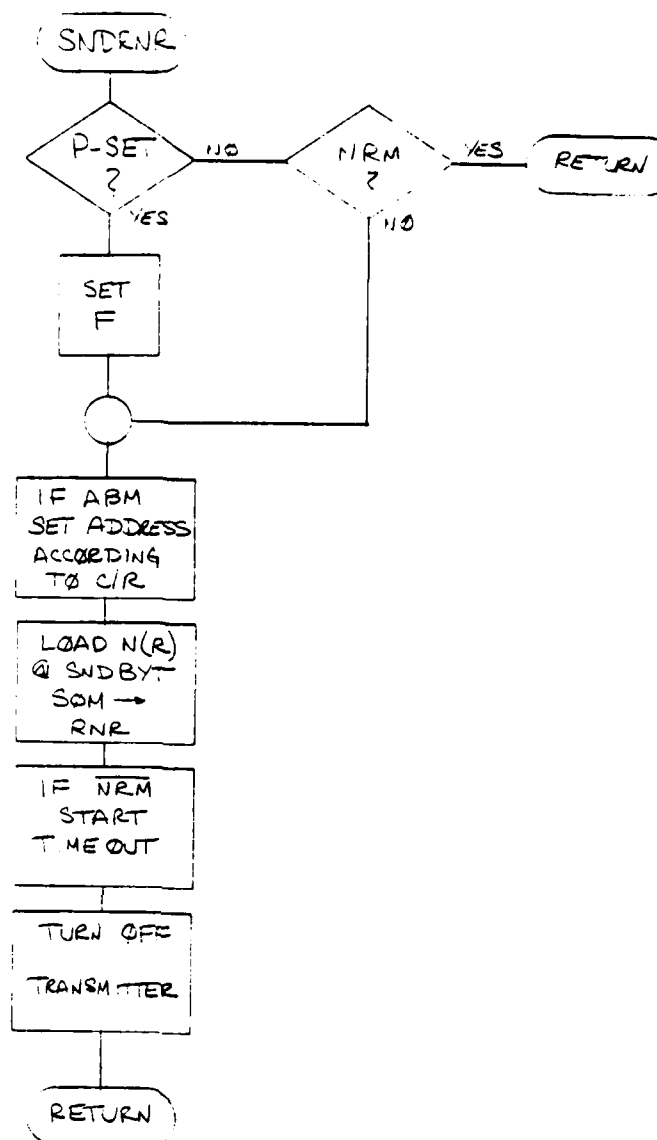


Figure 4-11 SNDRNR Subroutine

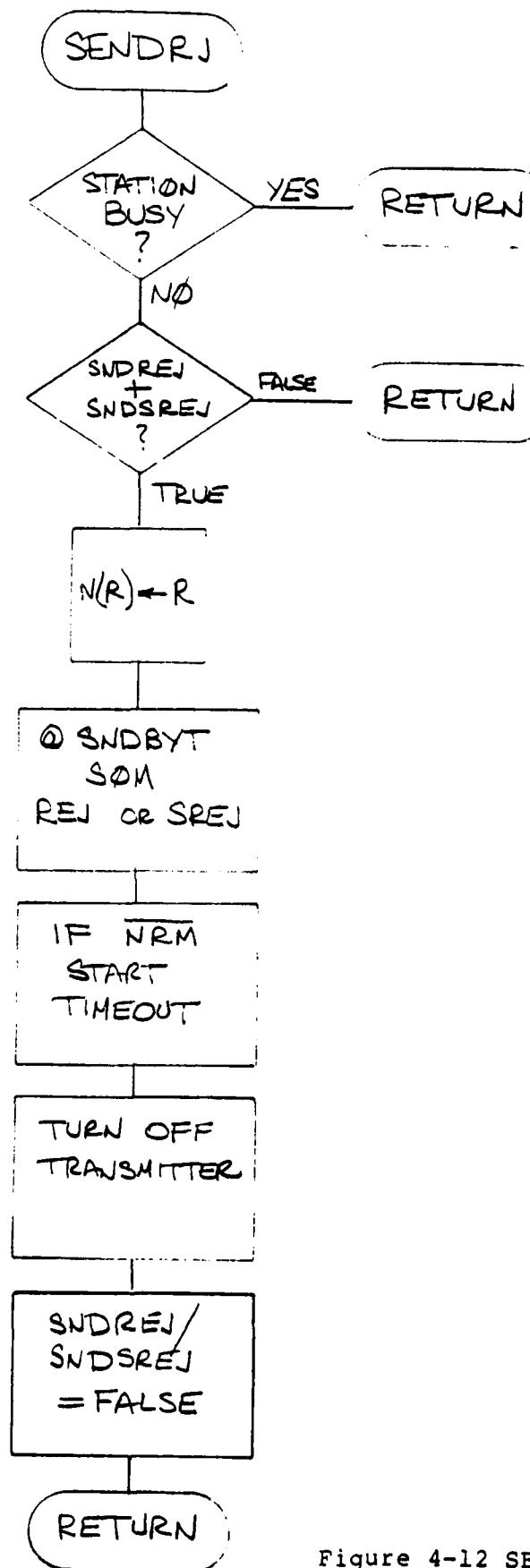


Figure 4-12 SENDRJ Subroutine

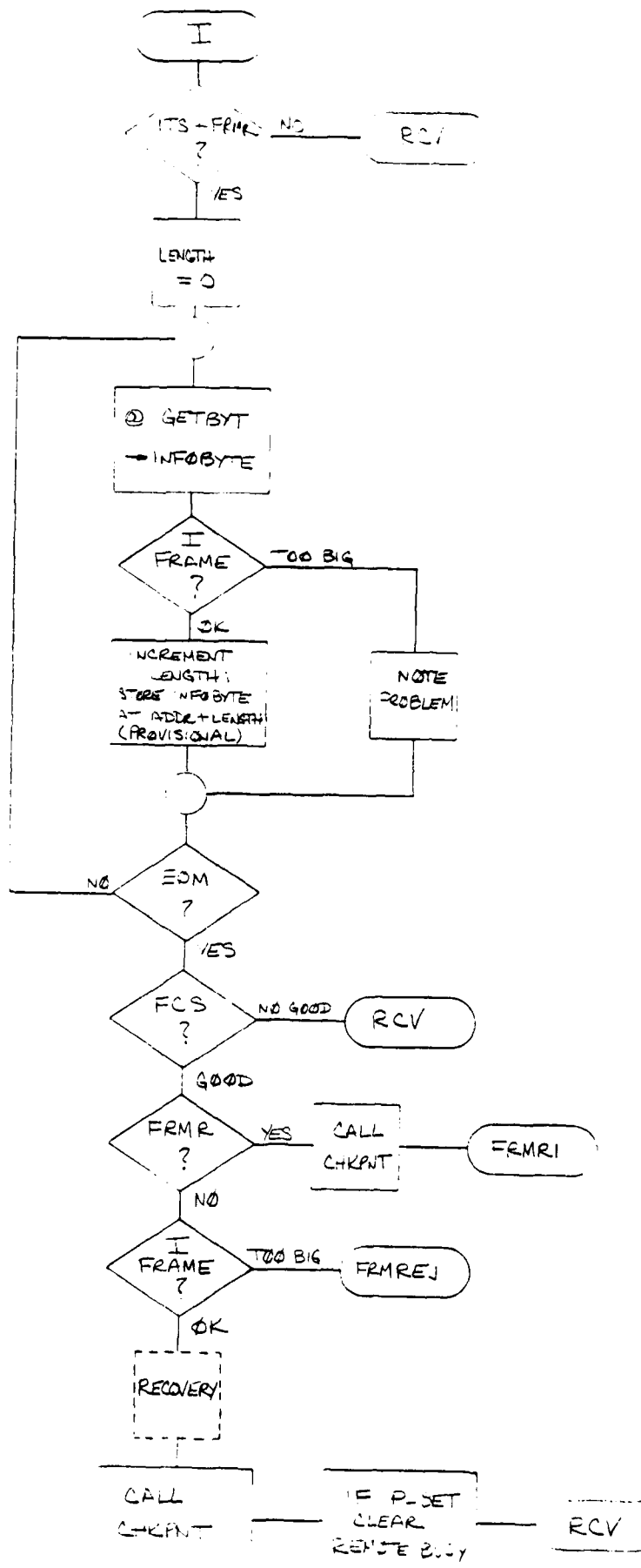


Figure 4-13
Transmit I
Subroutine (1/4)
4-39

CHECKPOINT RECOVERY

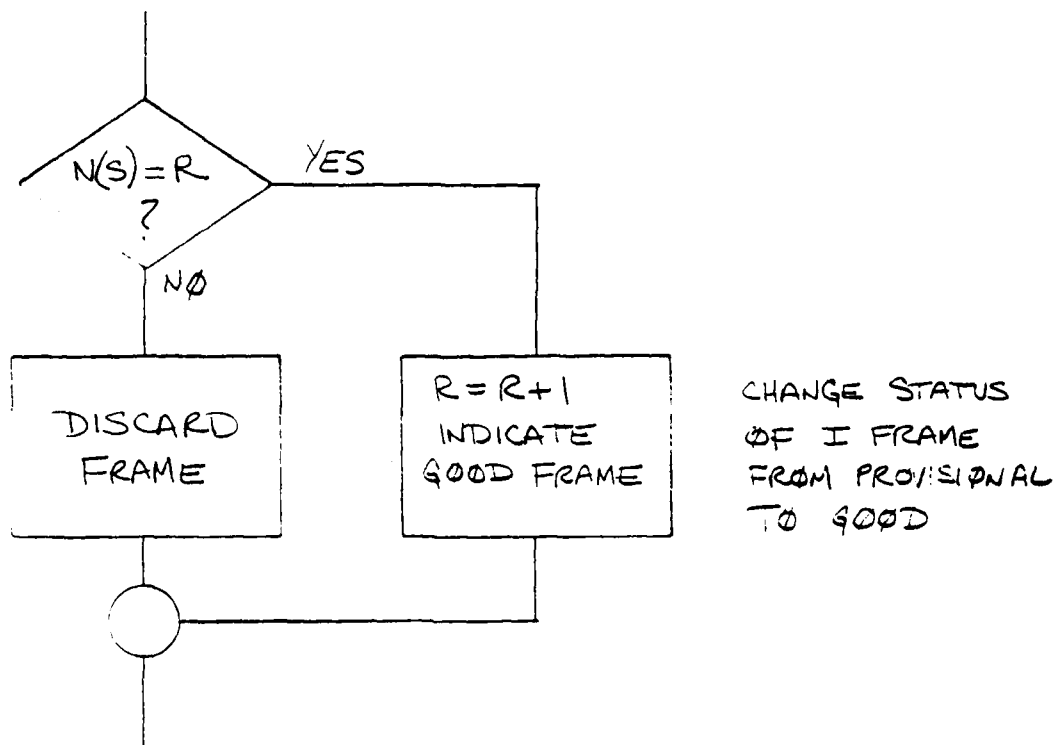


Figure 4-13 continued
Optional Checkpoint Recovery Module
for I Subroutine (2/4)

REJECT RECOVERY

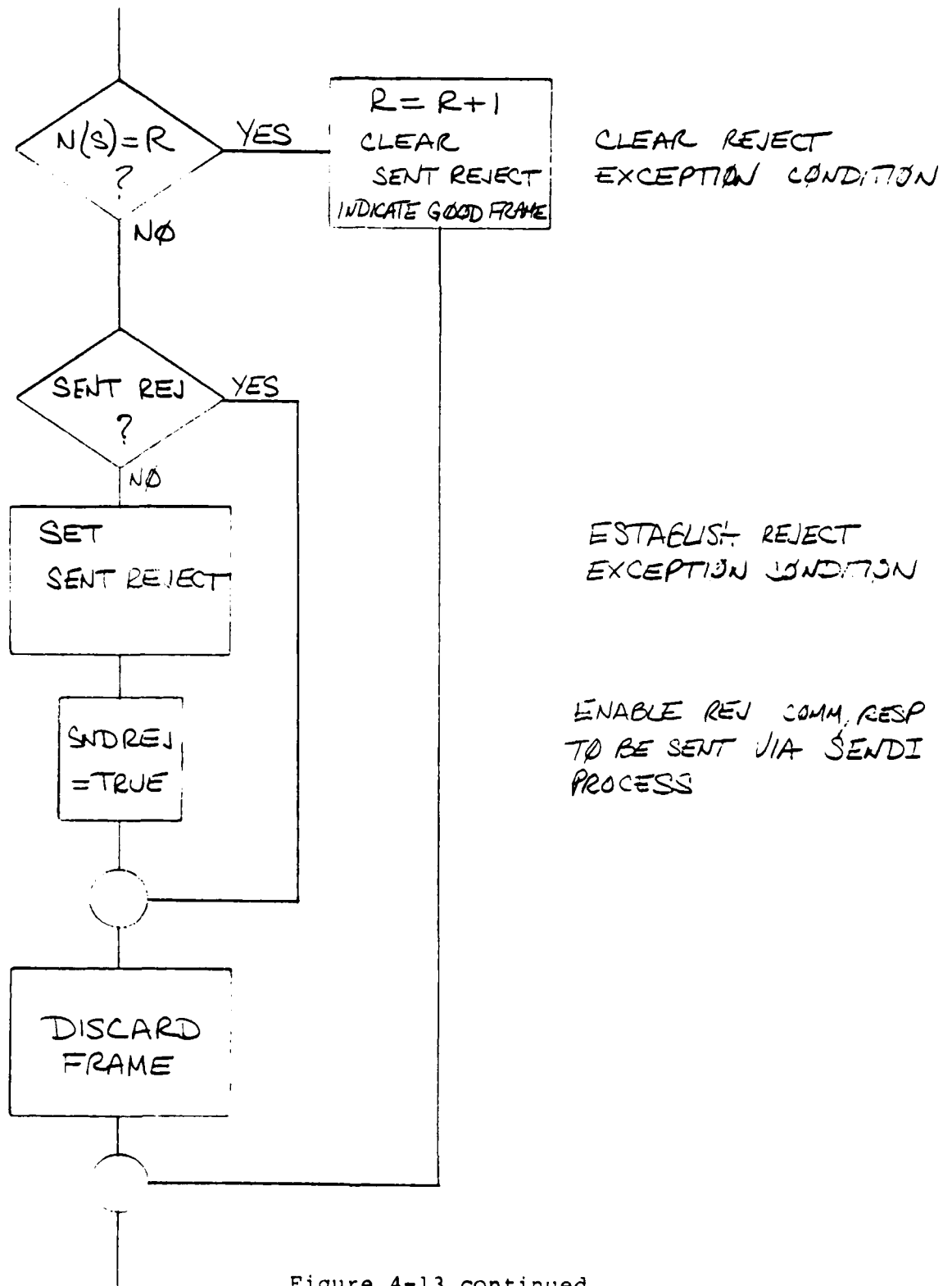


Figure 4-13 continued
Optional REJECT RECOVERY Module
for I Subroutine (3/4)

SREJECT RECOVERY

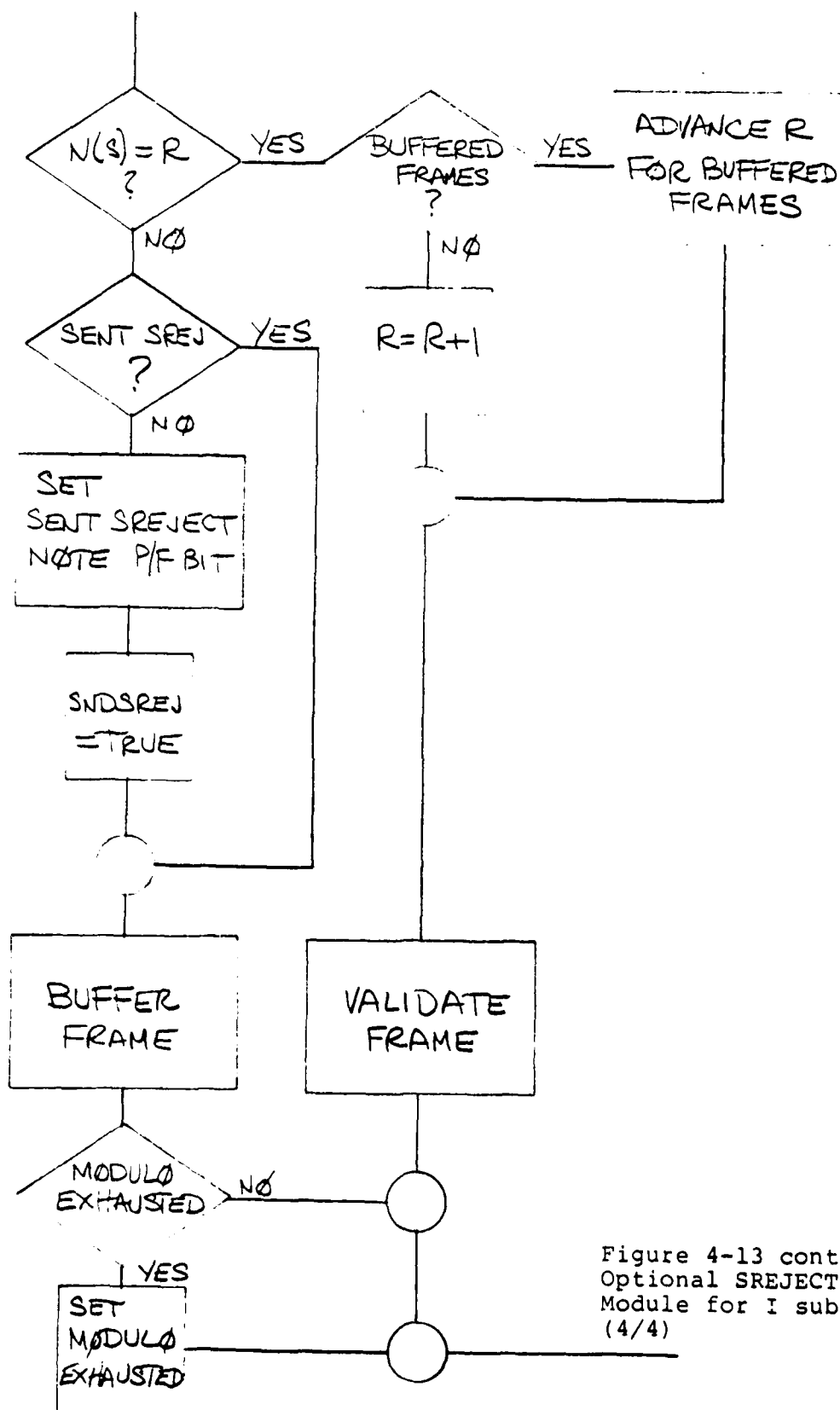


Figure 4-13 continued
Optional SREJECT RECOVERY
Module for I subroutine
(4/4)

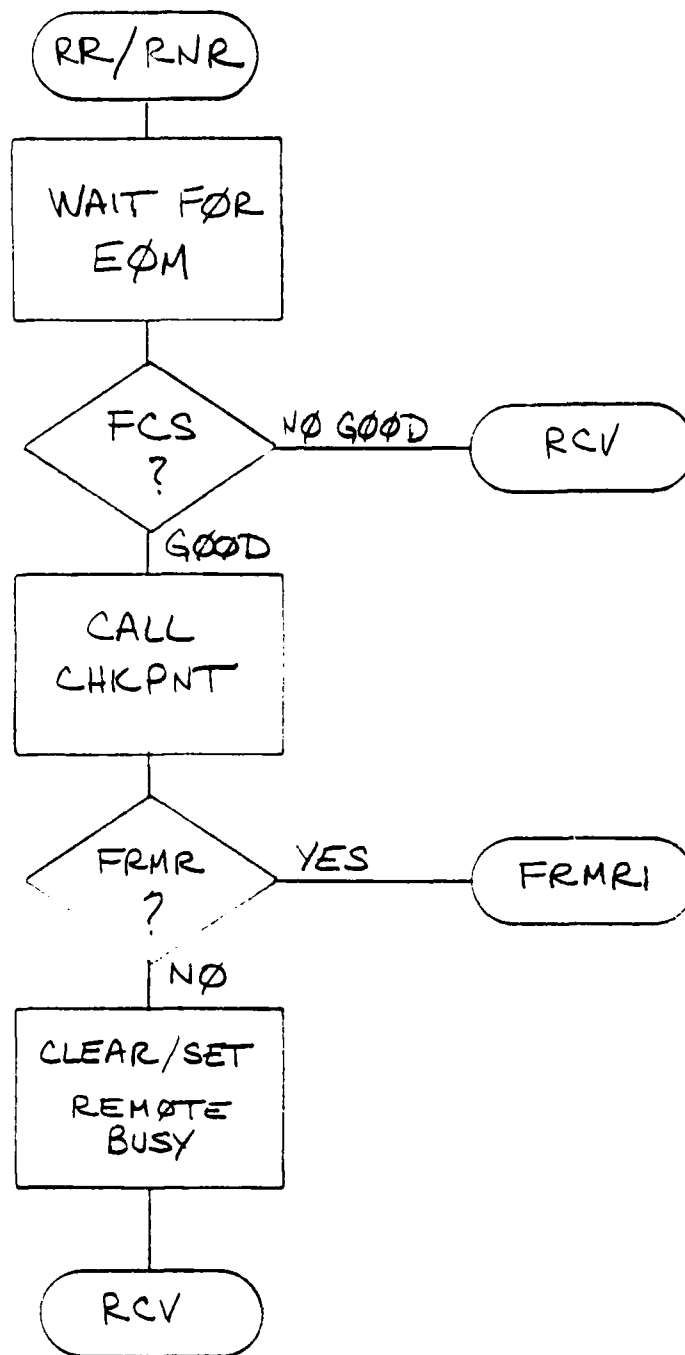


Figure 4-14 Receive Ready/Receive Not Ready Subroutine

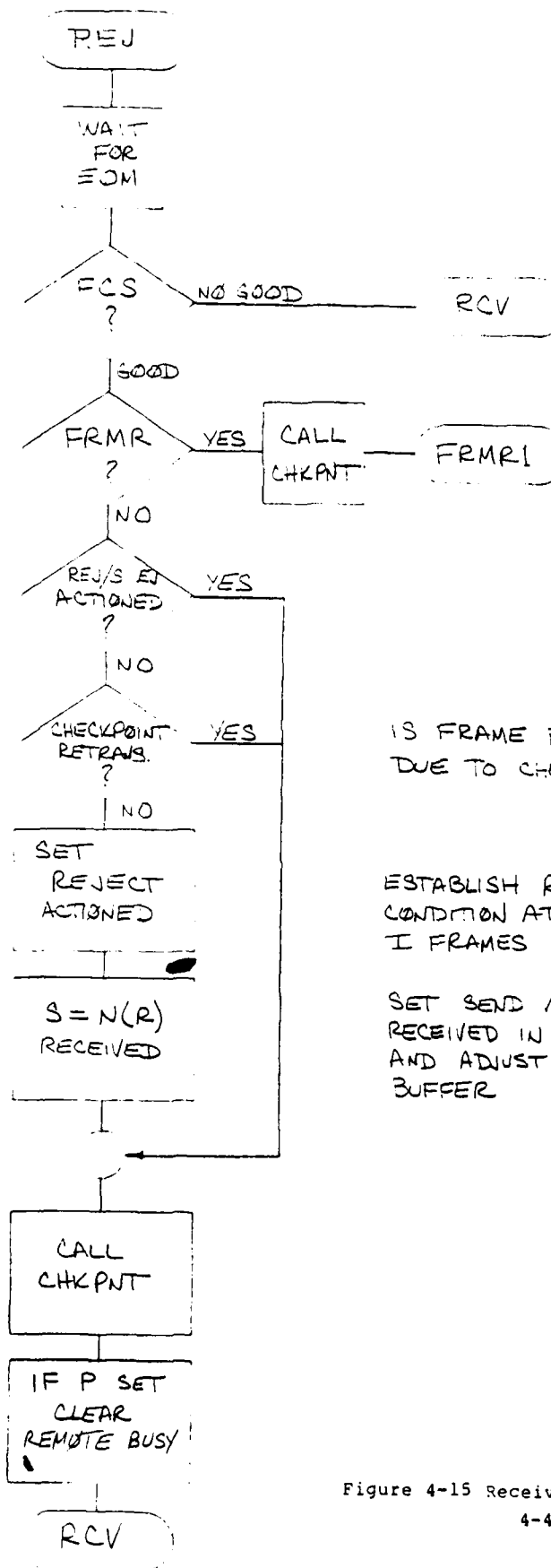
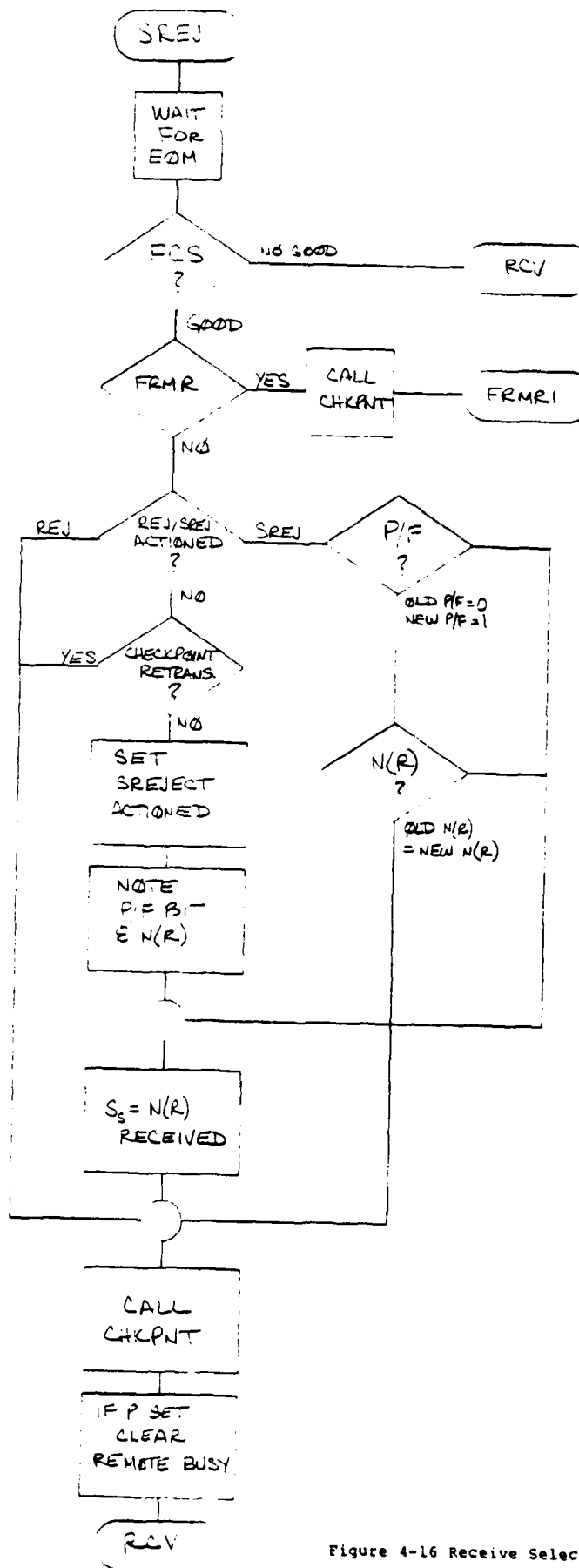


Figure 4-15 Receive REJ Subroutine



IF ORIGINAL P/F = 0 FOR SECONDARY OR PRIMARY/COMBINED, DISABLE ACTIONING NEXT SREJ IF P/F = 1 AND N(R) HAS SAME VALUE AND NUMBERING CYCLE AS THE FIRST SREJ

Figure 4-16 Receive Selective Reject Subroutine

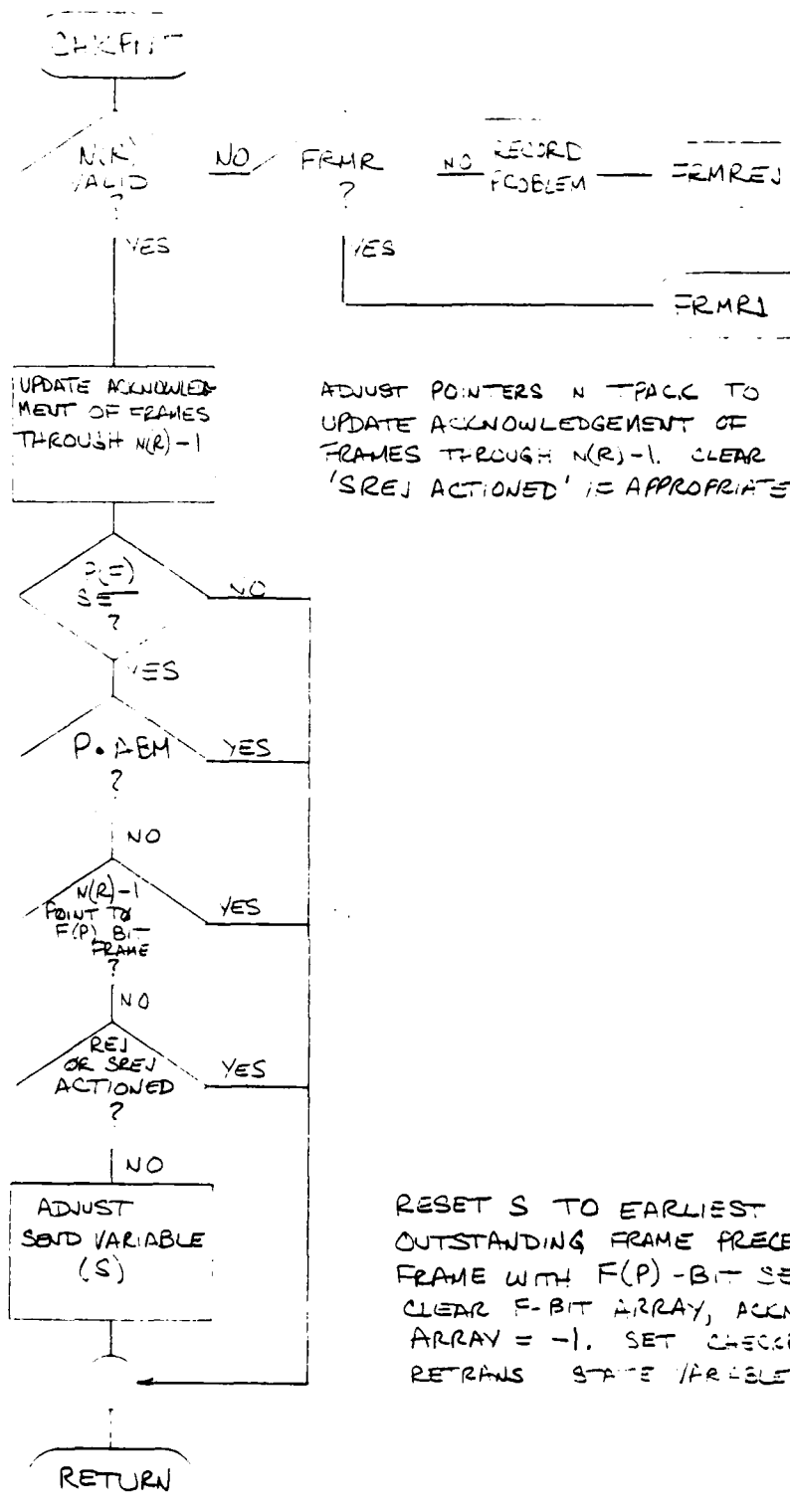


Figure 4-17 Checkpoint Subroutine

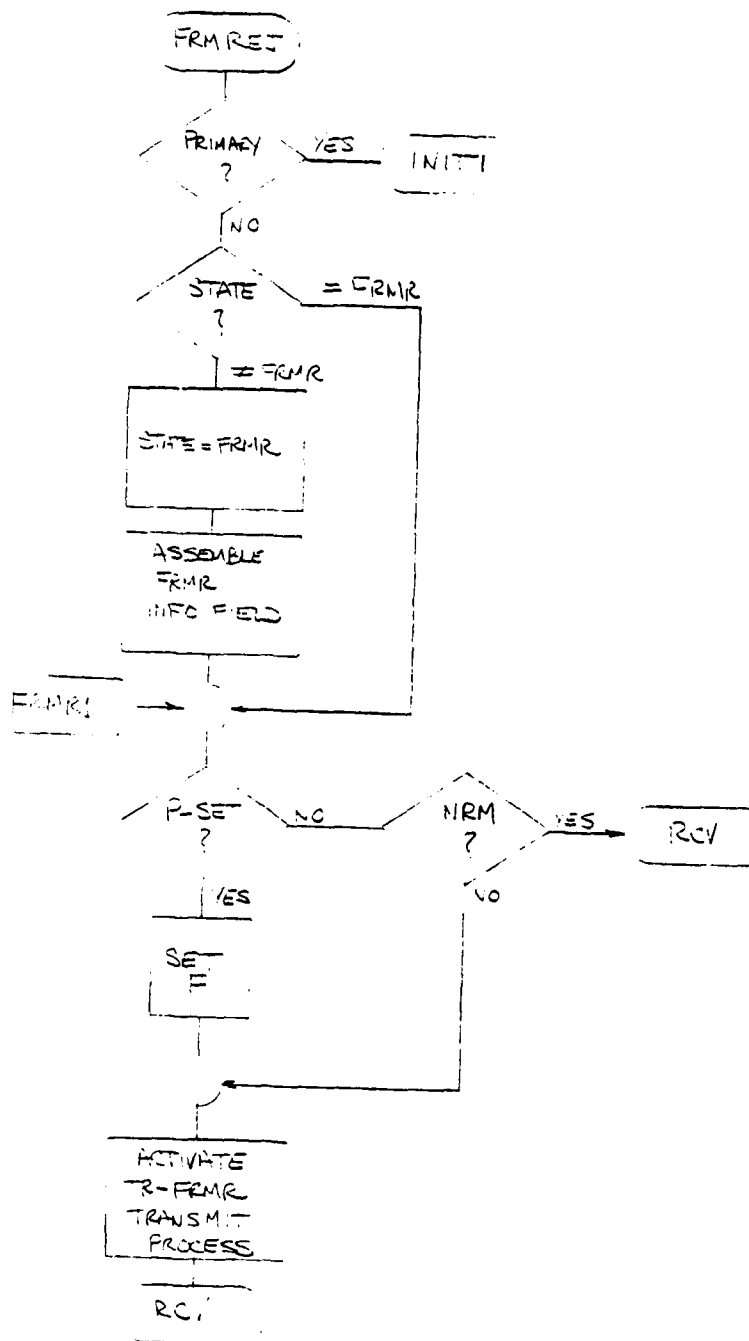


Figure 4-18 Transmit Frame Reject Routine

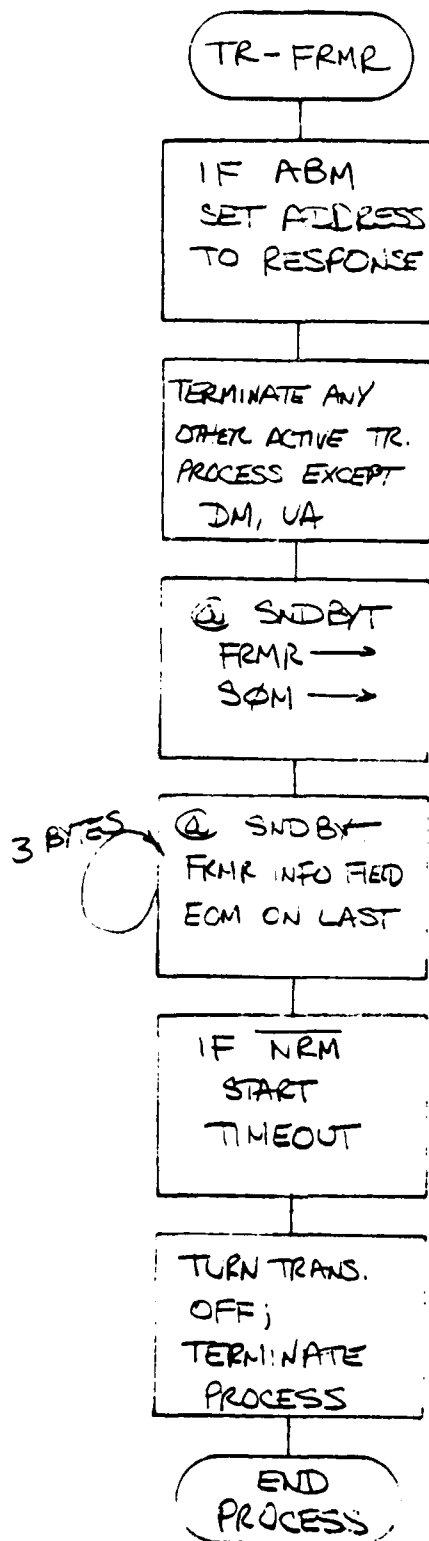


Figure 4-19 Transmit FRMR Process

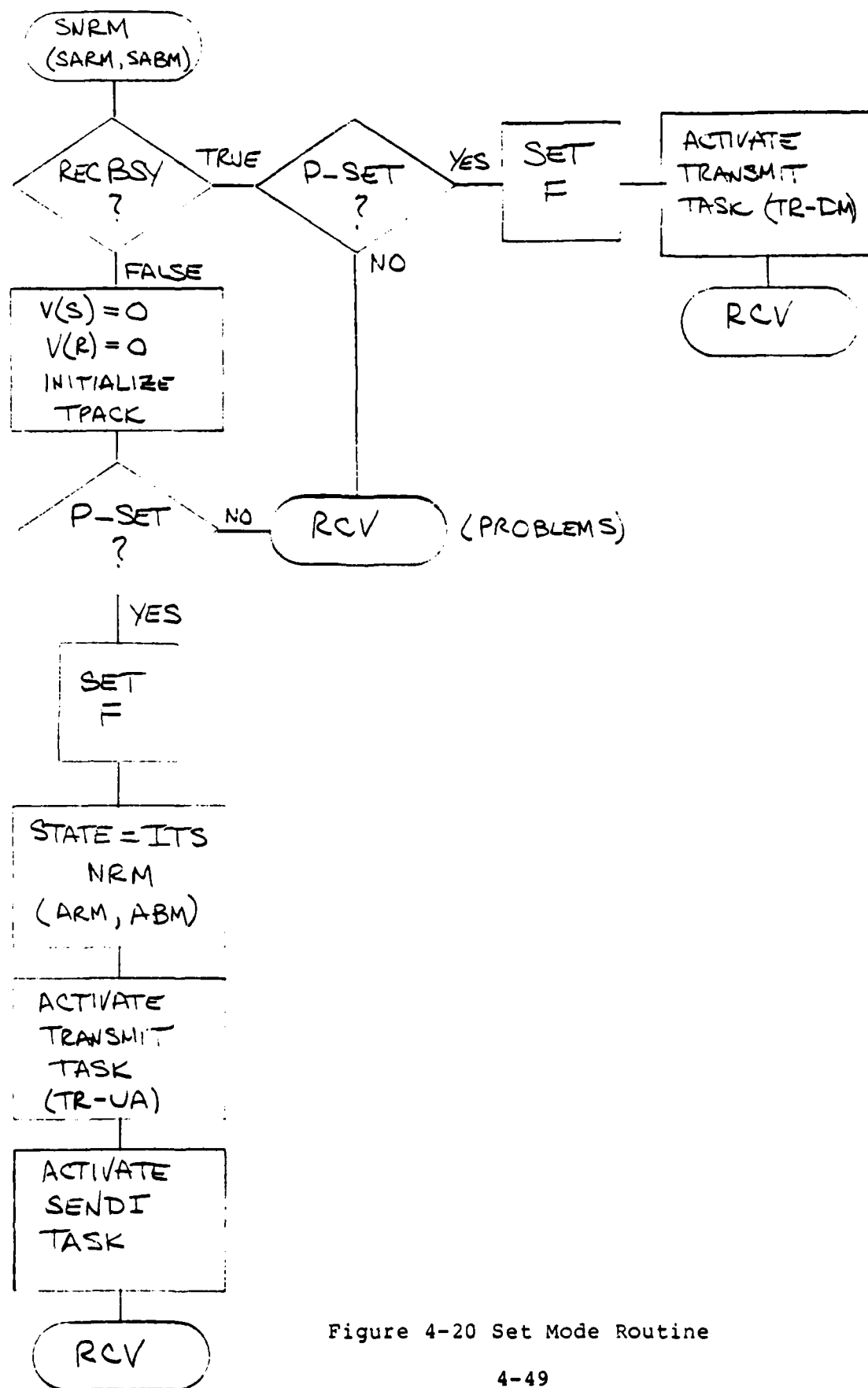


Figure 4-20 Set Mode Routine

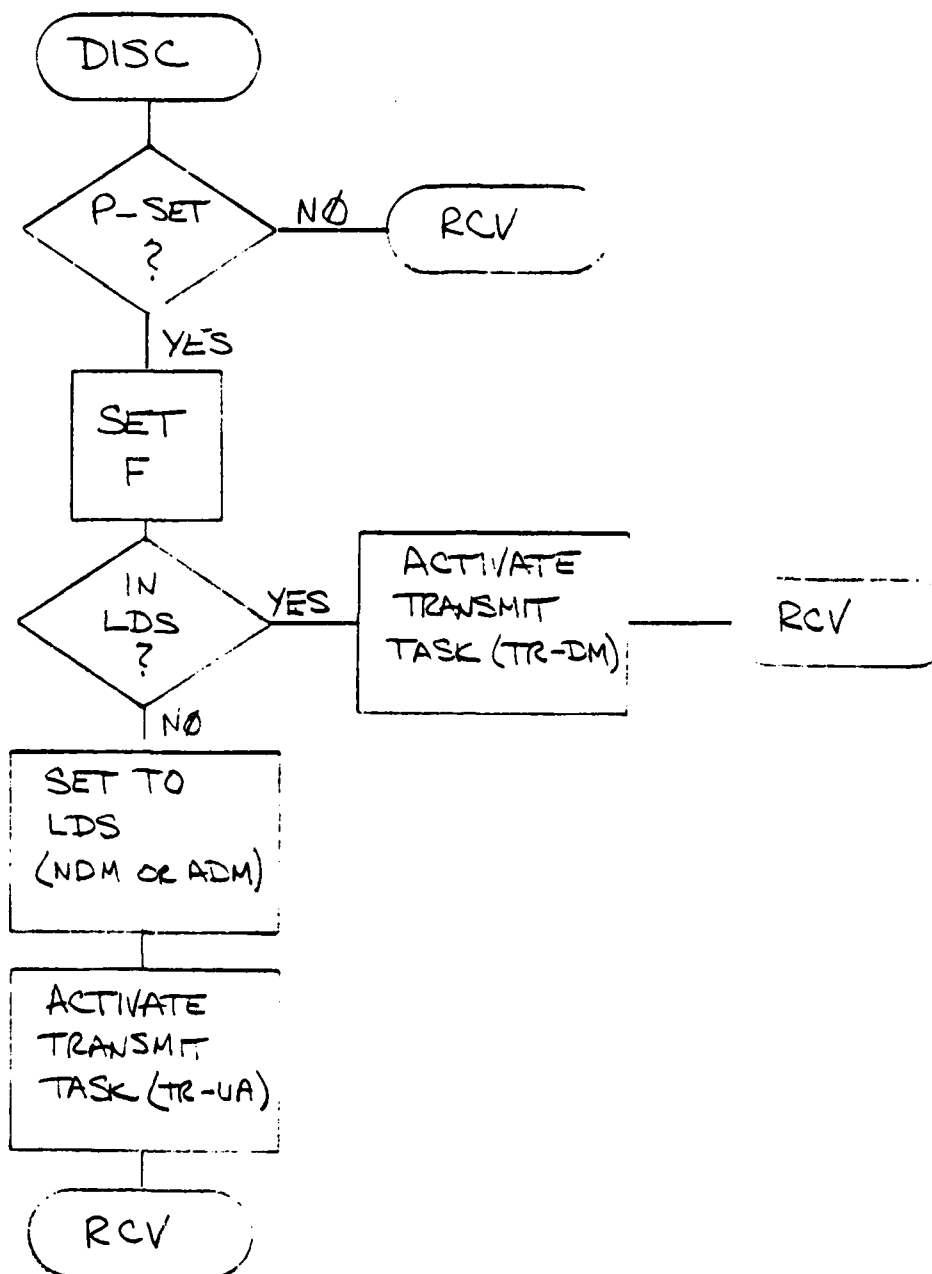
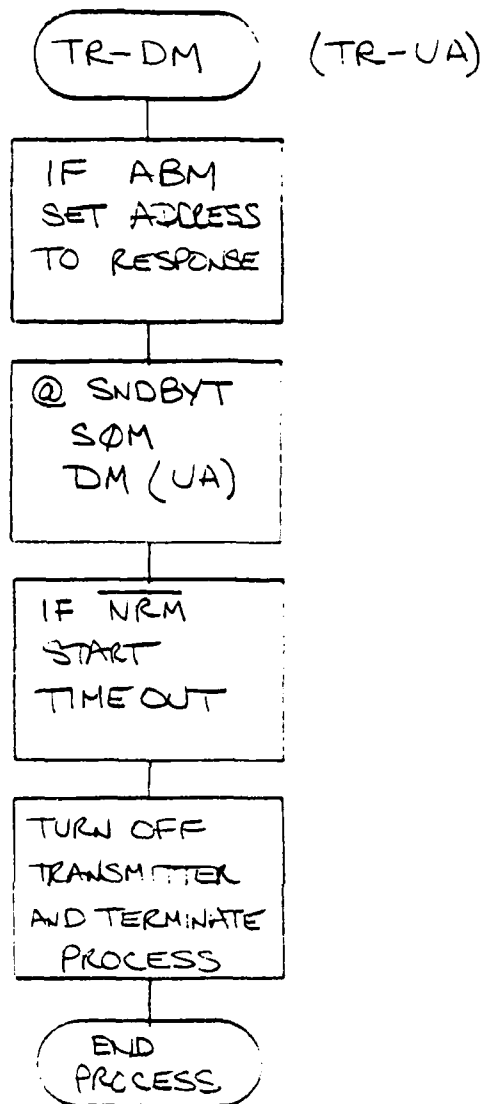


Figure 4-21 Disconnect Routine



IF ABM SET 6856
TO SECONDARY

TURN ON TRANSMITTER
& SEND DM (OR UA)

Figure 4-22 Transmit DM Process

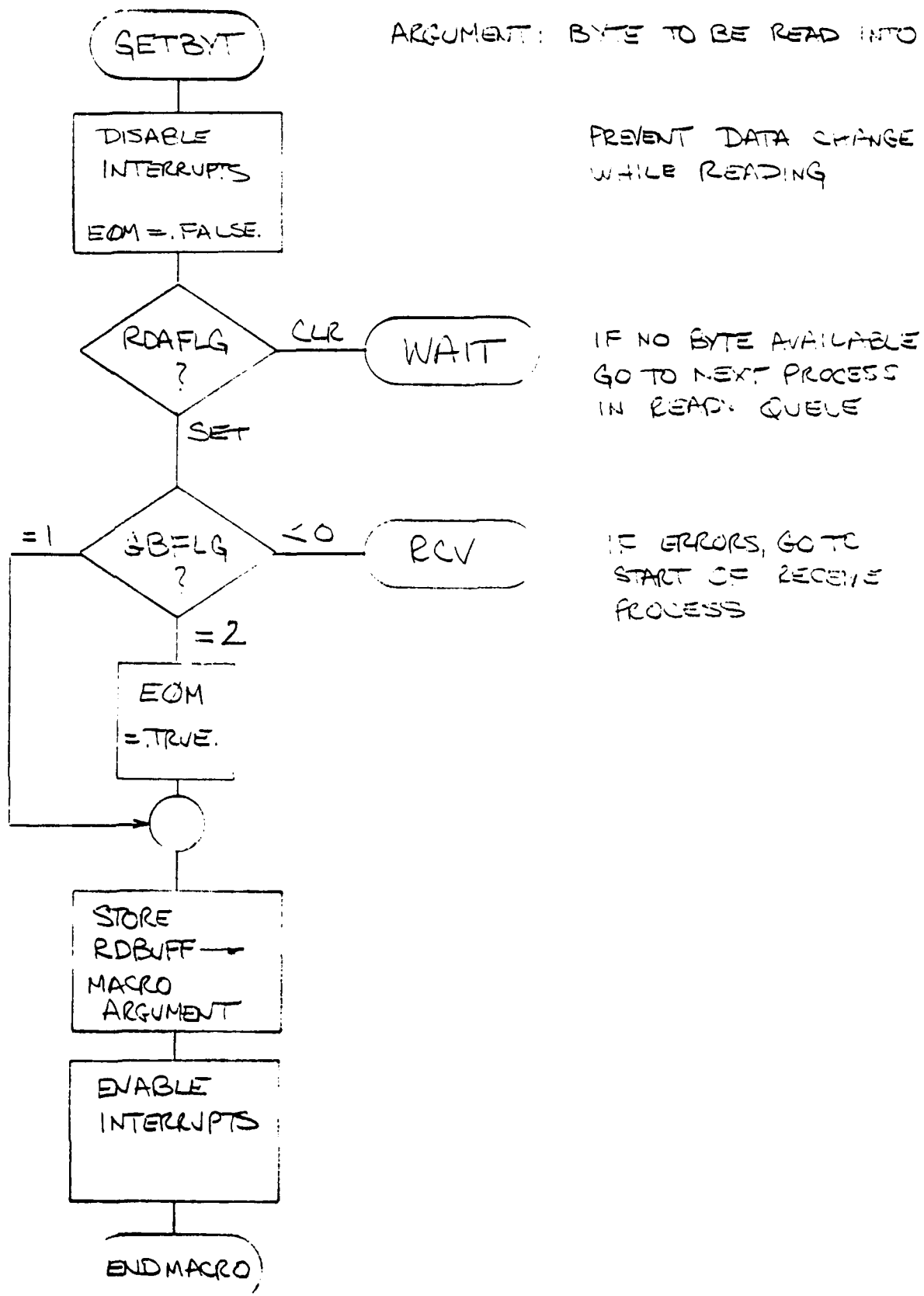


Figure 4-23
Read Data Byte Macro

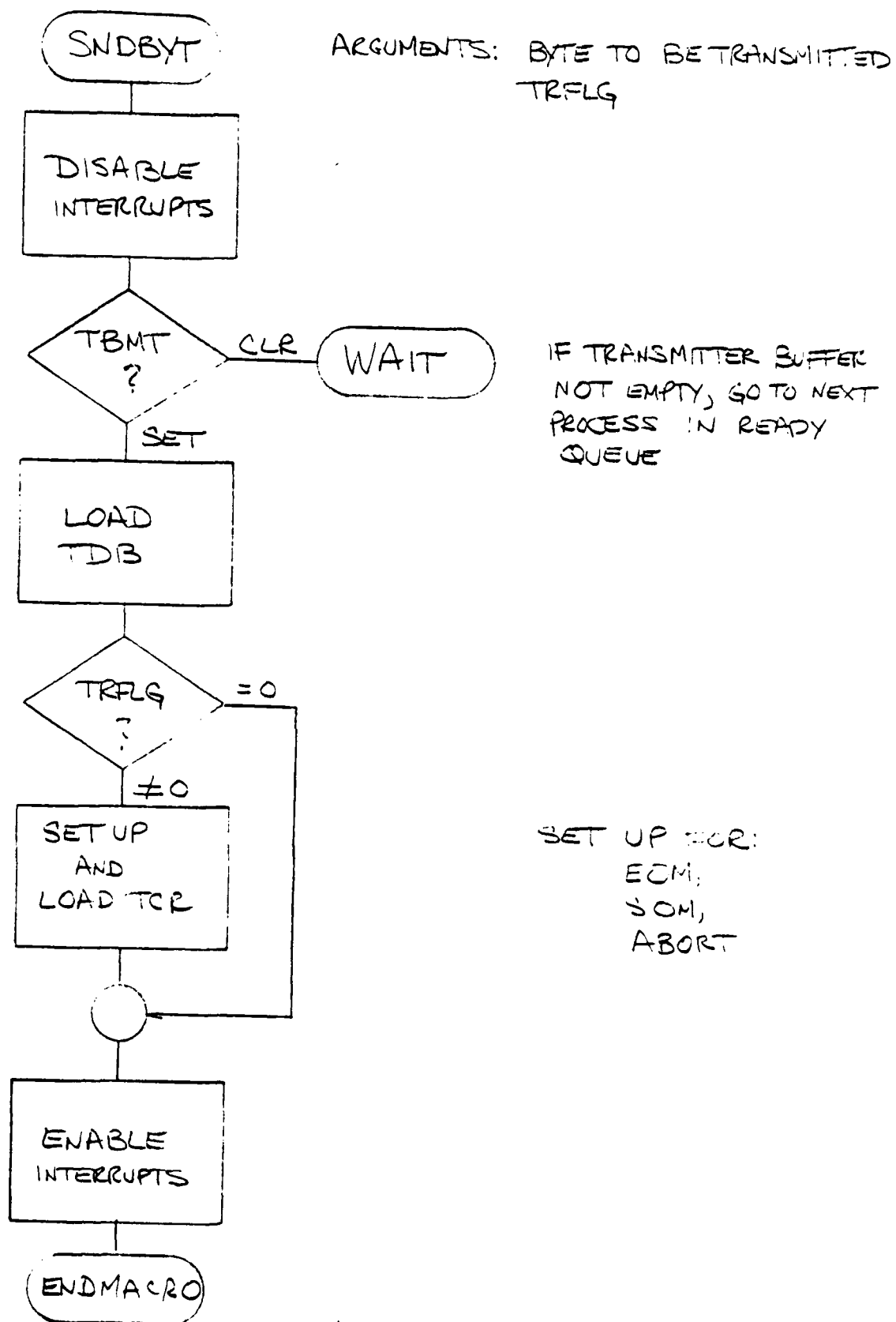


Figure 4-24
Transmit Data Byte Macro

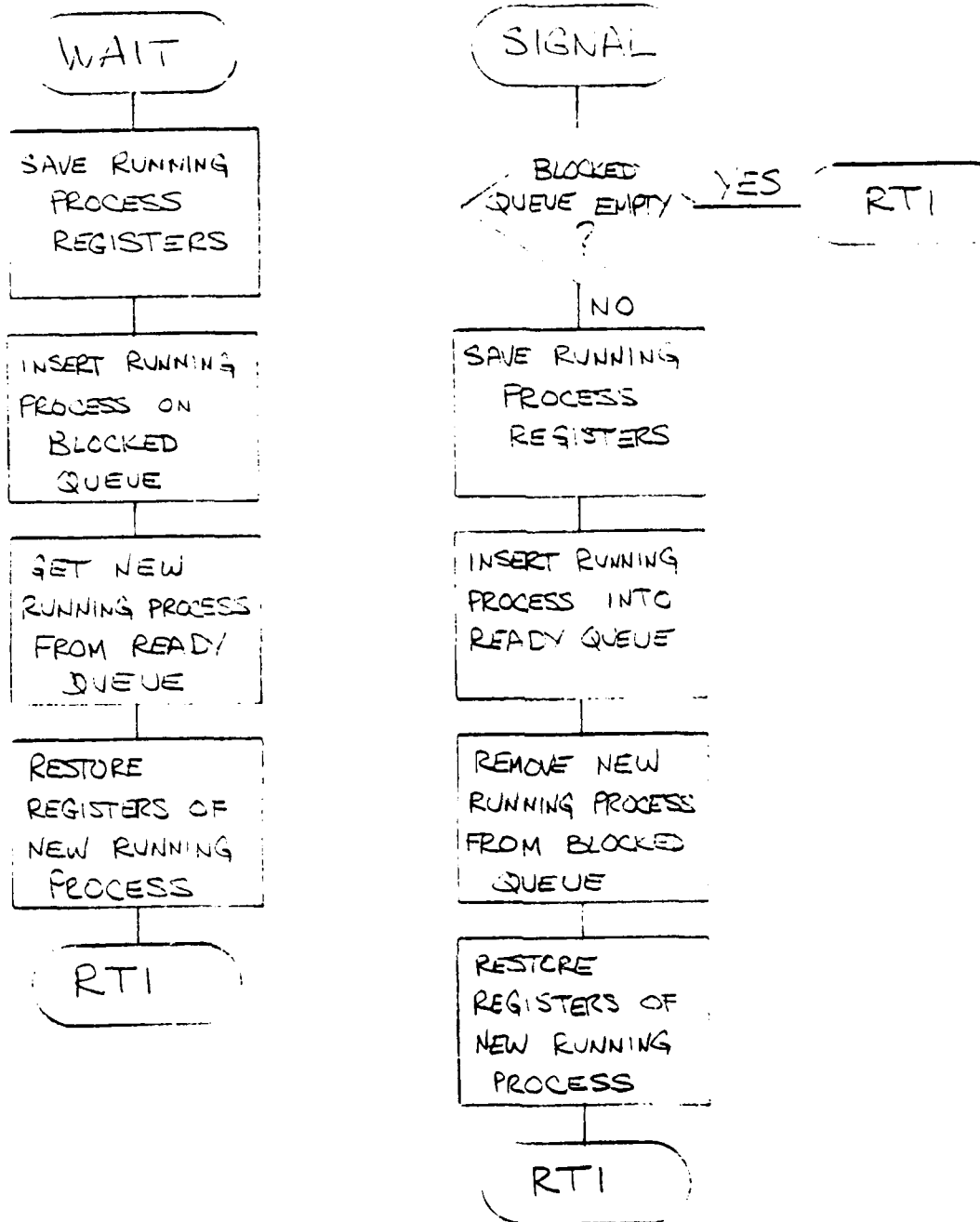


Figure 4-25 WAIT & SIGNAL Processes

INTERRUPT SERVICE ROUTINE

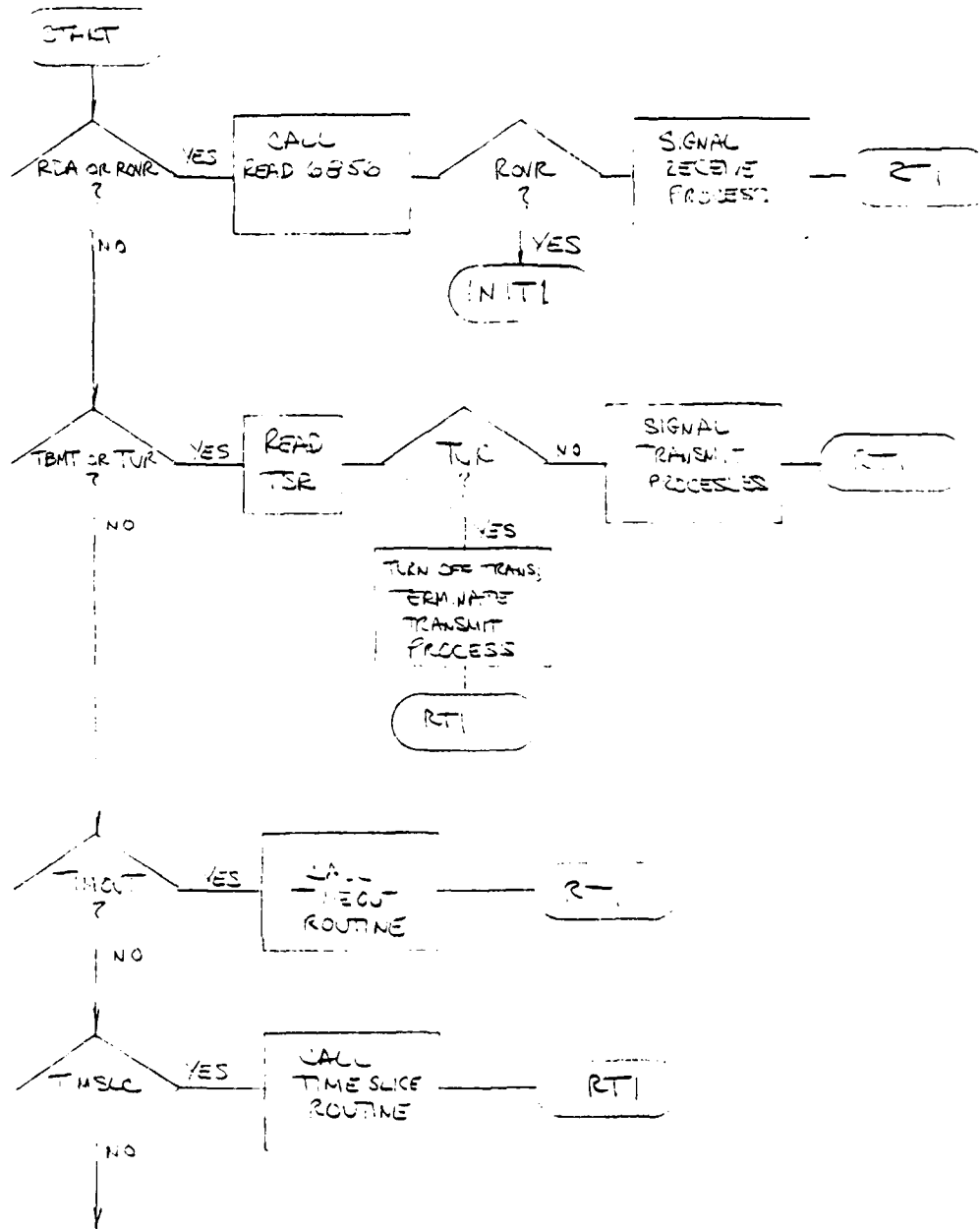
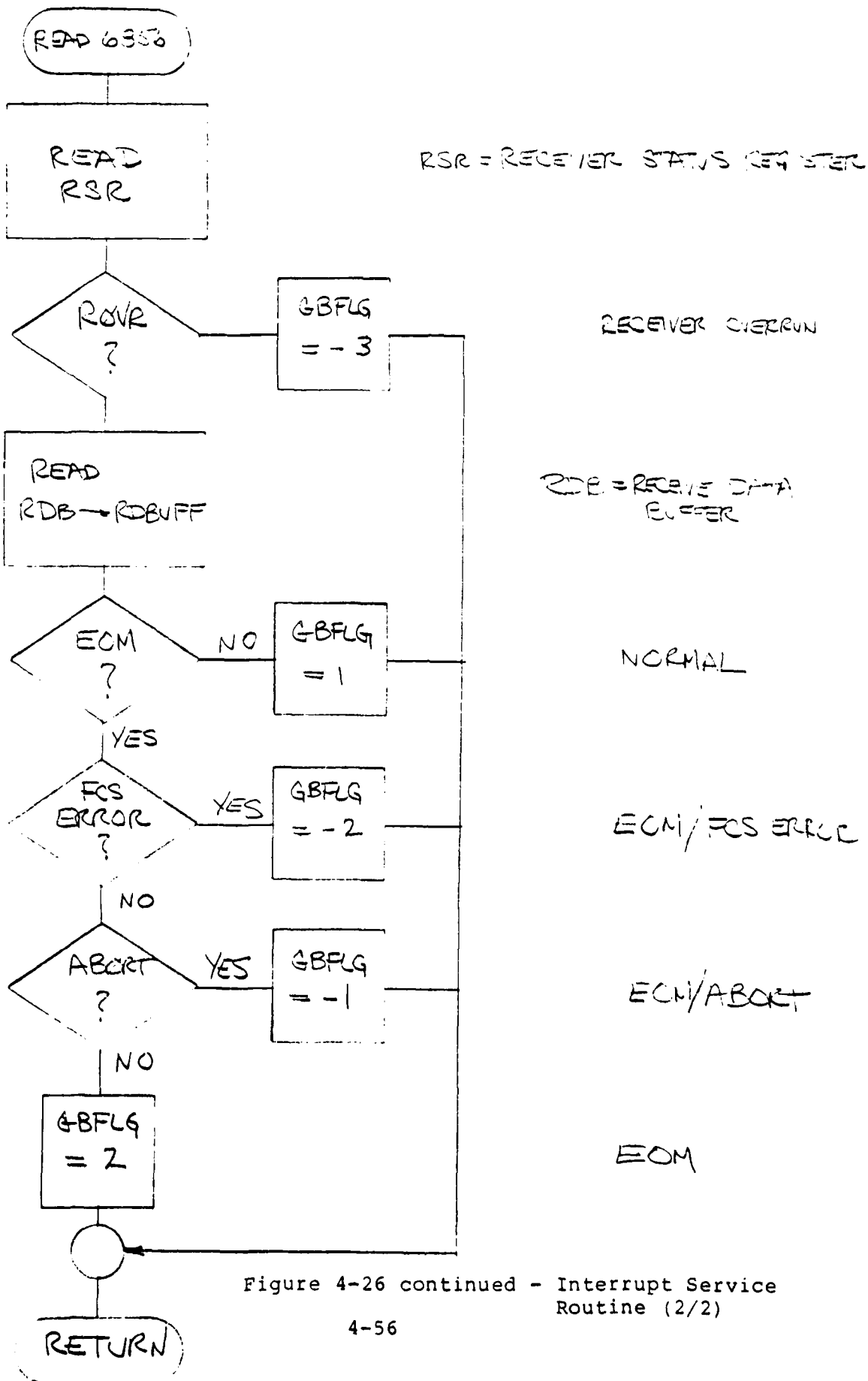


Figure 4-26 Interrupt Service Routine (1/2)



5.0 MICROPROCESSOR CODING AND TESTING

An example of the 6800 microprocessor code is shown in Figure 5-1. This figure shows the assembly language instructions and assembled code for the RCNTRL subroutine. The description of this subroutine was given in Section 4. This subroutine requires 94 bytes for instructions plus 39 bytes for tables for a total of 133 bytes in ROM. Testing of the 6800 code was accomplished on a 6800-based micro-computer. An exhaustive test was made of all 256 possibilities of the input control field. The resulting frame type, P/F bit, N(R), and N(S) extracted was examined for correctness and validity as compared to the frame valid table.

PKR LINE	ADDR	B1	B2	B3	B4	TEST	DESCRIPTION
30							*** KNTNL SUBROUTINE
31							*
32							* REFERENCES: CMTAB
33							* CMTAB
34							* VALTAB
35							* FKTAB
36							* STAT
37							* MODIFIES: PULP
38							* NSP
39							* ETYPE
40							* EXTRACTS PROVISIONAL F/F BIT, N(K) AND N(S)
41							* IF APPLICABLE, DETERMINES FRAME TYPE, CHECKS
42							* COMMAND/RESPONSE FOR VALIDITY AGAINST MODE,
43							* STATION TYPE.
44							
45							
46							
48	000F	B6	00	00			FSU
49	0012	16					LOGA
50	0013	C4	10				ANDR
51	0015	F7	00	01			STOB
52							PULP
54	0018	CE	00	6D			LDX
55	0018	16					TAB
56	001C	C4	01				ANDR
57	001E	E1	00				ORR
58	0020	27	21				REU
59	0022	08					IRX
61	0023	16					TAB
62	0024	C4	0F				ORR
63	0026	E1	00				ORR
64	0028	27	19				REU
65	002A	08					ORR
66	002B	8C	00	72			ORR
67	002E	26	F6				ORR
69	0030	16					TAB
70	0031	C4	EF				ORR
71	0033	F1	00				ORR
72	0035	27	0C				REU
73	0037	08					ORR
74	003B	8C	00	76			ORR
75	003E	26	F6				ORR
77							INVALID
78							INVALID
79							INVALID
80							INVALID
81							INVALID
82							INVALID
83							INVALID
84							INVALID
85							INVALID
86							INVALID
87							INVALID
88							INVALID
89							INVALID
90							INVALID
91							INVALID
92							INVALID
93							INVALID
94							INVALID
95							INVALID
96							INVALID
97							INVALID
98							INVALID
99							INVALID
100							INVALID
101							INVALID
102							INVALID
103							INVALID
104							INVALID
105							INVALID
106							INVALID
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112							INVALID
113							INVALID
114							INVALID
115							INVALID
116							INVALID
117							INVALID
118							INVALID
119							INVALID
120							INVALID
121							INVALID
122							INVALID
123							INVALID
124							INVALID
125							INVALID
126							INVALID
127							INVALID
128							INVALID
129							INVALID
130							INVALID
131							INVALID
132							INVALID
133							INVALID
134							INVALID
135							INVALID
136							INVALID
137							INVALID
138							INVALID
139							INVALID
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141							INVALID
142							INVALID
143							INVALID
144							INVALID
145							INVALID
146							INVALID
147							INVALID
148							INVALID
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151							INVALID
152							INVALID
153							INVALID
154							INVALID
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157							INVALID
158							INVALID
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161							INVALID
162							INVALID
163							INVALID
164							INVALID
165							INVALID
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167							INVALID
168							INVALID
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170							INVALID
171							INVALID
172							INVALID
173							INVALID
174							INVALID
175							INVALID
176							INVALID
177							INVALID
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183							INVALID
184							INVALID
185							INVALID
186							INVALID
187							INVALID
188							INVALID
189							INVALID
190							INVALID
191							INVALID
192							INVALID
193							INVALID
194							INVALID
195							INVALID
196							INVALID
197							INVALID
198							INVALID
199							INVALID
200							INVALID

Figure 5-1 KNTNL Code
5-2

ERR LINE	ADDR	B1	B2	B3	B4	TEST	STAT	TYPE	GET STATION TYPE & MODE
70	003F	F7	00	01			STAT		VAL TAB-CONTAB,X
79	0042	57					TYPE		TEST AGAINST FRAME TYPE
81	0043	F5	00	07			STAT		INVALID
82	0046	E4	00				STAT		PRIAR-CONTAB,X
83	004B	27	F3				TYPE		
84	004D	E6	16				STAT		
85	004C	F7	00	04			TYPE		
87	004F	C1	05				STAT		
88	0051	2E	19				TYPE		
89	0053	16					STAT		
90	0054	C4	E0				TYPE		
91	0056	54					STAT		
92	0057	54					TYPE		
93	0058	54					STAT		
94	0059	54					TYPE		
95	005A	54					STAT		
96	005B	F7	00	02			TYPE		
97	005E	F6	00	04			STAT		
98	0061	C1	01				TYPE		
99	0063	26	07				STAT		
100	0065	16					TYPE		
101	0066	C4	0E				STAT		
102	0068	54					TYPE		
103	0069	F7	00	03			STAT		
104	006C	39					TYPE		
105	006D	00					STAT		
106	006E	01					TYPE		
107	006E	01					STAT		
108	006F	05					TYPE		
109	0070	09					STAT		
110	0071	00					TYPE		
111	0072	B3					STAT		
112	0073	43					TYPE		
113	0074	43					STAT		
114	0075	0F					TYPE		
115	0076	B7					STAT		
116	0077	BF					TYPE		
117	0078	0F					STAT		
118	0079	3F					TYPE		
120	007A	F8					STAT		
121	007B	F8					TYPE		
122	007C	F8					STAT		
123	007D	F8					TYPE		
124	007E	F8					STAT		
125	007F	40					TYPE		
126	0080	0B					STAT		
127	0081	0B					TYPE		
128	0082	0B					STAT		

ERR LINE	ADDR	R1	R2	R3	R4	OP	DATA
129	00B3	AB				ICE	10101000R FARK
130	00B4	08				FCR	00001000R RSFT
131	00B5	B8				FCR	10111000R SGRH
132	00B6	08				FCR	00001000R SGRH
134	00B7	01	02	03	04	FCR	1,2,3,4,5,6,7,8,9,10,11,12,13
135	00B8	05	06	07	08	FFCR	
136	00B9	09	0A	0B	0C		
137	00BA	0D					
139	0054					END	

ASSEMBLER ERRORS = 0

RESIN

CROSS REFERENCE

LABEL	VALUE	REFERENCE			
UNITID	D 0000	-7	49		
UNITAB	F 005B	54	66	74	84 -106
UNONE	F 006C	88	99	-104	
UNITAR	F 0087	84	-134		
FTYPE	D 0004	-11	78	85	97
INVLID	F 0030	-77	83		
MATCH	F 0043	58	64	72	-81
MEMORY	M 0000	0			
MARG	D 0000	0			
NRG	D 0002	-9	96		
NSF	D 0003	-10	103		
POLEP	D 0001	-8	52		
RCNTRL	F 000F	27	-49		
TESF1	F 0007	-23	25		
SHACN	S 0000	0			
STAT	D 0005	-12	81		
US11	F 0026	-63	67		
US12	F 0033	-71	75		
UNITAB	F 007A	82	-120		

6.0 DISCUSSION OF FEASIBILITY

As discussed previously, one of the objectives of this program is to determine the practicality of using a microprocessor, such as the M6800, to implement the unbalanced normal, unbalanced asynchronous, and balanced asynchronous class of procedures. Two major factors affecting the feasibility are the number of instructions required to implement the protocol, and the time necessary to execute these instructions. The total number of instructions has a significant effect on the cost of developing a processor-based system, and the throughput (or baud-rate over the communication line in this instance) is determined by the execution speed through critical paths on the program. These factors are discussed below.

6.1 MEMORY REQUIREMENTS

The number of instructions required to implement the protocol including REJ or SREJ can be estimated by examining the detailed flow charts in Section 4. The protocol including pure SREJ is estimated to require 1300 instructions; this represents an increase of 450 instructions over the protocol without SREJ. The pure REJ protocol is estimated at 100 instructions less or 1200 instructions. Approximately 250 instructions will be required for the operating system, depending on desired features. RAM is required for variable storage and data buffers.

6.2 EXECUTION TIME

The speed at which the microprocessor can execute the protocol in real-time depends to a large extent on the actual

hardware/software design: The hardware design can be "standard" or it can include many processes accomplished in hardware (such as the F6856). For the purpose of this program, the standard approach with the aid of the F6856 is assumed. The software design must address the time-critical portions of the simultaneous transmit/receive processes to ensure that these critical processes may be serviced in real time. For this program, no attempt has been made to optimize these processes, since a thorough analysis is required to determine just what is "critical". However, some rough estimates can be made based on the current state of the design.

Assuming a MPU rate of 1 cycle/microsec. it appears that a 9.6 or 19.2 kilobit/sec. transmission rate would not be too difficult. That is, a 19.2 kilobit/sec. rate is equivalent to 400 microseconds per byte transmitted, which is approximately 100 instructions. It should be possible to implement the critical parts of the send/receive process using between 100 and 200 instructions. A more thorough analysis might reveal that 100 kilobit/sec rate may be possible, but certainly difficult. A faster MPU and additional hardware might be required. Another tradeoff that can be made is memory for speed; that is, table look-up may be used in some cases to reduce the number of instructions required to be executed.

7.0 REFERENCES

1. "Use of a Microprocessor To Implement an ADCCP Protocol (Federal Standard 1003)" Delta Information Systems, Inc. July, 1980
2. Malcom Easton, "Batch Throughput Efficiency of ADCCP/ HDLC/SDLC Selective Reject Protocols" Data Communications pp 187-195, February 1980.

APPENDIX A OPERATING SYSTEM

The design of the operating system (OS) is important because it can have a significant impact on the time required to switch the processor among concurrent processes and to handle interrupts. The approach taken makes use of the "standard" WAIT and SIGNAL primitives together with event variables. No attempt has been made to design a complete operating system; only those routines required to handle the concurrent processes are included.

Each software process is defined to be in one of three states:

ACTIVE (RUNNING) STATE - Executing computer instructions

BLOCKED STATE - Waiting for the occurrence of an event
in another process

READY STATE - Waiting for processor to run

State Transitions are illustrated in the state diagram of Figure A-1

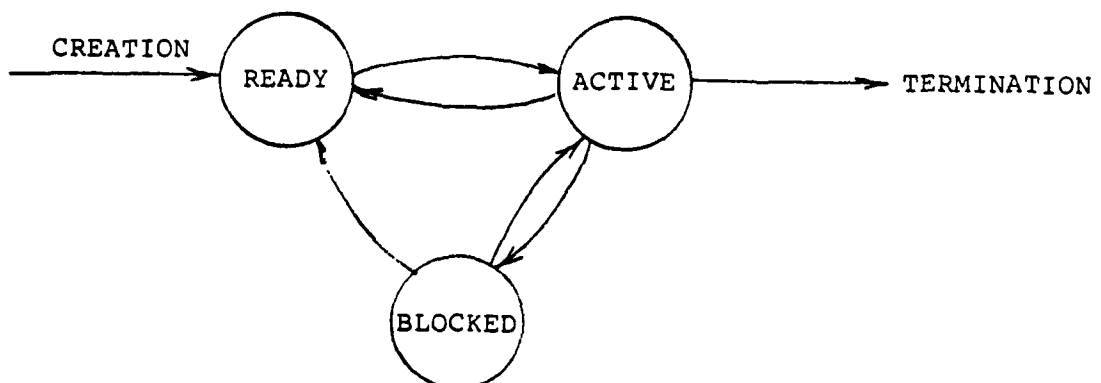


Figure A-1 Process State Diagram

Processes may be created or terminated by other processes, and each process is defined to be either running or on the blocked queue or the ready queue depending on its state. Associated with each process is a process control block (PCB) which contains an area to save the CPU's registers when the process is interrupted, a pointer to the next PCB in the queue, and the process' priority.

If the process currently running become blocked, it is changed from the ACTIVE state to the BLOCKED state via the WAIT routine. For example, if the receive process is executing instructions and wishes to obtain a byte of data from the LSI interface chip buffer, the process tests the event variable RDAFLG to determine whether or not the byte of data is available. If available, the process continues; if not, the WAIT routine is called to save the receive process registers, insert the receive process into the blocked queue, and get a new process from the ready queue, restore the registers of the new process, and run the new process. The receive process continues where it left off after an interrupt from the LSI chip signals that a byte of data is available, the interrupt service routine services the interrupts, and the receive process is moved to the running state via the SIGNAL routine. The SIGNAL routine removes the receive process from the blocked queue and restores it to the running state. Any process is blocked and restored in this way by the WAIT and SIGNAL routines respectively, and by the appropriate interrupt service routine.

The 6800 has but one interrupt input that is maskable.

This means that unless some additional hardware is used, all interrupt lines must be logically ORed and fed to the CPU via the single interrupt input, $\overline{\text{IRQ}}$. This requires that the interrupt service routine poll the various devices that might cause an interrupt to determine what device actually did cause the interrupt. The order in which the devices are polled determines the interrupt priority. The following five events cause interrupts from the 6856 protocol chip:

RDA - Received data available

ROVR - Receiver overrun (data was not read from buffer before new byte was loaded)

TOR - Transmitter overrun

TBMT - Transmitter buffer empty

TUR - Transmitter underrun (data was not loaded in transmitter buffer in time to transmit)

In addition, two timers are assumed to be part of the design, one to provide a time slicing function to interrupt a running process periodically to give the CPU to a different process, and a time-out timer to indicate an overdue response. These two functions may be provided by one timer and appropriate software or by two separate timers.

