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GaAs FET DEVICE MODELING AND PERFORMANCE

J. R. East
G. I. Haddad

Electron Physics Laboratory
Department of Electrical and Computer Engineering
The University of Michigan
Ann Arbor, Michigan 48109

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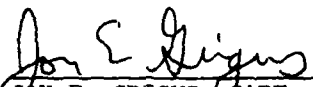
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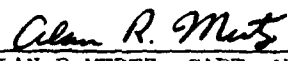ELECTE
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Project Engineer
Microwave Techniques &
 Applications Gp

ALAN R MERTZ, CAPT, USAF
Chief, Microwave Techniques &
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Avionics Laboratory

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GaAs FET device modeling
Full two-dimensional simulation
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This technical report contains a description of a quasi-two-dimensional model for GaAs FET operation. The model is based on modified expressions for the carrier continuity and Poisson equations in the conducting channel of an FET. The model is compared to full two-dimensional results to determine its accuracy. It is then used to study a variety of operating conditions. The effect of various material and device parameters are also discussed.

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## FOREWORD

This report describes the investigation of GaAs FET device

modeling and performance at the Electron Physics Laboratory, Department

of Electrical and Computer Engineering, The University of Michigan, Ann

Arbor, Michigan.  The work was sponsored by the Air Force Systems Command,

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# SECTION 1

## INTRODUCTION

During the past decade the field-effect transistor has become the single most important microwave solid-state device. It is used in small- and large-signal amplifiers, low-noise amplifiers, oscillators, mixers, and a variety of control applications. The FET has been the subject of numerous papers, leading to a better understanding of its operation and potential. Early FET papers were analytic approximations which neglected the effect of space charge in the channel. With faster computers and better numerical methods, full solutions of the two-dimensional carrier transport and Poisson's equations became possible. Results from these finite-difference and finite-element solutions increased our understanding of the device. However, the microwave FET structure poses a basic problem for the device modeler. An X-band FET has a typical doping density of $10^{17}/cm^3$, with higher doping for higher frequency operation. The characteristic length in a semiconductor material is the debye length which is given by[1]

$$L_d = \left[\frac{2kT\varepsilon}{q^2 N_d}\right]^{1/2} , \tag{1}$$

where  k = the Boltzmann constant,

   T = the temperature,

   $\varepsilon$ = the dielectric constant,

   q = the electronic charge,

   $N_d$ = the material doping

1

and the characteristic time is the dielectric relaxation time which is given by

$$\tau = \frac{\varepsilon}{q} \frac{1}{\mu N_d} ,$$ (2)

where $\mu$ = the low field mobility.

For $N_d$ of $10^{17}/cm^3$, the debye length is approximately 0.02 $\mu m$ and the dielectric relaxation time is approximately 0.01 ps. The problem with dc modeling in    two dimensions is constrained by the small mesh size and the resulting huge number of calculations required to get a solution. The RF or switching problem means doing a solution approximately 100 times per ps. Of course, though various approximations and clever programming, these problems can be overcome to some extent.

The approach used in this report is a combination of the analytic and the full simulation. The Poisson and electron transport equations, altered to account for the two-dimensional nature of the problem, are solved in one dimension. Several analytic expressions are used to determine the geometry of the channel. These approximations give a set of equations that can be solved rapidly. At the same time most of the two-dimensional device physics remains.

The approximations used in the FET model and the resulting equations are given in Section 2. The model is used to describe FET operation and to compare it with a full two-dimensional simulation in Section 3. Additional studies of GaAs FETs with varying velocity-field and diffusion-field characteristics are given in Section 4, where the effect of gate length is also studied. A summary of the major results is given in Section 5.

# SECTION 2

## MODEL DESCRIPTION

The purpose of this work is to devise a simplified but realistic model for the study of field-effect transistors. There are a variety of approaches to FET modeling. Shockley's[2] original paper used the gradual channel approximation and the approximation of zero channel space charge. This type of analytic model was also used by Pucel et al.,[3] Shur and Eastman,[4] and Dawson and Frey[5] to further study the FET. These models all neglect space charge and other physical effects within the conducting channel. At the other extreme of complexity is the full two-dimensional solution of the carrier transport and Poisson's equations.[6-10] The model developed here is a compromise between the two types. The hope is to have a model that is simple (i.e., low cost) enough to run a variety of cases and still complex enough to provide a further understanding of the properties and limitations of FETs. The model is intended to provide most of the information which requires full two-dimensional simulation.

The approach used can be discussed with the help of Figure 1. This shows the voltage distribution and gate depletion layer geometry for three FET structures obtained with a two-dimensional simulation. Throughout the conducting channel, the voltage contours are approximately straight and perpendicular to the axis of the device. This is true in the limits of long gates and is the basis of Shockley's[2] gradual channel approximation. However, as can be seen from Figure 1, the approximation of equipotential lines perpendicular to the axis of the
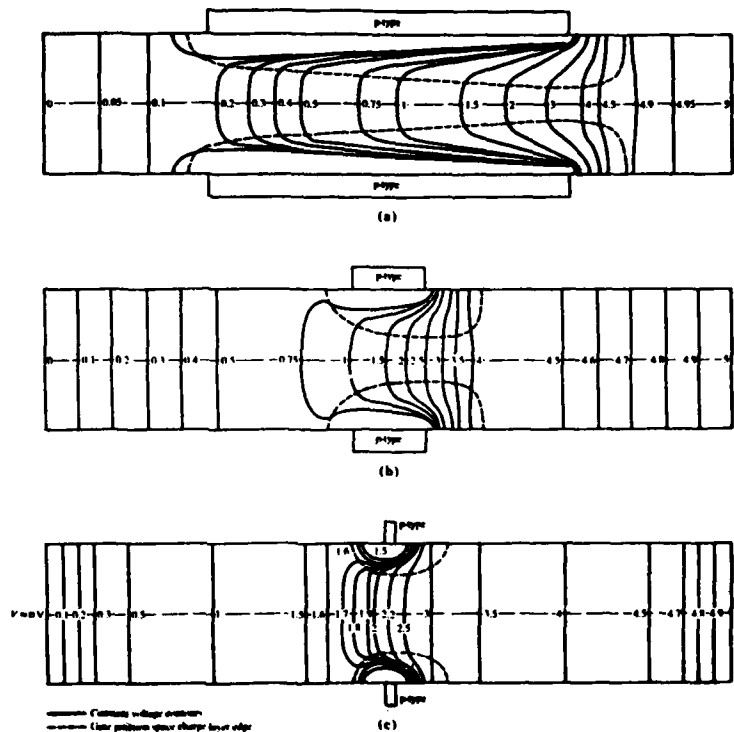
FIG. 1  CALCULATED VOLTAGE DISTRIBUTION WHEN $V_{sg}$ = 0 and

$V_{sd}$ = 5.0 V (FIELD-DEPENDENT ELECTRON MOBILITY).

(a) $2W_g/W_c$ = 5.0, (b) $2W_g/W_c$ = 1.0, (c) $2W_g/W_c$ = 0.143.

(KENNEDY AND O'BRIEN[6])

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device is also reasonable for very short gate devices. This approximation is equivalent to assuming that there is no vertical electric field in the channel. With the additional assumption of an abrupt transition between the conducting channel and the depletion layer a set of differential equations can be written to describe the channel.

Poisson's equation and the electron continuity equation for the channel can be written using the geometry and notation of Figure 2a. The electric field, voltage, electron concentration, and channel geometry factor B are functions of position $x$ along the channel. The velocity and diffusion are functions of position through the velocity-electric field and diffusion-electric field curves for the device material. $B(x)$, the channel geometry factor, is normalized to the height of the channel a. A small volume element of length $\Delta x$ and unit height is shown in Figure 2b. If it is assumed that there is (a) no current flow at the bottom (this is the channel-substrate interface), (b) no current flow at the sloping top (this is the channel-depletion layer interface), (c) an average electron concentration within the element of $N_I$ and (d) an average electric field on the right and left sides of $E_{I+1}$ and $E_I$, then Poisson's two-dimensional equation

$$\nabla \cdot \vec{E} = -\frac{Q}{\varepsilon}(N - N_d) \tag{3}$$

can be written as

$$B_I E_I - B_{I+1} E_{I+1} = -\frac{Q}{\varepsilon}(N_I - N_d)\Delta x \frac{B_I + B_{I+1}}{2} . \tag{4}$$

For small $\Delta x$ this is approximately
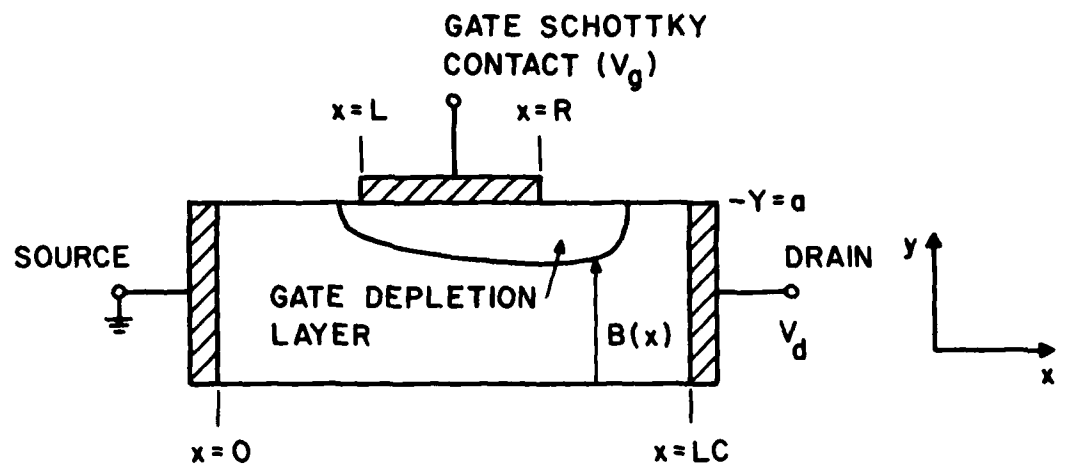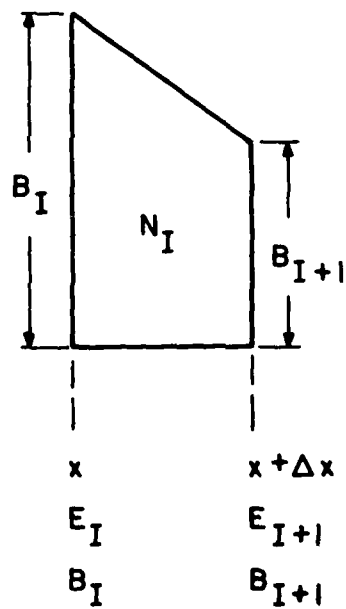
FIG. 2 (a) FET GEOMETRY AND NOTATION. (b) VOLUME ELEMENT
GEOMETRY AND NOTATION.

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$$\partial(BE)/\partial x = -\frac{Q}{\varepsilon}(N - N_d)B \quad . \tag{5}$$

Similarly, the electron continuity equation becomes

$$B_I J_I - B_{I+1} J_{I+1} = \frac{\Delta N_I}{\Delta T} \frac{\Delta x B_{I+1} + B_I}{2} \tag{6}$$

or

$$\frac{\partial(BJ)}{\partial x} = \frac{\partial(BN)}{\partial t} \quad , \tag{7}$$

where    $J$ = the electron current density

$$= Qv[E(x)]N(x) - QD[E(x)][dN(x)/dx] \quad , \tag{8}$$

$v[E(x)]$ = the velocity and

$D[E(x)]$ = the diffusion coefficient.

The voltage along the channel is

$$V(x) = -\int_{x=o}^{x} E(x') \, dx' \quad . \tag{9}$$

The channel opening $B(x)$ depends on the voltage along the channel.

The current in the channel depends on the material parameters used. The form of the velocity-field and diffusion-field curves are from Bauhahn.[11] The curves are

$$v(E) = \frac{[\mu_o E + v_{sat}(E/E_v)^4]}{1 + (E/E_v)^4} \tag{10}$$

and

$$D(E) = \frac{(kT/q)\mu_o + D_{sat}(E/E_d)^4}{1 + (E/E_d)^4} \quad , \tag{11}$$

where    $\mu_o$ = the low field mobility,

$v_{sat}$ = the saturated velocity,

$E_v$ = the peak field for velocity,

$D_{sat}$ = the high field diffusion coefficient and

$E_d$ = the corner field for diffusion.

Before Equations 5 and 7 can be solved, an equation relating the voltage along the channel and the depletion-layer width or channel geometry factor B is needed. The voltage drop across the depletion layer is related to its width by

$$V_d = (q/2\epsilon)N_d\omega^2 \quad . \tag{12}$$

One possible approximation is to assume that the equipotential lines within the depletion layer are parallel to the gate of the Schottky barrier, as shown in Figure 3. This approximation is typically used in analytic FET models and is correct in the limit of long gates. With this approximation, the voltage across the depletion layer depends on the voltage difference between the gate and the channel. Equation 12 can be used to find the depletion-layer width and the resulting channel geometry factor $B(x)$. This approximation is referred to as the parallel-potential approximation.

The problem with the parallel-potential approximation is that it always overestimates the width of the gate depletion layer and underestimates the channel geometry factor $B(x)$. This can be shown by referring to Figure 1. Although the constant voltage lines on the conducting channel are approximately parallel, they bunch together in the depletion layer near the drain end of the gate depletion layer. Thus a sloping straight-line approximation can be made for the equipotential lines within the depletion layer. If the voltage along the top of the channel outside the depletion layer is known

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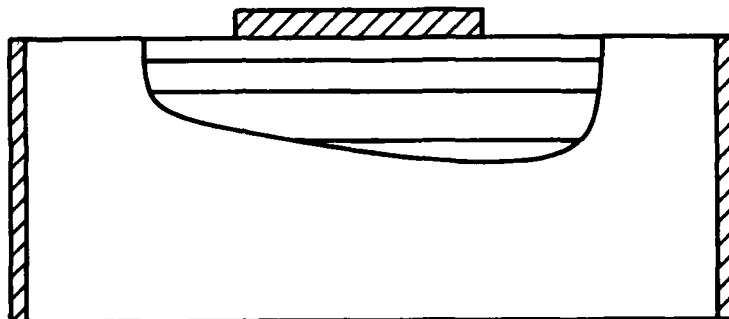
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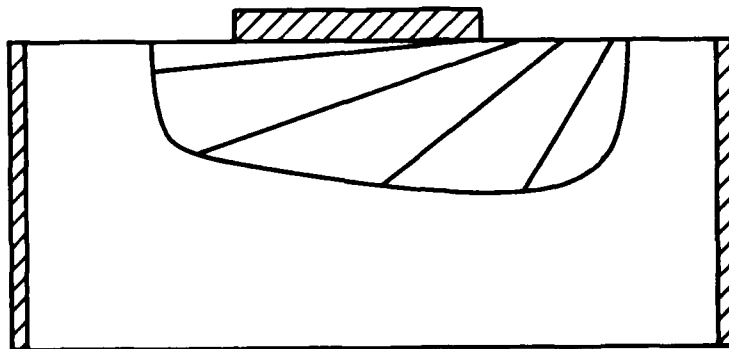


(b)

FIG. 3  POSSIBLE DEPLETION-LAYER POTENTIAL LINES.
(a) PARALLEL-EQUIPOTENTIAL LINES AND (b)
SLOPING-EQUIPOTENTIAL LINES.

(from Equation 9), Equation 12 can be used to find the corresponding depletion-layer width between the gate and the drain. Although the geometry of the equipotential lines is a two-dimensional problem within the depletion layer, there is only an x-direction electric field along the top surface of the channel. The voltage along the surface is

$$V'(x) = \frac{V_g + \Delta V_{dep} + (Q/2\varepsilon)N_d\Delta x^2}{\Delta x} x' - \frac{Q}{2\varepsilon} N_d x'^2 \quad , \quad (13)$$

where   $V_g$ = the gate voltage (applied gate voltage plus built-in potential),

   $x'$ = the distance along the surface from the right edge of the gate,

   $\Delta x$ = the width of the depletion layer along the top and

   $\Delta V_{dep}$ = the voltage drop across the depletion layer.

The straight-line approximation can now be drawn from position x at the top of the conducting channel to x' within the depletion layer. The geometry is shown in Figure 4. The angle θ in Figure 4 is related to the width of the depletion layer at x by

$$\theta = \tan^{-1} \frac{\omega'(x)}{x_R + x' - x} \quad , \quad (14)$$

where $\omega'(x)$ is defined geometrically in Figure 4. If it is assumed that the electric field lines are semicircles with radius r centered at x', then the length of the arc is related to the voltage between the gate and the channel by Equation 12. The arc length ω and radius r are related by

$$r\theta = \omega \quad\quad (15)$$

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FIG. 4 GEOMETRY FOR SLOPING–POTENTIAL APPROXIMATION.
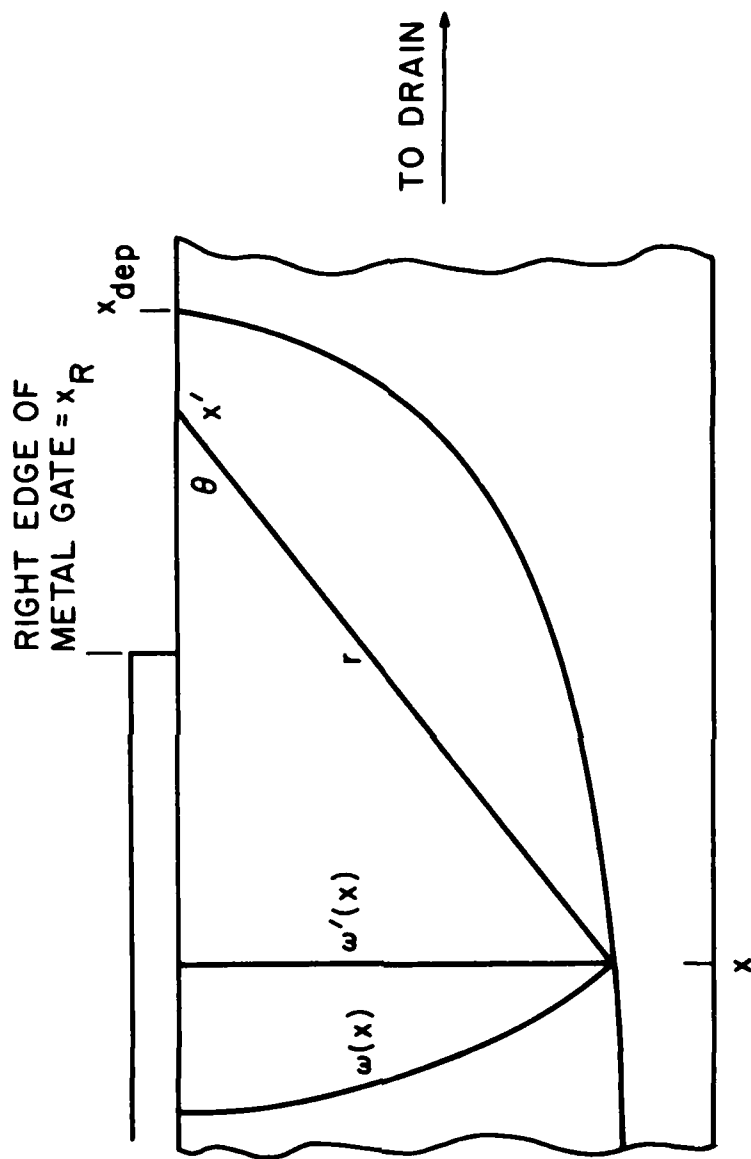
$\Delta x_{dep} = x_{dep} - x_R$

$\Delta V_{dep} = V(x_{dep}) - V(x_R)$

and the depletion-layer width at $x$ is

$$\omega'(x) = r \sin \theta \quad . \tag{16}$$

Using Equations 15 and 16 yields the depletion-layer width:

$$\omega'(x) = \omega(x) \sin \theta/\theta \quad . \tag{17}$$

This set of equations can be used to find the electron and field distribution along the channel. The program starts from an initial guess, typically with $n(x)$ equal to the background doping and $B(x) = 1$. For a given gate and drain voltage, Equation 5 can be solved to find $E(x)$. Then Equation 9 can be integrated to find the voltage along the channel. The channel geometry can be found using the voltage. When the geometry and electric field are known, Equation 7 can be used to update the electron distribution. This process is continued until a convergent solution is obtained.

Two versions of this program have been programmed; one in the HPL programming language running on an HP 9825 calculator and one in FORTRAN running on an AMDAHL computer. The HPL version requires several minutes to find a converged solution. A complete set of solutions, over a range of drain-source and gate-source voltages, requires less than a second of AMDAHL cpu time.

# SECTION 3

## COMPARISON OF THE SIMPLE MODEL AND THE TWO-DIMENSIONAL RESULTS

Introduction. The operation of field-effect transistors is
described in this section. A general discussion of FET operation is
given first so that the factors effecting the device performance
can be better understood. Then the results of the present work are
compared with two-dimensional results. This will show the approxi-
mations and accuracy of the present model.

FET Operation. The operation of FETs can be explained using
Equations 5 and 7. If the electron concentration in the channel is
equal to the channel doping and, in the case of dc operation, the
equations become

$$B(x)E(x) = \text{constant} \tag{18}$$

and

$$B(x)J(x) = J_{dc} \quad , \tag{19}$$

the constant in Equation 18 is set by the applied drain-source voltage.
The current density is

$$J(x) = qN_d\mu_o(x)E(x) \quad . \tag{20}$$

The current density, field, and geometry are shown in Figure 5 for
the simple approximation of a rectangular depletion layer. The
voltage across the device is

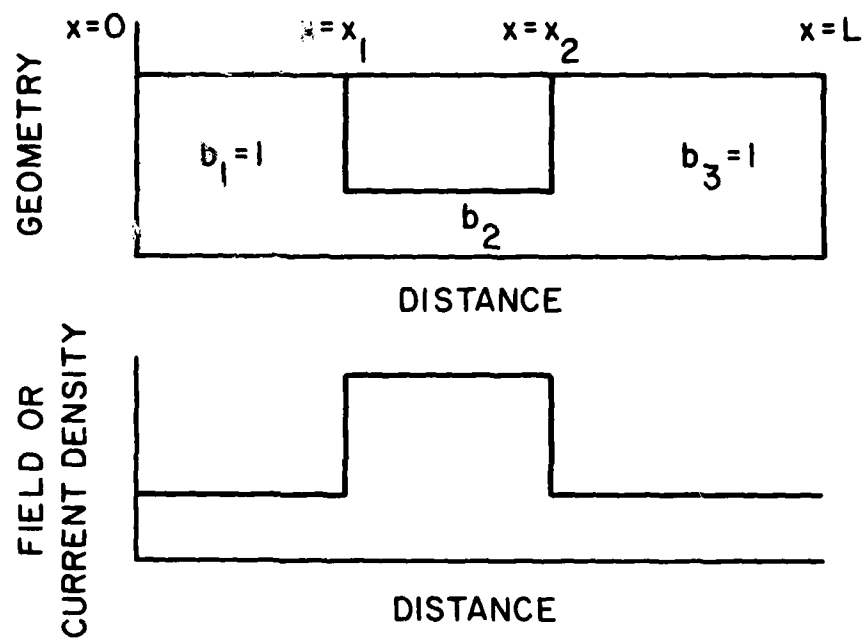$$V = E_1[x_1 + (L - x_2) + (x_2 - x_1/b_2)] \quad . \tag{21}$$

FIG. 5   CURRENT AND ELECTRIC FIELD FOR SIMPLE

RECTANGULAR DEPLETION LAYER.

The current is related to the field by Equation 20. If the width of the depletion layer is related to the voltage at the source edge of the depletion layer by

$$(1 - b_2) = K\sqrt{V(x_1)} , \qquad (22)$$

then the current-voltage characteristic is as shown in Figure 6. As the channel depletion layer gets wider with increasing drain to source voltage, a larger fraction of the total voltage drop occurs under the depletion layer and the current saturates. The channel under the depletion layer does not pinch off in this approximation. In fact, B pinchoff or $b_2 \to 0$ would imply an infinite potential drop between drain and source. The limitation of the zero space-charge approximation can be seen by referring to Equation 20. There will be current continuity in the channel as long as the current is linearly related to the field or the mobility is constant. In Si devices the mobility decreases with increasing electric field as follows:

$$\mu(E) = \mu_o \exp\left(-\mu_o E/v_{sat}\right) . \qquad (23)$$

At low fields the mobility is approximately constant and there is no space charge in the channel. As the drain-source voltage and field in the channel increase, the mobility decreases and there is a build up of electrons to satisfy the current flow. These extra electrons further increase the potential drop in the channel by further increasing the magnitude of the electric field in the channel. Beyond the end of the depletion layer toward the drain end of the channel the channel width increases. Since the field and total current must be continuous through this region, the electron concentration must drop
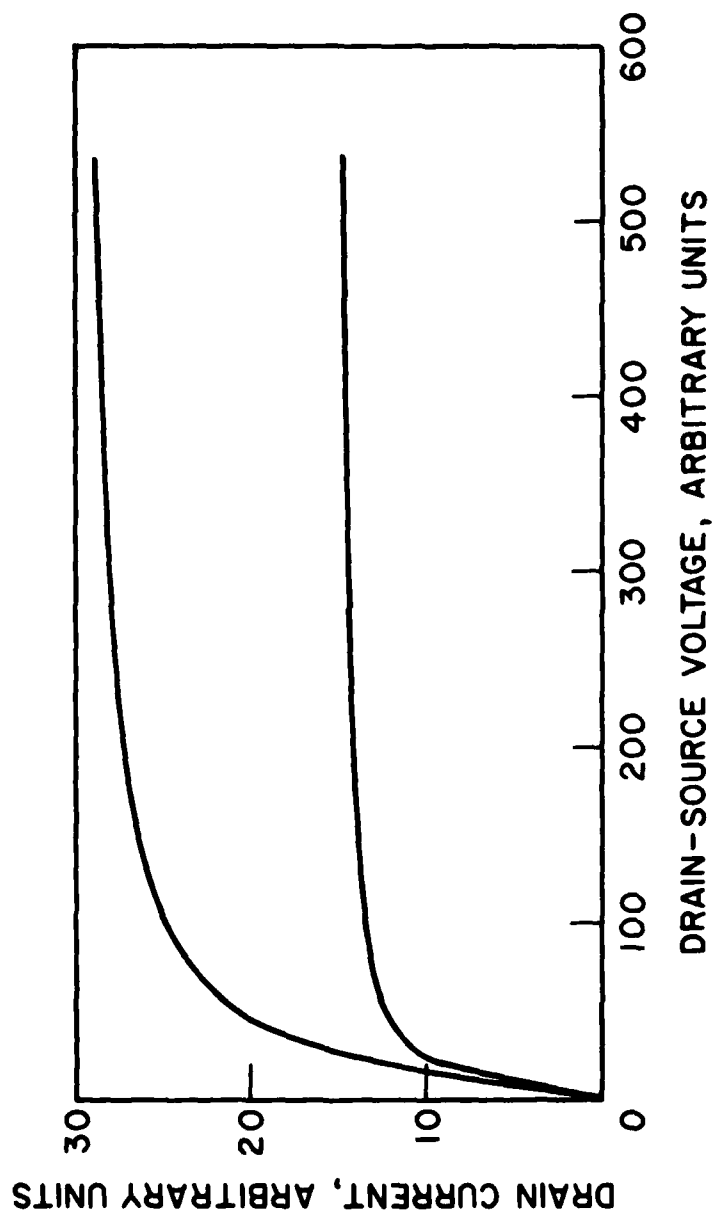
FIG. 6  DRAIN-CURRENT VS. DRAIN-SOURCE VOLTAGE FOR ZERO SPACE-CHARGE APPROXIMATION.

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below the background.  This depletion region becomes the second half
of the channel charge dipole.  The depletion layer lowers the magni-
tude of the channel electric field which increases the mobility and
reduces the amount of depletion further along the channel.

The operation of a GaAs transistor is slightly different.  For
GaAs, the mobility is approximately constant up to the peak velocity
field.  Beyond the peak velocity, the velocity decreases with in-
creasing field.  For low fields in GaAs FETs the amount of depletion
or accumulation is low, typically less than $10^{-4}$ times the background
charge.  At a field slightly above the peak velocity field the electron
velocity starts to decrease.  This, in turn, results in an accumulation
formation at this point as the higher velocity electrons from the
source end of the channel arrive at the high field point and slow down.
This further increases the field.  The field at equilibrium outside the
dipole must be low enough to prevent further buildup of charge.  This
results in a lowering of the drain current after the dipole has formed.
The field under the gate depletion layer on the source end must be
lower than the peak velocity field to prevent a second dipole from
forming.   By  changing  the drain-source voltage, the magnitude of the
field under the entire gate can be pulled above the peak field.  How-
ever, the electrons will still accumulate at the highest field or
lowest velocity point reforming a larger dipole at this point and again
reducing the field in the channel below the peak field.  Beyond the
narrowest part of the channel the magnitude of the field starts to
decrease.  This, in turn, increases the electron velocity and reduces
the electron concentration, forming a depletion layer.  This further

reduces the field below the peak field, moving the electron concentration back to the doping level near the drain contact.

Comparison with Two-Dimensional GaAs Results. The recent work of Laux[10] is the first two-dimensional simulation of a GaAs FET with reasonable doping levels. The device modeled has a 1-$\mu$m long channel, a 0.25-$\mu$m long gate, and a 0.25-$\mu$m high channel. The velocity-field curve used is Equation 10 with $\mu_o$ = 5000 cm$^2$/V-s, $v_{sat}$ = 1 x 10$^7$ cm/s and $E_v$ = 2690 V/cm. The diffusion-field curve used is Equation 11 with $D_{sat}$ = 20 cm$^2$/s and $E_d$ = 1.33 $E_v$. Figure 7 shows the electron concentration and potential along the channel for the two-dimensional model. The break in the 1.5-V electron concentration is numerical. Figures 8 through 10 show similar results for the present model. Figures 8 through 10 have the 0.2-, 0.4- and 1.5-V information for the simple-parallel and sloping-potential depletion-layer approximations. The geometry-distance plots in the three figures show the two approximations. The sloping-potential depletion layer is always smaller than the simple-parallel model. It is also sloping upward where the simple one is narrowest. Figure 8 with a 0.2-V drain-source bias shows the FET at its peak current point, with the velocity at the peak velocity of 1.2 x 10$^7$ cm/s. The velocity at the drain and source contacts is approximately the same for the two depletion-layer models. For all the GaAs devices modeled, the choice of the depletion-layer approximation changed the distribution of electrons and field in the channel but did not greatly change the terminal drain current. Because the field in the channel for the 0.2-V case is below the peak velocity field, the electron concentration is almost equal to the background doping. For all the cases modeled, the simple model slightly underestimates the
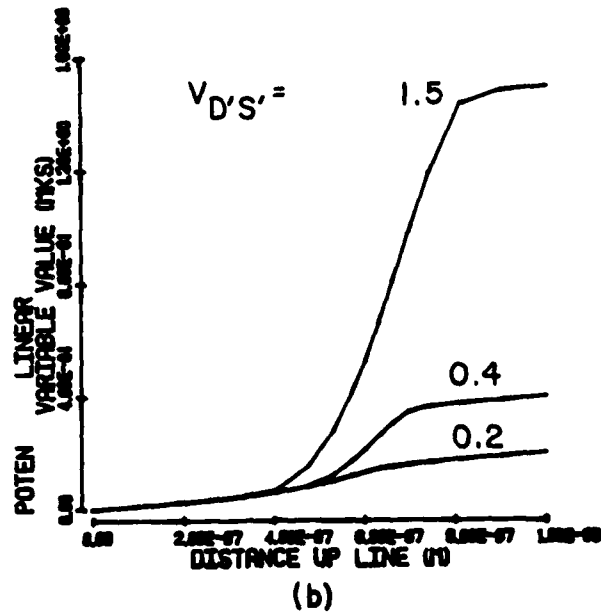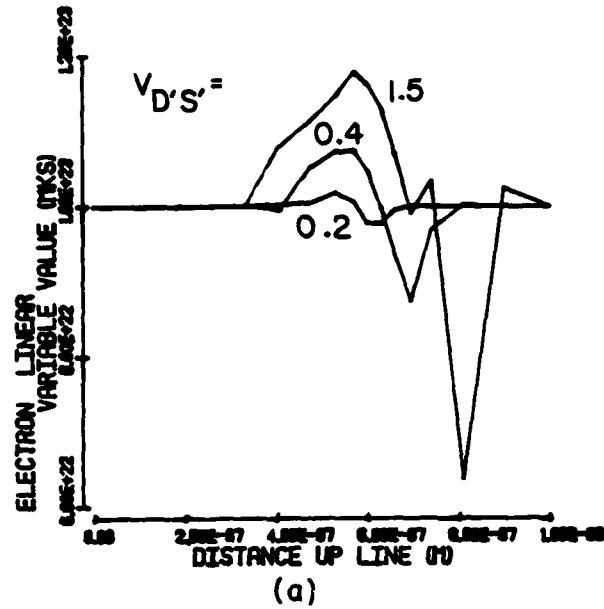
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FIG. 7 (a) ELECTRON CONCENTRATION $(m^{-3})$ AND (b) POTENTIAL (V) FROM

S' TO D' ALONG THE $y = 0$ SYMMETRY LINE FOR THE UNIFORMLY DOPED

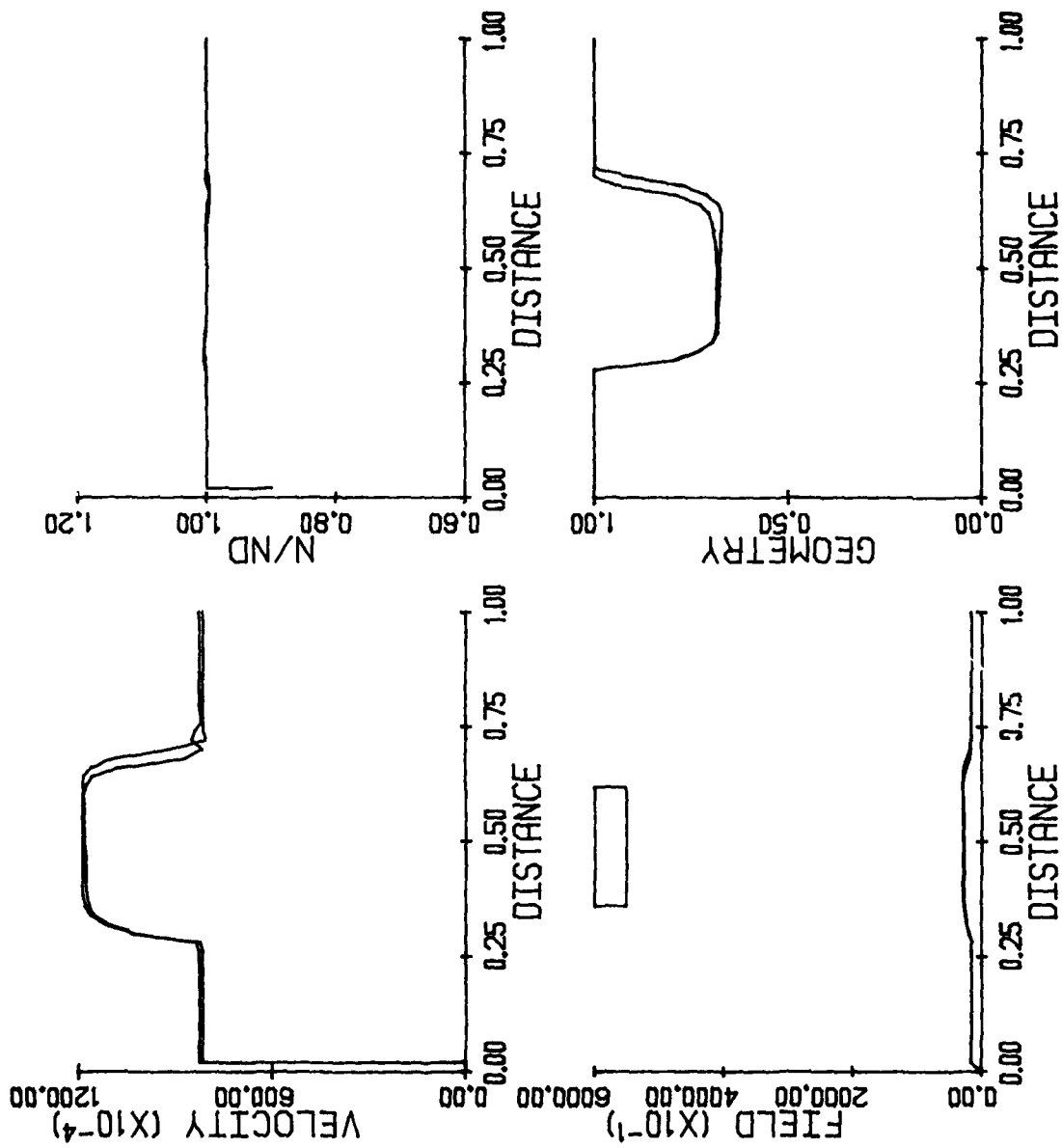INTRINSIC MESFET. $V_{G'S'} = 0$ V; $V_{D'S'} = 0.2$, 0.4 AND 1.5 V.

FIG. 8  0.2-V COMPARISON FOR THE SIMPLE-PARALLEL AND SLOPING-POTENTIAL DEPLETION-LAYER APPROXIMATIONS.
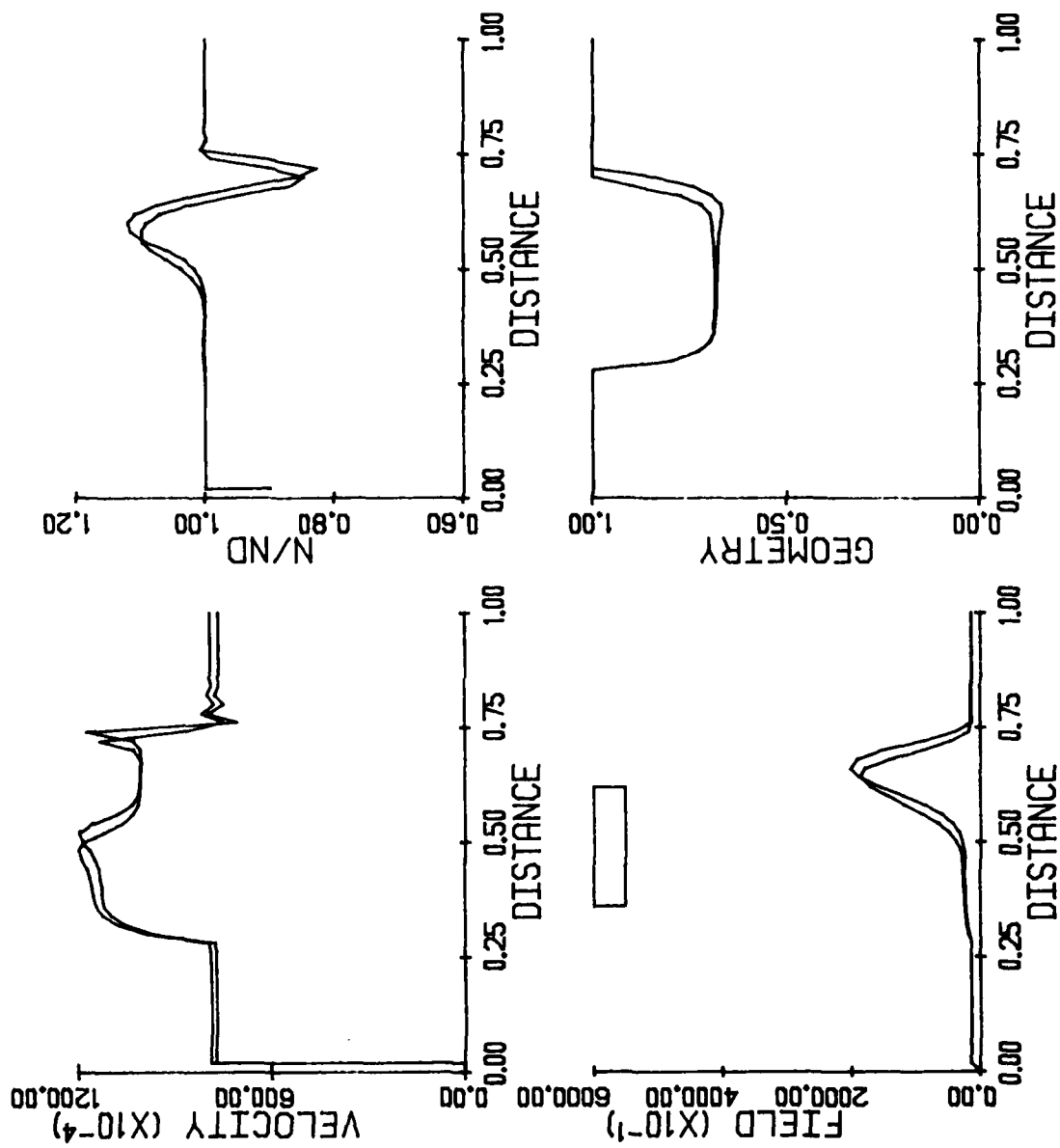
-20-

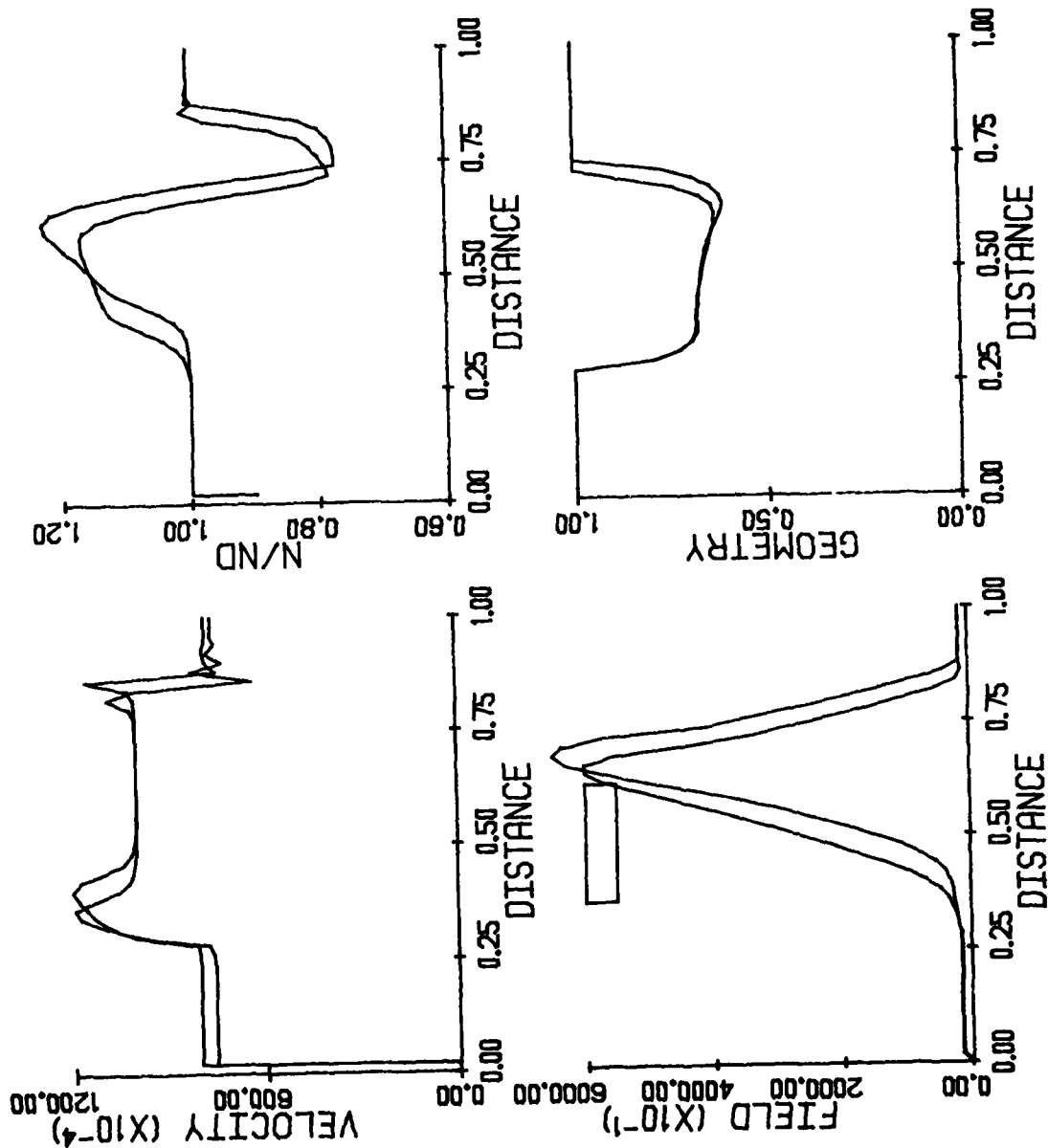FIG. 9  0.4-V COMPARISON FOR THE SIMPLE-PARALLEL AND SLOPING-POTENTIAL DEPLETION-LAYER APPROXIMATIONS.

FIG. 10  1.5-V COMPARISON FOR THE SIMPLE-PARALLEL AND SLOPING-POTENTIAL DEPLETION-LAYER APPROXIMATIONS.

field in the channel under the gate and overestimates the field in the rest of the channel. This means that a better approximation is needed for the depletion-layer geometry.

Figure 9 shows the results for the 0.4-V drain-source bias condition. Here a charge dipole has formed in the channel. The peak electron concentration is 1.1 times the background doping and the minimum concentration is 0.7 times the background concentration. There is good agreement between the simple-parallel and the two-dimensional results. The peak electric field is approximately 20 kV/cm and occurs beyond the drain end of the metal gate as shown in the field-distance plot of the figure. The excess charge region extends under approximately two thirds of the gate.

Figure 10 shows the results for the 1.5-V comparison. This condition shows the effect of the two depletion-layer approximations on the electron concentration along the channel. The simple depletion-layer approximation gives a narrower channel. This results in a high electron concentration that is more peaked. The sloping-potential approximation gives less change in channel geometry with position. This spreads out the excess electron peak and reduces its maximum value. This is closer to the two-dimensional result of Figure 7. The sloping potential also lowers the peak electric field. The peak field has moved closer to the drain contact under this bias condition. The field is above the peak-velocity field through the entire gate.

Figure 11 shows the potential vs. distance results for the six cases. The sloping potential depletion layer gives a slower rise in potential and moves the curve to the left. Again, these curves agree well with the two-dimensional results of Figure 7b.
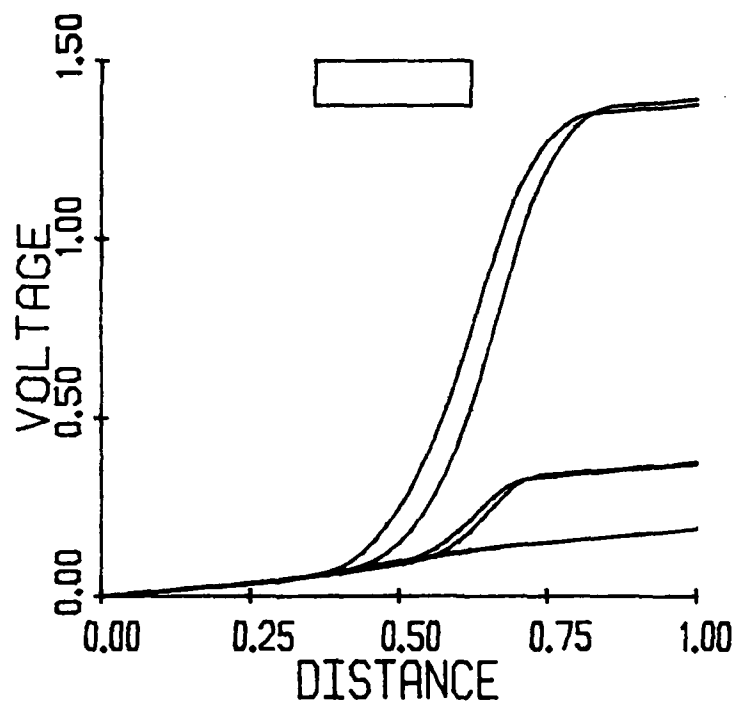
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FIG. 11  POTENTIAL VS. DISTANCE ALONG THE CHANNEL.

The common source output characteristics of the two models are shown in Figures 12 and 13. The simple model drain currents are approximately 25 percent higher than the two-dimensional results. This difference is a result of the high mobility of GaAs. The 600-mA difference between the drain currents at zero gate bias corresponds to an electric field difference of only 300 V/cm at the contacts. This is less than 1 percent of the peak channel field. Further study of the depletion-layer model and the two-dimensional results are needed to resolve this difference. Although the drain currents in the simple model are high, the change with gate bias is approximately correct. The drain current for a 0.5-V drain-source voltage at different gate voltages is shown in Figure 14. Over a gate voltage range from zero to -2 V the slopes of the curves and thus the transconductance are approximately equal. A similar comparison is shown in Figure 15 for a 1.0-V drain-source voltage.

Summary of Comparison. Over the range of data available there is good agreement between the present model and a full two-dimensional simulation. There is very good agreement on the potential and electron distribution. Although the currents in the simple model are high, the electric field in the channel is only off by 300 V/cm. The best approach at this time would be to make further runs with both programs in order to pinpoint the reasons for the differences. However, there are two problems with this. First, the two-dimensional problem has a relatively large mesh spacing. It is not clear that further runs would give much additional information. Second, the two-dimensional program is costly. A current voltage set such as shown in Figure 12 costs hundreds of dollars of computer time. By comparison, the data
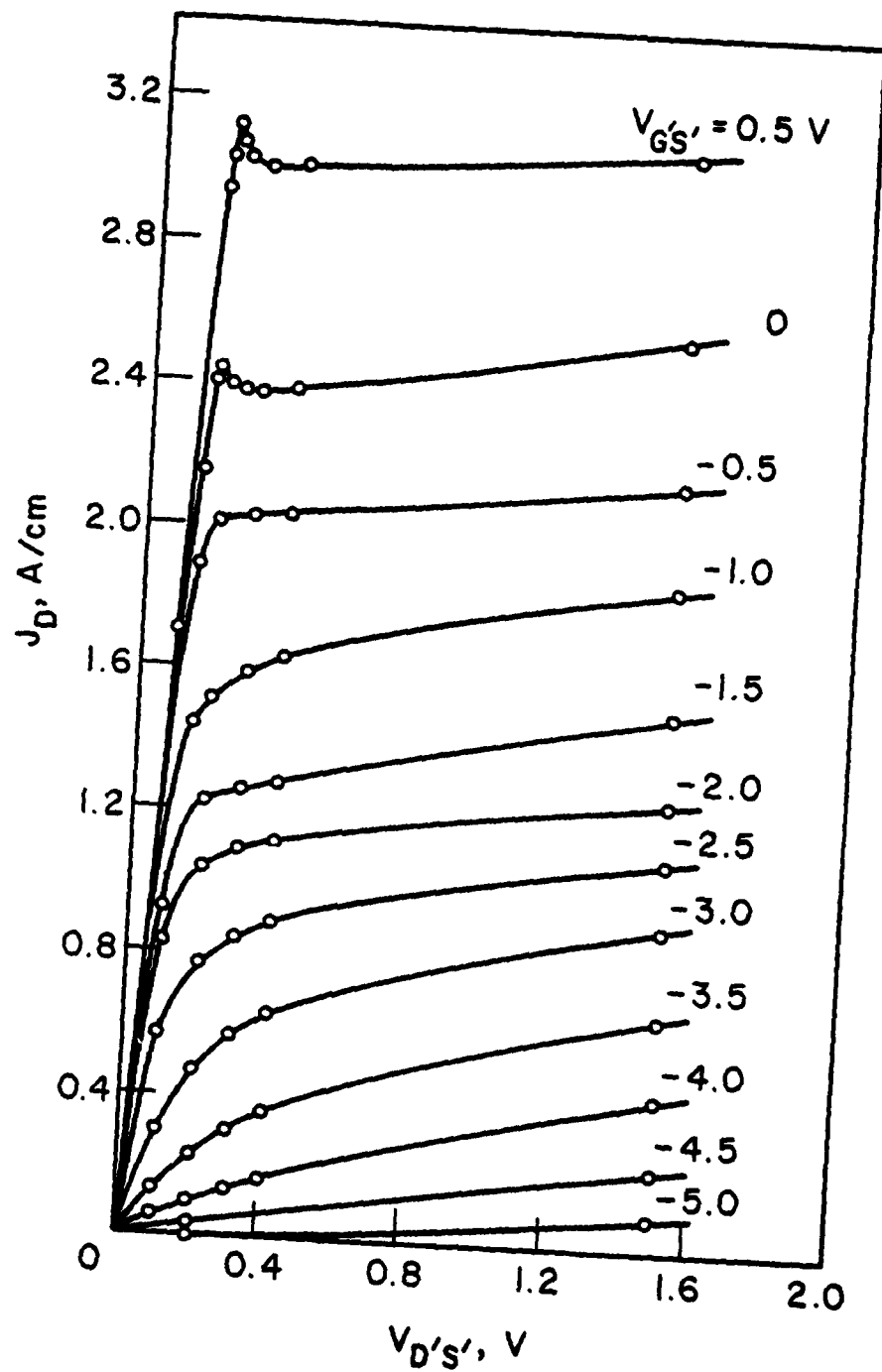
-25-

FIG. 12  COMMON SOURCE OUTPUT CHARACTERISTIC OF A MESFET
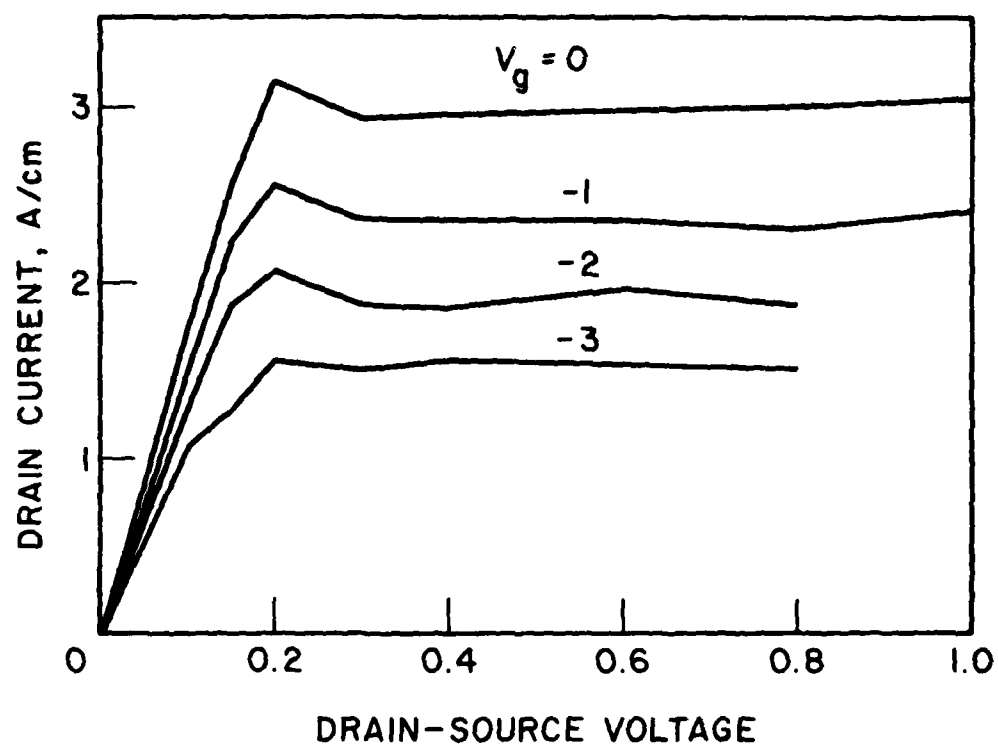
OBTAINED BY TWO-DIMENSIONAL NUMERICAL SIMULATION.

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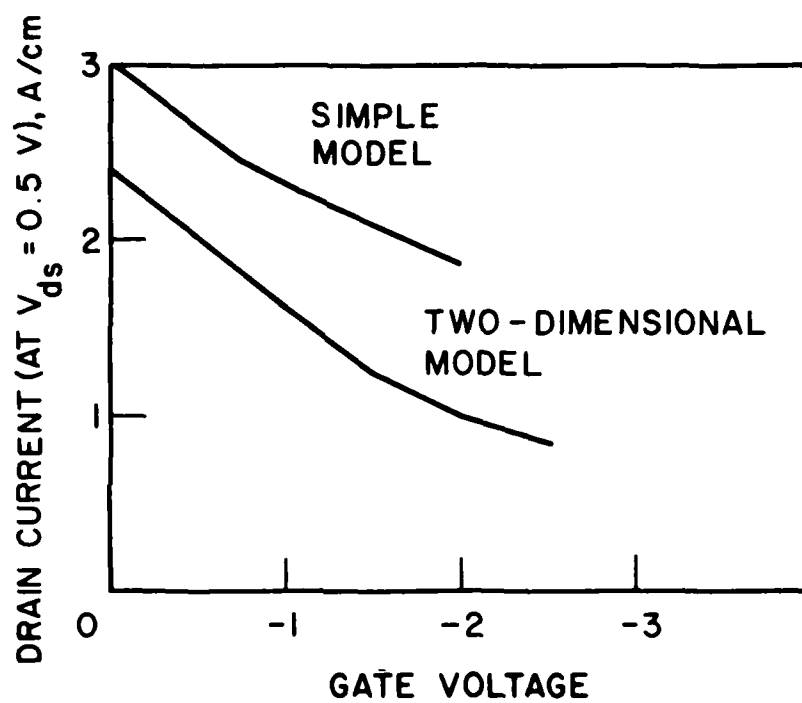FIG. 13  COMMON SOURCE OUTPUT CHARACTERISTIC.

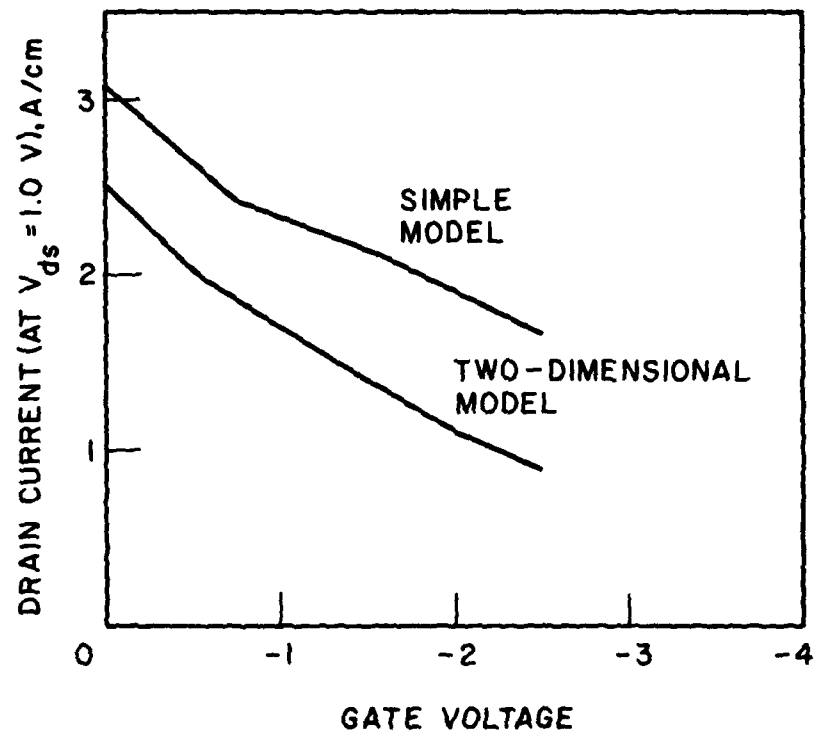FIG. 14   TRANSCONDUCTANCE COMPARISON.   ($V_{ds}$ = 0.5 V)

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FIG. 15 TRANSCONDUCTANCE COMPARISON. $(V_{ds} = 1.0 \text{ V})$

in Figure 13 cost less than $3. It would be better to use the simple model data as input to the full program. Finally, although the currents are high, the transconductance is a more important parameter for ac operation.

## SECTION 4

## EFFECTS OF VARIOUS PARAMETERS ON FET OPERATION

Introduction. The idea behind the study of FETs is to understand better their operation so that their actual performance can be improved. Subject to technical limitations, the device builder has a choice of materials and geometry when building FETs. The material choice, in turn, gives a particular velocity-field and diffusion-field characteristic. In this section a variety of geometries, velocity-field choices, and diffusion-field choices are investigated in order to provide a better understanding of FET operation.

Gate Length Variation. The effect of gate length on FET operation is considered here. The device is 1 μm long with a 0.25-μm high channel doped at $1 \times 10^{17}/cm^3$. The velocity-field and diffusion-field characteristics are given by Equations 10 and 11 with $\mu_o$ = 5000 cm²/V-s, $v_{sat}$ = $10^7$ cm/s, $E_v$ = 3500 V/cm, $E_d$ = 1.33 $E_v$. The resulting characteristics for gate lengths of 0.01, 0.2, 0.3 and 0.5 μm are shown in Figures 16 through 19.     The drain current vs. drain-source voltage at zero gate bias is shown in Figure 20 for the various cases. At channel fields below the peak velocity field there is little space charge and Equations 18 and 19 apply. The current depends on the boundary electric field, so increasing the gate length lowers the current. However, even at a very short gate length of 0.01 μm, the gate depletion layer covers 20 percent of the channel length. Since the integral of the total field along the channel in each case must equal the drain-source voltage, the narrower gate gives a higher field and
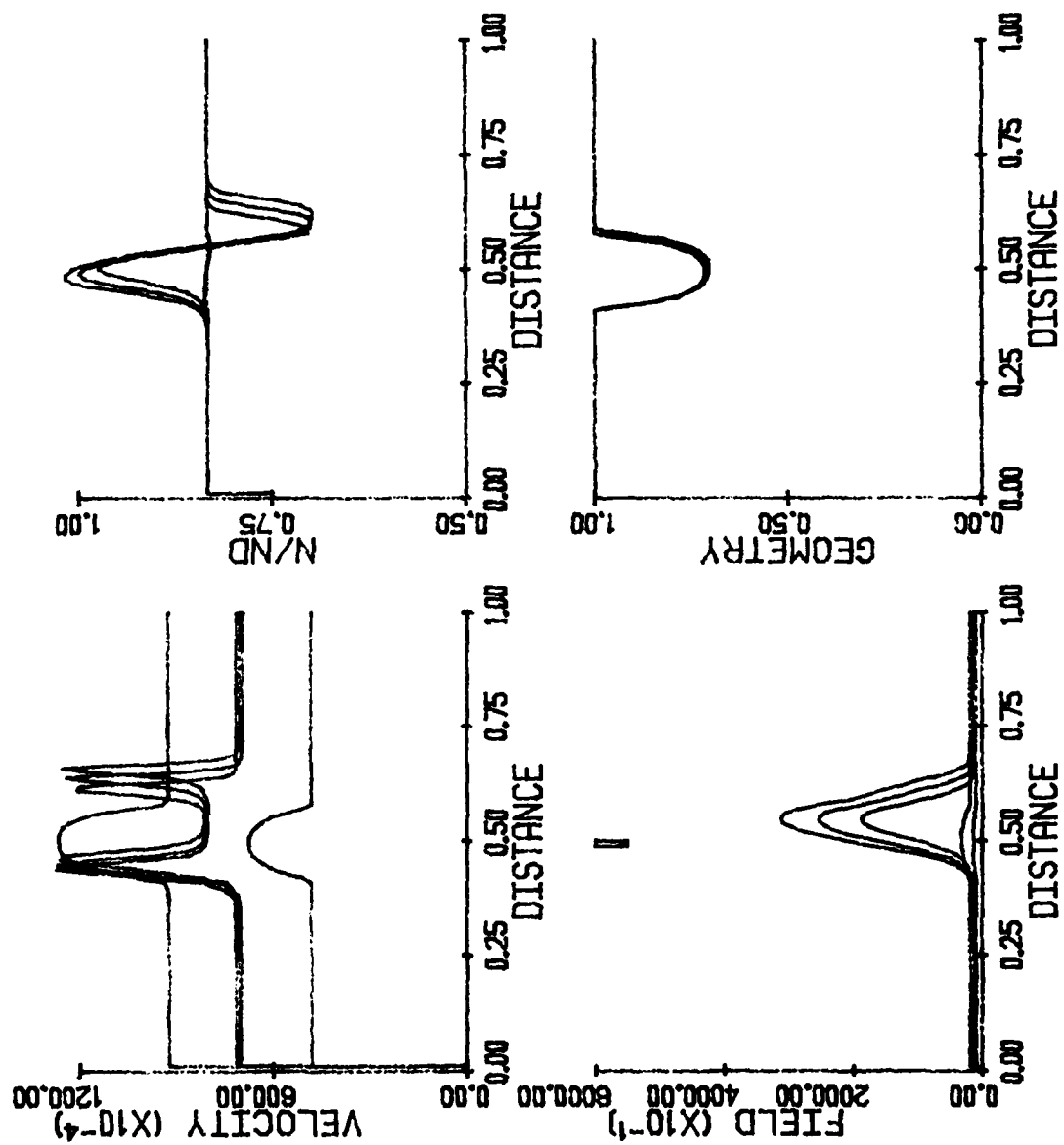
-31-

FIG. 16 CHARACTERISTICS OF 0.01-μm GATE FET.
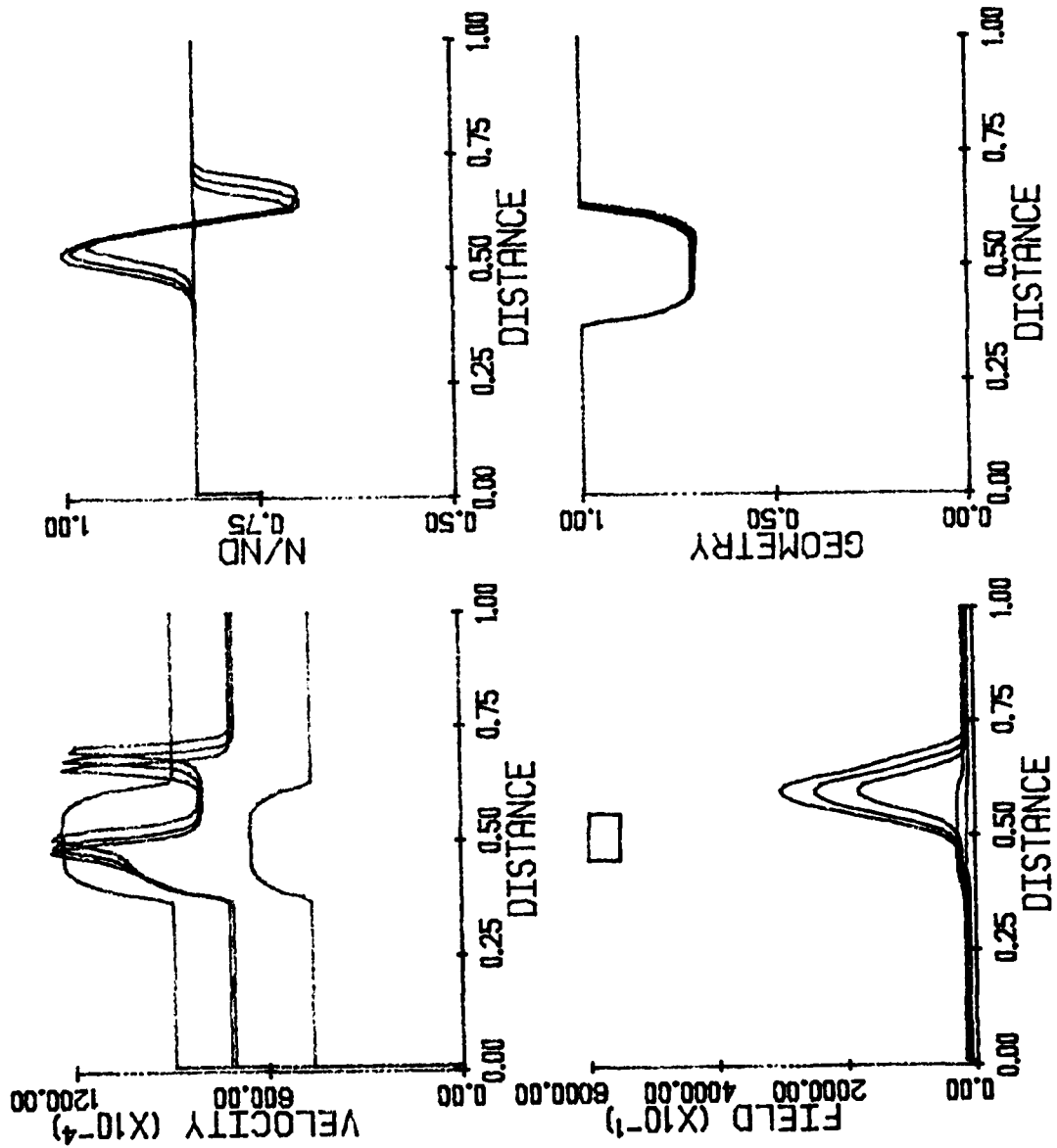
-32-

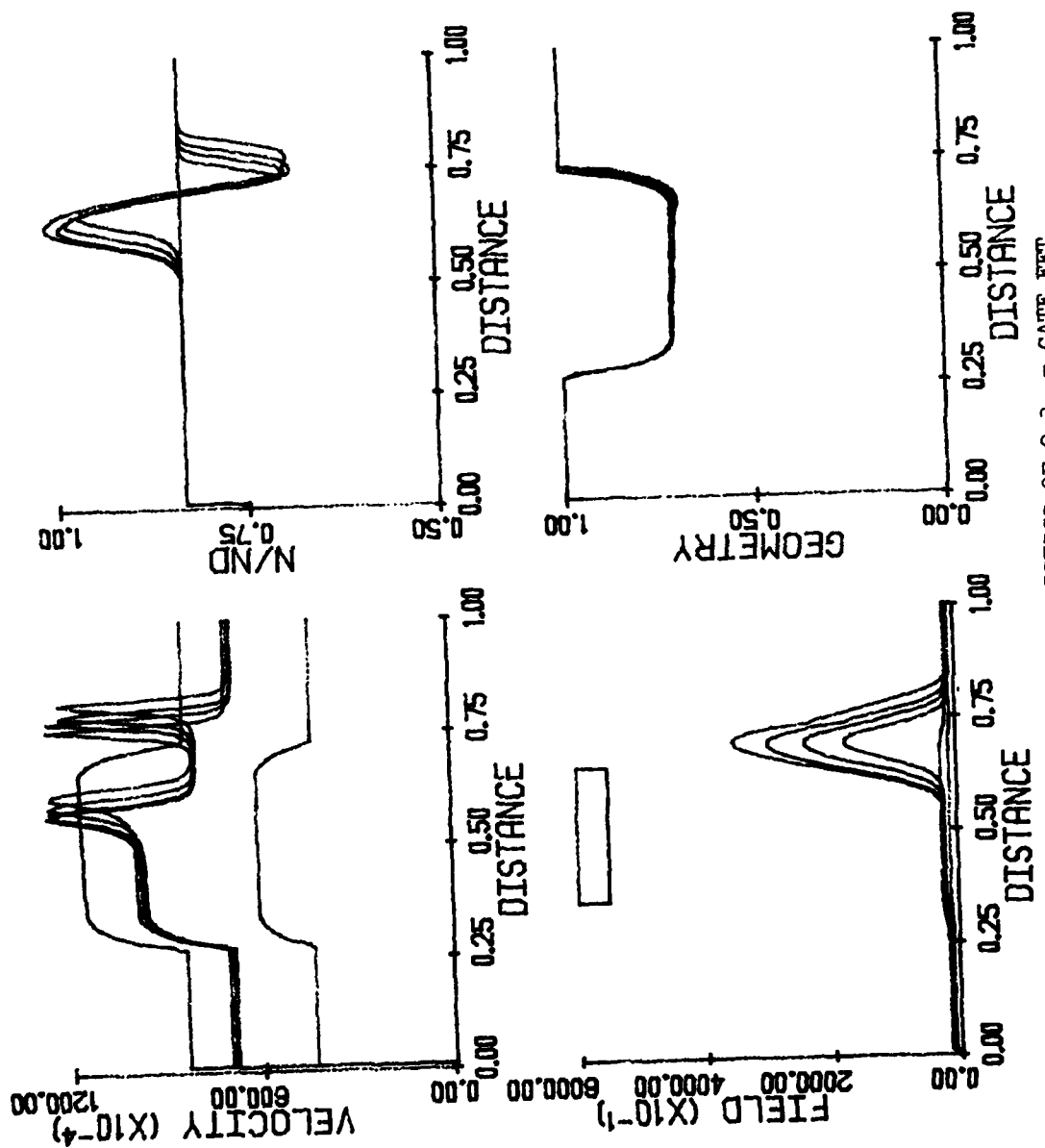FIG. 17  CHARACTERISTICS OF 0.2-μm GATE FET.

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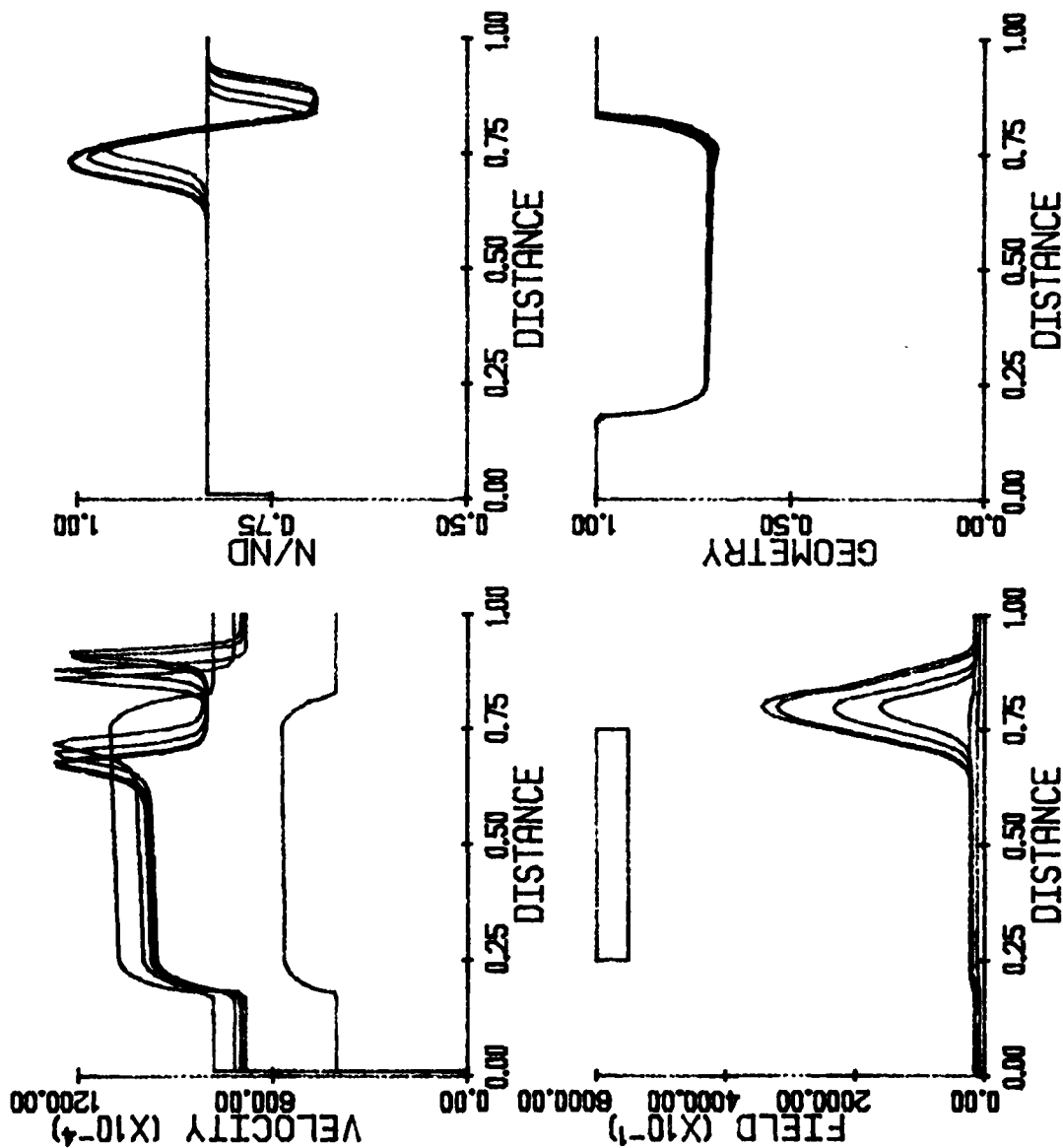FIG. 18 CHARACTERISTICS OF 0.3-μm GATE FET.

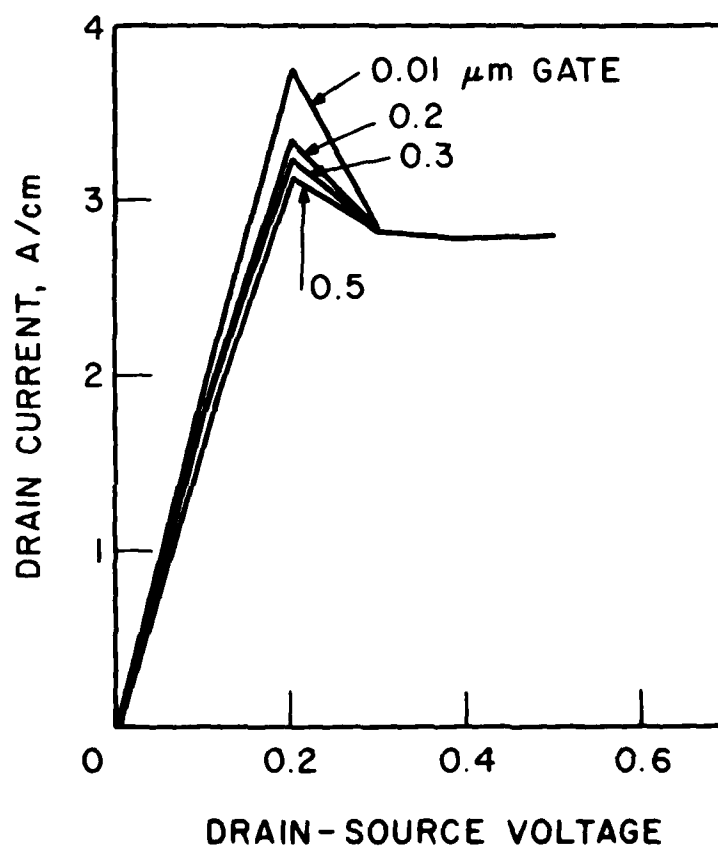FIG. 19  CHARACTERISTICS OF 0.5-μm GATE FET.

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FIG. 20  DRAIN CURRENT VS. DRAIN-SOURCE VOLTAGE WITH

GATE LENGTH AS PARAMETER.

current at the peak current point around a drain-source voltage of 0.2 V.
Increasing the gate length decreases the peak current. Beyond the
peak current point a charge dipole forms for each gate length. After the
charge dipole forms it dominates the current flow in the channel. Ex-
cept for the position along the channel, the dipole in each case is
approximately the same. The peak field in the dipoles for 0.5-V drain-
source voltage varies less than 5 percent for the range of gate lengths
considered. The maximum and minimum charge concentrations vary even less.
Beyond 0.3-V drain-source voltage on Figure 20, the drain current is
approximately the same for each case. Since the current characteris-
tics of FETs with varying gate lengths are the same, the main effect of
varying the gate length is the capacitance of the gate. Changing the
gate length changes the volume of the depletion layer and this changes
the amount of current required to change the layer. However even the
very short gate 0.01-$\mu$m device occupies approximately 20 percent of
the channel length at zero gate bias.

Diffusion-Coefficient Variation. Figures 21 through 25 show a
0.25-$\mu$m gate FET with the same velocity-field characteristic and geometry
as the gate length variation test. The diffusion coefficient vs. field
curve has been multiplied by a factor of 0.5, 1, 5, 10 and 20 in the
figures. Figure 26 shows the resulting drain current vs. drain-source
voltage curve for the various diffusion coefficients. Progressing
through Figures 21 through 25 shows that the effect of increasing the
diffusion coefficient is to reduce the gradient in the electron con-
centration. This lowers the magnitude of the maximum and minimum
electron concentrations, spreads out the charge dipole, and spreads
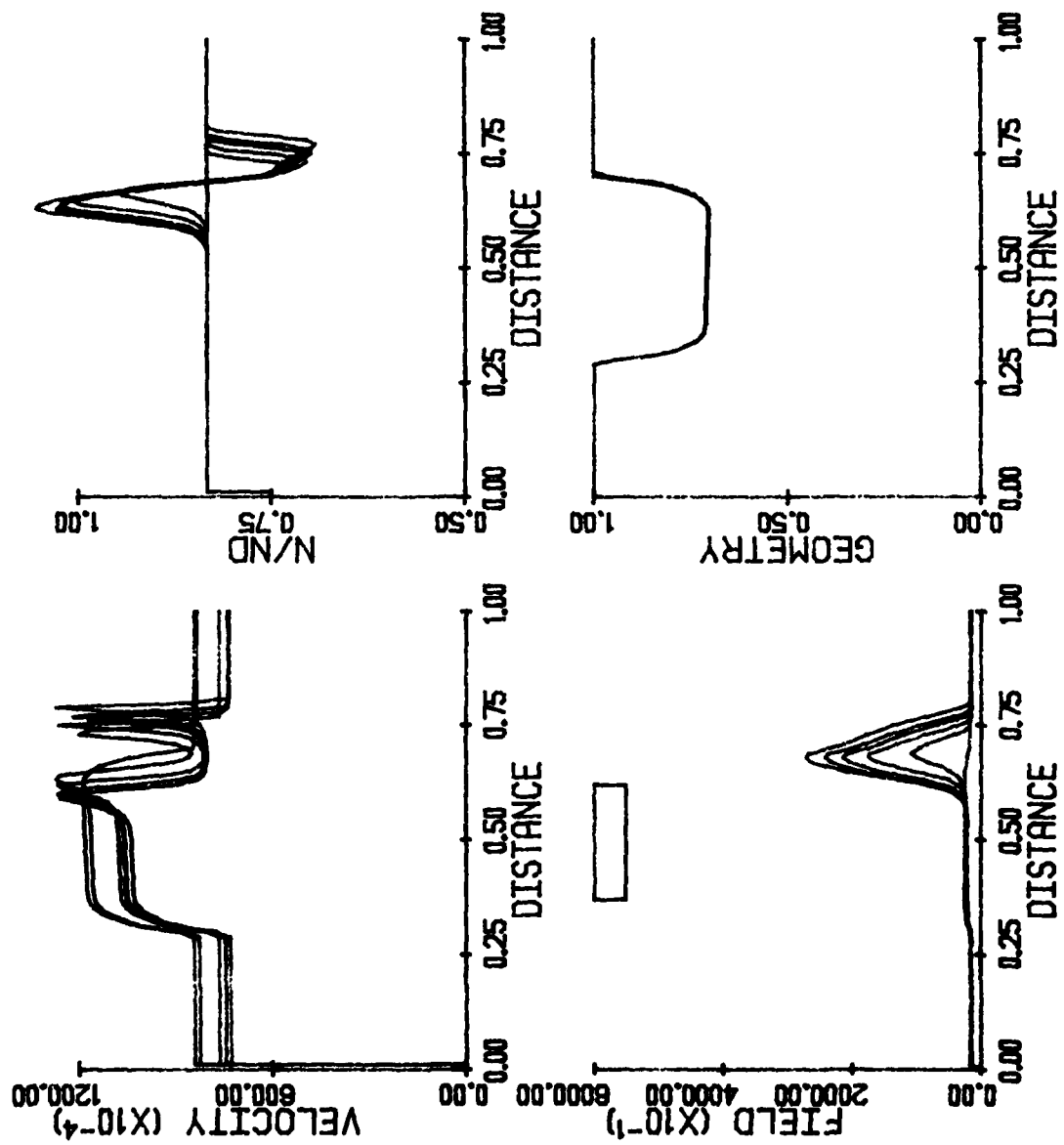out and lowers the electric field. For drain-source voltages lower
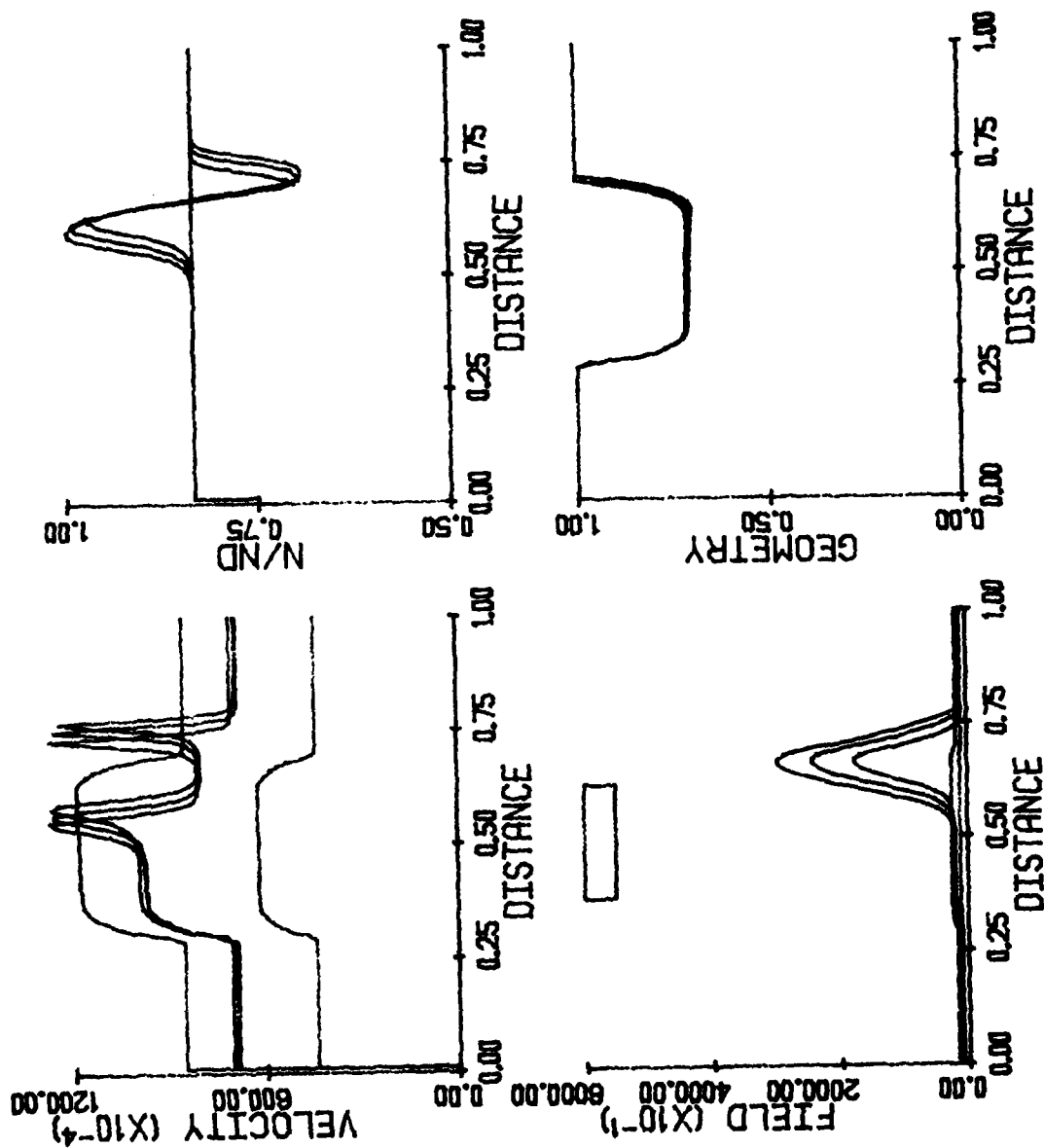
FIG. 21 DIFFUSION VARIATION TEST FACTOR = 0.5.
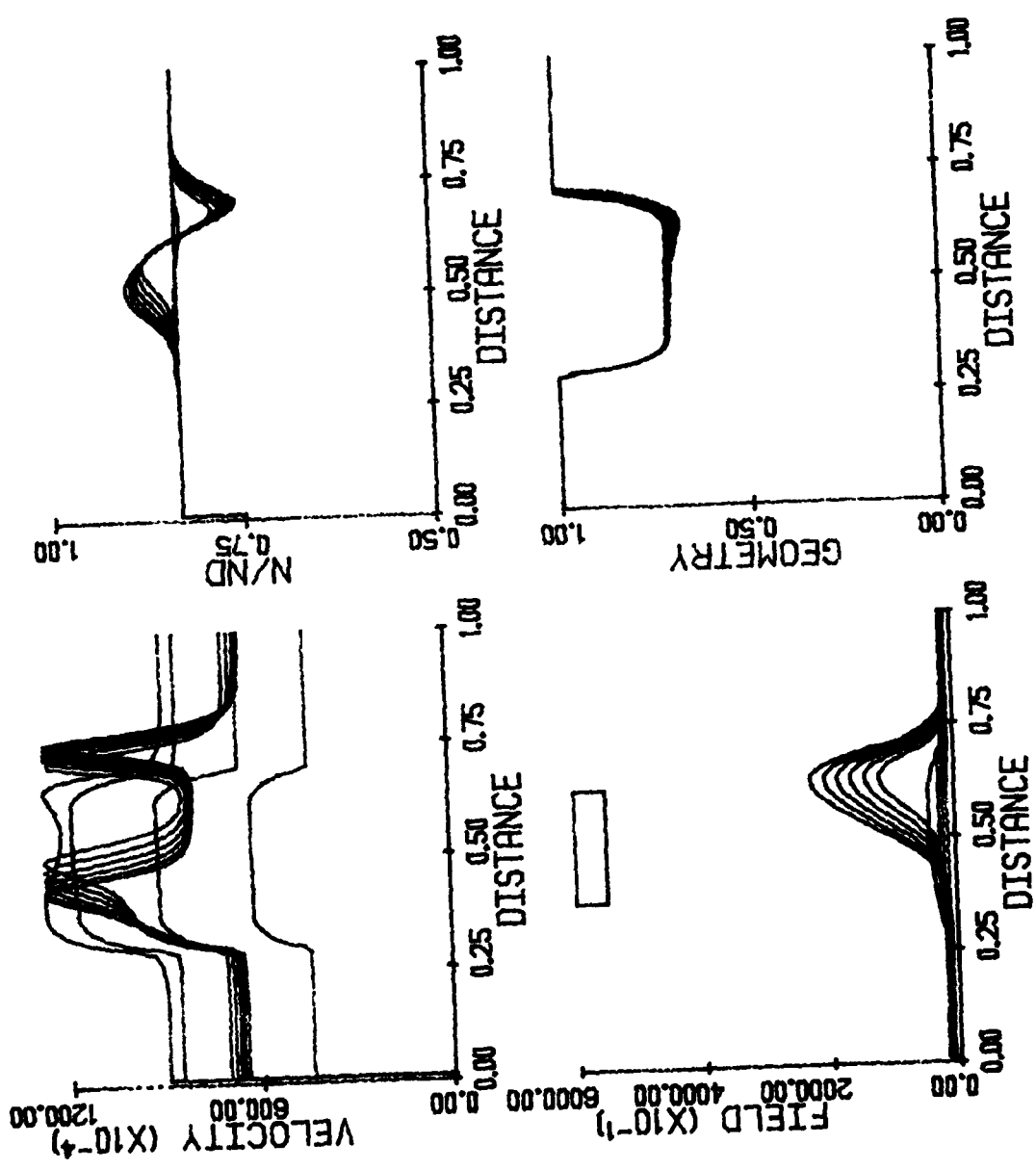
-38-

FIG. 22 DIFFUSION VARIATION TEST FACTOR = 1.
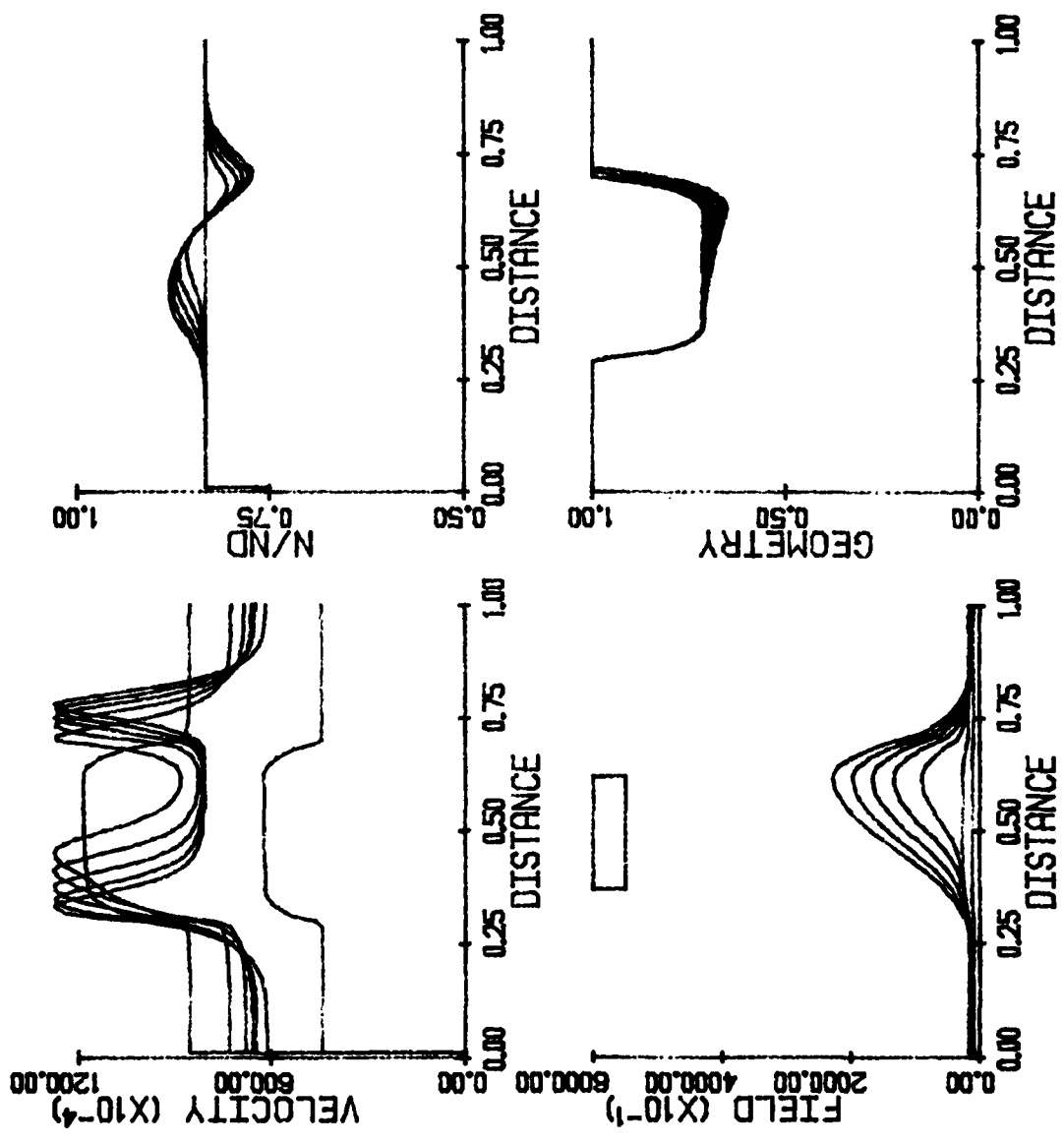
FIG. 23  DIFFUSION VARIATION TEST FACTOR = 5.

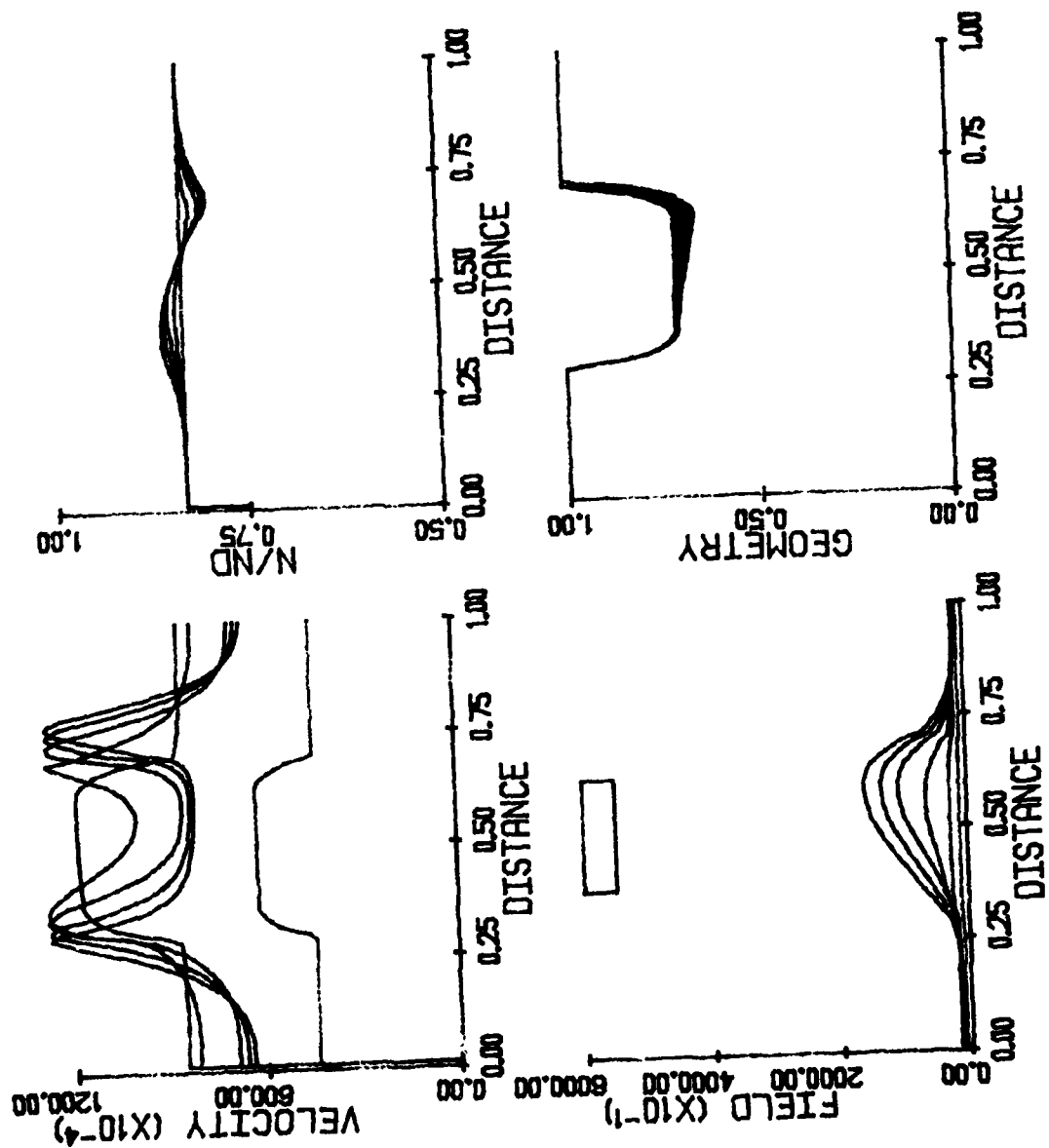FIG. 24  DIFFUSION VARIATION TEST FACTOR = 10.

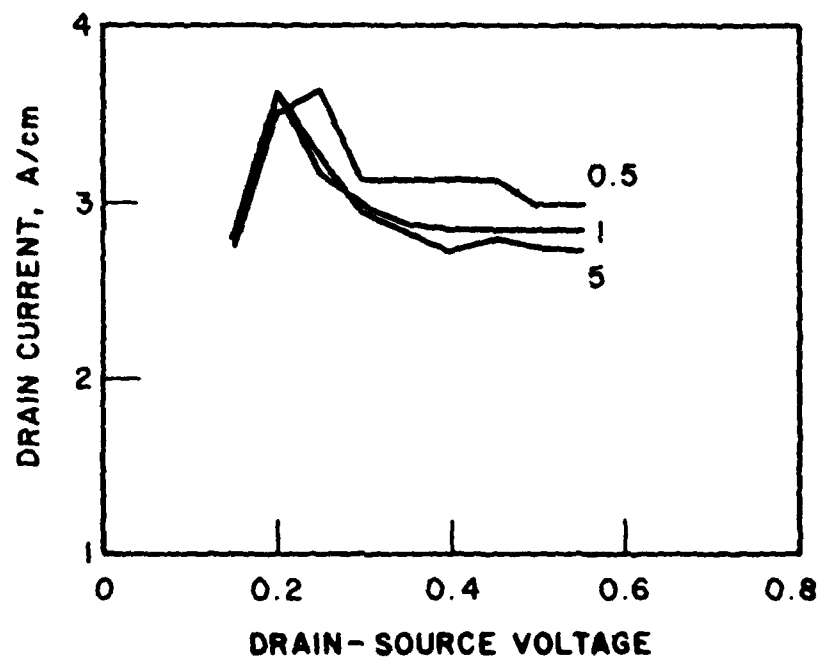FIG. 25 DIFFUSION VARIATION TEST FACTOR = 20.

FIG. 26  CURRENT-VOLTAGE CHARACTERISTIC AS A FUNCTION OF

DIFFUSION COEFFICIENT.

than 0.25 V, the electron concentration is approximately equal to the background doping, so there is no electron gradient and thus no diffusion current. The low voltage current is therefore the same regardless of the diffusion coefficient. Above 0.25-V drain-source voltage, the current depends slightly on the diffusion coefficient. The electric field curves shown in Figure 21 for the 0.5 factor case have a lower potential drop across the charge dipole than the rest of the curves. This, in turn, increases the field outside the dipole and increases the current. The factor = 1 and factor = 5 curves are also plotted in Figure 26. They are approximately the same. The factor = 10 and factor = 20 curves are the same as the factor = 5 curve.

From this set of data it is found that diffusion coefficient magnitudes greater than the typical value by factors up to 20 have no effect on the terminal current voltage characteristic. The potential drop over the resulting dipole is the same even though the shape and magnitude of the field and electron concentrations change. Thus, effects which increase the diffusion coefficient but do not change the velocity-field curve should not affect the FET terminal I-V characteristic.

Velocity-Field Curve Variation. In this section the effect of the velocity-field characteristic on FET operation is studied. The velocity-field curve used is Equation 10:

$$v(E) = \frac{\mu_o E + v_{sat} (E/E_v)^4}{1 + (E/E_v)^4} .$$

For $v_{sat} = 10^7$ cm/s and $E_v = 3000$ V/cm, the velocity-field characteristics for mobilities of 4000, 5000 and 6000 $cm^2$/V-s are shown in Figure 27. The resulting drain current vs. drain-source voltage characteristic is shown in Figure 28. For bias voltages below 0.2 V,
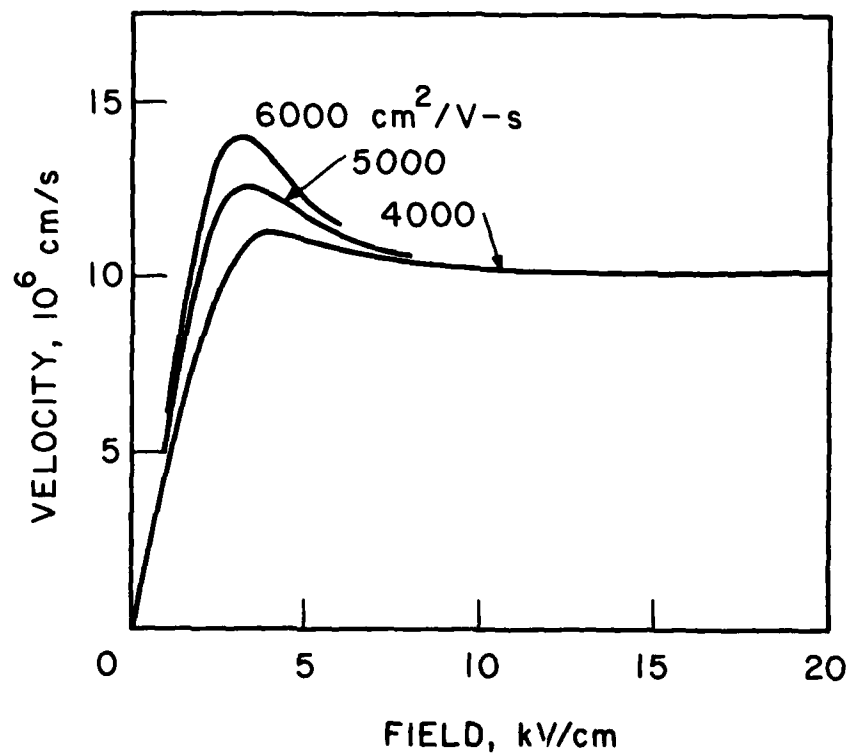
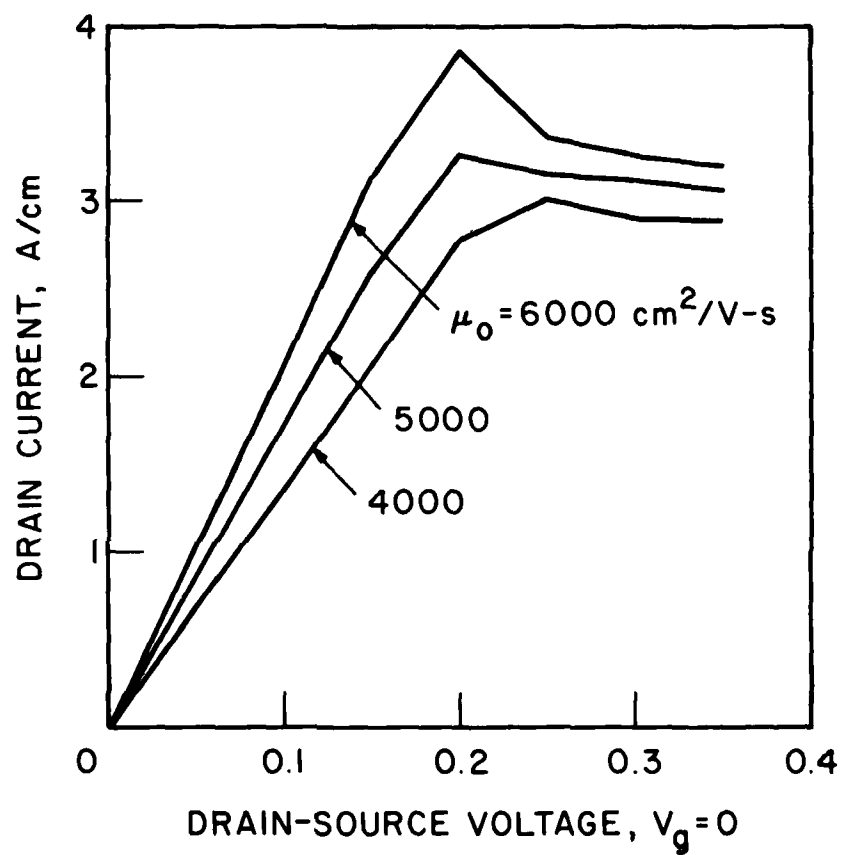FIG. 27   VELOCITY-FIELD CHARACTERISTICS FOR

VARIOUS MOBILITIES.

FIG. 28  FET OPERATION WITH VARYING MOBILITY.

there is no space charge in the channel so the electric field in the channel depends only on the geometry and is the same for the three mobility cases. The current difference then depends only on the mobility. Above the bias for peak current (0.2 to 0.25) the higher mobility currents are greater than the low mobility ones but the variation is much less than the ±20-percent variation in the low field mobility.

Saturated Velocity Variation. For $\mu_o$ = 5000 cm$^2$/V-s and $E_v$ = 3000 V/cm, the velocity-field curves for $v_{sat}$ = 8 x 10$^6$, 10$^7$ and 1.2 x 10$^7$ cm/s are shown in Figure 29. The corresponding current-voltage characteristic is shown in Figure 30. Here, since the low-field velocity-field curve is the same in each case, the linear portion of the curve is also the same. Again, a ±20-percent change in the saturated velocity produces less than a 10-percent change in the drain current in the saturated region of operation.

Peak Field Variation. For $\mu_o$ = 5000 cm$^2$/V-s and $v_{sat}$ = 10$^7$ cm/s, the $E_v$ was varied between 2000 and 5000 V/cm. The velocity-field curves for these cases are shown in Figure 31 and the resulting drain current vs. drain-source voltage curves are shown in Figure 32. Here, both the low-field and high-field velocities are the same. However, there is a greater than ±10-percent variation in the resulting current. This leads to the conclusion that the saturation current depends not on the low field mobility or saturated velocity directly but on the peak velocity. To show this, the current for a drain-source voltage = 0.35 V was plotted vs. the peak velocity for the various mobilities, saturated velocities, and peak fields in Figures 28, 30 and 32. This is shown in Figure 33. This shows the linear relationship between peak velocity and saturated current. That the saturated current should depend on the peak electron

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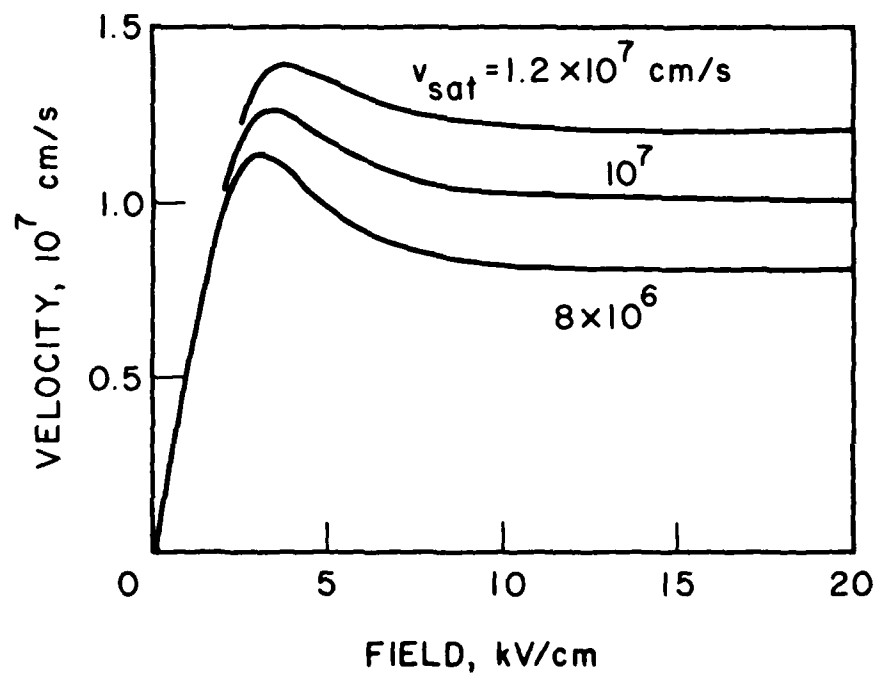
FIG. 29  VELOCITY-FIELD CHARACTERISTICS FOR

VARIOUS SATURATED VELOCITIES.

FIG. 30  SATURATED VELOCITY VARIATION EFFECTS IN FETs.

2.0

$E_p = 5000$ V/cm

1.5

4000

3000

VELOCITY, $10^7$ cm/s

1.0

2500

0.5

2000

0       5       10      15      20

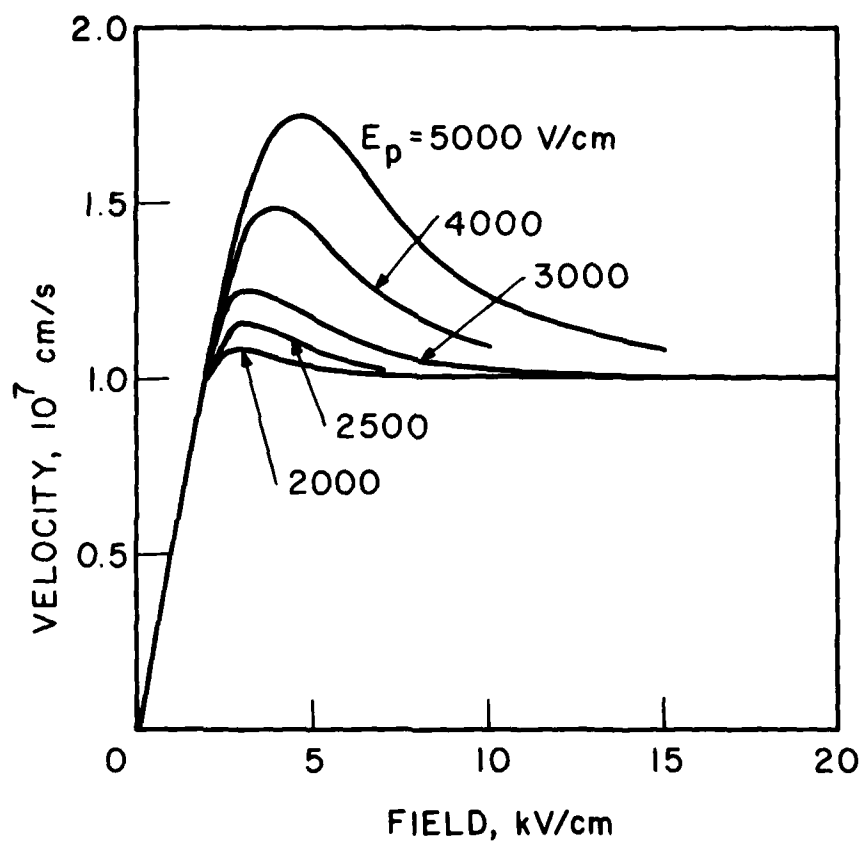FIELD, kV/cm
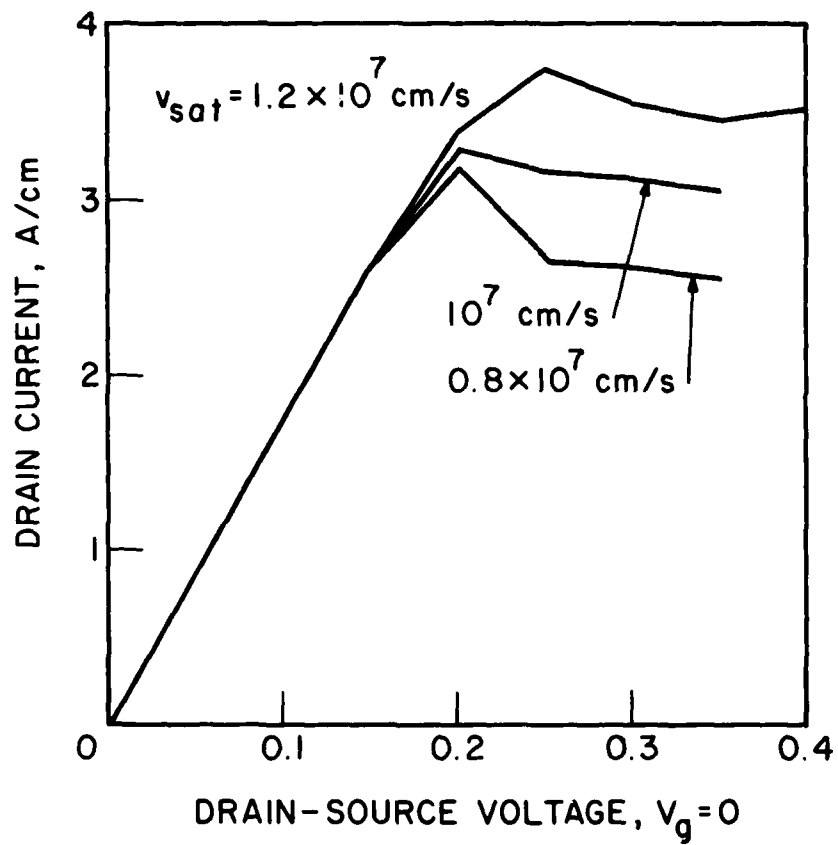
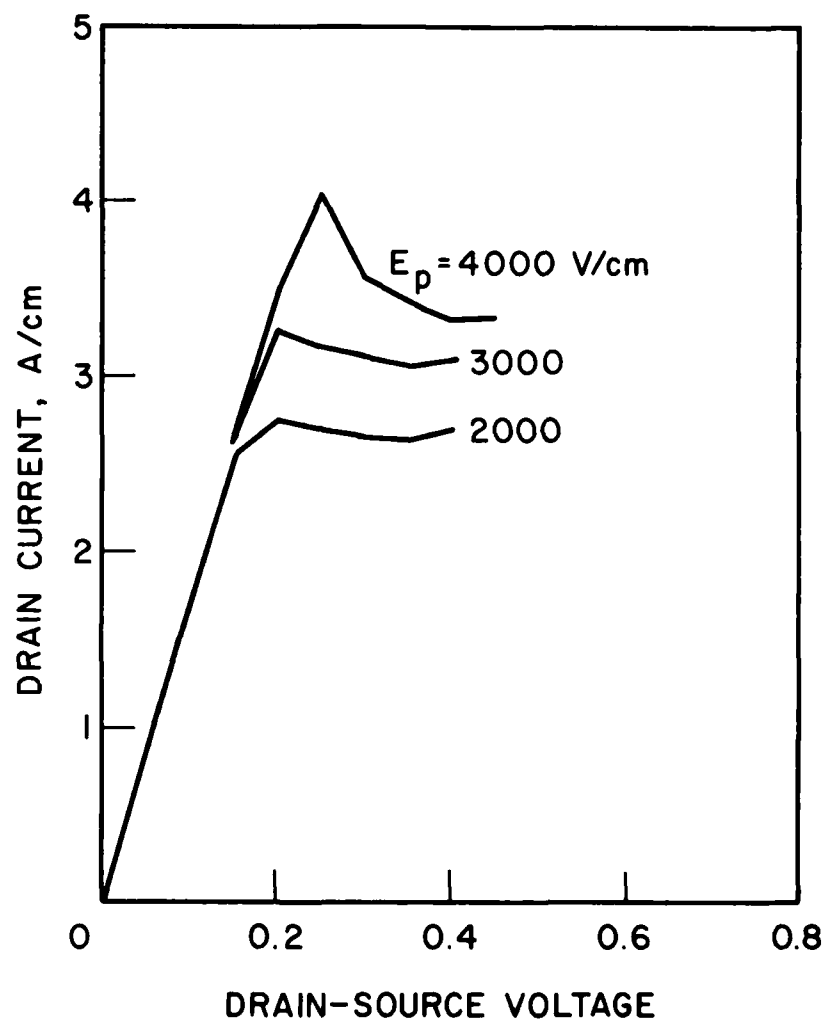FIG. 31   VELOCITY-FIELD CHARACTERISTICS WITH $E_p$ AS A PARAMETER.

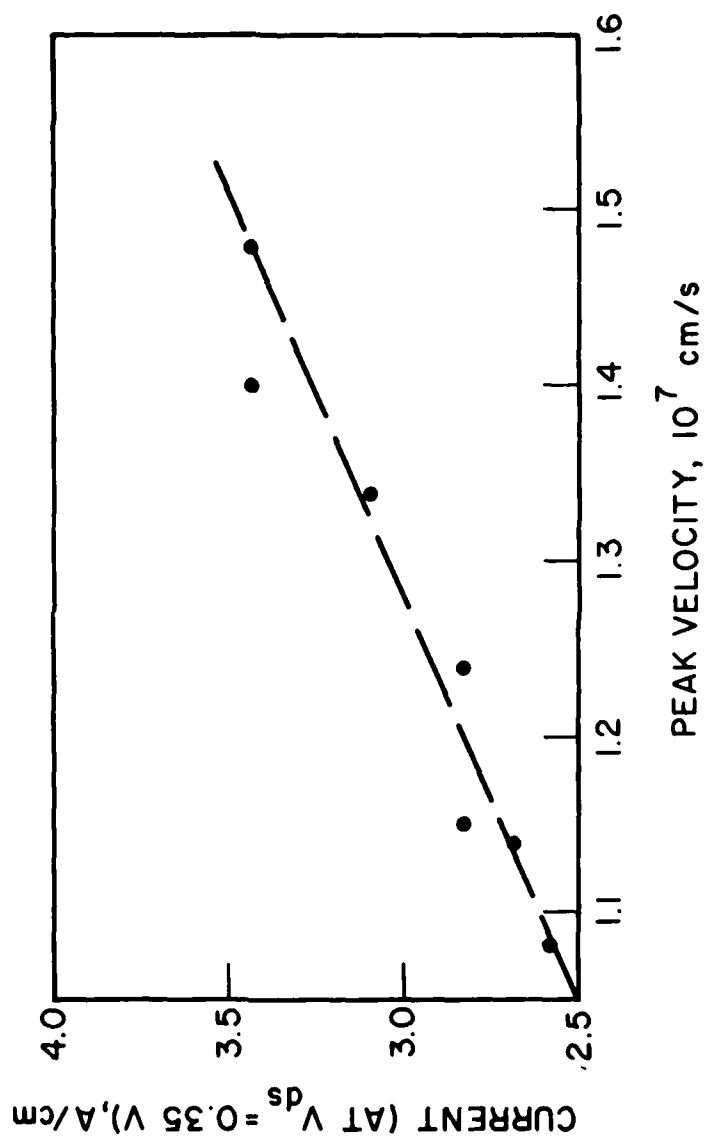FIG. 32   PEAK VELOCITY VARIATION EFFECTS IN FETs.

FIG. 33  SATURATED CURRENT VS. PEAK VELOCITY IN FETs.

velocity rather than on the mobility or the saturated velocity is reasonable for GaAs FETs. For fields below the peak velocity, there is little space charge in the channel. The high peak velocity in the high-field part of the channel corresponds to the high velocities and thus high currents at the drain and source contacts. Beyond the peak velocity field point, the current begins to drop with increasing bias. The amount of current dropback depends on the velocity dropback. This is shown in Figure 34 for the various cases of mobility, saturated velocity, and peak field. The larger velocity dropbacks give larger peak to saturation current dropbacks, but the larger peak velocities result in larger saturated currents.

Summary of Parameter Variation. FET operation over a range of gate lengths, diffusion coefficients, and velocity-field characteristics have been studied. The main factor in the saturated current and thus the transconductance is the peak velocity of the material used. The gate length and diffusion coefficient have almost no effect. The mobility, saturated velocity, and peak velocity affect the current by affecting the value of the peak velocity. Although the current is not affected by the low field mobility, the series resistance and thus the parasitics will be. Also the gate length affects the gate capacitance and thus the RF operation of the FET.
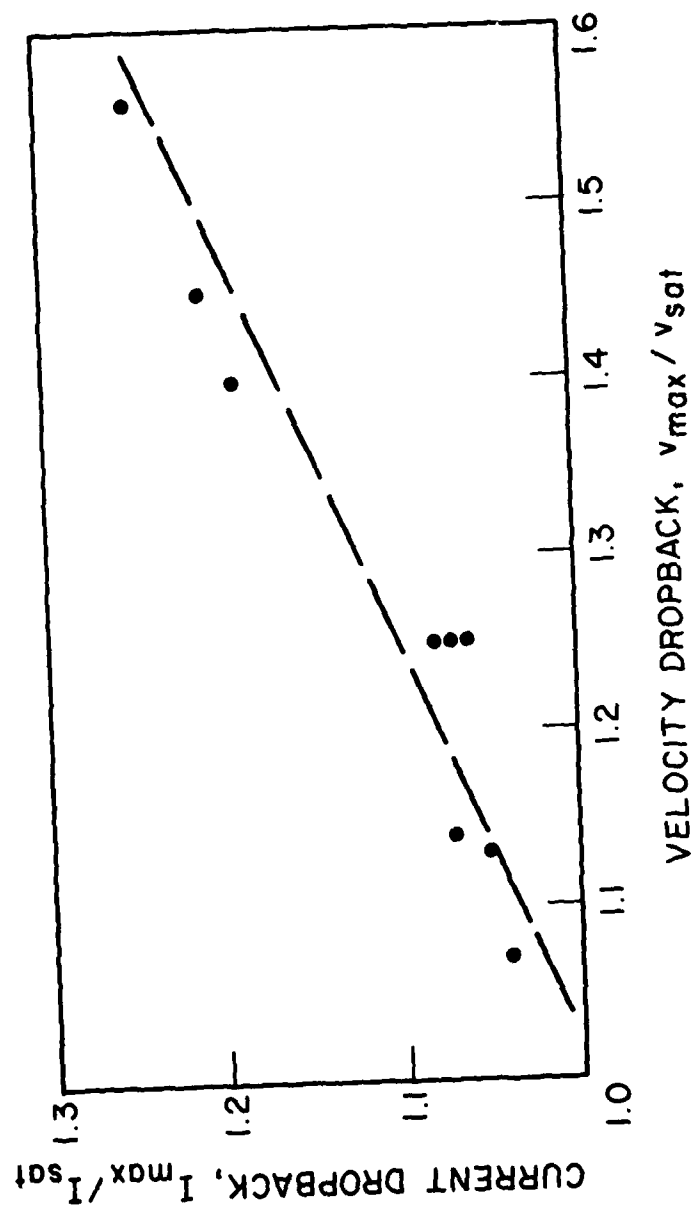
FIG. 34  CURRENT DROPBACK VS. VELOCITY DROPBACK IN FETs.

# SECTION 5

## SUMMARY AND CONCLUSIONS

The modeling and operation of GaAs FETs has been discussed in this report.  After discussing the basis of the model, the results were compared with similar two-dimensional results.  There is very good agreement between the electric field and electron distributions in the two models.  The drain currents for the simple model are approximately 25 percent higher than the similar two-dimensional results.  This problem can be solved with an improved depletion-layer model.

Various operating characteristics of FETs were discussed in Section 4.  The effect of velocity-field and diffusion-field characteristics on device operation were studied.  The diffusion coefficient has little effect on the current-voltage characteristic  of the device.  The main parameter affecting the current in the saturated region of operation is the peak electron velocity.  The gate length has little effect on the current in the saturated region.  This is because the current flow is dominated by the charge dipole formed for saturated operation.  The simple model developed here can be extended to study the following important parameters concerning FET operation:

1.  Small-signal characteristics.

2.  Electric field breakdown.

3.  High-power design.

4.  Nonequilibrium electron transport in the channel.

5.  Large-signal operation.

6.  Noise performance.

This can be achieved as follows. After the dc solution for a given FET geometry, material, and operating point has been found, the small-signal operating conditions as a function of frequency can also be determined. This involves making a linear expansion about the dc solution and solving the resulting matrix equation. The small-signal equations have been written as a subroutine for the dc program. The program is presently being added to the dc program and should be available soon. With the dc solutions available, the conditions of operation leading to avalanche breakdown can be studied. There are two high-field regions in the device, at the drain end of the gate metal and in the narrowest part of the conducting channel. The ionization integral can be found under various bias conditions to find the limits of high-power operation. This is an extension of the electric field breakdown problem. The current in the channel depends on the material parameters and geometry as discussed in this report. A variety of other possible FET materials and structures needs to be studied to find the best high-power structure.

The area of hot-electron effects can also be investigated. For a rapidly changing field (both in space and time) in the channel, the electron velocity is not well known. This, in turn, will affect the current in the channel and the operation of the FET.

The FET program as written is a time-dependent solution. The dc solution is found by solving the current transport and Poisson's equations through a transient to a steady-state solution. As presently written, the depletion-layer charging current is not included. By adding this term to the equations, large-signal operation and modeling can be achieved.

Again, as in the case of small-signal operation, having a dc solution makes a small-signal *noise* model possible. This model could improve on the simple analytic noise models presently available because of the increased complexity of the underlying dc solution.

# LIST OF REFERENCES

1.  Barnes, J., "A Two-Dimensional Simulation of MESFETs," Ph.D. Dissertation, The University of Michigan, 1976.

2.  Shockley, W., "A Unipolar 'Field-Effect' Transistor," <u>Proc. Inst. Radio Eng.</u>, vol. 40, No. 11, pp. 1365-1376, November 1952.

3.  Pucel, R., Haus, H. and Statz, H., "Signal and Noise Properties of Gallium Arsenide Microwave Field-Effect Transistors," <u>Advances in Electronics and Electron Physics</u>, Academic Press, Inc., New York, vol. 38, pp. 195-265, 1975.

4.  Shur, M. and Eastman, L., "Current-Voltage Characteristics, Small-Signal Parameters, Switching Times and Power-Delay Products of GaAs MESFETs," <u>Int. Microwave Symp. Digest</u>, Ottawa, Canada, pp. 150-152, June 1978.

5.  Dawson, R. and Frey, J., "A Simple Model for Determining Effects of Negative Differential Mobility and Magnitude of Saturated Velocity on the Performance of Schottky-Barrier Field-Effect Transistors," <u>Solid-State Electronics</u>, vol. 22, No. 3, pp. 343-346, March 1979.

6.  Kennedy, D. P. and O'Brien, R. R., "Computer-Aided Two-Dimensional Analysis of the Junction Field-Effect Transistor," <u>Semiconductor Device Modeling for Computer-Aided Design</u>, Herskowitz, G. and Schilling, R. (Ed.), McGraw-Hill, New York, 1972.

7.  Himsworth, B., "Two-Dimensional Analysis of Gallium Arsenide Junction Field-Effect Transistors with Long and Short Channels," <u>Solid-State Electronics</u>, vol. 15, No. 12, pp. 1353-1361, December 1972.

8.  Wada, T. and Frey, J., "Physical Basis of Short Channel MESFET Operation," <u>IEEE J. of Solid-State Circuits</u>, vol. SC-14, No. 4, pp. 398-411, April 1979.

9.  Himsworth, B., "A Two-Dimensional Analysis of Indium Phosphide Junction Field-Effect Transistors with Long and Short Channels," <u>Solid-State Electronics</u>, vol. 16, pp. 931-939, August 1973.

10. Laux, S. E., "Two-Dimensional Simulation of GaAs MESFETs Using the Finite-Element Method," Ph.D. Dissertation, The University of Michigan, 1980.

11. Bauhahn, P. E., "Properties of Semiconductor Materials and Microwave Transit-Time Devices," Ph.D. Dissertation, The University of Michigan, 1977.