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PHASE A REPORT
LOS SELECTIVE FADING AND AN/FRC-170(V)
RADIO HYBRID COMPUTER SIMULATION
OR 16,956

Contract No. DCA100-81-C-0016

SEPTEMBER 1981

Prepared by
Scientific Simulation Laboratory
Martin Marietta Corporation
Post Office Box 5837
Orlando, Florida 32855

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Prepared for
Defense Communications Agency
Defense Communications Engineering Center
1860 Wiehle Avenue
Reston, Virginia 22090

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FOREWORD

This report documents results of the first phase of simulation and study of the dual diversity AN/FRC-170(V) radio and frequency selective fading line of sight channel under DCA Contract DCA100-81-C-0016. Both hybrid computer and circuit technologies were used to develop an accurate and flexible simulation model of the radio and channel. A remote hybrid computer terminal has been maintained at the Defense Communications Engineering Center to provide off-site access to the simulation models.

Specific simulation tasks addressed during this period were the modeling and simulation of an improved diversity combiner, improved signal quality monitor, and adaptive threshold technique for carrier and clock recovery. Improvements, changes and additions were made to the simulation user displays and controls, a new error detection and calculation program was developed on the digital computer and a new display was developed to test and verify the individual taps that are used to develop the simulated channel.

The simulator was used to obtain simulated AN/FRC-170(V) bit error performance data for various two-ray multipath channel profiles in addition to the additive noise channel. The acquisition of AN/FRC-170(V) performance data for Rayleigh and multipath fading line of sight simulation configurations was also initiated during this first phase of study.

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<p>This report documents results of the first phase of modeling, simulation and study of the dual diversity AN/FRC-170(V) radio and frequency selective fading line of sight channel. Both hybrid computer and circuit technologies were used to develop a fast, accurate and flexible simulation tool to investigate changes and proposed improvements to the design of the AN/FRC-170(V) radio.</p>																	

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→ In addition to the simulation study, a remote hybrid computer terminal was provided to DCEC for interactive study of the modeled radio and channel.

Simulated performance of the radio for Rayleigh, line of sight two ray channels, and additive noise are included in the report. ←

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1.0 INTRODUCTION

This report discusses and documents the simulation, modeling and verification testing for the dual diversity AN/FRC-170(V) radio and line of sight (LOS) selective fading channel hybrid computer simulation. The simulated radio includes all of the circuits of the actual radio with the exception of the up and down conversions to and from the RF transmit and receive frequency. This capability will be added during the next phase of this study and will provide a tuneable RF frequency simulation. A modular approach was taken in the development of the radio model to accommodate changes and additions to the simulator. Changes and additions to the simulator are the result of evolution in the radio's design and proposed improvements to the radio. Major subsystems in the simulator are an accurate model of the AN/FRC-170(V) dual diversity radio, dual frequency selective fading LOS channels, dual signal quality monitors, diversity combiner, analog and digital displays of system variables and performance data, and an interactive users program that allows configuration and parameter changes and simulator control either locally or off-site from the Defense Communications Engineering Center (DCEC). These subsystems have been integrated to obtain the complete communication system for verification and performance testing of the AN/FRC-170(V) over LOS channels. This study has used a previous hybrid computer simulation developed under DCA Contract

DCA100-79-C-0048 as a baseline for developing an accurate model of the AN/FRC-170(V) radio for this simulation study.

The first phase of this study has included both simulation development and performance testing. The specific modeling tasks for this phase of the study are briefly described below. These include tasks 1, 2, 4, and 5 of the statement of work, R220-81-11.

Task 1 required the modeling and simulation of an improved diversity combiner for the AN/FRC-170(V) radio and integration of this simulation into the hybrid computer simulation model. The simulation user has the option of selecting the original or improved combiner at the beginning of each simulation test. The improved combiner utilizes both the signal quality monitor and received signal level (RSL) monitor. The thresholds and hysteresis of the monitors can be adjusted by the simulation user. The government provided the block diagram of the improved combiner that was used in developing the simulation module. This diagram is included in this report. The combiner response is provided as an analog output for monitoring to a Brush recorder and is also used in determining diversity bit error performance.

Task 2 included the modeling and simulation of an improved signal quality monitor (ISQM) function and integration of this function into the AN/FRC-170(V) hybrid computer simulation. The ISQM was based on a pseudo-error technique that was provided by the government. This model is an option that can be selected by the simulation user. Once selected the register length can be changed to provide the desired dynamic range.

A range in excess of 25 dB can be accommodated by the simulation. Variables that can be recorded on the Brush recorder during a simulation test include register position and register underflow and overflow switch positions. A block diagram of this technique is included in the report.

Task 4 required the maintenance of an accurate modular hybrid computer simulation of the dual diversity AN/FRC-170(V) radio and frequency selective fading channel and the addition of proposed product improvements, a tuneable RF feature and TDM framing pattern in the data stream. Under this task provision is made for DCEC access to the complete simulation via the hybrid remote terminal in place at DCEC, Reston, Virginia. Two new displays are called for under this task. They are a CRT and handcopy plot of BER versus received signal level and an indicator of fade outage measured in percent of time spent below a selectable threshold. Other requirements of this task will be reported on in the final report for this study.

Task 5 includes the development of all interactive displays and controls to be provided for the remote hybrid terminal user at DCEC. These have included the following:

- Display of all available program options
- Summary display of simulation configuration showing program options and parameter choices selected by the simulation operator
- Spectrum Analyzer Display of power density spectrum at Baseband, IF and RF (pre- and post-amplification filtering)

- Tabular listing of experiment Bit Error Rate for non- and dual diversity
- Baseband eye patterns for cophasal and quadrature QPR modem branches
- Logarithmic fading channel envelope displays (analog) vs. time
- Analog displays of AGC and SQM outputs vs. time
- Diversity switch status (on-line indications for channel "A" or channel "B")
- Channel Distribution Function
- Other displays as deemed necessary to the effective and efficient operation of the simulation.

The last requirement of this task was the provision for a hybrid computer remote terminal to be made available at DCEC for engineering use in verification and analysis of the simulated LOS transmission system.

2.0 AN/FRC-170(V) RADIO AND LOS CHANNEL SIMULATION

This section describes the current simulated model of the AN/FRC-170(V) radio and line of sight channel. It includes additions and circuit modifications needed to maintain an accurate, modular, and flexible waveform simulation of the LOS radio and channel characteristics. Three major improvements have been made to the baseline radio model developed under DCA Contract, DCA100-79-C-0048. These are an improved automatic gain control circuit (AGC), an adaptive baseband threshold circuit for demodulation and bit timing recovery and a multiple time scale capability that permits the modeling of multipath delay from 2.0 bits to .02 data bits. The channel model is unchanged from the model developed under the previous contract, but changes in the fixed fade rate of each tap are planned. Figure 2-1 is a functional flow diagram of the current system with the exception of the adaptive equalizers, up and down conversions and coherent combiners which will be added in the next phase of the study.

The major systems of this LOS transmission system model are the dual diversity radio, dual LOS frequency selective fading channels, performance monitors, diversity combiner, and an interactive user display and control program that allows off-site operation from DCEC, Reston, Virginia.

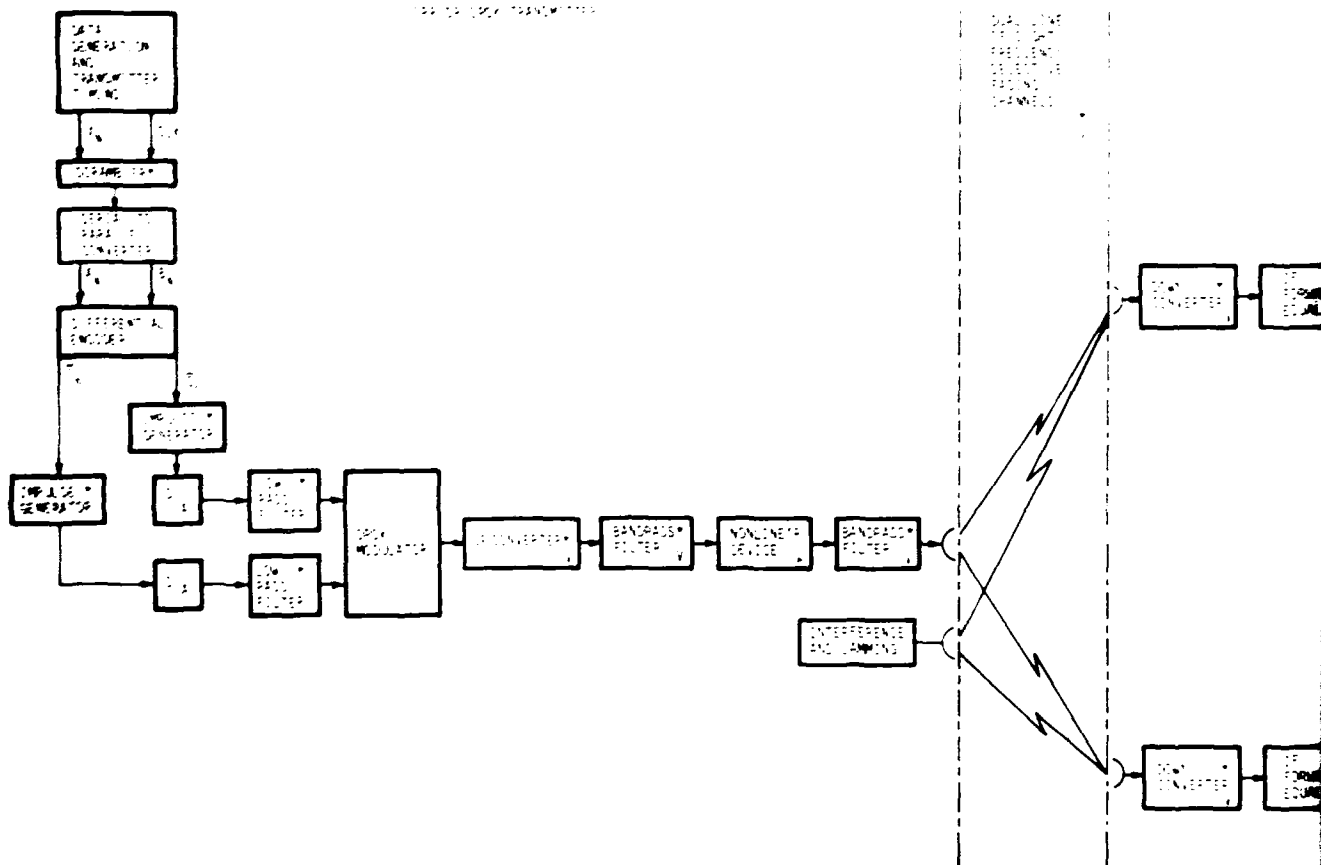
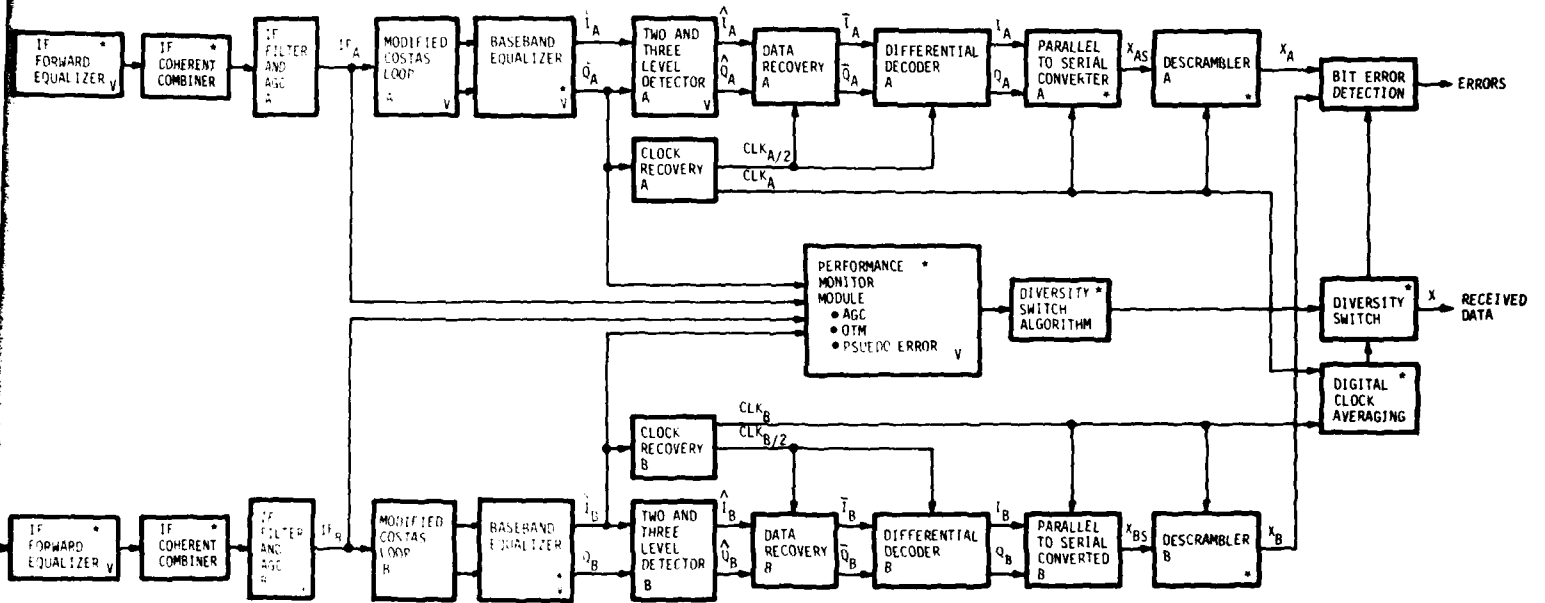


Figure 2-1. AN/FRC-170(V) LOS Simulation Model

QPSK OR QPSK RECEIVERS



* - OPTIONAL MODULE
 V - VARIABLE MODULE

2.1 DRAMA RADIO MODEL

The simulated model of the dual diversity AN/FRC-170(V) radio includes all of the important functional characteristics unique to the actual radio. These include the capability to simulate level I quadrature phase shift keyed (QPSK) transmission and level II quadrature partial response (QPR). Selection of one or the other modulation scheme can be accomplished almost instantaneously by the simulation user. Other important circuits of the simulated radio are the partial response baseband filters, modified Costas loop demodulator, adaptive baseband threshold detection, and separate bit timing recovery for each baseband rail.

The hybrid computer simulation of the AN/FRC-170(V) radio provides an interactive scale model which can be configured and changed programmatically by the simulation user to evaluate the resulting performance of product improvements and design changes for anticipated transmission channels. This simulation has been implemented by frequency scaling hybrid computer models of the prototype modem circuits and implementing these models with analog, parallel logic, and digital computing elements. The resulting computer simulation is more than 100 times faster than comparable waveform digital simulations. Two time scales are selectable in the simulator to provide a capability of simulating tap delays in the range of 2.0 to .02 data bits. The necessity of two time scales is a result of limited bandwidth of the digital delay device used in the channel model simulation. Normal time scale is unity (1) providing tap delays of 2.0 to .2 data bits and one-tenth (1/10) providing tap delays

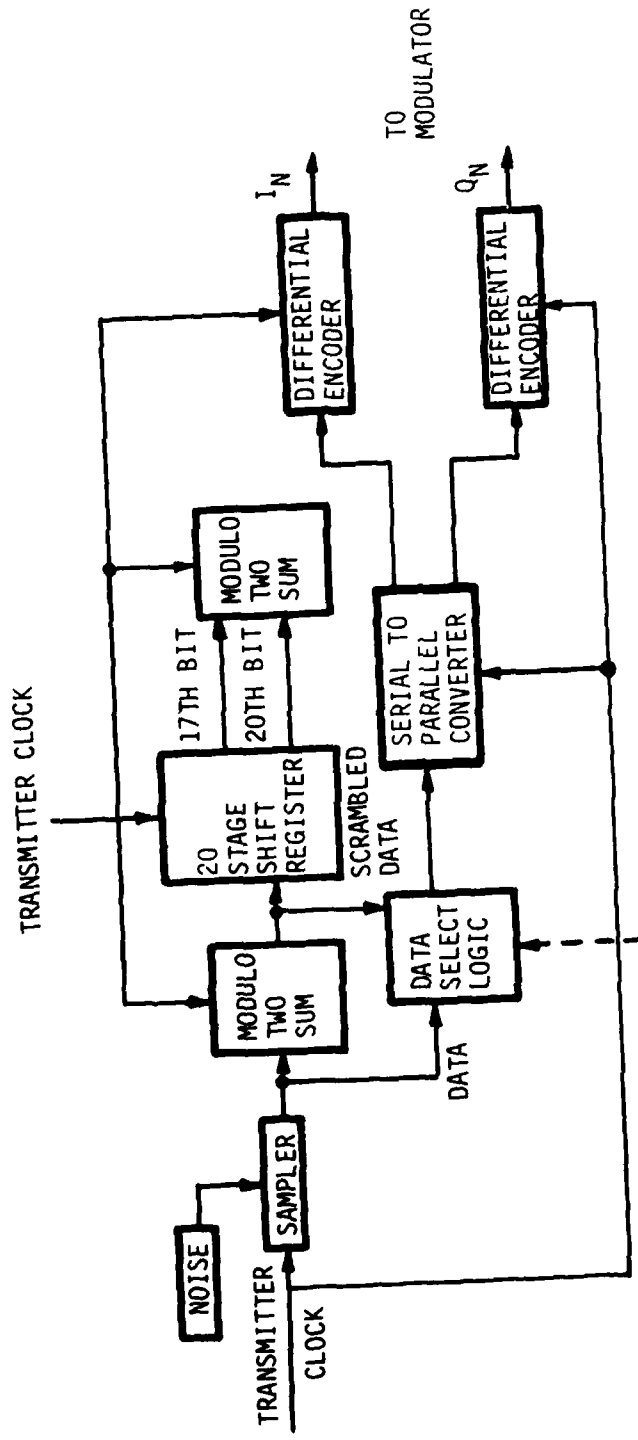
of .2 to .02 data bits. With the normal time scale selected a scale factor of 1/26,112 is used to scale actual radio frequencies down to values that fit within the hybrid computer bandwidth. In the normal time scale mode real IF, bit stream and baseband frequencies of 70 MHz, 26.112 MBS and 13.065 MBS are simulated at frequencies of 2.681 KHz, 1 KHz and 500 Hz respectively.

Major modules of the dual diversity AN/FRC-170(V) radio simulation are bit stream generation and processing, QPR/QPSK modulator, transmitter signal processing, IF filter and AGC, modified Costas' loop demodulator, bit timing recovery and data regeneration. The models and simulation of these modules are discussed in the subsequent paragraphs.

2.1.1. BIT STREAM GENERATION AND PROCESSING

The bit stream generation and processing module for the AN/FRC-170(V) radio is the same for both level I (QPSK), and level II (QPR) modes of transmission. This module includes the generation of a random data source, 20-bit self-synchronizing scrambler, serial to parallel converter and differential encoder. A functional flow diagram of the integration of these circuits is shown in Figure 2-2.

The serial bit stream generator provides the psuedo random data input which would be present at the multiplexer port. A serial bit stream simulating this output was generated by sampling an analog noise source with the simulated transmitter bit rate clock. The transmit bit rate clock was implemented on the analog computer by counting down a crystal oscillator. Bit stream generation will be converted to an all digital technique during the next phase of study to allow inclusion of the radio internal TDM frame pattern bits.



CONTROL

Figure 2-2. Data Generation and Processing

A self-synchronizing scrambler with 20 stages was modeled to ensure a random modulating bit stream. This circuit, which eliminates long series of ones and zeros from occurring in the modulating bit stream, has been provided as an option. The randomness guaranteed by implementing the scrambler results in a better spectral component of the bit rate clock and provides a better likelihood of clock recovery as a result of additional data transistions.

A model of the scrambler used in the AN/FRC-170(V) radio was obtained by modulo 2 summing the serial data stream with the modulo 2 sum of bits 17 and 20 from a 20 stage shift register. The 20 stage shift register was mechanized by ganging 5 four bit shift registers on the analog computer.

The serial to parallel converter was mechanized by retiming the scrambler output with the symbol clock (one-half the data rate). Symbol timing was used to clock the I and Q data with a one-half symbol delay with respect to one another. The delay between I and Q basebands improves resolution of the two-phase ambiguity states at the receivers.

Each of these parallel bit streams was input to differential encoders which resolve any polarity inversion at the demodulator. These encoders are modeled as a modulo sum (exclusive "OR"). This circuit does a logical multiply of the feedback and data. Outputs from the two encoders provide the inputs to the modulation circuit.

Except for data generation which consists of a broadband noise source and analog sampler (track/store integrator), the entire data generation and processing module was simulated using the parallel logic

capability of the analog computer. Modulo 2 sums and differential encoders were programmed using a combination of gates and flip/flop delays. The scrambler uses five 4-stage shift registers in series to provide the 20-bit delay. Serial-to-parallel conversion was simulated by using flip/flops enabled by inverted symbol clocks to provide a one-half symbol delay between one symbol bit stream and the other.

2.1.2 QPR/QPSK MODULATOR

The simulated AN/FRC-170(V) radio modulator section includes impulse generators for QPR transmission, digital-to-analog switches, transmit baseband filters, inphase and quadrature multipliers, and a crystal controlled reference oscillator. Input to the modulator module is from the I and Q differential encoders. Figure 2-3 is a functional flow block diagram of the major circuits for the modulator simulation. When QPR modulation is selected by the user, the I and Q modulation signals are generated by using the encoded I and Q nonreturn to zero (NRZ) logic to drive impulse generators. Each impulse stream becomes the driving function for one of the Class I partial response transmit filters, which provide the inputs to the inphase and quadrature balanced modulators. If QPSK modulation is selected, a path is provided directly from the encoded I and Q NRZ data to the inphase and quadrature balanced modulators. The I and Q modulators outputs are summed to generate either QPR or QPSK signaling.

The Class I partial response filters provide a controlled amount of intersymbol interference. Combined with the receiver baseband filters they approximate a cosine response that produces a three level signal

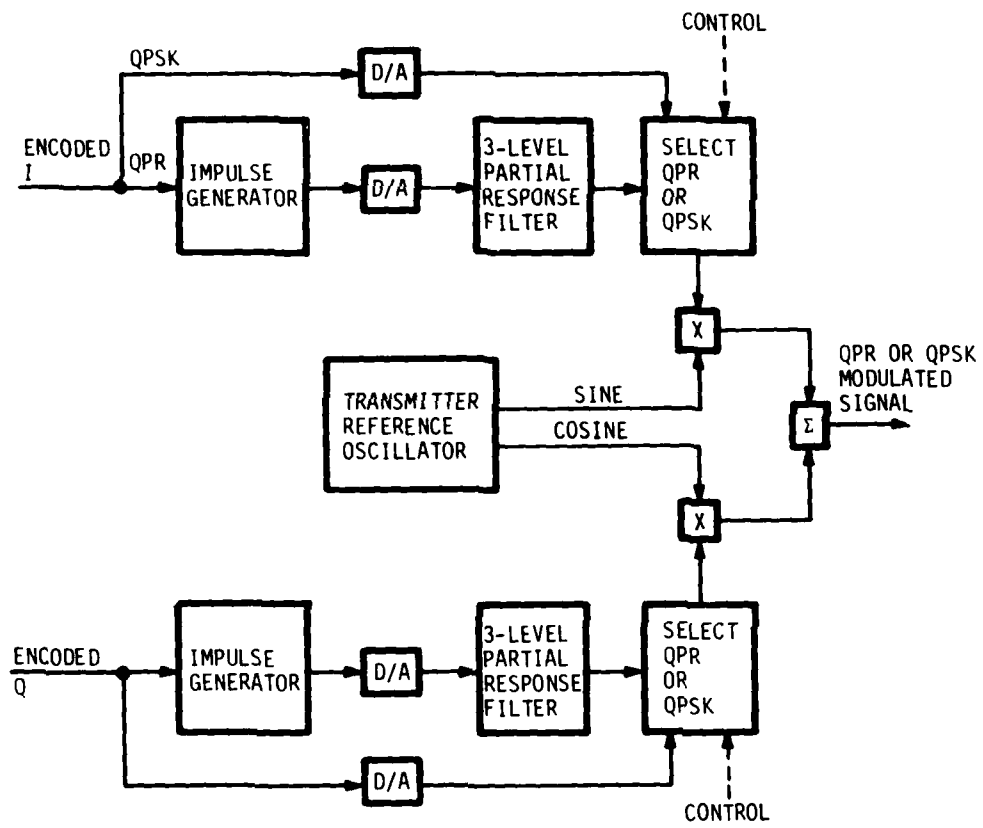


Figure 2-3. QPR/QPSK Modulator

at the receiver baseband output. In the simulation these filters are bypassed for QPSK.

Simulation models of the modulator circuits were programmed using both logical and analog computer techniques. Programs developed for the modulation functions and all other subsystems of the AN/FRC-170(V) radio are under the control of the digital computer segment of the hybrid computer. This approach makes parameter and configuration changes, set-up procedures and data acquisition very fast, and also provides needed documentation for every simulation test.

Encoded I and Q digital baseband signals are input to impulse generators if in a QPR mode, and to the quadrature multipliers if in a QPSK mode. The impulse generators were mechanized using monostable elements (one shots) of the parallel logic on the analog computer. These devices have an adjustable pulsewidth which was set to provide the desired impulse response from the partial response filters. The QPR or QPSK digital NRZ modulating signals were A to D converted using electronic digital-to-analog switches that generated plus and minus analog dc levels corresponding to the +1 and -1 logic.

If QPR was selected, these signals drove the I and Q transmit half of the partial response filters. When QPSK was selected, the digital computer sent control signals to the analog computer, which gated the encoded baseband signals directly to electronic switches and bypassed the partial response filters.

The processed baseband signals were input to four quadrant analog multipliers that multiplied the I and Q baseband with sine and cosine

signals from the reference oscillator. The summation of these two multipliers resulted in either QPR or QPSK signaling, as determined by the simulation configuration selected by the user. A crystal controlled reference oscillator for this modulator section was programmed using two analog integrators with feedback to stabilize the amplitude and a crystal controlled digital clock to maintain a fixed frequency.

2.1.3 PARTIAL RESPONSE FILTER MODEL AND SIMULATION

The transmit partial response filters were programmed from the transfer function:

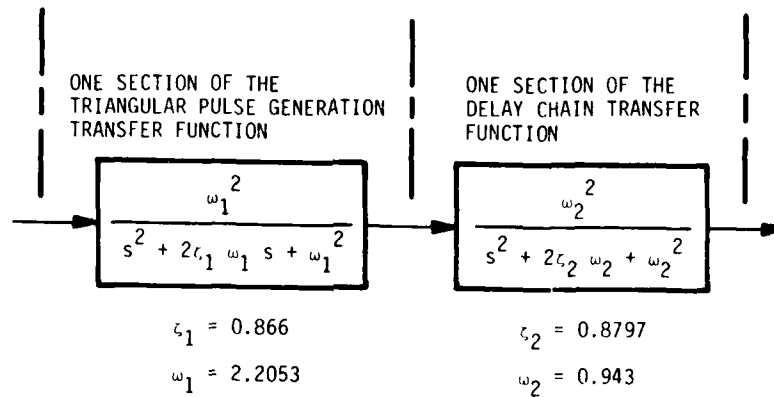
$$H(s) = \frac{3.25104}{s^4 + 4.3966s^2 + 9.28835s^2 + 8.105s + 3.25104}$$

Analog computer techniques for transfer function simulation were used to model these filters.

The partial response filters were designed to fit the frequency and the impulse response of a Class I, partial response filter. This approach ensured the desired intersymbol interference with adjacent pulses and prevented undesired intersymbol interference with other pulses.

This filter was mechanized as two identical fourth order stages, as shown in Figure 2-4. The first half is in the transmitter and the other half is in the receiver. The filter design was derived from a method based on the piecewise linear approximation to the impulse response curve. This system model was designed by allotting fourth order transfer functions to the triangular pulse generator and the delay chain, each formed as the square of a second order transfer function. Thus the identical

transmitters and receiver filters are formed from second order parts of the triangular pulse generator and delay chain.



WHERE s IS SCALED TO THE FILTER CUTOFF FREQUENCY

Figure 2-4. Partial Response Filter, Transmitter, and Receiver Filter Transfer Functions

The triangular pulse generator impulse transfer function is given

by

$$T(s) = \frac{T}{2} \left[\frac{1 - e^{-s\frac{T}{2}}}{s} \right]^2 \approx \left[\frac{\omega^2}{s^2 + 2\zeta\omega s + \omega^2} \right]^2$$

and its approximation was formed by equating the first few terms of the Taylor series for each.

The mechanized filter was tuned to give the desired impulse response. It has a bandwidth of three symbol pulsewidths and is essentially symmetrical about the peak. The filter has minimum intersymbol interference at the third and fourth symbol pulse times.

The baseband filters currently being used are the same as those used in a previous QPR transmission model. A new set of partial response baseband filters using elliptical functions have been mechanized and are

being tested. These elliptical filters will provide responses nearer to the actual AN/FRC-170(V) filters. Transfer functions of the transmitter elliptical baseband filters are given below.

$$H(S) = A \frac{a_0 \omega_c}{S + a_0 \omega_c} \prod_{i=1}^3 \frac{s^2 + \Omega_i^2}{s^2 + 2a_i S \omega_c + (a_i^2 + b_i^2) \omega_c^2}$$

This filter is a 7th order elliptical lowpass filter whose parameters determine the bandwidth and attenuation characteristics. The analog simulated response and theoretical response using the following parameters is shown in Figure 2-5.

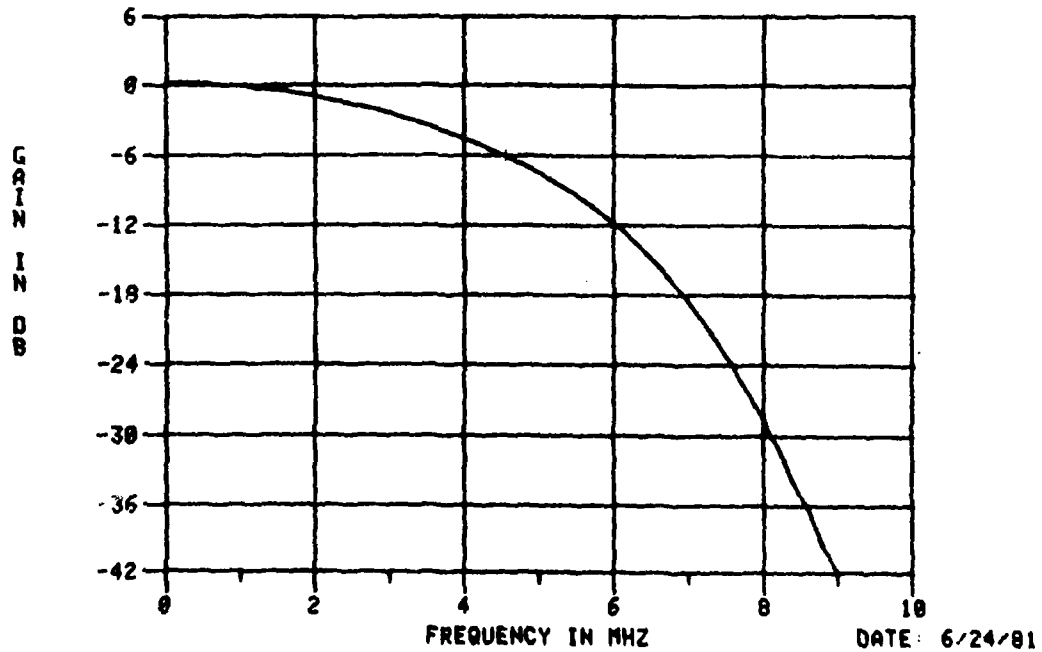


Figure 2-5. Simulated Response of the 7th Order Transmit Baseband Filter

Filter parameters are:

$$\Omega_1 = 1.4936$$

$$\Omega_2 = 1.7741$$

$$\Omega_3 = 2.9970$$

$$a_0 = .6746$$

$$a_1 = .5279$$

$$b_1 = .6183$$

$$a_2 = .2741$$

$$b_2 = .9588$$

$$a_3 = .0793$$

$$b_3 = 1.0826$$

$$W_c = 1688 \times 26,112 \text{ (ACTUAL RADIO FREQUENCY)}$$

and 1688 SIMULATED FREQUENCY

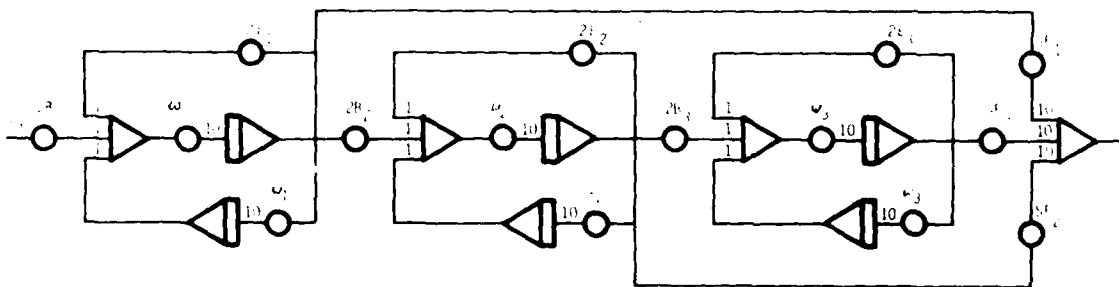
2.1.4 TRANSMITTER SIGNAL PROCESSING

A typical transmission section was modeled for the AN/FRC-170(V) radio. This configuration includes two transmitter bandpass filters for spectral limiting and a TWT power amplifier. All of these devices are modeled on the analog computer and can be configured by the simulation user. This RF portion of the transmission was simulated without the up and down conversion to RF frequencies; thus, the simulation was at IF frequency. This conversion process is to be added in the next phase of this study.

Optional spectral control bandpass filters and an optional non-linear amplifier were simulated for the transmission module. These bandpass filters were programmed to permit the selection of either Butterworth, Bessel, or Chebychev characteristics for two, four, or six poles. A stagger-tuned simulation approach was taken, where the

parameters for each stage were calculated and set by the digital computer, based on parameter inputs by the user for center frequency, ripple and bandwidth. The digital computer then calculates and sets the parameters of each stagger-tuned section to produce the desired overall frequency response of the filter.

Referring to Figure 2-6, the filter parameters β , ϵ , and ω of each stage represent the gain bandwidth product, bandwidth, and center frequency, respectively. SF_1 , SF_2 , and SF_3 are the scale factors that adjust the overall gain of the filter to ensure unity gain and select the order of the filter.



SIMULATES SECOND, FOURTH, OR SIXTH ORDER
 CHEBYSHEV, BUTTERWORTH, OR BESSEL BANDPASS FILTER.

Figure 2-6. Bandpass Filter Simulation

The nonlinear device subsystem simulates the AM/AM and AM/PM characteristics of the AN/FRC-170(V) radio TWT.⁽¹⁾ The TWT simulation is shown in Figure 2-7. The CPDFG function generators have been replaced by a Multi-Function Table Processor (MFTP). Both the AM/AM and AM/PM characteristics of the DRAMA TWT are generated by the MFTP.

The MFTP is a high speed special purpose digital device designed to perform the operations of table lookup and linear interpolation in a manner to generate functions of one to four variables from preloaded data tables.

The modulated carrier is input to an envelope detector, which determines the time-varying amplitude of the carrier by diode-detecting the signal magnitude and filtering out the carrier frequency. This amplitude output drives the two functions in the MFTP which are loaded with the AM/AM and AM/PM characteristics of the nonlinear device. The output of the AM/PM function determines the time constants for an analog computer programmed phase shifter that shifts the modulated carrier by the corresponding gain. Graphs of AM/AM and AM/PM characteristics for the TWT are shown in Figures 2-8 and 2-9.

(1) Thomas, C. M., Alexander, J. E., and Rahneberg, E. W., "A New Generation of Digital Microwave Radios for U.S. Military Telephone Networks," IEEE Transactions on Communications, Vol. Com-27, No. 12, December 1979.

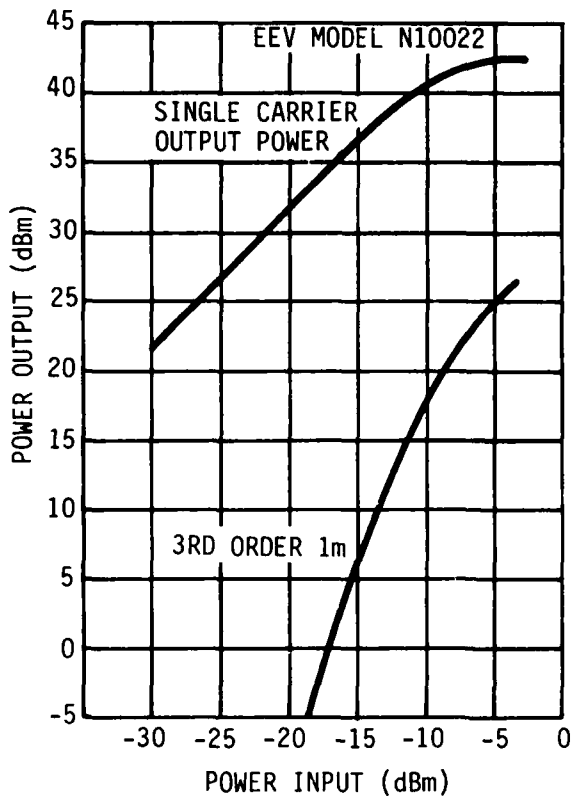
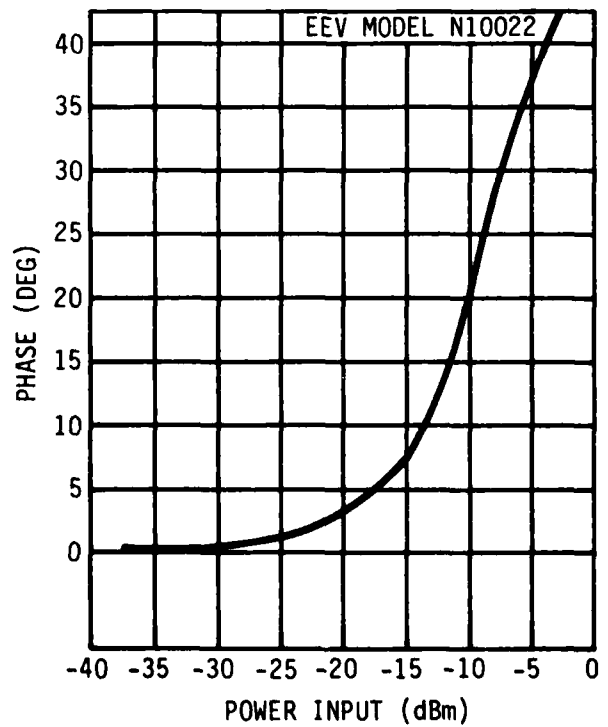


Figure 2-8. TWT AN/AM Characteristic

Figure 2-9. TWT AM/PM Characteristic



2.1.5 IF FILTER AND AGC CIRCUIT

The AN/FRC-170(V) dual-diversity receiver simulation was composed of two identical receiver chains. Each included an IF and AGC section, modified Costas loop demodulator, three-level detection for QPR and two-level detection for QPSK, bit timing recovery, and data regeneration.

Each receiver model has an IF and AGC section that preprocesses the receiver signal from the antenna using bandpass filtering and automatic gain controls.

The modeled IF filter model is a 6-pole bandpass filter with a variable bandwidth. Nominal bandwidth for a data rate of 26.112 Mb/s is 35 MHz. The AGC circuit for the real system and model has a dynamic range of >60 dB and controls the baseband signal level by gain adjustment to the IF signal.

The simulated IF section for each receiver filters the IF signal plus noise and automatically controls the gain of the received baseband signal. Nominal values for the prototype modem's IF filter center frequency and bandwidth are 70 MHz and 35 MHz, which are 2681 Hz and 1508 Hz for the simulated filter. The IF bandpass filter simulated on the analog computer was programmed to model the characteristics of Butterworth, Bessel, or Chebychev bandpass filters up to six poles. User programs have been developed to permit parameter changes for bandwidth, center frequency, ripple factor, and filter order.

The AGC circuit rectifies the baseband signal and filters it with a lowpass filter to detect the baseband amplitude. The error between this amplitude and the nominal value is produced. This error is then

applied to the AGC loop filter that sums the instantaneous error and an integrated error as shown in Figure 2-10. This summation is the gain which the baseband signal is multiplied by to achieve the nominal amplitude. The nominal value of amplitude is 25 volts. The dynamic range of the AGC circuit is 60 dB.

2.1.6 MODIFIED COSTAS LOOP DEMODULATOR

The AN/FRC-170(V) radio uses a coherent demodulation technique which makes hard decisions on the filtered baseband and detects cross channel contamination between the I and Q demodulated symbol streams to phase lock a voltage controlled oscillator. This method of demodulation uses a modified Costas loop to extract the modulating signal. By multiplying the received IF signal with the inphase and quadrature components of the phase locked reference oscillator, the two symbol streams (I and Q) can be detected. Outputs of the I and Q phase detectors drive partial response, full cosine filters for QPR and full response raised cosine filters for QPSK. The phase lock loop uses a cross correlation between the quadrature symbol streams low-pass filter outputs and hard decision estimates to generate a phase error signal. A difference of the resulting cross correlations is filtered and input to the reference VCO to phase lock it to the modulated carrier. The data estimation circuits provide two-level decisions for QPSK and three-level decisions for QPR. Baseband filter bandwidths are set to one-half data rate for QPSK and one-fourth data rate for QPR.

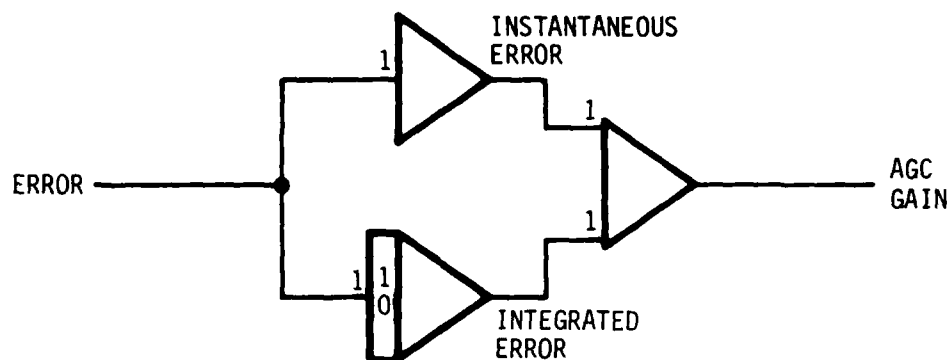


Figure 2-10. AGC Loop Filter

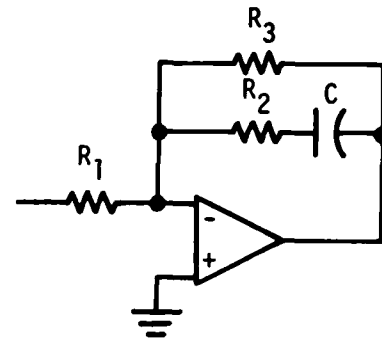
New design data for the carrier recovery phase lock loop filters have been incorporated into the AN/FRC-170(v) radio simulation. Separate filters for lock and acquisition modes of the phase lock loop are now selected based on the receiver's "lock" indicator. In the lock mode both a narrowband and crutch filter are selected. In the acquisition mode the carrier VCO is slaved to the modulator crystal controlled VCO and a wideband filter is selected. Both the narrowband and wideband PLL filters are Type 1 second order improved types. The crutch filter is a Type 2 second order type. The circuits and transfer functions of these loop filters are given in Figure 2-11.

Identical demodulators with modified Costas loops were simulated on the analog computer for each of the dual diversity receivers. This circuit coherently demodulates either QPSK or QPR transmission, depending on modulation technique selected. For QPR the low-pass filters following the phase detectors were complements to the transmit partial response filters.

The transfer function used for these filters was

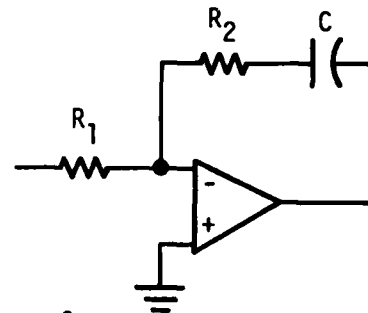
$$H_r(s) = \frac{3.25104}{s^4 + 4.3966s^3 + 9.28835s^2 + 8.105s + 3.25104}$$

$$H(S) = \frac{R_3}{R_1} \left[\frac{1 + SR_2C}{1 + S(R_2 + R_3)C} \right]$$



NARROWBAND AND WIDEBAND, TYPE 1, SECOND ORDER IMPROVED

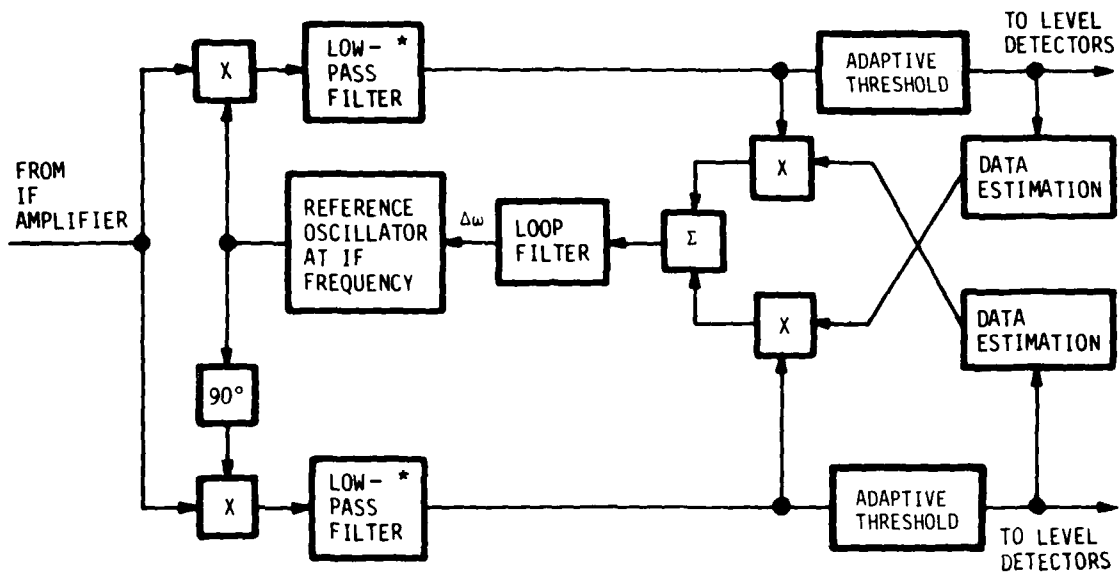
$$G(S) = \frac{1 + SR_2C}{SR_1C}$$



CRUTCH, TYPE 2, SECOND ORDER

Figure 2-11. Carrier Phase Lock Loop Filters

For the QPSK mode the filter was modified to approximate a full response with linear phase. By using a fourth order Butterworth low-pass filter, a two-level baseband signal was obtained instead of the three-level signal for QPR. The demodulator modeled on the analog computer is shown in Figure 2-12.



*COMPLEMENT OF TRANSMIT
PARTIAL RESPONSE FILTER
IN QPR MODE

Figure 2-12. Demodulation Model

Phase detection of the modulating signal was simulated by using analog quarter square multipliers to multiply the received IF and phase locked reference to recover the baseband signal. Low-pass filters for the I and Q baseband data streams were mechanized similar to those described in Section 2.1.1. These filters, partial response for QPR and full response for QPSK, filter out spurious components resulting from multiplication, leaving the difference frequency which is the baseband. These filtered baseband signals drive the data estimation circuits and cross channel I and Q multipliers. Data slicers for the data estimation and data recovery circuits were mechanized using analog comparators to determine upper, lower, and center for QPSK. Baseband adaptive threshold circuits were programmed on the analog computer and used to optimally determine slicing levels for threshold detecting either QPR or QPSK. The hard decisions from the data estimations of the I and Q basebands were +1, 0, -1 for QPR. Cross-coupling contamination products were obtained from the multiplication of the filtered baseband I and Q signals and an estimation of their value. The resulting signals were differenced using a summing amplifier on the analog computer and filtered by the appropriately selected narrowband and wideband PLL filters.

The optimum slicing level for data recovery, carrier recovery and the data clock is maintained using an adaptive threshold circuit. The system diagram for this circuit is shown in Figure 2-13 and the analog mechanization is shown in Figure 2-14. In the presence of noise and/or a fading channel the adaptive threshold derives an optimum

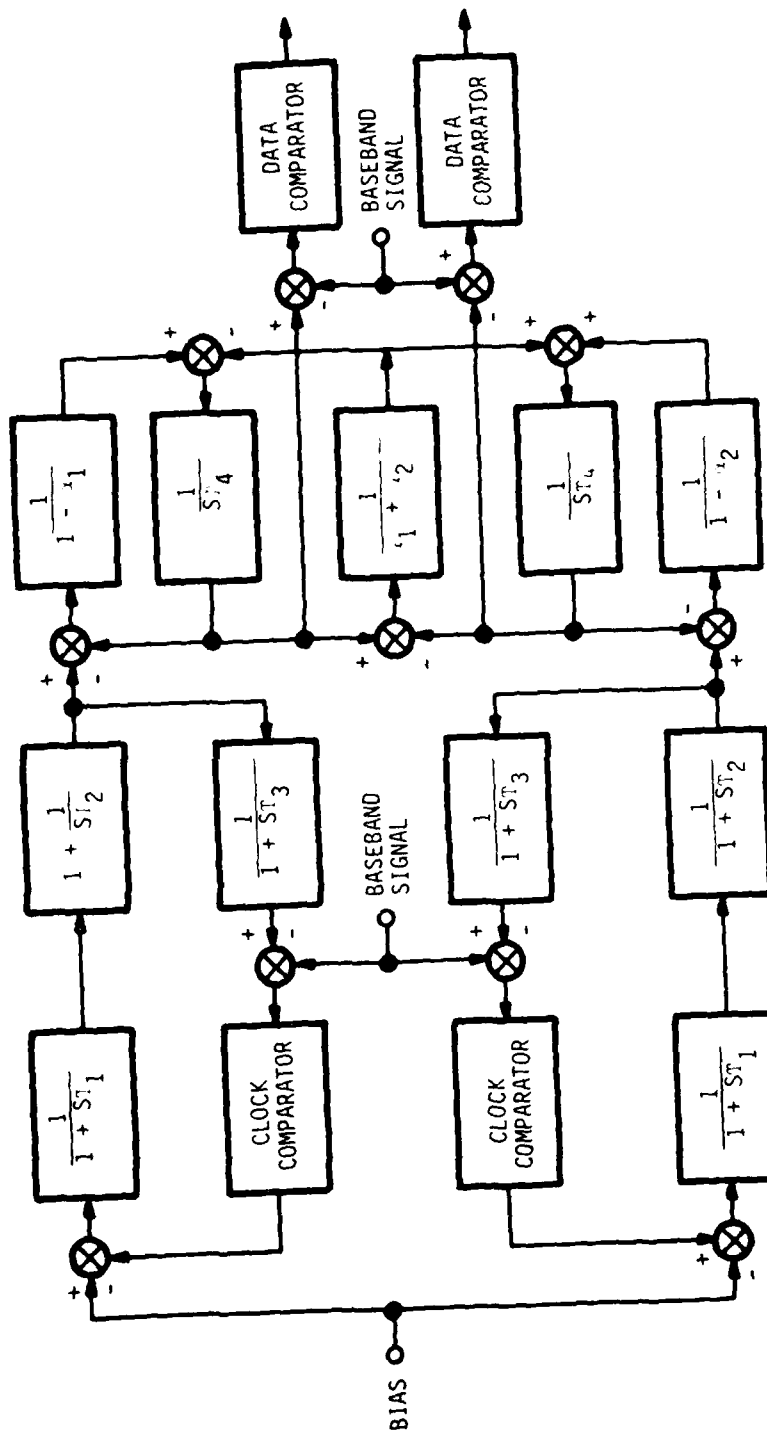


Figure 2-13. Adaptive Threshold Simulation Diagram

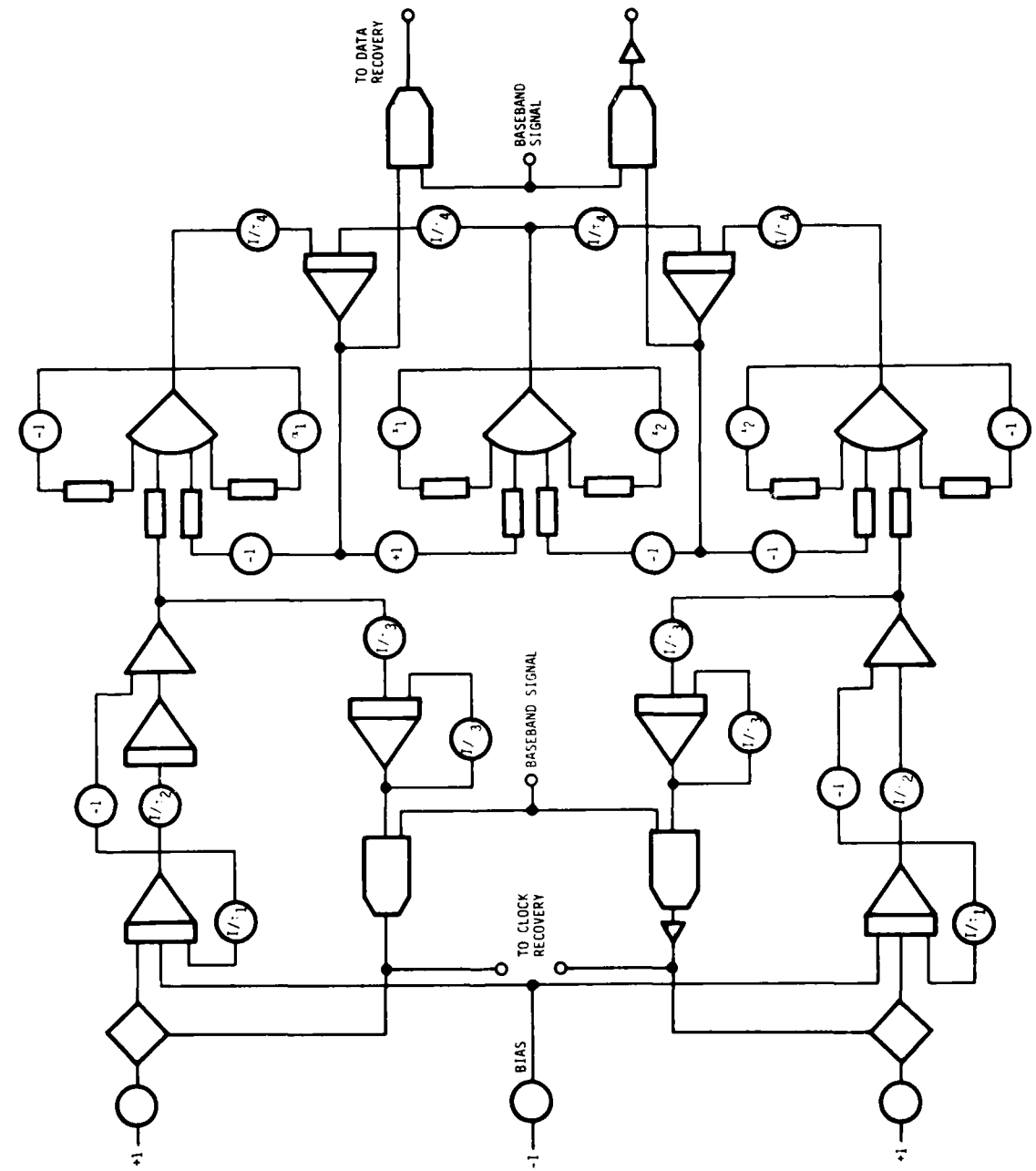


Figure 2-14. Analog Simulation of Adaptive Threshold

slicing level by maintaining on an average a 50 percent duty cycle for the recovered clock.

The analog mechanization of the adaptive threshold was determined using reasonable approximations, of the system circuitry, except for the highly coupled section that determines the data recovery slicing levels. This modernization is based upon the actual circuit equations, thereby assuring that affects of the coupling are accurately simulated.

The narrowband, crutch, and wideband filters were simulated as one composite filter whose time constants were controlled by the acquisition/lock detector. These filters were mechanized using analog amplifiers, electrically controlled switches, and attenuators. Nominal time constants and gain for the wideband filter were $T_1 = 29.53$, $T_2 = 0.5484$, and $A = 30.42$, and for the narrowband filter were $T_1 = 5958.8$, $T_2 = 4.178$, and $A = 26.83$. The crutch filter had time constants $T_1 = 261.12$ and $T_2 = 12.27$. The simulation of the composite filter is shown in Figure 2-15.

2.1.7 TWO- AND THREE-LEVEL DETECTION

To accommodate either QPSK or QPR required both two-level and three-level detection of the baseband data. For QPR each of the demodulated I and Q baseband signals was input to the adaptive threshold circuits and combined with slicing level coefficients to form the upper and lower slicing levels. These slicing levels and the baseband signals were input to comparators for detecting the presence of +1, 0, and -1 data from the demodulated baseband signals. For QPSK, the slicing coefficients were set to zero, and only the upper comparator is used to detect

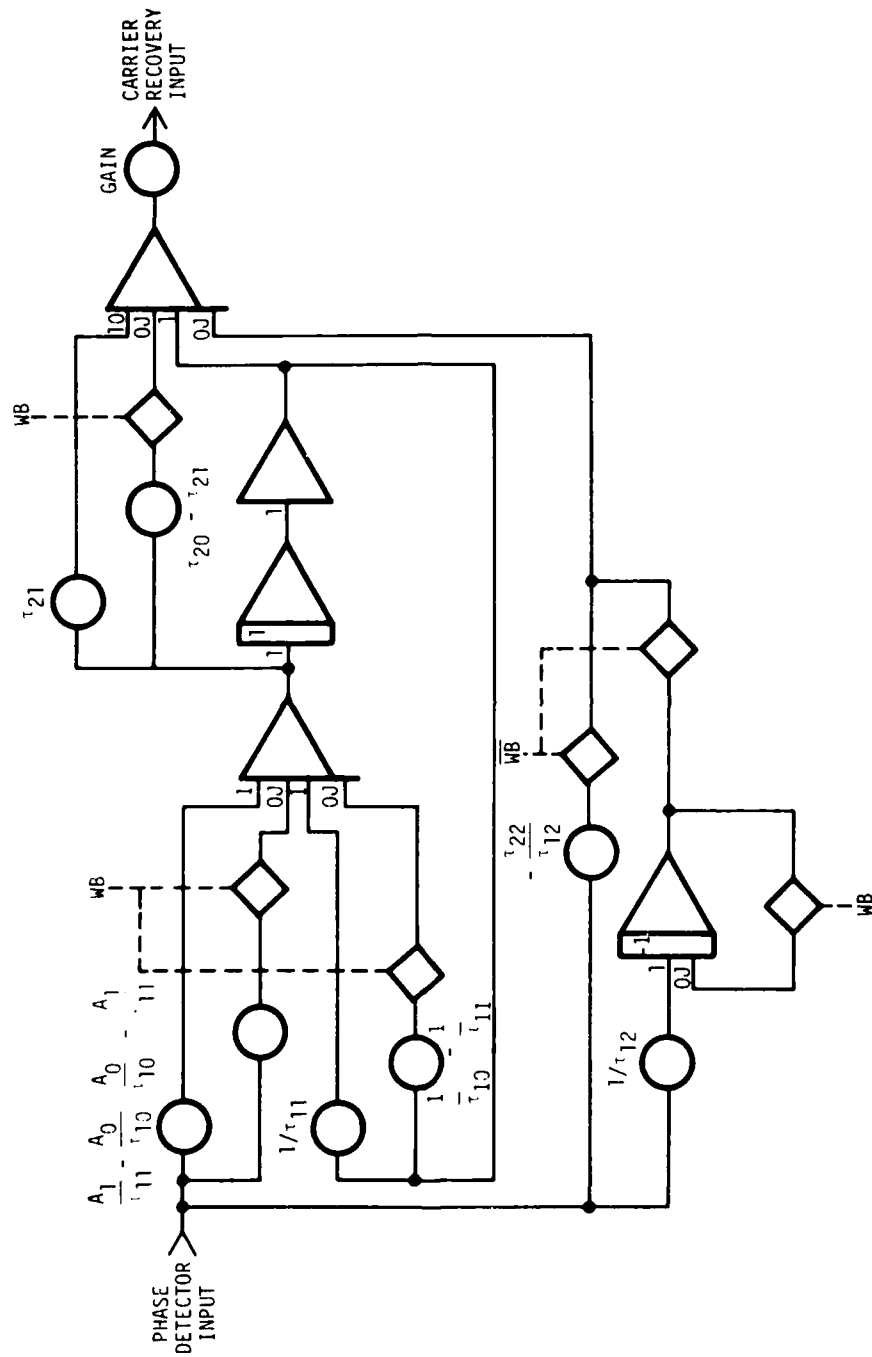


Figure 2-15. Carrier Recovery PLL Filter - Analog Simulation

the binary baseband +1, and -1. Nominally, slicing levels are set to 60 percent of peak amplitude of a baseband signal to obtain optimum detection.

2.1.8 RECEIVER CLOCK RECOVERY

The bit timing recovery circuit provides synchronization for the data recovery circuits. Separate clocks are recovered for each of the two baseband signals I and Q.

The clock comparators compare the baseband signals to threshold slicing levels which are derived from the plus and minus peak detectors. This comparison provides an indication of data transitions. These data transitions are exclusively or'ed with the clock outputs to produce phase error signals. These signals drive D/A switches whose outputs are input to the phase detector amplifiers. The transfer function of the phase detector amplifier is given in Figure 2-16.

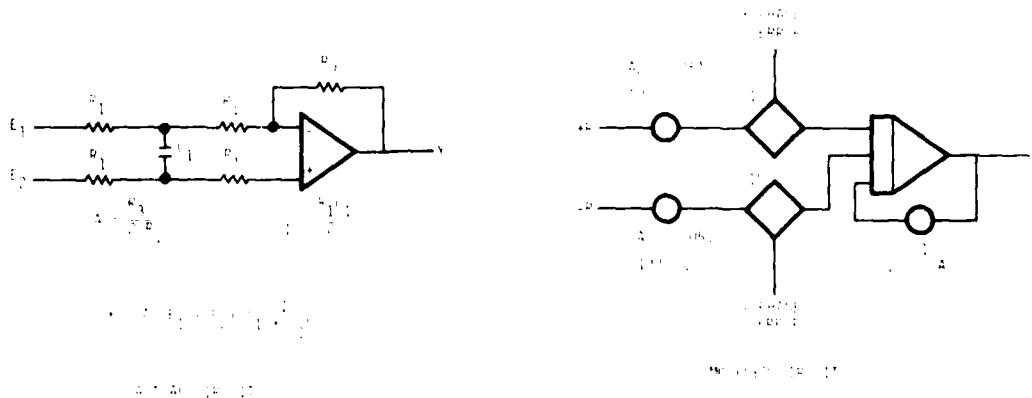


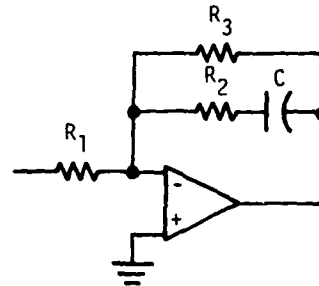
Figure 2-16. Clock Phase Detector Amplifier Model

The outputs of the Phase detector Amplifiers are processed by narrowband Type 2 second order filters if the carrier is in a lock state. When the carrier is in acquisition mode, a wideband Type 1 filter is electronically selected. Nominal time constants for these filters are for narrowband $T_1 = 146.2$ and $T_2 = 47.0$ and for wideband $T_1 = 47.47$ and $T_2 = 1.295$ with a gain, $A = 100.56$. Transfer function and circuits for these filters are shown in Figure 2-17.

The A clock output and B clock output are exclusively or'ed to provide an indication of clock synchronization. This signal drives the Sync Amplifier. When the output of the Sync Amplifier is above a set threshold a LOCK signal is produced by a difference amplifier. This LOCK signal controls the selection of wideband or narrowband clock recovery PLL filters discussed above.

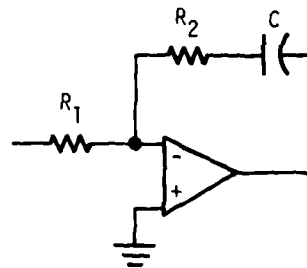
The outputs of the clock recovery PLL filters are applied to the A and B clock VCO's, which drive the VCO's into frequency and phase lock with the recovered clock. A block diagram of the clock recovery loop is shown in Figure 2-18.

$$H(s) = \frac{R_3}{R_1} \left[\frac{1 + sR_2C}{1 + s(R_2 + R_3)C} \right]$$



WIDEBAND, TYPE 1, SECOND ORDER IMPROVED

$$G(s) = \frac{1 + sR_2C}{sR_1C}$$



NARROWBAND, TYPE 2, SECOND ORDER

Figure 2-17. Clock Recovery PLL Filter Models

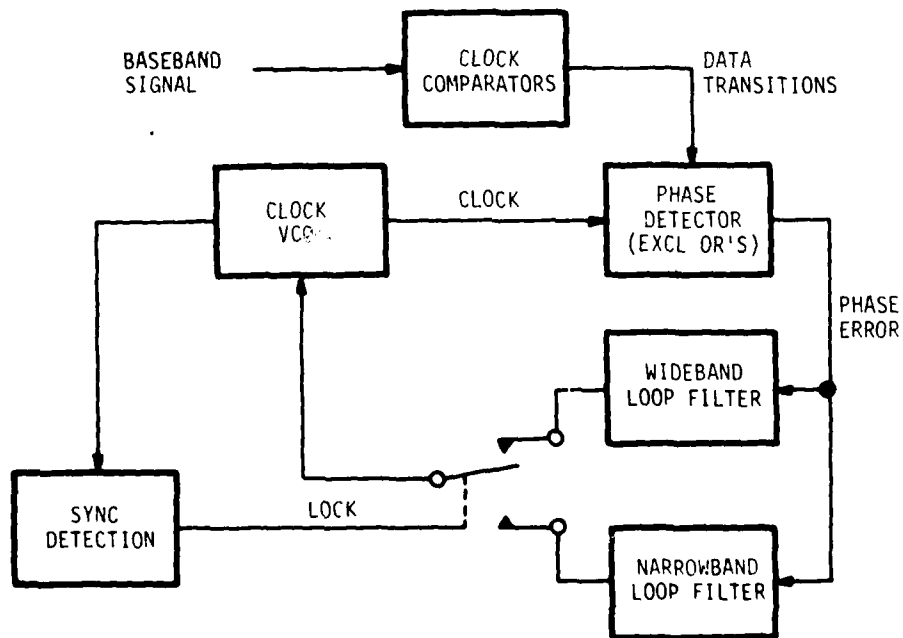


Figure 2-18. Clock Recovery Loop Diagram

2.1.9 AN/FRC-170(V) SIMULATED PERFORMANCE

Bit error tests have been run using additive noise and two ray stationary tap channels. These tests were used to verify receiver performance and obtain data for various signal-to-noise ratios. These simulations have been compared to theoretical and to Government provided data from the prototype radio. Level I (QPSK) and Level II (QPR) performance data taken from the simulation is compared to theoretical and prototype data in Figures 2-19 and 2-20.

Both the radio and simulation are degraded from the theoretical performance for QPR and QPSK due to implementation loss. Other degradations and offsets at the higher signal to noise ratios in the simulation performance curve are due to a limited number of samples taken for the higher ratios. For example an expected error probability of 10^{-5} would require the simulation of 10^6 bits. At the simulated rate of 10^3 BPS, this would take 1000 seconds. The data presented in this report was run for 200 seconds. Other tests have been run for longer periods of time to verify that a nearly fixed offset is obtained over the signal to noise ratios of interest.

Analog stripcharts showing typical channel envelopes, bit errors, AGC control voltages, and adaptive thresholds with respect to time for an E_b/N_o additive noise channel and Rayleigh fading are shown in Figures 2-21 and 2-22.

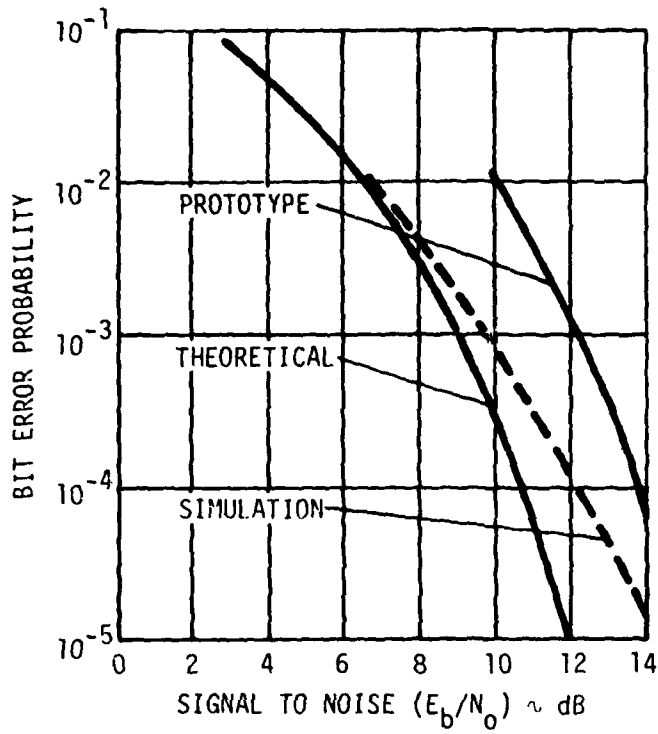
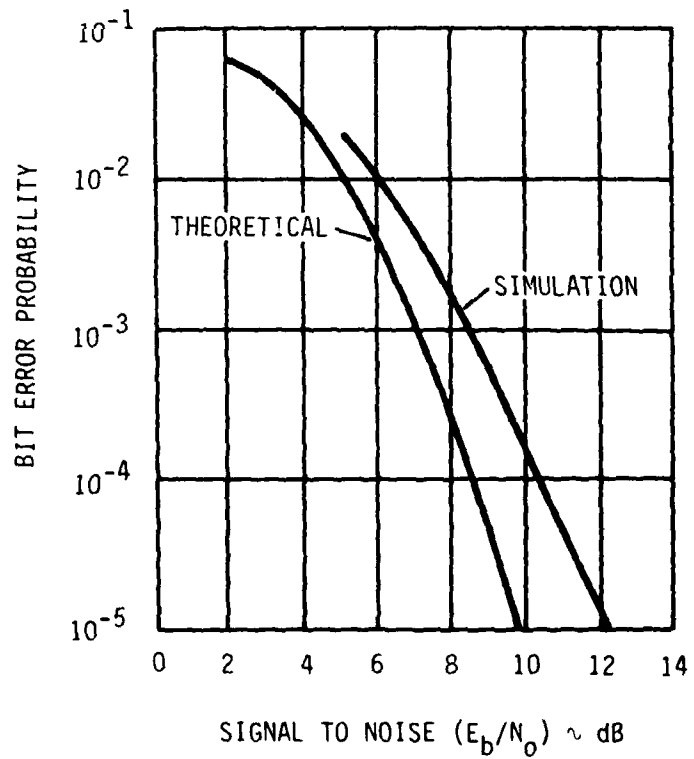


Figure 2-19. Simulated AN/FRC-170 QPR Mode Performance under Additive Noise Conditions

Figure 2-20. Simulated AN/FRC-170 QPSK Mode Performance under Additive Noise Conditions



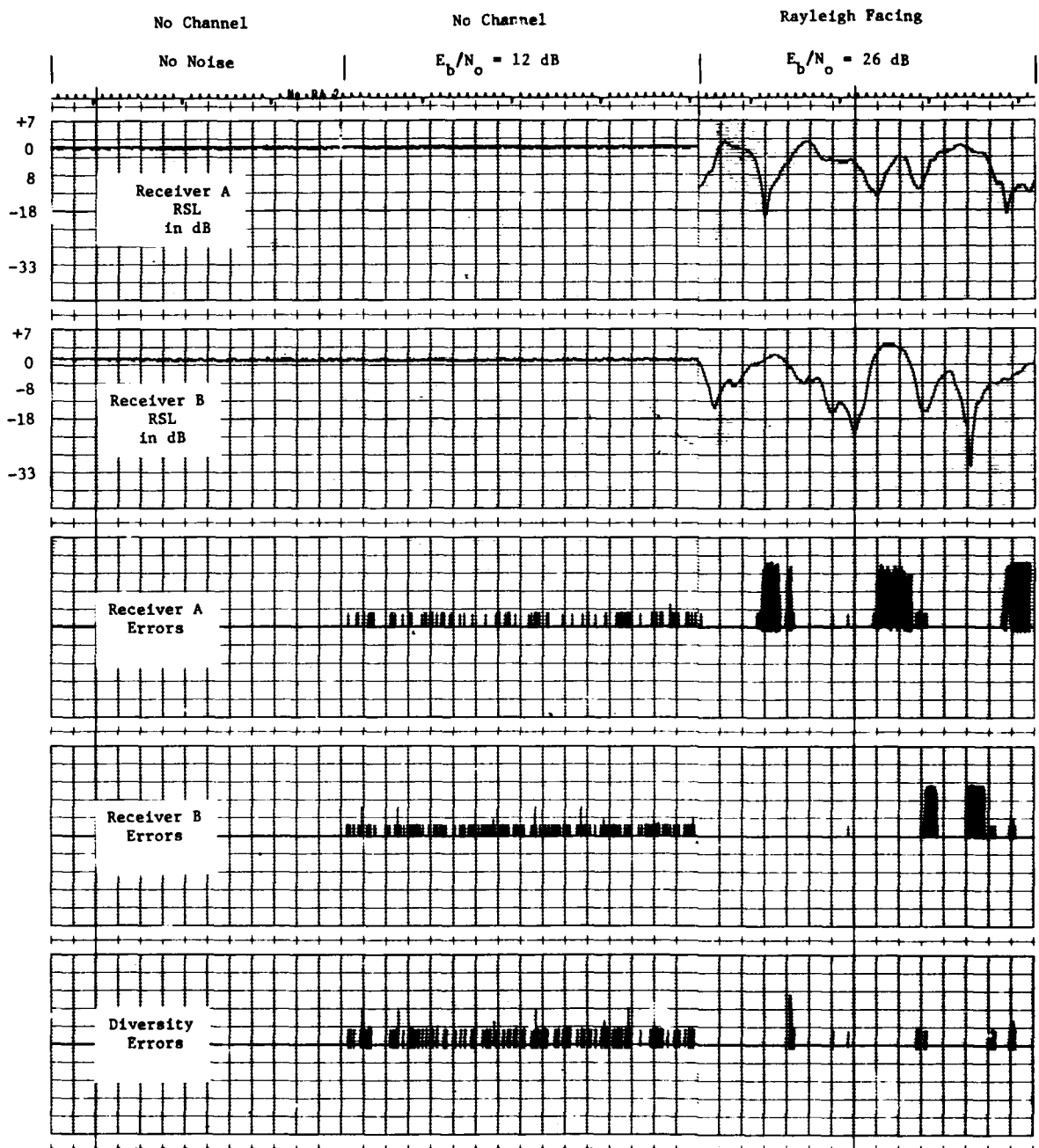


Figure 2-21. Analog Stripchart Recordings for QPR Configuration

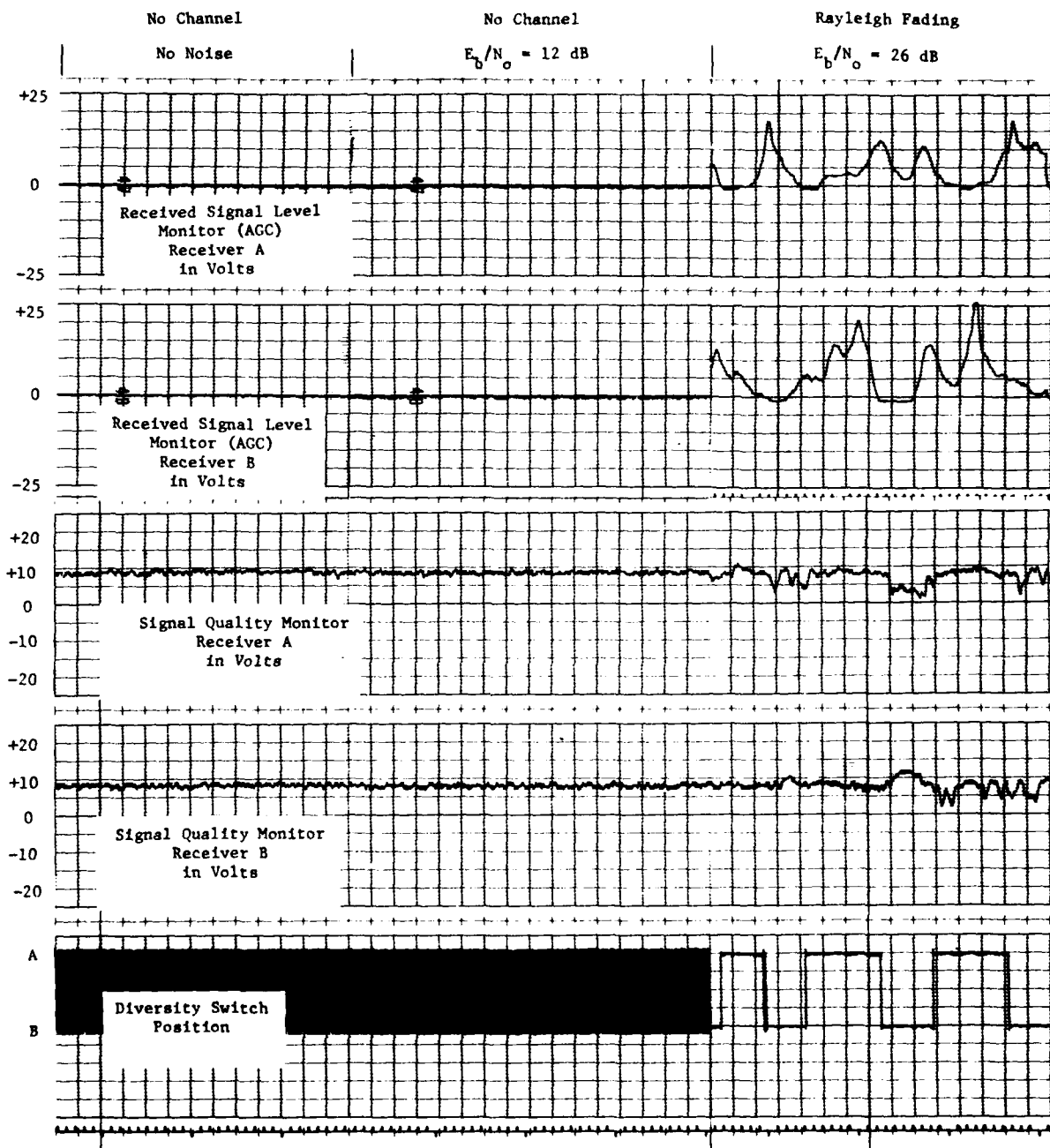


Figure 2-22. Analog Stripchart Recordings for QPR Configuration

During the next phase of this study tests will be made with the LOS frequency selective fading and Rayleigh fading channels. Simulated Rayleigh performance for QPR will be compared to the theoretical performance calculated by:

$$P_e = 3/4 \left[1 - \frac{1}{\left(1 + \frac{16}{\pi^2 (E_b/N_o)} \right)^{1/2}} \right]$$

and plotted in Figure 2-23.

Appendix B of this report contains examples of the remote user's simulation controls and displays for the AN/FRC-170(V) Hybrid Computer Simulation. These examples include tabular bit error data, plots of performance variables, user control menus and hard copy outputs from the Tektronix CRT depicting system configuration and system responses.

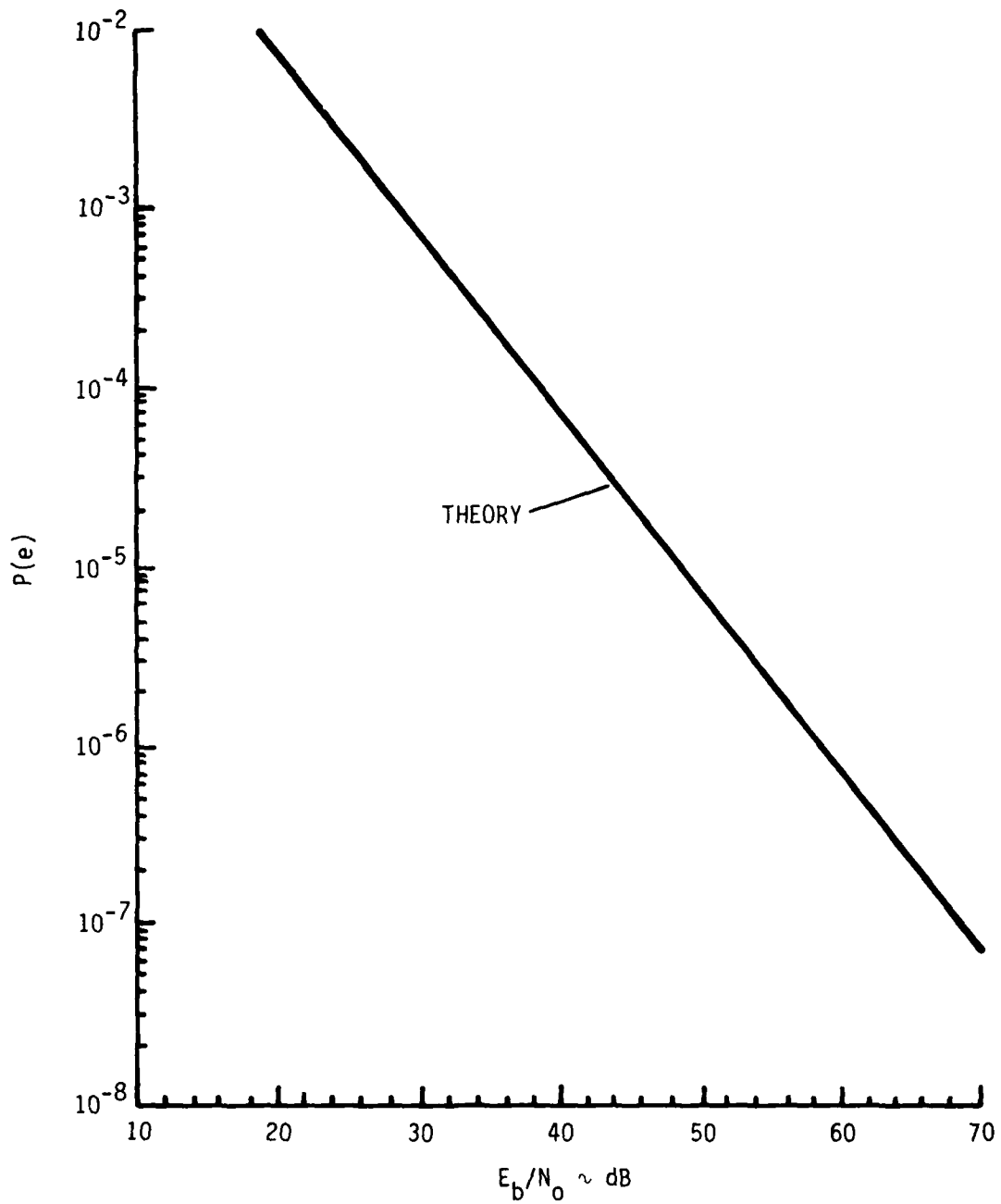


Figure 2-23. Theoretical Rayleigh Fading Performance for QPR Transmission under Additive Noise

3.0 DIVERSITY COMBINER AND SIGNAL QUALITY MONITORS

This section describes and discusses the models and simulations designed to provide a switched dual diversity combiner, psuedo error signal quality monitor and linear RSL monitor. Each monitor can be used to control the diversity switch and may be combined with the other monitor or future monitors in an algorithm to determine switch position.

3.1 RECEIVED SIGNAL LEVEL MONITOR

The receiver IF amplifiers are each supplied gain control multipliers at their outputs. These multipliers are driven by amplified analog signals derived from the filtered output of the AGC circuit. Using the output of this filter to drive a log function preloaded in the MFTP, a linear indicator of the received signal level (RSL) in dB is generated.

This linearity has been tested and is linear within ± 1 dB. The RSL monitor bandwidth may be varied from .001 Hz to 10 Hz by the simulation user.

When using RSL as the diversity driving function, the difference between RSLA and RSLB is tested. If the absolute value of this difference is greater than an operator chosen threshold (Th_2), then the receiver with the greater signal level is chosen. If the difference is less than Th_2 , no change in switch position is made. Th_2 is nominally set at 6 dB.

3.2 IMPROVED SIGNAL QUALITY MONITOR

The improved signal quality monitor is composed of two subsystems. They are the offset threshold monitor and the pseudo error counter.

The offset threshold monitor compares the baseband signal pulse amplitudes to user set acceptance ranges that are a percentage of the peak signal level. If the pulse amplitude at the time of sampling is outside of this acceptable range, then a pseudo error pulse is generated. This is shown in Figure 3-1.

α , which defines the psuedo error band, is determined by the simulation user. The Offset Threshold Monitor (OTM) user option requests the desired α from the user. This program calculates and changes the threshold levels to match the user selected α .

Threshold levels are calculated as follows:

The α given by the user is a percentage of peak pulse amplitude. This percentage is the width of an error band centered around one half of the peak value. The remaining percentge of peak amplitude is K , where $K = 1.0 - \alpha$. The lower threshold value is Peak multiplied by $\frac{K}{2}$. The upper threshold Peak is multiplied by $(1.0 - \frac{K}{2})$. This is shown in Figure 3-2.

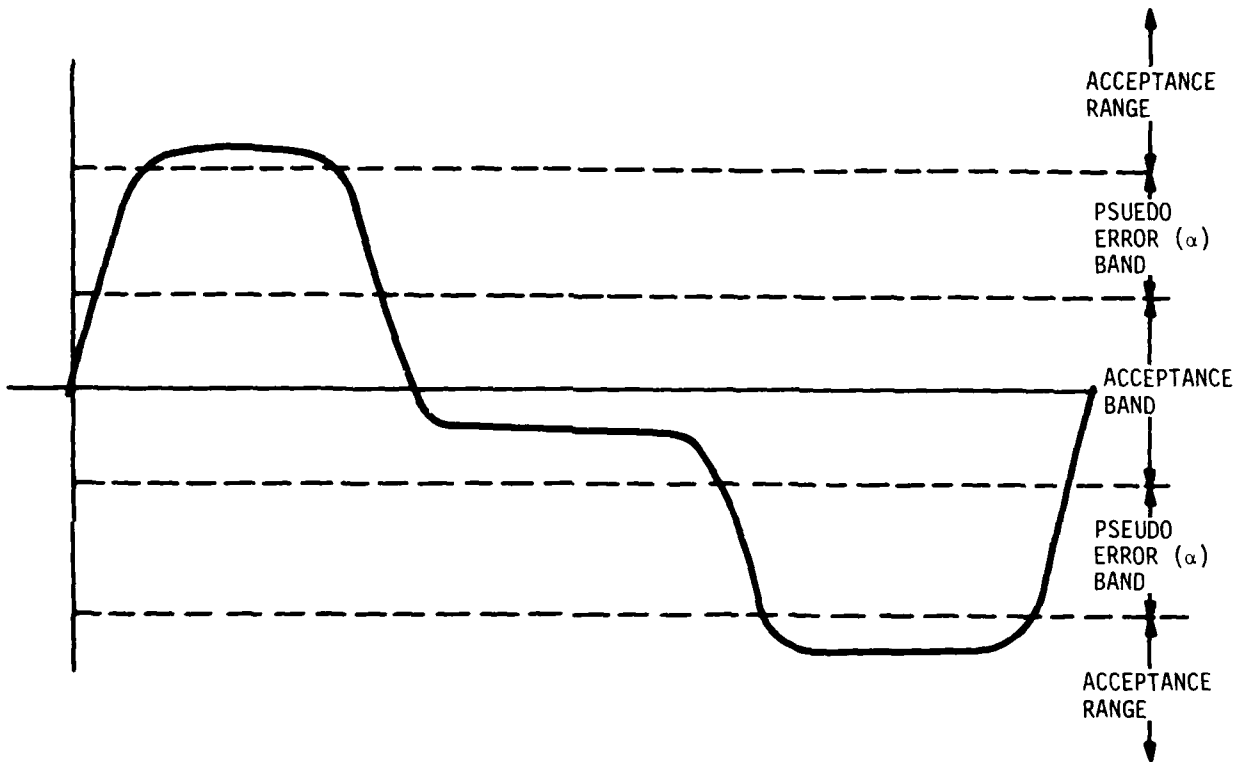


Figure 3-1. Baseband Threshold Levels

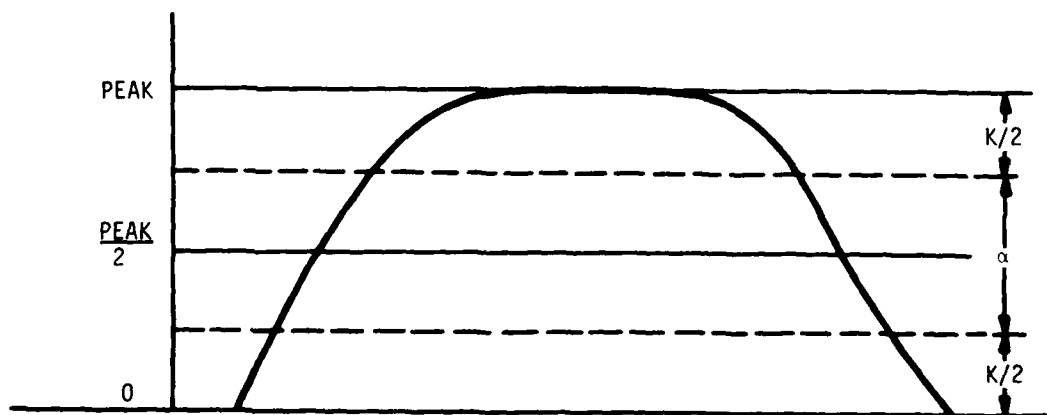


Figure 3-2. Threshold Levels for Offset Threshold Monitor

The hybrid circuitry for the offset threshold monitor is composed of comparators and logic as shown in Figure 3-3.

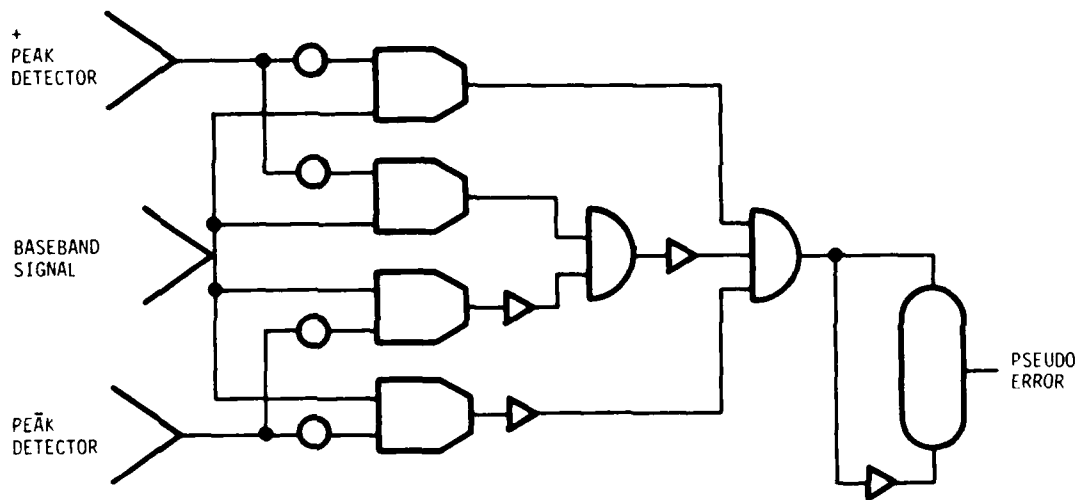


Figure 3-3. Offset Threshold Monitor Simulation

Inputs to the improved signal quality monitor are the A channel and B channel pseudo errors generated by the OTM. The diversity decision is based on the output of a digitally programmed up/down counter. The counter is initially loaded with one half of its maximum count. The counter then counts up on each A channel pseudo error and counts down on each B channel pseudo error. If the counter underflows the diversity switch is set to A channel, an overflow causes the switch to change to B channel. This is shown in Figure 3-4.

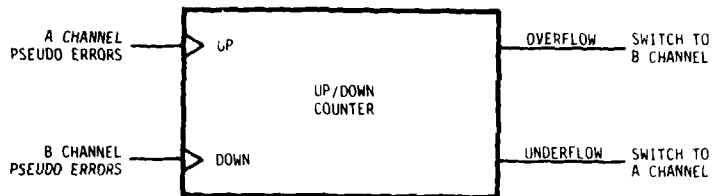


Figure 3-4. Pseudo Error, Improved Signal Quality Monitor

The current counter size of the monitor is seven bits (maximum count = 128_{10}). A user option to change the counter size is being added that will allow a count up to 14 bits. A diversity decision flow chart is given in Figure 3-5.

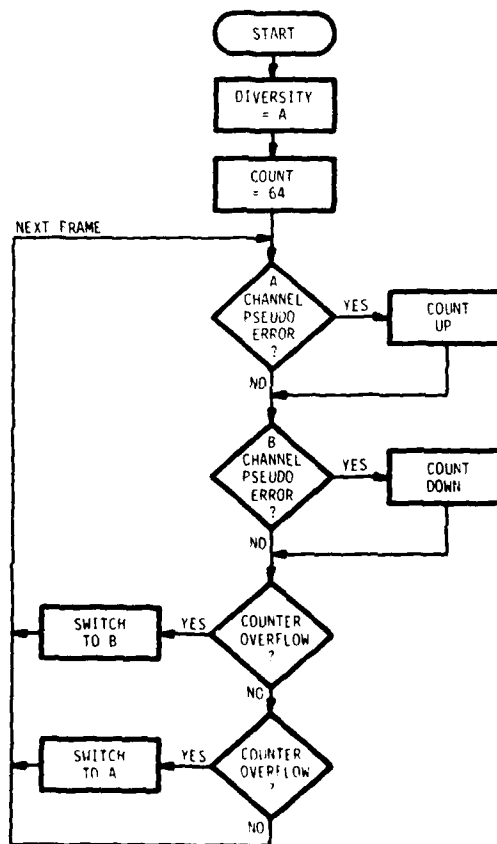


Figure 3-5. Diversity Algorithm for Pseudo Error Signal Quality Monitor

3.3 IMPROVED DUAL DIVERSITY SELECTION COMBINER

In the improved diversity selection algorithm two performance monitors are available as diversity driving functions. The available driving functions are received signal level (RSL) and improved signal quality monitor (SQM).

Selection of the driving function is made by the simulation operator. Decisions made by the algorithm are dependent upon choices of threshold values also made by the operator.

The algorithm for the improved dual diversity selection is given in Figure 3-6.

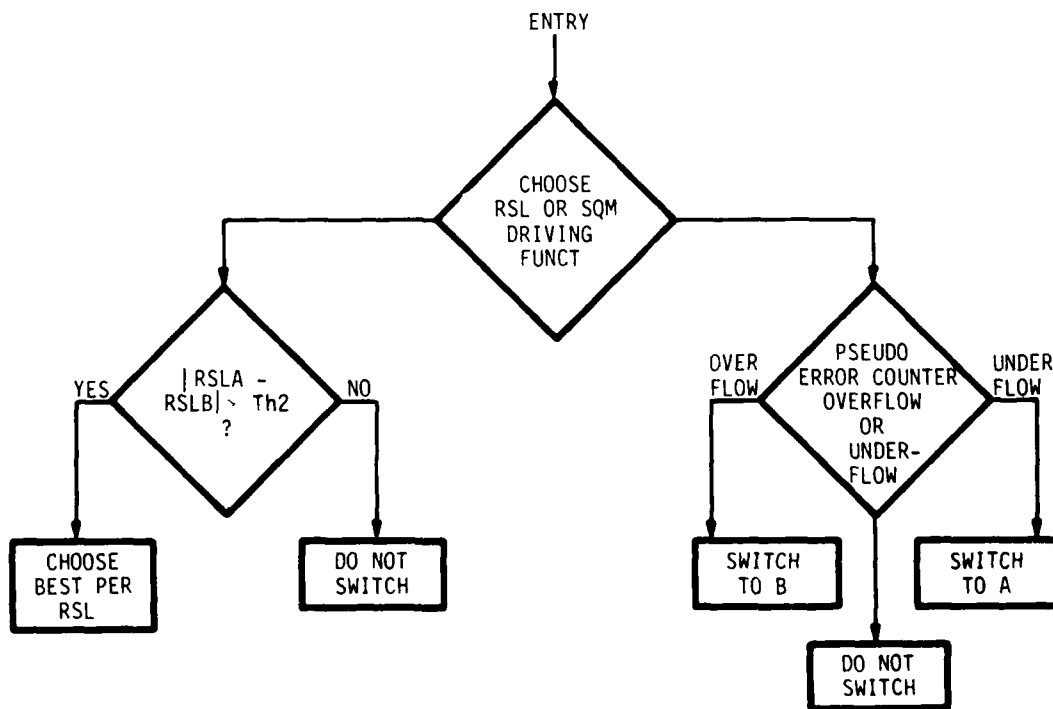


Figure 3-6. Diversity Combiner Algorithm

4.0 INTERACTIVE DISPLAYS AND CONTROLS

Interactive display and control programs have been developed for the hybrid simulation of AN/FRC-170(V) digital LOS radio equipment. These digital programs and subprograms allow the remote terminal user to interface with the Martin Marietta hybrid computer simulation system by means of remote hybrid terminal at DCEC. This versatile group of programs permits the remote terminal user to alter the system configuration, change system parameters, test and verify system elements, and yield sufficient data to make analytical evaluation of transmission system performance.

A Dispatch Operation System has been designed that gives the remote terminal user the full flexibility of a hybrid program operator. Requests to the Dispatch Operating System provide access to all program options. All interacting programs are under the digital computer's control, hence are automatically integrated into the system.

Input to the Dispatch Operation System is through the Tektronix graphic input terminal, and the output of the system simulation is to that terminal in the form of graphic and tabular data, and to the eight-channel stripchart recorder. The problem variables are all available for output to the eight-channel stripchart recorder. Two preset variable lists can be arranged at the time of operation such that the user

may select either set. Other variables may be selected at any time to replace one or more of those in the preset lists.

4.1 DISPATCH OPERATING SYSTEM

The Dispatch Operating System is entered by the input command OPTN. Receipt of this command gives a list of options available to the user. The first list is a broad classification list, and selection of the option number requested yields a more specific list of options. The selection of one of these options causes either execution of that option or the request for necessary data and subsequent execution.

The other means to change parameters and control the transmission simulation is through the argument list method. This software accepts input in the form

ARGUMENT 1, ARGUMENT 2, ... , COMMAND

The argument list is a list of parameters necessary to satisfy the command. If an error occurs, or an insufficient number of arguments is supplied, the program will request those it needs.

4.2 FILTER ALTERATION OPTION

The filter alteration program is a hybrid technique that provides the user with the capability of changing the two transmitter RF bandpass filters and the two receiver IF bandpass filters. The user may select a Butterworth, Bessel, or Chebychev characteristic and the order of the filter, and specify its center frequency and bandwidth. If the Chebychev filter characteristic is selected, the user supplies the computer with the ripple factor in decibels. These parameters are entered into the system as responses to questions asked by the computer.

The approach taken computes the low-pass filter prototype and converts it to a bandpass filter. The roots of Butterworth low-pass filter and Bessel low-pass filter are found by table lookup. The K roots of the low-pass prototype are converted to the 2K roots of the bandpass filter, using a low-pass transformation. If the Chebychev characteristic option is selected, the roots derived for the Butterworth low-pass filter prototype are altered by applying an algorithm based on the ripple factor, S as given below.

$$\epsilon_p = (10^S - 1)^{-1/2}$$

$$a = [(\epsilon_p^2 + 1)^{1/2} + \epsilon_p] / n$$

$$\tanh(a) = \frac{a - 1/a}{a + 1/a}$$

$$\cosh(a) = 0.5(a + 1/a).$$

The $\cosh(a)$ term is the normalized 3 dB cutoff frequency for the Chebychev characteristic filter. The $\tanh(a)$ term is multiplied by the real term. Thus, the chebychev roots are

$$r_K = \cosh(a) (-\tanh(a)\sigma_K + j\omega_k).$$

The coefficients for the transfer function of the bandpass filter are determined from the derived roots. These coefficients scaled properly are the values to which the digitally controlled attenuators are set in the filter mechanization on the analog computer.

The user has the option of running a frequency response test on the filter to verify visually that the filter is set properly. The user responds to questions from the computer to enter the lowest and highest frequencies of interest and the number of points to be tested. The program works by driving the input of the filter with the output from an amplitude-stabilized variable frequency controlled oscillator. The resulting filter output is peak detected, sampled, and stored. This process is repeated for each frequency point until the entire characteristic is stored. The ratio of the filter output to its input is determined in decibels, together with corresponding phase characteristic. The gain and phase characteristics for each frequency point are then printed in tabular form for the user. A Bode plot of the gain characteristic relative to changes in frequency is also displayed graphically.

In addition to the IF and RF bandpass filters, a frequency response test can be made of the baseband filters. The QPR partial response filter frequency response is defined for the total filter. By appropriately combining the transmitter and receiver baseband filters, the complete partial response can be obtained.

4.3 POWER SPECTRAL DENSITY COMPUTATION AND DISPLAY

The Power Spectral Density (PSD) program is a hybrid technique that incorporates an analog PSD circuit (Figure 4-1) that is controlled and sampled by the digital computer.

The analog circuit uses a heterodyne method of Fourier analysis to find the average power between the set oscillator frequency, and

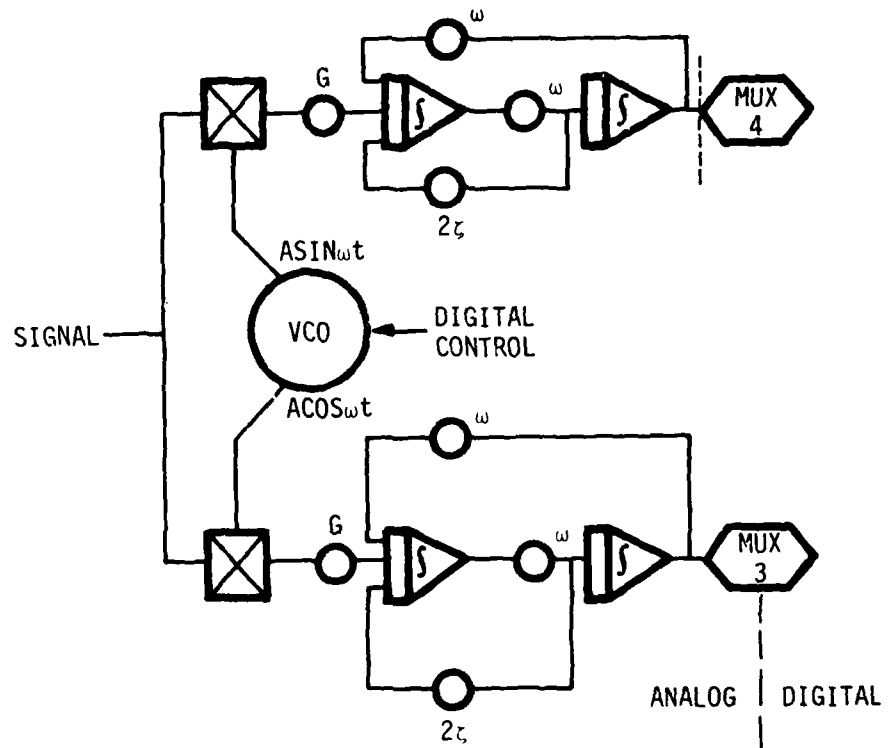


Figure 4-1. Power Spectral Density Analog Circuit

that frequency plus the bandwidth of the PSD filters. The signal to be analyzed is separately multiplied by the quadrature sinusoids of a variable frequency oscillator and filtered to a preset bandwidth. The resulting signals are squared, summed, and averaged to give the average power within the frequency band set.

The remote user is queued as to which signal to analyze: the lower frequency bound, the upper frequency bound, the number of points between those bounds, and the desired bandwidth of the PSD filters. The frequency range is divided by the number of points.

In addition to the spectral occupancy plot, the program displays the upper and lower frequency bounds of the band of frequencies that contain 99 percent of the power. This 99 percent spectral occupancy is determined for the frequency extremes defined previously by the remote user. The frequency at which the center of power exists is also displayed.

4.4 BIT ERROR MEASUREMENT

Both digital and analog computers are used in the measurement, storage, and processing of bit error data for the DRAMA radio LOS simulations. Detection of errors on a bit by bit basis is accomplished by digital processing of analog logic data.

The analog logic data for the transmitter, and both receivers consists of the transmitted and received data, clock status, and ring counter position, along with the diversity switch status. The data received by the digital computer, and a typical ring counter is shown in Figure 4-2.

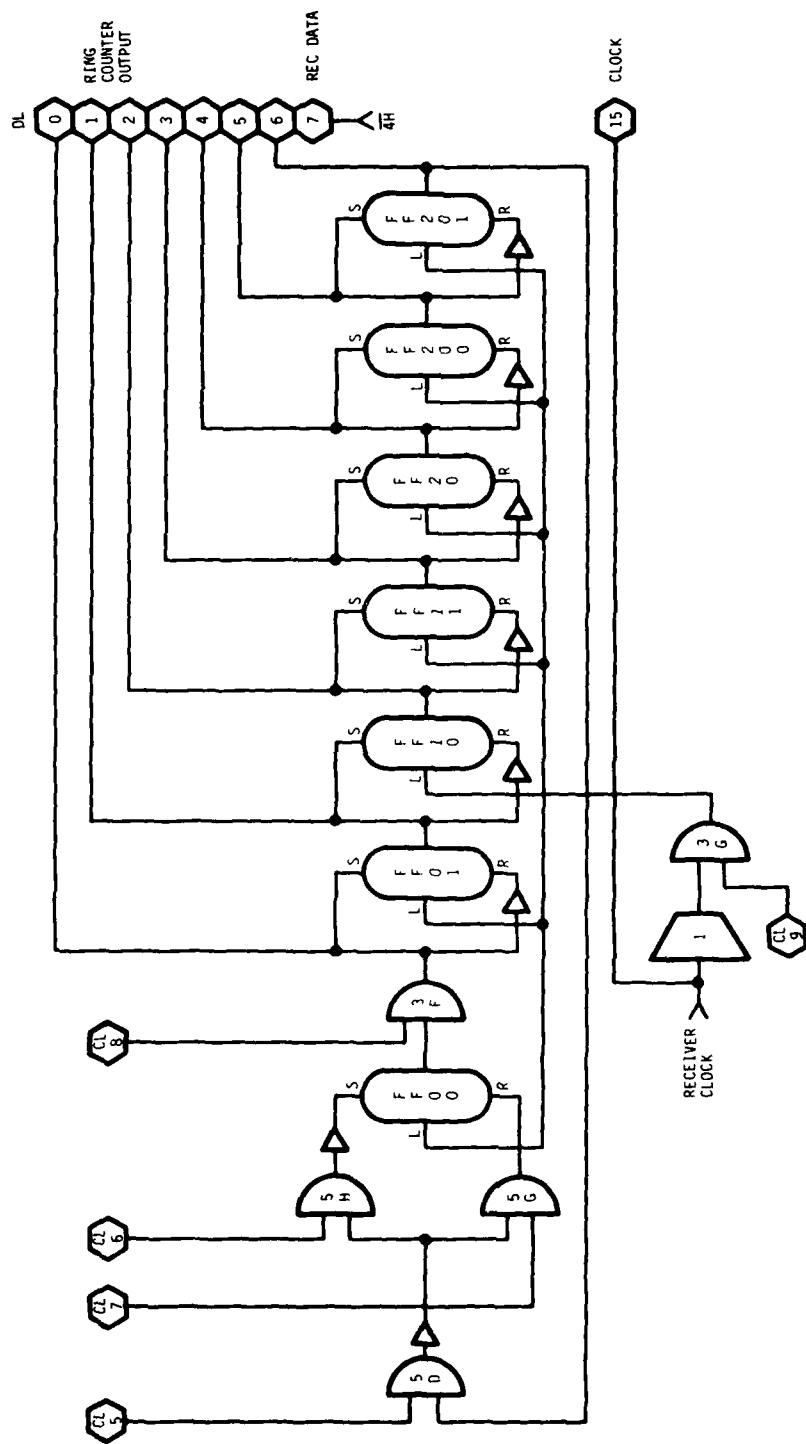


Figure 4-2. Bit Error Ring Counter Simulation

At the start of a bit error test, the channel is set to tap one stationary (the channel out condition), the ring counters are synchronized, and the transmitter and receiver bit streams are accumulated and compared to determine the transmitter receiver bit delay for each receiver.

The channel model selected is then established, the relative positions of the transmitter and receiver ring counters maintains the bit delay between the transmitter and the receiver. The desired noise level is established and the bit error test begins.

At each change of state of the transmitter clock, the data, the ring counters and clock status of the transmitter and each receiver is sampled and stored. The transmitted data is accumulated as each new bit is received, and based upon the bit delay determined through initialization and the relative position of the transmitter and receiver ring counters the correct transmit receiver bit delay is determined and the bits compared. The transmit and received clock status is used to ensure that the data has been received and the ring counters updated.

The bit errors for each receiver and the selected diversity channel are accumulated for the duration of the bit error lost. These accumulated sums are divided by the current number of bits transmitted and are outputted as analog signals available for stripchart recording, thereby forming a continuous bit error rate history. The total bits transmitted, the total errors for each receiver and the diversity channel, along with the respective bit error rates are reported in the Tektronix Terminal at the end of the bit error lost.

4.10 ANALOG USER DISPLAYS

Output of the transmission system simulation is not only made to the Tektronix terminal, but also to the eight-channel stripchart recorder, in the form of analog signals vs. time. The simulation variables are all available for output to the stripchart recorder. A typical set of eight simulation variables to the stripchart recorder are:

- 1 Logarithmic fading channel envelope, Receiver A
- 2 Logarithmic fading channel envelope, Receiver B
- 3 AGC amplitude, Receiver A
- 4 AGC amplitude, Receiver B
- 5 Bit errors, Receiver A
- 6 Bit errors, Receiver B
- 7 Running total of pseudo error counter
- 8 Status of diversity selector.

These simulation variables may be substituted for one or more of the above, such as the outputs of OTM for receivers A and/or B, or phase lock loop voltages of the clock and carrier recovery systems.

4.11 COMMAND MNEMONICS

The use of command mnemonics enables the user to perform the various operations used with the option dispatch system, often in a more efficient manner.

The input command mnemonic is executed either with the return key or with the simultaneous depressing of the CTRL key and an alpha character.

The termination by a CTRL and an alpha character is used as follows, CTRL and:

- B Aborts the current operation and returns the user to the control dispatch system
- S Terminates the updating of a flag or data list
- H Outputs a message depending upon the numeric proceeding its execution. The current list of messages is as follows:
 - None The word HELP is written and the bell tone is sounded. This is repeated five times.
 - 0 Same as none.
 - 1 Pick up the phone
 - 2 Please stand by
 - 3 System needs calibration
 - 4 System is calibrated and ready
 - 5 Will be back at (input time/message)
 - >6 Same as none.
- Other Alpha Not currently used and cause the letters NU to appear and the system returns to the control dispatch system.

The following list of command mnemonics is grouped and listed in the order of their apparent frequency of use.

- OPTN Places the system in the option dispatch mode.
- HELP The word HELP is written and the bell tone sounded. This is repeated five times.

BITE A bit error test is run under conditions input per requested
 input data.

TAP Requests and sets the channel model power profile.

ITS Sets the intertap spacing for the channel model.

CRL Sets the channel correlation coefficient.

PSD A PSD is performed on the device number input, and yields
 a plot of the data.

FLT Sets an RF or IF filter to the type, order, bandwidth and
 center frequency desired.

FRS Takes the frequency response of the device number input.

EYE Requests, takes and plots a baseband eye pattern.

LIS Requests, takes and plots a baseband constellation.

SEL Enables the sampling of signals during the execution of
 a bit error test.

GPH Plots the data stored in a data list between the sample
 numbers of the sample set.

HST Gives the histogram and cumulative distribution of the
 data stored in a data list.

KFL Sets or resets the system flags, to give various options
 to other command mnemonics functions. The return key
 allows the user to stop through the list and the CTRLS
 terminates the operation.

RST Reinitializes the analog computers by setting the operational mode control to pot set, hcl'd, and back to operate.

TSC A time scale of 1.0 or 0.1 is requested and set.

MOD Requests and sets the modulation type desired.

QPR Sets the system modulation to QPR.

QPSK Sets the system modulation to QPSK.

EBN Sets the value of E_b/N_0 to the input value.

CHN Requests and sets the desired channel model. Note, a fading channel is only operative with execution of a bit error lost.

AGC The AGC may be taken out or put in and its bandwidth changed.

OTM Sets the offset threshold monitor slicing level.

DPR Requests and sets the percentage of drive power.

RF The transmitter RF filters may be put in or taken out of the system.

SCR The scrambler may be put in or taken out of the system.

NLI The transmitter non-linearity may be put in or taken out of the system.

DVR Select diversity function, either AGC or SQM.

DATA STORAGE AND MANIPULATION

The command mnemonics DSM, SEL, GPH, MSQ, and HST yield operations that sample and store data and perform various functions on that data. There are eight data storage areas of 5000 words each identified by list numbers 0 through 8. The function of the various commands is as follows:

DSM This is the general/data sampling command, and operates independently of the bit error test. The data storage is limited to 5000 data points. The input request are:

Sample time = .0001

Block No. = 0

No. of Samples = 5000

The sample time is in secs and is limited to a maximum of four secs and a minimum of 0.000050 secs. The block number refers to the AD block to be sampled. All eight AD trunks are sampled and stored in the respective data storage lists.

SEL This selects the data that is to be stored during the execution of a bit error test. The execution requests:

BT No. = 2

Block No. = 0

Run Time = 100

The BT number identifies what data is to be stored. The data may be one or more digital at analog variables.

(Currently only BT number 2 is operational) The block number refers to which of four AD blocks represent the source

of the analog data, for example the channel monitors are on block 0. Runtime is requested to determine how many data items to skip before storing the data. The current mechanization allows for the storage of 10,000 samples each of two variables, sampled each data bit during the execution of a bit error lost. For example a 100 sec run yields 100,000 data bits therefore ten data samples are skipped before one is stored.

MSQ

This finds the mean and the mean squared deviation, and the standard deviation of the data in a list. The requests are as follows:

List No. = 0

First TERM = 1

Last TERM = 10,000

and the return is of the form

MEAN = 0.15155

MEAN SQUARE = 0.00647

STD DEV = 0.08045

GPH

This is the general plot command mnemonic, and will plot the data stored in a list. The input requests are:

LIST NO. = 0

FIRST TERM = 1

LAST TERM = 10000

DATA MAX = 0.5

DATA MIN = 0

Samples of plots obtained with this command are shown in Figures 4-3 and 4-4. The first term, last term allows the user to view the total data set, or any portion of interest.

HST This command forms the histogram and the cumulative distribution of the data stored in a particular list. The requested inputs are:

No. of Bins = 100
Data Max = 0.5
Data Min = 0
First Term = 1
Last Term = 10000

Samples of the outputs from this command are shown in Figure 4-5 and 4-6. The data maximum and minimum, and the first term, last term allow the user to examine various regions of the sampled data. The sample outputs shown are the distributions of the channel monitors.

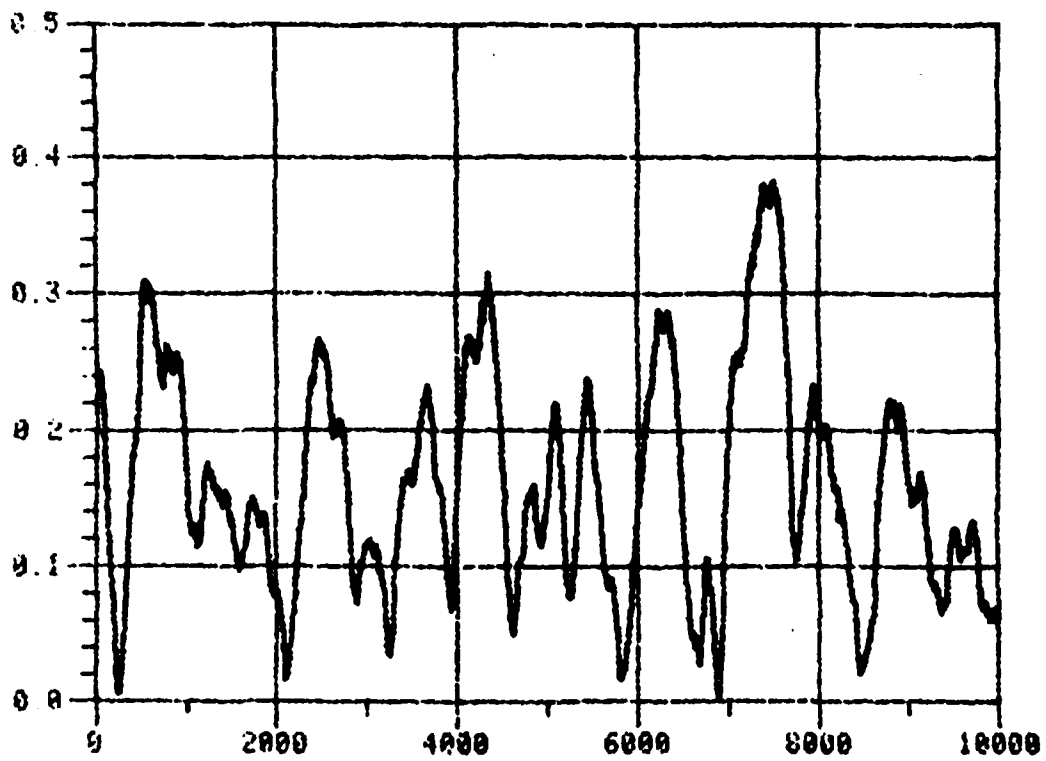


Figure 4-3. Data Storage Sample Plot

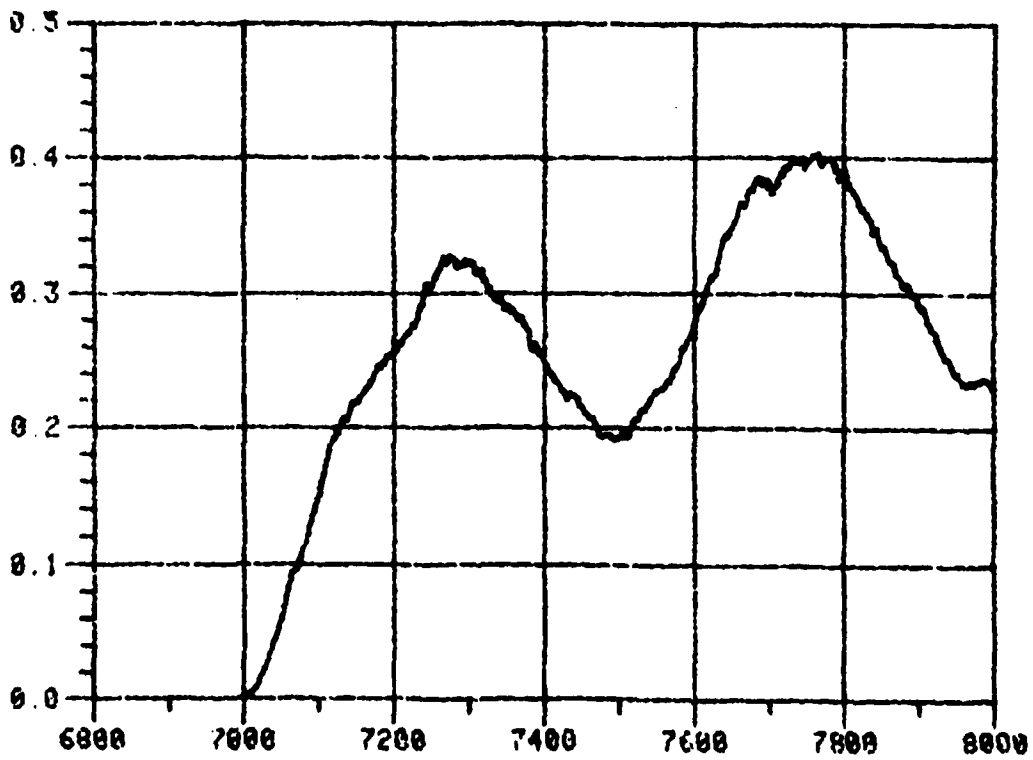


Figure 4-4. Expanded Data Storage Sample Plot

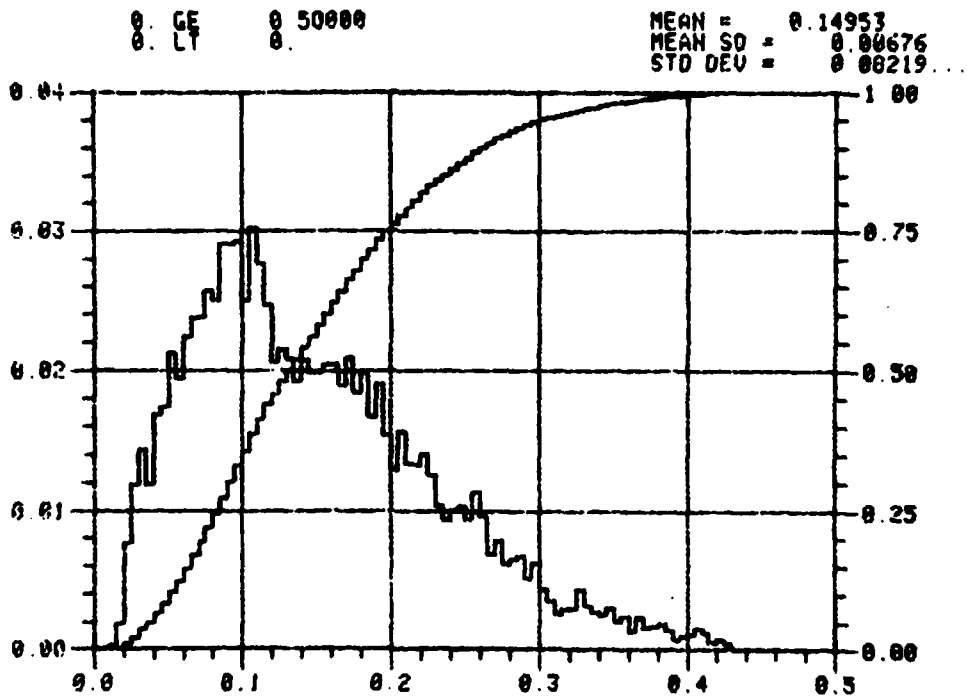


Figure 4-5. Channel "A" Distribution Plot

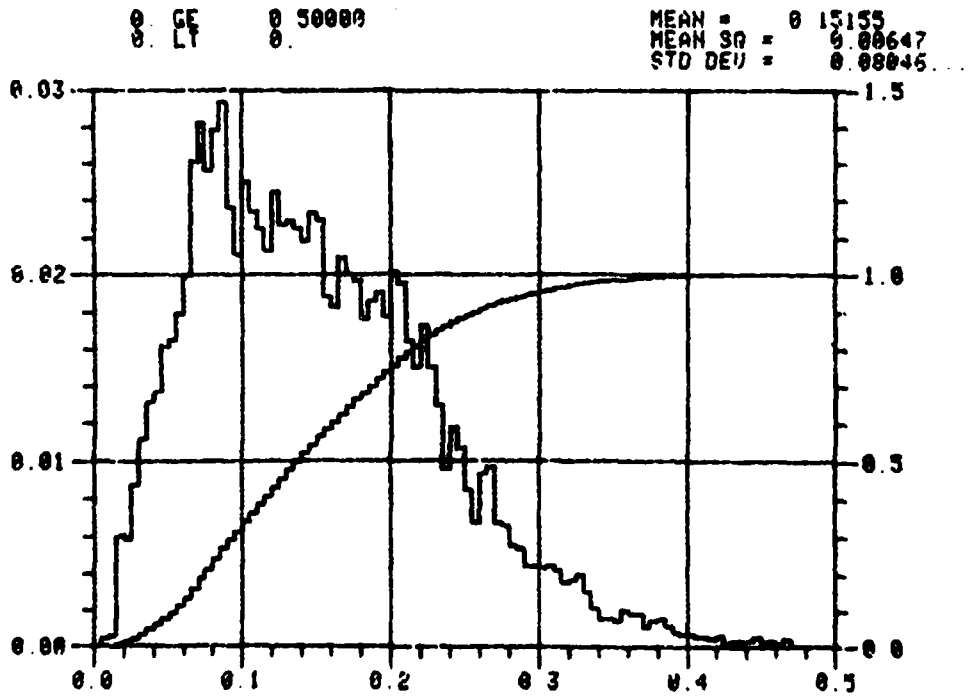


Figure 4-6. Channel "B" Distribution Plot

5.0 HYBRID COMPUTER REMOTE TERMINAL PROVISION

The Computational Sciences Laboratory provides the Defense Communications Engineering Center (DCEC), Reston, Virginia, with an advanced hybrid computer terminal through which they are able to operate and control the hybrid computer simulations developed in this study. This terminal uses two telephone lines and the equipment listed below to provide stripchart analog recordings for eight channels, digital graphical displays, and control of the hybrid simulations at Orlando, Florida.

The terminal equipment loaned to DCEC consists of the following items:

- 1 One Tektronix 4010 Terminal
- 2 One Tektronix 4610 Hard Copy Unit
- 3 One EMR Remote Terminal
- 4 One Eight-Channel Brush Recorder
- 5 One Full Duplex Telephone Modem
- 6 Two 1000A Data Couplers
- 7 One Lafayette RK-725 Cassette Tape Recorder.

The two telephone 1000A Data Couplers supplied by Martin Marietta Aerospace and installed at the DCEC facility at Reston, Virginia, are required as part of this installation to permit interchange of hybrid computer data with Orlando, Florida.

6.0 SUMMARY

Several major changes and additions were made to the AN/FRC-170(V) hybrid computer simulation to provide a simulation of the radio and channel that realistically models actual electronic circuits of the radio and has the capability to model expected channel characteristics. During this phase of the study the simulation was used to obtain performance data for two ray stationary channels with one undelayed and one delayed ray. These tests were run with various E_b/N_o settings via the remote terminal at DCEC. Other tests run during this phase were additive noise performance tests to verify that simulated performance compared favorably with actual prototype radio performance.

Specific accomplishments were the modeling and simulation of a psuedo error technique for measuring signal quality, adaptive threshold circuits for carrier recovery, clock recovery and data slicing, a new AGC technique, a test and display capability to verify the fading distribution for each tap pair in the channel model, and a new diversity switch algorithm for the switched diversity combiner.

The hybrid computer simulation was also provided with the flexibility of two time scales that permits tap delay selection from 2.0 data bits to .02 data bits.

The resulting simulation model of the AN/FRC-170(V) radio and channel has been verified for additive noise channels and numerous

2-tap stationary channels. Tests have commenced to verify system performance for fading channels. The first fading tests to be run were for a Rayleigh fading channel. In running these tests the simulation would cycle slip in both the carrier recovery and clock recovery loops when they were in a narrowband mode. By increasing the bandwidth of the narrowband filters by a factor of 10 for both the carrier recovery and clock recovery loop the simulation successfully performed under Rayleigh fading without cycle slip of the clock oscillator.

Future work will include the modeling and simulation of an IF combiner using an equal gain, equal phase technique, an improved baseband equalizer, two forward equalizers (one using a delay line technique), and proposed product improvements. Improvements to the simulation model will include up and down conversions IF to RF and RF to IF and a data stream which includes the TDM framing pattern. During the next phase of this study various line of sight frequency selective fading channel configurations will be modeled to test simulated AN/FRC-170(V) radio performance. During these tests the various combiners (coherent and switched) and equalizers (forward and baseband) will be evaluated to determine their effects on performance and optimum parameter values.

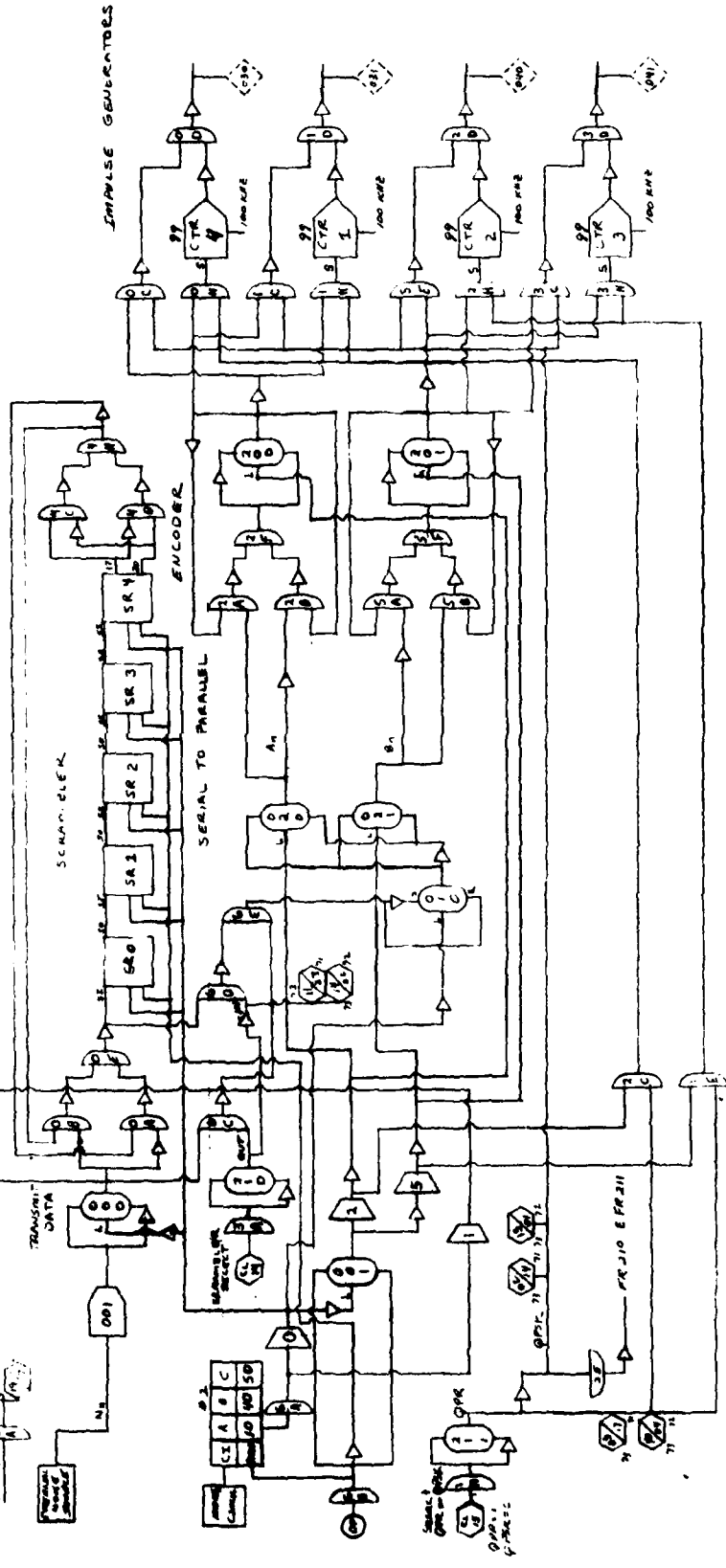
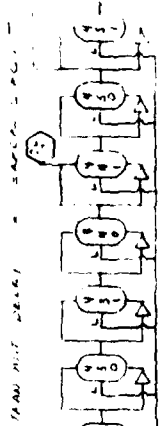
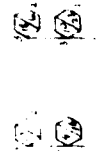
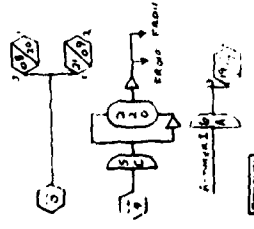
New user controls and displays will be designed and programmed during the next phase of this study to permit the engineer at DCEC using the remote hybrid terminal to configure, change parameters and display outputs from the equalizer and combiner models. Changes to the AN/FRC-170(V) radio effecting performance will also be incorporated

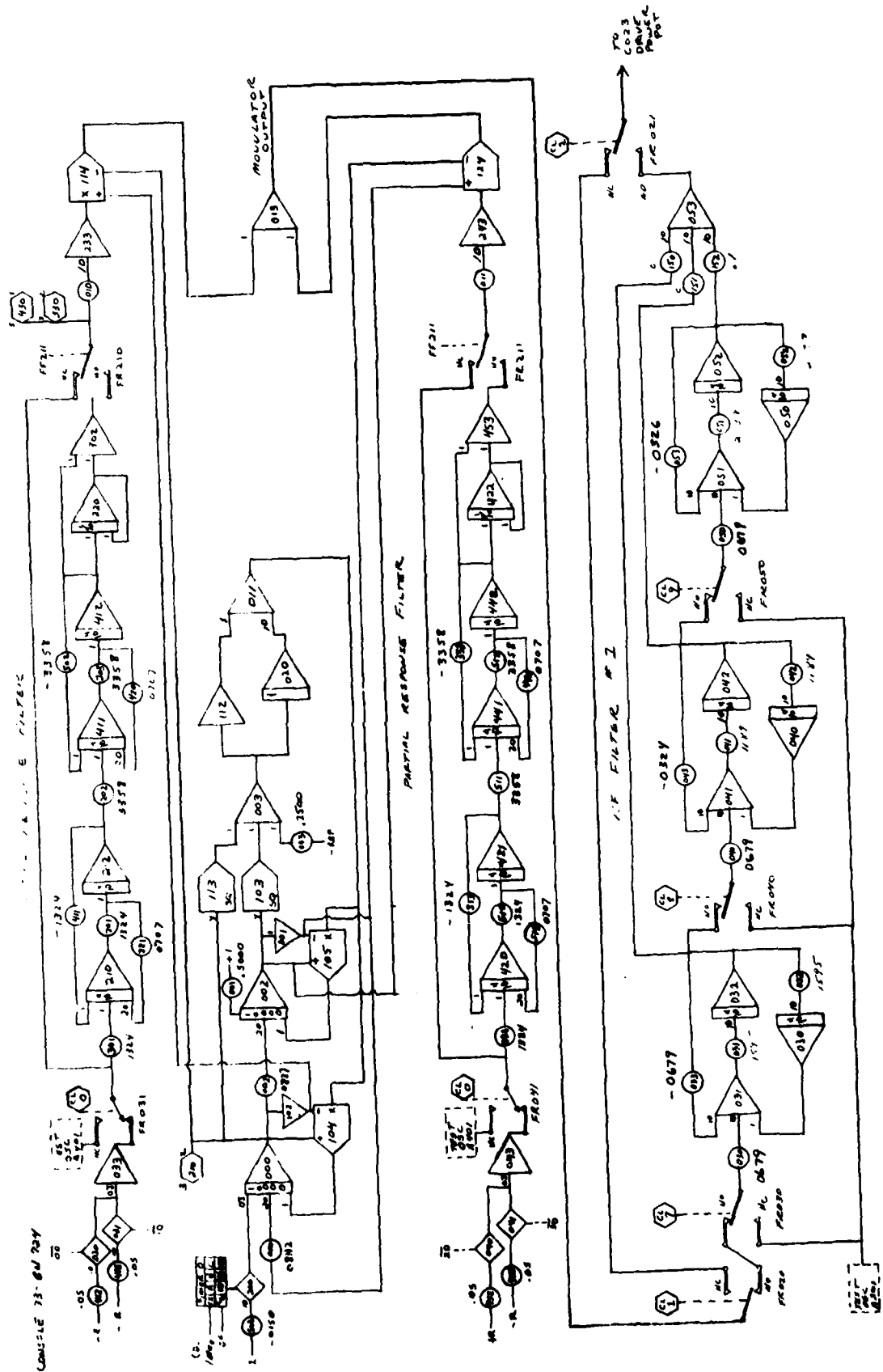
into the simulation model of the AN/FRC-170(V) radio during the next phase of this study.

APPENDIX A

ANALOG COMPUTER DIAGRAMS FOR
AN/FRC-170(V) HYBRID COMPUTER
SIMULATION

100 - E 73 - 60 214
 LOGIC QUANTUM QPE
 ANALOG EQUAL QPE

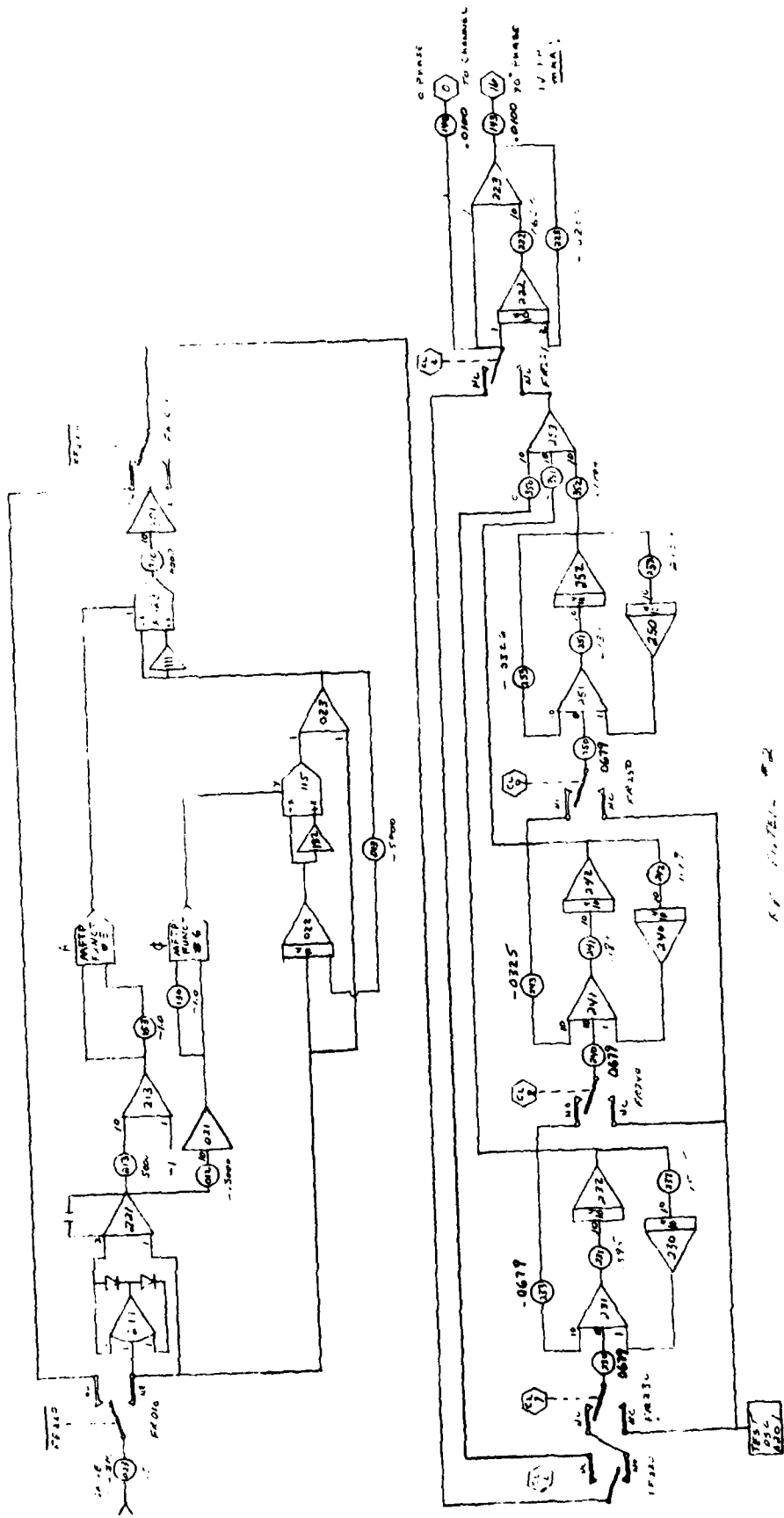




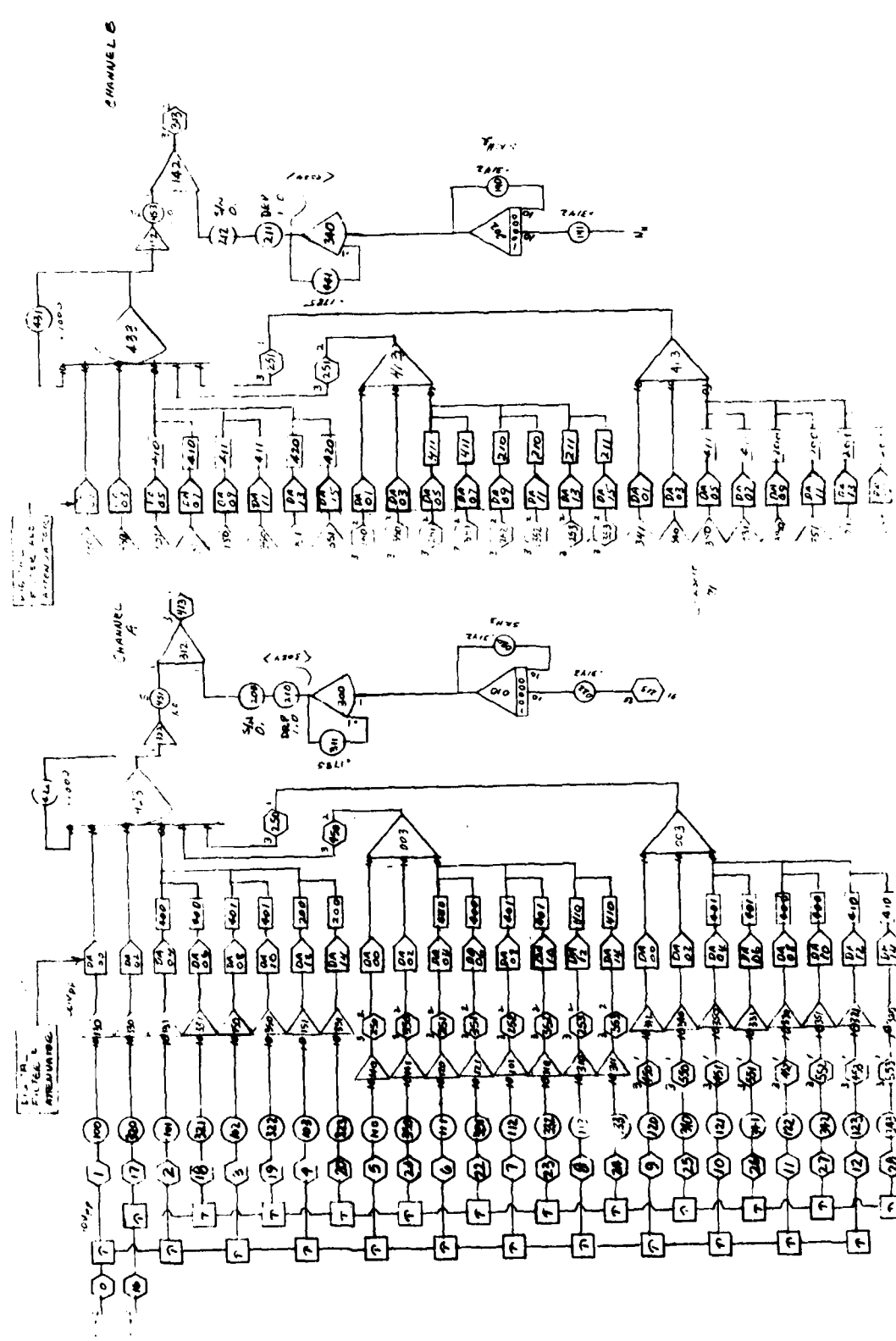
CONSOLE 23-61 204

Console 73-6N 724

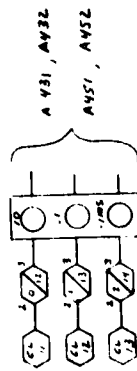
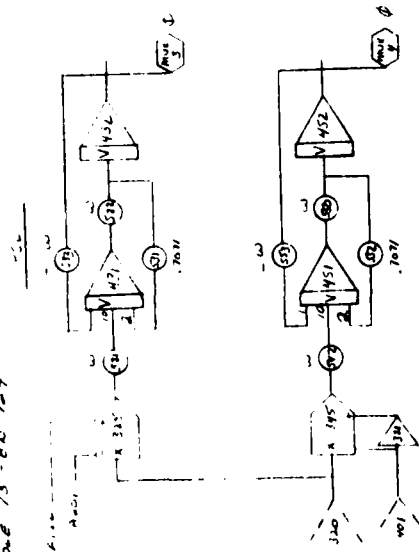
REVISION 1



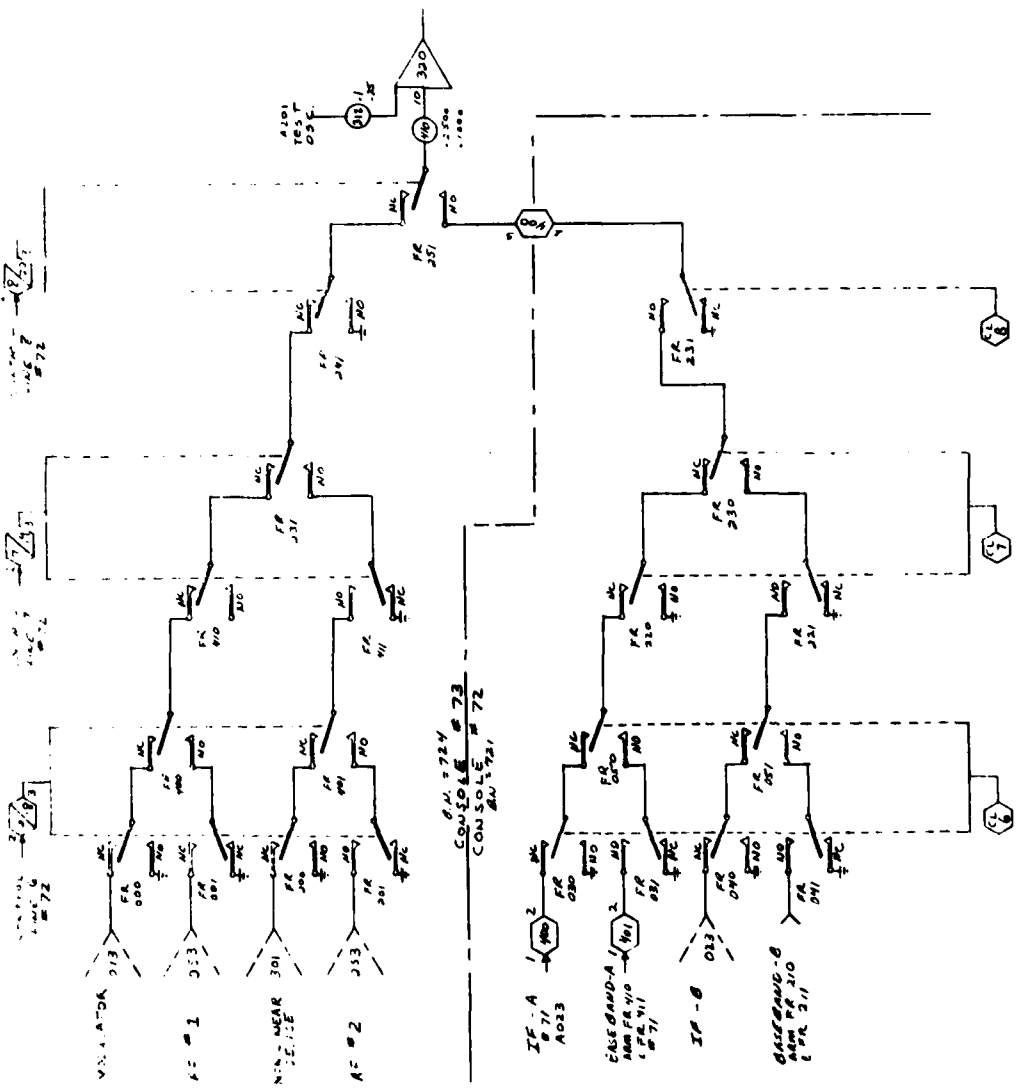
CHANNEL A



ANSWER 73-64 704

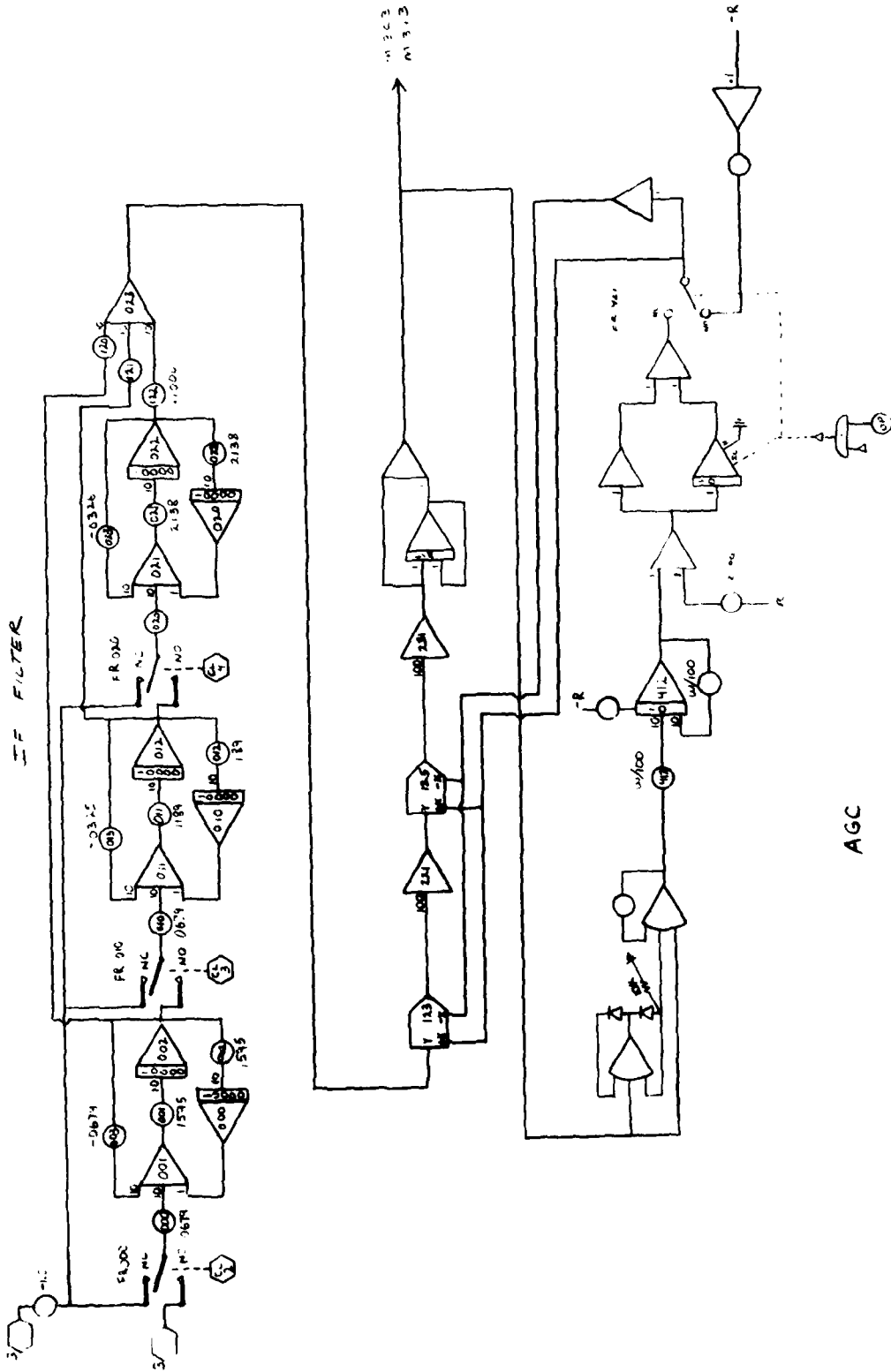


UNASSIGNED - BUS 724 - BUS 724
 UNASSIGNED - BUS 724 - BUS 724
 UNASSIGNED - BUS 724 - BUS 724

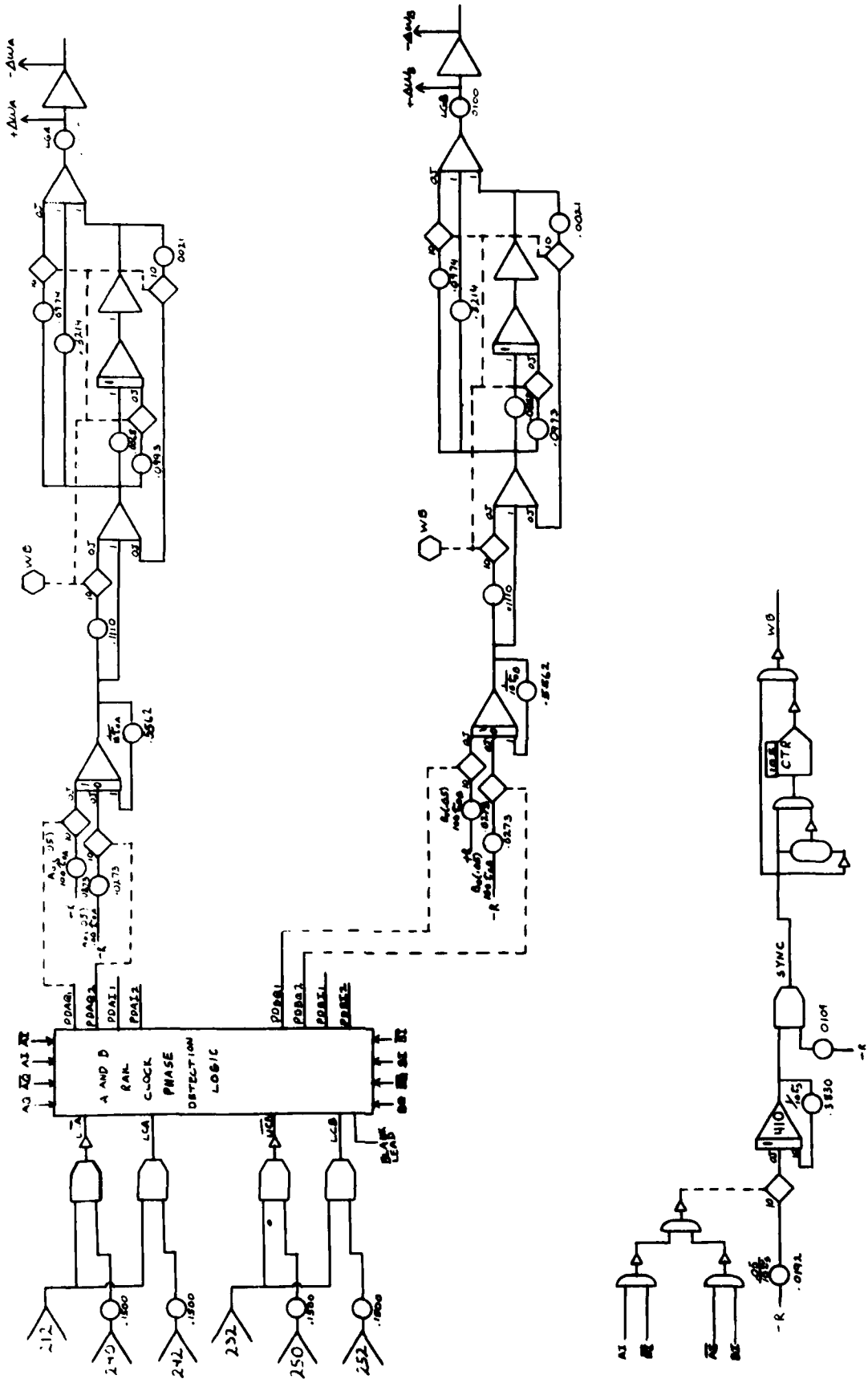


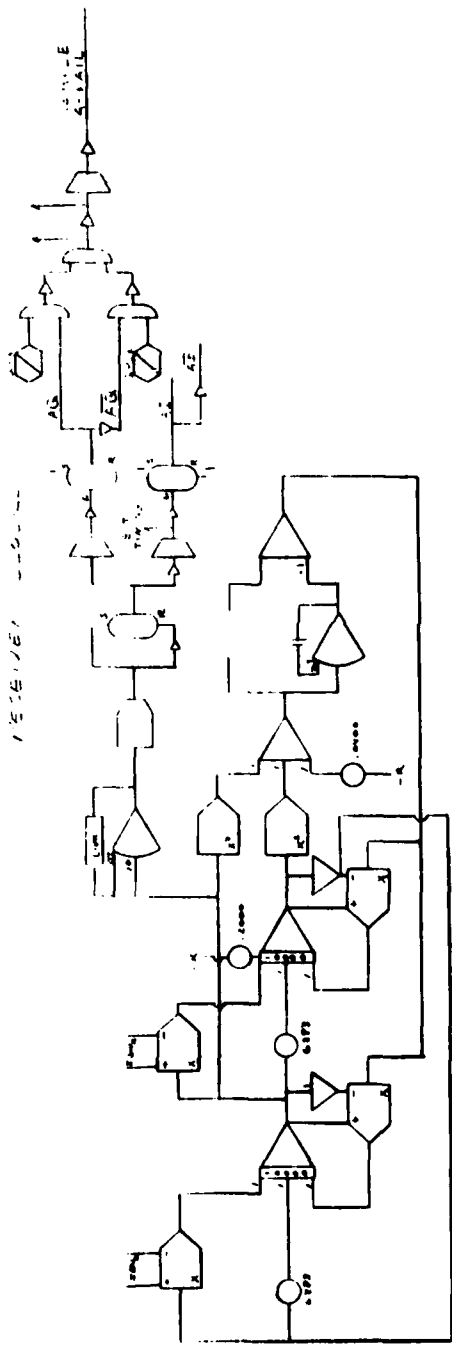
CON 71 00. 711

IF FILTER

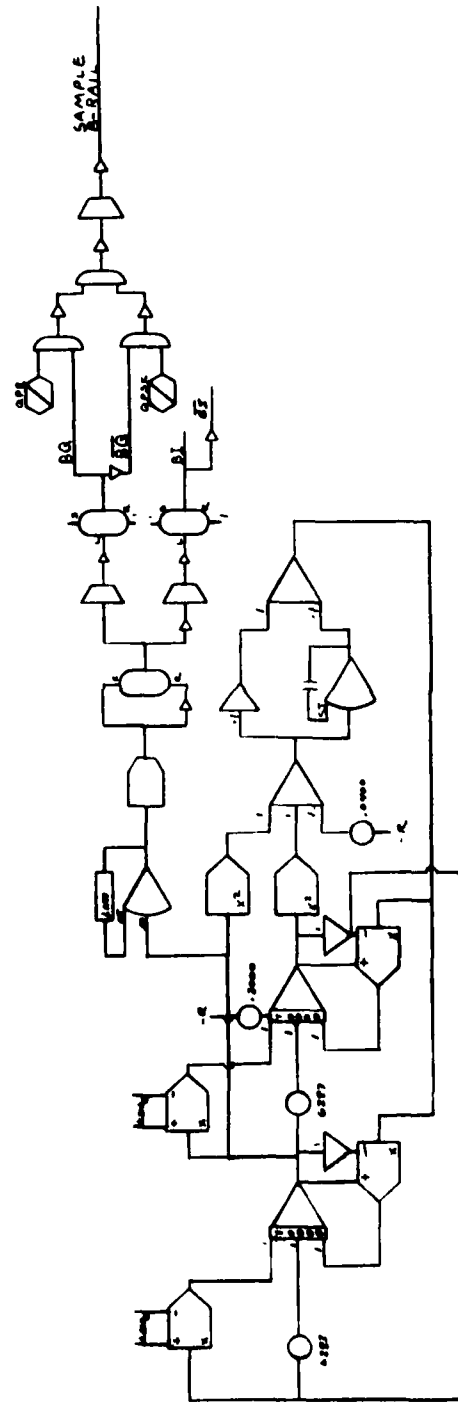


CLOCK RECOVERY PLW





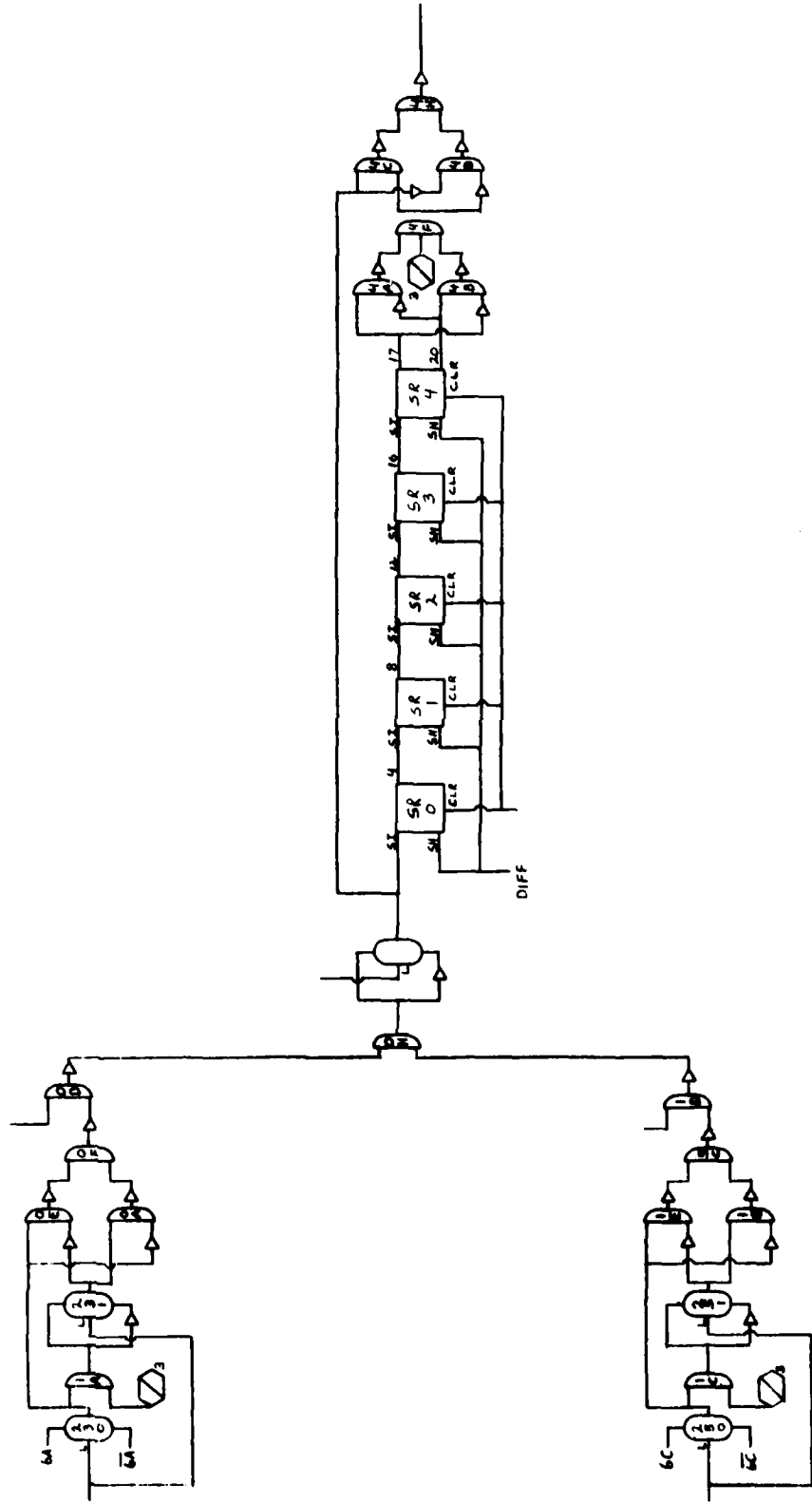
A - CLOCK 1000 Hz



B - CLOCK

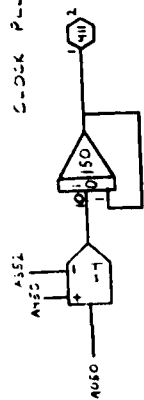
DATA REGENERATOR

BD 71

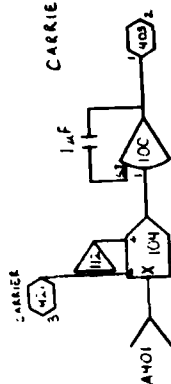


CUN. 1: 25 7-1

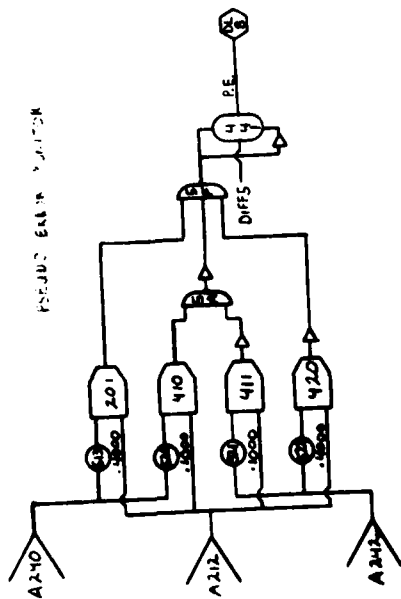
CLOCK PLL INDICATOR



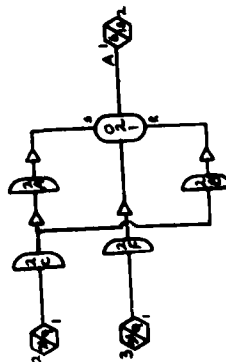
CARRIER PLL INDICATOR



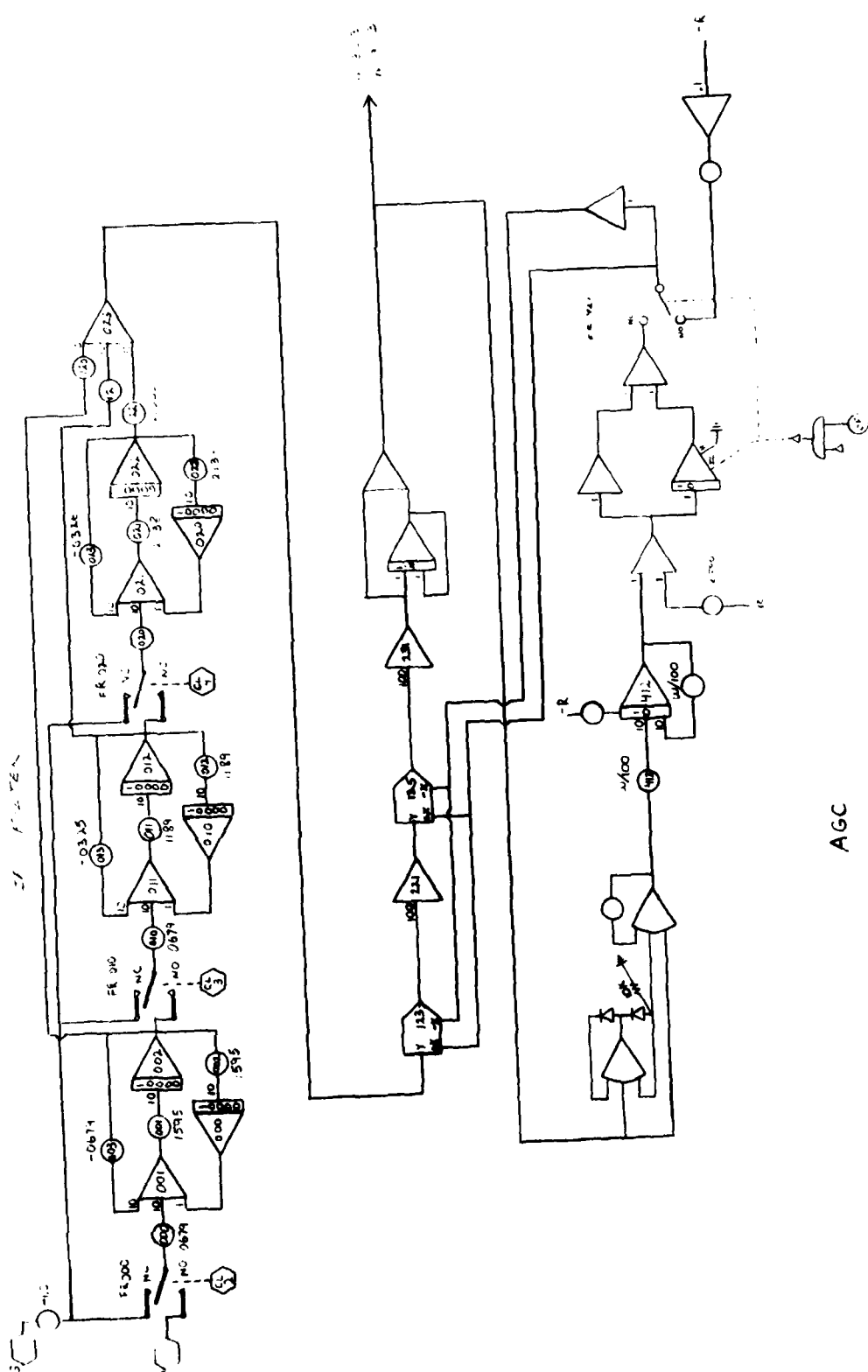
PSEUDO EARLY SWITCH



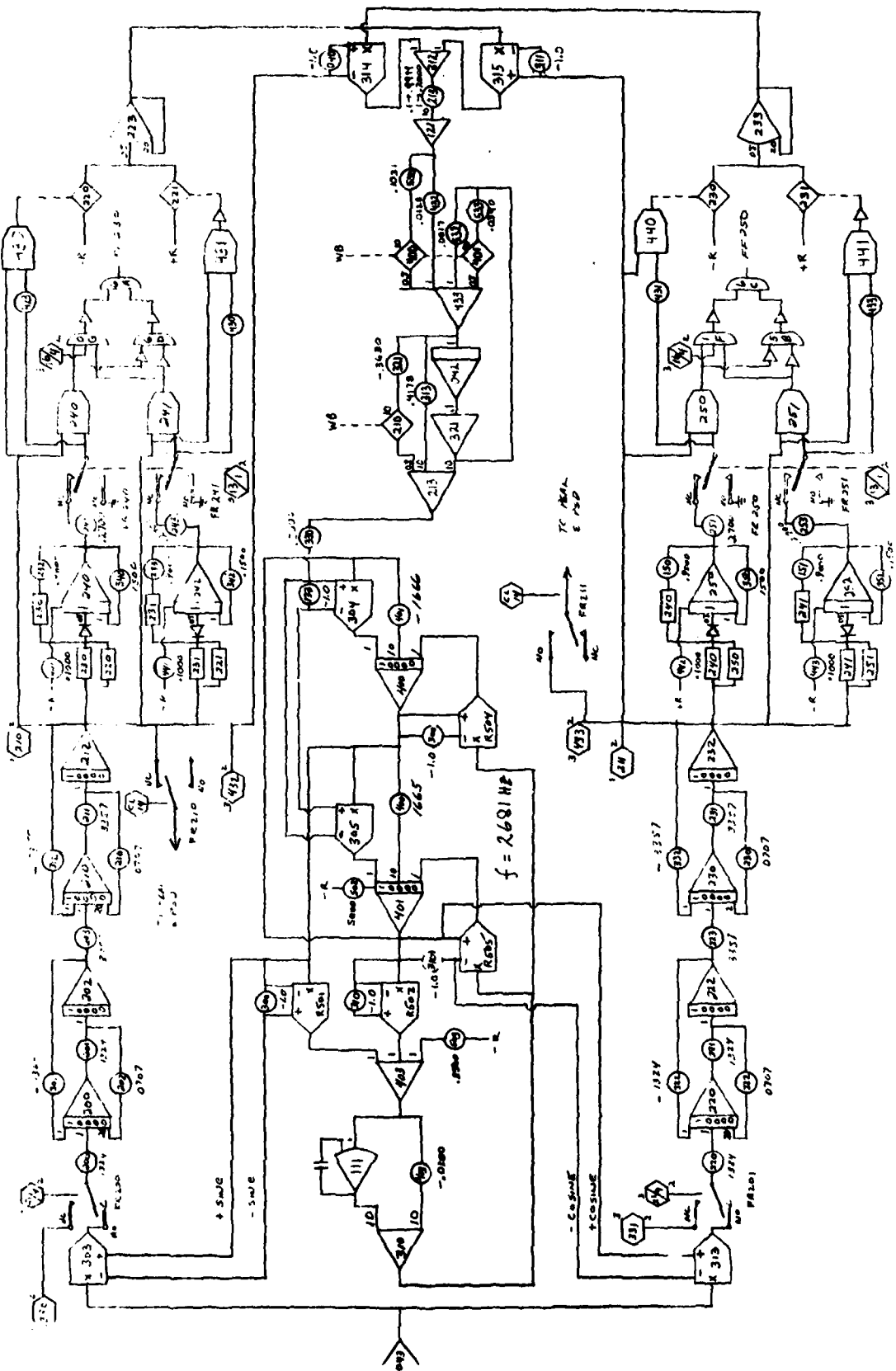
DIVERSITY SWITCH



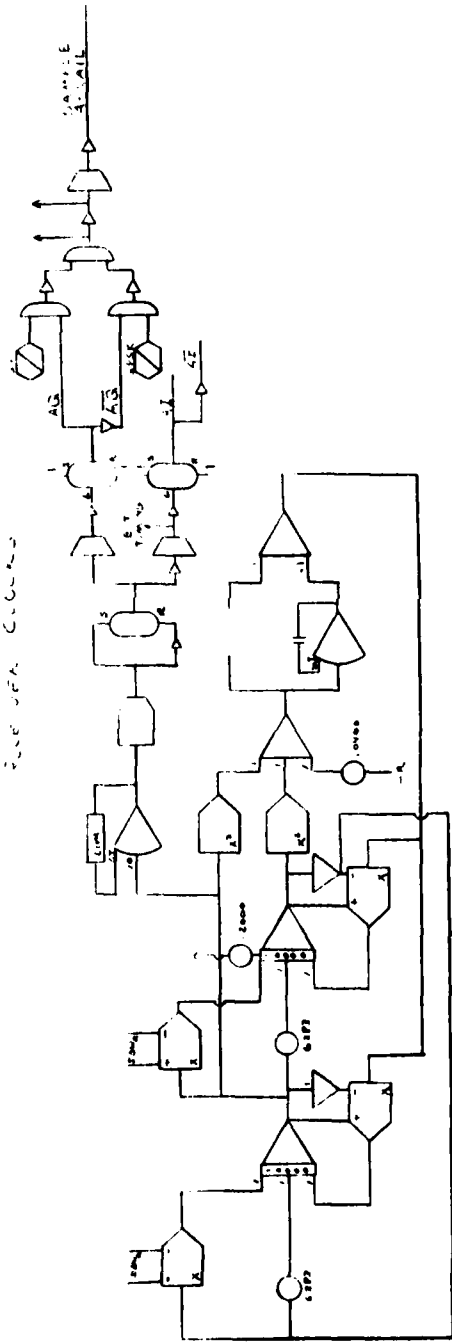
1000 1000 1000



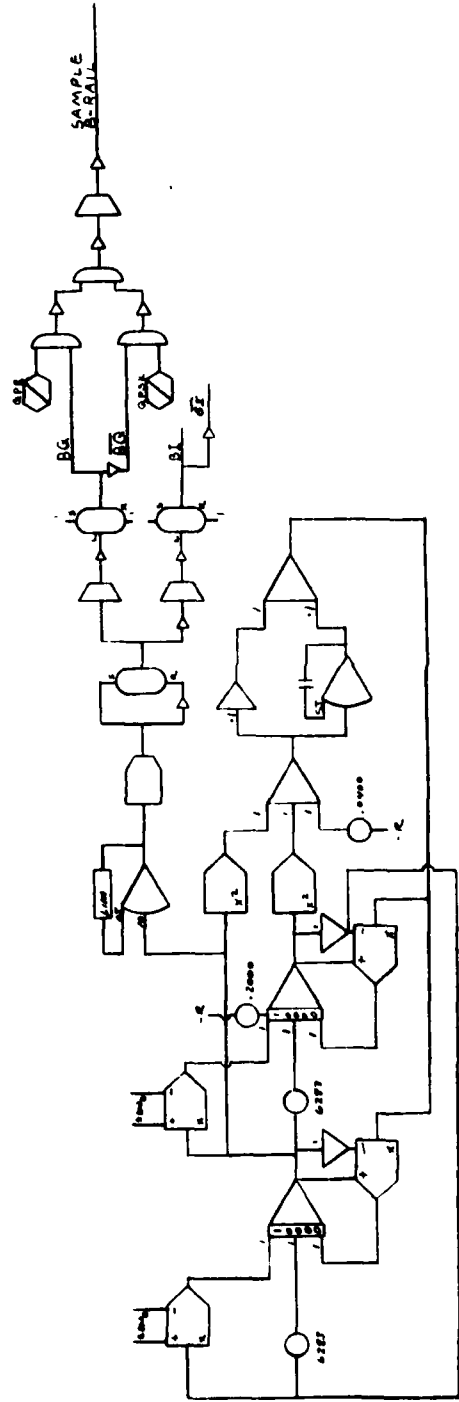
44-2526E 72 - 62A 721



SEE JFA COLUMN



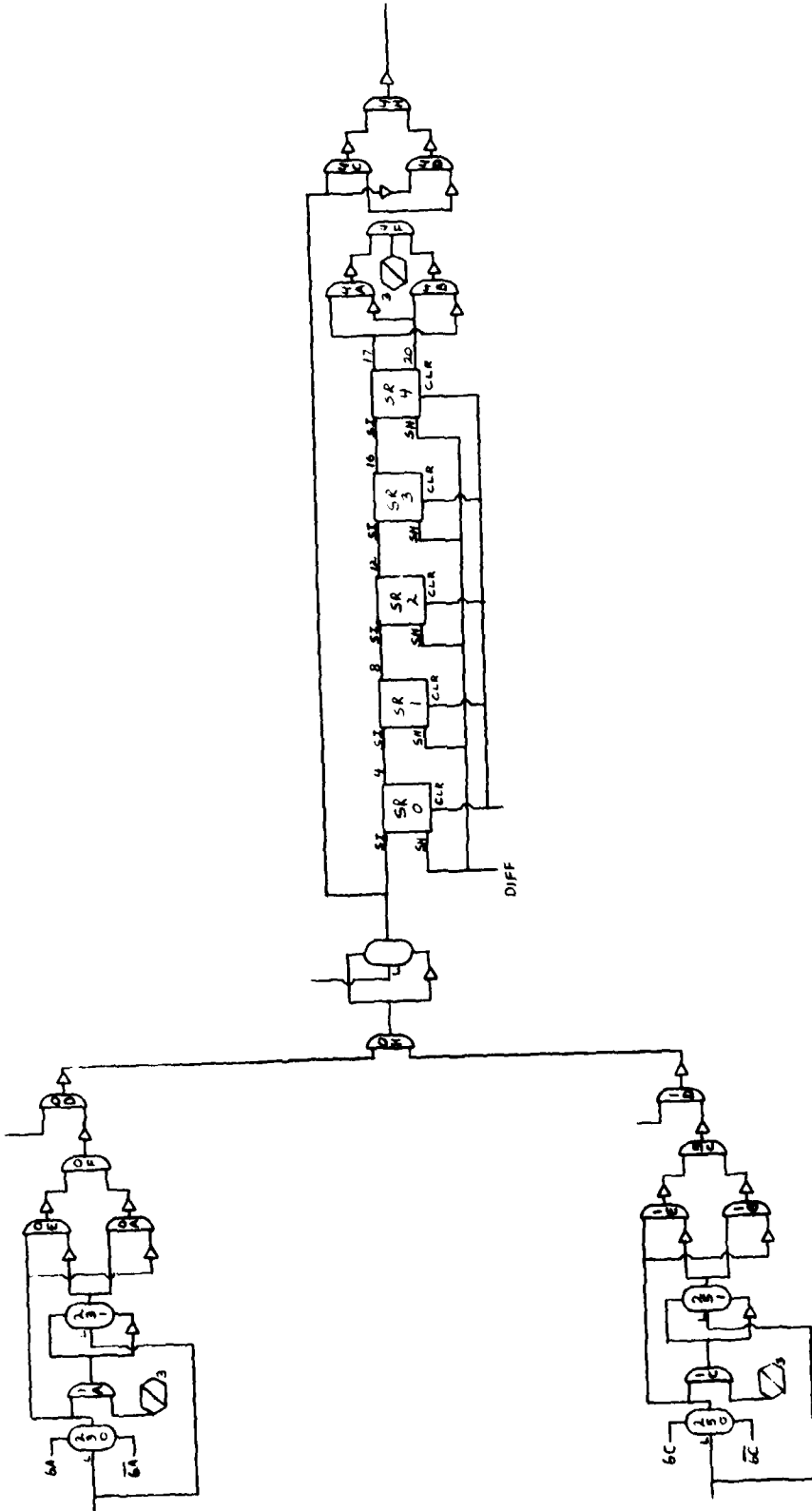
1 - CLOCK 1000 Hz



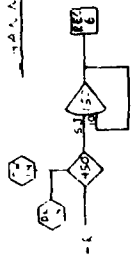
3 CLOCK

DATA REGENERATOR

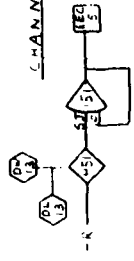
2 50 21



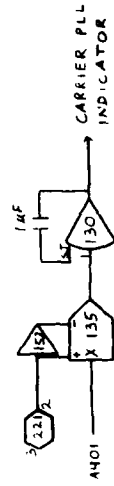
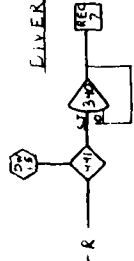
CHANNEL B ERRORS



CHANNEL A ERRORS

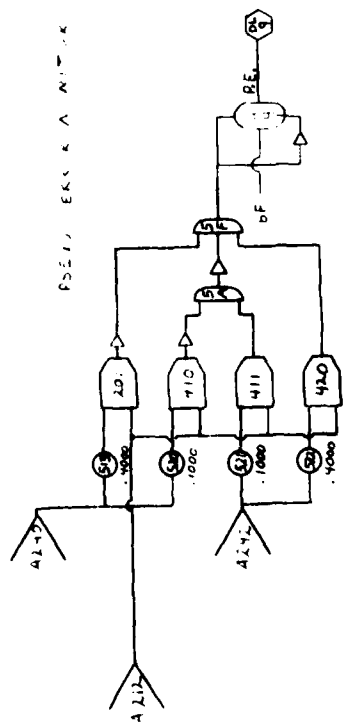


DIVERSITY ERRORS

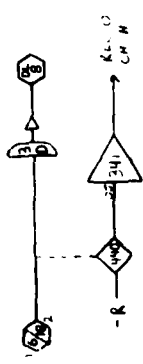
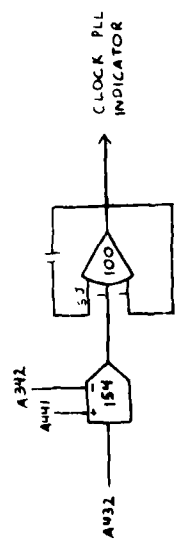


7-1

PSD, ERR A NITK



A-21



DIVERSITY SWITCH

AD-A108 747

MARTIN MARIETTA AEROSPACE ORLANDO FL

F/G 9/2

LOS SELECTIVE FADING AND AN/FRC-170(V) RADIO HYBRID COMPUTER SI--ETC(U)

SEP 81 M K KLUKIS, T I LYON, R WALKER

DCA100-81-C-0016

UNCLASSIFIED

OR-16956

NL

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2

4

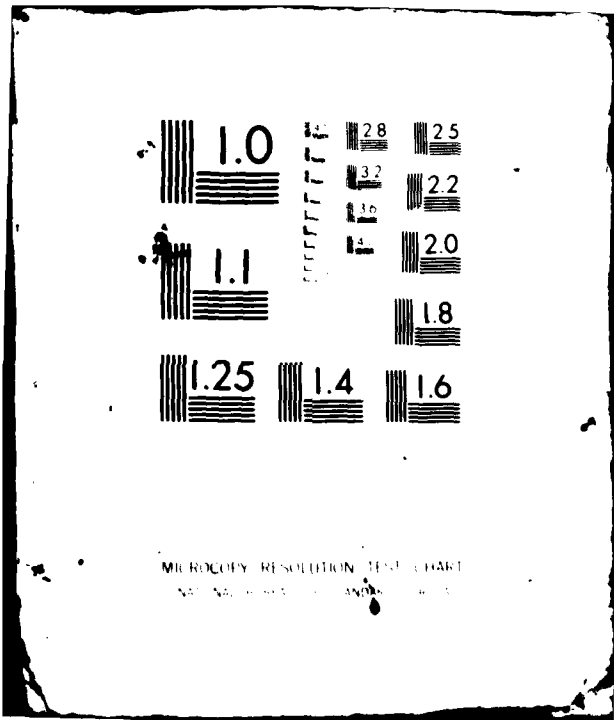
END

DATE

FILED

1 82

DTIC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

APPENDIX B

SIMULATION CONTROLS AND DISPLAYS FOR
AN/FRC-170(V) HYBRID COMPUTER SIMULATION

SYS. CNFG.

NOMINAL

OPTION NO. OPTION

- 1 BIT ERROR TEST
- 2 POWER SPECTRAL DENSITY
- 3 RF, IF AND BASEBAND FILTER
FREQUENCY RESPONSE
- 4 RF AND IF FILTERS
- 5 SYSTEM CONFIGURATION
- 6 EYE PATTERN
- 7 CONSTELLATION
- 8 FINISHED

OPTION NO. =

QPSK

CHANNEL MODEL ?

- 1 OUT
- 2 RAYLEIGH
- 3 LOS

EB/NO = 10
OPTION NO. = 1
RUN TIME = 100

BIT ERROR TEST IN PROGRESS
PRESS <RETURN> FOR EARLY TERMINATION
TOTAL RUN TIME = 100.0 SECONDS

TOTAL BITS = 100000
BIT ERRORS

BIT ERRORS BER

CHANNEL A
CHANNEL B
DIVERSITY

0 0.1000E-03
10 0 0.
0 0 0.

UNIT NO. DEVICE

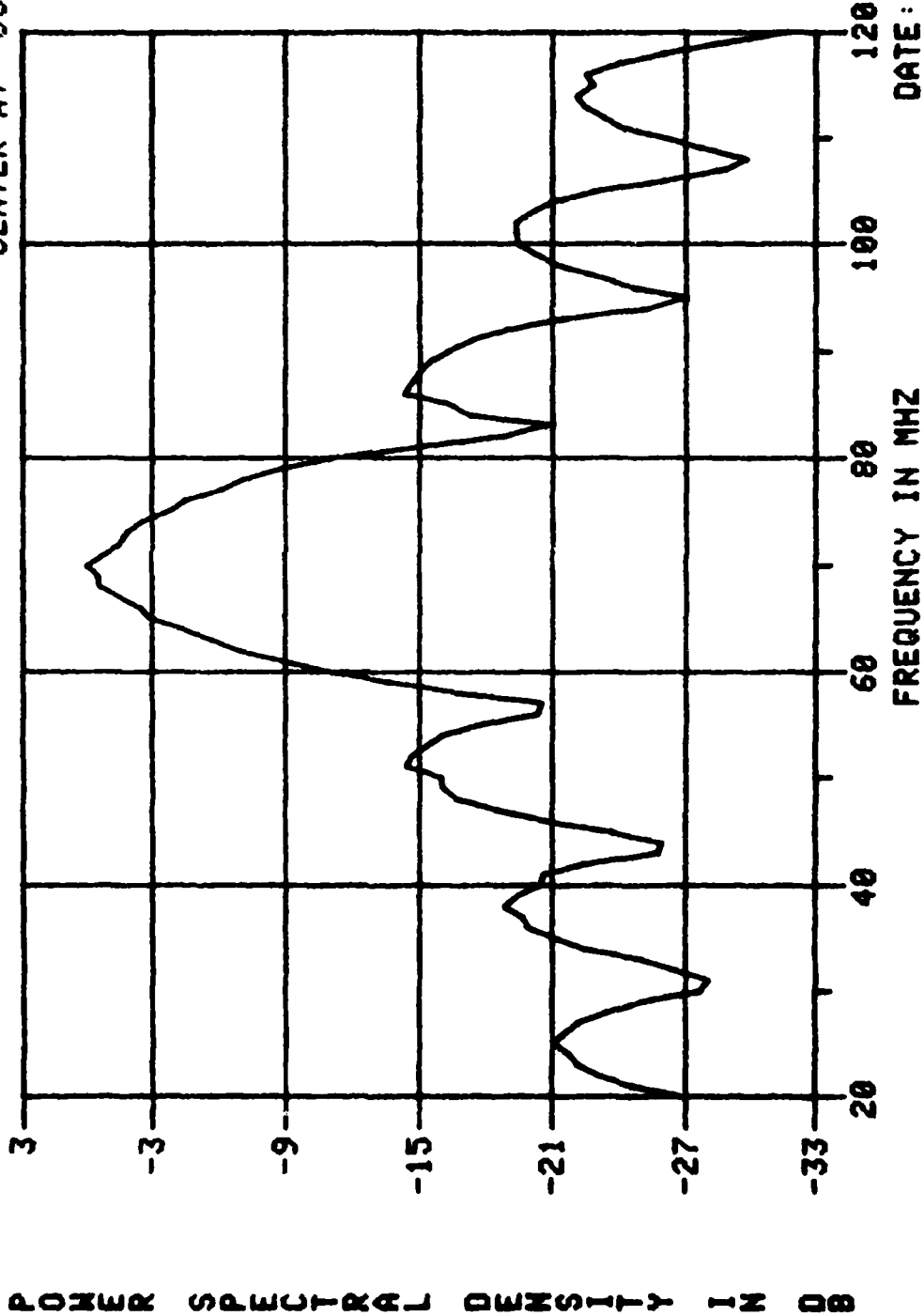
- 1 TRANSMITTER RF FILTER 1**
- 2 TRANSMITTER RF FILTER 2**
- 3 REC. IF FILTER CHANNEL A**
- 4 REC. IF FILTER CHANNEL B**
- 5 BASEBAND FILTER CHANNEL A-I**
- 6 BASEBAND FILTER CHANNEL A-Q**
- 7 BASEBAND FILTER CHANNEL B-I**
- 8 BASEBAND FILTER CHANNEL B-Q**
- 9 TRANSMITTER NON LINEARITY**
- 10 MODULATOR OUTPUT**

UNIT NO. 10

NO. OF POINTS = 100
LOWER FREQ. IN MHZ = 20
UPPER FREQ. IN MHZ = 120
PSD FILTER BANDWIDTH IN HZ = 50

QPSK

MODULATOR OUTPUT
PSD FILTER BW = 50.00 HZ
POWER : 99% BW= 97.00 MHZ
PEAK AT 70.00 MHZ
CENTER AT 68.50 MHZ

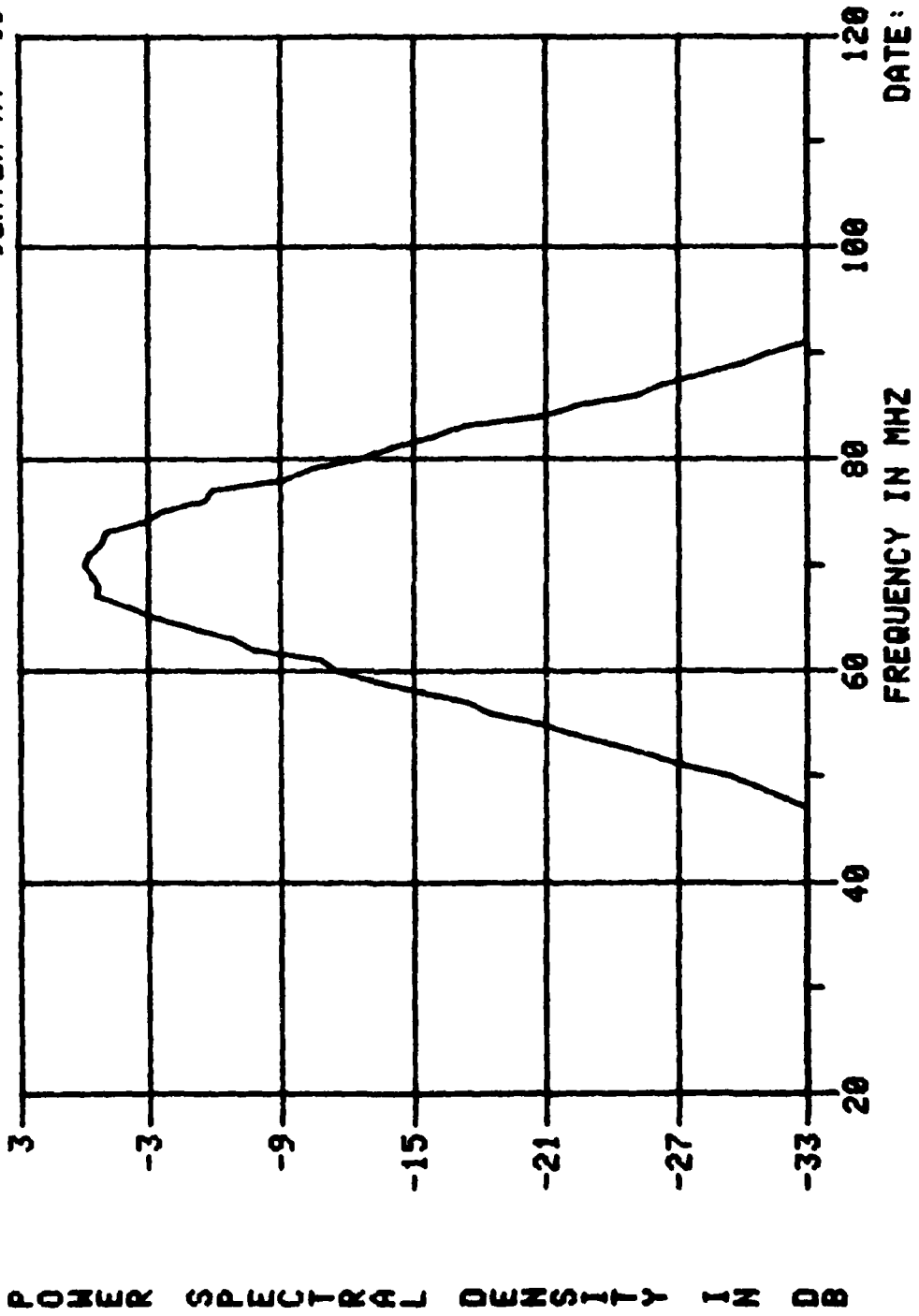


DATE: 4/22/80

QPR

MODULATOR OUTPUT
PSD FILTER BW = 50.00 HZ

POWER : 99% BW = 39.00 MHZ
PEAK AT 70.00 MHZ
CENTER AT 69.50 MHZ



DATE: 4/24/80

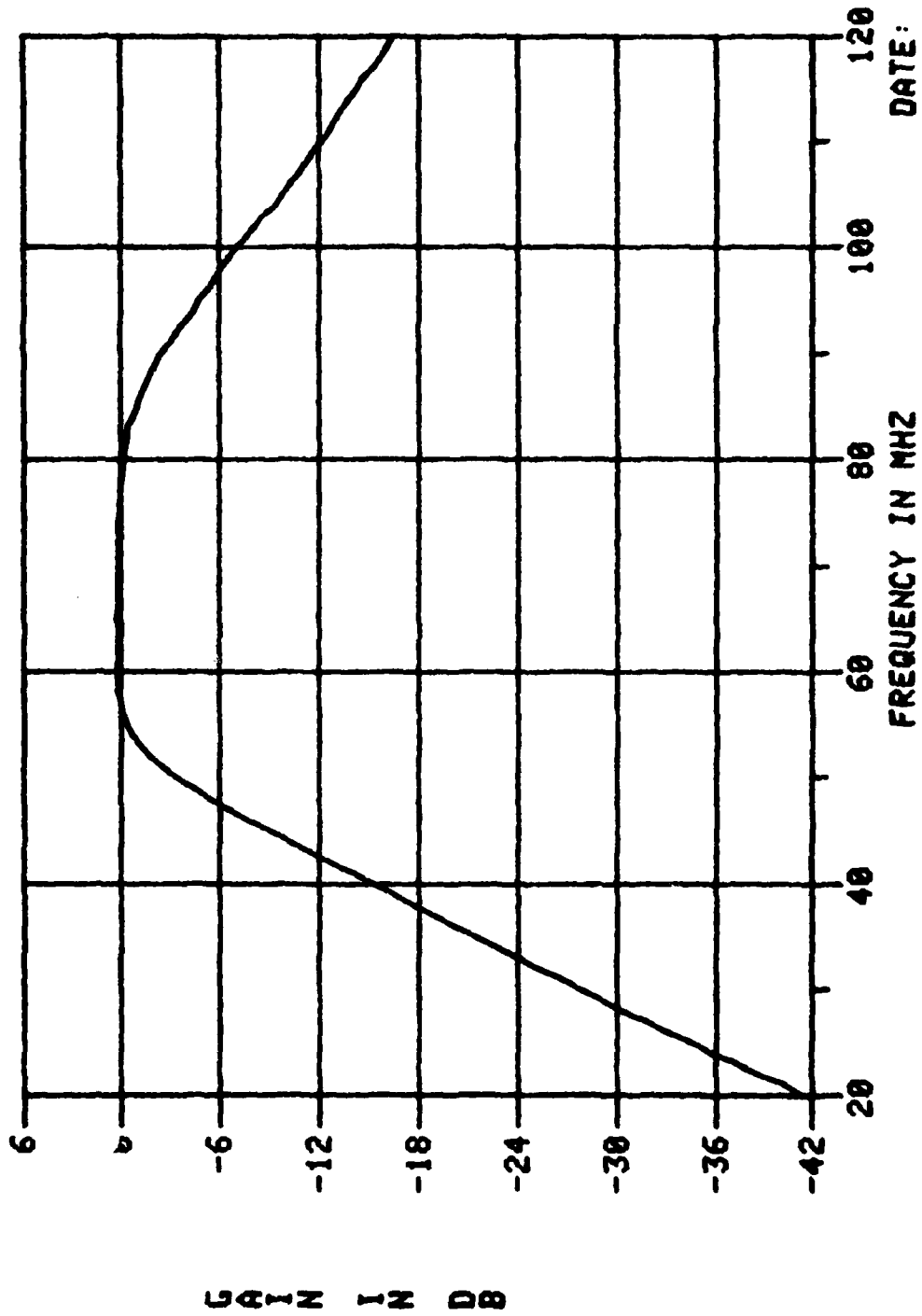
UNIT NO. DEVICE

- 1 TRANSMITTER RF FILTER 1**
- 2 TRANSMITTER RF FILTER 2**
- 3 REC. IF FILTER CHANNEL A**
- 4 REC. IF FILTER CHANNEL B**
- 5 BASEBAND FILTER CHANNEL A-I**
- 6 BASEBAND FILTER CHANNEL A-Q**
- 7 BASEBAND FILTER CHANNEL B-I**
- 8 BASEBAND FILTER CHANNEL B-Q**

UNIT NO. 1

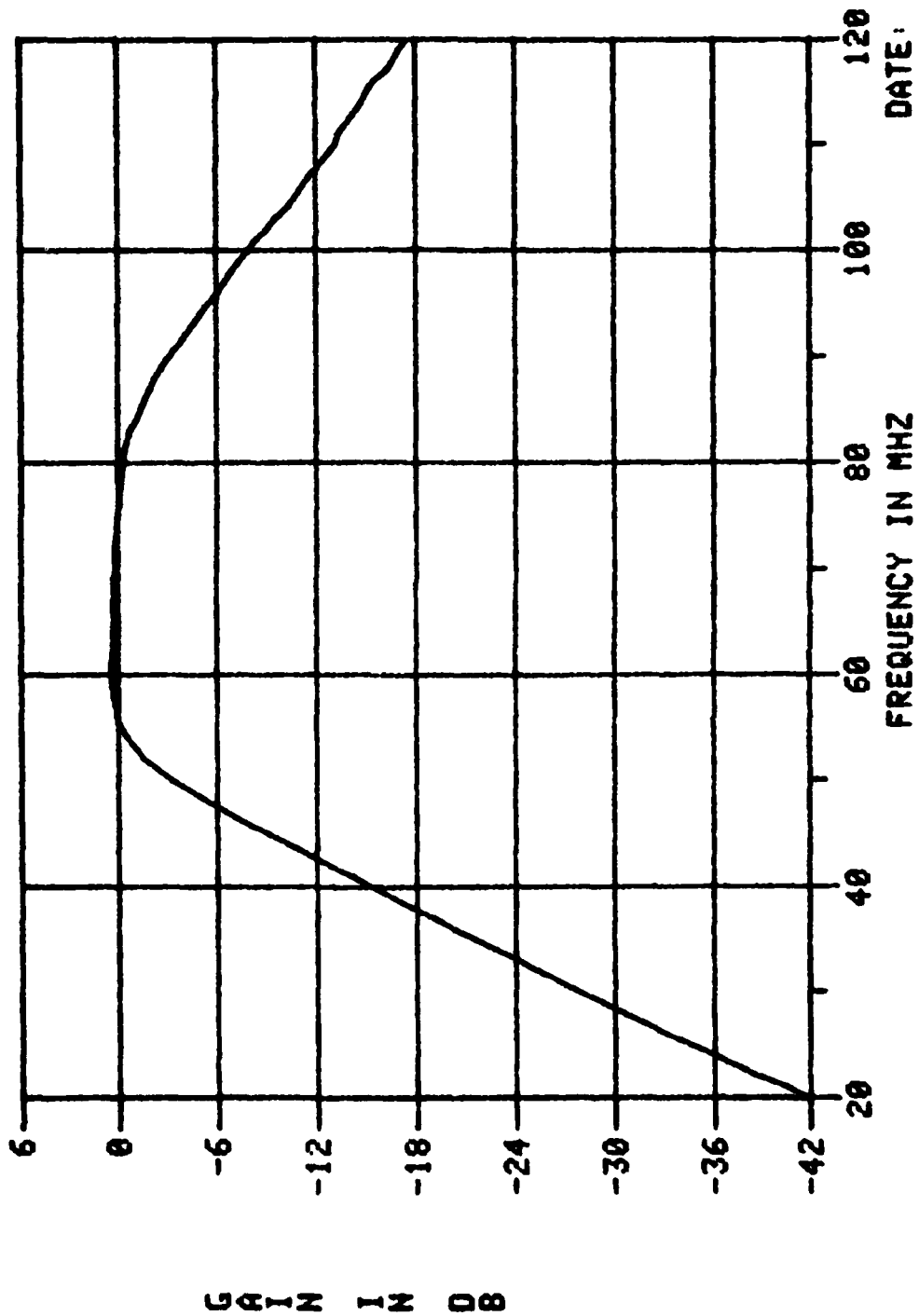
NO. OF POINTS = 100
LOWER FREQ. IN MHZ = 20
UPPER FREQ. IN MHZ = 120

TRANSMITTER RF FILTER 1



DATE: 4/22/80

TRANSMITTER RF FILTER 2



DATE: 4/22/80

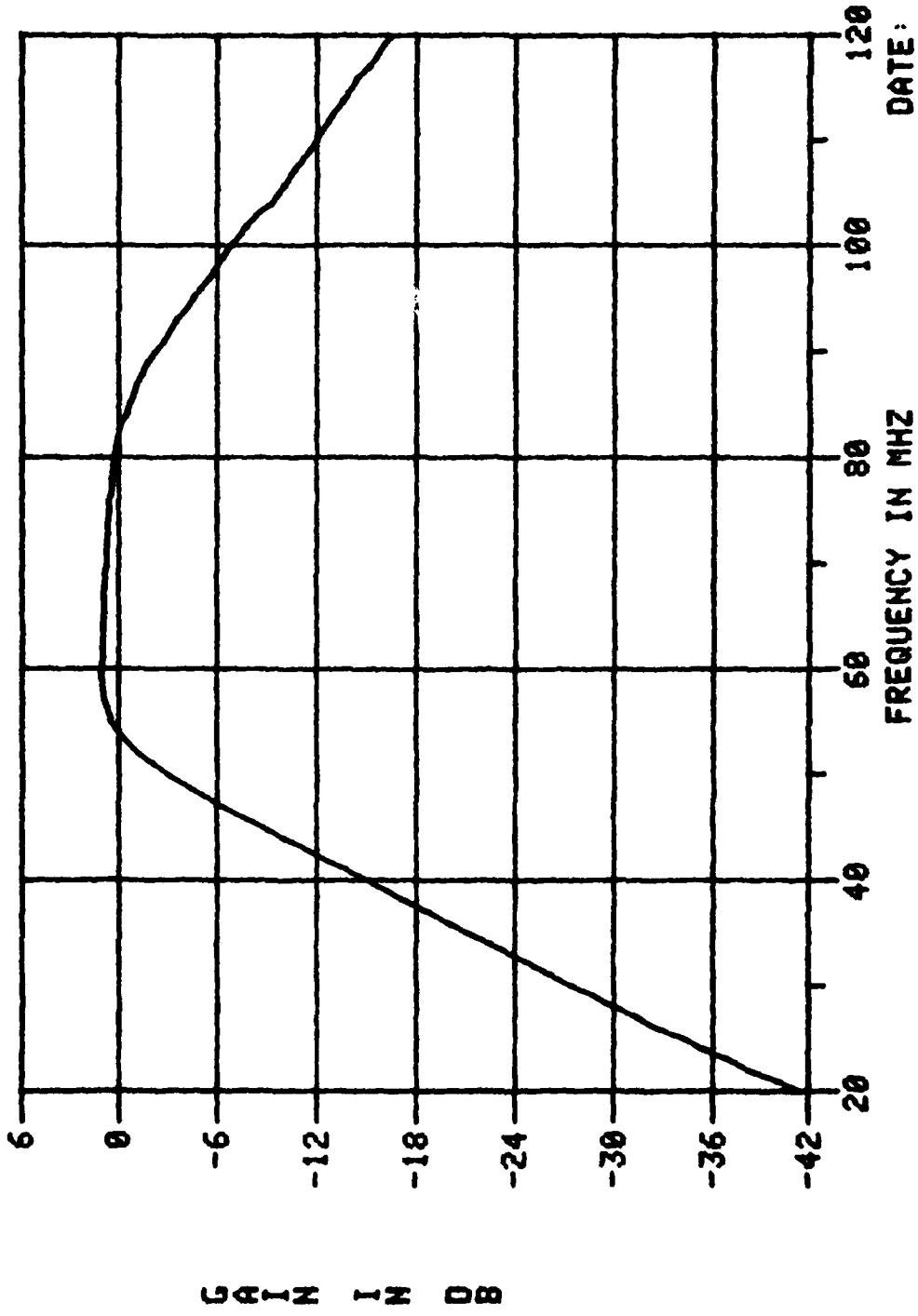
IF FILTER CHANNEL A
TYPE BUTTERWORTH

ORDER 6 DB
RIPPLE 0.000 MHZ
BANDWIDTH 40.000 MHZ
CENTER FREQ. 70.000 MHZ

GAIN 0.59628 0.46067 0.77186
DAMPING -0.59628 -0.28848 -0.28848
NATURAL FREQ. 0.16142 0.20894 0.12470

N = 2
C122 = 0.1155
UNIT 3 = 0.2002
DESIRED VALUE = 0.2000
ERROR = -0.0002

REC. IF FILTER CHANNEL A



DATE: 4/24/80

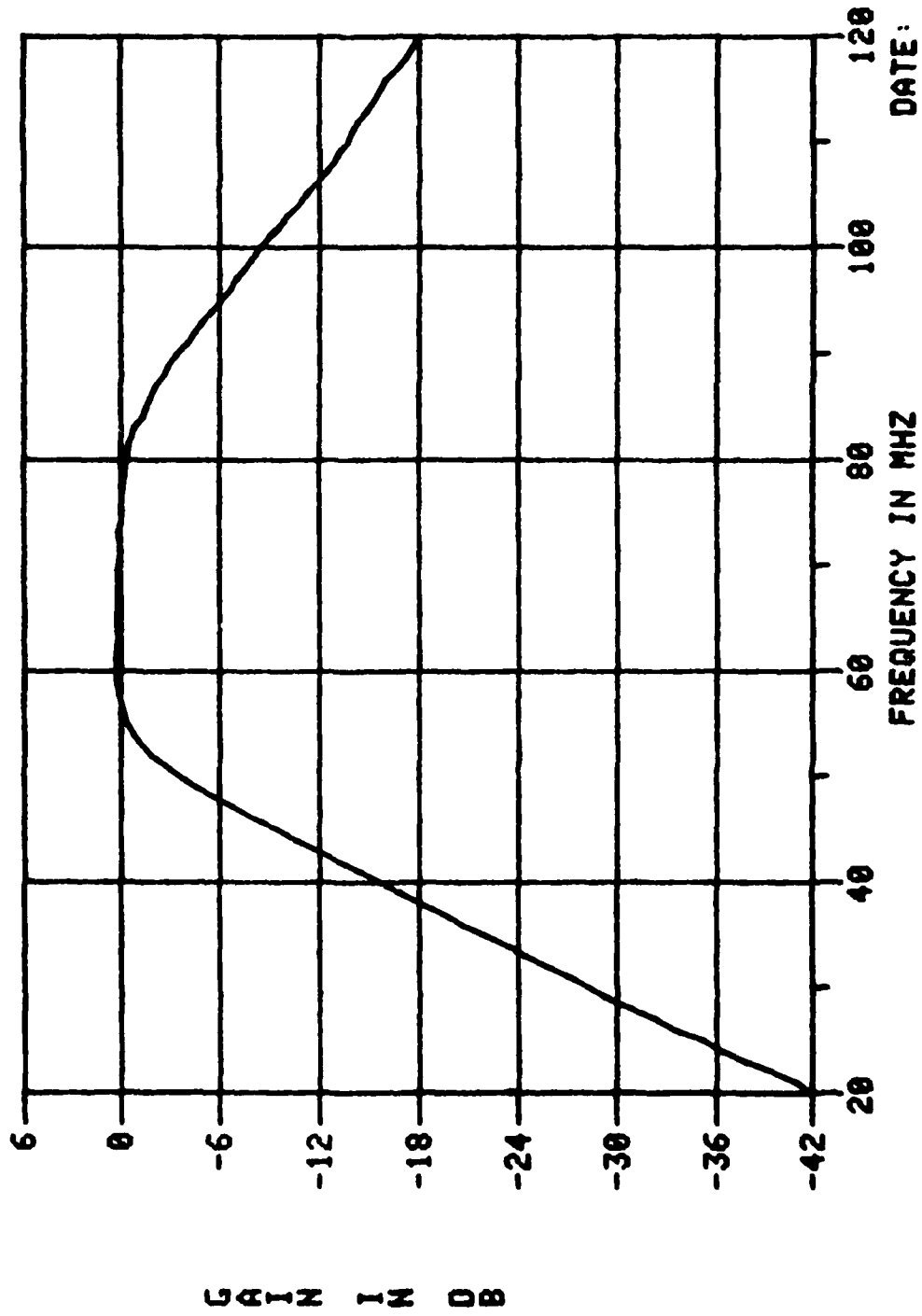
IF FILTER CHANNEL B
BUTTERWORTH

ORDER 6
RIPPLE 0.000 DB
BANDWIDTH 40.000 MHZ
CENTER FREQ. 70.000 MHZ

GAIN 0.59628 0.46067 0.77186
DAMPING -0.59628 -0.28848 -0.28848
NATURAL FREQ. 0.16142 0.20894 0.12470

N = 4
C122 = 0.1129
UNIT 4 = 0.2004 0.2000
DESIRED VALUE =
ERROR = -0.0004

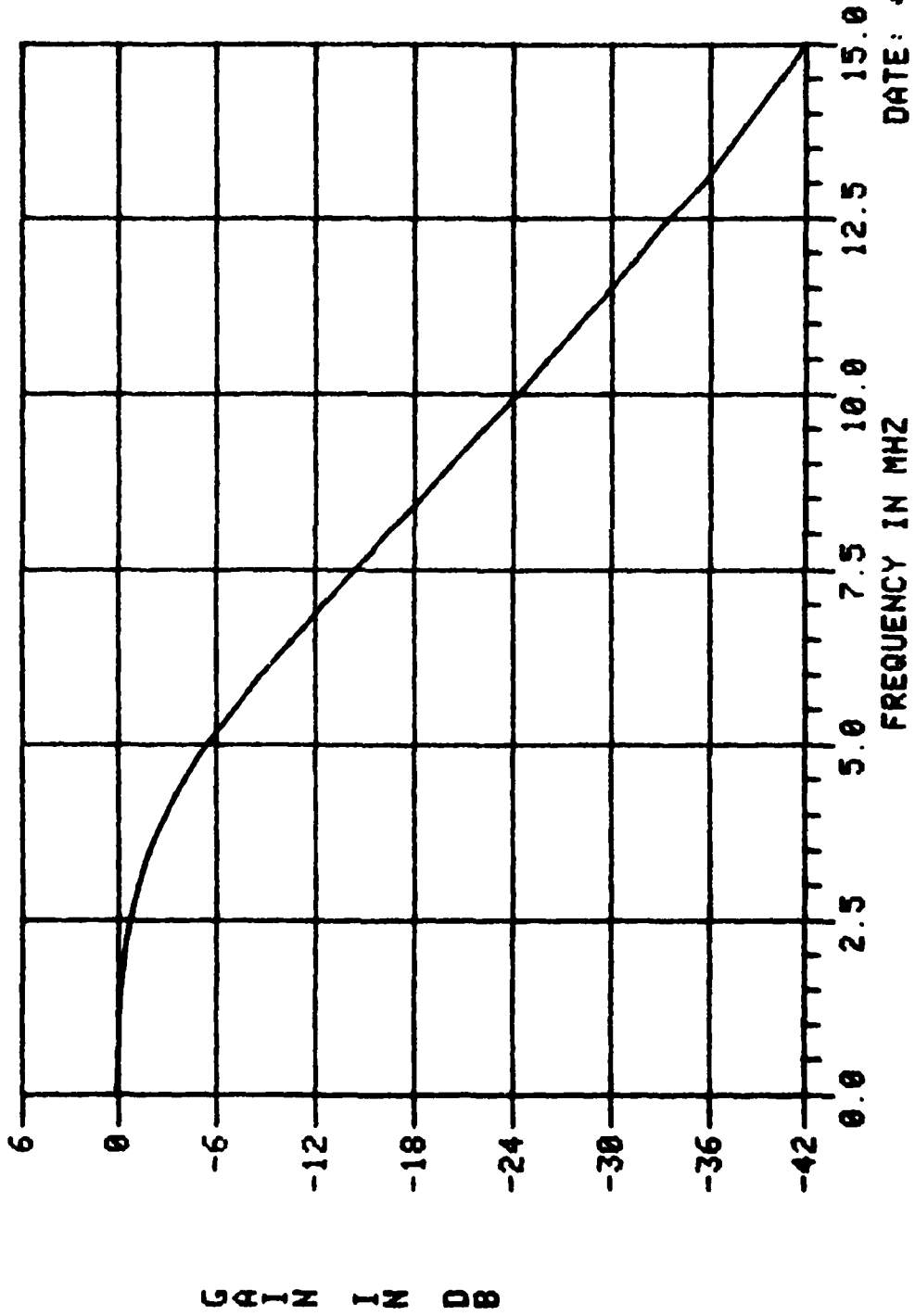
REC. IF FILTER CHANNEL B



DATE: 4/24/80

QPR

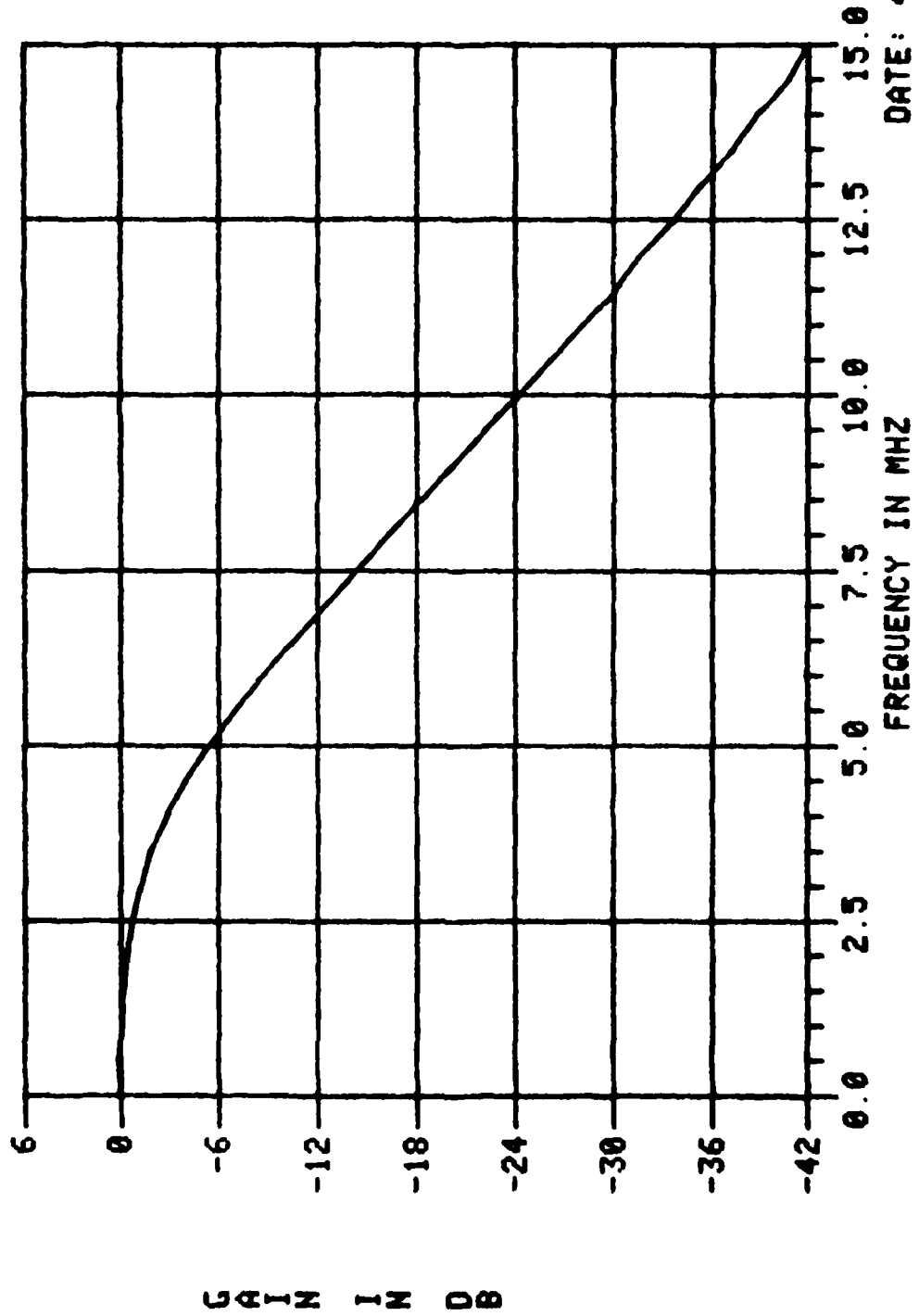
BASEBAND FILTER CHANNEL B-Q



DATE: 4/24/80

QPR

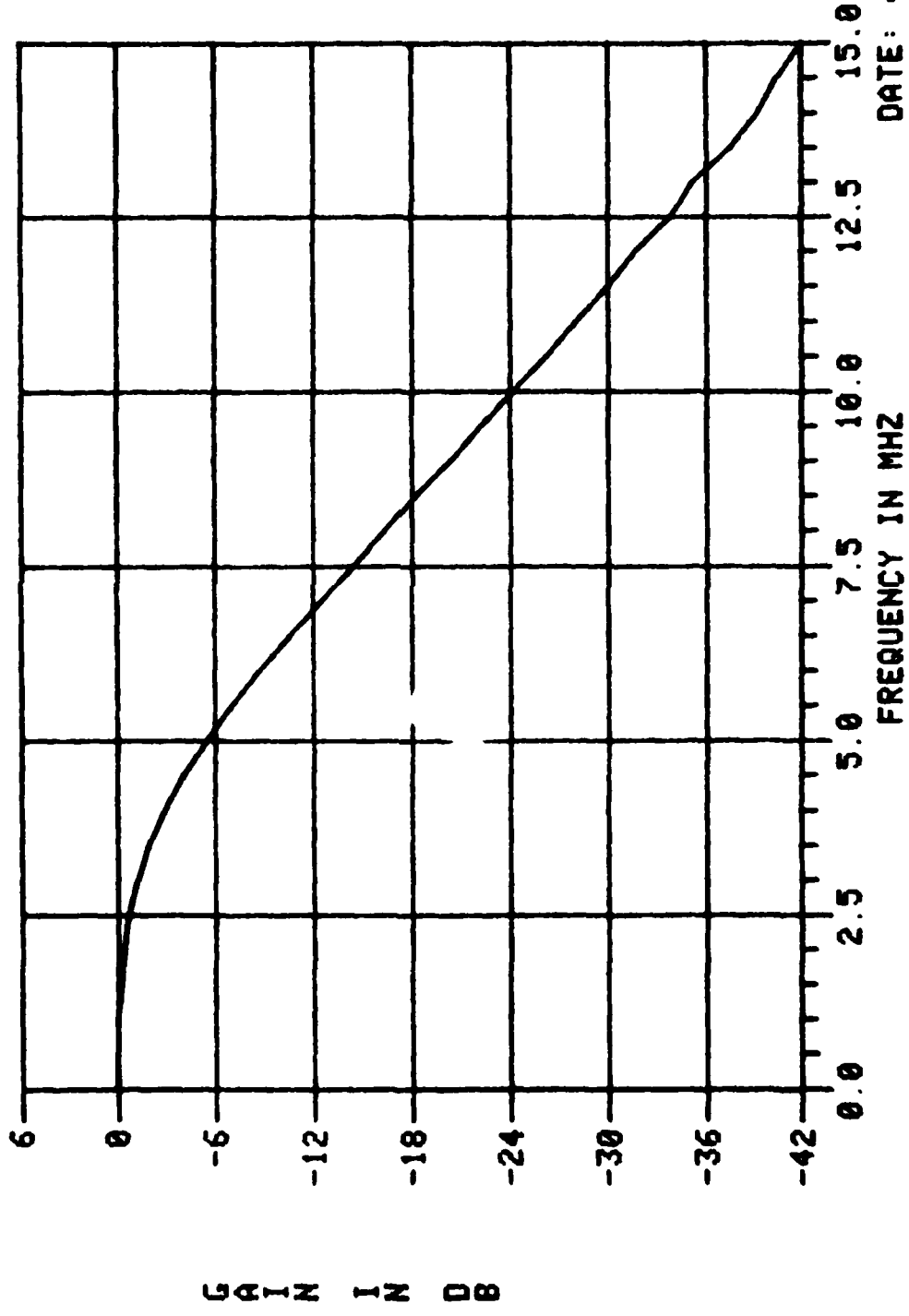
BASEBAND FILTER CHANNEL B-I



DATE: 4/24/80

QPR

BASEBAND FILTER CHANNEL A-Q

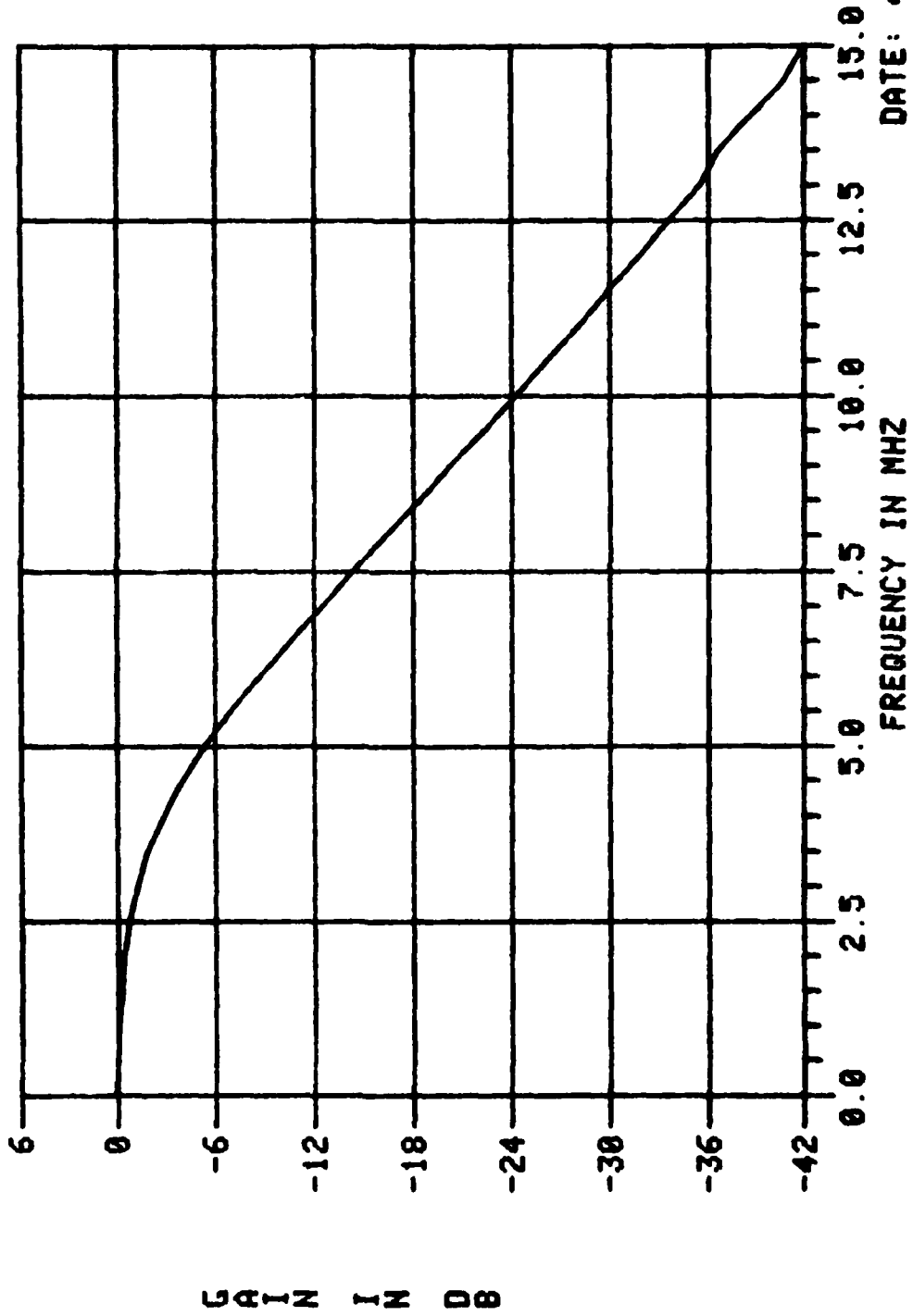


DATE: 4/24/80

G A I N I N D B

QPR

BASEBAND FILTER CHANNEL A-I



DATE: 4/24/80

RF AND IF FILTERS

- 1 LIST FILTER PARAMETER
- 2 CHANGE FILTER PARAMETER
- 3 FINISHED
OPTION NO. =1

RF FILTER NO. 1
TYPE BUTTERWORTH

ORDER 6 DB
RIPPLE 0.000 MHZ
BANDWIDTH 40.000 MHZ
CENTER FREQ. 70.000 MHZ

RF FILTER NO. 2
TYPE BUTTERWORTH

ORDER 6 DB
RIPPLE 0.000 MHZ
BANDWIDTH 40.000 MHZ
CENTER FREQ. 70.000 MHZ

IF FILTER CHANNEL A
TYPE BUTTERWORTH

ORDER 6 DB
RIPPLE 0.000 MHZ
BANDWIDTH 40.000 MHZ
CENTER FREQ. 70.000 MHZ

IF FILTER CHANNEL B
TYPE BUTTERWORTH

ORDER 6 DB
RIPPLE 0.000 MHZ
BANDWIDTH 40.000 MHZ
CENTER FREQ. 70.000 MHZ

RF AND IF FILTERS

- 1 LIST FILTER PARAMETER**
 - 2 CHANGE FILTER PARAMETER**
 - 3 FINISHED
OPTION NO. =2
DEVICE**
- UNIT NO.**

- 1 TRANSMITTER RF FILTER 1**
- 2 TRANSMITTER RF FILTER 2**
- 3 REC. IF FILTER CHANNEL A**
- 4 REC. IF FILTER CHANNEL B**

UNIT NO.2

FILTER TYPE
1 BUTTERWORTH
2 CHEBYSHEV
3 BESSEL

TYPE = 1

6

FILTER ORDER = 6

RIPPLE IN DB = 0

BANDWIDTH IN MHZ = 40

CENTER FREQ. IN MHZ = 70

RF FILTER NO. 2

TYPE CHEBYSHEV

ORDER

RIPPLE

BANDWIDTH

CENTER FREQ.

6

DB

40.000

70.000 MHZ

N = 2

C352 = 0.1378

UNIT 2 = 0.2003

DESIRED VALUE = 0.2000

ERROR = -0.0003

SYS. CHFG.
NOMINAL

- SYSTEM CONFIGURATION
- 1 LIST CURRENT CONFIGURATION
 - 2 LIST NOMINAL CONFIGURATION
 - 3 LIST SET CONFIGURATION
 - 4 CHANGE CURRENT CONFIGURATION
 - 5 CHANGE NOMINAL CONFIGURATION
 - 6 SET CURRENT CONFIGURATION
 - 7 SET NOMINAL CONFIGURATION
 - 8 CHANGE POWER PROFILE
 - 9 PLOT POWER PROFILE
 - 10 FINISHED OPTION NO. =

CONFIGURATION NO. = 6

AGC IS OUT
BANDWIDTH = 1.00 HZ
OTM THRESHOLD
% OF BIT AMPLITUDE = 5.00
OTM BANDWIDTH = 1.00 HZ

EB/N0 = 20.00 DB

CHANNEL MODEL
2 RAYLEIGH
FADE RATE = 1.00 HZ

RUN TIME = 10.00 SECS

% DRIVE POWER = 50.00

DIVERSITY SELECTION OTM

MODULATION TYPE = QPR

TRANSMITTER RF FILTER 1 IS OUT
TRANSMITTER RF FILTER 2 IS OUT

TRANSMITTER NON LINEARITY IS IN

SCRAMBLER IS IN

CONFIGURATION NOMINAL

AGC IS IN
BANDWIDTH = 5.00 HZ

OTM THRESHOLD
% OF BIT AMPLITUDE = 25.00
OTM BANDWIDTH = 5.00 HZ

EB/NO = 100.00 DB

CHANNEL MODEL
1. OUT

RUN TIME = 10.00 SECS

% DRIVE POWER = 1.00

DIVERSITY SELECTION AGC

MODULATION TYPE = QPSK

TRANSMITTER RF FILTER 1 IS IN
TRANSMITTER RF FILTER 2 IS IN

TRANSMITTER NON LINEARITY IS OUT

SCRAMBLER IS OUT

AGC IN Y/N ? Y
AGC BANDWIDTH IN HZ =5

OTM THRESHOLD
% OF BIT AMPLITUDE =55
OTM BANDWIDTH IN HZ =5

EB/NO IN DB =20

CHANNEL MODEL ?

- 1 OUT
- 2 RAYLEIGH
- 3 LOS

OPTION NO. =2
FADE RATE IN HZ = 2.5

RUN TIME IN SECS =300

% OF DRIVE POWER =.9999

DIVERSITY SELECTION

- 1 AGC
 - 2 OTM
 - 3 ALGO
- OPTION NO. =2

MODULATION TYPE ?

- 1 QPSK
 - 2 OPSK
- OPTION NO. =1

TRANSMITTER RF FILTER 1 IN Y/N ? Y
TRANSMITTER RF FILTER 2 IN Y/N ? Y
TRANSMITTER NON LINEARITY IN Y/N ? N
SCRAMBLER IN Y/N ? N

CONFIGURATION NO. = 7

AGC IS OUT
BANDWIDTH = 5.00 HZ

OTM THRESHOLD
% OF BIT AMPLITUDE = 55.00
OTM BANDWIDTH = 5.00 HZ

EB/NO = 20.00 DB

CHANNEL MODEL
2. RAYLEIGH

FADE RATE = 2.50 HZ

RUN TIME = 300.00 SECS

% DRIVE POWER = 1.00

DIVERSITY SELECTION OTM

MODULATION TYPE = QPR

TRANSMITTER RF FILTER 1 IS IN
TRANSMITTER RF FILTER 2 IS IN

TRANSMITTER NON LINEARITY IS OUT

SCRAMBLER IS OUT

CHANGE POWER PROFILE

NUMBER OF TAPS=12
SPECIFY STATIONARY TAPS Y/N ? Y
STATIONARY TAP NUMBER=3
STATIONARY TAP NUMBER=5
STATIONARY TAP NUMBER=7
STATIONARY TAP NUMBER=

CHANGE TAP GAINS Y/N ? Y

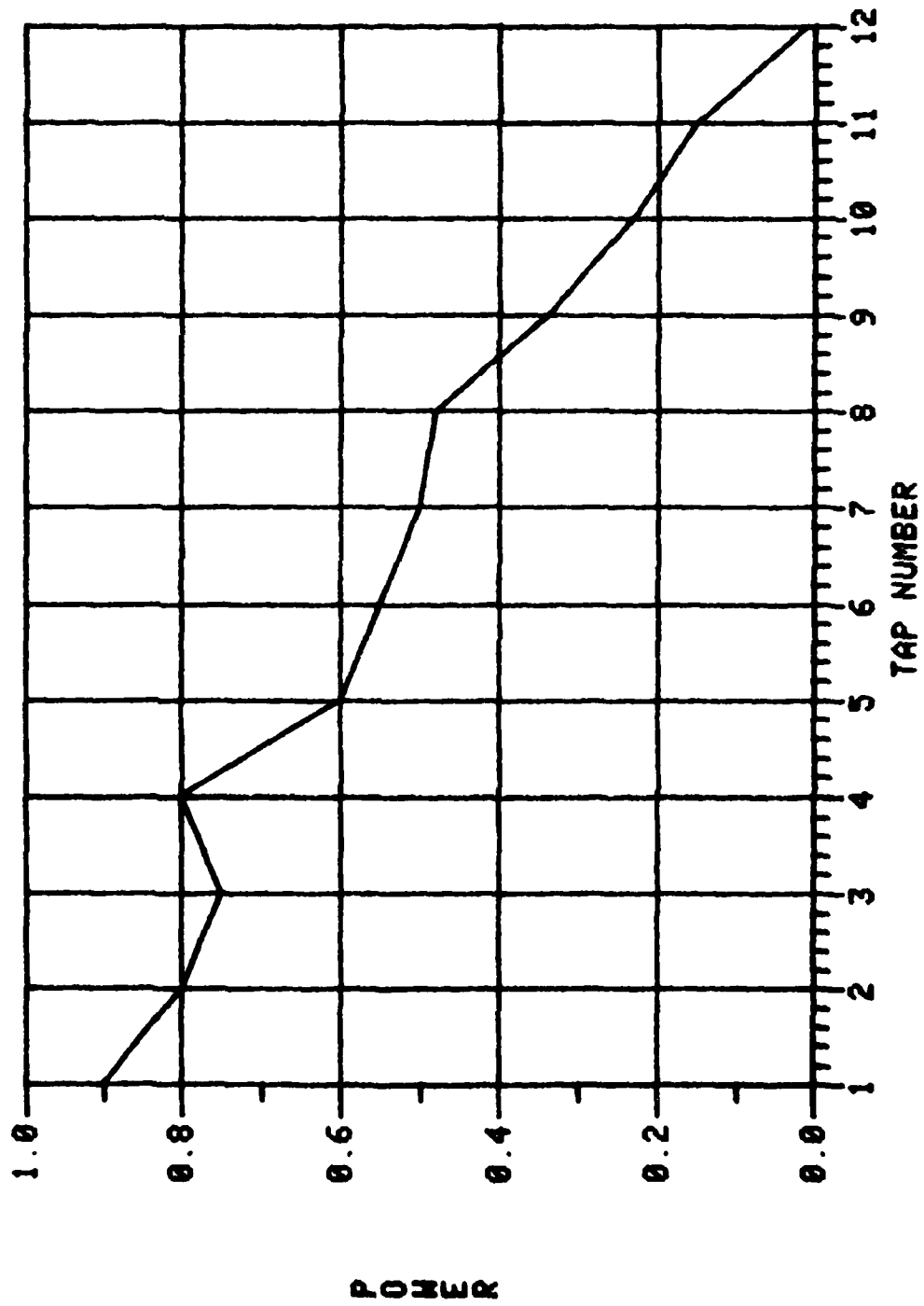
ENTER GAIN AS .XXXX

TAP 1 GAIN=.9
TAP 2 GAIN=.8
TAP 3 GAIN=.75
TAP 4 GAIN=.8
TAP 5 GAIN=.655
TAP 6 GAIN=.55
TAP 7 GAIN=.5
TAP 8 GAIN=.48
TAP 9 GAIN=.34
TAP 10 GAIN=.23
TAP 11 GAIN=.15
TAP 12 GAIN=.01

CHANNEL CORRELATION COEFFICIENT (0.10 - 0.95)=.4

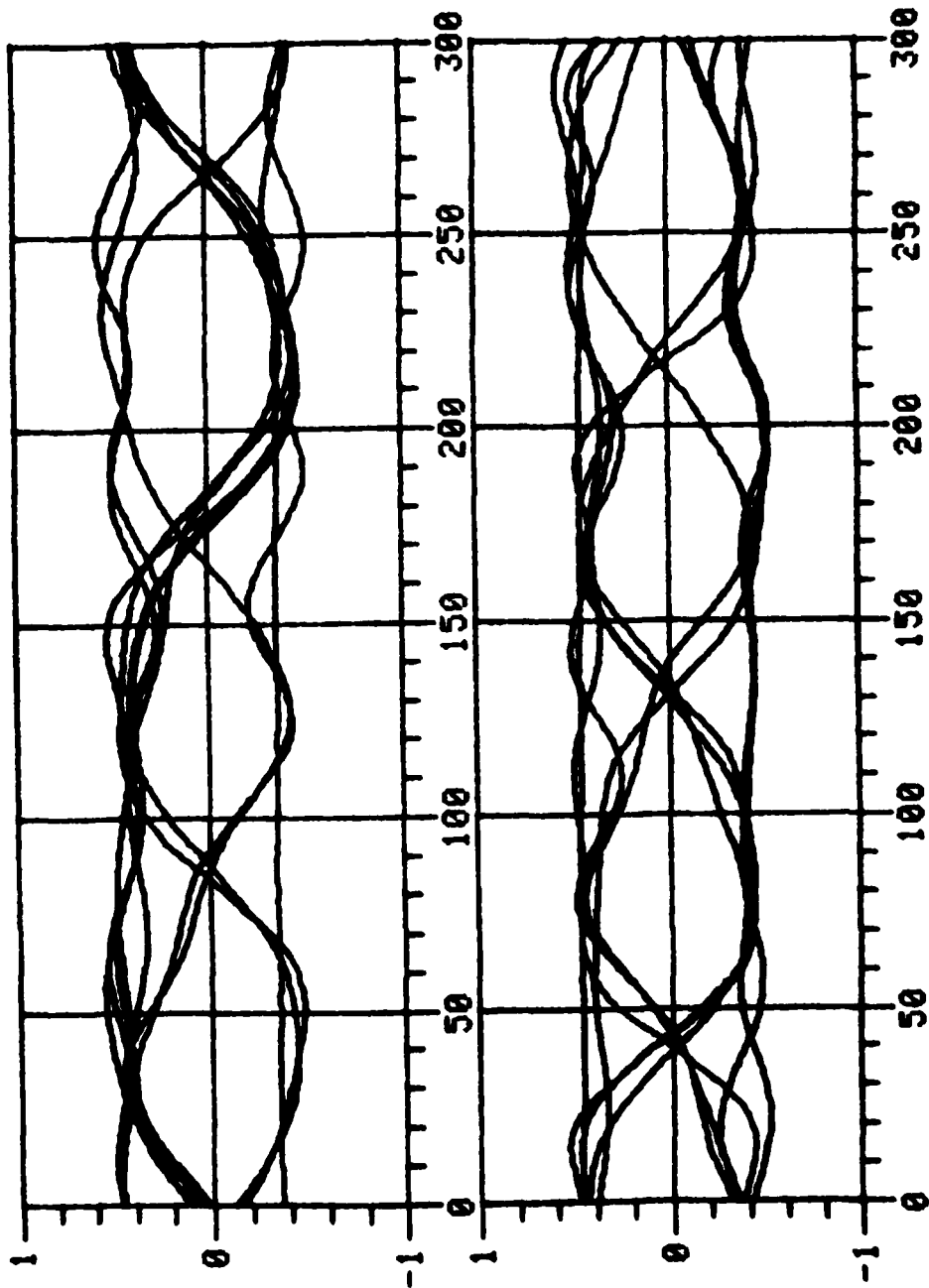
INTERTAP SPACING (0.1 - 1.0 BIT)=.6

POWER PROFILE PLOT



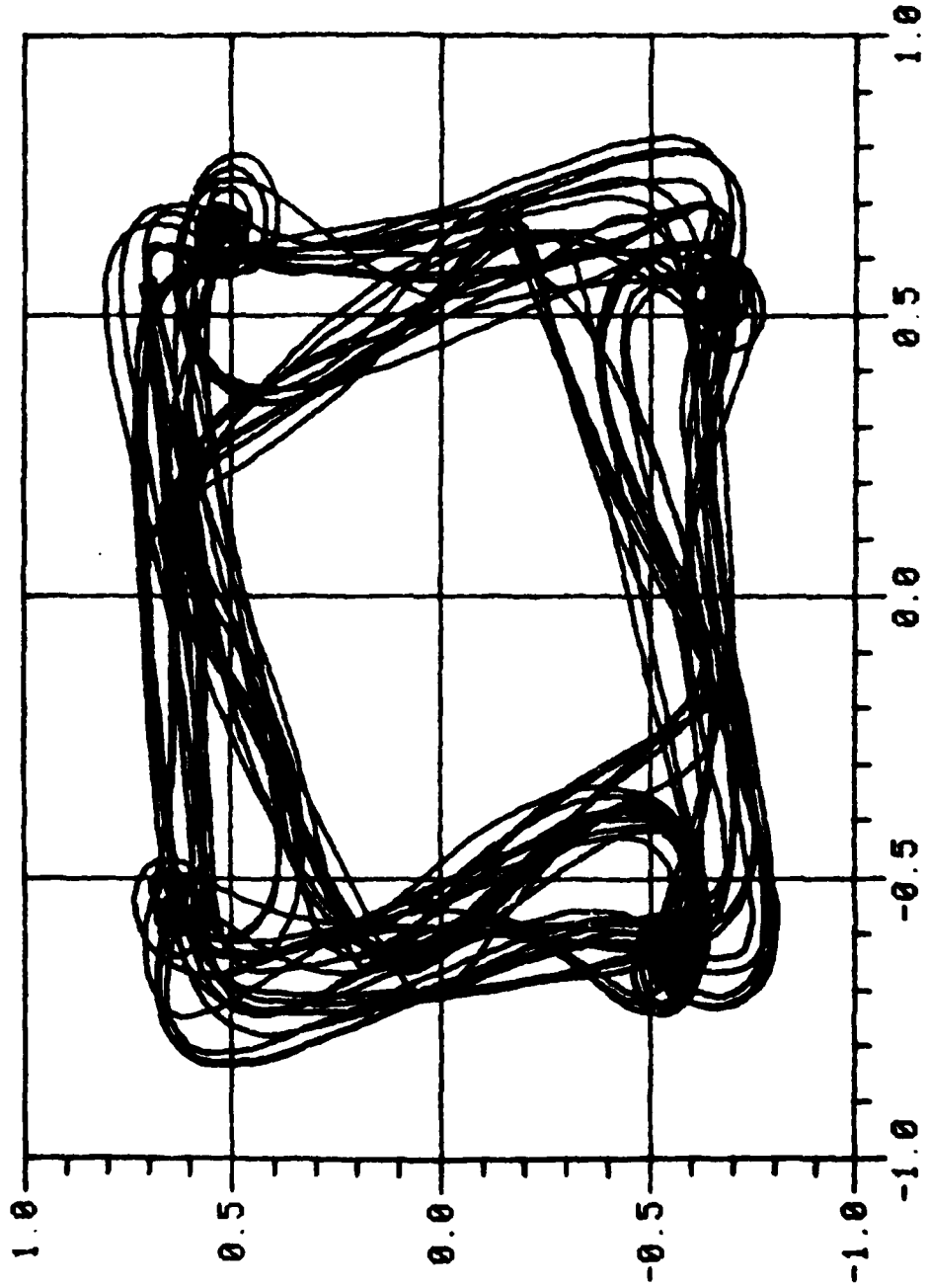
QPSK

EYE PATTERN
CHANNEL A



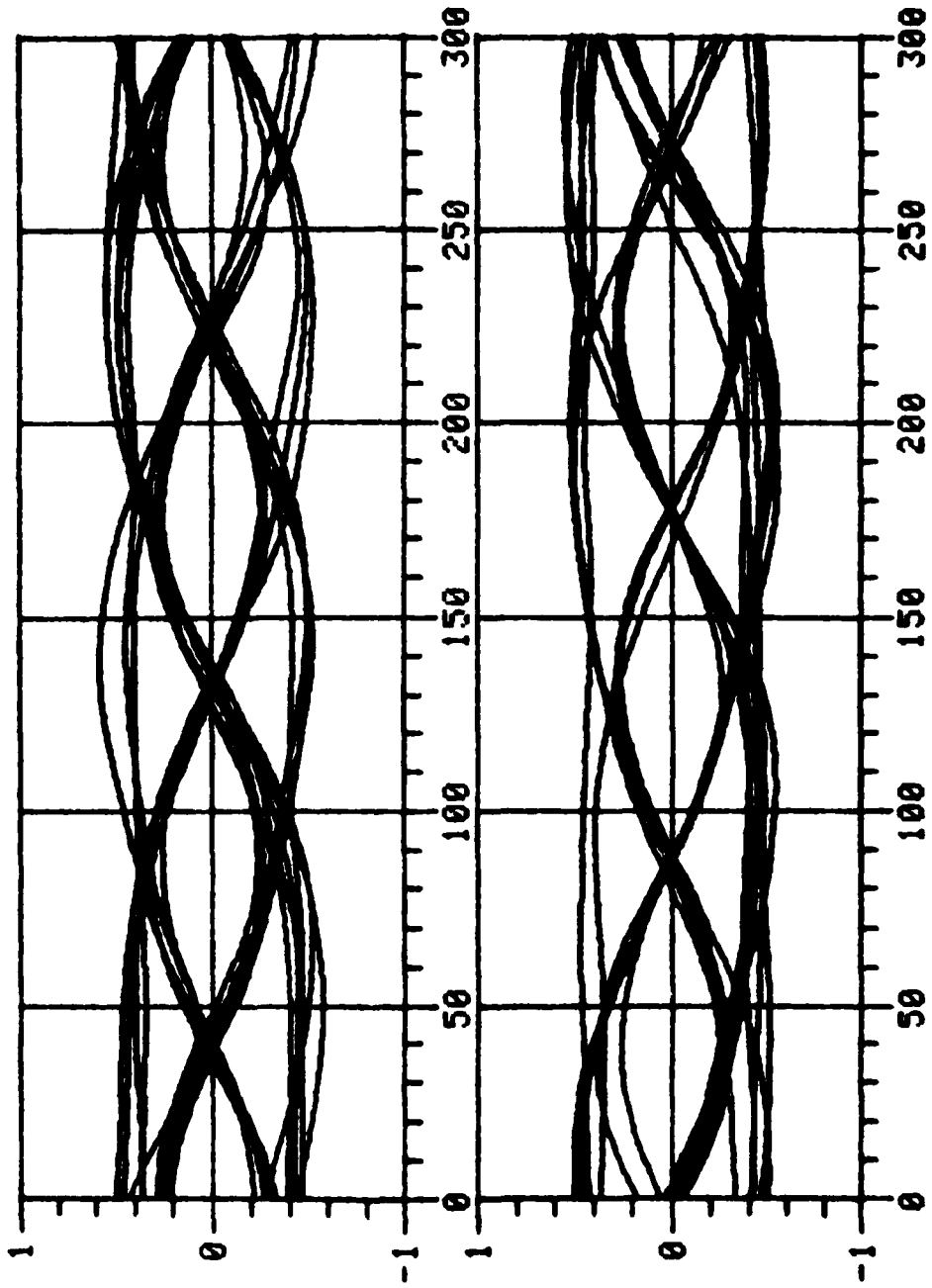
QFSK

CONSTELLATION
CHANNEL B



QPR

EYE PATTERN
CHANNEL B



QPR

CONSTELLATION
CHANNEL A

