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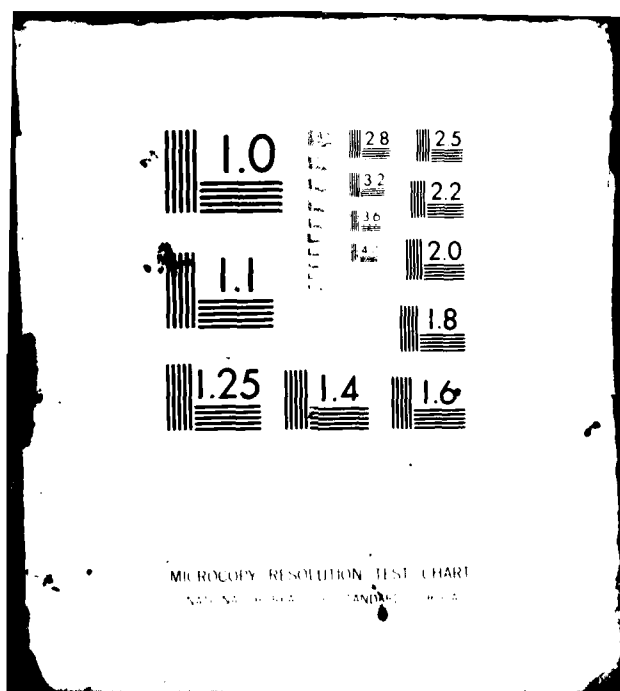
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Computational Sciences Laboratory  
Martin Marietta Corporation  
Post Office Box 5837  
Orlando, Florida 32855

February 1980

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Defense Communications Agency  
Defense Communications Engineering Center  
1860 Wiehle Avenue  
Reston, Virginia 22090

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| DRAMA<br>Line of Sight<br>Performance Monitors<br>Diversity Receivers                                                                                                                                                                                                                                                                                                                                                                  | Diversity Combiner<br>Hybrid Computer<br>Communication Systems<br>Equalizer | Simulation<br>Modeling                                                              |
| 20. ABSTRACT (Continue on reverse side if necessary and identify by block number)                                                                                                                                                                                                                                                                                                                                                      |                                                                             |                                                                                     |
| <p>This interim report describes and documents results of the first six months of hybrid computer simulations and communication systems modeling by Martin Marietta's Computational Sciences Laboratory in support of transmission systems for the Defense Communications Agency.</p> <p>This effort has included the modeling and simulation of the Dual Diversity DRAMA Radio, dual line-of-sight frequency selective fading and</p> |                                                                             |                                                                                     |

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20. ABSTRACT (Continued)

Rayleigh fading channels, signal quality monitors, diversity selection combiner. A baseband equalizer concept was modeled and simulated for incorporation into the simulation.

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## FOREWORD

This interim report describes and documents results of the first six months of communication systems modeling and hybrid computer simulations by Martin Marietta's Computational Sciences Laboratory in support of transmission systems for the Defense Communications Agency, Defense Communications Engineering Center, under contract DCA100-79-C-0048.

Models developed during this period have been programmed on one of Martin Marietta's hybrid computer systems. The current simulations utilize three modern industrial type analog computers, one modern digital computer, and an analog-to-digital/digital-to-analog interface.

Major accomplishments for this period have included the modeling and simulation of the dual diversity AN/FRC-170(V) DRAMA radio, dual line-of-sight (LOS) frequency selective fading and Rayleigh fading channels, signal quality monitors, diversity selection combiner, and baseband equalizers.

These simulations have been made accessible to personnel of the Defense Communications Engineering Center by a hybrid remote terminal at the engineering center in Reston, Virginia. This terminal, provided by Martin Marietta's Computational Sciences Laboratory, permits both configuration and parameter control from the Defense Communications Engineering Center. Several high level programs have been developed which allow the user at the Defense Communications Engineering Center to configure, change, and control the hybrid computer simulations at Martin Marietta Aerospace, Orlando, Florida, without requiring any knowledge of either hybrid or digital computer programming.

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## 1.0 INTRODUCTION

This report documents the first 6 months of a 12-month hybrid computer simulation study of a digital line-of-sight radio technique and frequency selective fading line-of-sight (LOS) channel. The simulated radio models the AN/FRC-170(V) radio which is part of the Digital Radio and Multiplexer Acquisition (DRAMA) Program. Also included in this effort are hybrid computer simulations of a baseband equalizer applique, signal quality monitors, and diversity switching alternatives. These simulations have been developed to evaluate performance of the DRAMA radio for Level I, 1 bit per hertz bandwidth efficient quadrature phase shift keyed (QPSK) transmission, and Level II, 2 bits per hertz bandwidth efficient quadrature partial response (QPR) transmission.

This study takes advantage of a previous QPR/QPSK hybrid simulation developed under DCA contract DCA100-77-C-0061. Proven hybrid computer models and user software developed for this previous effort have provided the baseline for this modeling and simulation study. Existing models for QPR/QPSK modulation and demodulation, fading channels, and signal processing have been modified and extended to simulate the DRAMA radio, frequency selective fading LOS channel, and signal quality monitors. Design data used in the DRAMA radio simulation has been provided by the government. In addition to the simulation effort, a remote hybrid computer terminal has been provided at the Defense Communications Engineering Center (DCEC), Reston, Virginia, for off-site study and monitoring of the DRAMA system modeling, simulation, and evaluation by the DCEC transmission systems engineering staff. To support this terminal capability, extensions to previous remote terminal

software have been made to allow additional parameter and configuration changes, faster response times, and to improve documentation of simulation analyses.

This report describes the results for the first five tasks in the statement of work for contract DCA100-79-C-0048. These tasks include simulation of the AN/FRC-170(V) DCS DRAMA radio, performance monitors, selection diversity combiner, frequency selective fading LOS channel, and adaptive equalizer applique. Each task is briefly described below.

Task 1 required the modeling and hybrid computer simulation of the AN/FRC-170(V) DRAMA radio using a QPR simulation, previously developed under contract DCA100-77-C-0061, as a baseline. Other requirements were the extension of this model to represent a dual diversity DRAMA terminal, the incorporation of government supplied AN/FRC-170(V) design data, and the provision for signal processing to accomplish the other tasks.

Task 2 included the modeling and simulation of offset threshold monitors and an AGC monitor for each of the dual diversity receivers. Two offset threshold monitors were modeled for each receiver with a capability to set different thresholds and bandwidths for each. When combined, these two offset monitors form the multiple offset threshold monitor. Each monitor has a threshold range of .1 to 1.0 bit amplitude and a bandwidth range of .01 to 10 Hz. The linearized AGC monitor has a bandwidth of .01 to 10 Hz.

Task 3 required simulation of the digital dual diversity selection combiner as provided by the U. S. Government and used in the AN/FRC-170(V) DRAMA radio. The diversity combiner utilizes outputs from the simulated performance monitors to derive diversity switch control. This control is based on an algorithm provided by the government. The diversity switch has

been programmed to operate without the introduction of bit errors or loss of bit count integrity due to the switching operation.

Task 4 required the modeling and simulation of the frequency selective fading LOS channel. This simulation was implemented using a 12 tap hybrid delay line using charge coupled devices and a crystal stabilized clock. Two channels have been mechanized and can be independent or correlated. The simulation user may vary the number of active taps, relative mean powers, intertap spacing (.1 bit to 1.0 bit), designation of stationary and fading taps, fade rate (.01 to 1 Hz), and correlation coefficient (.10 and .95).

Task 5 involved the modeling and simulation of an adaptive baseband equalizer applique for both QPR and QPSK transmission. The resulting simulation model is a decision feedback equalizer with a span of up to 3 taps. The simulation models a minimum mean square error equalizer at the receiver baseband. This simulation has been implemented so that the simulation user can configure the equalizer in terms of number of taps, bit duration per tap (.1 to 1 bit), and error signal loop bandwidth (.01 to 10 Hz).

The first six months of this simulation study have been devoted to the design and hybrid computer simulation of realistic models for the DRAMA radio and associated frequency selective fading LOS channel. The next six months will involve the integration of radio, channel, performance monitors, and diversity combiner, the verification of simulation models, and the evaluation of system performance for the baseband equalizer applique, performance monitors, diversity switch combiner, and transmission modes for various fading and noise environments.

## 2.0 DRAMA RADIO

This section describes the modeling and simulation of the line-of-sight radio, AN/FRC-170(V), which is being procured by the U. S. Army Communications Command under the Digital Radio and Multiplexer Acquisition (DRAMA) program. The radio model which is described in the following paragraphs has been developed using as a baseline the hybrid computer model for a quadrature partial response (QPR) radio simulation developed previously under DCA contract DCA100-77-C-0061. The QPR baseline model has been modified using government supplied design data for the DRAMA radio and has been simulated on a hybrid computer system. The resulting model represents a dual diversity DRAMA terminal which has two identical receivers, signal quality monitors, and a diversity combiner.

The hybrid computer model of the DRAMA radio includes the unique characteristics of this radio. These include Level I quadrature phase shift keyed (QPSK) performance rates to 13.065 megabits per second (MBS) and Level II quadrature partial response (QPR) performance at rates to 26.112 MBS. Other features are the switching of baseband filters for QPR and QPSK transmission, two and three level detection of the received baseband, and the signal processing required for measurement, signal quality, and diversity switch circuits peripheral to the radio.

The hybrid computer simulation of the DRAMA radio, frequency selective fading line-of-sight channel, and performance indicating circuitry provides a programmable scale model which may be configured and changed to evaluate performance and design for anticipated deployments. This model has been implemented by scaling down in time to permit simulation on the hybrid computer and use of

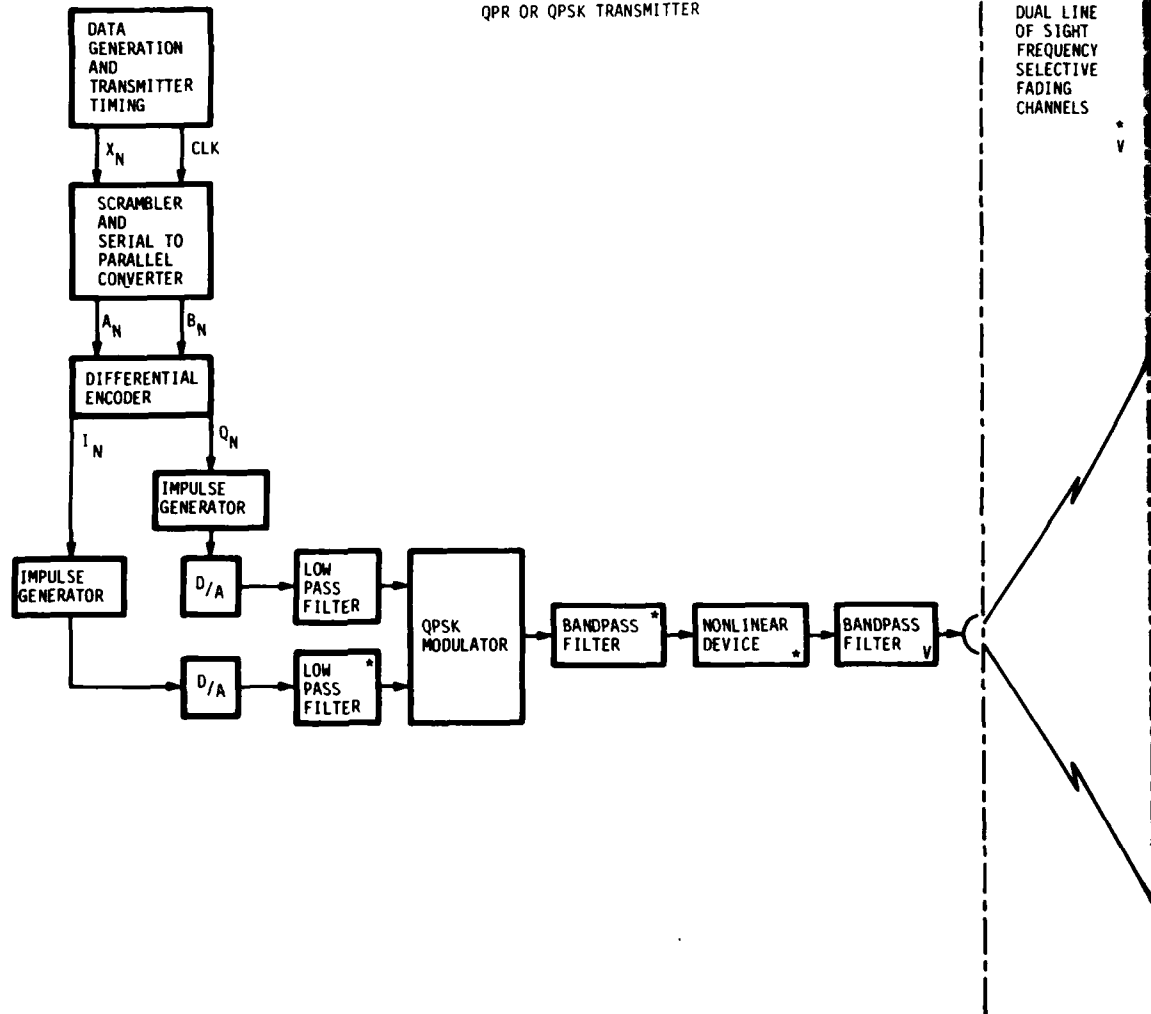
special purpose hybrid delay line hardware. Even with this time scaling, the hybrid simulation is 100 times faster and more efficient than digital simulation methods. The current scale factor for the DRAMA radio simulation is 26,112 which results in simulated IF, data rate, and baseband baud rate frequencies of 2,681 Hz, 1,000 Hz, and 500 Hz, respectively.

The DRAMA QPR/QPSK system simulation developed for this study is shown in Figure 2-1. This figure shows the major simulation modules for data generation, input data signal processing, QPR/QPSK modulation, transmitter signal processing, dual LOS fading channels, dual diversity receivers, data regeneration, performance assessment, and diversity combining. Both Level I, QPSK, and Level II, QPR, transmission and receiving can be accomplished with this model. Design parameters for filters, data rates, phase lock loops (PLL), nonlinear devices, and signal quality monitors have been accounted for in the simulation model. Validation of the DRAMA system simulation will be based on actual bit error measurements taken from the DRAMA radio prototype. Until this data becomes available, theoretical bit error performance data for QPR and QPSK transmission will be used as a guideline. Since the simulation on the hybrid computer tends to respond like the actual prototype, it is expected that simulated performance will be degraded from theoretical due to implementation losses. Figures 2-2 through 2-5 are typical theoretical noise and flat fading performance curves for PSK and QPR which will be used in the simulator verification process.

## 2.1 Data Input Model and Simulation

The data input module for the DRAMA radio is the same for both QPR and QPSK. This module includes a random data generator, 20-bit self-synchronizing scrambler, serial-to-parallel converter, and differential encoder. A functional

# QPR OR QPSK TRANSMITTER



AL LINE  
SIGHT  
FREQUENCY  
SELECTIVE  
CODING  
CHANNELS

# QPR OR QPSK RECEIVERS

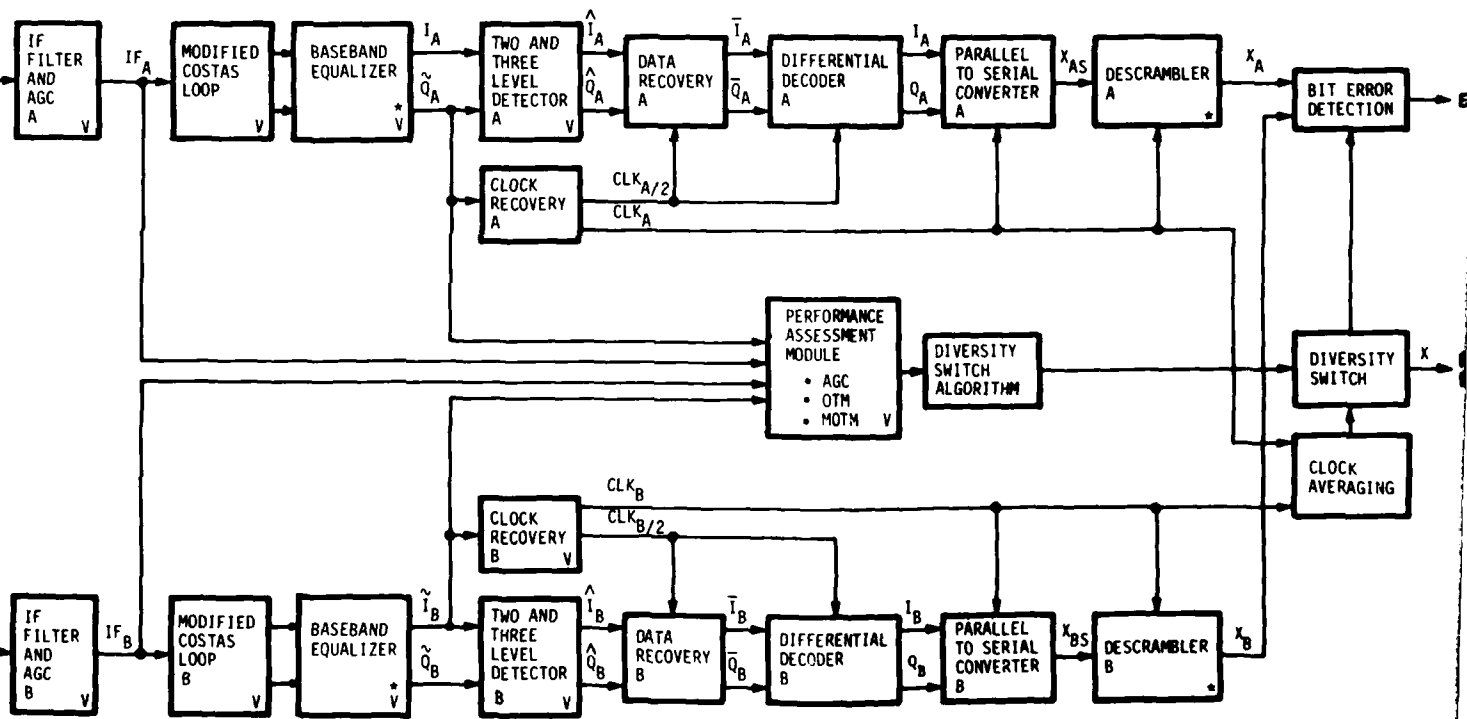


Figure 2-1. DRAMA LOS Simulation Model

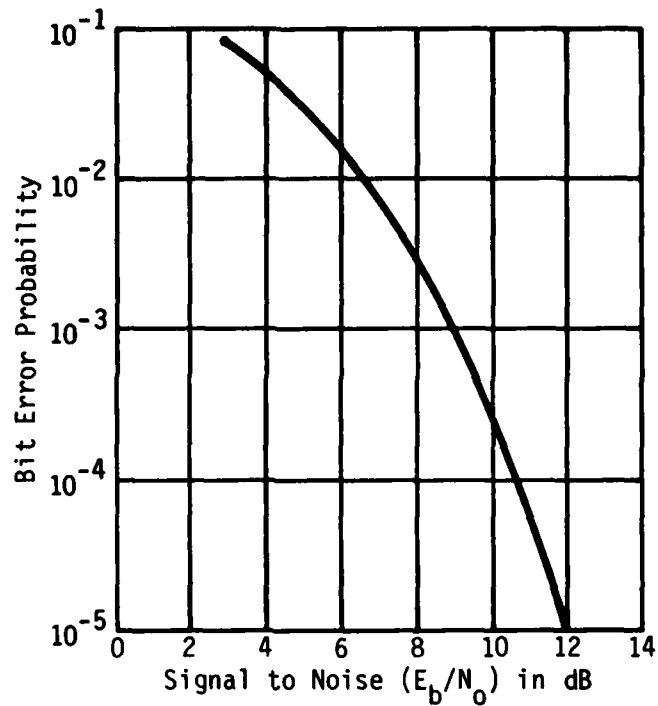


Figure 2-2. Theoretical QPR Noise Performance Under Additive Gaussian Noise Conditions

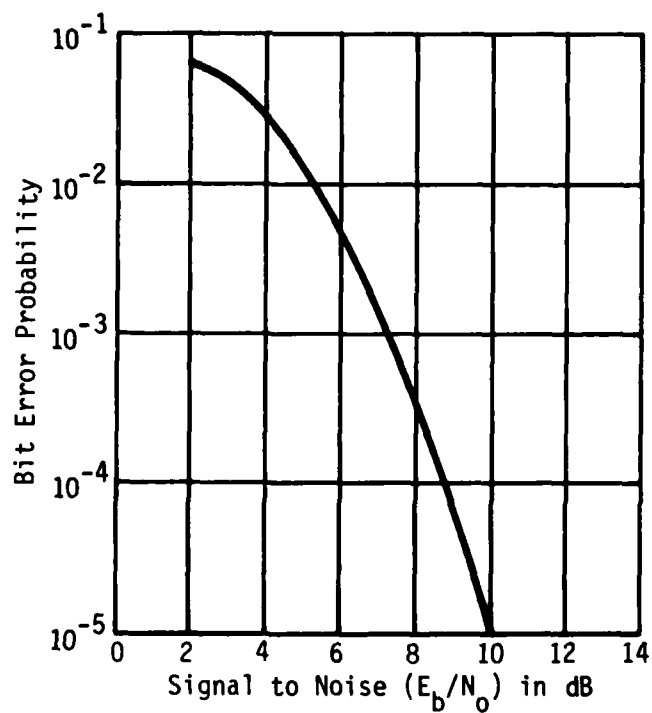


Figure 2-3. Theoretical QPSK Noise Performance Under Additive Gaussian Noise Conditions

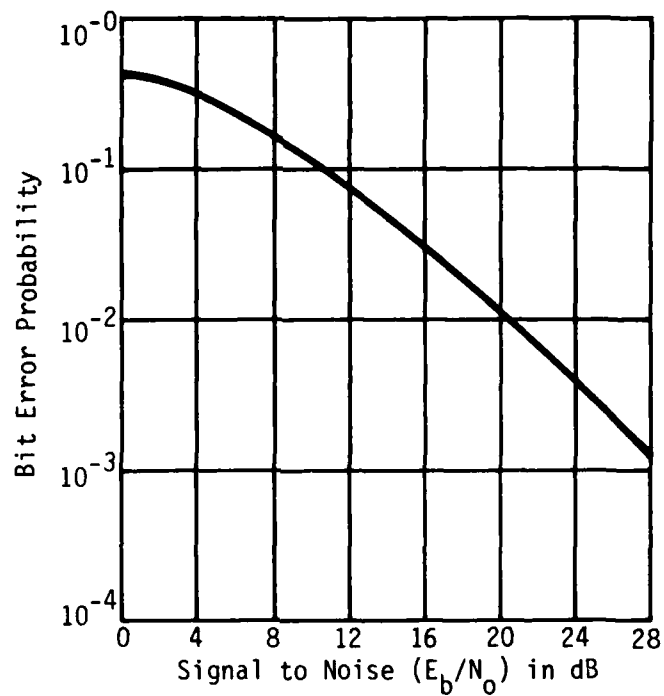


Figure 2-4. Theoretical QPR Rayleigh Fading Performance (Single Receiver)

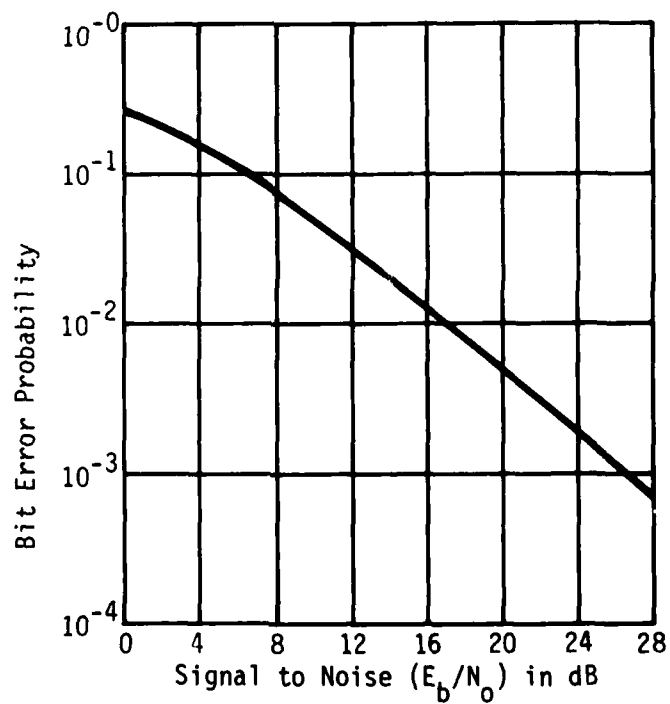


Figure 2-5. Theoretical QPSK Rayleigh Fading Performance (Single Receiver)

flow diagram for these circuits is shown in Figure 2-6. The data generator provides the pseudorandom data output which would be present at the multiplexer output ports. A self-synchronizing scrambler with 20 stages has been modeled to ensure a random modulating bit stream. This circuit, which eliminates long series of ones or zeros from occurring in the modulating bit stream, has been provided as an option and may be bypassed. The randomness guaranteed by implementing the scrambler results in a better spectral component of the bit rate clock at the receiver clock recovery circuit as a result of additional data transitions.

A model of the scrambler used in the DRAMA radio was obtained by modulo 2 summing the serial data stream with the modulo 2 sum of bits 17 and 20 of a 20-stage shift register. The scrambled or unscrambled data were input to the serial-to-parallel converter. The serial-to-parallel converter was mechanized by retiming the scrambler output with the symbol clock (one-half the data rate). To improve resolution of the two-phase ambiguity states at the receivers, the symbol timing clocks the I and Q data out with a one-half symbol delay with respect to one another. Each of these parallel bit streams was input to differential encoders which resolved any polarity inversion at the demodulator. These encoders were modeled as a modulo sum (exclusive "OR"). This circuit does a logical multiply of the feedback and data. Outputs from the two encoders provide the inputs to the modulation circuit.

Except for data generation which consists of a broadband noise source and analog sampler (track/store integrator), the entire data input module has been simulated using the parallel logic capability of the analog computer. Modulo 2 sums and differential encoders were programmed using a combination of gates and flip/flop delays. The scrambler uses five 4-stage

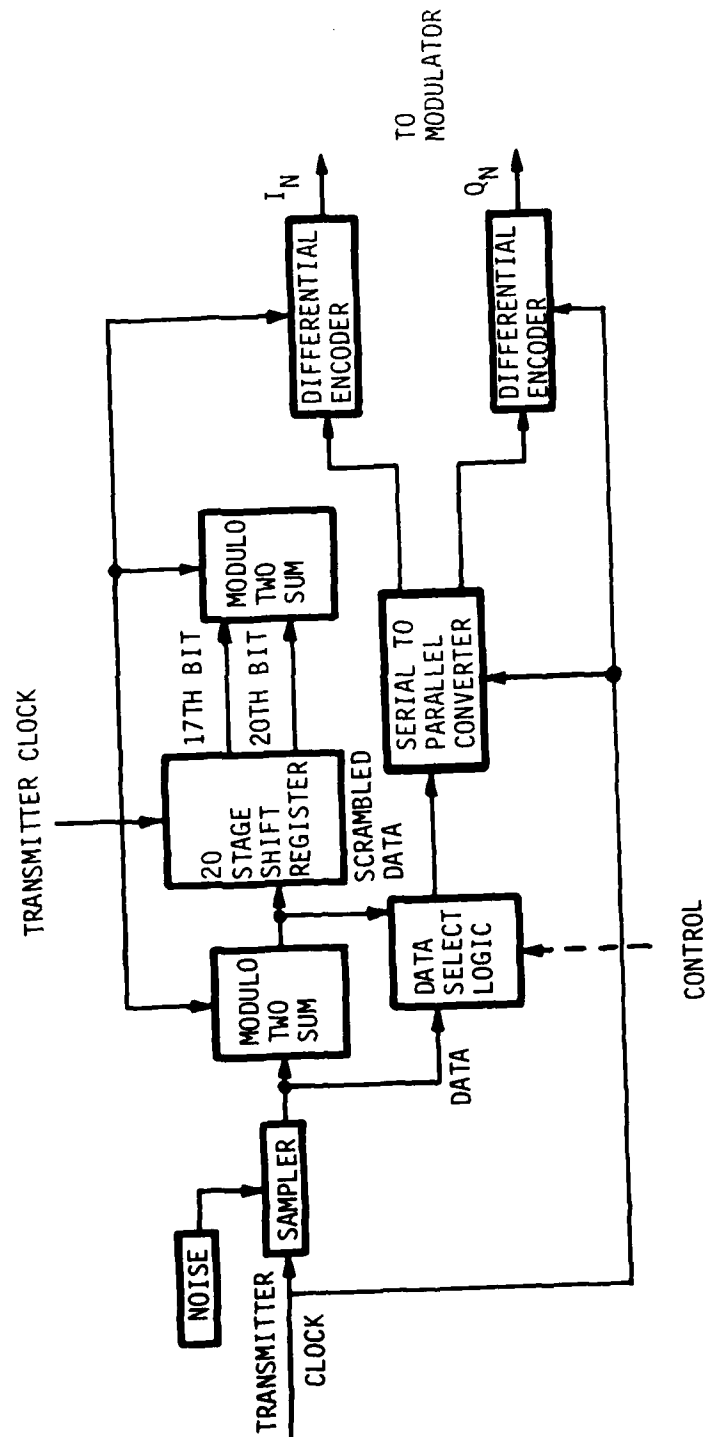


Figure 2-6. QPR/QPSK Data Input Model

shift registers in series to provide the 20-bit delay. Serial-to-parallel conversion was simulated by using flip/flops enabled by inverted symbol clocks to provide a one-half symbol delay between one symbol bit stream and the other.

## 2.2 QPR/QPSK Modulator Model and Simulation

The modeled DRAMA radio modulator section includes impulse generators for QPR transmission, digital-to-analog switches, transmit baseband filters, inphase and quadrature multipliers, and a crystal controlled reference oscillator. Input to the modulator module is from the I and Q differential encoders. Figure 2-7 is a functional flow block diagram of the major circuits for the modulator model. When QPR modulation is desired, the I and Q modulation signals are generated by using the encoded I and Q nonreturn to zero (NRZ) logic to drive impulse generators. Each impulse stream becomes the driving function for the Class I partial response filters.

If the QPSK modulation option is selected, a path is provided directly from the encoded I and Q NRZ data to the inphase and quadrature balanced modulators.

The partial response filters approximate a full cosine response to provide a controlled amount of intersymbol interference and combined with the receiver baseband filters produce a three level signal at baseband. For QPSK these filters are bypassed, although in the real system these filters are replaced with full response raised cosine filters. The reason for bypassing these filters in QPSK is that they have no effect on the performance of QPSK and are there for shaping of the rectangular baseband waveform before input to the phase shift keyed modulator. The processed baseband signals (two or three

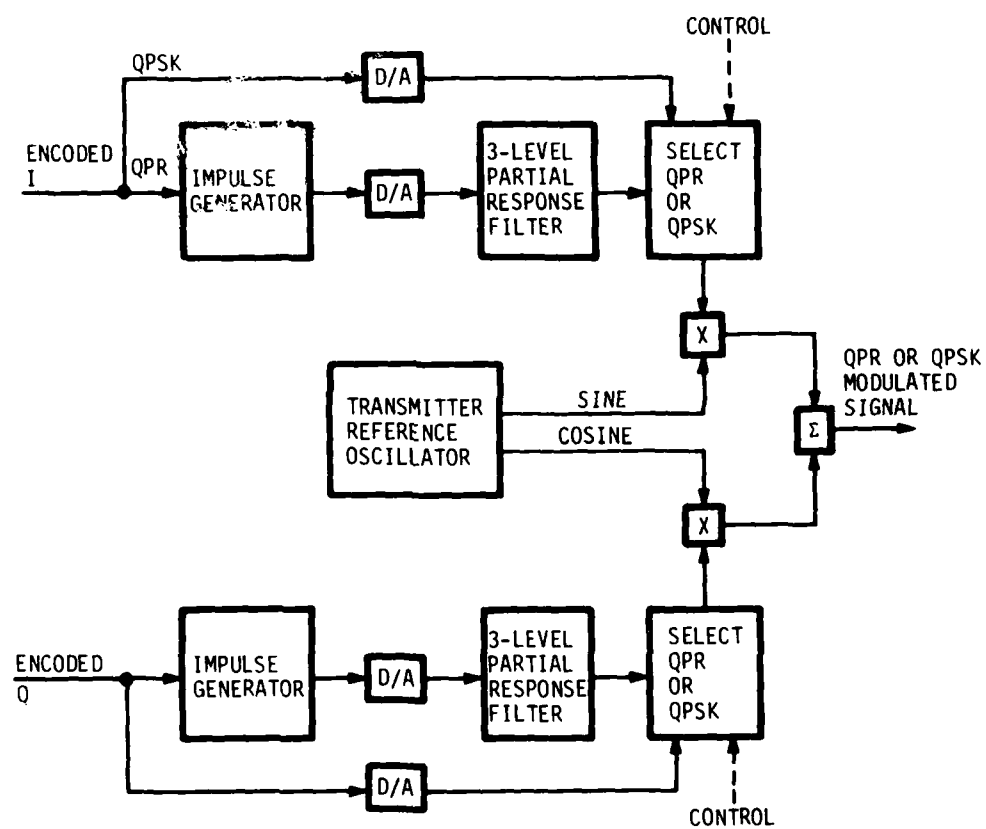


Figure 2-7. QPR Modulator

level) are input to separate balanced mixers (multipliers) along with the sine and cosine outputs from the reference oscillator (sine for the I channel and cosine for the Q channel). These mixer outputs are then summed to generate either QPR or QPSK signaling. Since the partial response filters are the most critical part of the QPR model, they are discussed further in following paragraphs.

The transmit partial response filters are programmed from the transfer function:

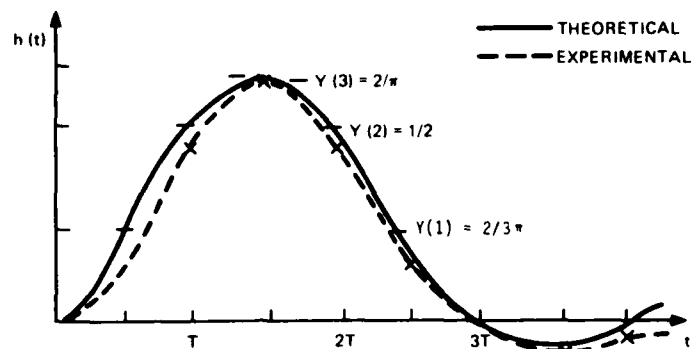
$$H(s) = \frac{3.25104}{s^4 + 4.3966s^2 + 9.28835s^2 + 8.105s + 3.25104}$$

Analog computer techniques for transfer function simulation are used to model these filters.

The partial response filters are designed to fit the frequency and the impulse response of a Class I, partial response filter. This approach ensures the desired intersymbol interference with adjacent pulses and prevents undesired intersymbol interference with other pulses.

The impulse response for the partial response filter is shown in Figure 2-8. This filter was mechanized as two identical fourth order stages, as shown in Figure 2-9. The first half is in the transmitter and the other half in the receiver.

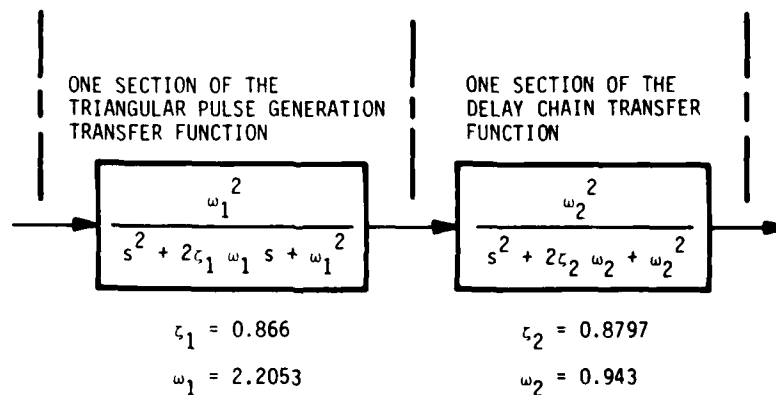
The filter design was derived from a method based on the piecewise linear approximation to the impulse response curve shown in Figure 2-8.  $Y(1)$ ,  $Y(2)$ , and  $Y(3)$  are the ordinates of the curve for the equally spaced sample points. The system block diagram resulting from this approach is shown in Figure 2-10. This system was mechanized, allotting fourth order transfer



$$h(t) = \frac{1}{2} \left\{ \frac{\sin \omega_c (t-T)}{\omega_c (t-T)} u(t) + \frac{\sin \omega_c (t-2T)}{\omega_c (t-2T)} u(t-T) \right\}$$

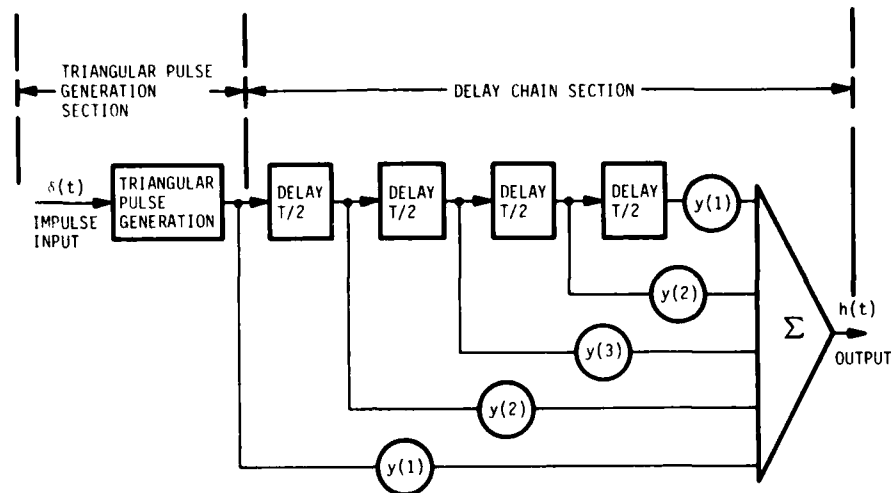
WHERE  $\omega_c$  IS THE FILTER CUTOFF FREQUENCY

Figure 2-8. Partial Response Filter Impulse Response,  $h(t)$



WHERE  $s$  IS SCALED TO THE FILTER CUTOFF FREQUENCY

Figure 2-9. Partial Response Filter, Transmitter, and Receiver Filter Transfer Functions



$$H(s) = T(s) \left\{ y(1) + y(2)e^{-sT/2} + y(3)e^{-2sT/2} + y(2)e^{-3sT/2} + y(1)e^{-4sT/2} \right\}$$

Figure 2-10. Partial Response System

functions to the triangular pulse generator and the delay chain, each formed as the square of a second order transfer function. Thus the identical transmitters and receiver filters are formed from second order parts of the triangular pulse generator and delay chain.

The triangular pulse generator impulse transfer function is given by

$$T(s) = \frac{T}{2} \left[ \frac{1 - e^{-sT/2}}{s} \right]^2 \approx \left[ \frac{\omega^2}{s^2 + 2\zeta\omega s + \omega^2} \right]^2$$

and its approximation was formed by equating the first few terms of the Taylor series for each. The resulting second order transfer function is shown in Figure 2-9.

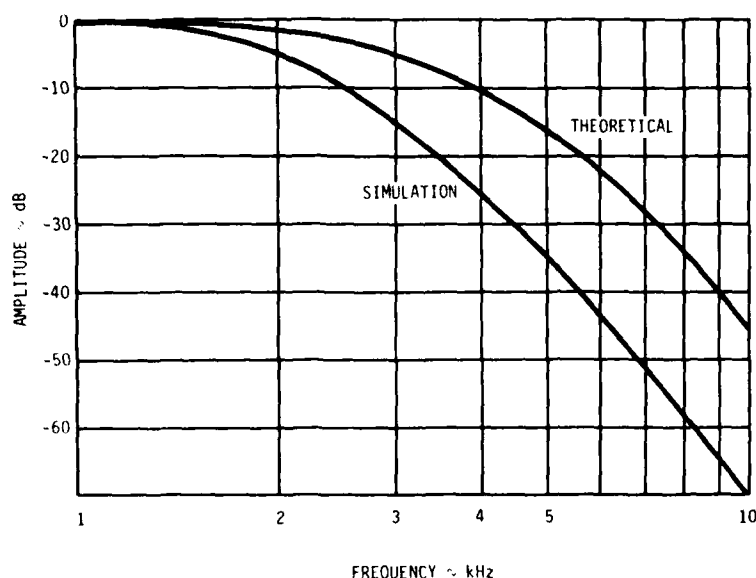


Figure 2-11. Frequency Response Plot of the Composite Partial Response Filter

The delay chain transfer function may be rewritten from that shown in Figure 2-9, utilizing the symmetry about the peak of the partial response impulse response. If the sampled values are substituted, the response magnitude is found to be the first three coefficients of the Fourier series for the magnitude of the cosine filter.

In this light, the delay chain transfer function was formed by equating the first two forms of the Taylor series for the squared magnitude of a second order system and for the desired cosine response. The resulting second order transfer function is shown in Figure 2-10.

The mechanized filter was adjusted to give the desired impulse response. It has a bandwidth of three symbol pulsewidths and is essentially symmetrical about the peak. The filter has minimum intersymbol interference at the third and fourth symbol pulse times. The impulse response is shown in Figure 2-8 and frequency response of the filter is shown in Figure 2-11.

The modulator circuits have been programmed using both logical and analog computer techniques. Programs developed for the modulation function and all other functions of the DRAMA radio simulation are under the control of the digital computer. This facilitates the parameter and configuration changes, setup procedures, and data acquisition.

Encoded I and Q digital baseband signals are input to impulse generators if in a QPR mode and to the quadrature multipliers if in a QPSK mode. The impulse generators were mechanized using monostable elements (one shots) of the parallel logic on the analog computer. These devices have an adjustable pulsewidth which has been set to provide the desired impulse response from the partial response filters. The QPR or QPSK digital NRZ modulating signals are input to electronic digital-to-analog switches that generate plus and minus analog dc levels corresponding to the +1 and -1 logic.

If QPR has been selected, these signals drive the I and Q transmit half of the partial response filters. These filters have been mechanized using analog integrators, summing amplifiers, and digitally set coefficient attenuators. The analog simulation of one of these fourth order partial response filters is shown in Figure 2-12. This filter models the transfer function shown in Figure 2-9. The actual implementation of this filter in the real system is a seventh order elliptical function which also approximates the full cosine response. Since data on these filters are not currently available, the fourth order filters derived above have been implemented for the simulation model.

When QPSK is selected, the digital computer sends control signals to the analog computer, which gates the encoded baseband signals directly to

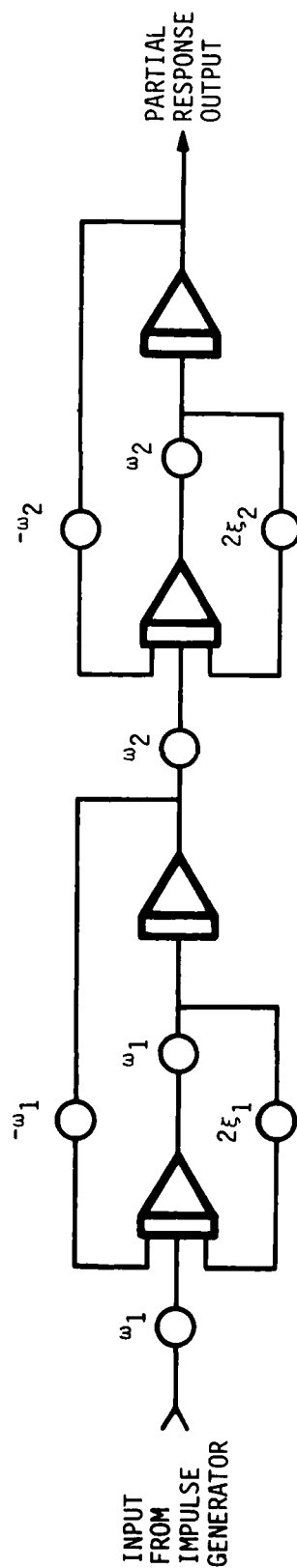


Figure 2-12. Analog Simulation of Partial Response Filter

the electronic switches and bypasses the partial response filters. The processed I and Q baseband signals are then input to four quadrant analog multipliers that multiply the I and Q baseband with sine and cosine signals from the reference oscillator. The summation of these two multipliers results in either QPR or QPSK signaling, as determined by the simulation user. A reference oscillator for this modulator section has been programmed using two analog integrators with feedback to stabilize the amplitude and a crystal controlled digital clock to maintain a fixed frequency.

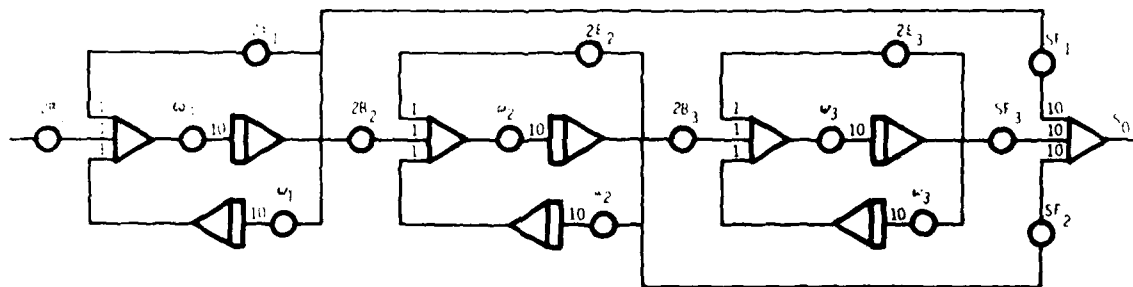
### 2.3 Transmission Model and Simulation

A typical transmission configuration has been modeled for the DRAMA radio. This configuration includes two transmitter bandpass filters for spectral limiting and a TWT power amplifier. All of these devices were modeled on the analog computer and can be configured by the simulation user. This RF portion of the transmission has been simulated without the up and down conversion to RF frequencies; thus, the simulation is at IF frequency. The reasons for this omission are faster computations, allowing for more detailed simulation of more important circuits, and it does not degrade the simulation accuracy or realism.

Optional spectral control bandpass filters and an optional nonlinear amplifier have been simulated for the transmission module. The two bandpass filters have been programmed to permit the selection of either Butterworth, Bessel, or Chebychev characteristics for two, four, or six poles. These filters, programmed on the analog computer, are controlled digitally by the simulation user. A stagger-tuned approach has been taken, where the

parameters for each stage are calculated and set by the digital computer. The center frequency, ripple and bandwidth of the filter are specified by the user. The digital computer then calculates and adjusts the center frequency and bandwidth of each stagger-tuned section to produce the desired overall frequency response of the filter.

Referring to Figure 2-13, the filter parameters  $\beta$ ,  $\xi$ , and  $\omega$  of each stage represent the gain bandwidth product, bandwidth, and center frequency, respectively.  $SF_1$ ,  $SF_2$ , and  $SF_3$  are the scale factors that adjust the overall gain of the filter to ensure unity gain and select the order of the filter.



SIMULATES SECOND, FOURTH, OR SIXTH ORDER  
 CHERYSHEV, BUTTERWORTH, OR BESSEL BANDPASS FILTER.

Figure 2-13. Bandpass Filter Simulation

The nonlinear device simulation models the AM/AM and AM/PM characteristics of the DRAMA radio TWT. Figure 2-14 shows the simulation of this function, using analog computing elements and card programmed diode function generators. The modulated carrier is input to an envelope detector, which determines the time-varying amplitude of the carrier by diode-detecting the signal magnitude and filtering out the carrier frequency. This amplitude output drives two function generators that are programmed with the AM/AM and AM/PM characteristics of the nonlinear device. The output of the AM/PM function generator determines the time constants for an analog computer programmed phase shifter that shifts the modulated carrier by the appropriate computed phase angle. The AM/AM function generator drives a gain circuit that multiplies the modulated carrier by the corresponding gain. AM/AM and AM/PM characteristics simulated for the TWT are shown in Figures 2-15 and 2-16.

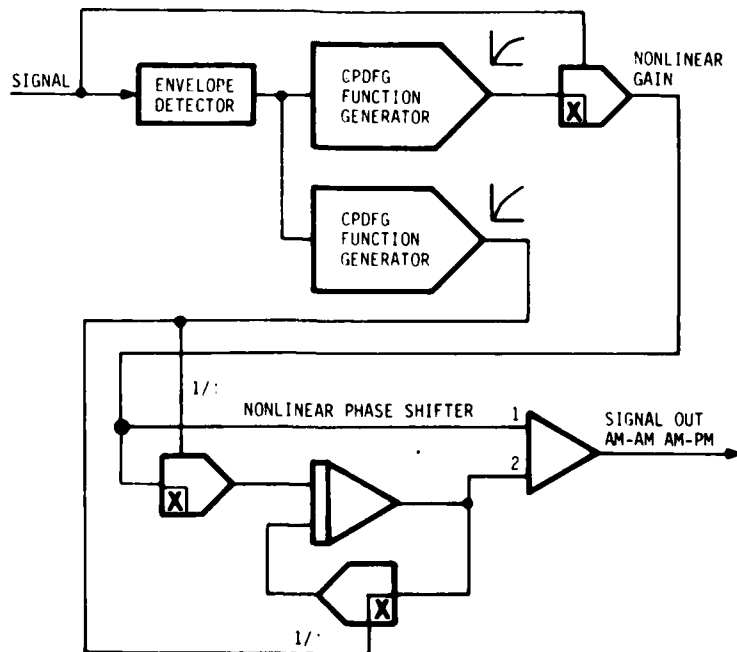


Figure 2-14. Nonlinear Device Implementation

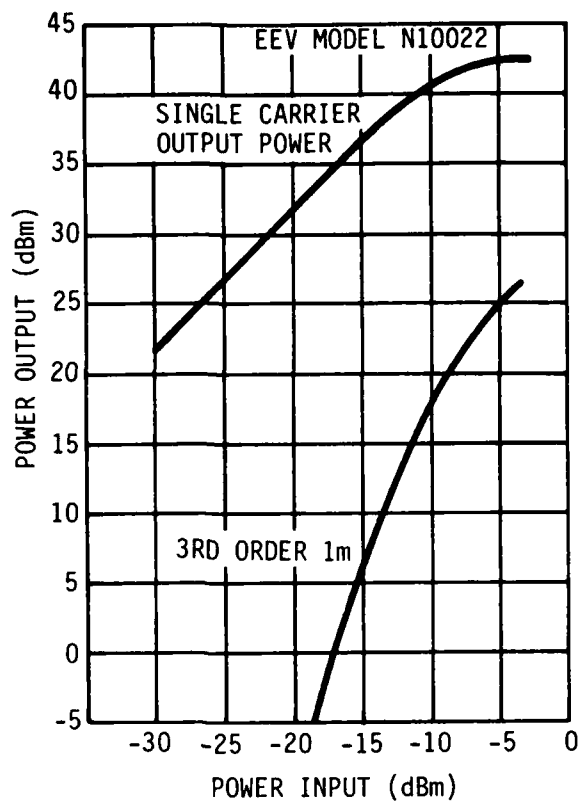


Figure 2-15. TWT AM/AM Characteristic

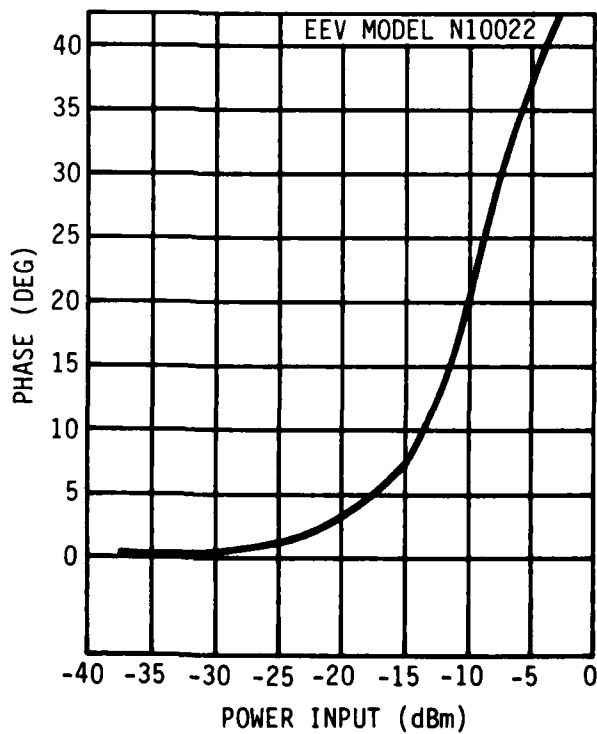


Figure 2-16. TWT AM/PM Characteristic

#### 2.4 Model and Simulation of Receiver IF

The DRAMA dual-diversity receiver simulation is composed of two identical receiver chains, each of which includes an IF and AGC section, modified Costas loop demodulator, three-level detection for QPR and two-level detection for QPSK, bit timing recovery, and data regeneration.

Each of the DRAMA receiver models has an IF and AGC section that preprocesses the received signal from the antenna using bandpass filtering and automatic gain controls. In the actual system the received antenna signal passes through an additional RF filter, which is used to eliminate noise outside the bandwidth of interest, before down conversion to the IF frequency. This RF processing has been eliminated in the simulation model for the same reasons that were given in Section 2.3.

The modeled IF filter model is a 6-pole bandpass filter with a variable bandwidth. Nominal bandwidth for a data rate of 26.112 Mb/s is 40 MHz. The AGC circuit for the real system and model has a dynamic range of >60 db.

Figure 2-17 illustrates the analog computer program for one of the two identical IF and AGC sections. The simulated IF filters and automatically controls the gain of the received transmitted signal plus noise. Nominal values for the actual IF filter center frequency and bandwidth are 70 MHz and 40 MHz, which are 2681 Hz and 1723 Hz for the simulated filter. The IF bandpass filter simulated on the analog computer has been programmed to model the characteristics of Butterworth, Bessel, or Chebychev bandpass filters up to six poles. User programs have been developed to permit parameter changes for bandwidth, center frequency, ripple factor, and filter order.

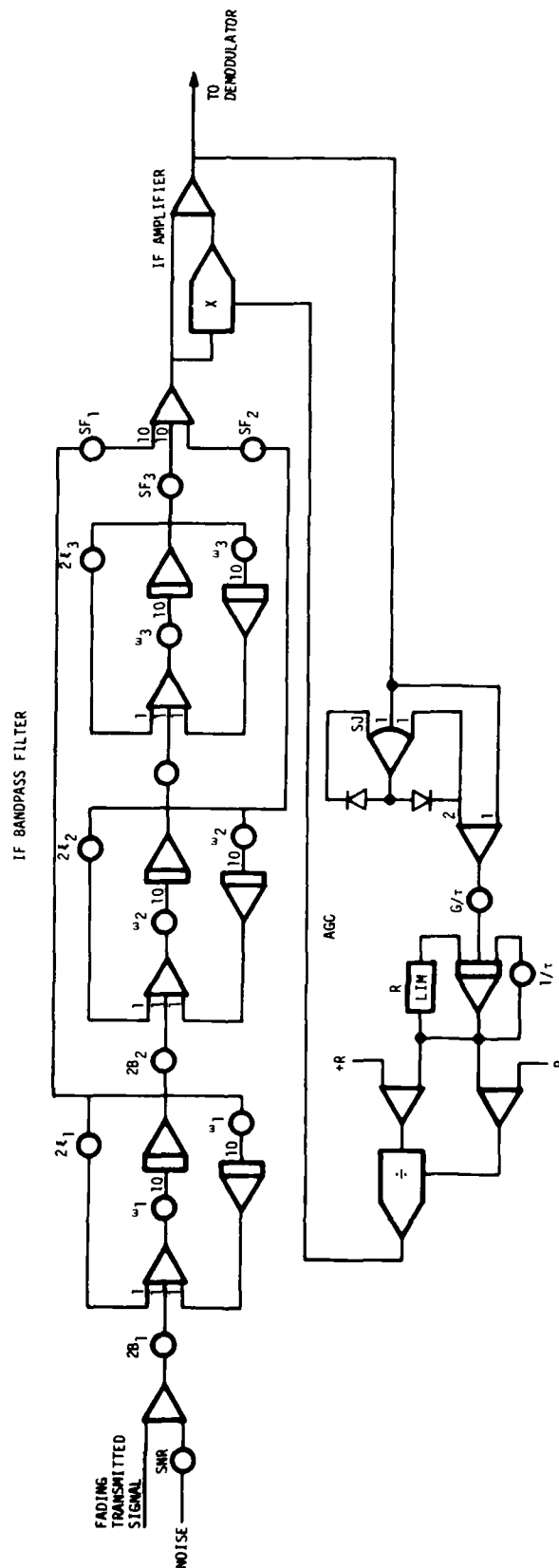


Figure 2-17. Simulation Model of AGC/IF

The AGC for each IF section was mechanized using a full-wave rectifier, low-pass filter, divider, and multiplier. Each IF signal was full-wave rectified and filtered with a low-pass filter (variable time constant normally equal to five times highest fade rate) to detect the received IF amplitude. This variable was input to a divider whose ratio determined a gain to increase the IF signal amplitude to its nominal value. The divider output controls the gain of the output IF amplifier through a multiplier with a range of 0 to 60 db.

#### 2.5 Modeling and Simulation of Modified Costas Loop

The DRAMA radio uses a coherent demodulation technique which makes hard decisions on the filtered baseband and detects cross channel contamination between the I and Q demodulated symbol streams to phase lock a voltage controlled oscillator. Demodulation is achieved using phase detectors to extract the modulating signal. These phase detectors multiply the received IF signal and quadrature components of the phase locked reference oscillator. Outputs of the I and Q phase detectors drive partial response, full cosine filters for QPR and full response raised cosine filters for QPSK. The phase lock loop uses a cross correlation between the quadrature symbol streams low-pass filter outputs and hard decision estimates to generate a loop error signal. A cross correlation difference between the filtered I baseband and estimate of Q and between the filtered Q baseband and estimate of I is filtered and input to the reference VCO to phase lock it to the modulated carrier. The data estimation circuits provide two-level decisions for QPSK and three-level decisions for QPR. Baseband filter bandwidths are set to one-half data rate for QPSK and one-fourth data rate for QPR.

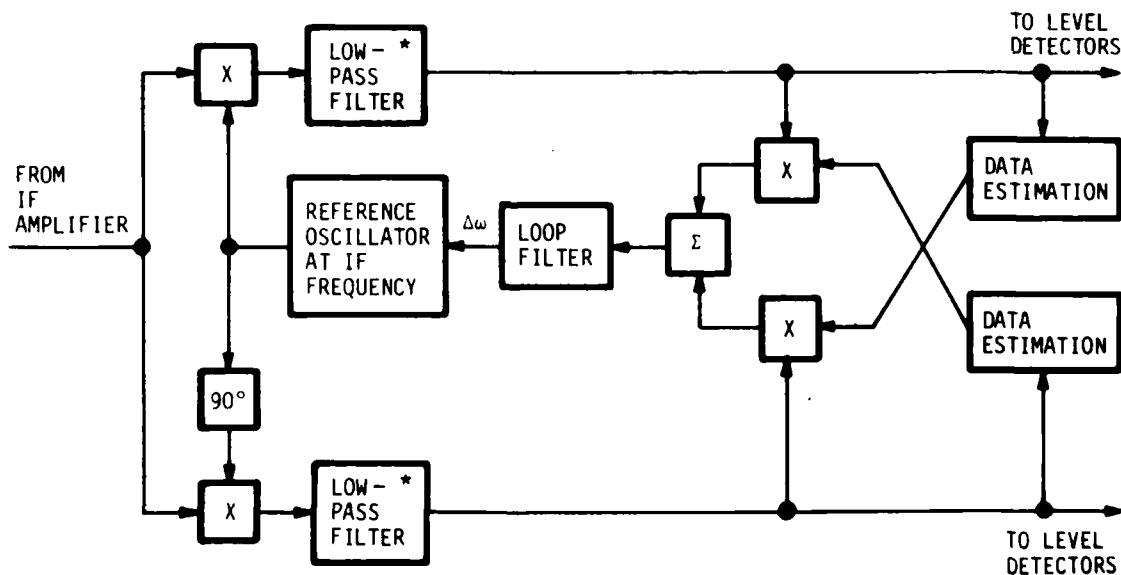
Two of the described modified Costas loops have been simulated on the analog computer, one for each of the dual diversity receivers. This circuit accepts the simulated IF transmitted signal and coherently demodulates either QPSK or QPR, depending on modulation technique selected. For QPR the low-pass filters following the phase detectors are complements to the transmit partial response filters. The transfer function used for these filters is

$$H_r(s) = \frac{3.25104}{s^4 + 4.3966s^3 + 9.28835s^2 + 8.105s + 3.25104}$$

For the QPSK mode the filter is modified to approximate a full response with linear phase. Use of a fourth order Butterworth low-pass filter produces a two-level baseband signal instead of the three-level signal for QPR. The modified Costas loop modeled on the analog computer is shown in Figure 2-18.

Phase detection of the modulating signal was simulated by using analog quarter square multipliers to multiply the received IF and phase locked reference to recover the baseband signal. Low-pass filters for the I and Q baseband data streams were mechanized similar to those described in Section 2.2. These filters, partial response for QPR and full response for QPSK, filter out spurious components resulting from the multiplication, leaving the difference frequency which is the baseband. These filtered baseband signals drive the data estimation circuits and cross channel I and Q multipliers. Data slicers for the data estimation and data recovery

circuits were mechanized using analog slicing circuits to determine upper, lower, and center for QPR and upper and lower for QPSK. Peak detectors were programmed on the analog computer to determine slicing levels and to threshold detect the signaling for either QPR or QPSK. The hard decisions from the data estimations of the I and Q basebands are  $\pm 1$  for QPSK and  $+1, 0, -1$  for QPR. Cross-coupling contamination products was obtained from the multiplication of the filtered baseband I and Q signals and an estimation of their value. The resulting signals were differenced using a summing amplifier on the analog computer and filtered by a lead/lag filter. This filter output was used to drive the analog programmed VCO carrier reference. The resulting PLL is a Type II second order loop. Nominal parameters for the simulation of



\*COMPLEMENT OF TRANSMIT  
PARTIAL RESPONSE FILTER  
IN QPR MODE

Figure 2-18. Modified Costas Loop Demodulator Model

this filter are a gain of 5, damping of 0.707, and a bandwidth of 0.651 Hz. The scaled bandwidth corresponds to a real-time loop natural frequency of 17.0 KHz.

## 2.6 Two- and Three-Level Detection

To accommodate either QPSK or QPR required both two-level and three-level detection of the baseband data. This simulation is shown in Figure 2-19. For QPR each of the demodulated I and Q baseband signals was input to plus and minus level detectors which, combined with threshold or slicing level coefficients, form the upper and lower slicing levels. These slicing levels and the baseband signals are input to comparators for detecting the presence of +1, 0, and -1 data from the demodulated baseband signals. For QPSK, the slicing coefficients are set to zero, and only the upper comparator is used to detect the binary baseband +1, and -1.

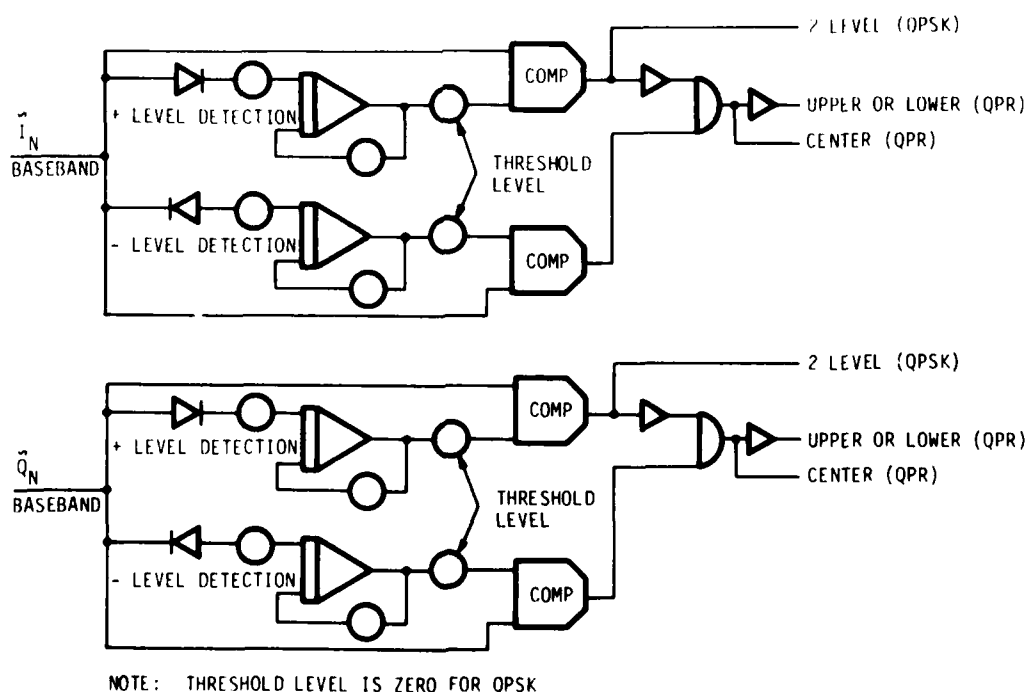


Figure 2-19. Two- and Three-Level Detection Simulation

The detected three levels for QPR are input to logic circuits that sample the received baseband data at the instant of zero crossover of the baseband eye, using timing from the receiver clock. For QPR, a +1 or -1 represents a recovered zero, and zero represents 1. For QPSK, where the baseband data are sampled during the period of maximum response, +1 represents a recovered 1, and -1 represents zero.

## 2.7 Receiver Clock Simulation

The bit timing recovery circuit for the line-of-sight modem provides synchronization for the data recovery circuits. This model, shown in Figure 2-20, uses an analog phase-locked loop to phase-lock a reference oscillator to one of the baseband signals. The I-channel baseband was chosen for this simulation. This baseband analog signal was sliced to produce a  $\pm 1$  square wave from which a good spectral line amplitude at the baseband frequency was obtained by using a logical one-shot. The signal from the one-shot was analog-to-digital converted and input to a phase detector (multiplier) together with the clock reference oscillator. The resulting phase error was filtered using a lead/lag circuit to obtain a dc component,  $\Delta\omega$ , which phase-locked the reference clock to the received data. The lead/lag filter provided a Type II, second order, phase-locked loop. The parameters of the filter are a gain of 1, damping of 0.707, and a cutoff frequency of 0.651 Hz, which corresponds to an actual system cutoff frequency of 17 KHz.

## 2.8 Data Recovery Modeling and Simulation

Data recovery for the DRAMA radio requires differential decoding of the received digital bit stream if QPSK modulated (if QPR, this function is bypassed), parallel-to-serial conversion to combine the two symbol streams,

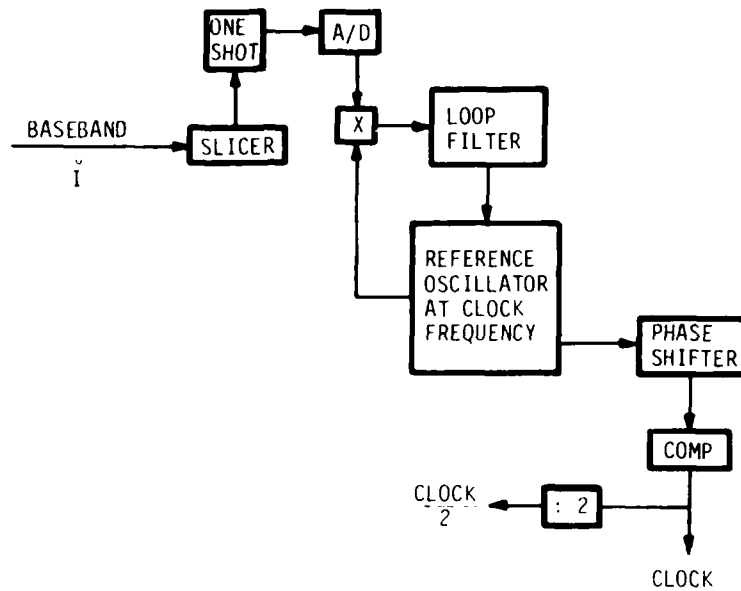


Figure 2-20. QPR/QPSK Bit Timing Recovery Model

and descrambling if the scrambler option was selected at the transmitter. This sequence of processing events is the reverse of the data input processing described in paragraph 2.1 and has been simulated on the logical portion of the analog computer in a similar fashion.

Detailed simulation diagrams of these functions and all others described in this report are included in Appendix C.

### 3.0 PERFORMANCE MONITOR SIMULATION

Three performance monitors have been simulated for each of the dual diversity LOS receivers and include two offset threshold monitors (OTM) and a linearized AGC monitor. These monitors may be used separately or in combination to control the selection diversity combiner, per a supplied algorithm or algorithms, and can be displayed as analog signals versus time. A block diagram of this simulation is shown in Figure 3-1. The two offset threshold monitors constitute a Multiple Offset Threshold Monitor (MOTM). Each monitor has an adjustable bandwidth from 0.01 Hz to 10 Hz which can be changed at the discretion of the simulation operator. Both threshold monitors have thresholds which can be varied between 0.1 and 0.9 of a bit amplitude.

#### 3.1 Offset Threshold Monitor

The Offset Threshold Monitor determines if the received baseband signal is within an offset threshold for each baseband level at the time the data is sampled, as illustrated in Figure 3-2. Received baseband signals which are within the offset threshold are indicated by pulses generated in synchronism with the symbol rate clock, and accumulated as an analog voltage output of a low-pass filter with a variable bandwidth between 0.01 Hz to 10 Hz. The mechanization of this OTM is shown in Figure 3-3.

The OTM input amplitude, the received baseband signal, is proportional to the received signal level. Therefore, the offset threshold is derived from the data threshold slicing level, thus ensuring that the monitor indicates the quality of the eye pattern and not the received signal level. The slicing level is set equal to the peak values of the received

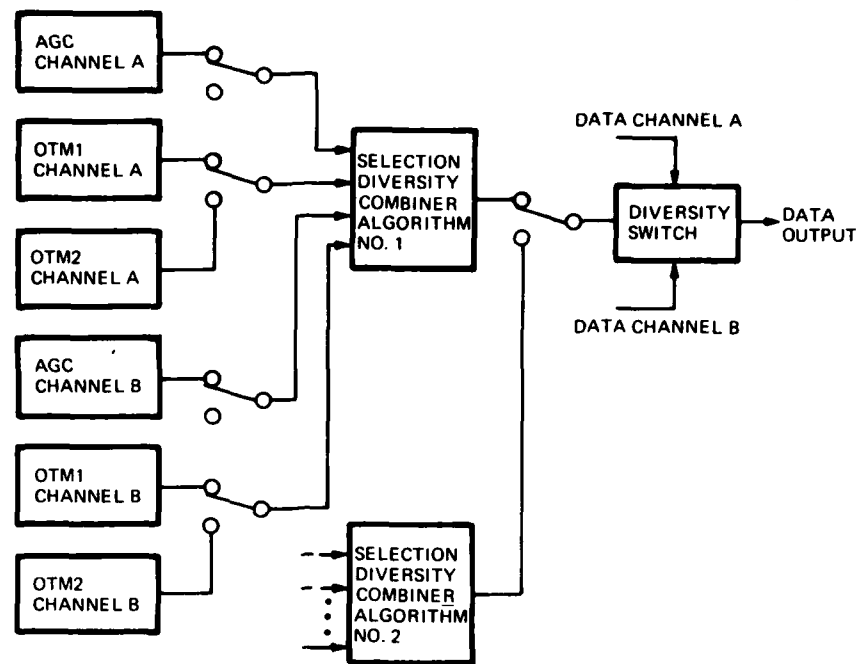


Figure 3-1. Block Diagram of Performance Monitor Simulation

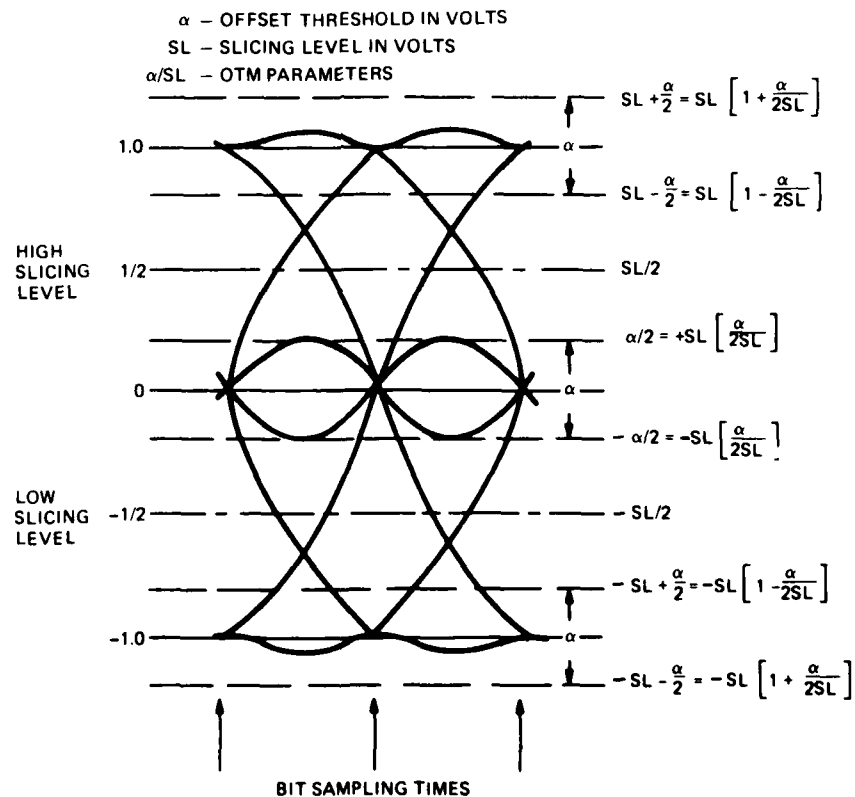


Figure 3-2. Baseband 3-Level Signal With Offset Thresholds

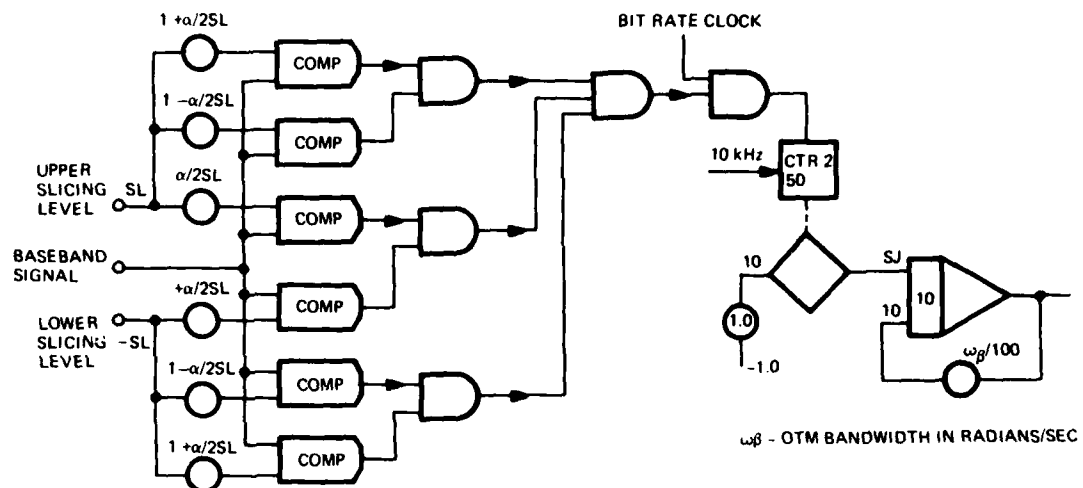


Figure 3-3. Simulation of Offset Threshold Monitor

baseband signal at the data sampling time. Thus, an offset threshold equal to the slicing level would yield a maximum number of pulses to the OTM output filter, and a zero offset threshold would send no pulses to the output filter. In this light, the ratio of the offset threshold ( $\alpha$ ) to the slicing level (SL) is the OTM parameter, the output of the monitor is a linear function of this parameter and, at the discretion of the simulation operator, may be varied from zero to unity (see Figure 3-2).

The offset thresholds of each monitor and baseband level are independently variable. In this light, the OTM mechanization has been made adaptable to two-level and three-level baseband signals (QPSK and QPR modulation types).

### 3.2 Receiver Automatic Gain Control (AGC)

The received IF amplifiers are each supplied gain control multipliers at their outputs. These multipliers are driven by amplified analog signals derived from the filtered output of the AGC circuit. By using the output of this filter to drive a log amplifier, a linear indicator of the received signal level (RSL) in dB can be derived. The circuit developed on the analog computer to provide this linear indication of RSL has been tested and is linear within  $\pm 1$  dB of the detected signal level. These indicators for receivers A and B are used as performance monitors for the diversity switch. The AGC monitor bandwidth may be varied from 0.01 Hz to 10 Hz, as selected by the simulation operator.

#### 4.0 DUAL DIVERSITY SELECTION COMBINER

A dual diversity selection combiner consisting of a government supplied algorithm and a diversity switch has been programmed for the LOS hybrid computer simulation. The algorithm has the option of using any of the performance monitors provided in the simulation as driving functions. Selection of these inputs to the diversity combiner are controlled by the simulation user. Decisions made by the algorithm are dependent upon variable threshold values set for the performance monitors.

##### 4.1 Government Supplied Diversity Combiner Algorithm

The functional flow diagram for the government supplied algorithm is shown in Figure 4-1. Inputs to this combiner are the signal quality monitors for receivers A and B (SQMA, SQMB), which are synonymous with the OTMs, and the received signal levels of receivers A and B (RSLA, RSLB), which are synonymous with the receiver AGCs.

The first test in the algorithm is a check to determine if the signal quality monitors are within their range of effectiveness. If they are within their range of effectiveness, then the diversity selection will be decided on by comparison of SQMA and SQMB. If they are not within their range of effectiveness, then the diversity selection will be decided by comparing the two received signal levels.

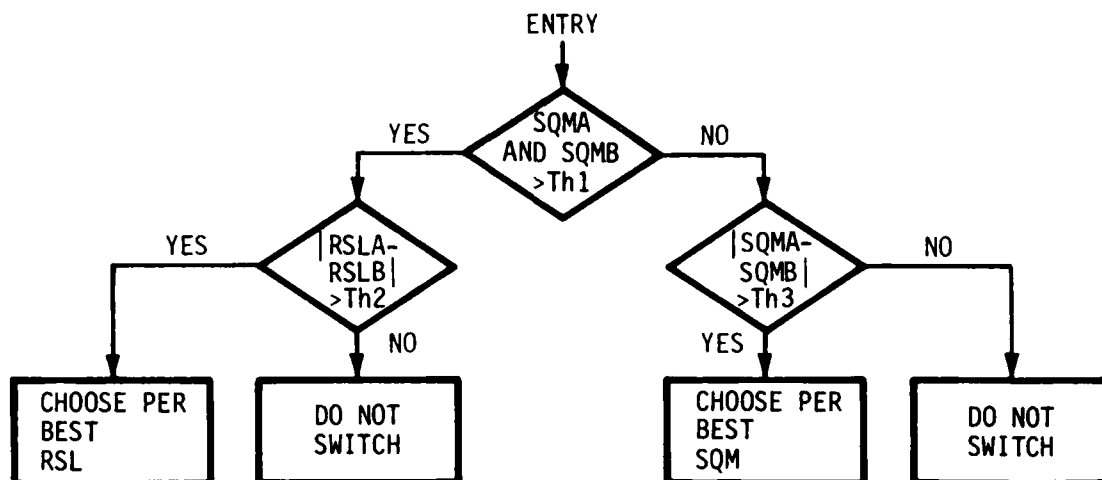


Figure 4-1. Diversity Combiner Algorithm

#### 4.2 Selection Diversity Combiner Simulation

The DRAMA simulation model for diversity combining is shown in Figure 4-2. This model uses analog absolute value circuits, summing amplifiers, comparators, and parallel logic to mechanize each of the decision blocks in Figure 4-1. The first block required the comparison of both signal quality monitors with a threshold establishing the lowest effective operating point,  $Th1$ . This threshold is nominally set to an RSL which provides a  $5 \times 10^{-2}$  bit error rate. If the signal quality monitors are above this operating point, a diversity combiner decision will be based on comparison of the two signal quality monitor outputs. If the signal quality monitors are below this operating level, the diversity combiner decision will be based on a comparison of the two receiver AGC levels which indicate RSL.

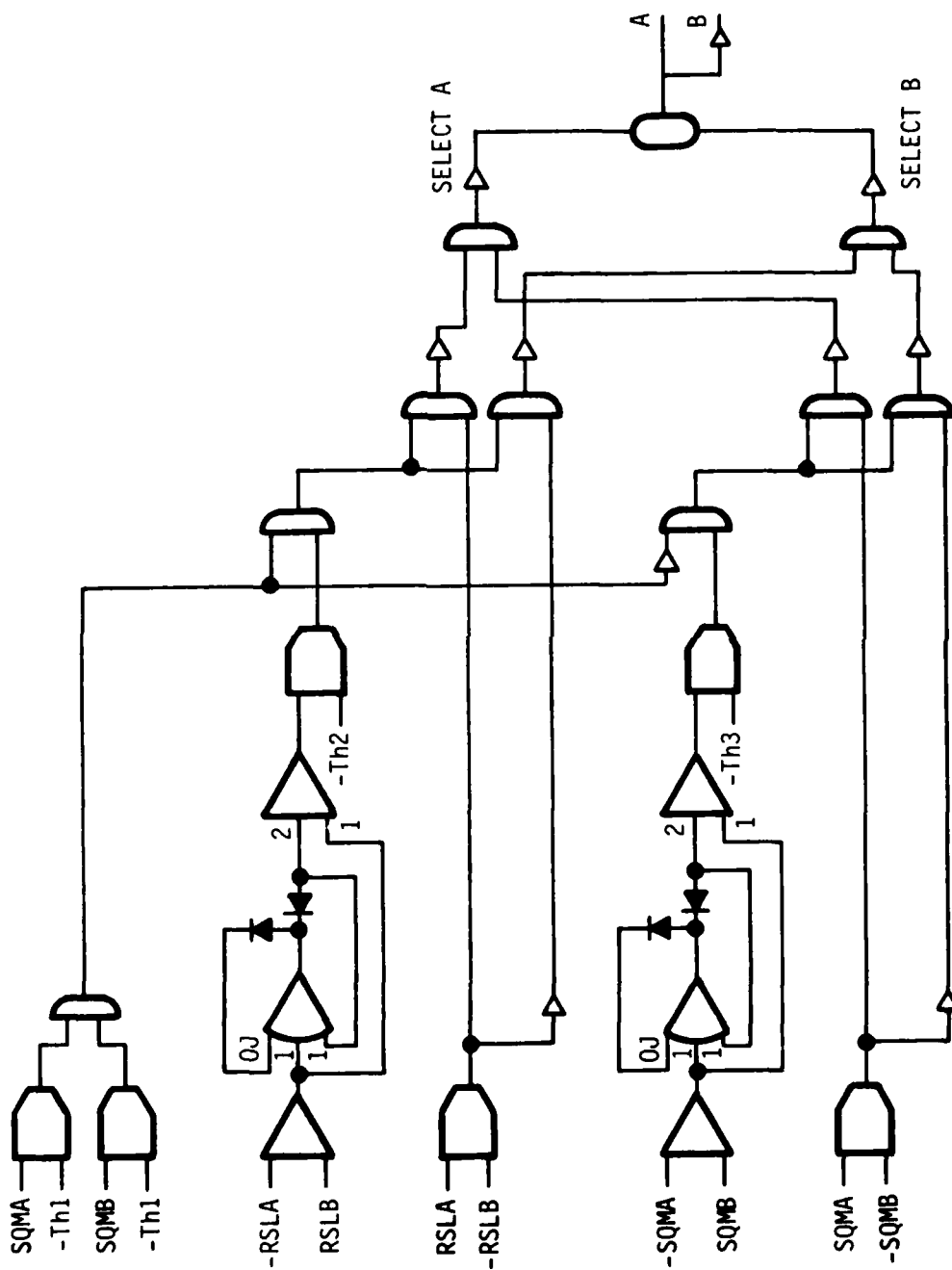


Figure 4-2. Diversity Combiner Simulation

The diversity switch selection based on the signal quality monitors required the analog computation of the difference between absolute values of SQMA and SQMB. This result was then compared to threshold 3, Th3, which is nominally set to -72 dBm, the noise floor of the analog computer. If this difference is above the noise floor, the selection is based on comparison of the two signal quality monitor outputs; otherwise no change in switch position is made.

Diversity switch selection based on the received signal levels follows a similar computation except that threshold 3 is replaced with threshold 2, Th2. This threshold is nominally set at 6 dB. If there is less than 6 dB difference between the two received signal levels, then no change in switch position is made. If the difference is greater than 6 dB, then the receiver with the greater signal level will be chosen.

## 5.0 FREQUENCY SELECTIVE FADING LINE-OF-SIGHT CHANNEL MODEL

The fading channel model developed under a previous DCA contract has been modified to provide increased model flexibility and enhanced operator interaction. Using a combination of hybrid computer technology and integrated circuit design, the channel model has been developed to provide up to four channels of line-of-sight (LOS) frequency flat fading, LOS frequency selective fading, or troposcatter frequency selective fading.

Modifications to the channel model allow selection of from 1 to 12 active taps and relative mean powers for each, and intertap spacing from 0.1 bit to 1.0 bit, inclusive. Also included is the capability to designate specific taps as Rayleigh fading or stationary, and to specify the correlation coefficient between the dual diversity fading signal envelopes from 0.10 to 0.95. Verification and validation of the channel model is currently in progress.

### 5.1 Previous LOS Channel Model

The LOS simulator is made up of three elements: a delay line module, a digital filter module, and a multiplier-summer module. The simulation model allows the user to change the tap gains, tap delay spacing, and signal-to-noise ratio. A block diagram of the simulated channel is shown in Figure 5-1.

The delay line module is a special purpose device integrated into the hybrid computer system. It consists of charge-coupled device (CCD) integrated circuits (256 samples/tap), interconnection and tap output filtering

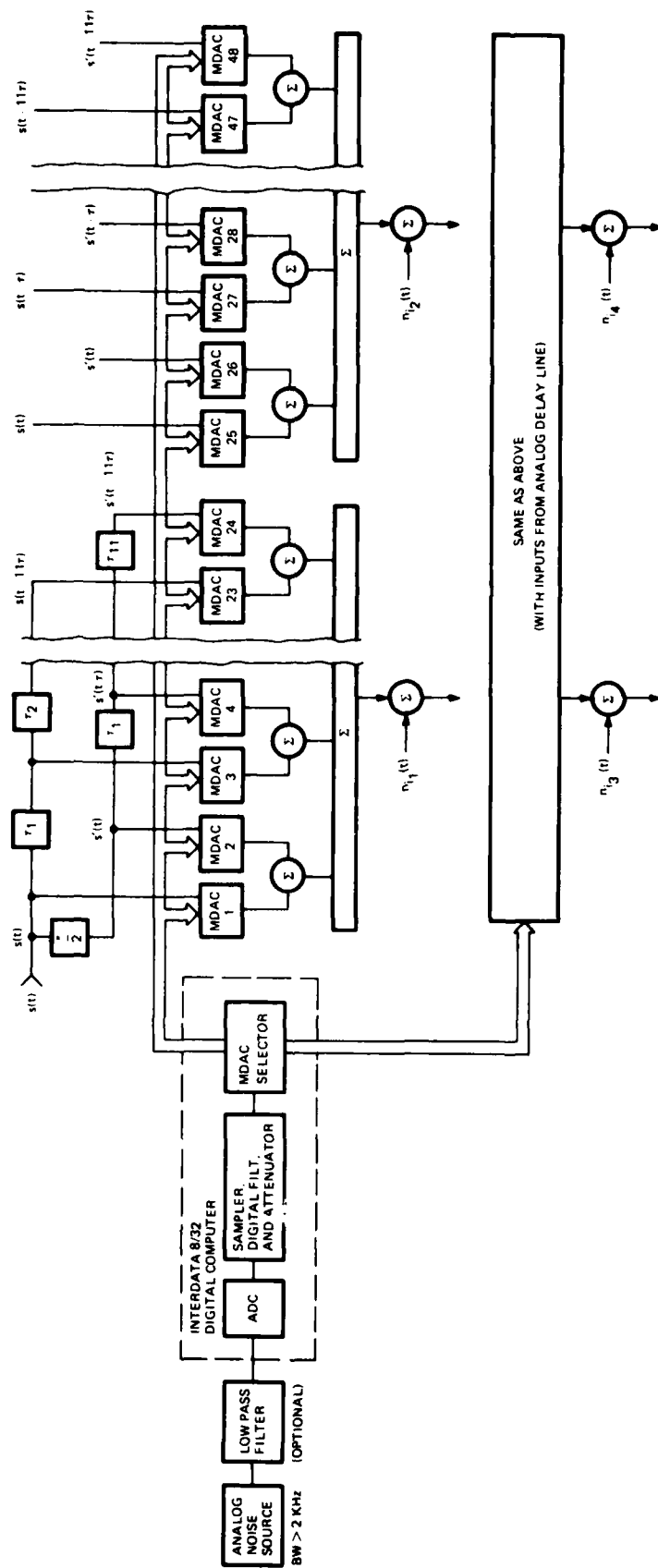


Figure 5-1. LOS Channel Model Implementation

circuits, clocking circuits, and a power supply. The clock frequency is chosen to provide a user specified delay between the taps. For example, a 2681 Hz signal and a clock frequency of 512 KHz yields a delay of 500  $\mu$ s per tap (0.5 bits) and ~200 samples per cycle. Each tap output is filtered to remove sampling noise. The channel simulator has 2 delay lines, each having 12 taps. Delay line 1 is the in-phase tapped delay line, while the quadrature delay, line 2, contains an additional  $\pi/2$  phase shift at each tap.

The digital filter module has been implemented on the hybrid computer system's digital computer. This computer provides the resources to generate 48 uncorrelated random noise sequences, filter them, and transfer the resulting signals to the multiplier summer module. The 48 random noise sequences are generated by sampling a wideband analog Gaussian noise source with an analog-to-digital converter. Capability exists to provide correlation between adjacent random noise sequences by decreasing the bandwidth of the sampled Gaussian noise source. The digital filters are second order Butterworth types, with a nominal cutoff frequency equal to the fade rate, and a maximum sample frequency of 1000 samples per second. The cutoff frequency can be selected by the remote hybrid terminal user at DCEC. The 48 Gaussian noise output signals from the digital filter are multiplied by the mean power coefficient at that tap, and then input to the multiplying digital-to-analog converters (MDAC) in the multiplier-summer module.

The multiplier-summer module for LOS consists of 2 channels, each of which contains 12 pairs of MDACs (1 pair per delay line tap) and a summing amplifier. One power coefficient in each pair multiplies the signal from

one of the taps in delay line 1 by one of the Gaussian functions,  $G_1(t)$ , while the other power coefficient multiplies the signal from the corresponding tap of delay line 2 (which is delayed an additional  $\pi/2$  radians) by another Gaussian function,  $G_j(t)$ . The output of the 12 MDAC pairs is then summed by an analog summing amplifier network to provide the final channel output.

## 5.2 LOS Channel Model Enhancements

The previous LOS channel model digital program has been modified to allow the simulation operator to specify the number of taps desired (from 1 to 12) and the relative mean powers for each tap. To provide the capability for altering the intertap spacing between 0.1 and 1 bit, a frequency synthesizer remotely controlled from the digital computer is used to provide the clock signal for the delay line. Options to select any tap as stationary or Rayleigh fading are also included in the model. Referring to the block diagram in Figure 5-1, a stationary tap will be implemented from the Rayleigh fading tap by zeroing the  $s'(t-\tau)$  MDAC coefficient and setting the  $s(t-\tau)$  MDAC coefficient to a constant value (determined from the relative mean power desired for that tap).

The correlation between the diversity channels is generated by correlating corresponding noise sources input at each tap of the simulated channel model. Assuming  $n_{sm,1}$  and  $n_{cm,1}$  are the independent noise sources for channel  $m$  at tap 1, the correlated noise sources ( $n'$ ) at tap 1 are generated as

$$n'_{s1,i} = \alpha n_{s1,i} + (1-\alpha)n_{s2,i}$$

$$n'_{s2,i} = (1-\alpha)n_{s1,i} + \alpha n_{s2,i}$$

$$n'_{c1,i} = \alpha n_{c1,i} + (1-\alpha)n_{c2,i}$$

$$n'_{c2,i} = (1-\alpha)n_{c1,i} + \alpha n_{c2,i}$$

The correlation model will add the indicated cross correlation processing prior to the point where the noise sources are sampled on the analog computer.

It is desired to achieve a determined cross correlation coefficient of the envelopes of the diversity fading signals. Since the cross correlation is introduced at the several independent inputs to the dual channels, this output cross correlation may not be the same as the cross correlation of the similar inputs. For this reason, the output envelope cross correlation coefficient is calibrated as a function of the input coefficient.

The cross correlation between two signals,  $s_1(t)$  and  $s_2(t)$ , is

$$\begin{aligned} \rho_{12} &= \text{cov}[s_1(t)s_2(t)]/\sigma_1\sigma_2 \\ &= \frac{\overline{s_1(t)s_2(t)} - \overline{s_1(t)}\overline{s_2(t)}}{\sqrt{[\overline{s_1(t)s_1(t)} - \overline{s_1(t)}\overline{s_1(t)}][\overline{s_2(t)s_2(t)} - \overline{s_2(t)}\overline{s_2(t)}]}} \end{aligned}$$

where  $\sigma_1$  is the standard deviation of  $s_1(t)$  and  $\overline{\quad}$  (overbar) denotes the expected value. Hence,  $\overline{s_1(t)}$  is the mean of  $s_1(t)$ .

The circuit illustrated in Figure 5-2 approximates the value of  $\rho_{12}$  on the analog computer has been implemented and verified. Here the time constants  $\tau_1$ ,  $\tau_2$ ,  $\tau_{11}$ ,  $\tau_{22}$ , and  $\tau_{12}$  are made long, compared to the time constants of the corresponding input signals.

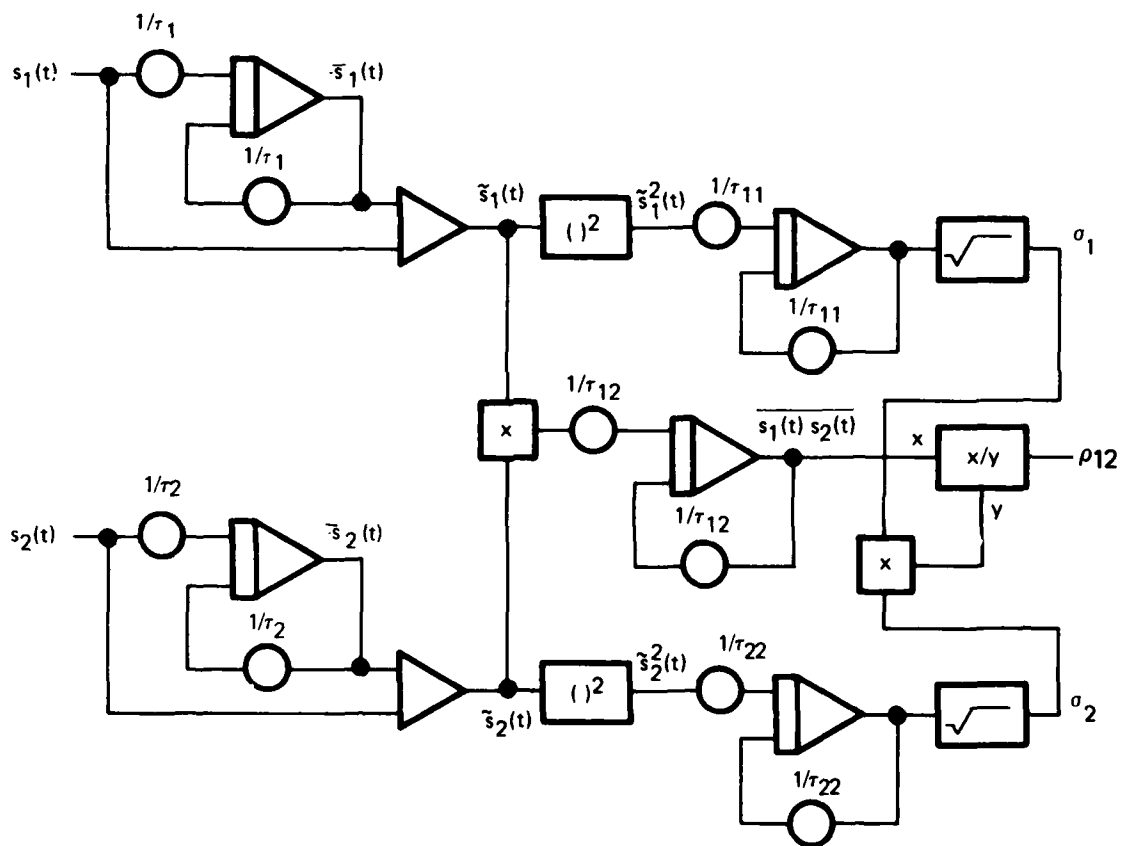


Figure 5-2. Cross-Correlation Analog Diagram

The relationship of  $\rho_{12}$  as a function of  $\alpha$  is determined by the above method, so that selection of the desired correlation coefficient can be made through selection of the appropriate  $\alpha$ . Since the long-term cross correlation of the two envelopes is zero for completely independent channels ( $\alpha=0$ ) and is 1 for identical channels ( $\alpha=0.5$ ),  $\alpha$  will vary from 0 to 0.5 for the full range of envelope correlation coefficients  $0 \leq \rho_{12} \leq 1.0$ .

## 6.0 BASEBAND EQUALIZER SIMULATION

The adaptive equalizer model described in this section is implemented at the output of the QPR/QPSK demodulator. At this output either a three-level or a two-level analog representation of the baseband signal is present. Using a minimum mean squared error technique, weights for the undelayed and delayed baseband signals are generated and multiplied with the delayed demodulated I and Q analog signals. The model used for this technique is shown in Figure 6-1.

### 6.1 Coefficient Generator Model and Simulation

This applique technique includes a coefficient generator that performs a cross correlation between the demodulated and equalized baseband signals, and a transversal filter that multiplies the resulting coefficients and delayed demodulated baseband signals. Limiters on the inputs to the coefficient generator are required for QPSK. These modifications are indicated on the figure and will be provided as an option in the user program.

Input to the coefficient generator includes the demodulated baseband signals and their respective equalizer outputs. Both the inphase (co-phasal) and quadrature basebands have associated coefficient generators. Each of these generators computes coefficients between the demodulated and equalized basebands for both channel and cross-channel errors. For example, the I channel error (coefficient) is generated by cross correlation of the demodulated I and equalized I for a given tap. The cross channel error for I is derived from the cross-correlation of demodulated I and equalized Q.

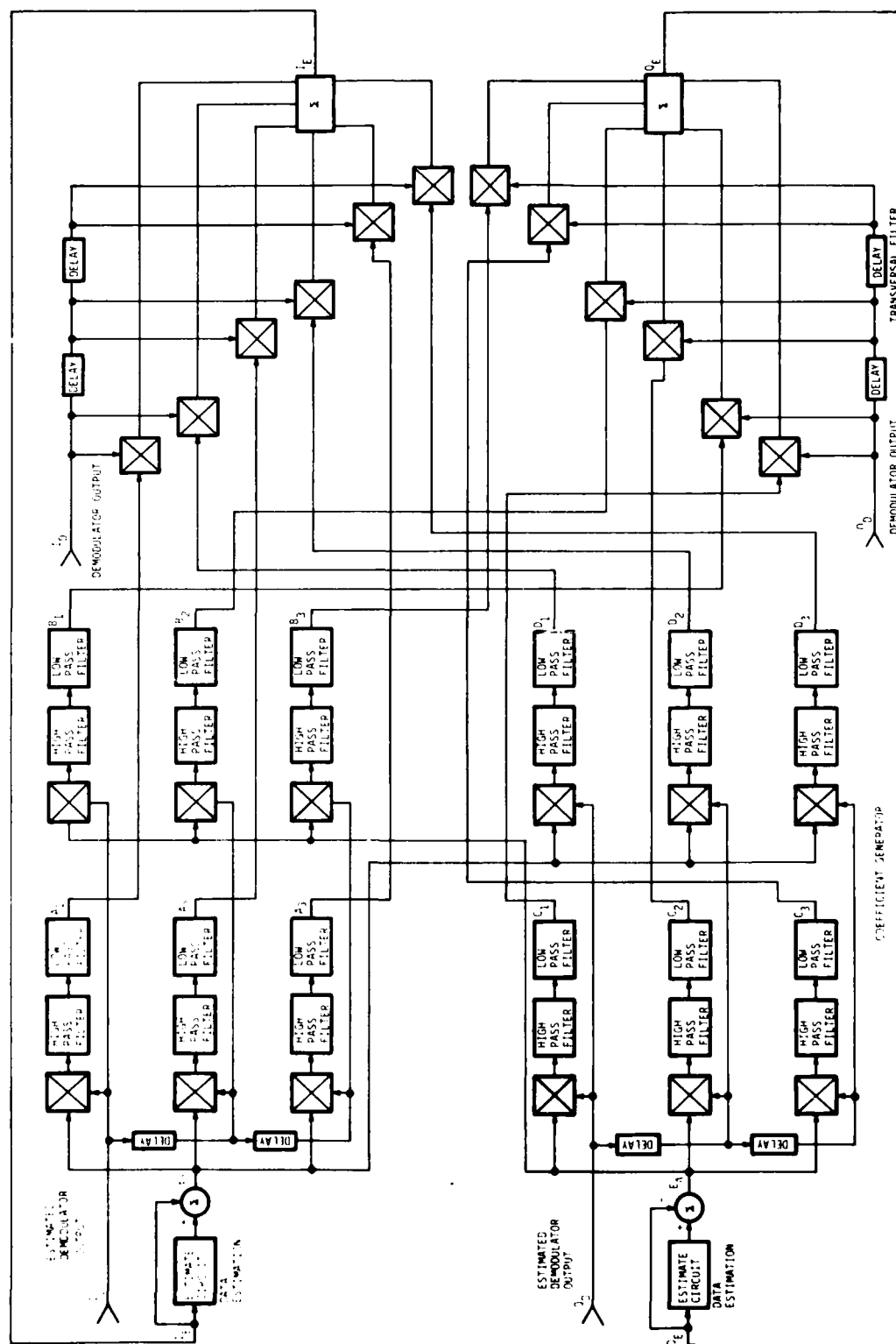


Figure 6-1. Baseband Adaptive Equalizer

Up to three taps can be accommodated using this model (one undelayed and two delayed). Length of delay and the number of taps can be specified via the user remote terminal program.

The output of each correlator was high pass filtered to remove multiplier dc offset before processing by the equalizer bandwidth control filter. A bandwidth control filter for each path was mechanized using a low pass filter, with a variable bandwidth between 0.01 and 10 Hz. Twelve of these computations (or paths) are mechanized for each of the dual receivers. Up to six coefficients for both the channel and cross channel error are computed for each receiver.

Figure 6-2 illustrates the simulation developed to compute one of the equalizer coefficients. Included are the simulation of the cross correlator, high pass filter, and low pass equalizer bandwidth control filter. A quarter-square multiplier was used to correlate the tap delay line input for either I or Q with the proper equalizer I or Q output. Both filters were simulated using analog simulation techniques for transfer function simulation.

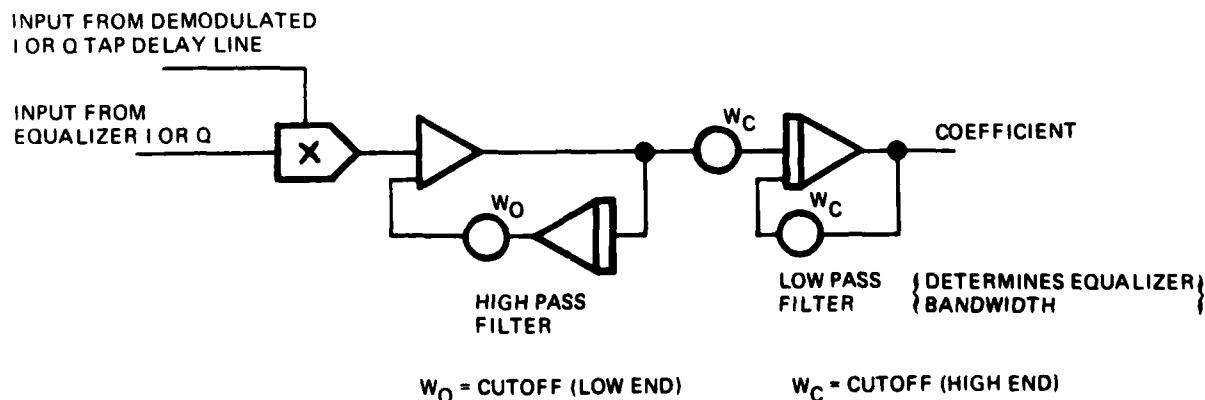


Figure 6-2. Analog Simulation of Equalizer Coefficient

## 6.2 Transversal Filter Model and Simulation

The transversal filter of the baseband equalizer performs the multiplication of each coefficient by its corresponding delayed demodulated baseband signal. For example, the equalizer output for tap 1 of the I channel is generated by summation of the products for the undelayed demodulated I, tap 1, and coefficient  $A_1$  (cross correlation between demodulated I, tap 1, and equalized I) and coefficient  $B_1$  (cross correlation between demodulated I, tap 1, and equalized Q). These components, representing the error (or weighting) of each tap, are summed to develop the equalized analog baseband signals. Equalizer outputs of I and Q are used as input to the data recovery circuits and as feedback to the coefficient generator.

## 6.3 Adaptive Equalizer Delay Mechanism

Variable delays for the Adaptive Equalizer Applique simulation are being implemented using charge coupled device (CCD) analog delay lines (32 samples/tap). Delay modules for the I channel have been fabricated and checked out and the Q channel delay modules are being fabricated. The delay modules allow user selection of from 1 to 3 taps, and the relative tap spacing may be varied from 0.1 to 0.5 bits. A block diagram of one delay module is shown in Figure 6-3. For a 2681 Hz demodulator output signal and a delay clock frequency of 63.98 KHz, a delay of 500  $\mu$ sec per tap (0.5 bit) is obtained.

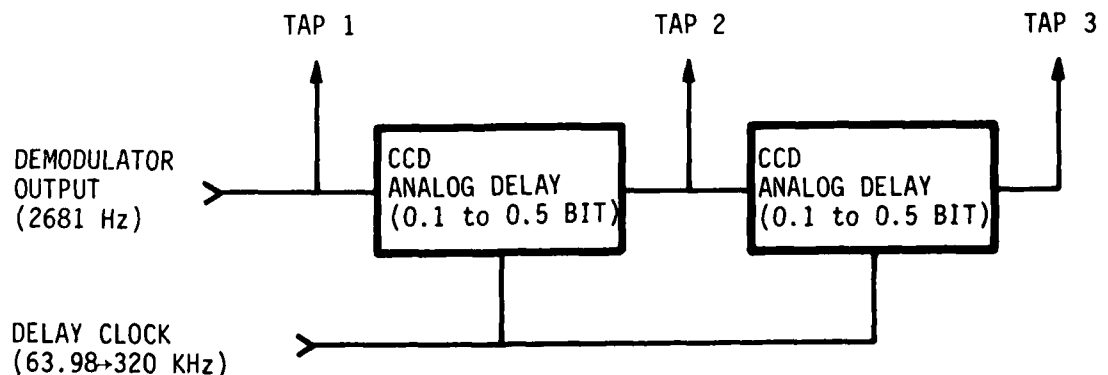


Figure 6-3. Adaptive Equalizer Variable Delay Module

## 7.0 SYSTEM SOFTWARE AND MEASUREMENT CIRCUITS

The simulation software for the hybrid simulation evaluation of frequency selective fading of DCS digital LOS radio equipment is a set of digital programs and subprograms that allow the remote terminal user to interface with the Martin Marietta hybrid computer simulation system by means of the remote terminal at DCEC. This versatile group of programs permits the remote terminal user to alter the system configuration, change system parameters, test and verify system elements, and yield sufficient data to make analytical evaluation of transmission system performance.

The Dispatch Operation System gives the remote terminal user the full flexibility of the hybrid programmer operator. Requests to the Dispatch Operating System provide access to all the program options. The majority of those are under the digital computer's control, hence are automatically integrated into the system. Some options require intervention by the hybrid operator. In this case simulation control is returned to the hybrid operator and the remote user is requested to wait.

Input to the Dispatch Operation System is through the Tektronix graphic input terminal, and the output of the system simulation is to that terminal in the form of graphic and tabular data, and to the eight-channel stripchart recorder. The problem variables are all available for output to the eight-channel stripchart recorder. Two preset variable lists shall be arranged at the time of operation such that the user may select either set. Other variables may be selected at any time to replace one or more of those in the preset lists. This is an example of a system change requiring operator intervention.

## 7.1 Dispatch Operating System

The Dispatch Operating System is entered by the input command OPTN. Receipt of this command gives a list of options available to the user. The first list is a broad classification list, and selection of the option number requested yields a more specific list of options. The selection of one of these options causes either execution of that option or the request for necessary data and subsequent execution. Examples of the option lists and data requests are shown in Appendix A of this report, along with typical data output.

The other means to change parameters and control the transmission simulation is through the argument list method. This software accepts input in the form

ARGUMENT 1, ARGUMENT 2, .... , COMMAND

The argument list is a list of parameters necessary to satisfy the command. If an error occurs, or an insufficient number of arguments is supplied, the program will request those it needs. The list of command mnemonics, with explanations, is included in Appendix A.

## 7.2 Filter Alteration

The filter alteration program is a hybrid technique that provides the user with the capability of changing the two transmitter RF bandpass filters and the two receiver IF bandpass filters. The user may select a Butterworth, Bessel, or Chebychev characteristic and the order of the filter, and specify its center frequency and bandwidth. If the Chebychev filter characteristic is selected, the user supplies the computer with the ripple factor in decibels. These parameters are entered into the system as responses to questions asked by the computer.

The approach taken computes the low-pass filter prototype and converts it to a bandpass filter. The roots of Butterworth low-pass filter and Bessel low-pass filter are found by table lookup. The K roots of the low-pass prototype are converted to the 2K roots of the bandpass filter, using a low-pass to bandpass transformation. If the Chebychev characteristic option is selected, the roots derived for the Butterworth low-pass filter prototype are altered by applying an algorithm based on the ripple factor, S.

$$\epsilon_p = (10^S - 1)^{-1/2}$$

$$a = [(\epsilon_p^2 + 1)^{1/2} + \epsilon_p]/n$$

$$\tanh(a) = \frac{a - 1/a}{a + 1/a}$$

$$\cosh(a) = 0.5(a + 1/a).$$

The  $\cosh(a)$  term is the normalized 3 dB cutoff frequency for the Chebychev characteristic filter. The  $\tanh(a)$  term is multiplied by the real term. Thus, the Chebychev roots are

$$r_K = \cosh(a) (-\tanh(a)\sigma_K + j\omega_k).$$

The coefficients for the transfer function of the bandpass filter are determined from the derived roots. These coefficients scaled properly are the values to which the digitally controlled attenuators are set in the filter mechanization of Figure 2-13.

The user has the option of running a frequency response test on the filter to verify visually that the filter is set properly. The user responds to questions from the computer to enter the lowest and highest frequencies of interest and the number of points to be tested. The program works by driving the input of the filter with the output from an amplitude-stabilized variable frequency controlled oscillator. The resulting filter output is peak detected, sampled, and stored. This process is repeated for each frequency point until the entire characteristic is stored. The ratio of the filter output to its input is determined in decibels, together with corresponding phase characteristic. The gain and phase characteristics for each frequency point are then printed in tabular form for the user. A Bode plot of the gain characteristic relative to changes in frequency is also displayed graphically.

In addition to the IF and RF bandpass filters, a frequency response test can be made of the baseband filters. The QPR partial response filter frequency response is defined for the total filter. By appropriately combining the transmitter and receiver baseband filters, the complete partial response can be obtained.

### 7.3 Power Spectral Density

The Power Spectral Density (PSD) program is a hybrid technique that incorporates an analog PSD circuit (Figure 7-1) that is controlled and sampled by the digital computer.

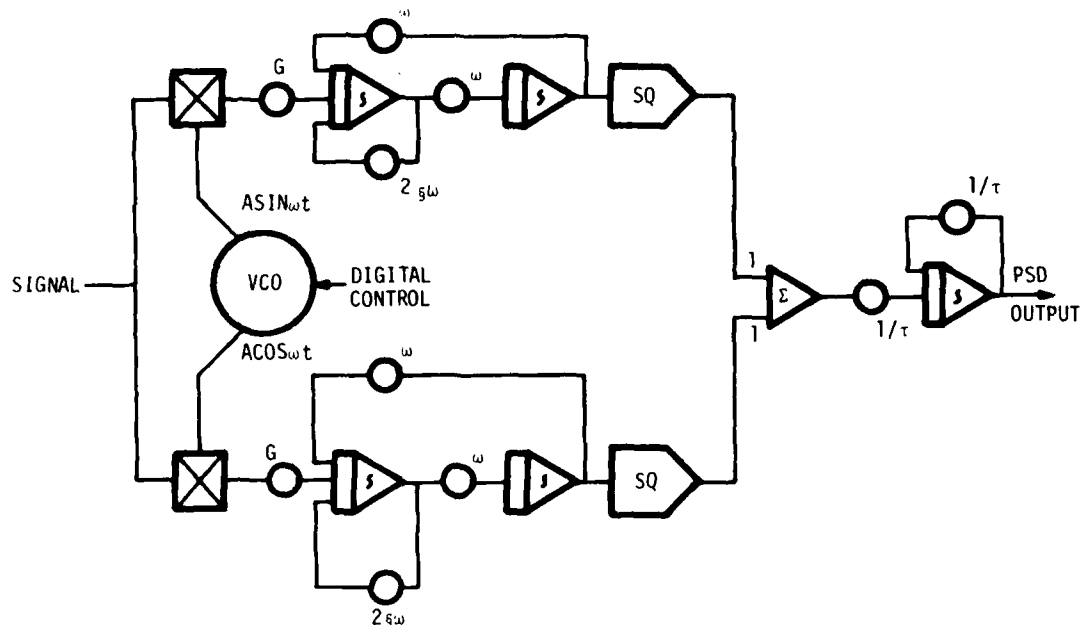


Figure 7-1. Power Spectral Density Analog Circuit

The analog circuit uses a heterodyne method of Fourier analysis to find the average power between the set oscillator frequency, and that frequency plus the bandwidth of the PSD filters. The signal to be analyzed is separately multiplied by the quadrature sinusoids of a variable frequency oscillator and filtered to a preset bandwidth. The resulting signals are squared, summed, and averaged to give the average power within the frequency band set.

The remote user is queued as to which signal to analyze: the lower frequency bound, the upper frequency bound, the number of points between those bounds, and the desired bandwidth of the PSD filters. The frequency range is divided by the number of points, and the average power

within the bandwidth of the PSD filter is measured at each point within the upper and lower frequency bounds. The data is sampled, converted to decibels, normalized, and plotted as a continuous plot of power in decibels over the range of frequencies.

In addition to the spectral occupancy plot, the program displays the upper and lower frequency bounds of the band of frequencies that contain 99 percent of the power. This 99 percent spectral occupancy is determined for the frequency extremes defined previously by the remote user. The frequency at which the center of power exists is also displayed.

#### 7.4 Bit Error Measurement

Both digital and analog computers are used in the measurement, storage, and processing of bit error data for the DRAMA radio LOS simulation. Detection of errors on a bit by bit basis is accomplished by logical programs on the analog computers. These programs, which use parallel logical elements, exclusively "OR" the received data and transmit data (with fixed delay) to test for an error during each bit interval. Alignment of the received data was accomplished by retiming the descrambled signals from each receiver by an appropriately delayed timing signal from the transmitter clock. This signal was delayed until retiming occurred at the midpoint of the received data. The transmit data used in the bit error test was also retimed and delayed until alignment with the received data was achieved. If the transmitted data and received data do not agree, the exclusive "OR" circuit goes high and a pulse is generated at the analog to digital interface. The digital computer accumulates these pulses for both receivers and also from the diversity

error circuit which gates the errors from one of the two receivers, depending on the state of the diversity switch. At the end of a test, the digital computer calculates the total number of bits transmitted using the bit rate and time elapsed during the test, calculates the bit error rates for each receiver and diversity, and displays these results on the Tektronix terminal.

## 8.0 REMOTE TERMINAL CAPABILITY

The Computational Sciences Laboratory has provided the Defense Communications Engineering Center (DCEC), Reston, Virginia, with an advanced hybrid computer terminal through which they can operate and control the hybrid computer simulations developed for this study. This terminal uses two telephone lines and the equipment listed below to provide stripchart recordings for eight channels, graphical displays, and control of the simulations at Orlando, Florida. The terminal equipment loaned to DCEC consists of the following items:

- 1 One Tektronix 4010 Terminal
- 2 One Tektronix 4610 Hard Copy Unit
- 3 One EMR Remote Terminal
- 4 One Eight Channel Brush Recorder
- 5 One Full Duplex Telephone Modem
- 6 Two 1000A Data Couplers
- 7 One Lafayette RK-725 Cassette Tape Recorder.

The two telephone 1000A Data Couplers supplied by Martin Marietta Aerospace and installed at the DCEC facility at Reston, Virginia, were required as part of this installation to permit interchange of hybrid computer data with Orlando, Florida.

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## APPENDIX A

Appendix A contains a list of dispatch mnemonics which can be used by the simulation operator. These mnemonics provide a means of directly addressing and executing specific test and measurement programs and, in doing so, bypass the conversational option list programs.

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## COMMAND MNEMONICS

The use of command mnemonics enables the user to change the system configuration, and perform certain tasks without using the option dispatch system.

The command mnemonic is inputted, terminated with the return key, and the system software requests the input of the information needed, if any, executes the request, and reports what was done. The execution of those commands changes the system, but does not change the current or nominal system defined under the option dispatch system.

Input errors may be deleted with a '?' or the simultaneous depressing of the CTRL and the B keys.

The following is a list of the command mnemonics and their function.

|      |                                                                                          |
|------|------------------------------------------------------------------------------------------|
| HELP | Causes the word 'HELP' to be written and the bell tone sounded. This is done five times. |
| PSD  | A PSD is performed on the device number inputted, and yields a plot of the data.         |
| FLT  | Sets an RF or IF filter to the type, order, bandwidth, and center frequency desired.     |
| FRS  | Takes the frequency response of the device numbers inputted.                             |
| BITE | A bit error test is run under conditions inputted per requested input data.              |
| AGC  | The AGC may be taken out or put in and its bandwidth changed.                            |
| EBN  | Sets the value of $E_b/N_0$ to the inputted value                                        |
| OTM  | Sets the offset threshold monitor bandwidth and the slicing level.                       |
| CHN  | Requests and sets the desired channel model.                                             |
| DPR  | Requests and sets the percentage of the drive power.                                     |

RF        The transmitter RF filters one and two may be put in or taken out of the system.

SCR       The scrambler may be put in or taken out of the system.

NLI       The transmitter nonlinearity may be put in or taken out of the system.

MOD       Request and sets the modulation type desired.

QPR       Sets the system modulation to QPR.

QPSK      Sets the system modulation to QPSK.

## APPENDIX B

Appendix B contains a complete set of the conversational simulation user option lists and typical responses. These options include programs for system configuration change, parameter change, system measurement, and performance evaluation.

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SYS. CNFG.  
NOMINAL

OPTION NO.                      OPTION

- |   |                                                  |
|---|--------------------------------------------------|
| 1 | BIT ERROR TEST                                   |
| 2 | POWER SPECTRAL DENSITY                           |
| 3 | RF, IF AND BASEBAND FILTER<br>FREQUENCY RESPONSE |
| 4 | RF AND IF FILTERS                                |
| 5 | SYSTEM CONFIGURATION                             |
| 6 | EYE PATTERN                                      |
| 7 | CONSTELLATION                                    |
| 8 | FINISHED                                         |

OPTION NO. =

QPSK

CHANNEL MODEL ?

- 1 OUT
- 2 RAYLEIGH
- 3 LOS

OPTION NO. = 1

EB/N0 = 10

RUN TIME = 100

BIT ERROR TEST IN PROGRESS  
PRESS <RETURN> FOR EARLY TERMINATION

TOTAL RUN TIME = 100.0 SECONDS

TOTAL BITS = 100000

BIT ERRORS

BER

CHANNEL A  
CHANNEL B  
DIVERSITY

0  
10  
0

0  
0.1000E-03  
0.

**UNIT NO.      DEVICE**

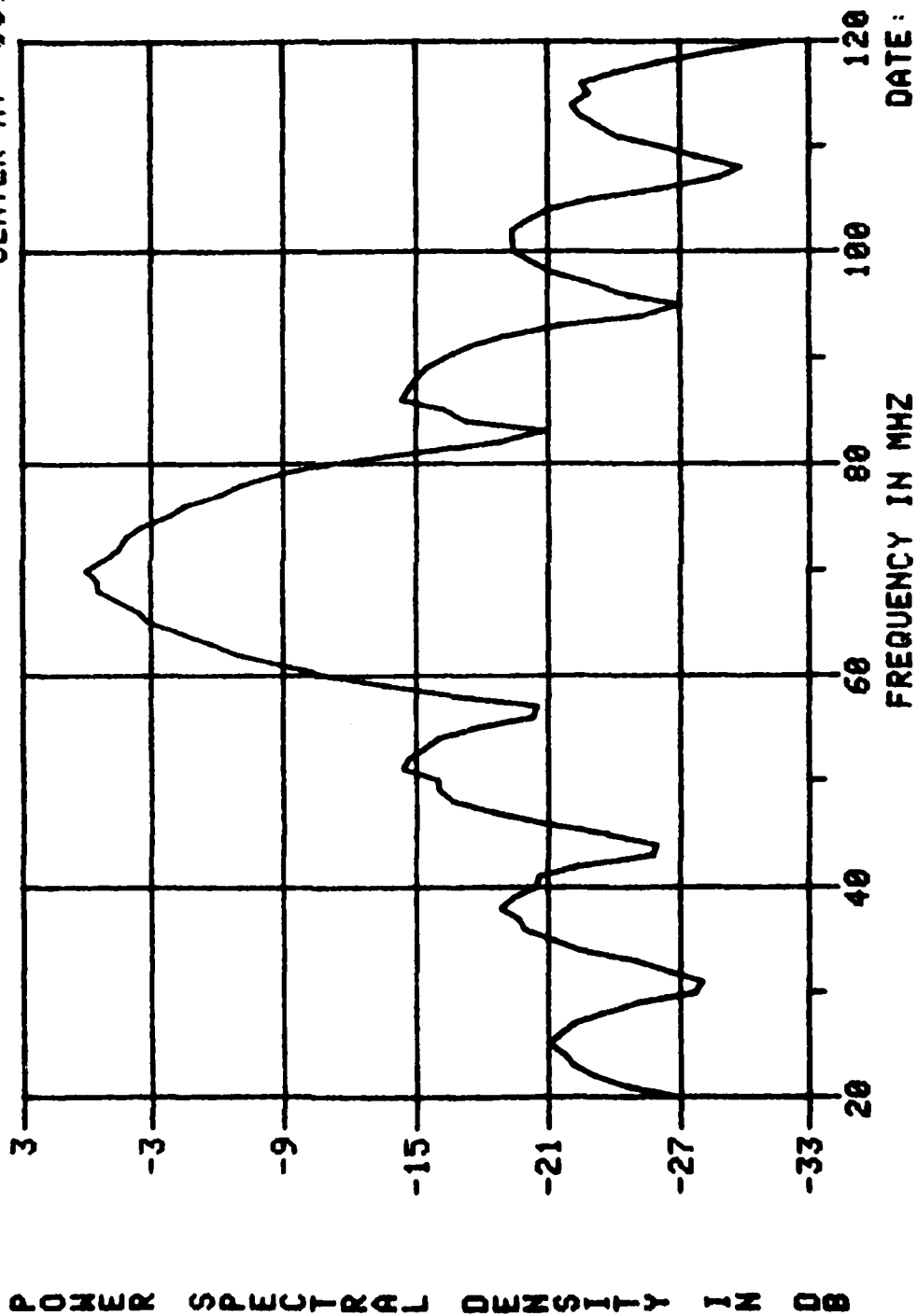
- 1   TRANSMITTER RF FILTER 1**
- 2   TRANSMITTER RF FILTER 2**
- 3   REC. IF FILTER CHANNEL A**
- 4   REC. IF FILTER CHANNEL B**
- 5   BASEBAND FILTER CHANNEL A-I**
- 6   BASEBAND FILTER CHANNEL A-Q**
- 7   BASEBAND FILTER CHANNEL B-I**
- 8   BASEBAND FILTER CHANNEL B-Q**
- 9   TRANSMITTER NON LINEARITY**
- 10  MODULATOR OUTPUT**

**UNIT NO.10**

NO. OF POINTS = 100  
LOWER FREQ. IN MHZ = 20  
UPPER FREQ. IN MHZ = 120  
PSD FILTER BANDWIDTH IN HZ = 50

QPSK

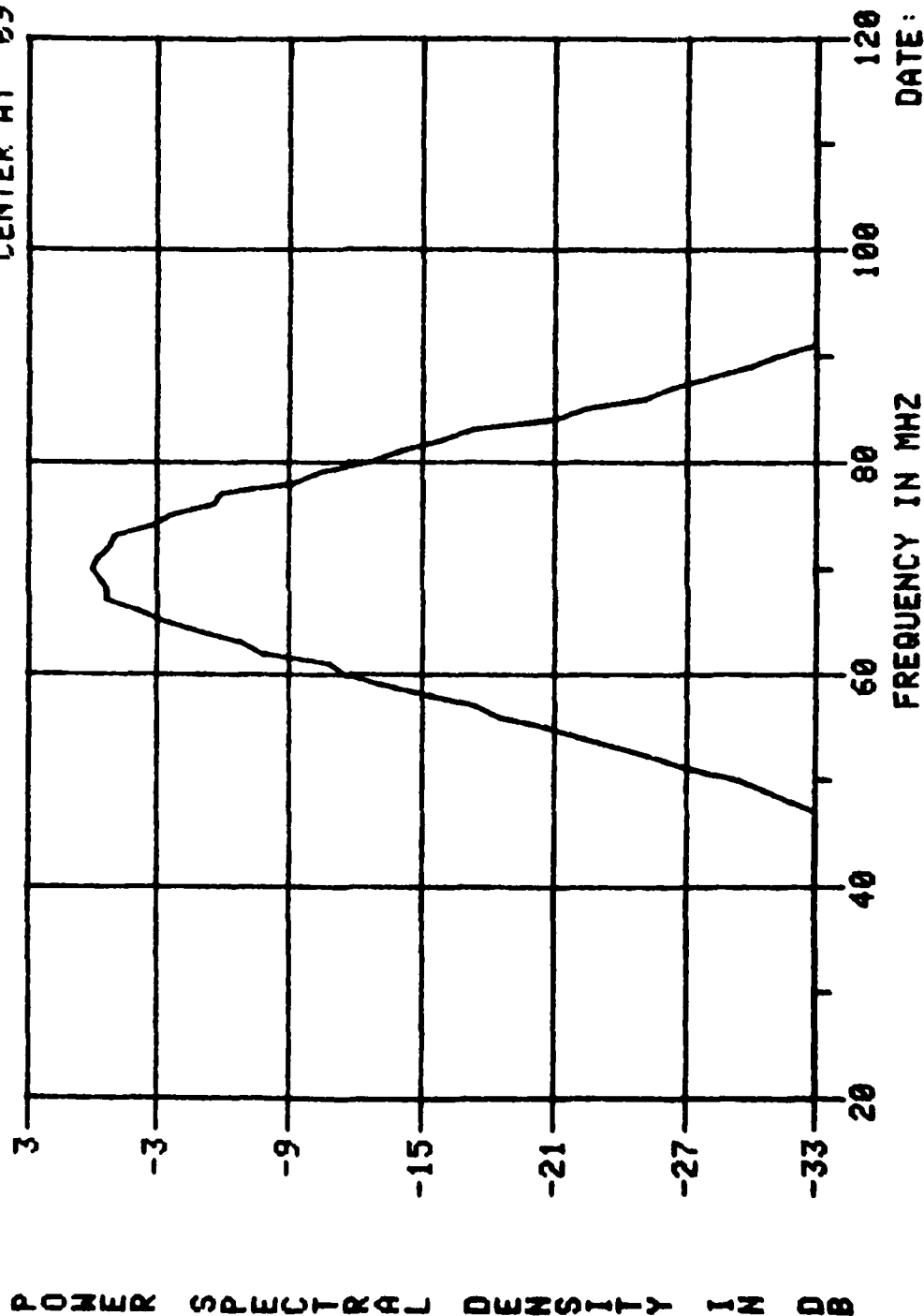
MODULATOR OUTPUT  
PSD FILTER BW = 50.00 HZ  
POWER : 99% BW= 97.00 MHZ  
PEAK AT 70.00 MHZ  
CENTER AT 68.50 MHZ



QPR

MODULATOR OUTPUT  
PSD FILTER BW = 50.00 HZ

POWER : 99% BW = 39.00 MHZ  
PEAK AT 70.00 MHZ  
CENTER AT 69.50 MHZ

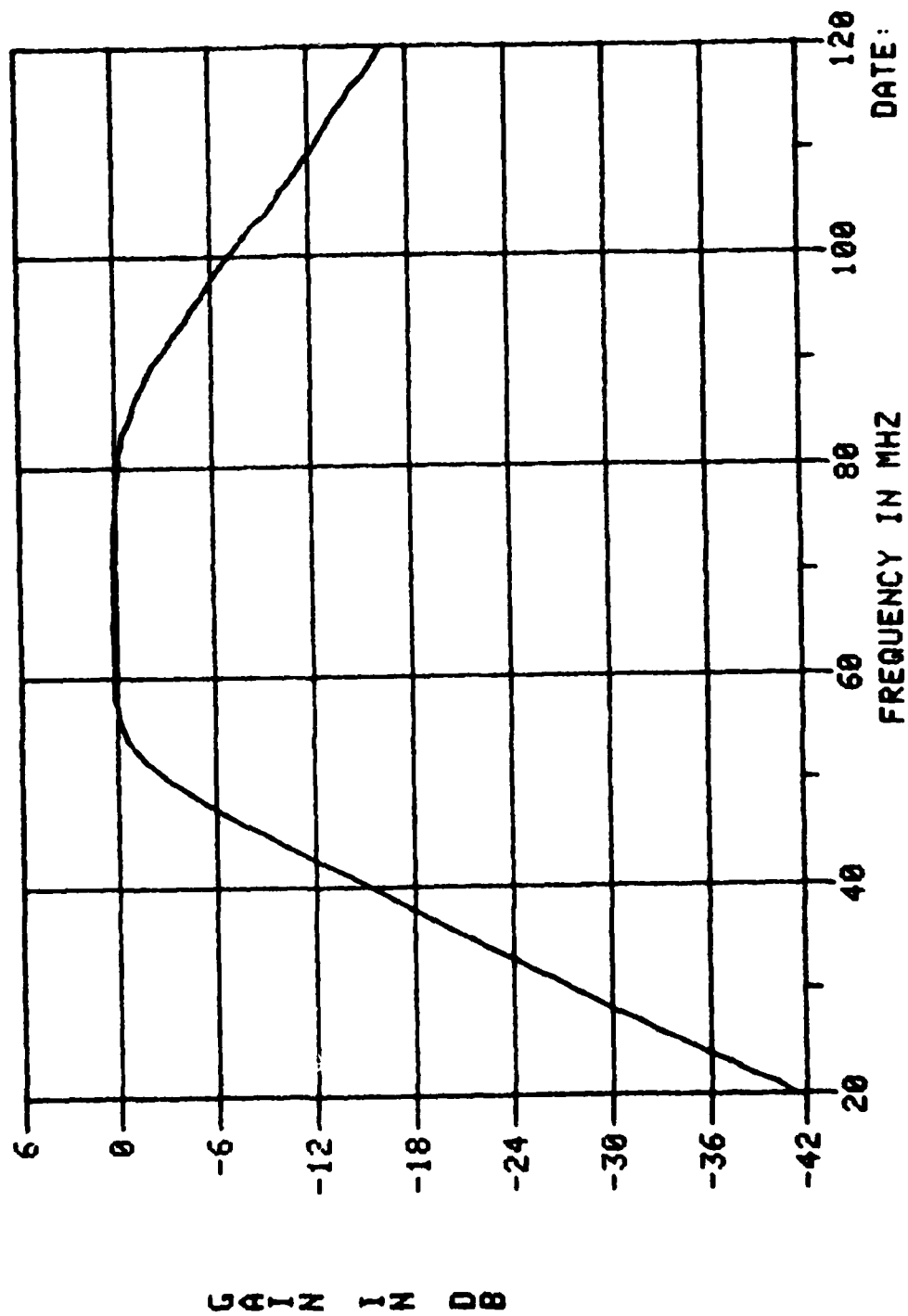


| UNIT NO. | DEV.                        |
|----------|-----------------------------|
| 1        | TRANSMITTER RF FIL.         |
| 2        | TRANSMITTER RF FILTER .     |
| 3        | REC. IF FILTER CHANNEL A    |
| 4        | REC. IF FILTER CHANNEL B    |
| 5        | BASEBAND FILTER CHANNEL A-I |
| 6        | BASEBAND FILTER CHANNEL A-Q |
| 7        | BASEBAND FILTER CHANNEL B-I |
| 8        | BASEBAND FILTER CHANNEL B-Q |

UNIT NO. 1

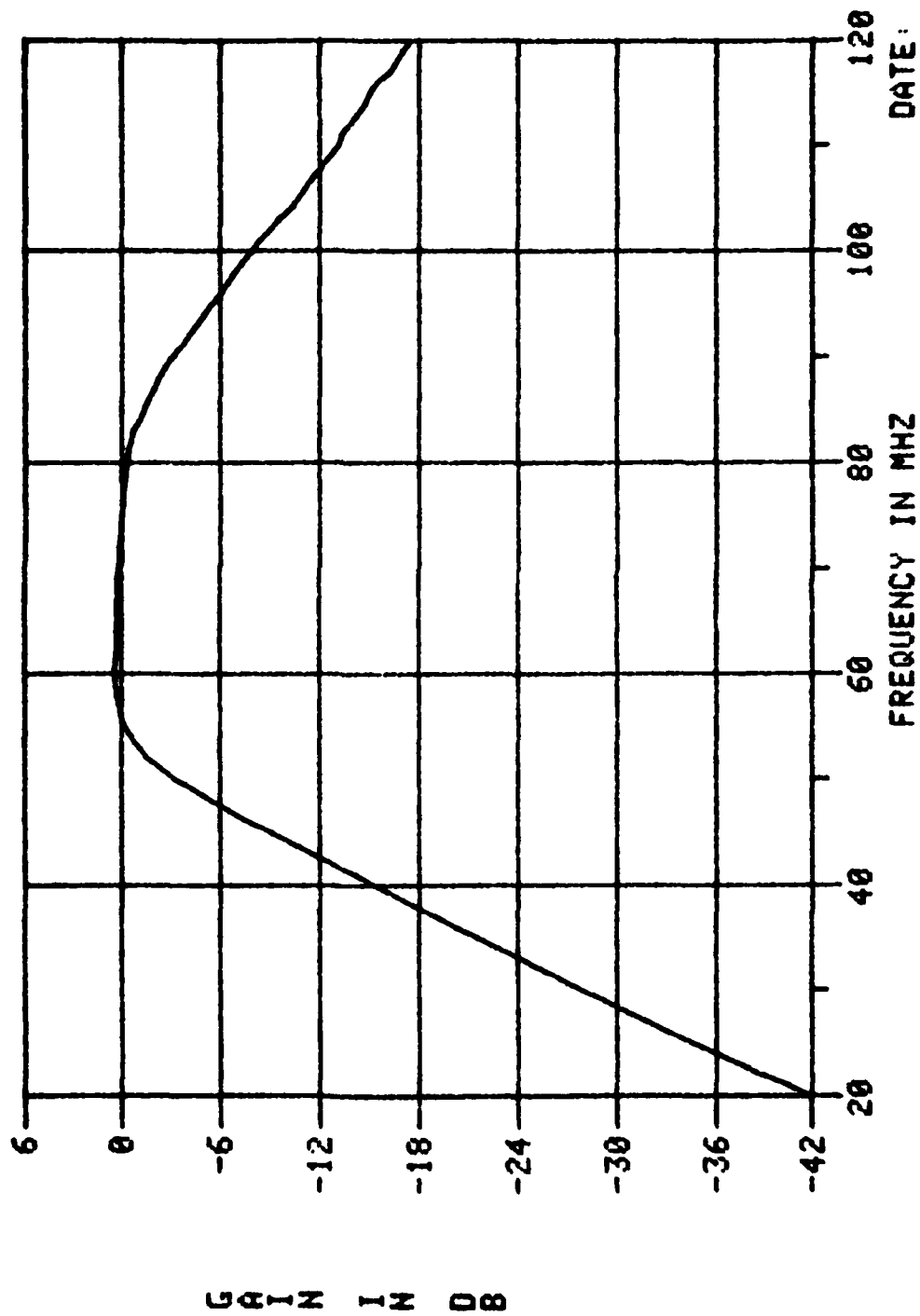
NO. OF POINTS = 100  
LOWER FREQ. IN MHZ = 20  
UPPER FREQ. IN MHZ = 120

# TRANSMITTER RF FILTER 1



DATE: 4/22/80

TRANSMITTER RF FILTER 2



DATE: 4/22/80

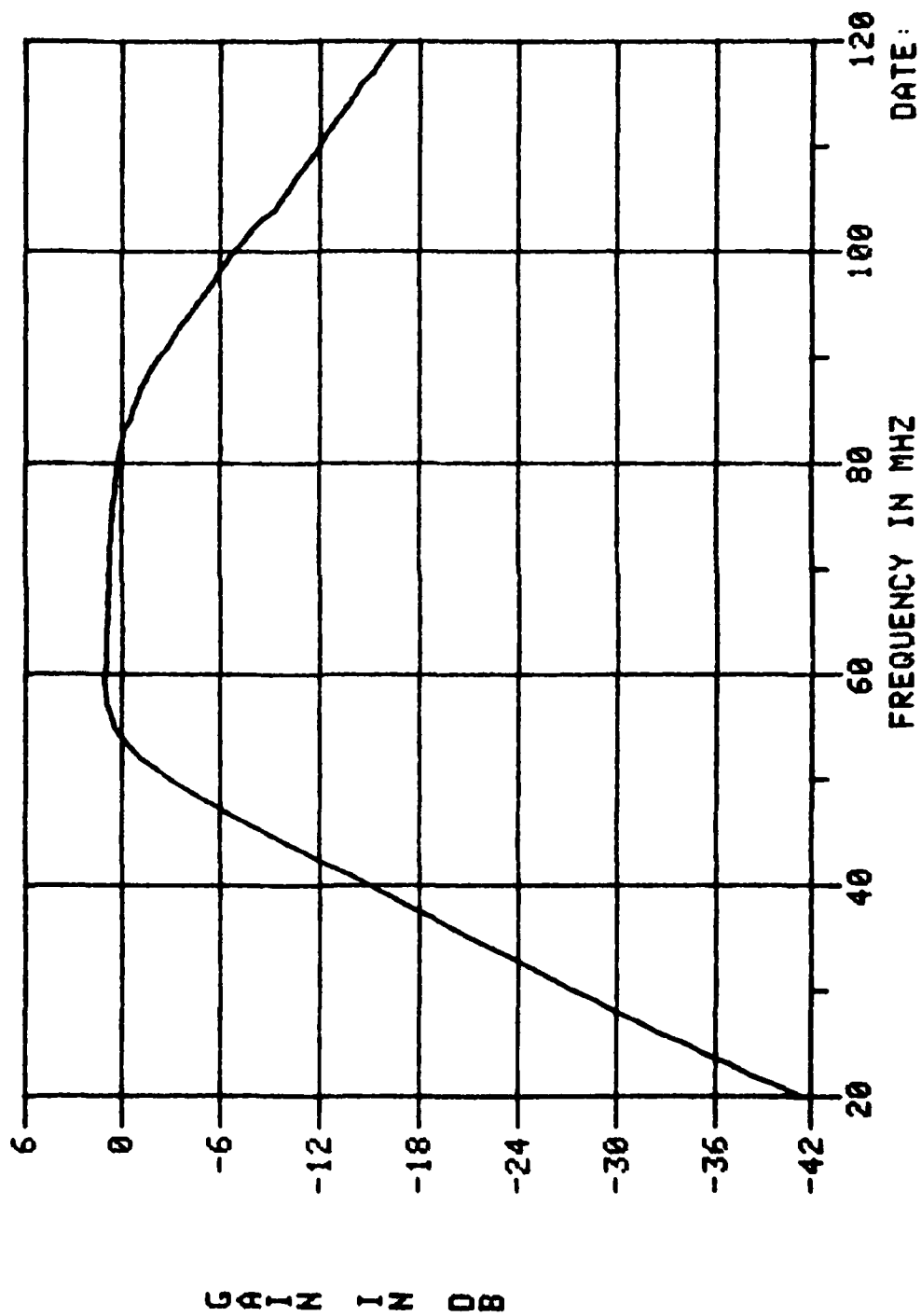
IF FILTER CHANNEL A  
TYPE BUTTERWORTH

ORDER 6  
RIPPLE 0 DB  
BANDWIDTH 40.000 MHZ  
CENTER FREQ. 70.000 MHZ

GAIN 0.59628 0.46067 0.77186  
DAMPING -0.59628 -0.28848 -0.28848  
NATURAL FREQ. 0.16142 0.20894 0.12470

N = 2  
C122 = 0.1155  
UNIT 3 = 0.2002 0.2000  
DESIRED VALUE =  
ERROR = -0.0002

REC. IF FILTER CHANNEL A



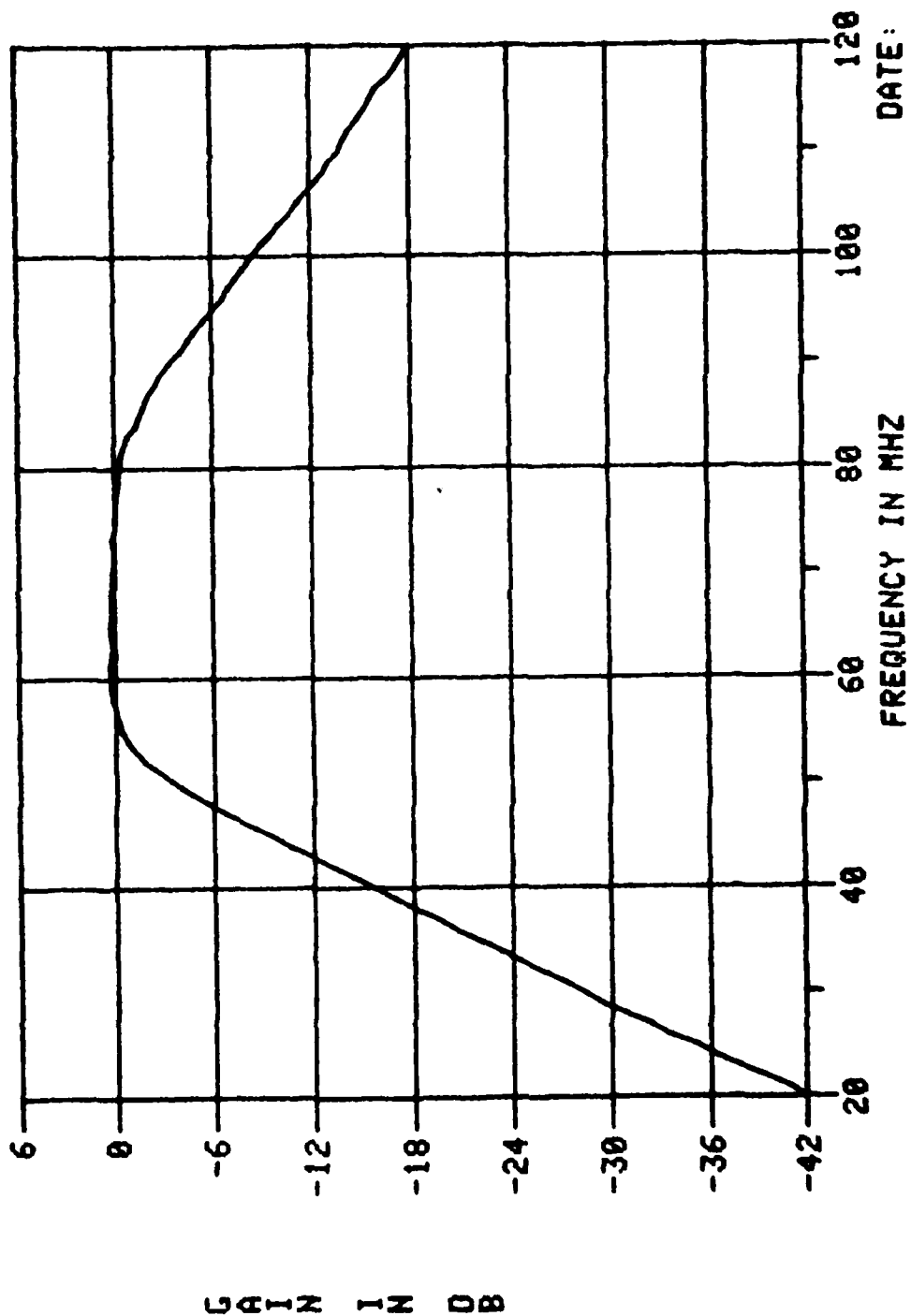
DATE: 4/24/80

IF FILTER CHANNEL B  
TYPE BUTTERWORTH

|               |          |          |
|---------------|----------|----------|
| ORDER         | 6        | DB       |
| RIPPLE        | 0.000    | MHZ      |
| BANDWIDTH     | 70.000   | MHZ      |
| CENTER FREQ.  |          |          |
| GAIN          | 0.59628  | 0.46067  |
| DAMPING       | -0.59628 | -0.28848 |
| NATURAL FREQ. | 0.16142  | 0.20894  |
|               |          | 0.77186  |
|               |          | -0.28848 |
|               |          | 0.12470  |

N = 4  
C122 = 0.1129  
UNIT 4 = 0.2004 0.2000  
DESIRED VALUE =  
ERROR = -0.0004

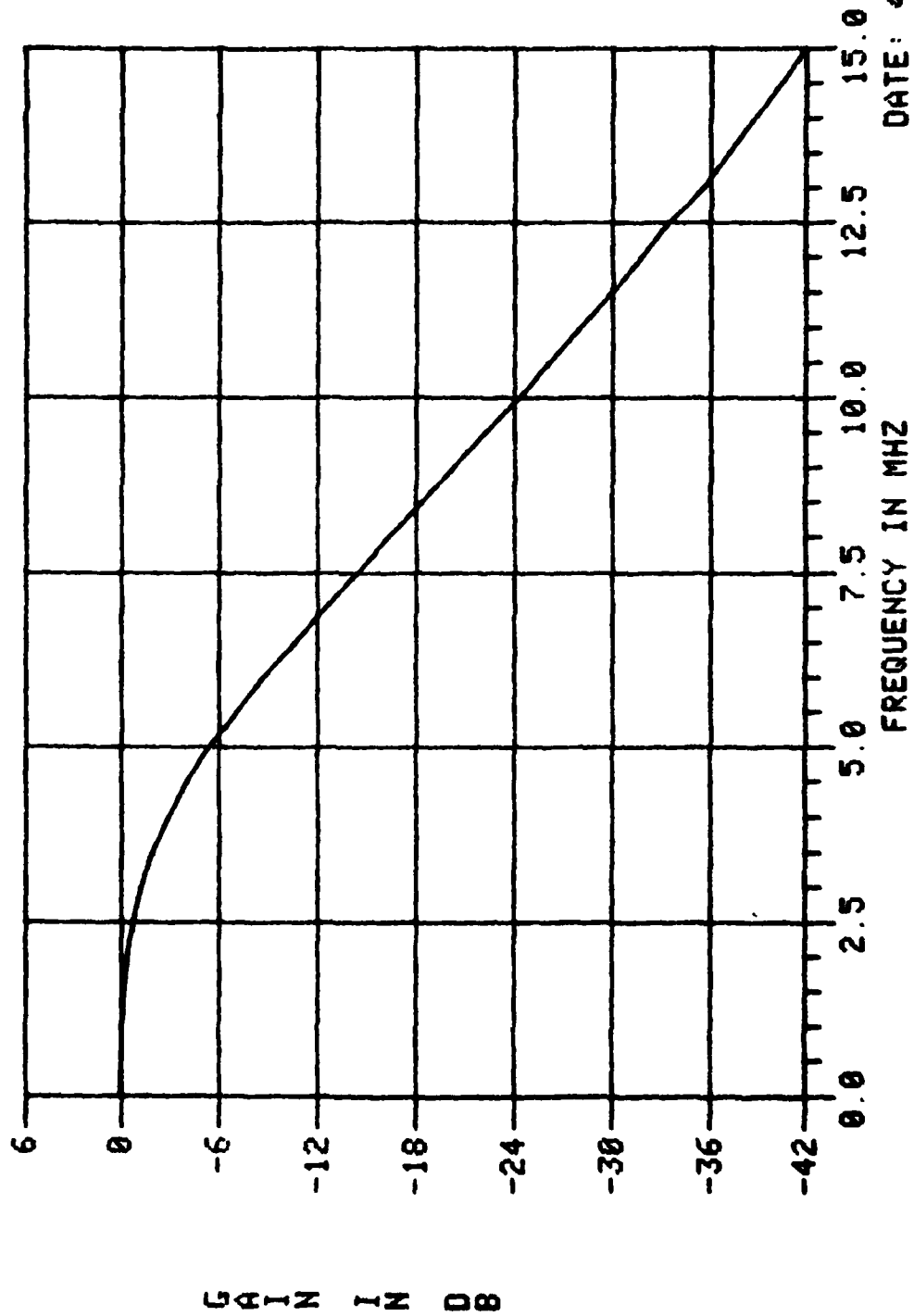
REC. IF FILTER CHANNEL B



DATE: 4/24/80

QPR

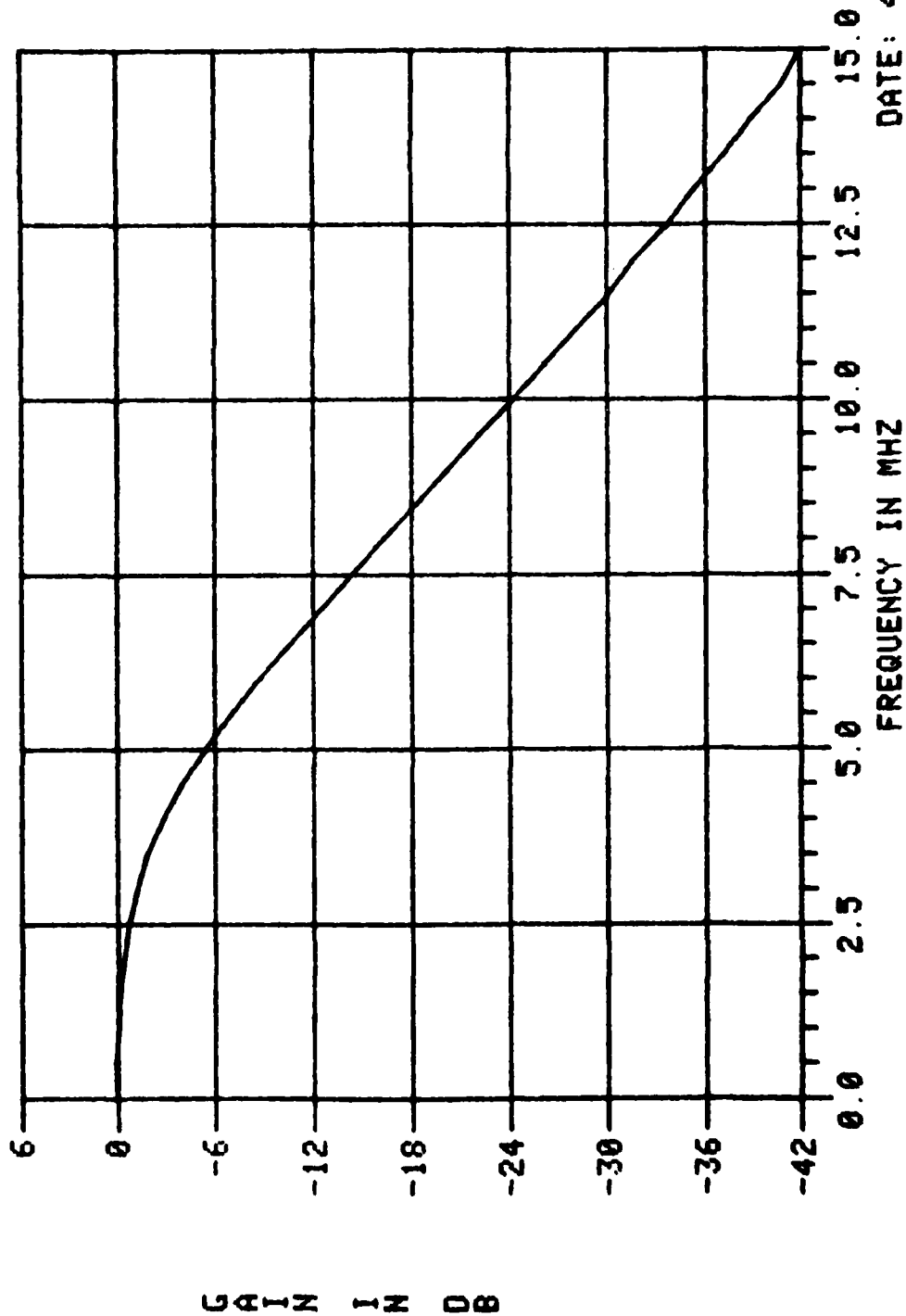
# BASEBAND FILTER CHANNEL B-0



DATE: 4/24/80

QPR

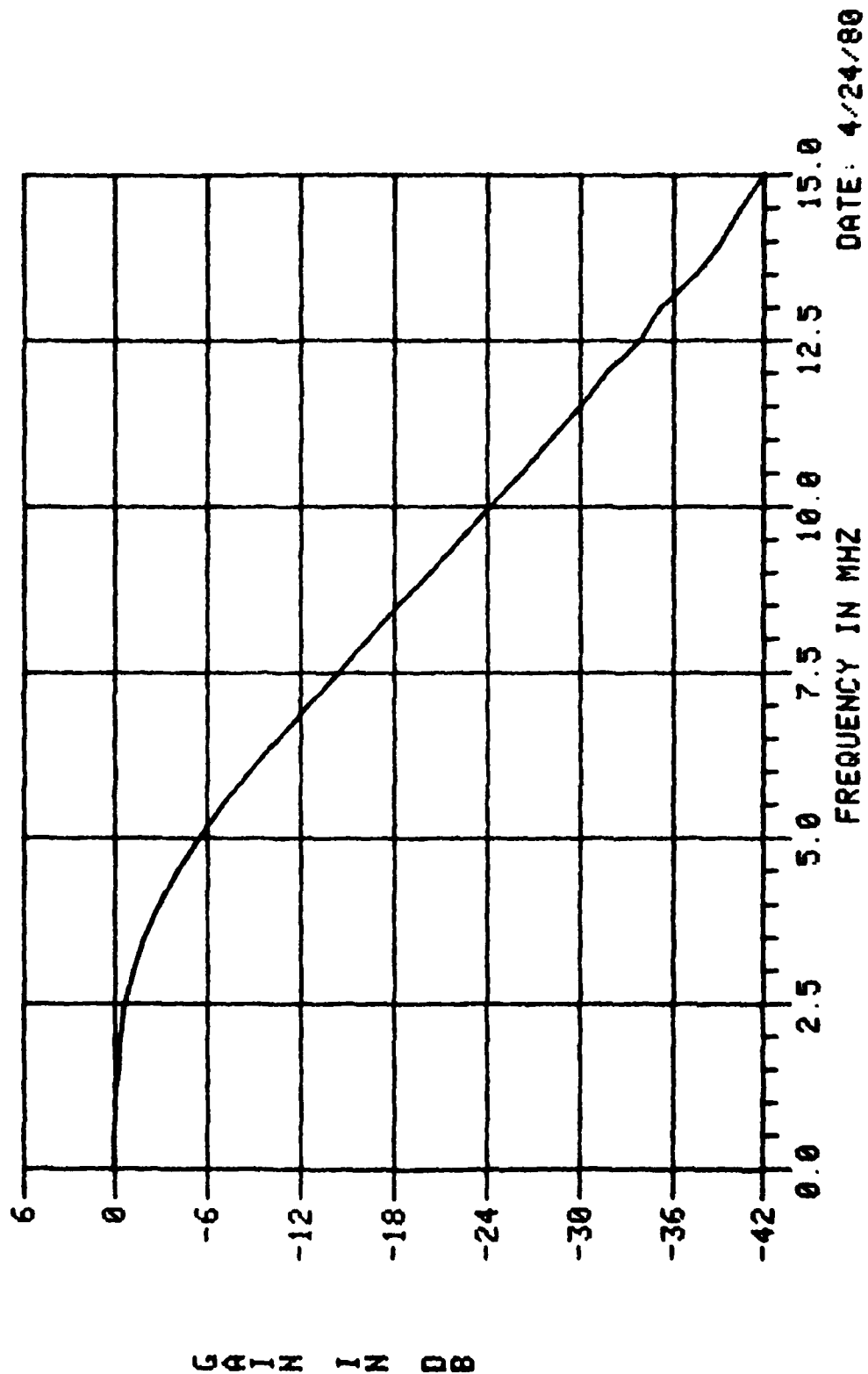
# BASEBAND FILTER CHANNEL B-I



DATE: 4/24/80

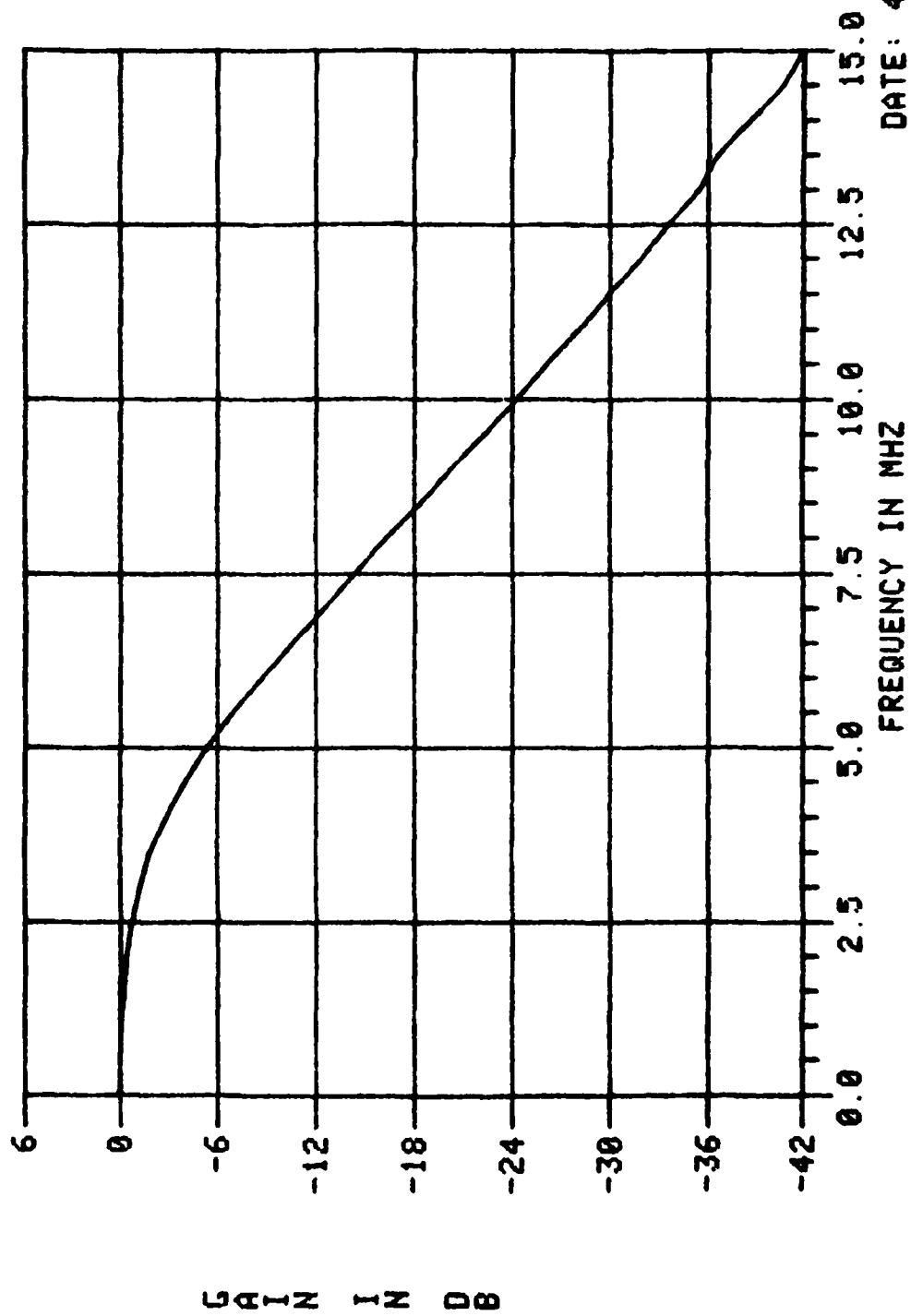
QPR

# BASEBAND FILTER CHANNEL A-Q



QPR

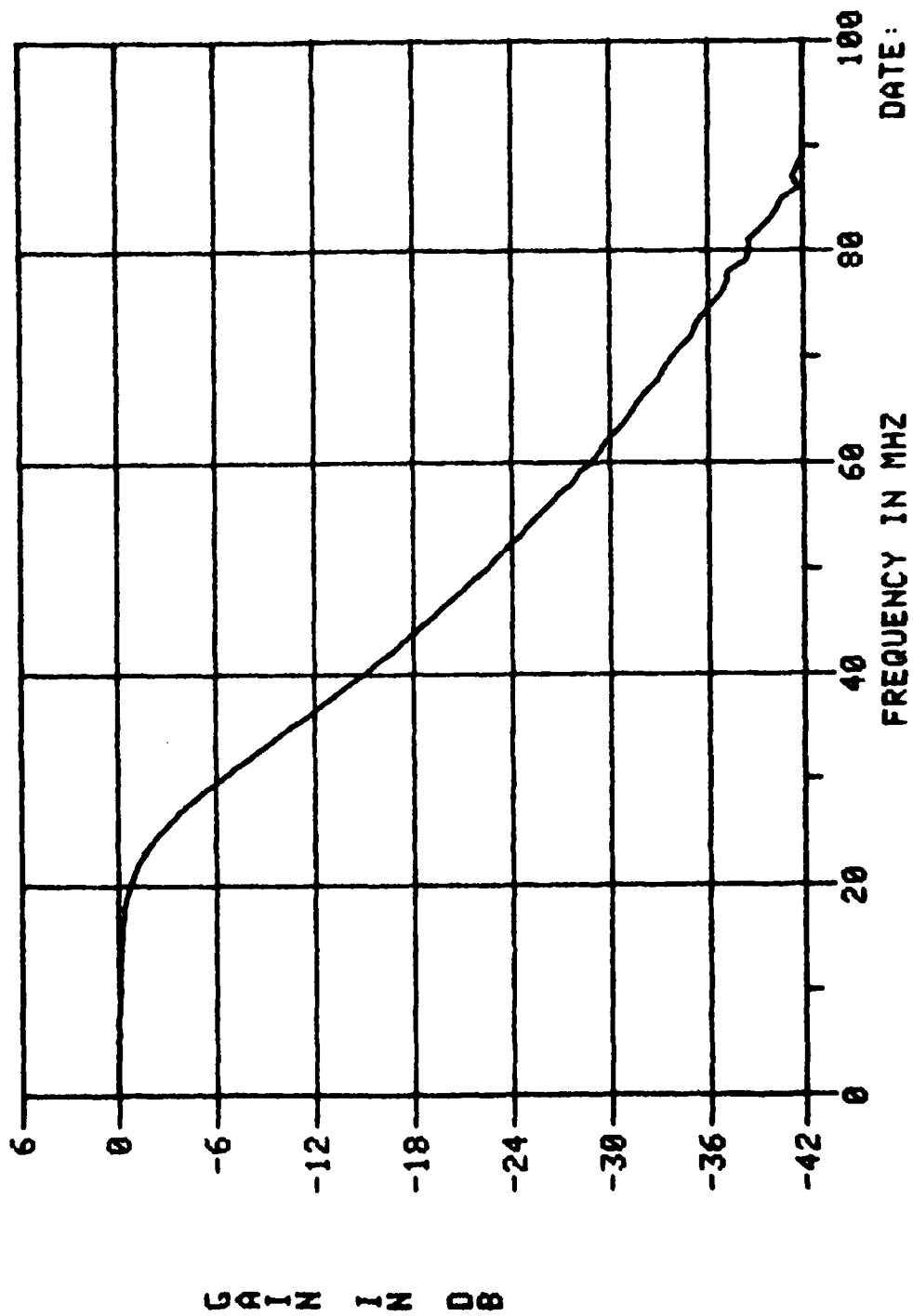
# BASEBAND FILTER CHANNEL A-I



DATE: 4/24/80

QPSK

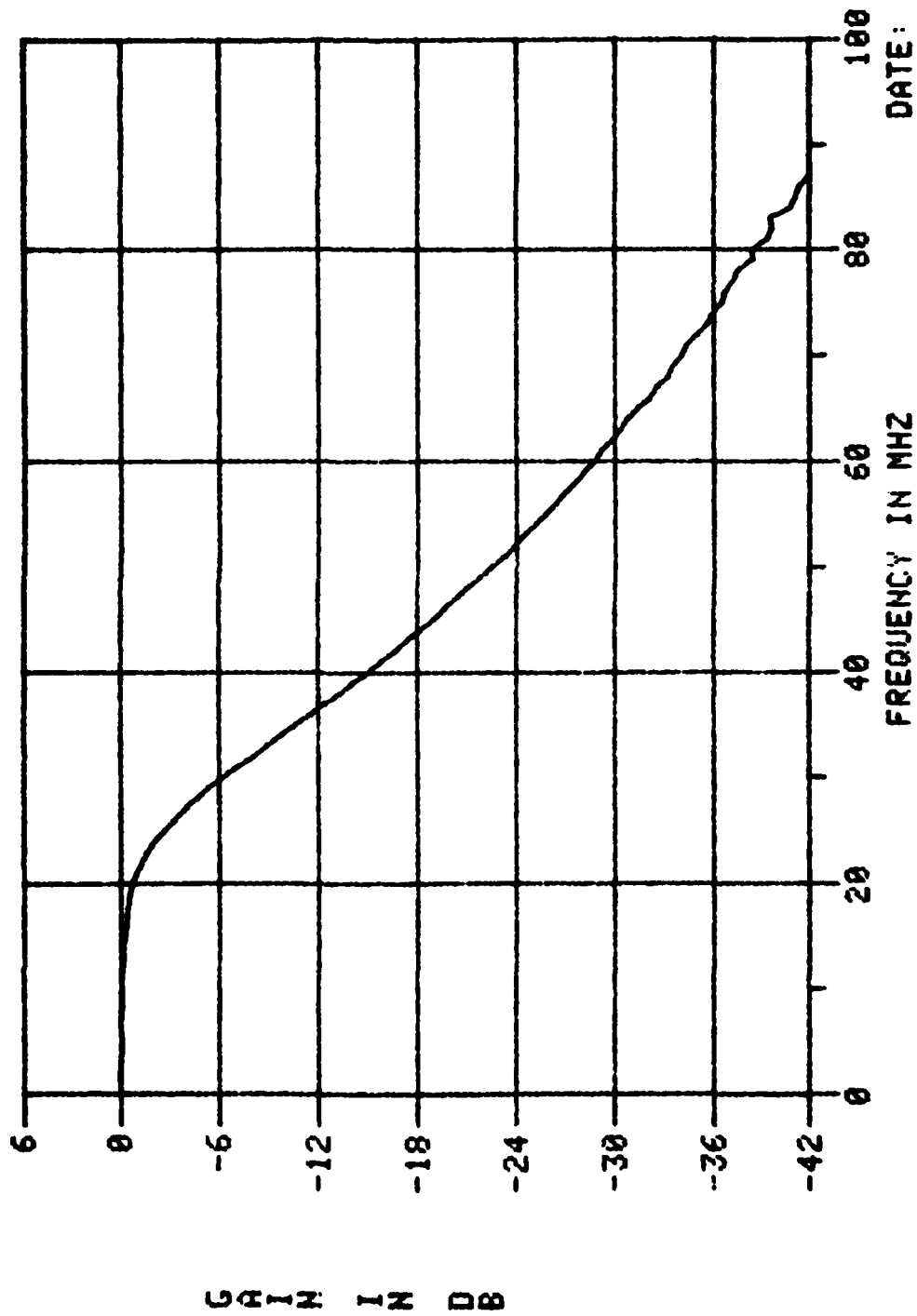
# BASEBAND FILTER CHANNEL A-1



DATE: 4/22/80

QPSK

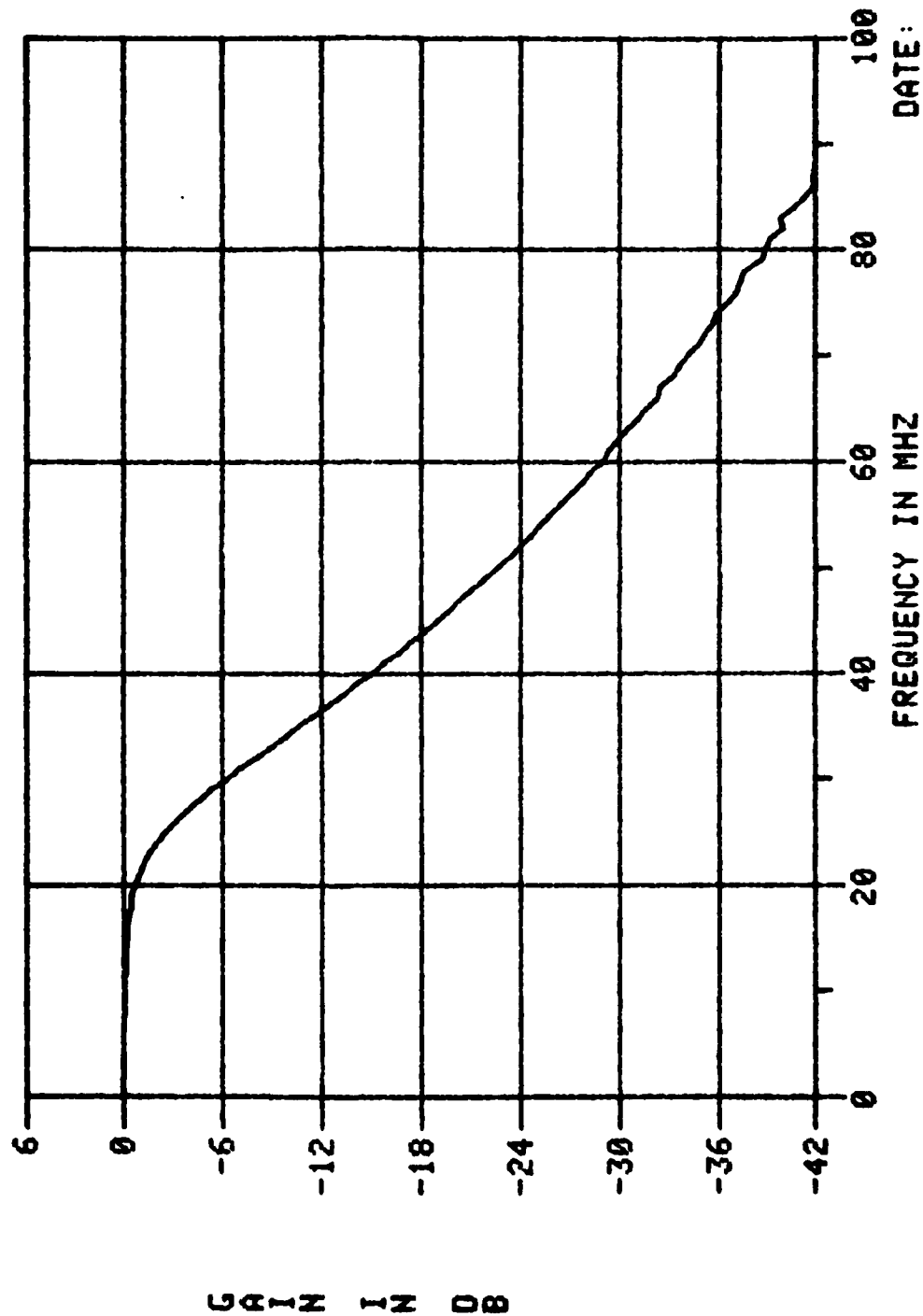
# BASEBAND FILTER CHANNEL A-Q



DATE: 4/22/88

QPSK

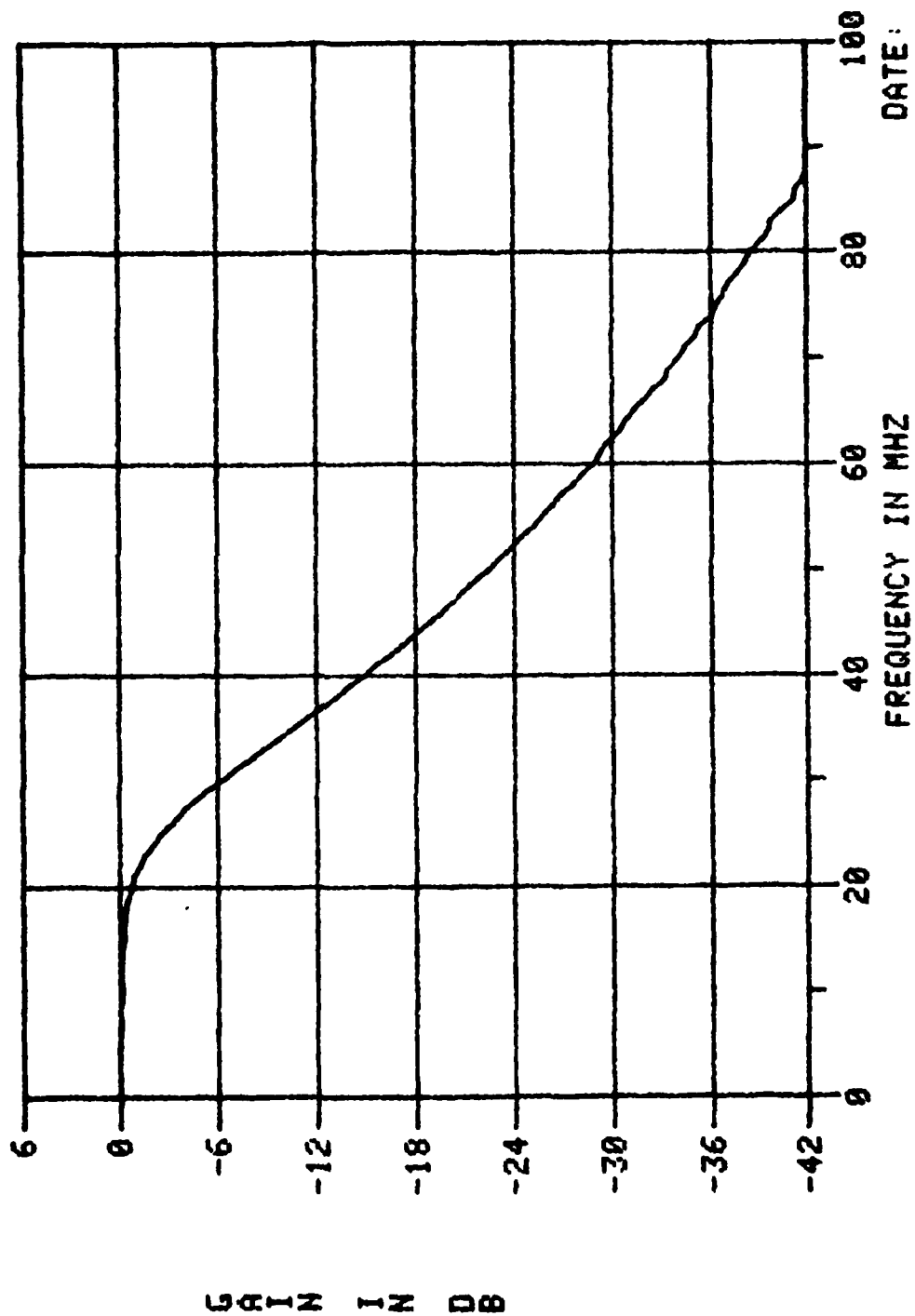
# BASEBAND FILTER CHANNEL B-I



DATE: 4/22/80

QTSK

# BASEBAND FILTER CHANNEL B-Q



DATE: 4/22/80

RF AND IF FILTERS

- 1 LIST FILTER PARAMETER
- 2 CHANGE FILTER PARAMETER
- 3 FINISHED  
OPTION NO. =1

RF FILTER NO.1  
TYPE BUTTERWORTH  
ORDER  
RIPPLE  
BANDWIDTH  
CENTER FREQ.

6 DB  
0.000 MHZ  
40.000 MHZ  
70.000 MHZ

RF FILTER NO.2  
TYPE BUTTERWORTH  
ORDER  
RIPPLE  
BANDWIDTH  
CENTER FREQ.

6 DB  
0.000 MHZ  
40.000 MHZ  
70.000 MHZ

IF FILTER CHANNEL A  
TYPE BUTTERWORTH  
ORDER  
RIPPLE  
BANDWIDTH  
CENTER FREQ.

6 DB  
0.000 MHZ  
40.000 MHZ  
70.000 MHZ

IF FILTER CHANNEL B  
TYPE BUTTERWORTH  
ORDER  
RIPPLE  
BANDWIDTH  
CENTER FREQ.

6 DB  
0.000 MHZ  
40.000 MHZ  
70.000 MHZ

RF AND IF FILTERS

- 1 LIST FILTER PARAMETER
- 2 CHANGE FILTER PARAMETER
- 3 FINISHED

UNIT NO.      OPTION NO. =2  
                    DEVICE

- 1 TRANSMITTER RF FILTER 1
- 2 TRANSMITTER RF FILTER 2
- 3 REC. IF FILTER CHANNEL A
- 4 REC. IF FILTER CHANNEL B

UNIT NO.2

FILTER TYPE  
1 BUTTERWORTH  
2 CHEBYSHEV  
3 BESSEL

TYPE = 1

FILTER ORDER = 6  
RIPPLE IN DB = 0  
BANDWIDTH IN MHZ = 40  
CENTER FREQ. IN MHZ = 70  
RF FILTER NO. 2

TYPE CHEBYSHEV

ORDER 6 DB  
RIPPLE 0.000 MHZ  
BANDWIDTH 40.000 MHZ  
CENTER FREQ. 70.000 MHZ

N = 2  
C352 = 0.1378  
UNIT 2 = 0.2003  
DESIRED VALUE = 0.2000  
ERROR = -0.0003

F/G 17/2.1

DCA100-79-C-0048

QR-15952

NL

2.2

$$A^* = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix}$$

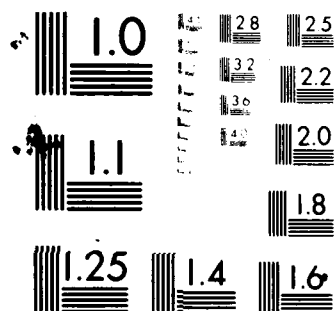
END

5016

1000

2 82

0110



MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-A

SYS. CNFG.  
NOMINAL

SYSTEM CONFIGURATION

- 1 LIST CURRENT CONFIGURATION
- 2 LIST NOMINAL CONFIGURATION
- 3 LIST SET CONFIGURATION
- 4 CHANGE CURRENT CONFIGURATION
- 5 CHANGE NOMINAL CONFIGURATION
- 6 SET CURRENT CONFIGURATION
- 7 SET NOMINAL CONFIGURATION
- 8 CHANGE POWER PROFILE
- 9 PLOT POWER PROFILE
- 10 FINISHED      OPTION NO. =

CONFIGURATION NO. = 6

AGC IS OUT

BANDWIDTH = 1.00 HZ

OTM THRESHOLD

% OF BIT AMPLITUDE = 5.00

OTM BANDWIDTH = 1.00 HZ

EB/N0 = 20.00 DB

CHANNEL MODEL

2. RAYLEIGH

FADE RATE = 1.00 HZ

RUN TIME = 10.00 SECS

% DRIVE POWER = 50.00

DIVERSITY SELECTION OTM

MODULATION TYPE = QPR

TRANSMITTER RF FILTER 1 IS OUT

TRANSMITTER RF FILTER 2 IS OUT

TRANSMITTER NON LINEARITY IS IN

SCRAMBLER IS IN

CONFIGURATION NOMINAL

AGC IS IN  
BANDWIDTH = 5.00 HZ

OTM THRESHOLD  
% OF BIT AMPLITUDE = 25.00  
OTM BANDWIDTH = 5.00 HZ

EB/N0 = 100.00 DB

CHANNEL MODEL  
1. OUT

RUN TIME = 10.00 SECS

% DRIVE POWER = 1.00

DIVERSITY SELECTION AGC

MODULATION TYPE = QPSK

TRANSMITTER RF FILTER 1 IS IN  
TRANSMITTER RF FILTER 2 IS IN

TRANSMITTER NON LINEARITY IS OUT

SCRAMBLER IS OUT

AGC IN Y/N ? Y  
AGC BANDWIDTH IN HZ =5

OTM THRESHOLD  
% OF BIT AMPLITUDE =55  
OTM BANDWIDTH IN HZ =5

EB/NO IN DB =20

CHANNEL MODEL ?

- 1 OUT
- 2 RAYLEIGH
- 3 LOS

OPTION NO. =2  
FADE RATE IN HZ = 2.5

RUN TIME IN SECS =300

% OF DRIVE POWER =.9999

DIVERSITY SELECTION

- 1 AGC
- 2 OTM
- 3 ALGO

OPTION NO. =2

MODULATION TYPE ?

- 1 QPR
- 2 QPSK

OPTION NO. =1

TRANSMITTER RF FILTER 1 IN Y/N ? Y  
TRANSMITTER RF FILTER 2 IN Y/N ? Y  
TRANSMITTER NON LINEARITY IN Y/N ? N  
SCRAMBLER IN Y/N ? N

CONFIGURATION NO. = 7

AGC IS OUT

BANDWIDTH = 5.00 HZ

OTM THRESHOLD

% OF BIT AMPLITUDE = 55.00

OTM BANDWIDTH = 5.00 HZ

EB/N0 = 20.00 DB

CHANNEL MODEL

2. RAYLEIGH

FADE RATE = 2.50 HZ

RUN TIME = 300.00 SECS

% DRIVE POWER = 1.00

DIVERSITY SELECTION OTM

MODULATION TYPE = QPR

TRANSMITTER RF FILTER 1 IS IN

TRANSMITTER RF FILTER 2 IS IN

TRANSMITTER NON LINEARITY IS OUT

SCRAMBLER IS OUT

CHANGE POWER PROFILE

NUMBER OF TAPS=12  
SPECIFY STATIONARY TAPS Y/N ? Y  
STATIONARY TAP NUMBER=3  
STATIONARY TAP NUMBER=5  
STATIONARY TAP NUMBER=7  
STATIONARY TAP NUMBER=

CHANGE TAP GAINS Y/N ? Y

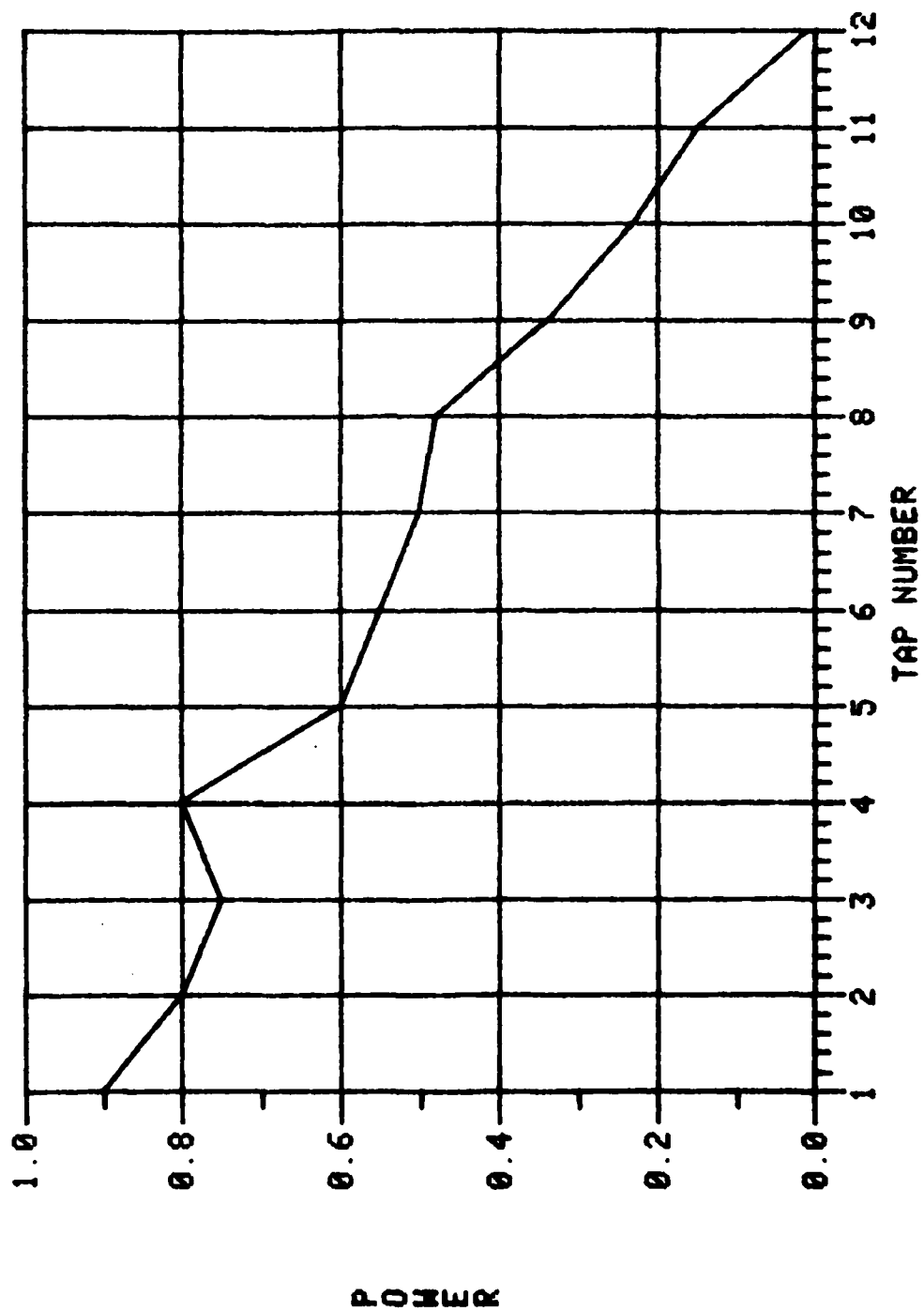
ENTER GAIN AS XXXX

TAP 1 GAIN=.9  
TAP 2 GAIN=.8  
TAP 3 GAIN=.75  
TAP 4 GAIN=.8  
TAP 5 GAIN=.6  
TAP 6 GAIN=.55  
TAP 7 GAIN=.5  
TAP 8 GAIN=.48  
TAP 9 GAIN=.34  
TAP 10 GAIN=.23  
TAP 11 GAIN=.15  
TAP 12 GAIN=.01

CHANNEL CORRELATION COEFFICIENT (0.10 - 0.95)=.4

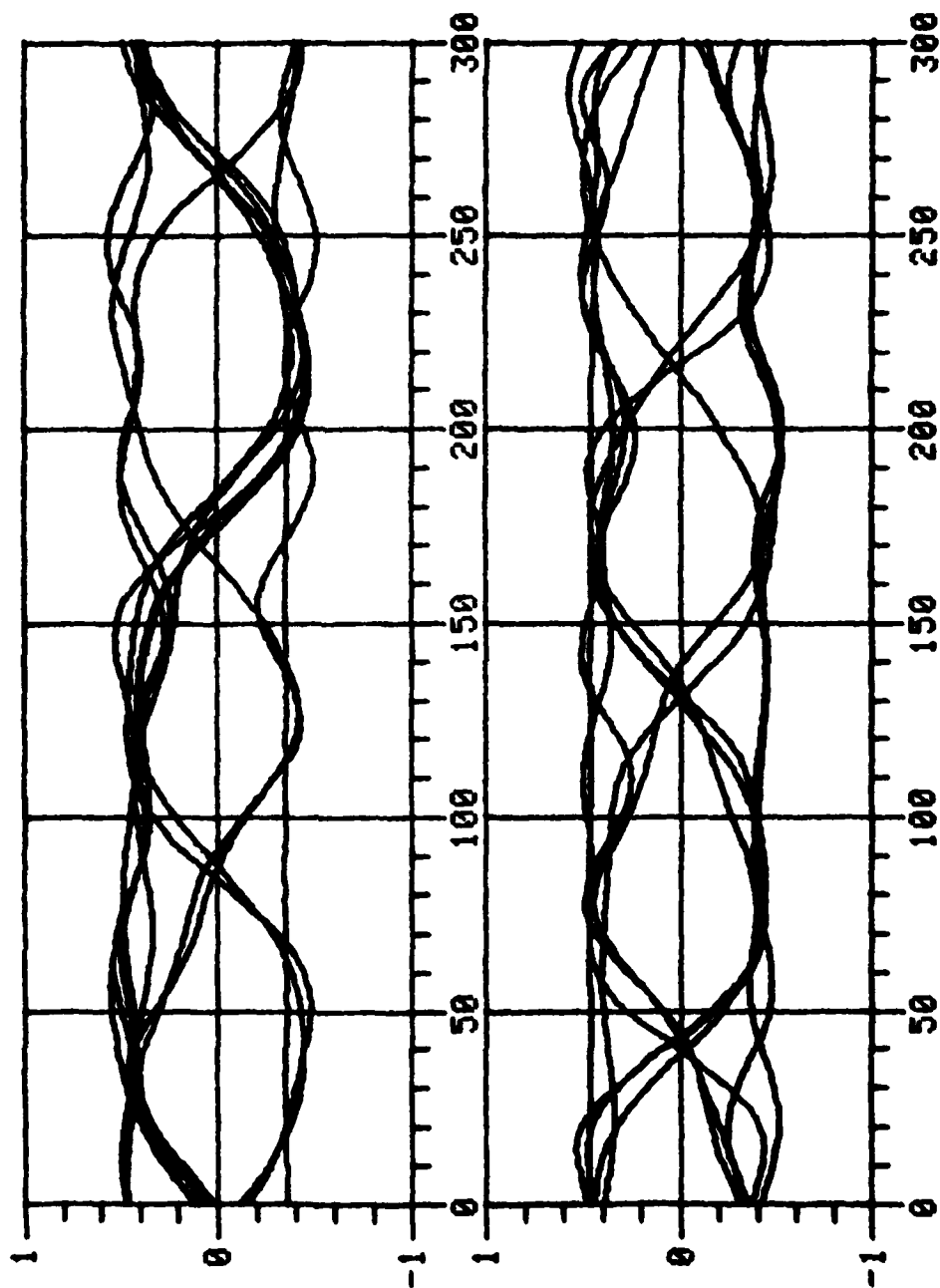
INTERTAP SPACING (0.1 - 1.0 BIT)=.6

POWER PROFILE PLOT



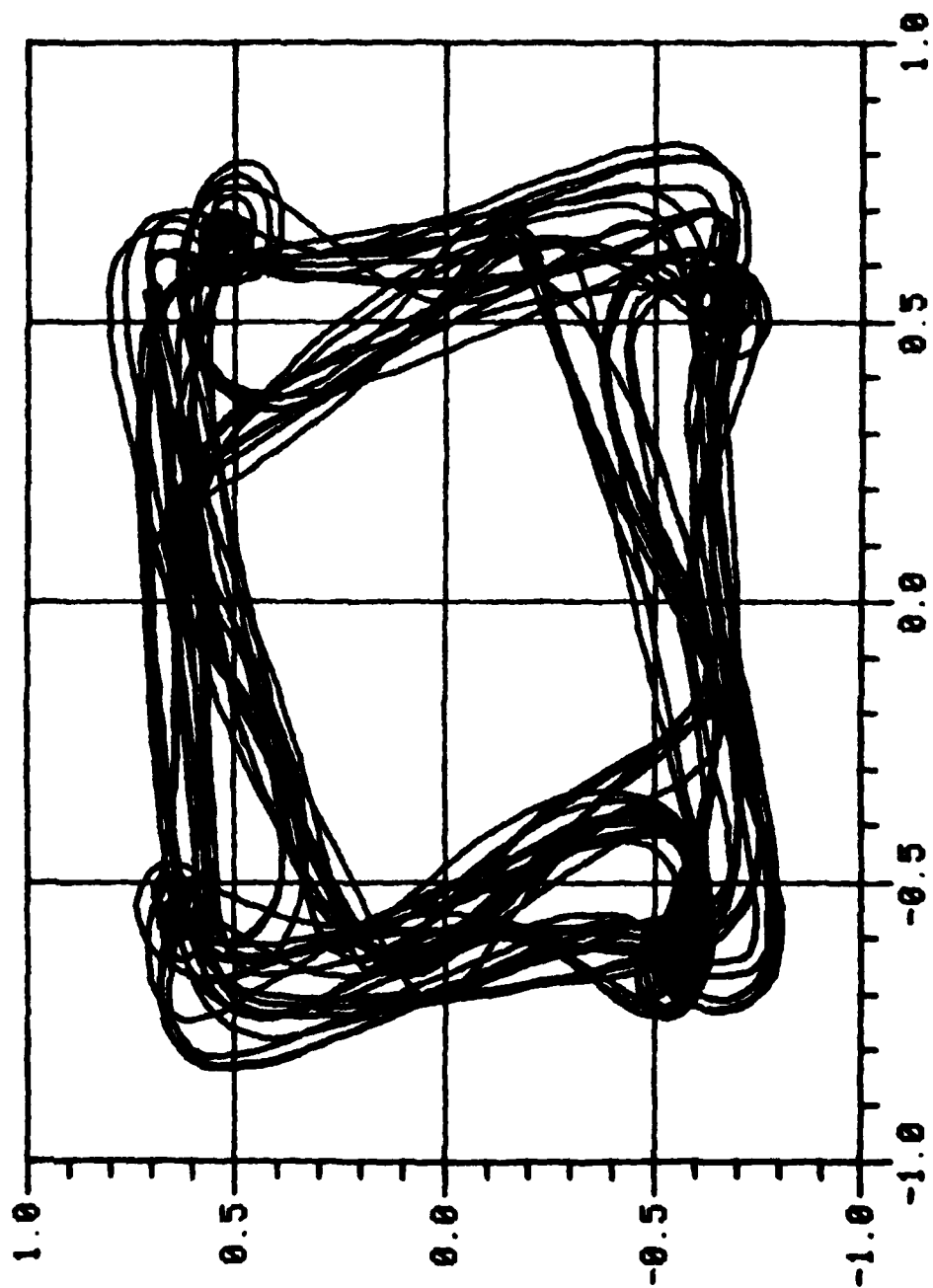
QPSK

EYE PATTERN  
CHANNEL A



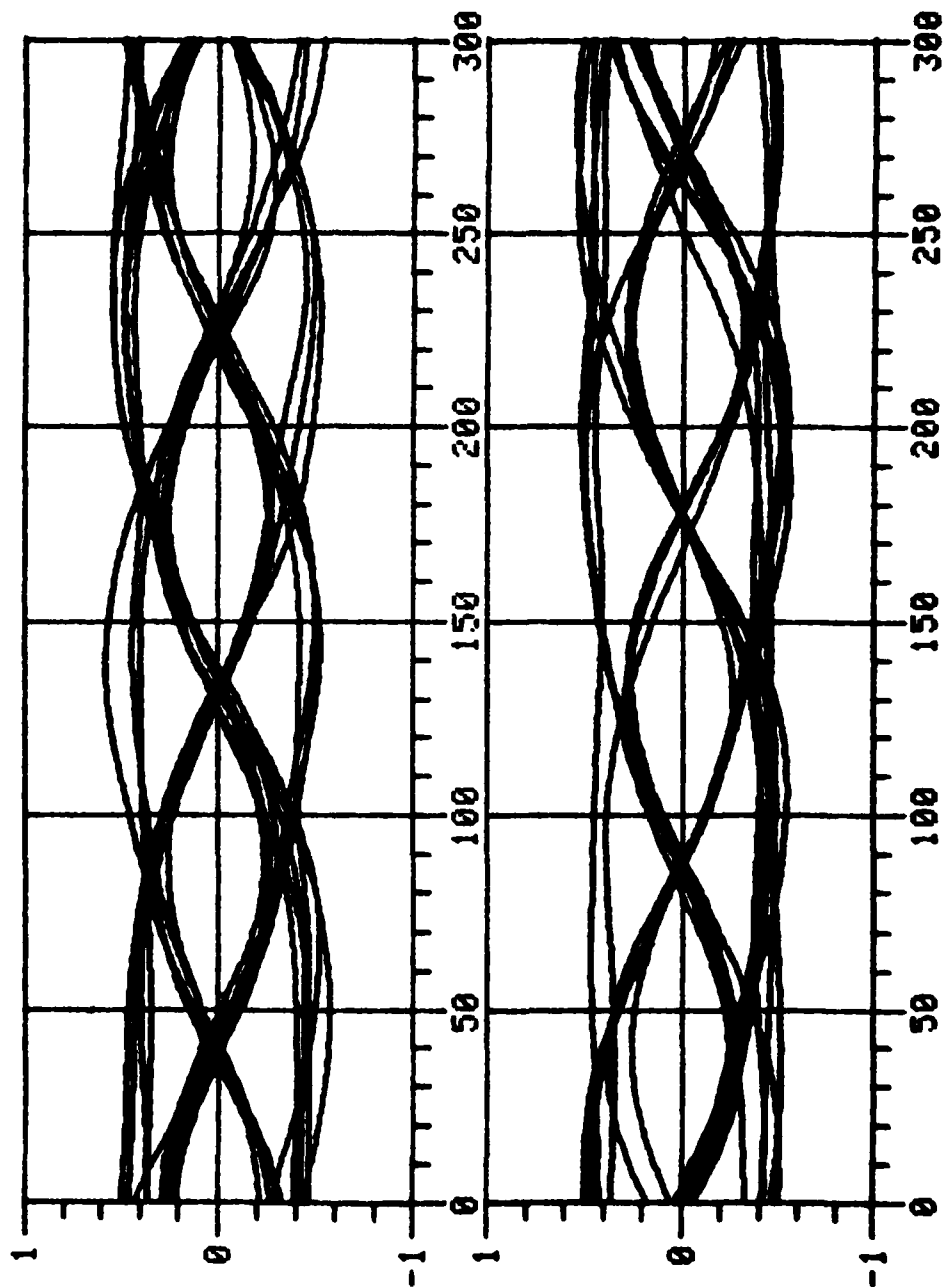
QPSK

CONSTELLATION  
CHANNEL B



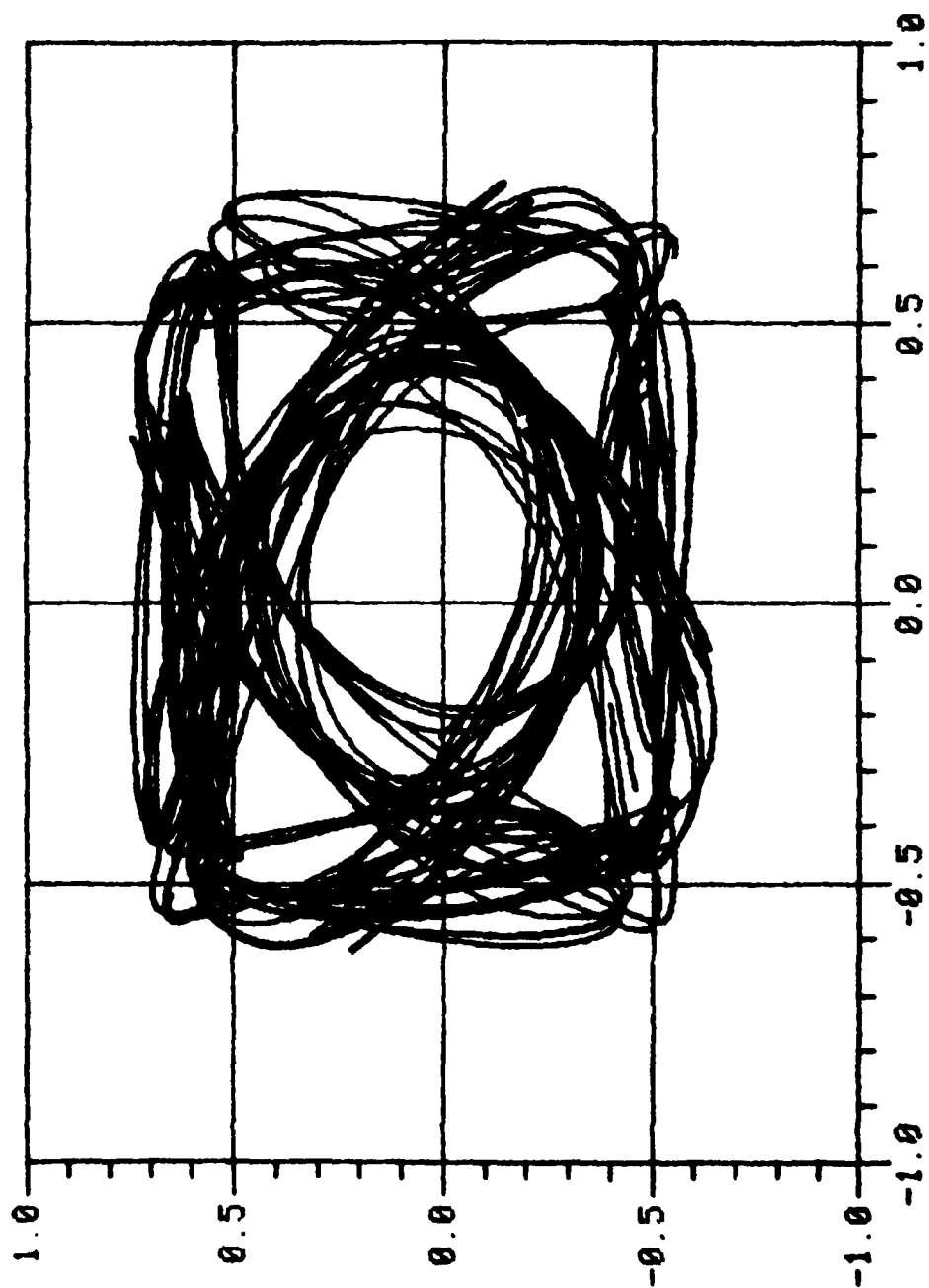
QPR

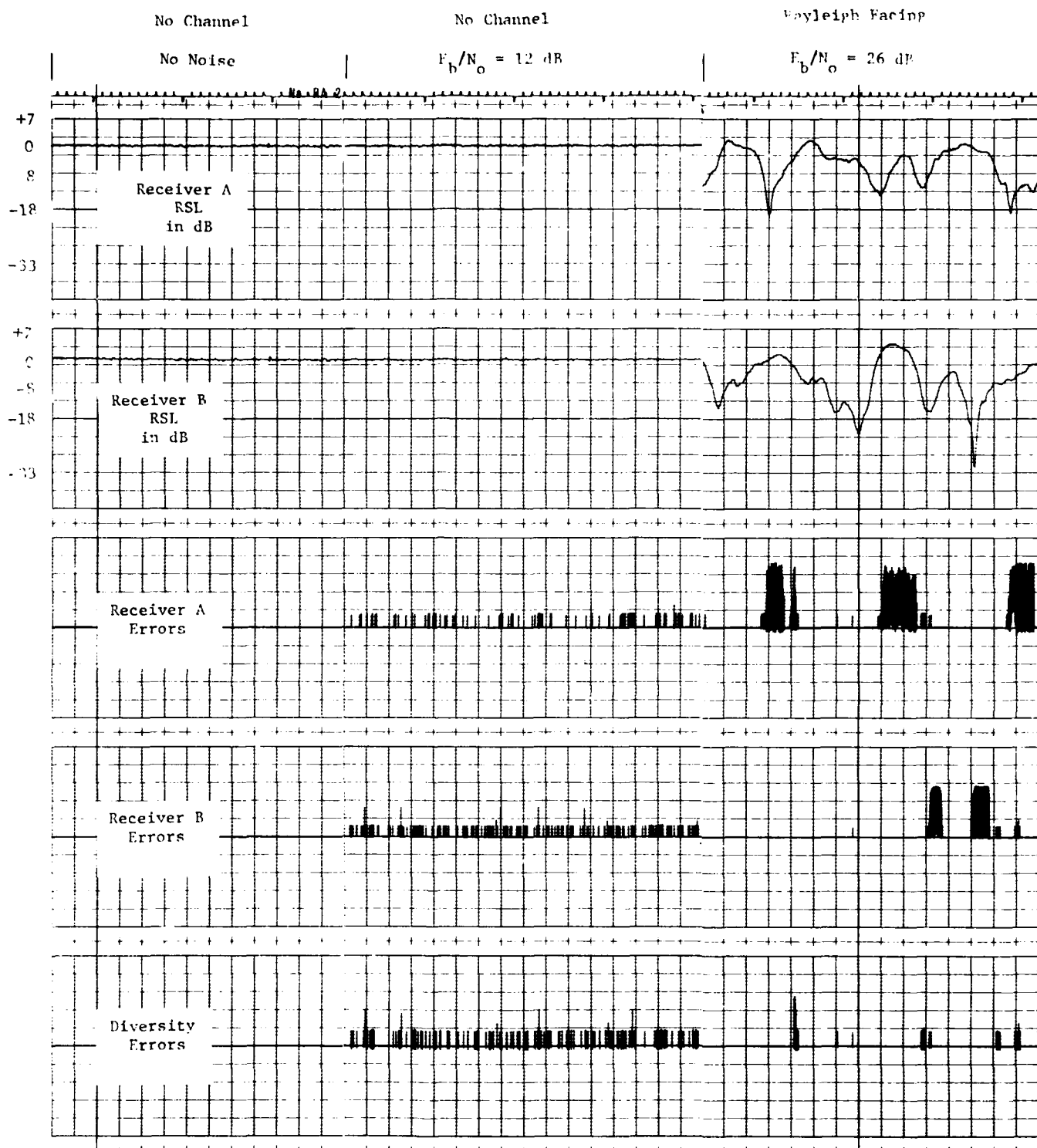
# EYE PATTERN CHANNEL 8



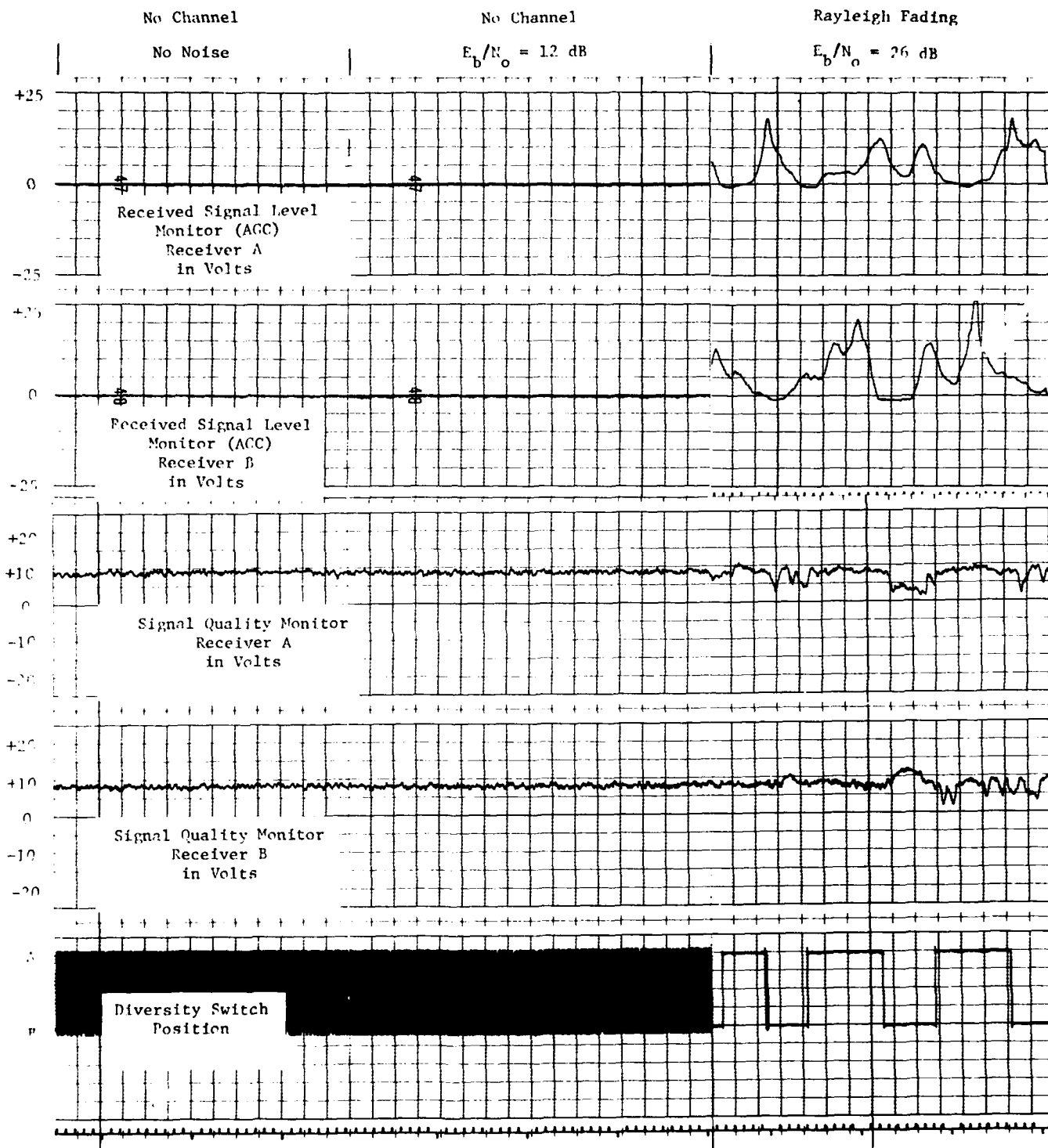
QPR

CONSTELLATION  
CHANNEL A





Analog Stripchart Recordings for QPR Configuration



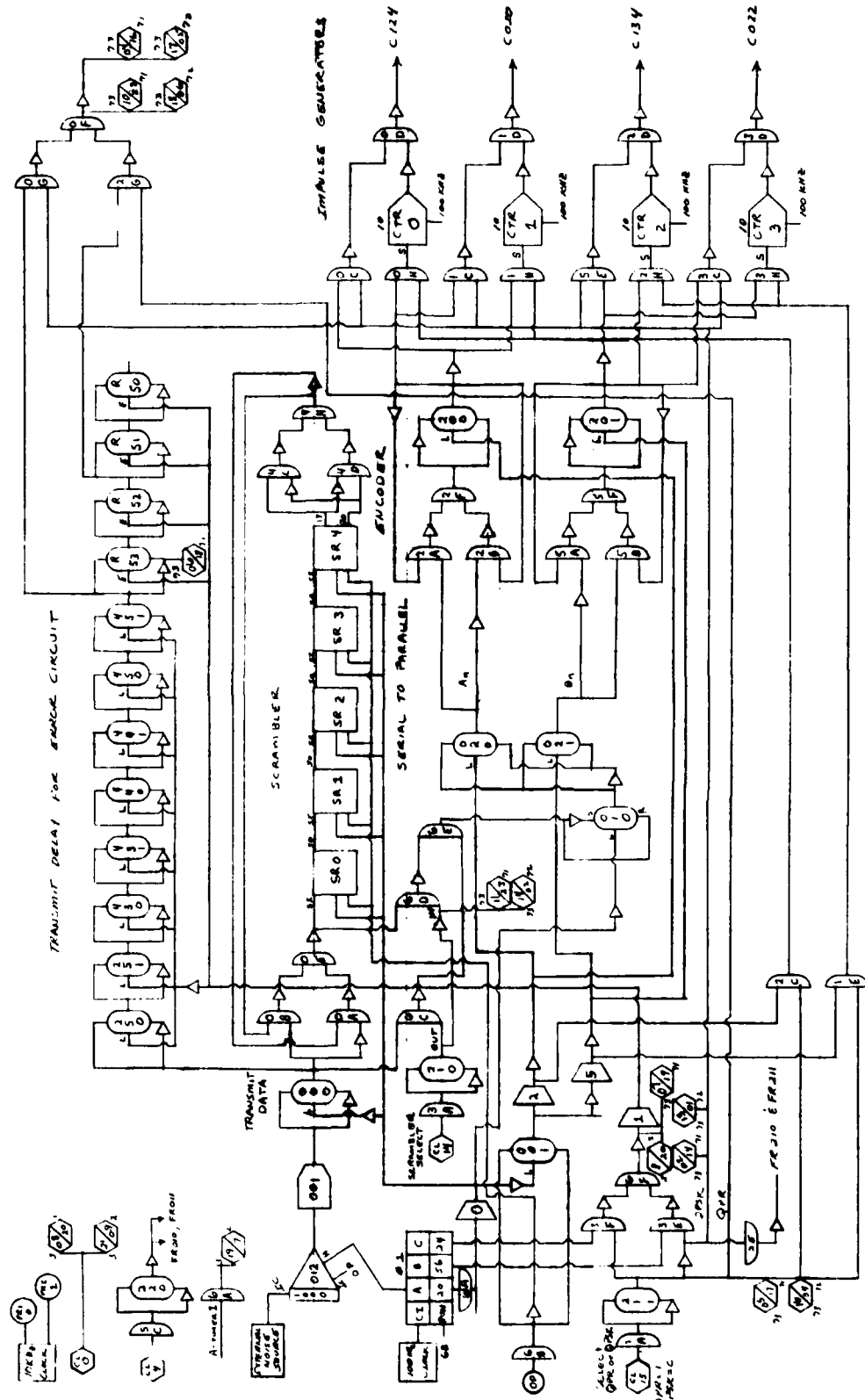
Analog Stripchart Recordings for QPR Configuration

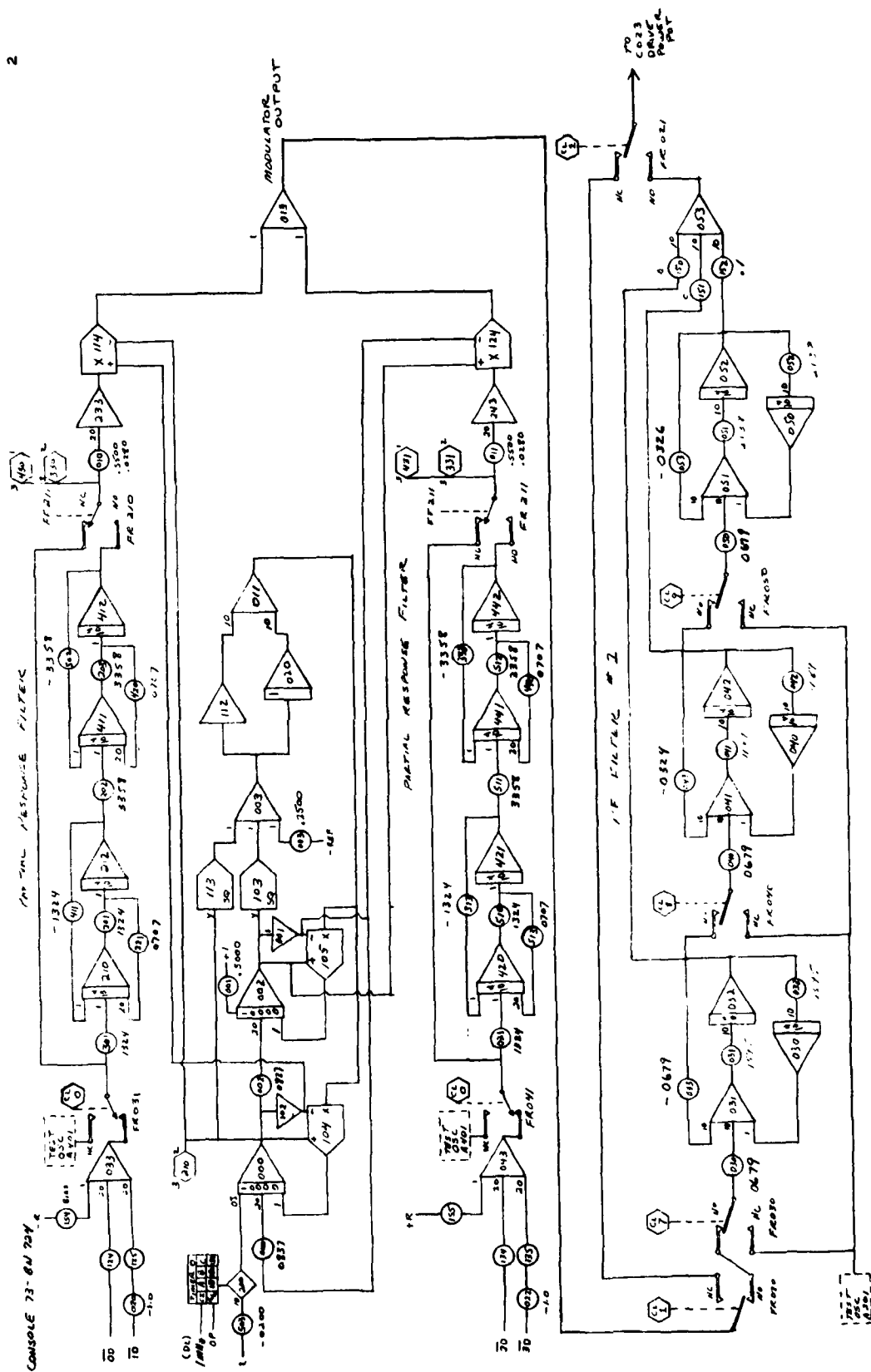
## APPENDIX C

Appendix C contains a complete set of the analog computer diagrams for the DRAMA radio simulation, LOS channel model, performance monitors, diversity combiner, and baseband equalizer.

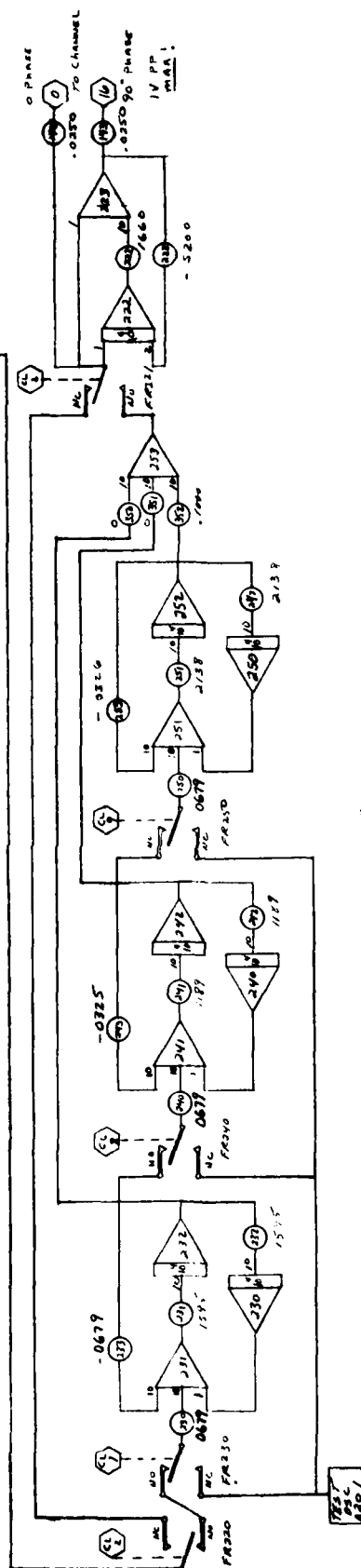
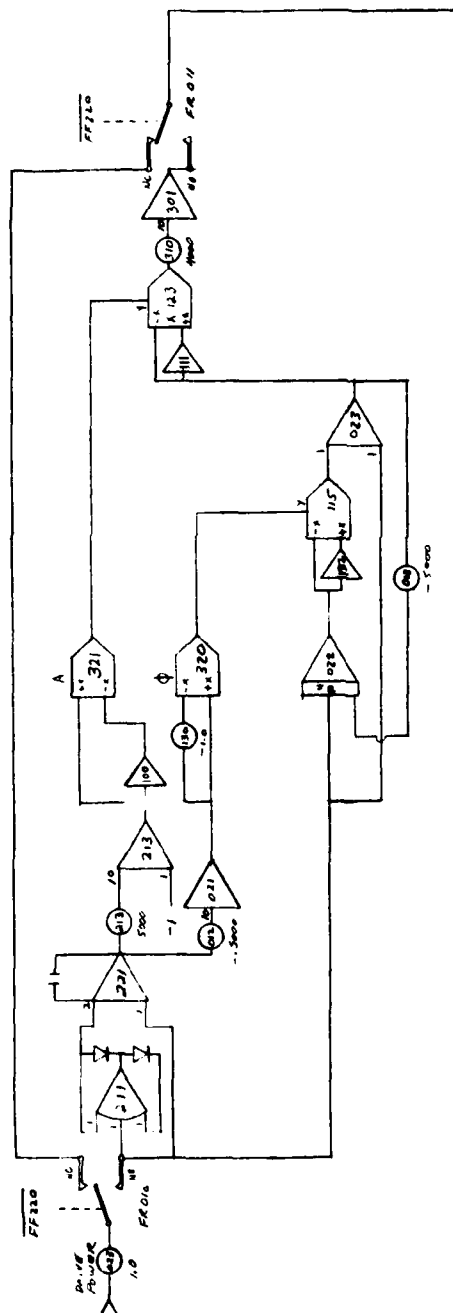
LRAMA RADIO SIMULATION

CONSOLE 73 - 84-284  
LOGIC BOARD QTR #1  
ANALOG BOARD QTR #1



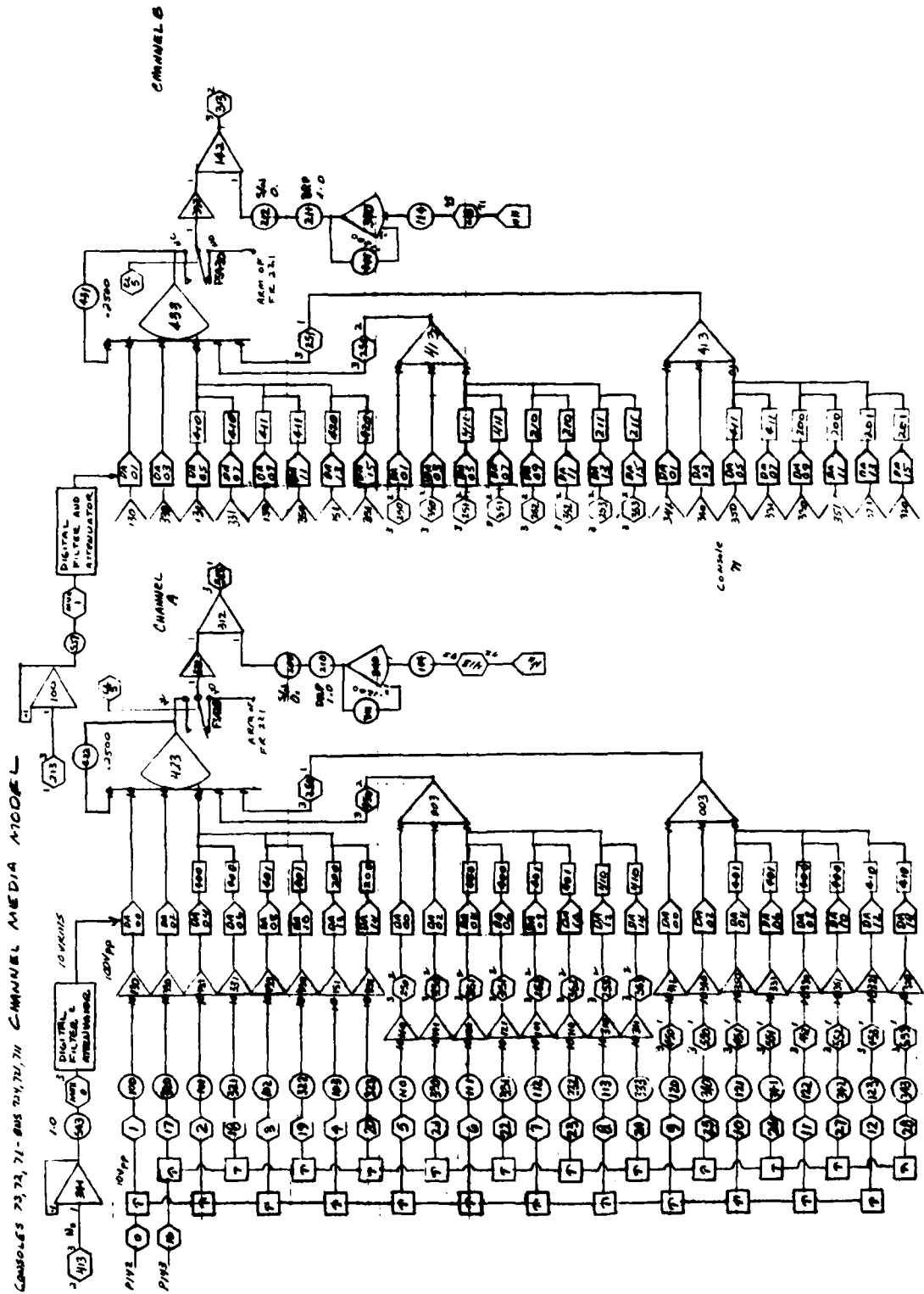


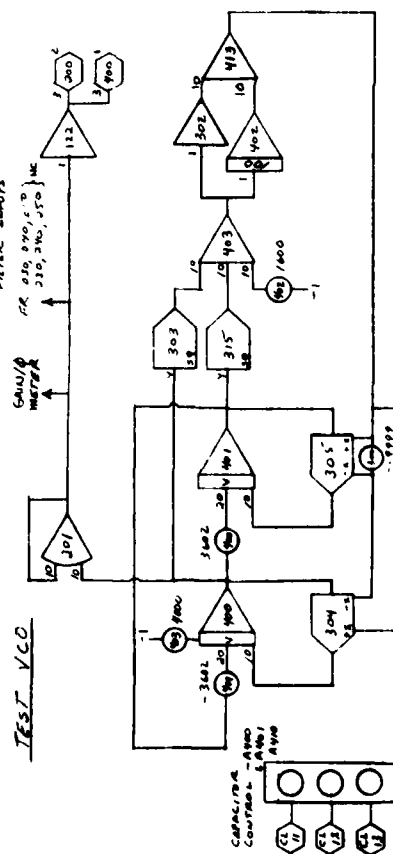
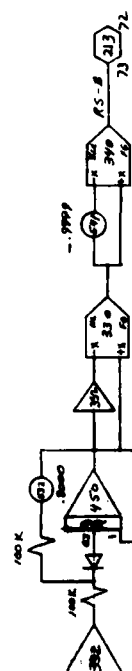
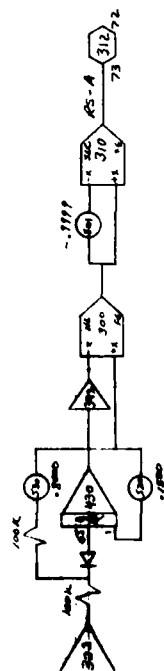
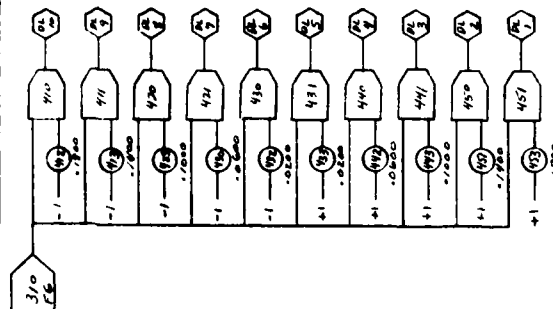
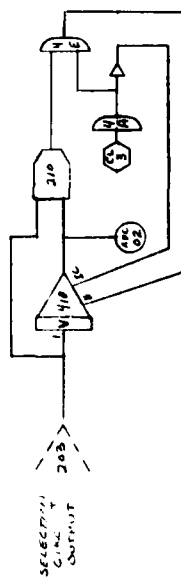
NON-LEAK DEVICE

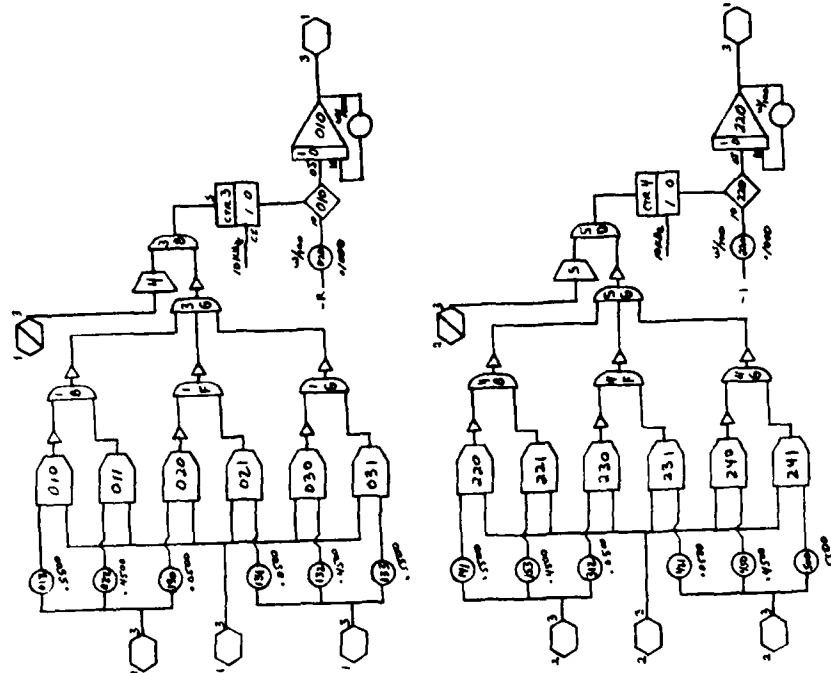


RF 114721-2

CONSOLES 73, 74, 75 - BUS 73, 74, 75 CHANNEL MEDIA A1000EL

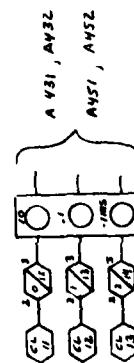
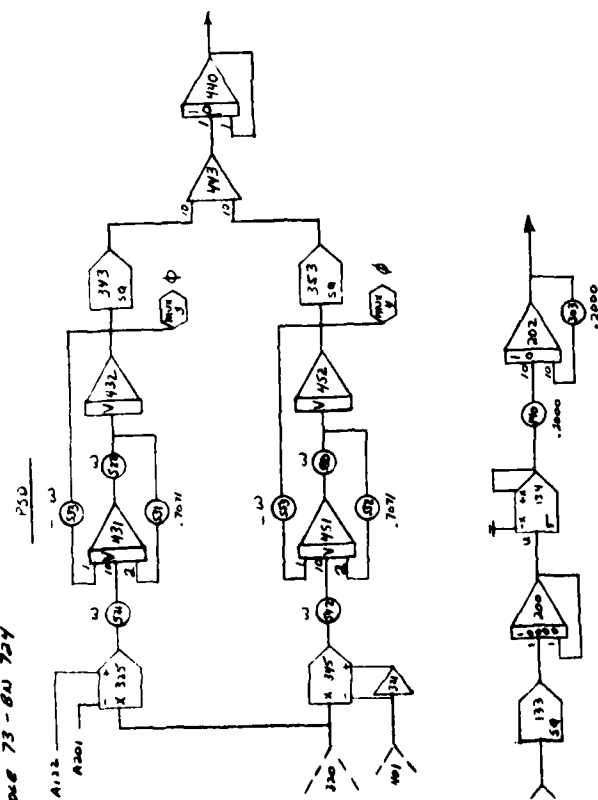






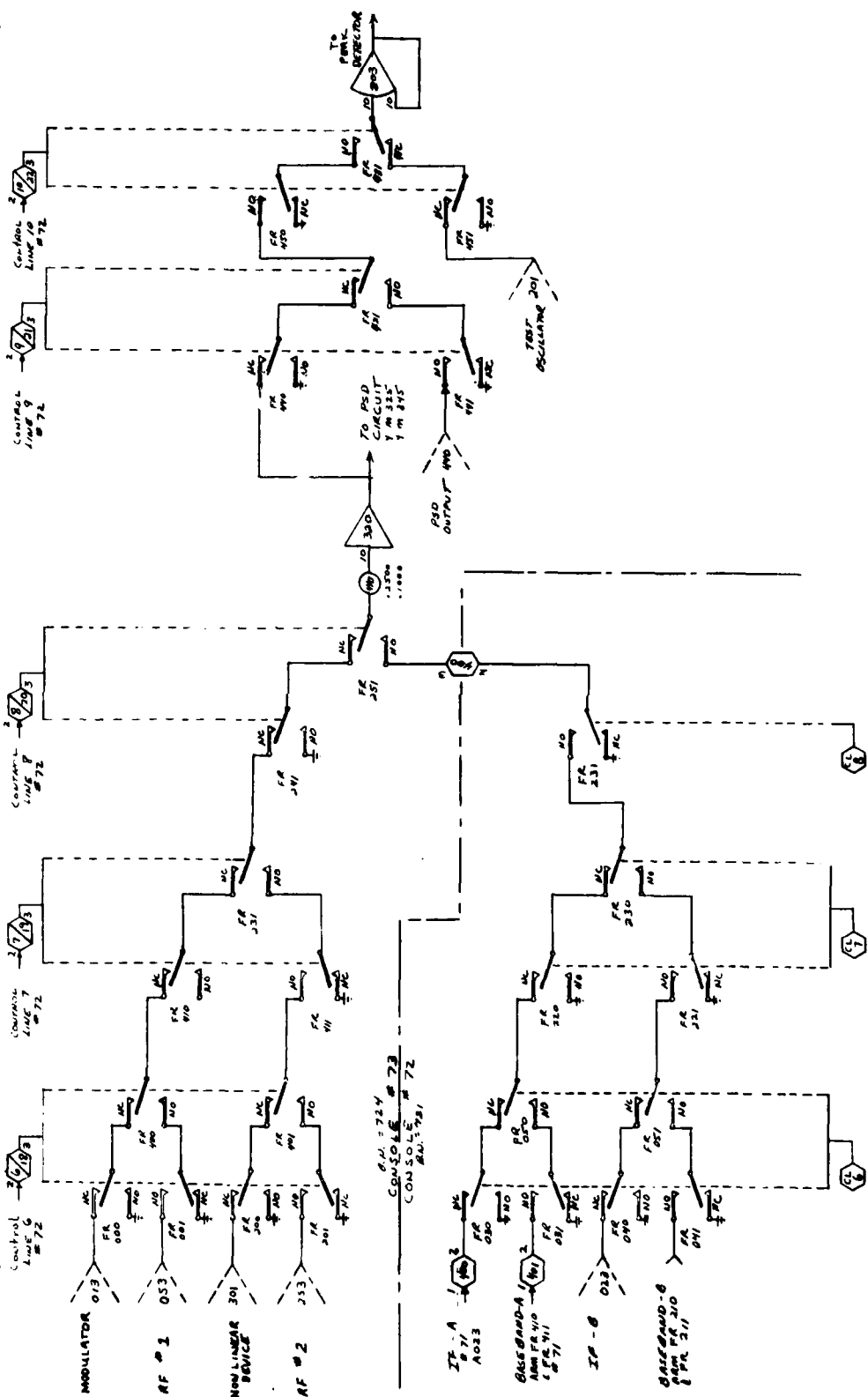
MOTM

Component 73-8A 724



MEASUREMENT AND TEST SELECTION

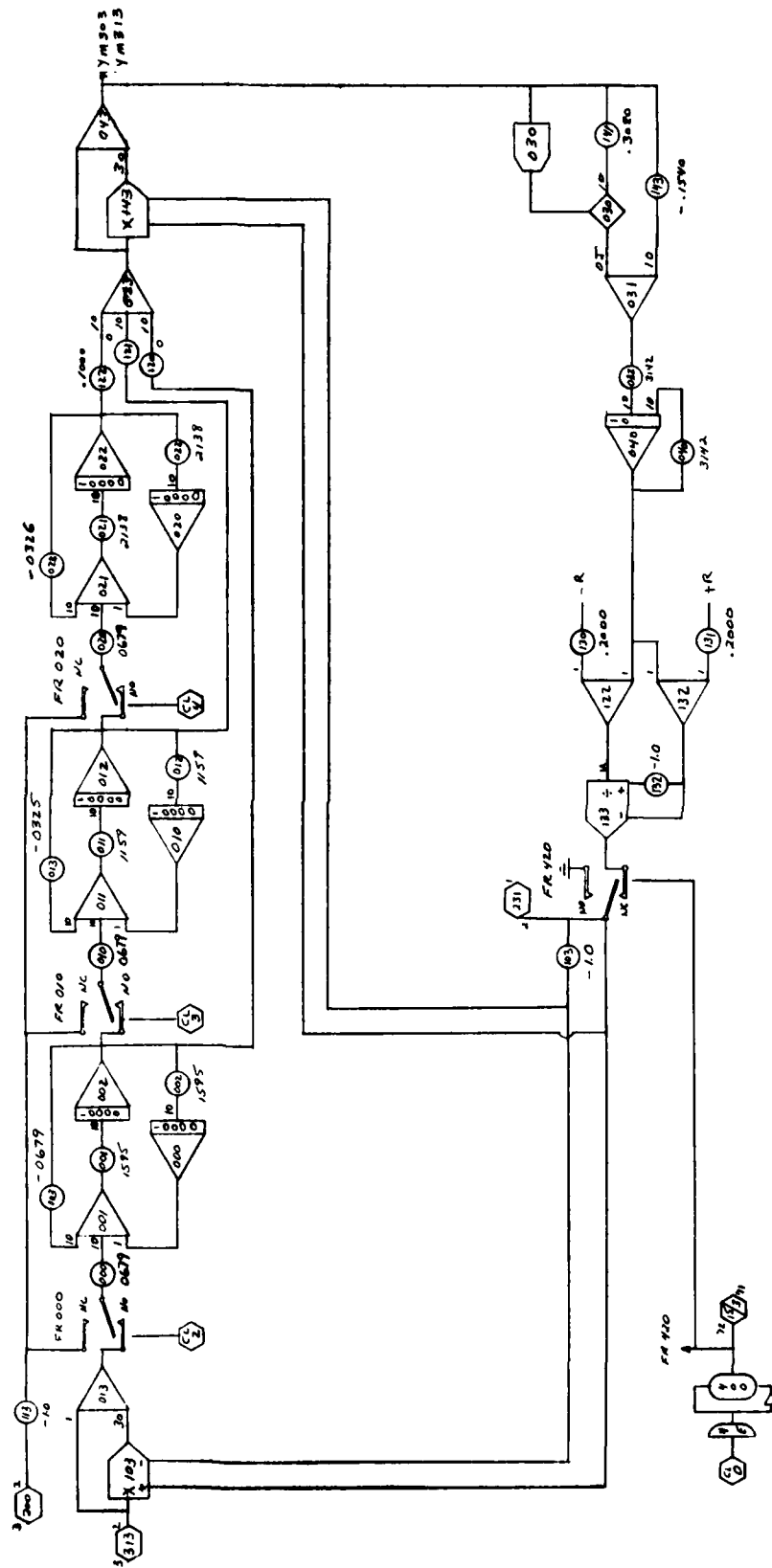
CONSOLES 73, 72 - BUS 704, 721



CONSOLE 73-80 721

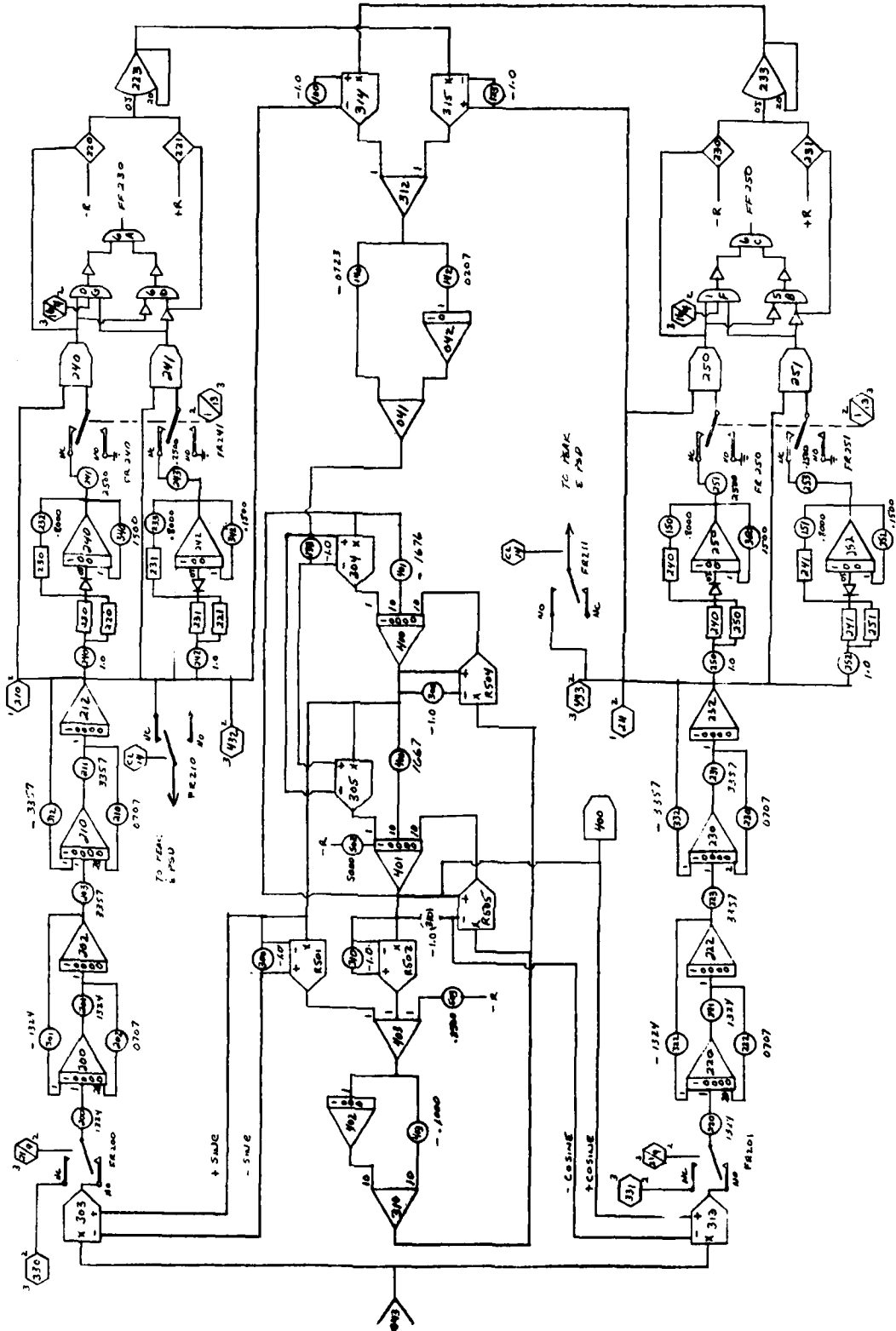
IF SECTION

1

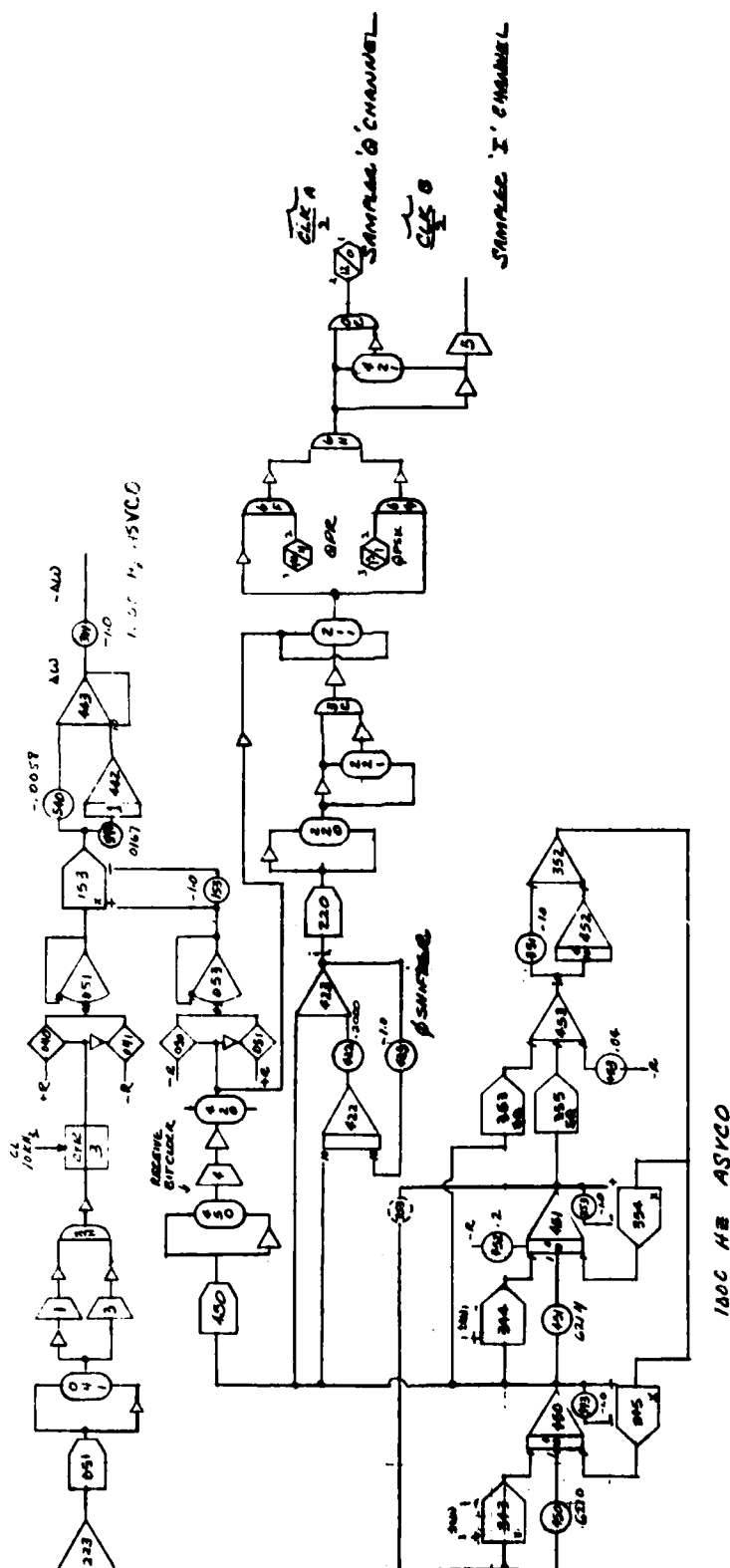


CONSOLE 72 - BU 721

COMPUTATIONAL



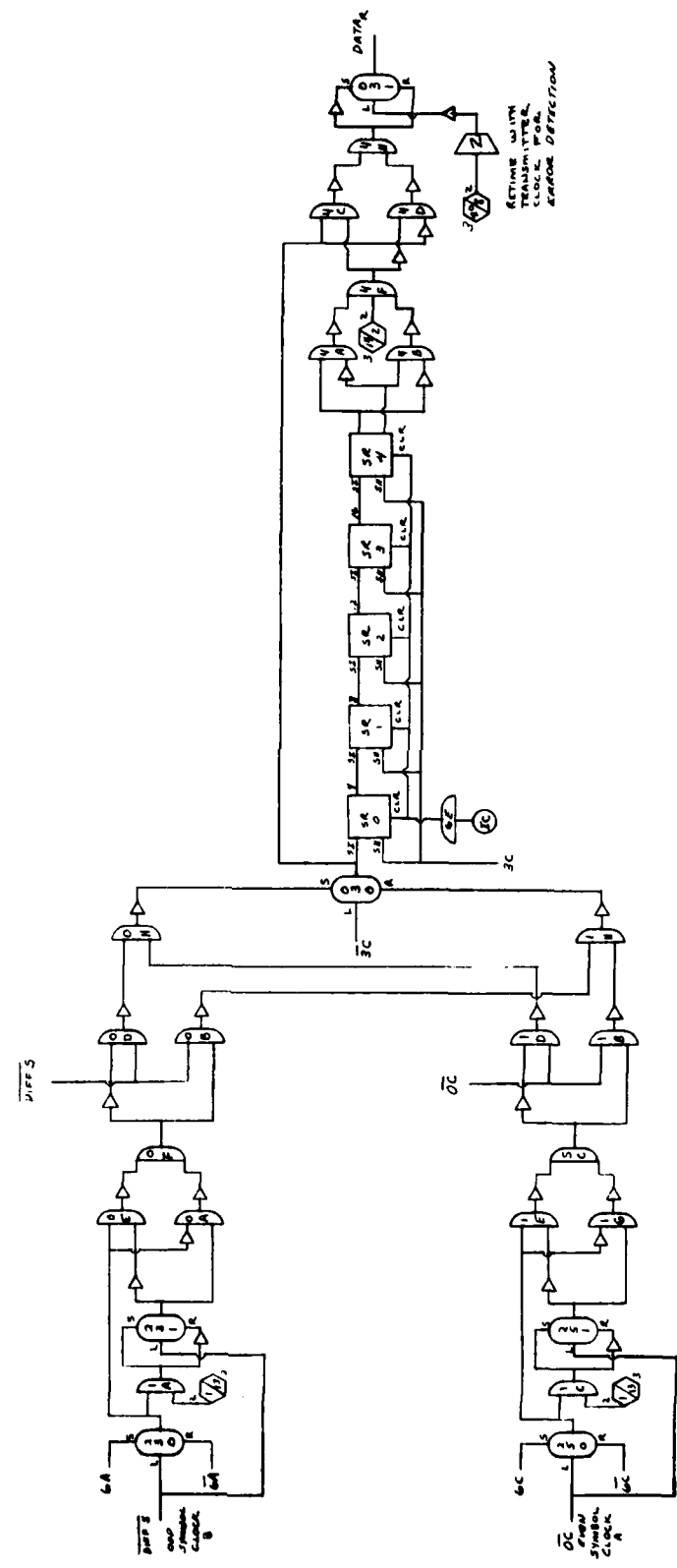
QPR - QRSK - DRAMA CLOCK RECOVERY



4

# DATA REGENERATION

CONSOLE 72-00 721

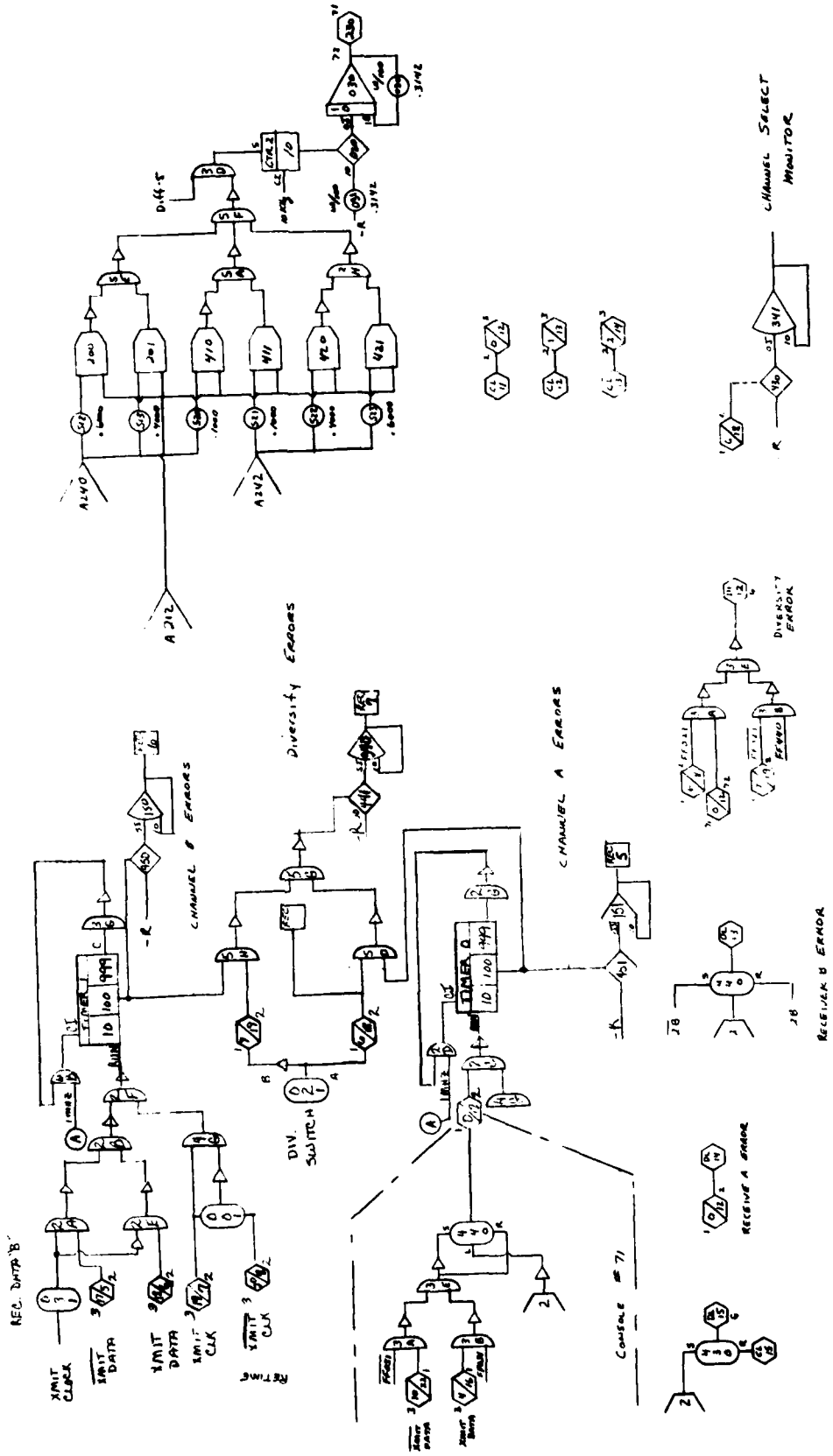


CONSOLES 72, 71 - BUS 72, 71

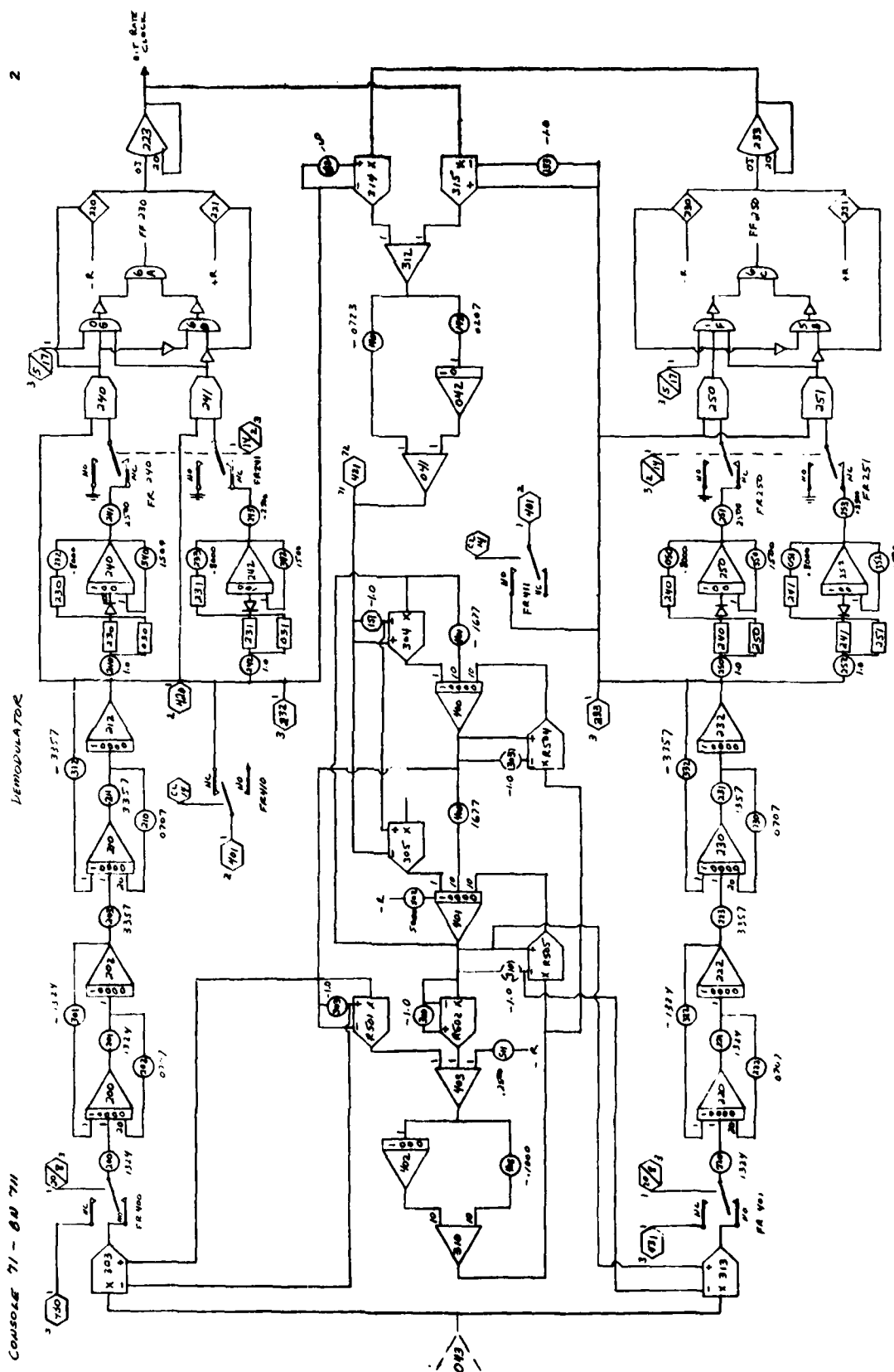
MONITOR WITH UNITS

DIF ERROR DETECTION

DIF DIVERSITY MONITOR



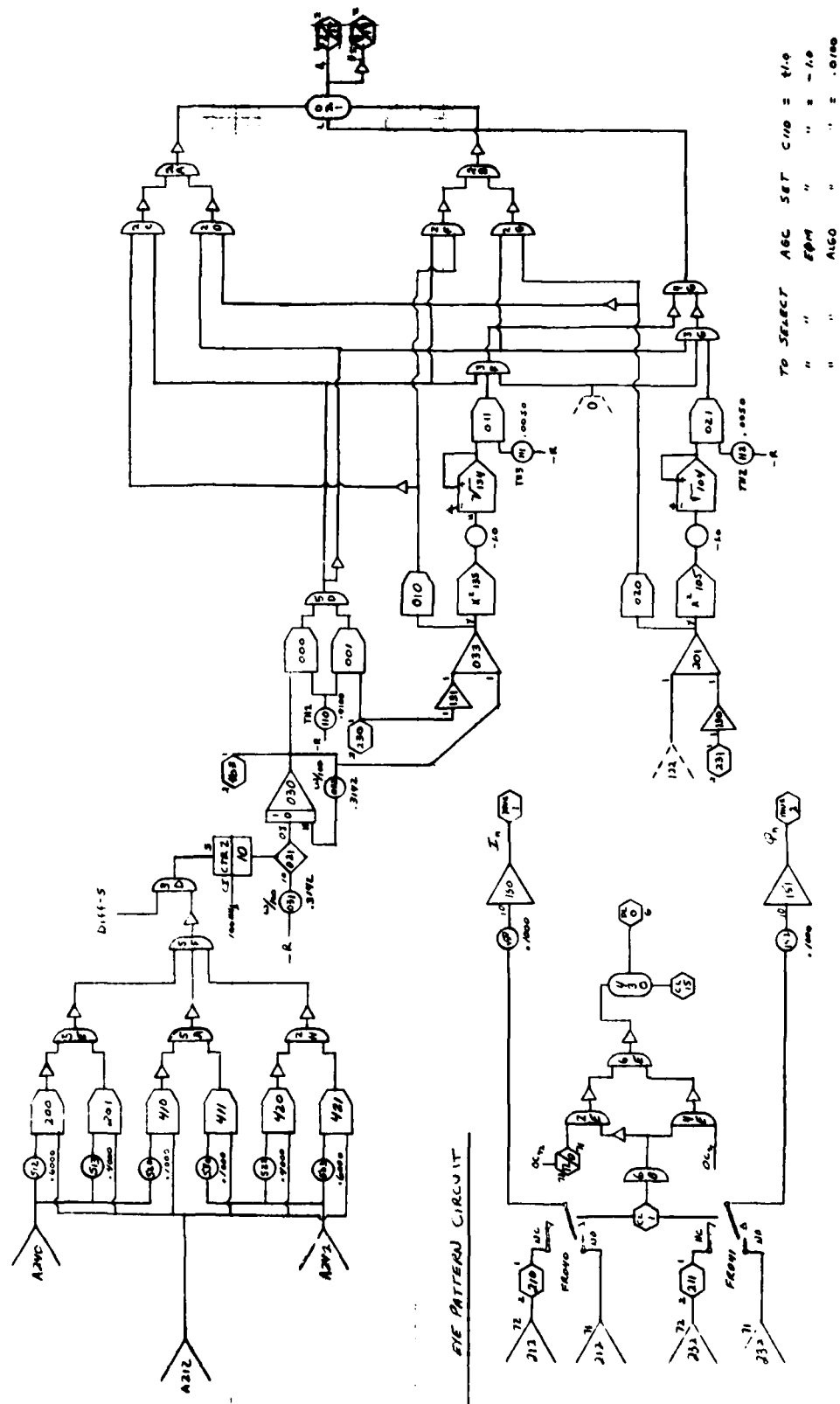




## CLOCK RECOVERY



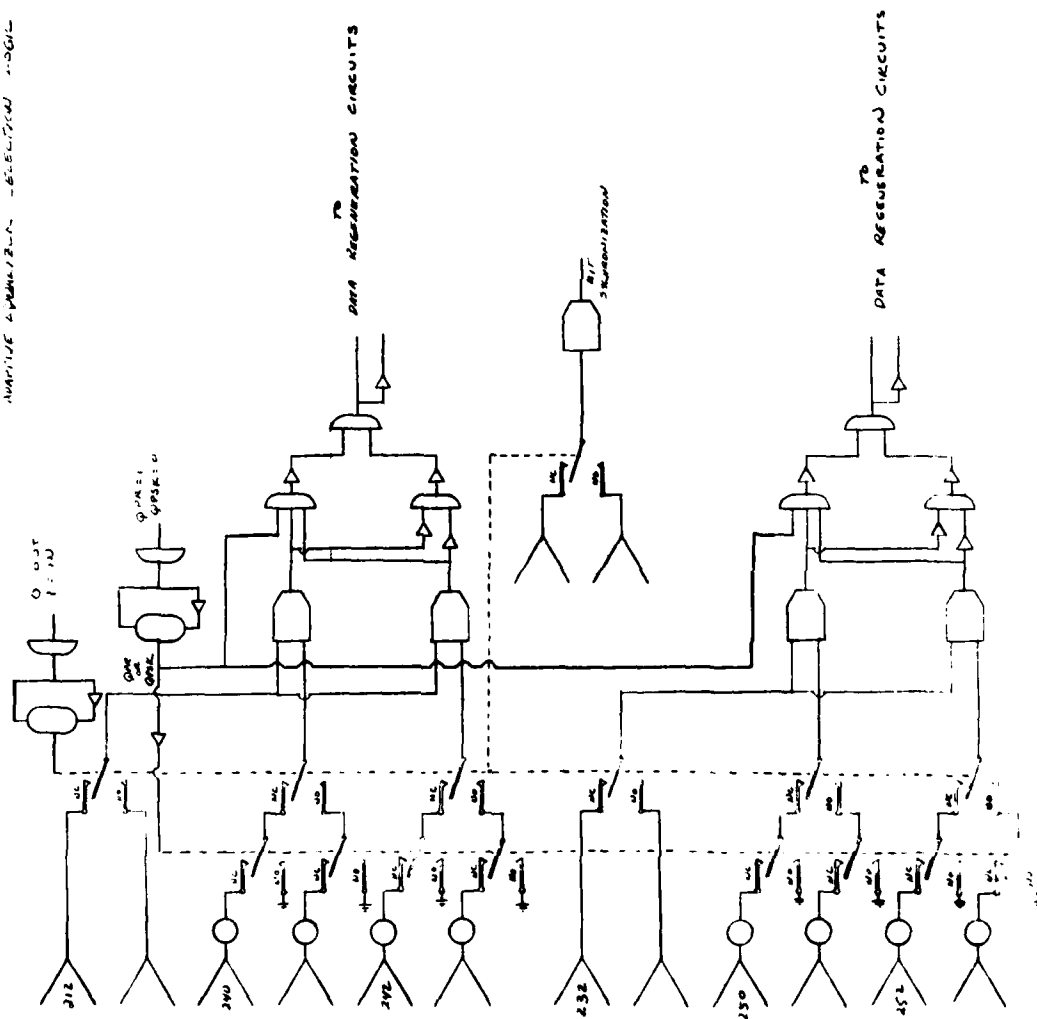


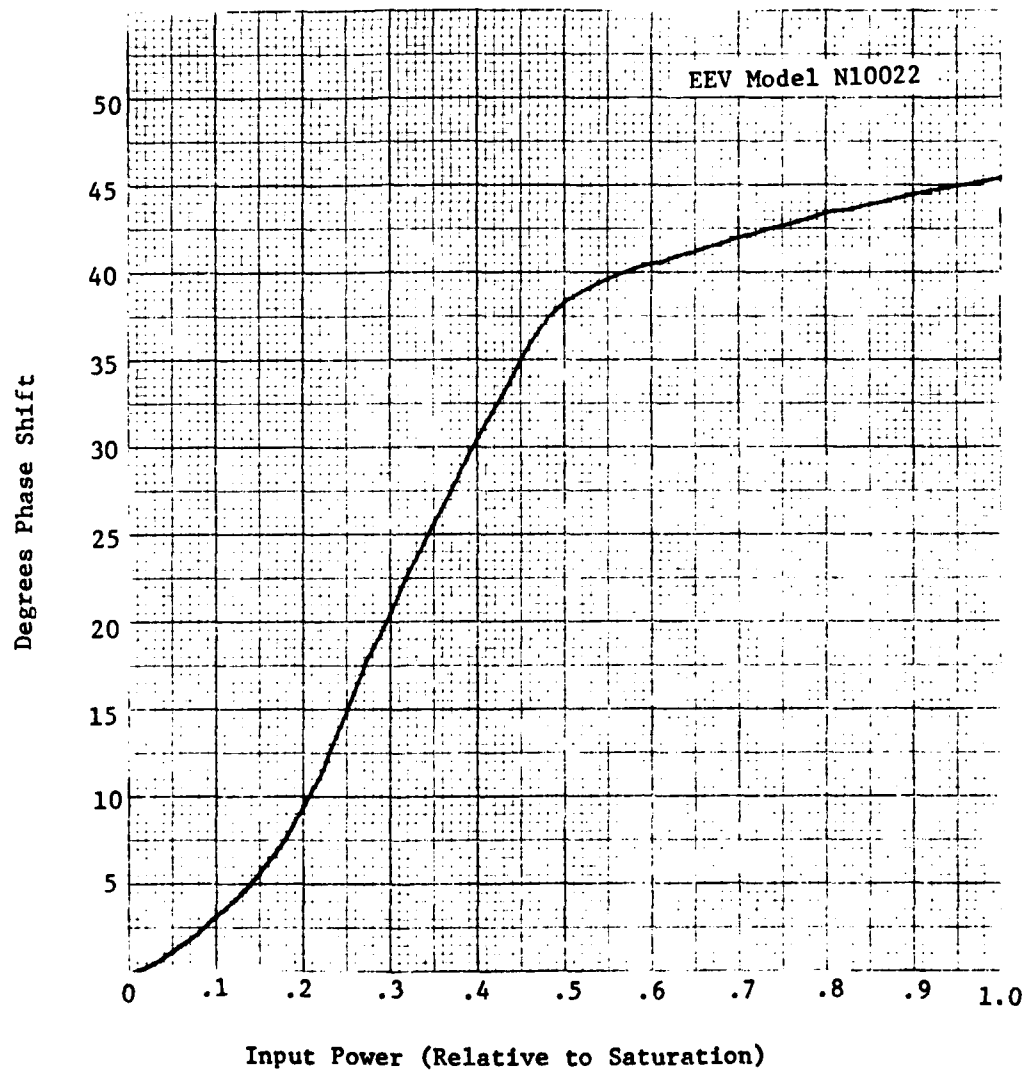


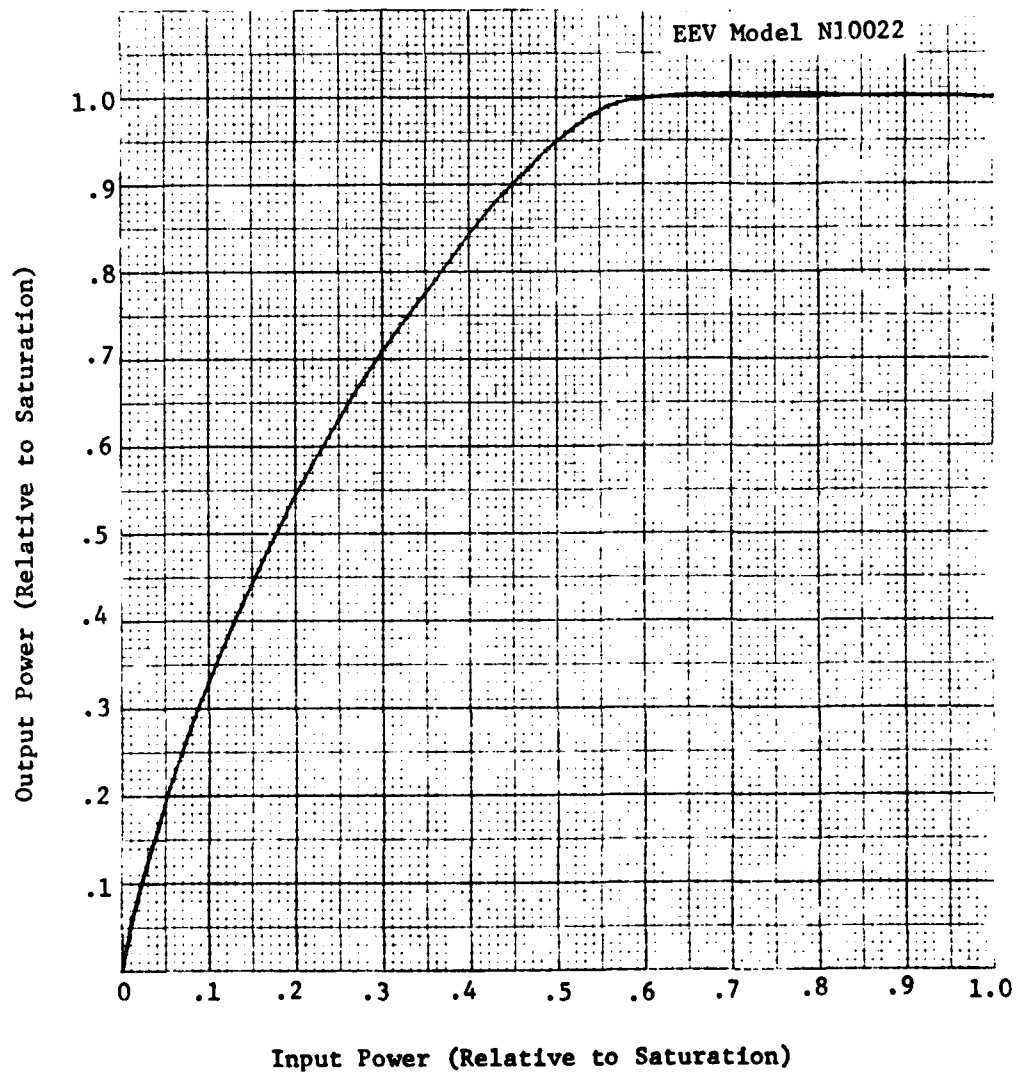
[illegible]

The schematic diagram illustrates the control logic for a digital computer. It features two main input sections at the top, labeled \$I\_1\$ and \$I\_2\$, each with four parallel lines representing data or address buses. These inputs feed into a central processing area containing several multi-input AND gates (represented by pentagons) and OR gates (represented by hexagons). The logic is organized into two symmetrical halves, likely for different stages of computation or memory access. Key components include delay elements labeled "DELAY" and various signal paths indicated by lines connecting the gates. At the bottom, there are output sections with labels like \$-C\_1, -C\_2, -D\_1, -D\_2\$ and other identifiers such as \$A\_1, A\_2, B\_1, B\_2\$. The entire circuit is powered by a \$\pm 2V\$ supply, as indicated by the voltage sources at the bottom.

MANIPULATED - ELECTRIC - SIGNAL







**DATA  
FILM**