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INVESTIGATION OF TECHNOLOGICAL PROBLEMS IN GaAs

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as of April 15, 1976

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SUMMARY

A selection scheme for Cr-doped semi-insulating GaAs substrate for ion implanted FET structures has been developed. The surface resistivity of high quality semi-insulating substrates protected by a Si_3N_4 cap is found to change by less than an order of magnitude after heat treatment at 850°C for 30 minutes. The reproducibility of the carrier concentration profiles achieved by Se implantation into those selected GaAs material (from 5 different boules) is approximately ± 10% in peak doping level and maximum penetration.

A capless annealing technique for the removal of crystal damages induced during ion implantation for FET structures has been successfully carried out. For high dose Se implants, nearly identical electron concentration can be achieved by the capless annealing technique as can be obtained by annealing with an aluminum oxy-nitride protective cap for samples implanted with the same dose and annealed for the same time period and temperature. The complexity of the ion implantation procedure for GaAs device structure preparation is considerably simplified by the development of this novel capless annealing scheme.

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1.0 INTRODUCTION

The lack of reproducibility and reliability in GaAs devices has resulted in low yield and high unit cost, preventing their potential system applications from being realized. The objective of this contract is to investigate and solve technological problems in the development of GaAs devices, such as the IMPATT diode and the Schottky barrier gate FET. The areas of research relevant to these devices are:

A. Growth of high quality semi-insulating GaAs substrate material.

B. Quality evaluation of semi-insulating substrates.

C. Epitaxial growth of high resistivity buffer layers.

D. Growth of ultra-thin and high purity epitaxial layers.

E. Ion implantation to form n-type layers on semi-insulating substrates or device structures.

F. RF measurement on GaAs devices for material characterization and technology evaluation.

These activities are carried out at the Science Center and the participating subcontractors. Improvement in reliability and yield of microwave devices is anticipated as a result of this GaAs technology program.

2.0 PROGRAM GOALS AND TECHNICAL APPROACH

2.1 Epitaxial Material Growth and Characterization

The goal is to investigate material and processing technology to

improve the control of growth parameters, enhancing the reproducibility and the reliability of devices. Problems related to epitaxial film properties such as the uniformity in thickness and carrier concentration, dislocation density, interface properties, surface damage, and background impurity densities are studied.

2.1.1 High Resistivity GaAs Layers

This research program is aimed at establishing parameters (temperature, dopants, distribution coefficients, etc.) necessary for the growth of thin layers of high sheet resistance ($\approx 10^5$ ohm/□) GaAs on semi-insulating GaAs substrates by means of liquid phase epitaxial (LPE) techniques. In addition, the electrical properties of these layers are measured to study electron transport mechanism and to provide information for device applications.

2.1.2 Ultra-Thin Layer Growth

Methods of growing submicron liquid phase epitaxial GaAs films with rigid tolerance on layer thickness and carrier concentration are being developed. Emphasis is on uniformity and reproducibility which are required for high yield in device production.

2.2 Semi-Insulating Material

The goal is to improve the state-of-the-art in material growth and characterization, so that a reproducible control on the doping characteristics of the material can be reached.

2.2.1 Crystal Growth

Bulk semi-insulating GaAs is grown by the horizontal Bridgman method. The effects of different concentrations of compensating dopants, namely oxygen and chromium, on the electrical properties of the material are being studied. New approaches aimed at a reduction of Si contamination are being attempted.

2.2.2 Material Evaluation

The goal is to evaluate semi-insulating GaAs crystals prepared under various conditions. Effect of impurities and growth procedure on material properties such as resistivity, carrier concentration and dislocation densities are studied. Transport measurements are used to test and model the mechanism of electrical compensation. Measurements of potential profiles across dc biased p-i-p and n-i-n structures using high resolution Auger Electron Spectroscopy in a scanning electron microscope are employed to investigate the density and the characteristics of the electrically active traps. The effect of heat treatment in H_2 atmosphere on the electrical compensation of the material is studied by measurements of sheet resistance and photoluminescence.

2.3 Ion Implantation

The goal is to investigate the effect of ion beam energy, dosage, and species of impurities on the carrier concentration profile of ion implanted GaAs substrates under various annealing conditions. The effectiveness of the annealing caps for the substrate surface during the annealing process is also being investigated. A combination of controlled stripping and C-V Hall measurements is being used to characterize the implanted layers.

2.4 Material Characterization--Theoretical and Experimental Investigation of the Effect of Material Properties on Device Performance

Electrical measurements performed on GaAs devices are employed to evaluate the effect of material parameters on device performance. Basic material parameters, such as the asymmetry of the hole and electron ionization rate and saturation characteristics are derived from data obtained on GaAs IMPATT amplifiers. Surface passivation techniques are studied. The effect of interface properties between the active layer and the semi-insulating substrate of GaAs FETs on device performance is investigated. FET devices made on epitaxially grown and ion implanted active layers are compared.

3.0 RESULTS

3.1 Epitaxial Material Growth and Characterization

3.1.1 LPE Activities at Stanford University, High Resistivity GaAs

During the past quarter, the work was concentrated on finding the bakeout transition temperature for the fused quartz-pyrolytic boron nitride-hydrogen (SiO_2-BN-H_2) system. Twenty-seven layers were grown in this system at bakeout temperatures ranging from 700 to 800°C. It was found that for bakeout temperatures about 700°C, with an accumulated bakeout period of more than 30 hours and a hydrogen flow rate of 0.6 ℓ/min, all layers were p-type and had carrier densities larger than $2\times10^{14}cm^{-3}$. It thus appears that the bakeout transition temperature for the SiO_2-BN-H_2 system is below 700°C.

Anodic oxidation of GaAs in aqueous H_2O_2 solutions was examined. Preliminary results show that one can remove up to 0.5μm of GaAs during each anodization step. This technique will be applied to differential Van der

Pauw measurements on semi-insulating GaAs LPE layers.

During this quarter, four high-resistivity layers (#1313, 1317, 1325 and 1326) were sent to the Science Center for further evaluation and device applications.

3.1.1.1 Growth Studies

Previous studies of the SiO_2-C-H_2 and SiO_2-BN(C)-H_2 systems showed that the bakeout transition temperatures were 775 and 700°C, respectively. Therefore, we expected that the SiO_2-BN-H_2 system, without carbon in the system, would have a bakeout transition temperature below 700°C. However, the first two series of growths (series #1400 and 1500)[1] showed that all of the layers grown from melts baked out at 700°C in the newly constructed SiO_2-BN-H_2 system were n-type. Note that, in all of our studies, a new melt is used in each series of growths. The third series of growths (#1600)[1] showed that for a bakeout temperature of 800°C, the stabilized undoped melt unyielded p-type layers with carrier densities in the range of $2x10^{14}cm^{-3}$.

In the current growth series #1700 (see Table 3.1.1) carried out at a bakeout temperature of 850°C and a bakeout period of 15 hours between each growth, p-type layers with carrier densities of $1x10^{15}$ to $3x10^{15}cm^{-3}$ were obtained after an accumulated 30 hours of bakeout. When 0.5 atomic % of chromium (Cr) was added to the same melt, the layers showed no change in their electrical properties. Based on these results, we assumed that the bakeout transition temperature was in the 700 to 800°C range. Two more series of growths were carried out, #1800 and 1900. In growth series #1800 (see Table 3.2.2), layers were grown from a melt baked out at temperatures between 790 to 750°C. After 30 hours of accumulated bakeout, all grown layers were p-type

TABLE 3.1.1

PROPERTIES OF EPITAXIAL GaAs LAYERS GROWN IN A SiO_2-BN-H_2 SYSTEM
GROWTH SERIES #1700

Growth Conditions: Bakeout Temperature: 850°C; Bakeout Period: 15 hrs.
Growth Temperature: 700°C; Cooling Rate: 4.5°C/min
H_2 Flow Rate: 0.6 ℓ/min.

Growth No.	Dopant	Mobilities @300/77°K (cm^2/V-sec)	Carrier Densities @300/77°K (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1701	-	5,700/39,000	$3.5/3.0 \times 10^{14}$	3.1	n
1702	-	1,350/ -	1.2×10^{15}/ -	3.8	n
1703	-	460/ -	1.1×10^{15}/ -	12	p
1704	-	450/5,700	$2.9/1.4 \times 10^{15}$	5	p
1705	-	400/5,300	$2.6/1.3 \times 10^{15}$	6	p
1706	-	(Grown on n^+ substrate)			
1707	-	350/4,500	$2.7/1.0 \times 10^{15}$	7	p
1708	Cr.(0.5 atm %)	350/ -	4.8×10^{14}/ -	37	p
1709	"	280/4,100	$2.1 \times 10^{15}/3.0 \times 10^{14}$	11	p
1710	"	380/5,400	$1.9 \times 10^{15}/8.5 \times 10^{14}$	9	p
1711	"	(Grown on n^+ substrate)			
1712	"	400/4,800	$1.9/1.0 \times 10^{15}$	9	p

TABLE 3.1.1

PROPERTIES OF EPITAXIAL GaAs LAYERS GROWN IN A SiO_2-BN-H_2 SYSTEM
GROWTH SERIES #1700

Growth Conditions: Bakeout Temperature: 850°C; Bakeout Period: 15 hrs.
Growth Temperature: 700°C; Cooling Rate: 4.5°C/min
H_2 Flow Rate: 0.6 ℓ/min.

Growth No.	Dopant	Mobilities @300/77°K (cm^2/V-sec)	Carrier Densities @300/77°K (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1701	-	5,700/39,000	$3.5/3.0 \times 10^{14}$	3.1	n
1702	-	1,350/ -	1.2×10^{15}/ -	3.8	n
1703	-	460/ -	1.1×10^{15}/ -	12	p
1704	-	450/5,700	$2.9/1.4 \times 10^{15}$	5	p
1705	-	400/5,300	$2.6/1.3 \times 10^{15}$	6	p
1706	-	(Grown on n^+ substrate)			
1707	-	350/4,500	$2.7/1.0 \times 10^{15}$	7	p
1708	Cr.(0.5 atm %)	350/ -	4.8×10^{14}/ -	37	p
1709	"	280/4,100	$2.1 \times 10^{15}/8.0 \times 10^{14}$	11	p
1710	"	380/5,400	$1.9 \times 10^{15}/8.5 \times 10^{14}$	9	p
1711	"	(Grown on n^+ substrate)			
1712	"	400/4,800	$1.9/1.0 \times 10^{15}$	9	p

TABLE 3.1.2

PROPERTIES OF UNDOPED EPITAXIAL LAYERS GROWN IN A SiO_2-BN-H_2 SYSTEM

GROWTH SERIES #1800 AND 1900

Growth Conditions: Growth Temperature: 700°C; Cooling Rate: 4.5°C/min
H_2 Flow Rate: 0.6 ℓ/min

Growth No.	Bakeout Temperature (°C)/Period (hr.)	Mobilities @300/77°K (cm^2/V-sec)	Carrier Densities @300/77°K (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1801	790/1	2,000/5,100	$1.8/1.4 \times 10^{14}$	17	n
1802	790/15	1,500/13,000	$3.0/2.5 \times 10^{14}$	14	n
1803	790/15	380/5,500	$2.0/1.9 \times 10^{14}$	82	p
1804	790/15	460/8,000	$3.2/2.8 \times 10^{14}$	43	p
1805	780/15	530/ -	5.7×10^{14}/ -	21	p
1806	780/15	470/6,100	$2.4/1.4 \times 10^{14}$	56	p
1807	780/15	510/11,000	$1.8/1.5 \times 10^{14}$	87	p
1808	770/15	380/6,600	$3.0/2.3 \times 10^{14}$	56	p
1809	750/15	340/6,100	$3.5/2.5 \times 10^{14}$	52	p
1901	-	6,100/56,000	$6.0/5.4 \times 10^{14}$	2	n
1902	750/15	5,100/ -	9.4×10^{13}/ -	13	n
1903	700/15	6,400/59,000	$2.0/1.8 \times 10^{14}$	5	n
1904	700/15	400/9,000	$2.2/1.7 \times 10^{14}$	70	p
1906	700/15	190/ -	3.7×10^{14}/ -	91	p
1907 *	700/15	6,300/34,000	$3.4/2.8 \times 10^{15}$	0.3	n

*A graphite lid was placed over the BN crucible.

and carrier densities were in the range of $3x10^{14}cm^{-3}$. In growth series #1900 (see Table 3.1.2) the first layer, grown from a fresh melt without bakeout, was n-type with a carrier density of $6x10^{14}cm^{-3}$. The following two growths, with a bakeout temperature of 700°C and 15 hours of bakeout before each growth, yielded n-type layers with lower carrier densities ($9x10^{13}$ and $2x10^{14}cm^{-3}$). However, when the accumulated bakeout period exceeded 30 hours at 700°C, the grown layers were p-type and had carrier densities in the range of $2x10^{14}cm^{-3}$. When the same melt was later baked out at 700°C for 15 hours and a graphite lid placed on the BN growth cell, the grown layer (#1907) was n-type and had a carrier density of $3.4x10^{15}cm^{-3}$. This is a significant result which indicates that carbon is an important ingredient for obtaining compensation in our systems.

In summary, series #1400, 1500 and 1900 were grown under the same growth conditions, but #1400 and 1500 gave n-type layers whereas #1900 gave p-type layers from stabilized melts. This may be due to (1) unknown impurities in the first two series of growths, which were carried out in a newly constructed system and/or (2) the system components were not stable during the early period of operation. The above results suggest that for bakeout temperatures in the range of 700 to 850°C, the dominant residual impurities from the reactions between the system components in the SiO_2-BN-H_2 system are p-type and the bakeout transition temperature appears to be lower than 700°C. The results, so far, obtained from studies of the three growth systems (SiO_2-C-H_2, SiO_2-BN(C)-H_2, and SiO_2-BN-H_2) show that the SiO_2-BN(C)-H_2 system must be used in order to obtain strong compensation between the residual donors and acceptors and that this system is more suitable for growing semi-insulating GaAs LPE layer from Cr-doped melts.

3.1.1.2 Anodic Oxidation of GaAs

The anodic oxidation of GaAs is being pursued to make differential Van der Pauw measurements on semi-insulating GaAs LPE layers. We found that with a concentrated (30%) H_2O_2 electrolyte and a few drops of H_3PO_4 added to adjust the pH value to ≈ 2,[2] we were able to grow relatively thick, uniform oxide layers on GaAs. The preliminary results show that a uniform oxide $\approx$ 0.8μm in thickness is grown on a GaAs sample by anodization in boiling H_2O_2-aqueous solution at a bias of 170 V. The oxide can be stripped by boiling in an HCl solution. The GaAs layer removed from the surface by this process is about 0.5μm. This technique will be used for lateral stripping in order to profile semi-insulating GaAs LPE layers.

3.1.2 LPE Activities at the Science Center

Over the last quarter, LPE activities at the Science Center have continued to fulfill the material requirements for the FET and substrate evaluation programs. Layers have been grown on Crystal Specialties substrates as well as a number of buffer layers supplied by Stanford University. The Stanford layers consisted of both undoped p^- and n^- layers as well as high resistivity Cr-doped layers. In as much as possible, parallel growths were performed in order to compare the effects of the Cr doped buffer vs. the semi-insulating substrate on the active layer and interface properties. Devices are being fabricated from this material.

Following the process developed at Cornell, we have attempted to grow several high purity undoped layers. Although we have achieved carrier densities in the low 10^{14} range, the mobility at 77K is at least a factor of 2 lower than we would expect from the Cornell data. Work is continuing and

several double layers, which have been grown for field effect transistor devices are presently being processed.

Mr. Yu-min Houng of Stanford University spent a week at the Science Center performing measurements on active layers grown on Stanford buffer material. Annealing experiments were also initiated during Mr. Houng's visit.

3.1.3 LPE Activities at Cornell University

Work has been done to further study and develop the properties of liquid phase epitaxial thin active channels and thicker pure buffer layers, as well as to test substrates from Crystal Specialties.

The purity of GaAs epitaxial buffer layers by LPE has been investigated further in an attempt to achieve doping concentrations in the low $10^{13} cm^{-3}$ repeatably. The incorporation of C or CO from the graphite boat into the melt is believed to be responsible for most of the background donor impurities. Earlier results yielded n-type layers with 160,000 $cm^2/v\text{-}s$ mobility at 77K, from melts baked 24 hours at 700°C. Layers grown at 665°C. from a melt that was baked at 665°C for various impurity purging times, exhibited relatively poor mobilities in comparison. Further examinations showed that O_2 adsorbed on the graphite during the loading process later forms a thin oxide skin on the melt during the bakeout period and this skin does not disappear unless the temperature is above 700°C. The porous nature of the graphite boat definitely facilitates the C or CO incorporation. A new boat, to be made of densified graphite, has been designed and has been ordered. The reduction of the pores will consequently tend to reduce the O_2 adsorption; thus, higher purity may be expected. The wafer area also has been increased

to 3 cm^2 from 1 cm^2, so that a uniform active layer thickness can be obtained over a larger area.

In an attempt to eliminate the graphite entirely, a Spectrosil (highest purity quartz) sliding boat has also been machined. The square depression in the slider, and the square bottom portion of the wells in the boat have been cut with an ultrasonic tool. The groove on the boat for the slider was made with repeated cuts with a diamond saw. The quartz surfaces that are in contact with the Ga have been roughened with abrasive to prevent the Ga from wetting and thus leaking through the cracks. This boat has been subjected to a thorough chemical cleaning procedure and it is ready for the first melt. The undoped layers are expected to be lightly-doped p-type (from a small, equilibrium amount of Si contamination) with a net acceptor level of approximately $2x10^{13}cm^{-3}$. When n-type layers are desired, a small amount of tin will be added to the melt. A mobility of over 200,000 cm^2/v-sec at 77K, with an associated total impurity concentration of $6x10^{13}cm^{-3}$ can be ultimately expected if this method succeeds.

Tests made on Crystal Specialties substrates show a remarkable improvement in surface conversion resistance after baking. The earliest material tested yielded less than 1,000Ω resistance between electrodes evaporated on chromium-doped GaAs surfaces after baking at 700°C for 7 hrs. The most recent material tested yielded over 30 Megohms after baking at 700° for 10 hrs. The high purity of undoped layers (low $10^{15}cm^3$ net donors and over 7000 cm^2/v-s mobility at 300K) grown at Crystal Specialties and also used by us for source crystals for liquid phase epitaxy, has allowed them to achieve high resistivity with low concentration of added ($3-4x10^{15}cm^3$) chromium atoms. This may be related to the improvements in the surface conversion problem.

FET devices were processed and tests made from one of the LPE wafers with about $8x10^{16}cm^3$ in the active layer and with 10,000Ω sheet resistance in the (5μm) buffer layer, at Bell Laboratories. With .8μm gate length and 500μm gate width, transconductance values about 60 millimhos were measured, which equalled the highest value obtained at that laboratory with their own material. At 6 GHz, a value of 2.3 dB noise figure with 9 dB of associated gain was obtained. No looping was detected in the I-V curves when the devices were tested in the dark. The substrate was obtained from Laser Diode Corporation. It is expected that significant improvement can be expected in this performance with the better substrates now available from Crystal Specialties, and with significantly higher sheet resistance in the buffer layers.

3.2 Semi-Insulating Substrate Material

3.2.1 Material Growth at Crystal Specialties

In the previous report[1] the possibility of carbon in the form of CO or CO_2 causing lineage was discussed. It is felt that this gas acts as an impurity which is soluble in the molten GaAs and can cause growth problems if it exceeds the solubility limit. CO or CO_2 was formed when residual O_2 reacted with the carbon cloth used to line the quartz boats. Although carbon cloth was not used when Cr-doped material was grown, carbon could be coming from backstreaming of the turbo-molecular pump. It was further conjectured that if CO or CO_2 were causing lineage then any gas other than As could well be causing growth problems, manifested by high dislocation densities and lineage.

A new all stainless steel vacuum manifold with a liquid nitrogen trap was constructed. The use of all backfill gases such as helium or nitrigen were also eliminated. The results were that lineage was reduced to almost zero. Etch pit densities have also been significantly reduced in much of the material.

Unfortunately, the production of Cr doped material is still somewhat erratic. The problem which still exists is caused by wetting or keying of the growing crystal to the quartz boat material. If a wetting condition exists, the growing crystal is stressed by the difference in contraction of the quartz and the cooling GaAs boule. Stress causes high dislocation densities and twinning in the crystal.

All of the factors causing boat wetting are not understood. It is known however, that water from inadequate pumpdown or OH from etch residues causes wetting. Quartz with high OH content is also known to cause boat wetting. Quartz which has been produced with a hydrogen-oxygen flame can not be used to produce GaAs by the boat process. It is probable that one of the most important and uncontrollable factors is reproducibility of quartz quality. At this time Crystal Specialties has no way of monitoring the incoming quartz for OH content.

Effort is being made to reduce the wetting problem by the addition of resistance bakeout furnaces. At the present, bakeout is accomplished with an oxygen-hydrogen torch, which is not a repeatable procedure. Attempts will be made to work in cooperation with a quartz supplier in an attempt to produce or select quartz with low OH content.

3.2.2 Semi-Insulating Material Evaluation at the Science Center

A compilation of all the information available on the Crystal Specialties substrates utilized under this contract has been made. The information, stored on a computer file, is indexed by boule number and type of experiment, for example, bulk growth, bulk measurements, implantation, buffer layers, devices, etc. Table 3.2.1 constitutes a quick reference index for this filing system. The X's on this table indicate what information is available on what boule. A description of the abbreviations used in Table 3.2.1 is contained in Table 3.2.2. This information will be periodically updated, and a printout of the table and all the stored information will be periodically distributed among the participants of the program. For the sake of simplicity, the information stored is very concise. If details are needed, they can be obtained directly from the person who performed the experiment.

In our recent semi-annual report[1], transport measurements on semi-insulating GaAs with low and high-Cr concentration were presented and analyzed in terms of models for the electrical compensation. The data from the low-Cr material did not support the "conventional model" with deep Cr acceptors compensating residual shallow donors. It was shown that a deep donor level had to be incorporated into the model, leading to a deep-donor-deep-acceptor model. With such model it was possible to interpret the experimental data. The deep donor level was assigned to oxygen.

Our analysis of the high-Cr data[1] indicated that in this case both electrons and holes had nonnegligible contributions to the electrical conductivity. The results of a nonlinear least square fit were $E_C - E_A = 0.84$ eV and $N_A/N_D = 1.06$ where $E_C - E_A$ was the depth of the acceptor level measured from the conduction band, N_A was the acceptor density, and N_D was the donor

Table 3.2.1

EXPERIMENTS ON SUBSTRATES

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BOULE	GRO	IMJ	TRA	HTR H2	HTR CAP	IMP S	IMP LSR	IMP HSR	IMP TE	EPI SC	EPI COR	BUF COR	BUF ST	PET EPI	PET IMP	PET IS	MIS	OTH
1715	X												X					
1718	X	X	X	X						X		X		X			X	X
1903	X				X	X	X	X	X	X						X		
2000	X	X	X	X	X	X	X			X		X		X			X	X
2004	X			X	X	X	X			X	X	X	X	X	X			
2109	X			X	X	X	X	X	X	X				X				
2132	X			X	X		X			X				X			X	
2299	X			X	X		X								X			
2312	X			X	X	X	X	X		X								
2440	X				X		X	X			X	X	X		X		X	X

Table 3.2.2

KEY TO ENTRIES

1	GRO	GROWTH DATA
2	INJ	INJECTION MEASUREMENTS
3	TRA	TRANSPORT MEASUREMENTS
4	HTR H2	HEAT TREATMENT HYDROGEN ATMOSPHERE
5	HTR CAP	HEAT TREATMENT CAPPED
6	IMP S	SULPHUR IMPLANTS
7	IMP LSE	LOW-DOSE SELENIUM IMPLANTS
8	IMP HSE	HIGH-DOSE SELENIUM IMPLANTS
9	IMP TE	TELLURIUM IMPLANTS
10	EPI SC	N-TYPE EPITAXIAL GROWTH SCIENCE CENTER
11	EPI COR	N-TYPE EPITAXIAL GROWTH CORNELL
12	BUF COR	BUFFER LAYERS CORNELL
13	BUF ST	BUFFER LAYERS STANFORD
14	FET EPI	FET ON EPITAXIAL LAYERS
15	FET ISE	FET ON SELENIUM IMPLANTED LAYERS
16	FET IS	FET ON SULPHUR IMPLANTED LAYERS
17	MIS	MISCELLANEOUS
18	OTH	OTHER LABORATORIES

density. However, the equation to which the data were fitted (Eq. 14 in Ref.1) was based on the assumption that the donors were all ionized. This assumption becomes questionable when N_A/N_D is nearly one and the donor and acceptor levels are not far apart from each other. Therefore, a more complete analysis of high-Cr data was necessary.

Starting from the condition of charge neutrality for semi-insulating GaAs which takes the simple form

$$N_A^- = N_D^+ \quad , \tag{1}$$

because the free carrier concentrations n and p are negligibly small, and substituting the Fermi functions leads to

$$\frac{N_A}{1 + \exp[(E_A - E_F)/kT]} = \frac{N_D}{1 + \exp[(E_F - E_D)/kT]} \quad , \tag{2}$$

where E_A and E_D are the energies of the acceptor level and donor level respectively, k is Bolzman's constant and T is the temperature. Eq. (2) can be solved for the Fermi energy E_F, which can then be substituted in Eq. (13) of Ref. 1 leading to a general expression for the electrical resistivity. With this purpose, the new variables

$$E_o \equiv (E_D + E_A)/2 \tag{3}$$

$$G \equiv \exp[(E_o - E_F)/kT] \tag{4}$$

are introduced. Substituting E_o and G, Eq. (2) becomes a quadratic equation

for G which can be solved:

$$G = (1/2)\left\{ - (1-N_A/N_D)\exp\left[(E_D - E_A)/2kT\right] + \right.$$

$$\left. + \left[(1 - N_A/N_D)^2 \exp\left[(E_D - E_A)/kT\right] + 4(N_A/N_D)\right]^{1/2} \right\} . \qquad (5)$$

Combining Eq. (13) of Ref. 1 and Eqs. (3) - (5), the electrical conductivity ρ^{-1} becomes

$$\rho^{-1} = (q\mu_e N_c/G)\exp\left[-(E_c - E_o)/kT\right] + q\mu_h N_v G \exp\left[-(E_o - E_v)/kT\right] . \quad (6)$$

Eqs. (5) and (6) express the electrical resistivity as a function of temperature, and of the density and energy of donors and acceptors. Notice that the donor and acceptor densities N_D and N_A appear only in ratios N_D/N_A. This originates from the form of Eq. (2), and it is a direct consequence of n and p being negligible in the condition of charge neutrality set by Eq. (1). Eq. (14) in Ref. 1 can be derived from Eqs. (5) and (6) when $N_A \gg N_D$.

The result of a nonlinear least square fit of the high-Cr data in Fig. 3.2-2 of Ref. 1 is shown with a solid line in Fig. 3.2-1. The two straight broken lines represent the separate contributions of electrons and holes to the resistivity. The least square fit was done after replacing the numerical values of the constants[3] and the values of the mobilities (Table 3.2-5, Ref. 1) in Eqs. (5) and (6). N_A/N_D and $E_c - E_A$ were the adjustable parameters. $E_c - E_D$ was treated as a fixed parameter. The excellent fit shown in Fig. 3.2-1 was obtained with $E_c - E_D = 0.006$ eV, $N_A/N_D = 1.04$ and $E_c - E_A = 0.83$ eV.

Fig. 3.2-2 shows how the results of the least square fit depend on

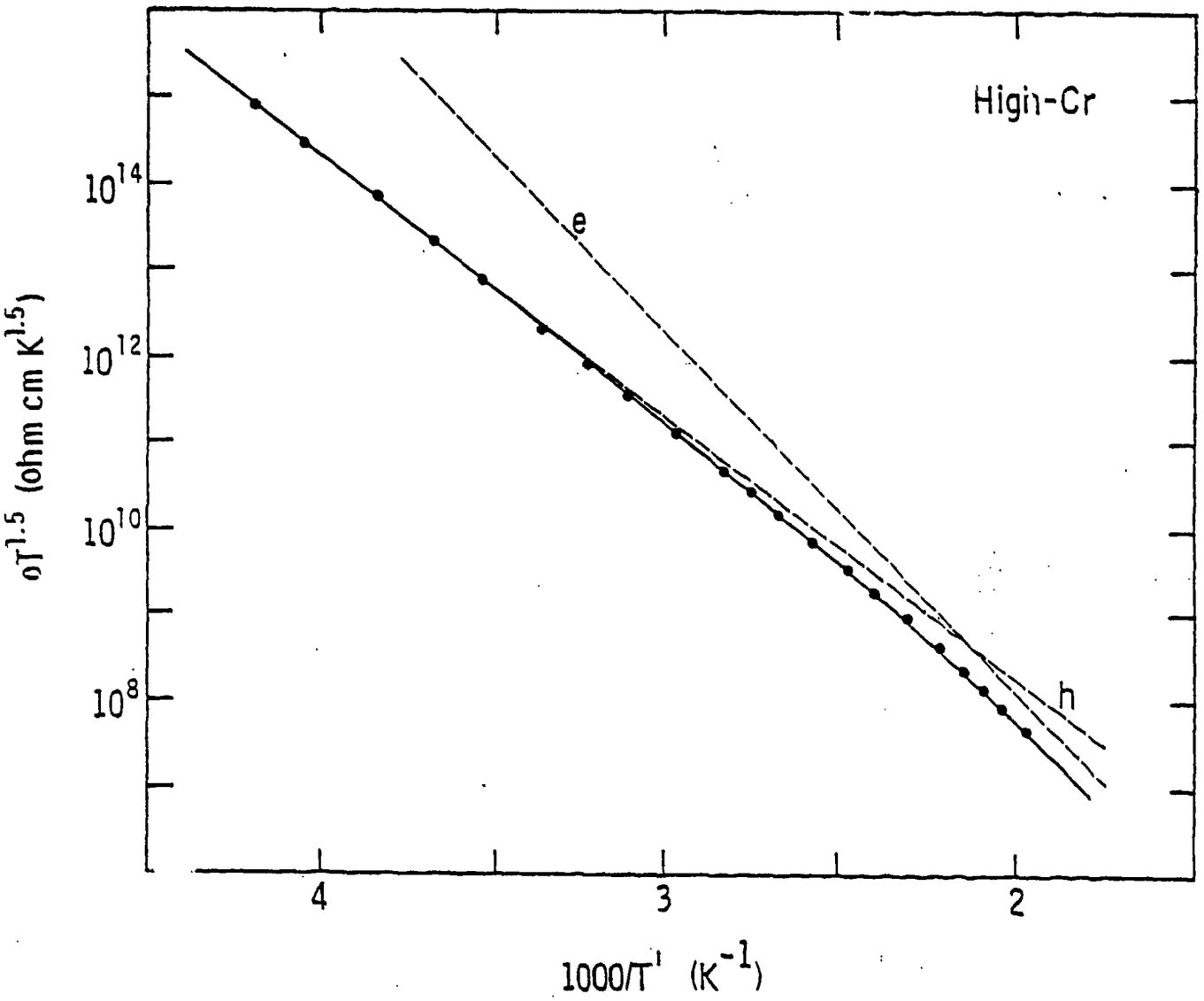

Fig. 3.2-1 Result of a nonlinear least square fit of the high-Cr data of Fig. 3.2-2, Ref. 1, for $E_C - E_D = 0.006$ eV.
Fitting parameters: $N_A/N_D = 1.04$; $E_C - E_A = 0.83$ eV.
The dots represent the experimental points. The dashed straight lines represent the separate contributions of electrons and holes.

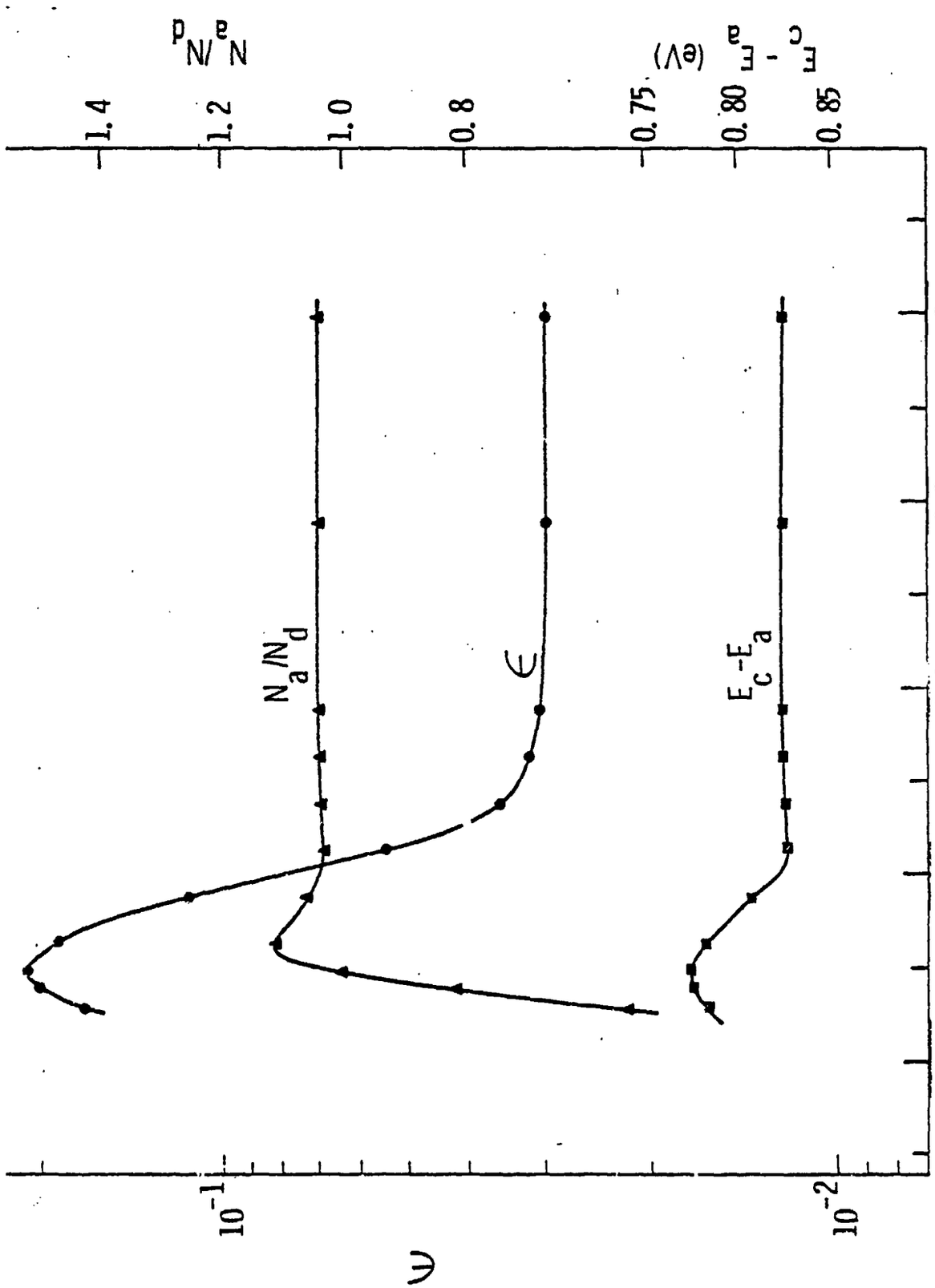

Fig. 3.2-2 Plot of the mean square ϵ and the fitting parameters N_A/N_D and $E_c - E_A$ in the nonlinear least square fit of the high-Cr data against the parameter $E_c - E_D$.

the value assigned to $E_c - E_D$. In this figure, the mean square deviation ε is plotted against $E_c - E_D$ along with the resulting values of N_A/N_D and $E_c - E_A$. The curve for ε shows that a good fit cannot be obtained with the donor level where it was in the low-Cr case ($E_c - E_D = 0.72$ eV). The donor level must instead be placed closer to the conduction band at a distance between 0 and 0.2 eV. In this range the values of N_A/N_D and $E_c - E_A$ are practically independent of $E_c - E_D$. Although the best fit is obtained for $E_c - E_D = 0$, there is some indetermination in the value of $E_c - E_D$ because the curve for ε in Fig. 3.2-2 has almost zero slope near zero. The value $E_c - E_D = 0.006$ eV, equal to the depth of shallow donors in GaAs was chosen[4] because no other donor level in the range between 0 and 0.2 eV from the conduction band where the curves are almost flat was known to us. The least square fit analysis was done with the constraint that the donor level was above the acceptor level ($E_c - E_D \leq E_c - E_A$). Another good fit could be obtained with the opposite constraint, but it would lead to the unrealistic results $E_c - E_D = 0.90$ eV, $N_A/N_D = 120$ and $E_c - E_A = 0.72$ eV.

The results of the least square fit analysis could not be significantly altered by modifying some of the fixed parameters used in the calculation even far beyond their error margins. By manipulating the values of the electron and hole mobility within reasonable limits, it was not possible to revert either the conclusion that $N_A/N_D > 1$ or the conclusion that the donors were shallow. The final results $N_A/N_D = 1.04$ and $E_c - E_A = 0.83$ eV are very close to those reported earlier.[1] The reason is that when the donors are shallow, $E_D - E_A \gg kT$ and Eq. (14) of Ref. 1 becomes a good approximation to Eqs. (5) and (6).

The results of the least square fit discussed above show that in the high-Cr case the ρ vs. T data are well described by a deep acceptor level

compensating shallow donors. This situation is different from the low-Cr case in which deep donors are the main compensating impurities. We conclude that there is a large difference in the relative density of deep and shallow donors between the low- and high-Cr material. It is not clear at this point how such difference relates to the conditions under which the crystals were grown. A direct correspondence between the difference in donor populations and the concentrations of O and Si impurities in the mass spectrographic data of Table 3.2-4 in Ref. 1 is not found. Lack of a direct correspondence may be due to the existence of impurity complexes that may lower the density of electrically active impurities, or to the presence of precipitates in which considerable portions of some impurities may be segregated.

Studies of the effects of heat treatment on semi-insulating GaAs have been continued. We have observed that annealing semi-insulating samples in a H_2 atmosphere simulating the type of heat treatment that occurs in epitaxial growth tends to form p-type surface layers while capping the same materials with Si_3N_4 and annealing simulating the conditions of post-implantation anneal, tend to form n-type surface layers. In order to study this different behavior, photoluminescence spectra at 77K from both types of samples were measured. In both cases the spectra have a strong gap recombination peak at 1.508 eV and a broad emission peak below the gap. However, the position of this peak is different for the two types of samples. For the samples heat treated in H_2 atmosphere, the peak is centered at 1.39 eV while for the capped and annealed sample the peak is centered at 1.36 eV. This difference indicates that different complexes are formed in each case. Unfortunately, the information on impurity levels supplied by photoluminescence spectra may be incomplete because there are nonradiative transitions in semi-insulating GaAs. Transient capacit-

ance measurements which have the advantage of detecting levels regardless of whether the transitions are radiative or not will be made in order to supplement the information from photoluminescence spectra.

3.3 Ion Implantation

Low dose Se implantations have been carried out using samples from 8 different boules of semi-insulating GaAs obtained from Crystal Specialties, Inc. in an effort to evaluate the effect of substrate differences on low dose implantation results. Unimplanted samples and krypton bombarded samples from these same boules were coated with sputtered silicon nitride at the same time as the Se implanted samples. The krypton bombardment was carried out at the same energy and dose as the Se implantation in order to simulate the damage produced during the Se implantation. All samples were annealed at 850°C for 30 min. Unimplanted and krypton bombarded samples from three boules showed conducting layers with sheet resistances in the range from about 500 - 2000 ohm^2 following annealing. Sheet resistance and sheet electron concentration data for these samples are shown in Table 3.3.1. The krypton bombarded samples appear to exhibit slightly larger changes than do the samples which were not bombarded. The material in boule 2132 which showed the greatest change, contained a deliberately high chromium content ($> 10^{17}$cm^3). The unimplanted and krypton bombarded samples from the other 5 boules remained semi-insulating following annealing. The sheet resistance for a typical insulating sample is also shown in the Table.

Electron concentration vs. depth profiles were measured with an automatic C-V profiler for all the Se implanted samples. Typical results are shown in Fig. 3.3-1. Substrate 2132, which had the very high chromium

Table 3.3.1

Cr-DOPED GaAs SAMPLES ANNEALED AT 850°C FOR 30 MIN

	Unimplanted		1.8×10^{12}-400 keV Kr ions/cm^2	
	ρ_s(Ω/□)	N_s(cm^{-2})	ρ_s(Ω/□)	N_s(cm^{-2})
2132	~ 1500		482	4.2×10^{12}
2299	2250	5×10^{11}	~ 1500	
2312			1220	1×10^{12}
Typical Good Material			~ 6×10^{8}	

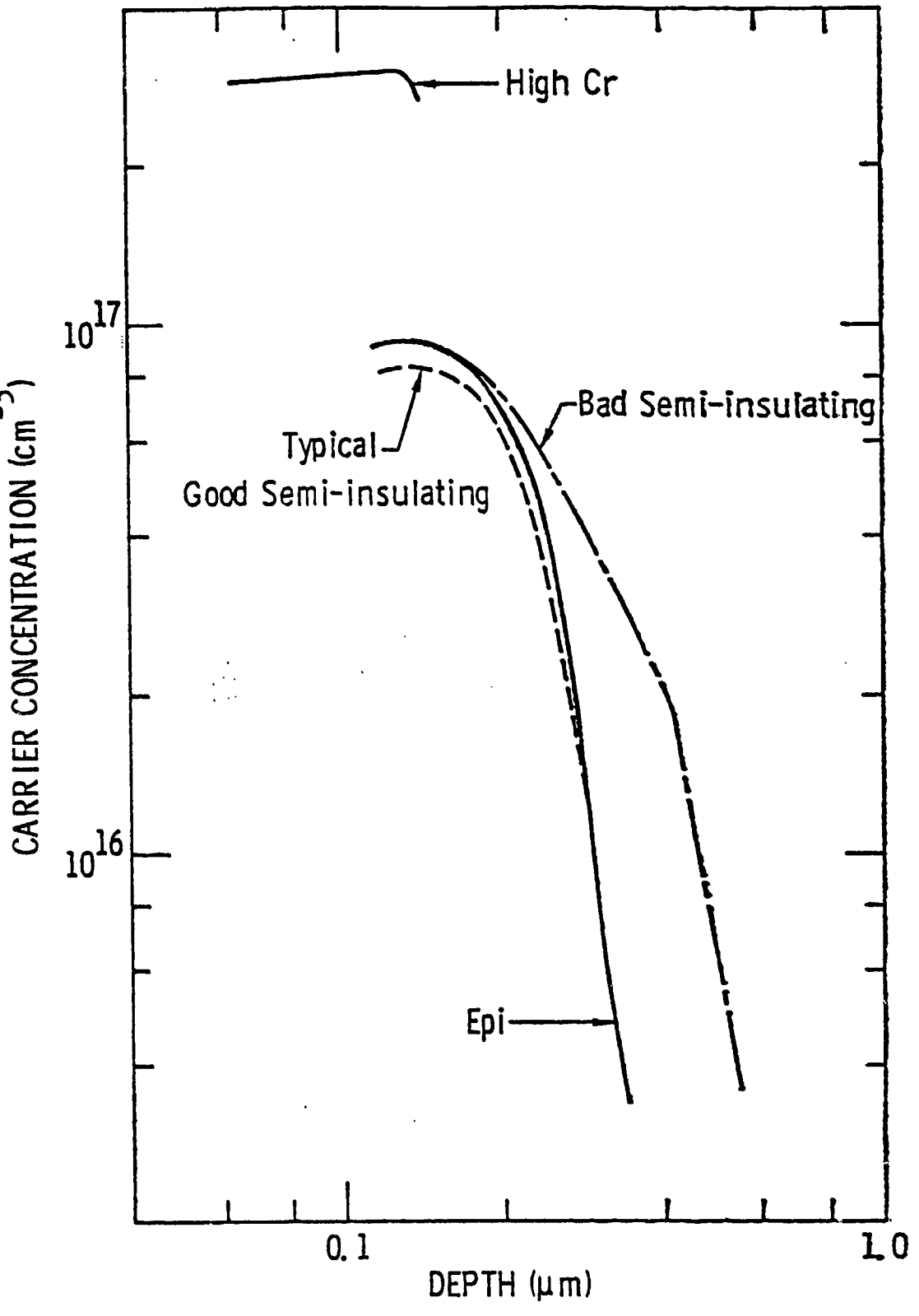

Fig. 3.3-1 Electron concentration profile of Se implanted semi-insulating substrate.

content, exhibited a much higher electron concentration than any of the other Se implanted samples. A typical profile obtained from an implant into good semi-insulating material is shown in the figure. The profile obtained from a similar Se implant into low electron concentration epitaxial material is also shown. These two profiles are quite close to each other. The effect of implanting into material from boules 2299 or 2312 is indicated by the profile labeled "bad semi-insulating." It can be seen that the principal effect is a considerably deeper tail than is observed for the good semi-insulating or epitaxial substrates. The reproducibility of the profiles obtained by implantation into semi-insulating material from the 5 good boules, was about ± 10% in both maximum doping level and doping depth.

A capless annealing technique, which was described in a recent publication submitted for approval, has been used to anneal high dose Se implantations into semi-insulating GaAs. Annealing has been carried out mainly at 850°C but some samples have been annealed at 900°C. Comparison of samples implanted with the same high dose of Se and annealed for the same time and temperature indicates that about the same maximum electron concentration can be achieved by the capless annealing technique as can be obtained by annealing with an aluminum oxy-nitride cap. The peak of the electron concentration profile tends to be somewhat deeper when the capless technique is used as compared to the result using aluminum oxy-nitride. Sheet resistances obtained using the capless technique are slightly higher than those obtained using aluminum oxy-nitride. The results of these measurements will be reported in detail in the next semi-annual report.

Preliminary experiments have been carried out to determine the lattice location of sulfur implanted into GaAs. Proton induced X-rays have

have been used to detect the interaction of a channeled proton beam with the implanted S atoms. With an implant dose of $1x10^{15}$ 100 keV S ions/cm^2, the S K X-ray peak height is comparable to the height of the broad X-ray background observed when GaAs is bombarded with protons. Preliminary channeling data indicate that S is largely substitutional following implantation at 350°C. Further work is required in order to make a quantitative estimate of the amount of substitutional sulfur.

Work on the reordering of amorphous layers on GaAs has been continued. Recent transmission electron microscopy and glancing angle X-ray diffraction measurements indicate that the reordering of the amorphous layer is epitaxial upon the underlying GaAs but that the reordered layer contains substructure. The nature of the substructure is not clear at present but it may consist of antiphase domains. Further work will be required to clearly illucidate the nature of this substructure in reordered layer. Backscattering is produced by the substructure. This suggests that it is necessary to re-evaluate the use of backscattering as a tool in studying the reordering of layers which are found to contain substructure. The influence of this substructure on the doping resulting from implantation, in which an amorphous layer is produced, is not clear at present. A paper describing the details of the present work is in preparation and the results will be included in the next semi-annual report.

3.4 Investigation of the Effect of Material on Device Performance

3.4.1 FET Devices

The GaAs FET with 1μm gate length is being used as a test vehicle in

the contract program to measure the effects of substrates and the effectiveness of high resistance layers used to buffer substrates. At present we are fabricating and measuring:

(a) FETs from single epitaxial layers on semi-insulating substrates,

(b) FETs from buffered two layer epitaxial combinations which consist of a layer of high resistance epitaxy between the active thin layer and the semi-insulating substrate,

(c) FETs from implanted layers on semi-insulating substrate, and

(d) FETs from implanted layers in high resistance epitaxial layers (buffer layers).

Results of comparative measurements of FET performance will be available in the next report.

3.4.2 GaAs Ionization Coefficients, Cornell University

In the last quarterly report, several measurements of electron ionization rates in different doping ranges of GaAs were given. Since only electron ionization rates were analyzed, the results given were subject to possible systematic error in the doping range where the hole ionization coefficient was greater than that of electrons.

In order to understand the unusual effect of doping density on the apparent ionization coefficient and to substantiate the interpretation of this effect as being due to interband scattering, it is necessary to obtain as accurate data as possible. This report describes what we believe to be our most accurate measurements of both hole and electron ionization coefficients made in the same junction on epitaxial material of $9.5 \times 10^{15} cm^3$ donor density.

Most of the GaAs epilayers available at hand are not suitable for

making accurate multiplication measurements. The difficulties range from non-uniform doping to high trap densities. In the latter case, large hysteresis loops were found between the up-trace and down-trace of the multiplication measurements. Also, the measurements were very sensitive to excitation of deep levels by ambient room illumination. Data taken from those samples were not consistent.

We have, however, obtained one piece of material which is free from the complications mentioned above. The material was grown by VPE technique at Raytheon. The doping of the active layer was found to be $9.5 \times 10^{15} cm^{-3}$. Platinum Schottky barriers were sputtered on and the material was sintered at 300°C for 45 min. A flat bottomed well was anodically etched out from the substrate side, such that the thickness of the diode substrate was about 1 mil. In this structure, pure holes and pure electrons can be injected into the same diode. Electron injection was obtained by illuminating the top of the opaque platinum contact. Hole injection was obtained by strong illumination of the substrate side with non-penetrating radiation and diffusion of the generated holes to the high field region. Different frequencies of the light source were used to insure pure electron or hole injection. Measurements were made on several diodes and they were consistent. The multiplication data are shown in Fig. 3.4-1.

The values of α and β were calculated from the data in Fig. 3.4-1 and the following relationships of α, β, M_n and M_p:

$$\alpha(E_m) = E_m \left[\frac{d(\ell n M_n)}{dV} - \frac{M_n - 1}{M_n} \frac{d(\ell n M_p)}{dV} \right] \tag{7}$$

$$\beta(E_m) = \frac{E_m}{M_n} \frac{d(\ell n M_p)}{dV} \tag{8}$$

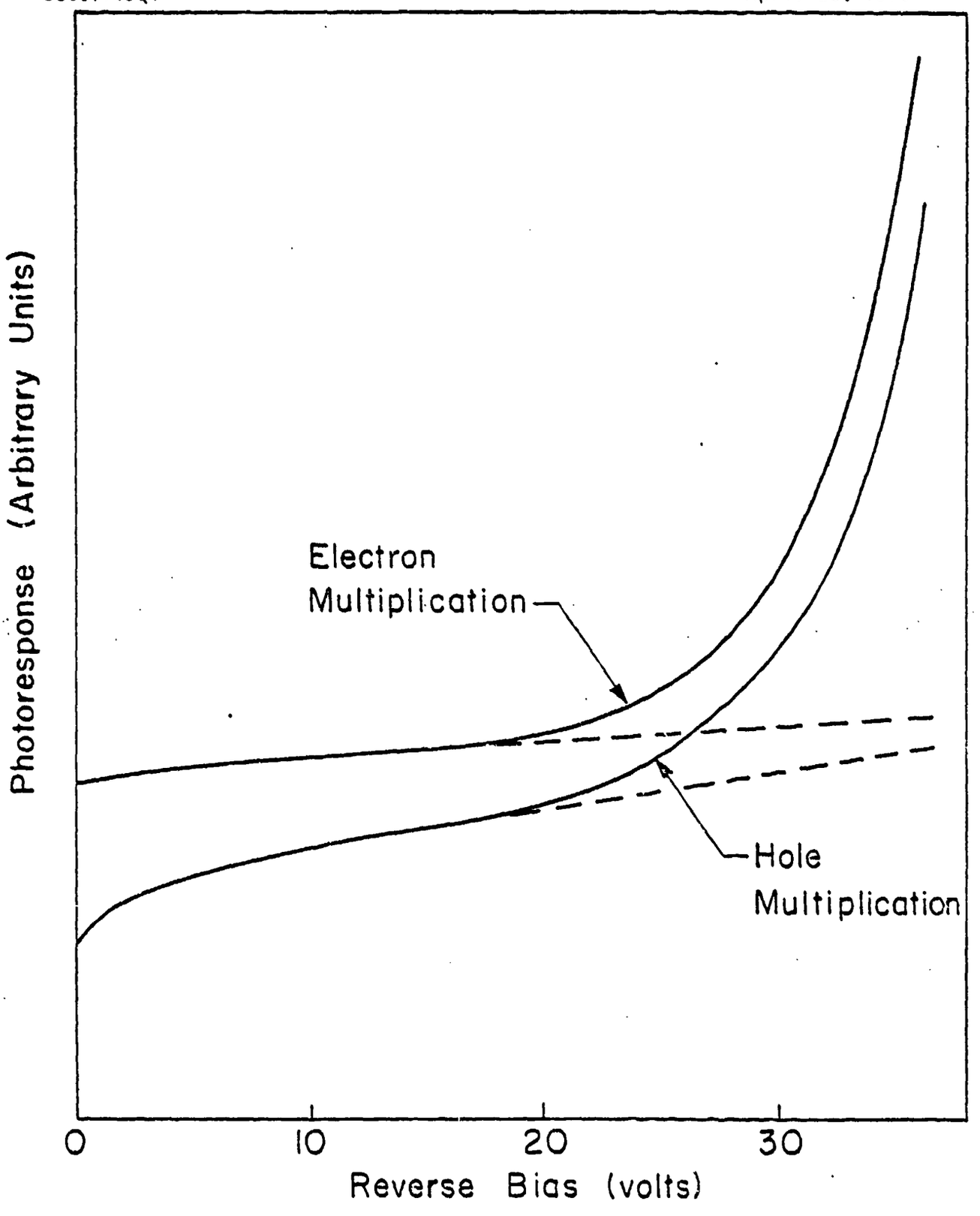

Fig. 3.4-1 Multiplication curves initiated by holes and electrons on n-type GaAs with $N_d = 9.5 \times 10^{15} cm^{-3}$.

where E_m = peak field

M_n = multiplication of electron

M_p = multiplication of hole.

The calculated results together with Stillman's results[5] and previous measurements[1] of electron ionization rate are shown in Fig. 3.4-2. Stillman's data were taken on a sample with doping $N_d = 1 - 2 \times 10^{16} cm^{-3}$ and it is obvious from these data that β is greater than α. The values of α and β for our data are almost the same.

This new data are consistent with the observed crossover of electron and hole ionization rates. There is no doubt from our previous measurements that hole ionization dominates for donor densities substantially greater than $10^{16} cm^3$ and that electron ionization dominates at densities of a few times $10^{15} cm^3$. The quantitative measurements for $N_d = 9.5 \times 10^{15} cm^3$ are consistent with the data of Stillman et al.[5] According to our present interpretation, the hole ionization coefficient should remain substantially the same for a wide range of doping density, but the effective electron coefficient should decrease substantially at higher doping.

4.0 FUTURE PLANS

4.1.1 LPE Activities at Stanford University - High Resistivity LPE GaAs

A. Further studies on the control of the growth conditions in the SiO_2-BN(C)-H_2 system at the transition temperature will be carried out in order to demonstrate the growth reproducibility of semi-insulating GaAs LPE layers.

B. Additicnal growths will be carried out below the 700° C bakeout temperatures to determine the transition temperature in our SiO_2-BN-H_2 system.

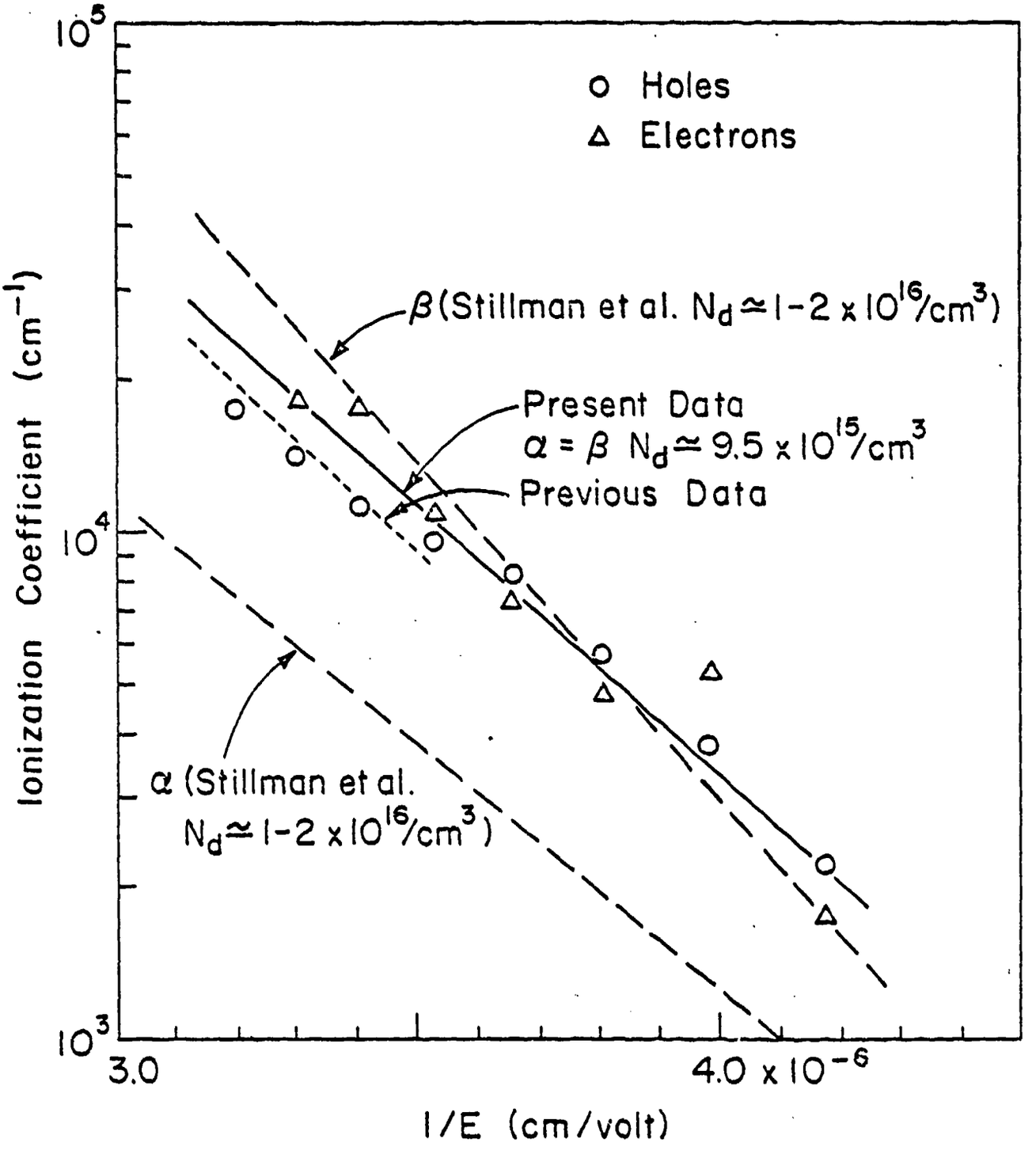

Fig. 3.4-2 Ionization coefficients of GaAs calculated from data in Fig. 3.4-1. Compare with Stillman's[5] data and previous measurement of α.

C. Studies on the carrier density profiles and the effects of the substrate on semi-insulating GaAs layers will be made by oxide stripping and differential Van der Pauw measurements.

D. Studies on the interface properties between the active epitaxial layer (grown at the Science Center) and the high resistivity buffer layer will be carried out.

4.1.2 LPE Activities at the Science Center

The growth of active FET layers on both Crystal Specialties substrate and Stanford buffer material will be performed as needed on a routine basis. We will also continue to investigate double layer buffer growths for FETs.

4.1.3 LPE Activities at Cornell University

In the next period, the buffer layers grown in the Spectrosil boat will be characterized. Some of these layers will be sent to the Science Center for ion implantation. Some buffered FET layers grown in the Spectrosil boat and the dense graphite boat will also be sent to the Science Center for FET processing.

4.2 Semi-Insulating Substrate Material

4.2.1 Material Growth

Semi-insulating material will be supplied as needed for epitaxial growth and ion implantation. Statistical data will be accumulated in order to quantify the reproducibility of bulk growth of semi-insulating material. Attempts to reduce the wetting problem by improvement of the bakeout procedure for quartz

will be made.

4.2.2 Material Evaluation at the Science Center

The measurement of transport properties will be continued in order to build some statistical information on a variety of samples. Study of effects of heat treatment will be continued using photoluminescence techniques. In addition, transient capacitance measurements will be attempted in order to complement the information on deep levels in the heat treated material. Transient capacitance measurements will also be made on n-type layers formed by implantation in different substrates and buffer layers in order to determine and compare the energy and density of deep levels.

4.3 Future Plans - Ion Implantation

Substrate qualification tests of the type described in Section 3.3 will be carried out on material from other boules of semi-insulating GaAs as they become available from Crystal Specialties in order to gather information on the amount of material produced which seems to be suitable for implantation. Sulfur lattice location experiments will be continued and measurements will be performed on annealed samples following either room temperature or elevated temperature implant. Further TEM studies of reordered amorphous layers will be carried out.

4.4 Investigation of Material Parameters on Device Performance

4.4.1 FET Devices

Fabrication of FET devices on epitaxial layers with and without buffer

layers and on layers made by implantation in substrates and buffer layers will be continued. Comparative measurements of FET performance will be made.

4.4.2 GaAs Ionization Coefficients, Cornell University

Attempts will be made to extend the electron-hole ionization coefficient measurements to other doping densities. The principal limitation in this regard is obtaining epitaxial material of good quality. Work will continue on trying to understand and quantitatively describe the systematic errors caused by deep levels.

5.0 REFERENCES

1. F. H. Eisen, J. A. Higgins, A. A. Immorlica, Jr., R. L. Kuvas, B. W. Ludington, B. M. Welch, C. P. Wen, and R. Zucca, "Investigation of Technological Problems in GaAs," Semi-annual Technical Report No. 1, AFCRL-TR-75-0435, Jan. 22, 1976, Contract No. F19628-75-C-0113.
2. S. M. Spitzer, B. Schwartz, and G. D. Weigle, J. Electrochem. Soc. 122, 398 (1975).
3. D. D. Sell and H. C. Casey, Jr., J. Appl. Phys. 45, 800 (1974).
4. C. J. Summers, R. Dingle, and E. J. Hill, Phys. Rev. B1, 1603 (1970).
5. G. E. Stillman, C. M. Wolfe, J. A. Rossi and A. G. Foyt, Appl. Phys. Lett. 24, 471 (1974).