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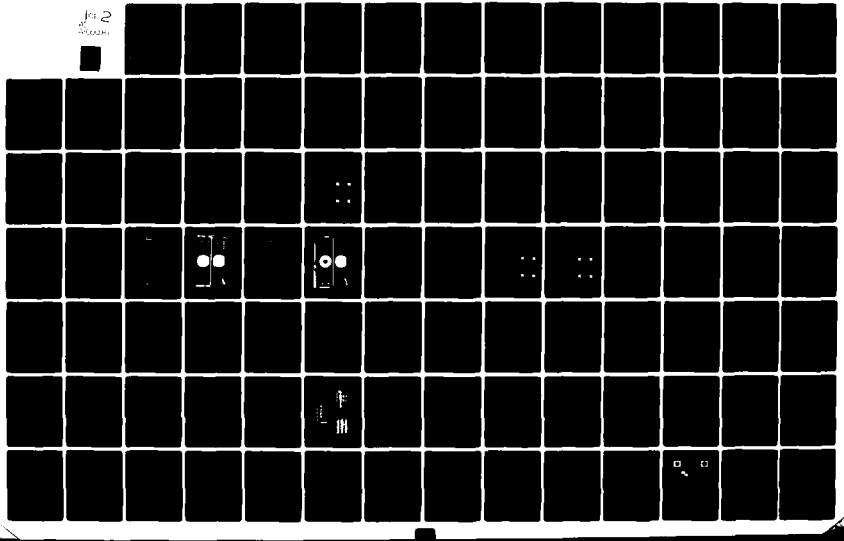

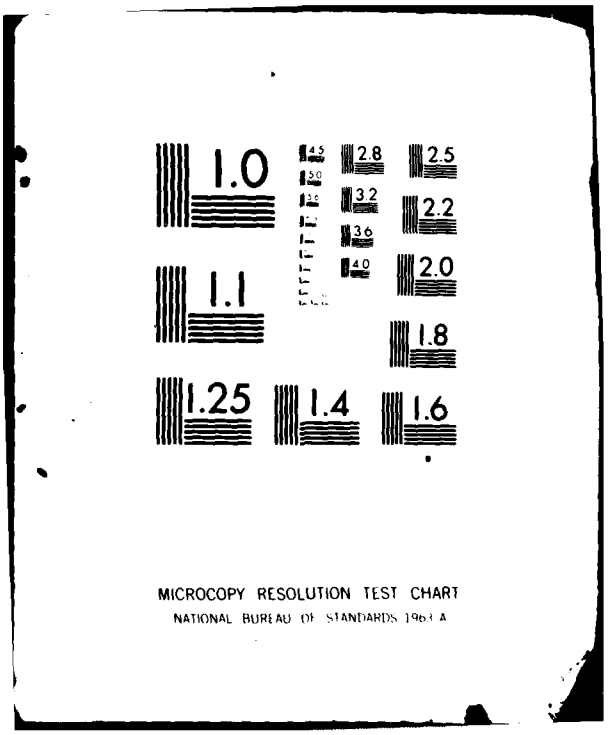
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DNA 5747F-2

FIBER OPTIC CODEC LINK (FOCOL)

Volume 2—Manual

Walter Naumann
Elizabeth Liles
R. Douglas Hogg
Effects Technology, Incorporated
5383 Hollister Avenue
Santa Barbara, California 93111

26 January 1981

Final Report for Period 1 November 1978—26 January 1981

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Data Link	Digital Electronics
Fiber Optic	Field Test
Data Transmission	Underground Test
Coder-Decoder	High Explosive Test
Codec	Nuclear Weapon Effects Test

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The fiber optic codec link was designed to meet the majority of data transmission requirements for both Underground Nuclear Weapon Effects Tests and High Explosive Tests at a substantial cost saving over current transmission methods including other multiplexing systems. The link is capable of transmitting a maximum of 92 channels of data over a fiber optic cable up to two kilometers in length. The bandwidth of the input data is switch selectable as 5kHz, 10kHz, or 20kHz. Fewer channels are available at higher bandwidths as lower bandwith channels are paralleled →

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to achieve higher bandwidth channels. Greater dynamic range is provided by the use of companding analog to digital converters which feature higher resolution for small signals.

Volume 1 of the final report includes the technical discussion of the link program.

Volume 2 of the final report is the manual for the link which provides a detailed description of the link and operating instructions.

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SECTION 1.0

SYSTEM DESCRIPTION

1.0 SYSTEM DESCRIPTION

1.1 INTRODUCTION

The ETI fiber optic data link is designed to transmit up to 92 channels of digitized analog data over a single optical fiber up to lengths of 1 kilometer or more. A complete list of system specifications can be found in Section 2.0. The data link is housed in two separate chassis, labeled transmitter and receiver. The functions performed by the transmitter are:

1) Digitizing of analog data

2) Multiplexing of data into a 12 Mbps Biphase-L bit stream

3) Modulating an LED or laser light source with the digital bit stream

4) Transmitting the light over a fiber optic cable.

The receiver performs the following tasks:

1) Detecting the modulated light beam and retrieving the 12 Mbps bit stream

2) Demultiplexing the bit stream into the original data channels

3) Converting the digital signals back to analog data.

Outputs are provided on the receiver which allow access to the digitized data. The data are provided on four output lines, each having a 3 Mbps NRZ-L serial bit stream. A 3 MHZ clock signal is simultane-

ously provided for external coding.

An optional computer interface card is described in Section 4.0.

1.2 SYSTEM COMPONENTS

In addition to power supply and line driver support circuits, the data link is composed of six basic components:

1) Coder
2) Multiplexer
3) Fiber Optic Transmitter
4) Fiber Optic Receiver
5) Demultiplexer
6) Decoder

Each of these components will be described below.

1.2.1 Coder. There are 24 coder boards which are sectioned into four groups in the transmitter chassis. These boards are interchangeable and are positioned in the 24 chassis slots labeled 1A through 4F. Each board houses the circuitry for the analog conversion of four channels. The input circuitry includes a voltage limiter for protection and a passive filter for removing aliasing signals. Refer to Section 1.5 for a discussion on input filtering. The analog to digital conversion is performed by a coder microcircuit (DF331) which has a companding transfer function that results in a 12 bit resolution at small signals with an eight bit word. The conversion process generates a 3 Mbps eight-bit serial data word which includes a sign bit. All digital data are gated onto one of four data lines by appropriate sync timing pulses. The maximum sampling rate for the codec chips is 16 KHz. This would limit the maximum system bandwidth to about 5 KHz, but higher bandwidths (up to 20 KHz) are achieved by paralleling codec chips. This

results in a reduction of total available channels. Refer to Section 3.4 for a detailed explanation of system bandwidth.

1.2.2 Multiplexer. There is one multiplexer board which accepts the four 3 Mbps serial bit streams from the 24 coder boards and further multiplexes them into one 12 Mbps serial bit stream. The bit stream (NRZ-L format) is then combined with a 12 MHz clock to produce a Manchester (Bi-phase L) encoded signal. The system clock is located on this board and generates all sync pulses which are used for that part of the multiplexing which is handled on the coder boards. Frame sync is accomplished by a period of omission of the 12 MHz clock in the Manchester encoded signal.

1.2.3 Fiber optic transmitter. The transmission of the encoded data is accomplished by modulating the current through a Spectronics light emitting diode (LED), using a Fibercom fiber optic emitter driver. Optionally two fiber optic transmitters can be located in the transmitter chassis which are operated in parallel; that is, both can transmit simultaneously. However, since the two receivers cannot be operated at the same time, the second transmitter and receiver are used as a backup. Refer to the data sheets in Section 6.0 for more detailed information on the transmitters. Other fiber optic transmitters can be installed depending upon laser requirements.

1.2.4 Fiber optic receiver. The fiber optic receiver consists of a silicon PIN photodiode, amplifier, and buffer output. The current output of the photodiode is converted into a voltage and amplified. The amplified voltage is then buffered to produce the 12 Mbps bit stream at TTL signal levels. Opitonally two fiber optic receivers can be located in the receiver chassis. However, they cannot be operated simultaneously and can be switch selectable. Refer to Section 6.0 for more details on the fiber optic receivers. Different fiber optic receivers can be installed for varied requirements.

1.2.5 Demultiplexer. The demultiplexer board is located in the receiver chassis and performs the function of decoding the Manchester encoded signal into NRZ-L formatted data and the 12 MHz clock. The clock is then used to demultiplex the 12 Mbps signal into four 3 Mbps data lines which are fed to appropriate decoder boards. In addition these four lines are brought out to the receiver back panel for external access. The absence of the 12 MHz clock during each frame is detected to provide a frame sync pulse which is used along with the clock to generate individual sync pulses used by the decoder boards.

1.2.6 Decoder. There are 24 decoder boards located in the receiver chassis and, like the coder boards, are sectioned into four groups. These boards are interchangeable and are positioned in the 24 chassis slots labeled 1A through 4F. Each group receives one of the 3 Mbps signal lines generated by the demultiplexer board. Each of the boards contains circuitry for four individual channels. The conversion from digital to analog data for each channel is performed by a codec chip (DF334) and occurs during the time determined by the sync pulse for that channel. The analog output is buffered through an operational amplifer. The minimum conversion time which must be allowed for the codec chips is 15 μsec which limits the maximum bandwidth of the system to 20 KHz (64 KHz sampling rate). Refer to Section 3.4 for more information on system bandwidth.

1.3 CHANNEL NOMENCLATURE

The analog channels are divided into four groups and numbered one through four. Since there are a maximum of 92 channels available, there are a maximum of 23 channels per group. Each group has six coder and decoder boards devoted to it and are labeled A through F in each group. Each circuit board contains four codec chips (DF331's for the coder boards and DF334's for the decoder boards). The codec chips on each board are labeled U1 through U4. Each channel is represented by the

three symbol code:

GROUP-BOARD-CHIP.

For example, channel 2B4 corresponds to group 2, board B and chip U4. The analog input and output BNC connectors on the back panels of the transmitter and receiver are labeled with this representation.

1.4 DATA FORMAT

For purposes of multiplexing the data, the frame time, which is fixed at 62.5 μsec, is subdivided into 24 equal time slots. This corresponds to the time between consecutive data samples of one 5 KHz channel*. Twenty-three of the time slots are used for converting analog to digital data and vice versa, while the 24th is reserved for signaling the end of the frame. To accomplish the A/D conversion of all 92 channels, four channels are converted simultaneously, one from each group. For example, channels 1C1, 2C1, 3C1 and 4C1 are converted simultaneously. That is, channels whose code representation differs by only the group number are converted during the same time slot. Each conversion results in a 3 Mbps eight-bit serial data word with the format shown in Figure 1. Bit one appears first in the code.

It should be noted that the Siliconix code chips include a zero code suppression in the A/D conversion to prevent transmission of an all zeros digital output code. A detailed discussion of the digital codes is given in Reference 5.a. Due to the companding nature of the codec chips, the step size of the A/D and D/A conversion depends on the analog voltage. Table 1 shows the corresponding step size versus analog voltage for both the coder (DF331) and the decoder (DF334).

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*The frame time and sampling time are synonomous for 5 KHz operation. However, for higher bandwidths where a channel is sampled more than once during the frame, these tiems are different.

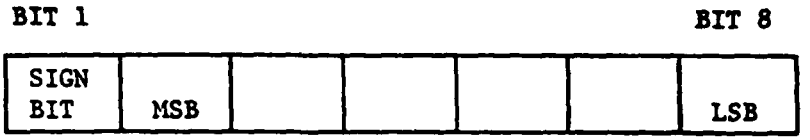

Figure 1. A/D Output Format

All the A/D output lines for a particular group are gated onto a common bus line during their respective time slots. The format for these four data lines is shown in Figure 2.

The four group data lines are further multiplexed onto one common line by means of a shift register. One bit of the eight-bit data word from each of the four group data lines is sumultaneously loaded into the shift register. These four bits are then clocked out serially at 12 MHz, which is four times the rate at which the bits are loaded into the register. They are clocked out in the order of group one through four. Figure 2 demonstrates this multiplexing scheme for one data frame.

1.5 INPUT/OUTPUT FILTERING

1.5.1 Input filtering. Each coder board is equipped with input passive filters to attenuate unwanted aliasing signals. There is a separate filter for each of the three bandwidth ranges. Selection of the appropriate filter is provided by the bandwidth selection switch discussed in Section 3.4. The frequency response (or gain accuracy versus frequency) of the system is strongly affected by these filters. Refer to Section 2.0 on System Specifications for this unit. More sophisticated filters can be used to achieve an arbitrarily flat response up to one half the sampling frequency. A discussion on input filtering by Siliconix is provided in Reference 5.d.

It should be noted that the input filters can be removed and re-

TABLE 1.

NO	DECODER	STEP	CODER	STEP	NO	DECODER	STEP	CODER	STEP	NO	DECODER	STEP	CODER	STEP
1	0.00uV	0.00uV	367.69uV	367.69uV	44	68.76mV	2.94mV	70.23mV	2.94mV	87	517.34mV	23.53mV	529.11mV	23.53mV
2	735.38uV	735.38uV	1.10mV	735.38uV	45	71.70mV	2.94mV	73.17mV	2.94mV	88	540.88mV	23.53mV	552.64mV	23.53mV
3	1.47mV	735.38uV	1.84mV	735.38uV	46	74.64mV	2.94mV	76.11mV	2.94mV	89	564.41mV	23.53mV	576.17mV	23.53mV
4	2.21mV	735.38uV	2.57mV	735.38uV	47	77.58mV	2.94mV	79.05mV	2.94mV	90	587.94mV	23.53mV	599.71mV	23.53mV
5	2.94mV	735.38uV	3.31mV	735.38uV	48	80.52mV	2.94mV	82.00mV	2.94mV	91	611.47mV	23.53mV	623.24mV	23.53mV
6	3.68mV	735.38uV	4.04mV	735.38uV	49	84.94mV	4.41mV	87.88mV	5.88mV	92	635.00mV	23.53mV	646.77mV	23.53mV
7	4.41mV	735.38uV	4.78mV	735.38uV	50	90.82mV	5.88mV	93.76mV	5.88mV	93	658.54mV	23.53mV	670.30mV	23.53mV
8	5.15mV	735.38uV	5.52mV	735.38uV	51	96.70mV	5.88mV	99.64mV	5.88mV	94	682.07mV	23.53mV	693.84mV	23.53mV
9	5.88mV	735.38uV	6.25mV	735.38uV	52	102.59mV	5.88mV	105.53mV	5.88mV	95	705.60mV	23.53mV	717.37mV	23.53mV
10	6.62mV	735.38uV	6.99mV	735.38uV	53	108.47mV	5.88mV	111.41mV	5.88mV	96	729.13mV	23.53mV	740.90mV	23.53mV
11	7.35mV	735.38uV	7.72mV	735.38uV	54	114.35mV	5.88mV	117.29mV	5.88mV	97	764.43mV	35.30mV	787.96mV	47.06mV
12	8.09mV	735.38uV	8.46mV	735.38uV	55	120.24mV	5.88mV	123.10mV	5.88mV	98	811.50mV	47.06mV	835.03mV	47.06mV
13	8.82mV	735.38uV	9.19mV	735.38uV	56	126.12mV	5.88mV	129.06mV	5.88mV	99	858.56mV	47.06mV	882.09mV	47.06mV
14	9.56mV	735.38uV	9.93mV	735.38uV	57	132.00mV	5.88mV	134.94mV	5.88mV	100	905.63mV	47.06mV	929.16mV	47.06mV
15	10.30mV	735.38uV	10.66mV	735.38uV	58	137.88mV	5.88mV	140.83mV	5.88mV	101	952.69mV	47.06mV	976.22mV	47.06mV
16	11.03mV	735.38uV	11.40mV	735.38uV	59	143.77mV	5.88mV	146.71mV	5.88mV	102	999.75mV	47.06mV	1.02 V	47.06mV
17	12.13mV	1.10mV	12.87mV	1.47mV	60	149.65mV	5.88mV	152.59mV	5.88mV	103	1.05 V	47.06mV	1.07 V	47.06mV
18	13.60mV	1.47mV	14.34mV	1.47mV	61	155.53mV	5.88mV	158.48mV	5.88mV	104	1.09 V	47.06mV	1.12 V	47.06mV
19	15.08mV	1.47mV	15.81mV	1.47mV	62	161.42mV	5.88mV	164.36mV	5.88mV	105	1.14 V	47.06mV	1.16 V	47.06mV
20	16.55mV	1.47mV	17.28mV	1.47mV	63	167.30mV	5.88mV	170.24mV	5.88mV	106	1.19 V	47.06mV	1.21 V	47.06mV
21	18.02mV	1.47mV	18.75mV	1.47mV	64	173.18mV	5.88mV	176.12mV	5.88mV	107	1.24 V	47.06mV	1.26 V	47.06mV
22	19.49mV	1.47mV	20.22mV	1.47mV	65	182.01mV	8.82mV	187.89mV	11.77mV	108	1.28 V	47.06mV	1.31 V	47.06mV
23	20.96mV	1.47mV	21.69mV	1.47mV	66	193.77mV	11.77mV	199.66mV	11.77mV	109	1.33 V	47.06mV	1.35 V	47.06mV
24	22.43mV	1.47mV	23.16mV	1.47mV	67	205.54mV	11.77mV	211.42mV	11.77mV	110	1.38 V	47.06mV	1.40 V	47.06mV
25	23.90mV	1.47mV	24.64mV	1.47mV	68	217.31mV	11.77mV	223.19mV	11.77mV	111	1.42 V	47.06mV	1.45 V	47.06mV
26	25.37mV	1.47mV	26.11mV	1.47mV	69	229.07mV	11.77mV	234.96mV	11.77mV	112	1.47 V	47.06mV	1.49 V	47.06mV
27	26.84mV	1.47mV	27.58mV	1.47mV	70	240.84mV	11.77mV	246.72mV	11.77mV	113	1.54 V	70.60mV	1.59 V	94.13mV
28	28.31mV	1.47mV	29.05mV	1.47mV	71	252.60mV	11.77mV	258.49mV	11.77mV	114	1.64 V	94.13mV	1.68 V	94.13mV
29	29.78mV	1.47mV	30.52mV	1.47mV	72	264.37mV	11.77mV	270.25mV	11.77mV	115	1.73 V	94.13mV	1.78 V	94.13mV
30	31.25mV	1.47mV	31.99mV	1.47mV	73	276.14mV	11.77mV	282.02mV	11.77mV	116	1.82 V	94.13mV	1.87 V	94.13mV
31	32.72mV	1.47mV	33.46mV	1.47mV	74	287.90mV	11.77mV	293.79mV	11.77mV	117	1.92 V	94.13mV	1.98 V	94.13mV
32	34.20mV	1.47mV	34.93mV	1.47mV	75	299.67mV	11.77mV	305.55mV	11.77mV	118	2.01 V	94.13mV	2.06 V	94.13mV
33	36.40mV	2.21mV	37.87mV	2.94mV	76	311.44mV	11.77mV	317.32mV	11.77mV	119	2.11 V	94.13mV	2.15 V	94.13mV
34	39.34mV	2.94mV	40.81mV	2.94mV	77	323.20mV	11.77mV	329.08mV	11.77mV	120	2.20 V	94.13mV	2.25 V	94.13mV
35	42.28mV	2.94mV	43.76mV	2.94mV	78	334.97mV	11.77mV	340.85mV	11.77mV	121	2.29 V	94.13mV	2.34 V	94.13mV
36	45.23mV	2.94mV	46.70mV	2.94mV	79	346.73mV	11.77mV	352.62mV	11.77mV	122	2.39 V	94.13mV	2.44 V	94.13mV
37	48.17mV	2.94mV	49.64mV	2.94mV	80	358.50mV	11.77mV	364.38mV	11.77mV	123	2.48 V	94.13mV	2.53 V	94.13mV
38	51.11mV	2.94mV	52.58mV	2.94mV	81	376.15mV	17.65mV	387.92mV	23.53mV	124	2.58 V	94.13mV	2.62 V	94.13mV
39	54.05mV	2.94mV	55.52mV	2.94mV	82	399.68mV	23.53mV	411.45mV	23.53mV	125	2.67 V	94.13mV	2.72 V	94.13mV
40	56.99mV	2.94mV	58.46mV	2.94mV	83	423.21mV	23.53mV	434.98mV	23.53mV	126	2.76 V	94.13mV	2.81 V	94.13mV
41	59.93mV	2.94mV	61.40mV	2.94mV	84	446.75mV	23.53mV	458.51mV	23.53mV	127	2.86 V	94.13mV	2.91 V	94.13mV
42	62.88mV	2.94mV	64.35mV	2.94mV	85	470.28mV	23.53mV	482.04mV	23.53mV	128	2.95 V	94.13mV	3.00 V	94.13mV
43	65.82mV	2.94mV	67.29mV	2.94mV	86	493.81mV	23.53mV	505.50mV	23.53mV	129	0.00uV	0.00uV	0.00uV	0.00uV

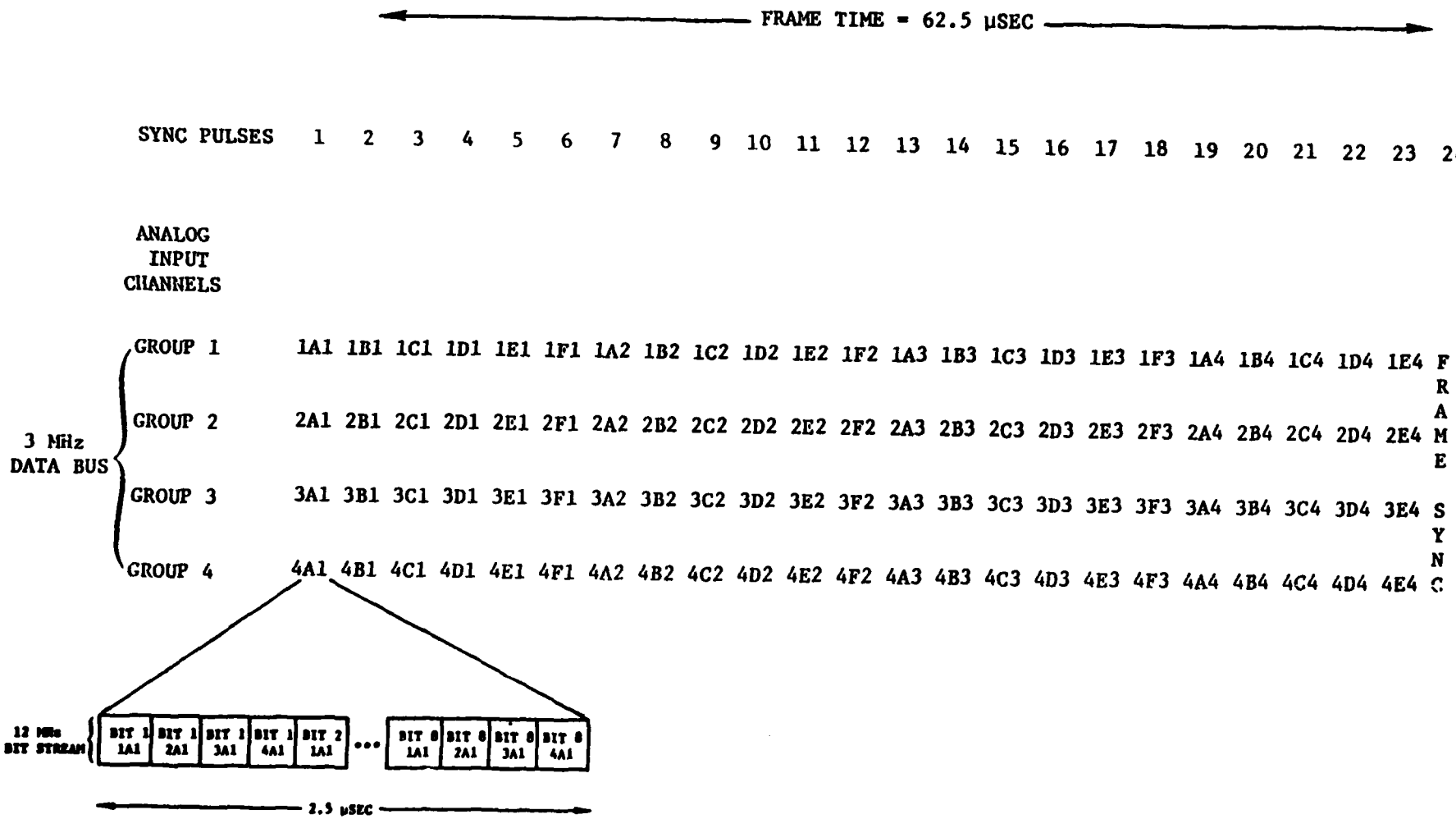

Figure 2. Formats for 3 Mbps Group Data Buses and the 12 Mbps Bit Stream

placed by jumpers. This will eliminate pulse overshoot and provide a flatter frequency response, but only at the expense of removing the aliasing protection.

1.5.2 Output filtering. The analog output is filtered through a passive RC network. The response of the system at frequencies near half the sampling frequency can be improved by including a sinX/X output filter. This type of filter can be implemented as either hardware or software additions. Refer to the discussion on signal filtering by Siliconix in Reference 5.d.

SECTION 2.0

SYSTEM SPECIFICATIONS

2.0 SYSTEM SPECIFICATIONS

GENERAL

Number of Channels	92 to 20
Sampling Rate	16 KHz to 64 KHz
Tradeoff of Channels versus Sampling Rate	4 channels at a time can be switched together to give 2 channels at 32 KHz or 1 channel at 64 KHz
Bandwidth	D.C. to 0.3 times the sampling rate for 6 dB attenuation
Resolution	8 bit companding analog to digital (0.025% resolution near zero)
Data Transmission Rate	12.28 Mbps decodable to 4 each 3.07 Mbps
Fiber Type	Graded index
Electrical to Optical Transducer	Light emitting diode (LED)
Optical to Electrical Transducer	PIN diode
Coding	Manchester (Biphase-L): 12.28 Mbps NRZ-L: 3.07 Mpbs

ELECTRICAL

Power	105 to 125 VAC, 60 Hz, 1.1 amp transmitter 1.0 amp receiver
Digital Levels	TTL
Connectors	BNC
Input Impedance, Analog	10K ohms
Input Impedance, Digital	50 ohms
Output Impedance, Analog	300 ohms
Output Impedance, Digital	50 ohms
Sampling Rate - f_o	16 KHz, 32 KHz or 64 KHz

ELECTRICAL (Continued)

*Frequency Response		
(D.C. to 0.3 f_o)	+0, -6db	Compensation can be employed to improve these specifications.
(D.C. to 0.1 f_o)	+0, -10%	
(D.C. to 0.03 f_o)	+0, -2%	
Resolution	8 bit digital, μ255 law companding[1]	
Small Signals	±0.025% of full scale or ± 0.74 mVolt	
Large Signals	±1.6% of full scale or ±47 mVolt	
Signals from 1% of Full Scale, to Full Scale	<±5% of signal	
*Noise (D.C. to 0.3 f)	(Quantizing Noise) + (<0.5 mV RMS)	
*Noise (D.C. to 1MHz)	(Quantizing Noise) + (<5 mV RMS)	
Linearity	Less than ±1 quantizing step size	
Zero Accuracy	0 ± 5 mV	
Voltage Gain	1 ± 1% plus quantizing noise	
Maximum Signal Voltage	+2.8 / -3.0 volts	
Input Signal Limiter	± 6 volts	
*Pulse Response	Ringing <±10% at ∿0.3 f Damping time constant <100 μsec	
Overload Recovery	To 1% of full scale within 10 μsec after a 100 volt, 10 μsec overload	
*Antialiasing Filter	>18 db attenuation at $f_o/2$	

*These specifications can be improved or modified with different input and/or output filters.

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(1) Siliconix Telecommunication Data Book, November 1979, Section 6.0, Reference 5.a.

OPTICAL

Connectors	Amphenol 906
Fiber Type Recommended	Siecor 122 63 μm core diameter 0.21 numerical aperture 6 db/km attenuation
Gain Margin; Typical (Depends on the transmitter and receiver installed and on other factors)	15 db (compared to a 10m link)

19 inch rack width

11.25 inch height

23 inch depth overall, Transmitter

18.5 inch depth overall, Receiver

21.5 inch depth behind rack mount. Transmitter

17 inch depth behind rack mount, Receiver

60 pounds weight, Transmitter

55 pounds weight, Receiver

ENVIRONMENTAL

Transmitter, 0 to 55°C

Receiver, 15 to 30°C

SECTION 3.0

SYSTEM OPERATION

3.0 SYSTEM OPERATION

3.1 EXTERNAL CONNECTIONS - TRANSMITTER

All external connections to the transmitter chassis are located on the back panel. Refer to Section 7.2 for a view of the transmitter back panel.

3.1.1 Analog. There are 92 BNC connectors available for analog input data. The analog channels are labeled with three symbols: number-letter-number. A detailed explanation of channel labeling can be found in Section 1.3. The input signal levels are ± 3 volts.

3.1.2 Digital. There are two BNC connectors which involve digital data:

MUX OUT - This TTL level output signal is the 12 Mbps time division multiplexed data containing all 92 channels of data. This signal is buffered through a 50-ohm coaxial cable driver. Any external connection to this output must provide a 50-ohm terminator. In normal operation this output is jumpered to the F/O XMIT IN connector.

F/O XMIT IN - This signal line accepts TTL level input signals which are simultaneously fed to both fiber optic transmitters. The input is terminated with 50 ohms. In normal operation this connector is jumpered to the MUX OUT connector.

3.1.3 Fiber optic. There are one or optionally two fiber optic output connectors. The connectors are Amphenol Model 906. One end of the fiber optic cable is connected to one of these outputs. See System specifications for recommended fiber optic cable.

CAUTION: INTERNAL DAMAGE MAY RESULT IF THE FOLLOWING INSTRUCTIONS ARE NOT FOLLOWED:

Red Connector: NO FERRULE
Green Connector: FERRULE REQUIRED.

A ferrule, furnished with the amphenol 906 connector, is required by certain connectors for proper alignment of the optical fiber; however, the presence of a ferrule where it is not needed may cause severe damage to the optical components behind the connector.

3.2 RECEIVER

All external connections to the receiver chassis are located on the back panel. Refer to Section 7.4 for a view of the receiver back panel.

3.2.1 Analog. There are 92 BNC connectors available for analog output data. The analog output channels are labeled with three symbols: number-letter-number. A detailed explanation of channel labeling can be found in Section 1.3. The output signal levels are ±3 volts.

3.2.2 Digital. There are a total of seven digital connections on the receiver. These signals are listed below:

1. F/O RECEIVE OUT - This signal is the TTL level output of the fiber optic receiver and has been buffered through a 50-ohm coaxial cable driver. Any external connection to this output must provide a 50-ohm terminator. It is the 12 Mbps multiplexed signal which contains data from all the operational channels. In normal operation, this output is jumpered to the MUX IN input. The data format is Biphase-L.

2. MUX IN - This input accepts the TTL level 12 Mbps multiplexed data. This input is terminated with 50 ohms. In normal operation this input is jumpered to the F/O RECEIVE OUT connector.

3. GROUP 1 OUT - This output provides the 3 Mbps group multiplexed data for all group 1 channels. This TTL level signal is buffered through a 50-ohm coaxial cable driver. Any external connection to this output must provide a 50-ohm terminator. The data format is NRZ-L.

4. GROUP 2 OUT - This output provides the 3 Mbps group multiplexed data for all group 2 channels. This TTL level signal is buffered through a 50-ohm coaxial cable driver. Any external connection to this output must provide a 50-ohm terminator. The data format is NRZ-L.

5. GROUP 3 OUT - This output provides the 3 Mbps group multiplexed data for all group 3 channels. This TTL level signal is buffered through a 50-ohm coaxial cable driver. Any external connection to this output must provide a 50-ohm terminator. The data format is NRZ-L.

6. GROUP 4 OUT - This output provides the 3 Mbps group mulitplexed data for all group 4 channels. This TTL level signal is buffered through a 50-ohm coaxial cable driver. Any external connection to this output must provide a 50-ohm terminator. The data format is NRZ-L.

7. CLOCK OUT - This TTL level output supplies a 3 Mbps clock signal which has been buffered through a 50-ohm coaxial cable driver. Any external connection to this

output must provide a 50-ohm terminator. This signal can be used in digitally recording the group data out signals when optional interface circuits are available.

3.2.3 Fiber optic. There are one or optionally two fiber optic receivers with one connector for each of the receivers. These connectors are Amphenol Model 906. Unlike the fiber optic transmitters, the fiber optic receivers are not operated in parallel. They are switch selectable by switch S1 located on the line driver board in the receiver chassis.

CAUTION: INTERNAL DAMAGE MAY RESULT IF THE FOLLOWING INSTRUCTIONS ARE NOT FOLLOWED:

Red Connector: NO FERRULE
Green Connector: FERRULE REQUIRED.

A ferrule is required by certain connectors for proper alignment of the optical fiber; however, the presence of a ferrule where it is not needed may cause severe damage to the optical components behind the connector.

3.3 FRONT PANEL DESCRIPTION

3.3.1 Transmitter. There are seven indicators and one switch located on the front panel of the transmitter and are described below. Refer to Section 7.1 for a view of the transmitter front panel.

1. Power ON/NOT ON Switch

   This switch is located on the bottom right-hand side of the front panel and is green in color. This switch turns on the AC power and will light up when AC power is ON.

2. Bit Stream

This indicator will be on when the 12 Mbps bit stream is present. If it is not, a problem on the multiplexer board would be suspected.

3. OVP OFF

This indicator will be on when the over voltage protection circuitry is disconnected from all internal power supplies. This is controlled by a switch located on the right-hand side, behind the lower front panel. The panel is lowered by unscrewing the thumb screws at the top of the panel. The switch is labeled OVP with ON and OFF positions clearly visible. In the ON position, the over voltage protection circuitry for each power supply is connected.

The OVP can be triggered by low radiation dose rates, thereby shutting off power. The OVP should be off when operating in radiation environments. The OVP should also be off whenever link operation is more important than protecting circuits from damage due to over voltage.

4. +7.5V

This indicator is on when +7.5 volts are present.

5. -7.5V

This indicator is on when -7.5 volts are present.

6. +3V

This indicator is on when +3 volts are present.

7. -3V

This indicator is on when -3 volts are present.

8. +5V

This indicator is on when +5 volts are present.

NOTE: Since the +3V supply is derived from the ±7V supplies and the -3V supply is derived from the +3 and ±7V supplies, interactions occur.

3.3.2 Receiver. There are nine indicators and one switch located on the front panel of the receiver, and are described below. Refer to Section 7.3 for a view of the receiver front panel.

1. Power ON/NOT ON

This switch is located on the bottom right-hand side of the front panel and is green in color. This switch turns on the AC power and will light up when AC power is ON.

2. Bit Stream

This indicator will be on when the 12 Mbps bit stream is present. If this light is off and the bit stream indicator on the transmitter is ON, a problem with the fiber optics would be suspected. Some fiber optic receivers put out an oscillatory signal when there is no input. When using these type receivers, the bit stream indicator will always be ON.

3. OVP OFF

This indicator will be on when the over voltage protection circuitry is disconnected from all internal power supplies. This is controlled by a switch located on the right-hand side, behind the lower front panel. This panel is lowered by unscrewing the thumb screws at the top of the panel. The switch is labeled OVP with ON and OFF positions clearly visible. In the ON position, the over voltage protection circuitry for each power supply is connected. See discussion on when to use OVP in Section 3.3.1.

4. +7.5V

This indicator is on when +7.5 volts are present.

NOTE: The voltage at the +7.5 volt power supply has been increased to approximately 9 volts in order to supply a necessary 8 volts to the codec circuits on the decoder boards.

5. -7.5V

This indicator is on when -7.5 volts are present.

NOTE: The voltage at the 7.5 volt power supply has been adjusted to approximately -9 volts in order to supply a necessary -8 volts to the codec circuits on the decoder boards.

6. +3V

This indicator is on when 3 volts are present.

NOTE: The -3 volt power supply has been adjusted to approximately -3.2 volts so as to provide a system gain of one.

8. +5V

This indicator is on when +5 volts are present.

9. +15V

This indicator is on when +15 volts are present.

10. -15V

This indicator is on when -15 volts are present.

3.4 Bandwidth Selection

The bandwidth of the system can be varied between 5 KHz, 10 KHz, and 20 KHz by switches located on both coder and decoder boards. These switches are accessible by lowering the front panels of each chassis. Each bandwidth selection switch determines the sampling rate for the four channels associated with a particular coder-decoder board set and assigns appropriate input filters. For proper operation, coder and decoder switches must be in the same position. It must be noted that higher bandwidths (10 KHz and 20 KHz) have been achieved by paralleling appropriate channels on the coder boards. This results in a reduction in sampling time and a reduction in the number of useable channels.

In the 5 KHz position, all four channels associated with a coder-decoder board set are operational.

In the 10 KHz position, two channels are paralleled to effect a faster sampling rate since the maximum sampling rate for one coding codec chip (DF 331) is 16 KHz. In this position, channel XX1 is paralleled with channel XX3 and channel XX2 with channel XX4. (Refer to Section 1.3 on channel nomenclature.) This has the effect of reducing the

number of useable channels to two for each coder-decoder board set. However, this is not true for those channels labeled F since there are only three channels available on these boards in the 5 KHz position. This limits the number of 10 KHz channels for each board labeled F to one. Thus, the total number of system channels with a bandwidth of 10 KHz is 44. The analog input signals must be connected to channels XX1 and XX2. Likewise, the analog output signals are found on channels XX1 and XX2, respectively.

In the 20 KHz position, all four channels on each coder-decoder board set are paralleled. Thus, there is only one 20 KHz channel per board. Again, this is not true for those boards labeled F and since there are only three 5 KHz channels on these boards, no 20 KHz channels can be formed. The total number of 20 KHz system channels is 20. The analog input signals must be connected to channels XX1. Likewise, the analog outputs are found on channels XX1.

In summary, the bandwidth versus maximum number of system channels is shown in Table 2.

Table 2

Bandwidth	Channels
5 KHz	92
10 KHz	44
20 KHz	20

Since the process of assigning bandwidths can become complicated, it is suggested that a worksheet be filled out for ease in setting up the channels. A sample worksheet is provided in Figure 4. Two blank worksheets are included in Section 7.0. To use this worksheet, these

steps should be followed:

1. Fill in the number of channels desired for each bandwidth.

2. Starting with the 20 KHz bandwidth, fill in the chassis slot numbers to accommodate the number of 20 KHz channels desired. For convenience, the slot numbers in the sample worksheet have been chosen to start with 1A and finish with 4F, to correspond to the first two characters of the channel numbers in that slot.

3. Fill in the slot numbers for the 10 and 5 KHz bandwidths, respectively.

4. Complete the Channels/Slot row for each slot number, and each bandwidth, remembering that there are a maximum of four 5 KHz channels per slot, two 10 KHz channels per slot, or one 20 KHz per slot for all slots except IF, 2F, 3F and 4F. For these slots, there are a maximum of three 5 KHz channels per slot or one 10 KHz channel per slot.

5. Fill in the matrix which corresponds to the back panel of each chassis by indicating both channel number and assigned bandwidth. It may be helpful to put an X in those blocks which are not operational due to the paralleling of channels to achieve higher bandwidths.

3.5 FIBER OPTIC RECEIVER SELECTION

A switch labeled S1 on the line driver board in the receiver chassis allows selection between fiber optic receiver #1 and receiver #2. Each position is clearly labeled on the board.

CHANNEL/BANDWIDTH ASSIGNMENT WORKSHEET

BANDWIDTH	NO. OF CHANNELS DESIRED	ASSIGNMENT																						
20 kHz	10	SLOT NO.	1A	1B	1C	1D	1E	2A	2B	2C	2D	2E												
		CHANNELS/ SLOT	1	1	1	1	1	1	1	1	1	1												
10 kHz	20	SLOT NO.	1F	2F	3A	3B	3C	3D																
		CHANNELS/ SLOT	1	1	2	2	2	2																
5 kHz	32	SLOT NO.	1F	2F	3F	4A	4B	4C	4D	4E	4F													
		CHANNELS/ SLOT	1	1	4	3	4	4	4	4	3													

X INDICATES A NON-OPERATIONAL CHANNEL

EACH BOX CORRESPONDS TO A BACK PANEL CONNECTOR

2F1 5	2E1 20	2D1 20	2C1 20	2B1 20	2A1 20	1F1 10	1E1 20	1D1 20	1C1 20	1B1 20	1A1 20
2F2 5	X	X	X	X	X	1F2 5	X	X	X	X	X
X	X	X	X	X	X	X	X	X	X	X	X
■	X	X	X	X	X	■	X	X	X	X	X
4F1 5	4E1 5	4D1 5	4C1 5	4B1 5	4A1 5	3F1 5	3E1 5	3D1 10	3C1 10	3B1 10	3A1 10
4F2 5	4E2 5	4D2 5	4C2 5	4B2 5	4A2 5	3F2 5	3E2 2	3D2 10	3C2 10	3B2 10	3A2 10
4F3 5	4E3 5	4D3 5	4C3 5	4B3 5	4A3 5	3F3 5	3E3 5	X	X	X	X
■	4E4 5	4D4 5	4C4 5	4B4 5	4A4 5	■	3E4 5	X	X	X	X

Figure 4. Sample Worksheet

3.6 OFFSET ADJUSTMENT

There are two analog offset adjustments available, one for the input stage of the transmitter and one for the output stage of the receiver.

3.6.1 Input offset. There is an input offset adjustment for each channel located on the coder boards. The potentiometers used for this adjustment are R17, R18, R19 and R20. Each pot is adjusted so that a shorted analog input produces the eight-bit code associated with a zero volt input on the output of the codec chip (DF331). This code is: 01111111 or 1111111. Refer to Diagram 7.10 for location of adjustment pots.

3.6.2 Output offset. There is an output offset adjustment for each channel located on the decoder boards. The potentiometers are labeled R22, R23, R24 and R25 on each decoder board. Each pot is adjusted so that the eight-bit bode corresponding to zero volts on the input to the codec chip (DF334) produces zero volts at the final output stage. Refer to Diagram 7.10 for location of adjustment pots.

3.7 GAIN ADJUSTMENT

A separate gain adjustment has been provided for each channel and is accomplished by adjusting pots R7, R10, R13 and R16 on each coder board. The gain should be adjusted so that the voltage at the input to the codec chip (DF331) is the same as the voltage at the input connector. Refer to Diagram 7.10 for location of adjustment pots.

3.8 INPUT SIGNAL LIMITER ADJUSTMENT

A limiter adjustment is available for each channel so that the

voltage level at which the input analog signal is limited can be varied. This is achieved by adjusting pots R5, R8, R11 and R14 on the coder boards. This adjustment has been set so that the input signal begins distorting above ±3 volts and is limited at ±6 volts. Refer to Diagram 7.10 for location of adjustment pots.

3.9 RECEIVER TIMING ADJUSTMENT

A timing adjustment pot, R1, is located on the demultiplexer board in the receiver chassis. It is used to set proper timing in the decoding circuitry. It should be set in the middle of the range for which an undistorted analog output signal is achieved. Refer to Diagram 7.10 for location of adjustment pot.

SECTION 4.0

COMPUTER INTERFACE OPTION

4.0 COMPUTER INTERFACE OPTION

4.1 DESCRIPTION

An optional computer interface board has been included to provide the following functions:

1) Fiducial Status
2) Calibration Status
3) Frame Counter
4) Sync Word

This board should be placed in the backplane connector slot labeled 1F. Thus, in choosing this option, channels 1F1, 1F2 and 1F3 are no longer available.

This interface board uses the eight-bit data time slots associated with channels 1F1 and 1F2, in the following format.

Sync Word. The sync word is an eight-bit selectable code which can be used as a frame sync. It occurs once in every frame during the time slot associated with the 1F1 channel. The circuit is wired so that the MSB bit of the code appears in the first bit position. The code is selectable by jumpers on the interface board. The format for the sync word is shown in Figure 3.

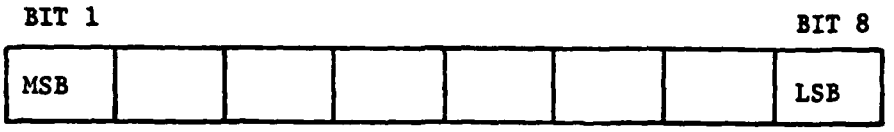


Figure 3. 1F1 Data Slot: Sync Word

Fiducial Status. An input connector is provided on the back panel of the transmitter chassis for a fiducial signal. The requirements for the signal are that it is between 20 and 200 volts in peak amplitude, with a 40 nanosecond minimum pulse width. The circuit is designed to provide a logical one in the first bit position of the 1F2 channel data slot for about 3 msec after the fiducial signal. A logical zero returns after about 3 msec following the signal.

Calibration Status. A calibration status input connector is located on the back panel of the transmitter chassis. It is designed to accept a switch closure input. Upon closure of the switch, a logical zero status bit is provided in the second-bit position of the 1F2 channel data slot; alternatively, a logical one results when the switch is open.

Frame Counter. A frame counter is provided on the interface board whose output is a continuous count of data frames with no reset. The format of the counter output is a six-bit binary code. It occupies the third through the eighth bit position of the 1F2 channel data slot. Frame count data can be used with the fiducial status bit to determine the number of frames transmitted since the fiducial signal. The format for the 1F2 data slot is shown in Figure 4.

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8
1- FIDU PRESENT 0- FIDU NOT PRESENT	1- NORMAL DATA 0- CAL DATA	FRAME COUNT MSB	FRAME COUNT	FRAME COUNT	FRAME COUNT	FRAME COUNT	FRAME COUNT LSB

Figure 4. 1F2 Data Slot: Fiducial Status, Calibration Status and Frame Count

4.2 EXTERNAL STATUS CONNECTIONS

Fiducial Input - A fiducial input is provided and has been termina-

ted with 50 ohms. The input is designed to accept 20 to 200 volt signals with a minimum of 40 nanoseconds pulse width. The circuitry for the fiducial status is located on the computer interface board which, when selected, resides in the backplane connector slot labeled 1F. The fiducial status appears as a logical one in the first bit position of the eight-bit time slot allotted to channel 1F2 for about 3 msec following a fiducial pulse, and a logical zero after this time.

Calibrate Input - A calibrate input is provided to indicate when calibration data is being transmitted over the data link. The circuit for the calibration input is located on the digital interface board. The circuit is designed such that a switch closure produces a logical zero in the second bit position of the eight-bit time slot allotted to channel 1F2. When normal data are being transmitted, the status bit appears as a logicial one.

NOTE: This computer interface option is developmental at the time of this writing and is not part of the standard link.

SECTION 5.0

SYSTEM OPERATION CHECKLIST

5.0 SYSTEM OPERATION CHECKLIST

In order to insure proper operation of the data link, the following steps should be carefully followed:

1. Assign bandwidths to the channels. Refer to Section 3.4 on bandwidth selection. It is suggested that a worksheet be filled out similar to the one provided in Figure 4. Two blank worksheets are included in Section 7.7.

2. Select the desired bandwidth for each channel. These switches are located on the edge of the coder and decoder boards. The front panels must be lowered in order to reach them. Make sure that switches on both the transmitter and receiver are in the desired position.

3. Connect coaxial cables to appropriate channels. Use matrix developed in Step 1.

4. Make sure the following jumpers are in place on the back panels:

   a) MUX OUT to F/O XMIT IN on transmitter
   b) F/O RECEIVE OUT to DEMUX IN on receiver.

5. Make sure fiber optic cable connectors are secured to panel connectors. Note the warning label concerning the use of ferrules. This warning is also described in Sections 3.1.3 and 3.2.3.

6. Select desired fiber optic reciever. This switch is

labeled S1 and is located on the line driver board in the receiver chassis.

7. Make sure power cords for both transmitter and receiver are securely plugged into AC power outlets.

8. Push Power ON switch for both transmitter and receiver chassis.

SECTION 6.0

DIAGRAMS AND SCHEMATICS

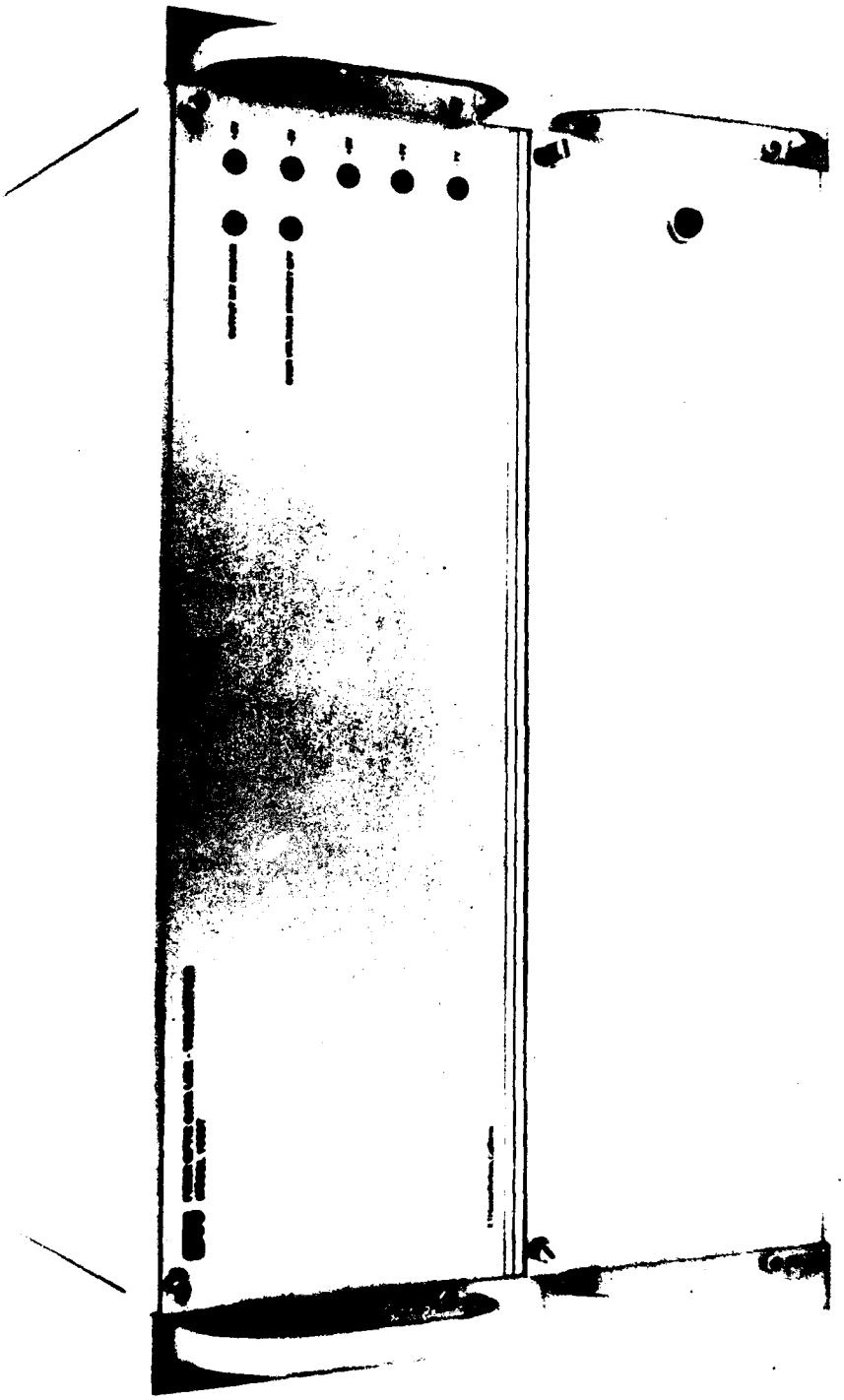


Diagram 6.1. Transmitter - Front View

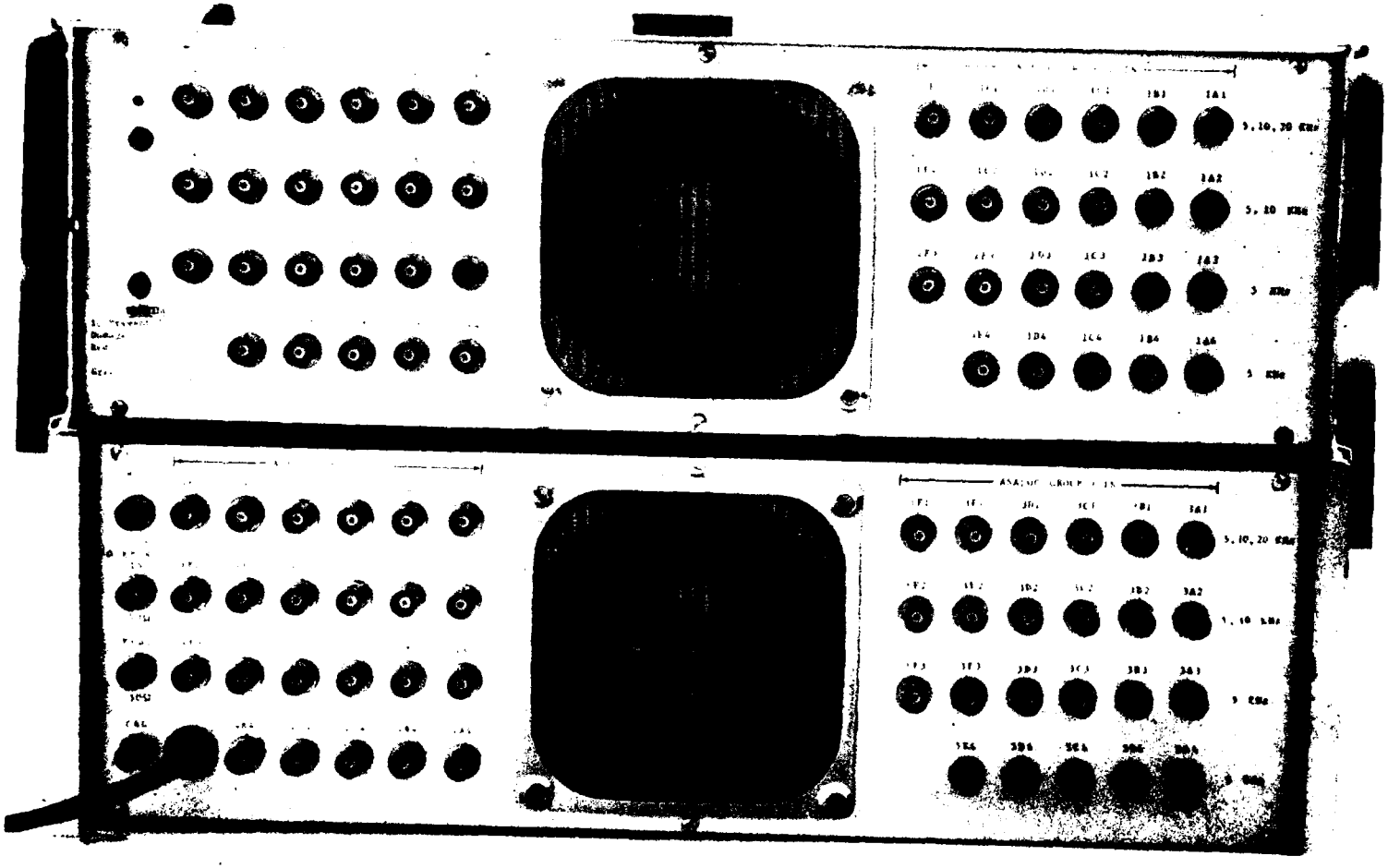


Diagram 6.2. Transmitter - Back View

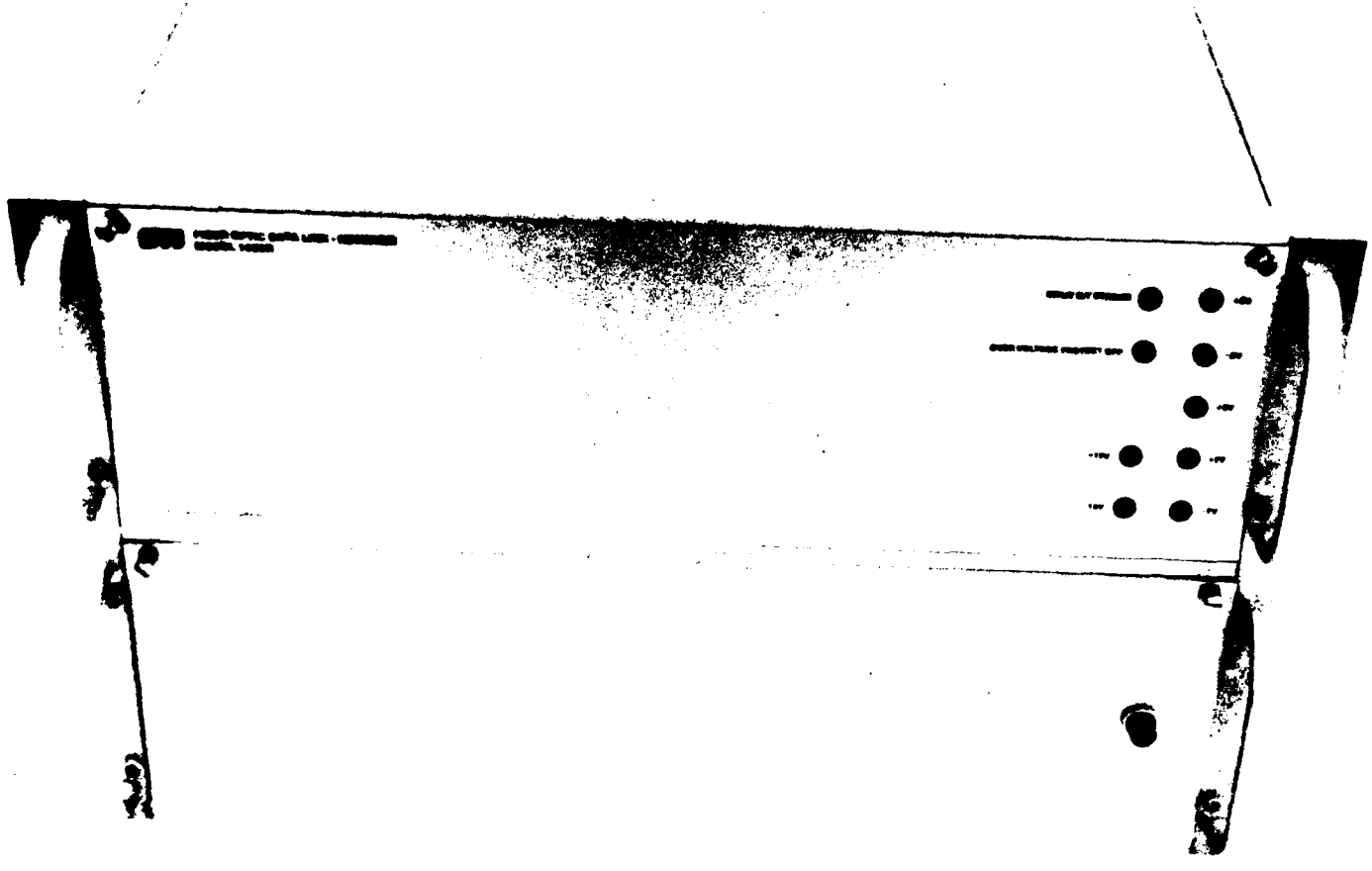


Diagram 6.3. Receiver - Front View

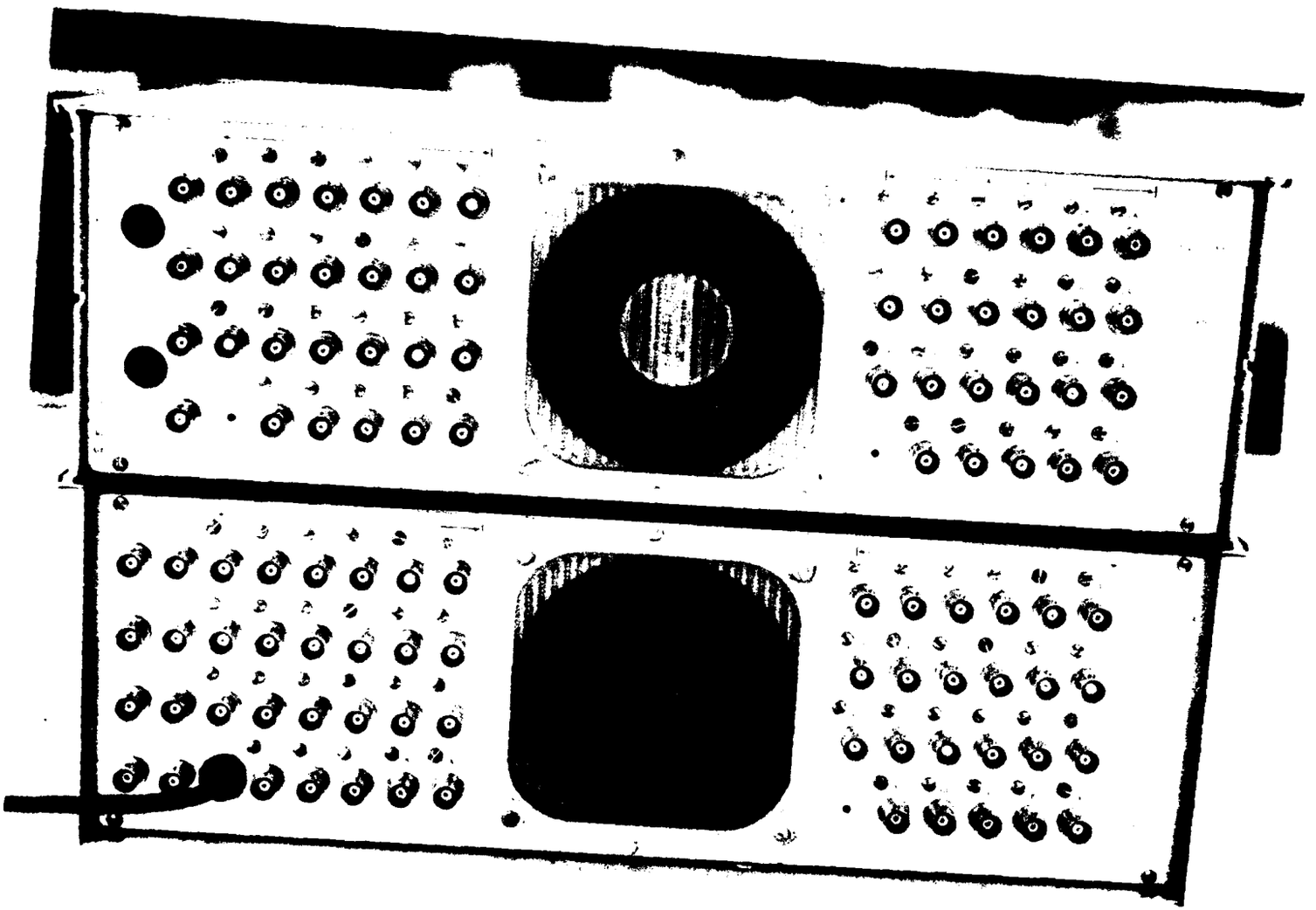


Diagram 6.4. Receiver - Back View

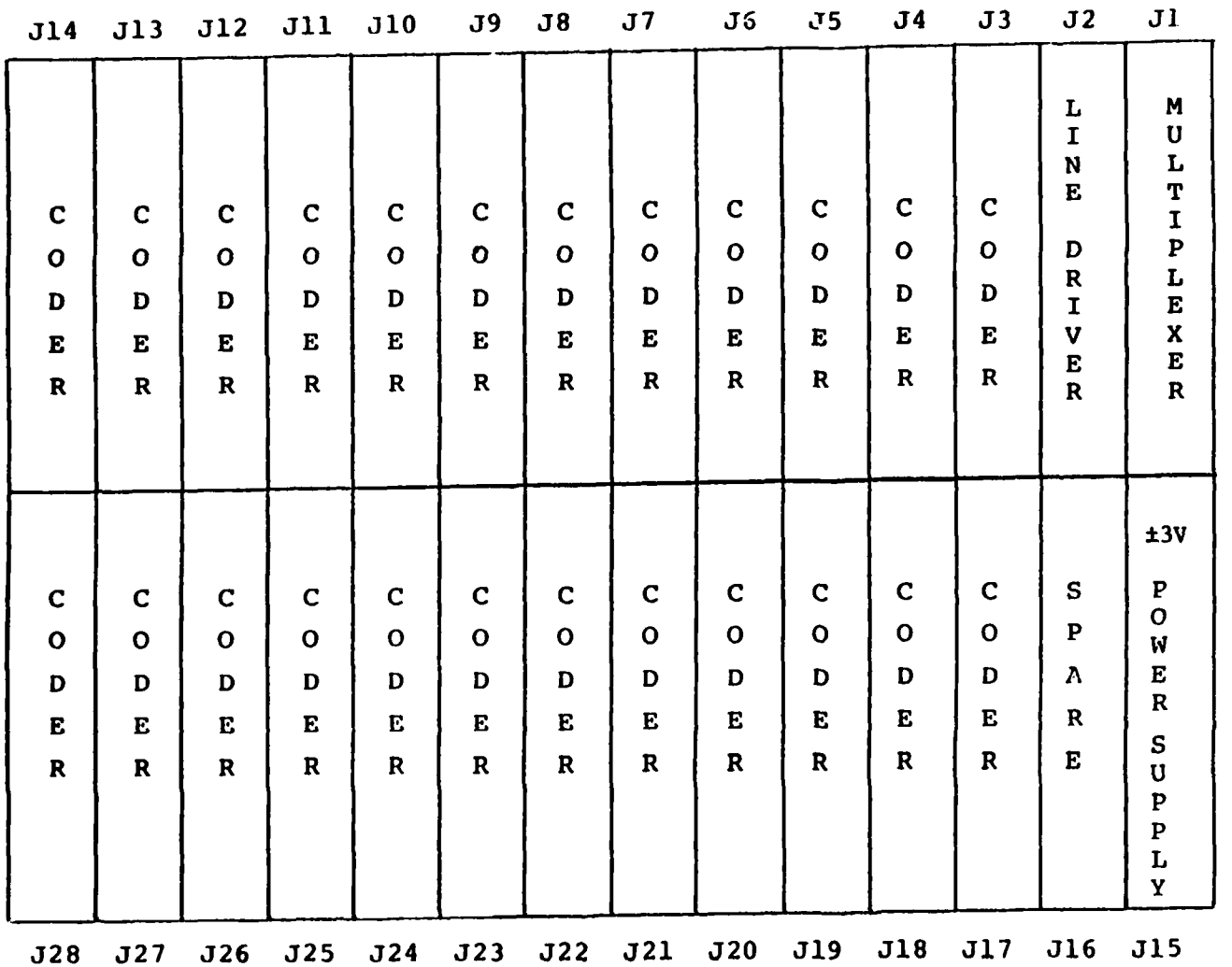


Diagram 6.5. Transmitter Chassis
Card Locations - Front View

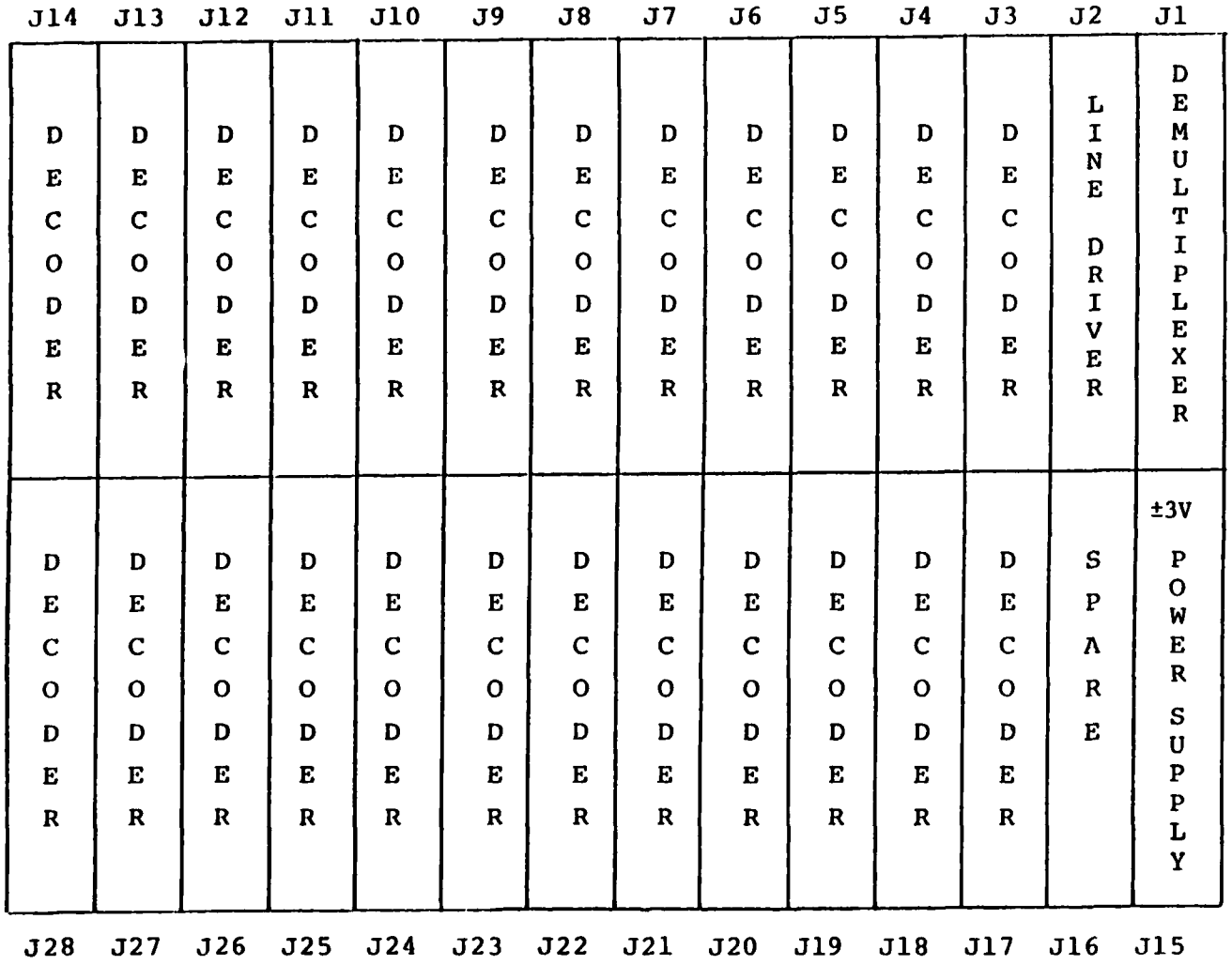
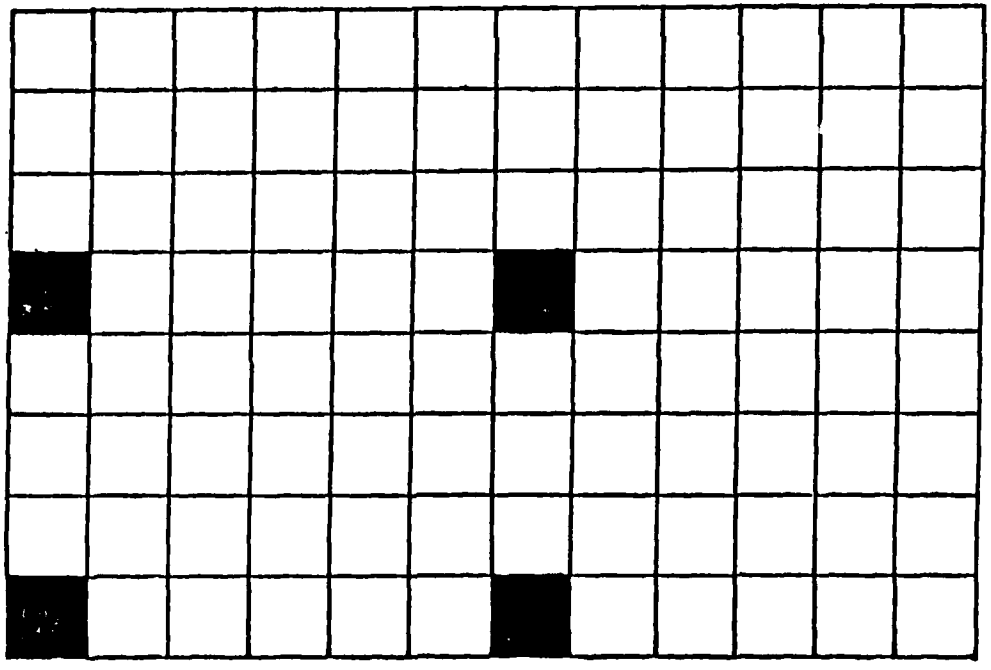


Diagram 6.6. Receiver Chassis
Card Locations - Front View

CHANNEL/BANDWIDTH ASSIGNMENT WORKSHEET

BANDWIDTH	NO. OF CHANNELS DESIRED	ASSIGNMENT
20 kHz		SLOT NO. CHANNELS/ SLOT
10 kHz		SLOT NO. CHANNELS/ SLOT
5 kHz		SLOT NO. CHANNELS/ SLOT

BACK PANEL MATRIX



X INDICATES A NON-OPERATIONAL CHANNEL

Diagram 6.7. Channel/Bandwidth Assignment Worksheet

CHANNEL/BANDWIDTH ASSIGNMENT WORKSHEET

BANDWIDTH	NO. OF CHANNELS DESIRED		ASSIGNMENT
20 kHz		SLOT NO. CHANNELS/ SLOT	
10 kHz		SLOT NO. CHANNELS/ SLOT	
5 kHz		SLOT NO. CHANNELS/ SLOT	

X INDICATES A NON-OPERATIONAL CHANNEL

BACK PANEL MATRIX

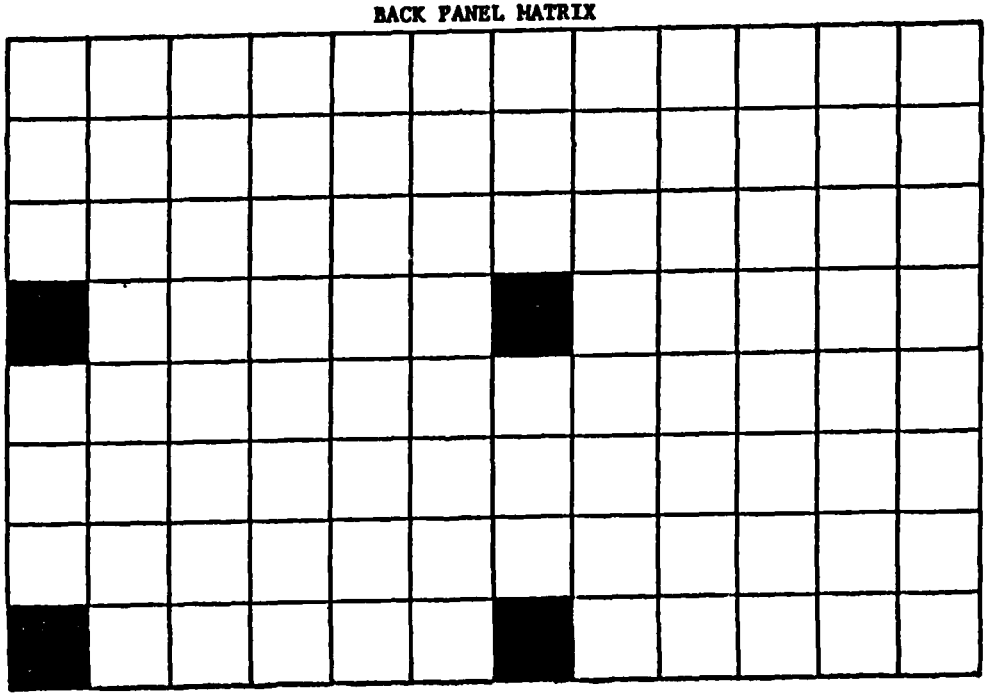


Diagram 6.7. Channel/Bandwidth Assignment Worksheet

6.8 BACKPLANE WIRE LIST - TRANSMITTER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J1	E	J3	9	Violet	3MHz Clock
J3	9	J4	9	Bus Wire	
J4	9	J5	9		
J5	9	J6	9		
J6	9	J7	9		
J7	9	J8	9		
J8	9	J9	9		
J9	9	J10	9		
J10	9	J11	9		
J11	9	J12	9		
J12	9	J13	9		
J13	9	J14	9		
J1	E	J17	9	Violet	
J17	9	J18	9	Bus Wire	
J18	9	J19	9		
J19	9	J20	9		
J20	9	J21	9		
J21	9	J22	9		
J22	9	J23	9		
J23	9	J24	9		
J24	9	J25	9		
J25	9	J26	9		
J26	9	J27	9		
J27	9	J28	9		
J1	F	J9	K	Blue	Group 1 Digital Data
J9	K	J10	K	Bus Wire	
J10	K	J11	K		
J11	K	J12	K		
J12	K	J13	K		
J13	K	J14	K		
J1	6	J3	K	Blue	Group 2 Digital Data
J3	K	J4	K	Bus Wire	
J4	K	J5	K		
J5	K	J6	K		
J6	K	J7	K		
J7	K	J8	K		
J1	H	J23	K	Blue	Group 3 Digital Data
J23	K	J24	K	Bus Wire	
J24	K	J25	K		
J25	K	J26	K		
J26	K	J27	K		
J27	K	J28	K		

BACKPLANE WIRE LIST - TRANSMITTER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J1	7	J17	K	Blue	Group 4 Digital Data
J17	K	J18	K	Bus Wire	
J18	K	J19	K	↓	↓
J19	K	J20	K		
J20	K	J21	K		
J21	K	J22	K		
J1	9	J8	10	White	SYNC1-2A1
J8	10	J14	10	↓	SYNC1-1A1
J1	9	J22	10		SYNC1-4A1
J22	10	J28	10		SYNC1-3A1
J1	K	J7	10	White	SYNC2-2B1
J7	10	J13	10	↓	SYNC2-1B1
J1	K	J21	10		SYNC2-4B1
J21	10	J27	10		SYNC2-3B1
J1	10	J6	10	White	SYNC3-2C1
J6	10	J12	10	↓	SYNC3-1C1
J1	10	J20	10		SYNC3-4C1
J20	10	J26	10		SYNC3-3C1
J1	L	J5	10	White	SYNC4-2D1
J5	10	J11	10	↓	SYNC4-1D1
J1	L	J19	10		SYNC4-4D1
J19	10	J25	10		SYNC4-3D1
J1	11	J4	10	White	SYNC5-2E1
J4	10	J10	10	↓	SYNC5-1E1
J1	11	J18	10		SYNC5-4E1
J18	10	J24	10		SYNC5-3E1
J1	M	J3	10	White	SYNC6-2F1
J3	10	J9	10	↓	SYNC6-1F1
J1	M	J17	10		SYNC6-4F1
J17	10	J23	10		SYNC6-3F1
J1	12	J8	L	White	SYNC7-2A2
J8	L	J14	L	↓	SYNC7-1A2
J1	12	J22	L		SYNC7-4A2
J22	L	J28	L		SYNC7-3A2
J1	N	J7	L	White	SYNC8-2B2
J7	L	J13	L	↓	SYNC8-1B2
J1	N	J21	L		SYNC8-4B2
J21	L	J27	L		SYNC8-3B2

BACKPLANE WIRE LIST - TRANSMITTER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J1	13	J6	L	White	SYNC9-2C2
J6	L	J12	L	↓	SYNC9-1C2
J1	13	J20	L	↓	SYNC9-4C2
J20	L	J26	L	↓	SYNC9-3C2
J1	P	J5	L	White	SYNC10-2D2
J5	L	J11	L	↓	SYNC10-1D2
J1	P	J19	L	↓	SYNC10-4D2
J19	L	J25	L	↓	SYNC10-3D2
J1	14	J4	L	White	SYNC11-2E2
J4	L	J10	L	↓	SYNC11-1E2
J1	14	J18	L	↓	SYNC11-4E2
J18	L	J24	L	↓	SYNC11-3E2
J1	R	J3	L	White	SYNC12-2F2
J3	L	J9	L	↓	SYNC12-1F2
J1	R	J17	L	↓	SYNC12-4F2
J17	L	J23	L	↓	SYNC12-3F2
J1	15	J8	11	White	SYNC13-2A3
J8	11	J14	11	↓	SYNC13-1A3
J1	15	J22	11	↓	SYNC13-4A3
J22	11	J28	11	↓	SYNC13-3A3
J1	S	J7	11	White	SYNC14-2B3
J7	11	J13	11	↓	SYNC14-1B3
J1	S	J21	11	↓	SYNC14-4B3
J21	11	J27	11	↓	SYNC14-3B3
J1	16	J6	11	White	SYNC15-2C3
J6	11	J12	11	↓	SYNC15-1C3
J1	16	J20	11	↓	SYNC15-4C3
J20	11	J26	11	↓	SYNC15-3C3
J1	T	J5	11	White	SYNC16-2D3
J5	11	J11	11	↓	SYNC16-1D3
J1	T	J19	11	↓	SYNC16-4D3
J19	11	J25	11	↓	SYNC16-3D3
J1	17	J4	11	White	SYNC17-2E3
J4	11	J10	11	↓	SYNC17-1E3
J1	17	J18	11	↓	SYNC17-4E3
J18	11	J24	11	↓	SYNC17-3E3

BACKPLANE WIRE LIST - TRANSMITTER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J1	U	J3	11	White	SYNC18-2F3
J3	11	J9	11	↓	SYNC18-1F3
J1	U	J17	11	↓	SYNC18-4F3
J17	11	J23	11	↓	SYNC18-3F3
J1	18	J8	M	White	SYNC19-2A4
J8	M	J14	M	↓	SYNC19-1A4
J1	18	J22	M	↓	SYNC19-4A4
J22	M	J28	M	↓	SYNC19-3A4
J1	V	J7	M	White	SYNC20-2B4
J7	M	J13	M	↓	SYNC20-1B4
J1	V	J21	M	↓	SYNC20-4B4
J21	M	J27	M	↓	SYNC20-3B4
J1	19	J6	M	White	SYNC21-2C4
J6	M	J12	M	↓	SYNC21-1C4
J1	19	J20	M	↓	SYNC21-4C4
J20	M	J26	M	↓	SYNC21-3C4
J1	W	J5	M	White	SYNC22-2D4
J5	M	J11	M	↓	SYNC22-1D4
J1	W	J19	M	↓	SYNC22-4D4
J19	M	J25	M	↓	SYNC22-3D4
J1	20	J4	M	White	SYNC23-2E4
J4	M	J10	M	↓	SYNC23-1E4
J1	20	J18	M	↓	SYNC23-4E4
J18	M	J24	M	↓	SYNC23-3E4
J1 *	8 *	J2 *	K *	Yellow *	12 Mbps Biphase Data
J2 *	9 *	BNC Back Panel		Coax	MUX Out
J1	8	Connector			
J2 *	10 *	BNC Back Panel		Coax	Ground
J1	5	Connector		Shield	
J2	7	Front Panel LED	Anode	Violet	Bit Stream Indicator
J2	8	Front Panel LED	Cathode	Green	Bit Stream Indicator

* Applicable to Serial Unit No. 1 Only

BACKPLANE WIRE LIST - TRANSMITTER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J9	C	BNC Back Panel Connector		Coax	FIDU
J9	8	BNC Back Panel Connector		Green	CAL
BNC Back Panel Connector		F/O Board Connector	7,20	Coax	F/O XMIT IN
BNC Back Panel Connector		F/O Board Connector	9,K,22,Z	Coax Shield	Ground
+5V Power Supply (+)		J1	1,2,A,B		
J1	1,2,A,B	J2		Red	+5V
J2		J3		Bus Wire	
J3		J4			
J4		J5			
J5		J6			
J6		J7			
J7		J8			
J8		J9			
J9		J10			
J10		J11			
J11		J12			
J12		J13			
J13		J14			
+5V Power Supply (+)		J15		Red	
J15	1,2,A,B	J16		Bus Wire	
J16		J17			
J17		J18			
J18		J19			
J19		J20			
J20		J21			
J21		J22			
J22		J23			
J23		J24			
J24		J25			
J25		J26			
J26		J27			
J27		J28			
J1	1,2,A,B	F/O Board Connector	1,A,14,R	Red	+5V
J15	1,2,A,B	Front Panel LED	Anode	Red	+5V Indicator

BACKPLANE WIRE LIST - TRANSMITTER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
+7.5V Power Supply (+)		J14	5	Orange	+7.5V
J14	5	J13		Bus Wire	
J13		J12			
J12		J11			
J11		J10			
J10		J9			
J9		J8			
J8		J7			
J7		J6			
J6		J5			
J5		J4			
J4		J3			
+7.5V Power Supply (+)		J28		Orange	+7.5V
J28	5	J27		Bus Wire	
J27		J26			
J26		J25			
J25		J24			
J24		J23			
J23		J22			
J22		J21			
J21		J20			
J20		J19			
J19		J18			
J18		J17			
J17		J16			
J16		J15			
+7.5V Power Supply (S)		J15	5	Orange	+7.5V
J16	5	Front Panel LED	Anode	Yellow	+7.5V Indicator
-7.5V Power Supply (-)		J14	E	Blue	-7.5V
J14	E	J13		Bus Wire	
J13		J12			
J12		J11			
J11		J10			
J10		J9			
J9		J8			
J8		J7			
J7		J6			
J6		J5			
J5		J4			
J4		J3			
-7.5V Power Supply (-)		J28	E	Blue	-7.5V
J28	E	J27		Bus Wire	
J27		J26			
J26		J25			

BACKPLANE WIRE LIST - TRANSMITTER

CONNECTOR	PIN	CONNECTOR	PIN	COLOR	SIGNAL
J25	E	J24	E	Blue	-7.5V
J24	↓	J23	↓	Bus Wire	↓
J23	↓	J22	↓	↓	↓
J22	↓	J21	↓	↓	↓
J21	↓	J20	↓	↓	↓
J20	↓	J19	↓	↓	↓
J19	↓	J18	↓	↓	↓
J18	↓	J17	↓	↓	↓
J17	↓	J16	↓	↓	↓
J16	↓	J15	↓	↓	↓
-7.5V Power Supply (S)		J15	E	Blue	-7.5V
J16	E	Front Panel LED	Cathode	Red	-7.5V Indicator
J15	7	J3	7	Red	+3V
J3	↓	J4	↓	Bus Wire	↓
J4	↓	J5	↓	↓	↓
J5	↓	J6	↓	↓	↓
J6	↓	J7	↓	↓	↓
J7	↓	J8	↓	↓	↓
J8	↓	J9	↓	↓	↓
J9	↓	J10	↓	↓	↓
J10	↓	J11	↓	↓	↓
J11	↓	J12	↓	↓	↓
J12	↓	J13	↓	↓	↓
J13	↓	J14	↓	↓	↓
J15	↓	J16	↓	↓	↓
J16	↓	J17	↓	↓	↓
J17	↓	J18	↓	↓	↓
J18	↓	J19	↓	↓	↓
J19	↓	J20	↓	↓	↓
J20	↓	J21	↓	↓	↓
J21	↓	J22	↓	↓	↓
J22	↓	J23	↓	↓	↓
J23	↓	J24	↓	↓	↓
J24	↓	J25	↓	↓	↓
J25	↓	J26	↓	↓	↓
J26	↓	J27	↓	↓	↓
J27	↓	J28	↓	↓	↓
J16	7	Front Panel LED	Anode	Green	+3V Indicator
J15	H	J3	H	Yellow	-3V
J3	↓	J4	↓	↓	↓
J4	↓	J5	↓	↓	↓
J5	↓	J6	↓	↓	↓
J6	↓	J7	↓	↓	↓

BACKPLANE WIRE LIST - TRANSMITTER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J7	H	J8	H	Yellow	-3V
J8		J9		Bus Wire	
J9		J10			
J10		J11			
J11		J12			
J12		J13			
J13		J14			
J15		J16			
J16		J17			
J17		J18			
J18		J19			
J19		J20			
J20		J21			
J21		J22			
J22		J23			
J23		J24			
J24		J25			
J25		J26			
J26		J27			
J27		J28			
J16	H	Front Panel LED	Cathode	Blue	-3V Indicator
5V Power Supply (-)		J1	21,22,Y,Z	Black	Ground
+7.5V Power Supply (-)		J1	21,22,Y,Z	Black	Ground
-7.5V Power Supply (+)		J1	21,22,Y,Z	Black	Ground
J1	21,22,Y,Z	J2	21,22,Y,Z	Bus Wire	Ground
J2		J3			
J3		J4			
J4		J5			
J5		J6			
J6		J7			
J7		J8			
J8		J9			
J9		J10			
J10		J11			
J11		J12			
J12		J13			
J13		J14			
5V Power Supply (-)		J15	21,22,Y,Z	Black	Ground
+7.5V Power Supply (-)		J15	21,22,Y,Z	Black	Ground
-7.5V Power Supply (+)		J15	21,22,Y,Z	Black	Ground
J15	21,22,Y,Z	J16	21,22,Y,Z	Bus Wire	Ground
J16		J17			
J17		J18			
J18		J19			
J19		J20			
J20		J21			

BACKPLANE WIRE LIST - TRANSMITTER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J21	21,22,Y,Z	J22	21,22,Y,Z	Bus Wire	Ground
J22	↓	J23	↓	↓	↓
J23		J24			
J24		J25			
J25		J26			
J26		J27			
J27		J28			
J15	21,22,Y,Z	Front Panel LED	Cathode	Black	+5V,+7V,+3V Indicator Ground
J15	21,22,Y,Z	Front Panel LED	Anode	Black	-7V,-3V Indicator Ground
J1	21,22,Y,Z	F/O Board Connector	9,K,22,Z	Black	Ground

BACKPLANE WIRE LIST - TRANSMITTER

BACK PANEL BNC CONNECTOR	CONNECTOR	PIN	CABLE	SIGNAL ANALOG IN
1A1	J14	13	Coax*	1A1
1A2	J14	16		1A2
1A3	J14	19		1A3
1A4	J14	20		1A4
1B1	J13	13		1B1
1B2	J13	16		1B2
1B3	J13	19		1B3
1B4	J13	20		1B4
1C1	J12	13		1C1
1C2	J12	16		1C2
1C3	J12	19		1C3
1C4	J12	20		1C4
1D1	J11	13		1D1
1D2	J11	16		1D2
1D3	J11	19		1D3
1D4	J11	20		1D4
1E1	J10	13		1E1
1E2	J10	16		1E2
1E3	J10	19		1E3
1E4	J10	20		1E4
1F1	J9	13		1F1
1F2	J9	16		1F2
1F3	J9	19		1F3
2A1	J8	13		2A1
2A2	J8	16		2A2
2A3	J8	19		2A3
2A4	J8	20		2A4
2B1	J7	13		2B1
2B2	J7	16		2B2
2B3	J7	19		2B3
2B4	J7	20		2B4
2C1	J6	13		2C1
2C2	J6	16		2C2
2C3	J6	19		2C3
2C4	J6	20		2C4
2D1	J5	13		2D1
2D2	J5	16		2D2
2D3	J5	19		2D3
2D4	J5	20		2D4
2E1	J4	13		2E1
2E2	J4	16		2E2
2E3	J4	19		2E3
2E4	J4	20		2E4
2F1	J3	13		2F1
2F2	J3	16		2F2
2F3	J3	19		2F3

*Coax shields are connected only to back panel connectors.

BACKPLANE WIRE LIST - TRANSMITTER

BACK PANEL BNC CONNECTOR	CONNECTOR	PIN	CABLE	SIGNAL ANALOG IN
3A1	J28	13	Coax*	3A1
3A2	J28	16		3A2
3A3	J28	19		3A3
3A4	J28	20		3A4
3B1	J27	13		3B1
3B2	J27	16		3B2
3B3	J27	19		3B3
3B4	J27	20		3B4
3C1	J26	13		3C1
3C2	J26	16		3C2
3C3	J26	19		3C3
3C4	J26	20		3C4
3D1	J25	13		3D1
3D2	J25	16		3D2
3D3	J25	19		3D3
3D4	J25	20		3D4
3E1	J24	13		3E1
3E2	J24	16		3E2
3E3	J24	19		3E3
3E4	J24	20		3E4
3F1	J23	13		3F1
3F2	J23	16		3F2
3F3	J23	19		3F3
4A1	J22	13		4A1
4A2	J22	16		4A2
4A3	J22	19		4A3
4A4	J22	20		4A4
4B1	J21	13		4B1
4B2	J21	16		4B2
4B3	J21	19		4B3
4B4	J21	20		4B4
4C1	J20	13		4C1
4C2	J20	16		4C2
4C3	J20	19		4C3
4C4	J20	20		4C4
4D1	J19	13		4D1
4D2	J19	16		4D2
4D3	J19	19		4D3
4D4	J19	20		4D4
4E1	J18	13		4E1
4E2	J18	16		4E2
4E3	J18	19		4E3
4E4	J18	20		4E4
4F1	J17	13		4F1
4F2	J17	16		4F2
4F3	J17	19		4F3

* Coax shields are connected only to back panel connectors.

6.9 BACKPLANE WIRE LIST - RECEIVER

CONNECTOR	PIN	CONNECTOR	PIN	COLOR	SIGNAL
J1	E	J3	9	Violet	3MHz Clock
J3	9	J4	9	Bus Wire	
J4	9	J5	9		
J5	9	J6	9		
J6	9	J7	9		
J7	9	J8	9		
J8	9	J9	9		
J9	9	J10	9		
J10	9	J11	9		
J11	9	J12	9		
J12	9	J13	9		
J13	9	J14	9		
J1	E	J17	9	Violet	
J17	9	J18	9	Bus Wire	
J18	9	J19	9		
J19	9	J20	9		
J20	9	J21	9		
J21	9	J22	9		
J22	9	J23	9		
J23	9	J24	9		
J24	9	J25	9		
J25	9	J26	9		
J26	9	J27	9		
J27	9	J28	9		
J1	F	J9	K	Blue	Group 1 Digital Data
J9	K	J10	K	Bus Wire	
J10	K	J11	K		
J11	K	J12	K		
J12	K	J13	K		
J13	K	J14	K		
J1	6	J3	K	Blue	Group 2 Digital Data
J3	K	J4	K	Bus Wire	
J4	K	J5	K		
J5	K	J6	K		
J6	K	J7	K		
J7	K	J8	K		
J1	H	J23	K	Blue	Group 3 Digitial Data
J23	K	J24	K	Bus Wire	
J24	K	J25	K		
J25	K	J26	K		
J26	K	J27	K		
J27	K	J28	K		

BACKPLANE LIST - RECEIVER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J1	7	J17	K	Blue	Group 4 Digital Data
J17	K	J18	K	Bus Wire	↓
J18	K	J19	K	↓	
J19	K	J20	K		
J20	K	J21	K		
J21	K	J22	K		
J1	9	J8	10	White	SYNC1-2A1
J8	10	J14	10	↓	SYNC1-1A1
J1	9	J22	10		SYNC1-4A1
J22	10	J28	10		SYNC1-3A1
J1	K	J7	10	White	SYNC2-2B1
J7	10	J13	10	↓	SYNC2-1B1
J1	K	J21	10		SYNC2-4B1
J21	10	J27	10		SYNC2-3B1
J1	10	J6	10	White	SYNC3-2C1
J6	10	J12	10	↓	SYNC3-1C1
J1	10	J20	10		SYNC3-4C1
J20	10	J26	10		SYNC3-3C1
J1	L	J5	10	White	SYNC4-2D1
J5	10	J11	10	↓	SYNC4-1D1
J1	L	J19	10		SYNC4-4D1
J19	10	J25	10		SYNC4-3D1
J1	11	J4	10	White	SYNC5-2E1
J4	10	J10	10	↓	SYNC5-1E1
J1	11	J18	10		SYNC5-4E1
J18	10	J24	10		SYNC5-3E1
J1	M	J3	10	White	SYNC6-2F1
J3	10	J9	10	↓	SYNC6-1F1
J1	M	J17	10		SYNC6-4F1
J17	10	J23	10		SYNC6-3F1
J1	12	J8	L	White	SYNC7-2A2
J8	L	J14	L	↓	SYNC7-1A2
J1	12	J22	L		SYNC7-4A2
J22	L	J28	L		SYNC7-3A2
J1	N	J7	L	White	SYNC8-2B2
J7	L	J13	L	↓	SYNC8-1B2
J1	N	J21	L		SYNC8-4B2
J21	L	J27	L		SYNC8-3B2

BACKPLANE WIRE LIST - RECEIVER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J1	13	J6	L	White	SYNC9-2C2
J6	L	J12	L	↓	SYNC9-1C2
J1	13	J20	L	↓	SYNC9-4C2
J20	L	J26	L	↓	SYNC9-3C2
J1	P	J5	L	White	SYNC10-2D2
J5	L	J11	L	↓	SYNC10-1D2
J1	P	J19	L	↓	SYNC10-4D2
J19	L	J25	L	↓	SYNC10-3D2
J1	14	J4	L	White	SYNC11-2E2
J4	L	J10	L	↓	SYNC11-1E2
J1	14	J18	L	↓	SYNC11-4E2
J18	L	J24	L	↓	SYNC11-3E2
J1	R	J3	L	White	SYNC12-2F2
J3	L	J9	L	↓	SYNC12-1F2
J1	R	J17	L	↓	SYNC12-4F2
J17	L	J23	L	↓	SYNC12-3F2
J1	15	J8	11	White	SYNC13-2A3
J8	11	J14	11	↓	SYNC13-1A3
J1	15	J22	11	↓	SYNC13-4A3
J22	11	J28	11	↓	SYNC13-3A3
J1	S	J7	11	White	SYNC14-2B3
J7	11	J13	11	↓	SYNC14-1B3
J1	S	J21	11	↓	SYNC14-4B3
J21	11	J27	11	↓	SYNC14-3B3
J1	16	J6	11	White	SYNC15-2C3
J6	11	J12	11	↓	SYNC15-1C3
J1	16	J20	11	↓	SYNC15-4C3
J20	11	J26	11	↓	SYNC15-3C3
J1	T	J5	11	White	SYNC16-2D3
J5	11	J11	11	↓	SYNC16-1D3
J1	T	J19	11	↓	SYNC16-4D3
J19	11	J25	11	↓	SYNC16-3D3
J1	17	J4	11	White	SYNC17-2E3
J4	11	J10	11	↓	SYNC17-1E3
J1	17	J18	11	↓	SYNC17-4E3
J18	11	J24	11	↓	SYNC17-3E3

BACKPLANE WIRE LIST - RECEIVER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J1	U	J3	11	White	SYNC18-2F3
J3	11	J9	11	↓	SYNC18-1F3
J1	U	J17	11	↓	SYNC18-4F3
J17	11	J23	11	↓	SYNC18-3F3
J1	18	J8	M	White	SYNC19-2A4
J8	M	J14	M	↓	SYNC19-1A4
J1	18	J22	M	↓	SYNC19-4A4
J22	M	J28	M	↓	SYNC19-3A4
J1	V	J7	M	White	SYNC20-2B4
J7	M	J13	M	↓	SYNC20-1B4
J1	V	J21	M	↓	SYNC20-4B4
J21	M	J27	M	↓	SYNC20-3B4
J1	19	J6	M	White	SYNC21-2C4
J6	M	J12	M	↓	SYNC21-1C4
J1	19	J20	M	↓	SYNC21-4C4
J20	M	J26	M	↓	SYNC21-3C4
J1	W	J5	M	White	SYNC22-2D4
J5	M	J11	M	↓	SYNC22-1D4
J1	W	J19	M	↓	SYNC22-4D4
J19	M	J25	M	↓	SYNC22-3D4
J1	20	J4	M	White	SYNC23-2E4
J4	M	J10	M	↓	SYNC23-1E4
J1	20	J18	M	↓	SYNC23-4E4
J18	M	J24	M	↓	WYNC23-3E4

BACKPLANE WIRE LIST - RECEIVER

FROM CONNECTOR	PIN	TO CONNECTOR	PIN	COLOR	SIGNAL
BNC Back Panel Connector		J1	8	Coax	DEMUX IN
BNC Back Panel Connector		J1	J	Coax Shield	Ground
J1	C	J2	C	Yellow	3MHz Clock
J2	3	BNC Back Panel Connector		Coax	3MHz Clock Out
J2	4	BNC Back Panel Connector		Coax Shield	Ground
J1	C	J1	D	Bus Wire	3MHz Clock for SYNC Counters
J1	F	J2	H	Blue	Group 1 Data
J2	7	BNC Back Panel Connector		Coax	Group 1 Data Out
J2	8	BNC Back Panel Connector		Coax Shield	Ground
J1	6	J2	K	Blue	Group 2 Data
J2	9	BNC Back Panel Connector		Coax	Group 2 Data Out
J2	10	BNC Back Panel Connector		Coax Shield	Ground
J1	H	J2	M	Blue	Group 3 Data
J2	11	BNC Back Panel Connector		Coax	Group 3 Data Out
J2	12	BNC Back Panel Connector		Coax Shield	Ground
J1	7	J2	P	Blue	Group 4 Data
J2	13	BNC Back Panel Connector		Coax	Group 4 Data Out
J2	14	BNC Back Panel Connector		Coax Shield	Ground

BACKPLANE WIRE LIST - RECEIVER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
F/O Board Connector	7	J2	S	Violet	12Mbps Biphase Data
F/O Board Connector	20	J2	U	Violet	12Mbps Biphase Data
J2	5	BNC Back Panel Connector		Coax	F/O Receive Out
J2	6	BNC Back Panel Connector		Coax Shield	Ground
J2	17	Front Panel LED	Anode	Violet	Bitstream Indicator
J2	18	Front Panel LED	Cathode	Green	Bitstream Indicator
+5V Power Supply (+)		J1	1,2,A,B	Red	+5V
J1	1,2,A,B	J2		Bus Wire	
J2		J3			
J3		J4			
J4		J5			
J5		J6			
J6		J7			
J7		J8			
J8		J9			
J9		J10			
J10		J11			
J11		J12			
J12		J13			
J13		J14			
+5V Power Supply (+)		J15		Red	
J15	1,2,A,B	J16		Bus Wire	
J16		J17			
J17		J18			
J18		J19			
J19		J20			
J20		J21			
J21		J22			
J22		J23			
J23		J24			
J24		J25			
J25		J26			
J26		J27			
J27		J28			
J1	1,2,A,B	F/O Board Connector	1,A,14,R	Red	+5V
J15	1,2,A,B	Front Panel LED	Anode	Red	+5V Indicator

BACKPLANE WIRE LIST - RECEIVER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
+7.5V Power Supply (+)		J14	5	Orange Bus Wire	+7.5V
J14	5	J13			
J13		J12			
J12		J11			
J11		J10			
J10		J9			
J9		J8			
J8		J7			
J7		J6			
J6		J5			
J5		J4			
J4		J3			
+7.5V Power Supply (+)		J28		Orange Bus Wire	+7.5V
J28	5	J27			
J27		J26			
J26		J25			
J25		J24			
J24		J23			
J23		J22			
J22		J21			
J21		J20			
J20		J19			
J19		J18			
J18		J17			
J17		J16			
J16		J15			
+7.5V Power Supply (S)		J15	5	Orange Yellow	+7.5V +7.5V Indicator
J16	5	Front Panel LED	Anode		
-7.5V Power Supply (-)		J14	E	Blue Bus Wire	-7.5V
J14	E	J13			
J13		J12			
J12		J11			
J11		J10			
J10		J9			
J9		J8			
J8		J7			
J7		J6			
J6		J5			
J5		J4			
J4		J3			
-7.5V Power Supply (-)		J28	E	Blue Bus Wire	-7.5V
J28	E	J27			
J27		J26			
J26		J25			
J25		J26			

BACKPLANE WIRE LIST - RECEIVER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J25	E	J24	E	Blue	-7.5V
J24	↓	J23	↓	Bus Wire	↓
J23		J22		↓	
J22		J21			
J21		J20			
J20		J19			
J19		J18			
J18		J17			
J17		J16			
J16	↓	J15	↓	↓	↓
-7.5V Power Supply (S)		J15	E	Blue	-7.5V
J16	E	Front Panel LED	Cathode	Red	-7.5V Indicator
J15	7	J3	7	Red	+3V
J3	↓	J4	↓	Bus Wire	↓
J4		J5		↓	
J5		J6			
J6		J7			
J7		J8			
J8		J9			
J9		J10			
J10		J11			
J11		J12			
J12		J13			
J13		J14			
J15		J16			
J16		J17			
J17		J18			
J18		J19			
J19		J20			
J20		J21			
J21		J22			
J22		J23			
J23		J24			
J24		J25			
J25		J26			
J26		J27			
J27	↓	J28	↓	↓	↓
J16	7	Front Panel LED	Anode	Green	+3V Indicator
J15	H	J3	H	Yellow	+3V
J3	↓	J4	↓	Bus Wire	↓
J4		J5		↓	
J5		J6			
J6	↓	J7	↓	↓	↓

BACKPLANE WIRE LIST - RECEIVER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J7	H	J8	H	Yellow	-3V
J8	↓	J9	↓	Bus Wire	↓
J9	↓	J10	↓	↓	↓
J10	↓	J11	↓	↓	↓
J11	↓	J12	↓	↓	↓
J12	↓	J13	↓	↓	↓
J13	↓	J14	↓	↓	↓
J14	↓	J15	↓	↓	↓
J15	↓	J16	↓	↓	↓
J16	↓	J17	↓	↓	↓
J17	↓	J18	↓	↓	↓
J18	↓	J19	↓	↓	↓
J19	↓	J20	↓	↓	↓
J20	↓	J21	↓	↓	↓
J21	↓	J22	↓	↓	↓
J22	↓	J23	↓	↓	↓
J23	↓	J24	↓	↓	↓
J24	↓	J25	↓	↓	↓
J25	↓	J26	↓	↓	↓
J26	↓	J27	↓	↓	↓
J27	↓	J28	↓	↓	↓
J16	H	Front Panel LED	Cathode	Blue	-3V Indicator
±15V Power Supply (+)		F/O Board Connector	3,16	Red	+15V
±15V Power Supply (-)		F/O Board Connector	5,18	Blue	-15V
5V Power Supply (-)		J1	21,22,Y,Z	Black	Ground
+7.5V Power Supply (-)		J1	21,22,Y,Z	Black	Ground
-7.5V Power Supply (+)		J1	21,22,Y,Z	Black	Ground
J1	21,22,Y,Z	J2	21,22,Y,Z	Bus Wire	Ground
J2	↓	J3	↓	↓	↓
J3	↓	J4	↓	↓	↓
J4	↓	J5	↓	↓	↓
J5	↓	J6	↓	↓	↓
J6	↓	J7	↓	↓	↓
J7	↓	J8	↓	↓	↓
J8	↓	J9	↓	↓	↓
J9	↓	J10	↓	↓	↓
J10	↓	J11	↓	↓	↓
J11	↓	J12	↓	↓	↓
J12	↓	J13	↓	↓	↓
J13	↓	J14	↓	↓	↓
5V Power Supply (-)		J15	21,22,Y,Z	Black	Ground
+7.5V Power Supply (-)		J15	21,22,Y,Z	Black	Ground
-7.5V Power Supply (+)		J15	21,22,Y,Z	Black	Ground

BACKPLANE WIRE LIST - RECEIVER

FROM		TO		COLOR	SIGNAL
CONNECTOR	PIN	CONNECTOR	PIN		
J15	21,22,Y,Z	J16	21,22,Y,Z	Bus Wire	Ground
J16	↓	J17	↓	↓	↓
J17	↓	J18	↓	↓	↓
J18	↓	J19	↓	↓	↓
J19	↓	J20	↓	↓	↓
J20	↓	J21	↓	↓	↓
J21	↓	J22	↓	↓	↓
J22	↓	J23	↓	↓	↓
J23	↓	J24	↓	↓	↓
J24	↓	J25	↓	↓	↓
J25	↓	J26	↓	↓	↓
J26	↓	J27	↓	↓	↓
J27	↓	J28	↓	↓	↓
J15	21,22,Y,Z	Front Panel LED	Cathode	Black	+5V,+7V,+3V Indicator Ground
J15	21,22,Y,Z	Front Panel LED	Anode	Black	-7V,-3V Indicator Ground
J1	21,22,Y,Z	F/O Board Connector	9,K,22,Z	Black	Ground
±15V Power Supply Ground		F/O Board Connector	9,K,22,Z	Black	Ground

BACKPLANE WIRE LIST - RECEIVER

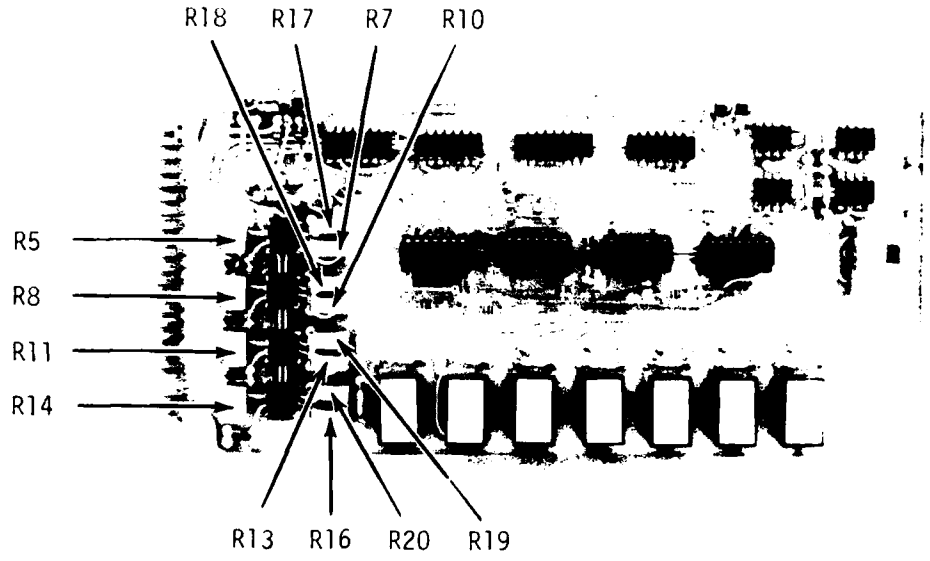
FROM		TO	CABLE	SIGNAL
CONNECTOR	PIN	BACK PANEL CONNECTOR		ANALOG OUT
J14	13	1A1	Coax*	1A1
J14	16	1A2		1A2
J14	19	1A3		1A3
J14	20	1A4		1A4
J13	13	1B1		1B1
J13	16	1B2		1B2
J13	19	1B3		1B3
J13	20	1B4		1B4
J12	13	1C1		1C1
J12	16	1C2		1C2
J12	19	1C3		1C3
J12	20	1C4		1C4
J11	13	1D1		1D1
J11	16	1D2		1D2
J11	19	1D3		1D3
J11	20	1D4		1D4
J10	13	1E1		1E1
J10	16	1E2		1E2
J10	19	1E3		1E3
J10	20	1E4		1E4
J9	13	1F1		1F1
J9	16	1F2		1F2
J9	19	1F3		1F3
J8	13	2A1		2A1
J8	16	2A2		2A2
J8	19	2A3		2A3
J8	20	2A4		2A4
J7	13	2B1		2B1
J7	16	2B2		2B2
J7	19	2B3		2B3
J7	20	2B4		2B4
J6	13	2C1		2C1
J6	16	2C2		2C2
J6	19	2C3		2C3
J6	20	2C4		2C4
J5	13	2D1		2D1
J5	16	2D2		2D2
J5	19	2D3		2D3
J5	20	2D4		2D4
J4	13	2E1		2E1
J4	16	2E2		2E2
J4	19	2E3		2E3
J4	20	2E4		2E4
J3	13	2F1		2F1
J3	16	2F2		2F2
J3	19	2F3		2F3

* Coax shields are connected only to the back panel connectors

BACKPLANE WIRE LIST - RECEIVER

FROM		TO	CABLE	SIGNAL
CONNECTOR	PIN	BACK PANEL CONNECTOR		ANALOG OUT
J28	13	3A1	Coax*	3A1
J28	16	3A2		3A2
J28	19	3A3		3A3
J28	20	3A4		3A4
J27	13	3B1		3B1
J27	16	3B2		3B2
J27	19	3B3		3B3
J27	20	3B4		3B4
J26	13	3C1		3C1
J26	16	3C2		3C2
J26	19	3C3		3C3
J26	20	3C4		3C4
J25	13	3D1		3D1
J25	16	3D2		3D2
J25	19	3D3		3D3
J25	20	3D4		3D4
J24	13	3E1		3E1
J24	16	3E2		3E2
J24	19	3E3		3E3
J24	20	3E4		3E4
J23	13	3F1		3F1
J23	16	3F2		3F2
J23	19	3F3		3F3
J22	13	4A1		4A1
J22	16	4A2		4A2
J22	19	4A3		4A3
J22	20	4A4		4A4
J21	13	4B1		4B1
J21	16	4B2		4B2
J21	19	4B3		4B3
J21	20	4B4		4B4
J20	13	4C1		4C1
J20	16	4C2		4C2
J20	19	4C3		4C3
J20	20	4C4		4C4
J19	13	4D1		4D1
J19	16	4D2		4D2
J19	19	4D3		4D3
J19	20	4D4		4D4
J18	13	4E1		4E1
J18	16	4E2		4E2
J18	19	4E3		4E3
J18	20	4E4		4E4
J17	13	4F1		4F1
J17	16	4F2		4F2
J17	19	4F3		4F3

* Coax Shields are connected only to the back panel connectors.



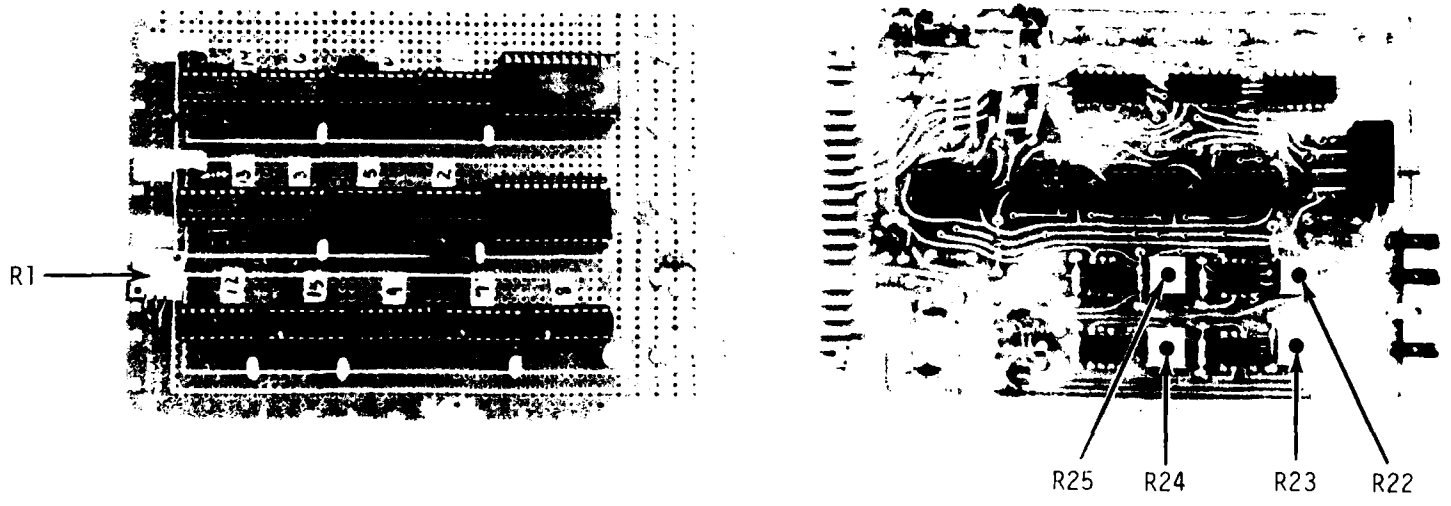
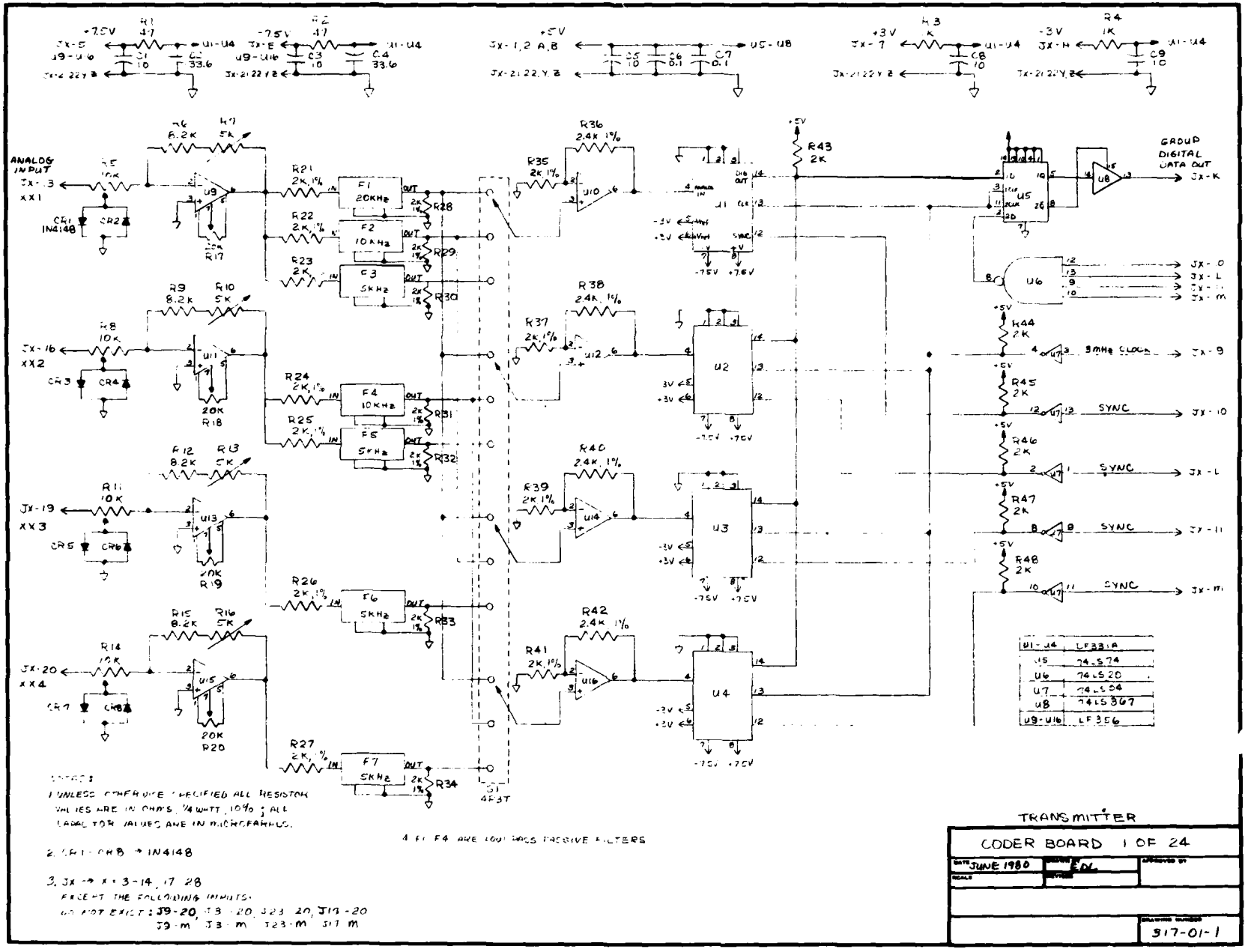
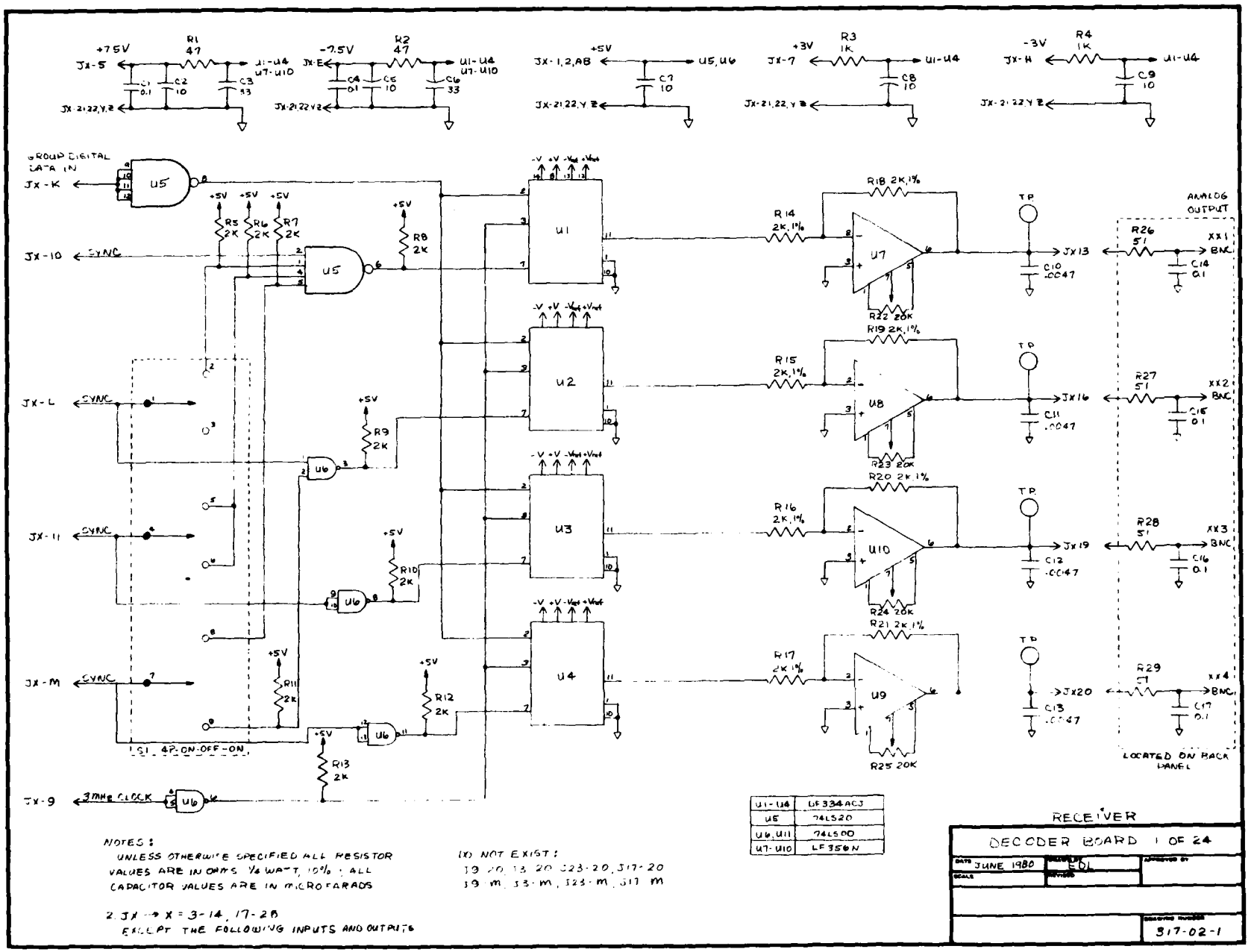


Diagram 6.10 Layout of Coder, Decoder, and Demultiplexer Boards

6.11 SCHEMATICS

Description	Drawing Number
1. Coder Board	317-01-1
2. Decoder Board	317-02-1
3. Multiplexer Board	317-03-1
4. Demultiplexer Board	317-04-1
5. Line Driver-Transmitter	317-05-1
6. Line Driver-Receiver	317-06-1
7. ±3 Volt Power Supply	317-07-1
8. Chassis Wiring - Transmitter	317-08-1
9. Chassis Wiring - Receiver	317-09-1
10. Fiber Optic Transmitter Board	317-10-1
11. Fiber Optic Receiver Board - Spectronics	317-11-1
12. Fiber Optic Receiver Board - Maxlight	317-12-1
13. Fiber Optic Receiver Board - Meret	317-13-1
14. Computer Interface Board	317-14-1


ANALOG INPUT
JX-3
XX1
JX-16
XX2
JX-19
XX3
JX-20
XX4
CR1 IN4148
F1 20KHz
F2 10KHz
F3 5KHz
F4 10KHz
F5 5KHz
F6 5KHz
F7 5KHz
4PST
R43 2K
R44 2K
R45 2K
R46 2K
R47 2K
R48 2K
5MHz CLOCK
SYNC
GROUP DIGITAL DATA OUT
JX-K
JX-0
JX-L
JX-M
JX-9
JX-10
JX-L
JX-11
JX-M
U1-U4 LF3314
U5 74LS74
U6 74LS20
U7 74LS04
U8 74LS367
U9-U16 LF356
NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS, ¼WATT, 10%; ALL LABELED VALUES ARE IN MICROFARADS.
2. CR1 - CR8 = IN4148
3. JX → X = 3-14, 17 28
EXCEPT THE FOLLOWING INPUTS:
DO NOT EXIST: J9-20, J13-20, J23-20, J17-20
J9-M J13-M J23-M J17-M
4 F1 F4 ARE 100 HOS PASSIVE FILTERS
TRANSMITTER
CODER BOARD 1 OF 24
JUNE 1980
917-01-1



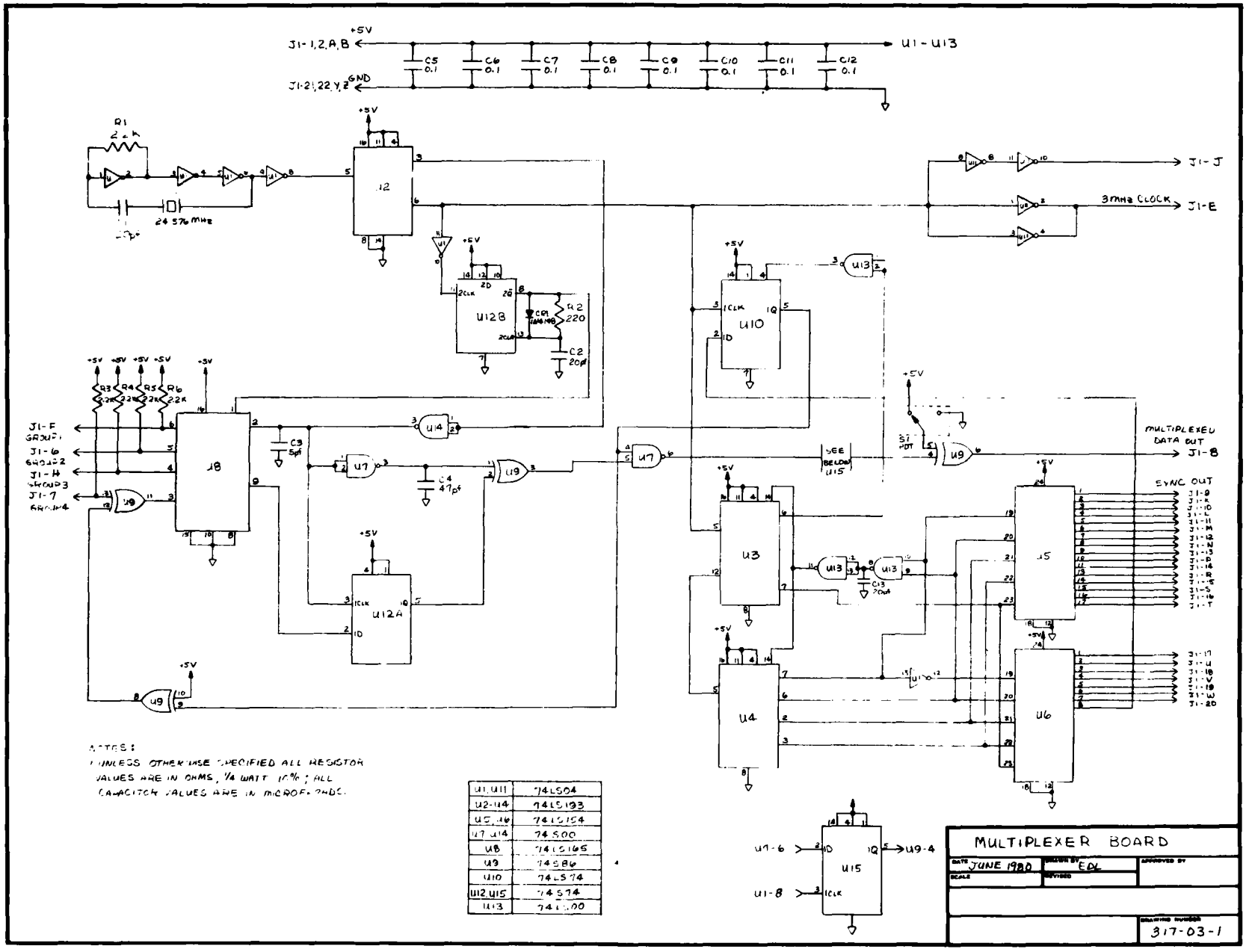
U1-U4	LF334ACJ
U5	74LS20
U6, U11	74LS00
U7-U10	LF356N

NOTES:
UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS ¼ WATT, 10% ; ALL CAPACITOR VALUES ARE IN MICROFARADS

2. Jx → X = 3-14, 17-28
EXCEPT THE FOLLOWING INPUTS AND OUTPUTS

(X) NOT EXIST:
J9, J20, J3, J20, J23-20, J17-20
J9-M, J3-M, J23-M, J17-M

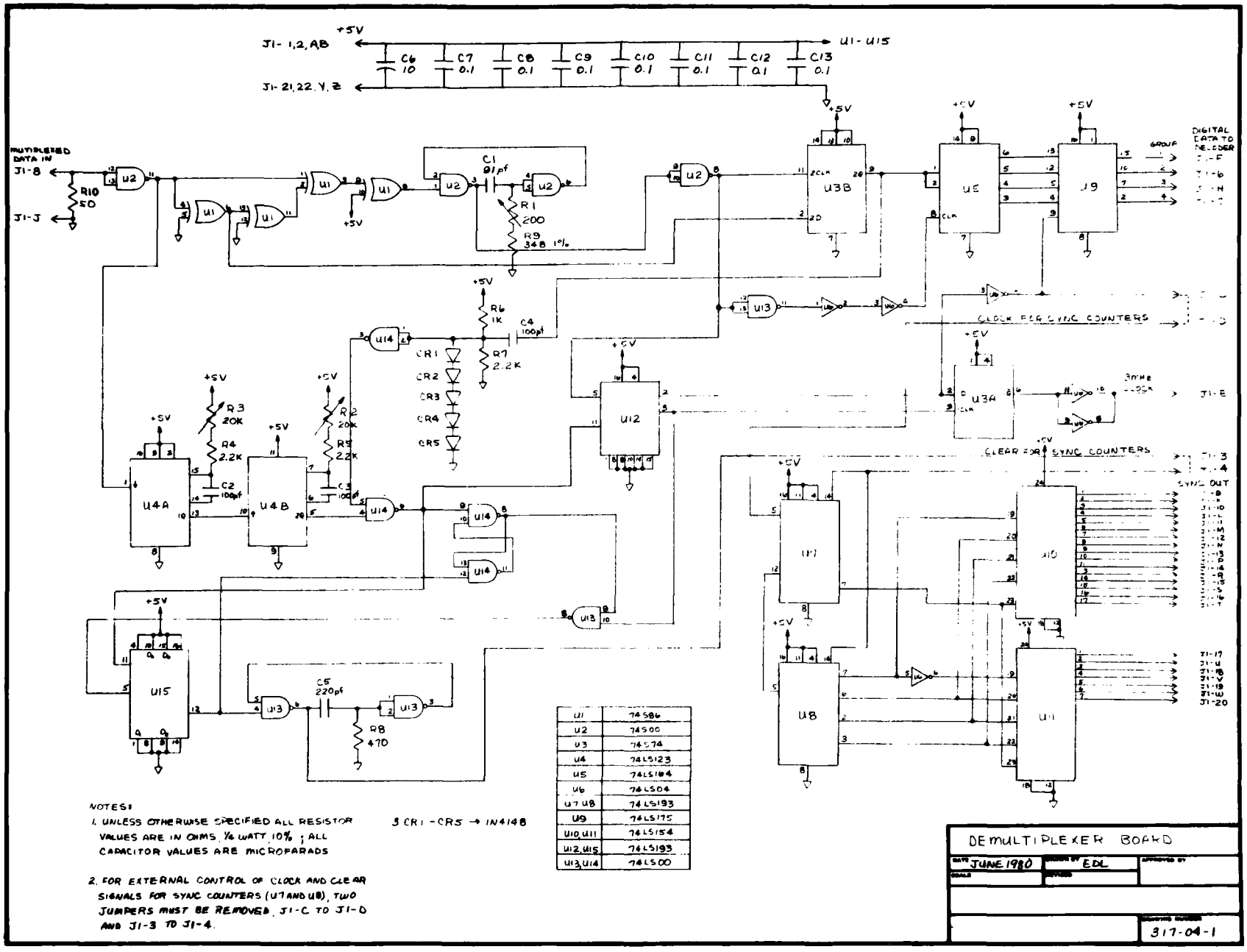
RECEIVER
DECODER BOARD 1 OF 24
DATE JUNE 1980
DRAWING NUMBER 317-02-1



NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS, 1/4 WATT 10%; ALL CAPACITOR VALUES ARE IN MICROFARADS.

U1, U11	74LS04
U2-U4	74LS193
U5, U6	74LS154
U7, U14	74S00
U8	74LS165
U9	74S86
U10	74LS74
U12, U15	74S74
U13	74[illegible]00

MULTIPLEXER BOARD	
DATE JUNE 1980	DRAWN BY EDL
SCALE	REVISED
APPROVED BY	
DRAWING NUMBER 317-03-1	



NOTES:

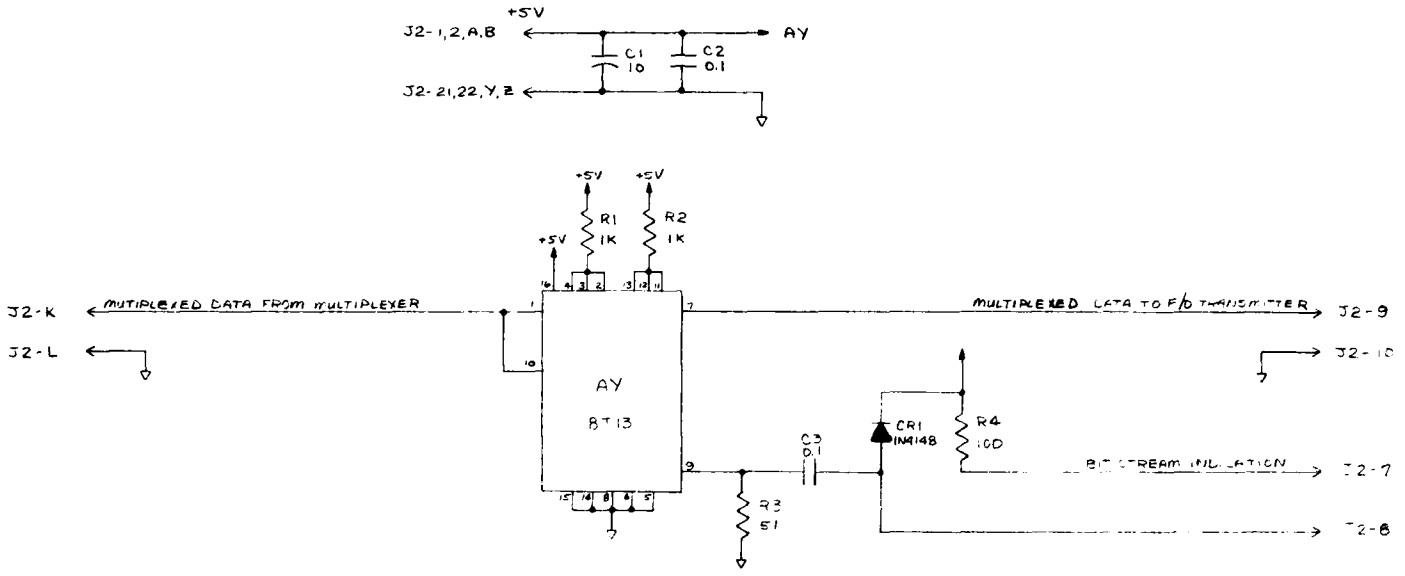
1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS, ¼ WATT, 10% ; ALL CAPACITOR VALUES ARE MICROFARADS

2. FOR EXTERNAL CONTROL OF CLOCK AND CLEAR SIGNALS FOR SYNC COUNTERS (U7 AND U8), TWO JUMPERS MUST BE REMOVED. J1-C TO J1-D AND J1-3 TO J1-4.

DEMULTIPLEXER BOARD

DATE JUNE 1980	DESIGNED BY EDL	APPROVED BY	
SCALE	DRAWN		

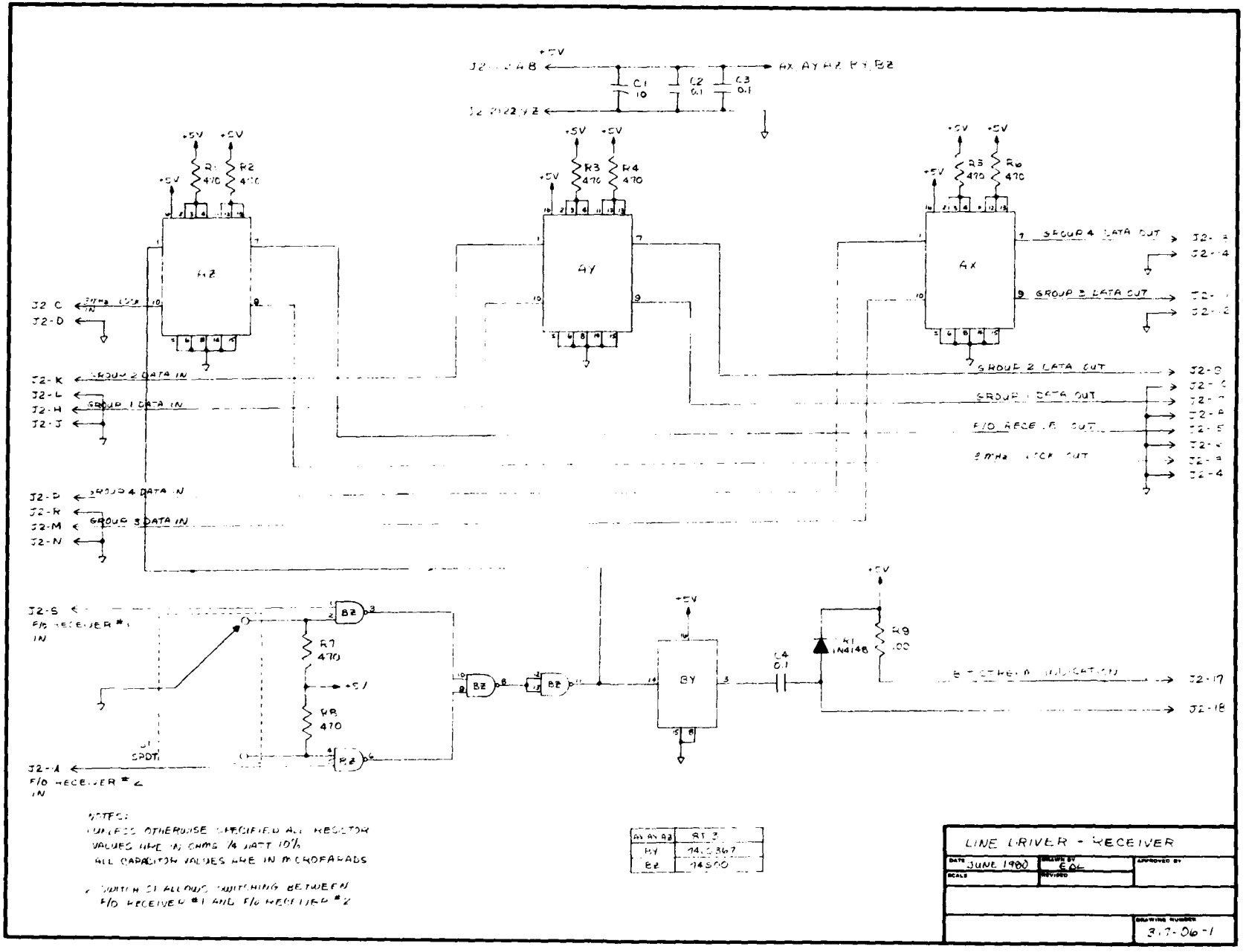
317-04-1



NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS, ¼ WATT, 10%.
   CAPACITOR VALUES ARE IN MICROFARADS.

LINE DRIVER-TRANSMITTER		
DATE JUNE 1980	DRAWN BY E.D.L.	APPROVED BY
SCALE	REVISED	
		DRAWING NUMBER 317-05-1



NOTES:
UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS ¼ WATT 10%
ALL CAPACITOR VALUES ARE IN MICROFARADS

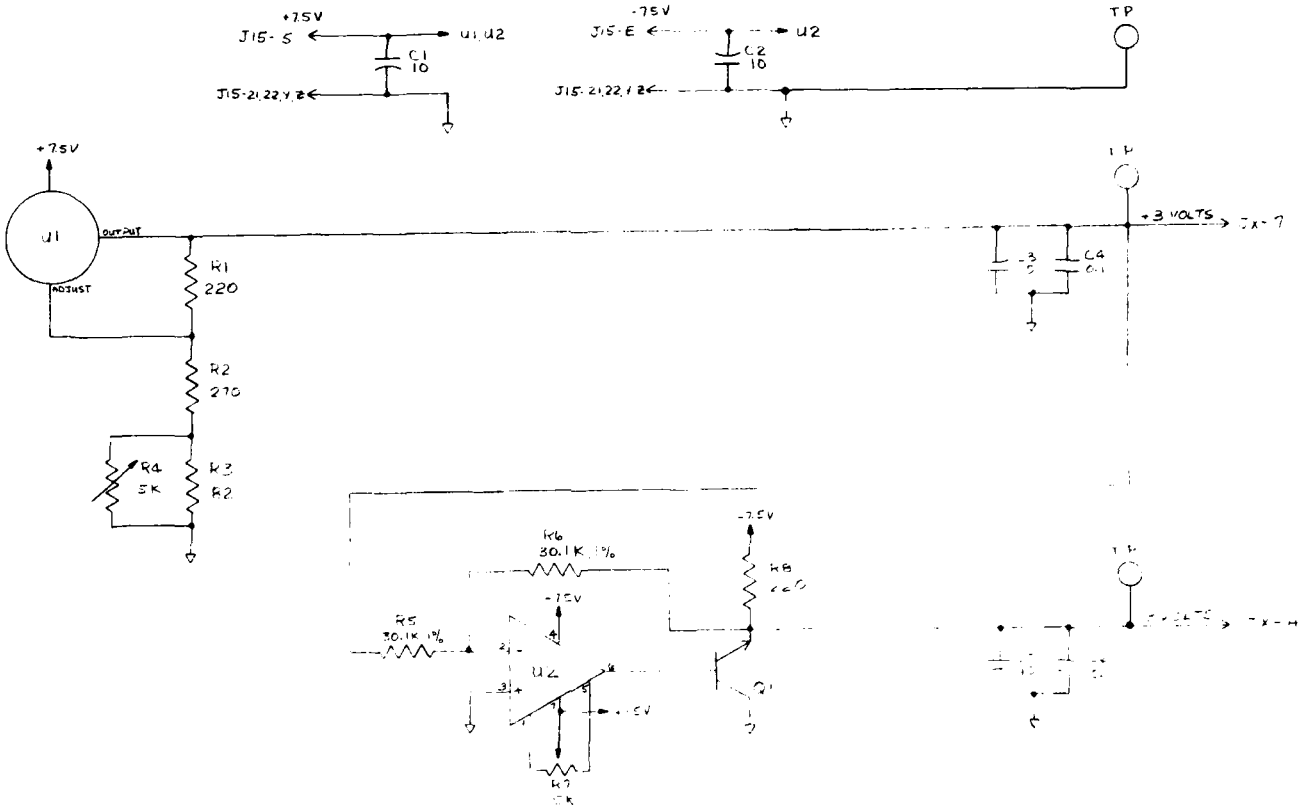
* SWITCH S1 ALLOWS SWITCHING BETWEEN F/O RECEIVER #1 AND F/O RECEIVER #2

AX AY AZ	R1-3
AY	74LS367
BZ	74S00

LINE DRIVER - RECEIVER

DATE	DRAWN BY	APPROVED BY
JUNE 1980	EAL	
SCALE	REVISED	

DRAWING NUMBER 3.7-06-1



NOTES:

1 UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS. ¼ WATT, 10%; ALL CAPACITOR VALUES ARE MICROFARADS

2 JX → X = 3-14, 17-28

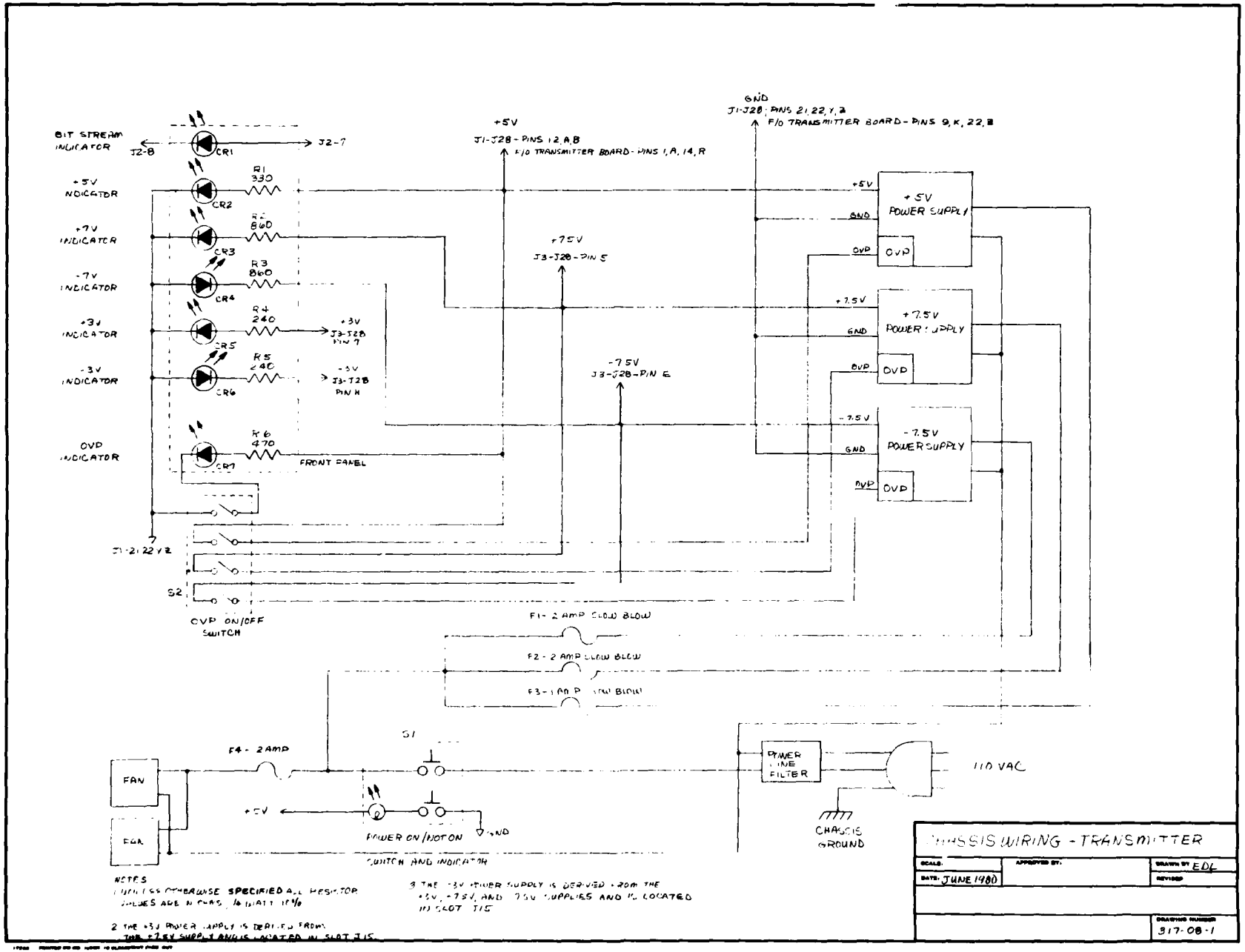
U1	LM317K
U2	LF356N
Q1	2N2222

+3 AND -3 VOLT POWER SUPPLY

DATE JUNE 1980 | DRAWN BY EDL | APPROVED BY

SCALE | REVISED

DRAWING NUMBER 317-07-1



NOTES

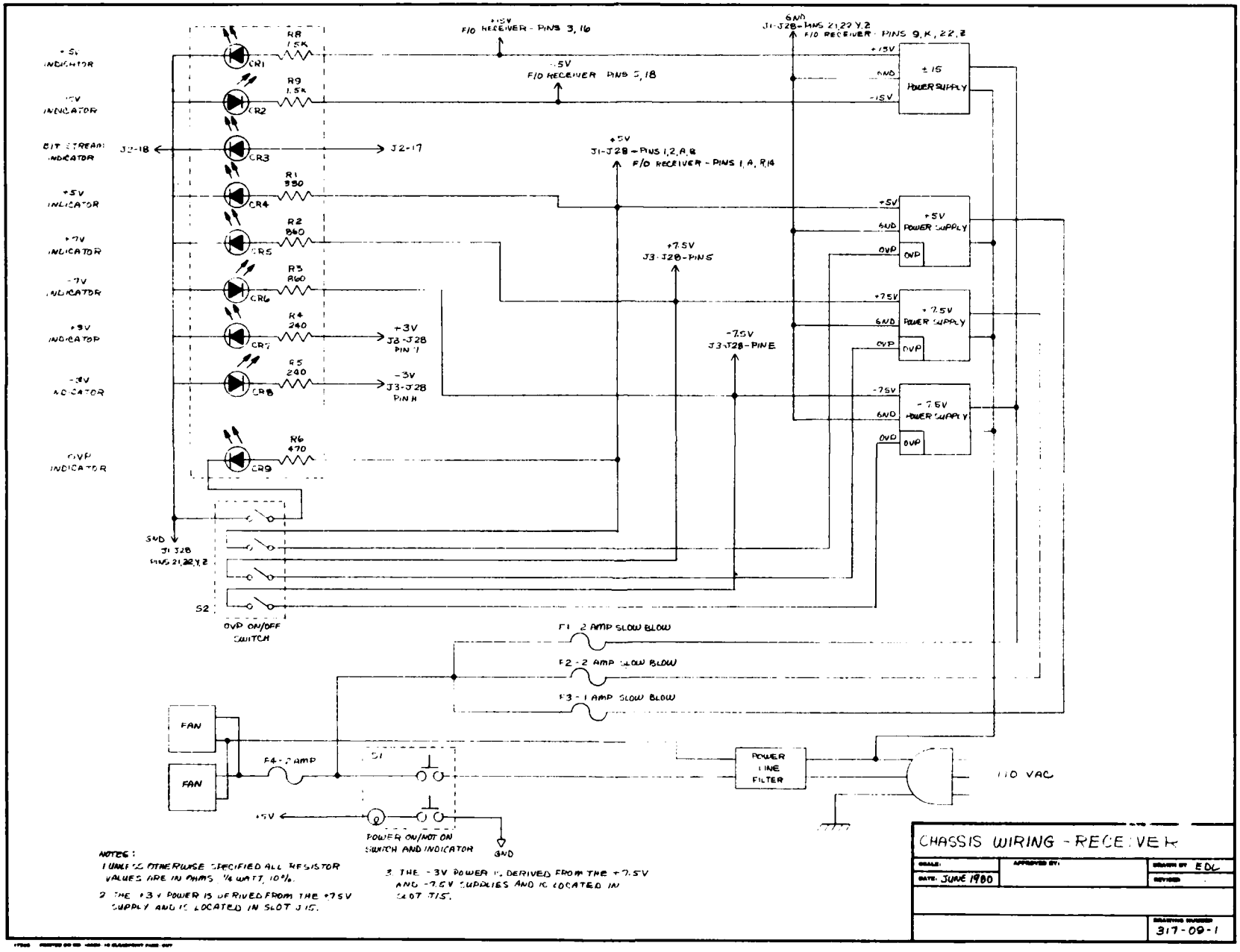
1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS, 1/4 WATT 1%

2. THE +3V POWER SUPPLY IS DERIVED FROM THE +7.5V SUPPLY AND IS LOCATED IN SLOT J15.

3. THE -3V POWER SUPPLY IS DERIVED FROM THE +3V, +7.5V, AND -7.5V SUPPLIES AND IS LOCATED IN SLOT J15

CHASSIS WIRING - TRANSMITTER

SCALE:	APPROVED BY:	DRAWN BY EDL
DATE: JUNE 1980		REVISED
		DRAWING NUMBER 317-08-1



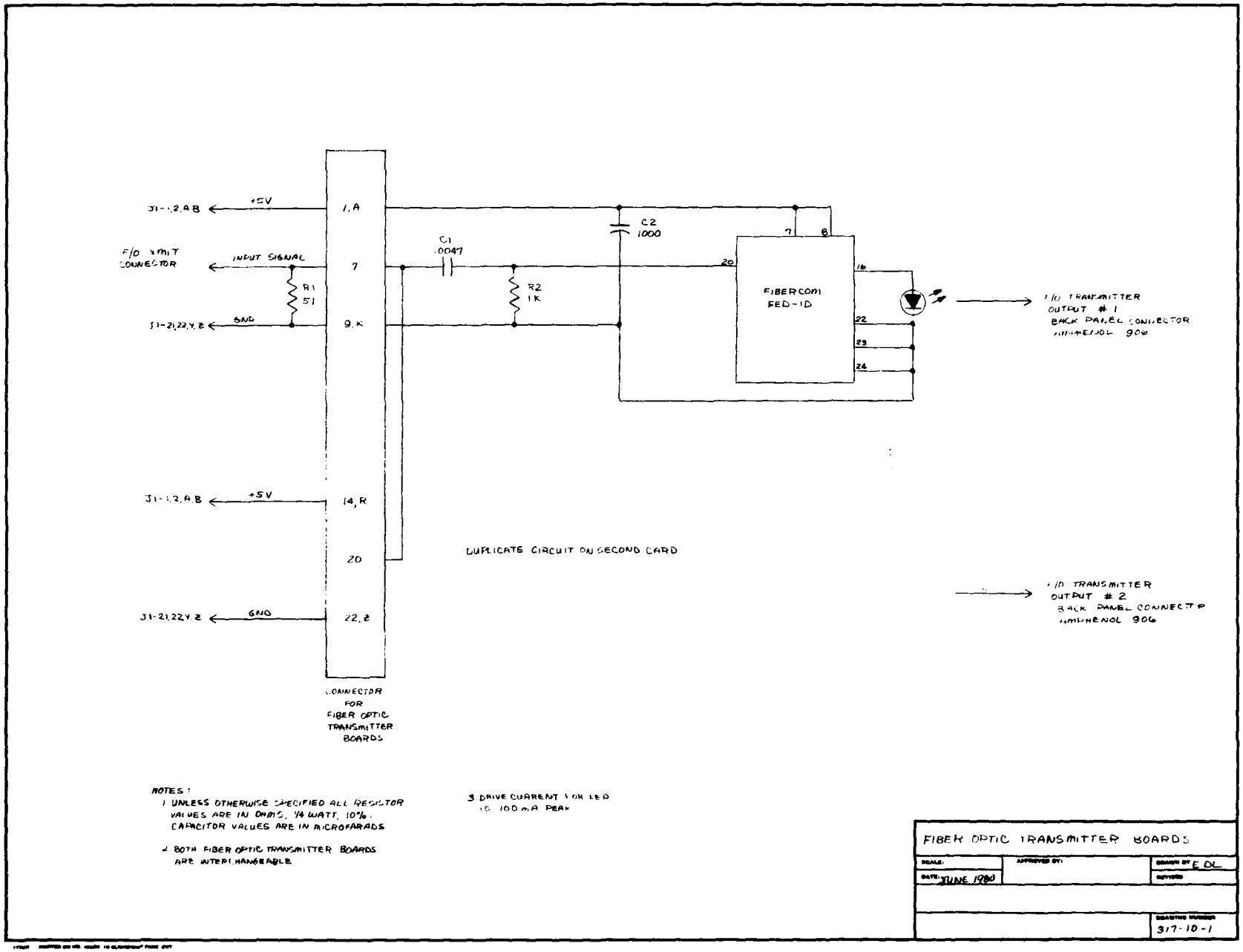
NOTES:

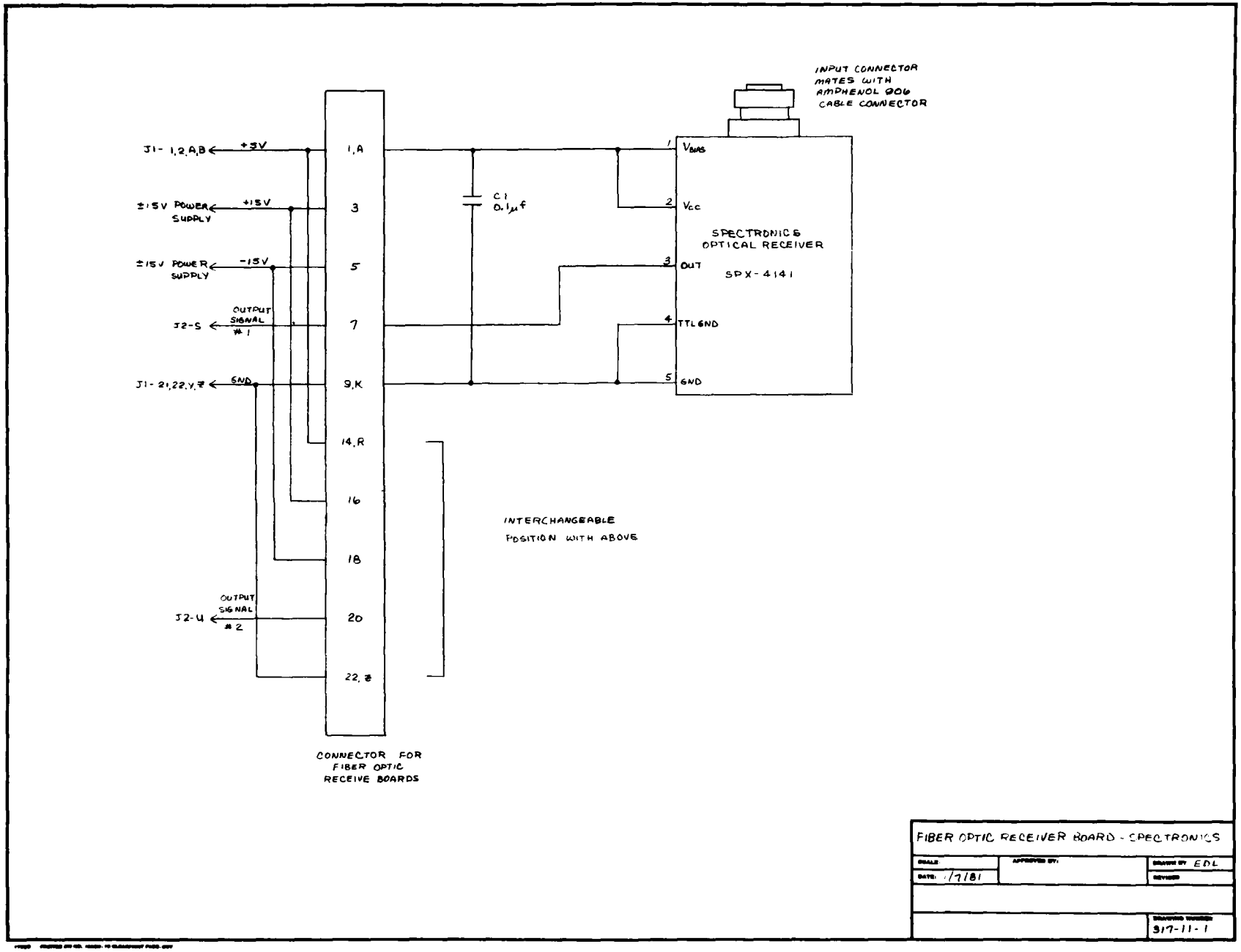
1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS, ¼ WATT, 10%.
2. THE +3 v POWER IS DERIVED FROM THE +7.5V SUPPLY AND IS LOCATED IN SLOT J15.
3. THE -3V POWER IS DERIVED FROM THE +7.5V AND -7.5V SUPPLIES AND IS LOCATED IN SLOT J15.

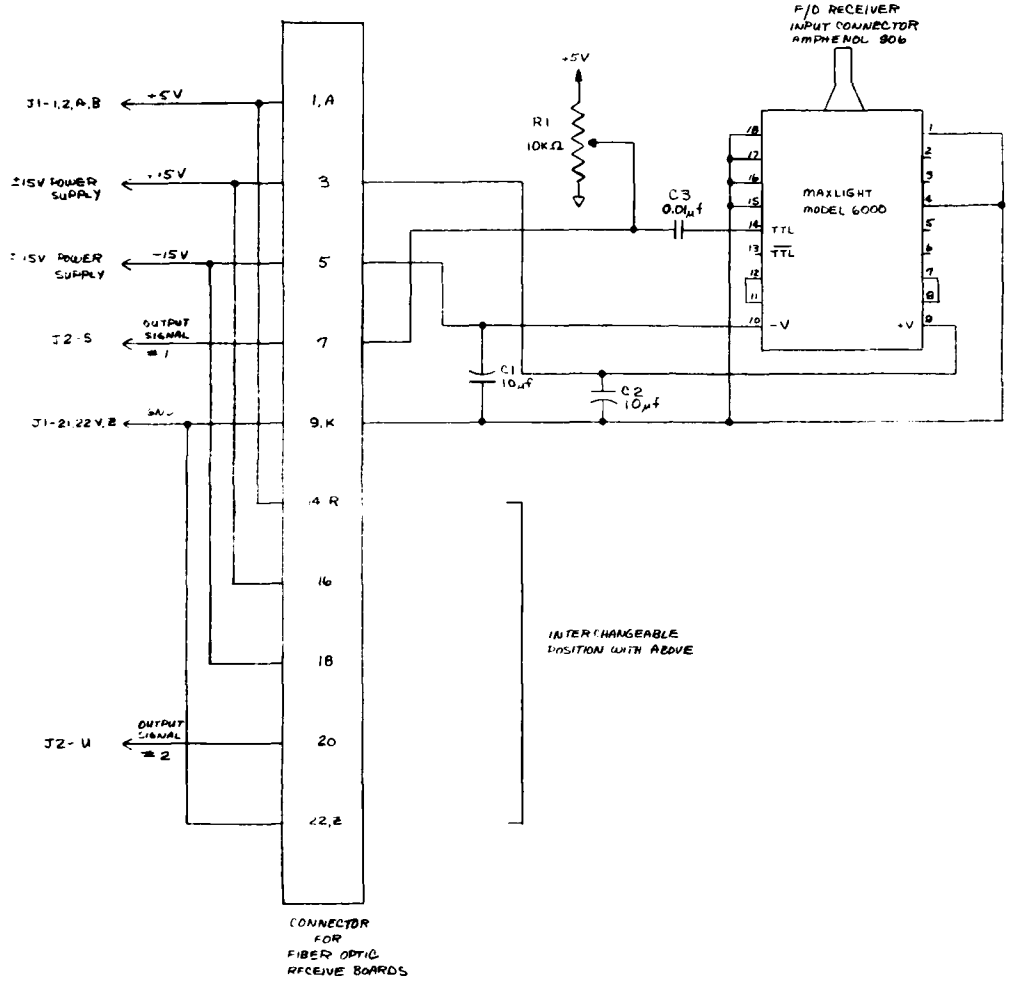
CHASSIS WIRING - RECEIVER

SCALE:	APPROVED BY:	DRAWN BY EDL
DATE: JUNE 1980		REVISED

317-09-1

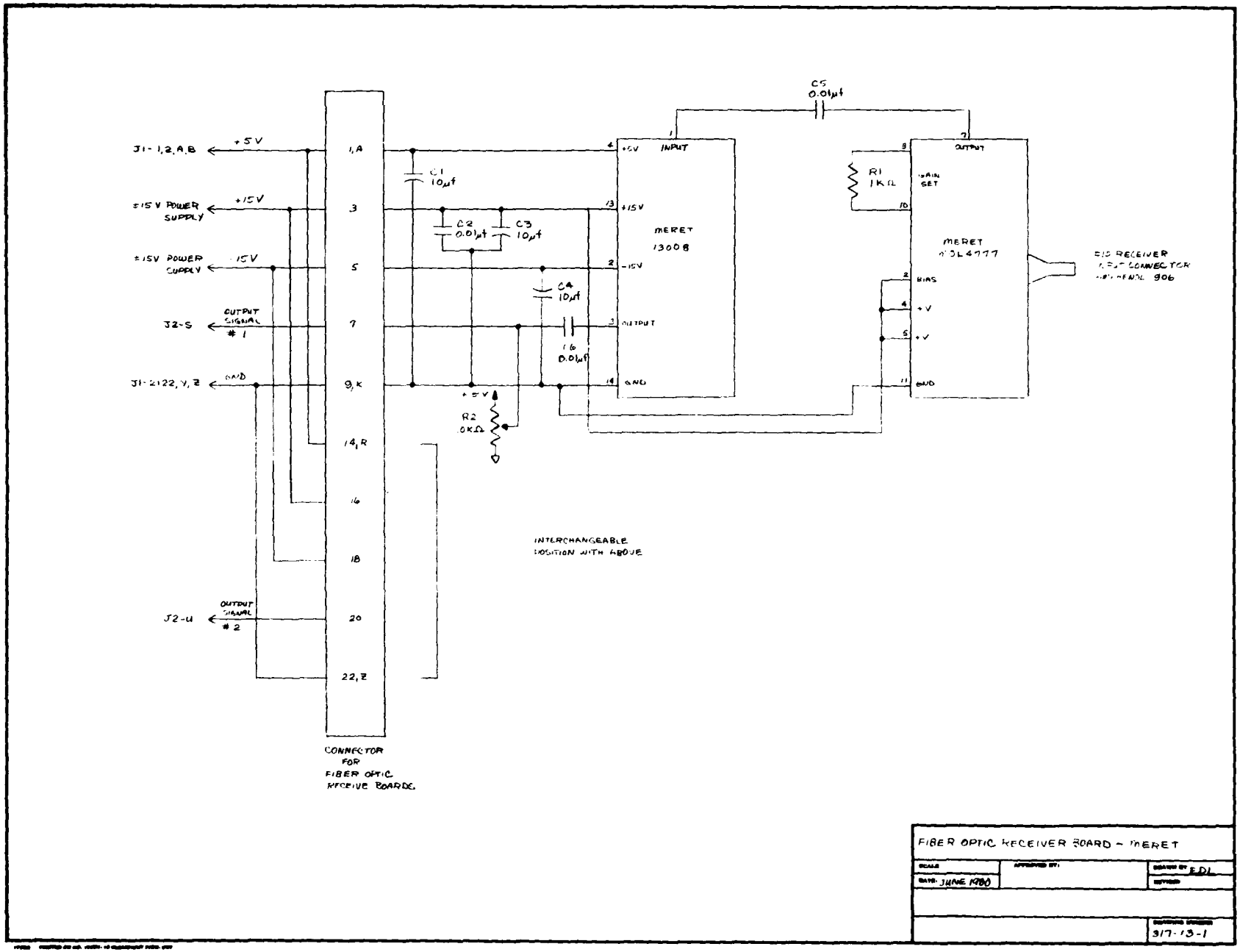

J1-1,2,A,B
+5V
1, A
F/O XMIT CONNECTOR
INPUT SIGNAL
7
R1 51
J1-21,22,Y,Z
GND
9, K
C1 .0047
R2 1K
C2 1000
7
8
20
FIBERCOM FED-1D
16
22
23
24
F/O TRANSMITTER OUTPUT #1 BACK PANEL CONNECTOR AMPHENOL 906
J1-1,2,A,B
+5V
14, R
20
J1-21,22,Y,Z
GND
22, Z
CONNECTOR FOR FIBER OPTIC TRANSMITTER BOARDS
DUPLICATE CIRCUIT ON SECOND CARD
F/O TRANSMITTER OUTPUT #2 BACK PANEL CONNECTOR AMPHENOL 906
NOTES:
1 UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS, 1/4 WATT, 10%. CAPACITOR VALUES ARE IN MICROFARADS
2 BOTH FIBER OPTIC TRANSMITTER BOARDS ARE INTERCHANGEABLE
3 DRIVE CURRENT FOR LED IS 100 mA PEAK
FIBER OPTIC TRANSMITTER BOARDS
SCALE:
APPROVED BY:
DRAWN BY E DL
DATE: JUNE 1980
317-10-1

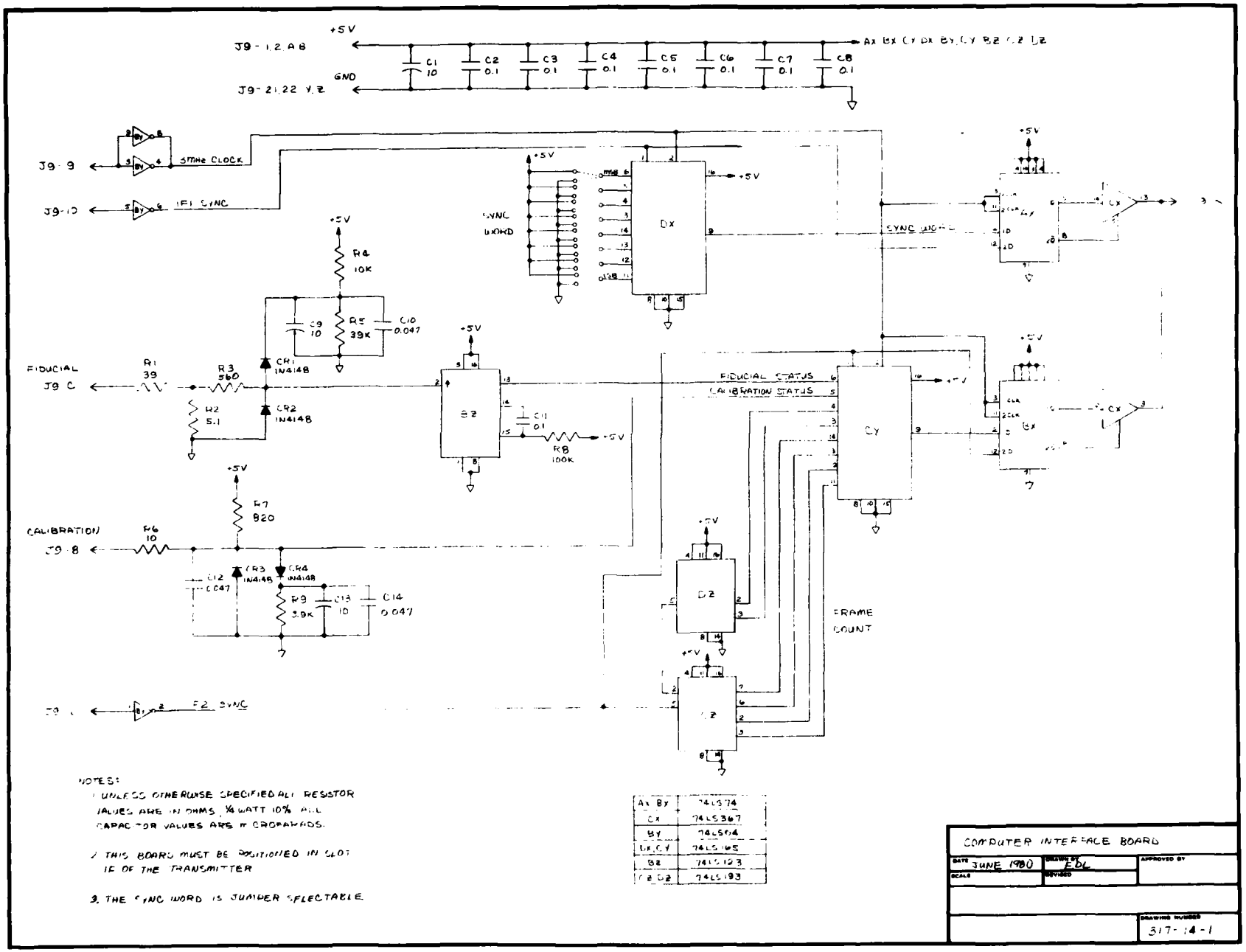

INPUT CONNECTOR MATES WITH AMPHENOL 906 CABLE CONNECTOR
J1- 1,2,A,B
+5V
±15V POWER SUPPLY
+15V
±15V POWER SUPPLY
-15V
OUTPUT SIGNAL #1
J2-S
J1- 21,22,Y,Z
GND
OUTPUT SIGNAL #2
J2-U
1,A
3
5
7
9,K
14,R
16
18
20
22,Z
C1
0.1μf
1 VBIAS
2 Vcc
3 OUT
4 TTL GND
5 GND
SPECTRONICS OPTICAL RECEIVER
SPX-4141
INTERCHANGEABLE POSITION WITH ABOVE
CONNECTOR FOR FIBER OPTIC RECEIVE BOARDS
FIBER OPTIC RECEIVER BOARD - SPECTRONICS
DRAWN BY EDL
DATE: 1/7/81
317-11-1



FIBER OPTIC RECEIVER BOARD - MAXLIGHT

SCALE:	APPROVED BY:	DRAWN BY E.DL
DATE: JUNE 1980		REVISED
		317-12-1


C5
0.01μf
J1-1,2,A,B
+5V
1,A
C1
10μf
4
+5V
INPUT
1
±15V POWER SUPPLY
+15V
3
C2
0.01μf
C3
10μf
13
+15V
MERET
13008
±15V POWER SUPPLY
-15V
5
2
-15V
C4
10μf
J2-S
OUTPUT SIGNAL #1
7
C6
0.01μf
3
OUTPUT
J1-21,22,Y,Z
GND
9,K
14
GND
+5V
R2
0KΩ
14,R
16
18
J2-U
OUTPUT SIGNAL #2
20
22,Z
CONNECTOR FOR FIBER OPTIC RECEIVE BOARDS
INTERCHANGEABLE POSITION WITH ABOVE
R1
1KΩ
GAIN SET
9
10
OUTPUT
7
MERET
MDL4777
BIAS
2
+V
4
+V
5
GND
11
FIBER OPTIC RECEIVER BOARD - MERET
SCALE
DATE: JUNE 1980
APPROVED BY:
DRAWN BY E.D.L.
317-13-1


+5V
J9-1,2 A B
GND
J9-21,22 Y,Z
C1 10
C2 0.1
C3 0.1
C4 0.1
C5 0.1
C6 0.1
C7 0.1
C8 0.1
Ax Bx Cx Dx Ex Cy Bz Cz Dz
J9-9
J9-10
STRIKE CLOCK
IFI SYNC
SYNC WORD
Dx
R4 10K
R5 39K
C9 10
C10 0.047
CR1 1N4148
CR2 1N4148
R1 39
R2 5.1
R3 560
FIDUCIAL
J9 C
Bz
C11 0.1
R8 100K
FIDUCIAL STATUS
CALIBRATION STATUS
Cy
Ex
Cx
R7 820
R6 10
CALIBRATION
J9-8
C12 0.047
CR3 1N4148
CR4 1N4148
R9 3.9K
C13 10
C14 0.047
Dz
FRAME COUNT
Ez
J9-
F2 SYNC
NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS, ¼ WATT 10% ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. THIS BOARD MUST BE POSITIONED IN SLOT 1E OF THE TRANSMITTER
3. THE SYNC WORD IS JUMPER SELECTABLE
Ax Bx 74LS74
Cx 74LS367
By 74LS04
Ex,Cy 74LS165
Bz 74LS123
Cz Dz 74LS193
COMPUTER INTERFACE BOARD
DATE JUNE 1980
DRAWN BY F.D.L.
APPROVED BY
SCALE
REVISED
DRAWING NUMBER
517-14-1

SECTION 7.0

REFERENCES

7.0 REFERENCES

1. Laser Diode Laboratories, Inc. "High Radiance, High Speed Etched Well Emitter with Fiber Pigtail for Fiber Optic Communications IRE 160 Series".

2. Radiation Devices Company, Inc. "Fibercom™ Fed - Series Fiberoptic Emitter Drivers".

3. Maxlight Optical Waveguide, Inc. "Model 6000 Receiver".

4. Meret, Inc. "Operation of Digital Skini-Dip Links".

5. Siliconix Incorporated Publications:

   a. "CMOS μ-255 Law Codec Set (DF331A [Coder], DF332A or DF334A [Decoder])"

   b. "Function/Application of the DF331/332 New Companding Converter Chip Set"

   c. "Design Aid to Build a CODEC Evaluation Demonstrator with the DF331/DF332/DF334"

   d. "Considerations for the Proper Filtering of Analog Signals in DF331/DF332/DF334 CODEC Converter Applications"

   e. "Designing with codecs: know your A's and μ's"

   f. "CODEC/Filter Level and Noise Measurements"

   g. "Publications Index".

7.0 REFERENCES (Continued)

6. Spectronics, A Division of Honeywell, "Optoelectronic Components in Fiber Optic Receptacles, SPX 3180/SPX 3190 Series," 110-0199-000, 4-79.

7. Spectronics, A Division of Honeywell, "Fiber Optic Receiver Module, SPX 4141," 110-0229-000, 7-80.

APPENDIX

FIBERCOM™

FED - SERIES

FIBEROPTIC EMITTER DRIVERS

APRIL 1978

- LOW COST
- SMALL SIZE
- TTL COMPATIBLE
- OPERATION TO 25MBPS RZ
- 24 PIN DIP CONFIGURATION

The FED series is comprised of several LED drivers designed for fiberoptic use. Each requires only an emitter or emitter assembly and a 5 volt power supply to realize a complete TTL compatible fiberoptic transmitter. The units have either adjustable, or fixed and compensated drive currents. They are encapsulated in 24 pin dual-in-line plastic packages.

PINOUTS AND CONNECTION DIAGRAMS

FED-1D

7.	+5V
8.	RL
16.	Output
18.	Strobe
20	Data In
22.	GND
23.	GND
24.	GND

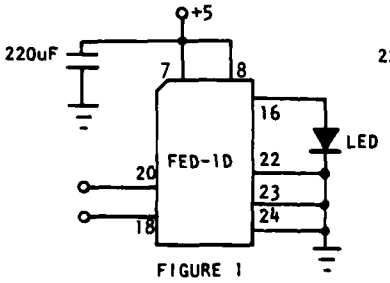


FIGURE 1

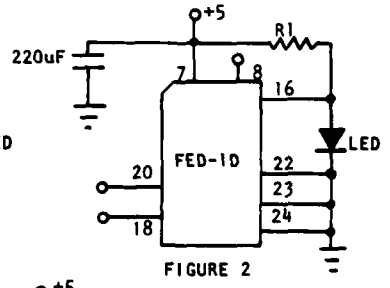


FIGURE 2

FED-2D/3D/4D

8.	+5
13.	Output
18.	GND
24.	Data In

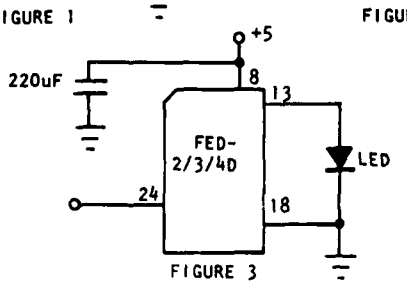


FIGURE 3

RADIATION DEVICES CO.,INC. ●P.O.BOX 8450●BALTIMORE,MD. 21234 U.S.A.●(301)628-2240

SPECIFICATIONS

PARAMETER[1]	FED-1D[2] MIN.	FED-1D[2] TYP.	FED-1D[2] MAX.	FED-*D MIN.	FED-*D TYP.	FED-*D MAX.	UNITS
Power Supply	4.5	5.0	5.5	4.5	5.0	5.5	V
Supply Current Input "1"		170	200		80	90	mA
Supply Current Input "0"		100	125		65	75	mA
Peak Emitter Drive Current		100	300		75		mA
Electrical Risetime		15	20		4	6	nsec
Electrical Falltime		5	10		4	6	nsec
Electrical Bandwidth		25			25		MHz
Optical Risetime[3]		55	60		SEE		nsec
Optical Falltime		20	25				nsec
Optical Bandwidth (-3dB @ Receiver)	10	16			TABLE		MHz
Optical Bandwidth (0.5 Optical Power)	15	20			BELOW		MHz
Data Input	1 standard TTL load			2 standard TTL loads			
Temperature Range (operating & storage)	0		70	0		70	°C

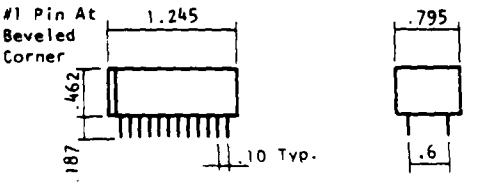
	FED-2D MIN.	FED-2D TYP.	FED-2D MAX.	FED-3D MIN.	FED-3D TYP.	FED-3D MAX.	FED-4D MIN.	FED-4D TYP.	FED-4D MAX.	UNITS
Optical Risetime[3]		25	30		22	30		15	20	nsec
Optical Falltime		20	25		18	25		14	20	nsec
Optical Bandwidth (-3dB @ Receiver)	15	20		10	17		15	20		MHz
Optical Bandwidth (0.5 Optical Power)	20	25		15	20		20	25		MHz

NOTES: 1. Test data was taken with the modules driving the following or similar light emitting diodes: FED-1D - FOE-3 with V_f=1.7V and C_o=150pf
FED-2D - FOE-3 with V_f=1.7V and C_o=150pf
FED-3D - FOE-1 with V_f=1.3V and C_o=100pf
FED-4D - FOE-9 with V_f=1.6V and C_o= 30pf

2. FED-1D has an internal limiting resistor which supplies a drive of 100mA (Figure 1). However, other drive currents may be externally set (Figure 2) up to 300mA maximum.

3. Certain types of LED's will exhibit slower risetimes at elevated temperature.

MECHANICAL INFORMATION



MATERIAL: GF Nylon UL Rated 94V-0
FINISH: Natural Black
PINS: Gold over Nickel On 1/2 Hard Brass

RADIATION DEVICES CO., INC. ● P.O.BOX 8450 ● BALTIMORE, MD. 21234 U.S.A. ● (301)628-2240

OPERATING CONSIDERATIONS

STANDARD CONFIGURATION

The FED-1D is a general purpose driver which can be used with any emitter requiring any forward current to 300mA. Figure 1 shows the use of the 100mA internal limiting resistor while Figure 2 shows the connections necessary for using an external limiting resistor. FED-2D/3D/4D's are connected as shown in Figure 3 and have fixed drive currents of 75mA.

BYPASSING

Bypassing the power supply at the module with a 220uf capacitor may be necessary to minimize switching spikes on power supply lines.

STROBE (FED-1D ONLY)

The output may be disabled by pulling the strobe input (TTL compatible) low. If not used the strobe pin is left unterminated. The strobe function is useful where a single source of data must be linked to several selectable data sinks.

ADJUSTABLE CURRENT (FED-1D ONLY)

Figure 2 shows the connections for a forward diode current (I_f) other than 100mA. R_1 should be non-inductive, have an adequate power rating and be chosen so that I_f does not exceed the LED continuous forward current rating.

$$R_1 = \frac{Vcc - V_f}{I_f} \quad \text{and} \quad PD_{R1} = (Vcc - V_f) I_f$$

where:

R_1 = load resistor (ohms)
Vcc = power supply voltage (volts)
V_f = LED forward voltage @ I_f (volts)
I_f = LED forward current (amps)
PD_{R1} = power dissipation R_1 (watts)

SELECTION OF EMITTER

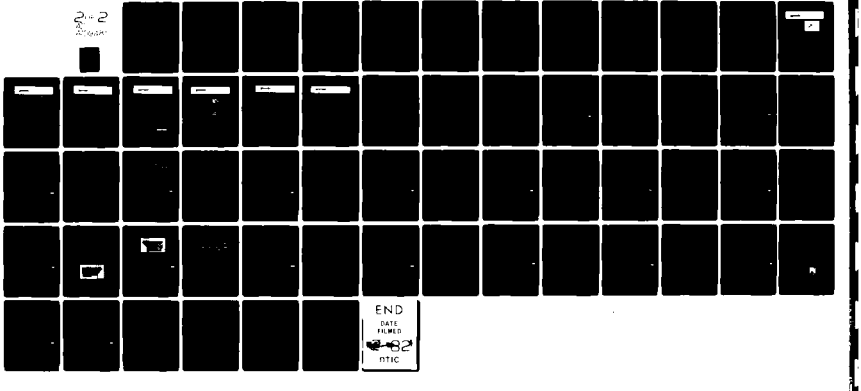
The FED-1D, being a general purpose driver, does not require careful matching of the emitter to the driver. However, LED's having large junction capacitances will exhibit slow risetimes which will produce a non-symmetrical light output when the FED-1D is driven by a square wave. The remaining modules in the FED series have equal rise and fall times and careful matching of the driver to the emitter will produce a symmetrical light output. Radiation Devices Co., Inc. will be happy to assist in the selection of the proper driver or reconfigure the output circuity of the FED modules to match any emitter.

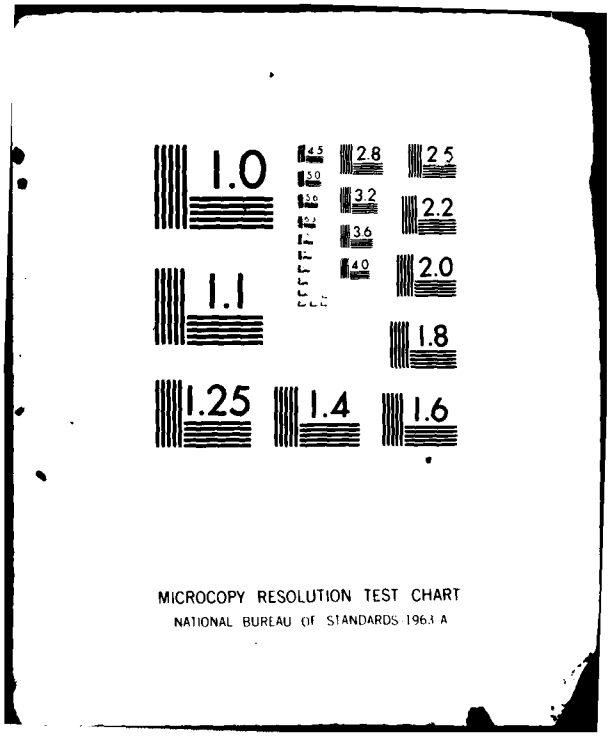
ACCESSORIES

FIBERCOM™ FOT terminals, which accept FIBERCOM™ FOC cable assemblies, may be used with metal cased TO-5 and TO-18 or T-1 3/4 plastic encapsulated devices. Complete emitter assemblies matching the characteristics of the FED series modules are available as the FIBERCOM™ FOE series.

RADIATION DEVICES CO., INC. ● P.O.BOX 8450 ● BALTIMORE, MD. 21234 U.S.A. ● (301)628-2240

AD-A109 481 EFFECTS TECHNOLOGY INC SANTA BARBARA CA F/G 17/2
FIBER OPTIC CODEC LINK (FOCOL), VOLUME 2 - MANUAL,(U)
JAN 81 W NAUMANN, E LILES, R D HOGG DNA001-79-C-0021
UNCLASSIFIED ETI-CR81-865 DNA-5747F-2 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

MODEL 6000 RECEIVER

FUNCTIONAL DESCRIPTION

A block diagram of the Model 6000 Receiver is shown in Figure 3. The receiver contains a pigtailed detector, a pre-amplifier, post amplifier/regenerator and ECL/TTL translator and buffers.

The detector used in the Model 6000 Receiver is a silicon PIN photodiode, which is operated in the photoconductive (current) mode with a reverse bias of about 9 volts. At 850um, the operating wavelength of the GaAlAs LED used in the Transmitter, the responsivity of the detector is typically between 0.5 and 0.55 A/W.

The detector is interfaced to an AMP fiber optic connector via a pigtail of Maxlight SC-300B PCS fiber. The use of this large core (300um) large NA (.41) fiber assures compatibility of the receiver with 200um core PCS fibers with virtually no interconnection losses (less than .5dB without index matching). Maxlight uses its FIBERSLEEVE^{TM} for mating the fiber to the AMP connector, thus avoiding the common problems of "punch through" and centering that plague other PCS connection techniques.

The photoinduced current provided by the detector is amplified and converted into a voltage signal by a transimpedance amplifier. The transimpedance amplifier is a low noise amplifier with a feedback resistor of 22kΩ shunted by approximately .17pF. To the first order the value of R_f determines the gain and bandwidth of the pre-amp. The combination of the detector and transimpedance amplifier yields an output of approximately 10mv per microwatt. Since the noise limited performance of the amplifier is less than .5uw, detector leakage current and DC amplifier drift due to temperature, power supply, and component aging become significant with respect to the desired signal. Therefore, the transimpedance amplifier is capacitively coupled to the post amplifier to eliminate these effects. One consequence of this AC coupling technique is that the DC level of the output side of the capacitor is a function of the duty cycle of the received signal. This ordinarily necessitates an AGC circuit and variable threshold comparator in order to maintain the optimum (mid value) threshold for all amplitudes of received signals. In the Model 6000 Receiver, the threshold is fixed and is adjusted to be mid value for 50% duty cycle signals. This approach avoids the complexity and attendant problems associated with the AGC approach. Another consequence of AC coupling with the threshold adjusted to mid value (essentially DC ground plus or minus bias currents) is that there is some minimum signaling rate as well as some minimum average amplitude which must be maintained or the capacitor will be discharged to a level within the uncertainity region of the regenerator and noise will be generated on the outputs. The noise is manifested as edge or phase jitter.

The post amplifier/regenerator increases the amplitude of the signal from the transimpedance amplifier to a usable level and then regenerates the edges essentially by comparison to a fixed voltage threshold (0.0v).

The post amp/regenerator is followed by translators/buffers that convert the signal into standard logic family levels, namely ECL and TTL. Both inverting and noninverting outputs are provided in ECL and TTL compatible formats enabling the driving of differential inputs at the user's interface. The ECL signals are internally pulled down to -5v through 510Ω resistors so that no external pulldown is required. 50Ω lines can be driven with the ECL outputs by AC coupling into the coaxial line and terminating with 50Ω at the user's interface. The TTL outputs are industry compatible and will drive 10 standard TTL loads.

INSTALLATION

All power and signal connections for the receiver are accessable at the pins underneath the unit. These pins are 0.018 inches in diameter and will plug into a universal wire wrap board or alternatively the unit may be mounted on the user's PC board. In applications where the unit is mounted other than top up or in applications with excessive vibration, it is recommended that the unit be physically secured by means other than the electrical pins. This may include nylon cable ties or spot tie cord around the unit and PC mounting board, or alternatively 2 screws may be removed from the bottom cover and replaced with 2-56 screws which pass through the PC mounting board and secure the unit to the board.

ELECTRICAL CONNECTIONS

The recommended connections for operation of the Model 6000 Receiver are shown in Figure 4(a). In this configuration, the user supplies ±8vdc to ±15vdc, and the receiver's internal regulators provide the required ±5vdc. While this implementation dissipates somewhat more power, it is preferred where possible because of the isolation afforded the sensitive, low level amplifier circuits.

Figure 4(b) illustrates the connection required for operation from externally regulated +5v, -5.2v supplies. Additional components are necessary to insure that the front end is minimally affected by power supply noise or transients. These components should be mounted as close as physically possible to the respective pins and the load length kept very short.

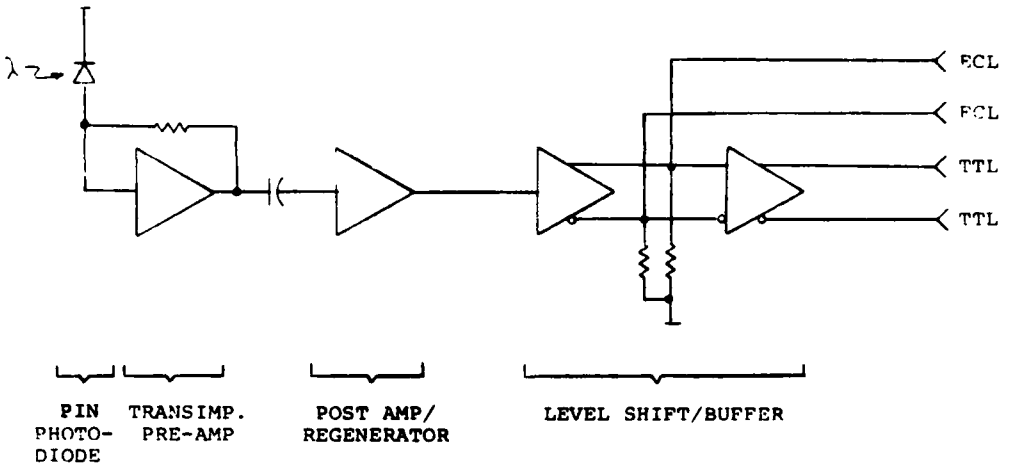
GROUNDING AND SHIEDLING CONSIDERATIONS

Great care has been taken to insure that the receiver circuitry is completely shielded from external E/M interference. The top and bottom covers have been sealed to the nickel plated housing with a conductive elastomer, and should not be removed. In order for the shielding to be effective, it is very important that good grounding techniques be used (I.E. #26 AWG wire as short as possible). Case ground and signal ground have been internally connected to provide the best necessary shielding.

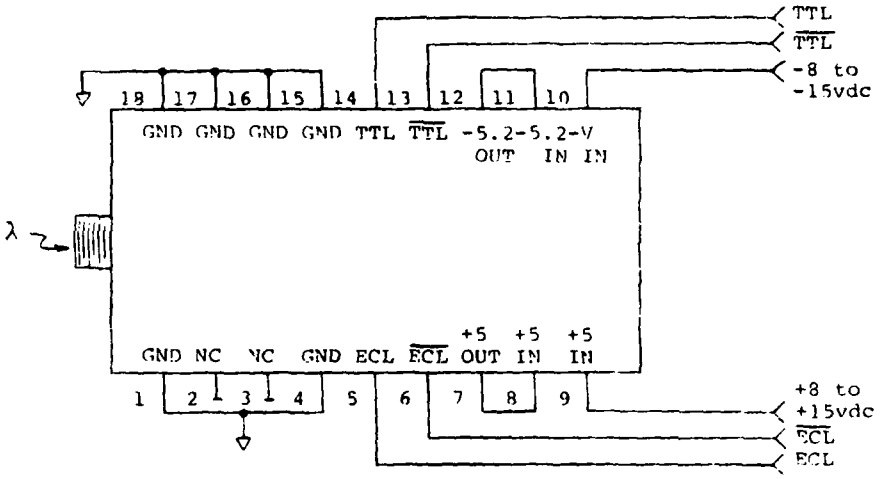
THERMAL CONSIDERATIONS

The circuitry in the receiver is mounted over a 0.031 inch thick copper heat sink which is thermally attached to the nickel plated housing. This technique provides minimum thermal resistance to the ambient which allows efficient removal of waste energy. The operation of the receiver is specified over a case temperature of -20 to +50° C, so that in some circumstances additional heat sinking and/or forced air cooling may be required to maintain the case temperature below 50° C. In particular, mounting adjacent to other large heat dissipating components or in small inclosed areas is not recommended unless consideration is given to removal of excess heat.

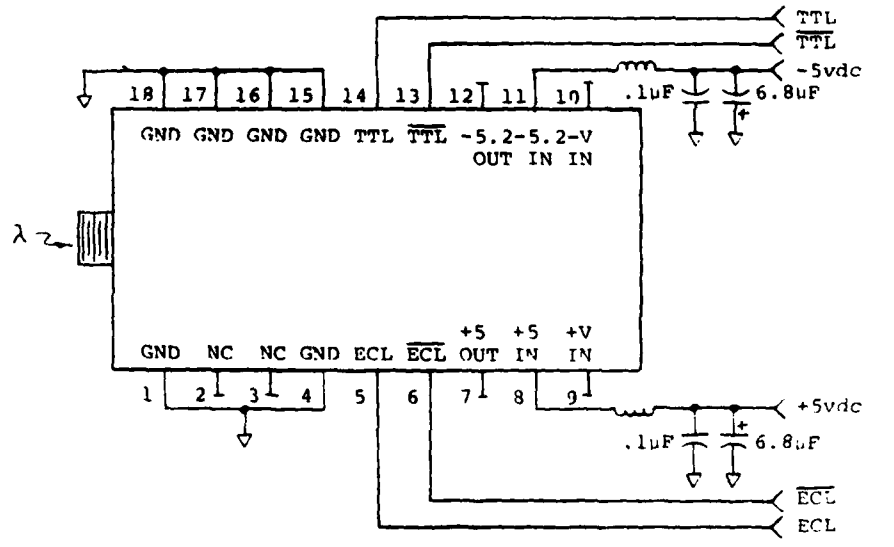
MODEL 6000 RECEIVER BLOCK DIAGRAM
FIGURE 3



MODEL 6000 ELECTRICAL CONNECTIONS
FIGURE 4



(a) INTERNALLY REGULATED



(b) EXTERNALLY REGULATED

INTERFACE CONSIDERATIONS

The Model 5000/6000 System essentially transfers binary digital information which is Intensity Modulated (IM) whereby the optical carrier is set to a maximum intensity to represent one binary state ("1" or "mark") and a minimum intensity to represent the other binary state ("0" or "space"). The data which is presented to the transmitter to be intensity modulated must be encoded by the user in such a manner so as to insure the average intensity is $\frac{1}{2}(I_{max} + I_{min})$, that is to say the data stream must have a 50% duty cycle. Maxlight recommends that phase or frequency coding techniques be used with the Model 5000/6000 Systems. These include Bi-Phase L, Bi-Phase M, Bi-Phase S, Frequency Shift Code and Frequency Shift Keying. The other techniques described either do not have 50% duty factor or require three levels of Intensity Modulation.

Considerable effort has been expended in developing suitable coding techniques for the transmission and storage of binary digital information. Individual industries have evolved preferred techniques to meet their particular requirements in the most cost effective manner. For example, the telecommunication industry uses Non-Return to Zero (NRZ) techniques and bipolar codes for most of their digital lines, while the magnetic recording industry has generally used NRZ or Phase Encoding (PE) schemes. Figure 5 illustrates some of the more commonly used codes.

In the NRZ(L) coding scheme, a binary "1" is represented by a high level, while a binary "0" is represented by a low level. In the NRZ(M) method, a level change is used to indicate a "1" (mark) and no level change for a "0"; the NRZ(S) scheme is the same as NRZ(M) except that a level change is used to describe "0" (space) and the absence of a level change for a "1". Both of these examples of the more general classification of NRZ(I) in which an inversion (level change) is used to represent one of the binary digits and no inversion delineates the other binary state. The NRZM and NRZS codes are an effort to create transitions during long streams of either all ones or zeros, respectively. Other methods, not shown in the figure, to provide transitions periodically include group coded recording (GCR) techniques in which a group of N bits in the original NRZL data stream are encoded to an M bit data stream such that there is never more than two consecutive zeros or ones, which simplifies clock decoding; however, a penalty is paid in bandwidth requirements.

The Non-Return to Zero representations allow maximum use of available bandwidth, but not without limitations. A clock must be regenerated at the receiving end, generally accomplished by phase lock loop (PLL) techniques or by synchronizing an accurate high speed clock to a start bit. NRZ inherently has a DC level which must be transmitted or restored, and for optimum recovery of the data at the receiver the comparator threshold must be variable.

Return to Zero(RZ) coding represents a "1" by a change to the high level for one half of the bit interval, after which the level returns to the low value for the remaining one half bit interval. A zero is indicated by no change, i.e. the low level. This technique breaks up long sequences of ones but requires twice the bandwidth of NRZL in the worse case (all 1's).

In the Manchester (Bi-Phase Level) code, a "1 " is represented by a high to low level transition at the center of the bit interval, while a zero is represented by a low to high level transition. Alternatively, Manchester may be viewed as one bit-two bit (1B2B) GCR technique whereby a one is represented by a "10" and a zero is represented by a "01". In the Bi-Phase Mark (Bi-Ø-M) method, a similar symmetrical representation is used except that a "1" is indicated by no phase reversal. Bi-Phase-M is equivalent to Manchester encoding of the NRZM data. In Bi-Phase Space (Bi-Ø-S) representation, a zero is indicated by a phase reversal with respect to the previous bit's phase and a one is described by no phase reversal, this is identical to Manchester encoding of NRZS data.

The PE techniques eliminate the variations in the average (DC) value because of their symmetry and since there is at least one transition per bit interval PE is inherently self clocking. Compared with NRZ, though, the phase encoding schemes require twice as much frequency response in the worse case. The worse case for Manchester is for a data stream of all 1's or all 0's, while the Bi-Phase-M worse case is realized by all zeros and worse case for Bi-Phase-S is all ones.

Frequency Shift Code (FSC) is a form of frequency modulation, whereby a "1" is represented by a frequency equal to the bit rate, while an "0" is indicated by a frequency equal to half of the bit rate. FSC is similar to Manchester except that Manchester uses the direction of the center bit transition to indicate the binary data, while in FSC any center bit transition indicates a one and no transition represents a zero. The worse case pattern for FSC is all ones, while the best case data stream is all zeros.

Frequency Shift Keying (FSK) is an extention of FSC in which two frequencies, both of which are greater than the data rate, are "keyed" or gated depending on the binary data value. The example shown in the figure represents a "1" by a frequency equal to twice the bit rate and a "0" by a frequency equal to the bit rate. Both the FSC and FSK coding techniques have 50% duty factors provided that the frequencies used involve multiples of the bit rate to insure that only full cycles of each frequency are included in the encoded data stream.

Pulse Position Modulation (PPM) is a code in which the beginning of each bit interval is marked by a pulse, and a "1" is represented by another pulse 1/3 of a bit interval later, while a "0" is represented by a pulse 2/3 of a bit interval after the sync pulse. PPM code has a constant duty factor which is not necessarily equal to 50%. There is no worse case data pattern for this type of code.

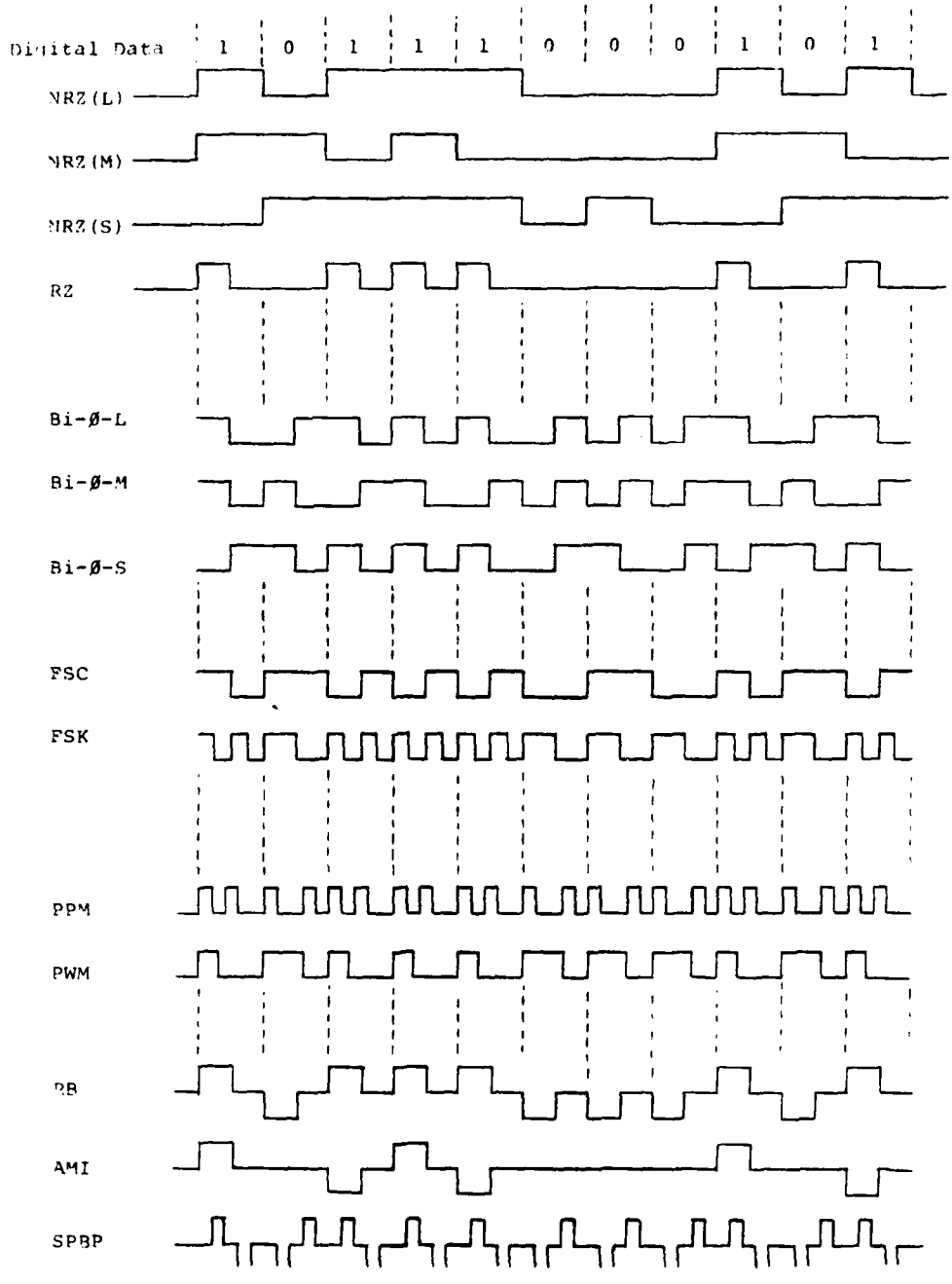
Pulse Width Modulation (PWM) is a code whereby the beginning of the bit is marked by a positive transitions and a one is represented by a return to the low level after 1/3 of a bit interval and a zero is represented by return to low level after 2/3 of a bit interval. The average or DC value of PWM is dependant on the data pattern. The bandwidth required for PWM is essentially constant regardless of the binary data pattern.

In the return to bias (RB) method, three levels are used "0", "1", and a bias level. The bias level may be chosen either below or between the other two levels (it may be zero reference as shown in the figure). The waveform returns to the bias level during the last half of the bit interval. The RB method has an advantage in being self clocking, since the clock is easily derived using an absolute value generator. However, the average value of the waveform depends on the particular proportion of ones and zeros present in the data stream. The RB representation also takes more bandwidth than necessary and it uses three levels.

In Alternate Mark Inversion (AMI) the first binary one is represented by a "+1", the second by a "-1", the third by "+1", etc. The AMI representation is easily derived from a RZ binary code by alternately inverting the ones. It has zero average value and is widely used in telephone PCM systems.

Split Phase Bi-Polar (SPBP) is a Bi-Polar version of Bi-Phase-L. The clock is very easily derived from SPBP code and has the advantage of having a 50% duty factor. However, this code requires excessive bandwidth and utilizes three levels.

FIGURE 5
CODING TECHNIQUES



MERET, inc.

Specialists in Optical Communications

Applications Note: Operation of Digital Skini-DIP Links

1. General

MERET Skini-DIP optical data links (MDL4700-SKP Series, digital) comprise high-injection efficiency IR-LED's with integral drivers, and PIN photodiodes with two cascaded transimpedance amplifiers.

2. Transmitter

Skini-DIP links with digital transmitters are TTL-compatible, emitting light at logic "0" levels, and turning off at logic "1" levels. One external resistor is required to limit the forward current through the LED. This resistor, R_{ext}, should be in the range of 20Ω to 100Ω, for a bias voltage of +5V. (A recommended value is 75Ω low forward current ensured long LED lifetime). It is necessary for the forward LED bias voltage to be extremely well by passed; that is, a 15μF capacitor should be placed from the power supply to ground, directly at the connection to R_{ext}.

Pin 10 (+5V supply to TTL driver) and R_{ext} may be connected to a common +5V. Note that no connections are necessary to pin 3 (LED cathode), which may be used as a convenient test point for checking operation of the driver.

If the digital transmitter is to be operated under conditions where average current drain is in excess of 50 mA, the unit should be operated with the heat sink attached. (The U-shaped heat sink slips over the top of the Skini-DIP package. The flange may be used for mounting to a PC board if desired). Note that average current, and thus, power dissipation, is a function of three variables: forward bias voltage, duty cycle of input signal, and R_{ext}. Therefore, if an average 50% duty cycle signal is applied to the input, and the bias voltage is +5V through R_{ext} of 50Ω or less, a heat sink should be used (see Fig.4 on MDL4777-SKP data sheet).

3. Receiver

Skini-DIP receivers utilize PIN photodiodes coupled to two cascaded amplifiers. Photodiode bias is positive and may be tied to the +12 V supply at pin 4 if high frequency response is not critical. (Bias is connected internally).

Receiver gain may be varied by attaching an external resistor between pins 3 and 10. (Gain is factory set at X1.6 with internal coupling resistor equal to 5k Ω). Second stage gain is described by the equation

$$G = \frac{8K\Omega}{Rc}$$

where Rc, the coupling resistance can be found by $\frac{1}{RC} = \frac{1}{5000} - \frac{1}{R_{ext}}$

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The first stage output gives a responsivity of 4 mV/uW at 900 nm.

Digital receivers are supplied with a 13008 signal processor (in standard DIP) which restores the output to TTL levels. Signal output is taken from pin 7 of the Skini-DIP through a .01uF capacitor, and into pin 1 of the 13008 signal processor. The 13008 operates on an edge-triggering scheme so that the signal may be coupled through a capacitor without losing the capability of responding to DC or low frequency signals. Thresholds are typically 30 mV.

An external resistor (Rext) is required between pins 4 and 13 of the 13008. Its purpose is to drop the +12 supply voltage at pin 13 to a +5V supply at pin 4. This resistor should be in the range of 175 to 200Ω. An external zener diode (such as a 1N5233) may be inserted inplace of the resistor to provide a more constant voltage drop to pin 4. Note that both units can be operated on the same +12V supply line since the Skini-DIP and the 13008 signal processor have internal decoupling circuits. Pin 4 of the Skini-DIP and pin 13 of signal processor should be tied in common to the +12V supply line.

All supply voltages to the 13008 must be fairly "clean" to avoid false triggering. If there is noise on the supply lines, a .01uF capacitor to ground is recommended for by passing the supply voltages at pins 2,4 and 13 of the 13008.

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FIBER OPTIC RECEIVER MODULE

PRELIMINARY DATA

FEATURES

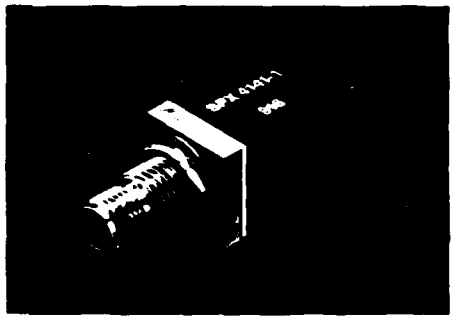
- 10K bits to 10M bit/sec data rates (Manchester)
- No shielding required
- Couples to wide variety of fibers
- Operation on single 5V supply
- Wide dynamic range (28dB)
- Versatile mounting options
- TTL compatible output
- Matched to SPX 4140 Transmitter Module

DESCRIPTION

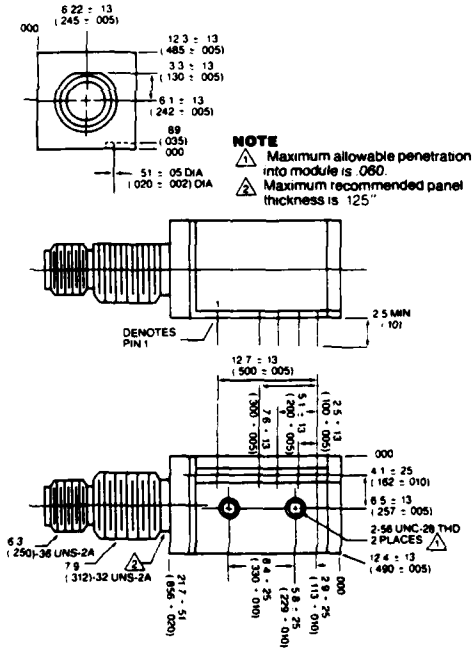
The SPX 4141 receiver module comprises a complete optical receiver for digital point-to point data transmission systems. Input data must be encoded such that its short-term average value is constant, and average duty cycle is fifty percent. Typical implementations of basic Manchester encoding will meet these conditions although certain other coding and formatting options are also satisfactory.

The receiver's PIN diode is integrated into an SMA style optical connector and efficiently couples to a wide variety of plastic or glass fibers. Peak responsivity occurs at 820nm.

Full internal power supply regulation and automatic gain control is provided allowing adjustment-free operation over the full operating temperature range. The output is TTL buffered for direct logic interface.



PACKAGE CONFIGURATION



DIMENSIONS IN MILLIMETERS (INCHES)

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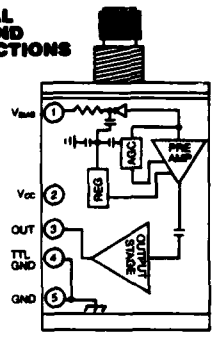
ABSOLUTE MAXIMUM RATINGS

	SPX 4141
Storage Temperature	−55°to +150°C
Case Operating Temperature, Tc	0 to 95°C
Lead Solder Temperature (10 seconds)	260°C
Supply Voltage, V_{CC}	7 Volts
Detector Bias Supply	30 Volts

FUNCTIONAL DIAGRAM AND PIN CONNECTIONS



OPERATING CONDITIONS

PARAMETER	SYMBOL	Min	Max	UNITS
Case Temperature	T_C	0	95°	°C
Supply Voltage	V_{CC}	4.75	5.25	Volts
Logic Output Terminal Loading[5]	I_O		16	mA
Average Input Power SPX4141-1	P_i[4]	.700	250	μW
SPX4141-2		.400	250	μW
Detector Bias	V_{BIAS}	4.75	25	Volts

NOTES:
5. The receiver output will drive 10 TTL loads but the sensitivity of the receiver is reduced as the load is increased from 2 TTL loads and will no longer operate at the specified minimum average optical input power (Pi).

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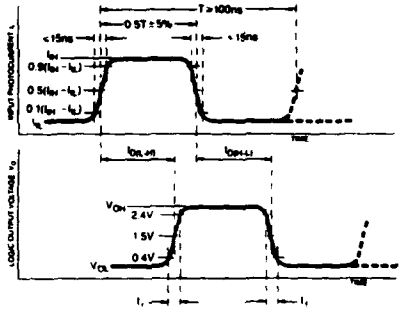
ELECTRO-OPTICAL CHARACTERISTICS

PARAMETER	SYMBOL	Min	Typ	Max	UNITS
High Level Logic Output Voltage	V_{OH}	2.4			Volts
Low Level Logic Output Voltage	V_{OL}			4	Volts
Short Circuit Logic Output[1]	I_{OSC}			-55	mA
Supply Current	I_{CC}		48	55	mA
Logic Output Delay Time[2, 3] Low-to-High High-to-Low	$t_{D(L-H)}$ $t_{D(H-L)}$	5 5	30 30	50 50	ns ns
Logic Output Transition Time Low-to-High High-to-Low	t_r t_f		7 2	10 10	ns ns
Logic Output Pulse Width Distortion[2]	$t_{D(L-H)} - t_{D(H-L)}$		0	7	ns
Logic Output Edge Jitter				3	ns

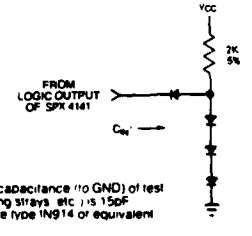
NOTES
1. Specified current flows during momentary connection to GND while input conditions are such that output would be at V_{OH}
2. Values specified are averages for a periodic signal
3. Delay times decrease with increasing input optical power
4. Input power at 10Mb/s (Manchester) for specified edge jitter

PARAMETER	SYMBOL	Min	Typ	Max	UNITS
Optical Aperture Diameter				300	μm
Numerical Aperture	NA			25	
Peak Responsivity Wavelength	λ_p		820		nm

SWITCHING WAVEFORMS



TEST LOAD CIRCUIT



NOTES
1. Shunt input capacitance (to GND) of test circuit (including strays, etc.) is 15pF
2. All diodes are type 1N914 or equivalent

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APPLICATION RECOMMENDATIONS

Mounting Considerations

P.C. Board Mounting

No special shielding is needed except the mounting screws should be used to hold the module to the printed circuit board and these mounting screws should be grounded to the printed circuit board ground.

Warning

Care should be taken that the mounting screws do not extend into the module beyond the maximum allowed penetration depth of .060 inches. Damage may result to components inside module if penetration is beyond the maximum allowed penetration depth.

TTL GND and GND pins should be tied together at pins on the printed circuit board.

Panel Mounting

Recommended maximum panel thickness, .125". Inside the receiver module, the ground is tied to the module metal housing. If a number of receiver modules are panel mounted a ground loop problem may exist. To avoid this problem the receiver module should be electrically isolated from the panel with insulating washers to avoid ground loops.

110 - 0229 - 000
Printed in U.S.A. 7-80

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A division of Honeywell
830 E. Arapaho, Richardson, Texas 75081
(214) 234-4271 Telex 73—0890

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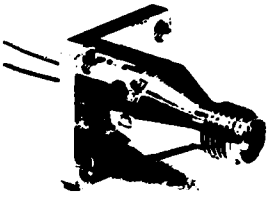
OPTOELECTRONIC COMPONENTS IN FIBER OPTIC RECEPTACLES

FEATURES

- Precision SMA-type interface for efficient coupling
- Comprehensive selection of device types available
- Compatible with single and multifiber cables
- Component electrically isolated from case
- Recessed back for socket clearance

DESCRIPTION

The SPX 3180 and 3190 series consists of two types of Amphenol 905 precision optical receptacles with a permanently mounted LED or photosensor. The receptacles are easily mounted on a module case, enclosure panel, or printed circuit board. The units provide electro-optical signal conversion in a fiber optic data link or data bus system. Both receptacles are plated for good heat sinking, shielding and dimensional stability.



DEVICES AVAILABLE FOR INTEGRATION INTO RECEPTACLES:

LED's
SE 1450
SE 3352 Single Fiber LED
SE 3353 Bundle Fiber LED

Photosensors
SD 1420 Photodiode
SD 3478 PIN photodiode
SD 1440 Phototransistor
SD 1410 Photodarlington
SD 3322 PIN photodiode
SD 3323 DC/1 MHz Detector
SD 3324 Schmitt Detector

ABSOLUTE MAXIMUM RATINGS

(T_{CASE} = 25°C unless otherwise specified)

SPX-3180, 3190

	0	1	2	3	4	5	6	7	8	9	UNITS
Storage Temperature	-65/ +100	-40/ +150	-30/ +125	-65/ +150	-65/ +125	-40/ +100	-65/ +150	-65/ +150	-40/ +150	-40/ +150	°C
Operating Temperature	-65/ +100	-40/ +85	-30/ +70	-65/ +125	-65/ +125	-30/ +70	-65/ +125	-65/ +70	-40/ +85	-40/ +125	°C
Peak Forward Current	120	140	-	-	-	-	-	-	150	-	mA
Reverse Voltage	5	-	+4.5/ +16.0	450	180	15	50	15	-	30	VOLTS
Power Dissipation	-	-	100	-	-	150	50	50	-	-	mW

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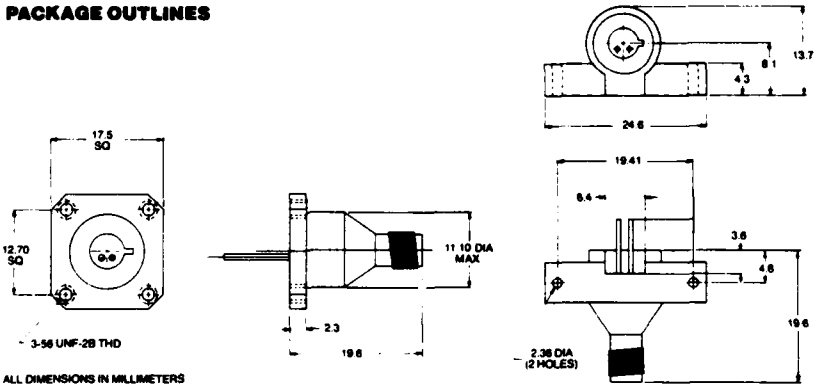
TYPICAL ELECTRICAL/OPTICAL CHARACTERISTICS ($T_{ambient}$ = 25°C)

DEVICE NO.	POWER COUPLED TO FIBER	TEST CONDITION	SOLID FIBER DIAMETER
SPX 3180, 3190	0.1 mW	I_f = 50 mA, NA = 66	1 14 mm
SPX 3181, 3191	0.7 mW	I_f = 100 mA, NA = 24	1 14 mm
SPX 3188, 3198	100 μW	I_f = 100 mA, NA = 34	100 μm

DEVICE NO.	LIGHT CURRENT	TEST CONDITION	SOLID FIBER DIAMETER
SPX 3183, 3193	8 μA	P_f = 50 μW, NA = 66	1 14 mm
SPX 3184, 3194	25 μA	P_f = 50 μW, NA = 24	1 14 mm
SPX 3186, 3196	2 mA	P_f = 50 μW, NA = 66, V = 5V, CE	1 14mm
SPX 3187, 3197	8 mA	P_f = 50 μW, NA = 66, 5 = V, CE	1 14mm
SPX 3189, 3199	12 μA	P_f = 50 μW, NA = 34	100 μm

PACKAGE OUTLINES



ALL DIMENSIONS IN MILLIMETERS

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ORDERING INFORMATION

Select the device best suited for the particular application based on parameters shown in this data sheet and in component data sheets. Detailed characteristics for the available opto devices are listed in separate data sheets. Contact your Spectronics representative for this information. To order receptacles, complete part numbers are determined as follows:

SPX—XXXX—YYY

UNMOUNTED COMPONENT	MOUNTED COMPONENT ASSEMBLY	
	Flange Mount	PC Mount
SE-1450 LED	SPX 3180	3190
SE-3353 Bundle LED	3181	3191
SD-3324 Schmitt Detector	3182	3192
SD-1420 Photodiode	3183	3193
SD-3478 PIN Photodiode	3184	3194
SD-3323 DC/1 MHz Detector	3185	3195
SD-1440 Phototransistor	3186	3196
SD-1410 Photodarlington	3187	3197
SD-3352 Single Fiber LED	3188	3198
SD-3322 PIN Photodiode	3189	3199

CABLES

Spectronics also has available five types of fiber optic cables in user specified lengths, terminated in 905 compatible connectors. The part numbers for these cables are determined as follows:

CABLE TYPE	SPX PART NO.
ITT T433	SPX-4029-XYZ Note
Galileo Galite 2000 type 200T	SPX-3131-XYZ Note
ITT T485	SPX-4539-XYZ Note
Siecor # 142 (single fiber)	SPX-3582-XYZ Note
Siecor # 133	SPX-4577-XYZ Note

For pricing information, contact a Spectronics representative.

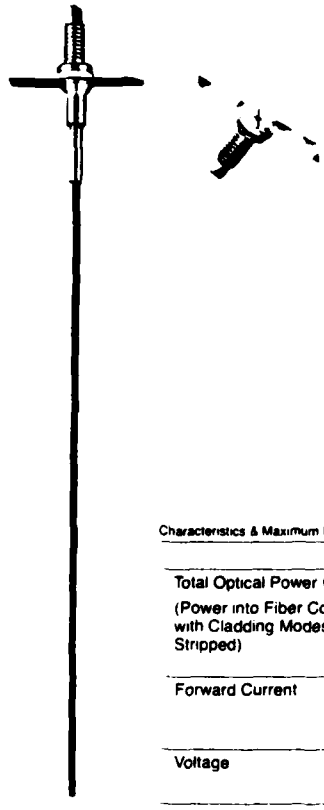
NOTE:
XYZ specifies length where XY are significant digits in centimeters and Z is power of ten multiplier

ORDERING INFORMATION

Dash numbers (YYY) are the same as those assigned to the component mounted in receptacle. Assemblies should be ordered with dash number of desired component.

EXAMPLE:
An SE 3352-003 mounted in a flange receptacle would be ordered as an SPX 3188-003

LASER DIODE



240 μw TYPICAL OPTICAL POWER IN THE CORE OF THE FIBER PIGTAIL

40 MHZ OPTICAL POWER BANDWIDTH

820 nm PEAK EMISSION WAVELENGTH

CUSTOM DEVICES AVAILABLE

Characteristics & Maximum Ratings at 27°C

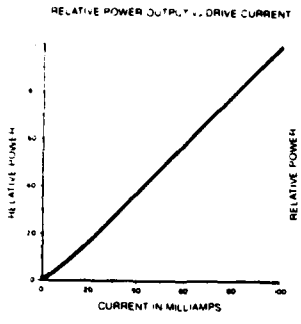
		Symbol	Min.	Typ.	Max.	Units
Total Optical Power Output at 100 MA D.C. (Power into Fiber Core with Cladding Modes Stripped)	* IRE-160	Po	200	300		μw
	** IRE-160FA	Po_{Fiber}	180	240		μw
	*** IRE-160FB	Po_{Fiber}	40	50		μw
Forward Current	D.C.	I_{DC}		100	150	ma
	Pulsed (1μ sec, 10^5PRF)	I_{PM}			750	ma
Voltage	Forward at 100 MA D.C.	V_F		2.0		volts
	Reverse	V_R			3.0	volts
Peak Wavelength of Emission		λP	see below	820	see below	nm
Spectral Width (50% points)		$\Delta\lambda$		40		nm
Bandwidth — Optical Power 3db points I_F = 20 ma D.C., 20 ma peak-to-peak				40		MHz
Rise Time of Optical Flux		T_R		14	20	ns
Operating & Storage Temperature		T_C	-40		-85	C

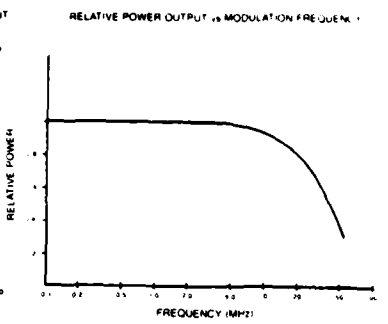
* IRE-160 — Without Fiber Pigtail with Exposed Emitting Surface into 17° Half Angle

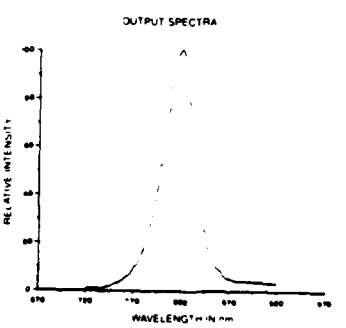
** IRE-160FA — With 0.48NA 100μm Core 125μm O.D. Step Index all Glass Fiber Pigtail

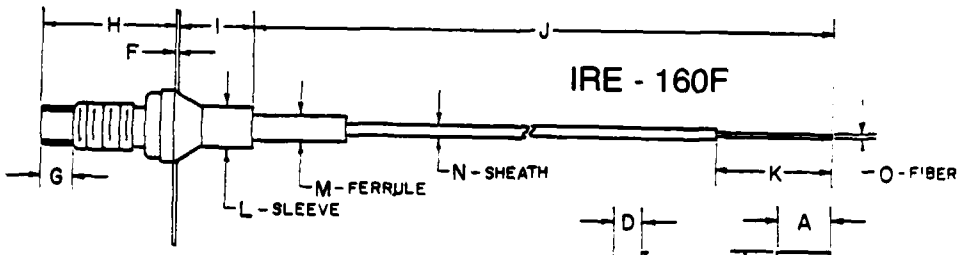
*** IRE-160FB — With 0.22 NA 55μm Core 125μm O.D. Graded Index all Glass Fiber Pigtail

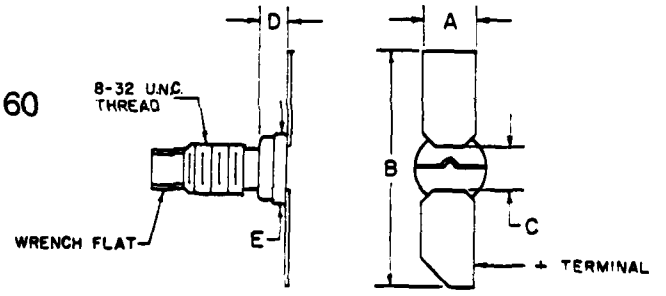
Wavelength Selection: Standard wavelength is between 805 nm and 835 nm. Wavelengths from 790 nm to 880 nm are available on special order.











DIMENSIONAL CHART IRE-160, IRE-160(F)

SYMBOL	INCHES TYP	MILLIMETERS TYP
A	225	5 71
B	875	22 22
C	185	4 69
D	060	1 52
E	275	6 98
F	005	12
G	115	2 92
H	500	12 70
I	330	8 38
J	12 00	304 80
K	1 00	25 40
L	155	3 93
M	098	2.48
N	040	1 01
O	006	125

LASER DIODE
LABORATORIES, INC
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LD-579-R

DF331A DF332A DF334A

CMOS μ-255 law CODEC set *designed for . . .*

Siliconix

- **Channel Banks**
- **Central Offices and PABXs**
- **Microprocessor Interface**
- **Remote Data Acquisition Systems**
- **Audio Delay Lines**

BENEFITS

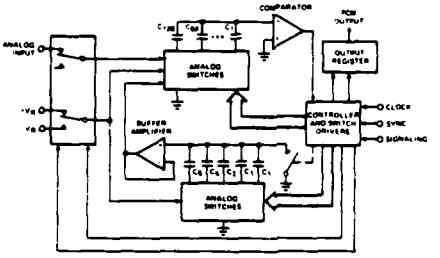
- **Minimizes System Power Requirements**
  - Standby Power 11 mW Typ
  - Typical Power 80 mW
- **Reduces External Component Requirements**
- **Reduces System Costs**
- **Easily Interfaced**
- **Eliminates Channel Crosstalk Problems**
- **Eliminates External Signalling Logic**
- **No External Zero Code Suppression Required**
- **Reduced System Noise Problems**
- **No External Sample and Hold or MUX Required**
- **No Additional Logic Required for Extended Bandwidth Applications**
  - 3.5 to 9 KHz Bandwidth Possible With Clock Frequency From 1.25 to 3.0 MHz

DESCRIPTION

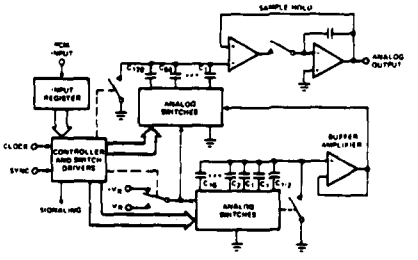
The DF331A coder is an A/D converter which has a transfer characteristic conforming to the telecommunication industry μ-255 law. Its counterpart, the DF332A or DF334A (decoder) is a D/A converter which also conforms to the μ-255 law.

Together the DF331A and DF332A or DF331A and DF334A form a CODEC (coder-decoder set) which is designed to meet the needs of the telecommunications industry for per channel voice frequency CODECs used in PCM Channel Bank and PBX systems. Digital output and input of the coder and decoder is in serial format. Actual transmission and reception of 8-bit data words containing the analog information is typically done at a 1.544 megabit/sec rate with analog signal sampling occurring at an 8 KHz rate. A sync pulse input pin is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line. The DF332A and DF334A differ in the output device for the A/B signal output pins, refer to the Functional Description. The devices have TTL logic input levels of 0.6 V and 3.4 V that are compatible with TTL logic using a pullup resistor to +5 V, they directly interface to CMOS logic.

FUNCTIONAL BLOCK DIAGRAMS



DF331A

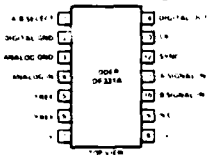


DF332A, DF334A

Figure 1

PIN CONFIGURATIONS

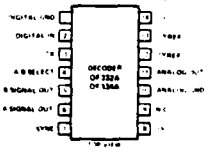
Dual In-Line Package



PLASTIC DIP
ORDER NUMBER: DF331ACJ
SEE PACKAGE 7

CERAMIC DIP
ORDER NUMBER: DF331ACP
SEE PACKAGE 11

Dual In-Line Package



PLASTIC DIP
ORDER NUMBER: DF332ACJ, DF334ACJ
SEE PACKAGE 7

CERAMIC DIP
ORDER NUMBER: DF332ACP, DF334ACP
SEE PACKAGE 11

ABSOLUTE MAXIMUM RATINGS

V_{in} (Digital Inputs) . . . $-0.3\ V, \leq V_{in} \leq +V + 0.3\ V$
V_{in} (Analog Inputs) . . . $-V - 0.3\ V, \leq V_{in} \leq +V + 0.3\ V$
$+V$ . . . $0 \leq +V \leq 11\ V$
$-V$ . . . $-11\ V \leq -V \leq 0$
$+V_{ref}$ . . . $-V \leq +V_{ref} \leq +V$
$-V_{ref}$ . . . $-V \leq -V_{ref} \leq +V$

V_O (Digital Output) DF331A, DF334A . . $-0.3V \leq V_O \leq 15V$
$V_{A/B}$ Signal Out DF332A . . . $+V + 0.3\ V \geq V_O \geq -7.5\ V$
Operating Temperature . . . 0 to 70°C
Storage Temperature . . . −55 to +125°C
Power Dissipation . . . 450 mW
Derate 6.5 mW/°C above 25°C

Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters to assure conformance with specifications.

		Characteristic		$T_A = 25°C$ Min	Typ Note 1	Max	Unit	Test Conditions, See Note 2 Clock = 1.544 MHz, Sample Rate = 8 KHz, +V = 7.5 V, $-V_{ref}$ = −3.0 V, −V = −7.5 V, $+V_{ref}$ = 3.0 V, R_L = 820 Ω, C_L = 12.5 pF
DC Characteristics DF331A (Coder)								
1	INPUTS	I_{in} (Analog)	Analog Input Current		0.5		mA	See Note 3
2		I_{inL} (Clock)	Clock Input Low Current		−0.1	−100	nA	V_{IN} = 0
3		I_{inL} (Sync)	Sync Input Low Current		−0.1	−100		
4		I_{inH} (Clock)	Clock Input High Current		0.1	100		V_{IN} = 7.5 V
5		I_{inH} (Sync)	Sync Input High Current		0.2	100		
6		R_{in} (Analog)	Analog Input Series Resistance		1		KΩ	Present During Sampling Time Only
7		C_{in} (Analog)	Analog Input Series Capacitance		200		pF	
8		V_{offset}	Analog Input Offset Voltage		5	10	mV	
9	OUT	C_O (Digital)	Digital Output Capacitance		3		pF	V_O = 7.5 V
10		V_{OL}	Digital Output Low Voltage		0.3	0.5	V	I_{OL} = 3 mA
11		V_{OH} (max)	Digital Output High Voltage			12		I_{OH} = 10 μA
12	SUPPLY	I^+	Positive Supply Current		2.5	6	mA	Clock = 1.544 MHz Sample Rate = 8 KHz
13		I^-	Negative Supply Current		−2	−6		
14		I^+_{stdby}	Standby Positive Supply Current		0.6			Analog Ground (Pin 3) Open
15		I^-_{stdby}	Standby Negative Supply Current		−0.05			
16			Supply Tolerance		±10		%	
17		I_{ref}^+	Positive Reference Current		3.5		μA	Average Current See Note 3
18		I_{ref}^-	Negative Reference Current		−3.5			
AC Characteristics DF331A (Coder)								
19	DYNAMIC	t_{ds}	Sync to Clock Delay Time			100	ns	See Figure 2
20		$t_{d(on)}$	Digital Output to Sync Delay Time		75	130		
21		$t_{d(off)}$	Digital Output to Sync Delay Time		165	220		
22		t_{dbr}	Digital Output to Clock Delay Time		65	130		
23		t_{dbf}	Digital Output to Clock Delay Time		70	130		
24		t_{fo}	Digital Output Fall Time		65	130		C_L = 100 pF
25		t_{ro}	Digital Output Rise Time		175	250		
26		t_{ss} (min)	A/B Signaling Input Setup Time			200		See Figure 4
27		t_{scs} (min)	A/B Select Setup Time			1000		
28		DC_C	Clock Duty Cycle	30		70	%	
29		t_{conv}	Complete A/D Conversion (Sampling, Data Storage, Resetting)			168	clocks	

ELECTRICAL CHARACTERISTICS (Cont'd)

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters to assure conformance with specifications.

		Characteristic		T_A = 25°C Min	Typ Note 1	Max	Unit	Test Conditions, See Note 2: +V = 7.5 V, V = -7.5 V, V_{ref} = 3.0 V, V_{ref} = -3.0 V, Clock = 1.544 MHz, Sync = 8 KHz Period, 8 Clock Pulses Wide
		DC Characteristics DF332A, DF334A (Decoder)						
1	IN	I_{inL} (Logic)	Digital Inputs Low Current		-0.1	100	nA	V_{in} = 0
2	IN	I_{inH} (Logic)	Digital Inputs High Current		0.1	100	nA	V_{in} = 7.5 V
3	OUT	I_{OL} (Signaling)	A/B Output Low Current — DF332A Only		0.1	100	nA	V_{OL} = 0
4	OUT	I_{OH} (Signaling)	A/B Output High Current — DF332A Only	0.2	0.5		mA	V_{OH} = 6.5 V
5	OUT	V_{OH} (max) (Signaling)	A/B Output High Voltage — DF334A Only			12	V	I_{OH} = 10 µA
6	OUT	V_{OL} (Signaling)	A/B Output Low Voltage — DF334A Only		0.3	0.5	V	I_{OL} = 1.5 mA
7	OUT	C_L (Analog)	Analog Output Load Capacitance			100	pF	
8	OUT	R_O (Analog)	Analog Output Series Resistance		50	150	Ω	See Input/Output Schematics See Note 4
9	OUT	V_{offset}	Analog Output Offset Voltage		50	100	mV	
10	SUPPLY	I^+	Positive Supply Current		3.5	8	mA	
11	SUPPLY	I^-	Negative Supply Current		2.5	-7	mA	
12	SUPPLY	I^+_{stdby}	Standby Positive Supply Current		0.8		mA	Analog Ground (Pin 10) Open
13	SUPPLY	I^-_{stdby}	Standby Negative Supply Current		-0.07		mA	Analog Ground (Pin 10) Open
14	SUPPLY		Supply Tolerance		±10		%	
15	SUPPLY	I_{ref}^+	Positive Reference Current		3.5		µA	Average Current See Note 3
16	SUPPLY	I_{ref}^-	Negative Reference Current		3.5		µA	Average Current See Note 3
		AC Characteristics DF332A, DF334A (Decoder)						
17	DYNAMIC	t_{ds}	Sync to Clock Delay Time	25		450	ns	See Figure 3
18	DYNAMIC	t_{dc}	Clock to Sync Delay Time	10			ns	See Figure 3
19	DYNAMIC	t_{sd}	Data to Clock Setup Time	100			ns	See Figure 3
20	DYNAMIC	t_{scs} (min)	A/B Select Setup Time			1000	ns	See Figure 5
20	DYNAMIC	t_{dd}	A/B Output Delay Time		5	10	µs	See Figure 5
21	DYNAMIC	t_{do}	Analog Output to Sync Delay Time			15	µs	See Figure 3
22	DYNAMIC	Slew*	3 V to +3 V Analog Output Slew Rate		5		V/µs	C_L = 100 pF
23	DYNAMIC	Slew	+3 V to -3 V Analog Output Slew Rate		5		V/µs	C_L = 100 pF
24	DYNAMIC	Droop	Analog Output Droop Rate		0.01		%/µs	
25	DYNAMIC	t_{conv}	Complete D/A Conversion (from Data Input, to Analog Output and Internal Resetting)			39	clocks	
		System Characteristics, Per Individual Part: DF331A, DF332A, DF334A						
26	SYSTEM	S/D	Signal to Total Distortion Total of Quantizing Noise, Thermal Noise and Harmonic Distortion with Sinusoidal Input and C Message Weighting Filter See Note 5	35	39		dB	P_{in} = 0 to -30 dBmO; f_{in} = 1020 Hz, +3 dBmO = 3 V Peak into Coder
27	SYSTEM	S/D		30	34		dB	P_{in} = -40 dBmO; f_{in} = 1020 Hz, +3 dBmO = 3 V Peak into Coder
28	SYSTEM	S/D		25	30		dB	P_{in} = -45 dBmO; f_{in} = 1020 Hz, +3 dBmO = 3 V Peak into Coder
29	SYSTEM	G_T	Gain Tracking Deviation of Gain from 0 dBmO Input Sinusoidal Signal	-0.25	±0.15	+0.25	dB	P_{in} = +3 to -40 dBmO; f_{in} = 1020 Hz, +3 dBmO = 3 V Peak into Coder
30	SYSTEM	G_T		-0.5	±0.15	+0.5	dB	P_{in} = -40 to -50 dBmO; f_{in} = 1020 Hz, +3 dBmO = 3 V Peak into Coder
31	SYSTEM	G_T		-1.5	±0.25	+1.5	dB	P_{in} = -50 to -55 dBmO; f_{in} = 1020 Hz, +3 dBmO = 3 V Peak into Coder
	SYSTEM	G_T	Deviation of Gain from -10 dBmO, White Noise Source Signal Input	-0.25	±0.1	+0.25	dB	P_{in} = -10 to -55 dBmO; f_{in} = 1020 Hz, +3 dBmO = 3 V Peak into Coder
	SYSTEM	G_T		-0.5	±0.2	+0.5	dB	P_{in} = -55 to -60 dBmO; f_{in} = 1020 Hz, +3 dBmO = 3 V Peak into Coder
32	SYSTEM	N_{IC}	Idle Channel Noise Coder (DF331A) to Decoder (DF332A or DF334A) of Known Quiet Code Output		12	15	dBrncO	V_{in} = 0
33	SYSTEM	N_{QC}	Quiet Code Output Output of Decoder (DF332A or DF334A) for +0 V Equivalent Digital Input Coder		10	12	dBrncO	Digital In = All "1" (Corresponds to +0 V Input)

NOTES

1. Typical values are for Design Aid only and not subject to production testing
2. $V_{in} \geq 3.4$ V for logic "1" $V_{in} \leq 0.6$ V for logic "0" for logic input levels
3. Peak currents of up to 2 mA occur during reconstruction of Analog Output and during encoding of Analog Input
4. Use of a load resistance ≥ 10K Ω is recommended to avoid output attenuation
5. Specifications are for pair (coder and decoder)

DF331A ICBL-II
DF332A ICBM-II-A
DF334A ICBM-II-B

FUNCTIONAL DESCRIPTION

Analog Input (Coder DF331A): The analog input accepts signals which have peak amplitudes less than the value of the voltage references, and which are bandlimited to less than 1/2 of the CODEC sample rate.

Digital Output (Coder DF331A): The digital output of the encoder is an 8-bit serial bit stream which is a sign-plus-magnitude binary representation of the analog input. This output is an open drain N-channel output, which allows for easy wire-OR multiplexing.

Sync Input (Coder and Decoder): The sync input accepts a sync pulse which should be 8 clock periods wide. The period of the sync pulse sets the sample rate. The sync pulse causes the encoder to serially shift its digital output data out at a rate equal to that of the clock, and it causes the decoder to accept the serial digital data.

Clock Input (Coder and Decoder): The clock input accepts a clocking signal which sets the data transmission rate for the CODEC, and also provides the clocking of the internal CODEC logic. Typical clock rate is 1.544 MHz.

Digital Input (Decoder DF332A, DF334A): The digital input accepts the 8-bit serial data output of the encoder upon reception of the sync pulse.

Analog Output (Decoder DF332A, DF334A): The analog output of the decoder is in the form of voltage steps having a width equal to the inverse of the sample rate, with amplitude equal to the value of the sample of the signal taken at the encoder analog input.

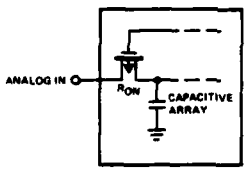
Reference Voltage Inputs (Coder and Decoder): Positive and negative DC reference voltages are required for both encoding and decoding. The maximum analog signal swing is set by the reference voltages.

Signaling Inputs and A/B Select (Coder DF331A): Two signaling inputs A and B are provided on the encoder allowing insertion of digital signaling data into the transmitted bit stream, which allows telecommunications users to transmit digital signaling information along with the data stream. When signaling is enabled, the voice signal is encoded with only 7 bits, the 8th bit being used for signaling. The signaling function is enabled by the application of a transition to the A/B select input. A positive transition at the A/B select input will insert the data at the A input into the 8th bit (the LSB) position in the transmitted word, whereas a negative transition will insert the data at the B input into the 8th bit position in the transmitted word. Refer to the timing diagram in Figure 4. To disable signaling function, simply tie the A/B select input to logic high or low, so that no transitions appear.

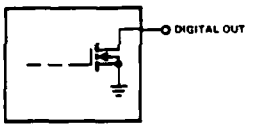
Signaling Outputs and A/B Select (Decoder DF332A, DF334A): Two outputs are provided on the decoder to output the signaling data. Application of a positive transition to the A/B select input places the 8th bit (the LSB) of the transmitted word at the A signaling output. Application of a negative transition to the A/B select input places the LSB at the B signaling output. These outputs are open drain P-channel outputs on the DF332A and are open drain N-channel outputs on the DF334A. Refer to output schematic for configuration, and to Figure 5 for timing waveforms.

INPUT-OUTPUT CIRCUIT SCHEMATICS

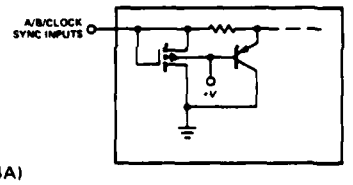
Analog Input (DF331A)



Digital Output (DF331A)

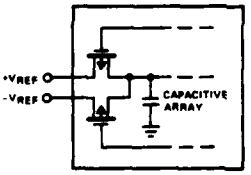


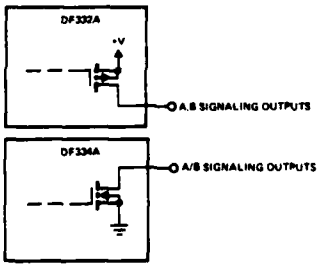
Digital Inputs



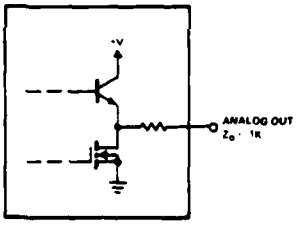
A/B Signaling Outputs (DF332A, DF334A)

Reference Inputs



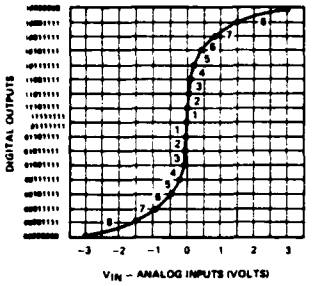


Analog Output (DF332A, DF334A)

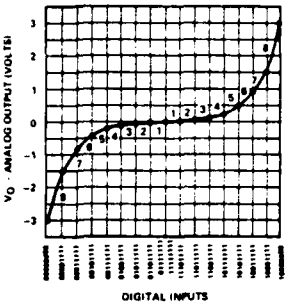


TYPICAL CHARACTERISTICS

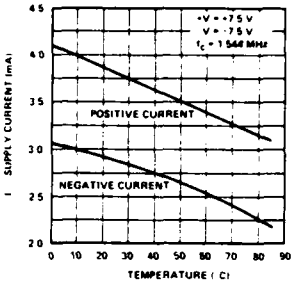
DF331A μ-Law Coder Transfer Characteristic



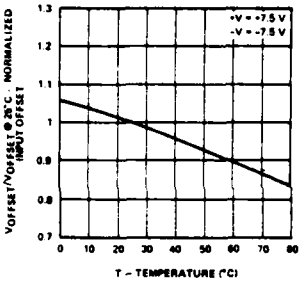
DF332A μ-Law Decoder Transfer Characteristic



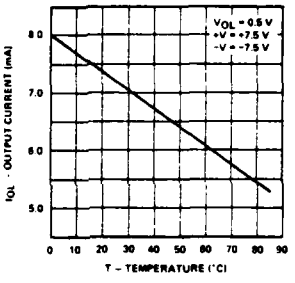
Positive and Negative Supply Current vs Temperature DF331A



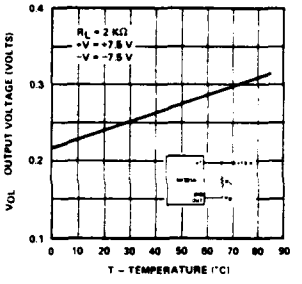
Normalized Input Offset vs Temperature DF331A



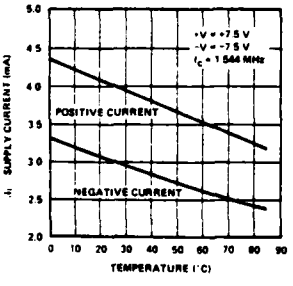
Digital Output Low Current vs Temperature DF331A



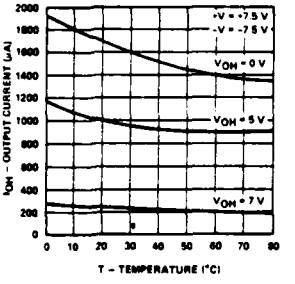
Digital Output Low Voltage vs Temperature DF331A



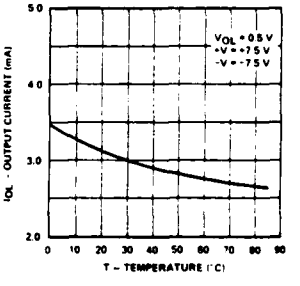
Positive and Negative Supply Current vs Temperature DF332A, DF334A



A/B Signaling Output Current vs V_{OH} and Temperature DF332A Only

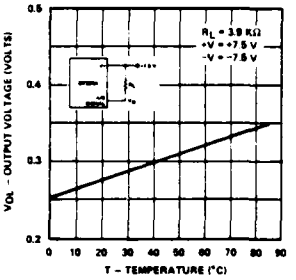


A/B Signaling Digital Output Low Current vs Temperature DF334A

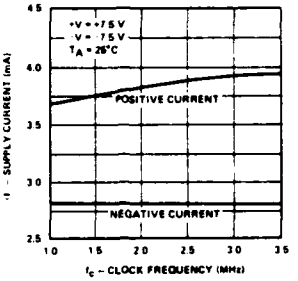


TYPICAL CHARACTERISTICS (Cont'd)

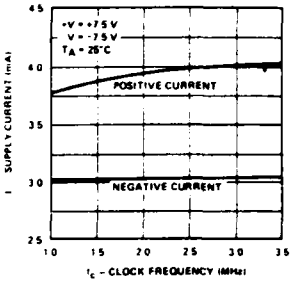
A/B Signaling
Digital Output Low Voltage
vs Temperature
DF334A



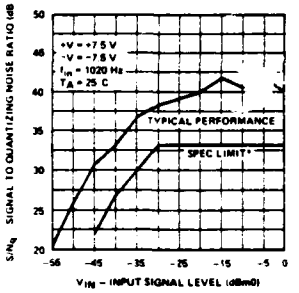
Positive and Negative
Supply Current
vs Clock Frequency
DF331A



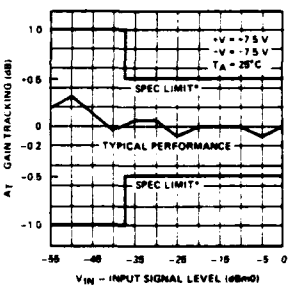
Positive and Negative
Supply Current
vs Clock Frequency
DF332A, DF334A



Signal to Quantizing Noise Ratio
vs Input Level
DF331A/DF332A or DF331A/DF334A Pair



Gain Tracking
vs Input Level
DF331A/DF332A or DF331A/DF334A Pair



*SPECIFICATION LIMITS FROM A T T CHANNEL BANK D-3 SPEC

APPLICATIONS INFORMATION

Positive and negative voltage references should be bypassed to analog ground with a 10 μF capacitor to supply the peak currents required (up to 2 mA) during sampling. Inadequate bypassing may cause sampling inaccuracy and crosstalk between adjacent channels. The absolute value of the voltage references should match and track each other to prevent asymmetry in the analog waveforms. The recommended reference value is ±3.0 V. Increasing this level may increase harmonic distortion in the CODEC, while decreasing the references will lower the system dynamic range.

The sync pulses to the decoder and encoder should be staggered as in Figure 6. The sync to the decoder precedes the sync to the encoder by one half of a clock period to allow for the delay times which can occur if the sync pulse is derived from the clock. If all syncs and clocks are coincident without delay, then the staggering is unnecessary.

All digital inputs will work when driven from TTL logic providing that the outputs of the TTL gates are pulled up to the 5.0 V TTL supply.

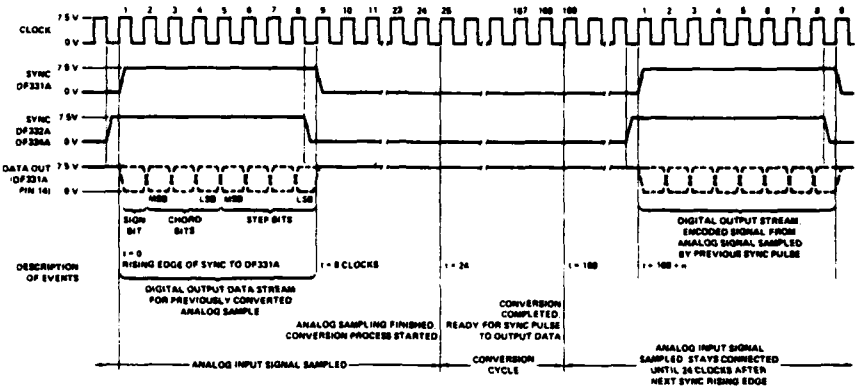
The sample rate of the CODEC is determined by the clock rate and the period between sync pulses. The minimum period between sync pulses is 168 clock periods, which is the time that the encoder requires to complete an analog-to-digital conversion (see Figure 6). The maximum clock rate for a functional system is 3.0 MHz. The actual sample rate of the CODEC is equal to the inverse of the period between sync pulses.

Zero code suppression is included in the A/D conversion to prevent the transmission of an all zeroes digital output code, which could cause a repeater to go down in a telecommunications system. Should an all zeroes code result from the A/D conversion (indicating a negative overvoltage condition), then bit 7 in the data stream is forced to a logic "1".

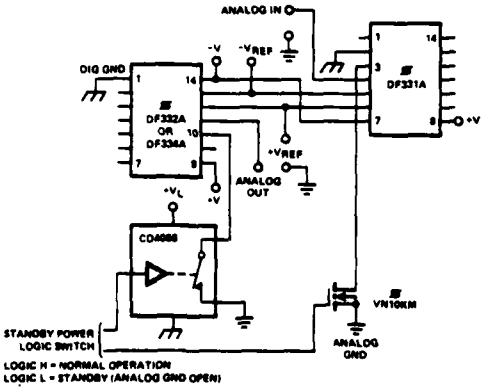
Open drain signaling outputs on the decoder allow easy interface to logic. The open drain P-channel of the DF332A allows a pull-down to ground or a negative voltage ($V_O \geq$ −7.5 V absolute max) giving logic compatibility with CMOS or other MOS logic. The open drain N-channel of the DF334A allows a pull-up to a positive supply (e.g., +5 V for TTL or up to +12 V for CMOS). This output has logic low level near ground making it compatible with TTL or CMOS logic.

APPLICATIONS INFORMATION

The CODECs can be put into a lower power standby condition. For standby, analog ground lines are open circuited. Relays or FET switches can be used. Figure 7 shows one implementation for standby switching. For the encoder (DF331A) the switch must be low $R_{DS(ON)}$ (<25 Ω) and have very low total offset voltage (<5 mV at 200 μA current). The VMOS switch shown (VN10KM) achieves these requirements. The decoder is not as critical, offset voltage should be minimized (<50 mV); use of a CD4066 CMOS switch is satisfactory.



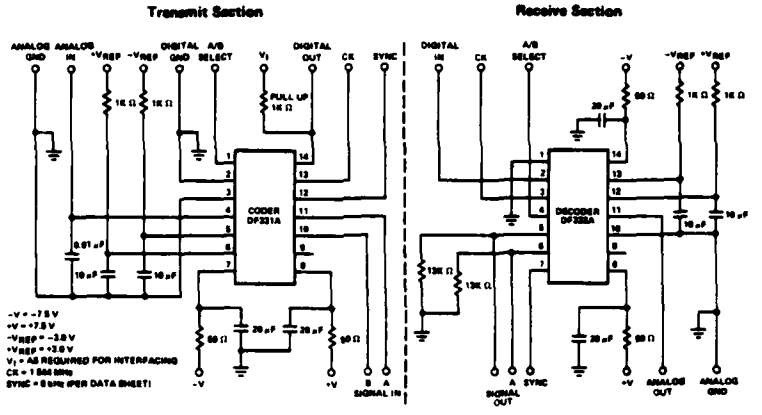
CODEC Timing Relationships
Figure 6



Coder/Decoder Circuit with Switches for Standby Power Condition
Figure 7

APPLICATIONS

Typical Coder/Decoder Circuit Configurations



Siliconix

Function/Application of the DF331/332 New Companding Converter Chip Set

Thomas J. Mroz

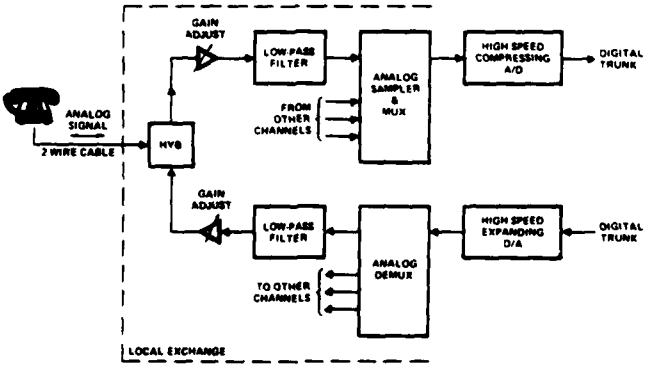
INTRODUCTION

The DF331/332 CODEC (coder/decoder) chip set offers the telecommunications industry an alternative in classical channel bank designs and a spectrum of application solutions outside of telecommunications.

Being the first commercially produced CMOS A/D, D/A converters to use a conversion technique incorporating a binary weighted capacitive array, the DF331/332 offer low power consumption, 12-bit resolution about zero and 72 dB dynamic range.

Telecommunications

Historically, the approach to doing the A/D and D/A conversion of the analog voice signals was as shown in Figure 1. This approach required the use of a high speed coder and decoder sampling at a 24 x 8 KHz rate for a 24 channel system. Because of analog multiplexing and demultiplexing this system was susceptible to crosstalk problems. Introduction of the Siliconix DF331/332 converters offers the channel bank designer an alternative system which replaces the high speed, high cost converters previously required with a low speed, low cost, high performance per channel LSI circuit. In this new system (Figure 2), each line of analog voice is individually coded or decoded by a dedicated converter. Multiplexing is now done after coding and demultiplexing on the receiving end is done prior to the D/A conversion. This approach virtually eliminates crosstalk between adjacent channels. Filter type, positioning and number remains the same as in the shared converter systems.



PCM in Existing Systems
Figure 1

Coding and Decoding

The μ-255 law, which is currently is use in the U.S., defines the transfer characteristic to be used in doing the analog (voice) to digital conversion in a telecommunication channal bank. The μ-255 law itself is defined by the equation.

$$F_{|x|} = S_{gn}(x) \frac{\ln(1 + \mu|x|)}{\ln(1 + \mu)}$$

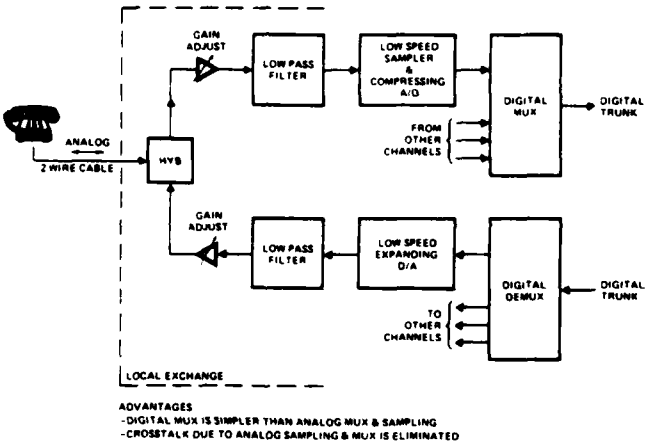
where $\mu = 255$.

Actual representation of the equation is done in a piecewise linear fashion. Thus, the transfer curve is comprised of 16 sections called chords, each of which contains 16 discrete steps (Figure 3). Decoding (Figure 4) is accomplished by implementation of the inverse transfer characteristic.

Pulse code modulation (PCM) is the method by which information is transferred between sending and receiving channel banks. The output of the A/D converter consists of an eight bit digital word which is the resultant of an analog sample. Sampling occurs at an 8 KHz rate while data transfer is done at 1.544 MHz. Maximum sampling frequency for the DF331 is 16 KHz when using a 3.088 MHz clock frequency.

Digital output of the DF331 is structured as a sign bit + magnitude (7 bits) word. Of the 7 bits following the sign the first three are dedicated to chord selection while the last four indicate which of the 16 steps within each chord contains the analog sample.

Decoding with the DF332 can be done at up to a 32 KHz rate while still using a 1.544 MHz clock.



Use of PCM with Per Channel CODEC
Figure 2

DF331 μ-Law Coder Transfer Characteristic

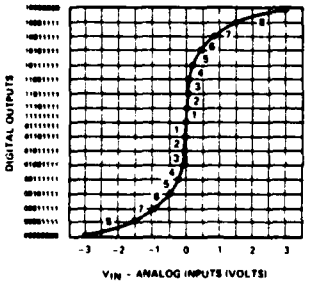


Figure 3

DF332 μ-Law Decoder Transfer Characteristic

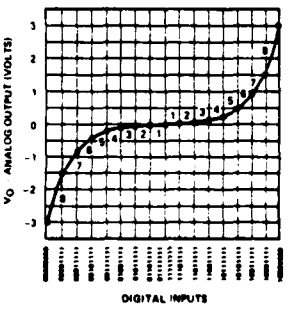


Figure 4

Non-linearity of the transfer characteristic results in a nearly constant signal to Quantizing Noise (S/Nq) ratio over a wide range of analog voice amplitudes (Figure 5). This, in telephone applications, makes possible a high degree of intelligibility when someone is speaking softly or very loudly into a phone. A linear transfer characteristic would result in a constant decay of voice quality as signal levels decreased.

A/D, D/A Conversion Algorithms

Actual conversions (A/D, D/A) are accomplished through the use of capacitive arrays on board the DF331 and DF332. For purposes of this discussion the array which is used to determine the chord in which the sample lies will be called the X-array. Steps are determined by a second array called the Y-array. The X-array contains 256 capacitors which are connected in a binary weighted fashion. The Y-array contains 16 capacitors connected in a like manner (Figure 6). Care was taken in layout to minimize edge effects which could cause mismatch between these capacitors. Top plates (metal) of all capacitors are common and are connected to one of the inputs of a comparator. The other comparator input is analog ground. Bottom plates of the capacitors of the array can be switched between V_{IN}, $+V_{REF}$, $-V_{REF}$ and ground. Principle steps in doing an A/D conversion are:

1. Acquire sample.
2. Determine sign.
3. Determine chord.
4. Determine step within the chord.
5. Load output shift register.
6. Reinitiate the system and return to sample mode.
7. Output data (digital).

During sampling the top (metal) plate of the capacitor array is connected to ground. The entire array is then charged to the input signal voltage via an analog switch. After sampling is complete, the switch grounding the top plate of the array is opened and the bottom plates of all capacitors are switched to ground. The top plate, being the input to a comparator, now has $-V_{IN}$ as a voltage. Sign of the input is determined by examining the comparator output.

Upon determination of the sign the selection of the appropriate reference is made. Chords are now selected by throwing the switches at the bottom plates of the capacitors, in a successive approximation manner, to the reference chosen while monitoring the comparator output.

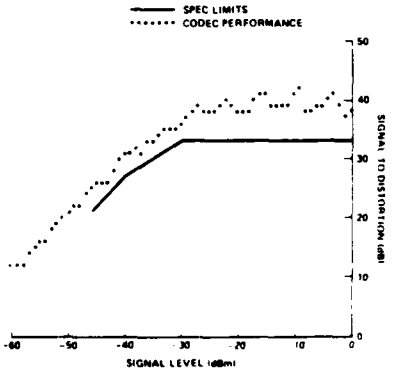
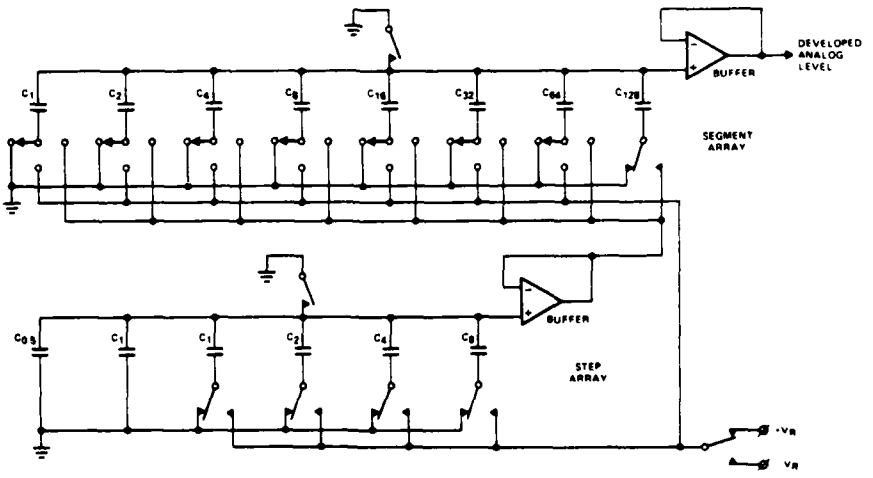


Figure 5



D to A Converter Based on Capacitive Ladders
Figure 6

During these steps the voltage at the top plate of the array is defined by the equation:

$$V_O = \frac{C_A}{C_A + C_B} \times V_r - V_{IN}$$

where C_A is the equivalent capacitance being switched to the reference and C_B is the equivalent capacitance remaining switched to ground. Since the capacitors are binary weighted C_{X8} equals 128 C_X. As an example then, if C_{X8} was switched to the reference, the comparator would see,

$$\frac{128\,C_X}{128\,C_X + 127\,C_X} \times V_r - V_{IN} \text{ or } \frac{128}{255} \times V_r - V_{IN}$$

which also indicates that the reference will be the same in polarity as the sample. The comparator output not changing after switching C_{X8} would indicate that the sample lies in the 8th chord

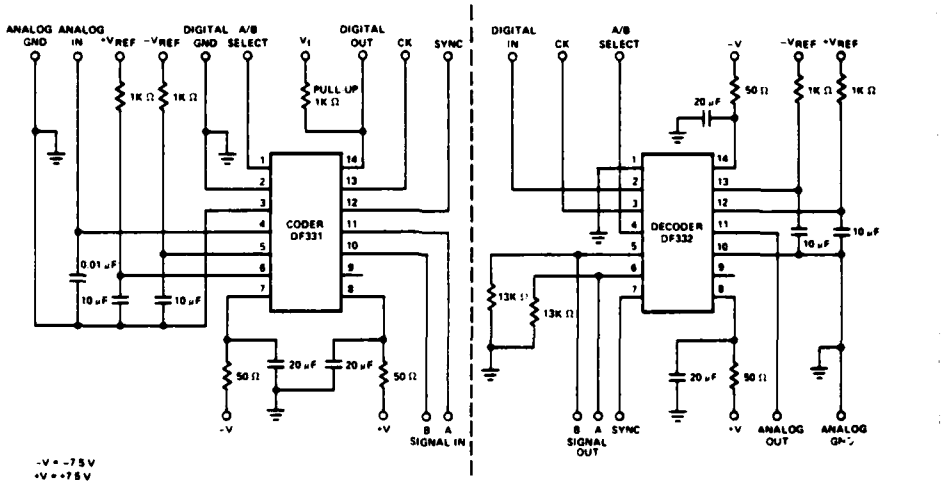
Step value is determined by switching the X-array capacitor indicating chord from the reference to the Y-array buffer output. Successive approximation techniques are again used to develop a step voltage. A fraction of this voltage, as determined by the X-array, appears at the comparator input. Transitions of the comparator output are monitored until the step value is determined.

After these determinations are made, the 8 bit binary word corresponding to the switch positions is loaded into the output shift register. The entire conversion system is then reinitiated and goes into a sampling mode.

The next sync pulse presented to the encoder transmits the previous data and starts the sequence over again.

General Considerations When Using the DF331/332

When using the DF331/332 in communication systems it is necessary to bypass certain pins to ground to reduce noise injection into the converters which could be detrimental to system performance. Figure 7 shows suggested external components to be used on a D_3 channel bank card. Important to note, is that references are bypassed to analog ground rather than digital ground. This prevents digital noise from being coupled into the reference pins. Analog ground must be connected to digital ground at some point. It's preferable that this point be at the supply or near, to prevent current flow through the analog ground, which would introduce offsets and noise at the analog input. Decoupling of coders and decoders is accomplished with the 50 Ω/20 μF networks in series with the supplies and the 1K/10 μF networks in series with the references This circuit is typical of a D_3 channel having an 8 KHz sample rate.



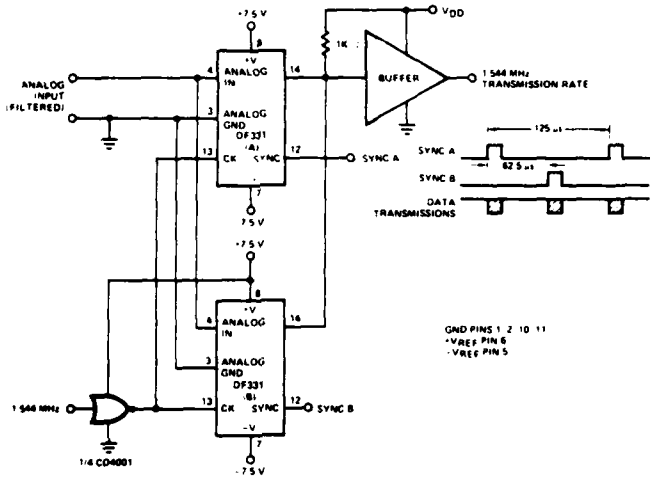
-V = -7.5 V
+V = +7.5 V
VREF = -3.0 V
+VREF = +3.0 V
VI = AS REQUIRED FOR INTERFACING
CK = 1.544 MHz
SYNC = 8 kHz (PER DATA SHEET)
LOGIC LEVELS = 0–7.5 V

Transmit Section | Receive Section

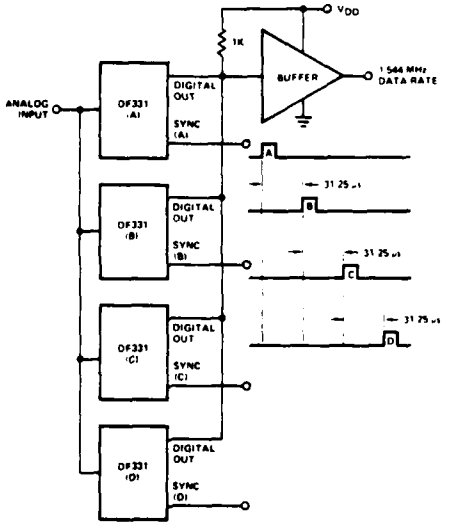
Typical D_3 Channel (Less Filters)
Figure 7

APPLICATIONS

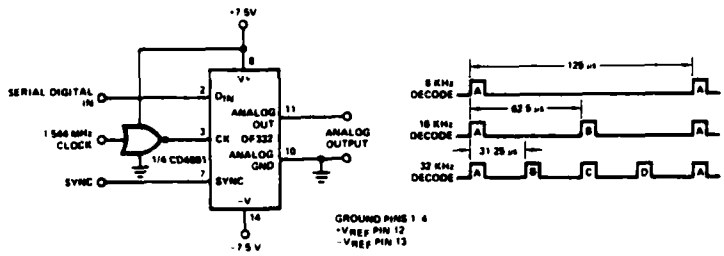
Circuits for various bandwidth requirements are shown in Figures 8, 9, 10 and 11. There exists several ways of achieving bandwidths wider than the 4 KHz required for a D_3 channel bank. Most obvious is a simple doubling of the clock frequency which allows a doubling of the sample rate. Therefore, a 3.088 MHz clock enables the use of a 16 KHz sample rate. The higher clock rate can prevent the use of CMOS in external circuitry, however, and the circuit of Figure 8 may become more economical from a power stand point. This circuit incorporates the 1.544 MHz, or slower clock rate by using multiple coders which are alternately sampling to accomplish a 16 KHz sample rate. This same technique can be expanded to perform a 32 KHz sample rate while needing only one decoder, Figure 10, to perform the D/A conversion. This is possible since decoding takes roughly a quarter of the time coding requires. Time for coding and decoding is directly related to a fixed number of clocks. Therefore, doubling of the clock frequency enables the use of a sync pulse rate twice as rapid as previously used. A minimum clock rate of around 700 KHz sets the lower limit for data transmission. No such limit exists for sample rate, however.



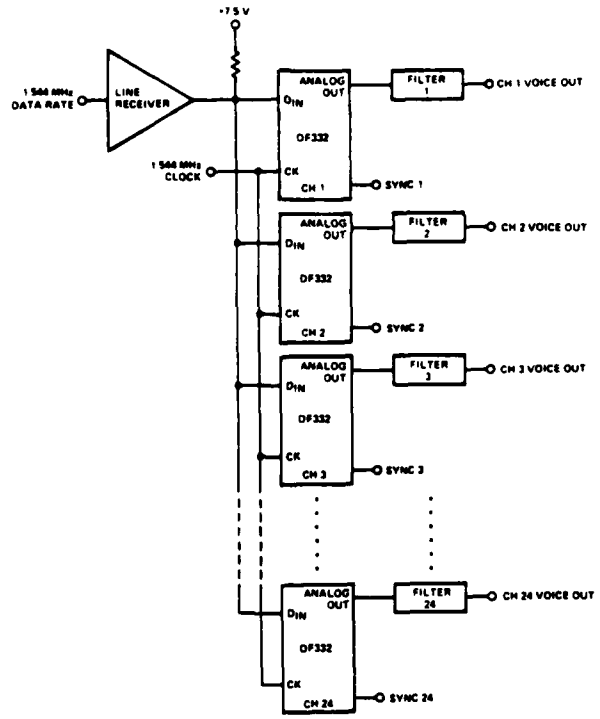
Multiple Coders for 16 kHz Sampling Rate
Figure 8



Multiple Coders for 32 kHz Sampling Rate
Figure 9



Basic Circuit for Decoding 8 KHz to 32 KHz Sampling Rate Coder Configurations Using 1.544 MHz Clock
Figure 10

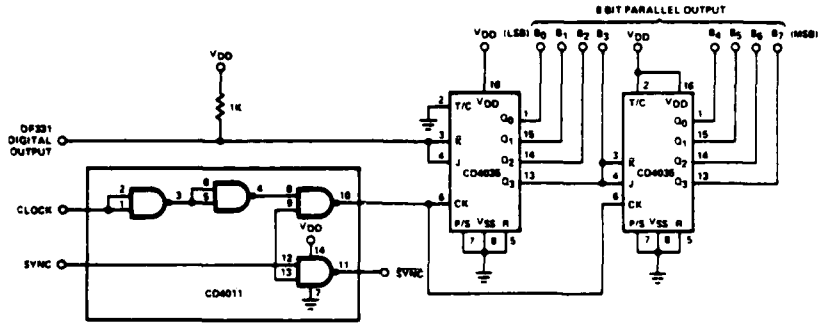


Block Diagram of a 24 Channel Decoder for D3 Channel Banks
Figure 11

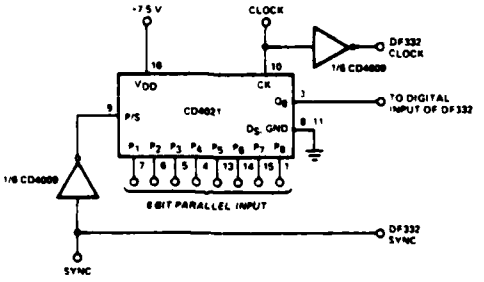
Serial to Parallel and Parallel to Serial Data Conversion

Often when interfacing external logic to the DF331/332, it may be advantageous to convert to a parallel data format after coding and to a serial format again when injecting data into the decoder. Figure 12 shows a simple 8 bit serial to parallel converter allowing easy interfacing asynchronously to systems requiring the 8 bit parallel format. During sync, data is being updated, therefore the sync output can be used as a data ready output. A single IC plus a couple of extra inverters is all that is needed to convert from parallel back to the serial format as shown in Figure 13.

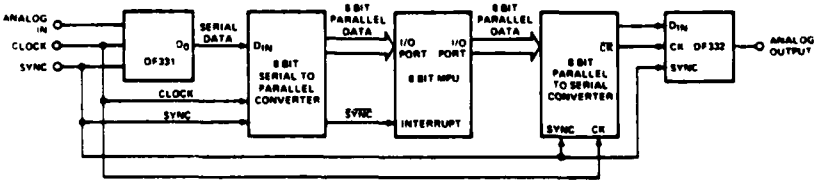
Interfacing to an 8 bit microprocessor is accomplished neatly using the previously described circuits as shown in Figure 14.



8 Bit Serial to Parallel Converter
Figure 12



8 Bit Parallel to Serial Converter
Figure 13



Typical MPU Parallel Data Interface to the DF331/332
Figure 14

Analog Demultiplexing of the Decoder

Some applications may require the use of a single decoder to decode more than one channel of information. If this is so, it is necessary to insert a dummy sync pulse between the two channel syncs to reduce crosstalk. At the time of dummy pulse the digital data should remain at all "1"s condition. Figure 15 shows the basics of such a circuit along with required waveforms.

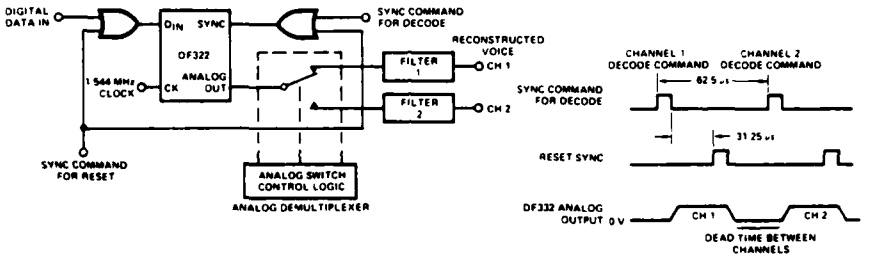
Servo Control Systems

Servo control loops offer an interesting application area in which the DF331/332 can prove useful. Since digital information is nearly immune to environmental noise, it is advantageous to convert to digital before transmitting data from a remote location to a control center. Figure 16 shows a microprocessor based servo loop and locations of the DF331/332 ICs within the loop. In this case the summer, to determine an error voltage, and the DF331 form the A to D section of the remote station. The DF332 plus integrator form the D to A conversion upon receiving data from the central control station.

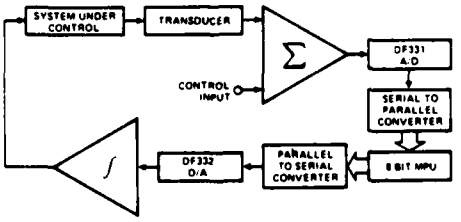
Advantages realized in a servo control loop employing the use of the DF331/332 include:

1. Digital data transmission from and to remote sites.
2. 12 bit resolution with 8 bits of data when resolving error voltages.
3. Wide dynamic range of coder and decoder allow wider breadth of feedback voltages and integrator input voltages.
4. Use of the MPU to change response characteristics of the loop based on inputs from feedback as well as external sources.

This basic configuration could prove useful in many applications where varying loop response characteristics is desirable to accommodate varying situations.



Analog Demultiplexing of the Decoder
Figure 15

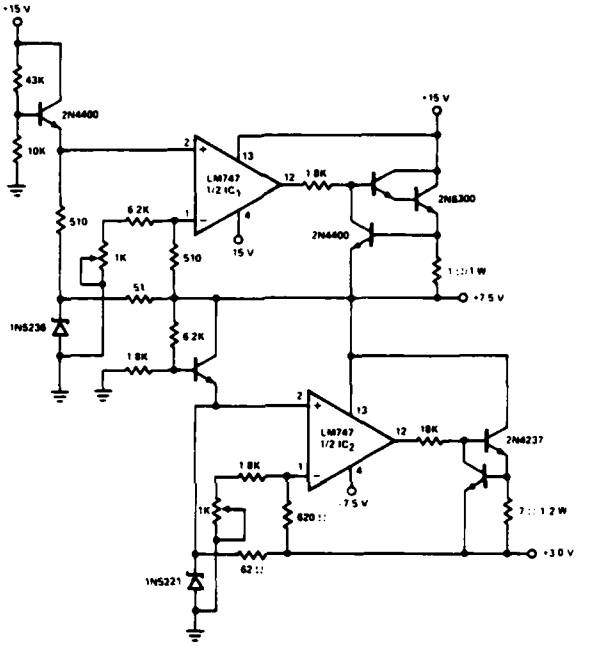


Block Diagram of a Servo Control System
Figure 16

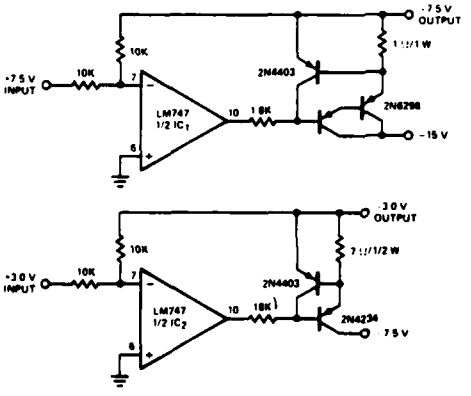
Peripheral Circuits

Circuits which may prove useful when evaluating the CODEC set are the ±7.5 V and ±3.0 V regulator circuits shown in Figures 17A and 17B. In general, the ±7.5 V supplies should be of a 10% tolerance nature. Reference supplies should be matched to one another to within 1%. Absolute value of the references and changes of the absolute values will be reflected by a gain change. The regulator shown in usable for powering 24 CODEC channels simultaneously. In most applications outside of telecommunications where signal to distortion ratio requirements are less stringent, simple three terminal regulators may be used in developing supply voltages.

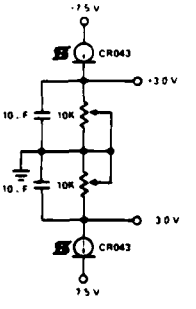
References may be supplied by using the resistor – constant current diode configuration shown in Figure 18.



Positive Supply and Reference Regulators
Figure 17A



Negative Supply and Reference Circuits
Figure 17B



±3.0 V Reference Generator
Figure 18

Sync generation can be accomplished by using the circuit in Figure 19. This is basically a divide by 24 of the clock input. The R/S flip-flop comprised of IC_2 synchronizes the sync edges to the rising edge of $\overline{CK}$. The D flip-flop following the R/S flip-flop delays the sync to the DF331 by a half clock. Thus, the proper sync/clock phase relationships are established for both coder and decoder. It is also possible to create additional sync pulses by shifting the previously generated syncs through a shift register being clocked by the system clock and $\overline{clock}$.

Offset Voltage Adjustment

Some applications may require zero input offset to be present at the coder. While the input offset of the coder is small (< 5 mV), the remaining offset can be zeroed out using the circuit of Figure 20. It is possible to inject small voltages between the analog ground and the digital ground. AC coupling the analog ground to the digital ground allows biasing of the analog ground by the 10K pot. This approach maintains analog input impedance and adds no degrading effects to the signal to be processed or the coder itself.

CONCLUSIONS

It's quite apparent that the information presented herein is generally an overview of the DF331/332. Applications not covered include audio delay lines, audio reverberation circuits, remote data acquisition and transmission and many others. The DF331/332 offers advantages over other CODEC circuits being presently manufactured by allowing system designers a new breadth in designs which reduce component count, cost and general system complexity while improving important system parameters.

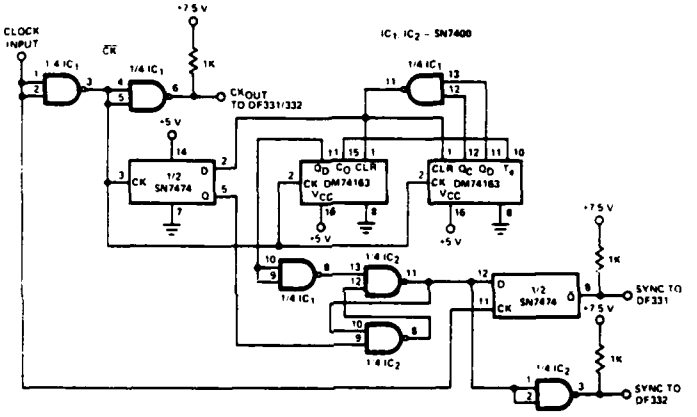
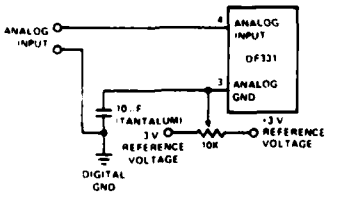


Figure 19



Analog Input Offset Adjust
Figure 20

Siliconix

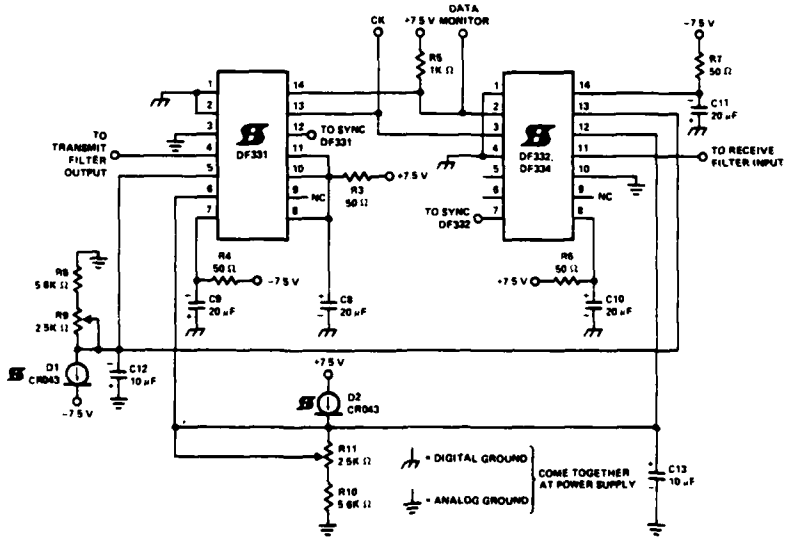
Design Aid to Build a CODEC Evaluation Demonstrator with the DF331/DF332/DF334

INTRODUCTION

The Siliconix CODEC (DF331/332) requires few external components to achieve per channel digital encoding of telephone voice signals. This design aid details the design and evaluation of a lab demonstrator for the CODEC set. Included in the demonstrator are the voltage references and the synchronization circuitry which is necessary to encode and decode a single voice channel. The encoded output of the DF331 encoder is simply applied to the digital input of the decoder. This allows an easy functional test as well as characterization of a CODEC pair.

Figure 1 shows the schematic details of the encoder and decoder with the voltage references and supply bypass elements. The ±3.0 volt voltage references are achieved by running a 430 μA current from a constant current diode (CR043) through a resistor with a trim pot for fine adjustment of the reference voltage. The references are bypassed with a 10 μF tantalum capacitor to supply the peak current (up to 2.0 mA) required by the CODEC during sampling. The digital output of the encoder (DF331), being an N-channel open drain output, requires a 1K Ω pull-up resistor.

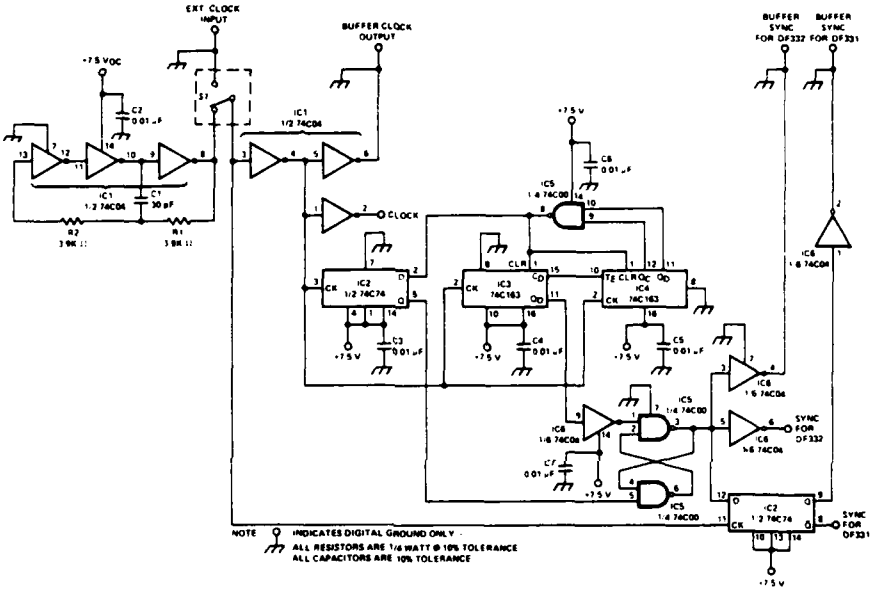
The analog and digital grounds are pinned-out separately on the CODEC, and should be tied together at the power supply ground.



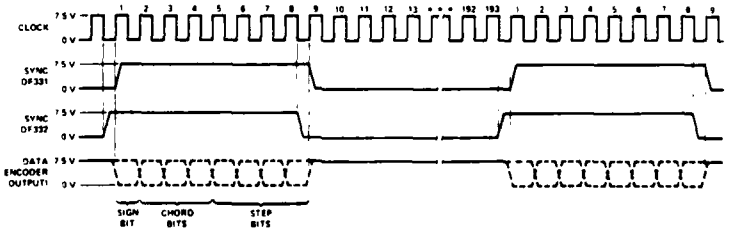
CODEC and References
Figure 1

Figure 2 shows the clock and sync generation circuitry which provides timing for the CODEC. The clock is a basic 3-gate CMOS clock with RC values set to achieve an approximately 1.5 MHz clock rate. The sync generator essentially divides the clock by 193 to provide a sync pulse which is eight clock periods wide and is applied at an 8 kHz rate. (Note that 1.544 MHz divided by 193 equals 8 kHz.) Figure 3 shows the relationship between the various waveforms generated by the sync circuitry, as well as the relationship between the sync, clock and digital data output of the encoder.

The sync waveform to the decoder (DF332 or DF334) is advanced by one-half of a clock period to allow for propagation delays which occur in the CMOS sync generator. Without advancing the DF332 sync, it is possible to lose the most significant bit in each data word, which results in a loss of the sign bit in transmission.



Clock and Sync Generator
Figure 2



Sync Generator Waveforms
Figure 3

Evaluation

This demonstrator allows simple evaluation of the CODEC set. A ±7.5 V (±10%) lab supply is applied to the CODEC and sync circuitry. Analog and digital grounds should be kept separate until meeting at the power supply ground to avoid ground loops in the analog portions of the board. Voltage references should be adjusted to ±3.0 volts. Mismatched voltage references will cause asymmetric waveforms, giving rise to harmonic distortion. References should match to within 0.1 volts.

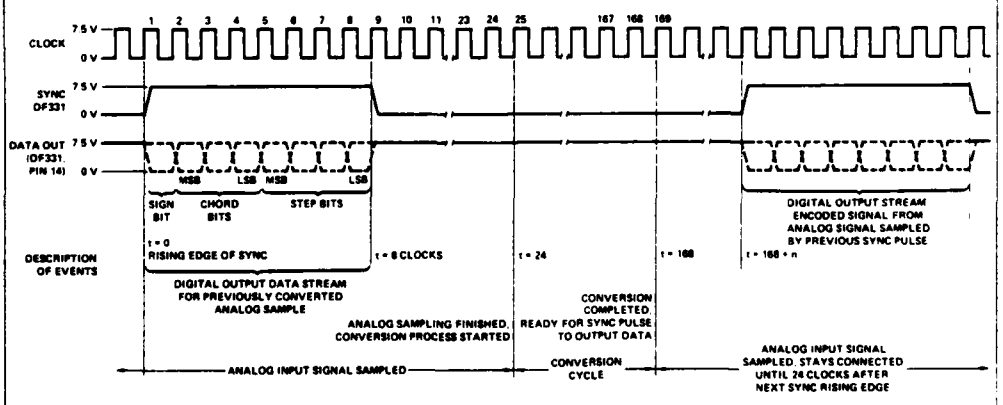
To look at the digital bit stream, the oscilloscope should be synchronized to the sync pulse of the DF331. The encoder output is seen at pin 14 of the DF331. Applying a slowly varying DC level to the analog input of the encoder allows observation of the changing data stream. The corresponding analog voltage levels should appear at the decoder (DF332) output.

For evaluation of voice or music signals, an anti-aliasing filter must precede the analog input and a filter which compensates for the sampling frequency characteristics must follow the decoder output. These filters should cut off before 4 kHz, which is one half of the sampling frequency. They are typically 5th order elliptic low pass filters.

The maximum peak signal swing through the CODEC is equal to the value of the voltage references. The CODEC will function with references as low as ±2.0 volts and as high as ±4.0 volts. Lowering the absolute value of the references compromises system dynamic range while raising the absolute value of the references increases the harmonic distortion of the system.

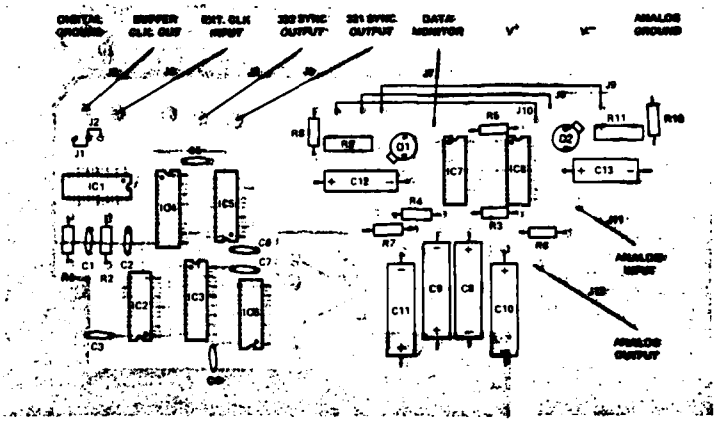
Timing of the CODEC System

The CODEC system timing is controlled by the sync pulse Figure 4 shows the encoder (DF331) timing relationship between the sync pulse, the analog sampling time, conversion time and encoded serial digital output. As shown, the rising edge of the sync pulse starts the serial output of data, starting with the MSB of the 8 bit code (the sign bit). This rising edge of the sync pulse also starts a 24 clock countdown for sampling of the analog signal input (the sampling starts immediately after the previous conversion is completed). At the end of these 24 clocks, the analog sampling is completed and the conversion cycle begins. 168 clock pulses after the sync rising edge, the conversion will be completed and the internal registers will have the encoded data ready for output. The Encoder (DF331) will now go to the analog input sampling state until the next sync pulse. At the rising edge of the next sync pulse, the digital encoded data will be serially shifted out on the output pin. The sampling conversion process for the next analog input starts again.



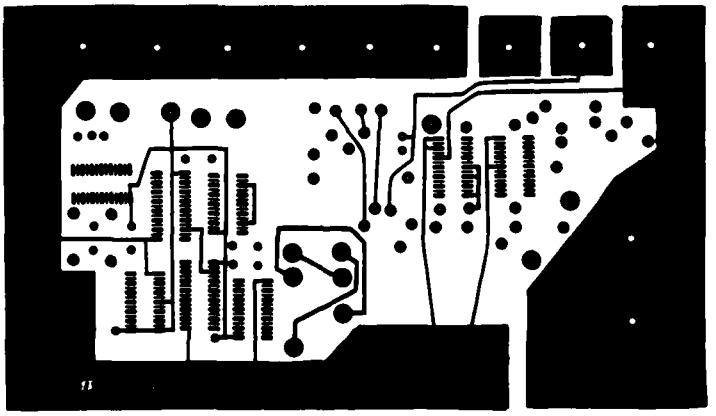
CODEC Timing Relationships
Figure 4

COMPONENT LAYOUT



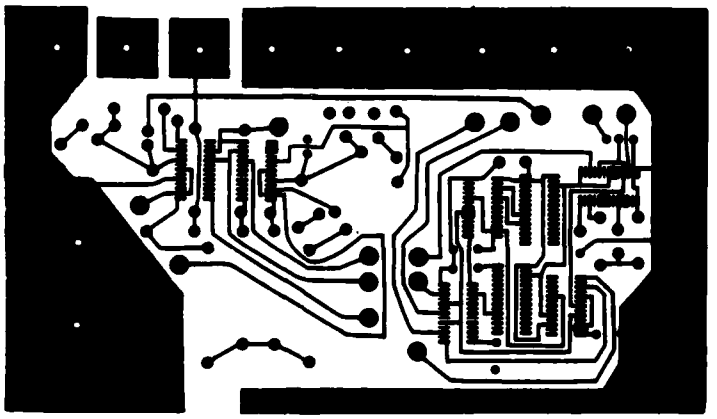
J1 CONNECTS THE INTERNAL CLOCK TO CIRCUIT
J2 CONNECTS THE EXTERNAL CLOCK TO CIRCUIT
J3 CONNECTS THE BUFFER CLOCK OUTPUT (1–6) TO BNC
J4 CONNECTS THE EXT CLK INPUT TO BNC
J5 CONNECTS THE 332 SYNC OUTPUT TO BNC
J6 CONNECTS THE 331 SYNC OUTPUT TO BNC
J7 CONNECTS THE DIGITAL MONITOR OUTPUT TO BNC
J8 CONNECTS R7 TO IC(8) PIN (14)
J9 CONNECTS R11 TO IC(7) PIN (6)
J10 CONNECTS R9 TO IC(8) PIN (13)
J11 CONNECTS ANALOG INPUT TO BNC
J12 CONNECTS ANALOG OUTPUT TO BNC

PC BOARD FOIL PATTERN



DF331, DF332, DF334 CODEC Demonstrator
Foil Pattern, Component Side of Board

PC BOARD FOIL PATTERN (Cont'd)



Foil Pattern, Bottom Side of Board

PARTS LIST

DEVICE	VALUE	SUGGESTED MANUFACTURER
R1, R2	3.9K Ω 1/4 Watt 5% Tolerance	Allen-Bradley
R3, R4, R6, R7	50 Ω 1/4 Watt 5% Tolerance	Allen-Bradley
R5	1K Ω 1/4 Watt 5% Tolerance	Allen-Bradley
R8, R10	5.6K Ω 1/4 Watt 5% Tolerance	Allen-Bradley
R9, R11	2.5K Ω Pot	CTS (X201 Series)
C1	30 pF Disc Mylar Capacitor	Sprague
C2–C7	0.01 μF Disc Ceramic Capacitors	Sprague
C8–C11	20 μF @ 25 WV Electrolytic Capacitor	Sprague
C12, C13	10 μF @ 25 WV Electrolytic Capacitor	Sprague
D1, D2	CR043 (Current Regulator Diode)	Siliconix
IC1, IC6	74C04 (Hex Inverter)	National
IC2	74C74 (Dual D Flip/Flop)	National
IC3, IC4	74C163 (Binary Counter)	National
IC5	74C00 (Quad NAND Gate)	National
IC7	DF331 (CODEC Encoder)	Siliconix
IC8	DF332 or DF334 (CODEC Decoder)	Siliconix
Misc	26 Gauge Wire, BNC Connectors, IC Sockets, Non-Insulated Banana Jacks, Stand Offs, PC Board	

CONSTRUCTION HINTS

The printed circuit layout included is for a double sided board. Foil patterns are shown with the foil side facing the reader. The stuffing diagram is viewed from the component side.

OPERATION

The potentiometer R9 adjusts the negative reference voltage and R11 adjusts the positive reference voltage. Use a DVM to adjust the references to ±3.0 volts. The digital bit stream may be viewed by triggering an oscilloscope on the DF331 sync pulse and connecting the data monitor output to the scope input. The demonstrator may be clocked by an externally generated clock if desired. Connect jumper J2 (only) for external clocking; connect J1 (only) to use the internal clock.

DA78-2 (DF331/DF332/DF334)

Siliconix

Considerations for the Proper Filtering of Analog Signals in DF331/DF332/DF334 CODEC Converter Applications

Walt Heinzer

INTRODUCTION

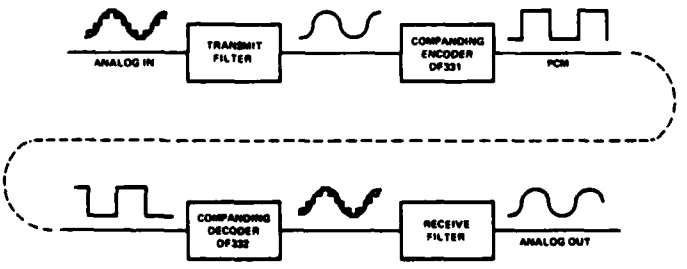
The practical use of CODEC's in telecommunications and audio systems requires two low pass filters, the transmit and receive (Figure 1). The transmit filter in telecommunications nomenclature performs the anti-aliasing (frequency folding) function. The receive* filter smooths the discrete sample voltages of the regenerated audio (voice) signal.

In order to understand the filtering requirements of the CODEC A/D–D/A system, a statement of the sampling theorem is in order:

"If a signal (voice, audio) that is bandlimited is sampled at regular intervals and at a rate at least twice the highest frequency in the band, then the samples contain all of the information of the original signal".

When the CODEC's (DF331/DF332/DF334) are used in telecommunications systems the sampling frequency (f_S) is set at 8 kHz. This implies that the maximum voice signal is limited to 4 kHz. The transmit filter is necessary to limit the input voice signal. For the 8-bit companding converter

*Sometimes called interpolation filter in telecommunications nomenclature.



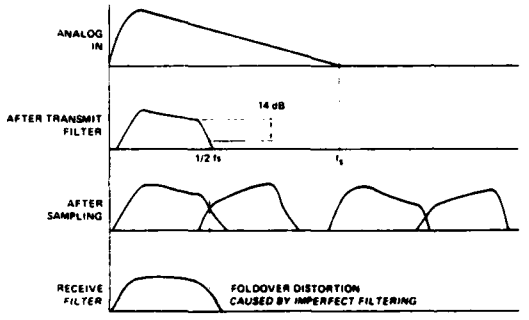
Filters Used in a CODEC System
Figure 1

approach, 14 dB of attenuation at 1/2 the sampling frequency, reduces frequency folding (Figure 2). However, a guardband is introduced on the voice signal typically resulting in a maximum usable frequency of 3.5 kHz. The receive filter smooths the discrete voltage samples of the regenerated signal. At the same time this filter corrects the sin x/x[†] frequency response introduced by the CODEC sampling system back to a flat bandpass by applying an x/sin x transfer characteristic (Figure 3).

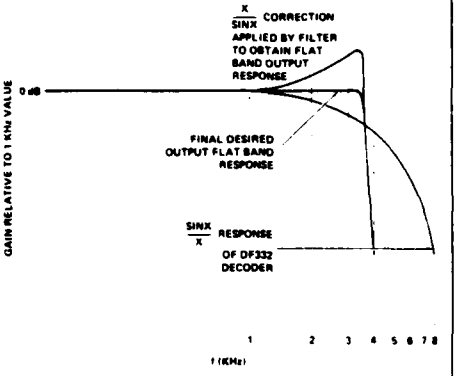
The exact specifications necessary for the transmit and receive filters are determined by the application. For the telecommunication industry the frequency and phase response characteristics are more precisely defined. D3 and D4 channel bank specifications define the overall voice-in, PCM, voice-out frequency and gain response requirements. Some of the more important specs are listed in Table I which is excerpted from "D3 Channel Bank Compatibility Specification–Issue 3" Oct. 1977 [4].

For audio and transducer applications it is important to consider sufficient filtering to avoid frequency folding and gain errors due to the sampling theorem. As a rule of thumb the passband of the transmit filter should attenuate the input signal by at least 14 dB at 1/2 the sampling frequency and by at least 30 dB at the sampling frequency. Remember that the DF331/DF332/DF334 can be operated at clock frequencies up to 3.088 MHz which results in a maximum sampling frequency (f_S) of 16 kHz. This is useful for extended bandwidth applications. The same guidelines of filter attenuation apply at this sampling frequency.

[†] In telecommunications f_S = 8 kHz implies $x = \frac{\pi f}{8\ \text{kHz}}$



Frequency Spectrum In a Sampling System
Figure 2



Effect of Sampling Theorem on Output Gain Versus Frequency
Figure 3

Important Gain vs Frequency Requirements for Telecommunications D3 Channel Bank
Table I

FREQUENCY	TRANSMIT FILTER	RECEIVE FILTER
60 Hz	< −20 dB	N/A
200 Hz	> −3 dB	> −2 dB
300–3 kHz	+0.25 dB, −0.50 dB } Passband Ripple	Same
3.4 kHz	> −1.5 dB < 0 dB	Same
4 kHz	< −14 dB	Same
4.6 kHz	< −32 dB	< −28 dB

It has been shown in AN77-4 that the bandwidth can be increased by using multiple encoders (DF331's) to achieve bandwidths approaching 8 kHz ($f_{s_{eff}}$ = 16 kHz) and 16 kHz ($f_{s_{eff}}$ = 32 kHz). The filtering requirements (Figure 4) necessary to prevent fold-over are the same as the single encoder case when the new effective sampling frequency ($f_{s_{eff}}$) is used.

IMPLEMENTATION

Now that we have examined actual filter requirements—what is the correct filter implementation? There is no exact answer, however, it is worthwhile to look at a summary of some of the major filter salient features on a comparison basis.

Simple Filters (Single Pole, Double Pole)

These filters are realizable in R and C's with op amps or the traditional approach of L, R, and C's. Inductors are avoided in low frequency applications due to size, cost, and non-linearities. The frequency characteristics and example implementations are shown in Figure 5. Note that each pole contributes −20 dB/decade in roll-off between the passband and stopband. When these filters are used with the CODEC's they severely limit the usable flatband bandwidth.

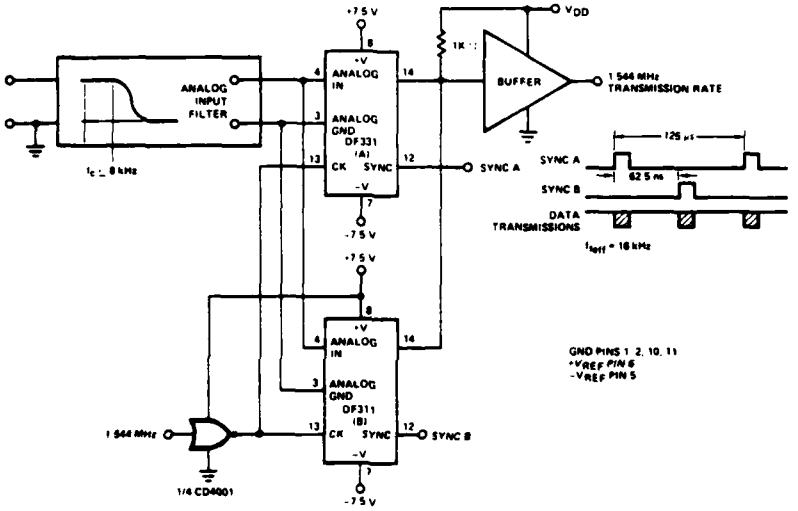
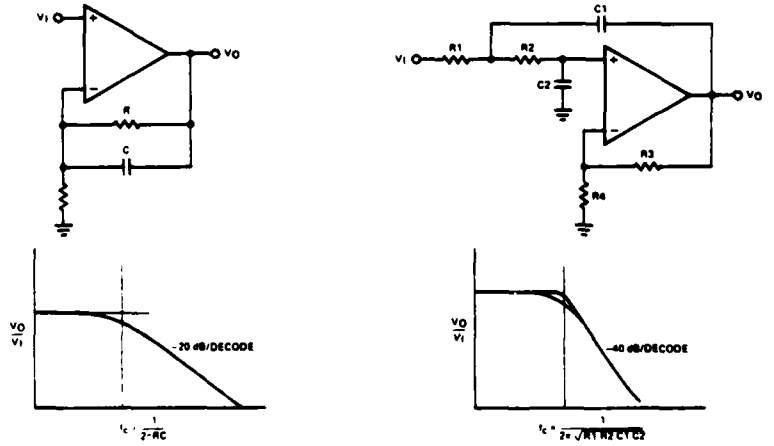


Figure 4



Single Pole Filter

Double Pole Filter

Simple Filter Implementations

Figure 5

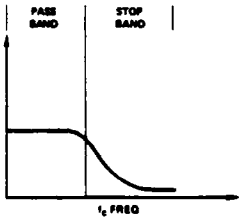
Higher Order Filters (3rd Order and Higher)

Butterworth filter is considered the maximally flat filter in the pass and stopband as shown in Figure 6. You are giving up sharp cutoff frequency when using this implementation compared to the next two approaches. This filter has all zero's at infinity.

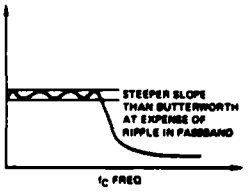
Chebychev filter trades flatness in the passband for sharp cutoff at f_c. It can be shown that the Chebychev has the steepest descent into the stopband of filters constructed with all zero's located at infinity. This filter approach is used in the evaluation filter that follows.

Elliptic filters obtain the steepest slopes into the stopband by positioning their response zeros near the passband. The zeros cause the lobes in the stopband (Figure 6). This approach does meet the stringent requirements of a D3 channel bank in the telecommunications industry. Element value tolerances are the most critical in elliptic filters. As a general rule, the more complex the filter calculations become, the tighter the required component tolerance.

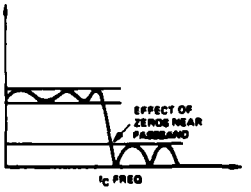
The filter approaches listed are traditional approaches that, at best, must be constructed as hybrid circuits with precise laser trimmed resistors. A monolithic integrated circuit is out of the question as a manufacturable approach using traditional resistors, capacitors and inductors due to the precision requirements and large component values.



Butterworth Maximally Flat Response



Chebychev Filter



Elliptic Filter

Comparing Butterworth, Chebychev & Elliptic Filter Responses
Figure 6

EVALUATION FILTER

In most applications outside of telecommunications the filter shown in Figure 7 will provide good performance in interfacing the CODEC to different transducers (e.g. strain gauges, audio pickups, accelerometers, etc.). The filter is a 6th order multiple feedback filter whose design is outlined in reference [1]. It is an all-pole filter (zeros all at ∞) which results in no lobes in the stopband.

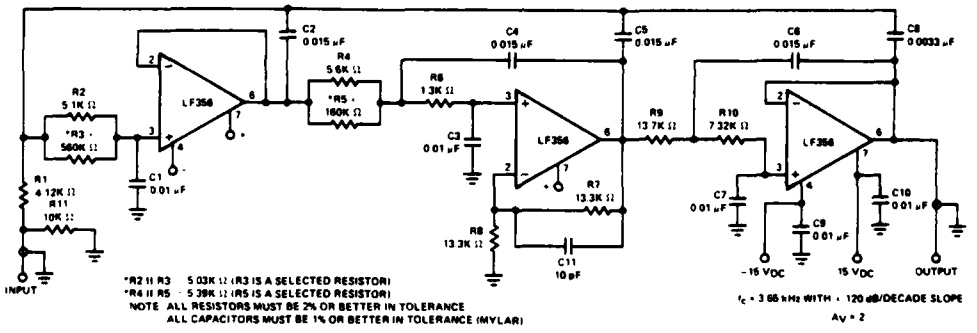
The choice of this filter and components was made on the following criteria.

1. The overall feedback from all three stages reduces the sensitivity to component tolerance compared to the 2-pole per stage cascaded approach.
2. The 6th order response results in −9 dB attenuation at one-half f_S and −45 dB attenuation at f_S adequate for both the transmit and receive filter locations.
3. When this filter is used in the receive position (output of DF332) it does not compensate for the cutoff frequency attenuation introduced by sampling (sin x/x effect).
4. The choice of LF356 op amps was made for their high input impedance (minimum circuit loading), low output impedance (ability to drive capacitive loads) and wide bandwidth.
5. The effective output impedance of this filter adequately drives the input sampling current requirements of the DF331 encoder.

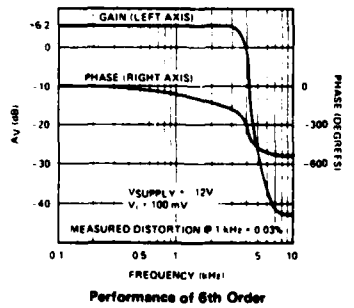
The gain and phase versus frequency response of the filter is shown in Figure 8. An HP3575A gain-phase meter was used for this measurement.

REFERENCES

1. D. Johnson, *Rapid Practical Designs of Active Filters*, Wiley 1975.
2. Technical Staff Bell Telephone Laboratories, *Transmission Systems for Communications*, fourth edition, 1971.
3. P. Geffe, *Simplified Modern Filter Design*, Hayden, New York, 1964.
4. The D3 Channel Bank Compatibility Specification–Issue 3, Oct. 1977. Technical Advisory No. 32 (This information is assembled by AT&T for distribution to non-Bell companies. It represents current plans and is subject to subsequent change.)



Multiple Feedback Low Pass Filter of the 6th Order
Figure 7



Performance of 6th Order
Multiple Feedback Low Pass Filter
Figure 8

Siliconix

Designing with codecs: know your A's and μ's

Nonlinear coders/decoders, or codecs, require your familiarity with framing, synchronization and signaling. Here's a brief intro.

Thomas J Mroz, Siliconix Inc

When designing telecommunications circuits using nonlinear A/D/A conversion, you'll choose from parts that conform to either the Bell Telephone-specified μ-255 Law or the CCITT (International Telegraph and Telephone Consultative Committee)-specified A Law, if you want to guarantee compatibility with other systems. While the first sees wide usage in North America, most of the world uses the second. These conventions govern the same basic operation—analog signal expansion and compression—but differ in their data formats. The differences become apparent upon examination of channel-bank concepts.

Channel banks translate voices into bits

Today's phone systems employ mazes of switches and filters for both analog and digital signals. One small part of these complex networks, the channel bank, transforms analog voice signals at a local exchange into easily transmitted digital signals. It's then easy to compress, transmit and repeat these digital signals in cable and microwave transmissions.

Circuits termed coders sample the analog voice signals generated by user phones, convert them to digital bytes and shift them serially out of the channel bank. On the receiving end, decoders accept these bytes and recreate the analog voice signals initially generated by the phone user. The term *codec* applies to a complete coder/decoder (A/D/A) set.

Channel banks, located in telephone-company central offices, use codecs to handle many phones, encoding analog voice signals into serial data streams for transmission to various receiving banks. One bank can also decode incoming calls and redistribute analog voice signals to user phones (**Fig 1**). Both codecs and channel banks follow specifications in the μ-255 Law or the A Law that not only govern transfer characteristics, but also define formats for framing, synchronization and signaling.

Pulse-code modulation (PCM), the technique channel banks employ to transmit and receive information, allows them to sample analog inputs

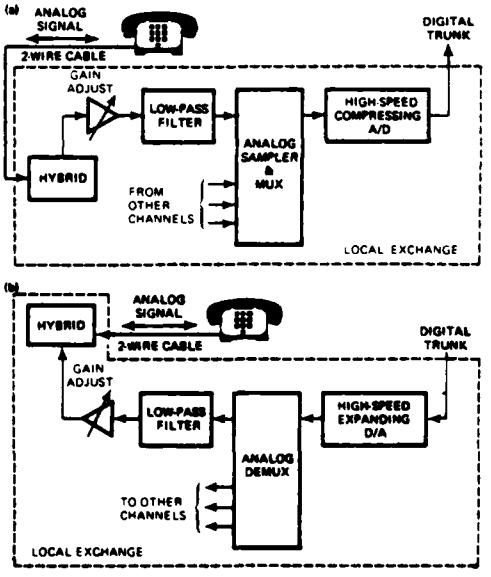
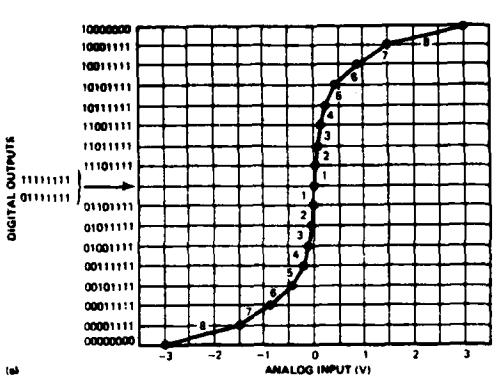


Fig 1—Most existing phone systems employing pulse-code modulation (PCM) use just one high-performance data converter in the transmitter (a) or receiver (b). Multiplexers make these converters available to all the channels the exchange handles. In these diagrams, a hybrid is a device that converts 2-wire phone signals to 4-wire signals, thus eliminating crosstalk between incoming and outgoing data.



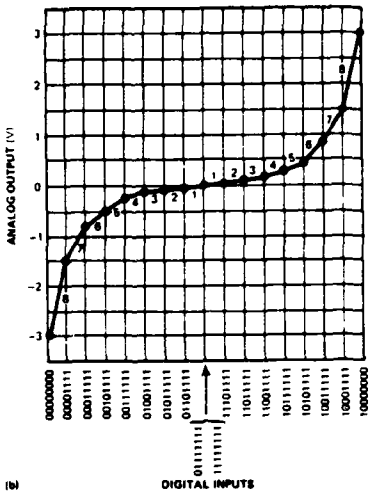


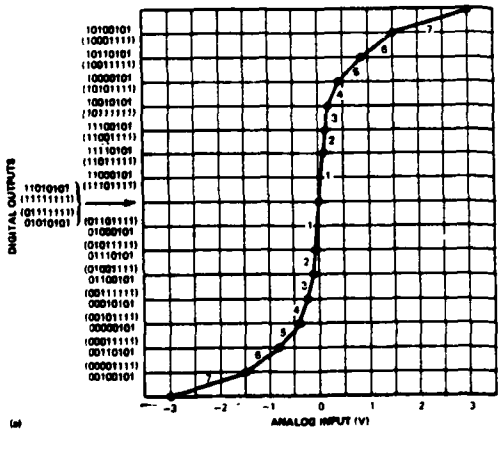
Fig 2—The μ-255 Law transfer characteristics for coders (a) and decoders (b) consist of piecewise linear approximations of the desired curve. Note that two digital values correspond to the origin because the sign bit can have either value at zero.

at a fixed rate and then perform an A/D conversion that quantizes the sample into an 8-bit sign-plus-magnitude word.

Coder and decoder nonlinear transfer characteristics (**Figs 2, 3**) maintain relatively constant signal-to-distortion (S/D) levels over a wide range of analog input levels. Because the channel bank compresses high input levels and expands low levels, a person speaking softly into a phone is nearly as intelligible as someone speaking loudly. Thus codecs are termed companding A/D/A converter sets.

How do the μ Law and A Law differ?

The μ-255 Law and A Law differ fundamentally in the transfer characteristics associated with their



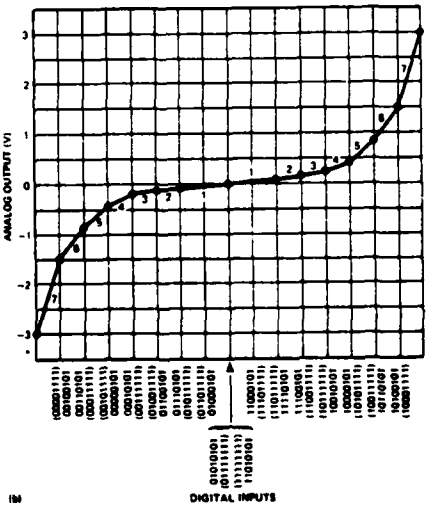


Fig 3—The A Law transfer characteristics for coders (a) and decoders (b) reduce the number of chords required in μ-255 Law curves by making chords near the origin colinear. Note that values listed in parentheses are the corresponding μ-255 Law values.

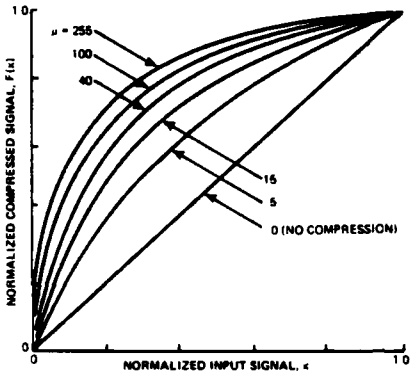


Fig 4—Logarithmic compression characteristics for the μ-255 Law equation show that μ = 0 corresponds to linear operation; large μ values provide increased compression.

A/D and D/A conversions. The equation

$$F(x) = \text{Sgn}(x)\,\frac{\ln(1+\mu|x|)}{\ln(1+\mu)}$$

defines the μ-255 Law (where μ = 255). A coder's A/D converter approximates this equation, while a decoder approximates the equation's inverse.

Two important equations apply to the A Law:

$$F(x) = \text{Sgn}(x)\,\frac{1+\log_{10} A|x|}{1+\log_{10} A} \text{ for } \frac{1}{A} \le |x| \le 1$$

$$F(x) = \text{Sgn}(x)\,\frac{A|x|}{1+\log_{10} A} \text{ for } 0 \le |x| \le \frac{1}{A}$$

where A = 87.6.

Examining the μ-255 Law equation, you can see that μ = 0 represents a linear conversion; increasing μ increases the converter's nonlinearity or compressing characteristics **(Fig 4)**. **Fig 5** illustrates the ability of nonlinear converters to maintain fixed S/D ratios over wide dynamic ranges.

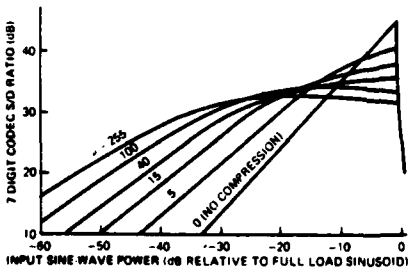


Fig 5—Signal-to-distortion performance of logarithmic companders remains fairly linear for low-power signals independent of the value of μ.

Actual devices such as codecs approximate these equations in piecewise linear fashion. The 8-bit digital code has a sign bit, three bits for chord selection and four bits for step selection within the chord. Thus the μ-255 Law uses a 15-segment approximation (16 segments if you break the line through the origin in half). The A Law, on the other hand, combines the two μ-255 Law chords centered about the origin; making them colinear reduces the number of chords needed. Thus the A Law employs a 13-segment curve.

These differences in chord count reflect conversion conventions in the first step about the origin. **(Fig 6)**. The μ-255 Law indicates that an analog input voltage relating to a digital output of zero should be half as large as the analog input span related to the next digital step—called a midstep condition with a silent interval. The A Law requires no silent interval and employs a mid-riser condition where the origin represents an indeterminate (bistate) digital output. But once past these first several chord segments, the two laws are identical.

Channel banks can use different circuit configurations to accomplish the same task. In the past, one A/D/A set encoded many voice channels, requiring analog multiplexing of these channels, along with a high-speed codec. Multiplexing after the A/D conversion could greatly reduce channel crosstalk, and per-channel codecs such as the Siliconix DF331/332 make this type of system easy to construct. Although implemented with CMOS, DF331/332's have NMOS open-drain digital outputs. Thus, while the per-channel approach eliminates the need for an analog MUX, open-drain outputs tied together eliminate the need for a digital MUX **(Fig 7)**. These two factors, eliminating crosstalk problems and analog multiplexers, have stimulated much interest in per-channel codecs within the telecommunications industry.

Frame formats structure multiplexed data

Multiplexing many analog voice channels after conversion into one serial data stream requires a method for synchronizing transmitters and receivers, so that channel banks can transmit digital information in a frame format. Under the μ-255 Law, a frame consists of 24 channels or 24 bytes of digital information **(Fig 8a)**, with one data bit dedicated as a framing bit—a definition resulting in a total of 193 bits/frame. The μ-255 Law specifies that these data bits be transmitted at 1.544M bps.

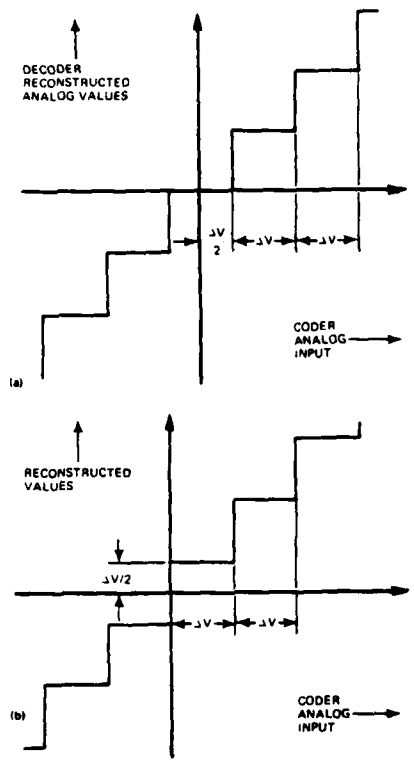


Fig 6—If you examine the first steps of μ-255 Law (a) and A Law (b) coder transfer characteristics you'll see an important difference: the μ-255 Law experiences a midstep condition with a silent interval while the A Law sees a mid-riser condition. Output coding differences reflect this discrepancy.

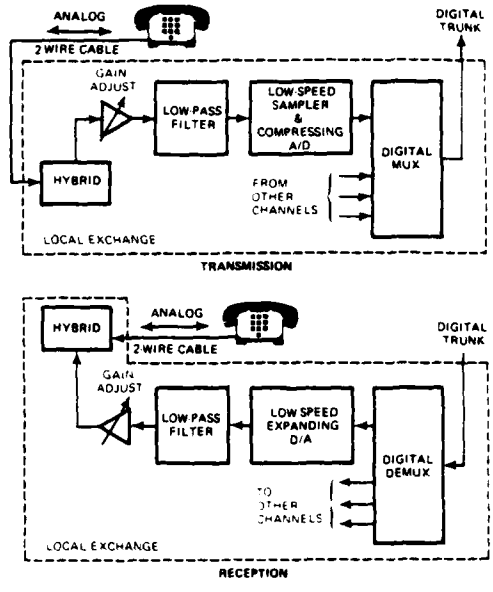


Fig 7—Per-channel coding/decoding of voice signals in new-design channel banks uses inexpensive IC codecs for each channel and multiplexes digital signals for cable transmission. This technique, simpler and cheaper to implement than analog multiplexing, also eliminates analog sampling crosstalk.

The A Law also employs a framing concept, but with a data-transmission rate of 2.048M bps, thus allowing enough time to transmit 32 8-bit words for each frame. Another difference: The A Law doesn't generate a framing bit as in μ-255 Law channel-bank systems; rather, it dedicates a complete channel time slot to framing **(Fig 8b)**.

Although a frame equals the time required to transmit one byte of data for each channel, still needed is a way to identify individual channels in the transmitted data stream. Previous designs synchronized the analog multiplexers in front of the A/D in the transmitter to those on the receiving end. New designs incorporating the DF331/332 codec set in a per-channel configuration use sync pulses. These pulses, ANDed with a clock, dump or load output or input shift registers that reside on the coder and decoder. Because channel-bank transmission-line lengths vary, received data looks asynchronous. Therefore you must derive clock and sync signals for the receiving channel bank from the incoming data.

New μ-255 Law codec designs must also accommodate signaling capability. Signaling information lets the transmitting and receiving banks communicate information such as alarms, off hook and on hook, and it checks to ensure that the banks operate in sync.

Under the μ-255 Law, every sixth frame becomes a signaling frame; thus the eighth bit of every channel carries signaling information presented at that channel. In other words, the bank performs 7-bit A/D/A conversions during a signaling frame, reserving the eighth bit-time slot for the signaling bit. By contrast, the A Law uses reserved-channel signaling, which dedicates to signaling one entire channel out of the total 32 in each frame. Thus, signaling frames don't exist as in the μ-255 Law because signaling occurs in every frame.

When testing and evaluating channel-bank performance, realize that it's only fair to simulate human limitations. You can accomplish this objective by inserting a C-message filter **(Fig 9)** in front of equipment used to test noise and distortion in the complete A/D/A path. Such filters simply simulate the human ear's frequency response to noise; weighting during measurements guarantees that measured distortion levels and noise relate directly to human ability to understand phone conversations.

The three most important codec specs

All new designs aimed at upgrading systems share a common goal: to meet or exceed existing specifications. Codecs face pressure on three important specifications: S/D ratio, idle channel noise and gain tracking. These specs will make or break new codec designs.

Because of codec nonlinear conversion techniques, the specifications generally appear as functions of input power ranges. Signal-to-distortion figures simply give the ratio of the signal power to the distortion power created by quantization errors and internal noise **(Fig 10a)**. Thus, specs for S/D ratio cover the following input power ranges:

P_{in} = 0 to −30 dBm0
= −30 to −40 dBm0
= −40 to −45 dBm0.

As a reference level, 0 dBm represents a 1 mW test tone, and the term dBm0 refers to relative power at the input. As an example, consider a transmission line with 3 dB loss to the end point. You would refer to −50 dBm of noise at the endpoint as −47 dBm0, and the line endpoint would be a −3 dBr point (relative to input).

Idle channel noise measures the noise power seen at the receiving end of the system with 0V on a transmitting channel's input. The last spec of interest, gain tracking **(Fig 10b)**, relates system gain to input power level.

These specifications define a system spec and imply that any new device intended to replace portions of existing systems must exceed these ratings by a suitable margin. For S/D ratio, the suitable term translates into several decibels; idle channel noise should be as low as possible, but certainly at least 5 dB better than system specs.

Codecs see a promising future

With the introduction of new codec IC's, a new world of application possibilities arises. In discrete form, these system components formerly required large areas and substantial investments in design time, making the cost of incorporating them into systems outside of telecommunications

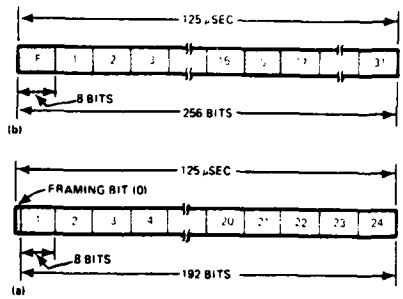


Fig 8—Frame formats place channel data in preassigned time slots. The μ-255 Law uses one framing bit every 24 bytes (a) with each byte corresponding to data from one channel. The A Law format (b) dictates complete channels for framing and signaling data

prohibitive. Now, codecs of the same quality are available at costs comparable to those of other mass-produced integrated A/D converters. Applications such as audio delay lines (digital form), portable communications using PCM, remote data acquisition and talking computers are becoming realizable and less expensive to develop and produce.

Because parts such as the present codec IC's arose primarily to serve the communications industry, their quality and function in other applications are guaranteed; the telecommunications industry sets very high standards of accuracy and reliability. The elimination of adjacent-channel crosstalk through the per-channel codec approach leads to major quality improvements in voice transmission over PCM communication links.

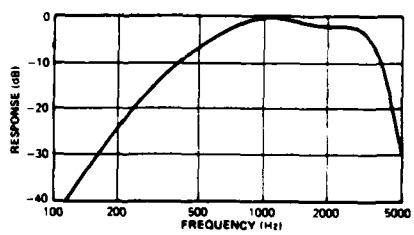


Fig 9—C-message frequency weighting simulates the response of a Model 500 telephone and voice characteristics of average phone subscribers when relating noise and distortion effects to voice-signal intelligibility.

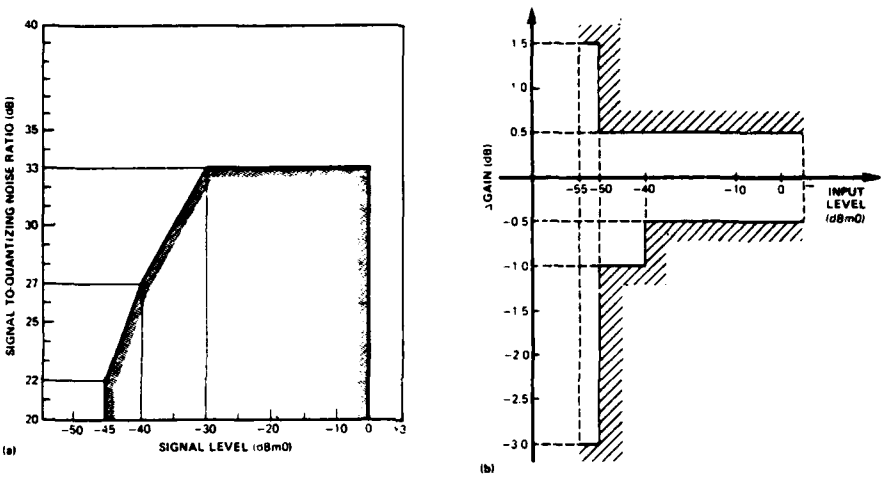


Fig 10—Codec IC's must meet performance standards in several important areas. Minimum specs for S/D ratio (a) and gain tracking (b) apply to both μ-255 Law and A Law systems. Note that ΔG represents system gain measured from the coder's input to the decoder's output and also gives an analog ratio.

Additionally, codec nonlinearity aspects offer some interesting alternatives to linear converters. The 8-bit data format covers a 72 dB dynamic range (equivalent to 12 bits) and lets you easily interface inputs from wide-dynamic-range natural phenomena, such as wind speeds or earthquakes, to popular 8-bit μC's. In voice-synthesis applications, codecs give computers more realistic voices. Additional codec applications will result as design information increases. □

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Author's biography

Tom Mroz develops telecommunications, timing and interface circuits as a design engineer for Siliconix, Santa Clara, CA. After earning his BSEE at Purdue Univ, he worked for Motorola Semiconductor Products Div and then joined Siliconix in March 1976 as an applications engineer. Among his hobbies Tom lists photography, boating, woodworking and listening to classical music.

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CODEC/Filter Level and Noise Measurements

REFERENCE LEVELS

The overload level (full scale) for the CODEC is 3 V peak. All performance measurements are made with respect to this 3 V peak full scale level. For the D_3 channel bank, the 0 dBmO test tone level is 3 dB below the overload level. Since 3 dB below 3 V peak is

3 V (0.707) = 2.12 V peak
or 2.12 (0.707) = 1.5 Vrms,

1.5 Vrms corresponds to 0 dBmO for the CODEC. Most instruments are calibrated in 600 Ω but read voltage. Therefore, a 0 dBm (1 mW) meter reading will be given for an input voltage of

$$E = \sqrt{PR} = \sqrt{10^{-3}\,(0.6)\,10^{3}} = \sqrt{0.6} = 0.775 \text{ Vrms}$$

When reading 1.5 Vrms, the meter will indicate

$$20 \log \frac{1.5}{0.775} = 20 \log (1.935) = 20\,(0.287) = +5.74 \text{ dBm}$$

Therefore, to convert to dBmO, 5.74 dB must be subtracted from the meter reading. Alternately, a 5.74 dB attenuator pad could be inserted in front of the meter to make it read directly in dBmO.

When using a generator with built-in meter which measures its generator output (such as the HP3551A), one cannot insert a pad in front of the meter when it is in the send level measuring mode. To get the correct output level one must either set the indicated generator output level 5.74 dB higher than the desired dBmO level or insert an amplifier which has 5.74 dB voltage gain at the generator output. This will make the meter read directly in dBmO.

Since harmonic distortion, gain tracking and signal to quantizing noise ratio are a function of signal level, it is important that the above correction factors are taken into account when signals are applied and measurements are taken. Also, noise measurements in dBrnc must be converted to dBrncO by subtracting 5.74 dB from the dBrnc reading (unless the pad has been inserted to make the meter read directly in dBrncO). Notice also that if there are any other voltage gains or losses in the signal path, their effect on readings and signal levels into the CODEC must be taken into account.

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