CORRELATION OF FIELD DATA WITH RELIABILITY PREDICTION MODELS

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IITRI/Reliability Analysis Center
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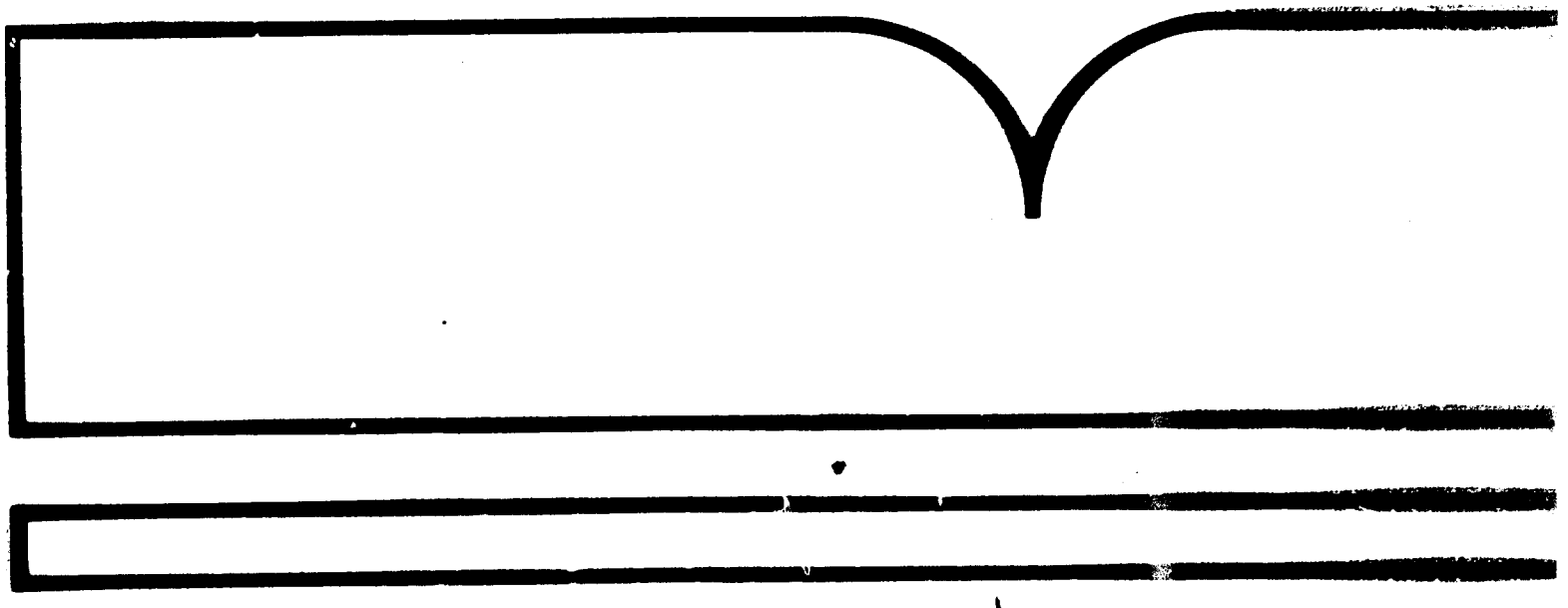
Nov 81



RADC-TR-81-329
Final Technical Report
November 1981

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IIT Research Institute

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Griffiss Air Force Base, New York 13441

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER RADC-TR-81-329	2. GOVT ACCESSION NO. AD/A111258	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) CORRELATION OF FIELD DATA WITH RELIABILITY PREDICTION MODELS		5. TYPE OF REPORT & PERIOD COVERED Final Technical Report Aug 79 - Sep 81
		6. PERFORMING ORG. REPORT NUMBER N/A
7. AUTHOR(s) K. A. Dey		8. CONTRACT OR GRANT NUMBER(s) F30602-78-C-0281
9. PERFORMING ORGANIZATION NAME AND ADDRESS IITRI/Reliability Analysis Center Griffiss AFB NY 13441		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62702F 23380197
11. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (RBRA) Griffiss AFB NY 13441		12. REPORT DATE November 1981 13. NUMBER OF PAGES 160
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Same		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Peter F. Manno (RBRA)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Modeling	Residuals
Reliability	Correlation Matrix
Prediction	
Goodness of Fit Tests	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report considers the factors influencing the goodness of fit of MIL-HDBK-217C prediction models. Although it is not possible to statistically separate casual factors in every case, areas in which the models are deficient are identified and quantified. Possible causes are reviewed and the most likely casual factors identified. Where positive inferences are possible, a range of statistical methods are used to give an unbiased assessment. The underlying distribution of time to failure is investi-

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gated since MIL-HDBK-217C assumes a constant failure rate model. Results suggest that no great error will accrue from such an assumption although strictly it is not always valid.

The statistical methods developed for this study may be used for future model evaluation whenever an unbiased assessment is required. The correlation matrix/ratio plot method may be used iteratively to construct an optimal model but least squares regression analysis is preferred. The ratio plot method allows empirical confidence intervals on predicted failure rates to be readily evaluated.

PREFACE

This report was prepared by IIT Research Institute/Reliability Analysis Center for the Rome Air Development Center, Griffiss AFB, New York, under Mod P00007 to contract F30602-78-C-0281. The RADC technical monitor for this program is Mr. Peter F. Manno (RBRA).

The principal investigators for this project were Mr. K.A. Dey, Mr. S.J. Flint and Mr. H.C. Rickers, with valuable assistance provided by Mr. V. Cavo, Mrs. C.A. Proctor and Mr. B.L. Radigan.

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EVALUATION

The objective of this effort was to provide additional verification of the monolithic microcircuit prediction models contained in MIL-HDBK-217C, Notice 1, "Reliability Prediction of Electronic Equipment", dated May 1980. The study evaluated the accuracy of the models through a comparison of predictions to actual observed device failure rates using data acquired since the completion of the model development program in March 1979. This newly acquired data base encompasses a total of 39.4×10^9 part hours on digital microcircuits including large scale integrated devices (LSI), memories, and linear devices.

Special statistical techniques such as ratio plots were applied to provide an objective and unbiased assessment of the models. These ratio plots for the 5 monolithic models in MIL-HDBK-217C are presented to show how accurately they predict failure rates. The digital models for both monolithic Bipolar and MOS devices shows some dependence on the complexity factor but overall the ratio plot shows that the moving average line passes through the middle of the observed versus predicted points, indicating good correlation. The overall performance of the Monolithic Bipolar and MOS Linear Devices model based on the new data proved satisfactory and showed some complexity factor dependence. Only limited data was available to validate the Monolithic Bipolar and MOS Random Logic LSI and Microprocessor Devices Models, however, but the moving average in the ratio plots showed that the model is predicting failure rates somewhat lower than the actual observed data. The Random Access Memories (RAMs) model again showed strong complexity dependence. The data scatter, particularly for 4K RAMs, results in an average line which differs significantly from the ideal observed to predicted ratio of one. There was

insufficient data to properly evaluate the Read-Only and Programmable Read-Only Memories Model.

Overall, the microcircuit failure rates predicted by the models in the present MIL-HDBK-217C, Notice 1, based on the data collected in this effort were verified to be an effective means for assessing the reliability of microelectronic devices. Future revisions to the failure rate models in MIL-HDBK-217C will consider the data generated in this effort.

Peter F. Manno

PETER F. MANNO
Project Engineer

1. INTRODUCTION

1.1 Objective. The objective of this study is to provide additional verification of the monolithic microcircuit prediction models originally developed in RADC-TR-79-97, "LSI/Microprocessor Reliability Prediction Model Development," dated March 1979 and later incorporated into MIL-HDBK-217C, Notice 1, "Reliability Prediction of Electronic Equipment," dated May 1980. Notice 1 also includes the revised digital SSI/MSI and linear device models. This study is concerned with the evaluation of monolithic reliability prediction model accuracy through a comparison of predictions to actual observed device failure rates. This verification process utilizes field failure rate information not employed in the previous model development programs.

1.2 Background. A means of predicting failure rate is essential in the development and maintenance of electronic equipments. Predictions performed as a part of the design stage provide an objective means of comparing design options. They also yield early estimates of anticipated equipment reliability which are useful in life cycle cost studies and forecasting of spares holding requirements. Previous microcircuit reliability prediction techniques, such as those presented in MIL-HDBK-217B, afforded reasonably accurate predictions for a variety of device technologies over the low and medium complexity range. However, the rapid evolution of microcircuit technologies introduced complex device configurations which were beyond the intended scope of those methods. The extensive use of these complex new technology devices in both military and commercial electronic systems created an urgent need for a relatively simple yet accurate method of predicting their reliability.

Such a method was derived in RADC-TR-79-97 "LSI/Microprocessor Reliability Prediction Model Development," dated March 1979. These models improved prediction accuracy without substantially increasing model

complexity by subdividing each parameter into a set of more detailed parameters. Thus, the reliability sensitive attributes of a device are more adequately represented.

To insure that these models remain accurate and realistically reflect the impact of emerging technologies and fabrication techniques, it is essential to monitor the correlation of reliability predictions (calculated using these models) with observed field failure rates.

This report describes the results of the verification study for MIL-HDBK-217C, Notice 1, Monolithic Microcircuit Reliability Prediction Models.

2. DATA COLLECTION AND DATA ANALYSIS TECHNIQUES

2.1 Data Collection. The development of the monolithic microcircuit models presented in MIL-HDBK-217C, Notice 1 were based on the analysis of over 32 x 10^9 part hours of reliability data including laboratory life testing, reliability demonstration, checkout, burn-in and field experience data. In this model development, the reliability data resources were complemented by a theoretical analysis of pertinent reliability considerations as suggested by the fruits of an extensive literature search. To establish confidence in the model, an additional set of data (not used in deriving the model) was used to compare predicted to observed failure rates.

Since the model was developed, additional reliability data have been collected as part of the IITRI/Reliability Analysis Center (RAC) operation. This latest data encompasses a variety of device types (including some new technology devices) in a number of different package configurations and applications for a total of 39.4 x 10^9 part hours. Thus a total of 71.4 x 10^9 part hours have now been used in deriving and validating the model.

Since the validity of failure rate prediction models can be best assessed through a comparison of predictions and reliability experiences in actual usage conditions, only field reliability data is employed in this validation study. All field data acquired since the completion of the model development program in March 1979 has been utilized and is presented in Appendix A. A summary of the data is given in Table 1.

TABLE 1: SUMMARY OF DATA ENTRIES EMPLOYED IN MODEL EVALUATION

Device Category	Number of Data Points
Digital, SSI/MSI	414
Digital, LSI	35
Memory	97
Linear	127
Total	673

(Note that the number of data entries in Appendix A is less than 673 since some of the data points are for the same device in identical conditions. Such data points are combined into one entry.)

2.2 Data Analysis Techniques. Special statistical techniques have been developed (or adapted from standard methods) to provide an objective and unbiased assessment of the models. The later stages of the study were largely concerned with developing a general procedure applicable to any study of this type. The goal was to provide a procedure which did not oversimplify the underlying statistics but at the same time was understood by the layman. Any presentation format which was based on engineering principles was considered particularly attractive.

The following techniques were used in the study:

(i) Logarithmic Failure Rate Ratio Plot. One way to assess the performance of a model is by residual analysis, i.e., the error remaining after the model has been fitted. We are concerned with relative (or percentage) errors, since a 10% error at a low failure rate is as serious as a 10% error at very high failure rate. Any attempt to consider actual error can be seriously misleading; hence, a type of standard error independent of the magnitude of the failure rate is called for. This is consistent with the concept of a multiplicative model (as employed in MIL-HDBK-217C) rather than the general linear (additive) model.

A further requirement is that the skew in the distribution of errors should be zero so that a predicted failure rate (λ_p) at twice the observed failure rate (λ_o) appears equally but oppositely as serious as a λ_p at half the observed failure rate.

Given these two stipulations the remarkable visuo-spatial analytic abilities of the brain can enhance the study in an unbiased fashion. The keyword here is "enhance," and rigorous statistical tests are also required; these are defined in later sections of this report.

From here on in this report a predicted failure rate will be referred to as "predicted" or as λ_p. The corresponding observed failure rate will be referred to as "observed" or λ_o.

A logarithmic plot of the ratio of observed to predicted (λ_o/λ_p) satisfied both stipulations defined above. An example of some hypothetical data is given in Figure 1 and some real data in Figure 3. Figure 2 gives a comparison of the various graphical methods to show why the logarithmic residual ratio plot was used.

The hypothetical data are for three points, all with $\lambda_o = 10$, but with λ_p respectively at 5, 10, and 20 failures per 10^6 hours.

The real data is a subset of Appendix A.

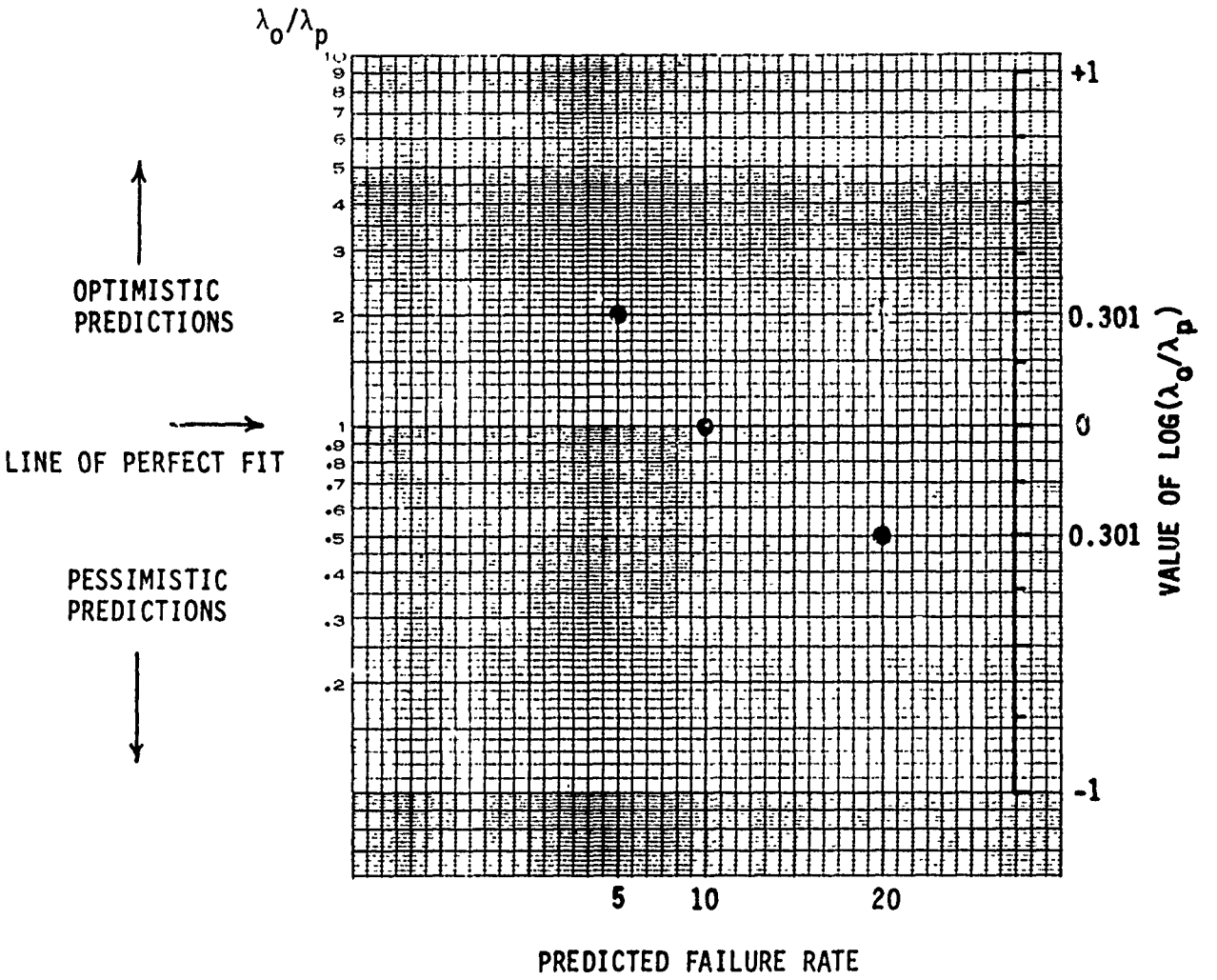
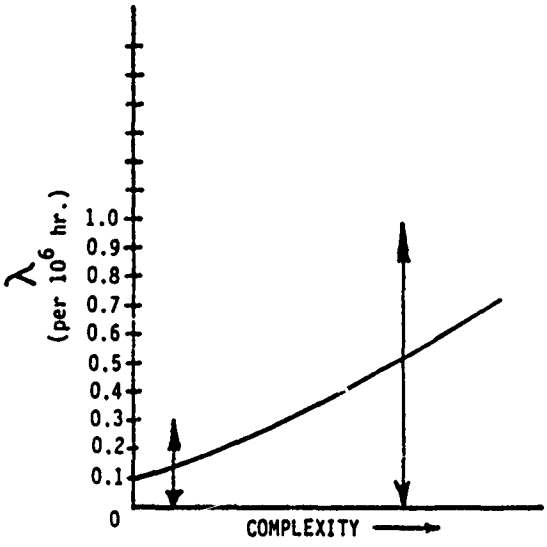
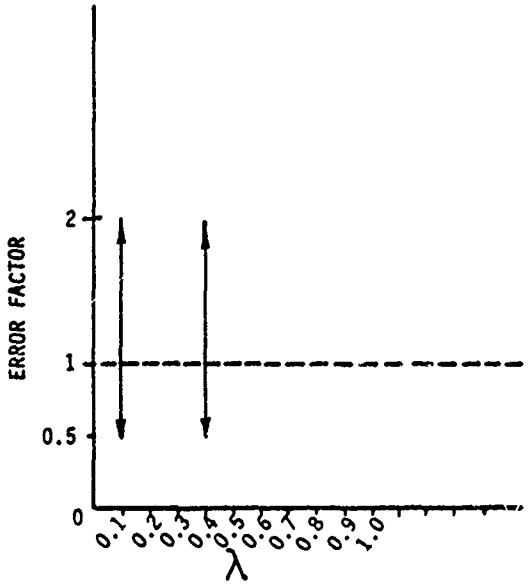


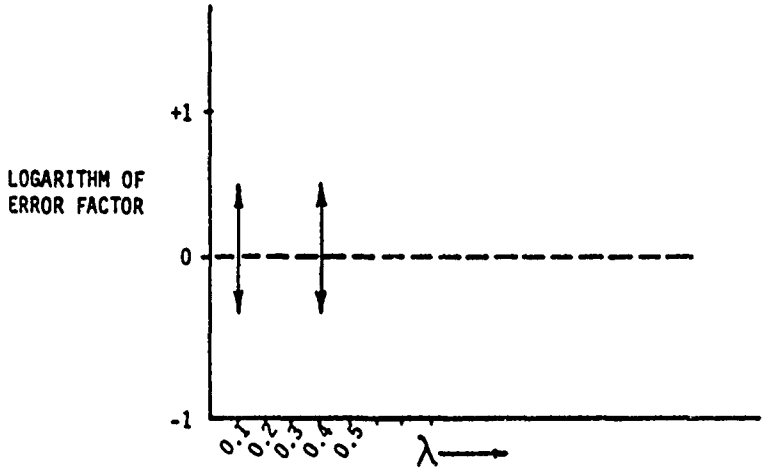
FIGURE 1: RATIO PLOT



(a) LINEAR: ± 100% ERROR APPEARS MORE SERIOUS FOR THE LARGER MAGNITUDE λ



b) LINEAR RESIDUAL RATIO PLOT: ± 100% ERROR MAGNITUDE DEPENDENCE ELIMINATED BUT HIGHLY SKEW.



(c) LOGARITHMIC RESIDUAL RATIO PLOT: ± 100% ERROR SYMMETRICAL, EQUALLY SERIOUS.

FIGURE 2: COMPARISON OF THE DIFFERENT METHODS OF DEPICTING ERROR IN PREDICTED FAILURE RATE (λ)

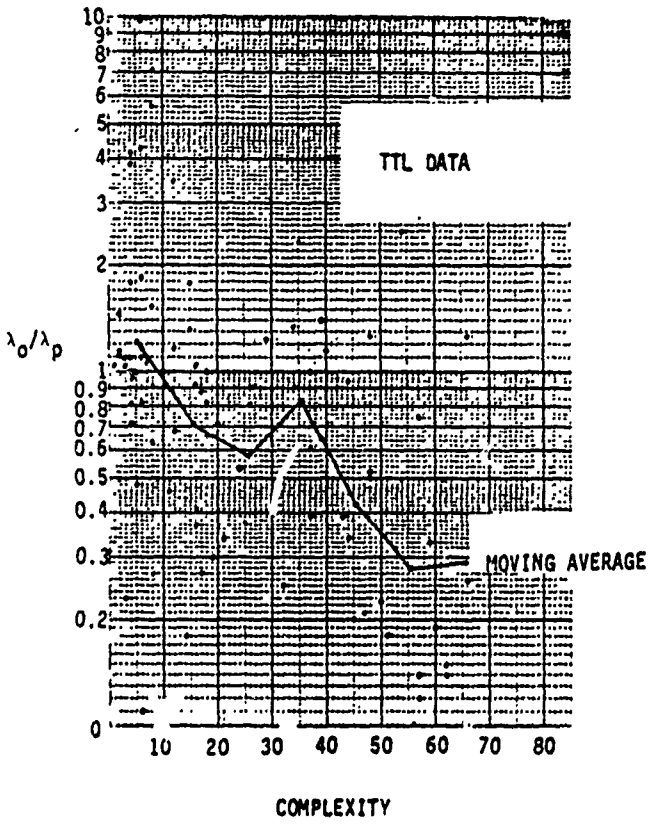


FIGURE 3: RATIO PLOT VS. COMPLEXITY

The moving average is simply a series of arithmetic means over certain ranges of the horizontal axis. In this case, the range is 10 gates on the complexity axis. The resultant series of points are joined for clarity. The moving average highlights and smooths the relation between the two variables, in this case log λ_o/λ_p, and complexity.

Mathematically, the principle of the ratio plot is explained by:

$$(\log 2 - \log 1) = (\log 1 - \log 0.5)$$

and $$\frac{2}{1} = \frac{1}{0.5}$$

so that a constant % error is shown as a constant distance from the line of perfect fit.

A perfect fit is found where $\lambda_o = \lambda_p$ and hence where $\log_{10} (\lambda_o/\lambda_p) = 0$. Therefore, the goodness of fit of the model is evaluated on a symmetrical scale about 0, typically not exceeding ± 1, as shown in Figures 1 and 3. Note that ± 1 represents an order of magnitude in either direction.

This plotting method is used extensively in the analysis. A computer program was written to automatically construct these plots directly from a data file.

(ii) Significance Test for the Sample Mean. For actual field data, the distribution of $\log_{10} (\lambda_o/\lambda_p)$ is found to be close to normality as shown in Figures 4 and 5. Figure 4 is a straightforward histogram for a particular set of data, and Figure 5 shows the same data on normal probability paper. The Kolmogorov-Smirnov statistic (See Section 2.2(v) or Ref. 3) concludes that there is no significant departure from normality.

This normal attribute of the logarithmic ratio plot is exploited in deriving a statistical test to decide whether a particular set of observations is significantly different from their associated predictions. In other words, they could not have arisen by chance at some predetermined level of significance.

If the variance of $\log_{10} (\lambda_o/\lambda_p)$ for a given set of conditions is σ^2 then the variance of the mean of a set of n such points is σ^2/n, where n is the sample size. If σ^2 is estimated from a sample of data, as s^2, then the variance of the sample mean is $\frac{s^2}{n}$. Since the expected value of $\log_{10} (\lambda_o/\lambda_p)$ is 0, and the distribution of $\log_{10} (\lambda_o/\lambda_p)$ is approximately normal then

$$t = \frac{\{\log_{10} (\lambda_o/\lambda_p)\}}{s/\sqrt{n}}$$

is distributed as Student's t distribution with (n-2) degrees of freedom.

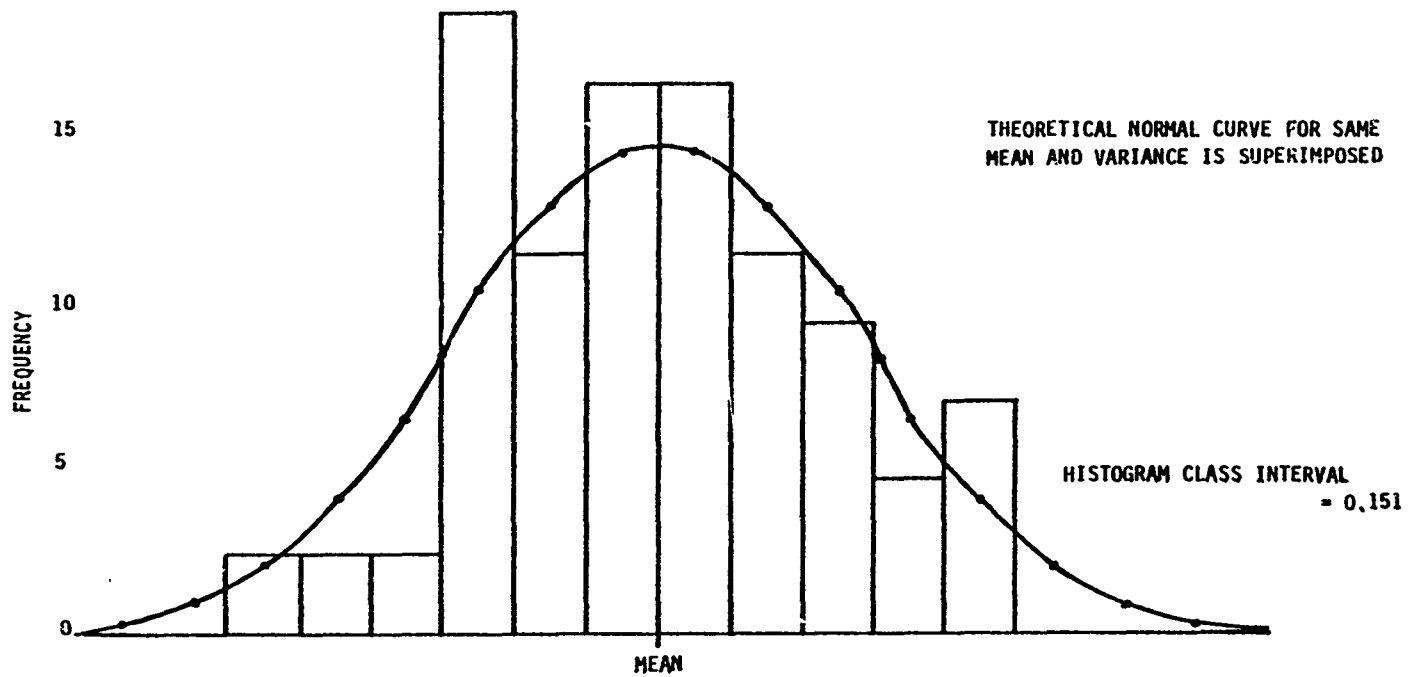


FIGURE 4: HISTOGRAM OF $\log_{10} \lambda_o/\lambda_p$

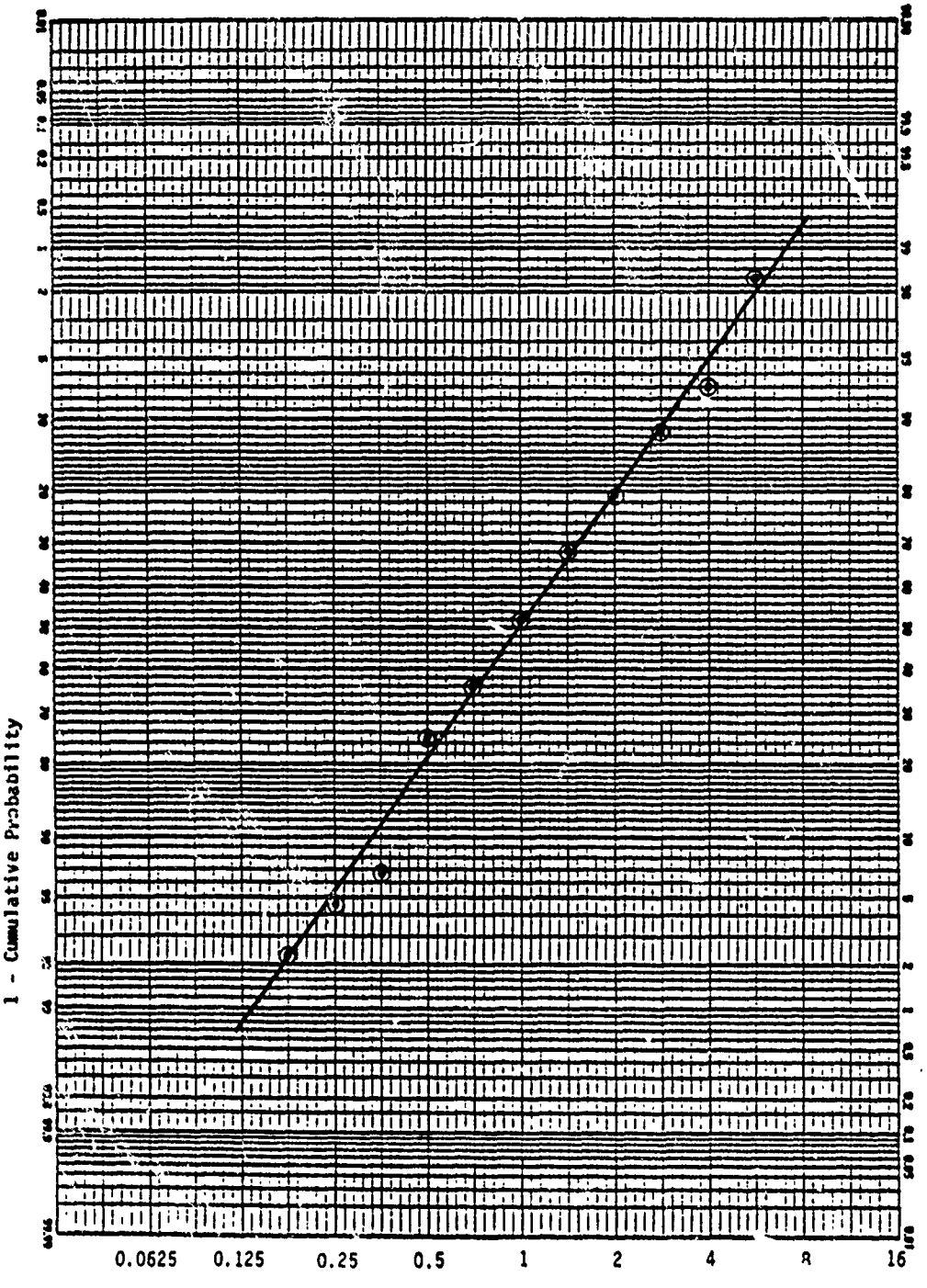


FIGURE 5: PROBABILITY PLOT (NORMAL) FOR DATA USED IN FIGURE 4

If t is found to be less than the critical value (found in tables, Ref. 4) at some significance level α, then the model is performing satisfactorily over the sample space, i.e., for the set of environmental, temperature and device conditions experienced by the data for a given technology type.

If t exceeds the critical value then the deviations from the perfect fit are not explained by the laws of chance and an improvement may be required.

(iii) Correlation Matrix. It is required to identify which factors are causing fluctuations in model accuracy, and one way to do this is to correlate the residual with each factor in turn. If it is found that some factor is always large when the residual is large, then that factor may be having a deleterious effect on the model. In the practical case, life is never quite as simple and we have to be satisfied with identifying the most likely factors. This is done by means of a matrix of correlation coefficients, commonly referred to as a correlation matrix.

The correlation coefficient is a standardized measure of the extent to which two variables are dependent on one another. For two variables x and y, the correlation coefficient r is defined as:

$$r = \frac{\text{Covariance } (x,y)}{\sigma x \cdot \sigma y}$$

where $\sigma x \cdot \sigma y$ is the product of the standard deviations of x and y. r varies between -1 and +1. Zero indicates no correlation and ± 1 indicates perfect (positive or negative) correlation.

Thus if there are a number of factors present, then each factor may be correlated with each factor to derive the correlation matrix. The correlations involving $\log_{10} (\lambda_o/\lambda_p)$ serve to indicate which factors are

causing model fluctuations. The other correlations provide additional useful information about the way in which the various factors interrelate with one another.

It is not intuitively obvious how large r has to be to indicate a significant correlation and so the sampling distribution of r is required. Exact derivation of the sampling distribution is difficult but an approximation is given by

$$r\sqrt{n-2}\,/\sqrt{1-r^2}$$

which has a t distribution (where n is the number of data pairs). These values are tabulated in Ref. 4. For example, an r value of 0.3 with 47 pairs of observations indicates a significant correlation at the 5% level. An r value of 0.01 with the same number of observations indicates no significant correlation and hence r is effectively zero.

An annotated example of the correlation matrix is given in Figure 6 below. Note that the terms above the diagonal would mirror those below and are not needed and therefore are not included.

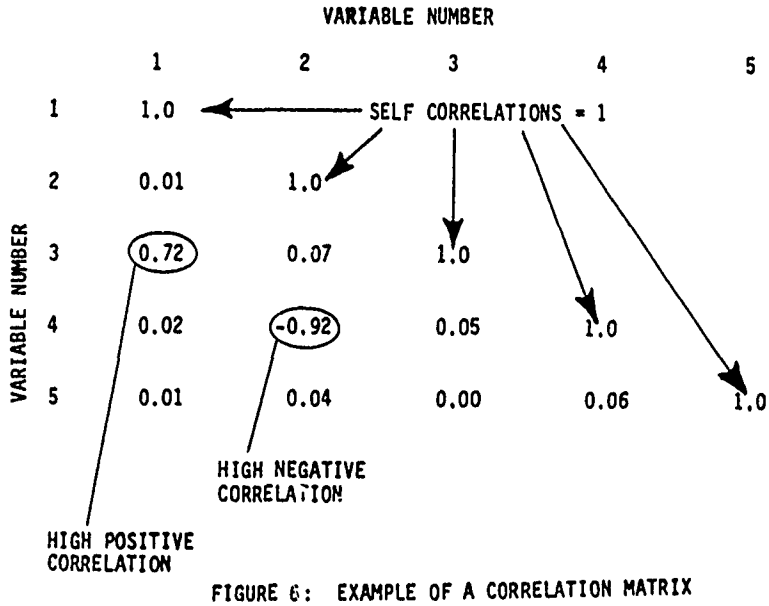


FIGURE 6: EXAMPLE OF A CORRELATION MATRIX

An objective assessment of which factors might cause model fluctuation is now possible and was used extensively in the analysis.

(iv) Wilcoxon Rank Sum Test. Where very little information is available in a particular class of data, it is sometimes not possible to apply the usual distribution statistics. Non-parametric tests may be used instead and they generally consider the probability of observing sequences of ranks under some null hypothesis.

Wilcoxon's rank sum test may be used instead of a parametric t test. Suppose two (small) sets of data are gathered and it is required to decide whether or not they are from the same distribution. The two sets are combined and ranked. The ranks for the smaller group are then summed (R). R^1 is then found from $R^1 = n_1 (n + 1) - R$

where

n_1 = number in smaller sample

n_2 = number in larger sample

n = total number $(n_1 + n_2)$

A critical value of w is then found from tables (Ref. 6) given n_1, n_2 and a significance level α. If either R or R^1 exceeds w then the hypothesis that both sets of data are from the same distribution is rejected.

The theoretical considerations in this test are given in Refs. 7 and 8.

(v) Goodness of Fit Testing. Since the sample sizes are often quite small, the Kolmogorov-Smirnov test is chosen for deciding how well some theoretical distribution fits a set of data.

If the observed cumulative distribution at some point x is evaluated as $F_O(x)$, and the theoretical cumulative distribution at the same point is evaluated as $F_E(x)$, then $D = \max. \left| F_O(x) - F_E(x) \right|$ is the Kolmogorov-Smirnov statistic. Tables of critical values of D are given in Ref. 3.

The test may also be used to compare two sets of data directly as an alternative to Wilcoxon's test. In that case, one would evaluate $D = \max \left| F_1(x) - F_2(x) \right|$.

(vi) Other Methods,

General. General statistical techniques are implemented throughout; those described previously were probably the most extensively used. References are provided for additional methods as necessary. Mathematics was also used as required, and, where necessary, formulae and derivations are provided.

Cautionary Note. It is extremely important to realize that when a series of separate statistical tests are performed, the significance levels can be invalidated. This is because of the fact that significant correlations can arise by chance with probability α. Thus if n tests are carried out, $n\alpha$ of them are expected to have arisen by chance. Care is therefore required in providing an explanation for each significant correlation. Since the significance level is not used other than to identify specific factors, we are not otherwise concerned with this phenomenon. Evaluation of exact significance is possible by construction of a multiple comparison test (of which analysis of variance and the Studentized range are examples). The interpretation of correlation matrices and "multiple" t-tests is tempered by this cautionary note.

Hypothesis Testing. This report assumes a rudimentary knowledge of the philosophy of statistical hypothesis testing, commonly referred to as the Neyman-Pearson theory. The points of that theory necessary to understanding this report are therefore summarized as follows.

First, a null hypothesis (H_0) is chosen; as far as possible this hypothesis should reflect the status quo. In many of the tests in this report, the null hypothesis is that the model is adequate. It is also

necessary to define an alternative hypothesis (H_1) in advance of carrying out the test. In this report the alternative is usually that the model is not adequate. It is also necessary to define a significance level (α) which is the acceptable risk of deciding that the model is not adequate, when in fact it is adequate. The statistical test is then performed and depending on whether the result is less than or greater than the tabulated critical value (Ref. 4) we accept or reject H_0 at that significance level. If we reject H_0, we have to accept H_1. This explains the use of the words "accept" and "reject" in many tabulated tests in this report.

The significance level α is traditionally taken as 0.05 (i.e., 5%). Depending on the particular study or experiment, one might specify a smaller risk (e.g., 1% or even 0.1%) or a greater risk (e.g., 10%). In view of the cautionary note above, α is taken in one case, in this report, to be 2½%. It should be noted that decreasing α increases β and vice-versa, where β is the risk of accepting H_0, when in fact H_1 is true (i.e., concluding the model is adequate when in fact it is not adequate). Note that the two risks are analogous to "producer" and "consumer" risks in a manufacturing process.

Thus, the lower the α, the more significant the finding. Strictly an α should be defined prior to starting the analysis; in this report, the conclusions are based on an α of 2½%. It is not orthodox to provide all significance levels as has been done in this report, but they are included to provide further information.

The two types of error, the significance levels, and the potential penalties are summarized as follows:

Truth/ Decision	H_0 True	H_1 True
Accept H_0	Model adequate and we decide it is adequate Everyone happy	Model inadequate and we decide is is adequate Users find models give bad predictions Probability β
Reject H_0	Model adequate and we decide it is not adequate Money wasted redoing a good model Probability α	Model inadequate and we decide it is inadequate Everyone happy

In practice it is never possible to eliminate these risks, α and β. In this study, it is very unlikely that the conclusions are erroneous since they are indicated by a series of tests and logical inferences rather than just one test based on a single sample.

3. MODEL VERIFICATION

3.1 Data File. A data file was created consisting of the data in Appendix 1. The file therefore consists of nearly six hundred line entries, each with fourteen variables entered in free format and defined as follows:

TABLE 2: VARIABLES USED IN DATA FILE

Variable Number	Name	Description
1	TECH	Technology type, coded as in Table 3.
2	COMP	Complexity expressed as number of gates or bits.
3	PKG	Package type, coded as in Table 4.
4	NPIN	Number of pins.
5	SC	Screen class, coded as in Table 5.
6	APEN	Application environment, coded as in Table 6.
7	TJ	Junction temperature in ^{o}C.
8	HRS	Total part hours.
9	#FAl	Total number of failures.
10	OB1	Lower 80% confidence limit on observed.
11	OB	Observed failure rate per 10^6 hr.
12	OB2	Upper 80% con.idence limit on observed.
13	PRED	Predicted failure rate per 10^6 hr.
14	LOG	Log_{10} (OB/PRED).

These codes are modified in the individual technology correlation matrices and defined above each matrix.

The codings used are given in the following four tables.

Table 3 Technology Coding

Technology Type	
Technology	Code
CMOS	1
HTTL	2
LSTTL	3
STTL	4
LTTL	5
TTL	6
ECL	7
Linears	8
PMOS	9
P-MNOS	10
NMOS	11
MNOS	12

Table 4 Package Coding

Package Type	
Package	Code
CMDIP	1
HDIP	2
PDIP	3
Can	4
HFPK	5
EDIP	6
SDIP	7
CDIP	8
CFPK	9
MGDIP	10
PINL	11
EINL	12

Table 5 Screen Coding

Screen Class	
Screen	Code
JB	1
JB/B-1	2
B-1	3
B-2	4
C-1	5
C-2	6
D	7
D-1	8

Table 6
Application Environment Coding

Environment	Code
GB	1
MGB	2
GF	3
GBC	4
GT	5
NSS	6
NS	7
AIF	8
AI	9
AUF	10
AIU	11
AIT	12

Non-numerical variables were coded numerically so that numerical methods could be approximately applied. Where possible the coding reflected the variable; for example, screen class was coded from 1 to 8 in order of decreasing screening level. In this way, approximate correlations, etc., could be derived for non-numerical data. Note that a non-parametric correlation coefficient (such as Spearman's rank correlation coefficient) might be more accurate in some cases but that we are not concerned with absolute accuracy in such computations; an ordering is sufficient. This point is, however, borne in mind when establishing significance of apparently highly correlated variables.

The data file thus created allows computer programs to be run efficiently for specified options.

3.2 General Analysis.

3.2.1 Correlation and Goodness of Fit Tests. The following options are first selected to establish any major trends of deviations.

(i) Correlation matrix for all variables, all data.
(ii) Logarithmic plot for all data, against technology type.
(iii) Logarithmic plot for all data, against screen class.
(iv) Logarithmic plot for all data, against environment.

(i) The correlation matrix is given in Table 7. The critical values of the correlation coefficient for the data (472 data points) were 0.0900 for a significance (α) of 5%, 0.1180 for α = 1% and 0.1501 for α = 0.1%. The smaller the α, the more significant the correlation. The values in the matrix were asterisked accordingly as defined in the legend.

Most significant correlations are easily explained and the obvious ones are not described here, e.g., observed with complexity. Some more obscure and some unexpected correlations require explanation.

TABLE 7: CORRELATION MATRIX, ALL DATA

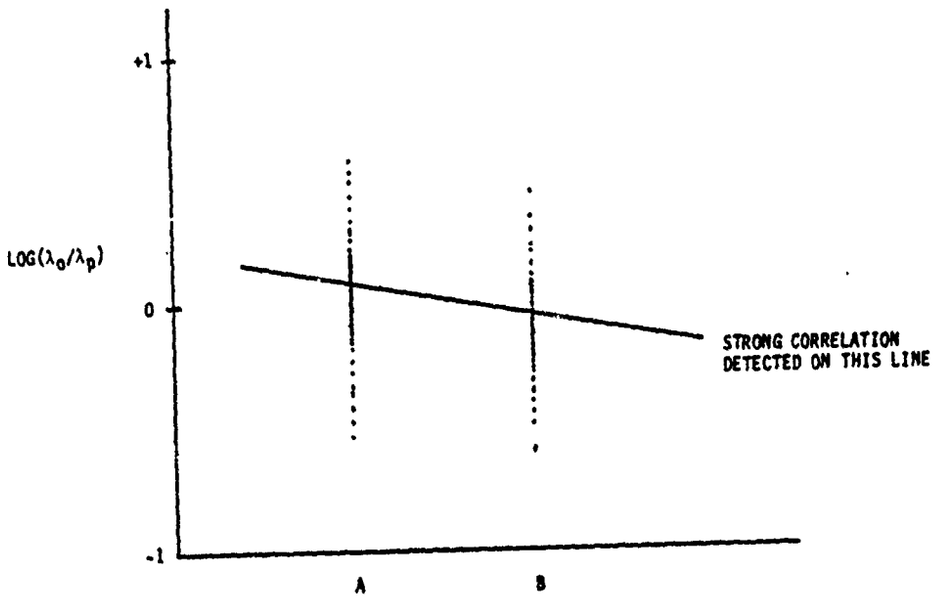
	TECH.	COMP.	PKG.	NPIN	SC	APEN	Tj	HRS	# FAI	OB1	OB	OB2	PRED	LOG
TECH.	1													
COMP	*** 0.393	1												
PKG.	*** 0.386	0.050	1											
NPIN.	0.005	*** 0.378	*** -0.270	1										
SC	*** -0.188	-0.090	-0.045	-0.033	1									
APEN.	* 0.095	-0.022	** 0.145	0.089	*** -0.535	1								
Tj	*** 0.253	0.030	*** 0.223	0.080	*** -0.388	*** 0.622	1							
HRS.	0.020	-0.015	-0.065	* -0.105	** 0.119	* -0.099	*** -0.153	1						
# FAI.	*** 0.160	0.025	0.062	*** -0.183	* 0.096	* -0.094	* -0.106	*** 0.822	1					
OB 1	*** 0.247	** 0.144	*** 0.275	0.085	-0.048	*** 0.172	*** 0.236	-0.069	0.089	1				
OB	*** 0.184	*** 0.169	*** 0.240	** 0.148	** -0.128	*** 0.277	*** 0.303	* -0.113	-0.014	*** 0.933	1			
OB 2	** 0.136	*** 0.178	*** 0.204	*** 0.184	*** -0.184	*** 0.366	*** 0.335	** -0.132	-0.074	*** 0.817	*** 0.969	1		
PRED	*** 0.294	*** 0.272	*** 0.310	0.069	0.053	* 0.101	*** 0.261	-0.087	-0.013	*** 0.343	*** 0.278	*** 0.218	1	
LOG	0.022	-0.060	-0.066	0.007	*** -0.292	0.011	-0.068	-0.043	0.078	*** 0.462	*** 0.450	*** 0.413	*** -0.265	1

LEGEND:

* Significant (5%)
** Highly Significant (1%)
*** Very Highly Significant (0.1%)

a) Technology vs. complexity (0.1%) - this correlation is attributable to the coding of the technologies. Those with large memories and the like, such as PMOS, NMOS, MNOS, are assigned the higher code values, so that LSI and VLSI technologies coincide with high code values.

b) Technology vs. package (0.1%) - this is a semi-spurious correlation attributable to the fact that many technologies divide into one or two groups of package. An example is sketched below for LTTL devices.



A AND B ARE HYPOTHETICAL GROUPINGS OF THE DATA

FIGURE 7: FORCED CORRELATION

For ease of explanation, this phenomenon will in future be referred to as the forced correlation.

c) Technology vs. screen class (0.1%) - similar to (a), the particular sample of data used for this study included a large number of digital parts of D-1 and D screen but there was a higher proportion of better quality parts in PMOS, NMOS, etc. From here on, this type of correlation is referred to simply as a sample correlation.

d) Technology vs. application environment (5%) - probably a sampling correlation but possibly also attributable to selective employment of certain technologies in different environments, due to the unique characteristics of each technology.

e) Technology vs. temperature (0.1%) - different technologies tend to have different operating junction temperature ranges.

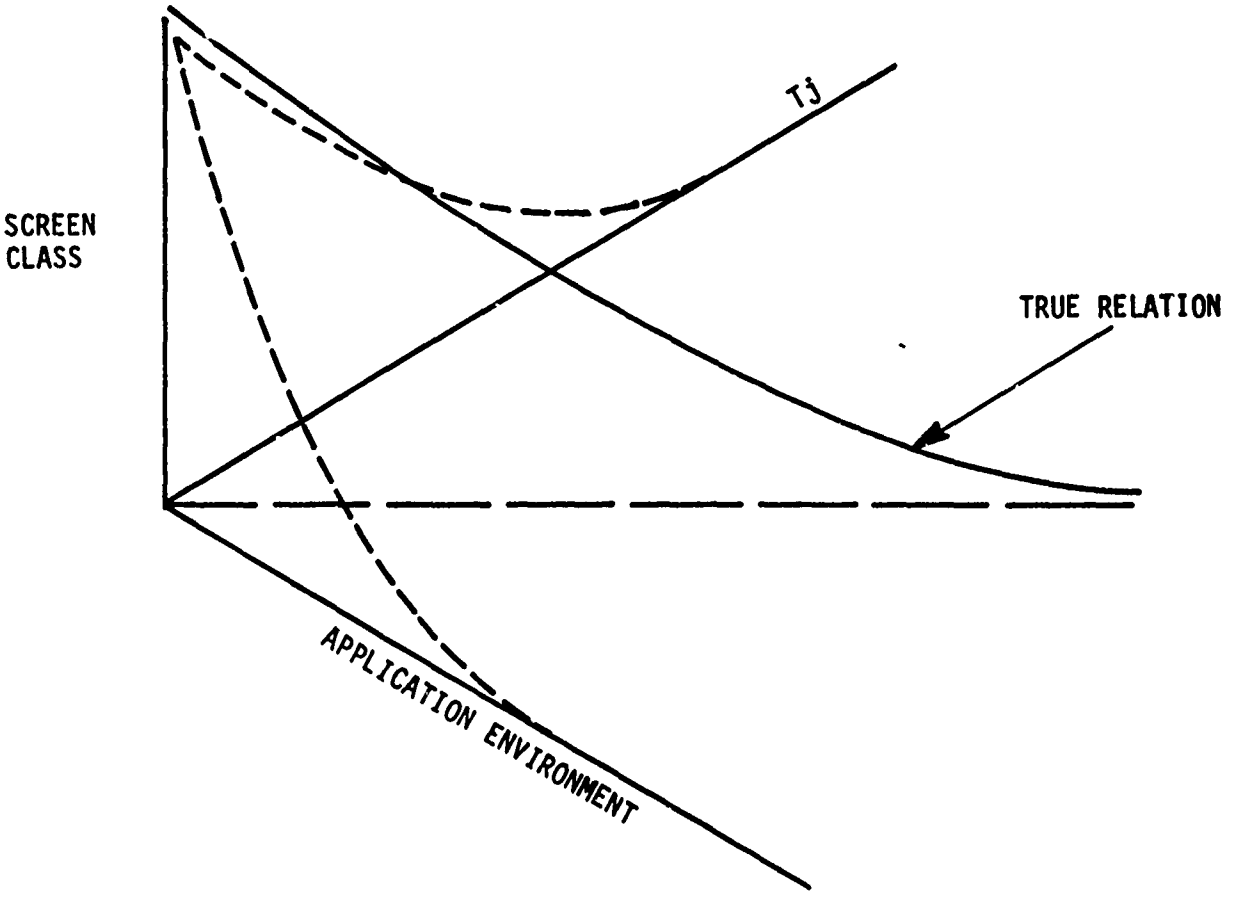
f) Technology vs. number of failures (0.1%) - more data is available in certain technologies, i.e., it is a sampling correlation.

g) Technology vs. observed (0.1%) - a combination of sampling and forced correlation resulting in a spurious correlation, although it is also true that different technologies have generally different failure rates. This also explains the correlations of technology with OB1 and OB2.

h) Technology vs. predicted (0.1%) - spurious (see g above).

i) Package vs. number of pins (0.1%) - there is a tendency for different package types to have certain ranges on numbers of pins but this is essentially a forced correlation.

j) Screen class, junction temperature and application environment (all 0.1%) - there is always a strong correlation between these three factors, since military environments use military quality parts, and temperature is a characteristic of environment. The orientation of their inter-relationships is sketched in Figure 8.



DOTTED LINES SHOW OBSERVED CORRELATIONS, THE PROJECTIONS OF THE TRUE RELATION ONTO THE DEFINED THREE PLANES

FIGURE 8: INTER-RELATIONSHIP BETWEEN SCREEN-CLASS, ENVIRONMENT AND TEMPERATURE

k) Number of pins vs. number of hours (5%) - probably a sampling correlation but certainly spurious. Similarly for hours vs. screen class (1%), which may also be due partially to more data being available in D and D-1 screen parts. Also applies to application environment and number of hours (5%); in addition, certain environments have typically larger sorties or missions.

l) Junction temperature vs. number of hours (0.1%) - more data is available at certain temperature ranges.

m) Number of hours vs. observed failure rate (5%) - may indicate an overall decreasing hazard rate (since the correlation is negative) but more specific matrices (for each technology) are required to investigate fully, since this matrix represents all technologies combined. Requires further investigation.

n) The observed and predicted failure rates are correlated with most factors as expected.

o) $\text{Log}_{10}\ (\lambda_o/\lambda_p)$ vs. screen class (0.1%) - requires further investigation, the implication being that the fit of the model is strongly dependent on screen class. It should be remembered that screen class appears to be correlated with technology on the evidence of this data and this must also be given further consideration.

p) $\text{Log}_{10}\ (\lambda_o/\lambda_p)$ vs. observed (0.1%) - a requisite of the ratio plot, i.e., as observed increases, the ratio plot increases. Similarly for predicted with $\log_{10}\ (\lambda_o/\lambda_p)$, (0.1%) - ratio plot decreases as predicted increases (correlation negative).

All but two of the above correlations are explained, and these require further investigation which is described in later stages of this report.

(ii) The logarithm ratio plot is first performed to achieve an approximate indication of the general performance of the model. The first ratio plot is run with technology type as the independent variable. The results are shown in Figure 9 below.

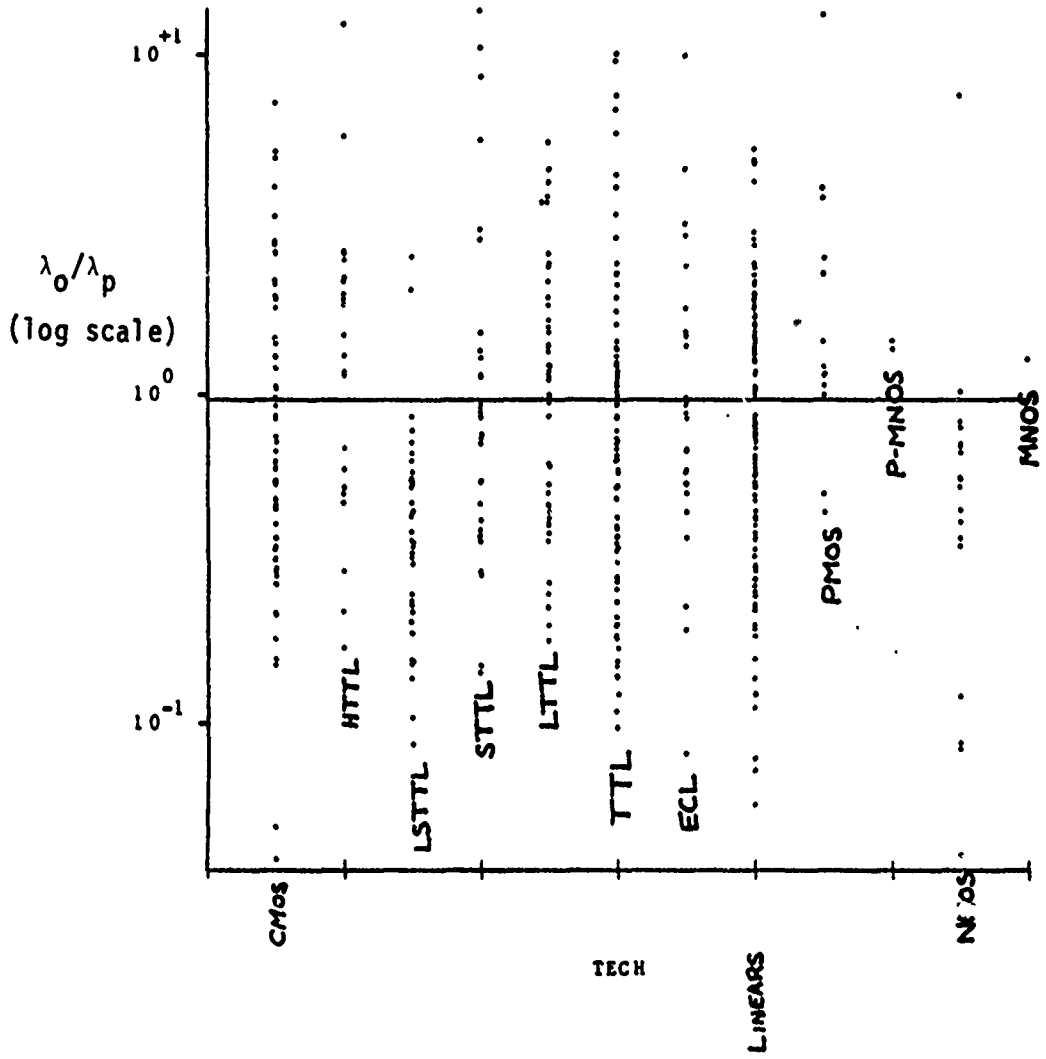


FIGURE 9: RATIO PLOT, AGAINST TECHNOLOGY TYPE

This plot indicates how well the model performs for each technology but it should be noted that some samples are very small and as such may be misleading because of sampling errors.

The sample size by technology is presented in Table 8 below.

TABLE 8: SAMPLE SIZES

CMOS	62	ECL	26
HTTL	23	Linears	115
LSTTL	38	PMOS	15
STTL	31	P-MNOS	2
LTTL	46	NMOS	18
TTL	95	MNOS	1

To decide which samples were significantly different from the perfect fit a t test on each mean was performed as defined in Section 2(ii). The following table gives all relevant statistics and decisions for each technology. An approximate method was used to evaluate the mean and S, since this is a preliminary analysis.

TABLE 9: TEST OF MODEL GOODNESS OF FIT, BY TECHNOLOGY

Technology	Sample size (n)	Mean log $(\lambda_0\lambda_p)$	Standard deviation	t	Decision
CMOS	62	-0.1739	0.433	-3.16	Reject (0.2%)
HTTL	23	0.1338	0.501	1.28	Accept
LSTTL	38	-0.4230	0.282	-9.25	Reject (0.2%)
STTL	31	-0.0535	0.574	0.52	Accept
LTTL	46	0.0624	0.449	0.94	Accept
TTL	95	-0.107	0.449	-2.32	Reject (5%)
ECL	26	-0.048	0.494	-2.02	Reject (10%)
Linears	115	-0.161	0.391	-0.23	Accept
PMOS	15	0.098	0.470	0.81	Accept
P-MNOS	2	—	—	—	—
NMOS	18	-0.246	0.418	-2.5	Reject (5%)
MNOS	1	—	—	—	—

Thus the mean of the samples for CMOS & LSTTL technologies were found to have greater deviations from the perfect fit than chance would indicate at the stated significance levels. This may be due to the model or it may be due to some other correlated factor. This will be assessed later. At this point the deviation has been noted and requires further investigation and subsequent explanation. Although it is not usual practice to present all the significant levels (one normally defines a single α in advance) they are given to provide additional information.

(iii) The ratio plot is repeated with screen class as the independent variable. The resultant plot is shown below in Figure 10.

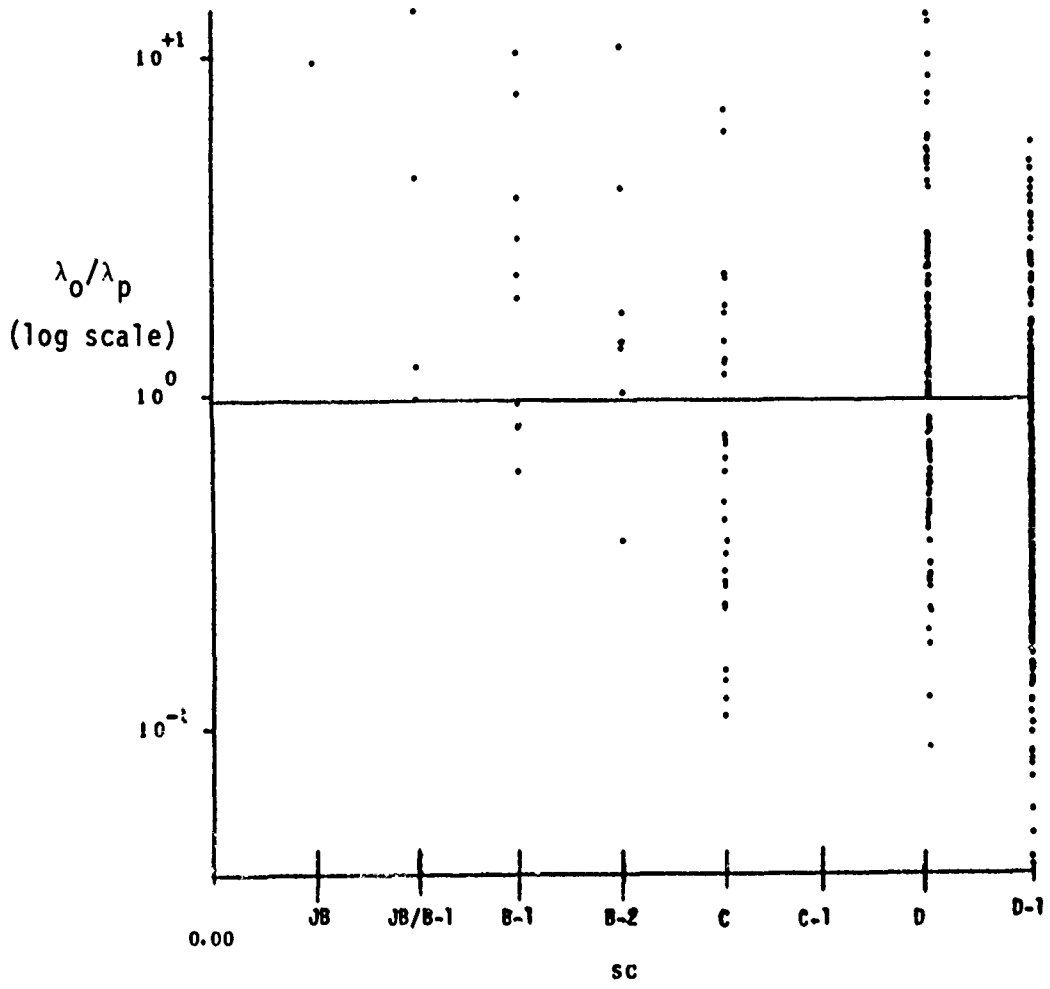


FIGURE 10: RATIO PLOT, AGAINST SCREEN CLASS

Table 10 below gives all relevant statistics and sample sizes.

TABLE 10: TEST OF MODEL GOODNESS OF FIT BY SCREEN CLASS

Screen Class	Sample Size (n)	Mean $\log(\lambda_o/\lambda_p)$	S	t	Decision
JB	1	—	—	—	
JB/B-1	4	0.483	0.533	1.81	Accept
B-1	10	0.335	0.433	2.44	Reject (5%)
B-2	7	0.276	0.458	1.60	Reject (20%)
C-1	29	-0.187	0.458	-2.20	Reject (5%)
C-2	0	—	—	—	—
D	134	0.107	0.458	2.71	Reject (1%)
D-1	289	-0.558	0.416	-22.8	Reject (0.01%)

Clearly there was insufficient information on some screen classes to apply a t test with validity. This problem is addressed further under the detailed section on screen class (Section 3.3.6). A conclusion at this stage, though, is that there was no evidence to show that the model was not performing satisfactorily with respect to screen class, with the notable exception of class D and D-1 screens. Failure rate predictions for D and D-1 screen classes deviated very significantly from the perfect fit for this sample of data. This required an explanation, which is given later.

(iv) The ratio plot is repeated with application environment as the independent variable. The resultant plot is shown in Figure 11.

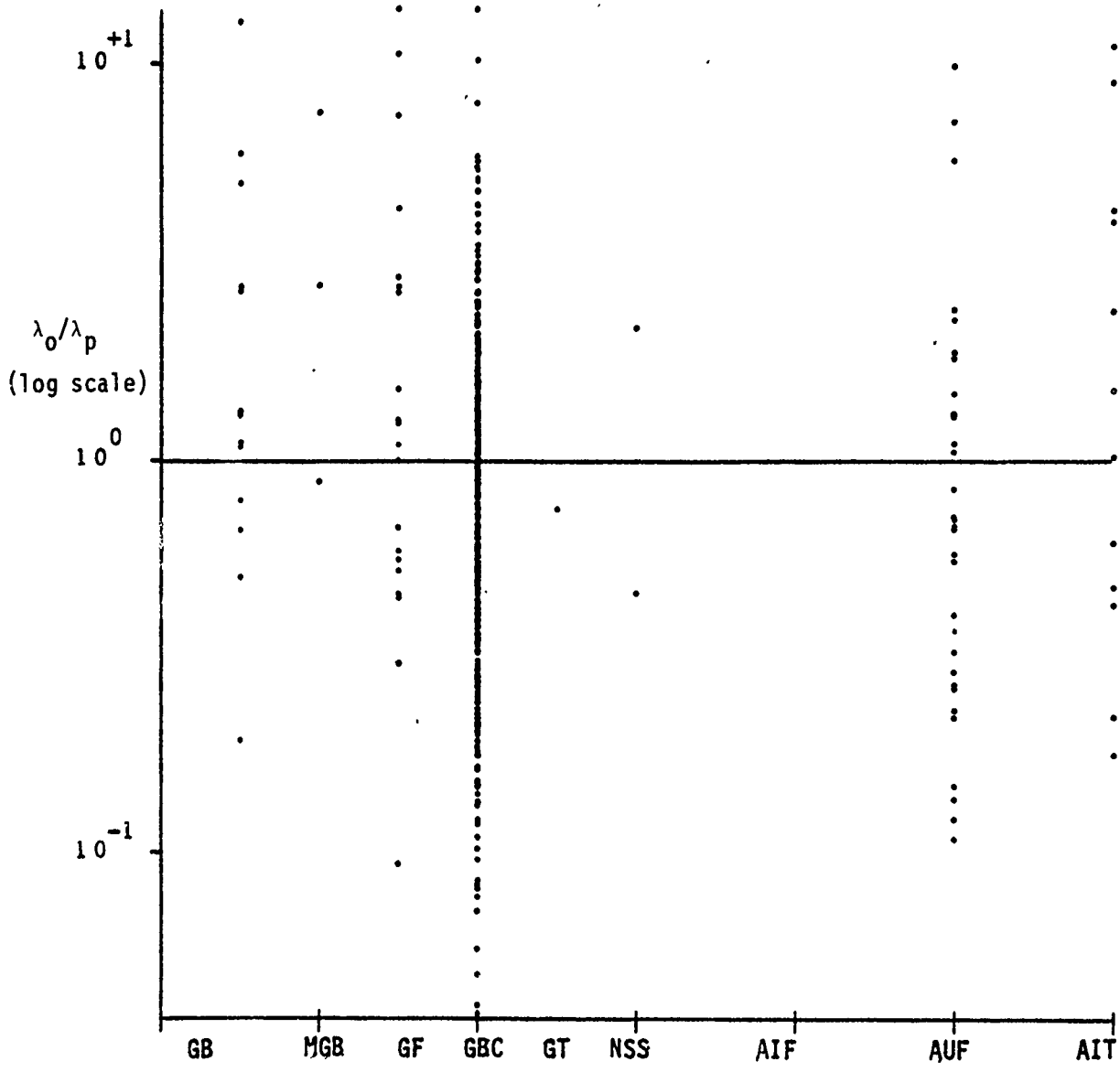


FIGURE 11: RATIO PLOT, AGAINST APPLICATION ENVIRONMENT

The relevant sample sizes and statistics are given in Table 11 below.

TABLE 11: TEST OF MODEL GOODNESS OF FIT BY APPLICATION ENVIRONMENT

Environment	Sample size (n)	Mean $\log_{10}(\lambda_o \lambda_p)$	s	t	Decision
Ground, Benign	13	0.119	0.568	0.76	Accept
Missile, Ground, Benign	3	0.442	0.467	1.64	Accept
Ground, Fixed	20	0.070	0.537	0.58	Accept
Ground, Benign, Commercial	388	-0.133	0.620	-4.24	Reject (0.05%)
Airborne, Uninhabited (Fighter)	31	0.159	0.620	1.43	Reject (20%)
Airborne, Inhabited (Transport)	12	0.091	0.690	0.46	Accept

The only significant departure from the perfect fit was exhibited by the Ground Benign, Commercial (GBC) environment. This consistently predicted higher than observed. Again an explanation is required.

3.2.2 Review of General Analysis. Combining the information in hand gave preliminary information as to where the model accuracy was unsatisfactory.

Very poor model performance was exhibited by D-1 screen class data, by LSTTL technology data, and by GBC environment data. The correlation matrix showed a correlation between screen class and environment; hence the observations could be from the same cause. Close inspection of the data confirmed this since all LSTTL data was GBC/D-1. To identify which factor was the cause, the GBC environment, D screen class data was considered and found not to follow the GBC/D-1 trend. The inference is, therefore, that the screen class was the cause. The inference is supported by the correlation matrix where screen class was identified as the only significant factor. Strictly speaking, an analysis of variance should be

performed on D and D-1 data for two different environments to fully confirm the inference; unfortunately, not enough data was available in any other environment for D and D-1 screen class.

The findings of this general analysis were therefore that the π_Q factor required re-evaluation for the D-1 screen. Currently it is assigned a value of 35, which is too large. Whether this was due to the particular sample of data is not known. There is a possibility that the parts were burned-in and screened after procurement since this would have the same deleterious effect on the goodness of fit of the model.

Before performing a detailed analysis the π_Q factor required correction because the bad fit interfered with the analysis. It should not be inferred that a change in MIL-HDBK-217C is recommended or that the same effect would be noted in all data. This correction was effected by forcing the mean of the D-1 screen data through the line of perfect fit.

Considering D-1 data only,

Let θ_1 be the mean $\log_{10} (\lambda_o/\lambda_p)$ for technology 1.
Let θ_2 be the mean $\log_{10} (\lambda_o/\lambda_p)$ for technology 2.

In general,

Let θ_i be the mean $\log_{10} (\lambda_o/\lambda_p)$ for technology i.
Let n_1 be the sample size for technology 1.
Let n_2 be the sample size for technology 2.

In general,

Let N_i be the sample size for technology i.
Let the total sample size be N.

i.e.

$$\sum_{i=1}^{12} n_i = N$$

then

$$\rho = \left[\prod_{i=1}^{12} \theta_i^{n_i} \right]^{1/N}$$

is the weighted geometric mean of $\log_{10} (\lambda_o/\lambda_p)$. (When dealing with ratios, a geometric mean is preferred.) Evaluating ρ from the data in Table 10 gave 0.558. Since π_Q is a multiplier in the MIL-HDBK-217C model (Ref. 2), the adjustment is made by finding $\rho\pi_Q$.

Hence, the adjusted π_Q for D-1 screen was $0.558 \times 35 \simeq 19.54$

Strictly a least squares fit should be used to optimise π_Q. The weighted geometric mean technique will optimise only approximately but was quite sufficient for the purposes of this study and was considerably quicker in synthesis. The π_Q factor for D data was not adjusted since it did not so severely hamper the investigation.

3.3 Detailed Analysis.

3.3.1 Data File and Program Options. The data file was updated to include the adjusted π_Q factor for D-1 screen class devices. Corresponding adjustments to $\log_{10} (\lambda_o/\lambda_p)$ were made. A family of correlation matrices and ratio plots were run to identify those factors causing model fluctuations. The data were first separated into technologies. For two technologies there was not enough data to apply the correlation matrix/ratio plot method and these were given special considerations separately. The two technologies were P-MNOS and MNOS. Then for each of the other ten technologies the following options were selected:

(i) A correlation matrix for each technology after adjustment of π_Q, giving a total of ten matrices.

(ii) Two ratio plots with complexity as the independent variable, one plot before adjustment of π_Q and one after adjustment.

(iii) Two ratio plots with application environment as the independent variable, before and after adjustment.

(iv) Two ratio plots with screen class as the independent variable, before and after adjustment.

(v) Two ratio plots with junction temperature as the independent variable, before and after adjustment.

Options (ii) to (v) give a total of eighty plots and a number were included in this report. The correlation matrices are included in Appendix B and a summary of the salient points is given in Table 12. The table shows which factors were correlated with $\log_{10}(\lambda_o/\lambda_p)$ by asterisks, whose legend is as before. In addition, a plus (+) indicates positive correlation, a minus (-) indicates negative correlation.

The positive correlations of $\log_{10}(\lambda_o/\lambda_p)$ with observed in all cases and the negative correlations with predicted in some cases was simply due to the method used, i.e., $\log_{10}(\lambda_o/\lambda_p)$ was forced to correlate with both observed and predicted.

The other correlations are considered in detail in Sections 3.3.2 to 3.3.8.

A selection of ratio plots, particularly those referenced in this report, have been provided in Appendix C. Their consultation is not essential to understanding the text but they considerably enhance an understanding of the points made and the data generally.

TABLE 12: FACTORS CORRELATED WITH MODEL FIT ($\log_{10} \lambda_o/\lambda_p$)

Tech.	Complexity	Package Type	# Pins	Screen Class	Application Environment	Junction Temp.	# of Failures	Observed	Predicted
CMOS	* -	* -		* -		*** -		*** +	*** -
HTTL		-	-				** +	*** +	
LSTTL								*** +	
STTL	* +			** -	* +			** +	
LTTL		*** +		*** +	*** -	*** -	** +	*** +	** -
TTL			*** -		* -	*** -		*** +	*** -
ECL								*** +	* -
Linears	*** -				* -	* -		*** +	*** -
PMOS								* +	
NMOS		* -	* +					*** +	

LEGEND:
* Correlation significant (5%)
** Correlation highly significant (1%)
*** Correlation very highly significant (0.1%)
- Negative correlation
+ Positive correlation

The factors influencing the model performance are now considered one by one in detail. The order in which they are considered is chosen so that inferences accumulate logically. In this way it is hoped to provide a readable account of a complex decision process. Additional ratio plots were run as necessary for specific investigations, and these are defined in each section. The relevant ratio plots are referenced at the end of each section.

3.3.2 Package Type. A ratio plot for all data with package type as the independent variable was run. This plot shows that there were no general problems with the package complexity factor C_3.

The correlations of $\log_{10}(\lambda_o/\lambda_p)$ with package, noted for CMOS, LTTL and NMOS are predominately sampling and forced correlations. It is possible that the values for C_3 in some cases are not truly optimal for the population but there is no evidence in this data to reject the current package complexity factor tables, wholly or partially.

Ratio Plot 1

3.3.3 Number of Pins. The number of pins affects both the package complexity factor C_3 and the estimated junction temperature T_j. Hence, any fluctuations in model performance with number of pins could affect both C_3 and T_j. A ratio plot was run for all data with number of pins as the independent variable. This plot shows that generally there are no serious problems with the model with respect to number of pins. Correlations previously noted in TTL and NMOS data appear to be forced.

Ratio Plot 2

3.3.4 Number of Failures. A strong correlation here would indicate an increasing or decreasing hazard rate. Although correlations are found in HTTL and LTTL data, there is not enough information to adequately assess the hazard rate. However, an indication is possible and an example is given in Figure 12 for TTL data. This graph shows how the failure rate estimate typically varies with number of failures per record (r); clearly this effect is simply due to the central limit theorem, (See Section 4), since the variability at low r is much greater than at r in excess of about 12. A running mean in steps of 5 on the r axis is shown by a dotted line, and a further smooth of that line (using the median of three) is constant at a value of $\hat{\lambda}$ which coincides almost exactly with the maximum likelihood

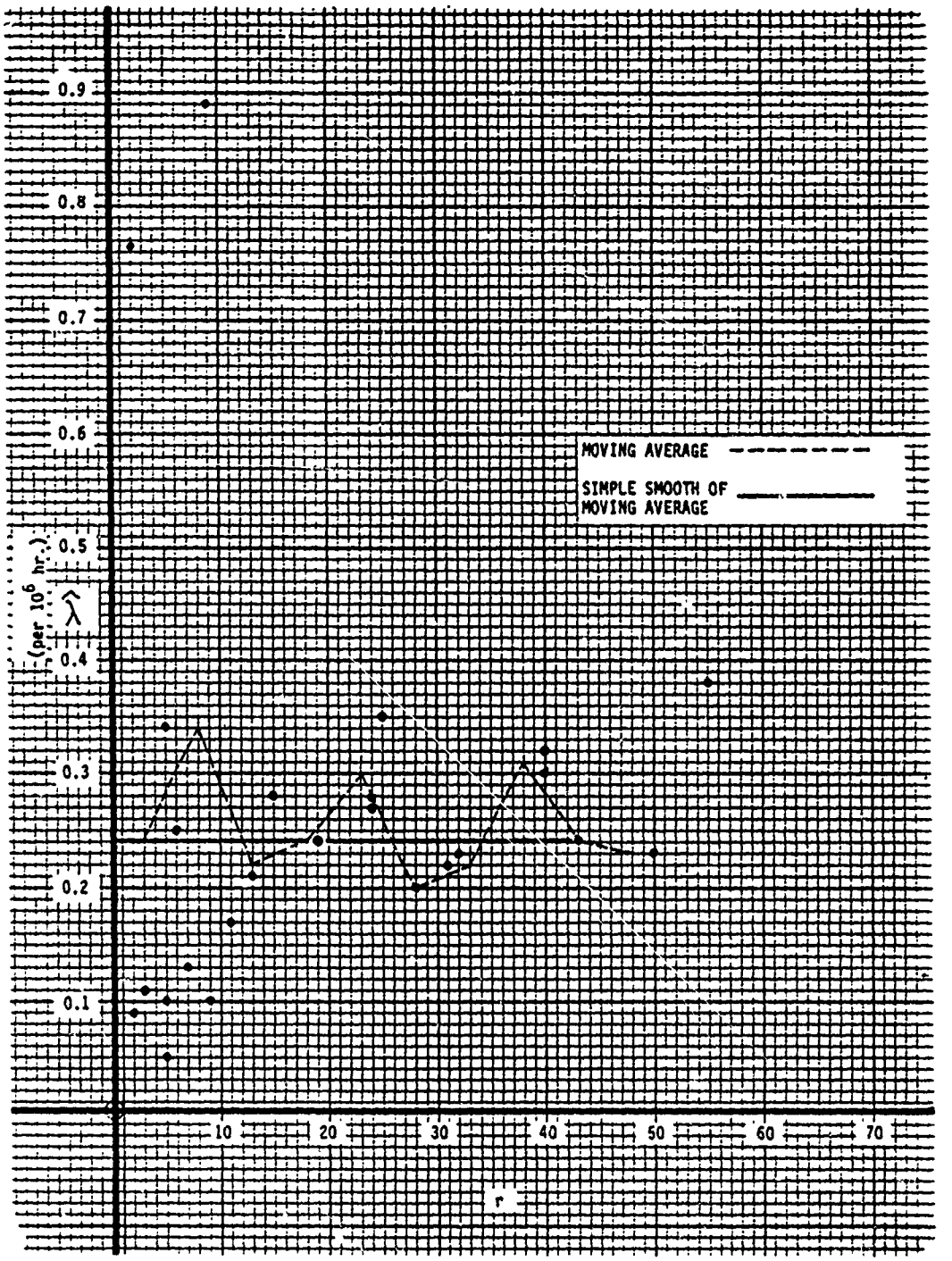


FIGURE 12: GRAPH OF THE MAXIMUM LIKELIHOOD ESTIMATOR OF FAILURE RATE ($\hat{\lambda}$) vs. "r", THE NUMBER OF FAILURES PER RECORD.

estimator of λ. Since the final smooth is extremely powerful, not too much emphasis should be placed on its constancy, but it provides reasonable support for the exponential (i.e., constant λ) model, for the data used here. Not all data sets are as well-behaved and some appear to have non-constant hazard rates initially but there is not enough data to confirm this.

Note that the data for smaller r probably give rise to the more extreme points in the ratio plots, and this is confirmed by reference to the correlation matrices where r is often correlated with $\log_{10}(\lambda_o/\lambda_p)$.

The distribution of time to failure is considered analytically in Section 4.

3.3.5 Complexity. There are three correlations with complexity, namely in STTL, CMOS and linear technologies. The correlation for STTL data is found to be spurious since it is the result of a couple of rogue points. The remaining two correlations are noted in CMOS and linear device data. Reference to the relevant ratio plots shows that there is indeed a definite although gentle slope in each case. A moving average is superimposed by hand with a continuous line. The trend is emphasized by the dotted line which is a simple smooth of the continuous line. Both technologies are seen to exhibit optimistic predictions for small complexities (since $\log_{10} \lambda_o/\lambda_p > 0$) and gradually move to pessimistic predictions at higher complexities. The perfect fit appears to be in the region of 25 gate complexity. It is worthy of note that the temperature factors for both CMOS and linear devices (but no other technologies) are estimated from the same table in MIL-HDBK-217C. While this would not directly explain the model dependence on complexity, there may be a complex relation between temperature and complexity. This is quite feasible for CMOS data where a simple correlation between temperature and complexity is found (significant at 1%). For linear device data, however, such a relation is less likely with almost zero correlation between temperature and complexity.

Overall the fit of the model with respect to complexity is good, and although a strong correlation is found between the ratio plot and complexity, the magnitude of the associated errors is small. Summarizing, there is high correlation with low bias. Any improvement to the model would be slight and this would have to be traded off against the time involved in recalculating the tables and the possibility of degrading the model in other areas (hereafter referred to as the domino effect).

If the improvement were considered worthwhile attempting, the complexity table (C1 & C2) for linear devices is independent of any other technology and therefore could be easily adjusted. For CMOS, the complexity table applies to all MOS technologies; hence its adjustment is not so simple and would probably necessitate a break out into separate tables for each variation of MOS technology.

Ratio Plots 3 & 4

3.3.6 Screen Class. Correlations noted for CMOS, STTL and LTTL data are forced (CMOS, LTTL) or due to rogue points (STTL) and as such do not indicate a trend in model goodness of fit with screen class. It is still of course possible that individual screen class data may not be adequately modelled. A ratio plot of all data with screen class as independent variable was run. As expected, D-1 data is now well modelled with very little bias, confirmed by a t value of 0.022 (not significant). The remainder of the screen classes are of course unaltered from the fits defined by the t values of Section 3.2.1 (iii) Table 10.

π_Q for D screen class has not been modified in study since it was not as badly biased as that for D-1. Nonetheless, a significant deviation from the perfect fit is noted with predictions tending to be optimistic. Since the majority of D screen class components are linear devices, the domino effect in all other technologies would be expected to be small. In linear

devices, the effect of a modified π_Q for D screen would result in a virtually perfect model. Numerically the ideal value for π_Q on the sample data would be in the region of 20.

Ratio Plot 5

3.3.7 Application Environment. The correlations noted for STTL, LTTL, TTL and linear devices are either forced or due to rogue points. They do not signify a general trend in model performance with respect to environment. The tendency for Ground Benign, Commercial data to exhibit extremely pessimistic predictions has been corrected by adjustment of the π_Q for D-1 screen parts, with which there is very high correlation. The t value for GBC data is now 0.021 which is not significantly different from the perfect fit.

Ratio Plot 6

3.3.8 Junction Temperature. Negative correlations are noted for CMOS, LTTL, TTL and linears. The first three are significant at the 0.1% level and the fourth is significant at the 5% level. Reference to the corresponding ratio plots confirms that there is a definite trend with junction temperature. There are a number of possible reasons for this effect and it is not possible to isolate a definite cause (or causes) statistically. Possible causes will be reviewed. Reference to ratio plots 7, 8, 9 and 10 illustrates the following discussion.

The first possibility is that the temperature tables used to evaluate the π_T factor are in error. The tables are derived from

$$\pi_T = 0.1 \exp\left[-A\left(\frac{1}{(T_j + 273)} - \frac{1}{298}\right)\right] \quad \ldots\ldots\ldots\ldots\ldots (1)$$

For LTTL and TTL data the slope and location of π_T are apparently incorrect. For CMOS and linear device data, the slope only of π_T is

apparently incorrect. This may be at least partially attributable to selective sampling by temperature on a π_T curve having an incorrect slope. This possibility is illustrated by the sketch below.

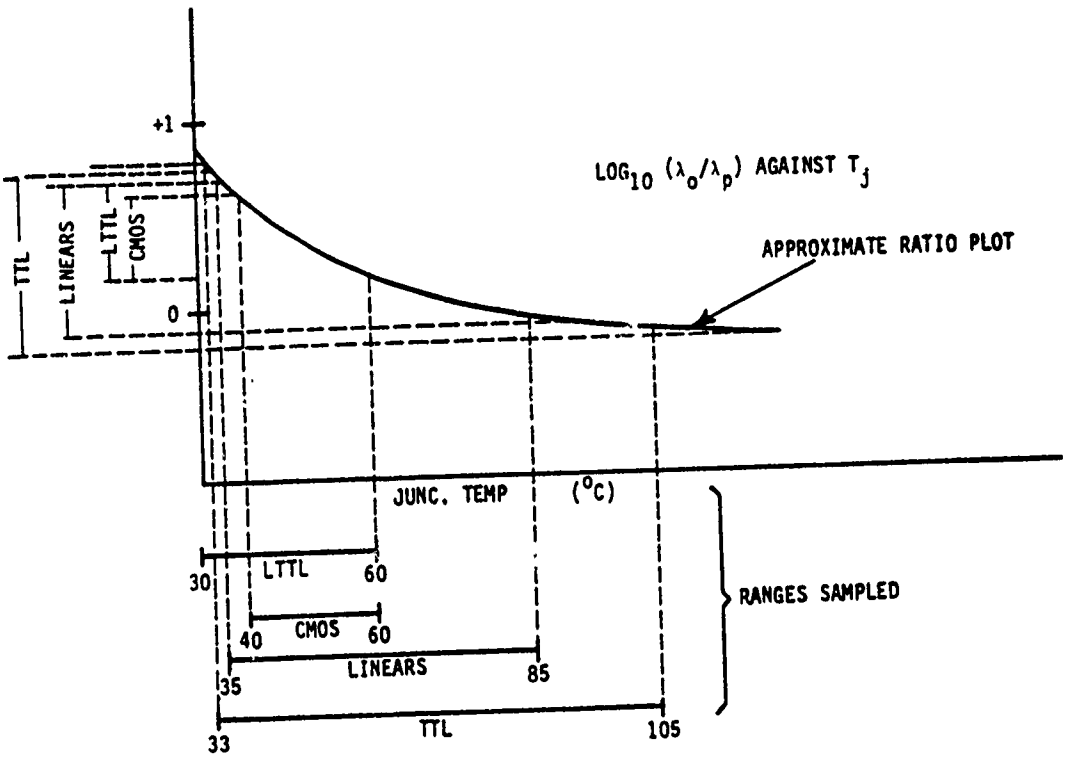


FIGURE 13: EFFECT OF SAMPLING RANGE

Care is required in any π_T adjustment to insure that the population (rather than the sample) is modelled in this respect.

The second possibility is that the model for estimating junction temperature may be inaccurate. This model is given by:

$$T_j = T_C + \theta_{jc} P$$

where

T_j = the junction temperature
T_C = the case temperature
θ_{jc} = the junction to case thermal resistance
P = the worst case power dissipation

T_C in turn is estimated directly from the environment according to a further tabulation. Any errors in the estimation of T_j would affect the subsequent evaluation of π_T.

A final possibility is that there is partial complexity dependence as noted in Section 3.3.4. Such a temperature/complexity correlation is found in CMOS data only and is therefore considered unlikely in general although it could well be a factor in the CMOS model alone.

Summarizing, a strong temperature dependence of $\log_{10}(\lambda_p/\lambda_b)$ is found in certain technologies which is due to either one or a combination of the following:

(i) The π_T equation (1) may be inaccurate, or the data to which it was fitted may have been biased.

(ii) The T_j estimation formula may be inaccurate.

(iii) Correlation with some other factor such as complexity may exist and degrade model performance.

Statistically there is no means of deciding with certainty which of these possibilities is the cause, although the correlation matrices tend to rule out (iii). Considering (i) and equation (1) above, A is the equivalent activation energy divided by Boltzmann's constant.

The equivalent activation energy Eea is used to show that the failure rate of a particular device type exhibits essentially the same temperature dependence as a device failing due to only one failure mechanism having an activation energy Ea=Eea. Since an activation energy Ea may only be associated with a specific mechanism, when speaking of the temperature dependence of failure rate of a device failing due to the cumulative effects of several mechanisms, it is reasonable to express the gross temperature dependence of failure rate for that device in terms of an equivalent activation energy Eea. It should be understood that while Ea is a constant, valid at any temperature, Eea will be approximately constant only for a limited temperature range. For many circumstances, the concept of equivalent activation energy provides a simple, convenient means of expressing the temperature dependence of failure rate for a variety of semiconductor components operating at "typical" temperatures.

It is possible that the equivalent activation energy was inaccurately assessed but there is no new information to justify changing it. Even if it were possible to justify increasing the equivalent activation energy, the resultant shift in π_T values would be small and furthermore would not correct the slope of the model with respect to T_j.

This is illustrated in Table 13 which gives a comparison for LTTL data between the current model and the model with an equivalent activation energy increased by 0.05 eV. The record number refers to the data line in Appendix 1.

TABLE 13: LTTL DATA WITH DIFFERENT ACTIVATION ENERGY (E_{ea}) ASSUMPTION

Record #	Complexity	Screen	Environment	Current Prediction	Prediction with Increased E_{ea}.
16	2	D	AIT	0.320	0.326
17	2	D-1	GBC	0.112	0.113
35	3	D	AIT	0.330	0.336
36	3	D-1	GBC	0.112	0.117
53	4	D	AIT	0.340	0.340
54	4	D-1	GBC	0.112	0.113
55	4	D-1	"	0.117	0.119
72	5	D-1	"	0.117	0.120
86	6	D-1	"	0.117	0.115
87	6	D-1	"	0.123	0.122
104	8	D-1	"	0.123	0.121
105	8	D-1	"	0.128	0.129
117	10	D-1	"	0.134	0.137
126	12	D	AIT	0.360	0.367
127	12	D-1	GBC	0.123	0.121
128	12	D-1	"	0.134	0.133
139	14	D-1	"	0.134	0.138
140	14	D-1	"	0.173	0.162
146	15	D-1	"	0.140	0.143
154	16	D-1	"	0.162	0.163
165	17	D-1	"	0.162	0.167
172	18	D-1	"	0.162	0.169
179	19	D-1	"	0.167	0.172
185	20	D-1	"	0.154	0.164
186	20	D-1	"	0.184	0.191
136	24	D-1	"	0.201	0.216
201	25	D	AIT	0.780	0.677
202	25	D-1	GBC	0.151	0.152
203	25	D-1	"	0.173	0.179
209	27	D-1	"	0.179	0.181
216	30	D-1	"	0.179	0.186
223	33	D-1	"	0.179	0.184
230	36	D-1	"	0.184	0.196
238	37	D-1	"	0.162	0.109
240	38	D-1	"	0.201	0.209
246	40	D-1	"	0.201	0.211
258	45	D-1	"	0.195	0.204
266	48	D-1	"	0.184	0.188
272	50	D-1	"	0.201	0.209
275	51	D-1	"	0.195	0.201
282	54	D-1	"	0.207	0.212
295	59	D-1	"	0.218	0.231
298	60	D-1	"	0.313	0.327
307	65	D-1	"	0.218	0.230
371	16	D-1	"	0.212	0.244
381	64	D-1	"	0.318	0.347

It is easy to explain mathematically the table results by considering the effect of π_T on the prediction. This is derived analytically below to show how a change in π_T can have a small effect on the overall model, numerically.

The prediction model is:

$$\lambda_p = \pi_Q \left[C_1 \pi_T \pi_V + (C_2 + C_3) \pi_E \right] \pi_L \qquad \text{(Ref. 2)}$$

where

λ_p = the device failure rate per 10^6 hours
π_Q = the quality factor
π_T = the temperature acceleration factor
π_V = the voltage derating stress factor
π_E = the application environment factor
C_1 and C_2 = circuit complexity factors
C_3 = the package complexity factor
π_L = the device production learning factor

For the LTTL data used, $\pi_L = 1$ and $\pi_V = 1$.

Hence, $\lambda_p = \pi_Q \left[C_1 \pi_T + (C_2 + C_3) \pi_E \right]$

If λ_p is to be adjusted by a factor of C, to $\lambda_p{}^1$ by adjusting π_T to $\pi_T 1$.

$$\lambda_p{}^1 = \pi_Q C_1 \pi_T{}^1 + (C_2 + C_3) \pi_E \pi_Q$$

Putting $\pi_Q C_1 = A$ and $(C_2 + C_3) \pi_E \pi_Q = B$

Then $\lambda_p{}^1 = A \pi_T{}^1 + B$

and $\lambda_p = A \pi_T + B$

but $\lambda_p{}^1 = C\lambda_p$

so $A \pi_T{}^1 + B = C(A \pi_T + B)$

$$\pi_T{}^1 = C \pi_T + \frac{B(C-1)}{A}$$

which gives a simple means of calculating $\pi_T{}^1$ given C.

If we assume for a first order approximation that A and B are of the same order, then

$$\pi_T^1 \simeq C\,\pi_T + (C-1)$$

So

$$\pi_T^1 \simeq C\,(\pi_T + 1) - 1 \quad \ldots\ldots\ldots\ldots (2)$$

Hence a 50% increase in π_T will only induce a 25% increase in λ_p. This approximation was used in quickly assessing various options for π_T adjustment. It was found to give very good approximations.

Hence, the small change in the predicted values in Table 13 are explained, and a simple formula for assessing any other proposed options on π_T adjustment is derived.

Returning to the temperature model, the second term in the brackets of equation (1) is $\frac{1}{298}$ and this is simply a standardization of 25°C which has no effect on model accuracy. It is possible that the premultiplier of 0.1 is in error; this could only be assessed by a regression analysis.

The first bracketed term is $1/(T_j + 273)$. Given that the ratio plot is of negative gradient, then the model gradient is too high.

Equation (1) gives $\pi_T = 0.1 \exp\left[-A\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)\right]$

Substituting $x = -A\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)$

$$\pi_T = 0.1e^x$$

Differentiating to find the slope expression, at x

$$\frac{d\pi_T}{dx} = 0.1e^x$$

Note that decreasing either the premultiplier or the exponent (or a combination) will have the desired effect on the slope.

(ii) T_j is estimated from the following expression:

$$T_j = T_C + \theta_{JC}P$$

where

T_C = case temperature

θ_{JC} = junction to case thermal resistance

P = worst case power dissipation

T_C is itself estimated directly from environment as below:

Environment	M_L	G_B	S_F	G_F	A_{IT}	G_M	N_S	AUT	N_V	A_{IF}	A_{UF}
$T_C(^oC)$	60	35	40	55	60	60	65	95	80	60	95

θ_{JC} is itself estimated directly from package type and number of pins.

Clearly any inaccuracy in T_j estimation would change the slope and position of the predicted model.

It is unlikely that such a strong temperature dependence as shown in the ratio plots would have been left in any model constructed by least squares regression analysis. For this reason it is suspected (though not proved) that the errors are due to the exponent in equation (1) rather than the premultiplier. Any such exponent error is most likely to be due to the method of junction temperature estimation, as shown earlier. The severity of inaccuracy in the model due to temperature and subsequent decisions as to adjustment of π_T values is considered later, for each technology separately.

Ratio Plots 7, 8, 9 & 10

3.3.9 Special Considerations. Some factors are not considered in the methods so far used, either because of a lack of data or because their effect is too small to be detectable.

(a) Programming Technique Factor π_{PT}. For many programming technologies, π_{PT} is 1.0 and the implication in such cases is that the mode of programming has no effect. There is not enough comparative data to check this value of π_{PT}. Although the same problem exists for all the data, where π_{PT} is not 1.0 it is possible to evaluate the effect on the overall failure rate. For some data on device 5300D, π_{PT} for NiCr programming is 1.08 and hence adds 4.3% to the prediction. For the C2708 EPROM the programming factor for UV eraseables is 1.56 and adds 53.4% to the prediction. The large difference is due to the possibility of accidental erasure and the relative newness of the technology. In view of the shortage of relevant comparative data it has to be concluded that there is no evidence to dispute the current π_{PT} factors. All that can be said is that π_{PT} appears to reflect the expected trends.

(b) Static/Dynamic RAMS. The data collected is limited, but a few data points allow direct comparison between static and dynamic RAMS. Parametric statistical tests are not valid on this amount of data with fourteen failure rate estimates, five for static and nine for dynamic. For both 1K data and 4K data, Wilcoxon's rank sum statistic shows that there is no signficant difference between static and dynamic failure rates. The complexity factors reflecting static and dynamic failure rate are so small as to be undetectable with the amounts of data available to this study. Therefore, no significant difference is expected. Although the actual numerical values of the static/dynamic factors cannot be verified, there is no evidence to reject their validity.

(c) PMOS and NMOS Technologies. Because of a worse than general lack of data, these two technologies are considered separately as follows. NMOS predictions are consistently pessimistic as shown in ratio plot 11. Part of this bias is certainly due to the majority of the parts being of D screen class, but this does not explain all the bias. It is quite possible that NMOS devices are not yet adequately modelled and this will be a function of complexity (consistently high in NMOS devices). A learning

curve in production may also be indicated to a greater degree than was modelled. Whatever the reasons, the data are inconclusive and a more reliable model is not possible without more data. To a lesser extent, the PMOS models are not yet adequate but here the bias is the other way (optimistic), and the bias is not so high as for NMOS nor is it so significant. Although special efforts were made, not enough data was available to evaluate the P-MNOS and MNOS models.

3.4 Model Evaluation. Since the model performance varies with technology, the model for each technology is considered in this section in the light of the inferences made so far.

The t - statistic for the mean $\log_{10}(\lambda_o/\lambda_p)$ is re-evaluated with π_Q adjusted to 19.5 for D-1 screen class data. Table 14 summarizes the results. The final column gives a set of possible decisions and evaluates their significance levels, α. These calculations are exact, and the earlier approximation method is not employed here. The goodness of fit is illustrated in ratio plot 11.

TABLE 14: TEST OF MODEL GOODNESS OF FIT BY TECHNOLOGY. π_Q ADJUSTED

	n	Mean $\log_{10}(\lambda_o/\lambda_p)$	s	t	Decision
CMOS	62	-0.022	0.413	-0.419	Accept
HTTL	23	0.183	0.420	2.090	Reject 5%
LSTTL	38	-0.100	0.319	-0.319	Reject 0.1%
STTL	31	0.152	0.451	1.874	Reject 10%
LTTL	46	0.210	0.422	3.370	Reject 0.2%
TTL	95	0.043	0.431	0.969	Accept
ECL	26	0.084	0.421	1.015	Accept
Linears	115	-0.053	0.376	-1.512	Reject 20%
PMOS	15	0.238	0.359	2.568	Reject 5%
P-MNOS	2	---	---	---	Accept
NMOS	18	-0.288	0.450	-2.700	Reject 2%
MNOS	1	---	---	---	Accept

For those technologies showing any significant overall departure from the perfect fit, by this test (significant being taken as $\alpha = 2\frac{1}{2}\%$) the results are summarized as follows:

LTTL	high bias and highly significant
LSTTL	high bias and highly significant
NMOS	high bias, significant

All others have insignificant, medium to low bias.

The LTTL bias is found to be temperature correlated, and there are other factors considered to be less influential as defined earlier in the report. The LSTTL with consistent high bias is found to be otherwise uncorrelated with the factors in the model. This could indicate an inaccurate model or simply a biased sample.

The overall error (and hence the t - statistic evaluated) may be sample dependent and this at least partially accounts for LTTL exhibiting high bias. LTTL data is all sampled between estimated junction temperatures of 30°C and 60°C. Because of the slope of the curve, a more fully represented temperature sample would exhibit considerably less bias. This was further illustrated in the sketch of Figure 13. Such sampling error should be standardized, or at least acknowledged, in any model adjustment.

If the temperature factor is in some way the major cause (and the evidence for this is strong) then a "reshuffle" of π_T tables for the technologies worst affected is not recommended, since the slope with respect to T_j would remain the same. The required π_T adjustments may be quickly estimated from equation (2), i.e.,

$$\pi_T^1 \simeq C\,(\pi_T + 1) - 1$$

although strictly a least squares analysis should be performed to optimize.

The penalties would be possible domino effects.

4. DISTRIBUTION OF TIME TO FAILURE

Information on the time at which each failure occurred is not often available. Most data is in the form of a certain number of failures in a certain time. Consequently the distribution of time to failure (TTF) is very difficult to assess. It should, however, be considered in any evaluation of MIL-HDBK-217C, since the models therein assume an exponential distribution by virtue of the constant failure rate assumption.

The only way to tackle this problem is to set up some null hypothesis and review it in the light of the data. Hence, we set up the null hypothesis that the data is exponential (against the alternative that it is not).

Under the null hypothesis, the TTF distribution is $f(t) = \lambda e^{-\lambda t}$

where

λ = the failure rate

t = time in part hours

therefore the distribution of time to r^{th} failure is straightforward to derive and is given by

$$g(t) = \frac{e^{-\lambda t} \lambda^r t^{r-1}}{\Gamma r}$$

where Γr represents the gamma function.

Since r itself has a distribution, the distribution of the type of data used in this study (see Appendix A) is given by a joint density function involving t and r. The largest group of data (TTL, GBC, D-1) was evaluated using a Monte Carlo simulation. The program simulated the joint density function and gave a Kolmogorov-Smirnov (K-S) statistic for the data, under the null hypothesis.

For the TTL, GBC, D-1 data, the K-S statistic with 30 degrees of freedom was found to be 0·15, which is found to be not significant. Hence it is concluded that the exponential assumption is not rejected by the data available. A fuller description of the simulation and statistical theory is given in Ref 5.

5. DATA SHORTCOMINGS

A major problem in constructing statistical models is always the lack of adequate data. The military data collection system can readily supply maintenance data in large quantities, but obtaining such data for a particular equipment or component over a large period of time (typically, in excess of eighteen months) is difficult. In addition, in many cases the data does not reflect the quantity of parts replaced on printed circuit boards, neither does it identify those parts. Hence, more depot maintenance data would be invaluable (as opposed to line and shop maintenance data). Another serious shortcoming is the lack of recorded operating time. Maintenance personnel are given provision on the appropriate forms to record operating time but are not required to fill them in (by directive). Thus, operating times have to be derived by tracing the using commands. Recent changes to the Navy system augur well for future work.

6. SUMMARY

The factors influencing the goodness of fit of MIL-HDBK-217C prediction models are assessed. Although it is not possible to scientifically separate causal factors in every case, areas in which the

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6. SUMMARY

The factors influencing the goodness of fit of MIL-HDBK-217C prediction models are assessed. Although it is not possible to scientifically separate causal factors in every case, areas in which the

models are deficient are identified and quantified. Possible causes are reviewed and the most likely causal factors identified. Where positive inferences are possible, a range of statistical methods are used to give an unbiased assessment. The underlying distribution of time to failure is investigated since MIL-HDBK-217C assumes a constant failure rate model, and this, if not vindicated, could induce considerable error into the predicted failure rate. Results suggest that no great error will accrue from such an assumption although it is not always strictly valid.

The statistical methods developed for this study may be used for future model evaluation whenever an unbiased assessment is required. The correlation matrix/ratio plot method may be used iteratively to construct an optimal model but least squares regression analysis is preferred. The ratio plot method allows empirical confidence intervals on predicted failure rates to be readily evaluated.

7. RECOMMENDATIONS AND CONCLUSIONS

The degree of acceptable error in MIL-HDBK-217C models has to be defined. Once this is done, the areas for improvement are discussed in this report. Depending on the accuracy required, the outstanding areas of poor model performance as identified by this study are:

(a) π_Q for D-1 screen class. Note that this could well be due to the particular sample taken and inspection confirmed that the components had undergone in-house screening. Additional information probably in the form of more data from diverse sources is desirable. At the time of writing it is understood that MIL-HDBK-217D will allow the use of a D factor for plastic encapsulated devices which undergo burn-in and temperature cycling and a high temperature continuity test.

(b) π_Q for D screen class. The perfect fit would be realized by a π_Q of about 20 which is not drastically different from the current value of 17.5.

(c) π_T for CMOS, LTTL, TTL and linear device technology is found to be correlated with poor model fit although only LTTL shows significant bias. For LTTL the bias is large but partially sample dependent. This dependency of model performance on π_T is most probably due to the method of estimating junction temperature although other contributing factors are not ruled out (as discussed in the main report).

(d) LSTTL and NMOS models. The poor fit observed in these technologies is not apparently correlated with any particular factor or factors. For NMOS there is clearly not enough data to adequately define a model, although what data there is statistically rejects the current model. For LSTTL the model is very poor; there is a possibility that this is due to the sample collected but there is no evidence to support such a possibility.

The microelectronic device section in MIL-HDBK-217C is divided into the following broad categories and it would be as well to summarize the conclusions in that format also.

(i) Monolithic Bipolar & MOS Digital (SSI/MSI). The performance of this model is illustrated in ratio plot #12. Overall there is very little bias although some complexity dependence is indicated with $\log_{10}(\lambda_o/\lambda_p)$ decreasing as complexity increases up to about 70 gates.

(ii) Monolithic Bipolar and MOS Linear Devices. The overall performance is satisfactory but again there is some complexity dependence, as illustrated by ratio plot #4.

(iii) Monolithic Bipolar and MOS Random Logic LSI and Microprocessor Devices. There is less data available to validate this model but the results do show negligible bias with ten points above and ten points below the line of perfect fit. The data are plotted in ratio plot #13.

(iv) Random Access Memories (RAMs). Again, a clear complexity dependence is illustrated (ratio plot #14). More specifically it would appear that 4K RAMs are not adequately modelled.

(v) Read-Only Memories (ROMs) and Programmable Read-Only Memories (PROMs). Ratio plot #15 shows that there is not enough data to properly evaluate the ROM and PROM model.

It may be desirable to construct confidence intervals on a prediction based on MIL-HDBK-217C. At the component level this can be appreciated by looking at the relevant ratio plot and observing the scatter. Numerically, it is possible to estimate the variance in the data since it is normally distributed about the line of perfect fit. This then allows a confidence interval on the mean to be set up in the usual way and a simple transformation will allow an interval on the predicted failure rate. An exact method for calculating confidence intervals has not been devised but may be the subject of future work.

At the system level, clearly the central limit theorem will dictate that confidence in predictions increases with the number of components in the system. Again this has not been evaluated but may be the subject of future work.

The most widely voiced criticisms of MIL-HDBK-217C appear to be in connection with its ever-increasing complexity and with errors of estimation in MTBF's, logistics requirements, etc. These two complaints are approximately equal and opposite but do not cancel out. However, both are quite valid and as such the following points are emphasized.

The prediction models provide an accurate means of assessing relative failure rates. These are of prime use in reviewing options and costing trade-offs. If absolute failure rate (or MTBF) is required, then other

factors should be taken into account; in particular, the variability in the data should be included in the prediction. The most popular of the available means of expressing the variability in a parameter estimate is some form of confidence interval. These may be constructed either from an assumed distribution or the data directly. Estimation from distribution theory is not entirely satisfactory in view of the variability found in this study. It is recommended that future editions of MIL-HDBK-217C should include some form of confidence interval estimation procedure, based on the data.

When the prediction model is found to be too complex then MIL-HDBK-217C, Part III is included as an alternative. This method is of course not as accurate. It is probably true that statistical theory would not fit as many parameters as are fitted in MIL-HDBK-217C, nor would it regress on a set of variables which are themselves correlated (in practice, some dependence is inevitable). However, where two such variables (e.g., junction temperature and application environment) are found to both have significant effects there is really little option given the user needs. Additionally a priori knowledge on influential factors was available. It could be worthwhile to investigate a simpler model and compare its accuracy with MIL-HDBK-217C Part II and Part III models.

Clearly the major problem, as with many statistical models, is a lack of adequate data. Many industries and manufacturers are unable or reluctant to provide reliability data. Government agencies and the military, while co-operating with data collection efforts, are often hampered by inadequacies of the current maintenance data collection system or lack of clear directive with respect to reliability data.

Although there are many problems in adequate estimation of reliability, the results of this study provide a clear analysis of the performance of the predictive models of MIL-HDBK-217C. The models generally stand up well to recent data in the categories for which data is available.

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APPENDIX A

TABULATED DATA ENTRIES

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
1	CMOS	1	PDIP	14	D-1	GBC	42	1.242	1	0.18	0.81	2.41	0.24
2	HTTL	1	HDIP	14	D	GB	27	14.925	0	—	—	0.11	0.09
3	LSTTL	1	PDIP	14	D-1	GBC	41	66.603	4	0.03	0.06	0.08	0.19
4	STTL	1	HDIP	16	D-1/JD	GF	27	1.458	1	0.15	0.69	2.05	0.05
5	STTL	1	PDIP	16	D-1	GBC	43	27.674	7	0.17	0.25	0.37	0.19
6	TTL	1	HFPK	14	C-1	AUF	71	5.906	0	—	—	0.27	0.41
7	TTL	1	PDIP	14	D-1	GBC	41	137.729	28	0.17	0.20	0.24	0.19
8	CMOS	2	PDIP	14	D-1	GBC	41	27.423	5	0.11	0.18	0.29	0.25
9	ECL	2	HDIP	16	D	GBC	55	11.766	2	0.07	0.17	0.36	0.12
10	ECL	2	PDIP	14	D-1	GBC	50	49.404	25	0.42	0.51	0.61	0.21
11	ECL	2	PDIP	16	D-1	GBC	50	90.978	20	0.18	0.22	0.27	0.24
12	HTTL	2	HFPK	14	C-1	AUF	77	15.947	4	0.14	0.25	0.42	0.43
13	HTTL	2	HDIP	14	D	GB	30	24.365	3	0.06	0.12	0.23	0.09
14	HTTL	2	HDIP	14	D	GB	35	16.931	1	0.01	0.06	0.18	0.09
15	LSTTL	2	PDIP	14	D-1	GBC	41	143.641	5	0.02	0.03	0.06	0.20
16	LTTL	2	HDIP	14	D	AIT	56	3.062	1	0.07	0.33	1.00	0.32
17	LTTL	2	PDIP	14	D-1	GBC	41	39.688	15	0.29	0.38	0.48	0.20

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^4)	No. Failures	20% C.L.	Pt. Est	80% C.L.	Predicted
18	STTL	2	HDIP	14	B-1/-1B	GF	35	12.438	0	—	—	0.13	0.04
19	STTL	2	PDIP	14	D-1	GBC	48	65.698	4	0.03	0.06	0.10	0.21
20	TTL	2	HDIP	14	B-1/-1B	CF	30	6.999	0	—	—	0.25	0.04
21	TTL	2	HFPK	14	C-1	AUF	73	6.393	4	0.36	0.63	1.25	0.43
22	TTL	2	PDIP	14	D-1	GBC	44	221.918	50	0.20	0.23	0.26	0.20
23	TTL	2	PDIP	16	D-1	GBC	45	89.464	24	0.23	0.27	0.33	0.24
24	CMOS	3	HDIP	14	D	GBC	41	23.023	5	0.13	0.22	0.34	0.12
25	CMOS	3	HDIP	14	D	GF	41	9.120	6	0.43	0.66	1.00	0.25
26	CMOS	3	PDIP	14	D-1	GBC	42	166.874	40	0.21	0.24	0.28	0.27
27	ECL	3	HDIP	16	D	GBC	63	1.531	2	0.54	1.31	2.79	0.13
28	ECL	3	PDIP	16	D-1	GBC	49	67.620	9	0.10	0.13	0.19	0.25
29	HTTL	3	HFPK	14	C-1	AUF	79	2.407	2	0.34	0.83	1.78	0.44
30	HTTL	3	HDIP	14	D	GB	30	12.409	3	0.12	0.24	0.44	0.09
31	HTTL	3	HDIP	14	D	GB	37	17.993	2	0.05	0.11	0.24	0.10
32	HTTL	3	PDIP	14	D-1	GBC	43	22.065	2	0.04	0.09	0.19	0.26
33	HTTL	3	PDIP	14	D-1	GBC	50	66.354	4	0.03	0.06	0.10	0.21
34	LSTTL	3	PDIP	14	D-1	GBC	41	311.089	24	0.06	0.08	0.09	0.21

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										observed			predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	
35	LTTL	3	HDIP	14	D	AIT	56	6.346	1	0.04	0.16	0.47	0.33
36	LTTL	3	PDIP	14	D-1	GBC	41	135.151	72	0.48	0.53	0.59	0.20
37	STTL	3	PDIP	14	D-1	GBC	48	155.281	26	0.14	0.17	0.20	0.21
38	TTL	3	HFPK	14	B-1	AUF	74	4.100	0	—	—	0.39	0.10
39	TTL	3	HFPK	14	C-1	AUF	74	10.082	1	0.02	0.10	0.30	0.43
40	TTL	3	PDIP	14	D-1	GBC	34	60.819	13	0.16	0.21	0.28	0.20
41	TTL	3	PDIP	14	D-1	GBC	44	137.680	32	0.20	0.23	0.27	0.21
42	CMOS	4	HDIP	14	D	GBC	42	126.220	17	0.11	0.13	0.17	0.12
43	CMOS	4	HDIP	14	D	GF	41	54.000	6	0.07	0.11	0.17	0.25
44	CMOS	4	PDIP	14	D-1	GBC	42	576.966	146	0.24	0.25	0.27	0.28
45	ECL	4	HDIP	16	D	GBC	51	49.598	4	0.05	0.08	0.14	0.12
46	ECL	4	HDIP	16	D	GBC	65	20.534	5	0.15	0.24	0.39	0.13
47	ECL	4	PDIP	16	D-1	GBC	50	387.472	49	0.11	0.13	0.14	0.25
48	ECL	4	PDIP	14	D-1	GBC	54	7.312	1	0.03	0.14	0.41	0.23
49	HTTL	4	HFPK	14	C-1	AUF	81	4.851	5	0.64	1.03	1.63	0.46
50	HTTL	4	HDIP	14	D	GB	35	21.928	1	0.01	0.05	0.14	0.10
51	HTTL	4	PDIP	14	D-1	GBC	52	76.173	26	0.28	0.34	0.41	0.22

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_A (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	
52	LSTTL	4	PDIP	14	D-1	GBC	43	1151.673	275	0.13	0.14	0.15	0.22
53	LTTL	4	HDIP	14	D	AIT	57	15,390	1	0.01	0.06	0.19	0.34
54	LTTL	4	PDIP	14	D-1	GBC	31	101.746	80	0.71	0.79	0.87	0.20
55	LTTL	4	PDIP	14	D-1	GBC	41	674.339	187	0.24	0.28	0.30	0.21
56	STTL	4	PDIP	14	D-1	GBC	35	57.144	2	0.01	0.03	0.07	0.21
57	STTL	4	PDIP	14	D-1	GBC	54	355.333	31	0.07	0.09	0.10	0.23
58	STTL	4	PDIP	14	D-1	GBC	68	18.330	2	0.04	0.11	0.23	0.27
59	TTL	4	HDIP	14	B-1/1D	GF	31	22.320	1	0.01	0.04	0.13	0.04
60	TTL	4	HFPK	14	B-1	AUF	75	11.248	0	—	—	0.14	0.10
61	TTL	4	HFPK	14	C-1	AUF	75	25.388	8	0.22	0.32	0.45	0.45
62	TTL	4	HDIP	14	B-2/None	AUF	75	2.212	3	0.69	1.36	2.49	0.76
63	TTL	4	HDIP	14	D	GBC	30	9.498	1	0.02	0.11	0.32	0.10
64	TTL	4	PDIP	14	D-1	GBC	35	10.175	9	0.63	0.88	1.23	0.21
65	TTL	4	PDIP	14	D-1	GBC	43	1855.757	323	0.16	0.17	0.18	0.21
66	TTL	4	PDIP	14	D-1	GBC	50	565.891	122	0.20	0.22	0.23	0.22
67	TTL	4	PDIP	16	D-1	GBC	52	135.291	40	0.26	0.30	0.34	0.26
68	TTL	4	HDIP	14	D-1	GBC	57	139.714	31	0.19	0.22	0.26	0.23

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	Predicted
69	HTTL	5	HDIP	14	D	GB	35	7.856	10	0.93	1.27	1.74	0.10
70	HTTL	5	PDIP	14	D-1	GBC	45	30.196	16	0.42	0.53	0.67	0.22
71	LSTTL	5	PDIP	14	D-1	GBC	41	42.194	2	0.02	0.05	0.10	0.22
72	LTTL	5	PDIP	14	D-1	GBC	41	17.700	2	0.05	0.11	0.24	0.21
73	STTL	5	PDIP	14	D-1	GBC	44	309.437	63	0.18	0.20	0.23	0.22
74	TTL	5	PDIP	14	D-1	GBC	43	48.754	5	0.06	0.10	0.16	0.21
75	CMOS	6	HDIP	14	D	GF	41	19.941	15	0.59	0.75	0.96	0.26
76	CMOS	6	HDIP	14	D	GBC	42	13.990	1	0.02	0.07	0.21	0.12
77	CMOS	6	HDIP	16	D	GBC	42	36.285	21	0.47	0.58	0.71	0.14
78	CMOS	6	PDIP	14	D-1	GBC	42	19.701	12	0.46	0.61	0.81	0.29
79	CMOS	6	PDIP	16	D-1	GBC	42	271.691	39	0.12	0.14	0.17	0.32
80	ECL	6	PDIP	14	D-1	GBC	65	8.340	7	0.57	0.84	1.23	0.26
81	HTTL	6	HFPK	14	C-1	AUF	58	5.754	3	0.27	0.52	0.96	0.48
82	HTTL	6	HDIP	14	D	GB	39	26.400	7	0.18	0.27	0.39	0.10
83	HTTL	6	PDIP	14	D-1	GBC	50	48.450	21	0.35	0.43	0.53	0.23
84	LSTTL	6	PDIP	14	D-1	GBC	44	856.421	151	0.16	0.18	0.19	0.22
85	LTTL	6	HFPK	14	D	AIT	56	10.906	0	—	—	0.15	0.34

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_j (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	
86	LTTL	6	PDIP	14	D-1	GBC	31	10.175	8	0.55	0.79	1.12	0.21
87	LTTL	6	PDIP	14	D-1	GFC	41	242.034	67	0.25	0.28	0.31	0.22
88	STTL	6	PDIP	14	D-1	GBC	60	183.449	37	0.17	0.20	0.23	0.23
89	STTL	6	HDIP	14	B-1/JB	GF	36	7.632	0	—	—	0.21	0.04
90	TTL	6	HFPK	14	JB	AUF	78	2.557	1	0.09	0.39	1.17	0.04
91	TTL	6	HDIP	14	B-1/JB	GF	31	11.734	2	0.07	0.17	0.36	0.04
92	TTL	6	HDIP	14	B-1	AUF	75	4.138	1	0.05	0.24	0.72	0.13
93	TTL	6	HFPK	14	C-1	AUF	75	21.068	1	0.01	0.05	0.14	0.46
94	TTL	6	HDIP	14	D	GBC	31	17.481	2	0.05	0.11	0.24	0.10
95	TTL	6	PDIP	14	D-1	GBC	45	783.401	142	0.17	0.18	0.20	0.22
96	TTL	6	PDIP	14	D-1	GBC	57	300.909	84	0.25	0.28	0.31	0.24
97	ECL	7	HDIP	16	D	GBC	63	4.547	1	0.05	0.22	0.66	0.14
98	TTL	7	HDIP	16	B-1/JB	GF	54	10.998	0	—	—	0.15	0.05
99	TTL	7	PDIP	16	D-1	GBC	70	14.835	5	0.21	0.34	0.53	0.32
100	CMOS	8	HDIP	16	D	GBC	41	25.565	1	0.01	0.04	0.12	0.14
101	CMOS	8	PDIP	16	D-1	GBC	42	14.445	3	0.11	0.21	0.38	0.34
102	HTTL	8	PDIP	14	D-1	GBC	49	3.586	2	0.21	0.51	1.10	0.23

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
103	LSTTL	8	PDIP	16	D-1	GBC	42	20.797	3	0.07	0.14	0.27	0.26
104	LTTL	8	PDIP	14	D-1	GBC	35	10.173	5	0.30	0.49	0.78	0.22
105	LTTL	8	PDIP	14	D-1	GBC	43	19.731	11	0.41	0.56	0.75	0.23
106	TTL	8	NDIP	14	B-1/-1B	GF	35	19.080	0	—	—	0.08	0.04
107	TTL	8	HFPK	14	C-1	AUF	76	1.201	4	1.91	3.33	5.66	0.47
108	TTL	8	HFPK	14	C-1	AUF	83	1.092	3	1.41	2.75	6.05	0.49
109	TTL	8	PDIP	14	D-1	GBC	49	71.994	25	0.29	0.35	0.42	0.23
110	TTL	8	PDIP	16	D-1	GBC	50	62.865	11	0.13	0.17	0.24	0.27
111	TTL	8	PDIP	16	D-1	GBC	70	22.329	2	0.04	0.09	0.19	0.33
112	ECL	10	PDIP	14	D-1	GBC	53	109.792	17	0.12	0.15	0.20	0.25
113	ECL	10	PDIP	14	D-1	GBC	65	34.804	9	0.18	0.26	0.36	0.29
114	HTTL	10	PDIP	14	D-1	GBC	50	25.870	1	0.01	0.04	0.12	0.24
115	LSTTL	10	PDIP	14	D-1	GBC	44	23.980	12	0.38	0.50	0.66	0.24
116	LSTTL	10	PDIP	20	D-1	GBC	46	43.711	3	0.04	0.07	0.13	0.35
117	LTTL	10	PDIP	14	D-1	GBC	46	11.603	1	0.02	0.09	0.26	0.24
118	STTL	10	PDIP	14	D-1	GBC	50	2.579	2	0.32	0.78	1.66	0.25
119	TTL	10	HFPK	14	D-1	GBC	53	24.736	6	0.16	0.25	0.37	0.25

Device Description					Application Description					Failure Rates (F./10^6 H.rs)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_A (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	
120	TTL	11	PDIP	14	D-1	GFC	47	28.141	3	0.05	0.11	0.20	0.24
121	CMOS	12	PDIP	14	D-1	GFC	43	15.341	2	0.05	0.13	0.27	0.53
122	ECL	12	HDIP	16	D	GFC	67	14.663	7	0.32	0.48	0.70	0.16
123	HTTL	12	HDIP	14	D	GB	45	11.700	0	—	—	0.14	0.11
124	HTTL	12	PDIP	14	D-1	GBC	60	16.635	1	0.01	0.06	0.18	0.28
125	LSTTL	12	PDIP	14	D-1	GBC	42	636.315	83	0.12	0.13	0.14	0.24
126	LTTL	12	HDIP	14	D	AUT	56	13.186	1	0.02	0.08	0.23	0.36
127	LTTL	12	PDIP	14	D-1	GBC	31	30.524	38	1.07	1.24	1.45	0.22
128	LTTL	12	PDIP	14	D-1	GEC	42	304.831	134	0.40	0.44	0.47	0.24
129	STTL	12	HDIP	14	B-1/ +B	GF	35	6.066	0	—	—	0.27	0.04
130	STTL	12	PDIP	14	D-1	GBC	57	259.698	50	0.17	0.19	0.22	0.28
131	TTL	12	HDIP	14	B-1/ +B	GF	34	5.922	0	—	—	0.27	0.04
132	TTL	12	HFPK	14	C-1	AUF	81	2.971	1	0.08	0.34	1.01	0.50
133	TTL	12	PDIP	14	D-1	GBC	35	2.617	2	0.32	0.76	1.64	0.22
134	TTL	12	PDIP	14	D-1	GBC	50	485.628	142	0.27	0.29	0.32	0.25
135	CMOS	14	PDIP	14	D-1	GBC	43	4.371	2	0.18	0.44	0.94	0.34
136	ECL	14	PDIP	16	D-1	GBC	65	256.910	37	0.13	0.15	0.18	0.35

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
137	HTTL	14	PDIP	14	D-1	GBC	68	5.603	1	0.04	0.18	0.53	0.33
138	LTTL	14	HDIP	16	D	AIT	58	6.118	0	—	—	0.26	0.44
139	LTTL	14	PDIP	14	D-1	GBC	42	55.430	15	0.21	0.27	0.35	0.24
140	LTTL	14	PDIP	16	D-1	GBC	52	45.345	17	0.29	0.37	0.47	0.31
141	STTL	14	PDIP	16	D-1	GBC	64	10.946	3	0.14	0.27	0.50	0.38
142	TTL	14	PDIP	16	D-1	GBC	57	97.144	5	0.03	0.05	0.08	0.28
143	LSTTL	15	PDIP	16	D-1	GBC	45	352.341	35	0.08	0.10	0.12	0.29
144	LTTL	15	PDIP	14	D-1	GBC	44	24.274	3	0.06	0.12	0.23	0.25
145	STTL	15	PDIP	16	D-1	GBC	60	6.551	2	0.13	0.31	0.65	0.35
146	TTL	15	HFPK	16	C-1	AUF	81	0.903	1	0.25	1.11	3.32	0.62
147	TTL	15	PDIP	14	D-1	GBC	57	145.297	55	0.34	0.38	0.43	0.29
148	ECL	16	PDIP	14	D-1	GBC	54	19.122	5	0.16	0.26	0.41	0.28
149	ECL	16	PDIP	16	D-1	GBC	59	27.628	8	0.20	0.29	0.39	0.33
150	HTTL	16	HDIP	16	D	GB	43	6.608	5	0.47	0.76	1.20	0.13
151	HTTL	16	PDIP	14	D-1	GBC	51	22.487	3	0.07	0.13	0.25	0.27
152	HTTL	16	PDIP	16	D-1	GBC	60	19.595	13	0.51	0.66	0.87	0.34
153	LSTTL	16	PDIP	16	D-1	GBC	45	453.217	83	0.17	0.18	0.20	0.30

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_J (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	
154	LTTL	16	HDIP	16	D-1	GBC	44	76.007	5	0.04	0.07	0.10	0.29
155	STTL	16	HDIP	16	B-1/1D	GF	45	4.662	0	—	—	0.35	0.05
156	STTL	16	HDIP	16	D	GBC	54	54.852	8	0.10	0.15	0.21	0.13
157	STTL	16	PDIP	16	D-1	GBC	54	217.578	74	0.31	0.34	0.38	0.29
158	STTL	16	PDIP	16	D-1	GBC	65	20.770	3	0.07	0.14	0.27	0.40
159	TTL	16	HDIP	16	B-1/1B	GF	41	10.098	0	—	—	0.16	0.05
160	TTL	16	HFPK	14	C-1	AUF	79	5.340	1	0.04	0.19	0.56	0.51
161	TTL	16	HDIP	16	B-2/None	AUF	79	0.937	1	0.24	1.07	3.20	1.03
162	TTL	16	PDIP	16	D-1	GBC	50	176.415	43	0.21	0.24	0.28	0.26
163	TTL	16	PDIP	16	D-1	GBC	55	53.173	7	0.09	0.13	0.19	0.32
164	LSTTL	17	PDIP	16	D-1	GBC	43	82.472	13	0.12	0.16	0.21	0.29
165	LTTL	17	PDIP	16	D-1	GBC	45	90.687	37	0.35	0.41	0.48	0.29
166	STTL	17	PDIP	16	D-1	GBC	52	2.548	1	0.09	0.39	1.18	0.32
167	TTL	17	HFPK	16	C-1	AUF	85	11.423	2	0.07	0.17	0.37	0.64
168	TTL	17	PDIP	16	D-1	GBC	54	53.468	15	0.22	0.28	0.36	0.32
169	CMOS	18	HDIP	16	D	GBC	43	4.369	1	0.05	0.23	0.69	0.16
170	CMOS	18	PDIP	18	D-1	GBC	43	14.677	1	0.02	0.07	0.20	0.39

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	
171	LSTTL	18	PDIP	16	D-1	GBC	44	64.817	8	0.09	0.12	0.18	0.30
172	LTTL	18	PDIP	16	D-1	GBC	45	42.489	5	0.07	0.12	0.19	0.29
173	STTL	18	PDIP	16	D-1	GBC	70	4.982	1	0.04	0.20	0.60	0.46
174	TTL	18	HFPK	16	C-1	AUF	87	11.730	5	0.26	0.43	0.67	0.65
175	TTL	18	PDIP	16	D-1	GBC	54	123.301	40	0.28	0.32	0.38	0.32
176	TTL	18	PDIP	16	D-1	GBC	60	36.590	24	0.23	0.28	0.34	0.34
177	CMOS	19	PDIP	16	D-1	GBC	42	21.765	4	0.08	0.13	0.23	0.37
178	LSTTL	19	PDIP	14	D-1	GBC	44	51.088	17	0.17	0.21	0.26	0.26
179	LTTL	19	PDIP	16	D-1	GBC	45	87.121	26	0.25	0.30	0.36	0.30
180	TTL	19	HDIP	16	B-1/J-B	GF	39	5.091	0	—	—	0.32	0.05
181	TTL	19	PDIP	16	D-1	GBC	55	92.716	9	0.07	0.10	0.14	0.33
182	CMOS	20	HDIP	16	B	GF	42	1.249	3	1.23	2.40	4.42	0.33
183	CMOS	20	PDIP	16	D-1	GBC	42	8.531	2	0.09	0.23	0.48	0.38
184	LSTTL	20	PDIP	16	D-1	GBC	46	106.403	24	0.19	0.23	0.27	0.31
185	LTTL	20	PDIP	16	D-1	GBC	41	10.175	5	0.30	0.49	0.78	0.29
186	LTTL	20	PLP	16	D-1	GBC	51	7.558	1	0.03	0.13	0.40	0.33
187	TTL	20	PLP	14	D-1	GBC	64	80.098	19	0.19	0.24	0.30	0.34

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
188	TTL	21	HFPK	14	C-1	AUF	92	5.154	1	0.04	0.19	0.58	0.58
189	CMOS	23	HDIP	16	D	GF	47	3.180	3	0.48	0.94	1.73	0.35
190	CMOS	23	PDIP	16	D-1	GBC	43	16.418	8	0.34	0.49	0.69	0.40
191	CMOS	24	HDIP	14	D	GBC	49	29.309	10	0.25	0.34	0.47	0.17
192	CMOS	24	PDIP	14	D-1	GBC	49	234.731	64	0.24	0.27	0.31	0.52
193	ECL	24	HDIP	16	D	GBC	65	105.160	4	0.02	0.04	0.06	0.18
194	LSTTL	24	PDIP	14	D-1	GBC	43	141.001	9	0.05	0.06	0.09	0.27
195	LSTTL	24	PDIP	16	D-1	GBC	45	242.151	20	0.07	0.08	0.10	0.32
196	LTTL	24	PDIP	16	D-1	GBC	55	137.162	28	0.17	0.20	0.24	0.36
197	STTL	24	HDIP	16	B-1/-1B	GF	52	4.030	0	—	—	0.40	0.06
198	TTL	24	HDIP	16	B-1/-1B	GF	39	7.236	0	—	—	0.22	0.05
199	TTL	24	PDIP	16	D-1	GBC	54	234.120	43	0.16	0.18	0.21	0.34
200	LSTTL	25	PDIP	14	D-1	GBC	45	64.272	11	0.13	0.17	0.23	0.28
201	LTTL	25	HDIP	24	D	AIT	60	3.040	1	0.07	0.33	0.99	0.78
202	LTTL	25	PDIP	14	D-1	GBC	42	19.181	8	0.29	0.42	0.59	0.27
203	LTTL	25	PDIP	16	D-1	GBC	45	17.937	6	0.20	0.33	0.51	0.31
204	TTL	25	PDIP	14	D-1	GBC	56	96.636	12	0.09	0.12	0.16	0.32

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	N. Est	80% C.L.	Predicted
205	CMOS	26	NDIP	16	D	GBC	42	7.386	1	0.03	0.14	0.41	0.16
206	CMOS	26	PDIP	16	D-1	GBC	42	5.847	1	0.04	0.17	0.51	0.39
207	LSTTL	26	PDIP	14	D-1	GBC	45	27.498	2	0.03	0.07	0.15	0.29
208	TTL	26	PDIP	14	D-1	GBC	54	88.306	22	0.20	0.25	0.30	0.31
209	LTTL	27	PDIP	16	D-1	GBC	45	83.131	26	0.26	0.31	0.38	0.32
210	ECL	28	NDIP	16	D	GBC	63	1.184	1	0.19	0.84	2.53	0.18
211	CMOS	29	PDIP	16	D-1	GBC	43	3.708	1	0.06	0.27	0.81	0.42
212	TTL	29	PDIP	16	D-1	GBC	57	2.189	1	0.10	0.46	1.37	0.37
213	CMOS	30	NDIP	16	D	GF	50	10.200	2	0.08	0.20	0.42	0.38
214	CMOS	30	PDIP	16	D-1	GBC	42	62.657	8	0.07	0.13	0.18	0.40
215	CMOS	30	NDIP	16	D	GBC	50	4.966	1	0.04	0.20	0.60	0.20
216	LTTL	30	PDIP	16	D-1	GBC	45	46.438	6	0.08	0.13	0.20	0.32
217	CMOS	31	NDIP	16	D	GF	42	7.085	3	0.22	0.42	0.78	0.34
218	CMOS	31	PDIP	16	D-1	GBC	41	56.364	11	0.14	0.20	0.26	0.39
219	CMOS	31	PDIP	14	D-1	GBC	65	81.744	7	0.06	0.09	0.13	1.83
220	CMOS	32	NDIP	16	D	GF	45	3.754	2	0.22	0.53	1.14	0.35
221	CMOS	32	PDIP	16	D-1	GBC	42	57.470	14	0.19	0.24	0.32	0.41

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										observed			predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	
222	TTL	32	PDIP	16	D-1	GBC	60	29.033	3	0.05	0.10	0.19	0.40
223	LTTL	33	PDIP	16	D-1	GBC	43	10.532	1	0.02	0.09	0.28	0.32
224	TTL	34	PDIP	14	D-1	GBC	65	12.833	7	0.37	0.55	0.80	0.41
225	CMOS	35	HDIP	16	D	GBC	41	5.704	2	0.14	0.35	0.75	0.16
226	CMOS	35	PDIP	16	D-1	GBC	41	28.120	6	0.14	0.21	0.32	0.16
227	TTL	35	PDIP	16	D-1	GBC	57	29.019	26	0.75	0.90	1.08	0.39
228	CMOS	36	HDIP	16	D	GF	41	29.315	3	0.05	0.10	0.19	0.33
229	LSTTL	36	PDIP	14	D-1	GBC	48	737.154	112	0.14	0.15	0.17	0.34
230	LTTL	36	PDIP	14	D-1	GBC	50	31.120	12	0.29	0.39	0.51	0.33
231	STTL	36	HDIP	16	B-1/ -B	GF	66	9.552	0	—	—	0.17	0.06
232	STTL	36	PDIP	16	D-1	GBC	70	1.144	2	0.72	1.75	3.74	0.60
233	TTL	36	HDIP	16	B-1/ -B	GF	61	26.370	0	—	—	0.06	0.06
234	TTL	37	PDIP	14	D-1	GBC	60	60.305	14	0.18	0.23	0.30	0.38
235	TTL	37	PDIP	16	D-1	GBC	60	112.814	40	0.36	0.41	0.47	0.41
236	CMOS	37	PDIP	16	D-1	GBC	58	10.458	3	0.15	0.29	0.53	1.14
237	LTTL	37	HDIP	14	D	AET	57	5.165	0	—	—	0.31	0.42
238	LTTL	37	PDIP	14	D-1	GBC	43	14.209	2	0.06	0.14	0.29	0.29

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_A (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
239	TTL	37	PDIP	14	D-1	GBC	60	19.989	3	0.08	0.15	0.28	0.38
240	LTTL	38	PDIP	16	D-1	GBC	48	171.067	11	0.17	0.23	0.31	0.36
241	CMOS	39	HDIP	16	D	GBC	42	10.817	1	0.02	0.09	0.28	0.17
242	LSTTL	39	PDIP	14	D-1	GBC	49	77.037	15	0.15	0.19	0.25	0.35
243	STTL	39	PDIP	14	D-1	GBC	98	3.672	1	0.06	0.27	0.92	0.75
244	TTL	39	PDIP	14	D-1	GBC	65	127.560	36	0.24	0.28	0.33	0.43
245	TTL	39	PDIP	16	D-1	GBC	65	28.958	19	0.53	0.66	0.82	0.47
246	LTTL	40	PDIP	16	D-1	GBC	48	60.164	4	0.04	0.07	0.11	0.36
247	TTL	40	HFPK	16	C-1	AUF	106	7.561	1	0.03	0.13	0.40	0.87
248	LSTTL	41	PDIP	16	D-1	GBC	47	43.082	4	0.05	0.09	0.16	0.37
249	ECL	42	PDIP	16	D-1	GBC	87	40.401	3	0.04	0.07	0.14	0.85
250	TTL	43	PDIP	14	D-1	GBC	61	6.240	1	0.04	0.16	0.48	0.41
251	CMOS	44	PDIP	14	D-1	GBC	66	10.144	5	0.30	0.49	0.78	1.36
252	STTL	44	PDIP	14	D-1	GBC	76	21.215	15	0.55	0.71	0.91	0.74
253	TTL	44	PDIP	14	D-1	GBC	48	6.642	2	0.12	0.30	0.64	0.32
254	TTL	44	FLAT	14	D-1	GBC	60	57.721	8	0.10	0.14	0.20	0.41
255	CMOS	45	PDIP	16	D-1	GBC	58	22.266	4	0.10	0.18	0.30	1.21

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	
256	CMOS	45	HDIP	16	D	GBC	60	27.431	4	0.08	0.15	0.25	0.32
257	LSTTL	45	PDIP	16	D-1	GBC	45	18.000	1	0.01	0.06	0.17	0.39
258	LTTL	45	PDIP	16	D-1	GBC	45	40.131	23	0.47	0.57	0.70	0.35
259	TTL	45	PDIP	16	D-1	GBC	65	41.074	4	0.06	0.10	0.16	0.49
260	CMOS	46	PDIP	16	D-1	GBC	50	10.166	2	0.08	0.20	0.42	0.68
261	CMOS	47	PDIP	16	D-1	GBC	47	13.107	2	0.06	0.15	0.33	0.57
262	STTL	47	PDIP	16	D-1	GBC	83	6.725	1	0.03	0.15	0.45	1.02
263	TTL	47	PDIP	16	D-1	GBC	58	21.978	2	0.04	0.09	0.19	0.43
264	CMOS	48	HDIP	16	D	GBC	50	3.241	2	0.25	0.62	1.32	0.22
265	LSTTL	48	PDIP	16	D-1	GBC	49	66.227	11	0.12	0.17	0.22	0.41
266	LTTL	48	PDIP	16	D-1	GBC	40	41.314	59	1.27	1.43	1.61	0.33
267	TTL	48	HDIP	16	B-2/ None	AUF	99	0.600	1	0.37	1.67	4.99	1.31
268	TTL	48	PDIP	16	D-1	GBC	56	14.446	3	0.11	0.21	0.38	0.42
269	TTL	48	PDIP	16	D-1	GBC	73	18.664	6	0.21	0.32	0.49	0.61
270	CMOS	49	PDIP	16	D-1	GBC	52	7.193	6	0.54	0.83	1.26	0.78
271	LSTTL	50	PDIP	16	D-1	GBC	49	209.475	25	0.10	0.12	0.14	0.41
272	LTTL	50	PDIP	16	D-1	GBC	45	21.787	7	0.22	0.32	0.47	0.36

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_j (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
273	TTL	50	PDIP	16	D-1	GBC	73	70.745	10	0.10	0.14	0.19	0.62
274	LSTTL	51	PDIP	16	D-1	GBC	46	27.013	4	0.08	0.14	0.23	0.39
275	LTTL	51	PDIP	16	D-1	GBC	43	21.220	3	0.07	0.14	0.26	0.35
276	TTL	51	PDIP	16	D-1	GBC	58	25.503	2	0.03	0.08	0.17	0.44
277	CMOS	52	HDIP	24	D	GBC	42	4.538	6	0.86	1.32	2.00	0.26
278	CMOS	52	PDIP	16	D-1	GBC	53	5.441	1	0.04	0.18	0.55	0.86
279	CMOS	53	PDIP	16	D-1	GBC	51	37.084	1	0.01	0.03	0.08	0.76
280	STTL	53	PDIP	16	D-1	GBC	53	3.721	2	0.22	0.54	1.15	1.09
281	LSTTL	54	PDIP	16	D-1	GBC	49	67.623	6	0.06	0.09	0.13	0.42
282	LTTL	54	PDIP	16	D-1	GBC	45	58.855	27	0.38	0.46	0.55	0.37
283	STTL	54	HDIP	16	D	GBC	77	158.855	16	0.08	0.10	0.13	0.37
284	TTL	54	PDIP	16	D-1	GBC	72	9.979	16	1.26	1.60	2.04	0.64
285	CMOS	56	HDIP	16	D	GF	42	12.347	2	0.07	0.16	0.35	0.35
286	TTL	56	PDIP	24	D-1	GBC	65	20.302	1	0.01	0.05	0.15	0.52
287	LSTTL	57	PDIP	16	D-1	GBC	49	228.885	16	0.05	0.07	0.09	0.43
288	TTL	57	HFPK	16	C-1	AUF	89	10.119	1	0.02	0.10	0.30	0.81
289	TTL	57	PDIP	14	D-1	GAC	44	29.491	7	0.16	0.24	0.35	0.32

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
290	TTL	57	PDIP	16	D-1	GBC	70	119.046	10	0.06	0.08	0.11	0.59
291	CMOS	58	PDIP	16	D-1	GBC	45	32.009	4	0.07	0.12	0.21	0.53
292	CMOS	58	HDIP	16	D	GBC	45	7.623	8	0.73	1.01	1.49	0.19
293	STTL	58	PDIP	20	D-1	GBC	36	2.467	1	0.09	0.41	1.21	0.58
294	ECL	59	HDIP	16	D	GBC	77	59.59	16	0.21	0.27	0.34	0.31
295	LTTL	59	PDIP	16	D-1	GBC	47	4.077	2	0.20	0.49	1.05	0.39
296	TTL	59	PDIP	16	D-1	GBC	74	12.766	3	0.12	0.23	0.43	0.70
297	LSTTL	60	PDIP	16	D-1	GBC	49	101.662	16	0.12	0.16	0.20	0.44
298	LTTL	60	PDIP	24	D-1	GBC	50	14.008	8	0.40	0.57	0.81	0.56
299	TTL	60	PDIP	16	D-1	GBC	70	50.030	6	0.08	0.12	0.18	0.62
300	CMOS	62	PDIP	16	D-1	GBC	47	43.945	4	0.05	0.09	0.15	0.60
301	ECL	62	HDIP	16	D	GBC	96	1.275	1	0.17	0.78	2.35	0.51
302	LSTTL	62	PDIP	16	D-1	GBC	49	61.902	5	0.05	0.08	0.13	0.44
303	TTL	62	PDIP	16	D-1	GBC	65	107.562	9	0.06	0.08	0.12	0.53
304	LSTTL	63	PDIP	24	D-1	GBC	48	38.060	12	0.24	0.32	0.42	0.57
305	TTL	63	HFPK	24	C-1	AUF	115	4.401	1	0.05	0.23	0.68	1.67
306	CMOS	64	HDIP	16	D	GBC	45	12.793	5	0.24	0.39	0.62	0.20

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_j (°C.)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	
307	LTTL	65	PDIP	16	D-1	GBC	46	6.139	6	0.64	0.98	1.48	0.39
308	LSTTL	66	PDIP	14	D-1	GBC	50	11.712	1	0.02	0.09	0.26	0.43
309	STTL	66	NDIP	16	D	GBC	86	9.838	3	0.16	0.30	0.56	0.53
310	TTL	66	HFPK	24	C-1	AUF	107	7.297	3	0.21	0.41	0.76	1.58
311	TTL	66	PDIP	16	D-1	GBC	73	17.728	16	0.71	0.90	1.15	0.71
312	LSTTL	70	PDIP	16	D-1	GBC	50	23.088	1	0.01	0.04	0.13	0.47
313	STTL	73	NDIP	28	D	GBC	65	1.492	1	0.15	0.67	2.01	0.43
314	CMOS	77	PDIP	16	D-1	GBC	45	33.212	4	0.12	0.18	0.27	0.55
315	LSTTL	77	EDIP	20	D-1	GBC	55	0.630	1	0.30	1.66	4.75	0.64
316	CMOS	80	PDIP	16	D-1	GBC	48	13.601	4	0.17	0.29	0.49	0.66
317	CMOS	86	IDIP	16	D	GF	47	16.455	2	0.05	0.12	0.26	0.40
318	CMOS	86	PDIP	16	D-1	GBC	48	60.224	12	0.15	0.20	0.26	0.70
319	TTL	98	CDIP	16	B-1	GF	63	1.207	1	0.18	0.83	2.48	0.08

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_j (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	Predicted
320	LSTTL	100	EDIP	16	D-1	GBC	51	4.311	1	0.05	0.23	0.69	0.55
321	TTL	100	EDIP	16	D-1	GBC	76	5.812	0	—	—	0.28	0.91
322	TTL	101	EDIP	24	D-1	GBC	69	11.977	0	—	—	0.13	0.89
323	LSTTL	104	EDIP	20	D-1	GBC	40	2.160	0	—	—	0.75	0.48
324	PMOS	107	HFPK	24	B-2	AIT	75	3.744	2	0.22	0.53	1.14	0.36
325	CMOS	109	EDIP	14	D-1	GBC	57	2.285	0	—	—	0.70	1.36
326	TTL	111	EDIP	24	D-1	GBC	65	8.951	4	0.26	0.45	0.75	0.83
327	CMOS	132	EDIP	16	D-1	GBC	41	12.436	0	—	—	0.13	0.49
328	LSTTL	145	EDIP	16	D-1	GBC	50	15.494	1	0.01	0.06	0.19	0.59
329	LSTTL	146	PDIP	16	D-1	GBC	50	13.315	4	0.17	0.30	0.50	0.61
330	PMOS	170	HFPK	32	B-2	AIT	75	0.468	0	—	—	3.44	0.53
331	PMOS	200	HFPK	28	B-2	AIT	80	0.468	1	0.48	2.14	6.40	0.52
332	TTL	260	PDIP	24	D-1	GBC	71	4.982	0	—	—	0.32	1.28
333	LTTL	263	EDIP	24	D-1	GBC	55	1.047	0	—	—	1.54	0.92
334	NMOS	350	CMDIP	40	D	GBC	55	6.035	2	0.14	0.33	0.71	0.50
335	P-MNOS	525	CMDIP	40	D	GBC	55	10.000	9	0.64	0.90	1.25	0.61
336	P-MNOS	525	EDIP	40	D-1	GBC	55	10.175	26	2.13	2.56	3.07	2.01

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_j (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	Predicted
337	PMOS	759	CMDIP	16	D	GF	65	17.566	14	0.61	0.80	1.03	0.73
338	PMOS	850	CMDIP	18	D	GBC	60	0.523	0	—	—	3.08	0.48
339	NMOS	900	CMDIP	28	D	GBC	55	2.992	1	0.07	0.33	1.00	0.53
340	NMOS	1100	CMDIP	40	D	GBC	60	1.492	0	—	—	1.08	0.77
341	NMOS	1100	PDIP	40	D-1	GBC	60	8.113	9	0.79	1.11	1.54	2.08
342	NMOS	1300	CMDIP	40	D	GBC	60	15.420	13	0.64	0.84	1.10	0.80
343	NMOS	1300	PDIP	40	D-1	GBC	60	0.506	0	—	—	3.18	3.64
344	PMOS	1333	CMDIP	16	D	GBC	50	28.761	28	0.82	0.97	1.16	0.37
345	PMOS	1333	EDIP	16	D-1	GBC	50	20.069	12	0.45	0.60	0.79	1.44
346	NMOS	1550	PDIP	40	D-1	GBC	57	1.723	0	—	—	0.91	2.67
347	PMOS	2000	EDIP	16	D-1	GBC	55	61.655	114	1.70	1.85	2.01	1.82
348	NMOS	2200	PDIP	40	D-1	GBC	55	4.713	6	0.83	1.27	1.93	2.98
349	NMOS	3000	CMDIP	40	D	GBC	60	0.244	2	3.38	8.20	17.5	1.04
350	NMOS	3530	CMDIP	40	D	GBC	57	3.038	1	0.07	0.33	0.99	0.94
351	NMOS	6260	CMDIP	40	D	GBC	65	1.068	0	—	—	1.51	1.01
352	NMOS	6250	EDIP	40	D-1	GBC	55	0.718	1	0.31	1.39	4.17	4.18

Device Description						Application Description					Failure Rates (F./10^6 Hours)			
											Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_A (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	
353	ECL NiCr PROM	16	PDIP	14	D-1	GBC	45	8.800	1	0.03	0.11	0.34	0.21
354	ECL NiCr PROM	256	CDIP	16	D	GBC	70	0.452	0	—	—	3.56	0.21
355	STTL TiW PROM	256	PDIP	16	D-1	GBC	65	0.155	0	—	—	10.4	0.50
356	TTL NiCr PROM	512	CDIP	24	C-1	AUF	95	1.605	0	—	—	1.00	1.45
357	STTL Poly Si PROM	1024	SDIP	16	D-1	GBC	75	0.671	0	—	—	2.30	0.96
358	TTL NiCr PROM	1024	CMDIP	16	B-1	AIT	87	12,666	1	0.02	0.08	0.24	0.13
359	PMOS UV PROM	2048	CMDIP	24	B-1	GT	55	0.827	0	—	—	1.95	0.19
360	PMOS UV PROM	2048	CMDIP	24	D	GBC	50	0.585	0	—	—	2.74	0.46
361	PMOS ROM	2048	CDIP	24	B-1	AUF	100	0.171	0	—	—	9.41	0.76
362	STTL AIM PROM	2048	HFPK	16	B-2	AIT	105	0.322	2	2.56	6.21	13.3	0.58
363	STTL NiCr PROM	2048	HDIP	16	B-2	GF	66	0.774	0	—	—	2.08	0.22
364	TTL ROM	2048	CMDIP	24	B-1	AUF	105	1.017	0	—	—	1.58	0.37
365	TTL NiCr PROM	2048	CMDIP	16	B-1	MGB	60	18.523	7	0.25	0.37	0.54	0.05
366	PMOS ROM	2300	CMDIP	24	D	AIT	80	0.855	0	—	—	1.88	1.81
367	PMOS ROM	5120	CMDIP	24	B-1	AUF	86	0.362	0	—	—	4.45	0.63
368	NMOS FAROM	8192	CMDIP	24	D	GBC	60	0.198	0	—	—	8.13	1.11
371	TTL ROM	8192	CMDIP	24	A-1	AUF	115	1.293	0	—	—	1.29	0.57

Device Description						Application Description					Failure Rates (F./10^6 Hours)			
											Observed			
Entry No.	Technology		Complexity	Package	No. Pins	Screen Class	Appl. Env	T_c (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	Predicted
370	FCL	RAM	16	EDIP	14	D-1	GBC	68	25.506	2	0.03	0.08	0.17	0.43
371	LTTL	S.R	16	PDIP	16	D-1	GBC	48	54.610	13	0.18	0.24	0.31	0.38
372	TTL	S.R.	16	CDIP	16	B-1/JB	GF	52	5.730	0	—	—	0.28	0.06
373	TTL	S.R	16	HDIP	16	B-1/JB	GT	57	0.764	0	—	—	2.11	0.09
374	TTL	RAM	16	HDIP	14	B-1	GT	55	1.444	0	—	—	1.11	0.07
375	TTL	S.R.	16	CDIP	16	B-1	NSS	52	2.294	0	—	—	0.70	0.09
376	TTL	S.R	16	HFPK	16	C-1	AUF	97	9.590	10	0.76	1.04	1.42	0.81
377	TTL	S.R	16	CFPK	16	C-1	AUF	103	0.474	1	0.47	2.11	6.32	0.89
378	TTL	S.R.	16	PDIP	16	D-1	GBC	70	20.192	0	—	—	0.08	0.60
379	CMOS	S.R	24	EDIP	16	D-1	GBC	45	5.200	0	—	—	0.31	0.32
380	CMOS	Static RAM	64	PDIP	16	D-1	GBC	45	2.870	1	0.08	0.35	1.64	0.52
381	LTTL	RAM	64	EDIP	16	D-1	GBC	48	1.122	3	1.37	2.67	4.92	0.57
382	STTL	RAM	64	HDIP	16	B-1/JB	GF	59	0.378	0	—	—	4.26	0.09
383	STTL	RAM	64	CDIP	16	B-1	AUF	105	0.512	0	—	—	3.14	0.35
384	STTL	RAM	64	CFPK	16	D	ALT	96	0.148	2	5.57	13.5	28.9	1.53
385	STTL	RAM	64	PDIP	16	D-1	GBC	55	75.050	25	0.28	0.33	0.40	0.65
386	STTL	RAM	64	PDIP	16	D-1	GF	59	0.893	0	—	—	1.98	1.07

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
387	TTL RAM	64	CDIP	16	B-1	AUF	67	7.397	0	—	—	0.22	0.10
388	TTL RAM	64	CDIP	16	B-1	AUF	106	0.974	0	—	—	1.65	0.39
389	TTL RAM	64	HFPK	16	B-1	AUF	111	0.536	0	—	—	3.00	0.36
390	TTL RAM	64	HDIP	16	B-1	GF	65	1.16	0	—	—	1.39	0.09
391	TTL RAM	64	CDIP	16	B-2	NSS	57	19.163	0	—	—	0.08	0.24
392	TTL RAM	64	PDIP	16	D-1	GBC	55	42.044	26	0.51	0.62	0.74	0.65
393	ECL RAM	128	HDIP	16	D	GBC	40	924.000	148	0.15	0.16	0.17	0.25
394	MNOS Static S.R.	128	CFPK	14	C-1	AUF	98	16.631	48	2.53	2.89	3.30	2.23
395	PMOS Dyn. S.R.	128	Can	8	B-1	GF	40	2.766	0	—	—	0.58	0.03
396	PMOS Static S.R.	160	Can	8	D	GBC	45	1.230	0	—	—	1.31	0.15
397	PMOS Dyn S.R.	200	Can	8	D	GBC	45	2.028	0	—	—	0.79	0.13
398	ECL RAM	256	HDIP	16	B-2	GBC	60	600,000	49	0.07	0.08	0.09	0.23
399	PMOS Static RAM	256	HDIP	16	B-1	GT	59	0.722	0	—	—	2.23	0.13
400	STTL RAM	256	HDIP	16	B-1/ +D	GF	62	76.99	0	—	—	0.02	0.16
401	STTL RAM	256	CMDIP	16	D	GBC	55	1.772	6	2.20	3.39	5.12	0.59
402	TTL RAM	256	HDIP	16	B-1	MGB	45	5.142	1	0.04	0.19	0.58	0.07
403	TTL RAM	256	HDIP	16	B-1/ None	MGB	40	10.659	3	0.14	0.28	0.52	0.32

Device Description						Application Description					Failure Rates (F./10^6 Hours)			
											Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_c (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	Predicted
404	TTL RAM	256	CMDIP	16	D	GBC	58	4.132	5	0.75	1.21	1.91	0.56
405	NMOS Static RAM	1024	CMDIP	16	B-1/1B	GBC	39	0.327	0	—	—	4.92	0.07
406	NMOS Static RAM	1024	HDIP	16	B-1	GT	39	18.754	2	0.04	0.11	0.23	0.15
407	NMOS Static RAM	1024	PDIP	16	B-1	GAC	40	75.400	0	—	—	0.02	1.17
408	NMOS Static Ram	1024	PDIP	16	D-1	GBC	40	77.457	8	0.07	0.10	0.15	0.85
409	PMOS Dyn S.R.	1024	HDIP	16	B-1/1B	GF	33	14.94	1	0.01	0.07	0.20	0.08
410	PMOS Dyn RAM	1024	CMDIP	24	B-1	AIT	79	0.797	1	0.28	1.25	3.76	0.32
411	PMOS Dyn. RAM	1024	CMDIP	18	B-1	GT	33	1.218	0	—	—	1.32	0.11
412	PMOS Dyn S.R.	1024	Can	8	B-1	NSS	45	17.406	3	0.09	0.17	0.32	0.08
413	PMOS Dyn S.R.	1024	Can	16	C-1	GT	35	0.414	0	—	—	3.89	0.33
414	PMOS Dyn RAM	1024	HFPK	16	D	AIT	99	0.390	3	3.94	7.69	14.1	3.25
415	PMOS Dyn S.R.	1024	Can	8	D	GB	45	160.464	47	0.26	0.29	0.33	0.27
416	PMOS Dyn RAM	1024	CMDIP	16	D	GBC	45	30.000	10	0.24	0.33	0.46	0.33
417	PMOS Dyn RAM	1024	CDIP	22	D	GBC	45	1.267	7	3.74	5.52	8.08	0.41
418	PMOS Dyn S.R	1024	CMDIP	16	D	GAC	49	7.096	0	—	—	0.23	0.38
419	PMOS Dyn S.R.	1024	Can	8	D	GBC	55	5.104	2	0.16	0.39	0.84	0.42
420	PMOS Dyn RAM	1024	CMDIP	16	D	GBC	50	496147	96	0.18	0.19	0.21	0.40

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
421	TTL RAM	1024	EDIP	16	D-1	GBC	55	10.202	4	0.23	0.39	0.66	2.36
422	NMOS Dyn RAM	4096	HDIP	22	D	GBC	50	876.70	68	—	0 08		
423	NMOS Dyn RAM	4096	CMDIP	16	D*	GBC	55	9.073	4	0.56	0.98	1.65	1.16
424	NMOS Dyn RAM	4096	HDIP	22	D*	GBC	50	900.000	351	0.37	0.39	0.41	0.99
425	NMOS Dyn RAM	4096	EDIP	16	D-1*	GBC	55	9.257	4	0.25	0.43	0.73	5.11
426	NMOS Dyn RAM	4096	EDIP	16	D-1	GBC	55	9.610	2	0.09	0.21	0.45	5.11
427	NMOS Dyn RAM	4096	CMDIP	16	D	GF	50	8.950	1	0.02	0.11	0.33	1.17
428	NMOS Dyn RAM	4096	CMDIP	18	D	GF	50	24.400	16	0.52	0.66	0.83	1.19
429	NMOS Dyn RAM	4096	CDIP	16	D	GF	55	16.600	14	0.65	0.84	1.09	1.42
430	NMOS Dyn RAM	16K	CDIP	16	D	GF	60	1.425	0	—	—	1.13	3.74

* Devices received board level burn-in

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Transistor Complexity	Package	No. Pins	Screen Class	Appl. Env	T_c (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	
431	Diff. Amp	3	Can	8	D	GBC	75	59.000	13	0.17	0.22	0.29	0.31
432	Multifng. Amp	3	Can	10	D	GBC	50	8.930	3	0.17	0.34	0.62	0.12
433	Clock Driver	4	Can	12	B-1	NSS	35	1.200	0	—	—	1.34	0.08
434	Clock Driver	4	Can	12	D	ED	35	4.700	3	0.33	0.64	1.17	0.13
435	Transistor Array	5	CDIP	14	D	GBC	50	135.000	47	0.30	0.35	0.40	0.19
436	Transistor Array	5	EDIP	14	D-1	GBC	50	369.000	257	0.66	0.70	0.74	0.53
437	Translator	6	Can	10	D	GBC	50	6.920	0	—	—	0.23	0.17
438	Diff Amp	6	Can	12	D	GBC	65	58.000	98	1.54	1.69	1.85	0.34
439	Driver	6	EDIP	10	D-1	GF	35	1.085	0	—	—	1.48	0.55
440	Diff. Amp	7	MGDIP	16	B-1	GT	43	2.000	0	—	—	0.80	0.11
441	Modem	8	Can	10	D	GBC	55	91.000	34	0.32	0.37	0.44	0.23
442	Driver	8	PDIP	14	D-1	GBC	50	70.600	24	0.28	0.34	0.41	0.68
443	Volt Comp	9	Can	8	B-1	GF	35	3.570	0	—	—	0.45	0.04
444	Volt. Comp	9	HTPK	8	B-1	NSS	35	1.200	0	—	—	1.34	0.05
445	Volt Comp	9	Can	8	D	GBC	54	151.100	62	0.30	0.34	0.38	0.21
446	Volt. Comp	9	Can	8	D	GBC	76	1.280	2	0.64	1.56	3.34	0.70
447	Line Driver	10	ATPK	14	C-1	AUF	79	2.270	0	—	—	0.71	1.26

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	
448	Wideband Amp	10	Can	10(7)	D	GBC	50	4.900	4	0.47	0.82	1.37	0.19
449	Op Amp	10	EDIP	14(12)	D-1	GBC	44	2,710	7	1.75	2.58	3.78	0.52
450	Driver	10	PDIP	8	D-1	GBC	50	125.077	64	0.46	0.51	0.57	0.68
451	Op Amp	10	EDIP	14(12)	D-1	GBC	57	6.480	4	0.35	0.62	1.04	1.24
452	Op Amp	11	Can	8	B-1	GF	35	3.570	0	—	—	0.45	0.04
453	Op Amp	11	HFPK	8	C-1	NSS	60	11.000	2	0.07	0.18	0.39	0.40
454	Volt. Comp	11	Can	10	D	GB	35	10.700	2	0.08	0.19	0.40	0.15
455	Volt Comp	11	Can	8	D	GBC	55	2.030	1	0.11	0.49	1.48	0.26
456	Diff Amp	11	Can	10	D	GBC	72	18.600	5	0.17	0.27	0.43	0.65
457	Op Amp	11	Can	8	D	GBC	86	35.600	29	0.69	0.81	0.97	1.38
458	Driver	12	HFPK	12	C-1	AUF	75	4.028	2	0.20	0.50	1.06	1.24
459	Translator	12	CDIP	16	D	GBC	40	23.900	8	0.23	0.33	0.45	0.22
460	Translator	12	EDIP	16	D-1	GBC	40	154.110	40	0.22	0.26	0.30	0.53
461	Line Receiver	12	EDIP	14	D-1	GBC	52	26.201	13	0.38	0.50	0.65	1.02
462	Volt Comp	13	Can	8	D	GBC	58	34.500	1	0.01	0.03	0.09	0.25
463	Line Receiver	13	CDIP	16	D	GBC	62	13.500	8	0.41	0.59	0.84	0.50
464	Audio Amp	14	CDIP	14	D	GAC	50	15.400	9	0.42	0.58	0.81	0.29

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
465	Op Amp	14	Can	8	D	GBC	55	3.300	3	0.47	0.91	1.67	0.30
466	Periph. Driver	14	EDIP	8	D-1	GBC	61	6.322	1	0.04	0.16	0.47	2.06
467	Volt Reg	14	FINL	3	D-1	GBC	50	9.660	5	0.32	0.52	0.82	0.77
468	Volt Reg	16	Can	3	D	GBC	50	44.340	31	0.59	0.70	0.83	0.24
469	Op Amp	16	Can	8	D	GBC	50	28.250	9	0.23	0.32	0.44	0.27
470	Multiplier	16	CDIP	14	D	GBC	54	3.320	2	0.25	0.60	1.29	0.38
471	Wideband Amp	16	Can	8	D	GBC	68	1.880	1	0.12	0.53	1.59	0.71
472	Volt Reg	16	FINL	3	D-1	GBC	50	340.713	231	0.64	0.68	0.72	0.89
473	Driver	16	EDIP	8	D-1	GBC	50	20.530	4	0.11	0.19	0.33	1.07
474	Line Receiver	16	FDIP	14	D-1	GBC	54	78.000	29	0.31	0.37	0.44	1.38
475	IF Amp	16	EDIP	8	D-1	GBC	58	8.900	2	0.09	0.22	0.48	1.83
476	Line Receiver	17	CDIP	16	D	GBC	49	11.040	6	0.35	0.54	0.82	0.31
477	Line Receiver	17	PDIP	16	D-1	GBC	50	105.901	64	0.54	0.60	0.68	1.03
478	Voltage Reg	17	FINL	3	D-1	GBC	56	14.400	7	0.33	0.49	0.71	1.77
479	Line Receiver	18	CDIP	16	D	GBC	47	92.900	24	0.21	0.26	0.31	0.32
480	Volt. Comp	18	CDIP	14(16)	D	GBC	56	10.800	6	0.36	0.56	0.84	0.41
481	Volt Reg	18	Can	8	D	GBC	58	22.500	24	0.88	1.07	1.29	0.44

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_A (°C)	Device Hours (10^6)	No. Failures	20% C.L.	Pt. Est	80% C.L.	Predicted
482	Line Perceiver	18	PDIP	16	D-1	GBC	50	80.000	29	0.30	0.36	0.43	1.12
483	Op Amp	19	Can	8	D	GBC	50	21.100	4	0.10	0.17	0.28	0.29
484	Volt Reg	19	Can	3	D	GBC	58	89.400	43	0.42	0.48	0.54	0.44
485	Op Amp	19	Can	8	D	GBC	61	228.568	40	0.15	0.18	0.20	0.52
486	Op Amp	19	EDIP	8(7)	D-1	GBC	55	22.400	2	0.04	0.09	0.19	1.59
487	Line Driver	20	CDIP	14	D	GBC	65	18.400	20	0.88	1.09	1.34	4.71
488	Volt. Reg	20	CDIP	14(11)	D	GBC	58	37.000	45	1.06	1.22	1.40	0.49
489	Func Gen	20	EDIP	8(7)	D-1	GBC	50	2.790	2	0.30	0.72	1.53	1.09
490	Volt Reg	20	EDIP	14(11)	D-1	GBC	58	68.000	110	1.49	1.62	1.76	2.12
491	Op Amp	21	Can	8	D	GBC	50	1071.192	573	0.51	0.53	0.54	0.32
492	Volt Reg	21	Can	3	D	GBC	50	27.110	5	0.11	0.17	0.27	0.29
493	Op Amp	21	Can	8	D	GBC	54	61.475	36	0.50	0.59	0.68	0.39
494	Volt Reg	21	CDIP	10(9)	D	GBC	71	4.690	6	0.83	1.28	1.94	0.98
495	Volt Reg	21	EINL	3	D-1	GBC	50	59.060	13	0.20	0.25	0.32	1.07
496	Op Amp	21	PDIP	8	D-1	GBC	50	51.600	14	0.21	0.27	0.35	1.16
497	Volt Reg	22	Can	2	D	GBC	58	73.400	48	0.57	0.65	0.75	0.46
498	Op Amp	22	Can	8	D	GBC	50	411.100	159	0.36	0.39	0.41	0.32

Device Description					Application Description					Failure Rates (F./10⁶ Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
499	Op Amp	22	Can	10	D	GBC	50	8.900	7	0.53	0.79	1.16	0.34
500	Op Amp	22	EDIP	8	D-1	GBC	45	436.000	235	0.51	0.54	0.57	0.98
501	Op Amp	23	Can	8	B-1	GT	35	8.544	0	—	—	0.19	0.10
502	Op Amp	23	Can	8	B-1	NSS	43	3.400	0	—	—	0.47	0.10
503	Op Amp	23	HFPK	10(?)	C-1	AUF	79	1.095	1	0.20	0.91	2.73	1.67
504	Timer	23	Can	8	D	GBC	50	101.980	62	0.54	0.61	0.68	0.33
505	Op Amp	23	Can	8	D	GBC	50	1338.020	478	0.34	0.36	0.37	0.33
506	Volt Comp	23	Can	8	D	GBC	61	226.480	50	0.19	0.22	0.25	0.58
507	Timer	23	PDIP	8	D-1	GBC	50	39.600	5	0.08	0.13	0.20	1.19
508	Op Amp	23	PDIP	8	D-1	GBC	52	193.300	107	0.51	0.55	0.60	1.37
509	Volt Comp	23	PDIP	14	D-1	GBC	50	55.040	15	0.21	0.27	0.35	1.27
510	Op Amp	24	Can	8	D	GBC	60	76.098	25	0.29	0.33	0.40	0.58
511	Translator	24	EDIP	16	D-1	GBC	40	166.000	27	0.14	0.16	0.19	0.73
512	Line Receiver	25	HDIP	16	B-1	GT	40	2.300	0	—	—	0.70	0.14
513	Volt. Reg	25	Can	10	D	GBC	50	54.400	39	0.62	0.72	0.83	0.37
514	Op Amp	25	Can	8(?)	D	GBC	52	25.400	17	0.53	0.67	0.84	0.38
515	Op Amp	25	Can	8	D	GBC	60	11.960	11	0.68	0.92	1.24	0.58

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
516	Op Amp	25	Can	8(7)	D	GBC	66	112.538	91	0.74	0.81	0.89	0.84
517	Line Receiver	25	EDIP	14(12)	D-1	GBC	53	2.700	9	2.38	3.33	4.64	1.64
518	Volt. Reg	26	EINL	3	D-1	GBC	50	7.080	6	0.55	0.85	1.28	1.24
519	Op Amp	26	EDIP	8	D-1	GBC	50	17.579	3	0.09	0.17	0.31	1.30
520	Volt Reg	27	EINL	3	D-1	GBC	58	25.610	68	0.81	0.90	1.00	2.62
521	Line Receiver	29	HFPK	14(12)	C-1	AUF	83	4.088	3	0.38	0.73	1.35	2.54
522	Line Receiver	29	CDIP	14(12)	D	GB	38	19.500	1	0.01	0.05	0.15	0.26
523	Op Amp	29	Can	8	D	GBC	50	303.040	162	0.50	0.53	0.57	0.35
524	Volt Reg	29	Can	9	D	GBC	58	20.500	70	3.07	3.41	3.81	0.63
525	Op Amp	29	PDIP	8	D-1	GBC	50	8.000	7	0.80	1.13	1.56	1.41
526	Op Amp	30	Can	8	D	GBC	50	55.800	48	0.75	0.86	0.98	0.40
527	Op Amp	30	Can	8(7)	D	GBC	70	37.760	42	0.97	1.11	1.28	1.19
528	Line Driver	30	PDIP	14	D-1	GB	35	2.370	1	0.09	0.42	1.26	0.54
529	Driver	32	HFPK	16	C-1	AUF	80	3.600	2	0.23	0.56	1.19	2.57
530	A/D Converter	32	CDIP	16	D	GBC	73	29.400	47	1.40	1.60	1.83	1.52
531	Clock Driver	32	EDIP	16	D-1	GBC	50	3.660	2	0.23	0.55	1.17	1.60
532	Bus Driver	32	EDIP	14	D-1	GBC	66	4.685	8	1.19	1.71	2.43	5.91

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			Predicted
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	
533	Line Driver	32	EDIP	14	D-1	GBC	78	4.600	16	2.23	3.48	4.42	16.2
534	Op Amp	34	Can	8	D	GF	35	3.600	1	0.06	0.28	0.83	0.42
535	Op Amp	34	Can	8	D	GBC	51	560.423	357	0.61	0.64	0.67	0.46
536	Op Amp	34	PDIP	8	D-1	GBC	48	192.000	38	0.17	0.20	0.23	1.33
537	Line Receiver	36	CDIP	16	B-1	GF	38	5.544	0	—	—	0.29	0.16
538	A/D Converter	36	CDIP	16	D	GBC	68	171.400	62	0.32	0.36	0.41	1.29
539	Op Amp	36	Can	8	D	GBC	71	100.000	119	1.08	1.17	1.27	1.45
540	Volt Comp	36	EDIP	14	D-1	GBC	50	52.800	43	0.71	0.81	0.94	1.73
541	Line Driver	38	CDIP	14	D	GB	45	14.700	8	0.38	0.54	0.77	0.41
542	Line Driver	38	EDIP	14	D-1$_2$	GBC	52	2.700	9	2.38	3.33	4.64	2.17
543	Multiplier	39	CDIP	16(15)	D	GBC	50	1.990	1	0.11	0.50	1.50	0.53
544	Op Amp	40	HFPK	10(8)	C-1	AUF	80	1.100	2	0.75	1.82	3.89	2.59
545	Op Amp	40	Can	8	D	GBC	50	222.009	76	0.31	0.35	0.38	0.48
546	Volt Reg	40	Can	10	D	GBC	50	5.060	1	0.04	0.20	0.59	0.50
547	Volt Reg	40	EDIP	10	D-1	GBC	50	1.900	2	0.43	1.05	2.25	1.79
548	Volt Comp	44	Can	10	D	GBC	50	16.800	9	0.38	0.54	0.95	0.53
549	Volt Comp	48	MDIP	14	D-1	GBC	53	81.200	131	0.63	0.69	0.74	2.64

Device Description					Application Description					Failure Rates (F./10^6 Hours)			
										Observed			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env	T_a (°C)	Device Hours (10^6)	No. Failures	20% C.L.	M. Est	80% C.L.	Predicted
550	D/A Converter	51	CDIP	14	D	GBC	57	3.910	1	0.06	0.26	0.77	0.91
551	Switch	52	CDIP	14	D	GBC	40	6.900	6	0.57	0.87	1.32	1.05
552	Op Amp	52	HFPK	14	D	GBC	50	20.100	17	0.67	0.85	1.07	0.60
553	Op Amp	52	MDIP	14	D-1	GBC	50	81.600	37	0.36	0.41	0.48	2.20
554	Sense Amp	58	HFPK	24	B-1	AUF	32	2.260	2	0.36	0.88	1.89	1.05
555	D/A Converter	60	CDIP	16	D	GBC	58	56.540	15	0.21	0.27	0.34	1.03
556	Op Amp	68	EDIP	14	D-1	GBC	48	26.000	16	0.48	0.62	0.78	2.21
557	Op Amp	100	PDIP	14	D-1	GBC	50	36.200	9	0.18	0.25	0.35	3.50
558	TTL	72	HDIP	16	JB	AUF		0.248	0	—	—	6.49	
559	TTL	64	HDIP	16	B-1	AUF		0.238	0	—	—	6.76	
560	TTL	512	HFPK	24	C-1	AUF		0.380	0	—	—	4.24	
561	TTL	72	HFPK	16	C-1	AUF		2.887	0	—	—	0.56	
562	TTL	72	HDIP	16	B-1	GF		2.621	0	—	—	0.61	
563	TTL	72	HDIP	16	B-1	GF		0.423	0	—	—	3.80	
564	TTL	4	HDIP	16	B-1	GF		0.927	0	—	—	1.74	
565	TTL	4	HDIP	16	B-1	GF		0.988	0	—	—	1.63	
566	TTL	2048	HDIP	16	B-1	GF		0.433	0	—	—	3.72	

Device Description.					Application Description				Failure Rates (F/10^6 Hours)			
Entry No.	Technology	Complexity	Package	No. Pins	Screen Class	Appl. Env.	T_j (°C)	Device-Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Pt. Est.	Observed 80% C.L.	Predicted
567	STTL	2048	HDIP	16	AUT			0·255	0	—	—	6·31	
568	MOS P-STAT	128	HFPL	14	AUF			4·716	1	0·05	0·21	0·63	
569	MOS P-DYN	200	HCAN	8	NS			0·303	0	—	—	5·31	
570	MOS N-STAT	1024	HDIP	16	QF			10·322	0	—	—	0·16	
571.	MOS N-DYN	16384	HDIP	16	CBC			171·00	38	0·19	0·22	0·26	

APPENDIX B

CORRELATION MATRICES

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	COMP	31.7258	22.5637	1.0000E 00	8.6000E 01
2	PKG	2.3645	0.4999	2.0000E 00	3.0000E 00
3	NPIN	15.5806	1.4090	1.4000E 01	2.4000E 01
4	SC	7.5645	0.4999	7.0000E 00	8.0000E 00
5	APEN	3.8226	0.3851	3.0000E 00	4.0000E 00
6	TJ	45.4353	5.5149	4.1000E 01	6.5000E 01
7	MTS	40.4958	85.4009	1.2420E 00	5.7697E 02
8	#FAI	9.1290	20.5638	1.0000E 00	1.4600E 02
9	OB1	0.1934	0.2224	1.0000E-02	1.2300E 00
10	OB	0.3445	0.3729	3.0000E-02	2.4000E 00
11	OB2	0.6250	0.6798	8.0000E-02	4.4200E 00
12	PRED	0.2829	0.1624	1.2000E-01	1.0200E 00
13	LOG	-0.0215	0.4135	-1.1461E 00	8.6171E-01

CORR. MATRIX

CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
	[9]	[10]	[11]	[12]	[13]			
[1]	1.000							
[2]	0.092	1.000						
[3]	0.443	-0.124	1.000					
[4]	0.092	1.000	-0.124	1.000				
[5]	0.041	0.529	0.042	0.529	1.000			
[6]	0.405	0.183	-0.031	0.183	0.160	1.000		
[7]	-0.249	0.224	-0.237	0.224	0.139	-0.074	1.000	
[8]	-0.252	0.181	-0.229	0.181	0.111	-0.097	0.963	1.000
[9]	-0.068	-0.250	0.243	-0.250	-0.261	-0.102	-0.038	0.098
[10]	1.000							
	-0.058	-0.261	0.248	-0.261	-0.297	-0.093	-0.156	-0.034
[11]	0.945	1.000						
	-0.057	-0.240	0.217	-0.240	-0.285	-0.092	-0.230	-0.126
[12]	0.810	0.955	1.000					
	0.424	0.242	0.036	0.242	-0.125	0.832	-0.106	-0.142
[13]	-0.016	-0.009	-0.025	1.000				
	-0.324	-0.274	0.046	-0.274	-0.068	-0.433	-0.032	0.126
	0.710	0.721	-0.606	-0.501	1.000			

ENTER NO. OF 'X' VARS, THEN INDEX OF 'Y' VAR
TERMINATED BY ENTRY OF ALL ZEROES

HTTL

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	COLP	6.6522	4.8467	2.0000E 00	1.6000E 01
2	PKG	3.0000	1.0445	2.0000E 00	5.0000E 00
3	NPIN	16.1739	0.5762	1.4000E 01	1.6000E 01
4	SC	7.1304	1.0998	5.0000E 00	8.0000E 00
5	APEN	4.0000	3.1334	1.0000E 00	1.0000E 01
6	TJ	31.6957	17.1078	3.0000E 01	9.0000E 01
7	TTS	21.7732	18.9395	2.4070E 00	7.6173E 01
8	CFAI	5.9130	6.8205	1.0000E 00	2.0000E 01
9	OE1	0.2257	0.2408	1.0000E-02	9.2000E-01
10	OE	0.3713	0.3443	4.0000E-02	1.2700E 00
11	OE2	0.6217	0.5355	1.0000E-01	1.7800E 00
12	PPED	0.1804	0.1306	9.0000E-02	4.8000E-01
13	LCG	0.1929	0.4200	-5.1180E-01	1.1038E 00

CORR. MATRIX

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CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
	[9]	[10]	[11]	[12]	[13]			
[1]	1.000							
[2]	-0.099	1.000						
[3]	0.608	-0.151	1.000					
[4]	0.401	-0.633	0.106	1.000				
[5]	-0.099	1.000	-0.151	-0.633	1.000			
[6]	0.141	0.941	-0.004	-0.558	0.941	1.000		
[7]	-0.208	-0.176	-0.144	0.467	-0.176	-0.228	1.000	
[8]	-0.024	-0.025	0.143	0.268	-0.025	-0.042	0.532	1.000
[9]	0.084	0.172	0.346	-0.255	0.172	0.170	-0.150	0.470
	1.000							
[10]	0.070	0.301	0.310	-0.401	0.301	0.296	-0.350	0.304
	0.961	1.000						
[11]	0.062	0.408	0.244	-0.501	0.408	0.406	-0.491	0.112
	0.840	0.956	1.000					
[12]	-0.102	0.939	-0.049	-0.829	0.939	0.916	-0.372	-0.143
	0.253	0.402	0.516	1.000				
[13]	0.071	-0.162	0.354	-0.003	-0.162	-0.165	-0.113	0.546
	0.818	0.780	0.679	-0.092	1.000			

ENTER NO. OF

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	COMP	30.8158	35.4834	1.0000E 00	1.4600E 02
2	PKG	3.2368	0.8198	3.0000E 00	5.0000E 00
3	NPIN	15.6316	2.0191	1.4000E 01	2.4000E 01
4	TJ	46.2105	3.3864	4.1000E 01	5.5000E 01
5	HRS	196.3143	357.3795	6.2000E-01	1.9517E 03
6	AFAI	26.8421	52.7162	1.0000E 00	2.7500E 02
7	OB1	0.1029	0.0853	1.0000E-02	3.7000E-01
8	OB	0.1774	0.2636	3.0000E-02	1.6600E 00
9	OB2	0.3292	0.7500	6.0000E-02	4.7500E 00
10	PRED	0.1992	0.0683	1.1000E-01	3.6000E-01
11	LOG	-0.1903	0.3175	-8.1292E-01	6.6381E-01

CORR. MATRIX
*

CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
	[9]	[10]	[11]					
[1]								
	1.000							
[2]								
	0.573	1.000						
[3]								
	0.317	0.250	1.000					
[4]								
	0.798	0.507	0.446	1.000				
[5]								
	-0.326	-0.157	-0.267	-0.277	1.000			
[6]								
	-0.306	-0.145	-0.243	-0.238	0.985	1.000		
[7]								
	-0.020	0.117	0.267	0.169	0.103	0.187	1.000	
[8]								
	0.205	0.532	0.393	0.439	-0.068	-0.046	0.735	1.000
[9]								
	0.249	0.612	0.388	0.479	-0.128	-0.103	0.573	0.976
	1.000							
[10]								
	0.913	0.583	0.621	0.906	-0.373	-0.346	0.124	0.410
	0.454	1.000						
[11]								
	-0.217	0.114	0.065	-0.052	0.216	0.293	0.595	0.677
	0.532	-0.104	1.000					

ENTER NO. OF 'X' VARS, THEN INDEX OF 'Y' VAR
FOLLOWED BY INDI
*

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	CONP	90.9032	364.8151	1.0000E 00	2.0480E 03
2	PMG	3.0323	1.2776	1.0000E 00	9.0000E 00
3	MPIN	15.2065	2.6002	1.4000E 01	2.5000E 01
4	SC	7.4839	1.2877	2.0000E 00	6.0000E 00
5	APEN	4.4839	2.0145	3.0000E 00	1.2000E 01
6	XJ	61.5484	18.0127	2.7000E 01	1.0500E 02
7	HRS	65.4300	100.6722	1.4000E-01	3.5535E 02
8	AGAI	12.7097	19.2911	1.0000E 00	7.4000E 01
9	C21	0.4839	1.1046	1.0000E-02	5.5700E 00
10	C2	1.0613	2.6077	3.0000E-02	1.3500E 01
11	C32	2.1919	5.5451	7.0000E-02	2.8900E 01
12	PPED	0.3148	0.2920	5.0000E-02	1.5300E 00
13	LOG	0.1521	0.4517	-6.0207E-01	1.1250E 00

CORR. MATRIX

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CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
	[9]	[10]	[11]	[12]	[13]			
[1]								
	1.000							
[2]								
	0.262	1.000						
[3]								
	0.050	-0.118	1.000					
[4]								
	-0.507	-0.030	-0.150	1.000				
[5]								
	0.699	0.836	0.010	-0.337	1.000			
[6]								
	0.473	0.442	0.055	-0.043	0.604	1.000		
[7]								
	-0.156	-0.076	-0.311	0.210	-0.162	-0.297	1.000	
[8]								
	-0.125	-0.051	-0.247	0.205	-0.136	-0.255	0.962	1.000
[9]								
	0.399	0.780	0.018	-0.273	0.862	0.480	-0.200	-0.139
	1.000							
[10]								
	0.403	0.837	0.051	-0.299	0.895	0.499	-0.225	-0.172
	0.999	1.000						
[11]								
	0.401	0.859	0.075	-0.314	0.903	0.501	-0.237	-0.192
	0.974	0.997	1.000					
[12]								
	0.238	0.679	0.155	-0.107	0.710	0.707	-0.342	-0.276
	0.842	0.843	0.842	1.000				
[13]								
	0.392	0.317	0.001	-0.554	0.454	-0.088	-0.208	-0.025
	0.571	0.561	0.554	0.237	1.000			

ENTER VC. 0

VAR	LABEL	MEAN	STD-DEV.	MIN	MAX
1	COMP	24.0435	10.7189	2.CCCCE CC	6.5CCCE 01
2	PKG —	2.9565	0.2560	2.CCCCE CC	6.CCCCE CC
3	SPIN	15.4348	2.0939	1.4CCCE 01	2.4CCCE 01
4	SC	7.8913	0.3147	7.CCCCE CC	8.CCCCE CC
5	APEL	4.8696	2.5176	4.CCCCE CC	1.2CCCE 01
6	TJ —	45.1957	6.4212	3.1CCCE 01	6.CCCCE 01
7	HRS	61.0664	109.8700	1.122CE CC	6.7434E 02
8	STAT	21.6087	36.2132	1.CCCCE CC	1.27CCE 02
9	CD1	0.2809	0.3072	1.CCCCE-02	1.37CCE CC
10	CC	0.4217	0.4406	6.CCCCE-02	2.67CCE CC
11	CD2	0.6400	0.7412	1.CCCCE-01	4.92CCE CC
12	PRED	0.1972	0.1097	1.1CCCE-01	7.CCCCE-01
13	LOC	0.2096	0.4227	-7.5334E-01	1.0143E CC

CORR. MATRIX

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CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
	[9]	[10]	[11]	[12]	[13]			
[1]	1.000							
[2]	0.414	1.000						
[3]	0.481	-0.022	1.000					
[4]	0.280	0.607	-0.095	1.000				
[5]	-0.280	-0.607	0.095	-1.000	1.000			
[6]	0.142	-0.314	0.308	-0.648	0.648	1.000		
[7]	-0.267	0.031	-0.177	0.170	-0.170	-0.181	1.000	
[8]	-0.254	0.052	-0.203	0.201	-0.201	-0.338	0.917	1.000
[9]	0.286	0.503	-0.012	0.286	-0.286	-0.436	0.020	0.279
	1.000							
[10]	0.370	0.703	0.054	0.181	-0.181	-0.272	-0.085	0.111
	0.939	1.000						
[11]	0.290	0.710	0.116	0.030	-0.030	-0.075	-0.167	-0.040
	0.790	0.951	1.000					
[12]	0.205	-0.283	0.653	-0.736	0.736	0.711	-0.246	-0.286
	-0.125	0.039	0.213	1.000				
[13]	0.098	0.490	-0.161	0.523	-0.523	-0.663	0.145	0.382
	0.819	0.715	0.560	-0.423	1.000			

ENTER NO. OF 'X'

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	COMP	75.6526	253.7596	1.0000E 00	2.0480E 03
2	PKG	3.3895	1.2989	1.0000E 00	9.0000E 00
3	NPIN	15.4105	2.0602	1.4000E 01	2.4000E 01
4	SC	6.7579	1.8946	1.0000E 00	8.0000E 00
5	APEN	5.4421	2.7472	2.0000E 00	1.2000E 01
6	TJ	62.6632	17.9269	3.0000E 01	1.1500E 02
7	HRS	83.2171	217.7419	4.7400E-01	1.8550E 03
8	#FAI	16.6105	41.1684	1.0000E 00	3.2300E 02
9	OB1	0.2376	0.2974	1.0000E-03	1.9100E 00
10	OB	0.4233	0.5431	4.0000E-02	3.3300E 00
11	OB2	0.7964	1.1742	8.0000E-02	6.3200E 00
12	PRED	0.3324	0.3194	4.0000E-02	1.6700E 00
13	LOG	0.0431	0.4323	-9.6300E-01	1.0160E 00

CORR. MATRIX

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CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
	[9]	[10]	[11]	[12]	[13]			
[1]	1.000							
[2]	-0.172	1.000						
[3]	0.109	0.198	1.000					
[4]	-0.250	-0.216	-0.010	1.000				
[5]	-0.070	0.488	0.069	-0.594	1.000			
[6]	0.029	0.516	0.393	-0.388	0.778	1.000		
[7]	-0.081	-0.108	-0.155	0.229	-0.187	-0.249	1.000	
[8]	-0.087	-0.119	-0.171	0.263	-0.210	-0.264	0.974	1.000
[9]	-0.025	0.119	-0.066	-0.021	0.161	0.151	-0.062	0.014
[10]	1.000							
	-0.032	0.285	-0.031	-0.235	0.357	0.318	-0.143	-0.102
[11]	0.893	1.000						
	-0.039	0.378	0.001	-0.360	0.452	0.404	-0.173	-0.162
[12]	0.670	0.931	1.000					
	0.051	0.447	0.498	-0.302	0.621	0.747	-0.202	-0.210
[13]	0.148	0.324	0.415	1.000				
	0.072	-0.131	-0.345	-0.082	-0.246	-0.370	0.073	0.165
	0.536	0.493	0.400	-0.413	1.000			

ENTER NO. OF 'X' VAR

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	CCMP	20.8462	53.8432	2.0000E 00	2.5600E 02
2	PKG	2.6538	0.8458	2.0000E 00	6.0000E 00
3	NPIN	15.3846	0.9414	1.4000E 01	1.6000E 01
4	SC	7.4231	0.8566	4.0000E 00	9.0000E 00
5	TJ	60.7308	12.3921	4.0000E 01	9.6000E 01
6	HBS	112.5729	214.5164	1.1240E 00	9.2400E 02
7	BFAI	16.7308	30.2993	1.0000E 00	1.4000E 02
8	OBI	0.1650	0.1475	2.0000E-02	5.7000E-01
9	OE	0.3081	0.3096	4.0000E-02	1.3100E 00
10	OE2	0.6008	0.7635	6.0000E-02	2.7900E 00
11	PRED	0.1900	0.1003	1.2000E-01	5.1000E-01
12	LOG	0.0935	0.4218	-8.2701E-01	1.0033E 00

CORR. MATRIX

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CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
	[9]	[10]	[11]	[12]				
[1]	1.000							
[2]	-0.247	1.000						
[3]	0.238	-0.580	1.000					
[4]	-0.802	0.541	-0.458	1.000				
[5]	0.076	-0.055	0.218	-0.128	1.000			
[6]	0.707	-0.155	0.253	-0.414	-0.353	1.000		
[7]	0.533	-0.130	0.187	-0.210	-0.400	0.900	1.000	
[8]	-0.162	-0.133	-0.127	0.097	0.067	-0.151	-0.019	1.000
[9]	-0.145	-0.253	0.031	-0.044	0.284	-0.282	-0.195	0.821
	1.000							
[10]	-0.094	-0.289	0.120	-0.112	0.370	-0.301	-0.257	0.565
	0.933	1.000						
[11]	0.384	-0.014	0.256	-0.140	0.784	0.101	0.074	-0.146
	0.048	0.178	1.000					
[12]	-0.375	-0.234	-0.137	0.135	-0.115	-0.363	-0.198	0.705
	0.009	0.679	-0.410	1.000				

ENTER NO. OF 'X' VARS, THEN INDEX OF 'Y' VAR.
FOLLOWED BY INDICES OF ALL 'X' VARS

=

*

Linears

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	COMP	24.2007	14.6134	3.0000E 00	1.0000E 02
2	PKG	5.4087	2.1041	3.0000E 00	1.2000E 01
3	MPIN	10.5730	4.0089	2.0000E 00	2.4000E 01
4	SC	7.2348	0.8200	3.0000E 00	8.0000E 00
5	APIN	4.1913	4.5154	1.0000E 00	1.0000E 01
6	TJ	55.2176	10.6399	3.5000E 01	8.8000E 01
7	MPS	35.6556	181.0617	1.0000E 00	1.3300E 03
8	MFAI	43.7130	85.9457	1.0000E 00	5.7300E 02
9	OB1	0.5054	0.5263	1.0000E-02	3.0700E 00
10	OE	0.7031	0.6607	3.0000E-02	3.4800E 00
11	OB2	1.0288	0.9418	9.0000E-02	4.6400E 00
12	SPED	0.7797	0.9472	1.2000E-01	9.0400E 00
13	LOG	-0.0529	0.3760	-9.9516E-01	9.4923E-01

CORR. MATRIX

=

CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
	[9]	[10]	[11]	[12]	[13]			
[1]	1.000							
[2]	-0.008	1.000						
[3]	0.271	0.045	1.000					
[4]	-0.057	0.117	-0.153	1.000				
[5]	0.112	-0.037	0.143	-0.679	1.000			
[6]	-0.007	-0.024	0.025	-0.518	0.642	1.000		
[7]	-0.031	-0.127	-0.154	0.051	-0.062	-0.135	1.000	
[8]	-0.026	-0.081	-0.172	0.070	-0.063	-0.094	0.940	1.000
[9]	0.069	0.042	0.103	0.121	-0.011	0.221	-0.045	0.105
[10]	1.000							
	0.083	0.059	0.146	0.027	0.101	0.281	-0.142	-0.012
[11]	0.957	1.000						
	0.094	0.060	0.175	-0.107	0.238	0.337	-0.236	-0.129
[12]	0.795	0.931	1.000					
	0.309	0.068	0.101	-0.031	0.302	0.400	-0.129	-0.096
[13]	0.430	0.473	0.466	1.000				
	-0.339	-0.031	-0.022	-0.034	-0.199	-0.199	0.035	0.102
	0.471	0.474	0.419	-0.314	1.000			

ENTER NO. OF 'X' VARS, THEN I

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	COMP	996.5333	440.9658	1.0700E 02	2.0000E 03
2	PKG	3.6000	2.2928	1.0000E 00	8.0000E 00
3	NPIN	16.6667	5.9362	8.0000E 00	2.8000E 01
4	SC	5.8667	2.0307	2.0000E 00	8.0000E 00
5	APEN	5.9333	3.9182	1.0000E 00	1.2000E 01
6	TJ	58.0667	17.8384	3.3000E 01	9.9000E 01
7	HRS	56.8983	128.1617	3.9000E-01	4.9615E 02
8	#FAI	22.7333	35.8279	1.0000E 00	1.1400E 02
9	OS1	0.6793	1.2705	2.0000E-02	3.9400E 00
10	OS	1.5213	2.1852	1.0000E-01	7.6900E 00
11	OS2	2.7293	3.9379	2.1000E-01	1.4100E 01
12	FREQ	0.6240	0.7687	8.0000E-02	3.2500E 00
13	LOG	0.2379	0.3590	-3.2331E-01	1.1292E 00

CORR. MATRIX

CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]
[1]	1.000												
[2]	0.038	1.000											
[3]	-0.463	0.126	1.000										
[4]	0.482	0.202	-0.208	1.000									
[5]	-0.532	0.132	0.653	-0.450	1.000								
[6]	-0.394	0.104	0.487	-0.067	0.855	1.000							
[7]	0.114	-0.298	-0.186	0.251	-0.296	-0.230	1.000						
[8]	0.572	-0.023	-0.190	0.474	-0.303	-0.230	0.692	1.000					
[9]	0.211	0.558	0.183	0.371	0.101	0.350	-0.199	0.004	1.000				
[10]	0.034	0.307	0.280	0.227	0.394	0.542	-0.244	-0.145	0.959	1.000			
[11]	-0.119	0.439	0.383	0.078	0.566	0.680	-0.273	-0.240	0.855	0.966	1.000		
[12]	0.140	0.265	0.027	0.356	0.300	0.672	-0.124	0.009	0.707	0.784	0.782	1.000	
[13]	-0.104	0.433	0.511	-0.228	0.381	0.245	-0.501	-0.307	0.502	0.606	0.607	0.069	1.000

ENTER NO. OF "X" VARS, THEN INDEX OF "Y"
*

VAR	LABEL	MEAN	STD-DEV	MIN	MAX
1	COMP	2969.2222	165.5132	3.5000E 02	6.2500E 03
2	PEG	3.5000	2.7062	1.0000E 00	8.0000E 00
3	NPIN	26.7778	11.2749	1.6000E 01	4.0000E 01
4	SC	7.1111	1.1313	3.0000E 00	8.0000E 00
5	APEX	3.8889	0.4714	3.0000E 00	5.0000E 00
6	TJ	53.1111	5.9199	3.9000E 01	6.0000E 01
7	HRS	63.7262	209.4909	2.4400E-01	9.0000E 02
8	FFAI	25.7222	31.4651	1.0000E 00	3.5100E 02
9	GE1	0.5217	0.7648	2.0000E-02	3.3800E 00
10	GB	1.0189	1.8373	1.0000E-01	8.2000E 00
11	GB2	1.9811	3.9793	1.5000E-01	1.7500E 01
12	PRED	1.2333	0.7624	1.5000E-01	2.8500E 00
13	LOG	-0.2876	0.4506	-1.1326E 00	8.9679E-01

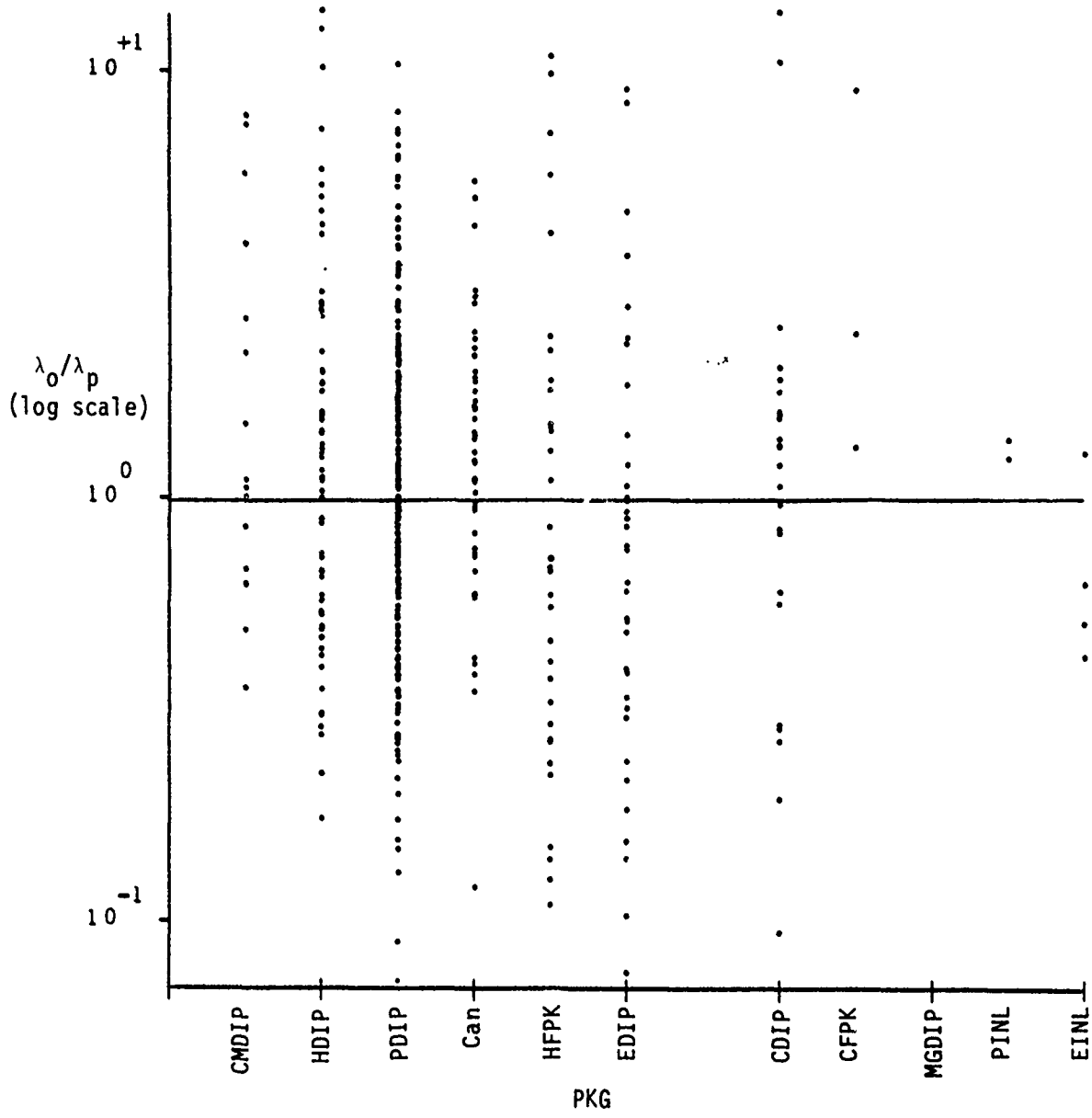
CORR. MATRIX
*

CORRELATION MATRIX

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]
[1]	1.000								
[2]	0.556	1.000							
[3]	-0.259	-0.468	1.000						
[4]	0.273	0.230	0.233	1.000					
[5]	-0.400	-0.692	0.216	-0.416	1.000				
[6]	0.128	-0.114	0.621	0.507	-0.206	1.000			
[7]	0.150	-0.133	-0.143	-0.023	0.057	-0.191	1.000		
[8]	0.176	-0.128	-0.120	-0.019	0.034	-0.137	0.996	1.000	
[9]	0.032	-0.214	0.370	0.077	-0.017	0.425	-0.065	-0.044	1.000
[10]	0.067	-0.216	0.390	0.057	0.037	0.397	-0.108	-0.094	0.975
[11]	0.098	-0.207	0.403	0.053	0.061	0.380	-0.123	-0.114	0.939
[12]	0.652	0.565	-0.112	0.363	-0.190	0.361	-0.106	-0.089	-0.019
[13]	-0.237	-0.522	0.552	-0.216	0.222	0.335	-0.004	-0.052	0.778

	[10]	[11]	[12]	[13]
[10]	1.000			
[11]	0.992	1.000		
[12]	0.004	0.023	1.000	
[13]	0.740	0.702	-0.410	1.000

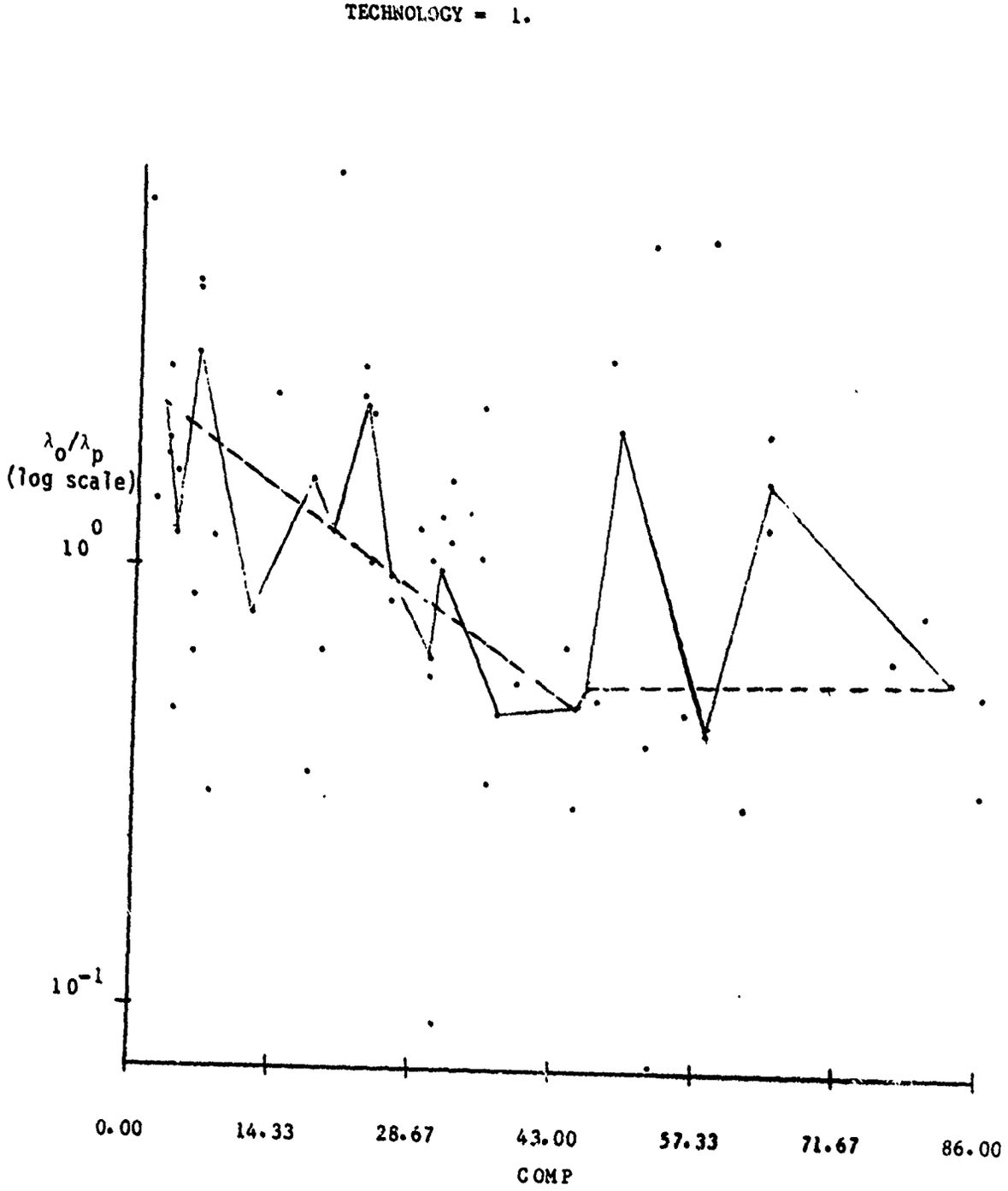
ENTER NO. OF 'X' VARS, THEN INDEX OF 'Y' VAR
*



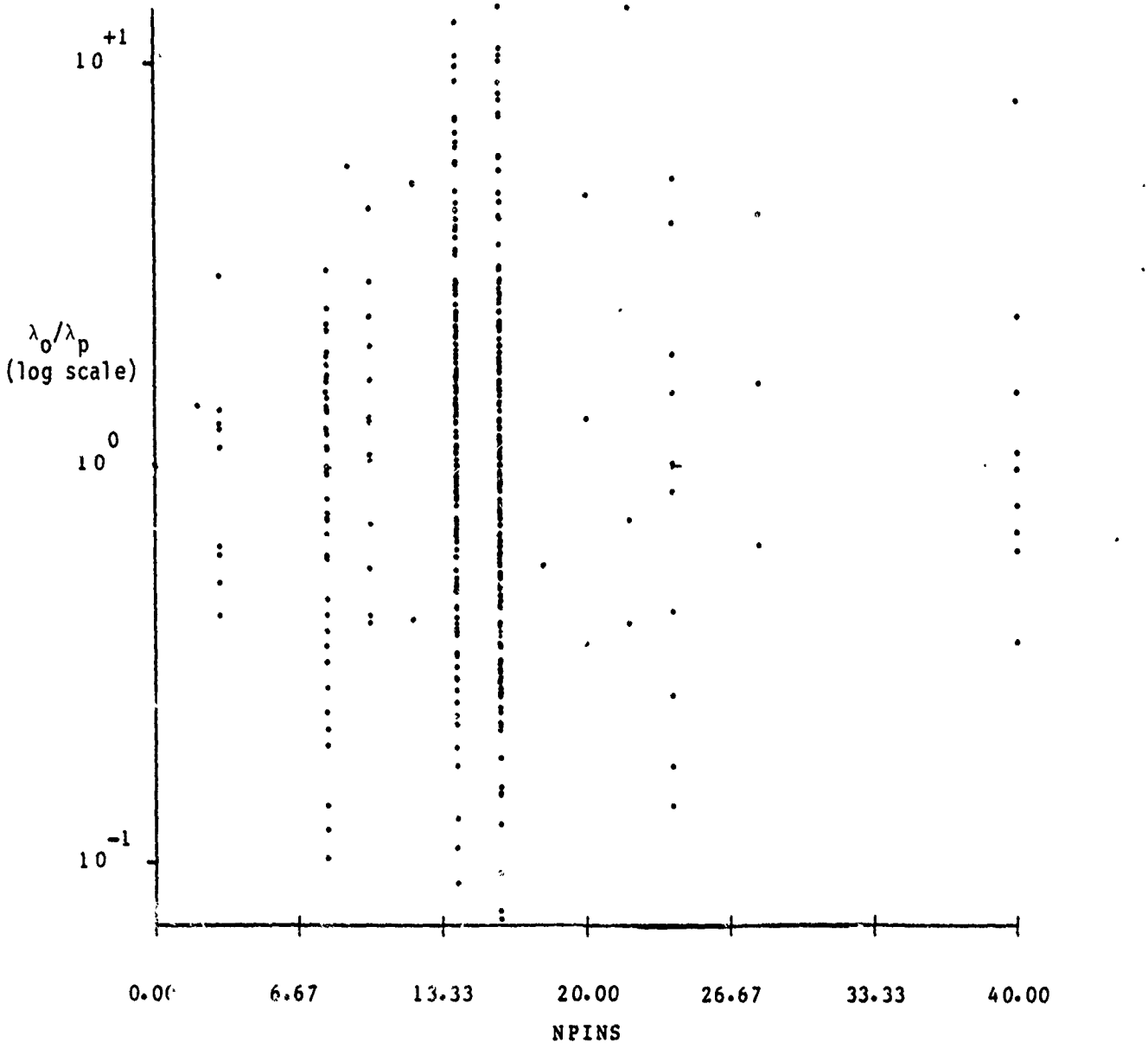
RATIO PLOT #1: PACKAGE

APPENDIX C

RATIO PLOTS

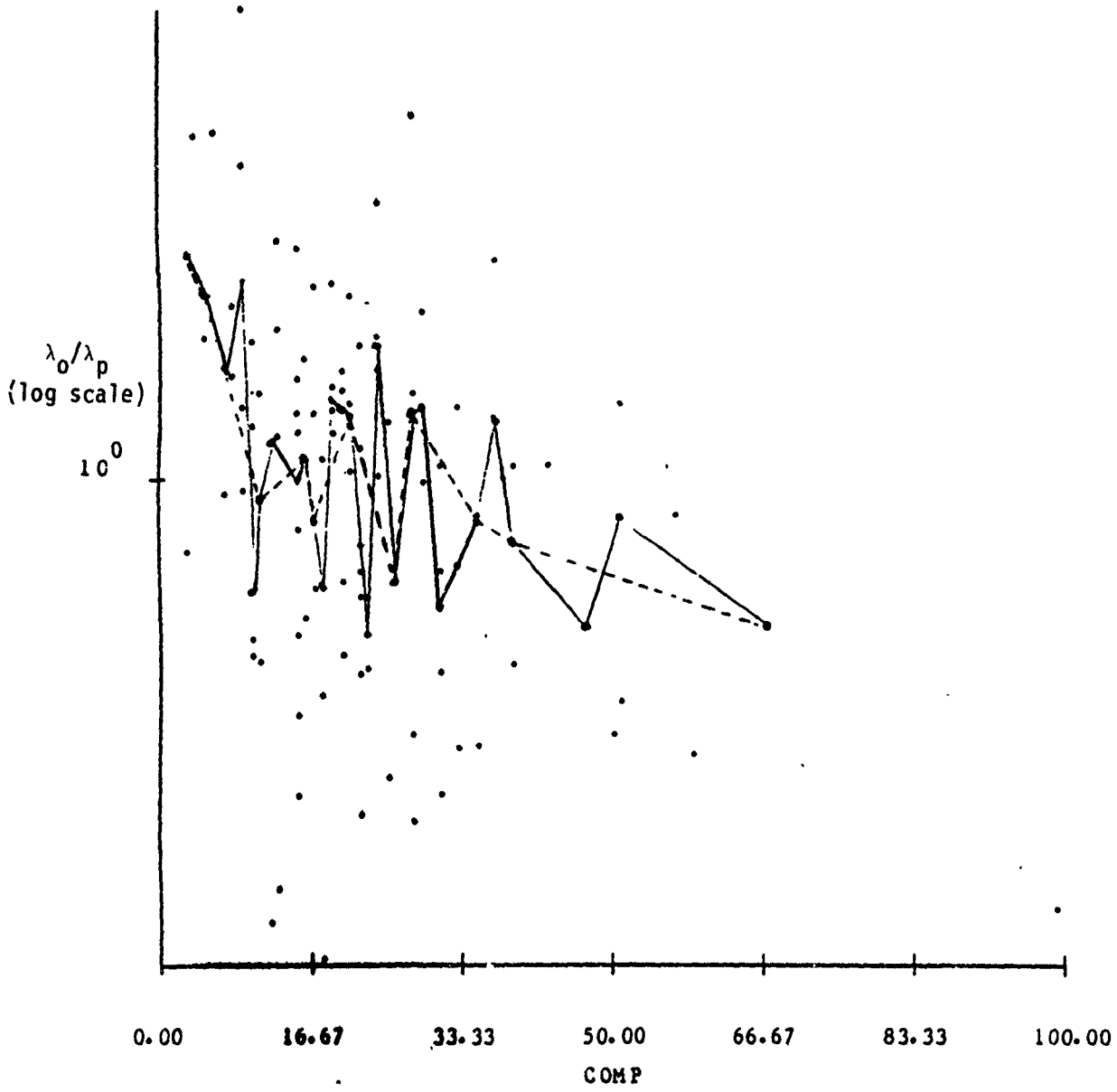


RATIO PLOT #3: CMOS DATA ON COMPLEXITY

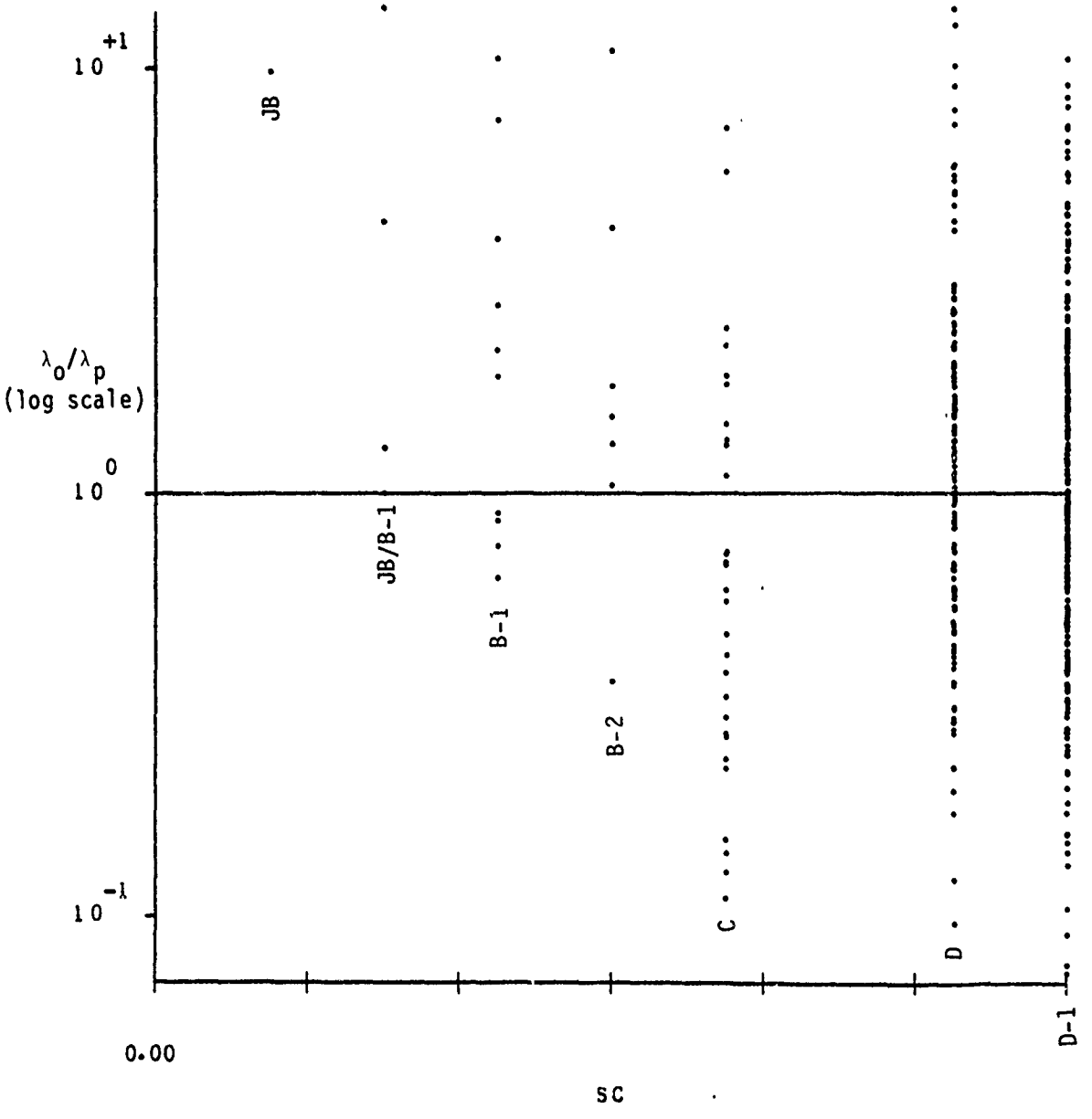


RATIO PLOT #2: NUMBER OF PINS

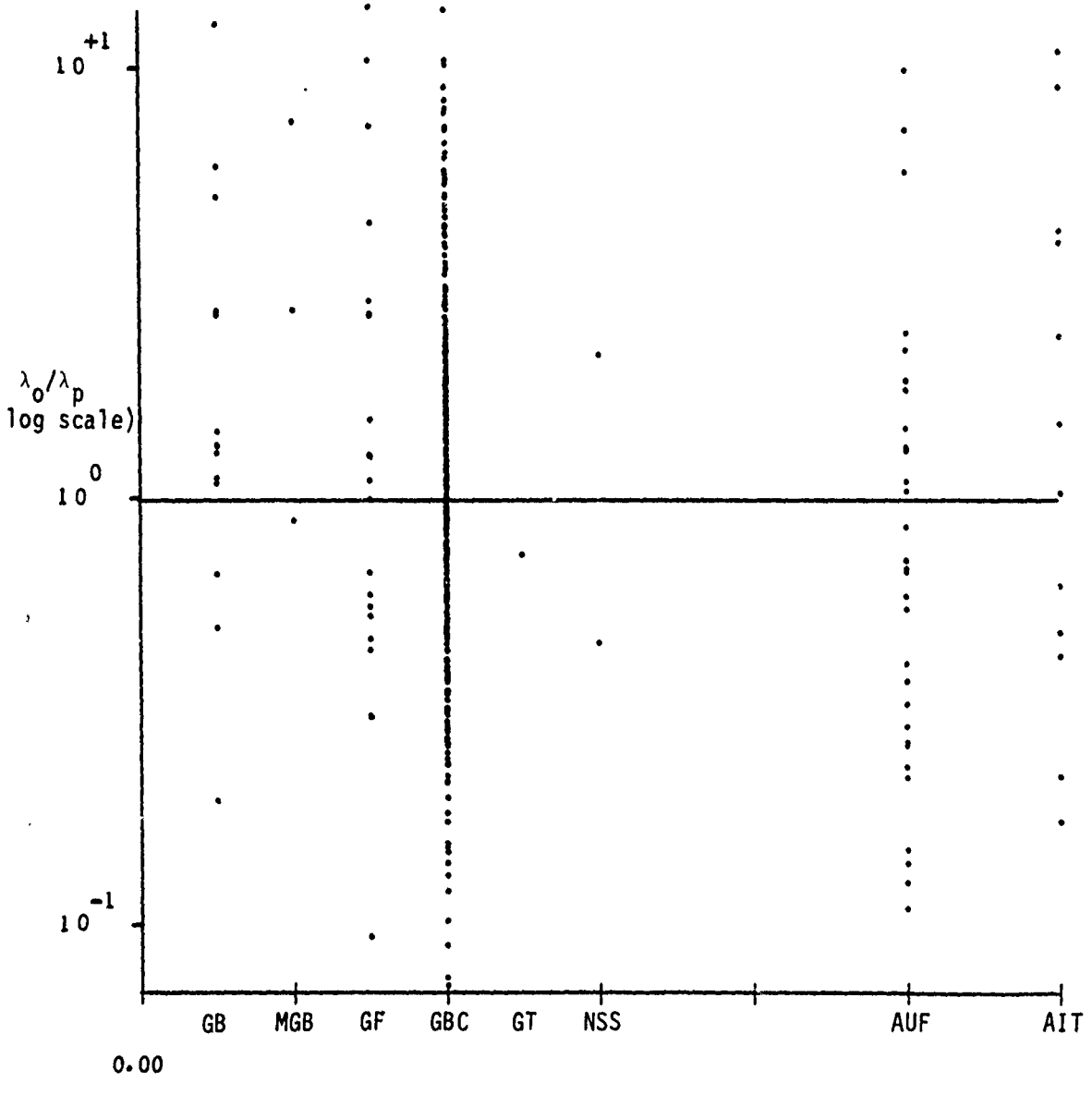
TECHNOLOGY = 8.



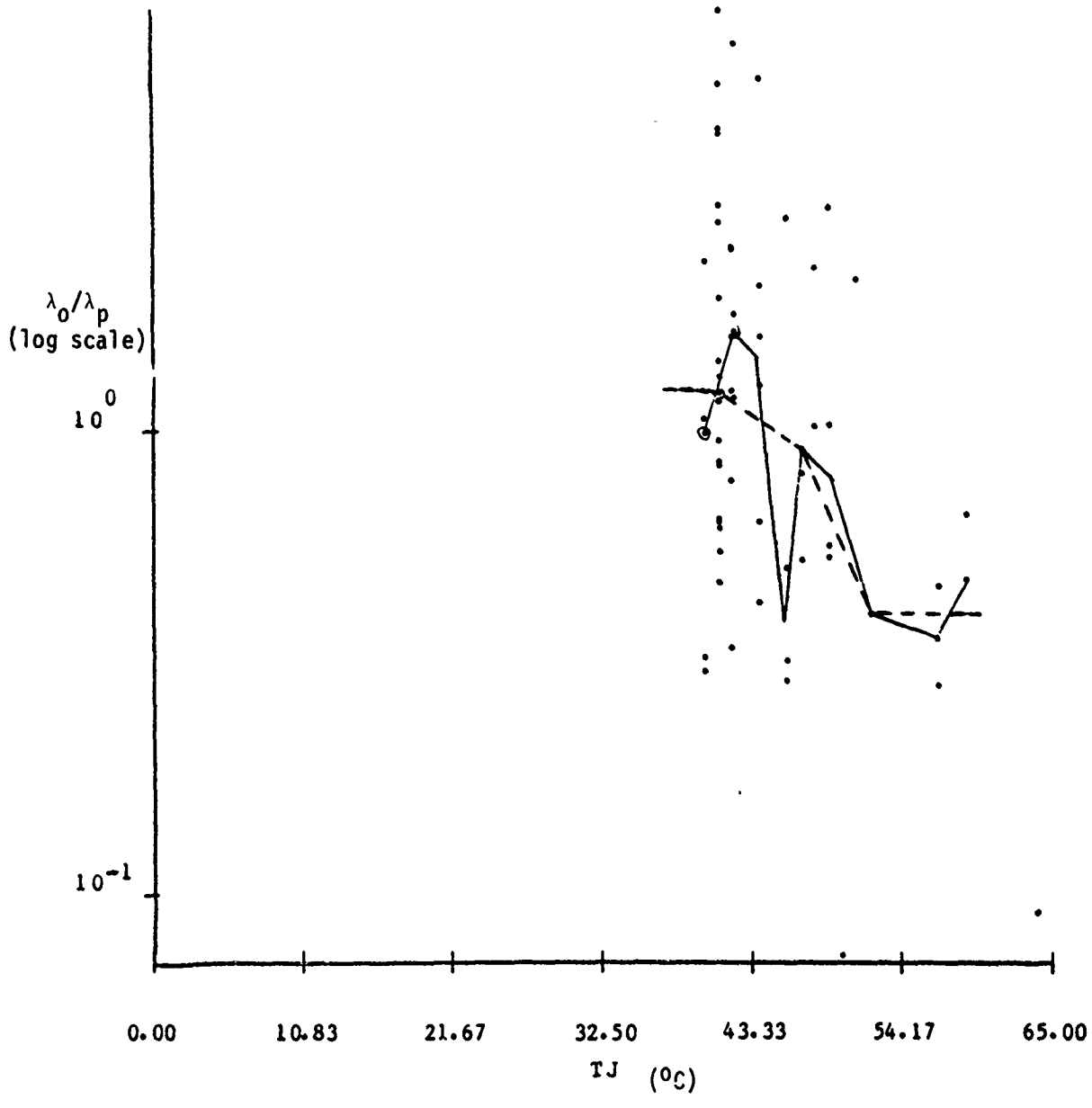
RATIO PLOT #4: LINEAR DEVICE DATA ON COMPLEXITY



RATIO PLOT #5: SCREEN CLASS

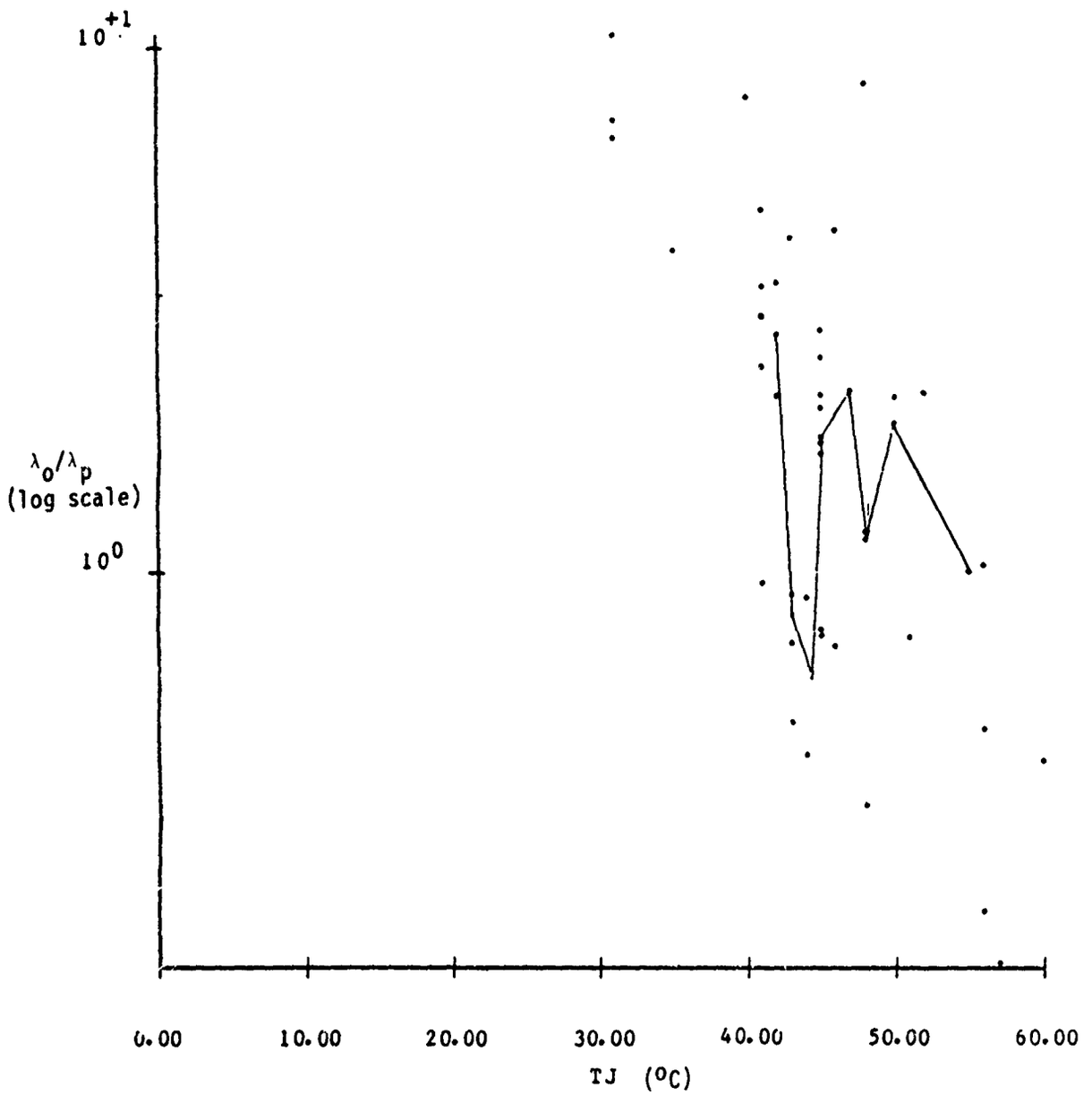


RATIO PLOT #6: APPLICATION ENVIRONMENT



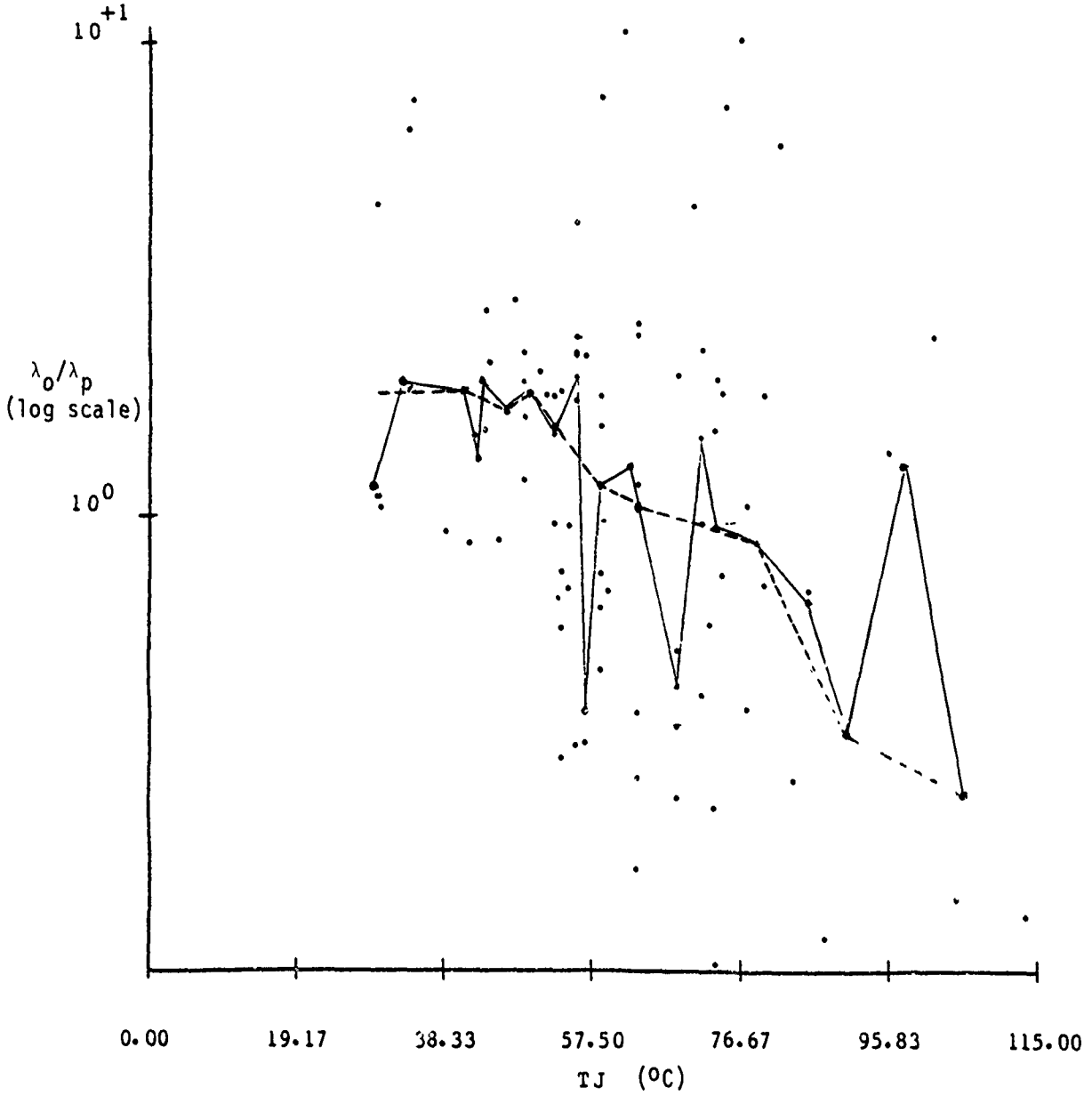
RATIO PLOT #7: CMOS DATA ON JUNCTION TEMPERATURE

TECHNOLOGY = 5.



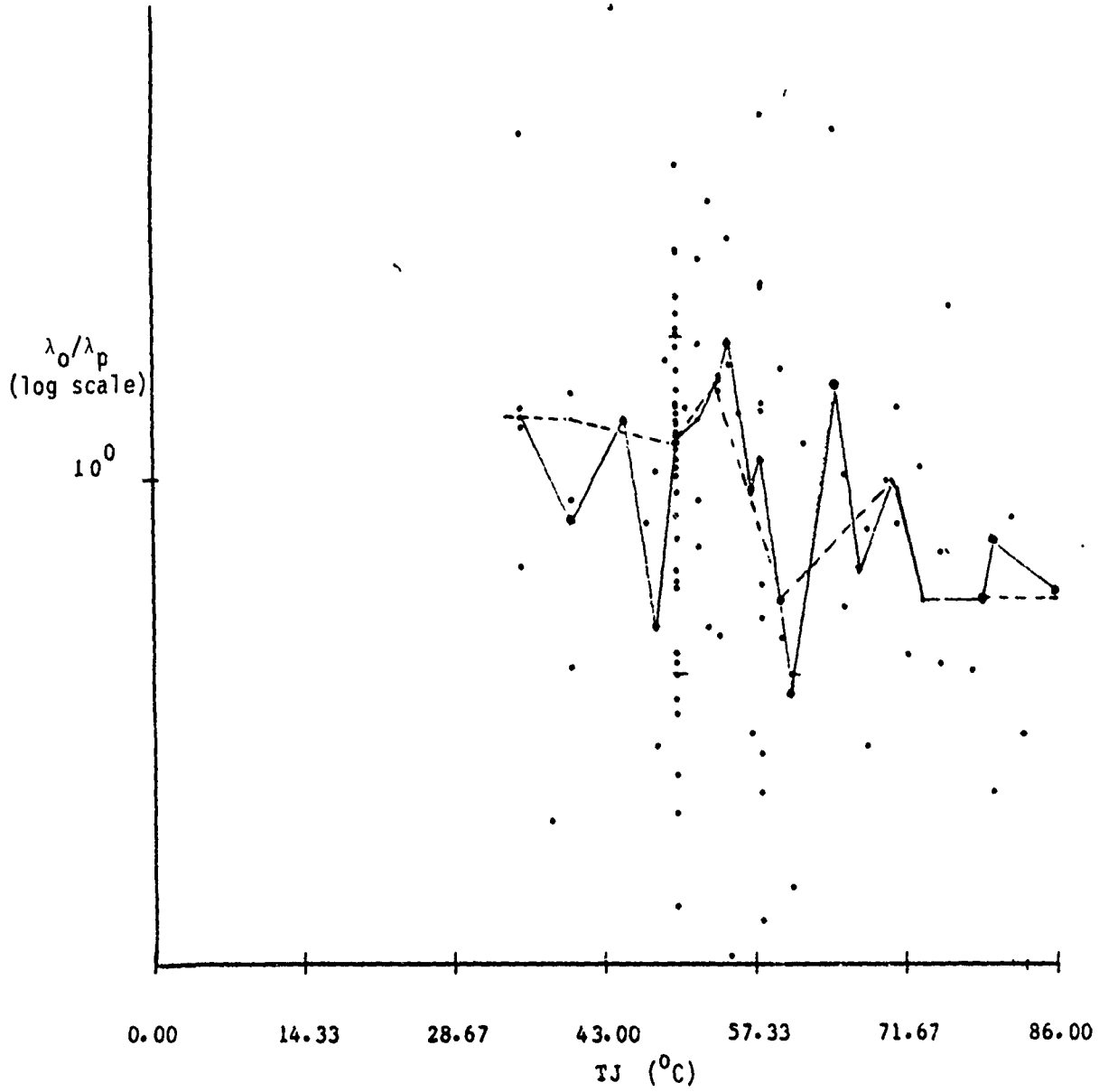
RATIO PLOT #8: LTTL DATA ON JUNCTION TEMPERATURE

TECHNOLOGY = 6.

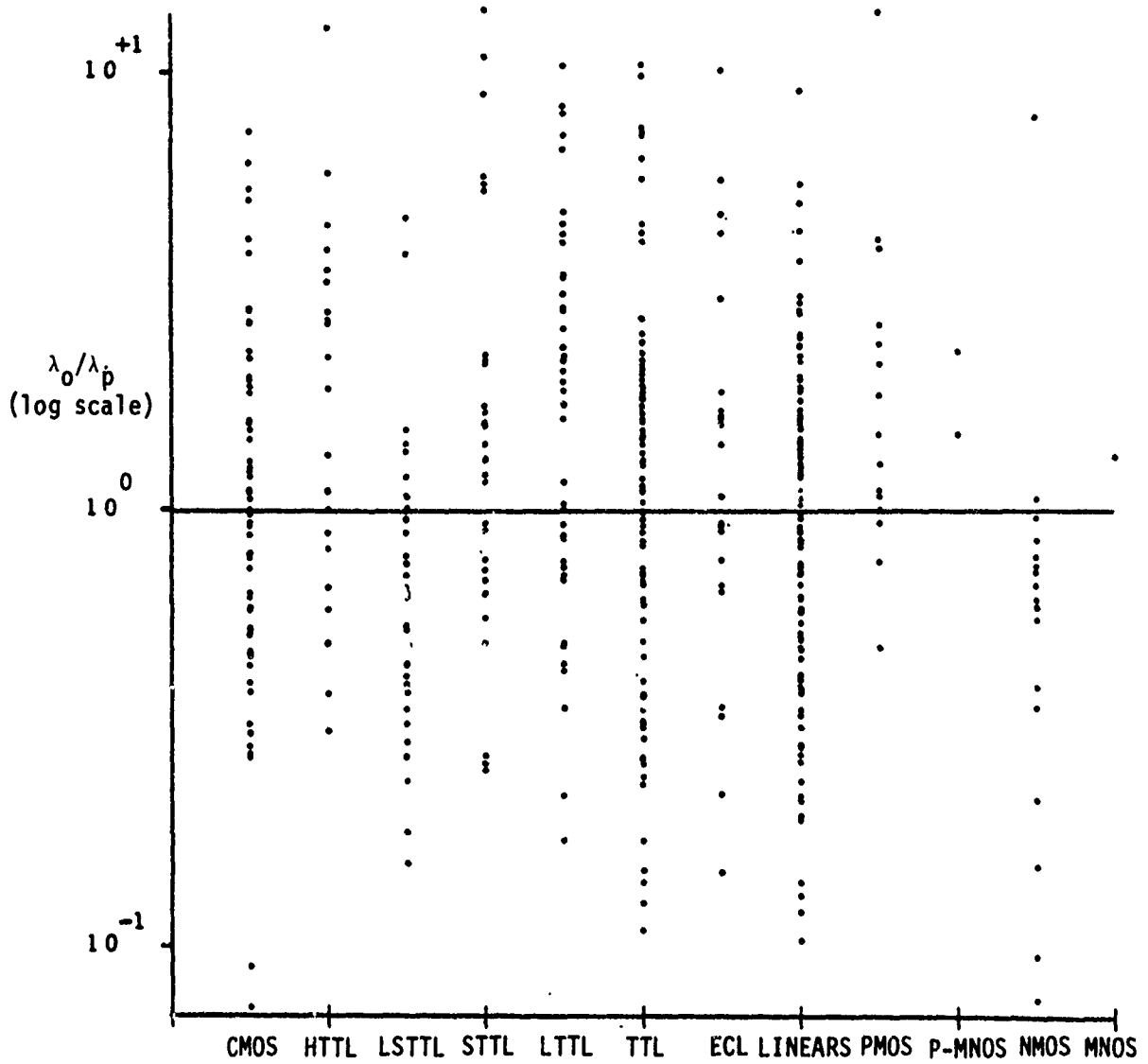


RATIO PLOT #9: TTL DATA ON JUNCTION TEMPERATURE

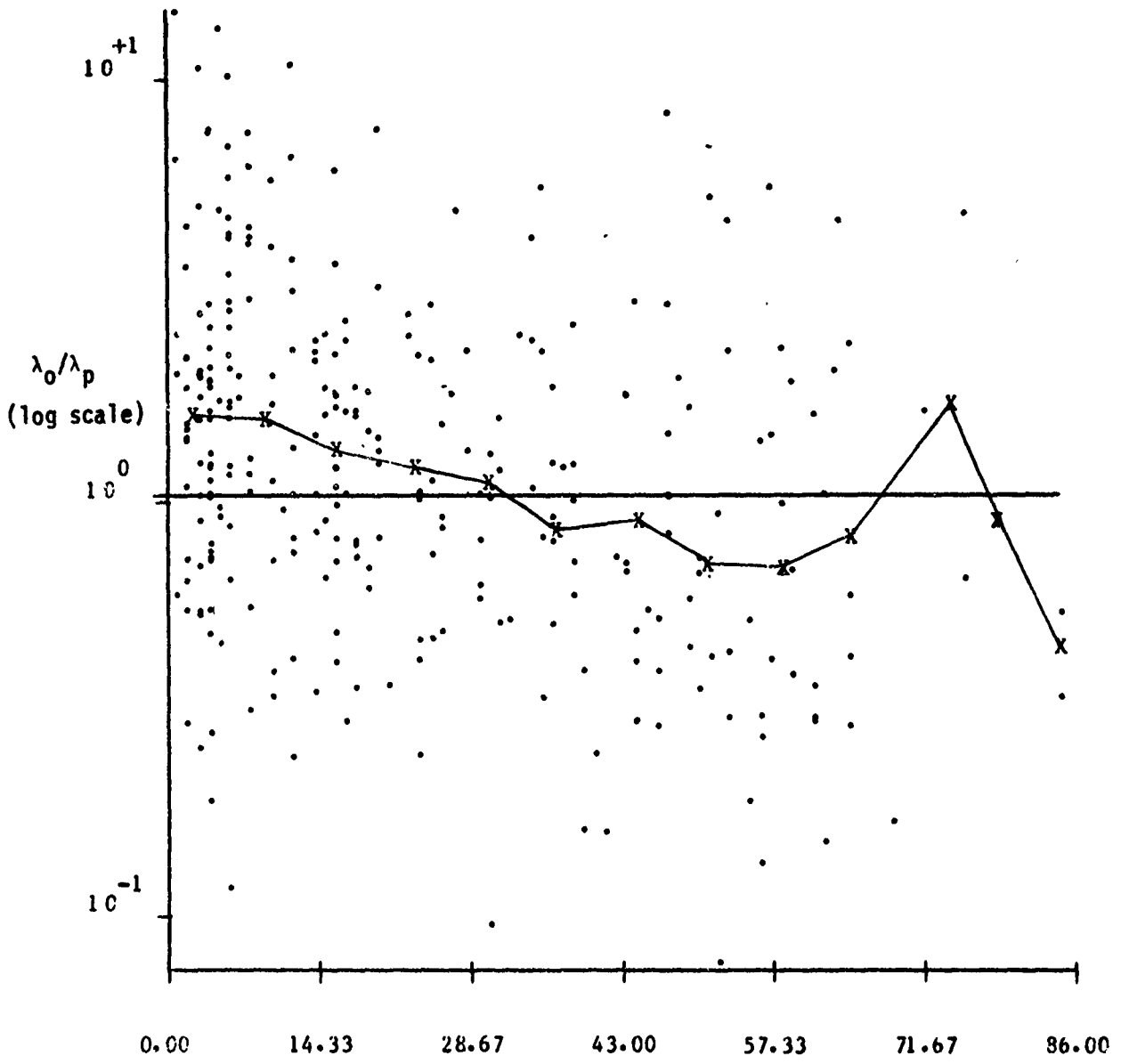
TECHNOLOGY = 8.



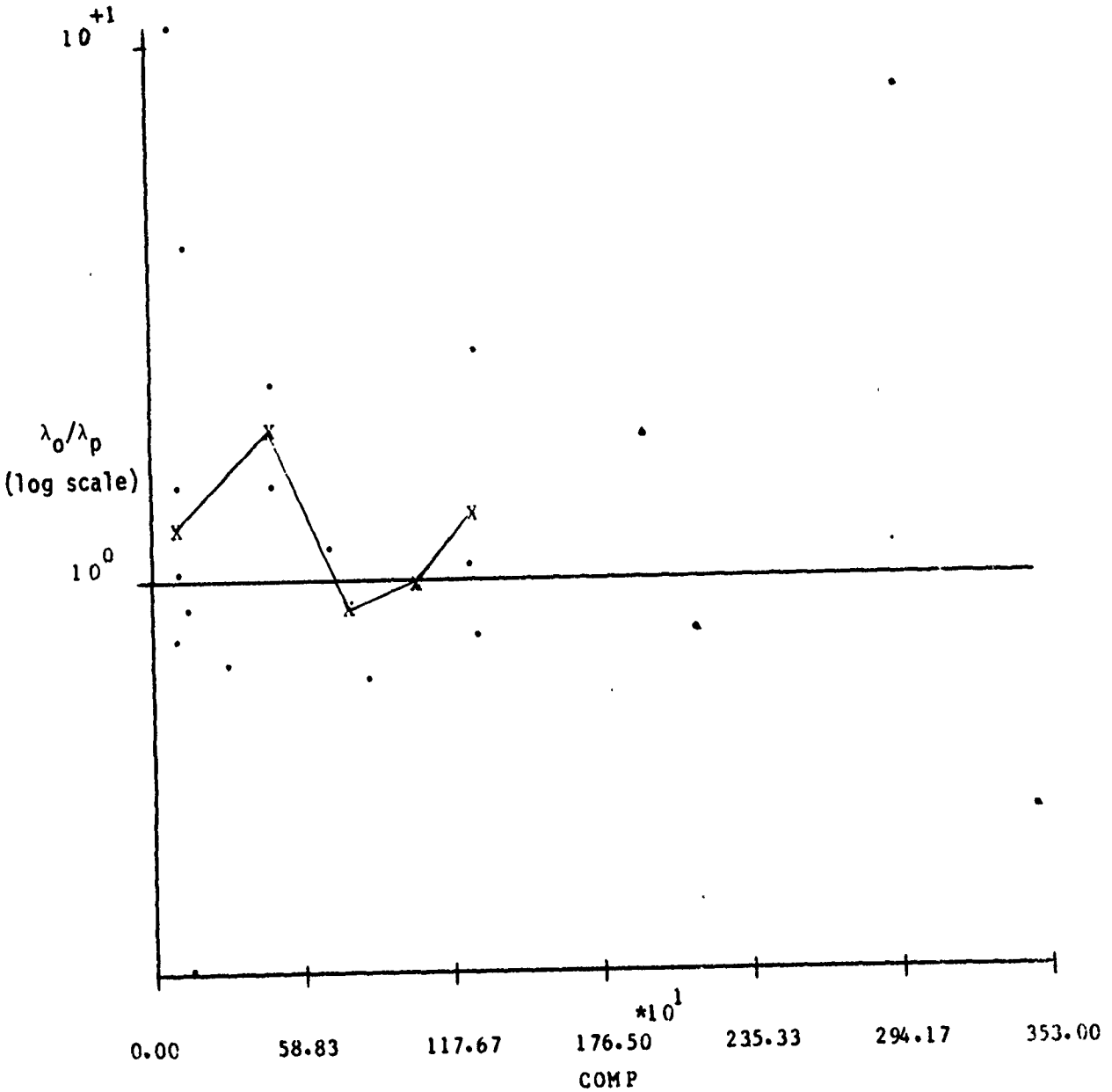
RATIO PLOT #10: LINEAR DEVICE DATA ON JUNCTION TEMPERATURE



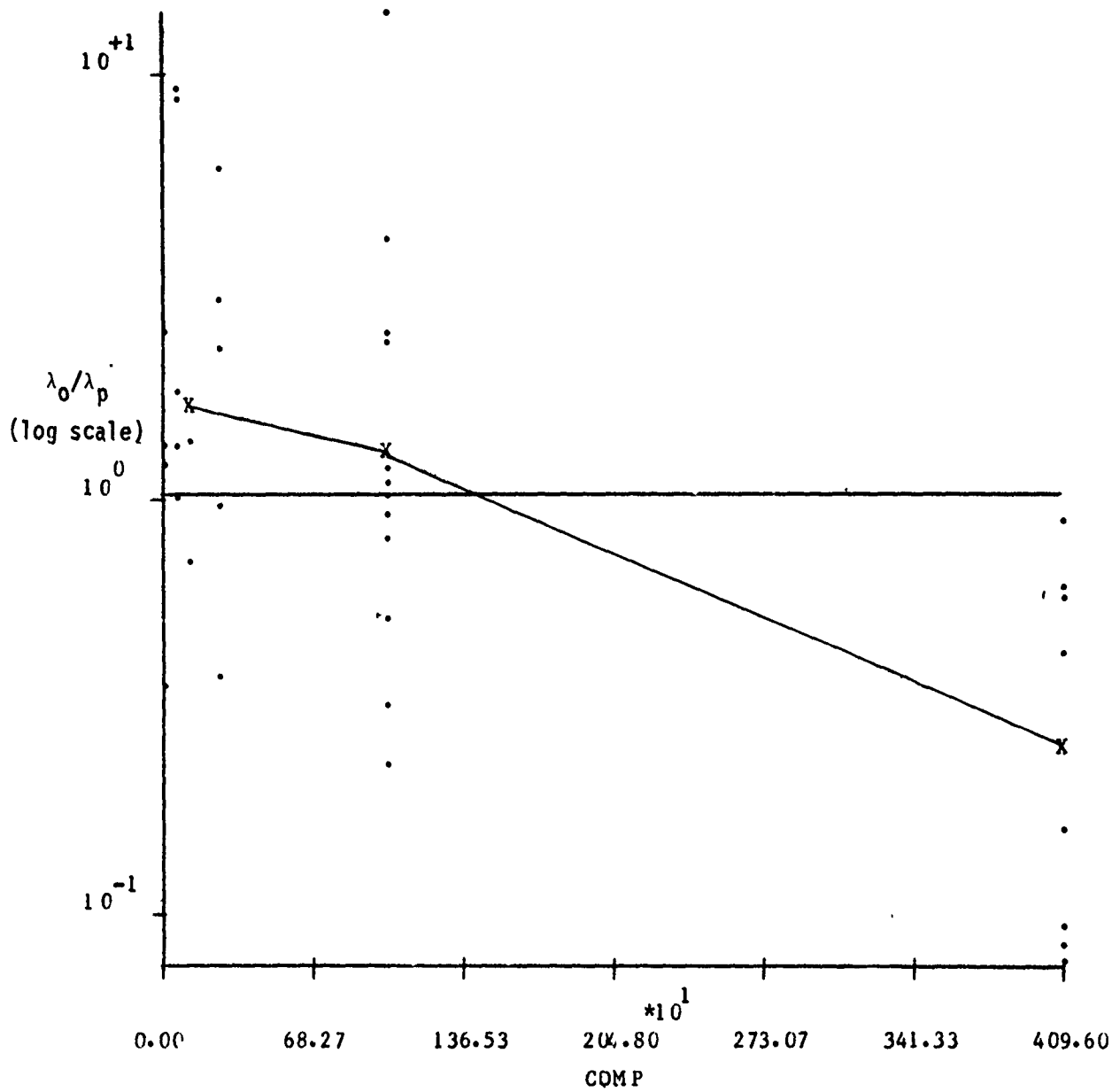
RATIO PLOT #11: TECHNOLOGY



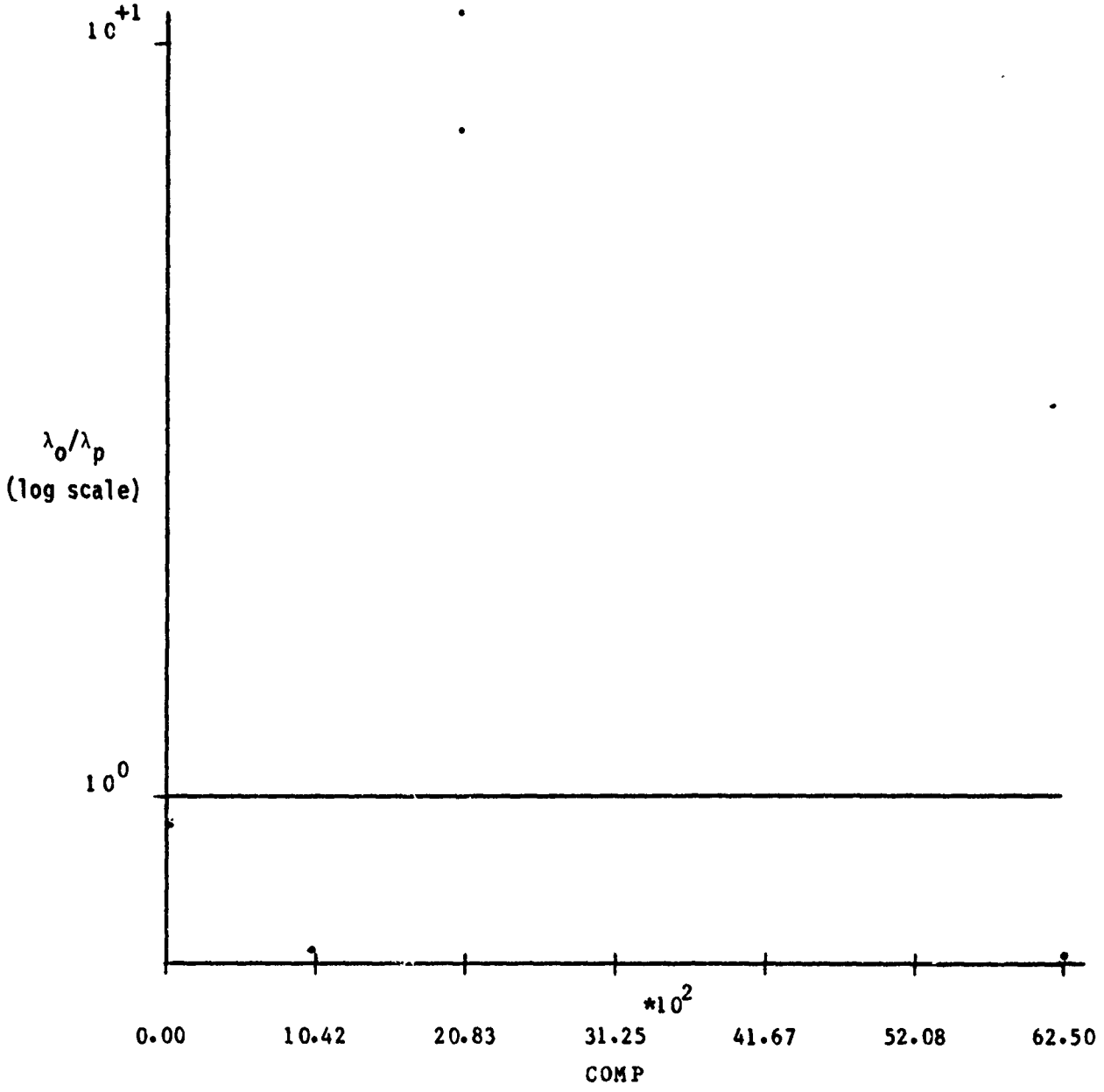
RATIO PLOT # 12: SSI/MSI MODEL



RATIO PLOT #13: LSI/MICROPROCESSOR MODEL



RATIO PLOT #14: RAM MODEL



RATIO PLOT #15: ROM/PROM MODEL

APPENDIX D

MIL-HDBK-217C, PART III UPDATE

TABLE 3-1 GENERIC FAILURE RATE, λ_G, FOR DIGITAL DEVICES IN HERMETIC PACKAGES vs. ENVIRONMENT (F./10^6 Hours)

DEVICE DESCRIPTION		APPLICATION ENVIRONMENT									
GATE COMPLEXITY	TECHNOLOGY	G_B or S_F	G_F	A_{IF}	G_M	M_S	A_{UI}	M_U	A_{IF}	A_{UF}	M_L
1-20	Bipolar	0.0064	0.016	0.022	0.025	0.026	0.029	0.035	0.041	0.050	0.057
	MOS	0.0065	0.018	0.025	0.028	0.030	0.038	0.048	0.044	0.059	0.060
21-50	Bipolar	0.0087	0.022	0.030	0.034	0.035	0.041	0.050	0.054	0.067	0.074
	MOS	0.0081	0.023	0.032	0.035	0.039	0.049	0.063	0.055	0.075	0.074
51-100	Bipolar	0.012	0.027	0.037	0.041	0.043	0.051	0.063	0.063	0.081	0.093
	MOS	0.011	0.032	0.044	0.048	0.054	0.072	0.093	0.070	0.10	0.093
101-500	Bipolar	0.024	0.060	0.078	0.084	0.096	0.12	0.15	0.12	0.16	0.15
	MOS	0.019	0.058	0.080	0.086	0.099	0.14	0.18	0.12	0.18	0.15
501-1000	Bipolar	0.037	0.090	0.12	0.13	0.14	0.19	0.23	0.17	0.24	0.21
	MOS	0.030	0.092	0.12	0.13	0.16	0.23	0.30	0.17	0.28	0.21
1001-2000	Bipolar	0.062	0.16	0.20	0.21	0.23	0.30	0.37	0.27	0.39	0.33
	MOS	0.049	0.15	0.20	0.21	0.25	0.38	0.48	0.27	0.45	0.33
2001-3000	Bipolar	0.085	0.21	0.26	0.27	0.31	0.42	0.50	0.33	0.60	0.40
	MOS	0.070	0.21	0.28	0.29	0.36	0.54	0.66	0.35	0.62	0.41
3001-5000	Bipolar	0.12	0.29	0.37	0.38	0.44	0.59	0.71	0.44	0.68	0.50
	MOS	0.10	0.30	0.41	0.42	0.51	0.79	1.0	0.47	0.87	0.53
5001-7500	Bipolar	0.18	0.42	0.51	0.53	0.62	0.84	1.0	0.59	0.92	0.66
	MOS	0.15	0.45	0.58	0.59	0.74	1.2	1.4	0.65	1.2	0.71
7501-10000	Bipolar	0.28	0.60	0.75	0.76	0.88	1.2	1.4	0.87	1.3	0.98
	MOS	0.23	0.66	0.87	0.88	1.1	1.6	2.1	0.99	1.8	1.1
10001-15000	Bipolar	0.39	0.85	1.0	1.0	1.2	1.6	1.9	1.2	1.8	1.3
	MOS	0.33	0.95	1.2	1.2	1.6	2.3	2.9	1.3	2.5	1.4
15001-20000	Bipolar	0.53	1.1	1.4	1.4	1.6	2.2	2.6	1.5	2.4	1.6
	MOS	0.48	1.3	1.7	1.8	2.1	3.3	4.2	1.9	3.4	2.0

TABLE 3-2 GENERIC FAILURE RATE, λ_G, FOR DIGITAL DEVICES IN NONHERMETIC PACKAGES vs. ENVIRONMENT (F./10^6 Hours)

DEVICE DESCRIPTION		APPLICATION ENVIRONMENT									
GATE COMPLEXITY	TECHNOLOGY	G_B or S_F	G_F	A_{IT}	G_M	N_S	A_{UT}	N_U	A_{IF}	A_{UF}	N_L
1-20	Bipolar	0.0068	0.018	0.026	0.027	0.029	0.032	0.040	0.044	0.055	0.061
	MOS	0.0072	0.024	0.035	0.038	0.045	0.072	0.10	0.055	0.094	0.071
21-50	Bipolar	0.0091	0.024	0.033	0.037	0.039	0.046	0.057	0.058	0.074	0.079
	MOS	0.0091	0.031	0.046	0.049	0.060	0.098	0.14	0.069	0.12	0.089
51-100	Bipolar	0.013	0.034	0.047	0.051	0.055	0.069	0.087	0.075	0.10	0.099
	MOS	0.013	0.049	0.071	0.075	0.097	0.17	0.24	0.10	0.20	0.12
101-500	Bipolar	0.025	0.070	0.091	0.096	0.11	0.15	0.18	0.13	0.20	0.17
	MOS	0.025	0.10	0.15	0.16	0.21	0.39	0.57	0.19	0.43	0.22
501-1000	Bipolar	0.041	0.11	0.15	0.15	0.18	0.24	0.30	0.20	0.30	0.24
	MOS	0.043	0.20	0.28	0.29	0.40	0.78	1.1	0.33	0.83	0.37
1001-2000	Bipolar	0.072	0.19	0.24	0.26	0.30	0.41	0.50	0.32	0.50	0.39
	MOS	0.080	0.36	0.53	0.54	0.71	1.4	2.0	0.60	1.5	0.66
2001-3000	Bipolar	0.10	0.27	0.34	0.35	0.41	0.58	0.72	0.42	0.67	0.49
	MOS	0.13	0.60	0.83	0.84	1.2	2.3	3.1	0.90	2.4	0.96
3001-5000	Bipolar	0.16	0.40	0.49	0.51	0.61	0.87	1.1	0.57	0.96	0.64
	MOS	0.22	0.97	1.4	1.5	2.0	3.8	5.2	1.5	3.8	1.6
5001-7500	Bipolar	0.23	0.57	0.72	0.74	0.88	1.3	1.6	0.80	1.4	0.87
	MOS	0.38	1.7	2.3	2.3	3.3	6.1	8.3	2.4	6.2	2.4
7501-10000	Bipolar	0.35	0.85	1.1	1.1	1.3	1.8	2.1	1.2	2.0	1.3
	MOS	0.61	2.6	3.7	3.7	5.0	9.4	13.	3.8	9.6	4.0
10001-15000	Bipolar	0.52	1.2	1.5	1.5	1.8	2.5	3.1	1.6	2.7	1.8
	MOS	1.1	4.3	5.8	5.8	8.0	15.	20.	5.9	15.	6.0
15001-20000	Bipolar	0.75	1.7	2.1	2.1	2.5	3.6	4.3	2.2	3.7	2.3
	MOS	1.7	6.6	9.1	9.1	12.	22.	31.	9.2	23.	9.4

TABLE 3-3 GENERIC FAILURE RATE, λ_G, FOR READ ONLY MEMORY (ROM)
DEVICES IN HERMETIC PACKAGES vs. ENVIRONMENT (F./10^6 Hours)

DEVICE DESCRIPTION		APPLICATION ENVIRONMENT									
BIT COMPLEXITY	TECHNOLOGY	G_B S_F	G_F	A_{IT}	G_M	N_S	A_{UT}	N_U	A_{IF}	A_{UF}	N_L
1-320	Bipolar	0.0079	0.020	0.028	0.031	0.032	0.037	0.045	0.049	0.062	0.068
	MOS	0.0091	0.027	0.038	0.041	0.046	0.063	0.081	0.060	0.089	0.080
321-576	Bipolar	0.0086	0.022	0.030	0.033	0.035	0.041	0.051	0.052	0.066	0.071
	MOS	0.010	0.031	0.044	0.047	0.054	0.076	0.098	0.067	0.10	0.096
577-1120	Bipolar	0.011	0.029	0.039	0.042	0.045	0.054	0.067	0.065	0.084	0.087
	MOS	0.015	0.047	0.064	0.068	0.082	0.12	0.15	0.091	0.15	0.11
1121-2240	Bipolar	0.017	0.044	0.058	0.064	0.070	0.082	0.10	0.096	0.13	0.13
	MOS	0.021	0.073	0.090	0.096	0.11	0.16	0.21	0.13	0.18	0.16
2241-5000	Bipolar	0.022	0.054	0.074	0.079	0.086	0.11	0.13	0.11	0.15	0.15
	MOS	0.029	0.095	0.13	0.14	0.17	0.25	0.33	0.17	0.30	0.21
5001-11000	Bipolar	0.033	0.075	0.095	0.10	0.11	0.14	0.18	0.13	0.19	0.17
	MOS	0.046	0.15	0.20	0.21	0.26	0.41	0.53	0.25	0.46	0.28
11001-17000	Bipolar	0.042	0.10	0.13	0.13	0.16	0.20	0.25	0.17	0.25	0.21
	MOS	0.058	0.20	0.26	0.27	0.33	0.54	0.70	0.31	0.59	0.35
17001-30000	Bipolar	0.063	0.15	0.19	0.20	0.23	0.30	0.36	0.24	0.36	0.28
	MOS	0.10	0.33	0.44	0.44	0.56	0.91	1.2	0.49	0.98	0.54
30001-74000	Bipolar	0.093	0.22	0.27	0.28	0.33	0.44	0.52	0.33	0.60	0.37
	MOS	0.18	0.55	0.73	0.74	0.95	1.5	2.0	0.79	1.6	0.85

TABLE 3-4 GENERIC FAILURE RATE, λ_G, FOR READ ONLY MEMORY (ROM) DEVICES IN NONHERMETIC PACKAGES vs. ENVIRONMENT (F./10^6 Hours)

DEVICE DESCRIPTION		APPLICATION ENVIRONMENT									
BIT COMPLEXITY	TECHNOLOGY	G_B & S_F	G_F	A_{IF}	C_M	N_S	A_{UF}	N_U	A_{IF}	A_{UF}	N_L
1-320	Bipolar	0.006	0.022	0.030	0.033	0.036	0.042	0.052	0.063	0.068	0.072
	MOS	0.010	0.039	0.059	0.062	0.079	0.14	0.20	0.082	0.17	0.10
321-576	Bipolar	0.0092	0.024	0.033	0.036	0.039	0.047	0.059	0.056	0.074	0.076
	MOS	0.012	0.046	0.070	0.074	0.096	0.18	0.26	0.094	0.20	0.11
577-1120	Bipolar	0.012	0.032	0.044	0.047	0.051	0.064	0.081	0.070	0.096	0.093
	MOS	0.018	0.082	0.12	0.12	0.17	0.33	0.45	0.15	0.36	0.17
1121-2240	Bipolar	0.019	0.049	0.065	0.070	0.079	0.099	0.12	0.10	0.14	0.14
	MOS	0.025	0.11	0.16	0.17	0.23	0.42	0.62	0.20	0.49	0.24
2241-5000	Bipolar	0.024	0.063	0.085	0.090	0.10	0.13	0.17	0.12	0.18	0.16
	MOS	0.041	0.19	0.29	0.29	0.40	0.79	1.2	0.33	0.83	0.36
5001-11000	Bipolar	0.034	0.089	0.12	0.12	0.14	0.19	0.23	0.16	0.24	0.19
	MOS	0.076	0.37	0.53	0.54	0.77	1.5	2.1	0.58	1.6	0.62
11001-17000	Bipolar	0.050	0.13	0.17	0.17	0.20	0.28	0.34	0.21	0.33	0.24
	MOS	0.097	0.48	0.70	0.70	1.0	2.1	2.8	0.75	2.1	0.80
17001-38000	Bipolar	0.079	0.20	0.25	0.26	0.31	0.43	0.53	0.30	0.49	0.34
	MOS	0.19	0.91	1.4	1.4	1.9	3.8	5.4	1.4	3.8	1.5
38001-74000	Bipolar	0.12	0.30	0.38	0.39	0.46	0.65	0.79	0.43	0.71	0.48
	MOS	0.38	1.8	2.5	2.5	3.7	7.2	9.7	2.5	7.2	2.6

TABLE 3-5 GENERIC FAILURE RATE, λ_G, FOR RANDOM ACCESS MEMORY (RAM) DEVICES IN HERMETIC PACKAGES vs. ENVIRONMENT (F./10^6 Hours)

DEVICE DESCRIPTION		APPLICATION ENVIRONMENT									
BIT COMPLEXITY	TECHNOLOGY	G_B&S_F	G_F	A_{IT}	G_U	N_S	A_{UT}	N_U	A_{IF}	A_{UF}	N_L
1-320	Bipolar	0.023	0.059	0.076	0.080	0.092	0.13	0.16	0.10	0.16	0.12
	MOS Dynamic	0.011	0.035	0.047	0.050	0.059	0.083	0.11	0.070	0.11	0.090
	MOS Static	0.016	0.053	0.073	0.076	0.92	0.14	0.18	0.097	0.17	0.12
321-576	Bipolar	0.031	0.081	0.10	0.11	0.12	0.18	0.22	0.13	0.21	0.15
	MOS Dynamic	0.014	0.044	0.060	0.063	0.076	0.11	0.15	0.084	0.14	0.11
	MOS Static	0.023	0.075	0.10	0.11	0.13	0.21	0.27	0.13	0.24	0.15
577-1120	Bipolar	0.054	0.14	0.17	0.17	0.22	0.30	0.37	0.20	0.34	0.22
	MOS Dynamic	0.022	0.073	0.10	0.10	0.13	0.20	0.26	0.13	0.23	0.15
	MOS Static	0.042	0.14	0.19	0.19	0.24	0.40	0.51	0.22	0.43	0.24
1121-2240	Bipolar	0.10	0.24	0.32	0.32	0.38	0.54	0.65	0.35	0.57	0.38
	MOS Dynamic	0.032	0.11	0.15	0.15	0.19	0.30	0.39	0.18	0.34	0.21
	MOS Static	0.064	0.22	0.29	0.30	0.37	0.62	0.79	0.33	0.66	0.36
2241-5000	Bipolar	0.18	0.45	0.54	0.55	0.65	0.94	1.1	0.58	0.99	0.61
	MOS Dynamic	0.060	0.20	0.27	0.27	0.35	0.57	0.73	0.31	0.61	0.34
	MOS Static	0.13	0.43	0.57	0.57	0.74	1.2	1.6	0.61	1.3	0.65
5001-11000	Bipolar	0.32	0.78	0.95	0.96	1.2	1.7	2.0	1.0	1.7	1.0
	MOS Dynamic	0.12	0.38	0.51	0.51	0.66	1.1	1.4	0.55	1.1	0.59
	MOS Static	0.27	0.86	1.1	1.1	1.5	2.4	3.1	1.2	2.5	1.2
11001-17000	Bipolar	0.59	1.4	1.7	1.7	2.1	3.0	3.5	1.8	3.0	1.8
	MOS Dynamic	0.18	0.58	0.77	0.78	1.0	1.7	2.1	0.83	1.7	0.88
	MOS Static	0.42	1.3	1.8	1.8	2.3	3.8	4.9	1.9	3.9	1.9
17001-38000	MOS Dynamic	0.26	0.88	1.2	1.2	1.5	2.5	3.1	1.2	2.6	1.3
	MOS Static	0.65	2.1	2.8	2.8	3.6	6.0	7.6	2.9	6.1	3.0
38001-74000	MOS Dynamic	0.55	1.7	2.3	2.3	3.0	4.9	6.2	2.4	5.0	2.5
	MOS Static	1.4	4.3	5.7	5.7	7.3	12.	15.	5.8	12.	6.0

TABLE 3-6 GENERIC FAILURE RATE, λ_G, FOR RANDOM ACCESS MEMORY (RAM) DEVICES IN NONHERMETIC PACKAGES vs. ENVIRONMENT (F. /10^6 Hours)

DEVICE DESCRIPTION		APPLICATION ENVIRONMENT									
BIT COMPLEXITY	TECHNOLOGY	G_B or S_F	G_F	A_{IT}	G_N	N_S	A_{UT}	N_U	A_{IF}	A_{UF}	N_L
1-320	Bipolar	0.025	0.072	0.095	0.098	0.11	0.17	0.21	0.12	0.20	0.14
	MOS Dynamic	0.014	0.058	0.084	0.088	0.12	0.22	0.30	0.11	0.25	0.13
	MOS Static	0.023	0.11	0.16	0.16	0.22	0.43	0.63	0.18	0.45	0.21
321-576	Bipolar	0.035	0.099	0.13	0.13	0.16	0.24	0.30	0.16	0.27	0.18
	MOS Dynamic	0.017	0.078	0.11	0.12	0.16	0.32	0.43	0.14	0.34	0.16
	MOS Static	0.033	0.16	0.24	0.024	0.34	0.66	0.98	0.27	0.69	0.29
577-1120	Bipolar	0.063	0.17	0.22	0.22	0.28	0.42	0.52	0.25	0.46	0.27
	MOS Dynamic	0.032	0.16	0.2[illegible]	0.24	0.33	0.64	0.96	0.26	0.67	0.28
	MOS Static	0.069	0.35	0.51	0.51	0.75	1.5	2.1	0.54	1.6	0.57
1121-2240	Bipolar	0.11	0.31	0.41	0.41	0.50	0.76	0.94	0.44	0.79	0.47
	MOS Dynamic	0.047	0.23	0.35	0.35	0.49	0.97	1.5	0.38	1.0	0.41
	MOS Static	0.11	0.55	0.80	0.80	1.2	2.4	3.3	0.84	2.4	0.87
2241-5000	Bipolar	0.22	0.58	0.73	0.73	0.92	1.4	1.7	0.77	1.4	0.80
	MOS Dynamic	0.099	0.51	0.73	0.74	1.1	2.2	3.0	0.77	2.2	0.81
	MOS Static	0.25	1.2	1.8	1.8	2.5	5.1	7.3	1.9	5.2	1.9
5001-11000	Bipolar	0.41	1.1	1.3	1.4	1.6	2.5	3.0	1.4	2.5	1.4
	MOS Dynamic	0.22	1.1	1.6	1.6	2.2	4.6	6.5	1.7	4.6	1.7
	MOS Static	0.60	2.8	3.9	4.0	5.9	12.	16.	4.0	12.	4.1
11001-17000	Bipolar	0.78	2.0	2.4	2.4	3.0	4.5	5.4	2.5	4.6	2.5
	MOS Dynamic	0.33	1.7	2.5	2.5	3.4	7.0	9.9	2.5	7.0	2.6
	MOS Static	0.94	4.5	6.2	6.2	9.2	18.	25.	6.3	18.	6.3
17001-38000	MOS Dynamic	0.50	2.5	3.8	3.8	5.2	11.	15.	3.8	11.	3.9
	MOS Static	1.5	7.0	9.7	9.7	15.	28.	39.	9.8	28.	9.9
38001-74000	MOS Dynamic	1.2	5.7	7.9	7.9	12.	23.	31.	8.0	23.	8.1
	MOS Static	3.4	15.	23.	23.	31.	61.	84.	23.	61.	23.

TABLE 3-7 GENERIC FAILURE RATE, λ_G, FOR LINEAR DEVICES vs. ENVIRONMENT (F./10^6 Hours)

DEVICE DESCRIPTION	APPLICATION ENVIRONMENT									
DEVICE COMPLEXITY	G_B&S_F	G_F	A_{IT}	G_M	N_S	A_{UT}	N_U	A_{IF}	A_{UF}	N_L
	HERMETIC PACKAGES									
1-32 Transistors	0.014	0.045	0.063	0.067	0.082	0.13	0.17	0.088	0.16	0.11
33-100 Transistors	0.038	0.13	0.19	0.19	0.24	0.40	0.53	0.23	0.45	0.27
100-300 Transistors	0.14	0.49	0.68	0.69	0.89	1.5	2.0	0.75	1.6	0.82
	NONHERMETIC PACKAGES									
1-32 Transistors	0.018	0.006	0.15	0.15	0.22	0.49	0.70	0.17	0.52	0.20
33-100 Transistors	0.069	0.34	0.56	0.56	0.80	1.8	2.7	0.60	1.9	0.64
100-300 Transistors	0.31	1.0	2.9	2.9	4.1	9.1	13.	2.9	9.2	3.0

TABLE 3-8

π_Q, QUALITY FACTORS FOR USE WITH TABLES 3-1 THRU 3-7

Quality Level	π_Q
S	0.5
B	1.0
B-1	3.0
B-2	6.5
C	8.0
C-1	13.0
D	17.5
D-1	35.0

TABLE 3-9

π_L, LEARNING FACTOR FOR USE WITH TABLES 3-1 THRU 3-7

The learning factor π_L is 10 under any of the following conditions:

(1) New device in initial production.
(2) Where major changes in design or process have occurred.
(3) Where there has been an extended interruption in production or a change in line personnel (radical expansion).

The factor of 10 can be expected to apply until conditions and controls have stabilized. This period can extend for as much as six months of continuous production.

π_L is equal to 1.0 under all production conditions not stated in (1), (2) and (3) above.

APPENDIX E

PARAMETRIC CURVES

Appendix E contains graphs of predicted failure rate as a function of complexity for junction temperatures of 25°C, 50°C, 75°C, 100°C and 125°C. Failure rate calculations are based on the microcircuit reliability prediction models of MIL-HDBK-217C and assume a part which has been screened to Class B specifications, used in a ground-fixed (GF) environment and in a ceramic dual-in-line (DIP) package with glass seal.

These graphs permit the reader to visualize the effects of complexity and temperature on predicted failure rate for various part types and technologies. The graphs are also useful for estimating the predicted reliability of alternative components during the early design and component selection stages.

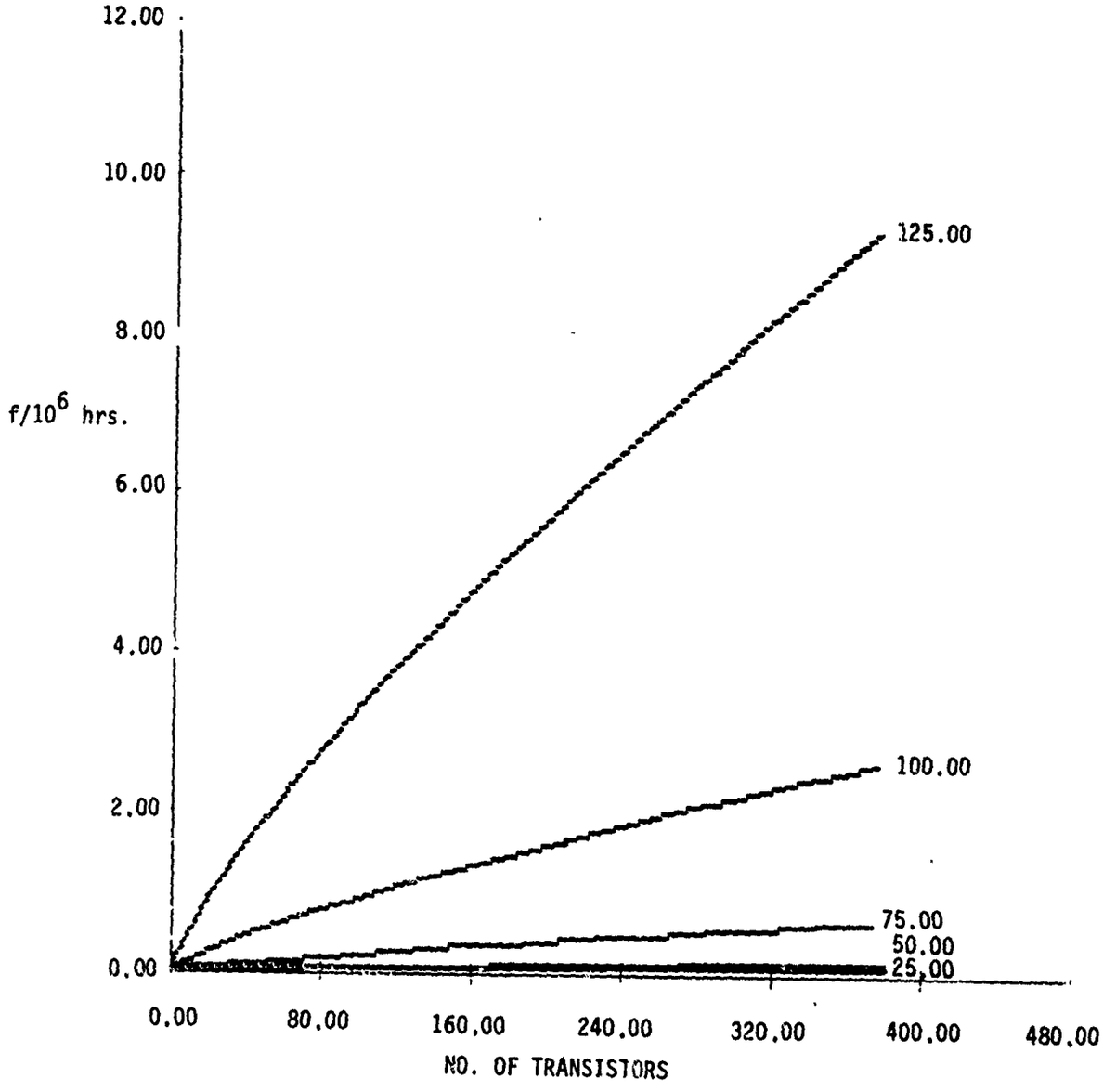


FIGURE 1: BIPOLAR LINEAR SSI/MSI

ASSUMES CLASS B PART, 16-PIN CERDIP, GF ENVIRONMENT

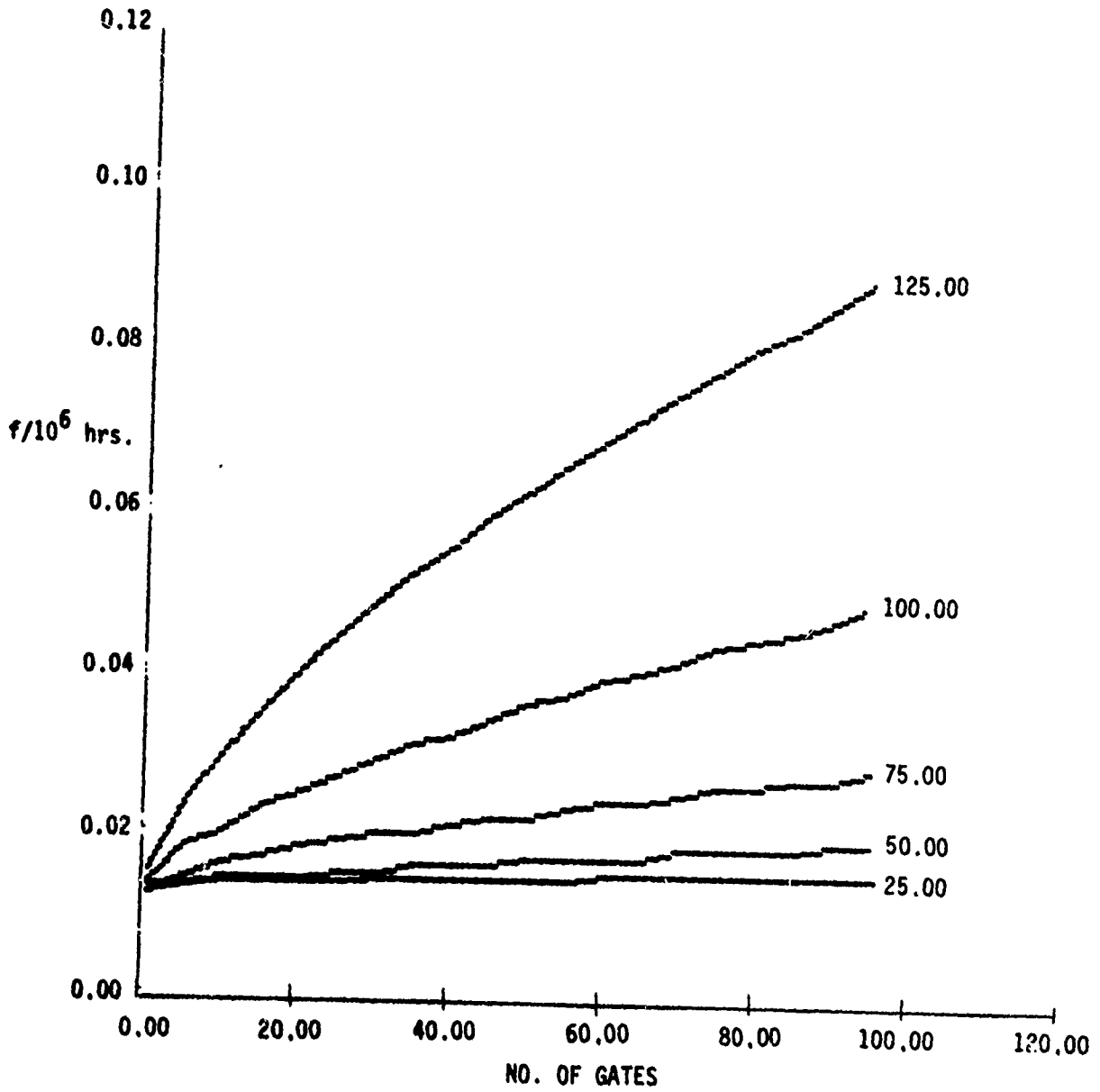


FIGURE 2: TTL SSI/MSI

ASSUMES CLASS B PART, 14-PIN CERDIP, GF ENVIRONMENT

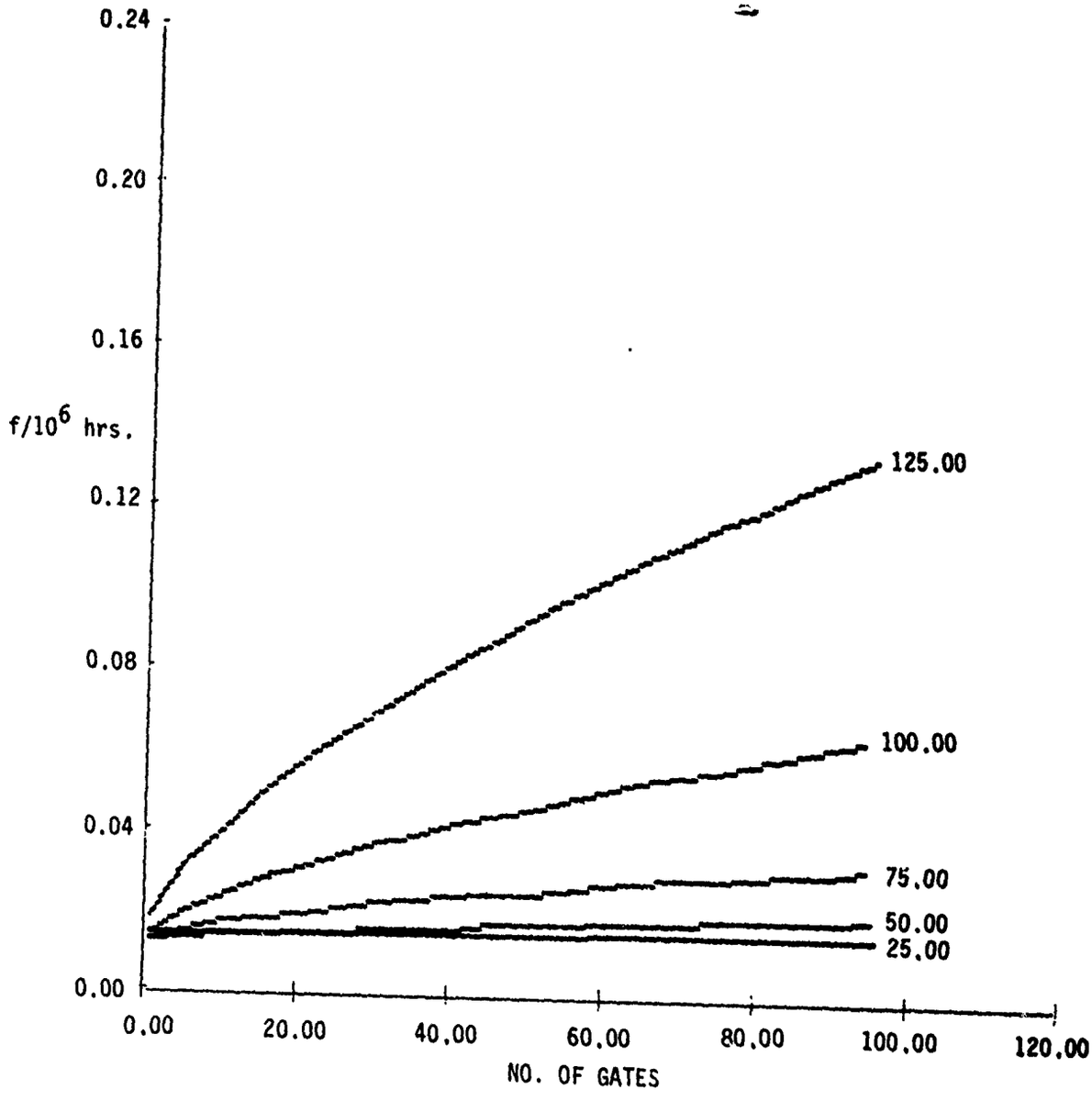


FIGURE 3: LTTL, STTL SSI/MSI

ASSUMES CLASS B PART, 14-PIN CERDIP, GF ENVIRONMENT

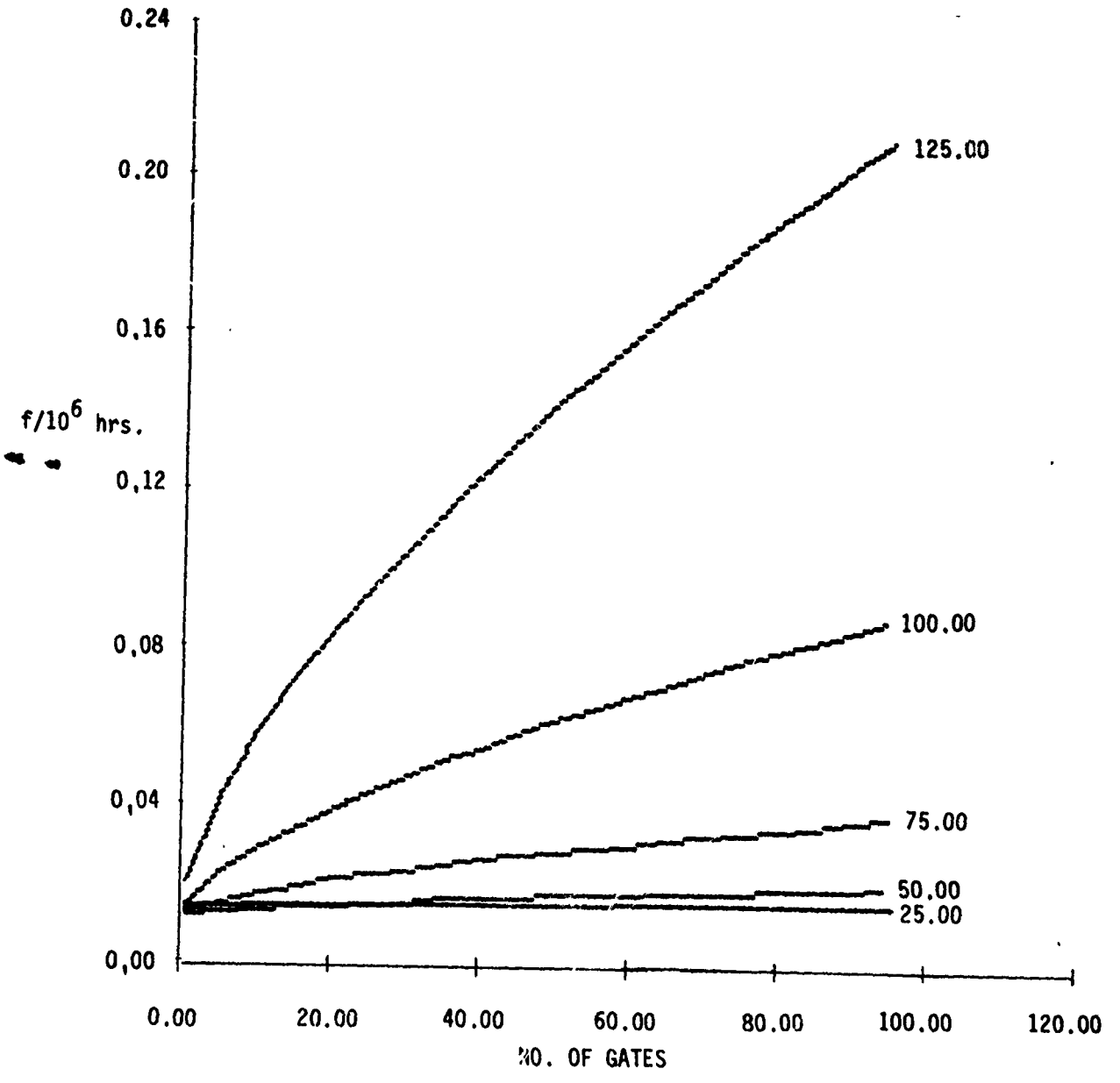


FIGURE 4: LSTTL

ASSUMES CLASS B PART, 14-PIN CERDIP, GF ENVIRONMENT

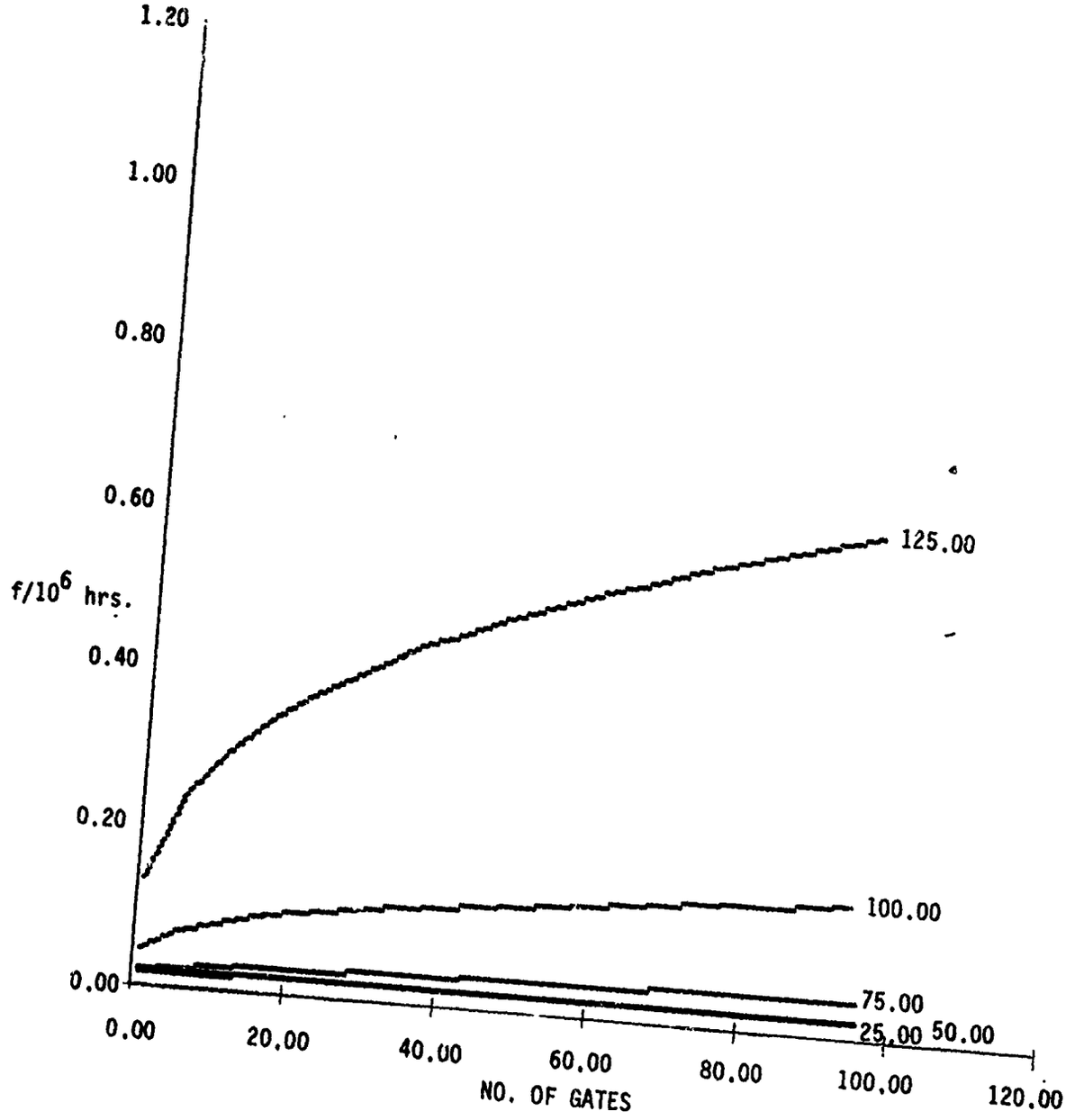


FIGURE 5: B-SERIES, CMOS SSI/MSI
ASSUMES CLASS B PART, 16-PIN CERDIP, GF ENVIRONMENT

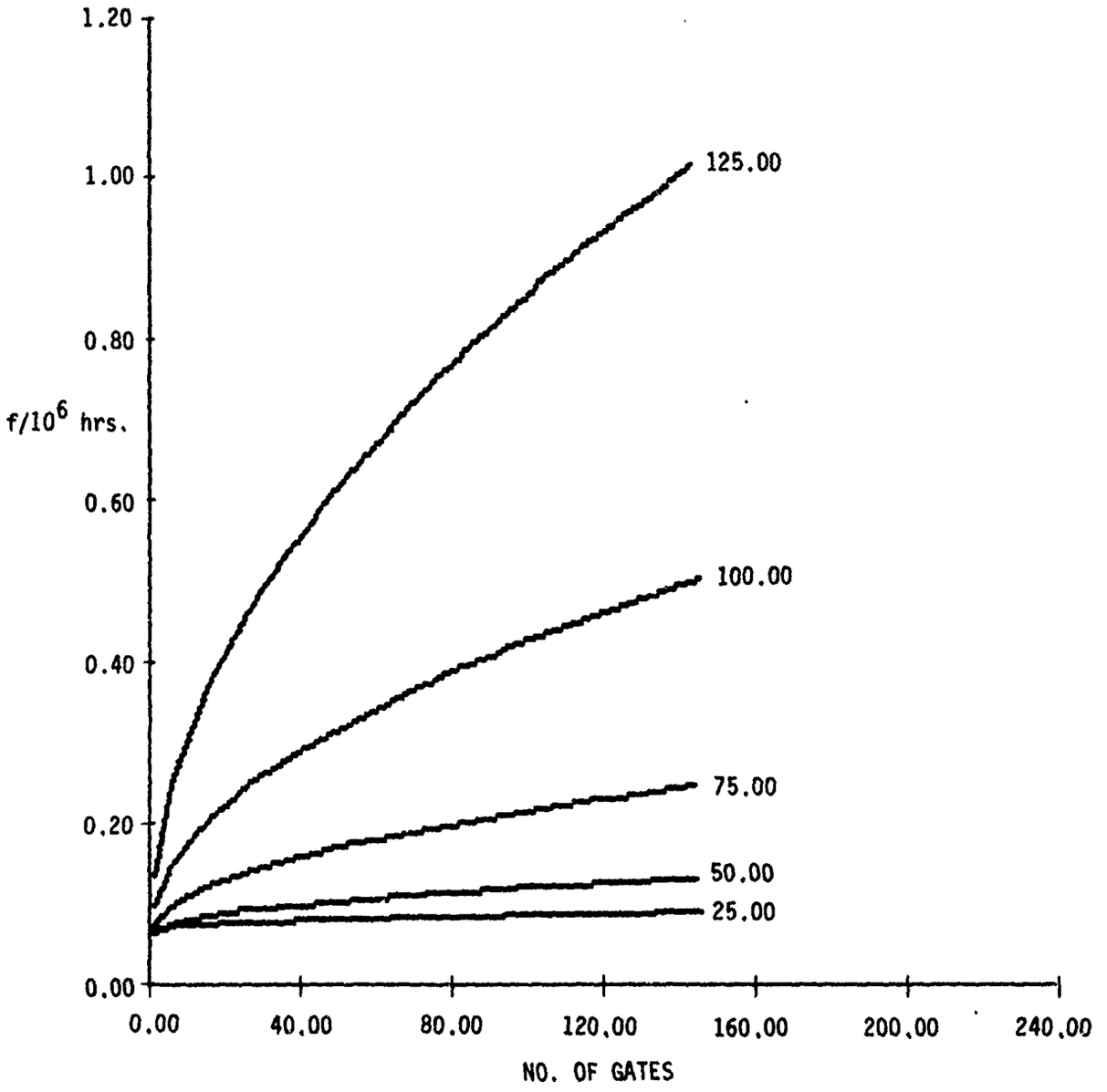


FIGURE 6: BIPOLAR LSI RANDOM LOGIC

ASSUMES CLASS B PART, 40-PIN CERDIP, GF ENVIRONMENT

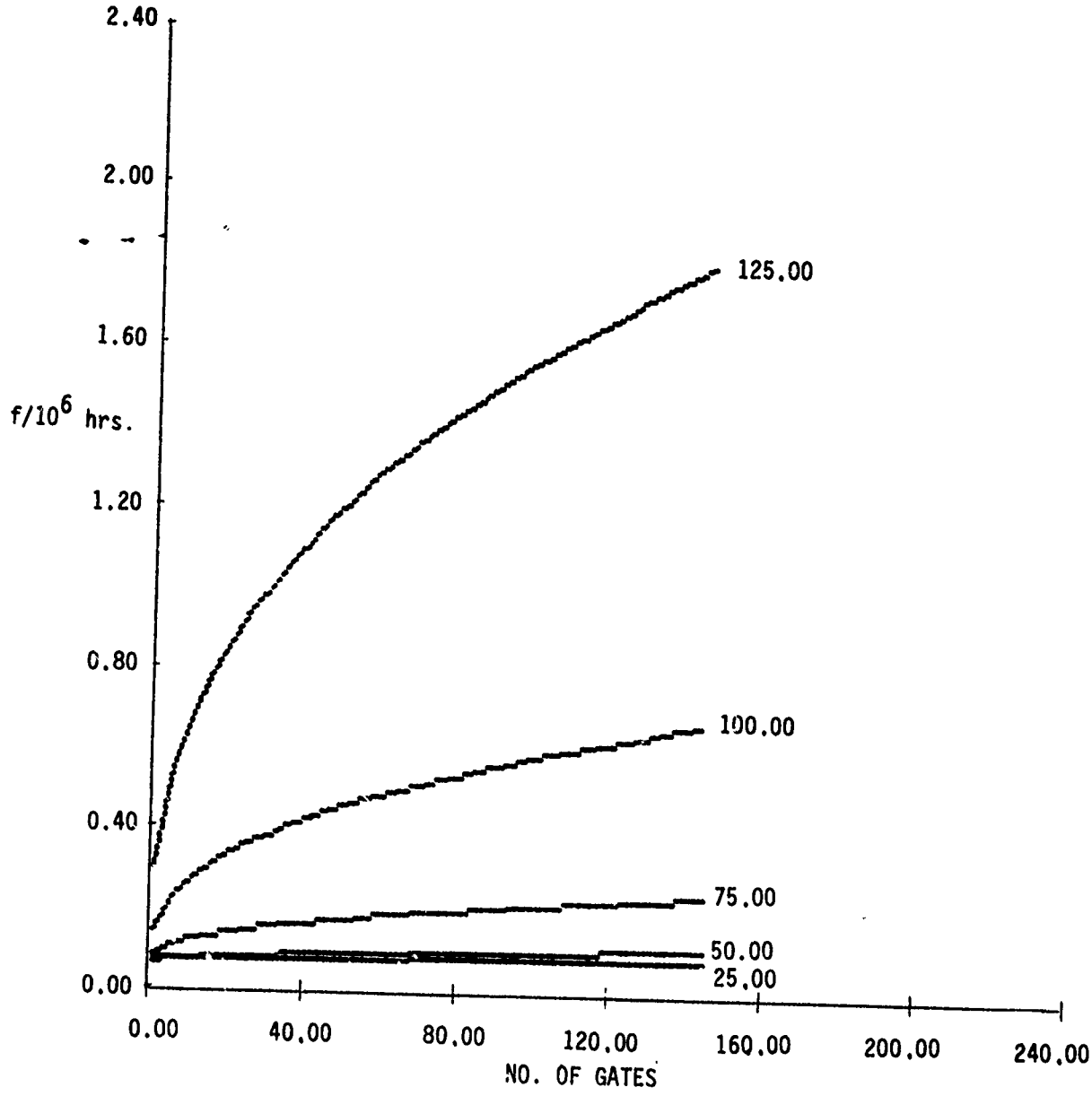


FIGURE 7: NMOS LSI RANDOM LOGIC

ASSUMES CLASS B PART, 40-PIN CERDIP, GF ENVIRONMENT

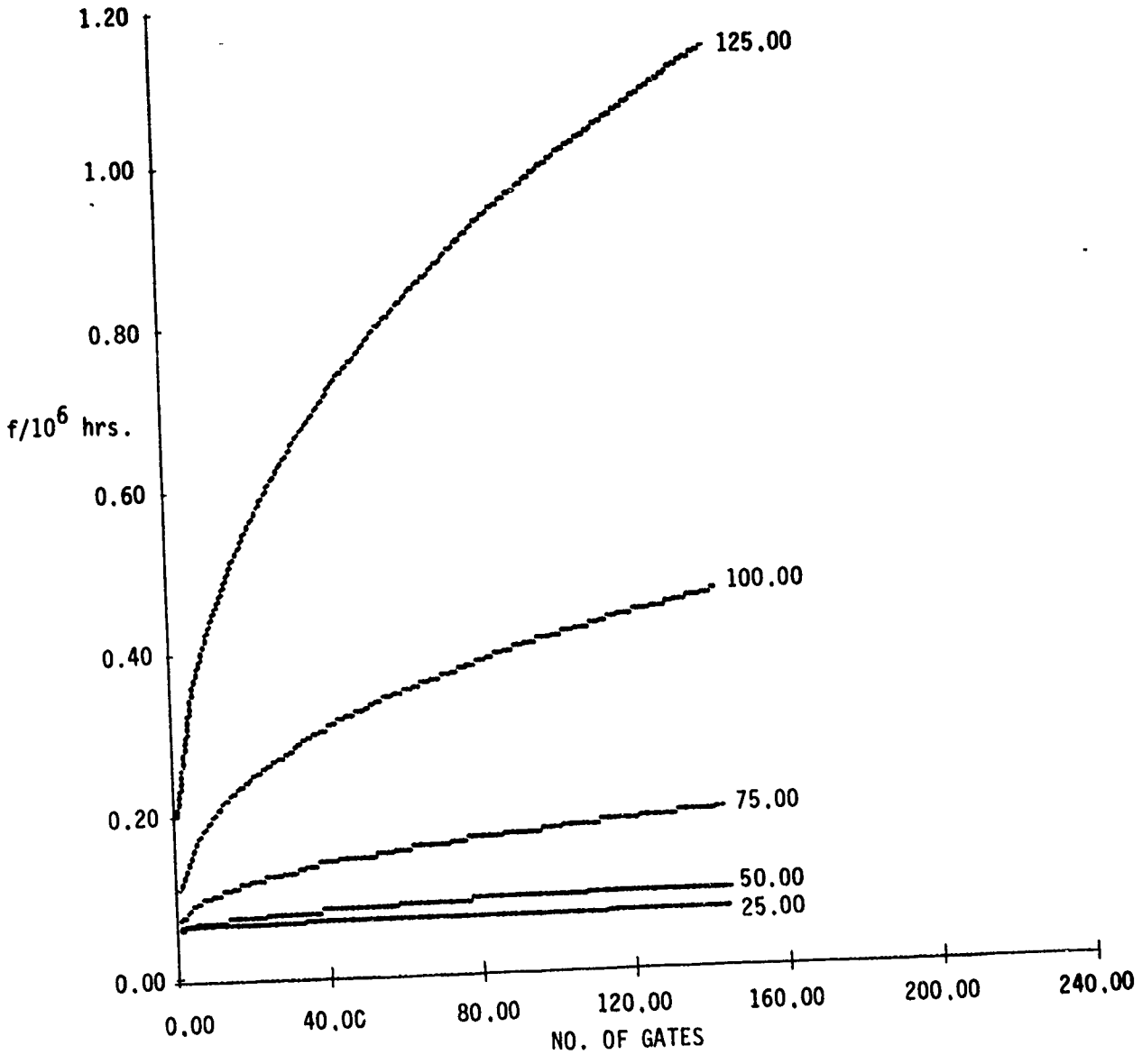


FIGURE 8: PMOS LSI RANDOM LOGIC MODEL

ASSUMES CLASS B PART, 40-PIN CERDIP, GF ENVIRONMENT

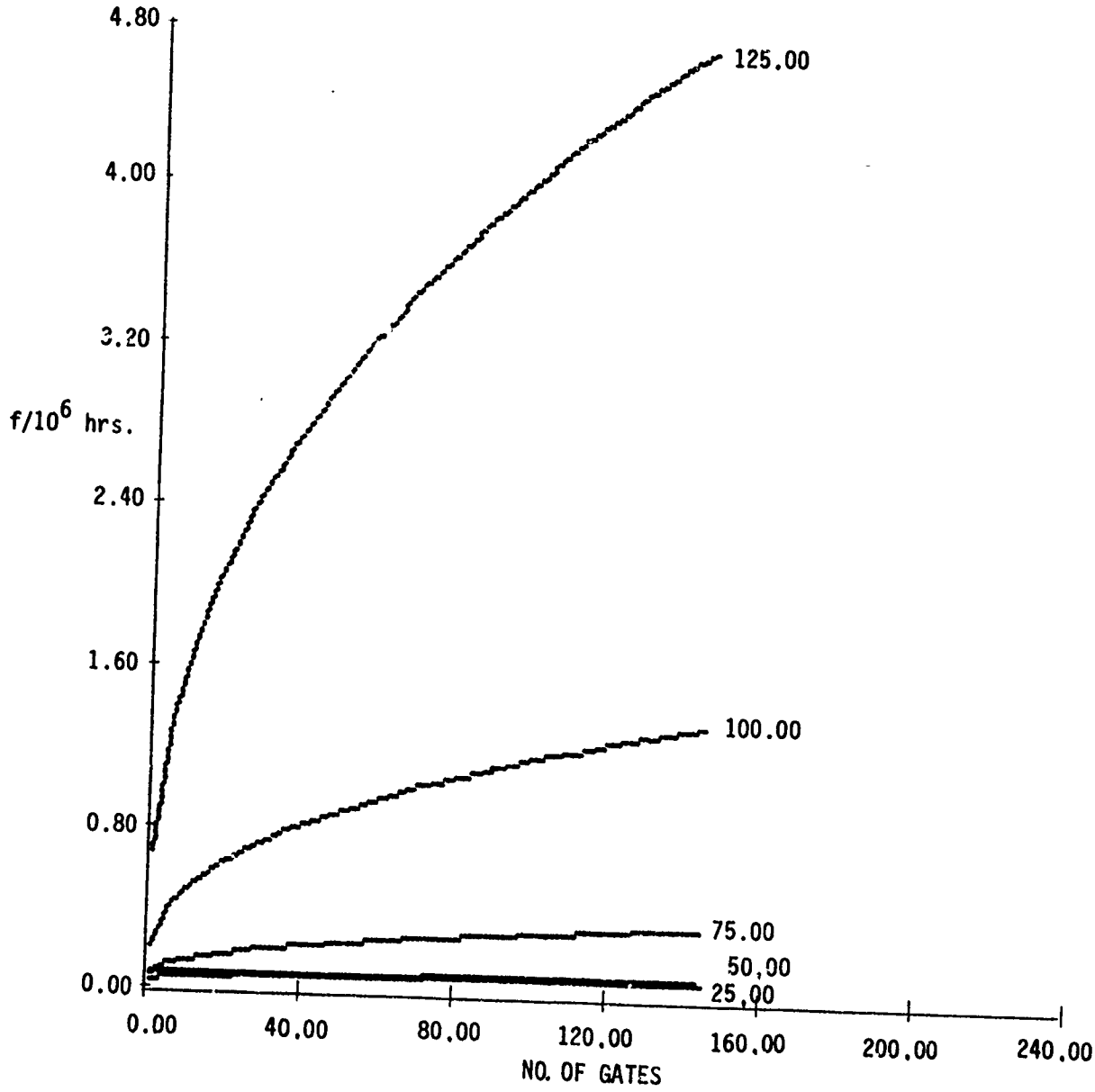


FIGURE 9: CMOS LSI RANDOM LOGIC
ASSUMES CLASS B PART, 40-PIN CERDIP, GF ENVIRONMENT

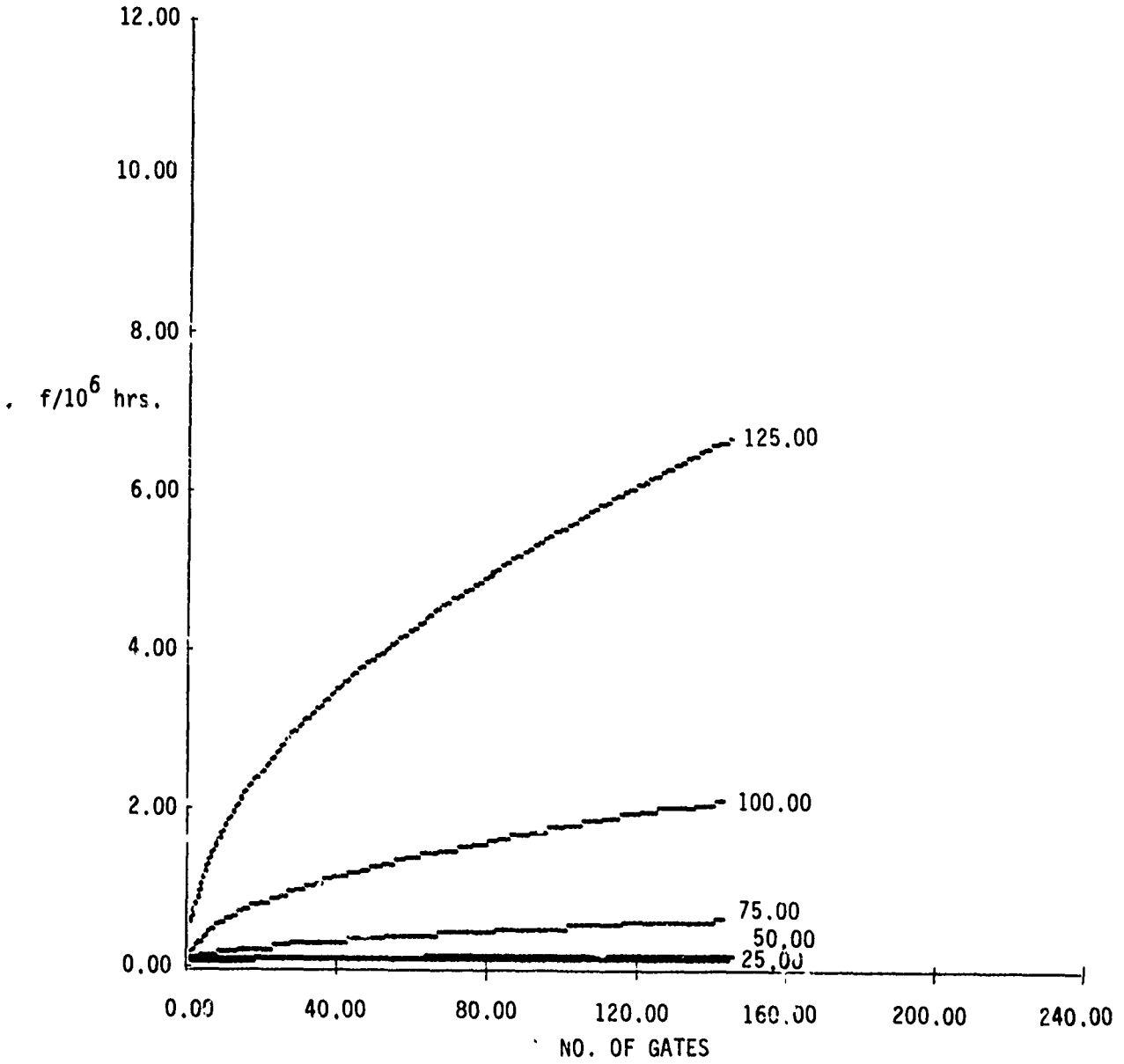


FIGURE 10: IIL LSI COMPONENTS

ASSUMES CLASS B PART, 40-PIN CERDIP, GF ENVIRONMENT

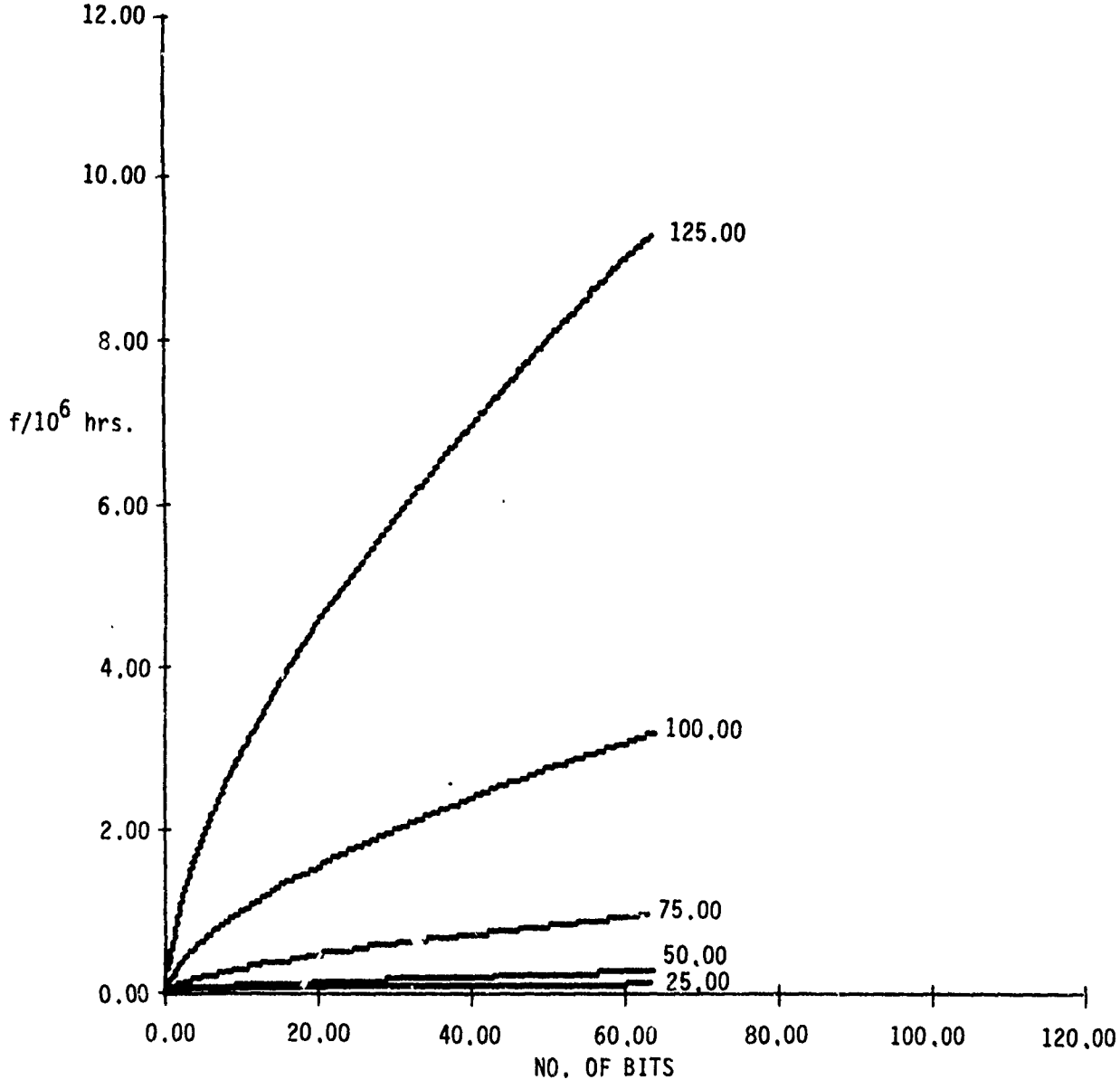


FIGURE 11: NMOS DYNAMIC RAM

ASSUMES CLASS B PART, 16-PIN CERDIP, GF ENVIRONMENT

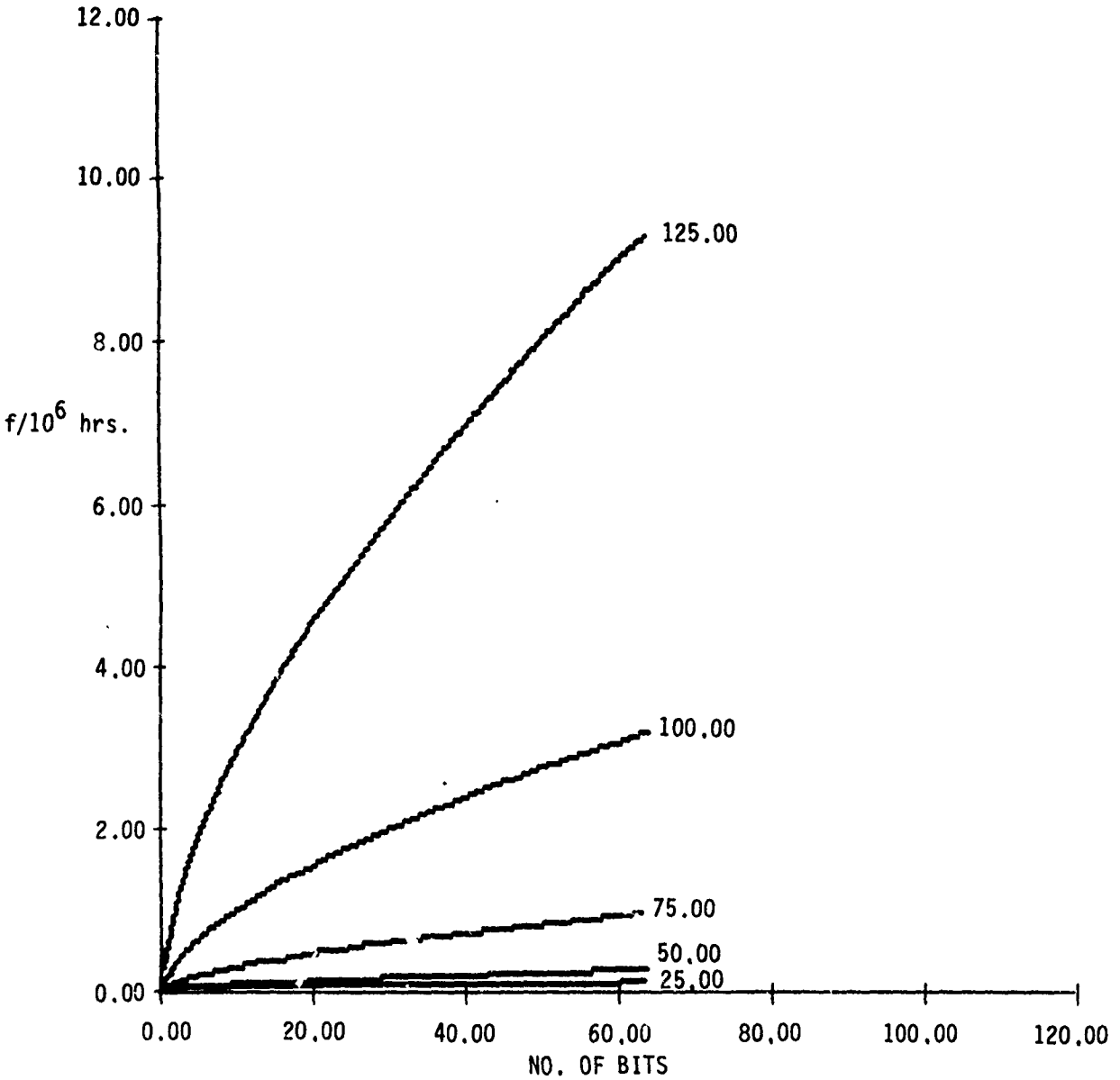


FIGURE 11: NMOS DYNAMIC RAM

ASSUMES CLASS B PART, 16-PIN CERDIP, GF ENVIRONMENT

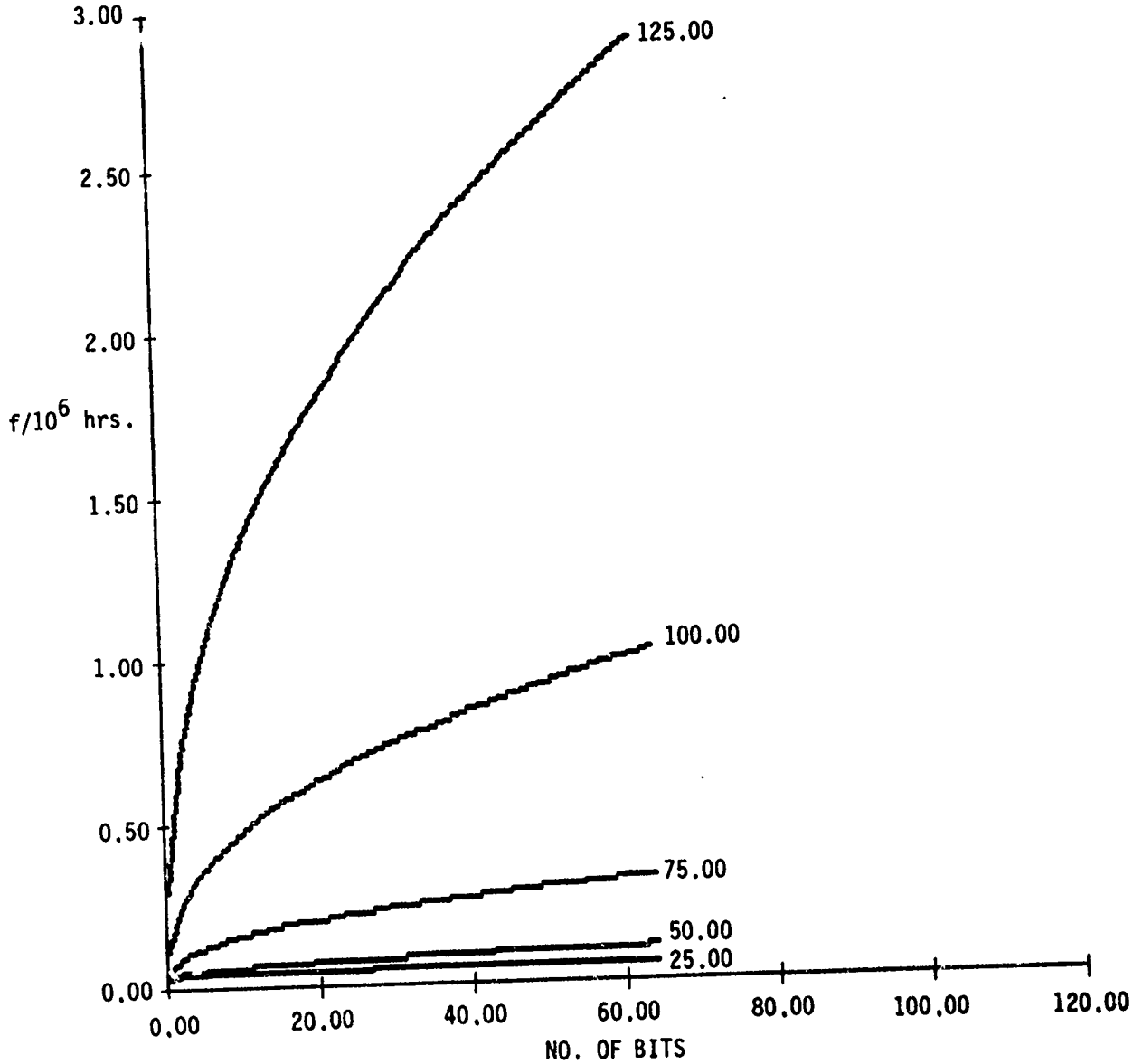


FIGURE 12: BIPOLAR ROM

ASSUMES CLASS B PART, 24-PIN CERDIP, GF ENVIRONMENT

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