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COMPUTER PROGRAM FOR MICROWAVE GAAS MESFET MODELING. (U)
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NRL Report 8561

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Computer Program for Microwave GaAs MESFET Modeling

R. E. NEIDERT AND C. J. SCOTT

*Microwave Technology Branch
Electronics Technology Division*

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February 12, 1982



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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER NRL Report 8561	2. GOVT ACCESSION NO. AD A111 299	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) COMPUTER PROGRAM FOR MICROWAVE GaAs MESFET MODELING	5. TYPE OF REPORT & PERIOD COVERED Interim report on one phase of an NRL problem.	
	6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s) R. E. Neidert and C. J. Scott	8. CONTRACT OR GRANT NUMBER(s)	
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Research Laboratory Washington, DC 20375	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 1493-C-2 RR021-03-46	
11. CONTROLLING OFFICE NAME AND ADDRESS Department of the Navy Office of Naval Research Arlington, VA 22217	12. REPORT DATE February 12, 1982	
	13. NUMBER OF PAGES 50	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report) UNCLASSIFIED	
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE	
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Microwave Computer program Solid state devices Field effect transistor FORTRAN MESFET Gallium arsenide Modeling Indium phosphide		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) A computer program is described which is used to calculate the equivalent circuit element values for microwave MESFETs (metal-semiconductor field effect transistors). The input information required by the program consists of the semiconductor material parameters and the physical dimensions of the semiconductor material and metallization. The program's name is FETREN; it is fully analytical and is inexpensive to use; it is written in FORTRAN language and configured for use with the Control Data Corporation timeshare system. A listing is provided.		

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COMPUTER PROGRAM FOR MICROWAVE GaAs MESFET MODELING

INTRODUCTION

There has long been a need for a simple, inexpensive, fairly accurate, easy-to-run computer program for calculating the equivalent circuit elements of MESFETs (metal-semiconductor field effect transistors). Microwave circuit designers use an equivalent circuit representation for the transistor, similar to that shown in Fig. 1, which will be discussed in detail later. They also sometimes use S-parameters to represent the active device, but they can be calculated directly from the equivalent circuit. A problem with all the analytical MESFET models proposed to date is that they do not give answers which agree well with measured data over all bias conditions. Provisions have been made, in the computer program FETREN, presented in this report, to improve on agreement with measured results over the full range of bias conditions (or over the full range of large signal "swing" conditions).

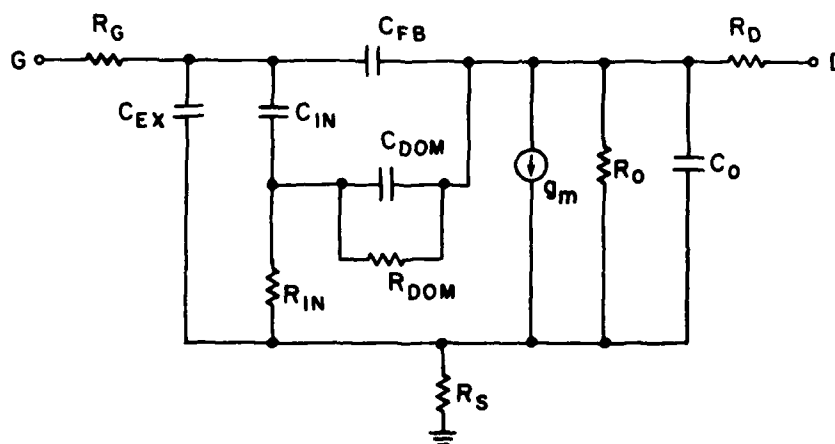


Fig. 1 — Equivalent circuit representation of a GaAs MESFET. The most significant bias-dependent device elements are C_{FB} , C_{IN} , g_m , R_{IN} , and R_O .

Certain new terms are added to the model employed in this program to permit adjustment of computed results to measured values—mostly in a self-consistent and plausible way, rather than by the use of arbitrary "fitting" constants. In areas where the analytical theory is not exact enough, or where the knowledge of the field behavior is not well enough known, computational methods of interpolation are employed to obtain estimates of the circuit element values between known values. For example, this approach is required to get reasonable answers when the drain voltage is somewhere between low values for which no Gunn domain can exist, and high values for which the domain is "fully" formed.

Other such departures from earlier, less practical, models will be described subsequently. The philosophy applied in the development of the model used for the computer program FETREN is: (1) apply whatever analytical theory gives the best agreement with measured results, (2) do not be disappointed with less than perfect agreement, and (3) keep the program simple and inexpensive to use. The program listing is included as Appendix A, and the flow diagram is included as Appendix B.

Table 1 describes the symbolic notations used in the text in the order in which they appear. A notation list for the computer program is included with the program listing in Appendix A.

Table 1 — Text Notation

δ	Conducting channel thickness in Region II
Φ	Potential
ρ	Volume charge density
ϵ_r	Relative dielectric constant
ϵ_0	Permittivity of free space
ϵ	Product of ϵ_0 and ϵ_r
V_{DS_1}	Longitudinal voltage drop across Region I
V_{DS_2}	Longitudinal voltage drop across Region II
V_{DS_m}	Longitudinal voltage drop along the conducting channel from the drain end of the gate to the source end of the gate
y	Vertical distance measured from bottom of active layer
b	Vertical thickness of conducting channel
a	Total active layer thickness
V_{PO}	Pinch-off voltage
q	Electronic charge
N_D	Volume donor impurity concentration
μ_0	Low field mobility
W	Gate width
x	Horizontal distance measured from source edge of gate
I_{DS}	Drain-to-source current
L	Gate length
L_1	Length of Region I under gate
L_2	Length of Region II under gate
f_1	A specific analytical function
V_{GS}	Gate-to-source voltage
V_{Br}	Metal-to-semiconductor gate schottky barrier built in voltage, taken as a positive voltage
b_1	Conducting channel thickness at first point right of source where the field has increased to E_s
E_s	Longitudinal field strength which just causes carrier velocity saturation
p	Square root of the ratio of: (1) the voltage at the junction point between Regions I and II, relative to the gate electrode, to (2) the pinch-off voltage

Table 1 — Text Notation (Continued)

s	Square root of the ratio of: (1) the voltage at the source end of the gate, relative to the gate electrode, to (2) the pinch-off voltage
E_{long}	Longitudinal electric field
R_S	Sum of bulk semiconductor resistance and contact resistance from source edge of gate to the source metal
R_D	Sum of bulk semiconductor resistance and contact resistance from drain edge of gate to the drain metal
$V_{GS_{int}}$	Voltage drop from gate metal to the conducting channel at the source end of the gate
$V_{GS_{ext}}$	Voltage drop from gate metal to source metal
$V_{DS_{ext}}$	Voltage drop from drain metal to source metal
AK	Substrate current multiplying constant
I_{SUB}	A current said to be passing through the substrate material, under the active layer, in parallel with the active current generator
$DR1$	Drain shunt resistance
v_{sat}	The assumed electron saturated velocity
RTH	Device overall thermal resistance
g_m	Transconductance
f_R	A specific analytical function
d	Square root of the ratio of: (1) the voltage at the drain end of the gate, relative to the gate electrode, when there is no Region II, to (2) the pinch-off voltage
r_0	Intrinsic transistor output resistance
g_{sub}	An output conductance term related to substrate current
r_{sub}	The reciprocal of g_{sub}
R_{IN}	The charging resistance for C_{IN}
C_{IN}	The gate-to-source capacitance
Q	Total charge
Q_R	Charge in depleted area under gate
Q_e	Charge of extended depletion area toward drain
Q_{dom}	Charge of domain
C_{gs0}	Gate-to-source capacitance for drain voltage near zero
C_{gs}	Gate-to-source capacitance for large drain voltage
n_{cr}	The "characteristic" doping density, which depends on the shape of the velocity vs electric field curve, see Ref. 12
$K(k)$	Complete elliptic integral of the first kind in terms of the modulus, k

Table 1 — Text Notation (Continued)

<i>DL</i>	Drain metal length
<i>DGL</i>	Distance between drain and gate metal
<i>WG</i>	Gate length, same as L
<i>SL</i>	Source metal length
<i>SGL</i>	Distance between source and gate metal
<i>SDL</i>	Distance between source and drain metal ($SDL = SGL + WG + DGL$)
<i>z</i>	Radius of sidewall capacitance area
Q_{SW}	Total charge depleted from source-end, sidewall, quarter circle depletion area
C_{SW}	Sidewall capacitance
C_{EX}	Same as C_{SW}
<i>RDOM</i>	Domain resistance
<i>CDOM</i>	Domain capacitance
<i>n</i>	Volume electron density
<i>J</i>	Current density
<i>t</i>	Time
<i>v</i>	Drift velocity
<i>D</i>	Diffusion coefficient
W_{th}	Threshold depletion layer thickness
E_{th}	Threshold field for bulk negative differential mobility
τ	Transit time

CONCEPTUAL REVIEW

Much has been written about the general evolution of microwave MESFETs and their modeling. For an excellent review see Liechti [1]. A repeat of that is not undertaken here. Rather, a review of the specific concepts used in the development of the computer program FETREN and its associated model is given. The origins of all the related concepts are referenced and discussed if they were derived from earlier literature, and are explained if they are new ideas developed by the authors of this report. It is assumed that the reader is familiar with the subject or will read the referenced material as required.

The majority of the calculations are based on the theory of Grebene and Ghandi [2]. They expanded on the work of Shockley [3], as Shockley himself suggested it might be done, to allow two distinct regions under the gate. Region I, nearer the source, is taken to have constant carrier mobility; and Region II, nearer the drain, has saturated carrier velocity. Figure 2 shows the configuration, with the point which separates Region I from Region II being free to move longitudinally, so that it can position itself at the first instance of longitudinal electric field large enough to produce velocity saturation. The longitudinal electric field in Region I is always least at the source end and is larger at positions closer to the drain end. The vertical conducting channel thickness in Region II, δ , is assumed

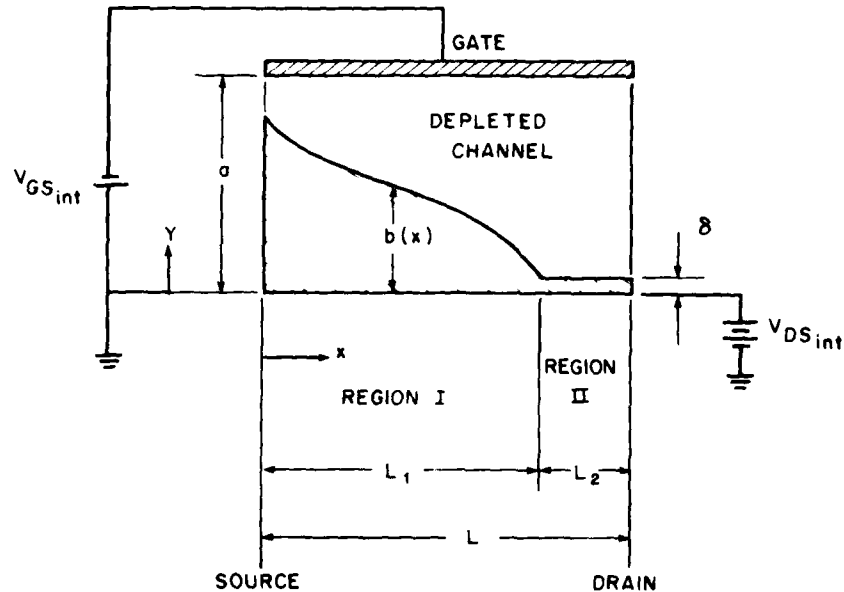


Fig. 2 — Assumed MESFET configuration for theoretical analysis

constant over the whole of that region. The method of solving the applicable equations for Regions I and II, separately, and applying suitable continuity criteria between the two regions is given in Grebene and Ghandi [2] and is extremely well detailed in Pucel et al. [4].

From a conceptual standpoint, the theory or model which is deduced from Refs. 2, 3, and 4 has some problems, even though it may never be greatly improved upon for small signal calculations at moderate drain voltages if no Gunn domain forms. Some obvious problems are: (1) no computational provision for the presence of a Gunn domain, (2) no provision for adjustment of parameters due to heating from the bias power, (3) no provision for the effects of extension of the depletion region longitudinally beyond the gate, (4) no specific provision for a gate to source shunting resistance arising from either simple "leakage" or from carrier fringing around the extremely high field region when a Gunn domain is present, (5) no provision for the effect of the incorrect approximation that the channel thickness in Region II is nearly zero at all times (this approximation is suggested in Refs. 3 and 4), (6) no way of knowing the effects on the Region II calculations for a drain terminal whose physical shape is not like the one Shockley assumed in his original formulation (a semicircle whose shape is approximately that of the assumed drain equipotential shape).

It is fairly safe to say that there are too many variables to expect to ever get near-perfect agreement between any model and measured data. If the agreement needed must be extremely good, it is probable that some fitting to measured data is required.

All of the problems mentioned above were addressed in the development of the program FETREN. The way they were handled and the effects of considering them and making some provisions for them can be seen in the following section as the circuit element calculation methods are described.

CIRCUIT ELEMENT CALCULATIONS

The Operating Point

The operating point is set by the longitudinal position of the dividing line between Region I and Region II, such that the sum of the calculated voltage drops across the two regions equals the total applied voltage. In Fig. 3, $V_{DS1} + V_{DS2} = V_{DS_{int}}$. From the outset, FETREN has been set up to work from the external values of the two bias voltages—that is, those values which would be measurable in the laboratory. Therefore, in the initial calculations to determine the operating point, the "parasitic" resistances must be included. They are calculated between lines 1359 and 1368 in the program, the listing for which is given in Appendix A, with the drain and source contact resistances included in R_S and R_D . The calculation method is taken from Fukui [5].

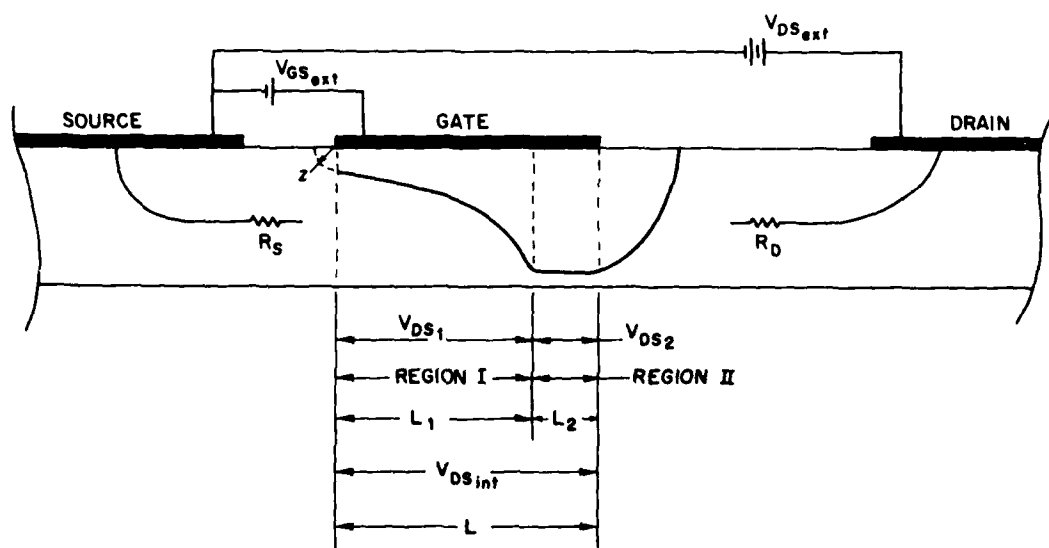


Fig. 3 — MESFET configuration showing internal and external voltages

An applicable relationship in the depletion region of Region I, for a volume charge density ρ , is Poisson's equation:

$$\nabla^2 \Phi = -\frac{\rho}{\epsilon_0 \epsilon_r} \quad (1)$$

where Φ is potential, ϵ_r is the relative dielectric constant of the intrinsic material, and ϵ_0 is the permittivity of free space. Then, by the gradual channel approximation [3], the potential variation in the y -direction is much greater than that longitudinally; the double integral of Eq. (1) in the y -dimension only, with appropriate boundary conditions, yields potentials for Region I:

$$\Phi = \frac{\rho}{\epsilon} \frac{y^2}{2} + \frac{\rho}{\epsilon} by + \left(\frac{\rho}{\epsilon} \frac{a^2}{2} - \frac{\rho}{\epsilon} ab \right) \quad (2)$$

where a is the total active layer thickness and b is the channel thickness as a function of horizontal position. The potential along the boundary between the depletion region and the conducting channel in Region I is given from Eq. (2) for $y = b$,

$$\Phi_{1-b} = \frac{\rho a^2}{2\epsilon} \left(1 - \frac{b}{a}\right)^2 = V_{PO} \left(1 - \frac{b}{a}\right)^2 \quad (3)$$

where $\rho = qN_D$, with q = electronic charge $\approx 1.602 \times 10^{-19}$ C; N_D = volume doping density; $\epsilon = \epsilon_0\epsilon_r$, with $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm and $\epsilon_r = 12.9$ according to Ref. 6; and $V_{PO} = (qN_D a^2)/(2\epsilon)$ is defined as the pinch-off voltage.

The current in the conducting channel of Region I is given by Ohm's law, such that

$$I_{DS_1} = q\mu_0 N_D b W \frac{\partial \Phi}{\partial x} \quad (4)$$

where $\partial \Phi / \partial x$ is the longitudinal electric field, W is the total gate width of the device, and μ_0 is the carrier low field mobility. After an integration over the length L_1 ,

$$I_{DS_1} = \frac{q\mu_0 N_D W a}{L_1} (f_1) \quad (5)$$

where

$$f_1 = \rho^2 - s^2 - \frac{2}{3} (\rho^3 - s^3) \quad (6)$$

with

$$\rho^2 = (V_{B_1} - V_{GS} + V_{DS_1}) / (V_{PO}) \quad (7)$$

and

$$s^2 = (V_{B_1} - V_{GS}) / (V_{PO}) \quad (8)$$

in terms of intrinsic voltages, with V_{B_1} = metal-to-semiconductor gate Schottky barrier built-in voltage, taken as a positive voltage. Also, V_{PO} is taken as a positive voltage.

In Region II, just at the boundary with Region I, the current may be calculated as

$$I_{DS_{II}} = q\mu_0 N_D b_1 W E_S \quad (9)$$

where E_S is the longitudinal field which just causes carrier velocity saturation, and b_1 is the channel thickness at that point. Since, as shown in Ref. 4,

$$b_1 = a(1 - \rho) \quad (10)$$

$$I_{DS_{II}} = q\mu_0 N_D a(1 - \rho) W E_S \quad (11)$$

If we equate Eqs. (11) and (5), to require current continuity at the junctions between Region I and II, then

$$L_1 = \frac{V_{PO}(f_1)}{E_S(1 - \rho)} \quad (12)$$

Then, to get voltage drops involved, the integral of the longitudinal electric field over the length of Region I is used to get V_{DS_1} :

$$\int_{x=0}^{x=L_1} E_{long} dx = V_{DS_1} = \int_{x=0}^{x=L_1} - \left(\frac{d\Phi_1}{dx} \right) dx \quad (13)$$

Also, in Region II, the potential distribution can be found with the solution of Laplace's equation in two dimensions:

$$\nabla^2 \Phi_{II} = 0. \quad (14)$$

However, an exact solution of this for the general case is difficult, and in Refs. 2, 3, and 4 the same approximate solution is used, originally proposed by Shockley [3]. The adequacy of the approximate solution requires that the physical shape of the drain conductor be "somewhat like" the shape of the equipotential lines far away from the drain. This is not the case in planar MESFETs, so in FETREN some liberty is taken with a constant related to this portion of the overall solution. The constant CDR2 in the program FETREN, at line 1415, may be varied to affect the amount of voltage drop assigned to Region II (but the form of the analytical expression is maintained). Specifically,

$$V_{DS_2} = \int_{x=L_1}^{x=L} \left(\frac{d\Phi_{II}}{dx} \right) dx. \quad (15)$$

for which an approximate solution, at $y = 0$, is:

$$V_{DS_2} = \frac{2a}{\pi} E_S \sinh \left[\frac{\pi(L - L_1)}{2a} \right]. \quad (16)$$

Also, from Eq. (13) in Region I, as shown in Pucel et al. [4],

$$V_{DS_1} = V_{p0}(p^2 - s^2). \quad (17)$$

So, the total (internal) voltage drop across the intrinsic transistor, after substituting Eq. (12) into Eq. (16), is:

$$V_{DS_{int}} = V_{p0}(p^2 - s^2) + \frac{2a}{\pi} E_S \sinh \left\{ \frac{\pi}{2a} \left[L - \frac{V_{p0}}{(1-p)E_S} (f_1) \right] \right\}. \quad (18)$$

Figure 4, a simplified transistor schematic, shows that the accessible (measurable) drain-to-source voltage is the sum of the intrinsic part, $V_{DS_{int}}$, and the drops across R_S and R_D . Note also that the accessible gate-to-source voltage is sum of the intrinsic part, $V_{GS_{int}}$, and the drop across R_S . Therefore the accessible drain-to-source voltage is

$$V_{DS_{av}} = V_{DS_{int}} + I_{DS}(R_S + R_D). \quad (19)$$

Also, the accessible gate-to-source voltage is

$$V_{GS_{av}} = V_{GS_{int}} + I_{DS}(R_S). \quad (20)$$

In the program FETREN, if there is a Region II, the determination of the overall operating point is determined by forcing, through iteration, the applied $V_{DS_{av}}$ to equal the terms of Eq. (19) at line number 5200, while forcing simultaneously the applied $V_{GS_{av}}$ to equal the terms of Eq. (20) at line 6010. The values of s , p , and I_{DS} are the final values which the iterative process assigns them. The value of s is calculated at line 3100, p by iterative assignment at 4700, and I_{DS} , indirectly, at 5200 and repeated explicitly at 6200. Also, within this iterative loop which extends approximately from line 2200, where the external gate-to-source voltage is set, to line 6040 where the s -iteration loop ends, the value of L_1 is determined at line 4900. Because the solution method is iterative, L_1 may sometimes overshoot and be temporarily assigned a value larger than the total gate length L , even though the final value may be less than L . Therefore the program, at line 4900, allows L_1 to be greater than L . After final convergence, however, if the final value for L_1 is larger than L , as tested at line 6100, the indication is that the bias levels were such that there is no Region II. For this case it is then necessary to completely re-solve the problem by using the equations that are applicable for Region I only. The

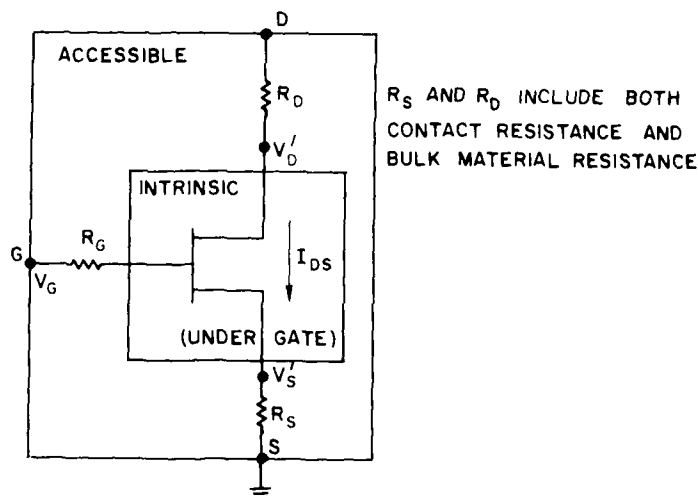


Fig. 4 - Simplified transistor schematic

authors derived these equations independently and found them to agree with those developed in Refs. 7 and 8; those references, Ref. 4, and the FETREN listing may be consulted for development formulation. This portion of FETREN starts at line 6620, and the operating point is determined by iterating the current and finding a simultaneous combination of s , d , and I_{DS} , for which the applied current equals the analytical value:

$$I_{DS} = aq\mu_0 N_D \frac{W}{L} V_{p0} \left[d^2 - s^2 - \frac{2}{3} (d^3 - s^3) \right] \quad (21)$$

where d is now related to the voltage at the drain edge of the gate. In terms of intrinsic bias voltages,

$$d^2 = (V_{fb} - V_{GS} + V_{DS}) / (V_{p0}) \quad (22)$$

analogous to Eq. (7). In summary, then, the operating point is prescribed as a function of the two bias voltages, as outlined above, after which the equivalent circuit parameters and the actual current can be computed.

The I-V Curves

The current calculated in the preceding section is an initial estimate of the actual current. Other factors must be considered in arriving at a better estimate of a value to agree with measured data. If there is a stationary Gunn domain present, a substrate current resulting from electron injection into the adjacent, otherwise assumed semi-insulating, substrate may result [9]. The arguments in Ref. 9 are not very strong for qualitative accuracy. Therefore, in FETREN, a constant AK , entered at line 1620 and used at lines 6206 or 6845, is included to make the substrate current effect variable—but the form of the analytical expression is maintained:

$$I_{SUB} \propto (N_D)^{2.5} (V_{DS_{op}})^{1/4} W \quad (23)$$

This shows that the substrate current, in the presence of a stationary Gunn domain, is proportional to the gate width, to the square root of the drain-to-source voltage, and to the fourth root of the doping level. For further detail, see Eastman and Shur [9]. (Substrate injection current can be eliminated by setting AK to zero at line 1620.)

One additional term is added to the currents already calculated to account for two physical phenomena not otherwise considered. One of these phenomena is simple resistive leakage across the top surface of the transistor or through the substrate whose overall conductivity is higher than desirable. The second is the resistive shunting effect of the doping "tail," which is typically disregarded. The doping tail, in Fig. 5, is the crosshatched area. It arises because of the use of: (1) the uniform doping assumption (adequate for almost all purposes), creating the horizontal dashed line at the doping level to be used in the analytical expressions; and (2) the specific active layer thickness assumption, creating the vertical dashed line at the thickness to be used in the calculations. The carriers "left over" constitute a shunting resistor in parallel with whatever other resistive shunting terms are present. In FETREN, provision is made for a fixed resistance to shunt the intrinsic device, in addition to the possible substrate current around a Gunn domain. The value of this resistance, assumed proportional to gate width, is assigned to *DR1* at lines 1420 and 1430, and its contribution to the drain current is calculated at lines 6216 (when there is a velocity saturated Region II) and 6862 (when there is no Region II).

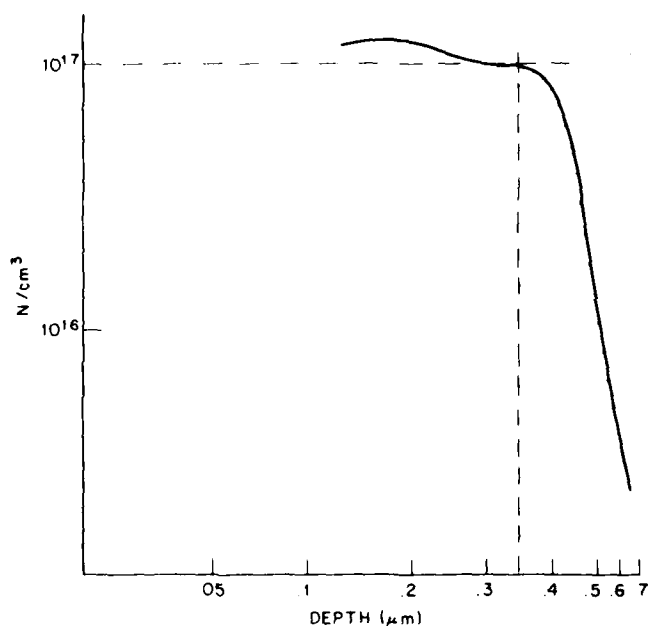


Fig. 5 - Example doping profile showing doping "tail"

In Refs. 2 and 4 it is hinted that typically the finite thickness of the conducting channel in Region II may be disregarded in the solution of Eq. (15). However, the authors carried out the derivation giving the channel the actual thickness it needs to carry the current which is flowing:

$$\delta = \frac{I_{DS}}{qN_D B v_{sat}} \quad (24)$$

where v_{sat} is the assumed electron saturated velocity and δ is the channel thickness. In the program this appears at line 6225. Then at line 6235, the program term *CDR1* is calculated; it represents the fraction of the active layer thickness, a , which is to be used in the next iteration. Notice that *CDR1* was preset to unity at line 1410, outside the loop which determines the operating point and the drain current.

One last adjustment is made after the first time through the operating point drain current loop. Based on the externally applied drain voltage and the preliminary calculated drain current, the power dissipation is calculated as simply the product of those two terms. This is done in the program at line 6230 and 6868. Then the low field mobility value is adjusted for the temperature rise resulting from the bias power dissipation, as indicated in Appendix C, at lines 6240 and 6872. Note that a typical value for the thermal resistance, RTH, of a MISFET is included in the program at line 1450, as suggested in Appendix C, and that inverse proportionality to gate width is assumed. (Thermal modification of mobility may be eliminated by setting thermal resistance to zero at 1450.) A single "first order" correction is all that is needed for the Region II channel thickness and for the low-field mobility. The mobility correction for bias power dissipation is primarily responsible for the downturn of the IV curves in Fig. C2 of Appendix C, while without it the substrate injection current, around the Gunn domain, would cause the curves to rise with increasing drain voltage.

Transconductance

When there is velocity saturation, or when there is a Region II under the gate, the transconductance g_m is calculated according to Statz et al. [10] as:

$$g_m = - \frac{\partial I_{DS}}{\partial V_{GS}} \Big|_{V_{DS} = \text{const}} = \frac{aq\mu_0 N_D W E_s}{V_{PO}} f_c \quad (25)$$

where

$$f_c = \frac{[(1-s) \cosh(\pi L^2/2a)] - (1-p)}{\left\{ \left[2p(1-p) + \frac{E_s L_1}{V_{PO}} \right] \cosh(\pi L_2/2a) \right\} - 2p(1-p)} \quad (26)$$

This calculation is seen at line 6370 in FETREN. It reduces to

$$g_m = aq\mu_0 N_D W (d-s)/L \quad (27)$$

at line 6888 for the gradual channel case. Equations (25) and (27) have included in them the temperature correction of mobility; also Eq. (25) has in it, by way of Eq. (26), the correction for nonzero channel thickness in Region II (picked up at line 6325 where the hyperbolic cosine argument is adjusted).

Resistance

Output Resistance

In addition to the intrinsic output resistance of the MESFET, the resistance associated with the leakage current and the substrate injection current must be considered. It is probably these additional terms, if they are disregarded analytically, which make the measured output resistance much lower than the calculated value. In the computer program FETREN they have been included.

The intrinsic transistor output resistance is developed analytically as

$$r_0 = \frac{\partial V_{DS}}{\partial I_{DS}} \quad (28)$$

In Statz et al. [10] the development of the expression for r_0 is concisely shown, for the assumption of zero-thickness-channel in Region II. The authors did the full derivation, using the actual channel thickness. Some additional terms appear in the expression for r_0 because the depletion thickness in Region II is a function of I_{DS} . The expression from Ref. 10 is:

$$r_{0\text{int}} = \frac{2pV_{PO}}{aq\mu_0 N_D E_s W} \left[\cosh \frac{\pi L_2}{2a} - 1 \right] + \frac{L_1}{aq\mu_0 N_D W (1-p)} \cosh \frac{\pi L_2}{2a} \quad (29)$$

The full expression, using $(a - \delta)$ for the depletion region thickness in Region II, where δ is the value given by Eq. (24), consists of two parts. The first part is

$$r_{01} = r_{0100} \Big|_{(a-\delta)} \quad (30)$$

This part is merely Eq. (29) with $(a - \delta)$ substituted for a . The second part is

$$r_{02} = \frac{2}{\pi q \mu_0 N_D W} \left[\frac{\pi L_2}{2(a - \delta)} \cosh \frac{\pi L_2}{2(a - \delta)} - \sinh \frac{\pi L_2}{2(a - \delta)} \right] \quad (31)$$

The total output resistance is the sum of r_{01} and r_{02} . It is not obvious by inspection, but after numerous computer runs to evaluate the significance of the additional part, r_{02} , it was found that almost all of the drain resistance correction comes from the substitution of $(a - \delta)$ for a in Eq. (29). Therefore, in FETREN, Eq. (30) is used for the intrinsic output resistance when the bias allows a Region II; it appears at line 6390 in the program. When there is no Region II, then L_2 is zero, d replaces ρ , and L_1 is L , so that the intrinsic output resistance is given by the modified second term of Eq. (29):

$$r_0 = \frac{L}{aq\mu_0 N_D W(1 - d)} \quad (32)$$

which is the same as that developed in Van de Ziel [7] and Shockley [3] for the "gradual channel" case. The calculation of Eq. (32) appears in the program at line 6890.

Shunting the intrinsic output resistance are two other resistors. The first is to account for simple surface leakage, and substrate leakage due to overall low resistivity and to the doping tail, as was described in the section entitled The I-V Curves. This term is added in parallel with the intrinsic output resistances at lines 6394 and 6896.

The second shunting resistor is related to the substrate injection current around the Gunn domain. Assuming that most of the drain voltage is dropped across the Gunn domain as described by Eastman and Shur [9], then

$$g_{sub} = \frac{\partial I_{SUB}}{\partial V_{DS}} = \frac{\partial (\text{Eq. 23})}{\partial V_{DS}} = \frac{0.5}{V_{DS}} I_{SUB} \quad (33)$$

The reciprocal of this is the resistance:

$$r_{sub} = 2 \frac{V_{DS}}{I_{SUB}} \quad (34)$$

The value of r_{sub} is calculated in FETREN at lines 6396 and 6892; it is paralleled with the intrinsic output resistance at lines 6398 and 6894.

Parasitic Resistance

The parasitic resistors are those external to the region under the gate, as shown in Fig. 4. The series drain resistor and source resistor, R_D and R_S in Fig. 4, and the method of calculating them were described in the first paragraph of the section entitled The Operating Point; they consist of bulk semiconductor resistance and ohmic metal contact resistance.

The gate resistor (to be involved in noise calculations in a later section) is a bulk resistance of the gate metal. Fukui [5] gives a suitable method of calculating its value. It is calculated in FETREN at line 1370 and used at line 9290 and 9300 in the noise calculations.

Obviously, if the values of these parasitic resistors are known from laboratory measurements, the measured values may be substituted by the program user at lines 1367, 1369, and 1371.

The Gunn domain resistance will be discussed later, in the section entitled Gunn Domain.

Input Resistance

There is still uncertainty in the modeling community about how to calculate R_{IN} of Fig. 1. The qualitative form of R_{IN} versus drain voltage for a particular transistor is shown in Ref. 11 and repeated here among the measured data curves to be discussed later. The qualitative form of C_{IN} versus drain voltage for the same transistor is also given in Ref. 11 and is repeated here among the measure data curves. It is assumed that for drain voltages between about 1 and 4 V the high field at the drain end of the gate is in the transition range between presence and absence of charge accumulation or between presence and absence of a dipole layer or a Gunn domain. This range is difficult to model. For drain voltages higher than about 3 V, however, an inverse proportionality between these two elements is apparent. Their product is in the vicinity of the transit time. So in FETREN the input resistance, R_{IN} , is taken as:

$$R_{IN} = \frac{\tau}{\text{CONST} \cdot C_{IN}} \quad (35)$$

where τ is the transit time to be discussed in the section entitled Transit Time. The resistance is calculated and called RINPHS at lines 6495 (if there is a Region II) and 7110 (if there is no Region II) for the case when the capacitance calculation disregards the Gunn domain; it is calculated and called RINSH at line 8662 if a Gunn domain is considered. In the interest of having an input resistance calculation which resembles measured data for low drain voltage, the transit time for a drain voltage of $V_{PO}/2$ is used when the drain voltage is any value less than $V_{PO}/2$.

Capacitance

Input Capacitance or Gate-to-Source Capacitance

The input capacitance, C_{IN} , has two different names (and derivations) in FETREN; it is CSG at line 6491 and 7100 (no Gunn domain) and CGS at line 8631 (with Gunn domain). In both cases the capacitance is developed as:

$$C_{IN} = \left. \frac{\partial Q}{\partial V_{GS_{int}}} \right|_{V_{DS_{int}} = \text{const.}} \quad (36)$$

However, the assumptions made to determine the total charge, Q , are different.

The calculation for CSG, assuming no Gunn domain, is from Pucel et al. [4] and considers only the charge in Region I and II directly under the Gate, plus a fringing term which is independent of bias.

The calculation for CGS is from Shur [12] and considers the charge in: (a) the depleted area under the gate, Q_c ; (b) the extended depletion area beyond the gate toward the drain, Q_e , when the high-field domain is present; and (c) the depletion area in the high-field domain itself, Q_{dom} , when it is present. Figure 6 shows these areas conceptually. The theory of Shur [12] also provides a valid derivation of the input capacitance when the drain-to-source voltage approaches zero; so, for small drain voltage:

$$C_{cs0} = \frac{L \cdot W}{2\sqrt{2}} \left(\frac{\epsilon_0 \epsilon_r q N_D}{V_B - V_G} \right)^{1.2} \quad (37)$$

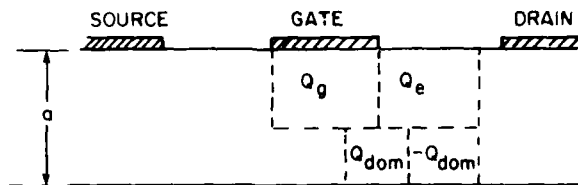


Fig. 6 - Conceptual charge arrangement for capacitance calculations when Gunn domain is present

and, for large drain voltage:

$$C_{gs} = LW \left[\frac{\epsilon_0 \epsilon_r q N_D}{2(V_{Bi} - V_G)} \right]^{1/2} + 1.46(PCDG) \epsilon_0 \epsilon_r W \left(\frac{N_D}{n_{cr}} \right)^{1/4} \left(\frac{V_{Bi} - V_G}{V_{ds}} \right)^{1/2} \left[1 - \frac{V_{Bi} - V_G}{V_{ds}} \right]. \quad (38)$$

The constant $PCDG$ (set at line 8000 in FETREN) has been selected for best agreement with available measured data. In the computer program, an interpolation routine has been provided to calculate a value for C_{gs} when the drain voltage falls between zero and half the pinch-off voltage. Experimental data indicate that in this range neither Eq. (37) nor (38) predicts the capacitance value accurately. The same experimental data have been used to establish the interpolation procedure, performed in FETREN between line numbers 8710 and 8780.

Feedback Capacitance or Gate-to-Drain Capacitance

The theory of Pucel et al. [4] makes no provision for a bias dependent feedback capacitance, C_{FB} in Fig. 1. It is there treated as a fixed parasitic capacitance, which will be described in the next subsection. Since measured data show C_{FB} to be bias dependent, in general, the theory of Shur [12] is used to calculate values and provide them as CDG in FETREN. For the same reasons as were outlined in the preceding subsection, two ranges of validity of the derivation exist. The value of capacitance which is valid for drain voltage approaching zero is equal to the corresponding gate-to-source capacitance because of symmetry at zero drain voltage.

$$C_{dg0} = C_{gs0} \quad (39)$$

given by Eq. (37). The value for large drain voltage is:

$$C_{dk} = 1.46(PCDG) \epsilon_0 \epsilon_r W \left(\frac{V_{Bi} - V_G}{V_{ds}} \right)^{1/2} \left(\frac{N_D}{n_{cr}} \right)^{1/2}. \quad (40)$$

Again, available experimental data have been used to interpolate between Eqs. (39) and (40) for drain voltages between zero and half the pinch-off voltage.

Parasitic Capacitances

As suggested in Pucel et al. [4], a method of calculating the fixed "interelectrode" capacitances is available in Smythe [13], with some interpretation. Figure 7 gives the dimensions which are used in the FETREN calculations. The capacitance between any two electrodes is given by:

$$C = W (\epsilon_r + 1) \epsilon_0 \frac{K(\sqrt{1-k^2})}{K(k)}. \quad (41)$$

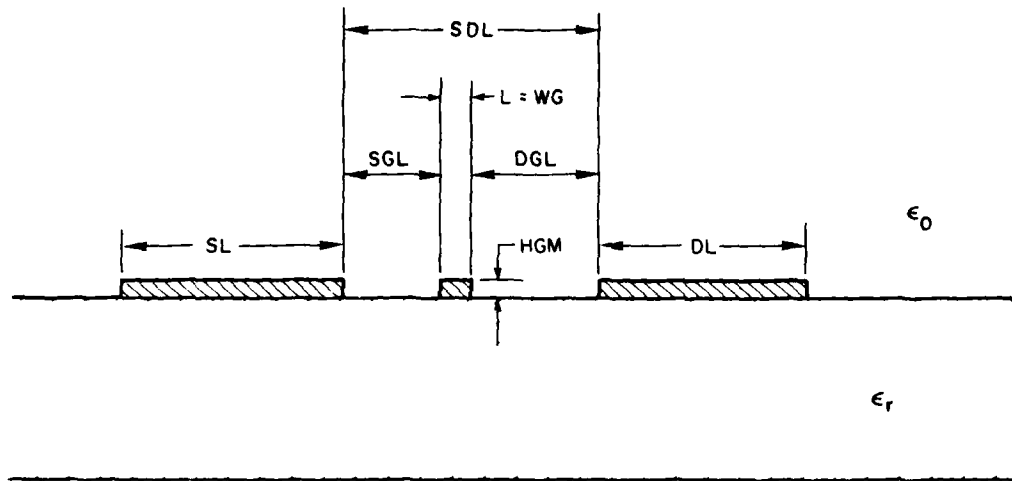


Fig. 7 - Dimensions for interelectrode capacitance calculations

where $K(k)$ is the complete elliptic integral of the first kind in terms of the modulus k . The moduli k , derived from Smythe [13] for the relevant geometries, are as follows:

$$\text{Drain-Gate, } k_{dg} = \left[\frac{(DL + DGL + WG)(DGL)}{(DL + DGL)(DGL + WG)} \right]^{1/2} \quad (42)$$

$$\text{Source-Gate, } k_{sg} = \left[\frac{(SL + SGL + WG)(SGL)}{(SL + SGL)(SGL + WG)} \right]^{1/2} \quad (43)$$

and

$$\text{Source-Drain, } k_{sd} = \left[\frac{(SL + DL + SDL)(SDL)}{(SL + SDL)(DL + SDL)} \right]^{1/2} \quad (44)$$

In FETREN a numerical approximation for the complete elliptic integral of the first kind, $K(k)$, is included as a subfunction CEIFK, calculated at lines 9100 to 9136. This was done in keeping with the objective of using closed form solutions throughout. The numerical approximation used was:

$$K(k) = [A_0 + A_1(1 - k^2) + A_2(1 - k^2)^2] + \ln \left[\frac{1}{1 - k^2} \right] [B_0 + B_1(1 - k^2) + B_2(1 - k^2)^2], \quad (45)$$

where

$$A_0 = 1.3862944$$

$$A_1 = 0.1119723$$

$$A_2 = 0.0725296$$

$$B_0 = 0.5$$

$$B_1 = 0.1213478$$

$$B_2 = 0.0288729,$$

giving an error of less than 3×10^{-5} in the value of $K(k)$, which is orders of magnitude better accuracy than needed. The values for these fixed capacitances are calculated between lines 1315 and 1351. The printout for them is at line 1393. Perhaps the most significant of these terms is CFSD, the output capacitance (C_0 in Fig. 1).

Sidewall Capacitance

Neither theory discussed so far for capacitance calculations (Shur [12] or Pucel et al. [4]) provides for the extension of the depletion region from under the gate in the direction of the source. In Cooke [14], for depletion depth less than the full active layer thickness, the charge depleted from the quarter-circle adjacent to the gate is:

$$Q_{SW} = q N_D \pi \frac{z^2}{4} W; \quad (46)$$

and for an abrupt junction from Poisson's equation, the voltage is:

$$V = \frac{z^2 q N_D}{2 \epsilon_0 \epsilon_r}, \quad (47)$$

so that the capacitance is

$$C_{SW} \Big|_{V \leq V_{PO}} = \frac{dQ_{SW}}{dV} = \frac{\pi}{2} \epsilon_0 \epsilon_r W, \quad (48)$$

where z is the radius of the sidewall depletion area (see Fig. 3). Also, from Cooke [14], when the gate-to-source voltage is larger than the pinch-off voltage, an approximate value for the sidewall capacitance is given by:

$$C_{SW} \Big|_{V \geq V_{PO}} = \epsilon_0 \epsilon_r W \sin^{-1} \sqrt{\frac{V_{PO}}{V}}. \quad (49)$$

This capacitance term is calculated in the computer program FETREN between lines 6500 and 6520. It is printed out as the third term in line 6545. This capacitance appears as C_{EX} in Fig. 1. Note also, however, that the interelectrode capacitance between gate and source metal may be significant in C_{EX} .

Pad Capacitance

It is also possible to have significant bond pad-to-source or bond pad-to-ground capacitance. Cooke [15] discusses of the pad-to-source capacitance. It consists of capacitance to the substrate offset by the Schottky barrier capacitance formed on top of the buffer or substrate material. The pad-to-ground capacitance is predominantly a "parallel plate" capacitance which may be significant when very thin substrate are used. Those terms are process dependent and may not be significant; they are not included in FETREN, but the user should take notice of their possible existence, estimate their magnitude, and include them separately if they are significant.

Gunn Domain

As described earlier, the presence of a stationary dipole domain, or a Gunn domain, near the drain end of the gate has a profound effect on the input capacitance C_{IN} , the input resistance R_{IN} , and the feedback capacitance C_{FB} . If a Gunn domain can exist, there is no indication in the FETREN printout—this is probably the most common case. The element values to use are those calculated assuming the presence of the Gunn domain—namely, CGS, RINSH, and CDG. Two additional terms are calculated and printed out for the "Gunn domain" case: CDOM, the domain capacitance; and RDOM, the negative resistance associated with the domain, both discussed in Shur [12]. They are calculated at lines 8460 and 8490 in the computer program, and printed out at line 8640. These terms are shown in Fig. 1 as CDOM and RDOM; they are not by themselves dominant terms in the equivalent

circuit—the domain effects on the other three terms, mentioned above, appear to be much more significant.

If a Gunn domain cannot exist, the printout "NGD" (No Gunn Domain) appears. In this case, the element values to use are those calculated assuming no Gunn domain—namely, CSG for C_{IN} , RINPHS for R_{IN} , and CFDG for C_{FB} .

The calculation for C_{IN} and C_{FB} , from Shur [12], for drain voltage approaching zero (CGSO and CDGO, respectively) is done at lines 8120 to 8140 and printed out at line 8180.

The criteria discussed in Yamaguchi et al. [16] are used in FETREN to determine whether a Gunn domain can or cannot exist. The analysis was done for planar geometry, like that used for MES-FETs. Poisson's equation (Eq. (50)), the current continuity equation (Eq. (51)), and the current density expression (Eq. (52)) were solved numerically by using a finite difference scheme:

$$\nabla^2 \Phi = -\frac{q}{\epsilon} (N_D - n), \quad (50)$$

$$\frac{\partial n}{\partial t} = \nabla \cdot \mathbf{J}, \quad (51)$$

$$\mathbf{J} = n\mathbf{v} + D\nabla n, \quad (52)$$

where n is volume electron density, t is time, \mathbf{J} is current density, \mathbf{v} is drift velocity, and D is diffusion coefficient. The result relative to domain formation was pleasantly simple. For a given gate-to-source voltage, the depletion layer width W_{th} , at which the maximum field strength just equals the threshold field E_{th} , for bulk negative differential mobility, is given by:

$$W_{th} = \left\{ \frac{2\epsilon}{qN_D} [V_{Bi} - V_{GS_{int}} + (E_{th} \cdot L)] \right\}^{1/2}. \quad (53)$$

Therefore, if the total active layer thickness a is less than the threshold width W_{th} , a Gunn domain cannot form.

The calculation of W_{th} is at line number 8100 in FETREN, and the test of W_{th} relative to the active layer thickness is at line 8105. If a Gunn domain can exist, the program proceeds to calculate the relevant parameter; if a Gunn domain cannot exist, the printout "NGD" appears but the program proceeds, anyway, into the calculations related mostly to the domain case. This is done to make available to the program user the value for CGSO and CDGO, calculated at line 8137 and printed out at line 8180; and the value of transconductance from Shur [12] for small drain voltage, for general information. This value of transconductance is calculated in the computer program as BGM at line 8220, and printed out at line 8330.

Incidentally, if the active layer thickness is more than twice W_{th} , the Gunn domain can even propagate. In summary the following classification can be made:

$$\begin{aligned} a < W_{th} & \quad \text{No Gunn domain,} \\ W_{th} < a < 2W_{th} & \quad \text{Stationary Gunn domain,} \\ a > 2W_{th} & \quad \text{Propagating Gunn domain.} \end{aligned}$$

Active layer thickness sufficient for domain propagation is normally not seen in microwave MESFETs; there is no provision in FETREN for such cases.

Transit Time

In the velocity saturated region (Region II) of a GaAs MESFET, the transit time is

$$\tau_2 = \frac{L_2}{v_{sat}} \quad (54)$$

In Region I,

$$\tau_1 = \frac{L_1}{v_{average}} \quad (55)$$

where an average velocity can be determined as

$$v_{average} = \mu_0 E_{average} = \mu_0 \frac{V_{DS1}}{L_1} \quad (56)$$

and where $V_{DS1} = V_{PO} (p^2 - s^2)$ from Eq. (17), and L_1 is obtained from the iterative process described earlier and has the value indicated by Eq. (12).

If there is no region II, then d is substituted for p in the expression for τ_1 , and there is no τ_2 . The substitution of d for p is here analogous to the similar substitution in the drain current expressions (5) and (21).

In the computer program FETREN, the calculations for transit time appear at line 6493 if there is a Region II, and at line 7105 if there is no Region II.

NOISE CALCULATIONS

The method of calculation of the noise parameters is taken directly from Pucel et al. [4]. In FETREN, printout has been arranged (at line 9340) for: (a) noise figure in decibels if the driving impedance is Z_S , given at line number 9156 (BFZSD); (b) noise figure in decibels for optimum noise driving impedance (BFMIND); (c) the optimum noise driving resistance (BRSO); and (d) the optimum noise driving reactance (BXS0).

The noise calculations appear as a separate subroutine (ANF) between lines 9150 and 9343. The gate metal thickness, HGM, is assigned at line 944, outside the subroutine.

COMPARISON WITH MEASUREMENTS

Figures 8 through 13 show measured and calculated values of the predominantly bias dependent elements of a particular GaAs MESFET. The measurements were done at NRL, and the experimental results were reported and discussed by Willing et al. [11]. The calculated values are from FETREN, using only the material and dimensional parameters given in Table 2.

The overall agreement between measured and calculated results is not perfect, but it is reasonably self-consistent and is better than any other method known over the full range of both of the bias voltages. No noise figure measurements were made on this device, but the calculated values of the noise parameters are included in the sample printout in Appendix A.

The values for the fixed resistances and capacitances are given in the sample printout in Appendix A. They also are in reasonable agreement with measured values.

Calculations and measurements of various parameters have been compared by using several other transistors for more limited, special cases. Similar fair agreement between the two is typical.

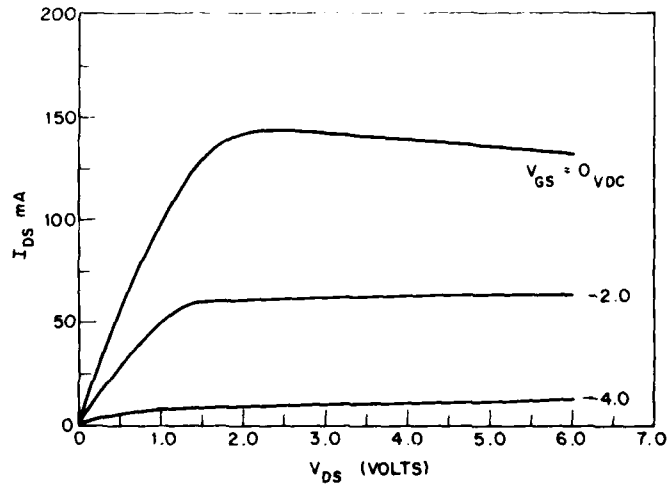


Fig. 8(a) — Measured static I_{ds} - V_{ds} characteristics

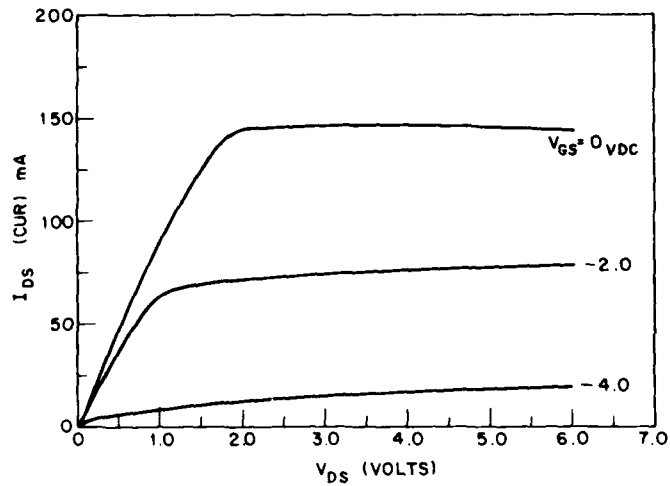


Fig. 8(b) — Calculated static I_{ds} - V_{ds} characteristics

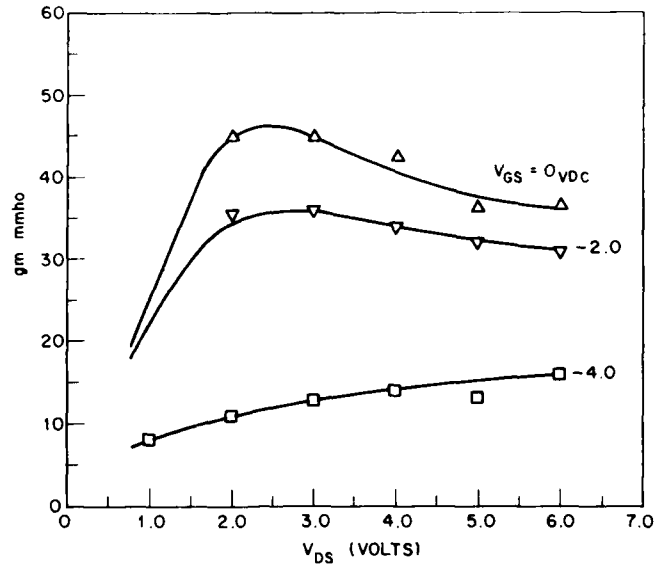


Fig. 9(a) - Measured transconductance

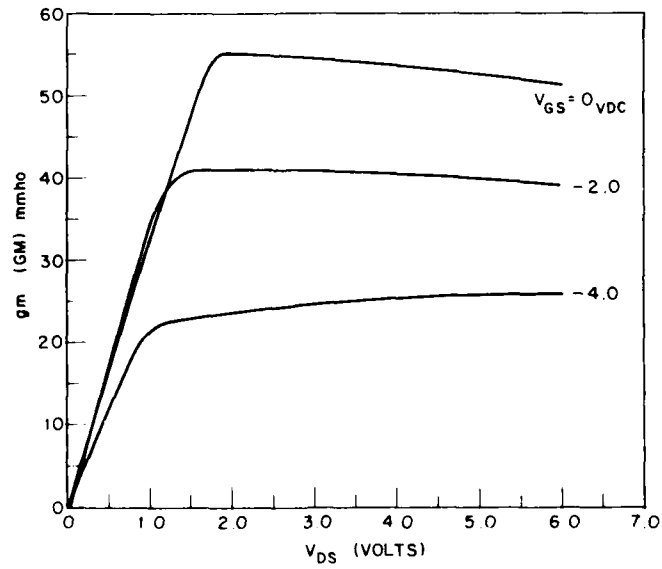


Fig. 9(b) - Calculated transconductance

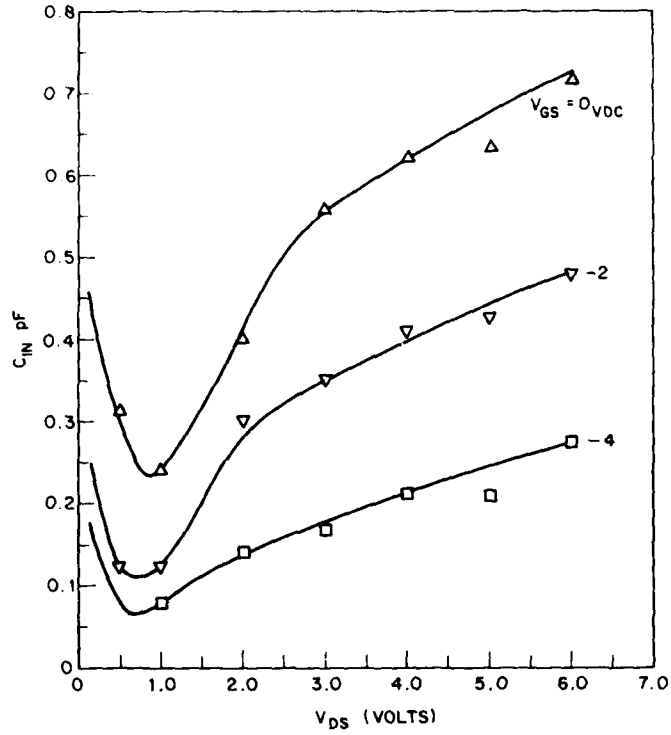


Fig. 10(a) - Measured input capacitance

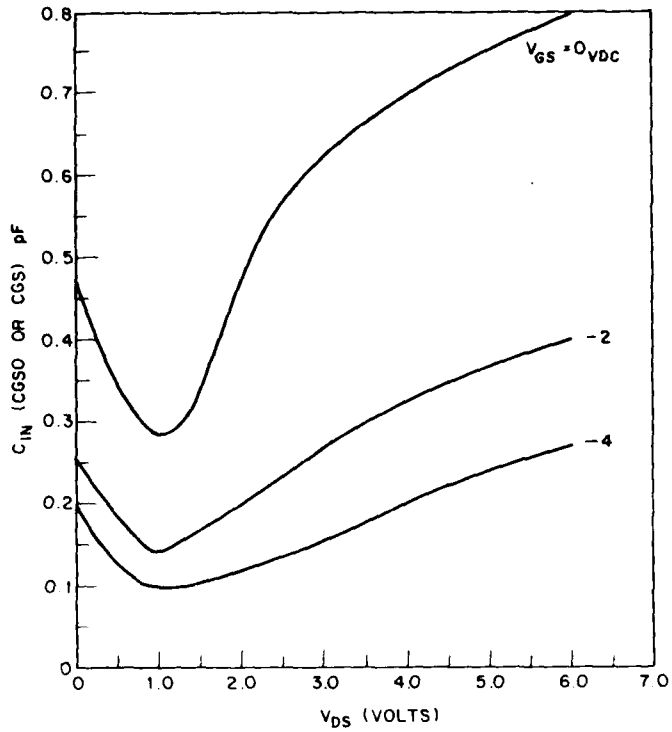


Fig. 10(b) - Calculated input capacitance

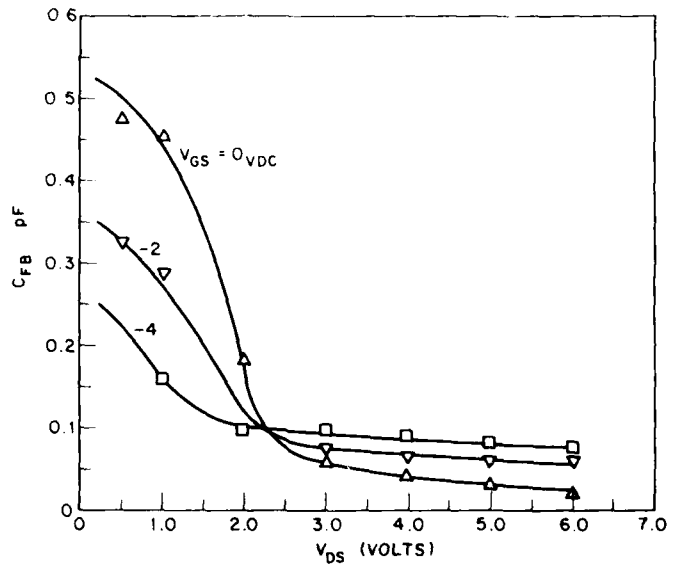


Fig. 11(a) — Measured feedback capacitance

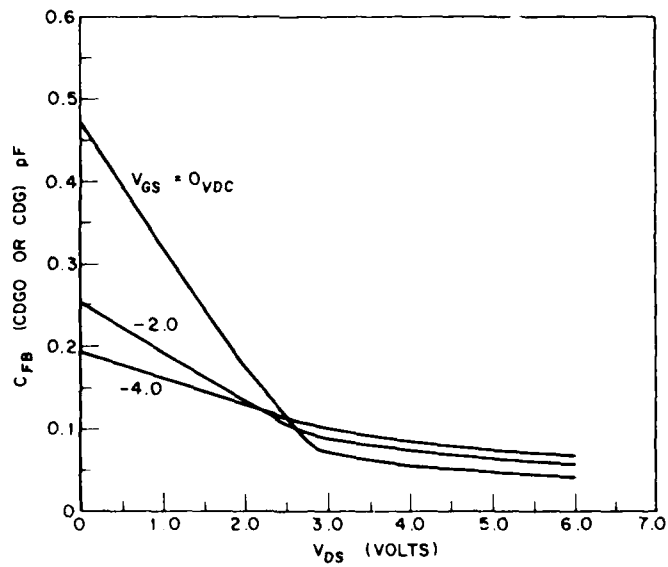


Fig. 11(b) — Calculated feedback capacitance

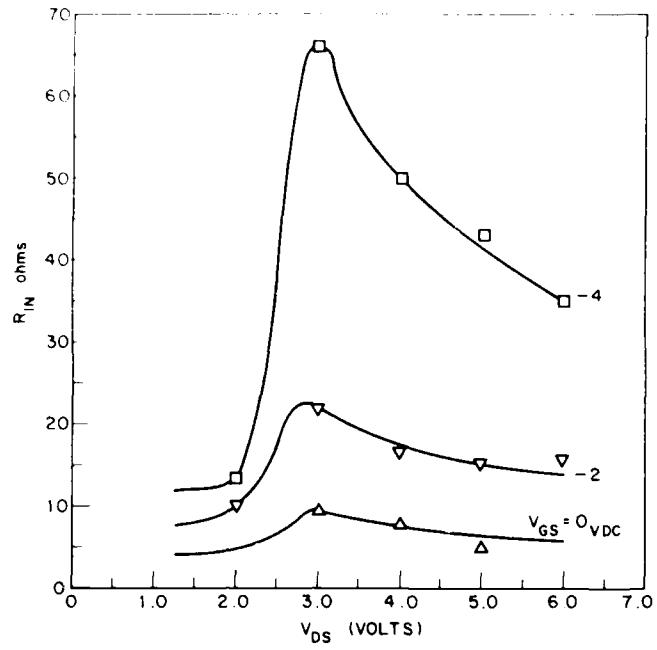


Fig. 12(a) - Measured input resistance

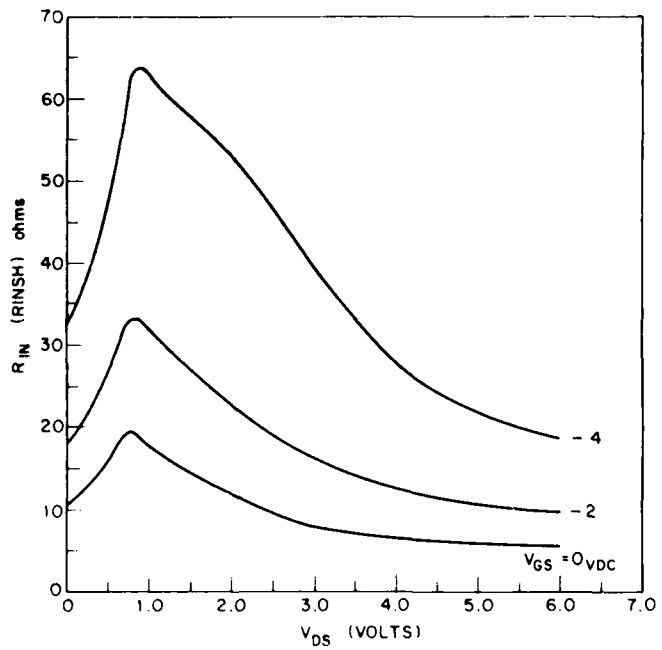


Fig. 12(b) - Calculated input resistance

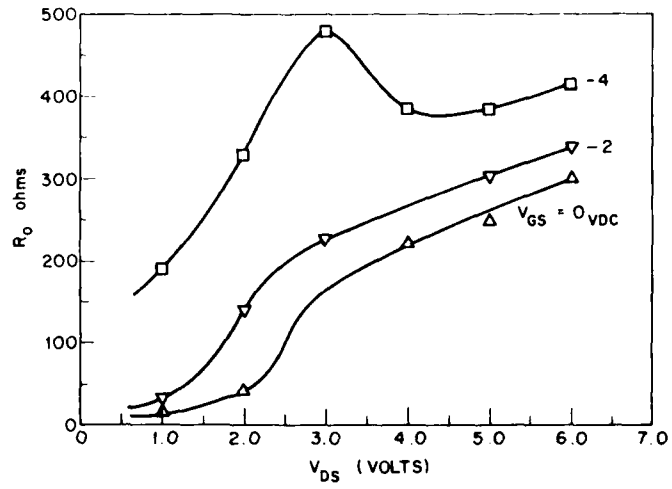


Fig. 13(a) — Measured output resistance

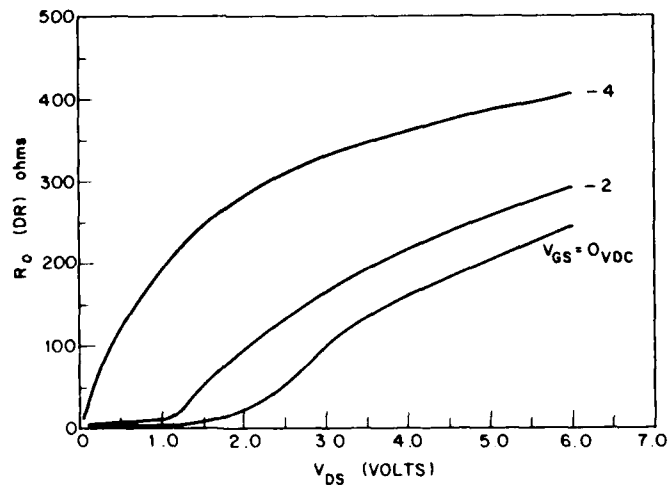


Fig. 13(b) — Calculated output resistance

Table 2 — Experimental GaAs MESFET — Physical Parameters

Gate Width, W	600 μm
Gate Length, L	1.7 μm
Active Layer Thickness, a	0.315 μm
Donor Impurity Concentration, N_D	$7.5 \times 10^{16}/\text{cm}^3$
Low Field Mobility, μ_0	4240 $\text{cm}^2/(\text{V} \cdot \text{s})$
Assumed Saturation Field, E_s	3.2 kV/cm
High Field Saturation Velocity in Gunn Domain	$0.8 \times 10^7 \text{ cm/s}$
Gate Metal Thickness, HGM	0.2 μm
GaAs Relative Dielectric Constant, ϵ_r	12.9
Source Metal Length, SL	75 μm
Drain Metal Length, DL	25 μm
Drain-to-Gate Spacing, DGL	2.15 μm
Source-to-Gate Spacing, SGL	2.15 μm
Drain Shunt Resistance, $DR1$	650 ohms
Thermal Resistance, RTH	117°C/W
Characteristic Doping Density, n_{cr}	$3 \times 10^{15}/\text{cm}^3$
Schottky Gate Built-in Voltage, V_{Bi}	0.8 V
Diffusion Coefficient, D	45 cm^2/s

CRYOGENIC CONSIDERATIONS

With the material parameters included in the computer program FETREN, it would seem a relatively simple matter to calculate the full equivalent circuit and the noise performance of a MESFET at any temperature. It should only be necessary to know how the material parameters vary with temperature. This may indeed be true—and it may not. The variation of the noise sources themselves with temperature is not well established; also the difficulty and inaccuracy associated with cryogenic measurements on MESFETs complicates correlation with calculations, especially if tuning must be done, with the tuners themselves at cryogenic temperatures. Weinreb [17] reported that the correlation between both room temperature and cryogenic (20 K) values of measured minimum noise figure were in good agreement with calculated values by Pucel et al. [4], the method used in FETREN; but at the same time there were extremely large discrepancies in various other noise coefficients, raising questions about the validity of the noise figure calculation as well. This area needs further research.

DISCUSSION

The user of FETREN should be familiar with FORTRAN programming and editing. Several of the input parameters must be written in by the user before running the program. The inputting procedures can be reprogrammed by the user to suit his own purposes.

The cost of the sample run in Appendix A was a bit less than \$8. It provided 154 calculated points, at a cost of about a nickel a point.

At NRL the output information from FETREN has been used as input information for the well-known time domain analysis program, SPICE. Large-signal, time domain analysis of a 2 GHz MESFET amplifier was carried out. The fundamental output signal and its first three harmonics showed good agreement with measured data. This was so in spite of the fact that the FET model in SPICE is the Schichman-Hodges model of a junction FET, simulated with calculated MESFET values from FETREN.

It is possible, therefore, to go from semiconductor material parameters and dimensions to large signal (as well as small signal, low noise) performance with no experimental intermediate steps. This is

true for GaAs MESFETs at or near room temperature. It would appear to be a fairly simple matter to modify the program FETREN to be suitable for other semiconductor materials; it is probably also possible to modify it for cryogenic calculations, but neither of these has yet been done.

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Appendix A
Program FETREN Listing, Sample
Printout, and Notation List

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100 PROGRAM FETREN(INPUT,OUTPUT)
150 GO TO 917
200 200 PRINT 300
300 300 FORMAT(ENTER A,CND,CND1,WG,W,HGM)
400 READ A,CND,CND1,WG,W,HGM
500 500 PRINT 600
600 600 FORMAT(ENTER IG,VGO,DVG)
700 READ IG,VGO,DVG
800 800 PRINT 900
900 900 FORMAT(ENTER ID,VDD,DVD)
910 910 PRINT 915
915 915 FORMAT(ENTER A,CND,FD)
916 READ A,CND,FD
917 917 A=.315
918 CND=7.5E16
919 FD=.424
922 CND1=CND/10.**16
924 CND2=CND1
926 TNOM=300.
928 FD=FD*((TNOM/300.))**(-.7)
930 WG=1.7
940 W=600.
942 W1=W*.001
944 HGM=.2
946 WG1=WG*1E-4
950 IG=3
960 VGO=0.
970 DVG=-2.
1000 ID=3
1010 VDD=1.
1020 DVD=2.
1100 GEL=1.602E-19
1200 EPSD=8.854E-12
1280 EPS=12.9
1285 SEIF=0
1290 CF=1.56
1300 SL=75.
1303 DL=25.
1306 DGL=2.15
1309 SGL=2.15
1312 SDL=SGL+WG+DGL
1315 CAPCO=EPSD*(1.+EPS)*W*1.E6
1321 AKDG=SQRT(((DL+DGL+WG)*DGL)/((DL+DGL)*(DGL+WG)))
1324 AKPDG=SQRT(1.-AKDG*AKDG)
1327 CFDG=CAPCO*CEIFK(AKPDG)/CEIFK(AKDG)
1333 AKSG=SQRT(((SL+SGL+WG)*SGL)/((SL+SGL)*(SGL+WG)))
1336 AKPSG=SQRT(1.-AKSG*AKSG)
1339 CFSG=CAPCO*CEIFK(AKPSG)/CEIFK(AKSG)
1345 AKSD=SQRT(((SL+DL+SDL)*SDL)/((SL+DL)*(DL+SDL)))
1348 AKPSD=SQRT(1.-AKSD*AKSD)
1351 CFSD=CAPCO*CEIFK(AKPSD)/CEIFK(AKSD)
1359 RDN=W1*A*CND1**.82
1360 RCD=2.1/(W1*A**.5*CND2**.66)
1362 RCHS=1.1*SGL/RDN
1364 RCHD=1.1*DGL/RDN
1366 RS=RCD+RCHS
1368 RD=RCD+RCHD
1370 RG=(17.*(W1/4.))**.2)/(WG+HGM+W1)
1372 PRINT 1380 ,RG,RS,RD
1380 1380 FORMAT(RG=,F4.1, ; RS=,F4.1, ; RD=,F4.1, )
1393 PRINT 1396,CFDG,CFSG,CFSD
1396 1396 FORMAT(CFDG=,F7.4,PF ; CFSG=,F7.4,PF ; CFSD=,F7.4,PF )

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1397 PRINT 1398
1398 1398 FORMAT(♦ ♦)
1400 VPD=DEL♦A♦A♦CND♦1.E-6/(2.♦EPSD♦EPS)
1410 CDR1=1.
1415 CDR2=3.
1420 RSHUNT=650.
1430 DR1=RSHUNT♦(600./W)
1450 RTH=70000./W
1500 ES=3.9
1550 PRINT 1560
1560 1560 FORMAT(♦ VG VD CSW CUR GM DR CSG♦)
1570 PRINT 1580
1580 1580 FORMAT(♦ ♦)
1605 F=FD
1610 AVELSAT=.8E5
1615 CNCR=3.E15
1620 AK=4.
1650 1650 PI=3.1415927
2000 XI=.1♦ES♦WG/VPD
2100 VBI=.8
2200 DO 1100 I=1,IG
2300 VG=VGD+(I-1)♦DVG
2400 T=1.
2600 WSN=(VBI-VG)/VPD
2700 IF(WSN.GE.0.)GO TO 1300
2800 PRINT 1200
2900 1200 FORMAT(♦VG GT VBI LINE 2600♦)
3000 RETURN
3100 1300 S=SQRT(WSN)
3150 ZP=S
3200 IF(S.LE.1.)GO TO 1500
3300 PRINT 1400
3400 1400 FORMAT(♦S GT 1.0 LINE 3100♦)
3500 RETURN
3600 1500 BET=2.♦A/PI
3800 DO 1100 J=1,ID
3900 VD=VDD+(J-1)♦DVD
3901 3901 S=ZP
3902 DET=1.5
3918 3918 PL=S
3920 PH=.99999
3930 VELSAT=ES♦F♦1.E5
3935 GD=A♦DEL♦F♦CND
3940 AIS=GD♦W♦ES♦.1
3950 1600 STEP=(PH-PL)/10.
4000 IF(STEP.GT.1.E-8)GO TO 1800
4100 PRINT 1700
4200 1700 FORMAT(♦STEP LE 1E-8♦)
4300 RETURN
4600 1800 DO 1900 K=1,11
4700 P=PL+(K-1)♦STEP
4800 F1=P♦P-S♦S-(P♦3-S♦3)♦2./3.
4900 AL1=GD♦W♦VPD♦F1/AIS/(1.-P)
5000 DEL1=VPD♦(P♦P-S♦S)
5030 XYZ=(WG-AL1)/BET
5040 XYZ=XYZ/CDR1
5060 XYA=EXP(XYZ)-EXP(-XYZ)
5080 XYB=XYA/2.
5090 XYB=XYB♦CDR1
5100 DEL2=VPD♦BET♦(XI/WG)♦XYB
5120 DEL2=DEL2♦CDR2
5200 DEL=VD-DEL1-DEL2-AIS♦(1.-P)♦(RS+RD)
5300 IF(ABS(DEL).LT.1.E-4)GO TO 2200
5400 IF(DEL.GT.0.)GO TO 2100
5500 1900 CONTINUE
5600 PRINT 2000

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5700 2000 FORMAT(ND CONVERGENCE IN 11 ITERATIONS)
5750 RETURN
5800 2100 PL=P-STEP
5900 PH=P
6000 GO TO 1600
6010 2200 S2=SQRT((VBI-VG+AIS*(1.-P)+RS)/VPO)
6020 IF (ABS(S2-S).LT.1.E-4) GO TO 6100
6030 S=S2
6040 GO TO 3918
6100 6100 IF (AL1.GT.WG) GO TO 6620
6150 AL2=WG-AL1
6151 BL21=AL2/AL1
6200 CUR=AIS*(1.-P)
6203 CVD=VD-CUR*(RS+RD)
6206 CSUBA=AK*((CND/1.E17)**.25)*((CVD**.5)**.5)/1.E6
6209 CSUB=CSUBA*(AVLSAT/.8E5)*((CNCR/3.E15)**.25)
6212 CUR=CUR+CSUB
6216 CUR=CUR+VD/DR1
6220 IF (DET.GT.2.) GO TO 6320
6225 DELT=CUR*1.E6/(DEL*CND*W*VELSAT)
6230 PD=VD*CUR
6235 CDR1=(A-.25*DELT)/A
6240 F=FO*(((TNOM+PTH*PD)/TNOM)**(-.7))
6245 DET=DET+1.
6250 GO TO 3918
6320 6320 X=F1*(WG-AL1)/2./A
6325 L=X/CDR1
6330 Y=(EXP(X)+EXP(-X))/2.
6340 AN=((1.-S)*Y)-(1.-P)
6350 AD=(2.*P*(1.-P)+XI*AL1/WG)*Y
6360 DENA=AD-2.*P*(1.-P)
6370 GM=AIS*AN/DENA/VPO
6390 DR=VPO*DENA/AIS/(1.-P)
6394 DR=(DR1*DR)/(DR1+DR)
6396 RSU=2.*CVD/CSUB
6398 DR=(DR+RSU)/(DR+RSU)
6400 F1=P*P-S*S-(P**3-S**3)*2./3.
6410 FG=AN/DENA
6420 F2=((P**3-S**3)*2./3.)-(P**4-S**4)/2.
6430 FC1A=(2.*P*P*(1.-P)*(1.-P)+F2)/(1.-P)
6440 FC1B=S*(1.-S)
6450 FC1=2.*AL1*(FG*FC1A-FC1B)/F1/A
6460 FC2A=2.*(WG-AL1)*FG/A
6470 FC2B=1.-2.*P*FG
6480 Z=(EXP(X)-EXP(-X))/(EXP(X)+EXP(-X))
6485 FC2C=(2.*WG*P/A/XI/Y)+Z
6490 FC2=FC2A+FC2B+FC2C
6491 CSG=EPS*EPSD*W*(FC1+FC2+CF)*1.E6
6492 IF (CSG.LT.(CFSG/2.)) CSG=CFSG/2.
6493 TAU=(AL1*AL1/(F*VPO*(P*P-S*S)))+10.*(WG-AL1)/VELSAT
6494 BFC=FC1+FC2+CF
6495 PINPHS=TAU/CSG
6496 IF (VD.EQ.0.) RINPHS=TAU/CFSG
6498 6498 IF (SEIF.EQ.10) GO TO 6560
6499 IF (SEIF.EQ.20) GO TO 6560
6500 6500 CVGP=VBI-VG+CUR+RS
6505 IF (CVGP.GT.VPO) GO TO 6520
6510 CSW=PI*EPS*EPSD*W*1.E8/2.
6515 GO TO 6545
6518 6520 CSW1=SQRT(VPO/CVGP)
6519 CSW2=ASIN(CSW1)
6520 CSW=EPS*EPSD*W*1.E8
6521 CSW=CSW*CSW2
6545 6545 PRINT 6550,VG,VD,CSW,CUR,GM,DR,CSG
6550 6550 FORMAT(F6.3,2X,F7.4,2X,F6.3,3X,F5.4,3X,F6.4,1X,F8.1,2X,E10.3)

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6560 6560 GO TO 8000
6570 6570 ABCD=3.
6580 PRINT 7130,TAU,RINPHS
6585 CALL ANF(P,S,F1,DENA,BL21,FG,XI,A,AL2,PI,F,VEL,WG,Y,CSS,PS,PG,GM,
6586+TNOM,BFC,RINSH)
6590 SEIF=0
6600 1100 CONTINUE
6610 RETURN
6620 6620 CURL=0.
6621 AL2=0.
6622 BL21=0.
6625 CURH=AIS
6630 2 STEP=(CURH-CURL)/10.
6635 IF (ABS(STEP).GT.1.E-8)GO TO 3
6637 GO TO 6500
6640 PRINT 7
6645 7 FORMAT(♦STEP LE 1E-8,NO.2♦)
6650 RETURN
6655 3 DO 4 L=1,11
6660 CUR=CURL+(L-1)♦STEP
6665 SSQ=(VBI-VG+CUR♦RS)/VPO
6670 DSQ=(VBI-VG+VD-CUR♦RD)/VPO
6675 F2D=DSQ-SSQ-2.♦(DSQ♦♦1.5-SSQ♦♦1.5)/3.
6680 E1=CUR-GD♦W♦VPO♦F2D/WG
6685 IF (ABS(E1).LT.1.E-4)GO TO 5
6690 IF (E1.GE.0.)GO TO 6
6700 4 CONTINUE
6702 GO TO 6500
6705 6. CURL=CUR-STEP
6710 CURH=CUP
6715 GO TO 2
6720 5 S=SQRT(SSQ)
6725 D=SQRT(DSQ)
6830 F1D=D♦D-S♦S-(2./3.♦♦D♦♦3-S♦♦3)
6835 CUR=GD♦W♦VPO♦F1D/WG
6840 CVD=VD-CUR♦(RS+RD)
6845 CSUBA=AK♦♦(CND♦1.E17)♦♦.25)♦♦(CVD♦♦.5)♦♦♦1.E6
6850 CSUB=CSUBA♦(AVELSAT♦.8E5)♦♦(CNER♦3.615)♦♦.25)
6860 CUR=CUR+CSUB
6862 CUR=CUR+VD♦DR1
6864 IF (DET.GT.2.)GO TO 6888
6868 PD=VD♦CUR
6872 F=FD♦♦(TNOM+PTH♦PD♦TNOM)♦♦(-.7)
6876 DET=DET+1.
6880 GO TO 3918
6888 6888 GM=GD♦W♦(D-S) WG
6890 IF (WG♦W♦GD ♦1.-D)
6892 PSU=2.♦EVD♦CSUB
6894 DR=DR♦PSU♦♦(DR+PSU)
6896 DR=DR1♦DR♦♦(DR1+DR)
6900 FG=♦1.-S♦♦1.-D♦♦♦2)
6950 F2=♦D♦♦3-S♦♦3)♦2.♦3.♦♦(D♦♦4-S♦♦4)♦2.♦
7000 FC1A=(2.♦D♦D♦♦1.-D♦♦♦1.-D♦♦+F2)♦♦1.-D)
7050 FC1=(FG♦FC1A-♦♦1.-D♦♦♦2.♦WG♦F1D)♦A
7060 BFC=FC1♦CF
7100 CIG=EPS♦EPS♦D♦W♦♦(FC1+CF)♦1.E6
7102 IF (CIG.LT.(CFIR♦2.♦CIG=CFIG♦2.
7105 TAU=MG♦WG ♦E♦VPO♦♦D♦D-S♦♦)
7110 RINPHS=TAU♦CIG
7115 IF (VD.EQ.0.)RINPHS=TAU♦CFIG
7130 7130 FORMAT(♦ TAU=♦F8.2♦♦F1E3 ♦ RINPHS=♦F8.2♦♦DHM)♦
7200 GO TO 6498
8000 8000 FCIG=.32
8040 RES=AVELSAT F♦♦1.E-5

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8735 VI=VPOT
8737 GO TO 3901
8740 8740 SLOP1=(CDG-CDG0)/VD
8741 SLOP2=(CGSD)/(-2.)*VDF1
8742 SLOP3=(CGS-(CGSD/2.))*VPO*2.5/7
8743 YINT=(CGSD/2.)-(SLOP3*VDF1)
8745 CEIF=20
8750 VI=VTEMP
8752 TAUP=TAU
8755 GO TO 3901
8760 8760 IF(VD.GE.VPOT)GO TO 8640
8765 CDG=SLOP1*VD+CDG0
8768 IF(VD.GE.VDF1)GO TO 8772
8770 CGS=SLOP2*VD+CGSD
8771 GO TO 8640
8772 8772 CGS=SLOP3*VD+YINT
8780 GO TO 8640
9000 END
9100 FUNCTION CEIFK(AKC)
9103 A0=1.3862944
9106 A1=.1119723
9109 A2=.0725296
9112 B0=.5
9115 B1=.1213478
9118 B2=.0288729
9121 AKC1=1.-AKC*AKC
9124 AKC2=AKC1*AKC1
9127 AKC3=A0+A1*AKC1+A2*AKC2
9130 AKC4=(B0+B1*AKC1+B2*AKC2)*ALOG(1./AKC1)
9133 CEIFK=AKC3+AKC4
9136 RETURN
9139 END
9150 SUBROUTINE ANF(P,S,F1,DENA,BL21,FG,XI,A,AL2,PI,F,DEL,WG,Y,CGS,PS,RG,
9151+GM,TNOM,BFC,RINSH)
9152 COMPLEX ZS,BZC,BY11N,BY11D,BY11,BY21,BGN1,BGN2,BZCA,BZCF,BZCC
9154 CGS=CGS*1.E-12
9156 ZS=(50.,0.)
9158 BF=10.E9
9159 BW=2.*PI*BF
9160 BPD=(P*P-S*S-((P**3-S**3)*4./3.)+(P**4-S**4)/2.)/F1
9165 BDEL=1.2
9170 BPD=(2.*BDEL/F1)*((1.-P)**3)*(S-P+ALOG((1.-S)/(1.-P)))
9172 BFR=DENA/(1.-P)
9175 BGAM=(1.-P)*(1.-P)*BFR/F1/Y
9180 BK=((P**4-S**4)/6.)-(P**3-S**3)/3.+(P-S)*((S**2)-(S**3)*2./3.)/F1
9181 BK=BK+BGAM*P
9185 BKP=BK+(1.-P)*BL21
9190 BRDA=BKP*BKP*(P*P-S*S)-BKP*(BKP+BGAM)*(P**3-S**3)*4./3.
9191 BROB=0.5*(BKP*BKP+4.*BKP*BGAM+BGAM*BGAM)/(P**4-S**4)
9192 BRDC=(BGAM*BGAM*(P**6-S**6)/3.)-0.8*(BKP*BGAM+BGAM*BGAM)*(P**5-S**5)
9193 BRO=(BRDA+BROB+BRDC)/(F1*F1*F1)
9195 BRDA=(2.*BKP*BGAM-BGAM*BGAM)*(P*P-S*S)
9196 BRDB=BGAM*BGAM*(P**3-S**3)*2./3.
9197 BRDC=2.*((BKP-BGAM)**2)*(P-S+ALOG((1.-P)/(1.-S)))
9198 BRD=RDEL*((1.-P)**3)*(BRDA-BRDB-BRDC)/(F1*F1*F1)
9200 BSDA=((P*P-S*S)-(P**3-S**3)*4./3.+(P**4-S**4)/2.)*BKP
9201 BSDB=((P**4-S**4)-((P**3-S**3)*2./3.)-(P**5-S**5)*2./5.)*BGAM
9202 BSD=(BSDA+BSDB)/(F1*F1)
9205 BDSA=(BKP-BGAM)*(S-P+ALOG((1.-S)/(1.-P)))+BGAM*(P*P-S*S)/2.
9206 BSD=2.*BDEL*((1.-P)**3)*BDSA/(F1*F1)
9210 BP1=(1.-P)*(BPD+RPD)/(F1*BGAM*RGAM*FG)
9215 BP2A=PI*AL2/A
9216 BP2B=(EXP(BP2A))-(4.*EXP(BP2A/2.))+3.+BP2A
9217 BP2C=(1.-P)*PI/2.
9218 BP2D=(SIN(BP2C)/BP2C)**2
9219 BDIF=35.

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9220 BDIFD=1.374E-23*TNOM*F*10000./DEL
9221 BF3=16.*BDIF*BP2D*BP2B/((PI**3)*BDIFD)
9223 BP2=(1.-P)*WG*BF3/(XI*BFR*BFR*FG*A)
9225 BKPP=BK*P-BGAM*P
9226 BR2=((WG/(A*XI*(1.-P)))**3)**2.*F1*BKPP/BFR/BFC)**2.*FG*BF3
9230 BR1=((F1/(1.-P))**3)**2.*WG*A*PI*BGAM/BFC)**2.*FG*(BFD+BFD)
9231 PL2TWG=AL2/MG
9235 BPP=BP1+BP2
9240 BRR=BR1+BR2
9245 BCCA=SQRT(BP1*BR1/BPP/BRR)
9246 BCCB=SQRT(BP2*BR2/BPP/BRR)
9247 BCCC=(BSD+BCD)/SQRT((BRD+BRD)*(BFD+BFD))
9248 BCC=BCCC*BCCA+BCCB
9250 BY11N=CMPLX(0.,BU*CGS)
9252 BY11D=CMPLX(1.,BU*CGS*PINCH)
9254 BY11=BY11N/BY11D
9260 BY21=GM/BY11D
9265 BGGN=(BW*BU*CGS*CGS)/GM*BPP
9270 BGDN=GM*BPP
9280 BGN1=BY11/BY21*SQRT(BGDN)
9282 BGN2=CMPLX(0.,(BCC*SQRT(BGGN)))
9284 BGN=(CABS(BGN1-BGN2))**2+(1.-BCC*BCC)*BGGN
9290 BPN=PG+PS+(BGDN/(CABS(BY21))**2)**2*(1.-BCC*BCC)*BGGN/BGN
9292 BPN=BRN-(PG+PS)+(PG+PS)*TNOM/300.
9295 BZCA=BGDN*CDNIG(BY11)/(CABS(BY21))**2)
9297 BZCB=BCC*SQRT(BGGN*BGDN)/BY21
9299 BZCC=(0.+1.)*BZCB
9300 BZC=PG+PS+(BZCA+BZCC)*BGN
9304 BNF1=(CABS(ZS+BZC))**2
9305 BNF2=(BRN+BGN*BNF1)/(REAL(ZS))
9306 BFZSD=10.*ALOG10(1.+BNF2)
9310 BRSD1=REAL(BZC)
9315 BRSD=SQRT(BRSD1**2+(BPN/BGN))
9320 BXID=-AIMAG(BZC)
9322 BK6=BRR*BPP-2.*BCC*SQRT(BPP*BPP)
9324 BK0=(BPP-BCC*SQRT(BPP*BPP))/BK6
9326 BK*P=BRR*BPP*(1.-BCC*BCC)/BK6
9330 BFMIN=1.+2.*BGN*(BRSD1+BRSD)
9335 BFMIND=10.*ALOG10(BFMIN)
9340 PRINT 9,BFZSD,BFMIND,BRSD,BXSD
9342 9,FORMAT(1X,NZ=*,F5.1,*,DB; NM=*,F5.1,*,DB; POP=*,F7.1,*,OHM; CDP=*,F7.1,*,OH

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9343+M*)

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9350 PRINT 9360
9360 9360 FORMAT(1X,*)
9370 RETURN
9380 END

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NRL REPORT 8561

(PG= 1.9 ; PS= 4.0; RD= 4.0)

CFDG= .0677PF ; CF1G= .0692PF ; CF1D= .0941PF

VS	VD	CSW	CUR	GM	DP	CG
0.000	1.0000	.030	.0883	.0328	3.8	.346E-01
CGSD=CDGD= .472FOR VD=0.						
BGM= 32.1MMHD (FOR VDINT LT VS)						
CGS,CDG,CDOM,RDOM= .283 .322 .01682 359.1						
RINSH= 17.61						
TAU= 22.65PSEC ; RINPHS= 654.74OHMS						
NZ= 5.3DB; NM= 3.9DB; POP= 33.00HM; XOP= 59.60HM						
0.000	3.0000	.030	.1456	.0543	101.6	.769E+00
CGS,CDG,CDOM,RDOM= .621 .070 .01444 567.8						
RINSH= 7.72						
TAU= 9.12PSEC ; RINPHS= 11.86OHMS						
NZ= 9.3DB; NM= 7.6DB; POP= 18.50HM; XOP= 31.50HM						
0.000	5.0000	.030	.1452	.0521	205.2	.776E+00
CGS,CDG,CDOM,RDOM= .754 .045 .00941 2051.7						
RINSH= 5.86						
TAU= 8.40PSEC ; RINPHS= 10.83OHMS						
NZ= 9.6DB; NM= 7.7DB; POP= 16.80HM; XOP= 29.10HM						
-2.000	1.0000	.030	.0626	.0349	10.0	.346E-01
CGSD=CDGD= .252FOR VD=0.						
CGS,CDG,CDOM,RDOM= .141 .193 .02069 45.5						
RINSH= 31.81						
TAU= 13.33PSEC ; RINPHS= 385.30OHMS						
NZ= 2.4DB; NM= 1.1DB; POP= 97.10HM; XOP= 137.30HM						
-2.000	3.0000	.030	.0738	.0408	165.9	.565E+00
CGS,CDG,CDOM,RDOM= .267 .088 .00576 2010.1						
RINSH= 16.30						
TAU= 8.28PSEC ; RINPHS= 14.64OHMS						
NZ= 4.6DB; NM= 3.0DB; POP= 42.20HM; XOP= 77.00HM						
-2.000	5.0000	.030	.0772	.0396	258.0	.567E+00
CGS,CDG,CDOM,RDOM= .366 .063 .00409 5512.7						
RINSH= 10.85						
TAU= 7.55PSEC ; RINPHS= 13.32OHMS						
NZ= 5.2DB; NM= 3.6DB; POP= 32.90HM; XOP= 61.50HM						
-4.000	1.0000	.030	.0086	.0212	191.8	.431E+00
NGD CGSD=CDGD= .193FOR VD=0.						
NGD CGS,CDG,CDOM,RDOM= .101 .160 .00173 1972.0						
RINSH= 62.93						
TAU= 16.08PSEC ; RINPHS= 37.28OHMS						
NZ= 3.5DB; NM= 1.5DB; POP= 128.00HM; XOP= 184.40HM						
-4.000	3.0000	.030	.0141	.0247	328.0	.426E+00
NGD CGS,CDG,CDOM,RDOM= .154 .099 .00079 18092.5						
RINSH= 39.62						
TAU= 11.57PSEC ; RINPHS= 27.14OHMS						
NZ= 3.1DB; NM= 1.5DB; POP= 104.60HM; XOP= 142.80HM						
-4.000	5.0000	.030	.0187	.0258	386.4	.429E+00
NGD CGS,CDG,CDOM,RDOM= .239 .074 .00057 44725.8						
RINSH= 22.03						
TAU= 10.02PSEC ; RINPHS= 23.36OHMS						
NZ= 3.2DB; NM= 1.9DB; POP= 70.60HM; XOP= 97.60HM						

Program FETREN Notation List

Input Parameters

A	Active layer thickness, μm
CND	Doping level under gate/ cm^3
CND1	Doping level between gate and drain and between gate and source in units of $10^{16}/\text{cm}^3$
WG	Gate length, μm
W	Gate width, μm
HGM	Thickness of gate metal, μm
IG	Number of gate voltages to be run, integer
VGO	Initial gate voltage, V
DVG	Gate voltage increment, V
ID	Number of drain voltages to be run, integer
VDO	Initial drain voltage, V
DVD	Drain voltage increment, V
FO	Low-field mobility, $\text{m}^2/(\text{V} \cdot \text{s})$
CND2	Not used in program
TNOM	Nominal, ambient operating temperature, K
QEL	Electronic charge, C
EPSO	Free space permittivity, ϵ_0 , F/m
EPS	Dielectric constant, relative, ϵ_r , of GaAs, dimensionless
SL	Source metal length, μm^*
DL	Drain metal length, μm^*
DGL	Gate metal to drain metal spacing, μm^*
SGL	Gate metal to source metal spacing, μm^*
SDL	Source metal to drain metal spacing, μm^*
VPO	Pinch-off voltage (calculated)
RTH	Assumed thermal resistance, $^{\circ}\text{C}/\text{W}$
ES	Saturation field, kV/cm
AVELSAT	Saturation velocity for extremely high fields, m/s (for Gunn domain calculations)
CNCR	The characteristic doping level (for Gunn domain calculations)/ cm^3
VBI	The gate metal-to-semiconductor Schottky barrier built-in voltage, V
ZS	Complex driving impedance, ohms, for calculation of noise figure, NZ
BF	Frequency for noise calculations, Hz
BDIF	High field diffusion coefficient, cm^2/s

Output Parameters

RG	Gate metal resistance, ohms
RS	Gate-to-source bulk semiconductor and source contact resistance combined, ohms
RD	Drain-to-gate bulk semiconductor and drain contact resistance combined, ohms
CFDG } CFSG } CFSD }	Metal pad-to-metal pad fixed capacitances, pF
VG	Applied gate voltage, V

*See Fig. 7.

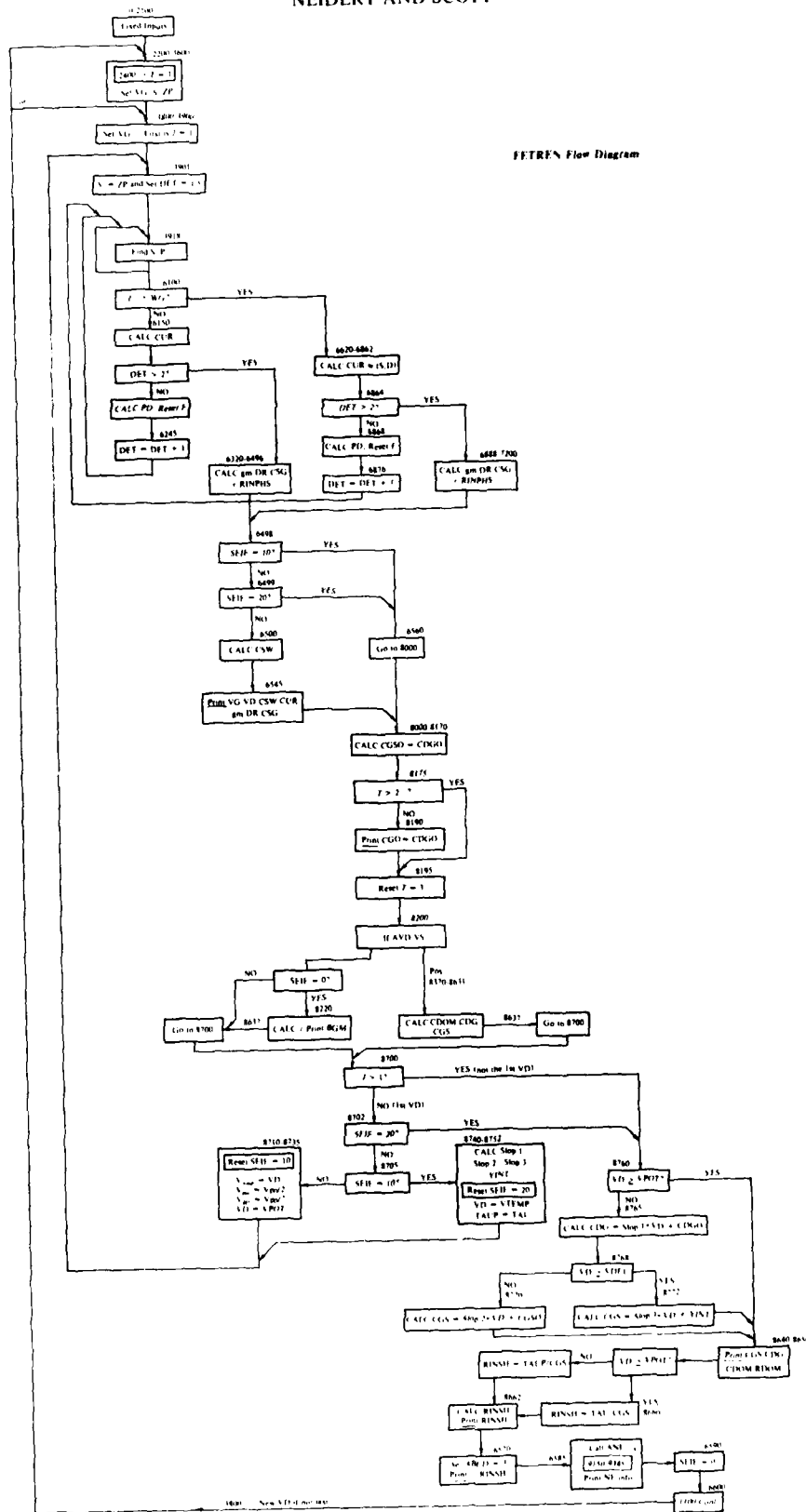
VD	Applied drain voltage, V
CSW	Sidewall capacitance, pF
CUR	Drain-to-source current, mA
GM	Transconductance, mmhos
DR	Drain-to-source resistance, ohms
CSG	Source-to-gate capacitance, pF, see text
CGSO	Gate-to-source capacitance, pF, when $V_D = 0$
CDGO	Drain-to-gate capacitance, pF, when $V_D = 0$
BGM	A transconductance calculation by [12]
CGS	Gate-to-source capacitance, pF, see text
CDG	Drain-to-gate capacitance, pF
CDOM	Domain capacitance, pF
RDOM	Domain negative resistance, ohms
RINSH	Input resistance, ohms, see text
TAU	Transit time, ps
RINPHS	Input resistance, ohms, by [4], using calculated transit time, TAU
NZ	Noise figure, dB, when driving impedance is ZS
NM	Minimum noise figure, dB, for optimum driving impedance
ROP	Optimum driving resistance, ohms, for minimum noise figure
XOP	Optimum driving resistance, ohms, for minimum noise figure
NGD	"No Gunn Domain" by the criteria of [16]

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Appendix B
Program FETREN Flow Diagram

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FFTRFS Flow Diagram



Appendix C
CALCULATION OF TEMPERATURE EFFECTS ON GALLIUM ARSENIDE MESFETS

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ABSTRACT

A simple way of accounting for temperature effects in analytical, equivalent circuit models for microwave gallium arsenide MESFETs is shown. The approach is based on the knowledge of the thermal resistance of the device in actual operation, and the variation of the device's low-field mobility with temperature. This paper develops working numerical estimates for both of these characteristics, gives a method of incorporating them into the model calculations, and compares measured data with temperature-corrected, calculated results.

I. INTRODUCTION

Comparisons between measured data and calculated results for MESFETs (metal-semiconductor field effect transistors) might agree better if temperature effects were included in the calculations. The method of accounting for these effects is simple, once the actual *thermal resistance* of the device in its operational configuration is known and a relationship between the device temperature and its *low-field mobility* is known.

Section II provides a theoretical basis for the determination of the above two unknowns and for their utilization. In Section III, some measured and calculated results are compared.

II. THEORETICAL CONSIDERATIONS

The variation of *low-field mobility* with temperature is a strong thermal effect in microwave GaAs MESFET operation [C1]. The rate of this variation is itself temperature dependent because different carrier scattering mechanisms predominate in different temperature ranges [C2]; also, the degree of temperature sensitivity appears to be doping-level-dependent, as is shown later. For purposes of this paper, and for most applications, 300 K will be used as the reference environmental temperature. The method used to develop the mobility-versus-temperature relationship centered at 300 K is of course applicable to any other reference ambient temperature. (See Ref. C2 for guidance.)

The published, measured Hall-mobility data given in Table C1 has been reviewed in an effort to find a suitable mobility-versus-temperature relationship. The distinction between Hall and Drift mobility may be neglected to a good approximation as explained in Ref. C3; moreover, only the slope is involved here. Table C1 gives the exponent, A , relating mobility and absolute temperature, in the vicinity of 300 K, for several impurity levels of *n*-type GaAs, according to the relationship

$$\mu_0 \propto T^A.$$

In the proportionality, μ_0 is low-field mobility and T is absolute temperature in degrees Kelvin. The sources of the data, Refs. C2 through C6, are also given in Table C1. A linear least-squares fit to the first five data points, merged with the asymptote given by the sixth data value (for intrinsic material),

Table C1 — Measured Temperature Sensitivity of Mobility versus Impurity Level (at 300 K)

Reference	Impurity Level/cm ³	A
C3,C4	2.2×10^{16}	-0.74
C3,C5	3.7×10^{15}	-0.97
C2	1.3×10^{15}	-1.46
C2	2.7×10^{16}	-1.01
C2	7.1×10^{15}	-1.06
C6	intrinsic	-1.80

yields the curve of Fig. C1. These data and the resultant curve are certainly not conclusive; but the indication is that in the vicinity of the $10^{17}/\text{cm}^3$ doping level of microwave GaAs MESFETs an exponent, A , of -0.6 can be used. In the convincing comparison with experimental results given in Section III, for which the transistor doping level is $7.5 \times 10^{16}/\text{cm}^3$, a value of -0.7 is used for the exponent (as suggested by Fig. C1). Also, in subsequent calculations, the saturated velocity was allowed to vary directly as the mobility, as was suggested in Ref. C1.

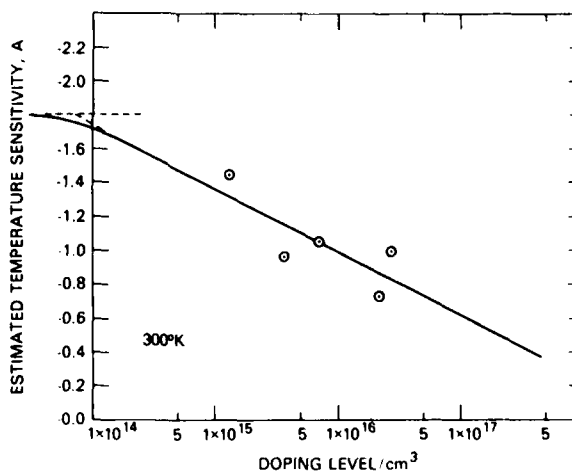


Fig. C1 — Estimated plot of mobility temperature sensitivity versus impurity level at 300 K

The other parameter which must be known in order to calculate the thermal effects is the device *thermal resistance* in actual operation. This value can be measured for a specific case; however, it can also be estimated with reasonable accuracy. All device manufacturers are aware that good heat sinking, especially for power FETs, is important; so they all tend toward the state of the art. A survey of several manufacturers was conducted (in a few cases proprietary information was provided), and published information was reviewed, to determine typical thermal resistances. The values were found to be in the vicinity of

$$R_{TH} = (70000/B) \text{ } ^\circ\text{C/W.}$$

where R_{TH} is thermal resistance in °C per watt and W is the gate width in microns. This equation is an oversimplification, but it provides a useful first order approximation. It is possible, of course, to deviate greatly from this value but, based on the findings of the above survey, such wide deviations are seldom found in practice, either for power or low-noise devices.

The above information forms the basis for calculating the device characteristics which are affected by operating temperature. By taking advantage of the fact that the temperature sensitivity of the low-field mobility is such a predominant factor in overall MESFET temperature sensitivity, the temperature-corrected values for the dc and small-signal characteristics can be obtained with a simple correction in the mobility value. The correction procedure consists of the following steps, noting that external voltages must be used so that all the parasitic resistances are included in the power dissipation calculation: (a) calculate the drain current at the relevant bias point; (b) calculate the total dissipated dc power, equal to drain current times drain voltage; (c) calculate the operating temperature of the device by using the total dissipated dc power and the thermal resistance; (d) calculate the corrected operating low-field mobility; (e) repeat steps (a) through (d) and use the new mobility value each time—until the mobility converges to its final value; and (f) recalculate all characteristics by using the final, corrected mobility value.

In the following section, the mobility correction is performed at each bias point, for the experimental device doping level of $7.5 \times 10^{16}/\text{cm}^3$, according to:

$$\mu_0(\text{at } T) = \mu_0(\text{at } 300 \text{ K}) \left[\frac{300 + R_{TH} \cdot P_D}{300} \right]^{-0.7},$$

where P_D is the total power being dissipated by the device.

III. COMPARISON OF EXPERIMENTAL AND CALCULATED RESULTS

The pertinent information on one of the transistors used for experimental comparison is given in Table C2. The calculation method was that of [C7], except that alternate equations were derived and utilized when the method of [C7] yielded a computed, constant-mobility region length under the gate which was longer than the gate itself. (See Refs. C7, C8, and C9 for some discussion of this case.) For temperature correction, the mobility was adjusted according to the method discussed in Section II. Typically, only one iteration was required.

Table C2 — Parameters of Experimental Transistor

Active layer thickness	0.315 μm
Doping level	$7.5 \times 10^{16}/\text{cm}^3$
Gate length	1.7 μm
Gate width	600 μm
Source parasitic resistance	2.8 ohms
Drain parasitic resistance	3.7 ohms
Intrinsic GaAs relative diel. const.	12.9
Thermal resistance	117°C/W
Low field mobility at 300 K	4240 $\text{cm}^2/\text{V-s}$
Schottky gate built in voltage	0.7 V

The calculated and measured I-V curves of the device are given in Fig. C2. Two sets of calculated curves are shown—one with temperature correction and one without. The similarity between the measured curves and the computed curves with temperature correction is convincing evidence of the existence of strong temperature effects and the suitability of the method of accounting for them. As would be expected, temperature effects diminish as the gate voltage approaches pinch off.

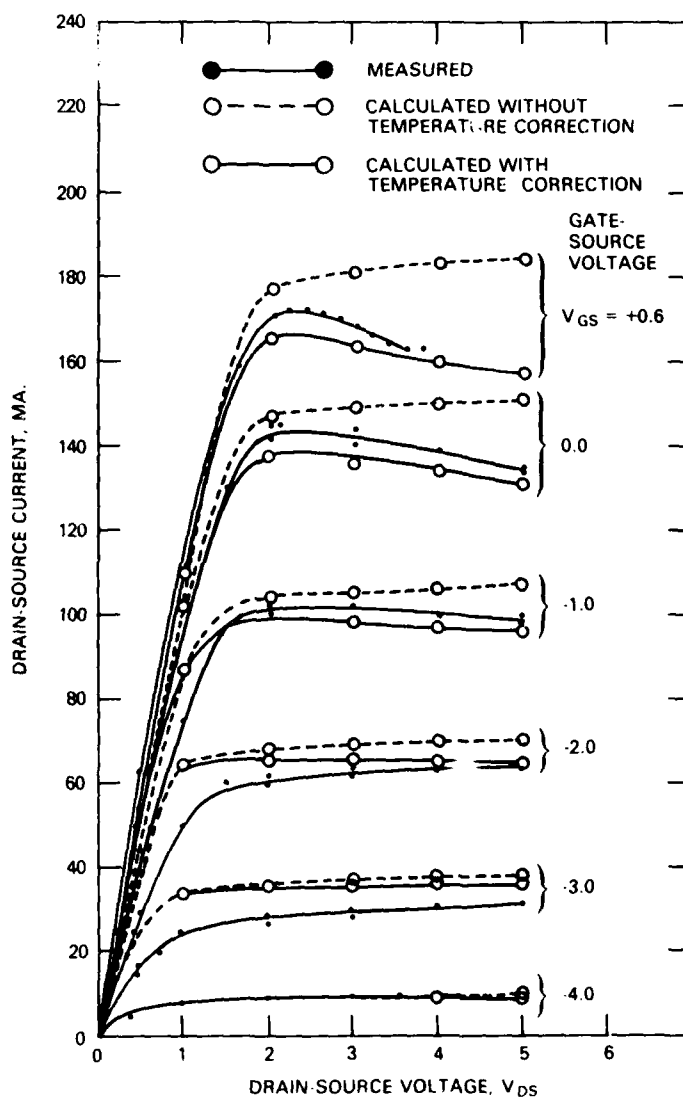


Fig. C2 — Experimental transistor I-V curves

Without showing additional curves, the following discussion outlines some other observations on temperature effects which were made. The calculations (both with and without temperature correction) were done according to Ref. C7. Note that, for constant applied gate voltage, an increase in the applied drain voltage results in an increase in operating temperature. The temperature-corrected, calculated

transconductance *decreased* with increasing drain voltage for gate voltages in the vicinity of 0 V, consistent with measured results. On the other hand, the equivalent transconductance values calculated without temperature correction *increased* with increasing drain voltage, contradictory to the measured data. The calculated values of input capacitance were nearly unaffected (less than 2%) by the temperature corrections. Finally, the temperature-corrected, calculated drain or output resistance was always higher than the value calculated without temperature correction. Therefore, with temperature correction, the increase in drain resistance with increasing drain voltage was somewhat larger than that calculated without temperature correction.

Fair quantitative agreement was obtained between the measured and the calculated values of transconductance and input capacitance, but the drain resistance calculated by Ref. C7 was in all cases much higher than the measured values (approximately four to ten times higher). Therefore, the actual sensitivity of the output resistance to temperature is not necessarily predicted by this method of calculation. Work is continuing to include additional terms which contribute to the output resistance, and to investigate their temperature dependence. The additional terms being studied are the Gunn domain negative resistance when present [C10-C12], the resistance representing hot electron injection into the otherwise semi-insulating substrate when the Gunn domain is present [C13], and simple substrate or surface leakage when it is present.

IV. CONCLUDING REMARKS

The effects of temperature on RF performance have not been explicitly presented in this paper. It is possible and straightforward to calculate these RF effects, in any special case, by computing them from the modified equivalent circuit element values.

A second and somewhat different transistor, having 300 μm gate width and 1.0 μm gate length, with an active layer thickness of 0.24 μm , has also shown good agreement between measured I-V curves and calculated curves when temperature correction was used in the calculations. The negative slope in the I-V curves at large values of bias power appeared again, both in the measured data and in the temperature-corrected calculations.

The static negative resistance in the I-V curves of GaAs MESFETs is not necessarily caused by temperature effects alone. There can be other effects involved; Norton and Hayes [C14] indicate this with some reservations. It is interesting to see, however, at least in the cases considered here, the much improved agreement in the calculated I-V curves by accounting only for temperature effects.

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