

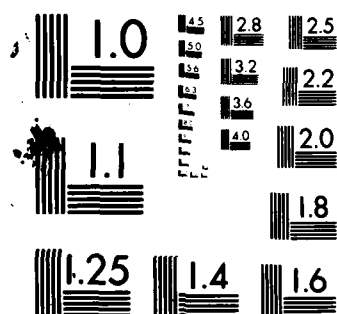
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COMPUTER-AIDED DESIGN/MANUFACTURING
(CAD/M) FOR HIGH-SPEED INTERCONNECT

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Norbert F. Santoski
Sperry Univac
Defense Systems Division
P.O. Box 3525
St. Paul, Minnesota 55165

October 1981

Final Report for Period 16 July 1980 - 15 August 1981

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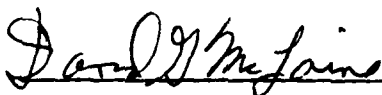
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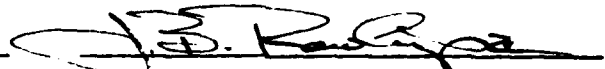
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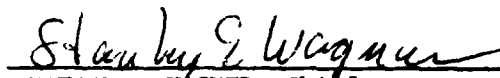


DAVID G. MCLAINE, Project Engineer
Design & Packaging Group



J. B. RAWLINGS, Capt, USAF
Chief, Design & Packaging Group

FOR THE COMMANDER



STANLEY E. WAGNER, Chief
Microelectronics Branch
Electronic Technology Division

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> is used for the design, analysis and fabrication of circuits. To implement these design rules in future software development, algorithms and software development techniques were defined.

Major emphasis was on Printed Wiring Board and hybrid level circuits as opposed to monolithic chips. Various packaging schemes were considered, including controlled impedance lines in the 50 to 200 ohms range where needed. The design rules developed are generic in nature, in that various architecture classes and device technologies were considered..

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SECTION 1

INTRODUCTION

The objective of the Computer-Aided Design/Manufacturing (CAD/M) for High-Speed Interconnect Program study was to assess techniques for design, analysis and fabrication of interconnect structures between high-speed logic ICs that are clocked in the 200 MHz to 5 GHz range. Interconnect structure models were investigated and integrated with existing device models. Design rules for interconnects were developed in terms of parameters that can be installed in software that is used for the design, analysis and fabrication of circuits. To implement these design rules in future software development, algorithms and software development techniques were defined.

Major emphasis was on Printed Wiring Board (PWB) and hybrid packages (as opposed to monolithic chips), and addressed the interconnections between chips. Various packaging schemes were considered, including controlled impedance lines in the 50 to 200 ohm range where needed. The design rules developed are generic in nature, in that various architecture classes and device technologies were considered.

This study was composed of seven tasks:

- o Survey to assess current capabilities and techniques for design, analysis and fabrication of interconnect structures for high speed logic.
- o Survey and define interchip connection models.
- o Survey computer programs that characterize high-speed devices.
- o Integrate the device models and interconnection models, and develop quantitative design rules.
- o Define algorithms and software modules which need to be developed to implement a system for automated design, analysis and fabrication of circuit card or hybrid functions.
- o Define CAD/M approach, including software transportability.
- o Generate a final report.

Appendix A contains the survey questionnaire and cover letter. Appendix B contains a list of the organizations to which these were sent.

It is evident that much work is being done, in many organizations, on CAD/M approaches to high speed digital circuits, and high speed interconnection modeling. These efforts are directed toward CAD/M program utilization and design and modification with respect to device and transmission line models. However, much of this work is proprietary and not readily available for the purposes of this project.

Sperry Univac - DSD gratefully acknowledges the time and efforts of those organizations and individuals that contributed information to this study.

SECTION 2

BACKGROUND

The clock rates at which high-speed digital logic circuits are able to perform, and the rates which will be feasible in the next several years (9, 12, 33, 34, 35, 36, 41, 46, 55, 70, 74, 82), demands more exacting design, analysis, fabrication and test techniques. The traditional methods of breadboarding and testing, as part of the design and analysis cycle, will no longer be adequate for accurate representation of the final product. Also, the design-build-test cycle with numerous iterations to accommodate necessary changes to obtain the required performance characteristics is not timely and cost-effective.

To accomplish the design and development of high speed digital circuitry, increased utilization of CAD/M systems will be required.

The main goal of this definition study was the consideration of several key areas (transmission line models, high speed device models, packaging approaches, etc.) that would lead to a definition of concepts and approaches that can serve as a foundation for future CAD/M system software development.

2.1 Interconnect Considerations

This study focused on various considerations related to the topics of high speed circuits, their interconnections, and relevant modeling.

The design and analysis of digital circuits is normally performed in the time domain because logic circuitry involves discrete signals and the timing of these signals. Performing the CAD/M function in the time domain provides waveforms that can readily be compared to the oscilloscope waveforms obtained from the actual finished product. Although much valuable information can be obtained by frequency domain analysis, the high level nonlinear circuits involved do not lend themselves readily to frequency domain analysis.

At the clock rates of 200 MHZ to 5 GHZ addressed in this study, the chip interconnections become significantly important because they function as electrically long transmission lines at the frequency components contained in the pulse signals of interest.

Traditionally, the subject of transmission line analysis has been treated by two application areas that are widely separated in the frequency spectrum, namely power engineering and microwave engineering.

Most of the transmission line characteristics are frequency sensitive and hence lend themselves to frequency domain analysis. Most of the classical microwave analysis is handled in the frequency domain (20, 68, 69) because:

- o A single frequency is of interest (e.g., an oscillator).

- o Only small signals are present, and the circuit exhibits linear behavior with respect to these small signal excursions. Hence, the device and interconnect modeling activity is relatively straightforward compared to nonlinear circuits.

For a time domain analysis program to be the key analysis tool for high-speed interconnections, it must be accurate over the clocking rate range of interest in this study, and, as a minimum, account for the following transmission line characteristics:

- o Conductor losses (DC and skin effect)
- o Dielectric losses
- o Line impedances
- o Propagation delays, especially for synchronous logic circuits
- o Dispersion
- o Line to line coupling (coplanar and interplanar)
- o Line discontinuities (levels, connectors, vias, etc.)

Thus, there is a basic need of having sophisticated CAD/M software available to permit the designer to determine, as early as possible, the anticipated performance characteristics of the hardware design.

2.2 CAD/M Considerations

Device and interconnect fabrication technologies and digital logic clocking rates have resulted in the expressed need of CAD/M techniques which can accurately accommodate not only state-of-the-art technologies, but future growth as well. The defined CAD/M approach becomes increasingly important for providing information regarding the absolute values to use for the interconnects (line widths, spacings, etc.) and also for obtaining insight into problem solving.

The consideration of CAD/M techniques for high speed interconnections must address many topics, such as:

- o Transmission line configurations and models
- o Device types and models
- o Processing (fabrication techniques)
- o Electromagnetics
- o Materials
- o Numerical analysis
- o Logic design
- o Packaging

Software utilized in a CAD/M system for high speed interconnections must treat the problem in a manner that is acceptable from a functional viewpoint. Also the software designer must consider the following characteristics:

- o Computer running time
- o Interfacing with user-orientated software
- o Transportability

This report initially presents an overview of a CAD/M system fulfilling the requirements stated above. The report then discusses several topic areas of importance in the evolution of a CAD system supporting design and fabrication of high-speed circuits. This includes packaging, interconnect models, circuit analysis tools, device models, model integration, and a CAD/M development approach.

SECTION 3

CAD/M SYSTEM FOR HIGH-SPEED INTERCONNECTIONS

This section presents a suggested CAD/M system concept that is oriented specifically for the interconnection of high speed logic chips. Figure 3.1 is a proposed CAD/M system for the design, analysis and layout (placement and routing) of high speed digital circuits. An explanation of this diagram, with a scenario for actual use, provides the foundation for more detailed sections in this report. This system is an outgrowth of ideas based on the literature search, survey questionnaire responses, and personal contacts accomplished in this study.

A brief description of the purpose of each CAD/M system module follows. The modules designated with an asterisk (*) were not the subject of the technical part of this study, but are included for the sake of clarity and completeness.

The primary effort within this study was oriented toward arriving at a reasonable approach for simulating high speed devices and their interconnections. The resulting approach utilizes a recently-documented analysis capability integrated into a time-domain analysis program. This approach allows determination of frequency-dependent transmission line (interconnect) characteristics and traditional device analysis. The approach provides transformation between linear and nonlinear portions of a network. This central focus of the present report is represented by the Computer-Aided Circuit Analysis (CACA) tool in Figure 3.1. This tool will have to be developed. Some of the other blocks illustrated in Figure 3.1 are, in concept, currently available tools in that they differ only slightly in capability from tools already being used in CAD systems. All permit direct user input data.

3.1 Block Diagram Description

The Design Rules and Specifications (DRS) allows entry of a formal set of requirements into the CAD/M system regarding a particular hardware product. This input contains information that is functional (e.g., the specification of logic family), and detailed (e.g., design rule parameters). The latter has the largest impact on the interconnections, such as number of layers, line types, line impedances, logic signal levels, etc. This module is shown dashed because the inputted parameters are in turn fed to various modules in the system to override built-in default values.

The CACA tool is a time-domain analysis program that performs transient analysis of network signals. It obtains data from several sources, with the user playing a very active I/O role. This tool has the capability of performing sophisticated transmission line and high-speed active device analysis. It must retain the capability of being used as a stand-alone analysis tool for convenient, rapid analysis of a circuit. The output of the CACA tool (tabular and/or

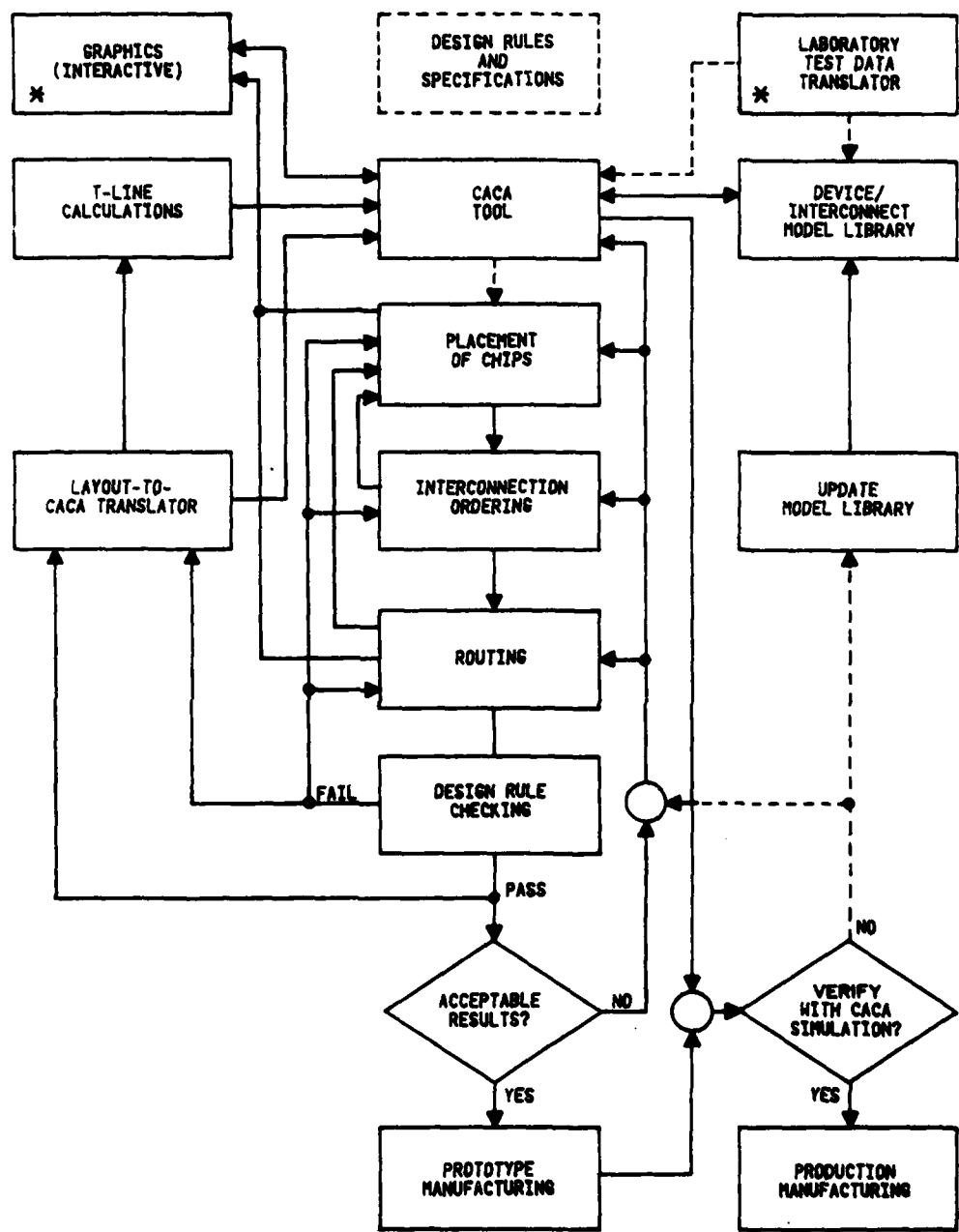


FIGURE 3.1 CAD/M SYSTEM PROCESS DIAGRAM

plotted data) is an indication of the performance of the logic system. The voltages and currents at any user-specified location on the interconnect can be requested. These results will demonstrate if the system signals are acceptable in magnitude, waveshape and timing. Thus, the output of the CACA tool is used in the prototype performance/simulation verification decision-making point in the CAD system.

It is at this point that information is provided which determines whether or not to proceed with manufacturing. If the design does not meet performance requirements, one or more additional iterations through the CAD process would be required.

Placement of Chips performs automatic placement on the layout medium of interest (PCB, thick film ceramic substrate, etc.). Manual placement is permitted, either before or after automatic placement, to effect a more desirable location of chips. Such a package places the chips, utilizing an algorithm based on such constraints as:

- o Available locations permitted by dimensional considerations
- o Thermal management
- o Clustering of chips to minimize routing line lengths and/or number of signal layers
- o Signal timing, particularly for synchronous logic circuits

Interconnection Ordering is performed by a software tool which determines the order in which subsequent routing is to be performed. This module incorporates, and is based in large part on, the various design rules that are pertinent to a specific application. These design rules can be modified or overridden by the user via the DRS module, or changing the input to the ordering module.

Routing is a sophisticated module that performs the interconnection of chips based on the output of the ordering module and on the built-in design rule constraints, such as:

- o Line width
- o Line spacing
- o Line length
- o Location of vias and thru holes
- o Location of sources and loads

The design rules can be overridden by the user. The routing module permits a combination of automatic and manual routing to best suit a particular application. Multilayer routing, and routing subject to controlled impedance transmission lines are implemented by this module.

The Design Rule Checking (DRC) module determines if any default or user-specified design rules were violated. This step must be performed to ensure that the remaining steps in the design/analysis/fabrication process lead to an acceptable final product. This checking module would contain a comprehensive set of error messages to clarify any instances of rules that are violated. The built-in default design rules can be overridden by the user for a specific

application by inputting design rule parameter values. When all such rules have been satisfied, the layout information is inputted to a module for layout-to-CACA translation.

The Layout-to-CACA Translator (LCT) module serves as an interface that automatically generates properly formatted input data for the CACA tool, based on the chip placement and chip interconnection routing pattern. It eliminates the error-prone and time-consuming task of manually generating CACA program input data based on layout information. The purpose is to describe the transmission line configurations and loads from the dimensional information. The type of line and its dimensions are all determined from the artwork data base information. This determination is performed for the entire interconnection of interest.

The Transmission-Line Calculation (TLC) module performs some of the detailed calculations that are associated with transmission lines, such as characteristic impedance, propagation constant and line loss (including skin effect, etc.). Unique calculations will be made for each unique line (microstrip, stripline, etc.). There may be some duplication of calculations with those performed by the CACA tool, but not necessarily in the same design/analysis cycle. The existence of the TLC module serves to reduce the complexity of the CACA tool proper. It also provides the user with a stand-alone module that can be used for particular transmission line static calculations without having to execute the larger time-domain program.

When a configuration satisfies the design rules and is considered acceptable prior to release to the manufacturing environment, two additional checks are performed:

- o Product verification to determine the correlation of the simulation results with the hardware test results. If the correlation is acceptable and the product performance is acceptable, the design is released for production manufacturing; otherwise an iteration through the CAD system is performed.
- o Product testing to determine parameters for input to the data reduction and model parameter generation software. This information is used for updating the Device/Interconnect Model Library (DIML).

Both of these activities require manual intervention. Finally, the improved DIML can be referenced by the CACA tool to automatically utilize the properly-formatted input data.

The DIML contains appropriate models and model parameter data for both active devices and chip interconnection structures. One or more of these models can be readily referenced via the user input data for the CACA tool by merely specifying the model name. Such a calling statement also permits the user to modify the data for one or more of the model parameters in the referenced model (e.g., specify that the threshold voltage in a called MOSFET is different than the built-in value in the model library without directly modifying the data in the DIML).

3.2. A Typical Scenario

A typical scenario based on the use of this CAD/M system follows. The scenario may vary depending on the particular application, user interests, options, logic clocking frequency, and performance.

1. Design circuit per design rules and specifications
2. Determine devices to be specified
3. Perform preliminary interconnect/layout to determine rough analysis of line length, vias, discontinuities, connectors, coupling, etc.
4. Develop special device and interconnect models
5. Model circuit in format compatible with CACA tool
6. Execute time domain analysis program (CACA tool)
7. Analyze results (tabulations, plots)
8. Repeat steps 1 through 7 as necessary to improve circuit performance
9. Provide input data to placement tool
10. Execute interconnection ordering based on chip placement
11. Execute routing
12. Perform automatic design rule checking. If results are acceptable, then design can be released for product verification. If not acceptable, then one or more iterations must be done, starting at the above appropriate step.

NOTE: For complex layouts, or circuits with high frequency clocking rates, the LCT module is utilized. Initial placement and routing data may not be known by the user. Consequently, the time-domain analysis results will be highly dependent upon the type and routing of the transmission lines (interconnections). Only with such data will a CACA execution be meaningful.

13. The circuit(s) provided by prototype manufacturing will be tested against the simulation results. If acceptable, then "final" design is released to production manufacturing. If not acceptable, one or more of the above steps must be repeated. With accurate models, data, and solution algorithms, the need for these iterations will be considerably reduced.

14. Circuits produced by production manufacturing are tested for performance characteristics. The results of such testing (signal integrity, propagation speeds, etc.) may be used, if needed, to manually or automatically update the model library. This procedure demands thorough and complete documentation to summarize test data and model changes.

The primary difference between the scenario described above and that of a "standard" CAD/M approach for digital logic is the incorporation of interconnect structures into the circuit analysis being performed. Normally, interconnects are assumed to be strictly point-to-point connections which have little or no influence on signal shape and propagation speed. At high frequencies, this assumption is not valid, and signal simulation must occur along interconnects, as well as within devices. This capability is necessary to make a CAD/M system for high speed circuits valuable.

The following sections describe the study results which led to the formulation of the CAD/M system described. These sections provide information on interconnect models, device models, the integration of these models, and pertinent design rules or constraints. In addition, other sections present an approach to software tool development and integration with existing applicable tools.

SECTION 4

INTERCONNECT CONSIDERATIONS AND MODELS

4.1 Packaging Considerations

There exists a wide variety of interconnection types, with variations of each based on materials and physical dimensions. In addition, the packaging techniques utilized can affect the selection of interconnects, and consequently, must also be considered (12, 41, 74).

Two characteristics of packaging which are of fundamental importance are the fabrication itself, and the associated tolerances which must be closely controlled and testable to ensure that with the small geometries involved, the tolerances will not adversely affect the electrical characteristics of the circuitry. For example, thick film conductor properties at microwave frequencies can dictate the actual packaging possible. Conversely, the combination of performance characteristics and packaging requirements can dictate the allowable materials that can be utilized (a more severe mode). Cost, quality control and repairability are all important associated parameters of packaging techniques.

For the purpose of this study, the following packaging types were considered: printed circuit board (PCB), thick film hybrid, and thin film hybrid, with variations within these types. For example, a given PCB could contain both dual-in-line packages (DIPs) and flat packs (FPs); hence, the interconnections may require different models for the lines and connections, and different design rules over particular portions of the PCB depending on chip placement and other forcing functions.

Table 4.1 indicates some characteristics of various fabrication technologies, and how they "bridge" the speed considerations addressed in this study (76).

4.2 Interconnections and Modeling Approaches

4.2.1 Interconnection Types

The chip interconnection types addressed in this study include coaxial cable, twisted pair, and flat ribbon cable between packages (PCB's, etc.), and microstrip, stripline and coplanar lines between chips.

Because of the digital clocking speed range of interest in this study, the first three types are included for possible application at the low rates, and for the sake of a certain amount of continuity. Most of the information in the literature, particularly for the higher speeds of interest (microwave region), was directed towards "standard" microstrip and "standard" stripline configurations. The number of feasible chip interconnection types which could be considered is large and includes such types as inverted stripline, suspended microstrip, offset stripline, uniform dielectric microstrip, etc. However, the CAD/M system and the pertinent modules and algorithms for the system described herein should prove sufficient as guidelines for more extensive line types and packaging approaches. The modeling details will change, but the implementation approaches will be similar to those described in this report.

4.2.2 Interconnection Modeling Approaches

For those digital circuit applications in which the physical interconnection line lengths are short compared to the electrical wavelengths at the highest frequency present in the signal, there is little need to treat the interconnections as electrical transmission lines. The only characteristic of interest in these cases may be resistive loss; excessive voltage drop would significantly affect the noise margin present at any given load. Two other associated characteristics which may prove important for certain lines and applications are:

- o Current-carrying capacity of an interconnection line at any given physical location on the line. The CAD/M software should have design rule limits specified (built-in), with error messages being outputted to alert the user of any "overloads". Such calculations can be improved to account for steady state, worst case and duty-cycle sensitive situations.
- o Power dissipation within the interconnection line. Though not generally a factor to be considered in a given line, the CAD/M software could incorporate such IR calculations for all interconnections within a package, and provide the total line dissipation information for subsequent thermal management considerations.

One of the items to consider in any interconnect study is that of the frequency range of interest. This determines whether the interconnections must be treated as transmission lines. The frequency range also determines which wave propagation effects must be taken into account. In this study, the digital clocking rate range of interest is 200 MHz to 5 GHz. The corresponding periods, rise/fall times for a trapezoidal pulse, and the highest frequency components present are shown in Table 4.2. Note that the assumption is made that the rise/fall times are each 20% of the clock period. Also, the simulated signal purity varies, depending upon the value of N, where N varies from 1 to 10, depending upon the application, "judgement" of the user, and/or test data (67).

PACKAGING TYPE	LINE WIDTH (MILS)	LINE SPACING (MILS)	VIA DIAMETER (MILS)	VIA SPACINGS (MILS)	LAYERS "ALLOWED"	RESISTIVITY (OHMS/SQ.)	CAPACITANCE (PF/IN ²)	DIELECTRIC CONSTANT	MAX. USABLE FREQ. (GHZ)
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PCB WITH EPOXY GLASS	10	10	20	100	14	1-5	180	4.8	0.15
THIN FILM ON ALUMINA	1	1	-	-	1	10	-	9.0	50
THICK FILM ON ALUMINA	4	4	10	10	10	5	2250	10.0	5
CO-FIRED MULTILAYER ALUMINA	3	3	5	25	25	5-15	133	8.9	50
POLYIMIDE WITH COPPER	3	3	4	10	6	1-5	393	3.5	1
PORCELIN ON STEEL	10	10	10	30	3	5	365	6.5	5

THESE DATA SELECTED FROM "TRENDS IN INTERCONNECT TECHNOLOGY"

BY JAMES D. WELTERLIN, PROCEEDINGS OF ISHM, 1980, PP. 111-114

Table 4.1 Chart of Packaging Types

DIGITAL CLOCK RATE	CLOCK PERIOD	PULSE t_r, t_s	HIGHEST FREQ. COMPONENT	
			$\frac{0.35N}{tr}$ N=1	$\frac{0.35N}{tr}$ N=10
100 MHz	10 NSEC	2 NSEC	175 MHz	1.75 GHz
250 MHz	4 NSEC	0.8 NSEC	438 MHz	4.38 GHz
500 MHz	2 NSEC	0.4 NSEC	875 MHz	8.75 GHz
1 GHz	1 NSEC	0.2 NSEC	1.75 GHz	17.5 GHz
5 GHz	200 PSEC	40 PSEC	8.75 GHz	87.5 GHz

Table 4.2. Period/Frequency Comparison

Acceptable digital signal integrity probably occurs near the lower limit (N=1 column) regarding the highest frequency that must be propagated. Therefore, the highest frequency of interest in this study is approximately 15-20 GHz. Table 4.3 indicates the corresponding wavelengths for the N=1 column:

FREQ	FREESPACE λ (cm) = $3 \times 10^4 / f(\text{MHz})$	DIELECTRIC λ (cm)	DIELECTRIC $\lambda/8$ (cm)
175 MHz	171	114	14.3
438 MHz	68	45	5.6
875 MHz	34	23	2.9
1.75 GHz	17	11	1.4
8.75 GHz	3.4	2.3	0.3

Table 4.3. Frequency/Wavelength Comparison

Assuming that the propagation velocity along a conductor supported by a dielectric is 2/3 that of free space, then the third column applies. The fourth column indicates an eighth wavelength; physical length of line longer than this dictates the use of transmission line theory, rather than merely considering the interconnection as a current-carrying conductor. Therefore, as a rough approximation at a digital clock rate of 5 GHz, any interconnection longer than 0.3 cm must be considered and treated as a transmission line. With a 20 GHz frequency component present, this "critical" distance is further reduced to 0.13 cm, or 0.052 inch. Obviously, these physical distances are extremely short, and complicate any analysis.

In a given analysis, at least three distinct parameters would be inputted by the user:

- o Clock rate of the digital logic input signal(s)
- o Rise time and fall time of the input signal(s)
- o The value for N (from 1 to 10) that will select the "level of signal purity" of interest (the default value is N=1)

The first two items and corresponding parameters (i.e., PER, TR, TF) can be automatically determined from the input data. If inputted separately by the user, then, especially if more than one independent voltage or current source is specified, the program-determined values for the above parameters are overridden by the user-specified values. Finally, these parameters serve two basic purposes:

- o They are used in the mathematical computation involved in the solution process for the application of interest.
- o They are used to automatically determine which level of models are to be used for the specific transmission line calculations and active device calculations. Again, these levels in the multi-level models can optionally be selected by the user.

There is an astounding amount of literature and information available treating modeling and analysis of various configurations of high-speed transmission lines. The most common types addressed are stripline, microstrip, coplanar, slotline and waveguide (19, 20, 26, 30, 44, 68, 69 and Bibliography).

Various approaches to time-domain simulation of transmission lines have been described in the literature. Branin's approach (11) for the transient analysis of lossless lines serves the needs of modeling when the conditions are such that the interconnect transmission line is indeed lossless. It is a computationally efficient algorithm that is cited in many papers.

Groudin's method (25) for the analysis of resistive lines applies to low impedance terminated lines that exhibit a high resistance due to the small conductor cross sections. The method permits time domain simulation of single lines or of coupled lines that are in a homogeneous medium. However, the approach is limited to frequencies at which skin effect is not present.

Wright and Gasiorok co-authored a study (81) in 1972 for the Air Force Weapons Laboratory that is based on an approach that can be applied to "any" transmission line configuration, including those used in the microwave region. This approach was developed for the class of n-conductor transmission lines, and is used in conjunction with the SCEPTRE program. The model treats the wave propagation by handling each of the orthogonal independent modes as an independent transmission line. The lines incorporate terminal-to-mode, and mode-to-terminal converters at each end of each single line. Differential velocity effects were correctly predicted and verified by the authors of the method. The work described is based on even earlier SRI work that resulted in an advanced transmission line modeling program called MODMAN. The "building block" method can be used for characterizing single and multiple-mode transmission lines and devices, including:

- o Multiconductor systems
- o Multimode systems
- o Uniform and nonuniform lines
- o Lossy lines
- o Dispersive lines and devices
- o Distributed sources and loads (for EMP effects)

- o Time-dependent line and load effects
- o Nonlinear effects
- o N-port scattering-matrix device descriptions
- o Time-domain scattering representations for N-port devices
- o Coupled-line devices
- o Distributed electron device modeling
- o Automated transmission-line and device-parameter measurements

The SRI report indicates "all the important effects on transmission-line systems have been categorized and can be synthesized by one or more of the basic building blocks". MODMAN has been used at SRI for a variety of microwave problems. The model description can be described by quantities such as impedance, propagation velocity, and length, for all model behavior of transmission lines.

An important point is that the property of orthogonality permits the representation of a multimode line by parallel single-mode lines. One such multimode line is the microstrip.

The SRI approach is essentially that of representing a transmission line with a time-delay generator at the receiving end of the line to represent the electrical length. Lossy effects can be accounted for. This approach is quite different than that of representing the transmission line with many RLGC sections, which generally requires much more computer running time. This model is compatible with such programs as SCEPTRE, CIRCUS, NET-2 and ASTAP. No calculation is performed in the frequency domain; all calculations are accomplished in the time domain.

Techniques related to that of Wright and Gasiorok have been described in (6, 21). Sperry Univac experience regarding the approach in Reference 21 has shown that the subfunction FDLAY should not be used if the two-way propagation delay is less than the original rise time. The general approach could be used, but would have to be modified. It is, however, applicable to both lossless and lossy lines of various geometries. The propagated response is represented as a time delay component and a waveshape component.

Bernstein (6) shows that simple networks can be used to represent dispersion and skin effect of homogeneous linear transmission lines.

In another approach (24), the ASTAP program is used to analyze both ideal (lossless) and lossy lines in the frequency and time domains. An overview of the approach is presented, but the details (program coding, etc.) are considered proprietary.

Blood (8) describes in detail a conversational BASIC program for the analysis of a transmission line for ECL designs. This program was effectively used by Sperry Univac to aid in development of design rules for ECL layouts. The program has not been updated by the original author, and is limited to the analysis of lines with lumped loads. Another reference (56) also describes this approach.

Lubell's approach (40) utilizes the Defined Parameters input data capability in the SCEPTRE program to treat terminal models of transmission lines. This technique is similar to that of Wright and Gasiorsek.

The Stienhelfer approach (28, 42, 71) is being used by a large number of organizations for the purpose of model development of a wide variety of physical systems, including transmission lines. The approach uses a special software package called TIME-ED that works in conjunction with the HP-8542B Automatic Network Analyzer. Observing any point along an existing transmission line, TIME-ED permits modeling in the frequency domain that can ultimately be translated to the time domain. Models for lines, circuits or systems can be called by a time domain program that in turn can be used to plot the particular configuration of interest. For certain circuit types, the time-domain data can further be reconstructed in the frequency domain for possible comparison with the original data.

Allen's article (2) presents yet another approach for transmission line modeling that utilizes the SCEPTRE and SPICE programs. It is this approach which this study recommends for the solution algorithm, described later in more detail.

The majority of the treatments in the literature tend to be very theoretical in nature, and hence it is difficult to immediately describe a particular configuration in terms that can readily be incorporated into a software package. Some of the above approaches could be utilized in the CAD/M system of interest for certain applications (e.g., Blood's approach for ECL). However, the goal is to recommend an approach that can handle a wide variety of interconnect and device possibilities, and, within that approach, include those effects that must be modeled for HSI applications. This should be done in a manner that provides multilevel models (54), each level treating additional higher-frequency effects.

4.2.3 Line Coupling

Some lines may be active while others are passive. Only if the latter are subjected to crosstalk effects need they be included in the coupling analysis. These effects are based on parameters such as line spacing, signal amplitude on active lines, loads, lengths of parallel segments, etc. A given passive line may also have segments that include the representations in Figures 6.1 and 6.2.

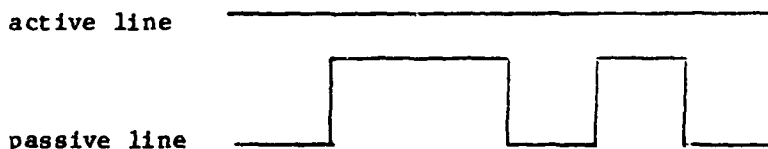


Figure 6.1. Line Segments Coupled to a Single Active Line

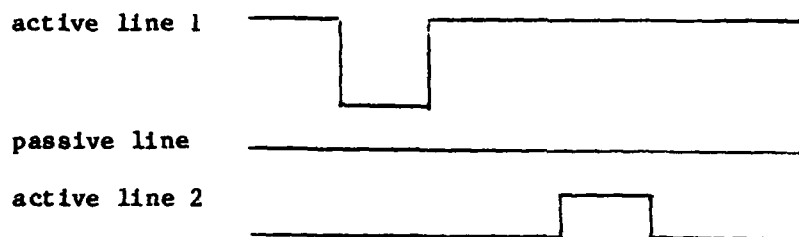


Figure 6.2. Line Segments Coupled to Multiple Active Lines

Such configurations considerably complicate the analysis because such lines must then be analytically segmented to properly account for the multiple signals being coupled. Because of time shifts (between the signals being coupled to segments of a given physically continuous line) and impedance mismatches encountered at various points along a given line, the interaction of primary (noncoupled) signals and secondary (coupled) signals becomes extremely complex from an analytical viewpoint.

In some cases, the coupling effect serves useful and desirable functions (e.g., couplers, filters, etc.). In most cases, especially on a PCB or ceramic-based substrate package, line-to-line coupling between the majority of lines is undesirable, and may even prevent the circuit from properly functioning.

A pair of coupled lines will exhibit two unique modes of propagation, each with unique characteristic impedances. For homogeneous lines, the two modes will have identical propagation velocities. In an inhomogeneous medium (e.g., microstrip), each mode exhibits a different velocity. Coupled lines are symmetrical if they are identical; if unlike, they are asymmetrical. Quasi-static analysis can be applied for the TEM mode; fullwave analysis is required for non-TEM mode coupled lines.

In the case of coupled microstrip or coupled coplanar lines, four methods of analysis are used (26):

- o The even and odd mode (53)
- o The coupled mode formulation (31, 39)
- o The graph transformation technique (59)
- o The congruent transformation technique (14, 27)

The first is indicated to be most convenient for symmetrical coupled lines. The second method can also be applied to asymmetrical lines, and can be used for all types of coupled lines. The last two methods use equivalent networks and are effective when more than two lines are coupled together. This is the likely case in HSI applications.

To minimize the complexity of the CAD/M system, one is tempted to choose a single coupled-line analysis technique. However, because a variety of line configurations exist, with many combinations of coupling possible, it appears best to specify more than one approach.

It is recommended that all four methods be installed in the CAD/M system, with the default method using the coupled mode formulation. Then, depending upon user-specified input data and/or program-determined information, a selection is made as to which analysis technique is to be used for each case of coupled lines within a given overall network. Such an approach is similar to that whereby more than one integration routine (algorithm) is available in a given CACA tool; the user is afforded the option of selecting one to be utilized for the analysis of interest. In the present case, with more than a single algorithm available within the CAD/M system for treating coupled lines, the best analytical choice available can be made for each situation. Two parallel lines that are coupled only to each other will then be analyzed using a method different from that to analyze many segments (entire lines or segments of lines) that are coupled to many other segments. As always, accuracy and computational efficiency are prime concerns.

4.2.4 Discontinuities

The topic of discontinuities involves not only the detailed mathematical representation of each configuration of interest (e.g., bend, via, connector, etc.), but how to best utilize this information in a larger CAD/M concept. Several authors treat the topic of line discontinuities (19, 26). Gupta, et. al. (26) also treats the coupling of coplanar lines. Reference 28 describes laboratory methods that can be utilized for "any" configuration to develop simulation models. Software is available to simulate discontinuities of certain line configurations.

A discontinuity in a transmission line forces the electric field lines to be modified; this causes a change in the line capacitance. Magnetic field charges are manifested in equivalent changes in the line inductance.

Dworsky (19) indicates that, with abrupt changes in the edges at the end of a transmission line, the fringing capacitance causes the electric field lines to rearrange themselves to satisfy electromagnetic constraints. A similar situation exists (depending, of course, on the frequency components that are present) with any abrupt changes. The surplus of electric field lines must "change position". Rather than solving this situation via Laplace equation techniques, Dworsky describes the "capacitance matrix approach". This 3-D technique reduces to a 2-D technique for certain conductor configurations. The algorithm requirement of having to examine a given geometry and then assign cell locations is a task that can, in part, be done by the LTC module (Figure 3.1). It is this type of calculation (discontinuity-related) that is done in the T-line calculation module. Because of the large quantity of cells that would be required for certain geometries, the method of images becomes especially attractive. Reference 19 contains a listing for a short FORTRAN program for the capacitance matrix solution for a stripline. Two program modifications are suggested by Dworsky:

- o Because of symmetry, only a fraction of a given physical configuration need be analyzed at the detailed cell level. This will reduce the array size requirements.

- o The coupling terms representing the voltage on one cell due to the charge on another cell can be determined in a interactive fashion, reducing program storage requirements.

Other FORTRAN routines are included in Reference 19, and could be included in the T-line module:

- o Calculation of stripline capacitance using a simple relaxation grid.
- o An improved method, using overrelaxation and prediction equations.
- o Overrelaxation and prediction equations for a boxed (enclosed) microstrip. This situation could be used to simulate a packaged hybrid ceramic substrate on which microstrip lines have been fabricated.

Gupta, Garg and Bahl (26) treat the topic of discontinuities in considerable detail. The authors indicate that since the dimensions of discontinuities are usually much less than the wavelength of interest, such discontinuities may be approximated with lumped element equivalent circuits. This is particularly true for thru-holes and vias. This approach lends itself especially well to a CAD/M approach, because the software can automatically determine, for each discontinuity, its location, type, and the equivalent lumped RLC network. Then, transparent to the user, the software can automatically insert such networks into the overall circuit description. The user initially inputs the original circuit, and can take two approaches:

- o Manually specify the discontinuities by calling the appropriate models from the DIML. The user then specifies that the CAD/M system ignore inserting the appropriate networks.
- o Permit the LTC module to determine from the layout the appropriate network to be inserted, which can be called from the DIML. The T-line calculation module can be initially used to determine what the specific RLC network values must be, based on the actual layout dimensions.

Reference 26 includes considerable detail regarding quasi-static analysis (for static capacitance and low frequency inductance) which is accurate up to perhaps a few gigahertz. Beyond that, frequency-dependent parameters must be determined; the fullwave analysis approach is also included in the reference. For static analysis of microstrip capacitances, four methods are used:

- o Matrix inversions method (for any discontinuity)
- o Variational method (for gaps and open ends)
- o Galerkin's method in the spectral domain (for any discontinuities, but results (26) are for open-ends)
- o Using line sources with charge reversal (for any discontinuity)

The quasi-static method is used for the low frequency line inductance calculations. These results are applied for open ends, gaps, steps in width, bends, T-junctions, and cross junctions. It is this group of analyses approaches that is to be implemented in the T-line calculations module (Figure 3.1). The line dimensions are inputted to that module by the user and/or by the LTC module.

Fullwave analysis methods that include frequency effects are described, along with measurement techniques, in detail in the cited reference. As above, the analytical capability will best reside in the T-line module. Because the level of complexity is much greater, the argument is strong for using a build-and-test cycle to generate the discontinuity models.

Several methods are used to measure transmission line characteristics, including discontinuities:

- o TDR (time-domain reflectometry) approach (13, 18, 78)
- o Linear resonator method (26)
- o Stinehelfer approach (28, 42)
- o Network analyzer (72)

Such laboratory measurements are especially attractive for use in creating and verifying models of discontinuities that can ultimately be included in the DML. Bonding techniques are also relatively conveniently modeled using measurement techniques. These methods are similar to methods used for semiconductor device modeling, whereby the model exists in the software (in the form of equations), but the model parameter values must be determined via measurements on the actual devices. If these values are estimated (rather than determined via laboratory data), then the final simulation results are only as good as the "closeness" of the original data estimates.

Several models (FORTRAN IV subroutines) for generating the frequency dependent scattering matrix for microstrip discontinuities are available from Verlag H. Wolff in West Germany (80). The available software consists of the following:

- o STEP for excentric impedance step
- o OVSTEP for overlapping impedance step
- o YJUNC for bends and Y-junctions
- o BEND for twofold truncated bends
- o SYJUNC for symmetrical T-junction, 90°-bend, and symmetrical crossing
- o JUNCT for 90° -bends, truncated 90° -bends, symmetric and unsymmetric T-junctions, and symmetric and unsymmetric crossings
- o FILTER for microstrip filters

Documentation includes theoretical background, program description, test run, program listing and card deck.

The key consideration with this approach is that software must be generated that automatically transforms these frequency-dependent scattering matrices that represent the various discontinuity configurations to a form that is compatible with the time-domain solution process identified in Section 6.

4.3 Software Considerations

Transmission line models in the form of input data for a specific circuit analysis program, or models in the form of stand-alone programs or subroutines, that account for all (or even many) of the high-speed effects of interest in this study do not exist, or at least are not readily available. Those models that are available are generally quite limited or are too simplistic. Hence, significant work must be done to provide accurate, sophisticated models that can be used in conjunction with one or more time-domain analysis programs. For the most part, such an effort will require the integration of various available models and analysis concepts. Such information, at the required level of detail, was obtained from existing literature. The nature and substance of this information, however, requires a "compilation" of approaches, ideas and suggestions that ultimately will result in meaningful and useful model-oriented information which can be applied to software development.

The integration of models entails not only the identification of the models and corresponding equations and assumptions, but the method in which they can be installed in a software package. This installation involves the generation of subroutines for handling each model of interest, with probably more than one subroutine for a given model. In the case of active devices, the parameters of key interest are the terminal voltages and currents. In the case of transmission line models, several items are of interest, at least in the general case of accounting for the highest frequency components indicated in Table 4.2:

- o Interconnect line voltages and currents
- o Signal propagation delay times
- o Inter-line coupling (crosstalk, etc.)
- o Line losses
- o Dielectric losses
- o Signal distortion due to dispersion

The defining equations in the time domain for device models are usually such that the frequency effects are automatically accounted for. However, the transmission line models must (in the time domain) account for not only the time-dependent effects (delay, reflections due to mismatch, etc.), but also the frequency-dependant effects (skin effect, dispersion, line-to-line coupling, etc.). Therefore, the integration of interconnect models requires some form of merging the effects associated with the two distinct domains (time and frequency). It should be noted that many CAD programs exist which contain models for active devices. In contrast, few CAD programs contain transmission line models, especially models that accurately account for the types of effects discussed above.

SECTION 5

ANALYSIS OF HIGH SPEED CIRCUITS

This section addresses the availability of computer programs for characterizing high speed logic devices, the accuracy of the models contained therein, and the capability of the programs to accurately simulate performance. None of the analysis programs presently available to the general user community were found to have built-in models for the accurate simulation of nonlinear semiconductor devices accommodating the upper range of digital clock rates of interest in this study. Furthermore, none of the available programs include complete models that accurately describe transmission line effects (e.g., dispersion, coupling, etc.) that are present at frequencies of interest in this study. However, a wide variety of circuit analysis programs is available. They are "free" as public domain, for cost (possibly under license agreement), or solely through commercial time-sharing services.

Sophisticated CACA tools have been available for over a decade. Several of these are large, general-purpose public domain programs. Descriptive information exists for many CACA programs (7, 10, 32). Most of those programs have built-in models that represent active devices, and some of the programs include transmission line models.

There are three prime considerations that must be met for a time domain analysis program to be of value for HSI:

- o The CACA tool must be accurate for analyzing digital circuits with clock rates up to 5 GHz.
- o Models, preferably built-in, must be available for the device technologies of interest. This study has considered silicon-based and gallium arsenide (GaAs)-based devices.
- o The transmission line models, preferably built-in, must be available for at least several of the most commonly used interconnect types (e.g., microstrip, stripline, coplanar, etc.). Additionally, these models should account for the high frequency effects referred to earlier in Section 4.

Other requirements of a time-domain circuit analysis program for high-speed digital circuits are:

- o Must perform nonlinear time-domain analysis
- o Must perform the analysis within acceptable CPU time and cost
- o Must be reasonably transportable to other computer installations (e.g., language, structure)
- o Must be relatively easy to use

Although the present circuit analysis user community has a large number and variety of programs at its disposal, the number of appropriate available programs that can be considered readily transportable to a variety of computer systems is significantly fewer, especially when one limits the selection to general purpose, large signal, nonlinear, time-domain analysis programs.

5.1 CACA Tool

The main purpose of the CACA tool in the proposed CAD/M system is to perform time-domain analysis of the network, including the effects of the interconnects which must be treated as transmission lines. This tool is essentially the "heart" of the CAD/M system, not only because of its analyses functions, but also because it normally interacts with several other functions in the system (e.g., model library, user, LCT module, etc.). The CACA tool must have stand-alone capability that still permits the user to analyze transmission lines and layouts of interest without requiring the use of the other modules in the proposed CAD/M system.

Because of the complexity of the network to be analyzed, especially when one considers the interconnects and transmission line (electromagnetic) effects and the resulting size of the matrices to be solved, large scale programs and attendant solution techniques must be considered (58).

5.2 Available Programs

Several programs that were considered for potential future use in characterizing high-speed logic devices and transmission lines include:

- o SPICE (Simulation Program with Integrated Circuit Emphasis) (15, 37, 48, 75)
- o SCEPTRE-II (System for Circuit Evaluation and Prediction of Transient Radiation Effects) (60, 61, 62, 63)
- o SUPER*SCEPTRE (An enhanced version of SCEPTRE that contains a front-end preprocessor for handling other disciplines such as hydraulic systems, etc.) (73)
- o NET-2 (Network Analysis Program) (49, 50)

Three additional time-domain analysis programs that are particularly attractive from a capability standpoint, though not considered readily available for general distribution and installation, are:

- o ISPICE (Interactive SPICE); available on a commercial time-sharing basis through NCSS.
- o ASTAP (Advanced Statistical Analysis Program); an IBM program available for IBM computer installation.

- o ASPEC (Advanced Simulation Program for Electronic Circuits); available on a commercial time-sharing basis through Information System Design, Inc.

COMPACT (Computer Optimization of Passive and Active Circuits) (16) and the highly-improved version called SUPER*COMPACT, though not time-domain analysis programs, offer much in the analysis/optimization capability for small-signal microwave region problems, especially for transmission line studies. Both are available from COMPACT ENGINEERING, which is considering the addition of time-domain analysis capability to SUPER*COMPACT. The SUPER*COMPACT program provides the capability for a wide variety of transmission lines (microstrip, stripline, coplanar waveguide, and suspended substrate modes), and treats dispersion, discontinuities, multilayer metallization, dielectric losses, conductor losses, and surface roughness. Used as is, SUPER*COMPACT could be a valuable complement to the larger, general-purpose time-domain program addressed in this study.

Table 5.1 indicates the salient capabilities and features of several available candidate programs cited above. These programs were often referred to in the literature and in the survey responses as being used for time-domain analysis of high-speed circuits that incorporate transmission lines and high speed device models of interest or that could be so enhanced.

The selection of these candidate programs was based primarily on the common capability of time-domain analysis. Another approach could be frequency-domain analysis by defining software required to transform the frequency-dependent effects to the time domain for direct comparison with actual test data in the time domain. Many other factors were considered, including nonlinear elements and program flexibility.

The recommendations for changes to the CACA programs, and to the device models used therein, are based primarily upon the information gathered in this study, and upon the experience in such modifications at Sperry Univac. Two basic avenues exist, depending upon the type of analysis program being addressed:

- o With SCEPTRE or similar programs, device models can be modified within the structures and formats of the input data, and can be done by the program user.
- o With SPICE or similar programs, devices can best be handled as built-in models, which require program modifications, a much more involved process which must be done by people familiar with the program functions that also have programming experience.

PROGRAMS	DC (NONLINEAR)	AC (LINEAR)	TR (NONLINEAR)	BUILT-IN TRANSMISSION LINE MODELS	BUILT-IN DEVICE MODELS	USER-DEFINED SUBROUTINES	FLEXIBILITY	DIFFERENTIAL EQUATION INPUTS	HANDLE SYSTEM-ORIENTED PROBLEMS	OPTIMIZATION	STATISTICAL ANALYSIS	MAINTAINED/ENHANCED	DOCUMENTATION (ALGORITHMS, ETC.)	CONVOLUTION
SCEPTRE-II	X	X	X			X	X	X	X				X	
SUPER*SCEPTRE	X	X	X			X	X	X	X			X	X	
NET-2	X	X	X	X	X	X	X	X	X	X	X	X		X
SPICE (2G.1)	X	X	X	X	X								X	

Table 5.1 COMPUTER-AIDED CIRCUIT ANALYSIS PROGRAMS

A series of tests have been run on several programs, including SUPER*SCEPTRE, SPICE and NET-2, to determine their run times and simulation accuracy (10). Of the three programs above, SPICE was shown to be the fastest and SCEPTRE the slowest. NET-2 and SCEPTRE perform dynamic writing, compiling and collecting of FORTRAN subroutines, which also contributes to relatively long running times compared to SPICE. The accuracies described in that reference indicate different combinations of best-to-worst for these three programs, depending on the circuits being simulated. Subsequent modifications to the programs affected running times, with SPICE remaining the fastest.

For several reasons, one must always use caution in such comparison of programs:

- o There may be a significant difference between the device models, whether built-in or user-defined. The model topology and/or model equations may differ enough, even if considered subtle at first glance, to affect results.
- o Depending on the circuit being simulated and the corresponding parameter values, the numerical analysis techniques can affect both the accuracy of the results and the computer running times. User selection of the integration method (if that is an option) can also considerably affect the results.
- o Built-in default values, for such items as convergence tolerance criteria, can also significantly affect accuracy and running times.

Some of the general considerations of circuit analysis programs that are of interest in this project are listed below:

- o Availability - The ideal case is public domain software, that is normally available at zero or very low cost. Depending upon the computer facility on which it is intended to operate, installation can be very simple (copying tape contents to a catalogued file) or very complex (involved conversion, installation and checkout). Especially in the latter case, excellent documentation is a prerequisite.
- o Capabilities, features and options - The main consideration is whether the software is applicable to high-speed interconnections, either as is, or after enhancements are added. This includes transient analysis, plotted output, ability to reference user-defined subfunctions, user selection of integration routine, etc.
- o Universality - This somewhat nebulous factor signifies the value in selecting a program that has a wide user base. This simplifies the communication process between users, and serves to introduce a high level of uniformity among various users and organizations, which in turn can improve user confidence.

Another consideration of importance is transportability of the software from one computer to another. Because of the complexity of NET-2, it would be difficult to transport it to different computers if conversion is required. The level of difficulty would be less for SCEPTRE (all versions), and the "easiest" for SPICE. This is in large part due to NET-2 and SCEPTRE being more "systems" than "programs"; SPICE is a "fixed program", rather than a "system". Beyond this consideration, any software is generally more readily transportable if written entirely in ADA, FORTRAN, PASCAL or some other high level language (HLL), rather than including any machine code.

A very important point to consider is that of the available documentation for a given program. Enhancements for incorporating improved or new models can require considerable modifications to the software. Unless complete and accurate documentation is available, any significant software development effort is destined to failure. Excellent documentation includes not only program subroutine descriptions, flowcharts and background information, but well-annotated source code to clarify the program flow.

5.3 Implementation Considerations

Closely associated with the concept of transmission line modeling is that of high-speed device modeling. Again, two distinct approaches are possible, depending upon the circuit analysis program of interest:

- o Programs such as SPICE, ISPICE and ASPEC are "closed" in that the executable program is fixed, regardless of the problem to be solved. Unless the model of interest is built into the code of the program, there is no convenient method to utilize the model, or to input corresponding model parameter values. To incorporate an enhanced or new model, the analysis program must be modified. Depending upon the nature and complexity of the model, such changes can be very involved, requiring the modification of several existing subroutines. These subroutines include:
 - The model equations for all desired effects
 - The input data error-checking
 - The modification of numerical analysis techniques that are model-dependent
- o Programs such as SCEPTRE and ASTAP, are "open" in that the complete analysis involves two or three separate and distinct executable programs. This affords great flexibility from a modeling viewpoint compared to a "closed" program, but is more cumbersome and expensive to use. The models can conveniently be referenced by name from a model library, but for initial design, development and acceptance of each particular model, the procedures for utilization of user-defined expressions and/or user-defined subfunctions is required. The models for such programs are actually "external" to the program, and consequently the model development is somewhat more straightforward.

In a "closed" program, the user provides values that correspond to the built-in model equation parameters. Otherwise, built-in default values are used. In an "open program", the user provides the model equations and tables, including all pertinent parameter values. The exception to the latter would be a conversational handler (or some other type of user interface) that would allow the inputting of parameter values that in turn are automatically inputted to the model proper.

A compromise is to merge the two concepts described above ("open" and "closed" programs) to ultimately develop an analysis tool that offers the best of both techniques. That is, utilize a program such as SPICE, develop the models as external subroutines, and during user execution, combine the new software with the relocatable elements of SPICE to generate the executable program. This technique is essentially that used by SCEPTRE.

The actual implementation of high-speed device models and transmission line models should permit several levels of simulation complexity (54). Each level will provide a model with an accuracy sufficient for a specific upper frequency limit. This is similar to the capability of SPICE for transistor simulation, wherein the user can indicate the model level of interest. Hence, overly complex models, with their attendant greater CPU running times, will not be used for applications involving lower digital clock rates.

A fundamental point is that no single circuit analysis program incorporates all of the capabilities, features and models of interest for the accurate characterization and simulation of the principal high-speed interconnect configurations and source/load device representations of interest.

This study recommends that the SPICE program be the CACA tool for incorporation into the proposed CAD/M system. The SPICE program was selected for several reasons:

- o Built-in models
- o Fast computational speed
- o Widely used throughout the world
- o Written in double-precision, ASCII Fortran language
- o Relatively easy to use
- o Well documented
- o Dynamic memory allocation
- o Presently installed on a variety of computer systems
- o Relatively easy to convert from one computer system to another (for software transportability considerations)
- o Continuously being improved.

The basic disadvantage with SPICE is that it lacks the flexibility of SUPER*SCEPTRE or ASTAP. It does not permit the direct inputting of mathematical expressions, tables, or user-defined subfunctions. However, as stated above, SPICE could be modified to function as an "open" program, such as SCEPTRE or ASTAP.

SECTION 6

THE MERGING OF INTERCONNECTS, DEVICES, AND ANALYTICAL SOFTWARE

The "integration" process is the manner by which the various models for interconnects and devices can be included in an analysis tool. In this study, the tool chosen is a time-domain program. Such integration basically involves the inclusion of the pertinent mathematical relationships and corresponding variables and values for the models.

The key questions addressed in this integration process were:

- o What major trade-offs are required?
- o What models (transmission line and devices) and characteristics are of interest?
- o How can these models be incorporated into the CAD/M system, particularly into the CACA tool?
- o What quantitative design rules are appropriate for the CAD/M system?
- o How can the pertinent parameters for these design rules be inputted to the CAD/M system?

6.1 Major Trade-offs

There are two initial questions that must be addressed prior to the consideration of incorporating and merging the elements of interest in this study:

- o What type of modeling approach should be used for interconnections (transmission lines)?
- o What problems exist with device and interconnect models "talking" to each other and to other portions of an analytical tool?

6.1.1 Time Domain Analysis Versus Frequency Domain Analysis

Built-in device models (including those that can be added for new high-speed devices) are currently described with simultaneous nonlinear equations and tables. These are solved "as is" for DC and transient analysis in the time domain. Performing device analysis in the frequency domain for large-signal digital circuits requires a set of nonlinear S-parameter equations for device characterization. This requires a complex modeling process.

Transmission lines can be mathematically described by several methods, e.g., Maxwell's equations, Kirchoff's equations, or a set of equations representing characteristic impedance, propagation velocity, etc. Essentially all of the line characteristics are a function of frequency (e.g., skin effect, dispersion, line losses, dielectric losses, line-to-line coupling, discontinuities, etc.). Consequently, analysis is more readily performed in the frequency domain.

Regardless of which domain the analysis is performed in, the eventual goal is to be able to simulate the chip interconnects, sources and loads in the time domain. Hence, some transformation were considered, such as:

- o Fast Fourier Transformation (FFT) from the time domain to the frequency domain of the input signals to the interconnects; utilize the line characteristics to determine the frequency amplitude and phase at the "load" locations; subsequent transformation of the solutions back to time domain waveforms at those locations.
- o FFT of the interconnect equations from the frequency domain to the time domain; utilize these "models" to perform the time-domain analysis, as would be performed with other time-dependent elements.

The signals on a given transmission line will exhibit reflections wherever impedance mismatches between the line and load exist. This phenomenon complicates the time-domain analysis, particularly with nonlinear loads that active devices present. Moreover, it further complicates a frequency domain analysis: how can existing impedance mismatch and reflections be accounted for? Reflections critically impact numerical analysis solution techniques and accuracies.

The inductive coupling between parallel lines (coplanar or interplanar) that results in crosstalk is a function of several parameters, including lengths of parallel segments, dielectric, signal on the source line, and line spacing. Capacitive coupling between lines at interplanar crossover locations is also a function of several parameters, including "common overlap area", dielectric, and distance between lines. Such crossovers also affect the line impedance by contributing to the distributed capacitive loading. Both types of coupling contribute to the complexity of the analysis, whether done in the time or frequency domain.

Transmission line discontinuities (e.g., bends, etc.) must be considered and included at high digital clock rates. Discontinuities are more readily represented in the frequency domain. Hence, there was merit in considering that the "total" interconnect analysis be performed in the frequency domain.

6.1.2 Interconnect Modeling Approach

A prime topic is that of modeling the chip interconnects. Several basic approaches are available for use in conjunction with available CACA programs:

- o Built-in transmission line models, as in SPICE and NET-2. The lossless model in SPICE is too limited for the higher frequency needs of this project. The NET-2 program is presently limited to a lossy dispersion model.
- o Multiple RLC sections that are used to model transmission lines, in nearly any configuration (e.g., series lines, junctions, stubs, etc.). This approach, although fairly easy to utilize and accurate for simple configurations at the lower clock frequencies addressed in this study, lacks the sophistication and accuracy required for the upper clock frequencies. In addition, the large number of RLC sections required to simulate an electrically long line (or combination of lines) generally results in prohibitively long computer running times. This aspect must be evaluated on a cost-effective basis, and often this information is available only after experimental simulation runs.
- o Use of the input language flexibility provided by such programs as NET-2, and SCEPTRE (and its variations) for inputting equations, or referencing user-defined subroutines that represent the transmission line models (40).
- o Sophisticated enhancements to a particular circuit analysis program to provide the accurate approaches and equations required to simulate high-speed transmission lines. Each such enhancement would, in general, be required for each type of line (e.g., microstrip, stripline, etc.).

6.2 Models of Interest

The available models (with few exceptions) do not exist as "nice, clean, compatible" coded models, but rather generally exist as theoretical expressions, or in some limited cases, FORTRAN subroutines. This is true for the interconnects, the devices, and other entities such as connectors, vias and discontinuities. Thus, a large part of the integration task is to determine what is necessary to "pull all of the loose ends together" into a description that is accurate, concise, and workable.

There is a great similarity between the approaches commonly used for semiconductor device modeling for CAD software and the considerations for interconnect (transmission line) modeling. The important aspects include the determination of an appropriate model (equations and constraints) for each line type of interest, an indication of the corresponding model parameters, how these parameters can be incorporated into existing software, and how the parametric data can be inputted. Additionally, model data parameter acquisition and a model data library are important for any modeling activity.

6.2.1 Device Models and Characteristics

None of the programs mentioned above have, in the readily available "standard" versions, a built-in model for the gallium arsenide (GaAs) technology devices. Of course, with SCEPTRE and ASTAP, one "builds" a device model that can be included in a device model library for subsequent reference. Silicon technology transistors perform acceptably up to approximately 1 to 2 GHz (1980), and it is anticipated that this will increase to 3 to 4 GHz by 1985 (54). Therefore, nonlinear large signal GaAs device models must be incorporated if design aids are to provide accurate simulation results up to the study goal of 5 GHz digital clock rates.

The active device nonlinear models of particular interest in this study are silicon and GaAs. Other devices that may be of interest in the future include Josephson junction (JJ's) transistors and charge-coupled devices (CCD's) (See Bibliography). Several items which must be defined at the outset of any analysis are:

- o Device type and appropriate model and level. The level selection is associated with the frequency range (model complexity) of interest.
- o User inputted parameters which override built-in default values.
- o Estimated junction temperature based on ambient temperature, the junction-to-ambient thermal resistance, and the power dissipation in the junction. The analysis program should automatically calculate the junction temperature for each device and adjust the affected model equations accordingly. This will account for the temperature gradients across a particular package (PCB, etc.).
- o Options selected (e.g., request for certain "internal" device parameters to be printed and/or plotted).

One of the very few papers available that described, in detail, the approach to modeling the large signal characteristics of a GaAs MESFET is that by Willing, Rauscher and deSantis (77). The method used time-domain analysis and includes the bias dependence of the small-signal model parameters. This effort was oriented towards large-signal microwave applications, but the findings prove interesting for the purposes of this HSI study. The bias and frequency dependence of the device scattering parameters were determined experimentally, including the use of a time-domain program. The nonlinear model that was developed for the CACA tool includes Gunn domain effects. S-parameter measurements were done from 1 to 10 GHz. Least-squares curve-fitting within the model showed good agreement with the measured data up to 18 GHz (approximately the upper limit considered in this study).

The GaAs MESFET transistor has been reported by others to have been successfully modeled for incorporation into CACA tools (4).

Dr. Michael Shur of the University of Minnesota has indicated the development of four programs for the simulation of microwave devices, including:

- o Static I-V of ion-implanted GaAs FETs
- o Simple and very fast model to calculate I-V and/or small signal parameters of a nonlinear equivalent circuit
- o Quasi two-dimensional model (does the same as the second program above)
- o Full two-dimensional simulation program

The first three programs (available) are for GaAs; the last is for any semiconductor. Of these four programs, the second is the most appropriate for the purposes of this study.

Shur and Eastman (65) describe a FORTRAN program for the simulation of MESFETs or JFETs. Si, GaAs, InP or other devices can be simulated. The following two-dimensional features are accounted for:

- o Field distribution
- o Possible Gunn domain formation
- o Diffusion effects
- o Contact and substrate resistance
- o Ohmic resistance of the gate-to-source sections
- o Ohmic resistance of the source-to-gate sections

The program can easily be enhanced to include field-dependent diffusion effects. Related references included (64, 65).

Chapter 2 of Milnes (47) indicates pertinent equations for Schottky-Barrier diodes. Chapter 6 treats JFETs and MESFETs and Chapter 7 treats MOSFETs, the latter including CAD techniques using the M-SINC program. All of this material is very pertinent to the CAD/M study.

Though specific CAD-oriented software models for GaAs devices are not explicitly defined in the references (5, 17, 23, 38, 43, 57, 83), key concepts, equations and approaches contained therein are excellent foundation for the generation of sophisticated CAD models to be included in the CACA tool and DIML for HSI applications.

6.2.2 Interconnect Models

The transmission line models of interest in this study are models of coaxial cable, twisted pair, flat ribbon cable, microstrip, stripline and coplanar. The design rules for the first three types are different than for the last three, primarily because the latter three are normally used at the highest frequencies of interest, and they usually contain several bends, crossover points and distributed loading that affect signal propagation and integrity.

The models for any type of line are not isolated, but are associated with various other items such as sources, loads, discontinuities, connectors and other lines. This impacts the actual implementation in software because the signal characteristics (integrity) along the interconnect line are a function of much more than just the line properties. Consequently, several items must be identified:

- o Line type (microstrip, etc.)
- o Line parameters (width, spacing, length, etc.)
- o Material (conductor, dielectric, other)
- o Loads (type and location)
- o Frequency range of interest (e.g., highest frequency component in the fastest signal transitions anticipated on the line)
- o Options (e.g., whether or not to account for, in the simulation, certain effects such as skin effect, dispersion, crosstalk, etc.). Such a set of options can do much to decrease computer time for "initial look" analyses, such as feasibility studies.

One of the powerful features in SPLICE (Simulation Program for Large Scale Integrated Circuit Evaluation) (51), a multilevel simulator, is that it dynamically determines which portions of the circuit are active and which are passive with respect to signal changes. If the signals and device parameter values in a certain portion of a circuit are changing rapidly, then the analysis of that portion is treated algorithmically differently than that portion that may be "OFF" or at least static from a functional viewpoint. There are more calculations (and calculation time points) required in the "dynamic" portion than in the "static" portion, where all calculations tend to remain relatively constant.

This approach differs from SPICE, in that SPICE uses an automatic time step control algorithm that takes narrower or wider subsequent time steps, depending on how many integration passes are required for the solution process to satisfy all of the convergence criteria.

In SPICE, all portions of the circuit are treated in an identical manner in that a given time step applies to every pertinent time equation in the circuit. Obviously, some portions of a circuit may be changing rapidly while others are idling because of the signal levels at their respective input terminals. Solution calculations are redundant and computationally wasteful for the "idling" circuits. A critical decision is that of determining whether a circuit is static (idling) or dynamic. If not done properly, accuracy suffers, with meaningless end results.

Because of the nature (functional operation) of the circuit/interconnect configuration, the complexity of the calculations, and the size of the circuit, this "scheduling" approach for the solution method appears extremely attractive. This is particularly true wherein both high speed digital circuits and the interconnect lines between the IC chips are being analyzed. The time delay along the transmission lines introduces an element that "promotes" the concept of both dynamic and static circuits in a given configuration being treated differently from a solution algorithm approach.

6.3 Implementation

The primary mathematical expressions that are related to any given line type, and the solution approach to be used to solve for the voltages and currents on a given line need to be addressed. Because of the nature of the line equations and the number of parameters involved, particularly at the high frequencies, an important aspect in the solution method is to calculate, whenever possible, the parameters and variable values on a one-time basis, rather than for each line at each time point or frequency point. These "fixed" values then can be uniformly utilized wherever and whenever needed.

There are several means by which various line configurations are analyzed, and by which the defining equations are determined (22, 26, 30). They include static, quasi-static and fullwave analysis.

The degree of difficulty increases towards the latter. Also, various mathematical constructs can be used, including:

- o Finite difference techniques
- o Finite element techniques
- o Conformal mapping techniques
- o Integral equation approach to partial elements (PEM)
- o Partial element equivalent circuits (PEEC)

A major difficulty is that, if the detailed line analysis is not done "selectively" (for certain selected lines) in a large circuit layout, rather than for the "entire layout", a prohibitive amount of computer time and memory will be required. The selective approach is used by Hewlett-Packard with their DESIG software system (45). This approach can be used effectively to reduce "the whole circuit" to only those portions or segments that need be treated in a given time.

The entire CAD/M approach for high-speed interconnects is very heavily dependent on the methods and details of integrating the transmission line models and necessary high-speed device models into the CACA tool (Figure 3.1). The effort of integration of the models consists of considering and defining the method(s) by which circuit analysis software can contain or reference the appropriate combination of models for devices and transmission lines. Of these two "classes" of models, the easier to incorporate is device modeling, for three main reasons:

- o Many analysis programs contain nonlinear models, so the inclusion of more sophisticated models or new device models is basically an extension of what exists.
- o Few transmission line models exist in the form of program source code that can be readily merged with existing software, especially for line models of sufficient complexity to accurately represent the high frequency effects of interest in this study.
- o A time-domain analysis of the devices is more straightforward than analysis of the interconnects, primarily because of the frequency-dependent nature of the latter.

The interconnect analysis approach is based on the SPICE program. Other programs can also be utilized in a complimentary way, prior to, or in conjunction with, SPICE. Certain model parameter values can be determined by SUPER* SCEPTRE; transmission line synthesis can be performed by COMPACT and SUPER* COMPACT. Such approaches are not required, but are likely situations.

The integration of the models is essentially an indication of how those models can be included in the SPICE program. The following items, as a minimum, should be considered in the actual software development:

- o Model equations must be installed in the software.
- o Model parameter values must be identified in such a way that the user can conveniently indicate the corresponding values, including the overriding of built-in default values.
- o The range limits under which the models are valid must be identified, both in the software and in the associated documentation.
- o The solution algorithms must be identified.
- o Appropriate input data checking procedures must be developed to ensure proper input formats and values that are in the acceptable ranges that correspond to the analysis equations and manufacturing techniques.
- o Appropriate error messages must be outputted to indicate not only the cause of the error (e.g., nonconvergent solution), but what the user should do to correct the situation.

With a program such as SPICE (which has built-in models, including a lossless transmission line model, and several device models), one can modify existing code to enhance the models or insert new models. The result is a "closed" program that remains the same for every problem that is inputted. SPICE can perform both frequency domain analysis (AC) and time domain analysis (TR); there is a possibility that some method exists to use both modes in a given analysis, whereby the AC and TR modes interact analytically with each other.

In a given circuit analysis program such as SPICE, there are several steps from input to final solution output. These steps are as follows:

- o The input data are read and checked for correct formats and acceptable circuit topology.
- o The solution matrices are formed, based on the input data.
- o The solution is obtained at each time value to determine the voltages and currents in the circuit. This operation is iterative, wherein each solution is checked to determine if the built-in convergence criteria are met before proceeding to the next time value.
- o The requested tabular or plotted solution results are generated.

Note that matrix formulation really depends on the built-in equations that represent each of the element models pertinent to a given problem description (e.g., resistors, capacitors, diodes, transistors and transmission lines). The key item is to provide those equations in a time-domain analysis tool in such a manner that the connected models interact properly and accurately. This is not an easy task because of the transmission line characteristics, and the fact that a given line may interact with other lines, sources, and loads. There is an interaction between any two elements (resistors, devices) that are physically connected, but generally this interaction is different than that for a connection to a transmission line, either directly or indirectly (inductive and/or capacitive coupling). Voltage/current reflections at one or both ends of a transmission line add an aspect to the analysis that becomes very important, and is difficult to efficiently model in any CAD implementation.

Because of the nature of the electrical characteristics of transmission lines (microstrip, etc.), several "submodels" are likely required to treat the various characteristics. For example, the main model can contain the equations for determining the line impedance, with various levels (subroutine paths) depending upon parameter values such as physical dimensions and dielectric constant. This main model, in turn, can reference other submodels that account for line-to-line coupling, crosstalk, losses, dispersion and discontinuities. This requires "multi-level" modeling. The actual integration is the passing of model characteristics (e.g., impedance, etc.) which the program utilizes in the numerical analysis solution process. The impact of the multi-level approach is felt in several areas:

- o It complicates the software development. Much more time and effort is required to introduce several models, compared to a single model, into a simulation tool. Unless a sophisticated overlay structure is well-planned and utilized, the resulting software size can become unacceptably large. Conceivably, different versions of the same interconnection analysis tool could be made simultaneously available to the user, with one being selected (manually or automatically) to best fit the technical problem.
- o It is computationally more efficient, in that only the level of model sophistication and complexity appropriate to the application is used.

- o Model enhancements and/or program debugging may become noticeably more difficult with the multi-level model approach.

A desirable software package would merge the routing, and possibly chip placement, with the electrical characteristics and performance of the interconnects in such a manner that the interconnect performance (voltage and current excursions on the lines) will help automatically determine the best of several alternatives to the routing.

Parameters must ultimately be determined and be inputted to a CAD/M system. Initial considerations include:

- o Formats for data input
- o Parameter default values
- o Parameter value checking per the built-in design rules described earlier.
- o The method(s) by which these values are utilized in the software (e.g., linked lists with pointers, as in the SPICE program, etc.).

A possible approach may be to define a preprocessor to the CAD/M system for interconnects that will offer conversational, interactive I/O as part of the user interface. Initial checking and setup could be accomplished at this stage that will do much to reduce cost and turnaround time.

Various design rules must be generated for different applications. Some are to be met by the designer, some by the software, and some may be a combination of these two. A typical rule that can be considered and eventually defined is based on the following approach.

Consider the parameters of microstrip line width and spacing. These parameters are important from the manufacturing aspect; depending upon the process (e.g., PCB or thick film), there are minimum values associated with each. From the interconnection routing aspect, maximum values apply so that there is sufficient area to perform the necessary net connections. From the line characteristic aspect, the dimensions affect impedance, propagation velocity, discontinuity, coupling (inductive and capacitive), and line losses; hence, certain paths through associated equations and subroutines apply, with correspondingly different solution accuracy and computer time.

Such considerations imply, at the highest level, design rules that are addressed directly by the designer (user). In this case, for line width and spacing, perhaps built-in default values can be identified in the documentation, each of which can be overridden by the user's input data. In this way, different manufacturing capabilities (sites) and/or improvements in materials and processing, and the related impact on producible line widths and lengths can be conveniently accommodated.

Another approach is to include certain design rules, such as acceptable line attenuation, within the software. The software can automatically alert the user if the attenuation exceeds the user-defined upper limit. Such an approach saves the user considerable time and effort.

6.4 Time Domain Algorithms

Two recent time-domain solution algorithms appear to be particularly appropriate for application to high-speed interconnections. Both have been described in the literature.

The first technique was described by James McClure (45). It uses the FFT and inverse FFT to transform the waveforms at particular predesignated nodes in a circuit. This method performs the following:

- o The time-domain signal at each source is transformed to the frequency domain to determine the amplitude and phase of each of the dominant frequency components.
- o The amplitude and phase of each of these components is calculated in the circuit at each node (physical location) of interest (e.g., at each load).
- o An inverse FFT is performed at these nodes to determine the time-domain waveforms. These synthesized waveforms indicate the amplitude/delay information which is of primary interest to the user.

The main limitation of this method is that linearity is assumed; this assumption is required to ensure that the FFT algorithm is usable. Obviously, this linearity restriction is too severe over the entire frequency range and signal levels of interest in this study. However, the algorithm is of sufficient value and interest to warrant serious consideration for implementation in the HSI CAD/M system under certain application restrictions.

The second technique was described by James Allen (2, 3). It permits the time domain solution of networks containing both transmission lines and lumped linear and/or nonlinear elements. The major advantage of Allen's approach is in the method for generating the system matrix which involves only sums of subnetworks, with the problem reduced to a solution of sparse algebraic equations. The network is automatically partitioned into two parts. One part contains only the linear distributed and/or lumped elements. The other part contains the independent sources and any lumped elements that are nonlinear or time-varying. Allen's approach is based on Silverberg's approach (66). A portion of the algorithm is similar to McClure's method in that an inverse FFT technique is utilized to solve the time behavior of the linear portion of the network once the frequency domain behavior has been determined. These results are then merged (convolved) with the time domain solution to the differential equations representing the nonlinear portion of the network. Allen indicates that Kron's transformation methods along with a port description were selected.

Short-circuit admittance parameters are used to represent every connection as a parallel type of connection. This requires that open-circuited ports be included in certain configurations. Obviously, such an approach requires additional software that will automatically determine these admittance parameters from the user-inputted network element/topological description. This software capability must be incorporated into the CACA tool to partition and model the network prior to the analysis process.

Allen indicates that any implicit integration method may be used. He used a trapezoidal method with a fixed time interval. A variable interval trapezoidal method and Gear-type methods may also be used; both of these algorithm methods are available in SPICE.

This solution algorithm is considered a hybrid approach in that both frequency domain and time domain analyses are utilized, each for different parts of the partitioned network. As stated earlier, the AC analysis mode capability within SPICE can conceivably be used to perform the frequency domain analysis with additional "interface software" required to permit the frequency domain and time domain matrices and solutions to interact properly with one another.

Time-varying reflection coefficients are accommodated by Allen's approach, a vital consideration for lines terminated with active loads. A future report by Allen will cover lossy lines, coupled lines, and other structures.

6.5 Design Rules for the CAD/M System

By definition, a "quantitative design rule" is that entity that governs, with a specific upper limit, lower limit, or both, some specific item(s) in the design process. An example is the maximum permissible interconnection line length. This limit is generally a function of several parameters and considerations, one of which may be the application itself. Some of the rules may be embedded in the software and alert the user if they are violated, along with a message regarding the specific violation.

An important portion of any interconnect activity is that regarding the constraints imposed on a particular configuration (or constraint that may force the choice of a given configuration), namely, the set of design rules. These rules are, in total, determined by constraints in each of a number of areas, such as:

- o Electrical characteristics of the transmission lines (e.g., controlled Z0)
- o Mechanical or fabrication factors (e.g., line widths, line spacings)
- o Thermal considerations (e.g., component placement based on heat source and flow)
- o Processing considerations (e.g., thick film, material properties)
- o Software constraints (e.g., data bases available, capabilities and limitations of software)

- o Testing considerations (e.g., the requirements to couple signals between lines, or to directly access specified lines using T-branching from connector pins to monitor signals)
- o Overall packaging constraints (e.g., package header type and distance affect transmission line electrical characteristics)

Design rules can serve two main functions. The first is that of ensuring that the configuration being simulated by a CAD program (or CAD/M system) is, in fact, physically realizable. This can also provide input data error-checking, so that a costly computer run is not made for an unrealistic physical/electrical description. The second is to determine which level (of several for a given model) will be used in the solution process for a given interconnect line configuration. In some cases, the model could "adjust" or determine specific design rules, rather than solely relying on the design rules driving the CAD/M software.

The design rule development is based on three major areas: mechanical, electrical and software. The mechanically-based rules are a function of such items as line types, line widths and materials. The electrically-based rules are a function of such items as circuit speed, signal rise/fall times, line lengths (for timing), discontinuities, loading, and line losses. The software-based rules are a function of the equations that represent the line characteristics, computer program, system constraints, etc. Obviously, these three areas are interdependent. The key consideration is that, if the simulation software is to accurately represent the physical system that will ultimately be manufactured and tested, and if the simulation equations are dependent upon certain constraints, assumptions, qualification, or limits, the user must be cognizant of those same items to enable valid and usable results. For example, if the equation representing the characteristic impedance of a microstrip line is valid for a certain dimensional ratio limit, then the user must know of such a limit to effectively utilize the analysis tool.

An important aspect of software-based design rules in a CAD/M system is that the system itself should not permit design, analysis or fabrication approaches that cannot be "handled" by such a system. For example, if the analysis tool does not accommodate a certain interconnection line type, then one of the rules would be to force the user to specify only those line models that are included if the CAD/M system is to serve its intended function. Another possible design rule would be one that is associated with the maximum number of interconnect lines that the analysis software can accommodate effectively (due to memory size or execution time limitations) as opposed to the number that can be accommodated by the routing software.

There are many potential design rules that can be incorporated in any given CAD/M system. Only those that specifically affect the topics of interest in this HSI study are included herein.

The following list of representative design rules that can be quantified in appropriate various CAD/M system modules is intended to focus on the aspect of HSI considerations that may affect the interconnect itself. Note that quantitative values are not included; specific values need be incorporated only with the CAD/M software when it is actually developed, using a technique that permits each user to specify input values to override the built-in default values.

Three fabrication technologies are considered: PCB, thick film and thin film. Some of the design rules are unique to a single technology, whereas other rules apply to two or three. Obviously, not all design rules necessarily apply to a given design. Some are critical regarding the impact on the electrical characteristics of the interconnect transmission lines. Each rule is stated along with an associated justification, and also an indication of the technologies to which it applies, using the legend P for PCB, K for thick film and N for thin film. Finally, the quantitative parameter(s) for each rule are identified; these are to be ultimately incorporated in various modules in the system (Figure 3.1).

1. Line width and spacing (P, K, N). This is perhaps the highest priority rule because it impacts layout/routing density, line impedance, and line-to-line coupling. LW, LS
2. Conductor (signal layer) thickness (P, K, N). Fabrication considerations, and current-carrying capability. Impacts line impedance and interlayer coupling. CT
3. Maximum line length (P,K,N). Primarily determined by electrical properties (attenuation, propagation delay, line-to-line coupling, number of crossovers). Fabrication considerations imply that, the longer the line (source to load), the higher the probable quantity of vias, thru-holes and discontinuities (bends). MLL
4. Internal layer thicknesses (P,K). A minimum is required for mechanical stability. Affects line impedance, capacitance and inductance values. ILT
5. Controlled impedance requirements (P,K,N). The specific circuit technology used (ELC, etc.) on a given interconnect line is the prime factor that determines the value of the required controlled impedance of each interconnect line, and every segment of the total line from source to load. The impact is somewhat the converse of many other of the design rules, in that, if the controlled impedance is of utmost importance, then the interconnect line dimensions (width, thickness, distances to ground and voltage planes, etc.), the materials used, and the fabrication considerations are highly dependent upon the required impedance specified. CI
6. Minimum allowable distance between routing (signal) lines and board/substrate edge (P,K,N). Minimizes structural problems, including dimensional stability. May impact electrical characteristics such as Z_0 due to fringing of electromagnetic fields. BE

7. Use of specific materials for internal and external signal layers (P,K,N). Fabrication considerations may affect conductor line losses. ISLM, ESLM
8. Use of ground and/or voltage buses on the same layer (P,K,N). Impacts interconnect electrical characteristics; may even result in a constraint to use coplanar configuration rather than microstrip or stripline. GB, VB
9. Specific conductor length-to-width ratios (P,K,N). Fabrication and reliability considerations. Impacts interconnect electrical characteristics. LTW
10. Component value ranges and tolerances (P,K,N). Determined by fabrication considerations. Impact is on the proper interconnect line termination resistors to obtain the required signal integrity. RX
11. Ground plane versus ground conductor or grid (P,K,N). Fabrication and/or line characteristics justify this rule. Impact is on essentially all interconnect line electrical characteristics. A similar rule applies to voltage plane versus conductor or grid. GP, GG, VP, VG
12. Board thickness (P,K). Maximum is specified regarding component insertion lead length. Impacts line inductance and capacitance values, and consequently, impedance. Also affects number of layers, including signal layers. BT
13. Via hole dimensions (P,K). Fabrication considerations. May impact interconnect line impedance, including discontinuity effects due to line impedance level changes. VL, VD
14. Placement of chips (P,K,N). Constrained by thermal, packaging, or critical timing affinity of circuits. May affect interconnect line length, number of crossovers, line-to-line coupling, etc. PLACE
15. Bonding types (P,K,N). Fabrication considerations, including such items as length of wire bond, etc. Impacts line impedance discontinuities, and also rework possibilities and results, which may change the discontinuity characteristics. BOND
16. Substrate material selection (K,N). Material and fabrication considerations. Has large impact on line characteristics due to relative dielectric constant value. SM
17. Quantity of lines that can be connected to a pad (P,K). Fabrication limitations. Impacts the electrical discontinuity effects of transmission lines. LTP
18. Maximum fanout (P,K,N). Logic circuit considerations. May impact placement, routing and transmission line loading (termination resistance). MFO

19. Maximum fan-in (P,K,N). Logic circuit considerations. May impact placement, routing and transmission line loading (termination resistance). MFI
20. Minimum/maximum load impedance (P,K,N). Electrical signal considerations. Impacts reflection coefficient on interconnect line, and also fan-in and fanout limits. MNLZ, MXLZ
21. Maximum crosstalk (P,K,N). Signed/noise considerations. Impacts the line spacing and line length (both coplanar and interplanar). May be a severe constraint that forces line type, material type and layout. MC, MCL (Note: MC is maximum crosstalk; MCL is crosstalk per unit line length.)
22. Acceptable noise margin (P,K,N). Constrained by circuit technology (e.g., TTL, ECL, etc.). Impacts placement, routing, interconnect configurations, and packaging configurations. ANM
23. Acceptable attenuation (P,K,N). Constrained primarily by interconnect configuration, materials and digital clock frequency. Impacts placement, routing, and interconnect. AA
24. Optimum line length (P,K,N). Constrained by signal level, line configuration, materials, digital clock frequency, and loading. "Optimum" in this case refers primarily to achievement of the maximum possible transfer of signal, subject to logic network constraints. Line loading (and corresponding reflection coefficients and signal reflections) are very important governing factors. OLL
25. Fanout point locations (P,K,N). Layout and electrical considerations. Impacts interconnect discontinuities, and consequently, signal integrity. Locations may be governed by digital clock frequency and interconnect configuration. FOPL
26. Maximum number of vias (P,K,N). Constrained by layout and electrical (discontinuity) considerations. Impacts layout density and signal integrity. MV
27. Signal attenuation versus line length (P,K,N). Interconnect configuration, materials, digital clock frequency, and loading are contributing factors. Impacts layout (placement and routing), interconnect types and loading. SAL

This representative list of quantitative design rules is not complete; specific users of a CAD/M system may enhance or modify it, depending on the particular system and end product constraints. Note that the design rules are not isolated entities; many rules directly impact one or more other rules.

As mentioned previously, the intent is to incorporate these design rules into the CAD/M system. The corresponding parameters are inputted by the user to the Design Rules and Specifications Module (Figure 3.1). This module, in turn, interfaces with all of the other modules in the CAD/M system. Any user-defined values automatically override built-in default values in each appropriate driven module. Hence, by inputting a new value of required controlled line impedance, the following modules (and corresponding built-in equations and checks) are affected:

- o CACA tool
- o Routing
- o Design rule checking
- o T-line calculations

Because most of the design rules ultimately "interact" with one another, it is difficult to separate them into groups (electrical versus mechanical, PCB versus thick film, etc.). A logical method is to form a matrix that indicates which rules affect which modules. The end result is that the proper modules are impacted by pertinent rules, and corresponding built-in equations and design rule checks are automatically updated. Note that, by inputting a parameter such as "PCB" to designate that the packaging will utilize printed circuit board technology, all pertinent design rule values can be modified "en masse". Similarly, by inputting "ECL", another set of pertinent parameters will be affected. Again, a key point to emphasize is that "ease of use" is a prime consideration in this CAD/M system.

Table 6.1 indicates the matrix that identifies which CAD/M system modules (Figure 3.1) are affected by (directly receive data from) the DRS module outputs.

DESIGN RULES	C A C A	P L A C E	O R D E R	R O U T E	D R C	L T C	T L C
1	X	X	X	X	X		X
2	X						X
3		X	X	X	X		X
4	X			X			X
5	X	X	X	X	X		X
6	X			X	X		X
7	X						X
8	X	X	X	X			X
9					x		
10	X				X		X
11	X						X
12		X	X	X			
13	X	X		X			X
14		X	X	X			
15	X						X
16	X						X
17		X	X	X	X		
18		X	X	X	X		
19		X	X	X	X		
20	X		X	X			X
21	X			X			X
22	X	X	X	X	X		
23	X	X	X	X	X		
24	X	X	X	X	X		
25	X	X	X	X	X		X
26		X	X	X	X		
27	X	X	X	X	X		

Table 6.1 Design Rule Parameter/Module Matrix

6.0 Integration From the User's Viewpoint

The end user is a very important element associated with a CAD/M system. The topic of the integration of interconnect and device models within an analysis program focuses on the manner in which the user can interface directly with the analysis tool. Because the tool recommended by this study is the SPICE program, the following discussion applies specifically to it. However, the general approach, and much of the detail, can also be applied to other CACA programs.

One of the basic premises of this study is that the CACA tool should have the capability of doing as much of the high speed interconnect analysis as possible as a stand-alone program. In this way, the user can take full advantage of the program without having to rely on "peripheral software" (e.g., placement, routing, DRC, etc.), to use the tool for feasibility studies, proposals, etc. The transmission line input and analysis approach within SPICE should, therefore, be similar to that already available in SPICE for transmission lines. That is, models for various interconnect configurations should be built into SPICE that can be conveniently accessed via the user input data.

For the six basic interconnect types that are of prime interest in this study, the immediate topic is that of identifying a reasonable format for SPICE user input data for each of the transmission lines in a given application.

Presently, SPICE incorporates a lossless model for a transmission line that requires the user to specify the line name, nodal (two-port) connections in the network, and the numerical values of the characteristic impedance and the total delay of the line. Alternatively, the user, instead of specifying the line delay, may specify the normalized electrical length at a specified frequency; a quarter-wave length is assumed if the length parameter is omitted. Optional initial conditions (voltages, currents) can be included to help "prompt" the analytical solution. This model treats only one propagating mode. If the four model nodes are topologically distinct, then two nodes may be excited, which requires the reference of two transmission line elements. All the nodes need not be connected (used), to allow for unterminated lines.

The following six sections indicate the proposed formats for various transmission line configurations that can be incorporated into a modified version of SPICE. Each of the line types has a unique keyword name and unique parameter names (similar to that of the other element types in SPICE). Some of the entries are required, whereas others are optional. If the latter are not entered, the appropriate default values are used. Note that these proposed input parameters and formats could be modified (improved upon) when an actual software development effort commences. Part numbers (P) reference a model in the DIML. When ZO is not entered, it is calculated by the program. A list of materials and appropriate properties would be an integral part of the program. English, metric or user dimensions can be specified.

6.6.1 Coaxial Cable

CC N1 N2 N3 N4 Z0 L D1 D2 P

where CC designates the line type

N1, N2, N3, N4 are the topological nodes

Z0 is the characteristic impedance (ohms)

L is the line length (inches)

D1 is the conductor inner diameter (inches)

D2 is the conductor outer diameter (inches)

P is the standard part type number (e.g., RG8U)

If P is entered, D1 and D2 are not entered or, if entered, are ignored.

Examples:

CC 1 2 3 4 Z0=50 L=36 D1=0.1 D2=0.2

CC 2 4 6 8 P=34812X15

6.6.2 Twisted Pair

TP N1 N2 N3 N4 Z0 L C W T M P

where TP designates the line type

N1, N2, N3, N4 are the topological nodes

Z0 is the characteristic impedance (ohms)

L is the line length (inches)

C is the conductor diameter (inches)

W is the wire diameter, including insulation (inches)

T designates the twists per inch (assumed uniform along the entire length of the line)

M is the insulation material type

P is the standard part number. If P is entered, C, W and T are not entered, or if entered, are ignored.

Example:

TP 6 14 22 9 Z0=100 L=3.7 C=.001 W=.002 T=6 M=510X

6.6.3 Flat Ribbon Cable

FR N1 N2 N3 N4 Z0 L WS WR S T M P

where FR designates the line type

N1, N2, N3 and N4 are the topological nodes

Z0 is the characteristic impedance (ohms)

L is the line length (inches)

WS is the width of the signal conductor (inches)

WR is the width of the return conductor (inches)

S is the space between the signal and return conductors (inches)

T is the thickness of the conductor (inches)

M is the dielectric type

P is the standard part number. If P is entered, only the nodes and the length need be entered; if other data are entered, they are ignored.

Examples:

FR 1 2 3 4 L=3.3 WS=5 WR=6 S=8 T=0.25 M=Ay

FR 1 2 4 7 P=PN501

6.6.4 Microstrip

MS N1 N2 N3 N4 Z0 L W T H M P

where MS designates the line type

N1, N2, N3 and N4 are the topological nodes

Z0 is the characteristic impedance (ohms)

L is the length of the line (inches)

W is the width of the conductor (inches)

T is the thickness of the conductor (inches)

H is the distance from the conductor to the ground plane (inches)

M is the dielectric material type

P is the standard part number. If P is entered, only the nodes and the length need be entered; if other data are entered, they are ignored.

Examples:

MS 1 3 5 9 L=1.85 W=0.007 T=0.0015 H=0.005 M=EG01

MS 1 3 5 9 L=1.85 P=4219M

6.6.5 Stripline

SL N1 N2 N3 N4 Z0 L W T H1 H2 M P

where SL designates the line type

N1, N2, N3, N4 are the topological nodes

Z0 is the characteristic impedance (ohms)

L is the length of the line (inches)

W is the width of the conductor (inches)

T is the thickness of the conductor (inches)

H1 is the distance to voltage/ground plane 1

H2 is the distance to voltage/ground plane 2

M is the dielectric material type

P is the standard part number. If P is entered, only the nodes and length need be entered; if other data are entered, they are ignored.

Examples:

SL 2 0 5 9 L=2.1 W=0.006 T=0.0015 H1=3.0 H2=4.0 D=XYZ

SL 2 0 5 9 L=2.1 P=3295BA

6.6.6 Coplanar

CP N1 N2 N3 N4 Z0 L WS WR T D M P

where CP designates the line type

N1, N2, N3 and N4 are the topological nodes

Z0 is the characteristic impedance (ohms)

L is the length (inches)

WS is the width of the signal conductor (inches)

WR is the width of the return conductor (inches)

T is the thickness of the conductors (inches)

D is the distance between the signal and return conductors (inches)

M is the dielectric material type

P is the standard part number. If P is entered, only the nodes and length need be entered; if other data are entered, they are ignored.

Examples:

CP 1 8 16 21 L=3.0 WS=1.0 WR=1.0

+ T=0.001 D=0.005 M=POLY5

(Note: The continuation statement begins with a "+").

CP 1 2 3 5 L=1.8 P=K29

One can note the similarity of inputs of these six line types and the lossless line already installed in SPICE. Upon input, the syntax and data are checked for proper format and for certain selected reasonable limits. Any errors or questionable data values are denoted, and the job aborted before the analysis phase begins, to eliminate, or at least reduce, costly but meaningless computer runs.

As with the active device models, certain line parameter calculations are performed by the program (SPICE) prior to, or as part of, the transient analysis. Such values (e.g., Z₀ calculated from the geometrical description using W, H, T, etc.) can be flagged in the output listing so that the user can visually check the data. This could be done in the "DC only" mode prior to requesting a complete transient analysis. For manually-generated input, the user (depending on the application) will also need to indicate the directional orientation of each transmission line segment, the method by which line segments on different layers are interconnected, and which line segments are electromagnetically coupled to a given line segment. For the case where the LCT module has generated the SPICE input from the layout data for the interconnect lines, the orientation and interlayer connection methods are performed automatically. Additionally, the LCT module can indicate those line segments that are to be considered as coupled during the subsequent network time-domain analysis. Default values can also be built into LCT that determine which particular line segments are considered "coupled" for crosstalk calculation purposes. This can be done by two methods:

- o Include all parallel line segments that are within a default distance of the line segment of interest.
- o Include the most adjacent line segments with respect to the line segment of interest. For example, if this default is set to 3, then only the closest 3 line segments on either side of a given line will be included in the crosstalk calculations.

These default values (distance, number of lines) can be overridden by the user via the input data. There are two basic methods for handling this feature:

- o On the SPICE OPTIONS statement, the entry CN=2 would request that the program consider only the two closest parallel line segments on either side of each line segment. Alternatively, an entry of CD=10.5 would request that only those parallel line segments that are 10.5 mils or closer (edge-to-edge) would be included in the crosstalk calculations. If both CN and CD are entered, SPICE will include only those line segments that meet both options. For example, if the second farthest segment is more than 10.5 mils from the primary line of interest, it will not be included.

- o Each transmission line type statement could include a CN and/or a CD entry. Then, only those lines that meet the appropriate option will be included in the crosstalk calculations with respect to that particular line. The CN and CD entries made on the individual transmission line statement will override both the program default values and the corresponding parameter values that may have been entered on the OPTIONS statement.

A similar approach could be used for the following items: line width, line thickness, dielectric type, etc. For the situation whereby all of the microstrip lines are of the same dimensions, or where the dielectric is of one type, there is no need to enter that information on each statement for each of the (possibly many) line segments. An option such as MSW=5.1 signifies that all microstrip lines have a width of 5.1 mils; similarly SLM=ABC signifies that the dielectric material associated with all striplines is type ABC. As always, simplification and clarity are two watchwords regarding user inputted formats.

To considerably reduce the computer time required to perform a network analysis, the user may prefer to request that crosstalk calculations not be included for any (or possibly for specified) interconnect lines. This could be requested by an NCT (no crosstalk) entry on the OPTIONS statement, or an NCT entry on any particular transmission line statement.

At the risk of further complexity for the user, one should also have the option of indicating, on any transmission line statement, if that line is to be used as a crosstalk source (CS), crosstalk load (CL) or both (CSL). Such considerations are particularly important if, in a given network, the user is only interested in the crosstalk effects on critical signal paths.

Having described (inputted) the interconnect line types, physical dimensions, and network topology, the user must also include references to vias and thru-holes in those applications and analyses where these entities will affect the electrical performance characteristics. Each type, and variations of these can be treated as elements that can be connected (included) in the network similar to other elements. For example, Figure 6.3 is a cross-sectional diagram of a typical two-layer interconnect.

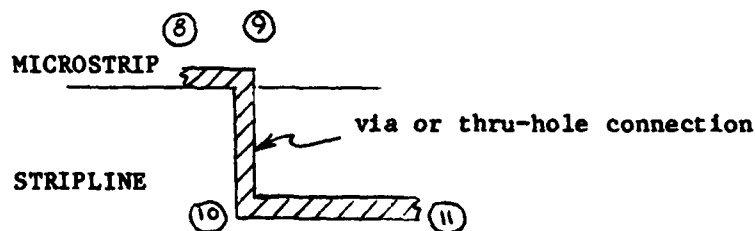


Figure 6.3 Connection Element Between Layers

The via (or thru-hole) element is connected into the circuit in a manner similar to other elements per the following examples of input statements:

MS 8 9 L=1.5 P=Z22 (microstrip)

A 9 10 L=0.7 D=1.0 (via)

SL 10 11 L=1.8 P=TYPE88 (stripline)

A "P" entry could be inputted to refer to a specific "part" number in the model library. Alternately, the user could represent the interlayer connection as an RLC network (subcircuit); this latter model would include parameter values determined by calculation, measurements or documentation.

The whole concept of discontinuities in transmission lines is concerned with changes in the line geometries (e.g., bends, junctions, etc.). For the frequencies and applications for which discontinuities will affect the analysis results, the user must have some method by which such discontinuities can be conveniently described via the input data. This really implies that one of two basic description approaches be considered:

- o Each "continuous" interconnect could be treated as a continuum, whereby each discontinuity and line segment is identified along a given input statement. Using this method, the topological node numbers, segment lengths and type of discontinuity would be entered for each identifiable segment, each segment being entered in a sequential pattern.
- o Each segment is entered as a separate transmission line entity (and corresponding user inputted statement). This approach is basically that taken above for the input formats for the six interconnect types. In that description, no mention was made of orientation of the line (bends, etc.) because each was treated as a unique and separate segment. Such segments must be topologically connected (as they are by the use of node numbers); additionally, the discontinuities must be included.

SECTION 7

SYSTEM DEVELOPMENT AND IMPLEMENTATION

Because this is a definition study, specific hardware and software programs were not addressed for each of the modules in Figure 3-1. However, certain general equipment capabilities and software characteristics are evident in order to implement the CAD/M system approach for High Speed Interconnects.

7.1 Hardware (Computer) System Considerations

The complete system should be resident on a large scale mainframe computer. However, specific software modules may be implemented on minicomputers. A 32 bit single precision word length is recommended to ensure transportability among the very common 32 bit architecture machines. The exception is that the CACA tool should be implemented as double precision.

A reasonable host computer system can be postulated: The system is comprised of the usual peripheral devices such as seven/nine track tape units, high speed mass storage devices, multiple card readers and printers, and 1.5 million words of user memory. The system supports both batch and interactive processing. It is capable of providing good interactive response for up to 75 users. Most of the circuit development is done interactively through remote CRT terminals. The terminals also contain user memory and floppy disks for offline data entry.

Recommended offline systems include multiple interactive graphics design systems, color graphics intelligent terminals and flatbed X-Y plotters. In order to support documentation, users need a word processing capability with a graphics automated documentation system that outputs to both Computer Output Microfilm (COM) and a phototypesetter. The COM unit is used for quick turn-around rough documents, including graphics, and the phototypesetter is used for very high quality graphics and documentation.

7.2 Software Considerations

The complete system is characterized by user friendliness, software transportability and software maintainability. These goals can be met through conversational user interface, Higher Order Language (HOL) implementation, top-down structured software development and complete, easy-to-use documentation.

7.2.1 User Interface

User friendliness is a primary goal of the software system. Some of the key guidelines to achieve this are:

- o The system will be capable of conversational user interaction to at least the intermediate software module level.

- o If a family of data cards is applicable, a HELP command will be provided to display a menu of appropriate cards or options and the formats required. During batch processing these solicitations will be eliminated.
- o For skilled users, truncations and combinations of commonly used commands will be allowed. The system will allow variable spelling approximations for commonly used terms.
- o The system will employ numerous integrity checks to ensure the validity of the input data, and for the interactive user, provide an opportunity to always recover from a data card error. During batch processing, the software will automatically differentiate between fatal and nonfatal errors.
- o For program control parameters, a default condition will always be present and assigned to what has been judged the most normal mode of operation. The more experienced user will have the capability to override the system defaults through English-like commands rather than numeric card options. The data cards used within the system will be free format whenever possible, and comment cards and fields will be provided as a normal course of operation.
- o The error reporting technique will accommodate both the novice and experienced user. The error printout will explicitly identify the abnormality, list the most probable cause, and recommend an error recovery technique.
- o The system will inform the user each time a major software module has been initiated. If it is anticipated that a significant amount of wall-clock time will be expended within a module, the user will be kept informed of the ongoing progress and a summary message will be provided once the module is completed.
- o The system executive control sequence to execute a run will be extremely simple. All internal working files will be assigned automatically by the program.

7.2.2 Programming Languages

Transportability is a primary requirement of the completed system. This requirement dictates use of a higher order language. ADA, a language specifically oriented to increasing transportability, would be the obvious choice if ADA compilers are available. An additional problem is that some modules already exist as functional FORTRAN programs. The solution is to allow ANSI standard FORTRAN/77 components, program new modules in PASCAL and migrate to ADA in the future.

PASCAL has several advantages for transportability. First, a standardized version of PASCAL is being developed by the ANSI X3J9 committee which is close to completion. Second, implementation of the software in ADA is highly desirable, and PASCAL is the current HOL closest to ADA. Hence, the effort to convert software to ADA will be far less for PASCAL software than for any other HOL. Finally, PASCAL compilers currently exist for most commercially available computers, including DEC VAX, PDP-11, IBM 370, UNIVAC 1100 series and CDC Cyber services.

The experience of Sperry Univac Defense System Division with acquiring and converting FORTRAN programs such as SPICE for circuit analysis, and MP2D (Multiport 2-Dimensional) for placement, routing and artwork, has successfully demonstrated transportability. It is expected that conversion of FORTRAN-based software can be accomplished by those who receive the source code.

7.2.3 Software Development Practices

Software maintainability is a primary goal of the system. Top-down structured development is an industry recognized approach to accomplish this objective. A functionally organized, modularized design will also simplify portability of new software modules.

Some recommended development practices are:

- o The use of top-down structured design with single function elementary modules.
- o Avoid, even at the loss of some efficiency, the use of non-standard language extensions offered by compiler vendors.
- o Physically isolate and clearly indicate areas of potential machine dependency. Avoid the use of internal machine values and representations.
- o Parametrize program constants, constraints and necessary architectural dependencies.
- o Compile all programs on machines of at least two vendors to help ensure transportability.

7.2.4 Software Documentation

The usability of the complete system will be enhanced through complete, well organized, easily read documentation. The documentation supplied should be in accordance with military standard practices.

Items include a Program Specification (Design Specification), Test Plan, User's Manual and Program Maintenance Manual for each software component. In addition, the code should be annotated at the detailed design level. The use of the HOL structured and procedural languages will complement documentation.

Section 8

CONCLUSIONS AND RECOMMENDATIONS

This section will summarize the findings of this HSI study. It will reiterate the goals and objectives of the study and present the major findings. The extent to which the goals and objectives were met will be stated.

This section will also provide recommendations based upon the findings of the HSI study. These recommendations will include software approaches to HSI.

Finally, an implementation plan will be set forth that will attack the problem of converting the results of this study into a useable software system for design of high-speed interconnect packages.

The goal of this study was to assess the techniques for design, analysis and fabrication of interconnections between high-speed logic IC chips with clock frequencies in the 200 MHz to 5GHz range. The study included:

- o Survey of techniques for design, analysis and fabrication of interconnect structures
- o Survey and define interchip models
- o Survey computer programs that characterize high-speed devices
- o Indicate an algorithm for integrating device models and interconnection models
- o Develop a set of quantitative design rules
- o Define algorithms and software modules which need to be developed to implement a system for automated design, analysis and fabrication
- o Define a CAD/M approach, including software transportability
- o Generate a final report

8.1 Conclusions

The major findings include the following items:

- o A wider variety of interconnect structures exist; only six of these were directly addressed in this study, with emphasis on microstrip, stripline, and coplanar.
- o A vast amount of information exists regarding transmission line theory and interconnection fabrication techniques. Unfortunately, relatively few readily available software programs/subroutines exist for transmission line models that are available for the purposes of this study.

- o Of the many readily available CACA tools that accommodate high-speed devices, only a limited few include transmission line models. Of these, the SPICE program was selected as the recommended CACA tool to serve as the "heart" of the proposed CAD/M system.
- o The primary algorithm selected to perform the time domain analysis is that by James Allen (2, 3). This algorithm must ultimately be implemented in SPICE.
- o A set of 27 quantitative design rules were specified that pertain to PCB, thick film, and thin film packaging.
- o Several software modules were specified for inclusion in the defined CAD/M system. These modules are very interdependent.
- o A CAD/M approach was defined which included specifics regarding hardware implementation considerations, recommended software languages, and software transportability.

The overall goals and objectives of the study were met. It would have been desirable to have readily available software for each of the CAD/M system modules, whereby additional material would have addressed the interfacing and installation requirements for each of those modules.

8.2 Recommendations

This study recommends that comprehensive parallel software development and hardware development efforts be undertaken for the development of the CAD/M system for HSI. The main reason for such an approach is for thorough opportunities for simultaneous design and verification (e.g., time-domain algorithm, device modeling, interconnect modeling, design rule checking, etc.). Only in this way can complete performance-to-simulation correlation testing be accomplished.

This study further recommends that a broad spectrum of personnel qualifications and backgrounds be utilized in a CAD/M system development effort for HSI, including:

- o Electromagnetics
- o Numerical analysis
- o Device physics/modeling
- o Computer science
- o Electrical engineering
- o Mechanical engineering
- o Production engineering
- o Support personnel (technicians, etc.)
- o Laboratory facilities (devices, circuits, packaging)

Finally, a key to any such CAD/M system development is that the latest available hardware (graphics, etc.), software tools, and solution techniques be monitored, and if possible, utilized in the system.

Section 9

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APPENDIX A

SURVEY LETTER AND QUESTIONNAIRE

The mailed survey questionnaires that were returned in generally sketchy, not very thorough responses. Pertinent important work is being done by many organizations, but the results are considered proprietary. Hence, the most effective information-gathering activity was literature searching, followed-up with telephone calls to pertinent authors. Of the three survey tasks, perhaps Task III was the most straightforward, in that programs either exist or they do not, and they accommodate certain configurations (transmission lines and/or high speed devices) or they do not. Several organizations have an in-house capability in this respect, but unfortunately consider such software as proprietary.

The prime consideration of the cover letter was that a description of the project background, rationale and objectives in the letter would do much to encourage questionnaire recipients to respond, thus affording a better opportunity to obtain information relevant to the project. Introductory telephone contacts were made prior to mailing the letter and questionnaire.

Generally, the people contacted were very open and encouraging, realizing that a technical survey is, at best, a difficult undertaking. The respondents offered many comments regarding their work, ideas and suggestions, and indicated a willingness to receive and complete the questionnaire.

The following pages contain the letter that was sent to each of the questionnaire recipients. The questionnaire follows the letter.

Although some recipients were not involved in projects relating to each of these three tasks, the entire packet was mailed to them for two reasons:

- o Completeness. The questions asked in each task may have helped indicate in detail the objectives of other tasks, and to help justify other tasks and questions.
- o The questionnaires could be forwarded to associates who are involved in other task-related activities, or who know of others to recommend as potential contacts regarding the survey.

Each of the questionnaire recipients was first contacted by telephone to indicate an overview of this study contract, to determine the applicability of their activities to the survey, and to determine other potential contacts, appropriate references, and suggestions. To these ends, the telephone contacts were very informative and beneficial. Many individuals were contacted to whom survey packets were not sent because their activities were not directly related to the objectives of the survey tasks, but who were helpful by sending printed material, in recommending other individuals to contact, or in specifying appropriate literature.

A.1 Letter

Introduction

As part of government contract F33615-80-C-1175 entitled "CAD for High Speed Interconnect", Sperry Univac - Defense Systems Division is conducting surveys within the industrial and academic communities to solicit information relative to the contract study effort tasks and objectives. Extensive literature searches are also being conducted as part of the survey tasks. This contract is sponsored by the Air Force Avionics Laboratory at Wright-Patterson AFB, Ohio.

Background

The following six paragraphs are from the Statement of Work written by the Air Force.

As digital Integrated Circuit (IC) technology advances toward higher levels of integration and subnanosecond gate propagation delays, complex circuits with clocking rates approaching the gigahertz range are becoming feasible. The electrical performance of these high speed complex circuits becomes very dependent on the physical design of the interchip interconnect and packaging structures. For example, if the signal risetime or faltime is less than 2 times the signal propagation time between IC chips, controlled impedance lines with proper terminations must be used to minimize the effects of reflected wavefronts. Also, timing problems become pronounced; and, cross talk and other noise related phenomena become increasingly more difficult to suppress.

The objective of this program is to develop techniques for efficiently designing, analyzing and fabricating interconnect structures between high speed logic ICs clocked in the 200 MHz to 5 GHz range. Interconnect structure models will be developed and integrated with existing device models. Interconnect structure design rules will be developed in terms of parameters that can be implemented into computer aids for designing, analyzing and fabricating circuits. Algorithms and software developments required to implement the design rules will be defined for future development. For the purpose of these surveys, consider the clocking frequency range of interest to be 10 MHz to 5 GHz.

Major emphasis will be on Printed Wiring Board (PWB) or hybrid level designs as opposed to chip level designs and it will therefore be assumed that the chip designs are fixed. Concepts developed should be flexible enough to accommodate various packaging schemes; however, it is assumed that controlled impedance lines (50-200 Ω) can be used between chip packages or bare chips, where needed. Since this program is not directed at any specific system, design rules that are developed must be somewhat generic in nature. It may be possible to categorize design rules in terms of architectural classes such as synchronous, asynchronous, or pipeline type structures or in terms of device technologies.

This program is a definition study that should lead to a well defined approach for development of generally applicable Computer Aided Design/Manufacturing (CAD/M) tools. These tools can use the defined interchip connection and device models and the quantitative design rules. Then the algorithm definition and the modification or creation of software models can complete the design and analysis loop. The contractor is not expected to develop extensive software during this program, but is expected to survey the software market for programs that may be applicable to this application. Also, the software that he defines or recommends must be transportable to other potential users and thus cannot be proprietary.

Numerous computer aids have been developed for use in designing, fabricating, and analyzing slow and modest speed logic families. These programs have adapted with limited success to high speed logic by implementing design rules that limit such parameters as the maximum line length, the maximum unterminated line length, maximum coupling distance, etc. Distributed element programs are typically used to solve microwave design and analysis problems. These programs are specifically designed for fixed frequency with limited bandwidth excursions. A number of lumped element AC analysis programs are also available and used extensively for characterizing devices. None of these programs will adequately handle the problem of designing and analyzing high speed logic circuits where the pulse risetime is short relative to the propagation delay between chips. A distributed element time domain analysis approach will likely be required.

Program Tasks

The seven tasks of this program are:

- o Task I - Survey Interconnect Structures
- o Task II - Survey Interconnect Models
- o Task III - Survey Available CAD/M Programs
- o Task IV - Integrate Device and Interchip Models
- o Task V - Define Algorithms and Software Modules
- o Task VI - Document CAD/M Approach
- o Task VII - Final Report

Surveys

Sperry Univac herein requests that you respond to the attached questionnaires that pertain to the survey tasks outlined above. Please respond to Sperry Univac in writing and/or by telephone. For those portions of the responses that you hesitate to forward to Sperry Univac, please forward directly to the Air Force contract officer:

DEPARTMENT OF THE AIR FORCE
Air Force Systems Command
Aeronautical Systems Division
Attn: Lt. Tebo/AFWAL/AADE-3
Wright-Patterson AFB, Ohio 45433

Please reference this survey by the contract number stated above. Only the technical portions of such responses will subsequently be made available to Sperry Univac for the purpose of this study. Upon completion of this study, the results will be made available to requesting respondents.

With any responses, please include any additional appropriate information regarding the surveys, such as:

- o Related papers that you have published or are aware of, including title, author and publication.
- o Other personnel that should be contacted, either within your organization or elsewhere, that can contribute to this survey.
- o General or detailed comments, suggestions, recommendations, etc., that are appropriate extensions of the questionnaire proper.

Sperry Univac is grateful for your attention, cooperation and promptness in this survey activity. Please contact the undersigned if you have any questions or comments. I look forward to receiving your replies in the near future. Please use the enclosed, self-addressed, stamped envelope.

Sincerely,

Norbert F. Santoski
Principal Investigator
Design Automation, ATE and Microprogramming Dept.
Mail Station U2U25
Telephone: (612) 456-2382, 2310

cc: Lt. Tebo, USAF

Attachments: Task I Questionnaire
Task II Questionnaire
Task III Questionnaire

Enclosure: Self-addressed envelope

A.2 Questionnaires

TASK I

Name of Organization:

Address:

Name of Respondent:

Date:

Title:

Phone:

Responsibility:

As part of a government contract, Sperry Univac is conducting a survey to assess capabilities and techniques currently used for design, analysis and fabrication of interconnect structures for high speed logic with clock rates exceeding 10 MHz. This study contract is oriented towards CAD/M approaches. Please provide appropriate detailed information for the items below, using additional necessary sheets that refer to question numbers.

1. What fabrication techniques are being utilized (stripline, microstrip, coplanar, and variations of these)? What are the corresponding line impedances and tolerances?
2. What physical dimensions and materials are used? Consider dielectrics, interconnects, and spacings.
3. With what approaches are these being utilized (PC board, thick film, thin film)?
4. What is the upper clocking frequency limit that still results in satisfactory signal integrity? For what pulse rise and fall times? What are the limiting factors?
5. Please comment on what must be considered and done to extend the frequency range above 10 MHz? Consider 5 GHz as the highest clock frequency of interest.
6. To what degree is automation used in your design, analysis and fabrication disciplines? Example: automation to control the interconnect linen impedance.
7. What are some specific areas in which automation is desirable, but not used? What are the reasons for not automating?
8. What are some of the requirements concerning rework? What types of rework are possible, and are done? When is rework justified? What steps are taken to ensure the rework is satisfactory? What steps should be taken in the design-to-fabrication cycle to minimize the need for rework?
9. What tests are done to check actual vs. predicted performance? What is the correlation? What is the most difficult aspect of such checks (e.g., equipment, test techniques, electrical and/or mechanical constraints).

TASK I (CONTINUED)

10. What analysis and test techniques are used during the design and prototyping operations?
11. What design rules are used during the design, analysis and fabrication processes that apply specifically to the high-speed interconnections?
Examples: maximum line lengths and stub lengths in the placement/routing process; maximum number of fan-outs per driver; maximum number of vias and crossovers per interconnect network; layout (artwork) constraints to control line impedances, etc. Please elaborate on how your design rules are justified.
12. In an attempt to keep this questionnaire as brief as possible, perhaps some relevant items were not addressed. Please include any additional comments, background information, etc., that pertains to this Task I survey that you feel are important and appropriate. Special attention should be focused on the CAD/M disciplines.

TASK II

Name of Organization:

Address:

Name of Respondent:

Title:

Responsibility:

Date:

Phone:

As part of a government contract, Sperry Univac is conducting a survey to obtain information regarding computer models of transmission lines. For pulses with risetimes and falltimes in the 100 to 500 picosecond range, indicate appropriate detailed responses to the items below. This study contract is oriented towards CAD/M approaches. Please provide appropriate detailed information for the items below, using additional necessary sheets that refer to question numbers.

1. For what interconnection geometries do you have models (e.g., microstrip, stripline, coplanar, and variations of these)?
2. What physical dimensions and materials are used? Consider dielectrics, interconnects, and spacings.
3. Is distributed element loading accounted for (e.g., gates connected at specific locations along interconnect)? How? How accurate is this technique?
4. Are distributed effects accounted for? Examples include propagation delay, line loss, dispersion, crosstalk coupling, etc.
5. Are other effects accounted for, such as vias, connectors, coupling type mismatches (including test point couplers) that cause reflected power problems, etc?
6. To what extent are these interconnection models computerized?
7. Are the programs or subroutines available for the objectives of this project? Under what conditions can they be made available?
8. What are some specific items regarding such software (e.g., language, amount and contents of documentation, computer(s) installed on, number of program statements, number of subroutines, computer memory required, etc)?
9. What features of this software can be noted (e.g., conversational, permits user-defined expressions, built-in default values, plotted output, etc.)?
10. What interconnection model verification techniques were/are used? Examples include test equipment such as time domain reflectometry, FFT spectrum analysis, etc.).
11. How successful are such verifications? Do the stimulations accurately predict the actual results?

TASK II (CONTINUED)

12. Do you analyze in the frequency domain, then transform results to the time domain? What is done in f ? in t ?
13. In an attempt to keep this questionnaire as brief as possible, perhaps some relevant items were not addressed. Please include any additional comments, background information, etc., that pertains to this Task II survey that you feel are important and appropriate. Special attention should be focused on the CAD/M disciplines.

TASK III

Name of Organization:

Address:

Name of Respondent:

Date:

Title:

Phone:

Responsibility:

As part of a government contract, Sperry Univac is conducting a survey to obtain information regarding available computer analysis programs. This study contract is oriented towards CAD/M approaches. Please provide appropriate detailed information for the items below, using additional necessary sheets that refer to question numbers.

1. What computer programs do you have/use that characterize high speed logic devices (diodes, transistors) in the time domain? In the frequency domain? What analyses modes are allowed in each domain (e.g., statistical analysis, sensitivity, worst case,, etc.)?
2. What types of devices are modeled with each program (silicon, gallium arsenide, etc.)?
3. Assess the accuracy of the models and the program (e.g., the correlation of simulation results with the "real world").
4. For what frequency ranges are these models accurate? Base your responses on tested ranges.
5. Provide a sketch of each model, and list the parameters that can be assigned numerical values, either by the user or by a default mode. If possible, include appropriate equations used in the models.
6. List appropriate references that pertain to the programs; to the models. This includes user manuals, technical papers, etc.
7. Which programs contain transmission line models? What special efforts do these models include (e.g., dispersion,, distributed loading, design rules, etc.)?
8. List the salient features of the software (e.g., conversational, allow user-inputted equations, etc.).
9. What are some specific items regarding such software (e.g., language, amount and contents of documentation, computer(s) installed on, number of program statements, number of subroutines, computer memory required, etc.)?
10. Are the programs or subroutines available for the objectives of this project? Under what conditions can they be made available?

Task III (CONTINUED)

11. What verification techniques are used to access the model/program accuracy?
12. Do you perform analysis in the frequency domain, then transfer results to the time domain? If so, how successful is this technique? Assess this approach for the speed/accuracy needs of this project.
13. In an attempt to keep this questionnaire as brief as possible, perhaps some relevant items were not addressed. Please include any additional comments, background information, etc., that pertains to this Task II survey that you feel are important and appropriate. Special attention should be focused on the CAD/M disciplines.

APPENDIX B

SURVEY CONTACTS

The survey questionnaire packet was sent to the following organization during the months of September and October 1980. The following legend applies to the status of those surveys:

- R - Returned with response information furnished
- D - Declined to respond
- M - Furnished pertinent articles and/or manuals

<u>Organization</u>	<u>Status</u>
BDM Corporation McLean, Virginia	D
Compact Engineering, Inc. Palo Alto, California	M
Department of Electrical Engineering University of Minnesota Minneapolis, Minnesota	R,M
Department of Electrical Engineering University of South Florida Tampa, Florida (sent survey to two individuals)	R,M
Hewlett-Packard/Data Process Cupertino, California	D
Hewlett-Packard Laboratories Palo Alto, California	D
Hughes Aircraft Company Los Angeles, California	R
Hughes Research Laboratories Malibu, California	R
IBM Hopewell Junction, New York	D,M
IBM Watson Research Center Yorktown Heights, New York	D
MacDonnel-Douglas Astronautics Huntington Beach, California	R

MADE-IT Associates Burlington, Massachusetts	M
Mayo Clinic Rochester, Minnesota	D
Microwave Associates, Inc. Burlington, Massachusetts	D
Raytheon-Missile System Division Bedford, Massachusetts	D
RCA Laboratories Princeton, New Jersey	D
Rockwell International Electronics Research Center Thousand Oaks, California	D
Sperry Gyroscope Great Neck, New York	D
Sperry Microwave Electronics Clearwater, Florida	D
Sperry Research Center Sudbury, Massachusetts	R
Sperry Univac Blue Bell, Pennsylvania	D
SRI Menlo Park, California	M
TRW Defense and Space Systems Redondo Beach, California (sent to two individuals)	R,D
University of Texas Austin, Texas	R

APPENDIX C

LIST OF ACRONYMS

CACA - COMPUTER-AIDED CIRCUIT ANALYSIS

CAD - COMPUTER-AIDED DESIGN

CAD/M - COMPUTER-AIDED DESIGN/MANUFACTURING

CAM - COMPUTER-AIDED MANUFACTURING

DIP - DUAL IN-LINE PACKAGE

DRC - DESIGN RULE CHECKER

DRS - DESIGN RULES AND SPECIFICATIONS

FP - FLAT PACK

HSI - HIGH-SPEED INTERCONNECT

LCT - LAYOUT-TO-CACA TRANSISTOR

PCB - PRINTED CIRCUIT BOARD

TEM - TRANSVERSE ELECTROMAGNETIC

TLC - TRANSMISSION LINE CALCULATIONS

**DAT
FILM**