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ELECTRICAL CHARACTERIZATION OF THE 68000 MICROPROCESSOR.(U)

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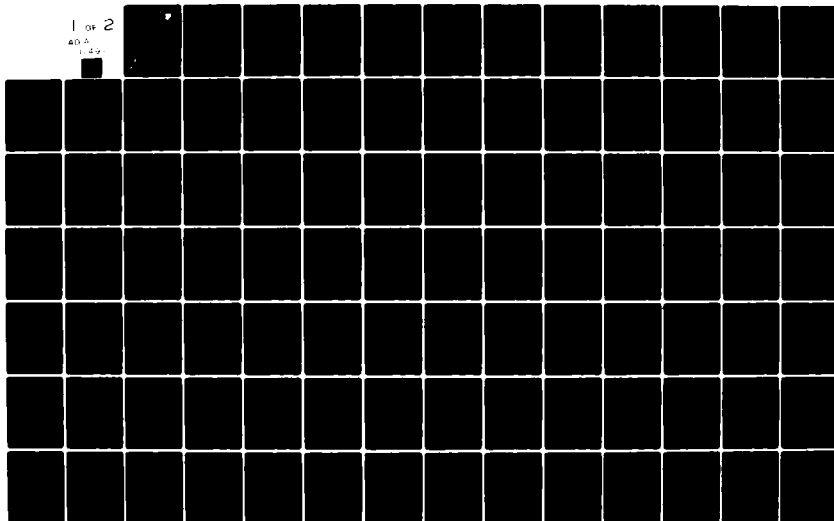
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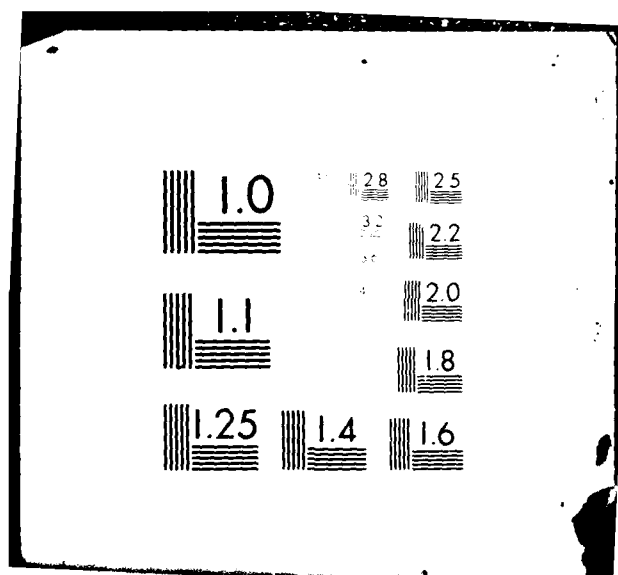
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Final Technical Report
December 1981



ELECTRICAL CHARACTERIZATION OF THE 68000 MICROPROCESSOR

IBM Corporation

Jim D. Bailey

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ELECTRICAL CHARACTERIZATION OF THE 68000 MICROPROCESSOR

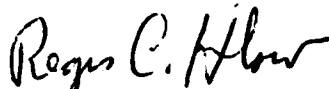
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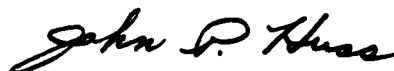
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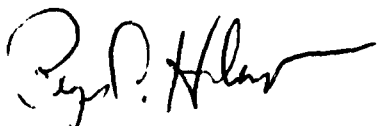
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EVALUATION

The objective of this effort was to electrically characterize the 68000, 16 bit microprocessor. From the resulting data, a MIL-M-38510 detail specification was to be prepared in a format compatible with DOD coordination standards.

The electrical characterization of the 68000 was successfully accomplished through a very complex and time consuming task. Over the course of this program, this state-of-the-art microprocessor was updated several times by the vendor to enhance performance and/or to improve yields. Each change required a thorough evaluation and comparison of the design or process enhancements versus potential reliability degradation. IBM produced a military detail specification M38510/540 to cover the latest update of the 68000. This specification defines three versions of the 68000 categorized by frequency and enclosed in three package types including two state-of-the-art leadless chip carrier packages.

This program demonstrates what can be accomplished when there exists a good working relationship between the user and the manufacturer of the part. IBM took a basic commercial part and provided the manufacturer the data he needed to militarize it. Motorola on the other hand cooperated in providing information, some proprietary, on key architectural and circuit designs, in addition to information on processing enhancements.


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Project Engineer



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1.0 INTRODUCTION

The MC68000 is one of the most technologically advanced and architecturally superior microprocessors available today. It follows that an acceptable electrical evaluation of this device would be a complex and time consuming task. This document will discuss in detail the MC68000 Electrical Characterization program and the results that were obtained as various mask sets and device lots were tested across an extended temperature range. For additional information on device description and system integration the reader should reference the Motorola Users Guide MC68000UM (AD2).

At the outset it must be noted that no MIL-883B type part was available for this test exercise from Motorola. Due to the recent announcement and frequent performance enhancements, a military device is now feasible. This program supports the accelerated development of that military product. Early functional failures at the MIL- temperature extremes are noted in this report and are to be expected since these devices were not screened to those corners. As the report tracks the maturity of the masks and process, the functionality at the temperature extremes improved greatly, yielding over 80% fully functional devices (of the test samples) to the military specification generated.

2.0 DEVICE DESCRIPTION

2.1 TECHNOLOGY

The MC68000 is a single chip 16-bit microprocessor fabricated using an N-channel, depletion load, silicon gate technology. The die, measuring approximately $40 \mu\text{m}^2$ contains approximately 70,000 transistors. This level of density was achieved with the use of $3 \mu\text{m}$ ground rules (HMOS I).

Further enhancements (HMOS II) and shrinkage is expected in 1982.

2.2 BLOCK DIAGRAM

A block diagram of the MC68000 is shown in Figure 1.0. The processor is composed of seventeen 16-bit registers, a program counter, status register, 16-bit ALU and control section. The flexible instruction set consisting of 56 instructions and 14 different addressing modes is implemented using an on-board microcode ROM. In addition the processor control section will support direct memory access, seven levels of processor peripheral interrupt and 6800 peripheral interface control. The 23 address lines that are supported by the processor allow direct access to over 16 M bytes of memory.

2.3 PIN DESCRIPTION

The MC68000 signal and pin assignment diagram is shown in Figure 2.0.

2.3.1 Address Bus

The address bus is composed of 23 tri-state bus outputs which provide addressing for all bus cycles except DMA operations and interrupts. The 23-bit address range of the processor allows addressing of over 8 MWords (16-MBytes) of memory.

2.3.2 Data Bus

The data bus is a 16-bit, bi-directional, tri-state path for data flowing to and from the processor. Data can be in byte or word length.

2.3.3 Address Strobe (AS)

The address strobe is an active low unidirectional tri-state signal. When AS is low it indicates that the address present on the address pins of the processor is valid.

2.3.4 READ/WRITE (R/W)

The READ/WRITE pin is a unidirectional tri-state signal that defines the processor operation and data bus direction. The signal is low (logic 0) during processor write operations and is high (logic 1) for all subsequent processor operations.

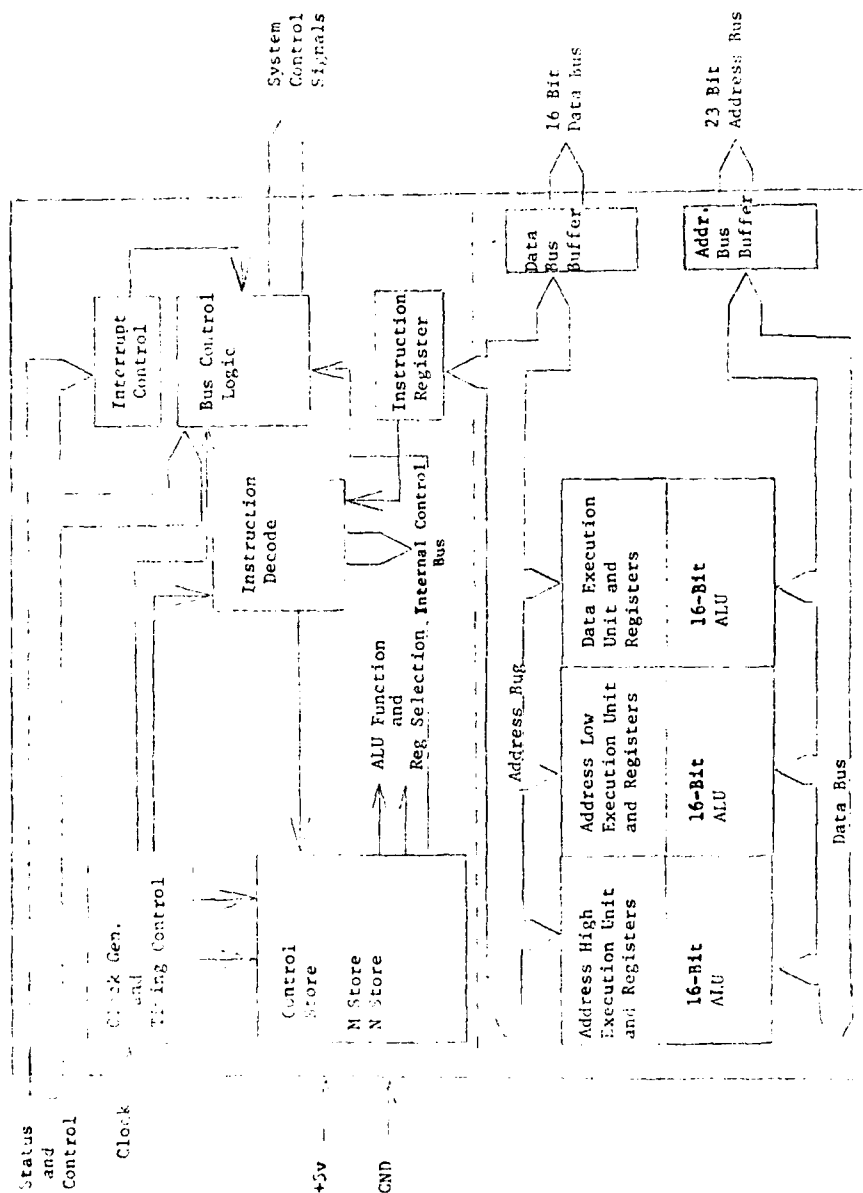


Figure 1.0 MC68000 Block Diagram

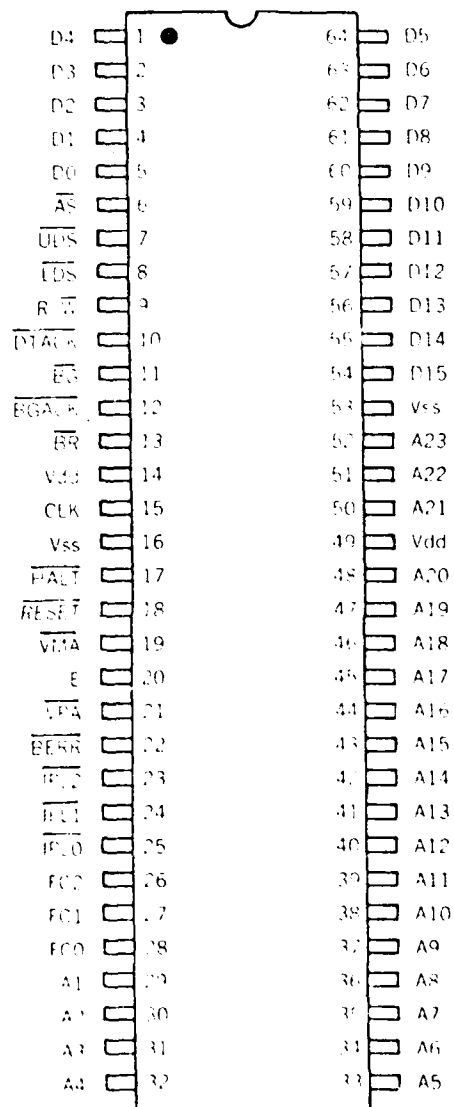


Figure 2.0 Terminal Connection and Pin Assignment

2.3.5 Upper and Lower Data Strobes (UDS-LDS)

The UDS and LDS are active low unidirectional control signals that indicate which half (upper 8 bits -UDS, lower 8 bit -LDS) are valid on the data bus during processor write operations. The UDS and LDS will always be active during processor read operations.

2.3.6 Data Transfer Acknowledge (DTACK)

The DTACK input is an active low asynchronous control line used to signal the CPU that a particular bus operation has been completed. The DTACK input is recognized by the processor on the falling edge of the input clock during CPU READ/WRITE operations. In early mask set devices (R9M, T6E) if DTACK was active by the fall of the input clock during bus cycle two (for READ/WRITE) the particular operation would be shortened by one CLK cycle. In later mask set devices (CC1) if DTACK is active at the fall of the input clock during bus cycle two it will have no effect on the overall bus operation.

2.3.7 Bus Request (BR)

This active low unidirectional input is used to signal the CPU that some other device wishes to take control of the system bus.

2.3.8 Bus Grant (BG)

The active low unidirectional output is used to signal other potential bus masters that the CPU will release the bus following completion of the current bus operation.

2.3.9 Bus Grant Acknowledge (BGACK)

This active low unidirectional input is used to signal the CPU that another device has control of the system bus.

2.3.10 Interrupt Control (IPL0, IPL1, IPL2)

These three active low unidirectional inputs are used by other devices that request a CPU interrupt. The three inputs allow seven levels of prioritized interrupts with level zero being the lowest priority.

2.3.11 Bus Error (BERR)

This active low unidirectional input is used to signal the CPU when a problem has occurred during a bus operations. It is used in conjunction with HALT to determine if the operation should be retried or the processor should initiate exception processing.

2.3.12 Reset

This bi-directional active low signal is used in conjunction with the HALT line to reset the CPU (system initialization sequence). In addition it is used to reset peripheral devices (see reset instruction).

2.3.13 HALT

The active low bi-directional signal is used to halt the processor at the end of a current bus cycle or to indicate the processor has halted due to a system failure.

2.3.14 Enable (E)

The unidirectional tri-state output is used to synchronously interface M6800 peripheral devices with the MC68000. The E output is a divide by ten of the input clock. The state of E output cannot be determined following a power on reset sequence.

2.3.15 Valid Peripheral Address (VPA)

This active low unidirection input indicates that the device being addressed and the subsequent data transfer should be synchronized to the MC68000 by the use of the E signal. If active low during an interrupt this signal indicates to the processor that auto vectoring should be used.

2.3.16 Valid Memory Address (VMA)

This active low unidirectional output indicates that the address on the bus is valid and that the device being addressed (M6800) is in sync with the processor.

2.3.17 Processor Status (FC0, FC1, FC2)

These three unidirectional tri-state output signals indicate the state of the present processor operation (user or supervisor) and the type cycle being executed.

2.3.18 CLOCK (CLK)

This unidirection input is the primary processor clock. The clock input waveform should be a signal having a 50% duty cycle and vary in frequency from 3 MHZ to 10 MHZ.

2.3.19 Signal Summary

All MC68000 signals are TTL compatible signals. The signal descriptions given in this section have been abbreviated and serve to familiarize the reader with the device and to point out some areas of interest that were discovered during characterization and are not mentioned in the vendors users guide. A more detailed description of the device pins and their function can be found in the Motorola Users Guide MC68000UM (AD2).

3.0 ELECTRICAL CHARACTERIZATION PROGRAM DEVELOPMENT

3.1 TEST EQUIPMENT

Due to the complexity of the MC68000 and the asynchronous bus structure of the device, an extensive amount of hardware was necessary in order to develop the function test vectors that would be used during the device characterization. The hardware included:

- o In-house 16-bit Proto-typing System
- o MDS-800 Development System
- o HP 1615A Logic Analyzer
- o IBM System S/370 (Editor)
- o Macrodata MD-501 LSI Tester

The procedure for developing the software was to load a MC68000 test program into the proto-type system using the MDS-800 Development System. The program was then executed and the device outputs monitored using the H.P. 1615A Logic Analyzer. After determining the sequence in which the processor executed the program, the assembly code necessary to generate the Binary tester pattern for each clock cycle of execution was entered and properly coded with the aid of an IBM S/370 editor. The software was then downlinked to magtape and transferred to the Macrodata MD-501 LSI tester for final compilation and assembly into a Binary format. All device testing (functional, AC and DC) was performed using the MD-501. The Macrodata MD-501 is a 10 MHZ, 64 channel LSI tester. All 64 channels can be configured as either input, output or as a power supply. All power supplies are accurate to within 0.1% of their programmed value. All AC measurements are accurate to within ± 1 ns.

3.2 Functional Testing

3.2.1 Logic Block Element Testing

Functional test software development was broken into two categories. The first category was Logic Block Element Testing (LBET). The objective was to stimulate the various logic sections of the device using a minimum number of instructions to insure that each of the relatively large functional blocks were operational, prior to instituting the very long and detailed instruction decode verification testing. The categories to be tested were:

- o Reset
- o Register, Array
- o PC Test
- o ALU
- o Stack Test
- o Interrupts

The reset test verifies the power-on reset sequence and the reset and halt instructions are operational.

The register array test ensures the integrity of each of the data and address registers. Pattern sensitive data is loaded into each register and checked for proper loading. In addition all other registers are tested for any possible adjacent register disturbance.

The objective of the ALU test is to insure functionality of the ALU. This is accomplished by executing all arithmetic and logical operations and testing the resulting output.

The PC and stack test verify operation of the program counter and supervisor stack pointer, by incrementing and where feasible decrementing each counter through overflow or underflow.

The interrupt test verifies the processor will respond to all levels of interrupt and that the proper interrupt vector location is executed for each level of interrupt.

3.2.2 Instruction Decode

The level of complexity of the MC68000 (56 instructions and 14 different addressing modes) makes testing of all instructions a very lengthy process. The approach to instruction testing was to break the instruction set into six categories. These categories were:

- o Data movement
- o Arithmetic operations
- o Shift, rotates and logicals
- o BCD operations
- o Bit Test Operations
- o Program/System Control

A detailed description of each program and the opcodes tested are given in Appendix A. When the functional test programs are converted to the conventional (Binary) format the result was over 13,000 lines of executable code. Due to the length of the Binary patterns they are not included within this document. However, they can be obtained from Rome Air Development Center (RADC) Reliability Branch. These patterns represent the forced and expected data by clock cycle for the automatic test equipment stimulation (MD-501) of the MC68000 device.

3.3 A.C. PERFORMANCE TEST DEVELOPMENT

The primary objective of the AC Test Development was to measure all of the most critical delays that are associated with the MC68000. The functional test patterns were used to precondition the device to a known state prior to performing the required measurement. The baseline used to determine which delays would be measured was the vendors data sheet. The delays shown in Table 1.0 are the actual delays that are measured using the MD-501. All measured times are accurate within ± 1 ns. Due to the enable output (E) being in an undetermined state after power-on reset it was necessary to obtain the

As a first step, we have to find the C_{max} and C_{min} of the drug.

TEST	SIGNAL	TYPE	NO.	SETUP	HOLD	STATUS	REMARKS
CLK TO CLK LOW (TCLL)	TCLL	1	47	NS			SEE P. 60 FOR VTS
MIN TO CLK LOW (TCLML)	TCLML	1	47	NS			TRNG 1 - 10% MIN
DATA TO CLK LOW (TCLDLO)	TCLDLO	1	47	NS			LOWE ORG. I.C.
EN TO CLK LOW (TCLNEL)	TCLNEL	1	47	NS			EXP. ALL TESTS
HR TO CLK LOW (TCHRL)	TCHRL	1	47	NS			
NRACK TO CLK LOW (TCLRACK)	TCLRACK	1	47	NS			
VRACK TO CLK LOW (TCLVRACK)	TCLVRACK	1	47	NS			
VPA TO CLK LOW (TCLVPA)	TCLVPA	1	47	NS			
VRA TO CLK LOW (TCLVRA)	TCLVRA	1	47	NS			
SRM TO CLK LOW (TCLSRM)	TCLSRM	1	47	NS			
SRN TO CLK LOW (TCLSRN)	TCLSRN	1	47	NS			
CLK WIDTH LOW	TCLL	1	2	NS			
CLK WIDTH HIGH	TCLH	1	3	NS			
CLK HIGH TO $\overline{A}$ VALID	TCLAV	1	6	NS			
CLK HIGH TO $\overline{AS}$ LOW	TCLSEL	1	9	NS			
CLK HIGH TO $\overline{AS}$ LOW	TCLSEN	1	10	NS	L		
CLK HIGH TO $\overline{DS}$ LOW	TCLSEN	1	9	NS			
CLK HIGH TO $\overline{DS}$ LOW	TCLSEN	1	10	NS	L		
CLK LOW TO $\overline{AS}$ HIGH	TCLSH	1	12	NS			
CLK LOW TO $\overline{DS}$ HIGH	TCLSH	1	12	NS			
CLK H TO R-W H	TCHRH	1	18	NS			
CLK H TO R-W H	TCHRHN	1	19	NS	L		
CLK HIGH TO R-W LOW	TCHRL	1	20	NS			
CLK L TO ADDR VALID	TCLDO	1	23	NS			
CLK L TO ADDR VALID	TCLAV	1	6	NS			
CLK HIGH TO $\overline{AG}$ LOW	TCHAL	1	33	NS			
CLK HIGH TO $\overline{AG}$ HIGH	TCHAH	1	34	NS			
CLK LOW TO VMA LOW	TCLVML	1	40	NS			
CLK LOW TO VMA HIGH	TCLVMH	1	40	NS			
CLK LOW TO E LOW	TCELL	1	41	NS			
CLK LOW TO S HIGH	TCLSH	1	41	NS			
CLK H TO ADDR VALID T.S.	TCHAZ	1	7	NS			OUTPUTS +0.5V
CLK H TO ADDR INVALID	TCHAZ	1	8	NS	L		OUTPUTS +0.5V
CLK HIGH TO A-B T.S.	TCHST	1	16	NS			OUTPUTS +0.5V
CLK HIGH TO R-W T.S.	TCHRT	1	24	NS			OUTPUTS +0.5V
CLK HIGH TO DATA T.S.	TCHAZA	1	7	NS			OUTPUTS +0.5V

Table 1.0

AC PERFORMANCE SPECIFICATION (MCMC00)

TEST	SYMBOL	FLAG NO.	REF NO.	UNIT	NOTES	CONDITIONS
ACR VALID TO ADRV E	TAVAL	1	11	NS		DERIVED DELAYS
ADR HIGH TO ADR INVALID	TAHAI	1	11	NS		
ADR WIDTH LOW	TEL	1	19	NS		
ADR WIDTH HIGH	TEH	1	19	NS		
DS HIGH TO HZ HIGH	TDHSH	1	17	NS		
ADDR VALID TO HZ LOW	TAVAL	1	21	NS		
HZ LOW TO DS LOW	TDHSL	1	22	NS		
DS HIGH TO DOUT INVALID	TDHDI	1	25	NS		
DS H TO DI INVALID INHDI	TDHDI	1	29	NS		
DS LOW TO EG LOW	TDHSL	1	25	CLKS		
HG HIGH TO HG HIGH	TDHSH	1	30	CLKS		
EG LOW TO EG HIGH	TDGLH	1	37	CLKS		
HG LOW TO BUS T+S	TDGL	1	38	CLKS		
HG WIDTH HIGH	TDH	1	39	CLKS		
VNS LOW TO L HIGH	TDVNLH	1	43	CLKS		
CLAS HIGH TO VPA HIGH	TDHVPH	1	44	NS		
E LOW TO ADDR INVALID	TELAT	1	45	NS		
CLCK WIDTH	TDGL	1	46	CLKS		
PERH LOW TO CLCK LOW	TDHCLL	1	48	NS		
N WIDTH HIGH	TEH	1	50	NS		
E WIDTH LOW	TEL	1	51	NS		

Table 2.0

TEST	SYMBOL	CONDITIONS	UNITS	TEST TEMP. CODE	COMMENTS
ICC TEST	ICC	VCC = 5.5V	MA		VCC = 5.5VOLTS
VOL A23-1,FC0-2,BU,E	VOL	IOL = 3.2MA	VOLTS		VCC = 4.5VOLTS
VOL HALT	VGL	IOL = 3.6MA	VOLTS		"
VOL AS,R/W,DIS-0 UDS,ICDS,VMA	VOL	IOL = 5.2MA	VOLTS		"
VOL RESET	VOL	IOL = 5.0MA	VOLTS		"
VOH (ALL OUTPUTS)	VOH	IOH = 400UA	VOLTS		
VIH (ALL INPUTS)	VIH	VIH = 2.4 VOLTS	UA		
VIL (ALL INPUTS)	VIL	VIL = 0.4 VOLTS	UA		
IOHZ (ALL OUTPUTS)	IOHZ	VOH = 2.4 VOLTS	UA		
IOLZ (ALL OUTPUTS)	IOLZ	VOL = 0.4 VOLTS	UA		
VIH (ALL INPUTS)	VIH	VGS TEST	VOLTS		VCC = 4.5
VIL (ALL INPUTS)	VIL		VOLTS		VCC = 4.5

Table 3.0

test mode for syncing the E output from Motorola. This information is considered proprietary and thus cannot be disclosed in this document. The delays shown in Table 2.0 are referred to as derived delays. These delays are output to output delays and are not directly measured by the MD-501 but are calculated based upon data obtained from the measured delays. Additional delays not specified by the vendor were measured and used to calculate these output to output delays.

The output loads used during AC testing were based upon the vendors recommended load circuit. The output load circuits are shown in Figure 3.0. A modification to the vendors load circuit was required to properly measure the tri-state delays. In Figure 3.0 the resistor Rx was added during tri-state measurements only. The resistor Rx when in parallel with R1 will make the pull-down resistance equal to the pull-up resistance (Rn). This will result in the outputs which are at a high level (logic 1) prior to tri-stating having the same tri-state fall transition as the rise time of the outputs which are at a low level (logic 0) prior to tri-stating. Without this loading change fall times exceed 2 to 3 clock cycles of decay (fall) time and are immeasurable by most modern ATE.

3.4 DC PARAMETRIC TEST DEVELOPMENT

The D.C. tests developed to evaluate the MC68000 are shown in Table 3.0. The baseline for test development was the vendors data sheet. Icc was measured dynamically (device running). In all tests Vcc was set to worse case. It was necessary to use the special tester configuration to sync Enable (E) and (VMA) outputs for D.C. measurements. All other test conditions were obtained from the vendors data sheet.

3.5 MAXIMUM OPERATING FREQUENCY (FMAX) TEST DEVELOPMENT

Due to the very high operating frequency (Fmax) of the MC68000 (8 MHZ - 10 MHZ) it was necessary to develop a method of determining the High Frequency limit of device operation. The exchange functional test pattern was used to implement an FMAX test. The FMAX test insures the MC68000 is operating correctly for the following frequencies:

- o 4.0 MHZ
- o 5.8 MHZ
- o 7.14 MHZ
- o 7.7 MHZ
- o 8.3 MHZ

The upper limit is the maximum that could be achieved by the 10 MHZ MD-501.

3.6 CHARACTERIZATION PROGRAM SUMMARY

The finalized characterization program used to evaluate the MC68000 consisted of all the previously described tests except the LBET which is used for preliminary verification on development products only. Each test block

was varied by frequency, and/or Vcc variations as necessary to determine the MC68000 operability limitations. The test compendium is repeated at -65°C , 25°C and $+110^{\circ}\text{C}$ case temp. A brief summary of the specified test variations follows.

All DC tests were measured at worse case supplies. All functional tests were executed at two frequencies (2.0 - 2.88 MHz) with $V_{cc} = 4.5\text{v}-5.5\text{v}$. The FMAX test was performed at $V_{cc} = 4.5\text{v}-5.5\text{v}$. All AC performance measurements were made with $V_{cc} = 5.0\text{v}$ and an operating frequency of 2 MHz. Shown in Appendix B is a sample test run of the MC68000 characterization program.

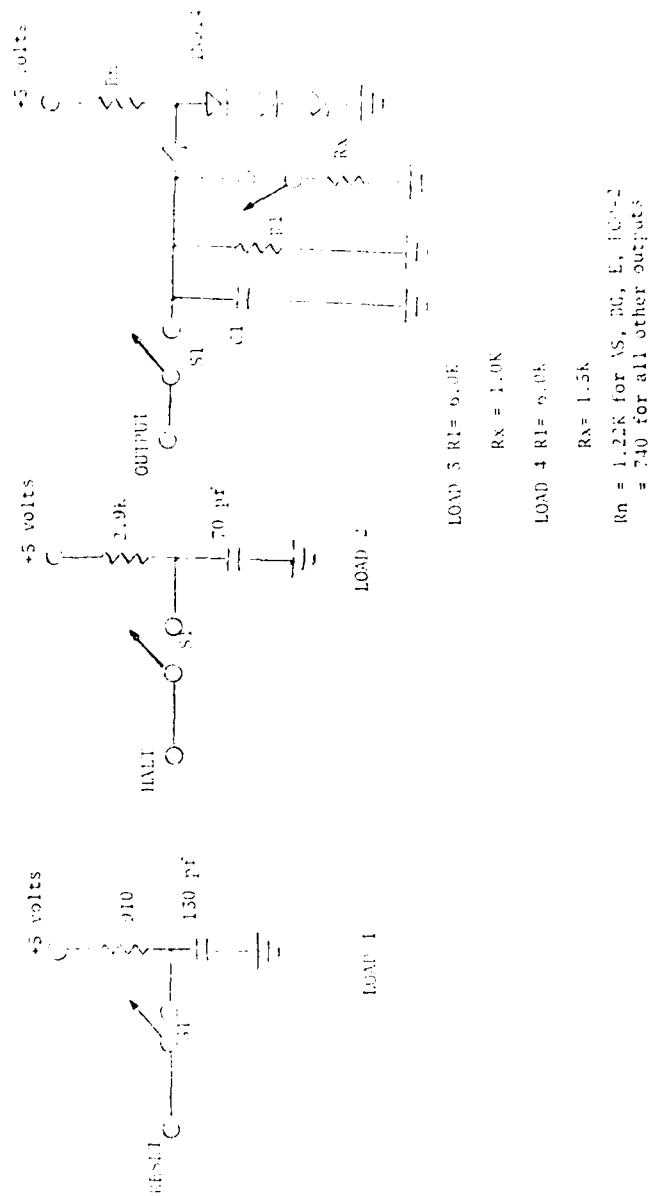


Figure 3.0 Output Load Circuit

T6E Device Functional Fail Summary

TEST	T E H P	Vcc @ 1MHz			Vcc @ 2.0MHz			Vcc @ 2.85MHz			COMMENTS
		4.5	4.75	5.0	5.25	5.5	4.5	4.75	5.0	5.25	
RESET	-55 +25 +100		X	X			X			X	Reset Instruction
MEMORY CYCLE:	-55 25 +100										
P. C. COUNTER:	-55 25 +100		X	X	X		X	X		X	P. C. Fail
STACK POINTER:	-55 25 +100		X	X	X		X	X	X	X	Stack Fail
REGISTER ARRAY:	-55 25 +100										
ALU:	-55 25 +100		X	X			X				
PROCESSOR INTERRUPT:	-55 25 +100		X	X	X		X	X		X	Stack Fail

Device #: 2
Date: 7/22/80

TABLE 4.0

TEST	TEMP	Vcc @ 1MHz			Vcc @ 2.0MHz			Vcc @ 2.85MHz			COMMENTS	
		4.5	4.75	5.0	5.25	5.5	4.5	4.75	5.0	5.25		5.5
RESET	-55											
	+25											
	+100	X	X	X	X	X	X	X	X	X	X	Reset Instruction
MEMORY CYCLE:	-55											
	25											
	100											
PROGRAM COUNTER:	-55											
	25											
	100	X	X	X	X	X	X	X	X	X	X	PC Increment
STACK POINTER:	-55											
	25											
	100	X	X	X	X	X	X	X	X	X	X	SP Addr. Plus Lbyte
REGISTER ARRAY:	-55											
	25											
	100											
ALU:	-55											
	25											
	100											
PROCESSOR INTERRUPT:	-55											
	25											
	100	X	X	X	X	X	X	X	X	X	X	XRTG = 36

Device #1
Date: 7/22/84

Table 4.1

TEST	T E M P	Vcc @ 1MHz			Vcc @ 2.0MHz			Vcc @ 2.85MHz			COMMENTS
		4.5	4.75	5.0	5.25	5.5	4.5	4.75	5.0	5.25	
RESET	-55										
	25										
	100										
MEMORY CYCLE:	-55										
	25										
	100										
PROGRAM COUNTER:	-55										
	25										
	100					X					P.C. Increment
STACK POINTER:	-55										
	25										
	100					X					SP 1 byte Write
REGISTER ARRAY:	-55										
	25										
	100										
ALU:	-55										
	25										
	100										
PROCESSOR INTERRUPT:	-55										
	25										
	100					X					SP 1 byte Write

Device #1 - 5
Date: 7/7/73

Table 4.2

TEST	T E M P	Vcc @ 1MHz			Vcc @ 2.0MHz			Vcc @ 2.85MHz			Comments	
		4.5	4.75	5.0	5.25	5.5	4.5	4.75	5.0	5.25		5.5
RESET	-55											
	25											
	100											
MEMORY CYCLE:	-55											
	25											
	100											
PROGRAM COUNTER:	-55											
	25											
	100	X										P.C. Increment
STACK POINTER:	-55											
	25											
	100	X										SP Lbyte Write
REGISTER ARRAY:	-55											
	25											
	100											
ALU:	-55											
	25											
	100											
PROCESSOR INTERRUPT:	-55											
	25											
	100											

Table 4.3

Device #1: 100
Date: 1/22/90

TEST	T E M P	Vcc @ 1MHz			Vcc @ 2.0MHz			Vcc @ 2.85MHz			COMMENTS
		4.5	4.75	5.0	5.25	5.5	4.5	4.75	5.0	5.25	
RESET	-55										
	25										
	100										
MEMORY CYCLE:	-55										
	25										
	100										
PROGRAM COUNTER:	-55										P.C. Increment
	25										
	100			X							
STACK POINTER:	-55										SP Lbyte Write
	25										
	100			X							
REGISTER ARRAY:	-55										
	25										
	100										
ALU:	-55										Extended Div Time
	25										
	100			X							
PROCESSOR INTERFRT:	-55										SP Lbyte Write
	25										
	100			X							

Table 4.4

Device # 7
Date: 7/7/80

TEST	T S P	Vcc @ 1MHz			Vcc @ 2.0MHz			Vcc @ 2.85MHz			Comments
		4.5	4.75	5.0	5.25	5.5	4.5	4.75	5.0	5.25	
RESET	-55										Processor Load (no reset)
	25										
	100	X									
MEMORY CYCLE:	-55										
	25										
	100										
PROGRAM COUNTER:	-55										P.C. Increment
	25										
	100	X	X				X				
STACK POINTER:	-55										SP 1 byte write
	25										
	100	X	X				X				
REGISTER ARRAY:	-55										XRTG = 167
	25										
	100	X									
ALU:	-55										XRTG = 80
	25										
	100	X	X				X				
PROCESSOR INTERFMT:	-55										XRTG = 96
	25										
	100	X	X				X				

Continued on
sheet 2/22/00

Table 4.5

4.0 DEVICE EVALUATION

4.1 The data base used in evaluating the MC68000 was quite extensive. It involved three mask set iterations, devices with very noticeable process changes in addition to samples from one second source vendor (Hitachi).

The preliminary evaluation of the MC68000 was performed using the R9M mask set XC68000 device. This mask set of devices was the first set released by the vendor for user evaluation. It was not a fully functional device and therefore was shortly replaced with the T6E mask set. The R9M mask set was not evaluated using the characterization program due to the functional anomalies that were present.

The following mask set devices were evaluated using the existing characterization program.

- o T6E (10 pcs)
- o CCl - 8 MHZ (10 pcs)(early)
- o CCl - 10 MHZ (5 pcs)
- o CCl - 8 MHZ (5 pcs)(late)
- o T6E - Hitachi (6 pcs)

4.2 T6E DEVICE EVALUATION

The T6E mask set devices were tested prior to completion of the instruction decode test and AC/DC performance test. Therefore early analysis of the device was performed using the Logic Block element test (LBET) software only. Week codes for these devices were 8013 and 8019.

Shown in Table 4.0-4.5 are the functional failures for the T6E devices. The 10 samples were tested with one device indicating no functionality at +25°C. This device was deleted from the remaining tests. The remaining 9 pcs of the XC68000 (T6E) were all functional at 25°C and -55°C TCASE. Problems with 6 of the devices occurred between 90°C and 100°C (TCASE) most notably with Vcc = 4.5 volts and FREQ = 1.0 MHZ. The nature of the failure centered on small geometry devices that were either leaking or failing to keep the internal bus precharged at slow frequencies and high temperature. When the device is operated at a slow frequency 1.0 - 3.0 MHZ and at an elevated temperature (<70°C) it is believed that the nodes were not maintaining (bleeding-off) the precharged level. This resulted in the address being lost prior to being latched into the output buffer logic. This anomaly was seen in the Program Counter Test, Stack Pointer Test and (on some devices), the Reset Test.

The software was modified to perform the functional tests at 2.0 MHZ and 2.88 MHZ in addition to the 1.0 MHZ test. The data in Table 4.0 - 4.5 indicates that functionality improved with increasing frequency due to the fact that the dynamic like nodes have less time to bleed-off prior to being latched into the output buffer. This problem was to be corrected on later devices and prompted an evaluation of the CCl (8 MHZ) MC68000 mask set. Motorola,

however, changed the minimum operating frequency to 2.0 MHZ, and finally 3.0 MHZ in order to allow for the faster 8, and 10 MHZ drivers being developed

4.3 CCI (8 MHZ) DEVICE EVALUATION

4.3.1 Functional Testing

The first evaluation of the CCI mask set MC68000 was performed on 10 devices. The devices were week coded 8105.

The devices were initially screened across the mil-temp range of -55°C to $+125^{\circ}\text{C}$ (TCASE). The functional performance of the devices at the $+125^{\circ}\text{C}$ was degraded significantly from the $+110^{\circ}\text{C}$ (TCASE) performance. This resulted in the loss of a majority of the functional dependent AC-DC performance data. In evaluating the cause of the device failures it was discovered that at the elevated case temperature of $+125^{\circ}\text{C}$, the θ_{jc} of the device (the temperature difference between junction temperature and case temperature) was approximately $10\text{--}15^{\circ}\text{C}/\text{watt}$. At the case temperature of 125°C , the junction temperature of a device dissipating 750 mw would be in excess of 135°C . At the date of manufacture the vendor was varying his process in order to optimize his yield and it is doubtful that the process would support functionality at this elevated temperature. The data taken at $+110^{\circ}\text{C}$ (TCASE) indicated acceptable device performance therefore functional testing was performed across a temp-range of -55°C to $+110^{\circ}\text{C}$ (TCASE).

Shown in Table 5.0-5.2 is a summary of the functional test results obtained during device testing. Due to the lengthy test time (approximately 25 min) required to test each device, the LBET portion of the functional test was bypassed. One device was found non-functional at room-temperature testing after delivery and was therefore deleted from the remaining temperature test runs.

At the -55°C (TCASE) test functional failures were noted on devices #1, #8. Device #8 exhibited high Vcc (5.5 volts) fails on select tests. The failure mechanism was found to be the status register in that during the op-code execution of CMP D5, D3, and Ext D3 (Byte) the EXTEND bit in the status register was being set. Device #1 exhibited similar failures at different Vcc levels. When tested at 25°C (TCASE) device #1 exhibited similar failures to those that were noted at the -55°C temp. test. All other devices were fully functional. The final temp. test was performed at $+110^{\circ}\text{C}$ (TCASE). Functional failures were noted on devices #7, #9. Device #7 would not process out of RESET vector 0 (power-on RESET) for any functional tests. Device #9 exhibited low Vcc (4.5 volt) fails on select tests. The failure mechanism centered on the inability of AS and DS to function properly during processor READ/WRITE operations. While this lot of devices showed significant improvement in functionality over previous T6E devices, IBM pursued testing of more mature CCL MASK product at 10 MHZ and a re-test of 8 MHZ devices to obtain full functionality at the mil temperature extremes.

[illegible]

4.3.2 DC Parametric Tests

The minimum and maximum data values obtained across the tested temperature range are shown in Table 5.3. It was noted that one device exhibited a slightly lower VOL (2.35 volts) than desired on the Enable output. It was later learned that the enable output would be redesigned. Power dissipation was found to be 1.1 watts worse case ($V_{CC} = 5.5$ volts @ -55°C TCASE). This was within the vendors specification of 1.2 watts max. All remaining DC parameters were within the vendors specification.

4.3.3 FMAX Testing

FMAX testing indicated all devices to be operating at an FMAX of approximately 7.1 to 7.7 MHZ. The maximum frequency of operation occurs at the -55°C TCASE temperature. The 8 MHZ commercial temperature devices being tested were adequate to meet 6 MHZ military temperature operations. Therefore, the 6 MHZ commercial specifications for frequency and performance were used as pass/fail criteria for the devices in a military temperature environment.

4.3.4 AC Performance Testing

All devices were tested across the temp range of -55°C to $+110^{\circ}\text{C}$ TCASE. Shown in Table 5.4 - 5.5 are the min-max summary for all measured delays. All devices met the vendors 0°C - 70°C specification for a 6 MHZ device. It was noted during testing that the clock pulse width high delay (tCH) seemed to track with the frequency of the device. Through experimentation and later correlation it was found that the frequency of the device could be determined (± 0.5 MHZ) by the following equation.

$$\text{FMAX} = 1/[2(\text{Tch}) + \text{trise} + \text{tfall}]$$

Where: $\text{trise} + \text{tfall} = 6\text{ns}$

Using this method of determining FMAX it was found that worse case FMAX was:

$$\begin{aligned}\text{FMAX} &= 1/[2(61)\text{ns} + 6\text{ns}] \\ &= 1/128 \text{ us} \\ &= 7.8 \text{ MHZ}\end{aligned}$$

This clearly indicated the 8 MHZ 0°C - 70°C devices could meet an FMAX of 6.0 MHZ across the temperature range of -55° to $+110^{\circ}\text{C}$ (TCASE).

4.3.5 MC68000L8 Test Summary

Overall the AC, DC and FMAX performance was found to be acceptable when compared to a 6 MHZ device specification. However, functionally the devices exhibited some unusual anomalies at the lower (-55°C) test temp. It should be noted that the devices which exhibited the cold-temperature failures were the devices having the highest FMAX. This tends to point out a parameter of the process (threshold, or ion implantation) that results in increased performance but does not support functionality at the -55°C TCASE temperature.

REPORT TITLE -- MODELED DC PARAMETRIC TEST

RAOC CCL MASK SET PARTS

9 PCS SAMPLES 137

DATE 06/01/80

TEST	SWITCH	CONDITIONS	SPEC.	15M TEST		COMMENTS
				DATA	UNITS	
1. $V_{CE} = 10V$						
2. $V_{CE} = 10V$						
3. $V_{CE} = 10V$						
4. $V_{CE} = 10V$						
5. $V_{CE} = 10V$						
6. $V_{CE} = 10V$						
7. $V_{CE} = 10V$						
8. $V_{CE} = 10V$						
9. $V_{CE} = 10V$						
10. $V_{CE} = 10V$						
11. $V_{CE} = 10V$						
12. $V_{CE} = 10V$						
13. $V_{CE} = 10V$						
14. $V_{CE} = 10V$						
15. $V_{CE} = 10V$						
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36. $V_{CE} = 10V$						
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96. $V_{CE} = 10V$						
97. $V_{CE} = 10V$						
98. $V_{CE} = 10V$						
99. $V_{CE} = 10V$						
100. $V_{CE} = 10V$						

Table 5.3

It may also indicate a race condition or design problem with the device that precludes 1-2 MHz testing on the faster devices. At the higher test temp. (+100°C) the functional failures seem to be frequency related and supports the position that the lower frequency limit of 2 MHz must be changed to a minimum of 3 MHz, based on data obtained.

4.4 MC68000L10 DEVICE TESTING

Device testing was performed on 5 pcs of the MC68000L10 devices. Week codes for these devices were 8116 and 8119. These devices were loaned out by the vendor for characterization purposes only and were off-the-shelf, 0°C - 70°C, 10 MHz devices.

4.4.1 Functional testing

Functional tests results for the five devices tested are shown in Table 6.0 - 6.2. One device (#2) indicated functional failures at -55°C and +25°C TCASE temperature. All remaining devices were found to be functional. Generally, the failures were found to be related to low Vcc (4.5 volts), low frequency (2.0 MHz). The failure mechanism was failure to process out of Power-on reset and loss of address during RD/write operations. When tested at +110°C TCASE device #2 and #5 indicated functional failures. Device #5 failures occurred at Vcc = 4.5 volts with Freq = 2.0 MHz only. At the frequency of 2.85 MHz device #5 was functional. Device #2 exhibited across the board failures at Vcc = 4.5 volts.

4.4.2 DC Testing

DC parametric testing was performed across the temperature range -55°C to +110°C TCASE. Shown in Table 6.3 is the summarized D.C. parametric data. All devices tested within the vendors specification. It was noted that the two devices (#2, #5) exhibited higher supply current values (Icc) than the remaining 3 devices. This was especially evident on device #2 which exhibited an Icc (171 MA) 5% - 10% higher than the other devices (<165 MA). It was later shown that a screen of ICC <165 MA or a functional test at 3.0 MHz at 110°C would eliminate any potential functional fail devices.

4.4.3 FMAX Testing

All devices passed at the maximum tested FMAX of 8.33 MHz across the temperature range of -55°C to +110°C TCASE. Calculated FMAX (see sec. 4.3.4) indicates all devices operating with FMAX = 9.2 MHz worst case (Tc = +110°C).

4.4.4 AC Performance Testing

All 10 MHz, 0 to 70°C commercial devices tested within the vendors' 8 MHz specification in full mil operation. Table 6.4 shows performance measurements obtained during device testing.

[illegible]

Table 6.0

Res. 101

Table 6.1

2 x 9 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
300 INST. TEST	1 425	1	1	1	1 425	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
400 INST. TEST	1 425	1	1	1	1 425	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
500 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
600 INST. TEST	1 425	2	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
700 INST. TEST	1 425	1	1	1	1	1
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
800 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
900 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1000 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1100 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1200 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1300 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1400 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1500 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1600 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1700 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1800 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
1900 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1
2000 INST. TEST	1 425	1	1	1	1245	2
	1 540	1	1	1	1	1
	1 547	1	1	1	1	1

[illegible]

Best Available Cost

REPORT TITLE: MOTOROLA MC68000 AC PERFORMANCE TESTS --- CELL MASK SET PARTS: DEVICE: 1 #870
 DEVICE TYPE: 1 LG DATE CODE: 1000

TEST	SYMBOL	CONDITIONS	SPEC		TDM TEST DATA			COMMENTS
			MIN	MAX	100	125	140	
DIN TO CLK LOW (TSET)	TDIOL		25	-	0	1	0	TEMP: 100C TO 110C TOL
DIN TO CLK LOW (THOLD)	TDIOL		-	-	0	4	4	VCC: 5.0V VLTG FREQ: 2.0 MHz
DTACK TO CLK LOW (TSET)	TDIOL		25	-	0	0	0	
DR TO CLK LOW (TSET)	TDIOL		25	-	1	0	0	
DR TO CLK LOW (THOLD)	TDIOL		-	-	2	2	2	
DGACK TO CLK LOW (TSET)	TDIOL		25	-	15	15	15	
DGACK TO CLK LOW (THOLD)	TDIOL		-	-	0	14	14	
VMA TO CLK LOW (TSET)	TDIOL		25	-	3	4	4	
VMA TO CLK LOW (THOLD)	TDIOL		-	-	4	4	4	REQUIRES SPECIAL TEST MGR
DSN TO CLK LOW (TSET)	TDIOL		25	-	3	2	3	
DSN TO CLK LOW (THOLD)	TDIOL		-	-	4	3	3	
CLK WIDTH LOW	TL		75	250	26	23	31	
CLK WIDTH HIGH	TH		75	250	33	43	52	
CLK HIGH TO FC VALID	TECLV		-	60	30	38	45	
CLK HIGH TO AN LOW	TEHNL		0	-	19	31	42	(MIN)
CLK HIGH TO AN HIGH	TEHNL		-	70	31	40	50	(MAX)
CLK HIGH TO DS LOW	TEHNL		0	-	19	26	35	(MIN)
CLK HIGH TO DS HIGH	TEHNL		-	70	29	39	47	(MAX)
CLK LOW TO AN HIGH	TELSH		-	60	34	40	51	
CLK LOW TO DS HIGH	TELSH		-	60	31	45	53	
CLK H TO R-W H	TEHRL		0	-	16	24	29	(MIN)
CLK H TO R-W H	TEHRL		-	62	11	14	16	(MAX)
CLK HIGH TO R-W LOW	TEHRL		-	60	10	15	25	
CLK L TO DOUT VALID	TELDV		-	60	30	38	50	
CLK L TO ADDR VALID	TECLV		-	60	43	50	60	
CLK HIGH TO PG LOW	TEHGL		-	60	12	16	26	
CLK HIGH TO PG HIGH	TEHGL		-	60	15	19	24	
CLK LOW TO VMA LOW	TEVML		-	60	20	24	36	
CLK LOW TO VMA HIGH	TEVML		-	60	11	16	28	REQUIRES SPECIAL TEST MGR
CLK LOW TO E LOW	TEELE		-	60	15	21	31	
CLK LOW TO E HIGH	TEELE		-	60	16	20	27	REQUIRES SPECIAL TEST MGR
CLK L TO ADDRESS L2 L3	TEHNL	VOLT: 1.2V	-	60	66	74	87	
CLK L TO ADDR INV L2 L3	TEHNL		0	-	76	87	95	
CLK L TO ADDR L2 L3	TEHNL	VOLT: 1.2V	-	60	45	50	61	
CLK HIGH TO R-W L2 L3	TEHNL		-	60	45	50	61	
CLK HIGH TO DATA L2 L3	TEHNL	VOLT: 1.2V	-	60	52	58	74	

6. CASE TEMPERATURE

Table 6.4

4.4.5 MC68000L10 Summary

The DC, AC and FMAX data obtained on the MC68000L10 devices indicates that the devices performed extremely well across the Mil-temp range when compared to the vendors 8 MHZ 0-70°C specification. The functional failures on device #5 would not have been noted if the minimum FMAX specification was 3 MHZ. The functional problems noted with device #2 are attributed to the vendors process and can be detected with a 4.5 volt functional screen across temp. The graph shown in Figure 4.0 (ICC vs TEMP) clearly illustrates that the processing parameters of devices #2 and #5 are somewhat different from the remaining three devices. All five parts were hand-screened 8 MHZ devices for 0 to 70°C operations. It is quite obvious from the test data that the vendors process had improved significantly during the time between early 8 MHZ and these 10 MHZ device evaluations and consequently the most recent 8 MHZ should show a much improved performance.

4.5 MC68000L8 (Later Vintage) Device Testing

Based upon the data taken on the MC68000L10 devices, 5 pcs of the most recent vintage MC68000L8 were loaned by the vendor for evaluation.

4.5.1 Functional Testing

Functional testing of the most recent 8 MHZ devices indicates similar results as were obtained during 10 MHZ device testing. Shown in Table 7.0 - 7.2 is a summary of the functional test results. One device (#3) was non-functional at the -55°C test temperature. The failure mode centered on loss of address during process of RD/WRITE cycles and failure to process out of reset vector 0 (Power-on Reset) at low Vcc (4.5v). All devices were functional at +25°C. Devices #3 and #1 exhibited functional failures at the +110°C test temperature. Device #1 exhibited low Vcc/Low Freq (4.5 volts/2.0 MHZ) failures. These failures were not detected as the frequency increased (2.85 MHZ). Device #3 continued to exhibit low Vcc (4.5 volts) failures. The failure mode was similar to those noted at the -55°C test temperature.

4.5.2 D.C. Parametric Testing

All devices tested within the vendors 8 MHZ 0°-70°C specification. Shown in Table 7.3 are the D.C. test results obtained for all devices tested. Worst case supply current was measured to be 217.8 MA at Vcc = 5.5 volts @ -55°C TCASE. This translates into 1.2 watts maximum power dissipation.

4.5.3 FMAX Testing

Maximum frequency of operation for all devices tested was measured to be 7.1 MHZ (MAX). Based upon clock pulse width high calculations, the slowest device across the tested temperature was calculated to have an FMAX = 7.9 MHZ worst case.

ICC VS TEMPERATURE FOR MC68000L10

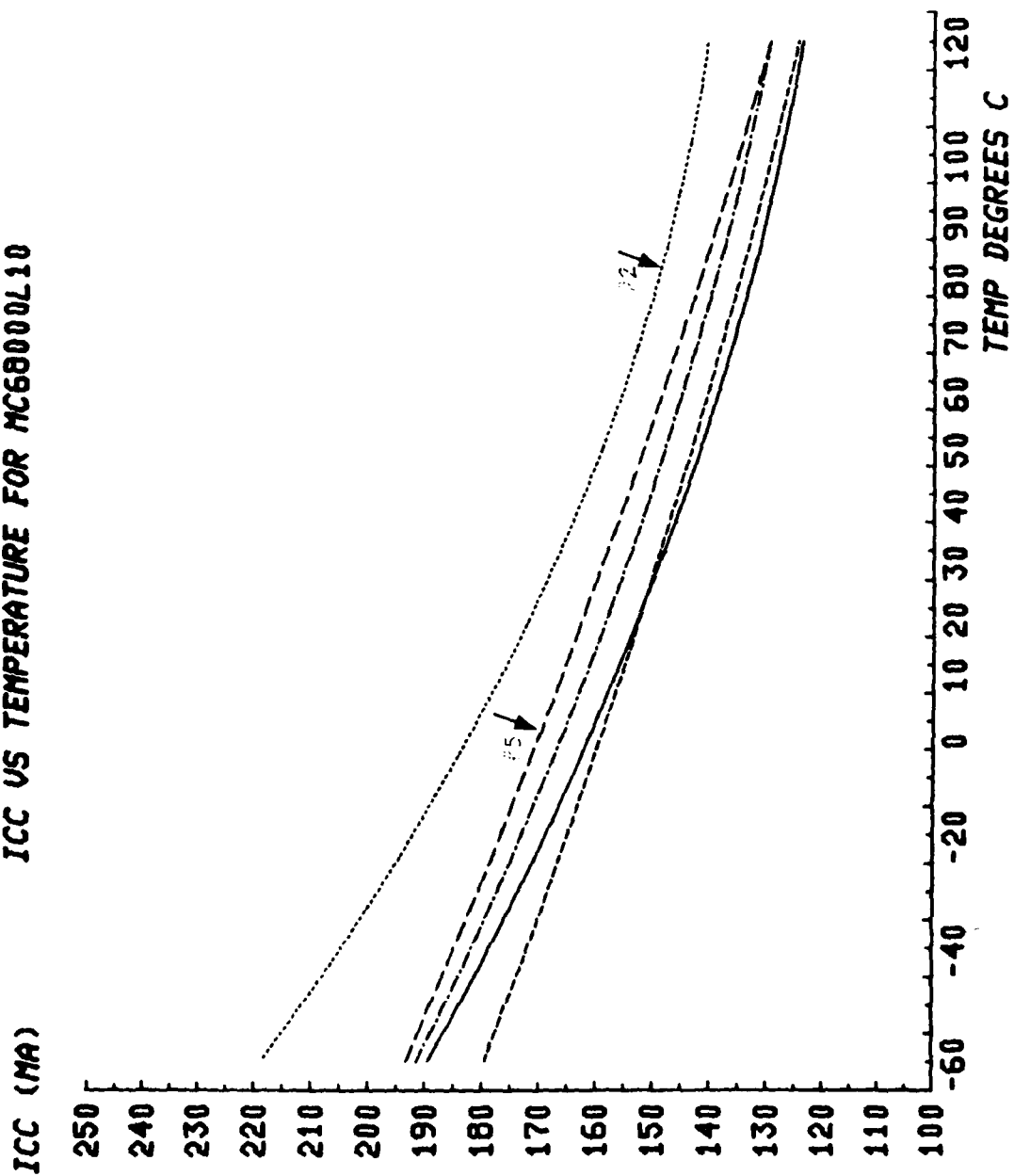


Figure 4.0

Available Copy

[illegible]

Table 7.0

[illegible]

Table 7.1

TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
TEST NAME INST. TEST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54																																														

Table 7.2

REPORT TITLE: MOTOROLA MC68000 AC PERFORMANCE TIMES, CPU MARK SET TABLES, DEVICE 1, # 1, 1
 DEVICE: MC68000, DATE: 03/02/88

TEST	NAME	CONDITIONS	SPEC.		TYP. TEST DATA *				COMMENTS
			MIN	MAX	100	125	150	170	
CLK TO CLK LOW (TCLCL)	TCLCL		25	-	3	3	2	2	TEMP: 100°C TO 150°C, VCC = 5.0V
CLK TO CLK LOW (TCLCL)	TCLCL		-	-	4	4	3	3	TEMP: 125°C MAX
CLK TO CLK LOW (TCLCL)	TCLCL		25	-	0	0	0	0	
CLK TO CLK LOW (TCLCL)	TCLCL		25	-	2	2	2	2	
CLK TO CLK LOW (TCLCL)	TCLCL		-	-	3	2	2	2	
CLK TO CLK LOW (TCLCL)	TCLCL		25	-	-1	-1	-1	-1	
CLK TO CLK LOW (TCLCL)	TCLCL		-	-	0	0	0	0	
VMA TO CLK LOW (TCLVMA)	TCLVMA		25	-	-4	-2	-5	-5	REQUIRES SPECIAL TEST MODE
VMA TO CLK LOW (TCLVMA)	TCLVMA		-	-	-1	-2	-4	-4	
DATA TO CLK LOW (TCLD)	TCLD		25	-	3	3	4	4	
DATA TO CLK LOW (TCLD)	TCLD		-	-	4	4	4	4	
CLK WIDTH LOW	TCLL		25	250	23	23	32	32	
CLK WIDTH HIGH	TCLH		25	250	39	48	59	59	
CLK HIGH TO CL VALID	TCLAV		-	60	35	45	65	65	
CLK HIGH TO AS LOW	TCLASL		0	-	28	39	49	49	(MIN)
CLK HIGH TO AS LOW	TCLASL		-	70	37	47	59	59	(MAX)
CLK HIGH TO DS LOW	TCLDSL		0	-	23	36	46	46	(MIN)
CLK HIGH TO DS LOW	TCLDSL		-	70	33	42	56	56	(MAX)
CLK LOW TO AS HIGH	TCLASH		-	60	37	46	63	63	
CLK LOW TO DS HIGH	TCLDSH		-	60	34	53	72	72	
CLK H TO R-W H	TCLRHX		0	-	23	29	34	34	(MIN)
CLK H TO R-W H	TCLRHX		-	70	14	18	22	22	(MAX)
CLK HIGH TO R-W LOW	TCLRHL		-	60	13	25	28	28	
CLK L TO OOUT VALID	TCLDGO		-	60	33	45	57	57	
CLK L TO ADDR* VALID	TCLAV		-	60	48	58	73	73	
CLK HIGH TO BG LOW	TCLBGL		-	60	14	26	30	30	
CLK HIGH TO BG HIGH	TCLBCH		-	60	18	23	31	31	
CLK LOW TO VMA LOW	TCLVML		-	60	24	33	42	42	
CLK HIGH TO VMA HIGH	TCLVMH		-	-	15	27	34	34	REQUIRES SPECIAL TEST MODE
CLK LOW TO E LOW	TCLLEL		-	-	16	29	39	39	
CLK LOW TO E HIGH	TCLLEH		-	-	18	24	34	34	REQUIRES SPECIAL TEST MODE
CLK H TO ADDR* PC T.S.*	TCHAZX	VOUT ±0.5V	-	100	68	69	79	79	
CLK H TO ADDR* INVALID T.S.*	TCHAZ	"	0	-	65	66	77	77	
CLK HIGH TO AS+DS T.S.*	TCHZ	VOUT ±0.5V	-	100	48	51	56	56	
CLK HIGH TO R-W T.S.*	TCHRZ	"	-	100	31	25	-	-	
CLK HIGH TO DATA T.S.*	TCHAZX	VOUT ±0.5V	-	100	57	71	101	101	

* CASE TEMPERATURE

Table 7.4

4.5.4 AC Performance

All devices tested within the vendors 0° - 70° C 6 MHZ specification. Shown in Table 7.4 are the summarized results of the data obtained during device testing.

4.5.5 MC68000L8 (Latest Vintage) Summary

It is obvious that the performance of this set of 8 MHZ devices has improved significantly from the performance of the earlier 8 MHZ devices. Shown graphically in Figures 5.0-5.1 are two trends that illustrate the performance of the later vintage 8 MHZ devices. It is obvious that at the time of manufacture the vendor was making process changes to optimize yield and performance. This resulted in somewhat different NMOS trends in the earlier devices (L8). The later vintage (L8X) device trends are nearly those of the L10 devices as evidenced by the graphs of Figures 5.0-5.1. The later vintage MC68000L8 improved functionality and performance as a direct result of the vendors matured and stabilized process.

4.6 HD68000 DEVICE TESTING

Device Testing was performed on 6 pcs of Hitachi's HD68000. Hitachi is manufacturing the device under a Mask Exchange Agreement with Motorola and are manufacturing the device using the T6E mask set. Devices were marked as HD68000 with a 1D3 lot code identifier.

4.6.1 Functional Testing

Shown in Table 8.0 - 8.2 is the functional test summary for the HD68000 devices. Device testing at -55° C (TCASE) indicated functional failures on 3 devices (#2, #5, #6). These failures were very similar to the failures noted on late T6E/early CCL Mask Set device MC68000's with the faster devices exhibiting high V_{cc} (5.5 volt) fails at the -55° C test temp. The failure mechanism was the loss of address and improper conditions on AS, DS during processor RD/WRITE operations. Device #2 exhibited gross functional failures at the $+25^{\circ}$ C test temperature. The failure mechanism was the loss of address during processor RD/WRITE operations. All devices were functional at the $+110^{\circ}$ C (TCASE) test temperature.

4.6.2 D.C. Parametric Testing

All device parameters were within the vendors 0° - 70° C specification with the exception of supply current (I_{cc}). Shown in Table 8.3 is the data summary obtained during device testing. I_{cc} was measured to be 209 MA typically ($+25^{\circ}$ C). This was approximately 25% higher than typical I_{cc} measured on the MC68000 devices. This resulted in a 1.7 watt part worst case ($V_{cc} = 5.5$ Volts, @ -55° C) and exceeded the vendors original specification of 1.2 watts maximum.

MC68000

ICC VS TEMP

ICC (mA)

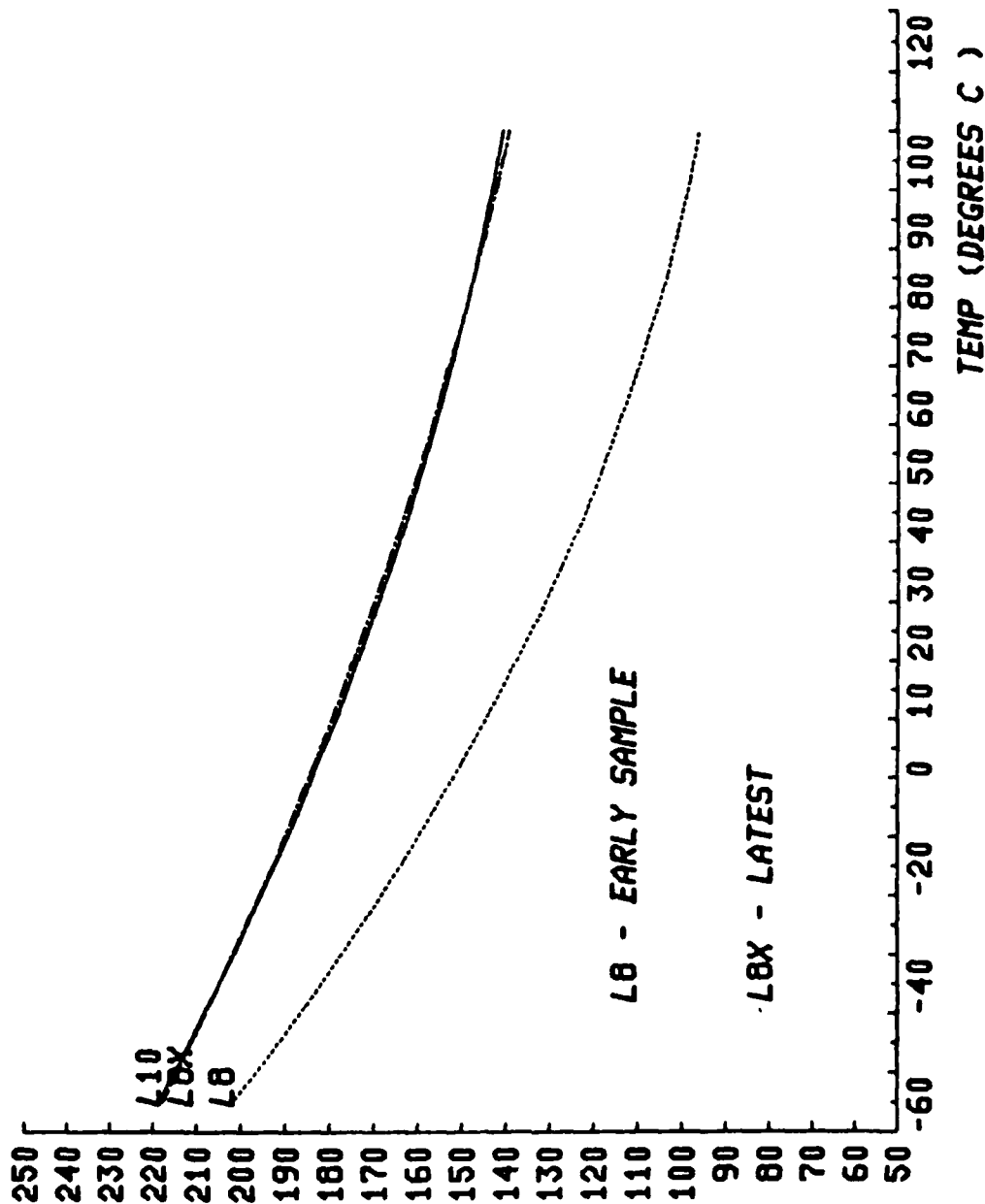


Figure 5.0

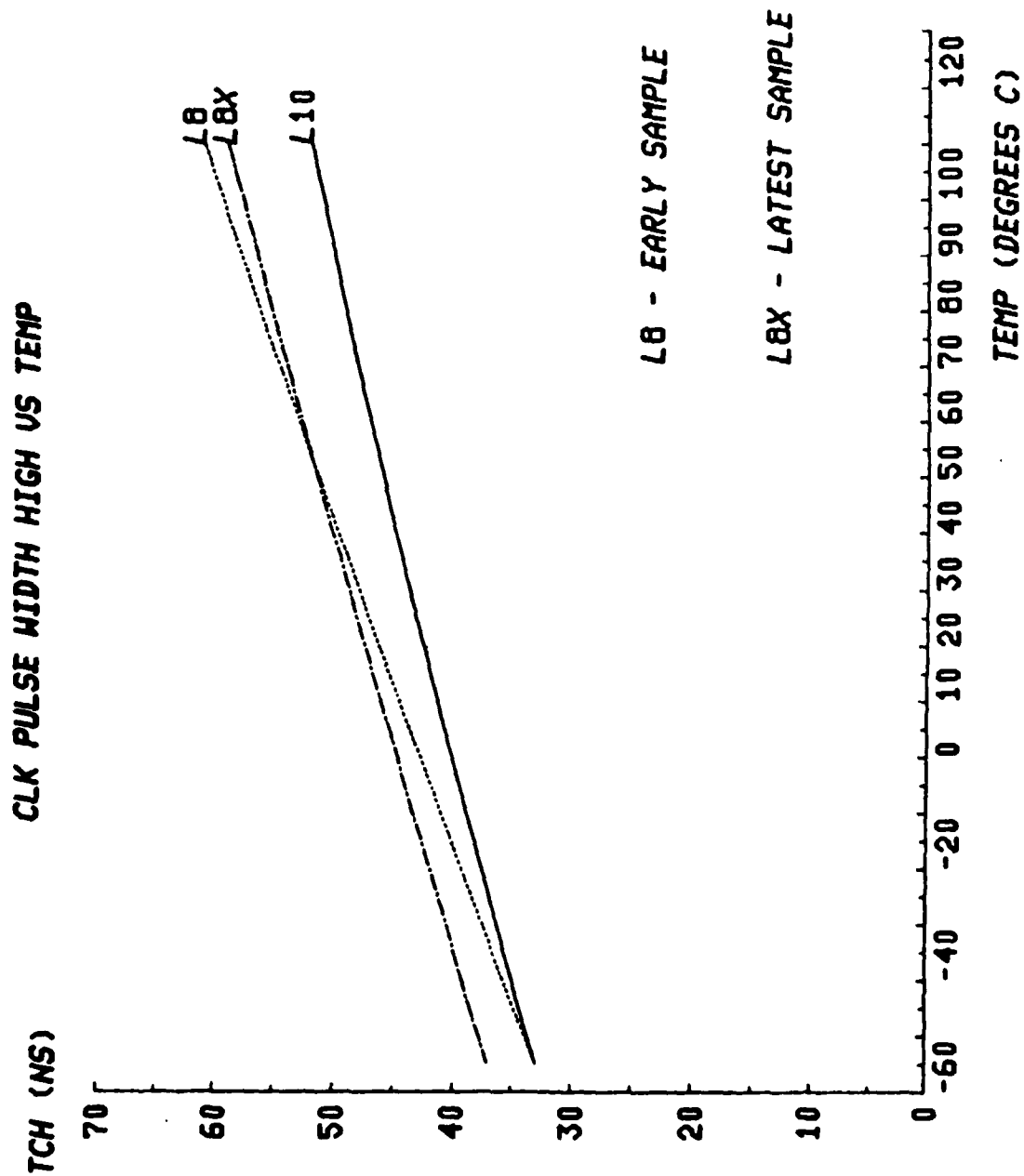


Figure 5.1

MEMOIR TITLE INSTRUCTION DECODER FAILURE SUMMARY MEMOIR - FOR

	VCC	FREQ MHz @ -55C [2.00] ± 0.25	FREQ MHz @ +110C [2.00] ± 0.25	FREQ MHz @ +110C [2.00] ± 0.25	COMMENTS
1.00 INST. TEST	1.45	1	1	1	NO FUNCTIONAL FAILURES NOTED AT +110C
	1.50	1	1	1	
	1.55	1	1	1	
1.01 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.02 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.03 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.04 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.05 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.06 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.07 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.08 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.09 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	
1.10 INST. TEST	1.45	1	1	1	
	1.50	1	1	1	
	1.55	1	1	1	

Table 6.0

• CAST TEMPERATURE

50

4.6.3 Maximum Frequency of Operation (FMAX) testing

All devices passed the maximum tested FMAX of 8.33 MHZ at the temperature range of -55°C to $+110^{\circ}\text{C}$ (TCASE). Calculated using pulse width high, the FMAX was found to be approximately 13.8 MHZ worst case ($+110^{\circ}\text{C}$), however more samples need to be tested to guarantee this method of calculation holds true with the second vendor's process.

4.6.4 AC Testing

All device tested to within the vendors specification for a 6 MHz device shown in Table 8.4 are the AC performance results obtained during testing.

4.6.5 HD68000 Test Summary

The HD68000 device exhibited an unusually high FMAX (13.8 MHZ worst case). This is directly related to the vendors process. This is further illustrated by the supply current (I_{cc}) data which resulted in an unusually high power dissipation. Having noted these two process parameters the functional performance was as expected. The fastest parts exhibiting the low temp (-55°C), High Vcc (5.5 volt) failures. However, it should be noted that not all the devices exhibited failures at the low temperature and that in general the devices have a higher than anticipated maximum frequency of operation. It can be expected as the vendor homes in on the corners of his process that the device failures noted during functional testing will go away resulting in a much improved MIL-temp device. In addition, the second source vendor's will be receiving next generation masks (vintage CCl) for processing. This mask set allows more margining due to critical path enhancements.

5.0 CONCLUSION

The evaluation of the MC68000 microprocessor was a complex and time consuming task. It involved the evaluation of many different mask set devices and devices with varying performance characteristics. However, the data presented within this report clearly shows that the device from its infant stage of development (R9M MASK SET) to the present day device has matured into one of the most technologically advanced 16-bit microprocessors available. Its performance across the MIL-temp range clearly indicates its applicability to a military environment. The vendors commitment to develop and provide this device for use within a Hi-Rel market combined with the general acceptance of the device by the design community should serve to provide a valuable tool to the electronic industry.

The existence of 5 potential sources through mask exchange with Motorola will provide a highly competitive and reliable part to military users. Of the five vendors, Motorola, Hitachi, Mostek and Rockwell have samples, while Signetics plans availability in 1982.

Motorola also plans enhancements to the performance of the MC68000 up to 16 MHZ in 1982. By 1Q82, a 12 MHZ device should be available, which by past experience should yield a 10 MHZ mil-temp device.

The performance growth and large compendium of peripheral circuits planned make this processor not only an excellent present design choice, but one that will offer future growth in all military applications.

APPENDIX A

EXG

NOP
MOVE AAAA, D₁
MOVE 5555, D₇
MOVE FF00, A₁
MOVE 00FF, A₆
MOVE D₁, (A₇)
MOVE D₇, (A₇)
MOVE A₁, (A₇)
MOVE A₆, (A₇)
EXG D₁, D₇
MOVE D₁, (A₇)
MOVE D₇, (A₇)
EXG A₁, A₆
MOVE A₁, (A₇)
MOVE A₆, (A₇)
EXG D₇, A₁
MOVE D₇, (A₇)
MOVE A₁, (A₇)
EXG A₆, D₁
MOVE D₁, (A₇)
MOVE A₆, (A₇)
NOP
STOP

LEA

```

NOP
MOVE      0000, A0
MOVE      0000, A1
MOVE      0000, A2
MOVE      0000, A3
MOVE      0000, A4
MOVE      0000, A5
MOVE      0000, A6
MOVE      A0, (A7)
MOVE      A1, (A7)
MOVE      A2, (A7)
MOVE      A3, (A7)
MOVE      A4, (A7)
MOVE      A5, (A7)
MOVE      A6, (A7)
LEA        xxx.W, A0
LEA        xxx.W, A1
LEA        xxx.W, A2
LEA        xxx.W, A3
LEA        xxx.W, A4
LEA        xxx.W, A5
LEA        xxx.W, A6
MOVE      A0, (A7)
MOVE      A1, (A7)
MOVE      A2, (A7)
MOVE      A3, (A7)
MOVE      A4, (A7)
MOVE      A5, (A7)
MOVE      A6, (A7)
NOP
STOP

```

LINK

NOP
MOVE 1000, A₁
NOP
LINK A₁, 0100
NOP
NOP
UNLINK A₁
NOP
STOP

PEA

NOP
MOVE 00001200, A₄
PEA A₄
NOP
STOP

MOVE

NOP
MOVE

5555, D₀
AAAA, D₇
D₀, (A₇)
D₇, (A₇)
AAAA, D₂
5555, D₆
FOFO, A₁
OFOF, A₆
D₂, (A₇)
D₆, (A₇)
A₁, (A₇)
A₆, (A₇)
AAAAAAAA, D₃
55555555, D₅
FOFOFOFO, A₂
OFOFOFOF, A₅
D₃, (A₇)
D₅, (A₇)
A₂, (A₇)
A₅, (A₇)
A₅, A₂
D₅, D₃
A₂, (A₇)
D₃, (A₇)
0000 OFOF, D₀
0050, D₁
D₀, (A₇) L. WORD
D₀, (A₇) + D L. WORD
D₀, (A₇) + INDX + D L. WORD
D₀, (A₇) - L. WORD

MOVE

NOP
STOP

D₀, (A₇) + L. WORD
(PC+DISP), D₁
(PC+DISP+INDX), D₁

MOVEM

NOP		MOVE	A ₅ , (A ₇)
MOVE	1200, A ₆		1300, A ₆
	D ₀ , (A ₇)	MOVEM	REG LIST, (A ₆)
	D ₁ , (A ₇)	MOVE	1300, A ₆
	D ₂ , (A ₇)	MOVEM	REG LIST (A ₆)
	D ₃ , (A ₇)	NOP	
	D ₄ , (A ₇)	STOP	
	D ₅ , (A ₇)		
	D ₆ , (A ₇)		
	D ₇ , (A ₇)		
	A ₀ , (A ₇)		
	A ₁ , (A ₇)		
	A ₂ , (A ₇)		
	A ₃ , (A ₇)		
	A ₄ , (A ₇)		
	A ₅ , (A ₇)		
	1250, A ₆		
MOVEM	(A ₆), REG LIST		
MOVE	D ₀ , (A ₇)		
	D ₁ , (A ₇)		
	D ₂ , (A ₇)		
	D ₃ , (A ₇)		
	D ₄ , (A ₇)		
	D ₅ , (A ₇)		
	D ₆ , (A ₇)		
	D ₇ , (A ₇)		
	A ₀ , (A ₇)		
	A ₁ , (A ₇)		
	A ₂ , (A ₇)		
	A ₃ , (A ₇)		
	A ₄ , (A ₇)		

MOVEP

```
NOP
MOVE      A000, A0
MOVEP     55FFAAFF, D0
MOVE      D0, (A7)
MOVEP     D1
MOVE      D1, (A7)
MOVE      A001, A0
MOVEP     FF55FFAA, D2
MOVE      D2, (A7)
MOVEP     D3
MOVE      D3, (A7)
MOVEP     D3, (A0)
MOVEP     D2, (A0)
MOVE      A000, A0
MOVEP     D1, (A0)
MOVEP     D0, (A0)
NOP
STOP
```

MOVEQ

```

NOP
MOVE      0000, D1
MOVE      0000, D3
MOVE      0000, D6
MOVE      D1, (A7)
MOVE      D3, (A7)
MOVE      D6, (A7)
MOVEQ     55, D1
MOVEQ     0A, D3
MOVEQ     0F, D6
MOVE      D1, (A7)
MOVE      D3, (A7)
MOVE      D6, (A7)
NOP
STOP

```

MOVE A

```

NOP
MOVE      0000, A0
MOVE      0000, A3
MOVE      0000, A6
MOVE      A0, (A7)
MOVE      A3, (A7)
MOVE      A6, (A7)
MOVEA     5555AAAA, A0
MOVE      A0, (A7)
MOVEA     A0, A3
MOVE      A3, (A7)
MOVEA     A0, A6
MOVE      A6, (A7)
NOP
STOP

```

SWAP

NOP

MOVEQ

00, D₀
00, D₁
00, D₂
00, D₃
00, D₄
00, D₅
00, D₆
00, D₇

MOVE

D₀, (A₇)
D₁, (A₇)
D₂, (A₇)
D₃, (A₇)
D₄, (A₇)
D₅, (A₇)
D₆, (A₇)
D₇, (A₇)

MOVEQ

0A, D₀
55, D₁
0A, D₂
55, D₃
0A, D₄
55, D₅
0A, D₆
55, D₇

SWAP

D₀
D₁
D₂
D₃
D₄
D₅

SWAP

MOVE

D₆
D₇
D₀, (A₇)
D₁, (A₇)
D₂, (A₇)
D₃, (A₇)
D₄, (A₇)
D₅, (A₇)
D₆, (A₇)
D₇, (A₇)

NOP

STOP

ADD

```

NOP
MOVE      5555, D1
MOVE      AAAA, D3
MOVE      OFOF, A1
MOVE      FOFO, A3
MOVE      D1, (A7)
MOVE      D3, (A7)
MOVE      A1, (A7)
MOVE      A3, (A7)
ADD       AAAA, D1
MOVE      SR, (A7)
MOVE      D1, (A7)
ADD       5555, D3
MOVE      SR, (A7)
MOVE      D3, (A7)
MOVE      FOFO, D1
ADD       D1, D0
MOVE      SR, (A7)
MOVE      D1, (A7)
MOVE      OOFU, D3
MOVE      0050, D1
ADD       D3, D1
MOVE      SR, (A7)
MOVE      D1, (A7)
MOVE      0000, D0
MOVE      5555, A0
MOVE      1300, A6
MOVE      AAAA, (A6)
ADDQ      5, D0
MOVE      SR, (A7)
MOVE      D0, (A7)

```

```

ADDQ      5, A0
MOVE      SR, (A7)
MOVE      A0, (A7)
ADDQ      5, (A6)
MOVE      SR, (A7)
MOVE      (A6), (A7)
NOP
STOP

```

ADDX

```

NOP
MOVE      0000, D2
MOVE      5555, D4
MOVE      12FE, A2
MOVE      1300, A6
MOVE      0505, A5
MOVE      D2, (A7)
MOVE      D4, (A7)
MOVE      A2, (A7)
MOVE      A4, (A7)
MOVE      2700, SR
ADDX      D2, D4
MOVE      SR, (A7)
MOVE      D4, (A2)
MOVE      5555, D2
MOVE      0000, D4
MOVE      2710, SR
ADDX      D4, D2
MOVE      SR, (A7)
MOVE      D2, (A7)
NOP
STOP

```

CLR

```
NOP
MOVE      FFFF, D0
MOVE      FFFF, D1
MOVE      FFFF, D2
MOVE      FFFF, D3
MOVE      D0, (A7)
MOVE      D1, (A7)
MOVE      D2, (A7)
MOVE      D3, (A7)
CLR       D0
MOVE      SR, (A7)
CLR       D1
MOVE      SR, (A7)
CLR       D2
MOVE      SR, (A7)
CLR       D3
MOVE      SR, (A7)
MOVE      D0, (A7)
MOVE      D1, (A7)
MOVE      D2, (A7)
MOVE      D3, (A7)
MOVE      1374, A6
MOVE      1350, A5
MOVE      1324, A4
CLR       (A6)
CLR       (A5)
CLR       (A4)
NOP
STOP
```

CMP

NOP
 MOVE 00AA, D₃
 MOVE 0055, D₅
 MOVE 1350, A₆
 MOVE D₃, (A₇)
 MOVE D₅, (55)
 CMP D₅, D₃
 MOVE SR, (A₇)
 MOVE D₃, (A₇)
 MOVE 00AA, D₃
 MOVE 0055, D₅
 CMP D₃, D₅
 MOVE SR, (A₇)
 MOVE D₅, (A₇)
 MOVE 0055, D₃
 MOVE 0055, D₅
 CMP D₅, D₃
 MOVE SR, (A₇)
 MOVE D₃, (A₇)
 MOVE 00AA, (A₆)
 MOVE 00AA, D₅
 CMP (A₆), D₅
 MOVE SR, (A₇)
 MOVE D₅, (A₇)
 MOVE AAAA, D₀
 MOVE 1300, A₆
 MOVE AAAA, (A₆)
 MOVE 2700, SR
 CMPI AAAA, D₀
 MOVE SR, (A₇)
 MOVE D₀, (A₇)

CMPI 5555, (A₆)
 MOVE SR, (A₇)
 MOVE (A₆), (A₇)
 MOVE 1300, A₆
 MOVE 1376, A₄
 MOVE 00AA, (A₆)
 MOVE AAAA, (A₄)
 MOVE 2700, SR
 CMPM (A₆), (A₄)
 MOVE SR, (A₇)
 NOP
 STOP

EXT

MOVE	0004, D ₀
MOVE	0084, D ₃
MOVE	D ₀ , (A ₇)
MOVE	D ₃ , (A ₇)
EXT	D ₀
MOVE	SR, (A ₇)
MOVE	D ₀ , (A ₇)
EXT	D ₃
MOVE	SR, (A ₇)
MOVE	D ₀ , (A ₇)
MOVE	7FFF, D ₀
MOVE	800F, D ₃
MOVE	D ₀ , (A ₇)
MOVE	D ₃ , (A ₇)
EXT	D ₀
MOVE	SR, (A ₇)
MOVE	D ₀ , (A ₇)
EXT	D ₃
MOVE	SR, (A ₂)
MOVE	D ₃ , (A ₂)
NOP	
STOP	

MULS

```

NOP
MOVE      5555, D0
MOVE      0002, D1
MOVE      2700, SR
MOVE      D0, (A7)
MOVE      D1, (A7)
MULS      D1, D0
MOVE      SR, (A7)
MOVE      D0, (A7)
MOVE      00FF, D0
MOVE      0000, D1
MOVE      2700, SR
MULS      D1, D0
MOVE      SR, (A2)
MOVE      D0, (A7)
MOVE      5555, D0
MOVE      FFFC, D1
MULS      D1, D2
MOVE      SR, (A7)
MOVE      D0, (A7)
NOP
STOP

```

NEG

```

NOP
MOVE      0000, D0
MOVE      0000, D3
MOVE      0000, D5
MOVE      D0, (A7)
MOVE      D3, (A7)
MOVE      D5, (A7)
MOVE      5555, D3
MOVE      AAAA, D5
NEG        D0
MOVE      SR, (A7)
MOVE      D0, (A7)
NEG        D3
MOVE      SR, (A7)
MOVE      D3, (A7)
NEG        D5
MOVE      SR, (A7)
MOVE      D5, (A7)
NOP
MOVE      1300, A6
MOVE      5555, (A6)
MOVE      0001, D0
MOVE      00AA, D3
MOVE      55555555, D5
MOVE      2700, SR
NEGX       D0
MOVE      SR, (A7)
MOVE      D3, (A7)
MOVE      2700, SR
NEGX       D5
MOVE      SR, (A7)

```

```

MOVE      D5, (A7)
MOVE      00FF, D0
MOVE      00AA, D3
MOVE      00000055, D5
MOVE      2710, SR
NEG        D0
MOVE      SR, (A7)
MOVE      D0, (A7)
MOVE      2710, SR
NEGX       D5
MOVE      SR, (A7)
MOVE      D5, (A7)
MOVE      2710, SR
NEGX       (A6)
MOVE      SR, (A7)
MOVE      (A6), (A7)
MOVE      2700, SR
NEGX       (A6)
MOVE      SR, (A7)
MOVE      (A6), (A7)
NOP
STOP

```

SUBI

NOP		MOVE	SR, (A ₇)
MOVE	AAAA, D ₀	MOVE	A ₀ , (A ₇)
MOVE	5555, D ₂	SUBQ	7, D ₂
MOVE	FFFF, D ₄	MOVE	SR, (A ₇)
MOVE	D ₀ , (A ₇)	MOVE	D ₂ , (A ₇)
MOVE	D ₂ , (A ₇)	MOVE	5555, D ₁
MOVE	D ₄ , (A ₇)	MOVE	AAAA, D ₀
SUBI	5555, D ₀	MOVE	2700, SR
MOVE	SR, (A ₇)	SUBX	D ₁ , D ₀
MOVE	D ₀ , (A ₇)	MOVE	SR, (A ₇)
SUBI	AAAA, D ₂	MOVE	D ₀ , (A ₇)
MOVE	SR, (A ₇)	MOVE	5555, D ₁
MOVE	D ₀ , (A ₇)	MOVE	AAAA, D ₀
SUBI	OFFF, D ₄	MOVE	2710, SR
MOVE	SR, (A ₇)	SUBX	D ₁ , D ₀
MOVE	D ₄ , (A ₇)	MOVE	SR, (A ₇)
MOVE	AAAAAAAA, D ₀	MOVE	D ₀ , (A ₇)
MOVE	55555555, D ₂	NOP	
SUBI	55555555, D ₀	STOP	
MOVE	SR, (A ₇)		
MOVE	D ₀ , (A ₇)		
SUBI	AAAAAAAA, D ₂		
MOVE	SR, (A ₇)		
MOVE	D ₂ , (A ₇)		
MOVE	AAAA, D ₀		
MOVE	5555, A ₀		
MOVE	0000, D ₂		
SUBQ	5, D ₀		
MOVE	SR, (A ₇)		
MOVE	D ₀ , (A ₇)		
SUBQ	5, A ₀		

AND

```

NOP
MOVE      AAAA, D0
MOVE      5555, D1
MOVE      FFFF, A0
MOVE      0000, D2
MOVE      1300, A6
MOVE      F0F0, (A6)
AND        D0, D1
MOVE      SR, (A7)
MOVE      D0, (A7)
MOVE      D1, (A7)
AND        (A6), D2
MOVE      SR, (A7)
MOVE      D2, (A7)
MOVE      5555, D0
MOVE      AAAA, A0
MOVE      1300, A6
MOVE      F0F0, (A6)
ANDI      0050, D0
MOVE      SR, (A7)
MOVE      D0, (A7)
ANDI      0050, (A6)
MOVE      SR, (A7)
NOP
STOP

```

OR

NOP
MOVE 1300, A₆
MOVE F0F0, (A₆)
MOVE AAAA, D₀
MOVE 2700, SR
OR D₀, (A₆)
MOVE SR, (A₇)
MOVE D₀, (A₇)
MOVE 5500, D₀
MOVE 0F00, D₁
OR D₀, D₁
MOVE SR, (A₇)
MOVE D₁, (A₇)
MOVE 0F0F, D₀
MOVE 0505, D₁
MOVE A0A0, (A₆)
ORI 0500, D₀
MOVE SR, (A₇)
MOVE D₀, (A₇)
ORI 0F, D₁
MOVE SR, (A₇)
MOVE D₁, (A₇)
ORI F0, (A₆)
MOVE SR, (A₇)
NOP
STOP

NOT

NOP	
MOVE	F0F0, D ₀
MOVE	1300, A ₆
MOVE	A0A0, (A ₆)
NOT	D ₀
MOVE	SR, (A ₇)
MOVE	D ₀ , (A ₇)
NOT	(A ₆)
MOVE	SR, (A ₇)
NOP	
MOVE	0001, D ₀
MOVE	0008, D ₁
MOVE	8000, D ₂
ASL	7, D ₀
MOVE	SR, (A ₇)
MOVE	D ₀ , (A ₇)
MOVE	0001, D ₀
ASL	D ₁ , 0
MOVE	SR, (A ₇)
MOVE	D ₀ , (A ₇)
ASR	D ₂ , 7
MOVE	SR, (A ₇)
MOVE	D ₂ , (A ₇)
MOVE	8000, D ₂
ASR	D ₂ , D ₁
MOVE	SR, (A ₇)
MOVE	D ₂ , (A ₇)
NOP	
MOVE	0001, D ₂
MOVE	8000, D ₄
MOVE	0008, D ₆

NOT (CONT)

LSL	7, D ₂	MOVE	2710, SR
MOVE	SR, (A ₇)	MOVE	8000, D ₁
MOVE	D ₂ , (A ₇)	ROR	D ₂ , D ₁
MOVE	0001, D ₂	MOVE	SR, (A ₇)
LSL	D ₆ , D ₂	MOVE	D ₁ , (A ₇)
MOVE	SR, (A ₇)	MOVE	0000, D ₀
MOVE	D ₂ , (A ₇)	MOVE	2710, SR
LSR	D ₄ , 7	ROXL	7, D ₀
MOVE	SR, (A ₇)	MOVE	SR, (A ₇)
MOVE	D ₄ , (A ₇)	MOVE	D ₀ , (A ₇)
MOVE	8000, D ₄	MOVE	0000, D ₀
LSR	D ₄ , D ₆	MOVE	2700, SR
MOVE	SR, (A ₇)	ROXL	D ₂ , D ₀
MOVE	D ₄ , (A ₇)	MOVE	SR, (A ₇)
NOP		MOVE	D ₀ , (A ₇)
MOVE	0001, D ₀	MOVE	0000, D ₁
MOVE	8000, D ₁	MOVE	2710, SR
MOVE	0008, D ₂	ROXR	7, D ₁
MOVE	2710, SR	MOVE	SR, (A ₇)
ROL	7, D ₀	MOVE	D ₁ , (A ₇)
MOVE	SR, (A ₇)	MOVE	0000, D ₁
MOVE	D ₀ , (A ₇)	MOVE	2700, SR
MOVE	2710, SR	ROXR	D ₂ , D ₁
MOVE	0001, D ₀	MOVE	SR, (A ₇)
ROL	D ₂ , D ₀	MOVE	D ₁ , (A ₇)
MOVE	SR, (A ₇)	NOP	
MOVE	D ₀ , (A ₇)	STOP	
MOVE	2700, SR		
ROR	7, D ₁		
MOVE	SR, (A ₇)		
MOVE	D ₁ , (A ₇)		

BTST

NOP		MOVE	SR, (A ₇)
MOVE	0880, D ₀	MOVE	D ₀ , (A ₇)
MOVE	2700, SR	BCLR	0002, D ₀
MOVE	0800, D ₁	MOVE	SR, (A ₇)
BTST	D ₀ , 0007	MOVE	D ₀ , (A ₇)
MOVE	SR, (A ₇)	MOVE	0008, D ₀
BTST	D ₀ , 0001	MOVE	0000, D ₁
MOVE	SR, (A ₇)	MOVE	0004, D ₂
BTST	D ₀ , D ₁	MOVE	2700, SR
MOVE	SR, (A ₇)	BCHG	D ₀ , D ₁
NOP		MOVE	SR, (A ₇)
MOVE	0007, D ₀	MOVE	D ₁ , (A ₇)
MOVE	0000, D ₂	BCHG	D ₂ , D ₁
MOVE	0006, D ₄	MOVE	SR, (A ₇)
MOVE	2700, SR	MOVE	D ₁ , (A ₇)
BSET	D ₄ , D ₂	BCHG	0002, D ₂
MOVE	SR, (A ₇)	MOVE	SR, (A ₇)
MOVE	D ₂ , (A ₇)	MOVE	D ₂ , (A ₇)
BSET	D ₁ , D ₂	NOP	
MOVE	SR, (A ₇)	STOP	
MOVE	D ₂ , (A ₇)		
BSET	0001, D ₂		
MOVE	SR, (A ₇)		
MOVE	D ₂ , (A ₇)		
MOVE	00F0, D ₀		
MOVE	0008, D ₁		
MOVE	0004, D ₂		
BCLR	D ₁ , D ₀		
MOVE	SR, (A ₇)		
MOVE	D ₀ , (A ₇)		
BCLR	D ₂ , D ₀		

BCD

NOP		MOVE	D ₁ , (A ₇)
MOVE	0000, D ₁	MOVE	2710, SR
MOVE	0012, D ₂	SBCD	D ₃ , D ₂
MOVE	0022, D ₃	MOVE	SR, (A ₇)
MOVE	2700, SR	MOVE	D ₂ , (A ₇)
MOVE	1300, A ₆	MOVE	2700, SR
MOVE	0012, (A ₆)	MOVE	1302, A ₆
MOVE	1350, A ₅	MOVE	1352, A ₅
MOVE	0012, (A ₅)	SBCD	(A ₅), (A ₆)
ABCD	D ₂ , D ₁	MOVE	SR, A ₇
MOVE	SR, (A ₇)	MOVE	0000, D ₁
MOVE	D ₁ , (A ₇)	MOVE	FFFF, SR
MOVE	2710, SR	MOVE	2700, SR
ABCD	D ₃ , D ₂	NBCD	D ₂
MOVE	SR, (A ₇)	MOVE	SR, (A ₇)
MOVE	D ₂ , (A ₇)	MOVE	D ₂ , (A ₇)
MOVE	2700, SR	MOVE	2710, (A ₇)
MOVE	1302, A ₆	NBCD	D ₁
MOVE	1352, A ₅	MOVE	SR, (A ₇)
ABCD	(A ₅), (A ₆)	MOVE	D ₁ , (A ₇)
MOVE	SR, (A ₇)	NOP	
MOVE	0000, D ₁	STOP	
MOVE	0012, D ₂		
MOVE	0022, D ₃		
MOVE	2700, SR		
MOVE	1300, A ₆		
MOVE	0012, (A ₆)		
MOVE	1350, A ₅		
MOVE	0012, (A ₅)		
SBCD	D ₂ , D ₁		
MOVE	SR, (A ₇)		

PGCNT

100E	NOP
	MOVE 000F, D ₀
	MOVE 00F0, D ₁
	MOVE 000F, D ₂
	CMP D ₁ , D ₀
	BRAcc ≠, 1050
1050	NOP
	MOVE 000F, D ₁
	CMP D ₁ , D ₀
	DBcc =, 1200
1200	NOP
	MOVE D ₂ , (A ₇)
	MOVE 0000, D ₁
	SETcc ≠, D ₂
	MOVE D ₂ , (A ₇)
	BRA 1250
1250	NOP
	BSR 1300
	NOP
	BSR 1350
1300	NOP
	MOVE 1450, A ₆
	RTS
1350	NOP
	MOVE SR, (A ₇)
	RTR
	NOP
	STOP

ADDA

NOP		MOVE	SR, (A ₇)
MOVE	00000000, A ₁	MOVE	A ₁ , (A ₇)
MOVE	000000F0, A ₂	NOP	
MOVE	1300, A ₆	STOP	
MOVE	0000000F, (A ₆)		
MOVE	2700, SR		
ADDA	A ₂ , A ₁		
MOVE	SR, (A ₇)		
MOVE	A ₁ , (A ₇)		
MOVE	00000A0A, A ₁		
ADDA	(A ₆), A ₁		
MOVE	SR, (A ₇)		
MOVE	A ₁ , (A ₇)		
MOVE	00000000, A ₁		
MOVE	00000FF0, A ₂		
MOVE	00000FF0, A ₃		
MOVE	2700, SR		
CMPA	A ₁ , A ₂		
MOVE	SR, (A ₇)		
MOVE	A ₂ , (A ₇)		
CMP	A ₃ , A ₂		
MOVE	SR, (A ₇)		
MOVE	A ₂ , (A ₇)		
MOVE	00000A0A, A ₁		
MOVE	00000A00, A ₂		
MOVE	1300, A ₆		
MOVE	0000000A, (A ₆)		
SUBA	A ₂ , A ₁		
MOVE	SR, (A ₇)		
MOVE	A ₁ , (A ₇)		
SUBA	(A ₆), A ₁		

SYSTEM CONTROL

NOP		MOVE	0010, CCR
MOVE	00000A0A, A ₁		SR, (A ₇)
	2700, SR	NOP	
	USP A ₁ T	NOP	
	SR, (A ₇)	NOP	
	00G00000, A ₁	MOVE	SR, (A ₇)
	USP A ₁ E	STOP	
	SR, (A ₇)		
	A ₁ , (A ₇)		
	2700, SR		
	SR, (A ₇)		
	2701, SR		
	SR, (A ₇)		
	2702, (A ₇)		
	SR, (A ₇)		
	2704, SR		
	SR, (A ₇)		
	2708, SR		
	SR, (A ₇)		
	270A, SR		
	SR, (A ₇)		
	0000, CCR		
	SR, (A ₇)		
	0001, CCR		
	SR, (A ₇)		
	0002, CCR		
	SR, (A ₇)		
	0004, CCR		
	SR, (A ₇)		
	0008, CCR		
	SR, (A ₇)		

CHK

```

NOP
MOVE      1000, D3
MOVE      0500, D1
MOVE      2000, D2
MOVE      2700, SR
CHK        D1, D3
NOP
NOP
MOVE      2700, SR
NOP
CHK        D2, D3
NOP
STOP

```

DIVS

```

NOP
MOVE      AAAA, D1
MOVE      0002, D2
MOVE      2700, SR
DIV        D0, D1
MOVE      AAAA, D1
MOVE      FFFFFFFE, D0
MOVE      2700, SR
DIV        D0, D1
NOP
STOP

```

TAS

NOP	
MOVE	1300, A ₆
MOVE	0000, D ₀
MOVE	00F0, D ₂
MOVE	2700, SR
TAS	D ₀
MOVE	SR, (A ₇)
MOVE	D ₀ , (A ₇)
MOVE	2700, (A ₇)
TAS	D ₂
MOVE	SR, (A ₇)
MOVE	D ₂ , (A ₇)
MOVE	AAAA, (A ₆)
MOVE	2700, SR
TAS	(A ₆)
MOVE	SR, (A ₇)
MOVE	(A ₆), (A ₇)
MOVE	0000, D ₀
MOVE	F000, D ₂
MOVE	2700, SR
TST	D ₀
MOVE	SR, (A ₇)
MOVE	2700, SR
TST	D ₂
MOVE	SR, (A ₇)
NOP	
STOP	

APPENDIX B

DEVICE NUMBER: 1 AT 25 DEG. CENT.

***** MC68000 DC PARAMETERS *****

1: ICC TEST (FREQ = 6MHZ) VCC = 5.5 VOLT	CHAN 8 = 161.719	MA
2: VOL : A23-1, FCP (0.5V @ 3.2MA):	CHAN 9 = .169501	V
	CHAN 9 = .16	V
	CHAN 10 = .187501	V
	CHAN 11 = .187501	V
	CHAN 12 = .194001	V
	CHAN 13 = .1935	V
	CHAN 14 = .1965	V
	CHAN 15 = .196	V
	CHAN 16 = .202501	V
	CHAN 17 = .202501	V
	CHAN 18 = .211501	V
	CHAN 19 = .210501	V
	CHAN 20 = .2145	V
	CHAN 21 = .220001	V
	CHAN 22 = .223501	V
	CHAN 23 = .229	V
	CHAN 24 = .224501	V
	CHAN 25 = .233501	V
	CHAN 26 = .2345	V
	CHAN 27 = .239	V
	CHAN 28 = .239	V
	CHAN 29 = .242501	V
	CHAN 30 = .2375	V
	CHAN 31 = .2375	V
3: VOL : FC1 (0.5V @ 3.2MA):	CHAN 7 = .169501	V
4: VOL : AS,DS,R-W (0.5V @ 3.3MA):	CHAN 60 = .285501	V
	CHAN 61 = .283301	V
	CHAN 62 = .2135	V
	CHAN 63 = .279001	V
5: VOL : DATA0 : (0.5V @ 5.3 MA):	CHAN 2 = .257501	V
6: VOL : DATA1 : (0.5V @ 5.3 MA):	CHAN 2 = .267	V
7: VOL : DATA2 : (0.5V @ 5.3 MA):	CHAN 2 = .265501	V
8: VOL : DATA3 : (0.5V @ 5.3 MA):	CHAN 2 = .2715	V
9: VOL : DATA4 : (0.5V @ 5.3 MA):	CHAN 2 = .2725	V
10: VOL : DATA5 : (0.5V @ 5.3 MA):	CHAN 2 = .2765	V
11: VOL : DATA6 : (0.5V @ 5.3 MA):	CHAN 2 = .2765	V
12: VOL : DATA7 : (0.5V @ 5.3 MA):	CHAN 2 = .282001	V
13: VOL : DATA8 : (0.5V @ 5.3 MA):	CHAN 2 = .284	V
14: VOL : DATA9 : (0.5V @ 5.3 MA):	CHAN 2 = .287001	V
15: VOL : DATA10 : (0.5V @ 5.3 MA):	CHAN 2 = .2875	V

16: VOL : DATA11 : (0.5V @ 5.3 MA) :	CHAN 2 = .292001	V
17: VOL : DATA12 : (0.5V @ 5.3 MA) :	CHAN 2 = .2895	V
18: VOL : DATA13 : (0.5V @ 5.3 MA) :	CHAN 2 = .292501	V
19: VOL : DATA14 : (0.5V @ 5.3 MA) :	CHAN 2 = .290501	V
20: VOL : DATA15 : (0.5V @ 5.3 MA) :	CHAN 2 = .307001	V
21: VOL : BG (0.5V @ 3.2MA) :	CHAN 57 = .154001	V
22: VOL : E (0.5V @ 3.2MA) :	CHAN 53 = .760201E-01	V
23: VOL : VMA (0.5V @ 5.3 MA) :	CHAN 52 = .146	V
24: VOL : FC2 (0.5V @ 3.2MA) :	CHAN 8 = .160501	V
25: VOL : RESET (0.5V @ 5MA) :	CHAN 2 = .211001	V
26: VOL : HALT (0.5V @ 1.6MA) :	CHAN 54 = .203	V
27: VOM : ADR,FC240,BG (2.4V @ 400UA) :	CHAN 6 = 3.35501	V
	CHAN 8 = 3.34501	V
	CHAN 9 = 3.36501	V
	CHAN 10 = 3.35001	V
	CHAN 11 = 3.36501	V
	CHAN 12 = 3.35501	V
	CHAN 13 = 3.38001	V
	CHAN 14 = 3.36501	V
	CHAN 15 = 3.39001	V
	CHAN 16 = 3.38501	V
	CHAN 17 = 3.39001	V
	CHAN 18 = 3.39001	V
	CHAN 19 = 3.39501	V
	CHAN 20 = 3.40001	V
	CHAN 21 = 3.42501	V
	CHAN 22 = 3.41001	V
	CHAN 23 = 3.42501	V
	CHAN 24 = 3.40001	V
	CHAN 25 = 3.40501	V
	CHAN 26 = 3.37501	V
	CHAN 27 = 3.38501	V
	CHAN 28 = 3.40001	V
	CHAN 29 = 3.44001	V
	CHAN 30 = 3.43501	V
	CHAN 31 = 3.45501	V
	CHAN 57 = 3.36501	V
28: VOM : DATA1 : (2.4V @ 400 UA) :	CHAN 2 = 3.33001	V
29: VOM : DATA1 : (2.4V @ 400 UA) :	CHAN 2 = 3.33001	V
30: VOM : DATA2 : (2.4V @ 400 UA) :	CHAN 2 = 3.32501	V
31: VOM : DATA3 : (2.4V @ 400 UA) :	CHAN 2 = 3.33001	V
32: VOM : DATA4 : (2.4V @ 400 UA) :	CHAN 2 = 3.32501	V
33: VOM : DATA5 : (2.4V @ 400 UA) :	CHAN 2 = 3.32501	V
34: VOM : DATA6 : (2.4V @ 400 UA) :	CHAN 2 = 3.33501	V

35: VOM : DATA7 : (2.4V @ 400 UA) :	CHAN 2 = 3.34501	V
36: VOM : DATA8 : (2.4V @ 400 UA) :	CHAN 2 = 3.35501	V
37: VOM : DATA9 : (2.4V @ 400 UA) :	CHAN 2 = 3.36001	V
38: VOM : DATA10 : (2.4V @ 400 UA) :	CHAN 2 = 3.37501	V
39: VOM : DATA11 : (2.4V @ 400 UA) :	CHAN 2 = 3.37501	V
40: VOM : DATA12 : (2.4V @ 400 UA) :	CHAN 2 = 3.40001	V
41: VOM : DATA13 : (2.4V @ 400 UA) :	CHAN 2 = 3.37501	V
42: VOM : DATA14 : (2.4V @ 400 UA) :	CHAN 2 = 3.39001	V
43: VOM : DATA15 : (2.4V @ 400 UA) :	CHAN 2 = 3.36501	V
44: VOM : AS, UDS, LDS, WR, FC1 (2.4V @ 400UA) :	CHAN 7 = 3.35001	V
	CHAN 60 = 3.37001	V
	CHAN 61 = 3.36501	V
	CHAN 62 = 3.39501	V
	CHAN 63 = 3.38501	V
45: VOM : E, VMA (2.4V @ 400UA) :	CHAN 52 = .250001E-01	V FAIL
	CHAN 53 = 3.35501	V
46: IIL : ALL INPUTS (1.0UA @ 2.4 VOLTS) :	CHAN 4 = .1E-02	UA
	CHAN 5 = -.250001E-02	UA
	CHAN 32 = .200001E-02	UA
	CHAN 33 = -.15E-02	UA
	CHAN 34 = .200001E-02	UA
	CHAN 35 = -.250001E-02	UA
	CHAN 36 = -.500001E-03	UA
	CHAN 37 = .350001E-02	UA
	CHAN 38 = -.250001E-02	UA
	CHAN 39 = .300001E-02	UA
	CHAN 40 = .1E-02	UA
	CHAN 41 = -.350001E-02	UA
	CHAN 42 = .200001E-02	UA
	CHAN 43 = -.300001E-02	UA
	CHAN 44 = -.500001E-03	UA
	CHAN 45 = .200001E-02	UA
	CHAN 46 = -.350001E-02	UA
	CHAN 47 = .250001E-02	UA
	CHAN 48 = -.250001E-02	UA
	CHAN 49 = .15E-02	UA
	CHAN 50 = -.300001E-02	UA
	CHAN 51 = .15E-02	UA
	CHAN 54 = .500001E-03	UA
	CHAN 55 = -.350001E-02	UA
	CHAN 56 = .200001E-02	UA
	CHAN 58 = -.350001E-02	UA
	CHAN 59 = .200001E-02	UA
47: IIL : ALL INPUTS (1.0UA @ 0.4 VOLTS) :	CHAN 4 = .500001E-03	UA
	CHAN 5 = -.250001E-02	UA
	CHAN 32 = .250001E-02	UA
	CHAN 33 = -.300001E-02	UA
	CHAN 34 = .200001E-02	UA
	CHAN 35 = .500001E-03	UA
	CHAN 36 = -.450001E-02	UA
	CHAN 37 = .300001E-02	UA

CHAN 38 = -1.250001E-02 UA
 CHAN 39 = -1.250001E-02 UA
 CHAN 40 = -1.1E-02 UA
 CHAN 41 = -1.300001E-02 UA
 CHAN 42 = -1.1E-02 UA
 CHAN 43 = -1.300001E-02 UA
 CHAN 44 = -1.300001E-02 UA
 CHAN 45 = -1.250001E-02 UA
 CHAN 46 = -1.200001E-02 UA
 CHAN 47 = -1.300001E-02 UA
 CHAN 48 = -1.200001E-02 UA
 CHAN 49 = -1.350001E-02 UA
 CHAN 50 = -1.300001E-02 UA
 CHAN 51 = -1.300001E-02 UA
 CHAN 52 = -1.250001E-02 UA
 CHAN 53 = -1.300001E-02 UA
 CHAN 54 = -1.400001E-02 UA
 CHAN 55 = -1.200001E-02 UA
 CHAN 56 = -1.10E-02 UA

481 10HZ : ALL OUTPUTS (7 UA @ 2.4VOLTS):
 CHAN 6 = -1.100001E-02 UA
 CHAN 7 = -1.100001E-02 UA
 CHAN 8 = -1.900001E-03 UA
 CHAN 9 = -1.900001E-03 UA
 CHAN 10 = -1.100001E-02 UA
 CHAN 11 = -1.1E-02 UA
 CHAN 12 = -1.900001E-03 UA
 CHAN 13 = -1.900001E-03 UA
 CHAN 14 = -1.100001E-02 UA
 CHAN 15 = -1.10E-02 UA
 CHAN 16 = -1.10E-02 UA
 CHAN 17 = -1.900001E-03 UA
 CHAN 18 = -1.900001E-03 UA
 CHAN 19 = -1.100001E-02 UA
 CHAN 20 = -1.10E-02 UA
 CHAN 21 = -1.10E-02 UA
 CHAN 22 = -1.900001E-03 UA
 CHAN 23 = -1.100001E-02 UA
 CHAN 24 = -1.900001E-03 UA
 CHAN 25 = -1.900001E-03 UA
 CHAN 26 = -1.1E-02 UA
 CHAN 27 = -1.900001E-03 UA
 CHAN 28 = -1.900001E-03 UA
 CHAN 29 = -1.100001E-02 UA
 CHAN 30 = -1.900001E-03 UA
 CHAN 31 = -1.100001E-02 UA
 CHAN 32 = -1.100001E-02 UA
 CHAN 33 = -1.900001E-03 UA
 CHAN 34 = -1.900001E-03 UA
 CHAN 35 = -1.900001E-03 UA
 CHAN 36 = -1.10E-02 UA
 CHAN 37 = -1.900001E-03 UA
 CHAN 38 = -1.900001E-03 UA
 CHAN 39 = -1.100001E-02 UA
 CHAN 40 = -1.1E-02 UA
 CHAN 41 = -1.10E-02 UA
 CHAN 42 = -1.900001E-03 UA
 CHAN 43 = -1.100001E-02 UA
 CHAN 44 = -1.100001E-02 UA
 CHAN 45 = -1.100001E-02 UA
 CHAN 46 = -1.900001E-03 UA
 CHAN 47 = -1.100001E-02 UA
 CHAN 57 = -1.100001E-03 UA

	CHAN 11	#	53	NS
	CHAN 12	#	59	NS
	CHAN 13	#	59	NS
	CHAN 14	#	63	NS
	CHAN 15	#	64	NS
	CHAN 16	#	54	NS
	CHAN 17	#	49	NS
	CHAN 18	#	60	NS
	CHAN 19	#	59	NS
	CHAN 20	#	56	NS
	CHAN 21	#	50	NS
	CHAN 22	#	52	NS
	CHAN 23	#	61	NS
	CHAN 24	#	54	NS
	CHAN 25	#	51	NS
	CHAN 26	#	64	NS
	CHAN 27	#	65	NS
	CHAN 28	#	60	NS
	CHAN 29	#	62	NS
	CHAN 30	#	63	NS
	CHAN 31	#	59	NS
273:CLK H TO ADDR. INVALID: (VDM & VOL)=2.5V:	CHAN 9	#	59	NS
	CHAN 10	#	58	NS
	CHAN 11	#	57	NS
	CHAN 12	#	53	NS
	CHAN 13	#	51	NS
	CHAN 14	#	65	NS
	CHAN 15	#	64	NS
	CHAN 16	#	54	NS
	CHAN 17	#	49	NS
	CHAN 18	#	60	NS
	CHAN 19	#	59	NS
	CHAN 20	#	57	NS
	CHAN 21	#	58	NS
	CHAN 22	#	60	NS
	CHAN 23	#	61	NS
	CHAN 24	#	54	NS
	CHAN 25	#	51	NS
	CHAN 26	#	64	NS
	CHAN 27	#	65	NS
	CHAN 28	#	60	NS
	CHAN 29	#	62	NS
	CHAN 30	#	63	NS
	CHAN 31	#	58	NS
274:CLK HIGH TO AS,OS T.S. (VDM = 2.5V):	CHAN 60	#	47	NS
	CHAN 61	#	35	NS
	CHAN 63	#	49	NS
275:CLK HIGH TO R-W T.S. (VDM=0.5V) :	CHAN 62	#	22	NS
276:CLK HIGH TO DATA T.S. ITCHAZ: (100NS MAX):	CHAN 32	#	58	NS
	CHAN 33	#	52	NS
	CHAN 34	#	51	NS
	CHAN 35	#	48	NS
	CHAN 36	#	46	NS
	CHAN 37	#	47	NS
	CHAN 38	#	53	NS
	CHAN 39	#	54	NS
	CHAN 40	#	55	NS
	CHAN 41	#	44	NS
	CHAN 42	#	49	NS
	CHAN 43	#	51	NS
	CHAN 44	#	48	NS
	CHAN 45	#	51	NS
	CHAN 46	#	62	NS
	CHAN 47	#	53	NS

CHAN 50 = -.167601E-02 A
 CHAN 51 = -.175E-02 A
 CHAN 52 = -.147601E-02 A
 CHAN 53 = -.147601E-02 A

49: IDLZ : ALL OUTPUTS (7 UA @ 0.4 VOLTS):

CHAN 5	=	-.17371E-02	A
CHAN 7	=	-.950001E-03	UA
CHAN 8	=	-.950001E-03	UA
CHAN 9	=	-.100001E-02	UA
CHAN 10	=	-.950001E-03	UA
CHAN 11	=	-.100001E-02	UA
CHAN 12	=	-.950001E-03	UA
CHAN 13	=	-.950001E-03	UA
CHAN 14	=	-.100001E-02	UA
CHAN 15	=	-.105E-02	UA
CHAN 16	=	-.100001E-02	UA
CHAN 17	=	-.100001E-02	UA
CHAN 18	=	-.100001E-02	UA
CHAN 19	=	-.105E-02	UA
CHAN 20	=	-.100001E-02	UA
CHAN 21	=	-.850001E-03	UA
CHAN 22	=	-.950001E-03	UA
CHAN 23	=	-.100001E-02	UA
CHAN 24	=	-.100001E-02	UA
CHAN 25	=	-.950001E-03	UA
CHAN 26	=	-.105E-02	UA
CHAN 27	=	-.950001E-03	UA
CHAN 28	=	-.950001E-03	UA
CHAN 29	=	-.105E-02	UA
CHAN 30	=	-.100001E-02	UA
CHAN 31	=	-.100001E-02	UA
CHAN 32	=	-.900001E-03	UA
CHAN 33	=	-.100001E-02	UA
CHAN 34	=	-.100001E-02	UA
CHAN 35	=	-.900001E-03	UA
CHAN 36	=	-.950001E-03	UA
CHAN 37	=	-.100001E-02	UA
CHAN 38	=	-.105E-02	UA
CHAN 39	=	-.900001E-03	UA
CHAN 40	=	-.100001E-02	UA
CHAN 41	=	-.850001E-03	UA
CHAN 42	=	-.900001E-03	UA
CHAN 43	=	-.11E-02	UA
CHAN 44	=	-.100001E-02	UA
CHAN 45	=	-.950001E-03	UA
CHAN 46	=	-.900001E-03	UA
CHAN 47	=	-.100001E-02	UA
CHAN 48	=	-.11E-02	UA
CHAN 49	=	-.100001E-02	UA
CHAN 51	=	-.900001E-03	UA
CHAN 52	=	-.850001E-03	UA
CHAN 53	=	-.100001E-02	UA

50: INPUT LOW TEST (ALL INPUTS) : PVCC = 4.5 IIL MAX = 1 V
 51: INPUT HIGH TEST (ALL INPUTS) : PVCC = 4.5 IIL MIN = 1.55224 V

81:	5,5	PASS
**** INTEGER ARITHMETIC INSTRUCTIONS ****		
82: ADD, ADD INSTRUCTION TEST	4,5	PASS
83:	5	PASS
84:	5,5	PASS
85: ADDX INST. TEST	4,5	PASS
86:	5	PASS
87:	5,5	PASS
88: CLR INST. TEST	4,5	PASS
89:	5	PASS
90:	5,5	PASS
91: CMP, CMPI, CMPM INST. TEST	4,5	PASS
92:	5	PASS
93:	5,5	PASS
94: DIV, DIVS INST. TEST	4,5	PASS
95:	5	PASS
96:	5,5	PASS
97: EXT INST. TEST	4,5	PASS
98:	5	PASS
99:	5,5	PASS
100: MULU AND Muls INST. TEST	4,5	PASS
101:	5	PASS
102:	5,5	PASS
103: NEG, NEGX INST. TEST	4,5	PASS
104:	5	PASS
105:	5,5	PASS
106: SUB, SUBI, SUBQ, SUBX INST. TEST	4,5	PASS
107:	5	PASS
108:	5,5	PASS
109:	5	PASS
109: TAS, TST INST. TEST	4,5	PASS
110:	5	PASS

AD-A111 491

IBM FEDERAL SYSTEMS DIV MANASSAS VA

F/G 9/2

ELECTRICAL CHARACTERIZATION OF THE 68000 MICROPROCESSOR.(U)

DEC 81 J D BAILEY

F30602-80-C-0119

UNCLASSIFIED

RADC-TR-81-350

NL

2 OF 2

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2.2



2.0



1.8

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1111	5,5	PASS
**** SHIFT, ROTATE, AND LOGICAL INSTRUCTIONS ****		
1121 AND, ANDI INST. TEST	4,5	PASS
1131	5	PASS
1141	5,5	PASS
1151 OR, ORI, EOR INST. TEST	4,5	PASS
1161	5	PASS
1171	5,5	PASS
1181 NOT, SHIFT & ROTATE INST. TEST	4,5	PASS
1191	5	PASS
1201	5,5	PASS
**** BIT MANIPULATION INSTRUCTIONS ****		
1211 BIT(TST, SET, CLR, CHG) INST. TEST	4,5	PASS
1221	5	PASS
1231	5,5	PASS
**** BCD INSTRUCTIONS		
1241 BCD (ADD, SUB, NEG) INST. TEST	4,5	PASS
1251	5	PASS
1261	5,5	PASS
**** PROGRAM AND SYSTEM, CONTROL INSTRUCTIONS ****		
1271 BRANCH, JMP AND RET INST. TEST	4,5	PASS
1281	5	PASS
1291	5,5	PASS
1301 ADDA, SUBA, CMPA INST. TEST	4,5	PASS
1311	5	PASS
1321	5,5	PASS
1331 MUSEP, MSR, MCCR INST. TEST	4,5	PASS
1341	5	PASS
1351	5,5	PASS
1361 TRAP, TRAPV INST. TEST	4,5	PASS
1371	5	PASS
1381	5,5	PASS
1391 MC68000 INSTRUCTION DECODE VERIFICATION @ 2.85MHZ		
**** DATA MOVE INSTRUCTIONS ****		
1391 EXG INST. TEST	4,5	PASS

1401	5	PASS
1411	5.5	PASS
1421 LEA INST. TEST	4.5	PASS
1431	5	PASS
1441	5.5	PASS
1451 PEA INST. TEST	4.5	PASS
1461	5	PASS
1471	5.5	PASS
1481 LINK,UNLINK INST. TEST	4.5	PASS
1491	5	PASS
1501	5.5	PASS
1511 MOVE INST. TEST	4.5	PASS
1521	5	PASS
1531	5.5	PASS
1541 MOVEM INST. TEST	4.5	PASS
1551	5	PASS
1561	5.5	PASS
1571 MOVEP INST. TEST	4.5	PASS
1581	5	PASS
1591	5.5	PASS
1601 MOVEA INST. TEST	4.5	PASS
1611	5	PASS
1621	5.5	PASS
1631 MOVEQ INST. TEST	4.5	PASS
1641	5	PASS
1651	5.5	PASS
1661 SWAP INST. TEST	4.5	PASS
1671	5	PASS
1681	5.5	PASS
**** INTEGER ARITHMETIC INSTRUCTIONS ****		
1691 ADD,ADDQ INSTRUCTION TEST	4.5	PASS
1701	5	PASS

1711	5.5	PASS
1721 ADDX INST. TEST	4.5	PASS
1731	5	PASS
1741	5.5	PASS
1751 CLR INST. TEST	4.5	PASS
1761	5	PASS
1771	5.5	PASS
1781 CMP,CMPI,CMPL INST. TEST	4.5	PASS
1791	5	PASS
1801	5.5	PASS
1811 DIV,DIVS INST. TEST	4.5	PASS
1821	5	PASS
1831	5.5	PASS
1841 EXT INST. TEST	4.5	PASS
1851	5	PASS
1861	5.5	PASS
1871 MULL AND MULLS INST. TEST	4.5	PASS
1881	5	PASS
1891	5.5	PASS
1901 NEG,NEGX INST. TEST	4.5	PASS
1911	5	PASS
1921	5.5	PASS
1931 SUB,SUBI,SUBQ,SUBX INST. TEST	4.5	PASS
1941	5	PASS
1951	5.5	PASS
1961		
1961 TAB,TST INST. TEST	4.5	PASS
1971	5	PASS
1981	5.5	PASS
**** SHIFT,ROTATE,AND LOGICAL INSTRUCTIONS ****		
1991 AND,ANDI INST. TEST	4.5	PASS
2001	5	PASS

201:	5,5	PASS
202: OR, ORI, EOR INST. TEST	4,5	PASS
203:	5	PASS
204:	5,5	PASS
205: NOT, SHIFT & ROTATE INST. TEST	4,5	PASS
206:	5	PASS
207:	5,5	PASS
**** BIT MANIPULATION INSTRUCTIONS ****		
208: BIT(TST, SET, CLR, CNG) INST. TEST	4,5	PASS
209:	5	PASS
210:	5,5	PASS
**** BCD INSTRUCTIONS		
211: BCD (ADD, SUB, NEG) INST. TEST	4,5	PASS
212:	5	PASS
213:	5,5	PASS
**** PROGRAM AND SYSTEM, CONTROL INSTRUCTIONS ****		
214: BRANCH, JMP AND RET INST. TEST	4,5	PASS
215:	5	PASS
216:	5,5	PASS
217: ADDA, SUBA, CMPA INST. TEST	4,5	PASS
218:	5	PASS
219:	5,5	PASS
220: MUSB, MSB, MCCR INST. TEST	4,5	PASS
221:	5	PASS
222:	5,5	PASS
223: TRAP, TRAPV INST. TEST	4,5	PASS
224:	5	PASS
225:	5,5	PASS

DEVICE NUMBER: 1 AT 25 DEG. CENT.

**** FMAX TEST ***

2261 FMAX TEST # 4MHZ	4.5	PASS
2271	5	PASS
2281	5.5	PASS
2291 FMAX TEST # 5.88MHZ	4.5	PASS
2301	5	PASS
2311	5.5	PASS
2321 FMAX TEST # 7.14MHZ	4.5	PASS
2331	5	PASS
2341	5.5	PASS
2351 FMAX TEST # 7.7MHZ	4.5	PASS
2361	5	PASS
2371	5.5	PASS
2381 FMAX TEST # 8.3MHZ	4.5	PASS
2391	5	PASS
2401	5.5	PASS

DEVICE NUMBER: 1 AT 25 DEG. CENT.

***** MC68000 AC PERFORMANCE TESTS *****

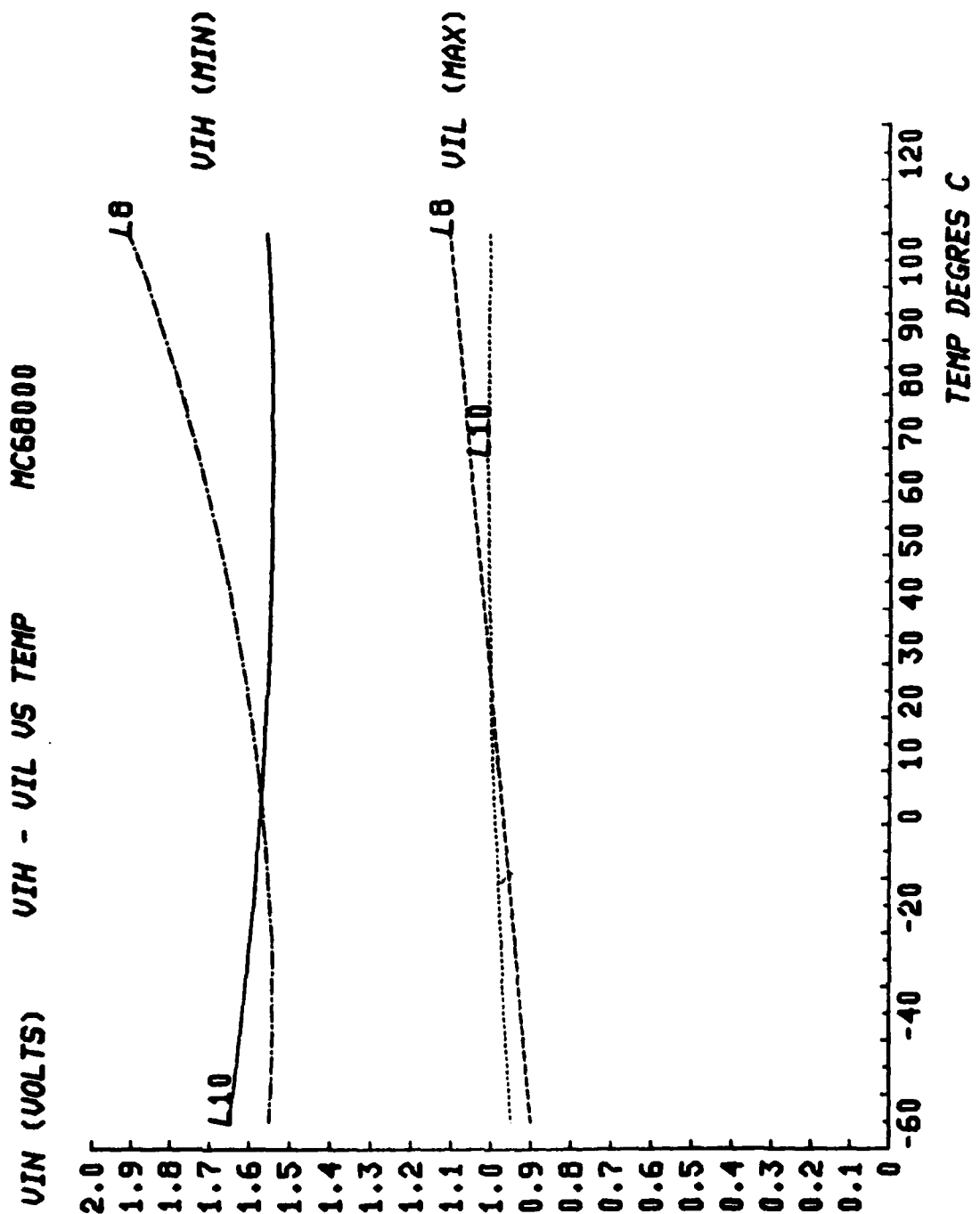
ALL SPECIFICATIONS REFLECT A 6 MHZ DEVICE

241: DIN TO CLK LOW (TSET): TDICL (25NS MIN):	CHAN 62 = 2	NS
242: DIN TO CLK LOW (THOLD): THDICL :	CHAN 62 = 0	NS
243: DTACK TO CLK LOW (TSET): TSDTCL (25NS MIN):	CHAN 62 = 0	NS
244: BR TO CLA LOW (TSET): TSBRL :	CHAN 57 = 2	NS
245: BR TO CLK LOW (THOLD): THBRL :	CHAN 57 = 2	NS
246: BGACK TO CLK LOW (TSET): TSBGCL :	CHAN 57 = -1	NS
247: BGACK TO CLK LOW	CHAN 57 = 0	NS
248: VPA TO CLK LOW (TSET): TSVACL :	CHAN 52 = -5	NS
249: VPA TO CLK LOW (THOLD): THVACL :	CHAN 52 = -3	NS
250: BERR TO CLK LOW (TSET): TSBRL :	CHAN 62 = 3	NS
251: BERR TO CLK LOW (THOLD): THBRL :	CHAN 62 = 4	NS
252: CLK WIDTH LOW : TCL (75NS MIN):	CHAN 32 = -22 CHAN 33 = -22 CHAN 34 = -22 CHAN 35 = -22	NS NS NS NS
253: CLK WIDTH HIGH : TCH (75NS MIN):	CHAN 32 = 42 CHAN 33 = 41 CHAN 34 = 41 CHAN 35 = 41	NS NS NS NS
254: CLK HIGH TO FC VALID : TCLAV (80NS MAX):	CHAN 6 = 39 CHAN 7 = 34	NS NS
255: CLK HIGH TO AS LOW (MIN): TCHSLX (20NS MIN)	CHAN 63 = 33	NS
256: CLK HIGH TO AS LOW (MAX): TCHSLN (70NS MAX):	CHAN 63 = 40	NS
257: CLK HIGH TO DS LOW (MIN): TCHSLX (20NS MIN)	CHAN 60 = 31 CHAN 61 = 29	NS NS
258: CLK HIGH TO DS LOW (MAX): TCHSLN (70NS MAX):	CHAN 60 = 37 CHAN 61 = 34	NS NS
259: CLK LOW TO AS HIGH: TCLSH (80NS MAX):	CHAN 63 = 41	NS
260: CLK LOW TO DS HIGH: TCLSH (80NS MAX):	CHAN 60 = 40 CHAN 61 = 40	NS NS
261: CLK H TO R-W H (MAX): TCHRH (80NS MAX):	CHAN 62 = 25	NS

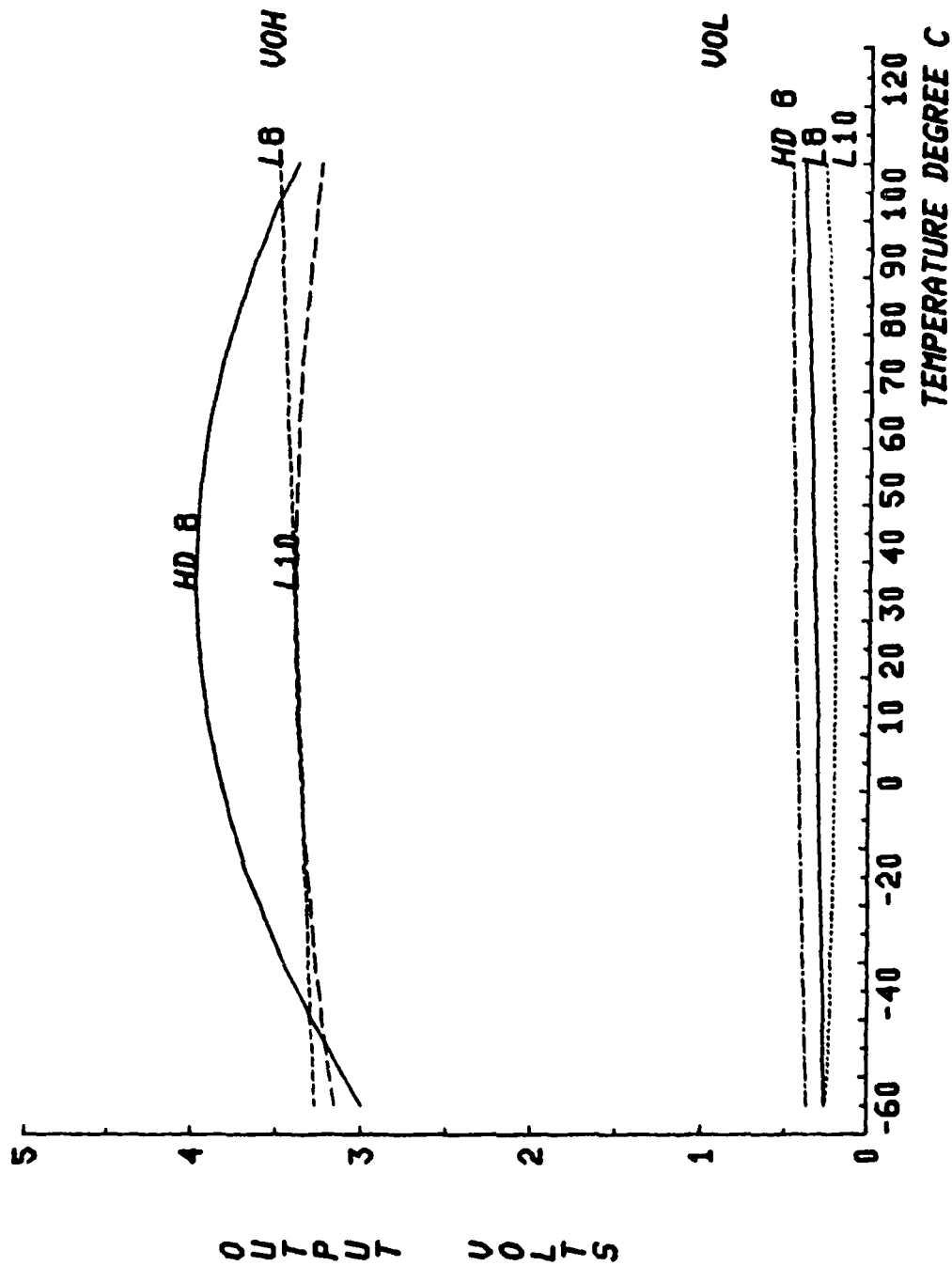
262: CLK H TO R-W H (MIN): TCHRH (20NS MIN):	CHAN 62 = 15	NS
263: CLK HIGH TO R-W LOW: TCHRL (60NS MAX):	CHAN 62 = 19	NS
264: CLK LOW TO DOUT VALID: TCLKO (80NS MAX):	CHAN 32 = 35	NS
	CHAN 33 = 34	NS
	CHAN 34 = 36	NS
	CHAN 35 = 37	NS
	CHAN 36 = 36	NS
	CHAN 37 = 34	NS
	CHAN 38 = 33	NS
	CHAN 39 = 36	NS
	CHAN 40 = 36	NS
	CHAN 41 = 33	NS
	CHAN 42 = 36	NS
	CHAN 43 = 34	NS
	CHAN 44 = 33	NS
	CHAN 45 = 35	NS
	CHAN 46 = 0	NS
	CHAN 47 = 30	NS
265: CLK L TO ADDR. VALID: TCLAV (80NS MAX):	CHAN 9 = 41	NS
	CHAN 10 = 38	NS
	CHAN 11 = 47	NS
	CHAN 12 = 39	NS
	CHAN 13 = 47	NS
	CHAN 14 = 49	NS
	CHAN 15 = 50	NS
	CHAN 16 = 46	NS
	CHAN 17 = 29	NS
	CHAN 18 = 49	NS
	CHAN 19 = 53	NS
	CHAN 20 = 35	NS
	CHAN 21 = 44	NS
	CHAN 22 = 32	NS
	CHAN 23 = 0	NS
	CHAN 24 = 46	NS
	CHAN 25 = 46	NS
	CHAN 26 = 45	NS
	CHAN 27 = 49	NS
	CHAN 28 = 49	NS
	CHAN 29 = 50	NS
	CHAN 30 = 45	NS
	CHAN 31 = 45	NS
266: CLK HIGH TO SG LOW: TCHGL (80NS MAX):	CHAN 57 = 19	NS
267: CLK HIGH TO SG HIGH: TCHGH (80NS MAX):	CHAN 57 = 20	NS
268: CLK LOW TO VMA LOW: TCLVHL (80NS MAX):	CHAN 52 = 29	NS
269: CLK HIGH TO VMA HIGH: TCHVHM:	CHAN 52 = 22	NS
270: CLK LOW TO E LOW: TCLEL:	CHAN 53 = 23	NS
271: CLK LOW TO E HIGH: TCLEH:	CHAN 53 = 21	NS
272: CLK H TO ADDR.-FC T.R. (VDM & VOL)-D.SV:	CHAN 6 = 57	NS
	CHAN 7 = 56	NS
	CHAN 8 = 58	NS
	CHAN 9 = 60	NS
	CHAN 10 = 63	NS

APPENDIX C

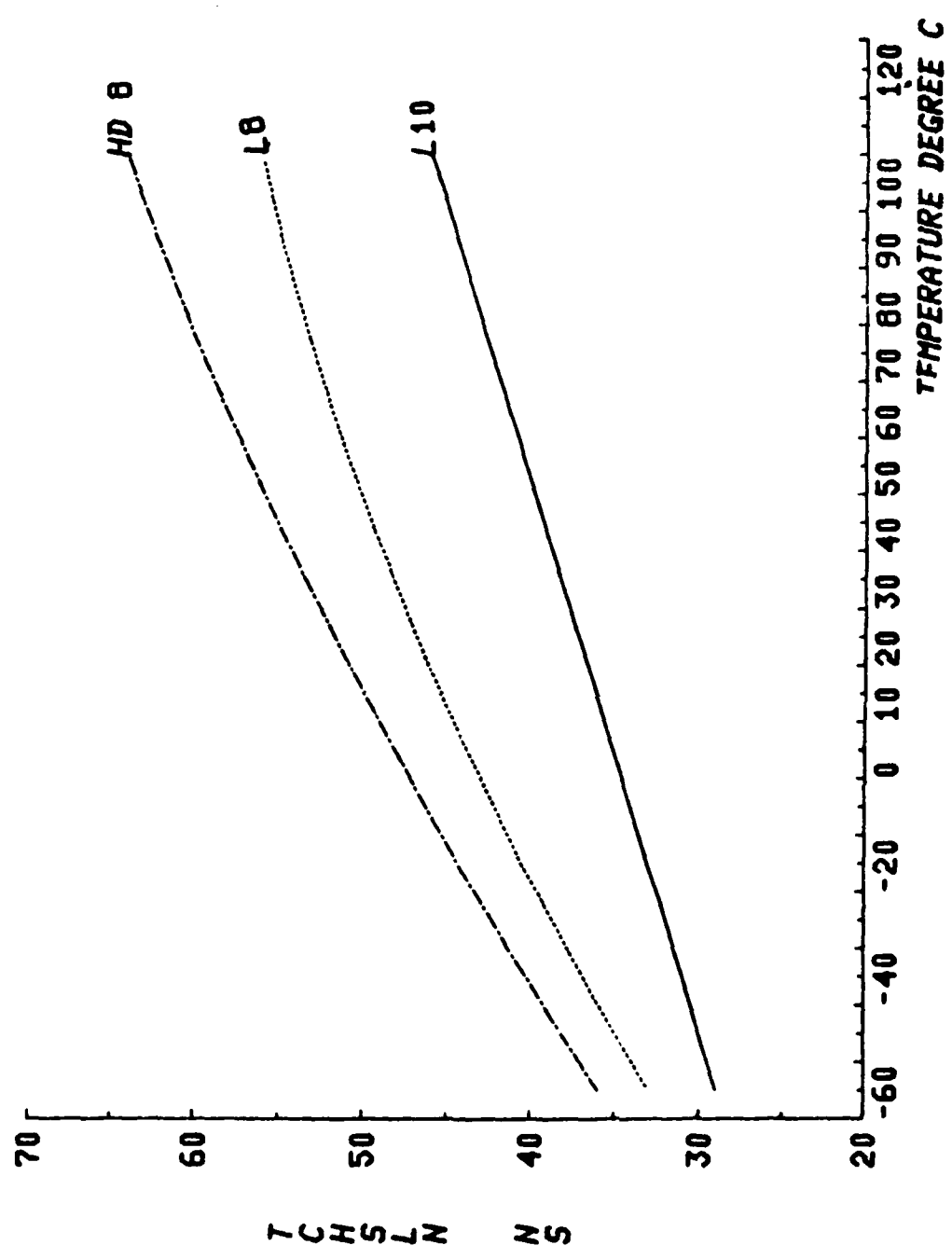
THE FOLLOWING GRAPHS ARE SELECT PARAMETERS OBTAINED
FROM THE MOST RECENT MC68000L8, MC68000L10 AND
HITACHI HD68000 DEVICES. THE DATA IS REPRESENTATIVE
OF THE WORSE CASE DATA OBTAINED ACROSS THE TEMPERATURE
RANGE OF -55°C TO $+110^{\circ}\text{C}$ T_{CASE}.



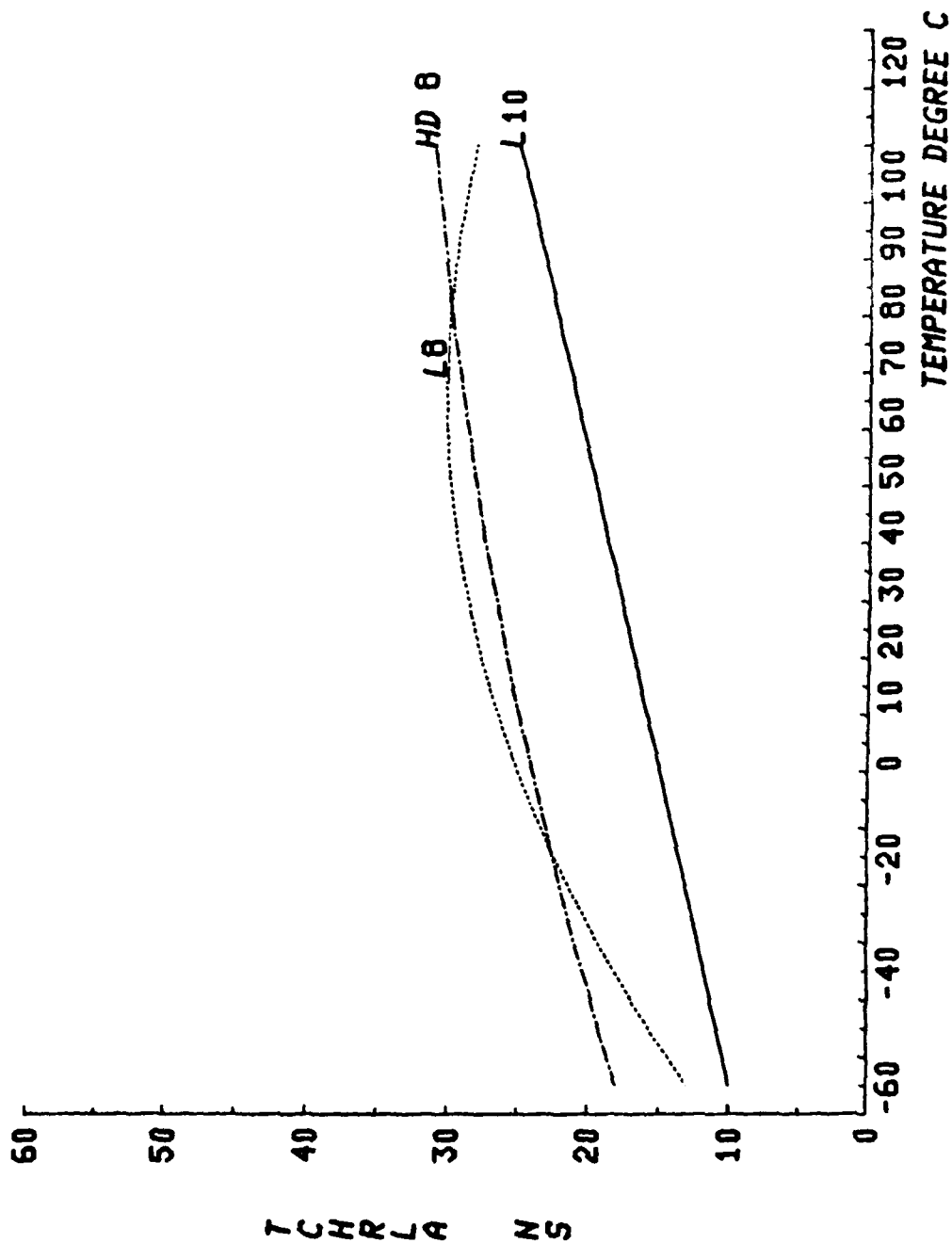
VOL - VOH VS TEMPERATURE



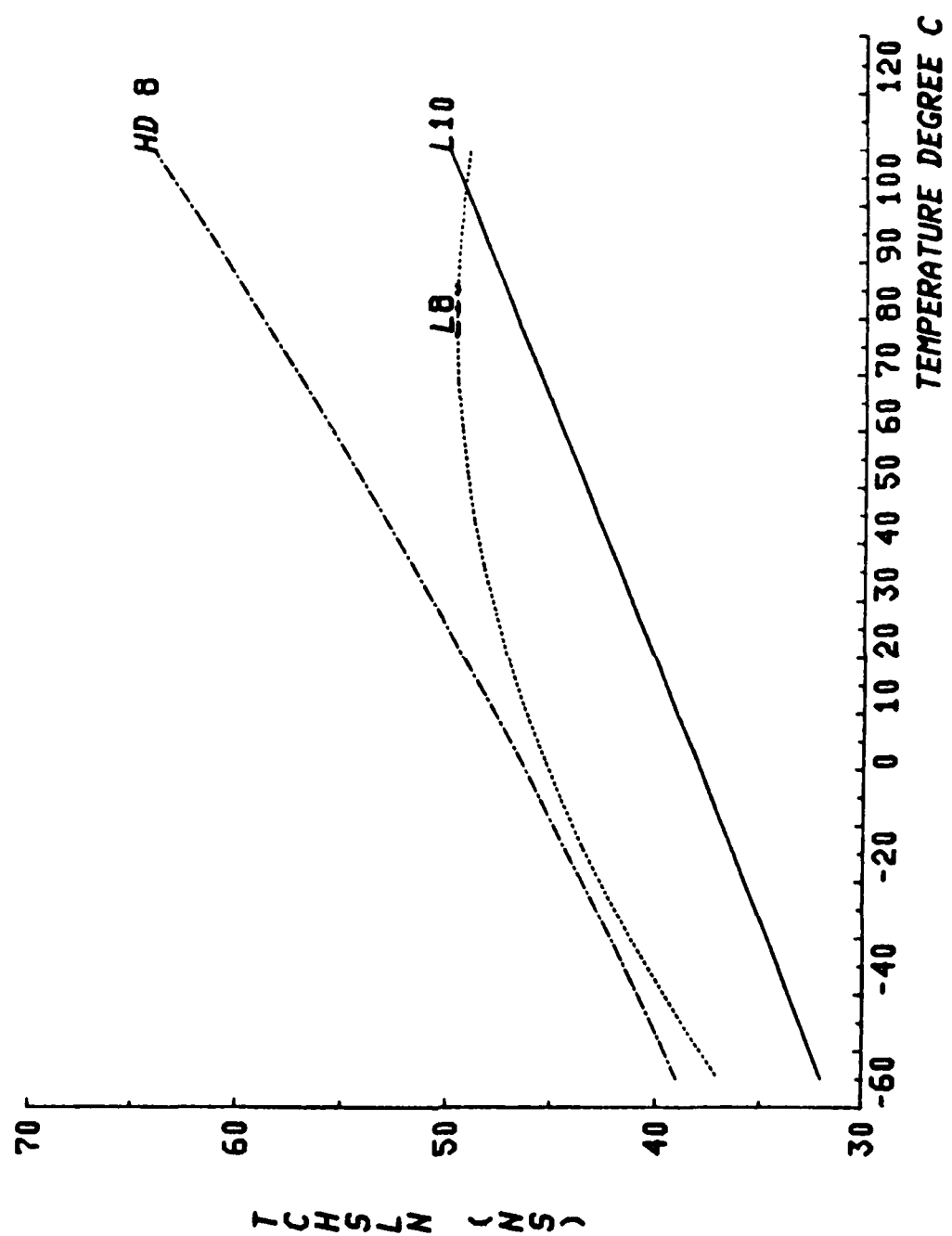
CLK TO DS LOW



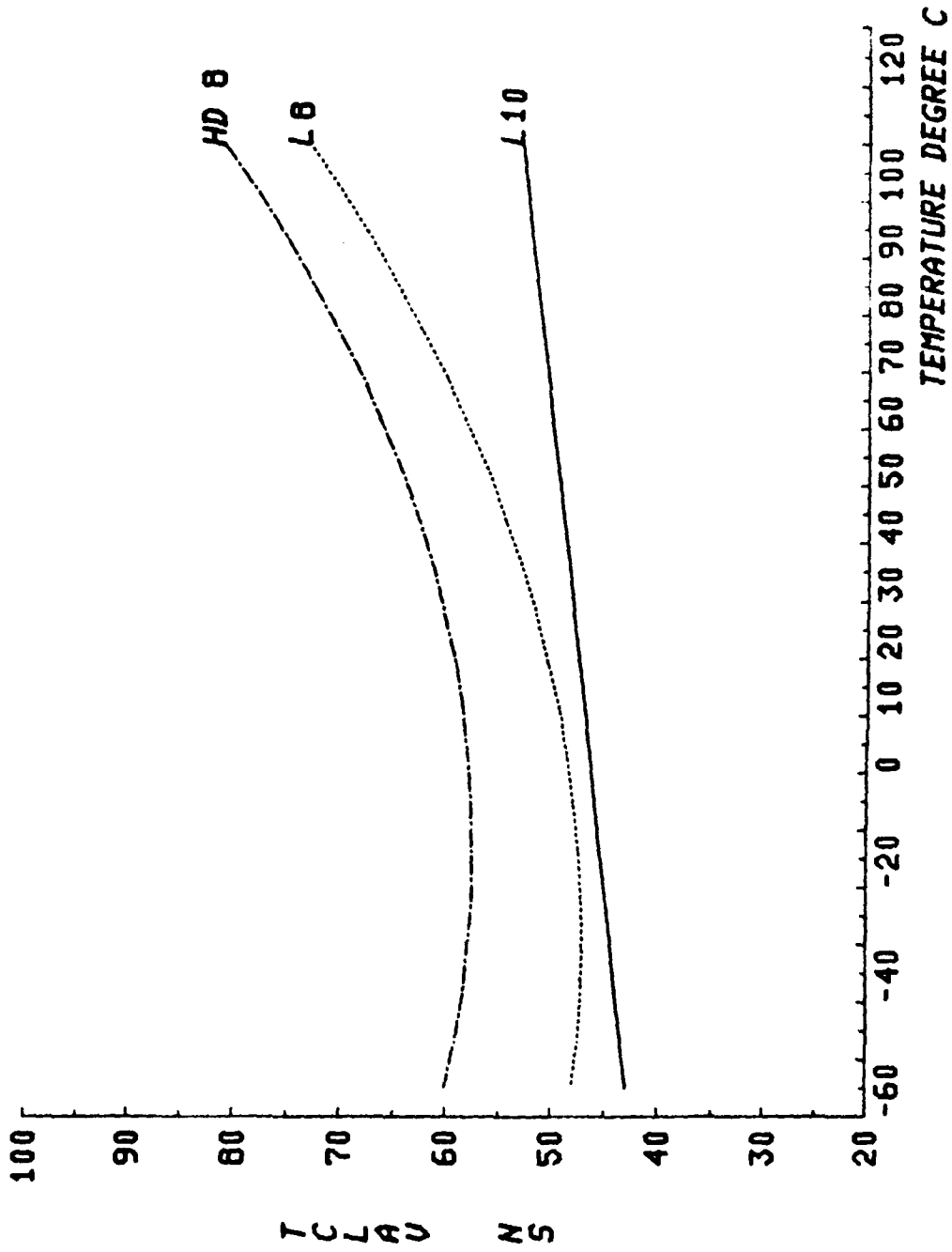
CLK TO R/H LOW



CLK TO AS LOW



CLK TO ADDRESS VALID



REFERENCES

1. Motorola Users Guide MC68000UM (AD)-(AD2)
2. Motorola Data Sheet AD1-814R2

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