

ADA111986

VLSI ARRAY PROCESSOR
R&D STATUS REPORT

DARPA ORDER NO. 4001
CONTRACT NO. N00014-80-C-0693
CONTRACT DATE: August 1, 1980
PRINCIPAL INVESTIGATOR: Ed Greenwood
PHONE: (602)949-3349

JANUARY 11, 1982
REPORTING PERIOD - Thru December 31, 1981

APPROVED BY:

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Scottsdale, AZ

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Detail design of the Arithmetic Processor Unit (APU) chip has been completed. All cell types (100) have been run through the design rule check (DRC) programs, corrected and verified. DRC runs on the entire chip have been run and all corrections have been made. Fifteen out of eighteen of the chip DRC corrections have been verified. The metal, polysilicon and information data layers of the APU layout is shown in Figure 1. Figure 2 is a high level chip plan. The attached drawings, titled "VLSI Array Processor Arithmetic Processor Unit Chip Plan" is a detail drawing of the APU Chip Plan. Completion of design checks will be accomplished by January 15, 1982. Then the APU chip data base will be sent to MICARL for shrink to 3 micron rules (design was done in 4 micron rules) and compensation before initiating mask fabrication.

The functional level simulator of the APU has been built and verified using a set of APU diagnostic code. A gate level logic simulation of the APU has been built. The same set of APU Diagnostic Code is in integration and checkout of the APU logic simulator. This integration and test task is approximately 25% complete. This task will be completed before January 31, 1982.

The APU breadboard modules have been fabricated and check out has been initiated. The Array Processor Demonstration System (APDS) modules are in the wire-wrap process.

The APDS and APU microcode assembler have been built and checked out. The linker and loader for the APDS have also been built. The APDS simulator is approximately 75% built.

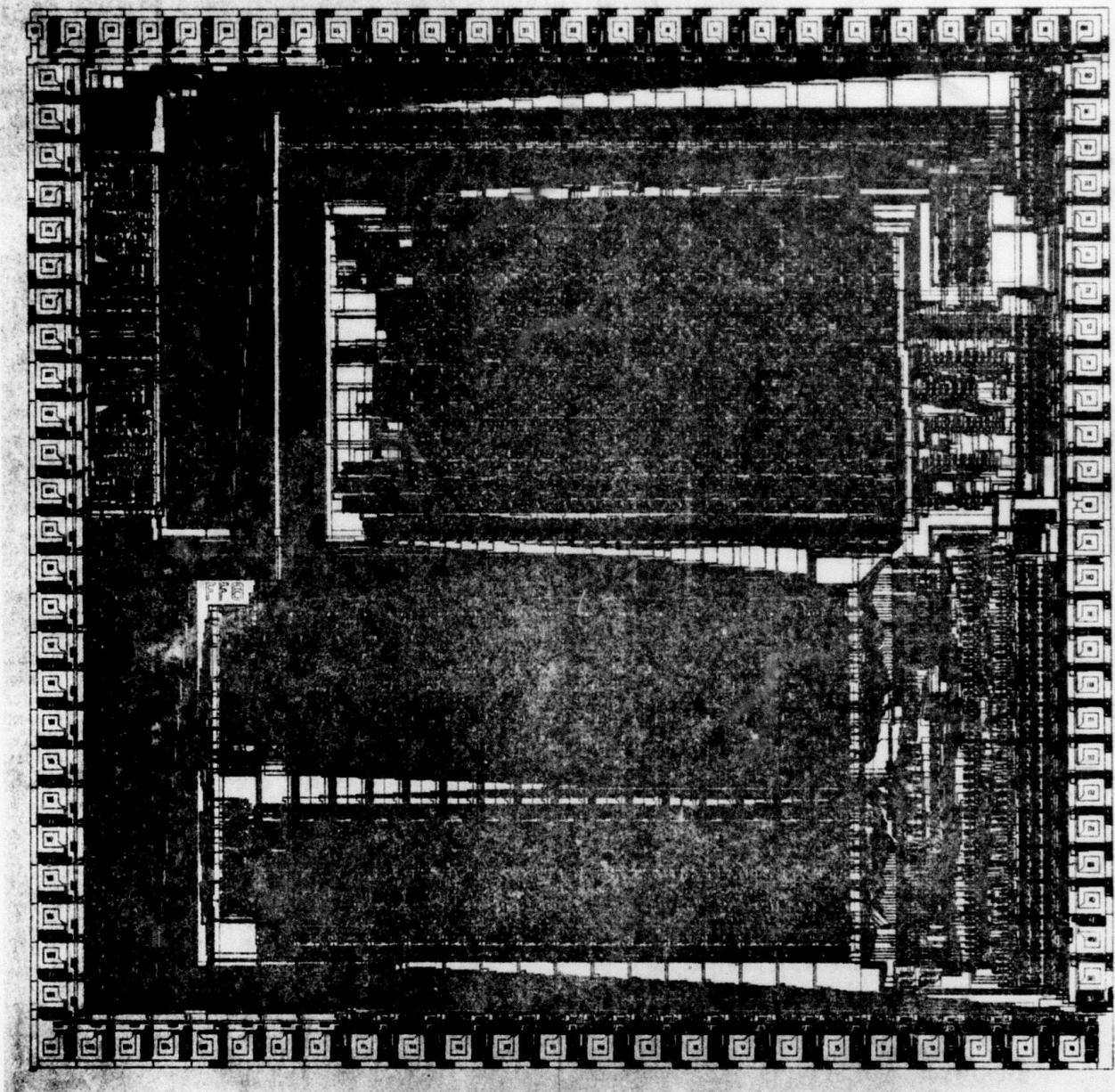
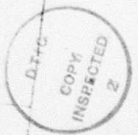


FIGURE 1
APU LAYOUT

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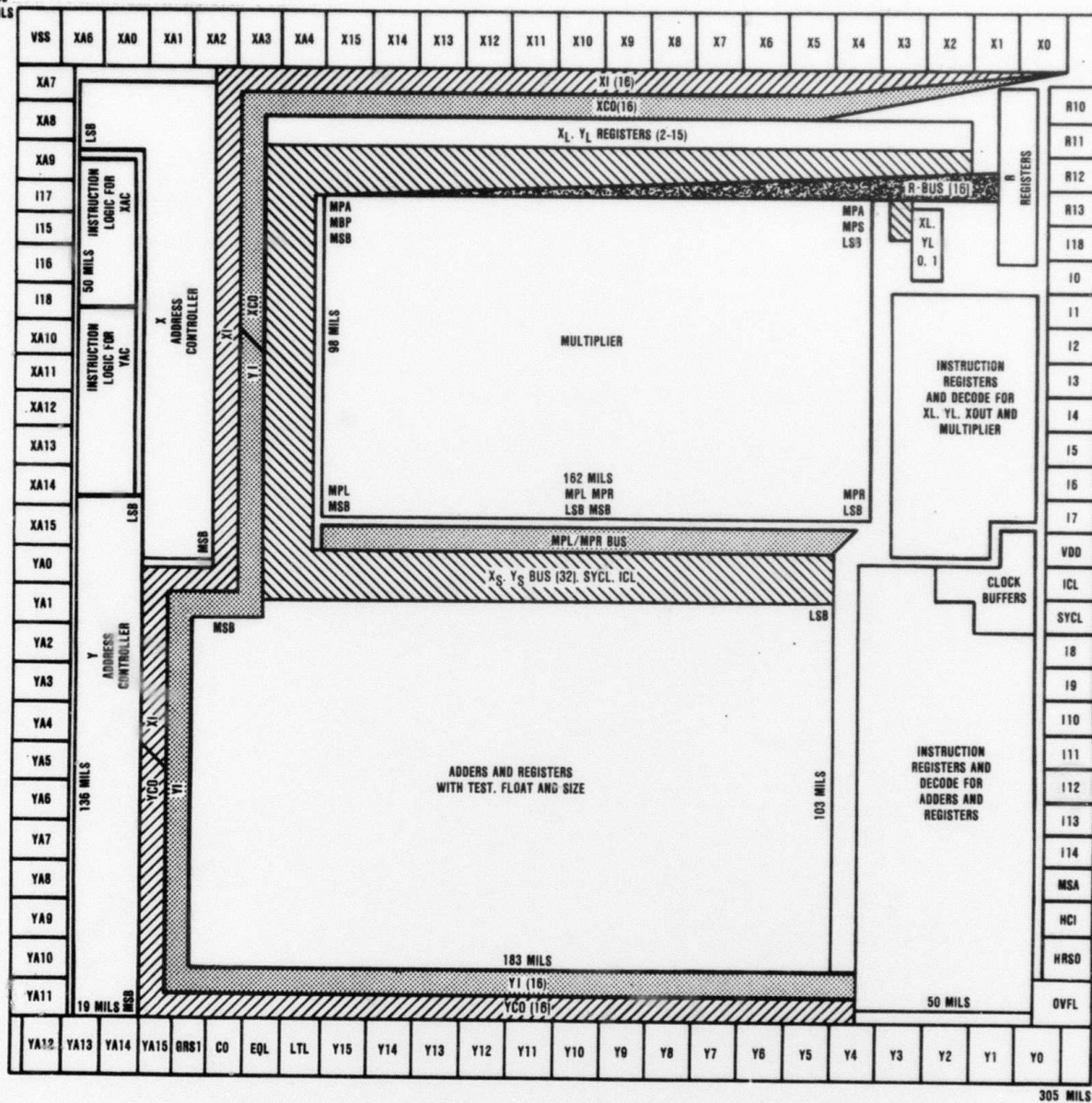


FIGURE 2
APU CHIP PLAN

The Architecture Report is being focused on and will be submitted to DARPA for review by January 31, 1982.

In the following quarter, the following activities are planned:

- 1) Complete VLSI APU design checks and deliver data base to MICARL
- 2) Fabricate APU mask set
- 3) Complete APDS simulator
- 4) Complete fabrication of APDS
- 5) Check out APU and APDS breadboards
- 6) Complete and deliver Interim Report (Architecture Report)

No technical problems are foreseen at this time. A funds expenditure report is provided in Table I.

Date Prepared January 12, 1982 Summary: Work Package Title Array Processor
 Contract No. N00014-80-C-0693 Report Month December 1981
 Contractor Motorola Inc. GED

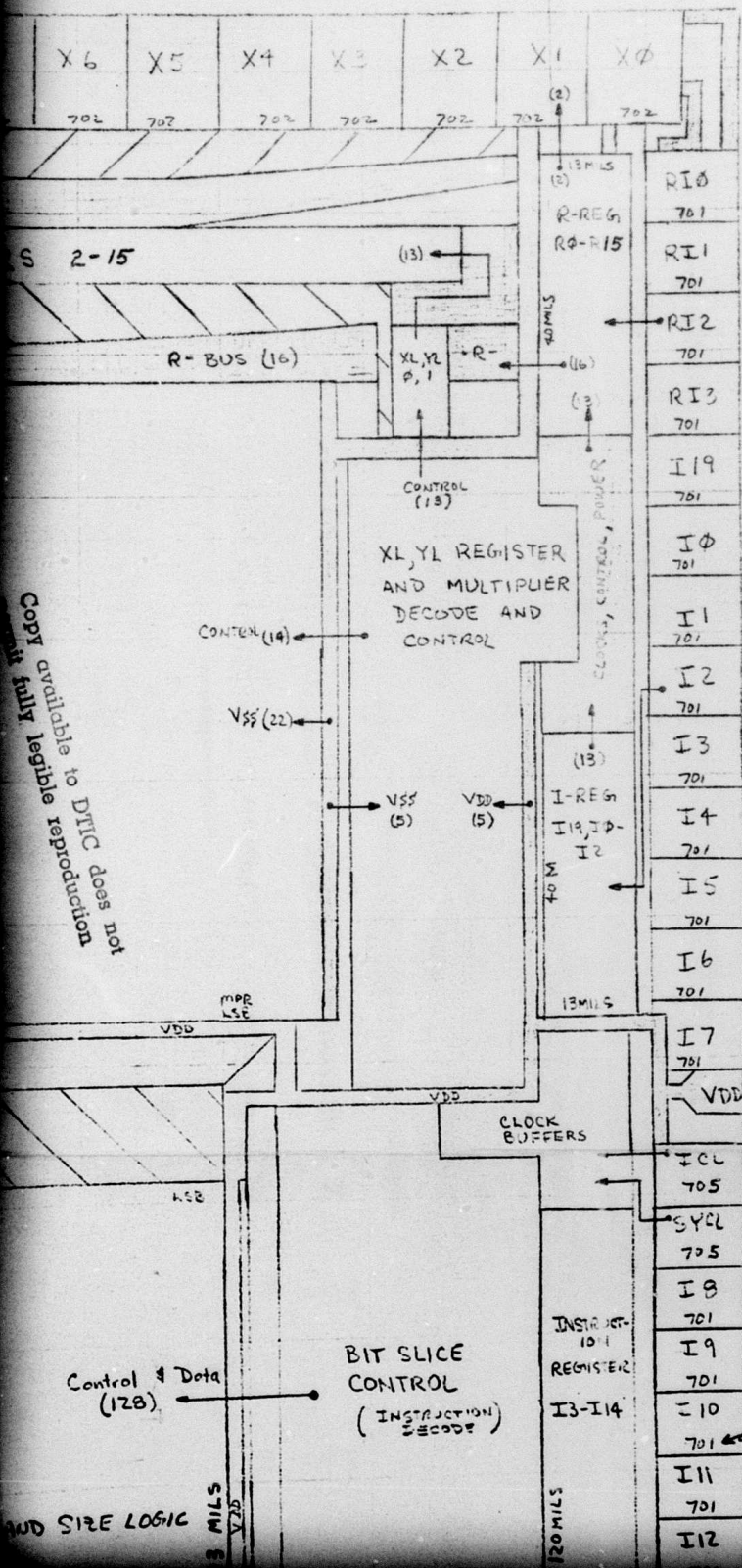
TABLE I
FUNDS EXPENDITURE REPORT

Column A ORIGINAL PROPOSAL	Column B Latest Accepted Revised Proposals (if any)	Column C Reporting Month Expenditures	Column D Cumulative Expenditures To Date			Column E Cost Complete estimate ..	Column F Latest Cost Estimate (D2 plus E) ..
			D1 Total Man Hours	D2 Dollar Value	D3* Percentage Dollar Value		
1. DIRECT LABOR							
Type No. of Hours@	Hourly Rate	Dollar Total					
Total Direct Labor		161,363	11,903	175,551		80,457	256,008
Overhead		155,230		168,767		76,010	244,777
Total direct labor & O'Head		316,593		344,318		156,467	500,785
2. MATERIALS & PARTS		500,256		325,297		262,477	587,774
3. TRAVEL EXPENSE		20,120		9,581		13,026	22,607
4. COST OF MONEY		9,900		18,275		10,775	29,050
5. GEN & ADMN		156,938		129,194		77,804	206,998
6. OTHER COSTS		86,193		45,258		36,049	81,307
TOTAL COSTS		1,090,000		871,923	80.0	556,598	1,428,521
7. FIXED FEE (OR PROFIT)		99,000		79,193	80.0	19,807	99,000
TOTAL CONTRACT PRICE		1,189,000		951,116	80.0	576,405	1,527,521
OUTSTANDING COMMITMENTS		--		42,734	--	(42,734)	--
TOTAL COMMITMENTS AND EXPENDITURES		1,189,000		993,850		533,671	1,527,521

Hand-drawn schematic diagram of a computer architecture, likely a digital logic circuit. The diagram is organized into a grid with columns labeled XA6 through XA9 and rows labeled XA7 through XA15. It shows various components including control logic, address controllers, multipliers, and registers. Key labels include 'CONTROL (12)', 'ADDRESS CONTROLLER [XAC] XA2-15', 'MULTIPLIER', 'REGISTER SLICE (16)', 'MCA REG. (16)', 'MCB REG. (16)', 'Xs, Ys BUS (32)', and 'BIT SLICE (17)'. Dimensions like '136 MILS', '50 MILS', and '2 MILS' are indicated for various sections. A note 'see Note 1' points to a specific area. The diagram is a detailed technical drawing of a computer's internal structure.

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REVISIONS			
ZONE	REV	DESCRIPTION	DATE APPROVED
	1	UPDATE LAYOUT	12/21/81 D.N.
	2	Documentation clean-up	12/21/81 E.G.



- Notes:
1. FF8 is mark set identifier
 2. 70# numbers refer to type of I/O cell
 3. M is mils
 4. (#) is the number (#) of lines
 5. poly is run vertical thru cells; metal is run horizontal thru cells

see note 2

