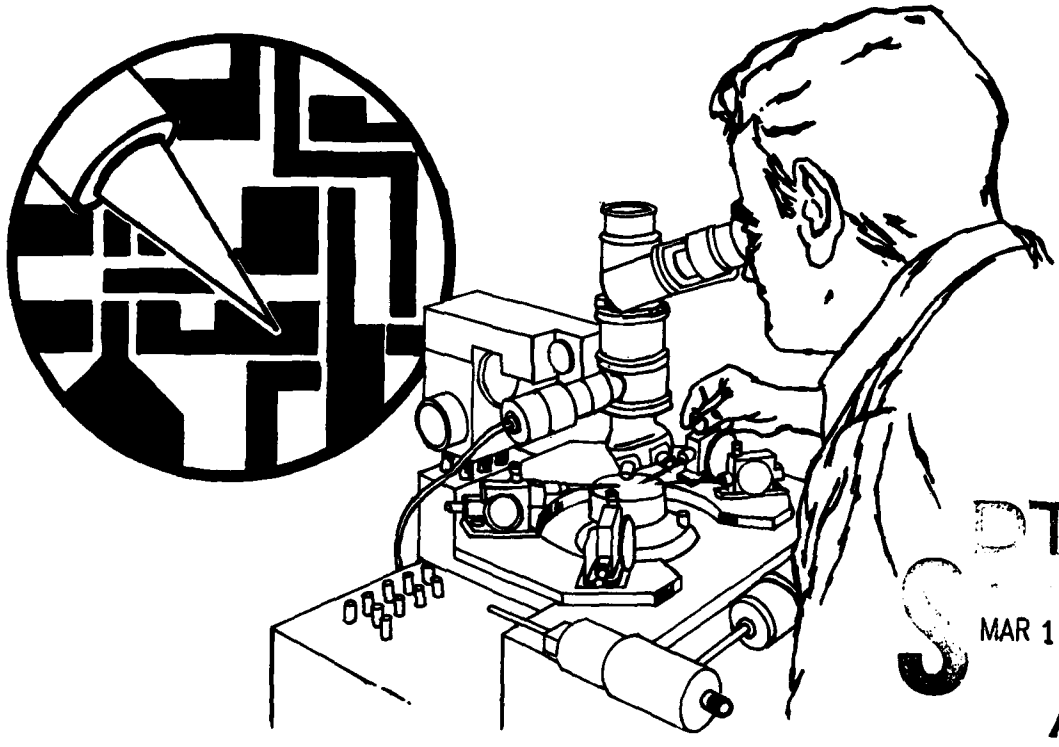
MICROELECTRONICS

FAILURE ANALYSIS TECHNIQUES

A PROCEDURAL GUIDE



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MICROELECTRONICS FAILURE ANALYSIS TECHNIQUES

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PREFACE

This Procedural Guide is intended to serve as a useful tool for the beginning failure analyst as well as a convenient reference source for the experienced analyst and other quality, reliability project engineers in the semiconductor industry. It represents a collection of the most useful failure analysis techniques being used by industry leaders in this growing field. Obviously, such a task can only be accomplished with the help of many people throughout the semiconductor industry. This document reflects the degree and extent of that industry-wide cooperation.

The procedural guide provides the analyst with a general technical discussion of each major failure analysis technique with samples or suggestions on its use in performing failure analysis on semiconductor devices. It provides a collection of in-depth technical references for additional reading or research in a specific technique area and approximate cost of major equipment required to perform the technique. No attempt has been made to provide a step-by-step procedural manual on every failure analysis technique but rather a general guide in selecting and utilizing the variety of failure analysis techniques available today to the failure analyst.

The foresight of the Reliability Branch of the Rome Air Development Center in recognizing the need for a comprehensive procedural guide to aid the failure analyst in achieving the goal of reliability improvement through in-depth failure analysis of semiconductor defects is commendable.

The cooperation and technical direction of Edgar A. Doyle, Jr., RADC Program Manager, in bringing this handbook into being is gratefully acknowledged. The General Electric Company is indebted to the many RADC and industry personnel who assisted as technical consultants on the Document Review Board and who, in many cases, provided useful technical comments on written material and supplied photographs which have been used in this procedural guide.

We view this document as only a useful beginning on which the semiconductor industry can build as more information on specific applications and procedural insights become available to the practicing failure analysts in the industry.

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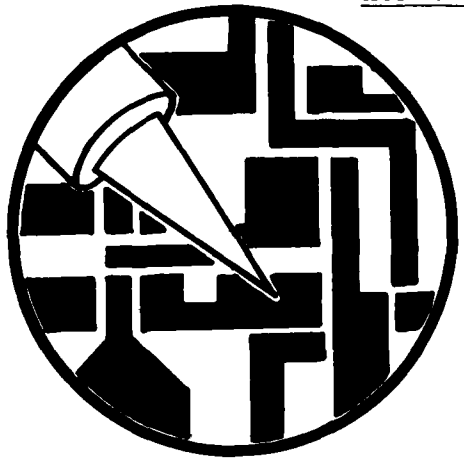

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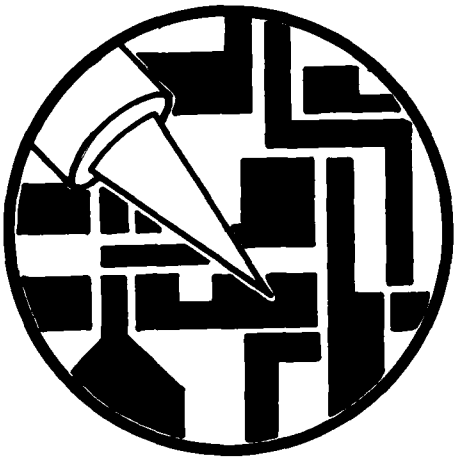

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FORWARD

Failure Analysis, an expanding reliability discipline, has provided significant impact in improving, through corrective action, the reliability of microelectronic technology devices. From the early 60's to the present, many innovative failure analysis techniques and analytical instruments have been developed. Although much technique information has been presented in the technical literature, definitive procedures were not usually included. Other useful analysis methods representing the collective corporate memory of many researchers have remained unpublished or undocumented. Due to this diversity of technique information sources, the microelectronics sector has long recognized the need for a compendium documenting proven analytical methods and available equipment for part failure analysis. This procedural guide is an initial effort in satisfying that demand and is intended to facilitate personnel training, increase analyst proficiency, project facilities upgrading and improve the reliability engineer's knowledge of diagnostics useful in performing or managing part failure analysis tasks or services.

The objective of this procedural guide was not to present an expose of device failure modes/mechanisms and applicable techniques for detection, identification and measurement but rather to provide a treatise on proven failure analysis techniques, equipment, procedures and expected analytical results. The guide thus represents a compilation and description of practical semiconductor failure analysis techniques rather than failure analysis flow sequences for verifying specific device failure mechanisms. The document is composed of six major sections outlined below:

- General Introduction
- Reference Documents
- Failure Analysis Techniques
- Laboratory Safety Procedures
- Glossary of Terms and Materials
- Technique References

The general introduction treats device reliability physics concepts, test and analysis methodologies and contains semiconductor device technology and failure mode/mechanism summaries. The reference document section includes a list and brief sketch of available, reliability oriented military handbooks/standards, relevant symposia, and other useful reliability technology information sources. The techniques section, the main text body, is comprised of seventeen descriptive failure analysis technique subsections covering different analytical methods. Required equipment, sources and cost and pertinent technical references are included at the end of each major technique section. The remaining sections define laboratory safety procedures, provide a glossary of selected terms and materials and present a comprehensive bibliography of failure analysis technique references.

The procedural guide is published using quality materials for extended usage and provided in looseleaf format to facilitate future update and addition of supplemental technical material by the individual user.

The compiling and editing of this failure analysis technique compendium, designed to meet the needs of both beginning and experienced analysts, R&QA activities and users of independent analysis services, was a formidable task. Although the guide information was derived from an extensive literature search, on-site failure analysis laboratory surveys, a document review board composed of acknowledged experts from goverment and industry, and technical inputs from reliability specialists, it is virtually impossible to incorporate all technique variations and unique applications. Admittedly, due to resource limitations, some technique sections are not considered all-inclusive and the level of detail presented throughout the document could be improved.RADC solicits user comments, corrections and technical inputs (contributor monetary compensation by the U.S. Government prohibited) for a future document revision and update.

The significant accomplishment of the General Electric Company in preparing this document is commendable. The diligent technical efforts of Mr. William L. Morris, GE Program Manager, and Mr. Earl L. Parks, GE Technical Editor, are gratefully acknowledged. RADC is also indebted to the Document Review Board members, GE E-Lab and RADC Reliability Branch Staff cited herin and other corporate personnel representing a spectrum of government and industry expertise for their technical and editorial contributions in preparing and reviewing this document.

RADC views this procedural guide as an initial positive step in transitioning both established and recent failure analysis technique developments and information to the expanding microelectronics reliability community.

Rome Air Development Center

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SECTION I

GENERAL INTRODUCTION

I. GENERAL

A. Reliability Physics Approach. Failure Analysis in the late fifties and early sixties consisted of determining when the device was good or bad using very limited equipment. Usually, this equipment consisted of an ohmeter to determine that functional junctions still existed or that a short existed between two or more terminals of the device. Over a period of years, semiconductor specialists realized that as semiconductor devices became more complex, a more detailed examination would have to be made of these microscopic parts if we were ever going to understand the basic material and process effects on the device's electrical performance.

During this period of time, an annual Physics of Failure Symposium was started to provide a technical forum for discussing specific failure modes and a detailed analysis of the various electrical, chemical, and physical characteristics. The failure analyst utilized these data to hypothesize a number of potential failure mechanisms. These symposia were very successful in developing technical interest and respect for the work of the failure analyst, particularly in the semiconductor industry. A series of Physics of Failure in Electronics books were printed covering each year's technical papers presented at the Battelle Memorial Institute in Columbus, Ohio. These initial symposia were jointly sponsored by the Rome Air Development Center and usually some industrial research laboratory.

Out of this developed the basic reliability of physics approach that there is a fundamental electrical, chemical, or metallurgical explanation for any microelectronic device failure. It only requires that the failure analyst be part Sherlock Holmes and Columbo, and find, store, massage, and utilize all of the available facts to piece together the complete failure scenario as it is postulated to have happened. It is imperative that the failure analyst consider "all possibilities" in examining the data so that a potential

failure mechanism is not overlooked because it is seen less frequently than some other failure mechanism.

Failure Analysis requires that all decisions be made on facts wherever possible, and if not possible, on considered judgement possibly with technical consultation with one's technical peers. Many times an analyst, in your own group, may have experience which can save you invaluable time by consulting on the problem.

B. Semiconductor Technology Summary. The failure analyst must have a basic understanding of the materials and typical processing steps used in a whole array of semiconductor devices to be successful in localizing a defect and identifying the cause(s). This section will briefly review the basic semiconductor and passive devices used to fabricate integrated circuits from both a topographical and cross-sectional viewpoint. It is hoped that this information will provide a ready reference to refresh the analyst's memory of the basic concepts of a particular semiconductor device type but will not go into an exhaustive treatment of any technology area. A large technical bibliography is provided at the end of this section if additional technical information is needed about any of these technologies. (See Reference 9 for additional examples of semiconductor processes.)

1. Bipolar. The bipolar transistor is by far the most significant single component in monolithic circuits. The planar process was initially developed for fabrication of discrete bipolar transistors and later extended to integrated circuits. Therefore, in going from a discrete to an integrated device, the bipolar structure usually involves the least amount of design compromise. The workhorse of almost all analog integrated circuits is the npn bipolar transistor.

a) NPN Transistors. A comparison of the basic bipolar structure for a discrete versus an integrated circuit npn transistor is shown in Figure 1. In the case of the discrete device, a heavily doped (low resistivity) substrate is used as the starting material, on which a higher resistivity n-type epitaxial layer is grown to serve as the active collector region. The basic difference between the two device structures shown in Figure 1 is that, in the case of an isolated integrated device structure, the collector region is only accessible from the top surface of the wafer. This, in turn, results in a considerably higher collector series resistance, r_{cs}, for the integrated device. The presence of a junction isolation pocket around the collector of the integrated device also introduces two additional parasites into the structure. These are the parasitic collector-substrate diode, D_{ss}, and the junction capacitance C_{ss}

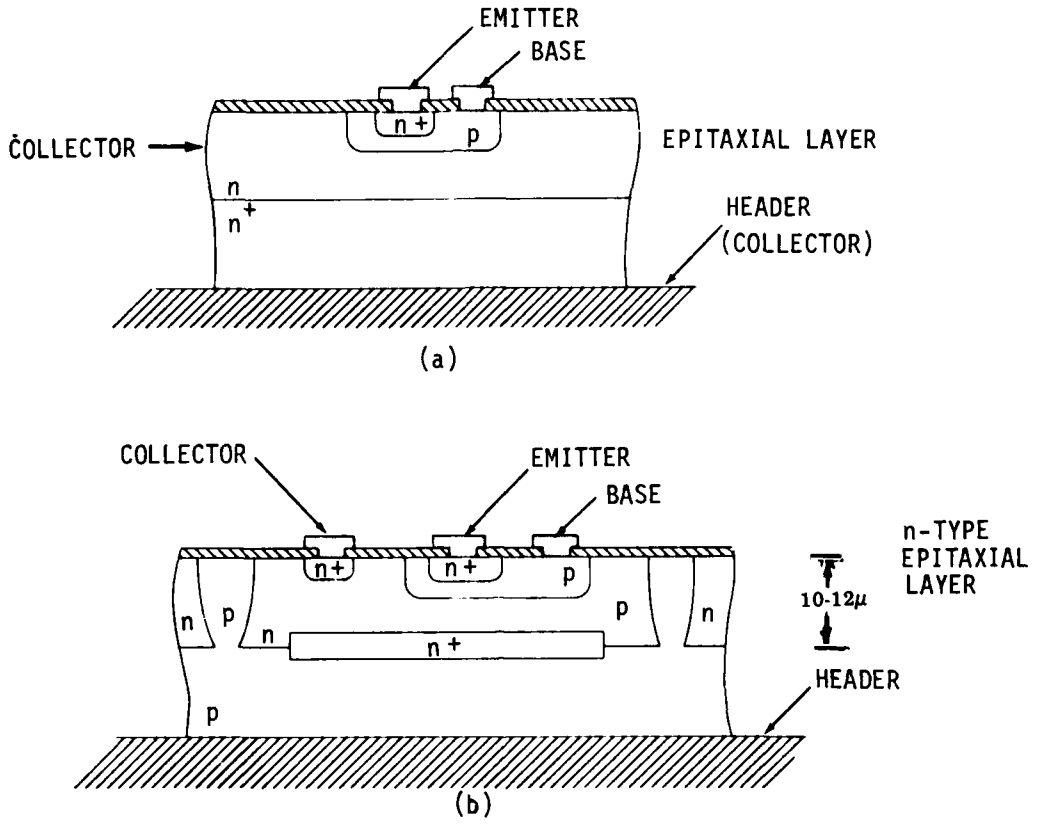


FIGURE 1. A COMPARISON OF DISCRETE (a) AND INTEGRATED (b) npn BIPOLAR TRANSISTOR STRUCTURES

associated with it as shown in Figure 2. In the figure, the intrinsic transistor between the terminals E, B and C is electrically equivalent to the discrete planar device of Figure 1 (a). The subepitaxial N+ layer (buried layer) in the integrated structure serves a dual purpose: it provides a low resistivity current path from the active collector region to the physical collector contacts; and it reduces the possibility of a parasitic pnp action between the substrate and the p-type base, if the collector-base region of the npn were to become forward-biased.

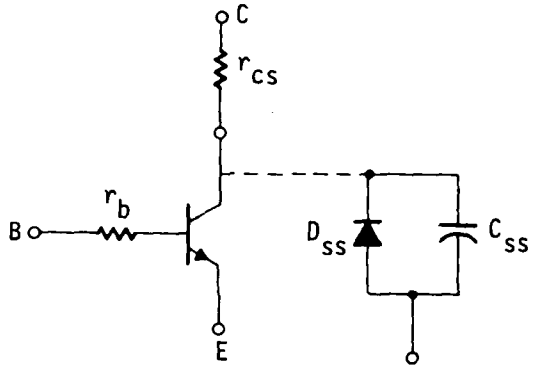


FIGURE 2. INHERENT PARASITICS ASSOCIATED WITH JUNCTION ISOLATED TRANSISTORS

Typical Resistivities (Ω-CM)

Layer	Range
n - type epitaxial layer	0.5 to 5
p - type base diffusion	120 to 200
n^+ subepitaxial layer	12 to 18

Figure 3 shows the lateral geometry of a typical integrated small signal npn transistor. The topographical view is drawn at 500X scale. The vertical or cross-sectional view is not drawn to scale.

The failure analyst should be aware of the basic voltage breakdown mechanisms of a pn junction. As the reverse bias across a pn junction is increased beyond a critical value, the current through the junction increases rapidly. This critical voltage is known as the junction breakdown voltage BV. In silicon, two separate breakdown mechanisms exist. These are avalanche and Zener breakdowns. Avalanche breakdown voltage is normally determined by the impurity concentration on the lighter doped side of the junction. Zener type breakdown mechanism happens if both sides of the junction are very heavily doped. For junctions which break down at 5 volts or less, Zener breakdown is the main conduction mechanism. In analog

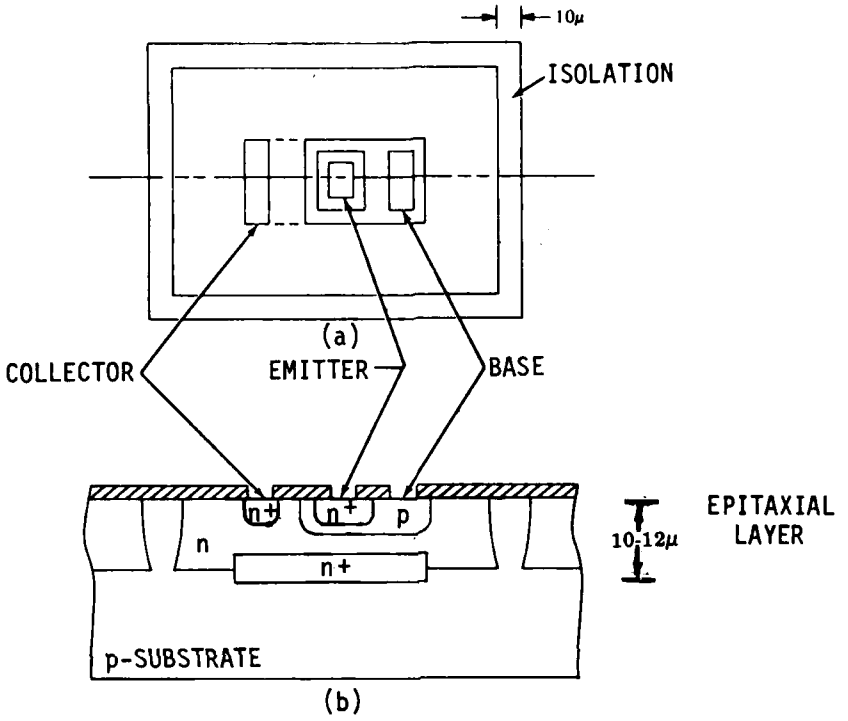


FIGURE 3. LATERAL GEOMETRY AND STRUCTURAL DIAGRAM OF A SMALL-SIGNAL npn TRANSISTOR

integrated circuit structures, impurity concentration levels which can give way to Zener breakdown are not normally encountered.

The transistor dc gain, βo, depends somewhat on the value of the collector current. The decrease of βo at high currents is due to two dominant factors: decrease of emitter efficiency and emitter-crowding effects. To reduce the βo falloff at high current levels, it is necessary to maximize emitter periphery-to-area ratio and to minimize the base-spreading resistance. This usually results in an interdigitated transistor structure as shown in Figure 4 for high current applications.

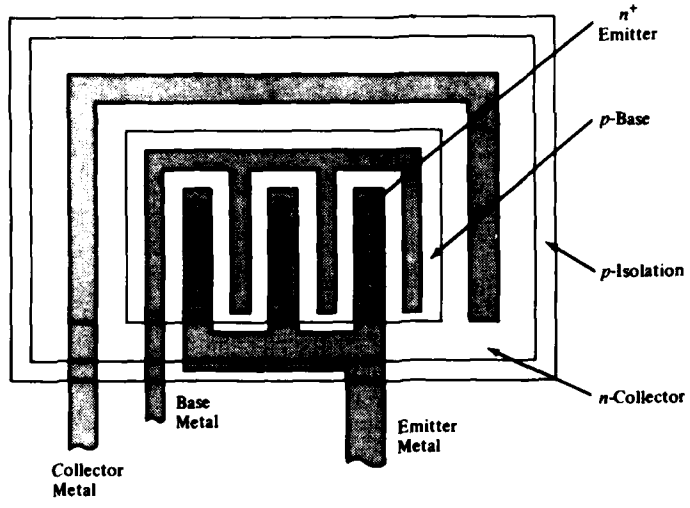


FIGURE 4. LATERAL GEOMETRY OF A HIGH CURRENT TRANSISTOR

In certain analog circuits, such as the input stages of operational amplifiers, it is necessary to have very high input impedance and low input bias currents. A punch-through or "super β" transistor is fabricated with a collector-emitter voltage breakdown limited to the 2 to 3-volt range. In circuit design, punch-through transistors are often used together with a conventional integrated circuit transistor which can provide the necessary voltage protection for it.

Figure 5 shows a composite connection of a punch-through transistor with a lateral pnp transistor, where the base-emitter diode of the pnp clamps the voltage swing across the punch-through transistor to a level below its breakdown voltage. The resulting transistor structure has the effective βo of the punch-through npn and the breakdown voltage of the lateral pnp.

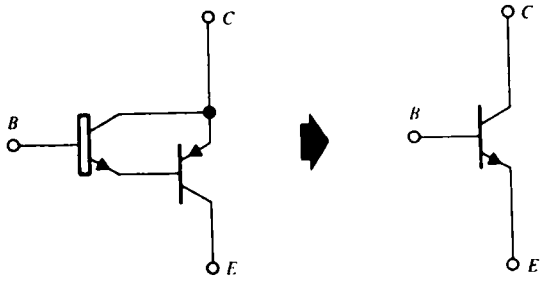


FIGURE 5. COMPOSITE CONNECTION OF A PUNCH-THROUGH npn WITH LATERAL pnp

b) PNP Transistors. Some analog circuit functions may require the use of complementary bipolar transistors. In such cases, it is necessary to fabricate functional pnp transistors on the same substrate with the npn devices. For this purpose, a number of monolithic pnp transistor structures have been developed which are totally or partially compatible with the standard npn bipolar process technology. Some of these will be reviewed in this section.

The simplest pnp transistor structure which can be fabricated simultaneously with the npn bipolars is the lateral pnp transistor, which requires no additional masking or diffusion steps. Figure 6 shows the topographical view and the structural diagram of a lateral pnp transistor. The base region of the device is formed by the n-type epitaxial layer which serves as the collector of the npn transistors. The p-type base diffusion of the npn is used to form the emitter and collector regions of the lateral pnp; the n^+ emitter diffusion of the npn is used to form the n^+ contact region for the pnp base. In such a device structure, the transistor action takes place in the lateral direction, i.e., parallel to the device surface. Since most of the current flows near or along the device surface, the lateral pnp current gain is also very strongly affected by surface recombination effects. Under production environment, the typical values of αo for the lateral pnp are of the order of 0.6 to 0.95, corresponding to typical βo values of 1.5 to 20.

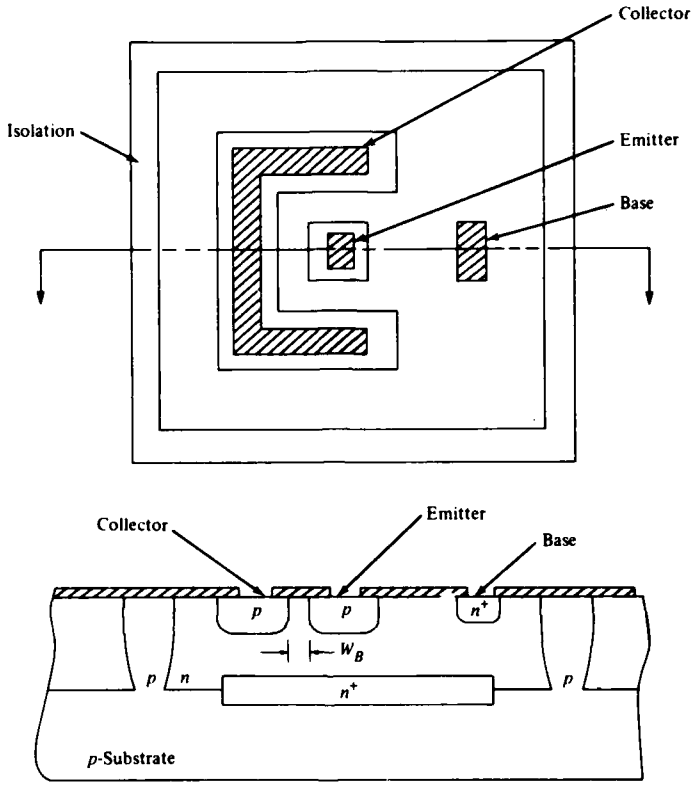


FIGURE 6. PLANE VIEW AND STRUCTURAL DIAGRAM OF A LATERAL pnp TRANSISTOR

The lateral pnp current gain and the frequency response can be significantly improved by creating a voltage gradient, or a drift field within the base region. This can be achieved using a "drift-aided" pnp structure, shown in Figure 7. A bias current is forced through the two drift electrodes at opposite ends of the base, setting up an electric field within the base region. This bias current has a twofold effect on the electrical characteristics of the device: (1) it preferentially biases the emitter such that it emits only along the edge facing the collector, and (2) it sets up an aiding field within the base region to reduce the base transit time for the emitted holes.

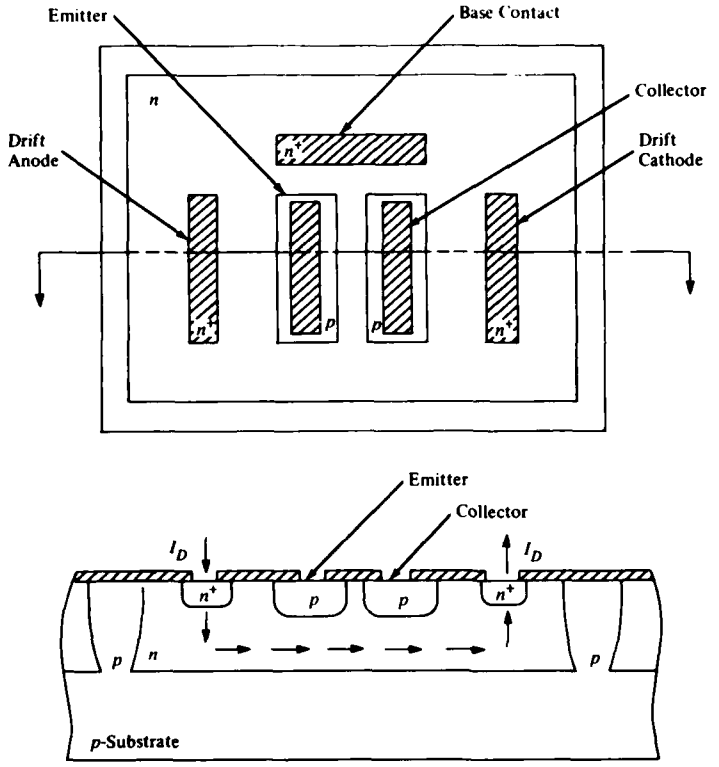


FIGURE 7. DRIFT-AIDED LATERAL pnp TRANSISTOR

The low βo of the lateral pnp can be improved by combining it with an integrated npn transistor, forming a composite transistor shown in Figure 8. The polarity and the electrical characteristics of such a composite device are equivalent to that of a single pnp transistor having a higher current gain.

A functional pnp transistor can also be obtained by using the base region of the npn as the emitter, the n-type epitaxial layer as the base, and the p-type substrate as the collector. Such a device is known as the "substrate pnp" and has the structure shown in Figure 9. The substrate pnp can be fabricated simultaneously with the npn bipolar transistors, without requiring additional masking or diffusion steps. The collector of the substrate pnp is formed by the

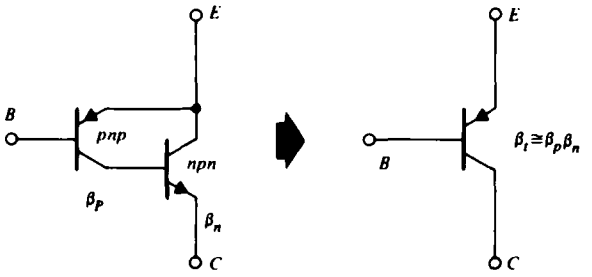


FIGURE 8. COMPOSITE CONNECTION OF COMPLEMENTARY TRANSISTORS

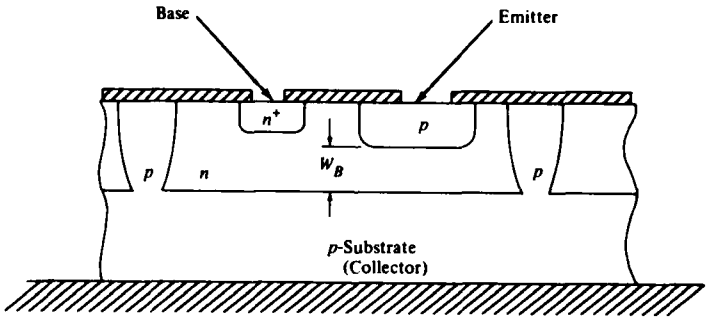


FIGURE 9. STRUCTURAL DIAGRAM OF A SUBSTRATE pnp

p-type substrate which is common to the rest of the circuit, and is at all times ac grounded. Therefore, the substrate pnp is only available in the grounded collector configuration and cannot be used for level shifting or voltage amplification. It does provide current amplification and can be used as a low impedance output device in Class B complementary stages.

A number of high performance pnp transistor structures have been developed for analog circuits. These structures have also demonstrated more tolerance for radiation environment. Each of these

device structures requires additional processing steps above and beyond what is required for the basic npn transistor. It is possible to fabricate high performance pnp transistors, simultaneously with the npn bipolars, using a device structure as shown in Figure 10. The pnp devices fabricated using dielectric isolation show a significant improvement over the lateral or the substrate type pnp transistors.

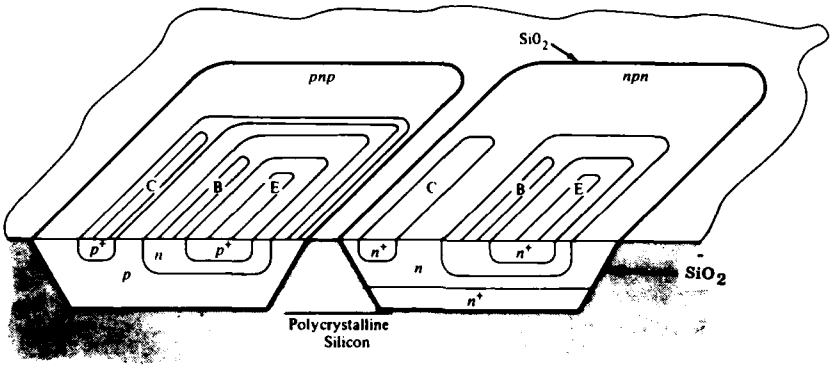


FIGURE 10. DIELECTRICALLY ISOLATED COMPLEMENTARY BIPOLAR TRANSISTORS

c) Integrated Diodes. Any one of the semiconductor junctions forming the monolithic circuit structure can be used as a diode. Figure 11 shows the basic diodes associated with an integrated npn

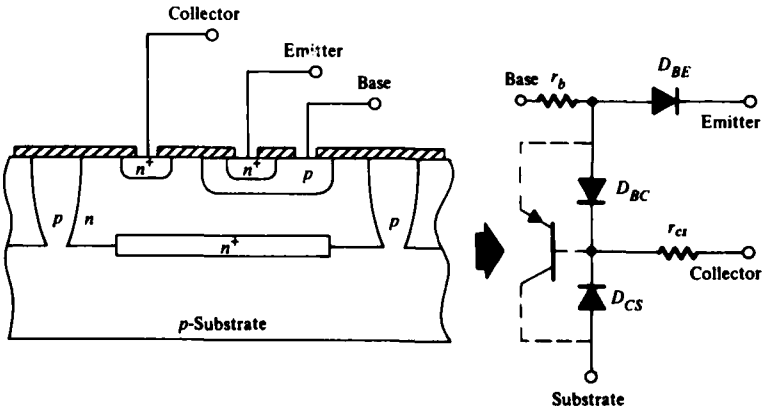


FIGURE 11. POSSIBLE DIODES AVAILABLE IN AN ISOLATED npn TRANSISTOR STRUCTURE

transistor. D_{BE} and D_{BC} represent the diodes formed by the base-emitter and the base-collector junctions; D_{CS} is the collector-strate diode in junction isolated circuits. Figure 12 gives a relative comparison of each of these diode connections with respect to the parasitics and the breakdown characteristics associated with each configuration. Diode connection (2) of Figure 12 combines two desirable electrical properties: low series resistance and no parasitic pnp action to the substrate. Therefore, it is the most commonly used configuration for integrated circuits.

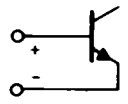
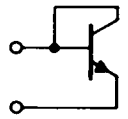
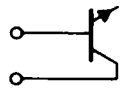
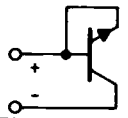
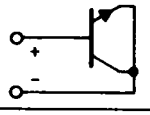
	Diode Connection	Series Resistance	Reverse Breakdown	Parasitic *pnp*
(1)		Low ($\approx r_b$)	Low (≈ 7 V)	No
(2)		Low ($\approx r_{cs} + r_b/\beta_o$)	Low (≈ 7 V)	No
(3)		High ($\approx r_b + r_{cs}$)	High (>40 V)	Yes
(4)		High ($\approx r_b + r_{cs}$)	High (>40 V)	Yes
(5)		High ($\approx r_b + r_{cs}$)	Low (≈ 7 V)	Yes

FIGURE 12. A COMPARISON OF PRACTICAL DIODE CONNECTIONS FOR AN npn TRANSISTOR

d) Avalanche Diodes. The avalanche breakdown characteristics of the junctions can be used for voltage reference or for dc level shift purposes. The base-emitter junction breakdown voltage which falls within the 6- to 9-volt range is the most commonly used avalanche diode structure since its breakdown voltage is compatible with the voltage levels available

in analog circuits. The avalanche breakdown voltage VB_{EB} associated with the base-emitter junction shows a positive temperature coefficient. Since the thermal drifts of the diode forward voltage V_D and BV_{EB} are in opposite directions, it is possible to partially compensate the thermal drift of an avalanche breakdown diode by connecting a forward-biased diode in series with it. Since both transistors have their collector and base regions in common, they can be designed as a single transistor with two separate emitters as shown in Figure 13.

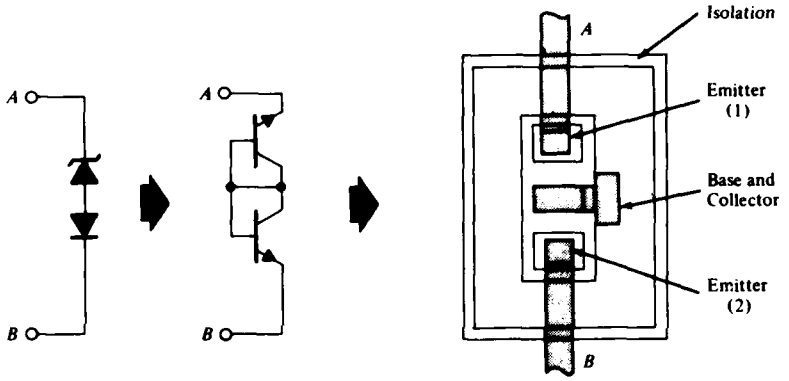


FIGURE 13. TEMPERATURE-COMPENSATED AVALANCHE DIODE AND ITS CIRCUIT LAYOUT

2. Passive Components. The choice and variety of passive components available in integrated circuits are severely limited. The heart of the integrated circuit technology is the planar process. This process is designed and developed around active devices; the passive components in general take second priority. This, in turn, results in limited sizes and kinds of passive components available in monolithic form. Capacitors and resistors are available only with poor control of absolute value or temperature tolerances and only over a relatively narrow range of values. In spite of the limitations on their size or absolute value tolerances, passive components in integrated circuits still enjoy some of the basic advantages of monolithic structures, such as close matching and close thermal tracking. The purpose of this section is to familiarize the failure analyst with the important features of passive components.

a) Integrated Capacitors. The most fundamental limitation on integrated capacitors is size. A general expression for the capacitance of a parallel-plate capacitor can be written as:

$$C = C_o A$$

where C_o is the capacitance per unit area and A is the area of one of the plates. The value of C_o is usually restricted to a narrow range (typically of the order of 0.05 pF/mil^2 to 0.5 pF/mil^2) due to the type of dielectric materials available in monolithic circuits and their voltage breakdown properties. Since the practical chip size of a monolithic circuit is dictated by yield considerations, this puts an upper limit on the value of capacitance which can be provided on the monolithic circuit. The basic classes of capacitor structures which are available are junction and thin film capacitors.

In a planar epitaxial integrated circuit, there are three separate junctions which can be used as capacitors. As shown in Figure 14, these are the base-emitter, base-collector, and collector-substrate capacitances associated with the integrated npn bipolar structure. Also shown in the figure is the resultant interconnection of these three capacitors, along with the ideal diodes in shunt with them to indicate the bias polarity requirements for each capacitor. Note that each capacitance also has a finite bulk resistance in series with it. Table I lists the typical values of C_o associated with each of these junctions, as a function of the reverse-bias voltage for an integrated device having a 10 Ω-cm p-type substrate and 5 Ω-cm n-type epitaxial layer, with the Gaussian and the complementary error function distribution for the base and the emitter diffusions. The emitter-base junction offers the highest capacitance per unit area; however, its low reverse breakdown voltage ($\tilde{}$ 7V) limits its use in some applications. The base-collector capacitance finds a wider range of applications than C_{EB} because of its high breakdown voltage (typically $\tilde{}$ 50V).

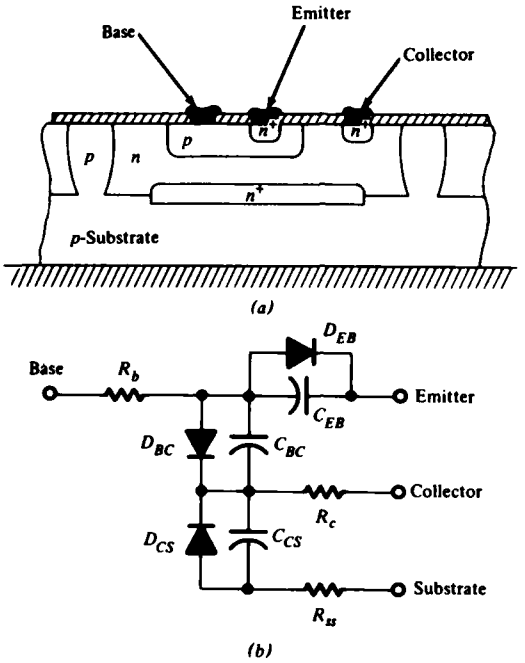


FIGURE 14. JUNCTION CAPACITANCES IN BIPOLAR INTEGRATED CIRCUITS
(a) PHYSICAL DEVICE STRUCTURE
(b) EQUIVALENT CIRCUIT OF JUNCTION CAPACITANCES

TABLE I

TYPICAL VALUES OF CAPACITANCE PER UNIT AREA
ASSOCIATED WITH INTEGRATED TRANSISTOR JUNCTIONS

Applied Voltage	Typical Junction Capacitance (pF/mil^2)			
	C_{EB}	C_{BC}	C_{CS} w/o $n+$ Layer	C_{CS} with $n+$ Layer
0 V	0.9	0.19	0.12	0.17
5 V	0.65	0.08	0.04	0.06
10 V	—	0.06	0.025	0.035

The thin film capacitor is a direct miniaturization of the conventional parallel-plate capacitor. It is comprised of two conductive layers separated by a dielectric. In integrated circuits, it can be fabricated in either one of two forms: (1) using a metal insulator semiconductor (MIS) structure as shown in Figure 15; or (2) using a thin dielectric layer between two metal layers as shown in Figure 16. The MIS structure of Figure 15 is the most commonly employed thin film capacitor in monolithic circuits, since it is readily

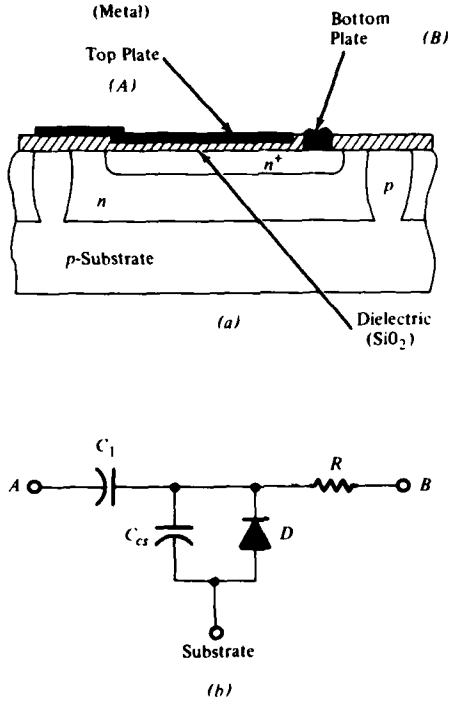


FIGURE 15. METAL INSULATOR SEMICONDUCTOR (MIS) CAPACITOR
(a) DEVICE STRUCTURE (b) EQUIVALENT CIRCUIT

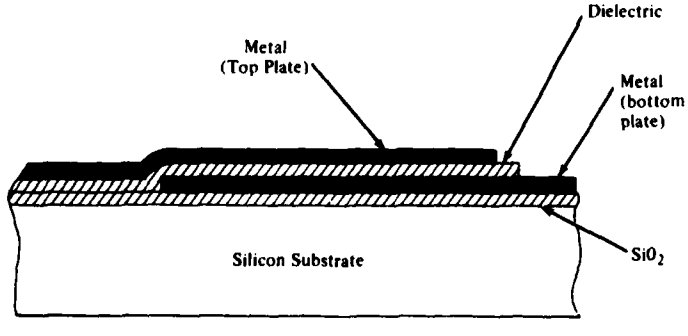


FIGURE 16. THIN-FILM CAPACITOR USING MULTIPLE METAL LAYERS

compatible with the conventional processing technology and does not require multiple metalization layers. In metal semiconductor structures, either SiO_2 or silicon nitride (Si_3N_4) can be used as a dielectric layer. The minimum thickness of the dielectric layer is set by the yield and process control requirements and is typically about 500 Å. The dielectric layer thickness usually is in the range of 800 to 1200 Å.

An alternate thin-film capacitor which uses a thin dielectric layer between two metal layers is illustrated in Figure 16. Although such a capacitor structure is virtually free from substrate parasitics, it requires a number of additional masking and deposition steps beyond the basic MIS structure. In such a structure one generally uses either aluminum or tantalum as the capacitor plates, with aluminum trioxide (Al_2O_3) or tantalum pentoxide (Ta_2O_5) as the dielectric material. Ta_2O_5 is particularly preferred for large value capacitors, since its dielectric coefficient is about an order of magnitude better than most other dielectrics used in thin-film capacitors. Typical failure mode of thin-film capacitors is breakdown of the gate dielectric when their voltage rating is exceeded. Table II gives a summary of the electrical characteristics of thin-film capacitors available in integrated circuits.

TABLE II

THIN-FILM CAPACITOR CHARACTERISTICS

	Dielectric Material			
	SiO_2	Si_3N_4	Al_2O_3	Ta_2O_5
Capacitance (pF/mil²)	0.25–0.4	0.5–1.0	0.3–0.5	2–3.5
Relative dielectric constant (ϵ_r)	2.7–4.2	3.5–9	4–8.5	24–28
Breakdown voltage (V)	50	50	20–40	20
Absolute tolerance (%)	±20	±20	±20	±20
Matching tolerance (%)	±3	±3	±5	±5
Temperature coef. (ppm/°C)	+15	+4–+10	+300	+200–+500
Q (at 10 MHz)	25–80	20–100	10–100	10–100

b) Integrated Resistors. Two general classes of resistors are available in monolithic circuits: semiconductor and thin-film. The semiconductor resistors in turn can be categorized into any one of the following four groups, based on their physical structure:

(a) Diffused resistors
(b) Bulk resistors
(c) Pinched resistors
(d) Ion-implanted resistors

Semiconductor resistors are by far the most commonly used monolithic resistor structures. With the exception of the ion-implanted resistors, they can be fabricated simultaneously with the rest of the circuit elements, without requiring extra processing steps.

A diffused resistor structure is formed by the bulk resistance of a diffused semiconductor region. In forming a monolithic resistor, the two basic diffusion cycles, i.e., the base or the emitter diffusions, can be utilized. Figure 17 shows a typical geometry and the cross-section of a p-type diffused resistor obtained using the npn base diffusion step. Table III shows typical values of the absolute value and ratio tolerances for diffused resistors fabricated during the base diffusion cycle.

The bulk resistance of the n-type epitaxial layer can be used in some applications to form a noncritical high value resistor. This can be done by using a structure as shown in Figure 18. Since the bulk resistor is formed by the epi-isolation junction, its breakdown voltage is also substantially higher than that for the diffused resistor structure. The sidewalls of the bulk resistor are formed by the deep isolation diffusion which diffuses sideways, as well as downward during the diffusion cycles. The absolute value tolerances for a bulk resistor are quite loose due to relatively poor control of the epi resistivity ($\pm$20 percent) and epitaxial layer thickness ($\pm$10 percent). Thus, practical absolute value tolerances for a bulk resistor are typically $\pm$30 percent.

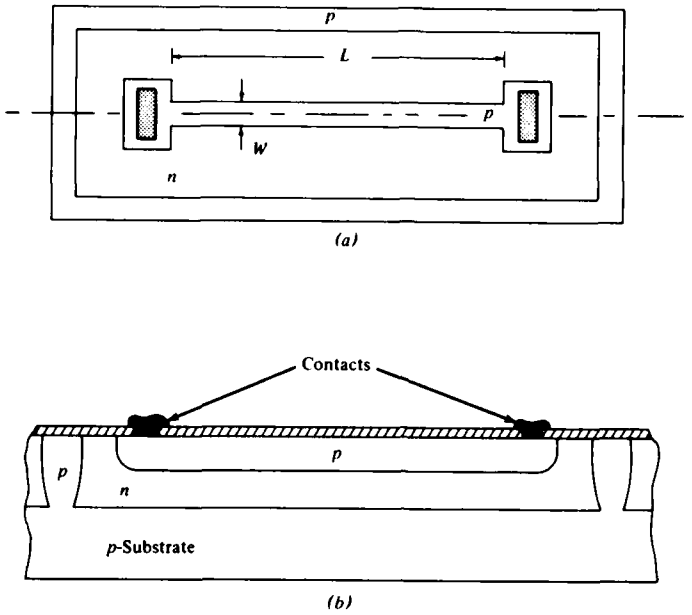


FIGURE 17. BASIC DIFFUSED RESISTOR STRUCTURE
(a) LATERAL GEOMETRY
(b) CROSS-SECTION

TABLE III

TOLERANCES ASSOCIATED WITH A DIFFUSED RESISTOR

Resistor Width	Absolute Value Tolerance	Ratio Tolerance	
		1:1	5:1
W = 7 μ	±15%	±2%	±5%
W = 25 μ	±8%	±0.5%	±1.5%

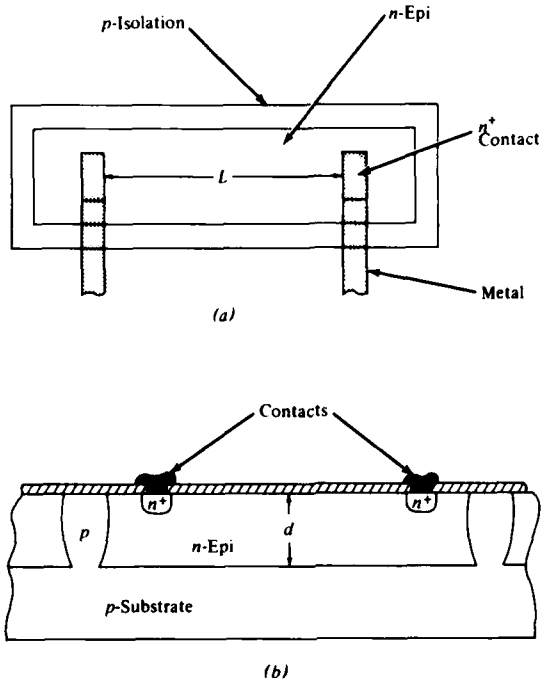


FIGURE 18. BULK RESISTOR: (a) LATERAL GEOMETRY; (b) CROSS-SECTION

The sheet resistivity of a semiconductor region can be increased by reducing its effective cross-section area. In a pinched resistor structure, this technique is used to obtain a high value sheet resistance from the ordinary base-diffused resistor. Figure 19 shows such a resistor structure formed by placing an n^+-type emitter diffusion over the p-type diffused resistor. The emitter diffusion greatly reduces the effective cross-sectional area of the p-type resistor and consequently raises its sheet resistivity. It should be noted that the effective depth of such a pinched resistor structure is equal to W_b, the npn transistor base width. Typical values of sheet resistivity, R_s, of a pinched resistor are in the range of 5 to 10K Ω. Figure 20 shows the circuit designation and the current-voltage characteristics for a pinched resistor. The current-voltage characteristics of the pinched resistor are linear only for small voltage drops across the resistor. Application of a higher dc voltage results in an increase

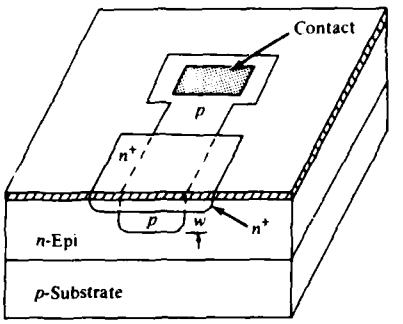


FIGURE 19. STRUCTURAL DIAGRAM OF A PINCHED RESISTOR

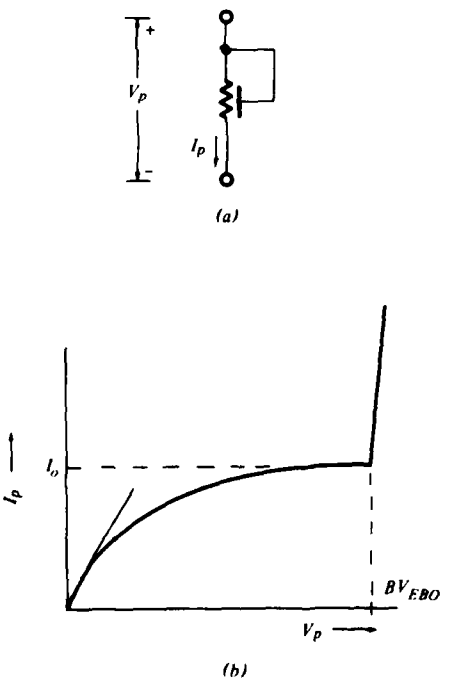


FIGURE 20. PINCHED-RESISTOR: (a) ITS ELECTRICAL SYMBOL; (b) CURRENT-VOLTAGE CHARACTERISTICS

of reverse bias between the p-type resistor body and the surrounding n-type island. This reverse bias causes the junction depletion layer to extend into the resistor, and "pinch" the effective resistor cross-section, in a manner similar to the case of a junction-gate FET. Since the top portion of the pinched resistor is comprised of the heavily doped emitter diffusion, the resistor exhibits a low breakdown voltage, equal to the transistor emitter-base breakdown, BV_{EBO} (typically 6 to 8 V).

The "buried FET" structure of Figure 21 provides an alternate method of obtaining high value resistors without the breakdown limitations of the base-diffused pinch resistor. In this case, the channel of the buried FET, which constitutes the body of the resistor, is formed by the n-type epitaxial region surrounded on all sides by the p-type substrate, isolation, and the base diffusion. Since all pn junctions forming the buried FET structure are lightly doped, the breakdown voltage associated with the device is quite high, typically of the order of transistor base-collector breakdown voltage.

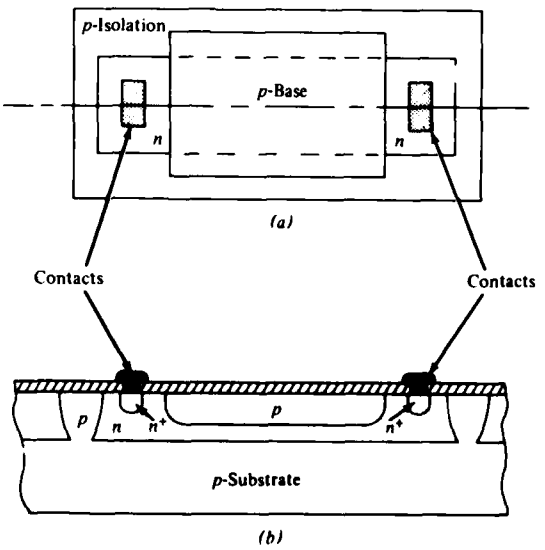


FIGURE 21. BURIED FET STRUCTURE: (a) DEVICE LAYOUT; (b) CROSS-SECTION

Ion-implantation techniques can be utilized to form resistor structures on the semiconductor surface. With this technique, the impurities are introduced into the silicon lattice by bombarding the wafer surface with high energy ions. The implanted ions lie within a very shallow layer (typically of the order of 0.1 to 0.8 μ) along the silicon surface. Thus, for similar doping levels, the implanted layers yield a sheet resistivity which is roughly 20 times higher than a corresponding doped diffused layer of 2 to 4 μ thickness. In fabricating ion-implanted resistors, normally boron-implanted p-type resistor structures are used. Figure 22 shows the planar layout and the cross-section diagram of a p-type ion-implanted resistor. Due to the

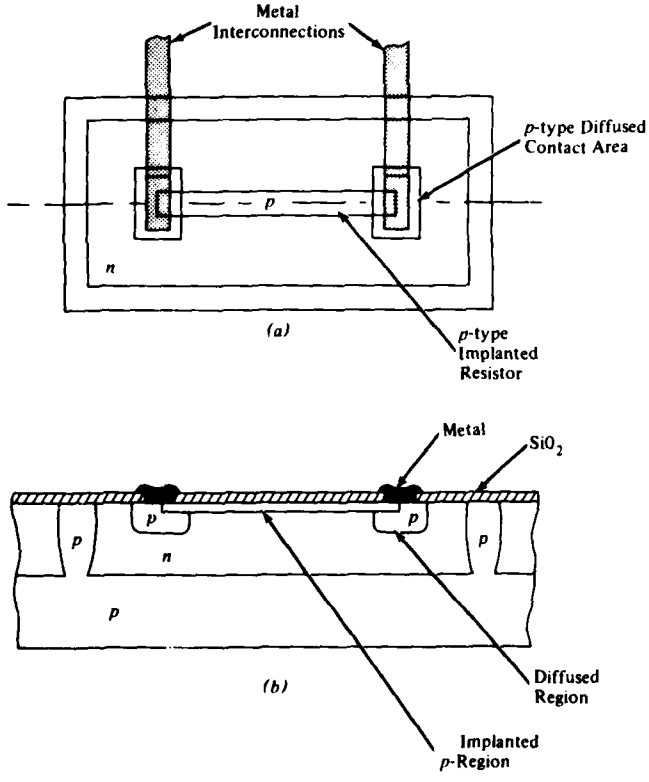


FIGURE 22. ION-IMPLANTED RESISTOR: (a) LATERAL GEOMETRY; (b) CROSS-SECTION

shallow depth of the ion-implanted resistor, it is difficult to obtain a good ohmic contact to the implanted region. Therefore, p-type diffused beds are used at the contact areas of the resistor as shown in Figure 22. At high values of sheet resistivity, i.e., R_s >10KΩ, the implanted resistors exhibit JFET-like characteristics due to the pinching off of the resistor by the resistor-substrate depletion layer.

Resistive thin film layers can be deposited and patterned on a silicon dioxide surface. Compared with the diffused resistors, thin films offer the following advantages:

(a) Low temperature coefficient
(b) Tighter absolute value control
(c) Lesser parasitics
(d) Higher sheet resistivity

The main disadvantage of thin-film resistors is the additional process steps required in their fabrication. In some cases, in addition to the basic deposition and patterning steps, an additional SiO_2 deposition is necessary to stabilize the resistor structure by sealing it off from the ambient atmosphere. The most commonly used thin-film resistors in integrated circuits are tantalum (Ta), nickel-chromium (Ni-Cr), and tin oxide (SnO_2). Table IV gives a summary of the basic properties of each of these thin-film resistors. The thin-film resistors should always be laid out over a smooth region of the surface oxide layer, with no steps or sudden changes of the oxide layer.

TABLE IV
CHARACTERISTICS OF THIN-FILM RESISTORS

Characteristic	Ta	Ni-Cr	SnO_2
Sheet resistance (ohm/square)	200–5000	40–400	80–4000
Temperature coefficient (ppm/°C)	100	100	0 to −1500
Absolute value tolerance	±5%	±5%	±8%
Matching tolerance	±1%	±1%	±2%
Breakdown voltage	200 V	200 V	200 V

3. Bipolar Circuit Implementations. A silicon integrated circuit consists of several regions, each containing one or more circuit elements, which are interconnected according to a specified network topology. Some method of isolation is necessary to prevent undesired electrical interconnection between regions in the same silicon substrate. For bipolar circuits, the simplest and most popular scheme is known as junction or diode isolation. The isolation is provided by the reverse-biased p-n junction, which is formed between the substrate and the isolation island when the substrate is connected to the most negative potential, as shown in Figure 23. There is a parasitic depletion-layer capacitance and a leakage current associated with the isolating junction.

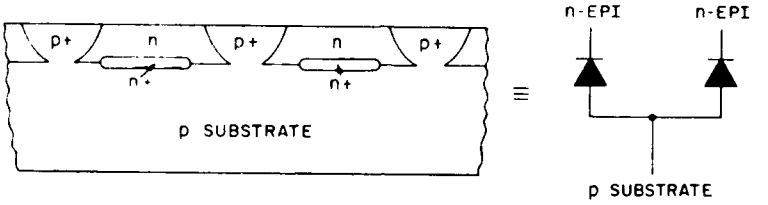


FIGURE 23. CROSS SECTION OF THE JUNCTION-ISOLATED MONOLITHIC STRUCTURE AND THE EQUIVALENT ELECTRICAL CIRCUIT

Another technique for producing integrated transistors is the oxide isolation process. A thin layer of silicon dioxide, as shown in Figure 24, replaces the pn junction around the collector region. In terms of transistor electrical characteristics, this technique is superior to the pn junction isolation technique, because

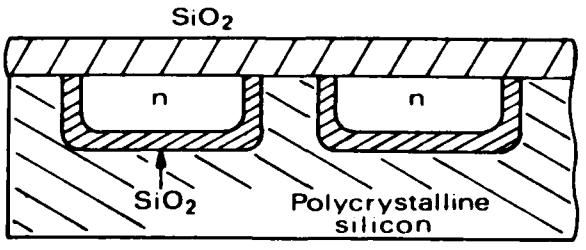


FIGURE 24. OXIDE ISOLATION TECHNIQUE

parasitic collector-to-substrate capacitance is reduced substantially, and pnp parasitic action is eliminated.

a) Transistor-Transistor Logic (T^2L). Transistor-transistor logic (TTL or T^2L) is probably the most popular type of integrated circuit logic. It is a type of saturating logic, so called because some of the transistors are allowed to saturate under certain conditions. There is no discrete component counterpart for T^2L. It was developed in the course of simplifying the design and improving the performance of integrated circuit diode-transistor logic (DTL). There are several varieties of T^2L circuits, but the one basic feature they all have in common is the two-transistor arrangement shown in the lower left of Figure 25, which is a positive NAND gate. These two transistors give the family its name: transistor-transistor logic. One transistor has a separate emitter region for each input. Figure 26 shows an example of the most compact form of T^2L logic: the layout for a four-input NAND expander gate.

Input and output voltages in T^2L circuits vary depending on the design and process used. Table V lists the various input and output voltages for the standard, low power, and Schottky T^2L. Low power T^2L offers certain advantages to the designer over standard T^2L. This type of logic has derived from medium-scale and small-scale integration of standard T^2L by effectively increasing all resistors by a factor of 4, thus reducing all current and power consumption. The drawback of low power T^2L is that it is slower than standard T^2L devices. Schottky T^2L has a speed-power product intermediate between standard T^2L and emitter-coupled logic (ECL). To obtain the fastest circuit operation, a transistor must be prevented from entering the saturation region. This condition can be achieved, as indicated in Figure 27a, by using a Schottky diode as a clamp between the base and collector. If an attempt is made to saturate this transistor by increasing the base current, the collector voltage drops, D conducts, and the base-to-collector voltage is limited to about 0.4V. Since the collector junction is forward-biased by less than the built-in voltage ($\simeq$ 0.5V), the

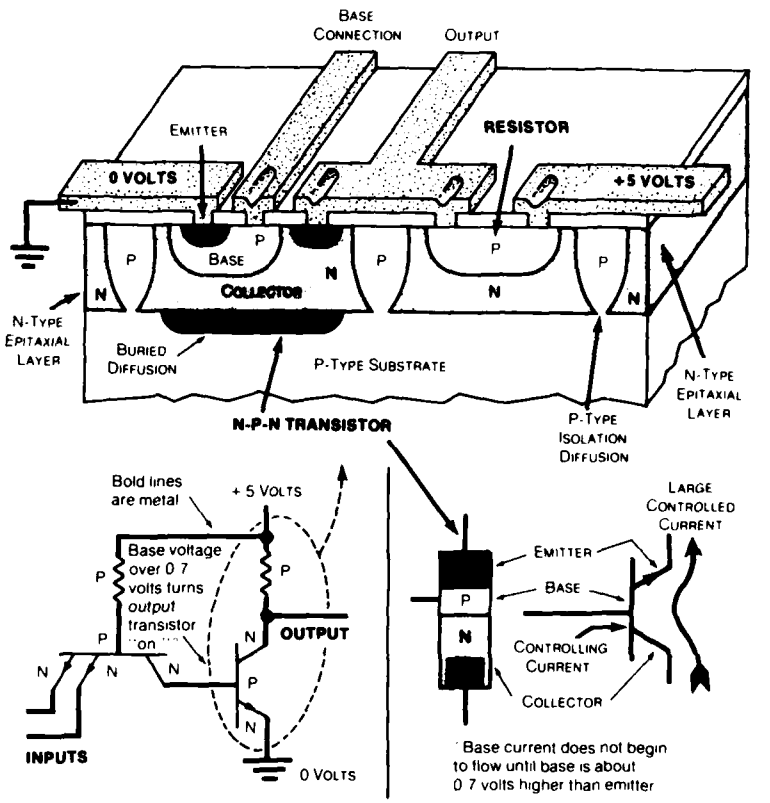


FIGURE 25. BASIC TTL POSITIVE NAND GATE, SHOWING SIMPLIFIED CUTAWAY VIEW OF ONE TRANSISTOR AND A RESISTOR IN AN IC CHIP

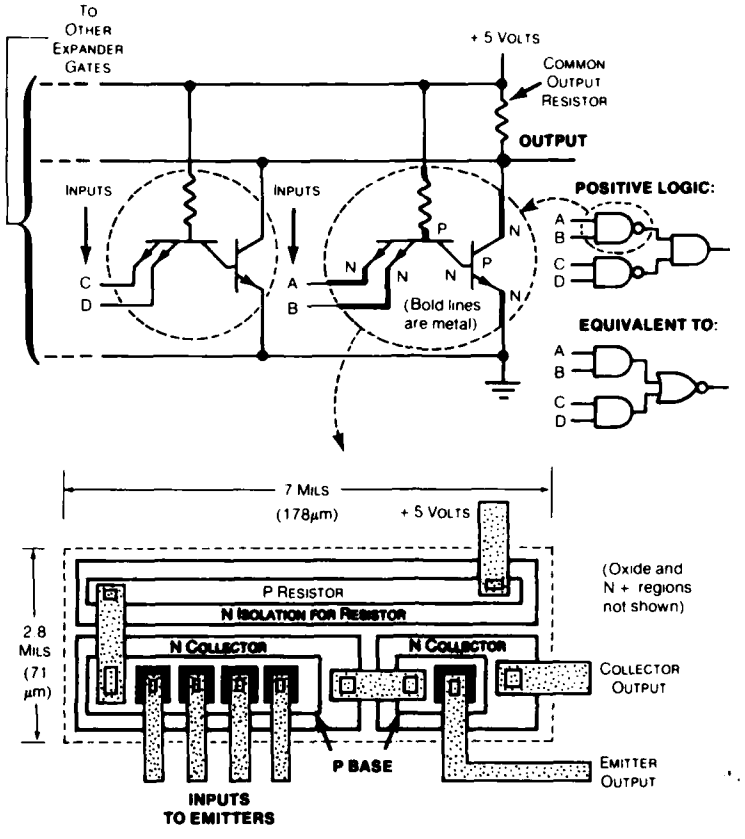


FIGURE 26. MOST COMPACT FORM OF TTL LOGIC: POSITIVE NAND "EXPANDER" GATES WITH COMMON OUTPUT RESISTOR (2-INPUT VERSIONS ABOVE, 4-INPUT CHIP LAYOUT BELOW)

TABLE V

T^2L INPUT/OUTPUT VOLTAGES

	STANDARD AND HIGH-SPEED TTL	LOW-POWER TTL	SCHOTTKY TTL
Maximum low-level output voltage, V_{OLmax}	0.4	0.3	0.5
Minimum high-level output voltage, V_{OHmin}	2.4	2.4	2.5
Maximum low-level input voltage, V_{ILmax}	0.8	0.7	0.8
Minimum high-level input voltage, V_{IHmin}	2.0	2.0	2.0

transistor does not saturate. Note that the fabrication of a Schottky diode is actually simpler than that of a p-n diode, which requires an extra (p-type) diffusion. As indicated in Figure 27b, the aluminum metallization for the base lead is allowed to make contact also with the n-type collector region (but without an intervening n^+ section). This simple procedure forms a metal-semiconductor diode between base and collector. This is referred to as a Schottky transistor and is represented by the symbol in Figure 27c. Figure 28 illustrates a two-input NAND gate designed with Schottky devices.

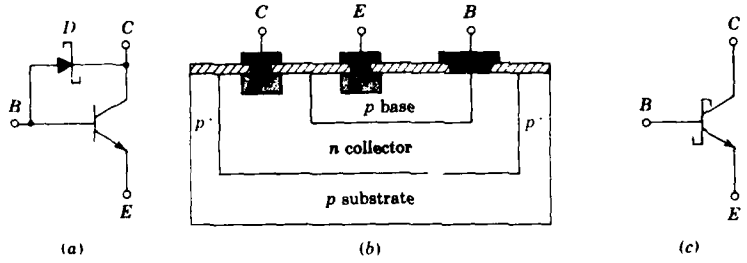


FIGURE 27. (a) A TRANSISTOR WITH A SCHOTTKY-DIODE CLAMP BETWEEN BASE AND COLLECTOR TO PREVENT SATURATION; (b) THE CROSS SECTION OF A MONOLITHIC IC EQUIVALENT TO THE DIODE-TRANSISTOR COMBINATION IN (a); (c) THE SCHOTTKY TRANSISTOR SYMBOL, WHICH IS AN ABBREVIATION FOR THAT SHOWN IN (a)

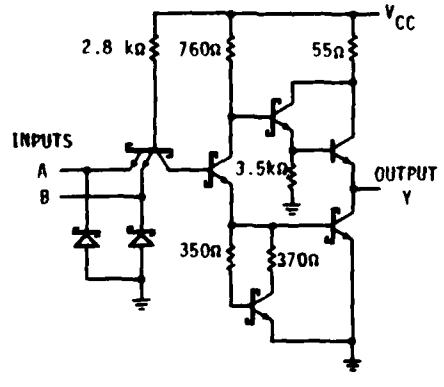


FIGURE 28. TWO-INPUT SCHOTTKY NAND GATES

Emitter-coupled logic (ECL) offers advantages and capabilities to the designer of high speed digital systems. High switching rates at relatively low power consumption, short propagation delays with slow edge rates, and the ability to drive low-impedance interconnections are some of the ECL features. Emitter coupled logic is a non-saturating form of digital logic which eliminates transistor storage time as a speed limiting characteristic. "Emitter coupled" refers to the manner in which the emitters of a differential amplifier within the integrated circuit are connected. The differential amplifier provides high impedance inputs and voltage gain within the circuit. The emitter follower outputs restore the logic levels and provide low output impedance for good line driving and high fanout capability. An improved ECL switch which can perform additional logic functions is shown in Figure 29.

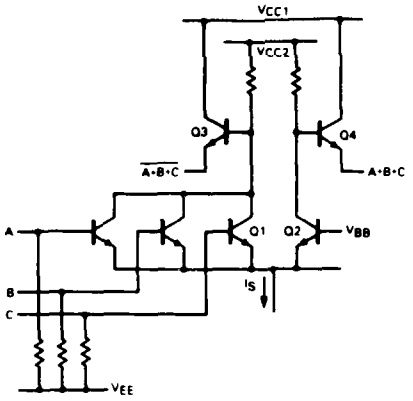


FIGURE 29. IMPROVED ECL SWITCH

A rather recent development in the logic family, is Integrated-Injection Logic (I^2L), which offers several advantages over T^2L and ECL. Although it may not be as fast as they are, it is easier and cheaper to fabricate. The basic building gate of I^2L is shown in Figure 30. It is a single input, multiple output inverter. Most terminals of the I^2L gate share the same semiconductor region (e.g., the collector of the pnp is the same as the base of the npn, and the

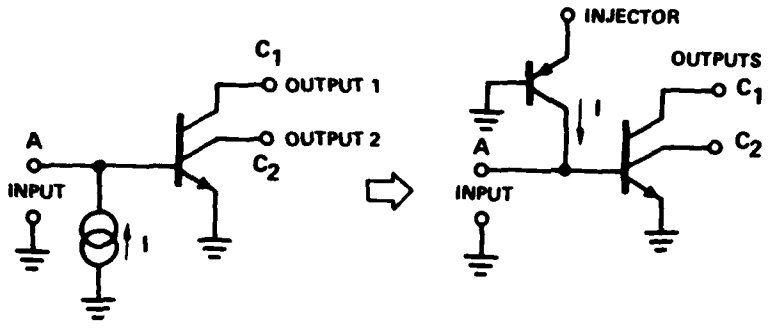


FIGURE 30. SINGLE INPUT, MULTIPLE OUTPUT INVERTER

emitter of the npn is the same as the base of the pnp). This leads to a very compact device structure, and results in very high packing density in monolithic device fabrication. Figure 31 shows the basic device cross section for a two-output gate. This basic structure can

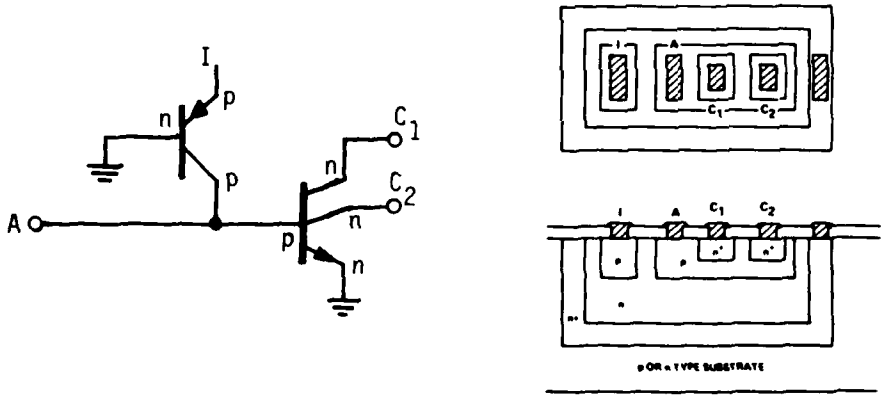


FIGURE 31. BASIC DEVICE CROSS SECTION FOR A TWO-OUTPUT GATE

be made compatible with basic bipolar IC technology by using a silicon p-type substrate as the semiconductor starting material. The bipolar compatible I^2L device structure is shown in Figure 32. A size comparison of the basic four-output I^2L gate, with a four-input T^2L gate, each fabricated with th same masking tolerances, is shown in Figure 33. Note that the I^2L offers a 5-to-1 reduction in gate area.

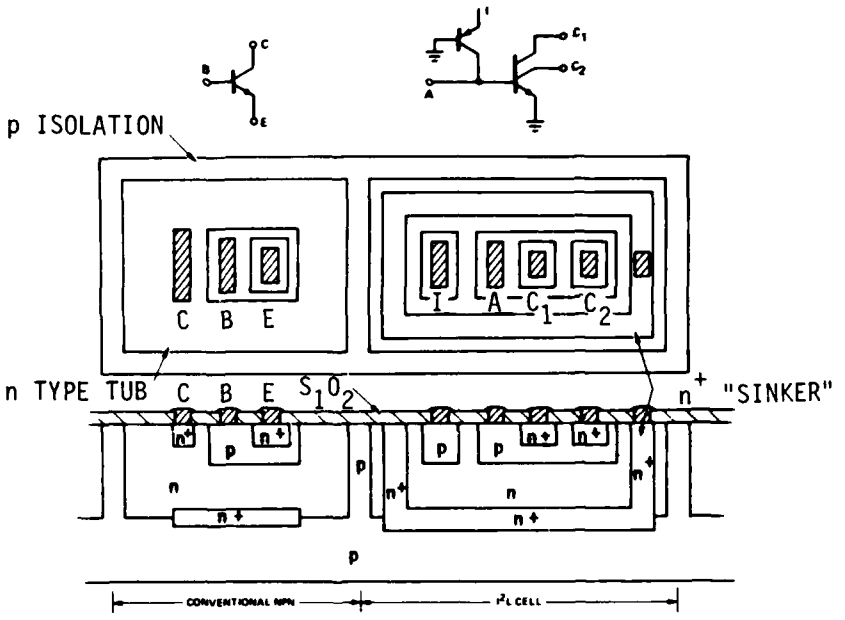


FIGURE 32. BIPOLAR COMPATIBLE I^2L DEVICE STRUCTURE

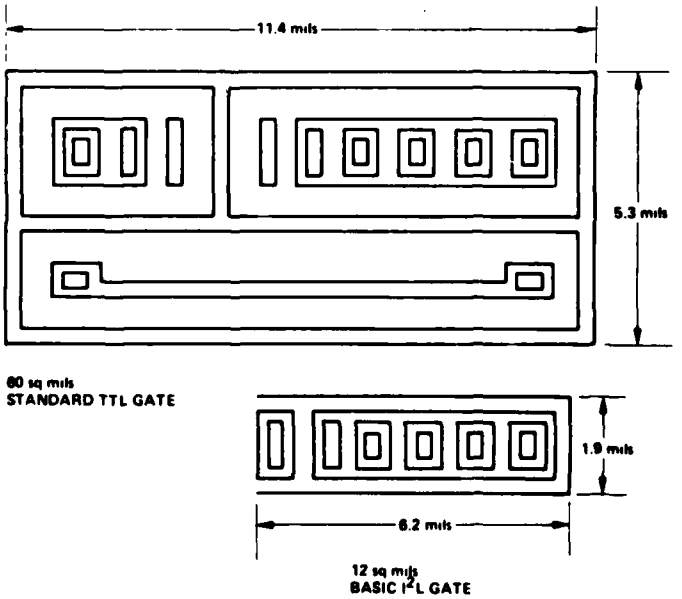


FIGURE 33. BASIC FOUR-OUTPUT I^2L GATE, WITH A FOUR-INPUT T^2L GATE

To obtain Schottky I^2L, the base and emitters of conventional I^2L must be modified. For example, in one approach, a deep p-type base implant forms the active base of the vertical npn transistor, while the doping of the n-type region is maintained at the surface to provide for the formation of the Schottky diodes as shown in Figure 34. This approach has the disadvantage of reducing noise margin. In fact, both noise margin and signal swing are reduced by the

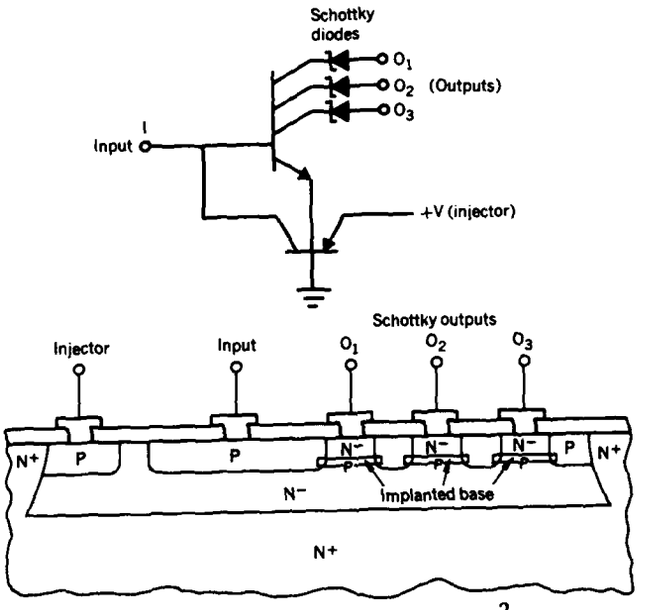


FIGURE 34. SCHOTTKY I^2L

same amount (the forward voltage of the Schottky diode). As a result, the usual one-level metal system, with its diffused silicon cross-unders, becomes marginally acceptable for Schottky I^2L. Noise immunity can be preserved by use of a two-level metal interconnect system, which avoids parasitic voltage drops in diffused cross-unders that are responsible for the noise-margin loss. Schottky I^2L also improves intrinsic gate delay by reducing a downward injection of minority charge into the lateral extremities of the pnp device. An often understressed advantage of I^2L results from the logic's low-voltage (less than 1 volt) operation. It actually enhances reliability by avoidance of electro corrosion, which occurs in the presence of humidity and electrolytic contaminants although chemical corrosion would be unaffected. Impressive reliability results have been demonstrated on nonhermetic LSI devices employing I^2L.

Isoplanar Integrated Injection Logic (I^3L) is an example of an advanced I^2L process. It uses oxide guard rings to prevent parasitic p-n-p action between adjacent gates and ion implantation to produce doping profiles that are tailored to I^2L devices. The performance is further improved by designing the p-n-p injector to have a high gain and by the use of antisaturation clamps. An interesting circuit technique called "graduated collectors" is used to overcome the decrease in β of the collectors far away from the injector in the "stick" geometry shown in Figure 35. If collector areas are equal, the current gain at collector 4 is less than that of collector 1. In the graduated collector scheme, the collector areas are adjusted such that the upward gain of all collectors is equal at some reasonable value of injector current for LSI circuits, for example, 500 μA.

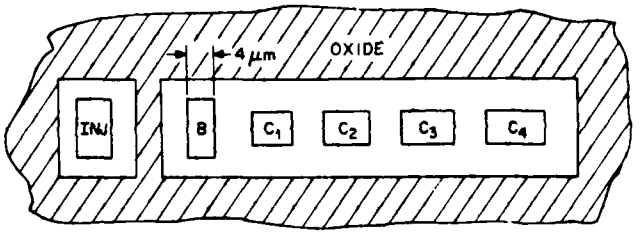


FIGURE 35. TOP VIEW OF AN I^3L STICK TRANSISTOR WITH GRADUATED COLLECTORS

4. Field Effect Devices. The principle of operation of the field-effect transistor (FET) differs significantly from that of the bipolar type. In the case of the FET, the current transport or conduction mechanism within the device relies solely on majority carriers. Therefore, the name "unipolar transistor" is also used interchangeably with the name FET, to distinguish it from the bipolar transistor, where both majority and minority carriers actively participate in the current transport process. A detailed coverage of the FET device theory is readily available in the bibliography of this section and will not be repeated here. Instead, this section is aimed at covering the salient features and properties of integrated FET structures. The FET is a voltage-controlled device where the current conduction between source and drain regions is controlled or modulated

by means of a control voltage applied to the gate terminal. Depending on the physical structure of the gate region, the FET's can be classified into two categories: (1) junction-gate (JFET) and (2) insulated gate (IGFET) devices. In the following sections, the physical structure and some of the characteristics of each type will be examined separately.

a) Junction Gate FET. Figure 36 shows a cross-section diagram of an integrated JFET with n-type channel region. In the structure of such a device, the reverse bias is applied to the gate-channel depletion layer so as to extend it into the channel region and modulate the effective width of the conductive path between the source and the drain. The reverse bias across the junction necessary to cause the depletion region to extend into the channel from both gates far enough to totally deplete or "pinch" the channel is known as the pinch-off voltage V_p. Referring to the dc voltage levels defined in Figure 36, for low values of the drain potential, the ohmic drop along the channel due to the flow of the drain current I_D is negligible, and the JFET operates as a voltage-controlled resistor. At any given gate bias $V_G < V_p$, as the drain voltage is increased, the drain current also increases, thus increasing the ohmic drop along the channel. For drain voltages in excess of

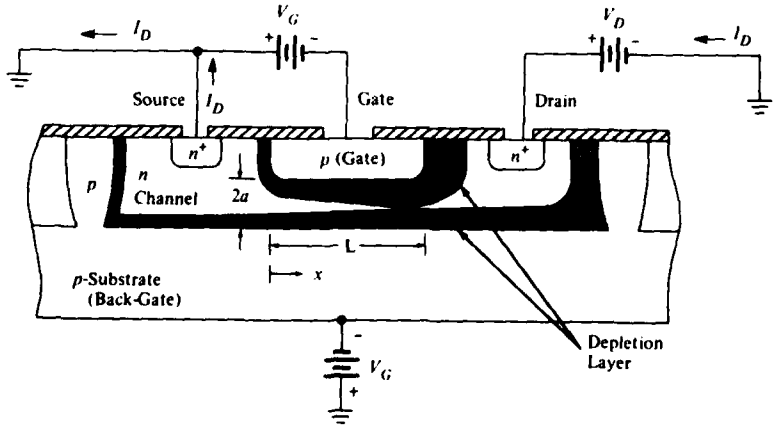
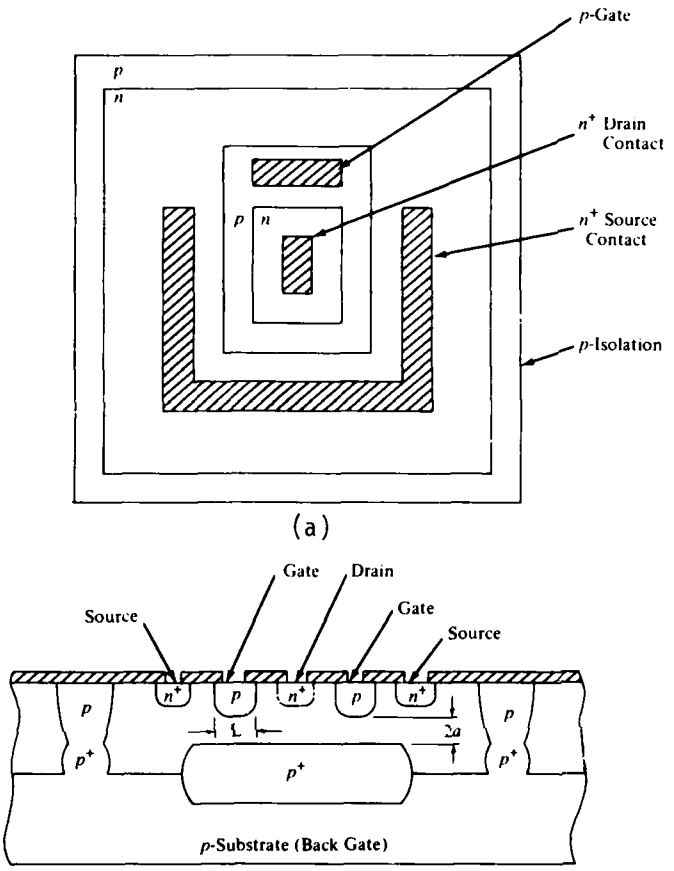


FIGURE 36. STRUCTURAL DIAGRAM OF AN n-CHANNEL JFET (CROSS-HATCHED REGIONS DENOTE GATE-CHANNEL DEPLETION LAYER)

the pinch-off voltage, a space charge region is formed near the drain end of the channel. This space charge layer then causes I_D to reach a saturation level and be relatively insensitive to the further increase of the drain potential. This is known as the "pinched" operation of the FET, where the device functions as a voltage-controlled current source.

The parasitic bulk resistances R_S and R_D at the source and drain end of the channel, between the active channel region and the external source and drain contacts, introduce an additional ohmic drop within the FET. The exact values of R_S and R_D depend on the channel resistivity and the geometrical layout of the device. For practical FET structures compatible with monolithic circuits, the values of R_S and R_D are in the range of 30 to 30 Ω. The high voltage capability of the JFET is determined by the avalanche breakdown of the gate-channel junction, BV_{GC}. The drain-source breakdown voltage BV_{DS} is slightly less than the gate-channel breakdown due to the additional reverse bias provided by the gate voltage (reference Figure 36). For typical integrated FET structures, using the n-type collector region of the epitaxial npn transistor, the gate-channel breakdown is the same as the collector-base breakdown BV_{CBO}, associated with the integrated npn transistors.

b) Integrated JFET Structures. For monolithic integrated circuits, the most useful JFET structures are those which are compatible with the npn bipolar technology and can be fabricated simultaneously with npn transistors. Figure 37 shows the layout and the cross-section of an n-channel JFET structure which is readily compatible with the bipolar diffusion schedules. This device uses the n-type epitaxial collector region of the npn transistor as the channel of the FET. Similarly the p-type base diffusion of the npn transistor is used to form the control gate with the source and drain contacts formed by the n^+ emitter diffusions for the npn transistor. To obtain a narrow channel width without degrading the npn bipolar breakdown characteristics, a p^+ subepitaxial layer is diffused under the FET gate region, as well



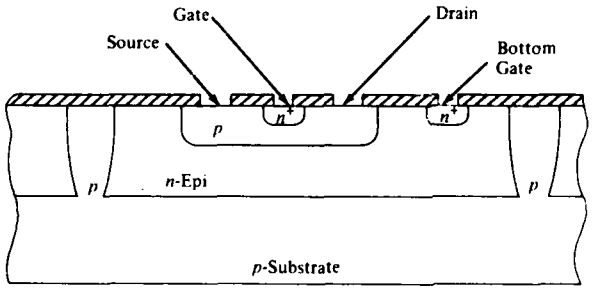
37. LAYOUT AND CROSS-SECTION OF n-CHANNEL JFET COMPATIBLE WITH npn BIPOLAR TRANSISTORS

the isolation walls. Then, during the isolation diffusion, pitaxial p^+ layer out diffuses into the epitaxial layer and ıe effective channel width of the n-channel FET. In such a , the p-type substrate is also a part of the FET gate. How-ːe the substrate is common to the rest of the circuit, it cannot ; a control terminal. Therefore, only the top gate functions ıtrol electrode, and the bottom one is at all times connected l negative potential, with respect to the rest of the device.

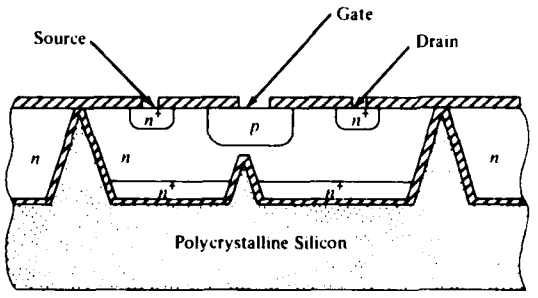
Two additional JFET structures which are also compatibl ıpn bipolar technology are shown in Figure 38. The structure 38(a) is a p-channel device, with a diffused channel region.

The p-type channel region can be either formed by npn base diffusion or by an additional p-diffusion step resulting in a deeper junction structure. If the ordinary base and emitter diffusions of npn transistors are used to form the p-channel FET, the resulting device is referred to as a "pinched-resistor." Since the transistor base-emitter junction is used as the gate-channel junction of the FET, such a device has a very low voltage breakdown, with $BV_{GD} = BV_{EBO} \simeq 7$ volts.

The structure of the device in Figure 38(b) is particularly suitable for high frequency applications and uses dielectric isolation and an isotropic etch technique. The gate and the source and drain contacts are again formed by the npn base and emitter diffusions. The channel is formed by a wedge-shaped groove etched under the gate region. To obtain such a sharp "V"-shaped groove, isotropic etching methods are used. Using such a device, it is possible to reduce the (width/length) ratio of the channel to approximately unity and thus greatly increase the cutoff frequency.



(a)



(b)

FIGURE 38. OTHER JFET STRUCTURES COMPATIBLE WITH INTEGRATED CIRCUITS

c) Insulated-Gate FET. In an insulated-gate FET structure, (IGFET) a thin dielectric barrier is used to isolate the gate and the channel. The control voltage applied to the gate terminal induces an electric field across the dielectric barrier and modulates the free carrier concentration in the channel region. The IGFET structures can be classified as p-channel and n-channel devices, depending on the conductivity type of the channel region. In addition, these devices can also be classified according to their mode of operation as "enhancement" or "depletion" type devices. In a depletion-mode FET, a conducting channel exists under the gate, with no applied gate voltage. The applied gate voltage controls the current flow between the source and the drain by depleting a part of this channel. This is very similar to the operation of the JFET described previously. In the case of the enhancement-mode IGFET, no conductive channel exists between the source and the drain at zero applied gate voltage. As a gate bias of proper polarity is applied and increased beyond a threshold value V_T, then a localized inversion layer is formed directly below the gate; this serves as a conducting channel between the source and the drain electrodes. If the gate bias is increased further, the resistivity of the induced channel is reduced and the current conduction from the source to the drain is enhanced. Figure 39 shows a cross-section diagram of a p-channel enhancement-mode IGFET. The particular polarities of the gate and drain bias for the proper operation of the device are also identified on the figure. Normally an SiO_2 layer is used as the gate dielectric. The thickness of this oxide layer is normally much less than the oxide layers commonly used for masking or surface passivation. The enhancement-mode IGFET is preferred over its depletion-mode counterpart because it is a "self-isolating" device, does not require tight control of diffusion cycles, and can be fabricated by a single diffusion step forming the source and drain pockets. Since all the active regions of the IGFET are reverse-biased with respect to the substrate, adjacent devices fabricated on the same substrate are electrically isolated, without requiring a separate isolation diffusion.

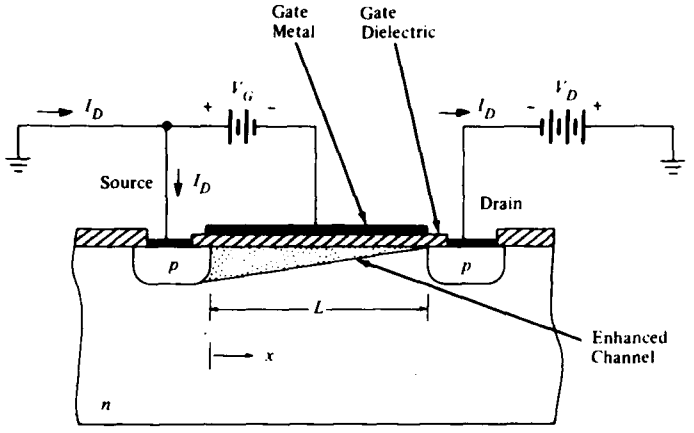


FIGURE 39. CROSS-SECTION OF A p-CHANNEL ENHANCEMENT-MODE IGFET

d) Integrated IGFET Structures. The p-channel enhancement device is the simplest insulated-gate FET structure which can be fabricated simultaneously with npn bipolar transistors, without requiring additional diffusion cycles. In such a device, the n-type collector and the p-type base regions of the npn are used as the "substrate" and the source and drain pockets for the IGFET. Figure 40 shows the layout of a typical p-channel enhancement device which can be fabricated in this manner. The channel length L is determined by the final separation between the source and the drain pockets; and it is normally chosen to be $\geq$ 5μ to avoid punch-through breakdown between the source and the drain. Typically the source and drain diffusion windows are 12μ apart, and if the pockets are diffused to a depth of 4μ, the resulting channel length is approximately 6μ. Furthermore, in an enhancement mode FET, the gate metal layer must overlap the source and drain pockets to form a continuous channel. The threshold voltage, V_T, is a strong function of the cleanliness of the device surface. To obtain repeatable and stable values of V_T also requires that the gate dielectric be free of ionic contamination. With present day process technology, typical values of V_T are in the range of 2.5 to 3 volts, with a gate oxide thickness of approximately 1500 Å and a substrate resistivity of 4 to 6 Ω-cm. The minimum gate oxide thickness is

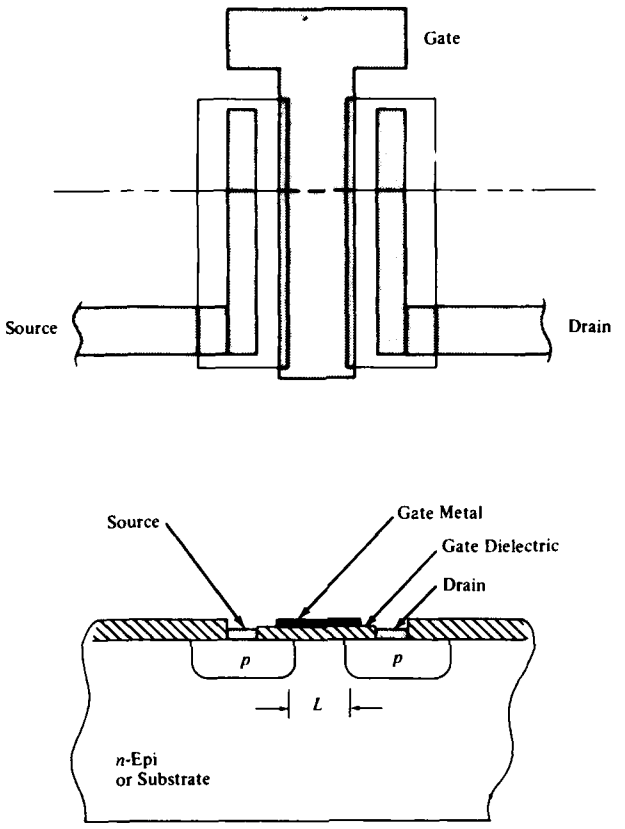


FIGURE 40. TYPICAL DEVICE LAYOUT FOR A p-CHANNEL IGFET

set by the voltage breakdown requirements of the gate electrode. If SiO_2 is used as the gate dielectric, the typical values of V_{GB} are of the order of 40 to 60 volts for the gate oxide thickness of $\simeq$ 1000 Å. In an IGFET, the gate breakdown results in a permanent damage to the gate dielectric; therefore, it is a destructive failure mechanism. Hence, in circuit applications and in handling of the device, proper precautions must be taken to protect the gate electrode from transient voltage spikes.

e) Complementary MOS Structures. Complementary MOS (CMOS) is the most complex MOSFET process because both n-channel and p-channel devices are made on the same chip. A typical CMOS process

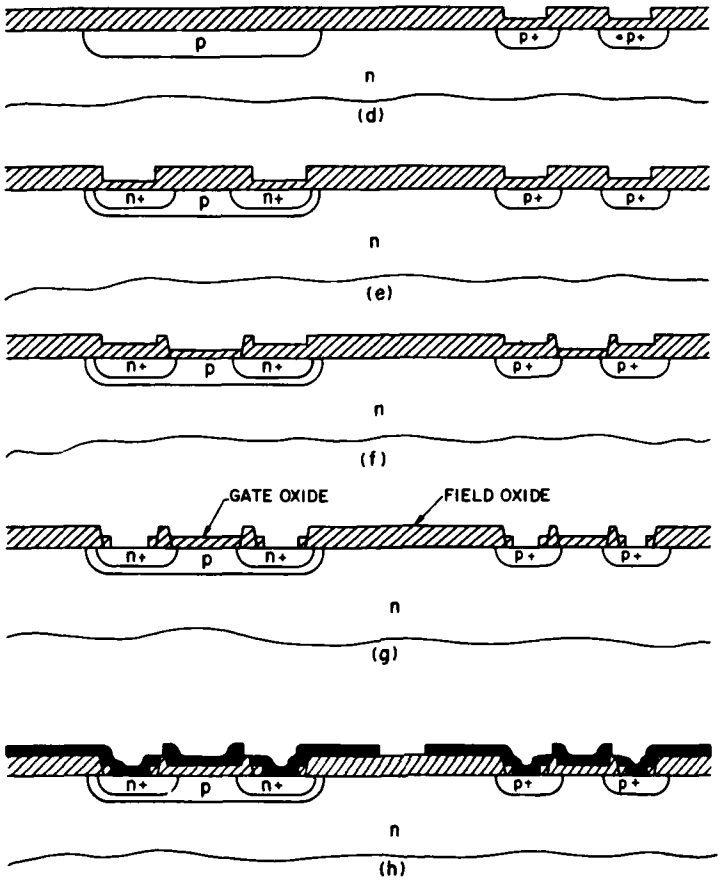
begins with n-type (100)-silicon wafers of about 5 Ω-cm resistivity. The n-type material is the background for the p-channel enhancement-mode transistors. The substrate is n-type because the p-type substrate required for n-channel devices must be more heavily doped than the n substrate required for complementary transistors with equal threshold voltages. It is easier to dope the n-type substrate to form p wells than the converse. The first task is to form wells of p-type material of about 3 to 5 Ω-cm resistivity. Next are the p^+ source and drain diffusions. The next step is the n^+ source and drain diffusion for the n-channel transistors. The resulting CMOS structure is shown in cross-section in Figure 41.

f) Other Processing Methods. There are a number of other MOS processing methods that the failure analysis should recognize in cross-section form. One of these is the Metal-Nitride-Oxide Semiconductor (MNOS) process. This process uses a silicon nitride (Si_3N_4) as the dielectric material to reduce the threshold voltage, V_T, on top of a thin layer of SiO_2. There are also silicon-gate as well as self-aligning gate structures. Other processes the analyst may encounter are:

RMOS (Refractory metal-oxide-semiconductor)
SATO (Self-aligning thick-oxide)
DMOS (Double-diffused MOS)
VMOS (V-shaped MOS)

The silicon-on-sapphire (SOS) MOS structure is shown in Figure 42. The major advantage of silicon-on-sapphire circuits is that the silicon can be selectively removed from those areas where it is not an active part of the circuit, thus reducing parasitics and increasing speed. The SOS process does have, however, a number of unsolved problems associated with it.

There are some unique input protection techniques for MOS devices with which the failure analyst should be familiar. Figure 43 shows some of the protective devices used on MOS device inputs which



(d) After p^+ source-and-drain diffusion; (e) after the n^+ source-and-drain diffusion for the *n*-channel transistors; (f) after growth of the gate oxide; (g) opening of source-and-drain contacts; (h) completed device.

FIGURE 41. METAL GATE CMOS PROCESSING SEQUENCE

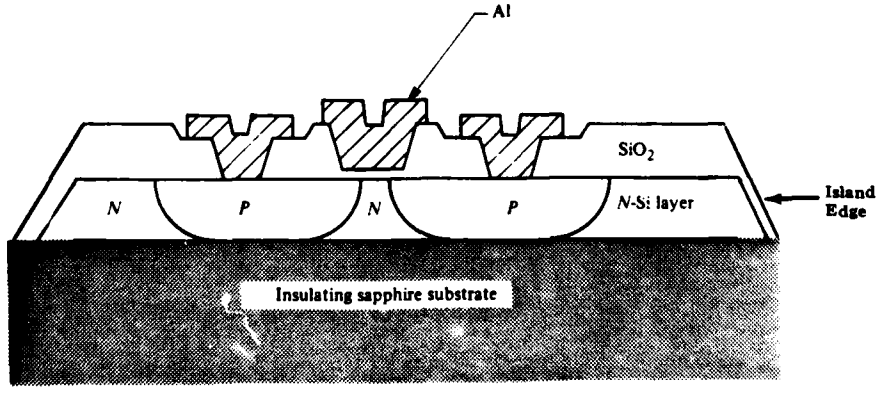
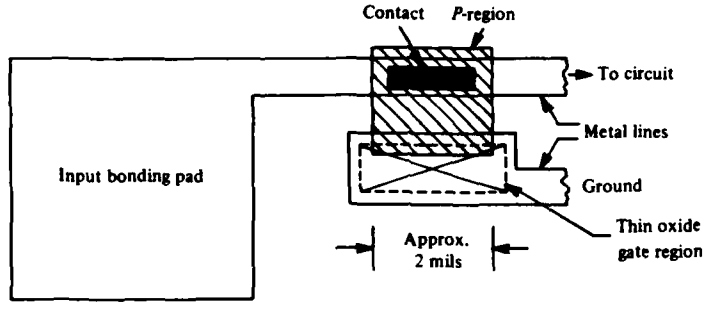
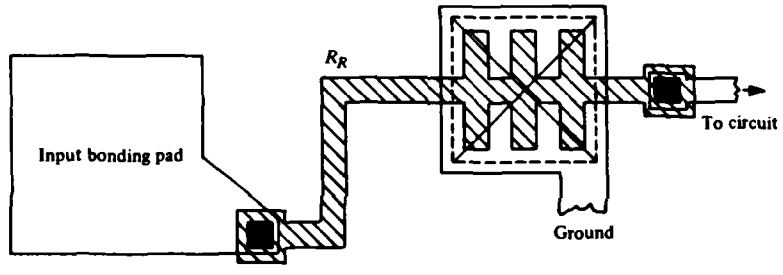


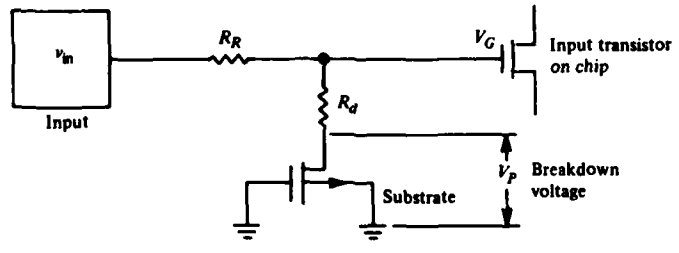
FIGURE 42. SILICON-ON-SAPPHIRE (SOS) MOS STRUCTURE



(a) Early version



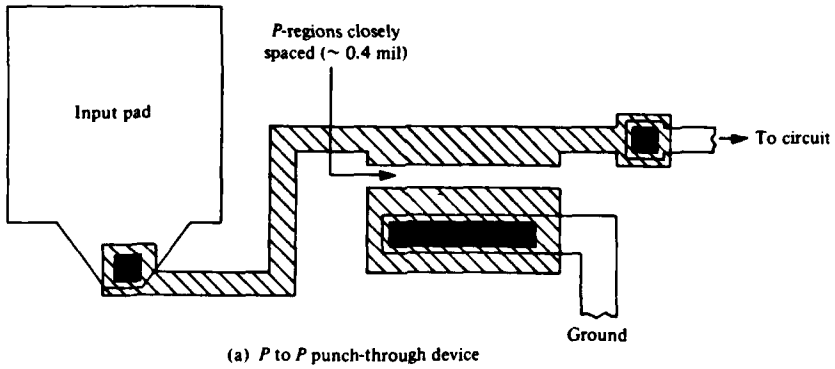
(b) Improved version



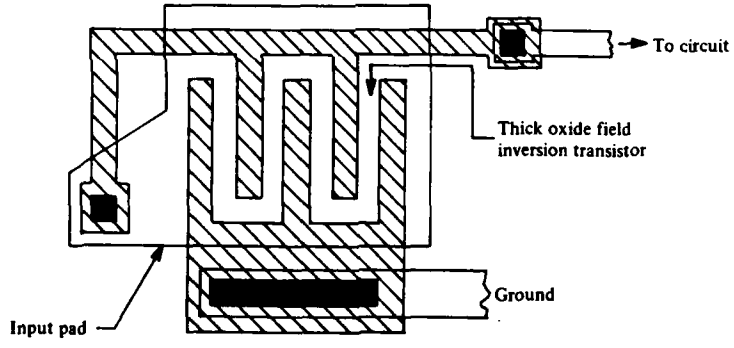
(c) Equivalent circuit

FIGURE 43. MOS PROTECTIVE DEVICES BASED ON GATE MODULATED JUNCTION BREAKDOWN

utilize a gate modulated junction breakdown mechanism. Other types of gate protective devices which the analyst may encounter are shown in Figure 44.



(a) *P* to *P* punch-through device



(b) Field inversion device

FIGURE 44. OTHER TYPES OF GATE PROTECTIVE DEVICES

g) Other Practical/Useful Integrated Devices. In addition to the bipolar and field-effect transistors, several other active device structures can be fabricated using the monolithic integrated circuit processes. The most significant among these are the unijunction transistor, the four-layer diode, the thyristor or the controlled rectifier structures, and the triac. A brief review of each of these structures will be given in this section.

The unijunction transistor or the UJT is a single junction device with two ohmic base contacts. Figure 45 shows a simplified diagram of a UJT, along with its integrated realization. The device exhibits a voltage-controlled negative resistance characteristic as a result of the conductivity modulation within the high resistivity base region. For a given base bias V_B, negligible anode current I_j flows until the anode terminal is raised to a sufficiently positive voltage level V_q to cause the junction to be forward-biased. The minority carriers injected into the base region cause the effective value of R_A to decrease, due to conductivity modulation, thus forward biasing the junction. This results in a negative resistance characteristic where I_j increases rapidly, without requiring V_j to raise, and the device switches to its "ON" state. Similarly, it can be returned to its stable "OFF" state by reducing the anode voltage to below V_q. The voltage-controlled negative resistance characteristics of the UJT make it useful for relaxation oscillator applications. It should be noted that in a conventional junction isolated structure, if one uses the n-type epitaxial layer as the base region of the UJT in Figure 45(b), this may lead to a parasitic pnp action between the p-type substrate and the UJT anode. This can be eliminated by using dielectric isolation techniques.

The four-layered (pnpn) diode and its three-terminal version, the thyristor, each contain four semiconductor regions. As shown in Figure 46(a), for analysis purposes a pnpn diode can be decomposed into a set of cross-coupled pnp and npn transistors. It can be shown that if one gradually raises the anode voltage, the device initially remains in a nonconductive state, until a turn-on voltage, V_{BO}, is reached. Then, the device suddenly switches to its "ON" state where it can carry a large amount of current with a very little voltage drop across it. The device can be turned off by reducing the current

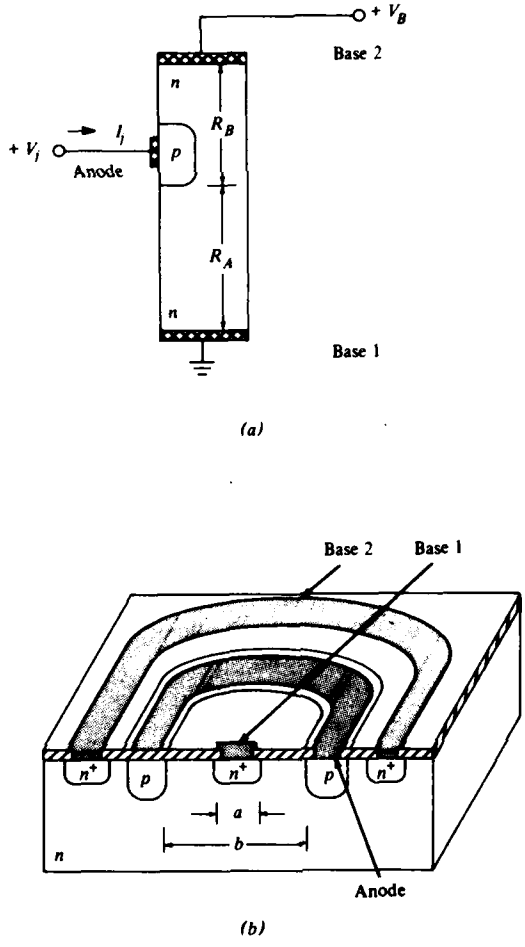


FIGURE 45. THE UNIJUNCTION TRANSISTOR:
(a) ITS SCHEMATIC REPRESENTATION
(b) A PRACTICAL INTEGRATED UJT STRUCTURE

to a level below the critical current level, known as the "holding current." This is shown as current level I_H in Figure 46(b). By examining the two-transistor equivalent circuit of a four-layer diode, one can show that the device switches from its nonconductive to conductive state at a point where the product of the current gains ($\beta_1\beta_2$) reaches unity. The four-layer diode is readily available in a junction isolated integrated circuit structure, using the p-substrate, n-epitaxial layer, p-base and the n-type emitter regions of a conventional npn transistor. However, such a structure is not directly useful, since its anode is formed by the substrate, which is also

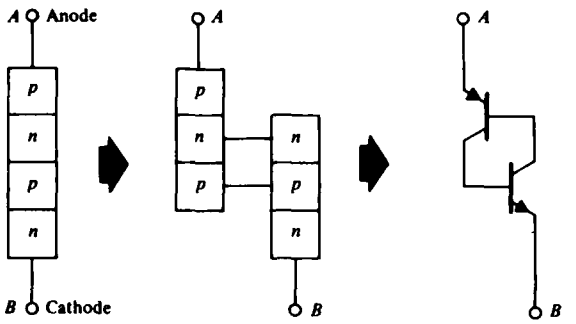


FIGURE 46. THE FOUR-LAYER DIODE: (a) TRANSISTOR EQUIVALENT CIRCUIT
(b) I-V CHARACTERISTICS

constrained to be at the most negative potential in the circuit to ensure that the isolation junctions are reverse-biased. Figure 47 shows an alternate four-layer diode structure which overcomes this difficulty, using dielectric isolation.

An additional control of the turn-on characteristics can be obtained by connecting a "gate" electrode to either of the two center regions. By injecting a small amount of current into this gate, the turn-on voltage can be kept at a value below V_{BO}, giving the device an additional degree of control. Such a three-terminal pnpn device is known as a thyristor or silicon controlled rectifier (SCR). A typical commercial alloy-diffused pellet formation for a high power SCR is shown in Figure 48. An example of a planar pnp pellet fabrication is

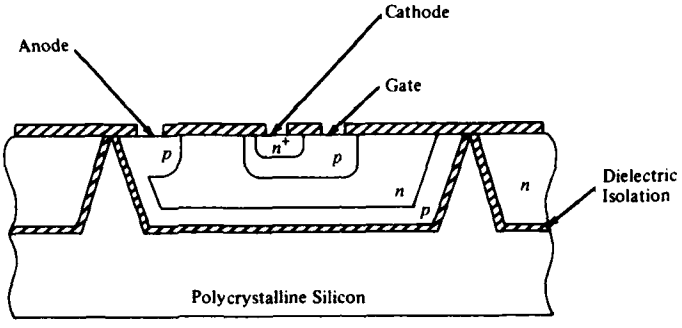
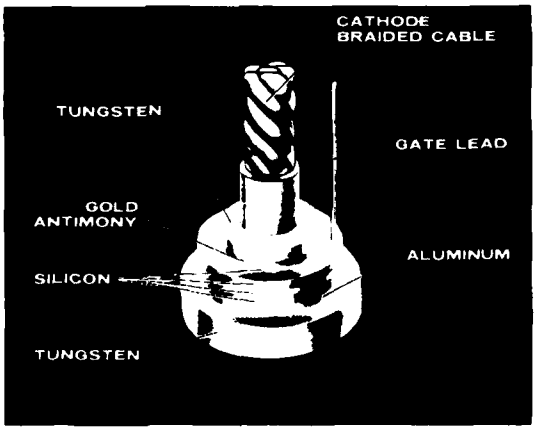


FIGURE 47. A FOUR-LAYER DIODE STRUCTURE USING DIELECTRIC ISOLATION



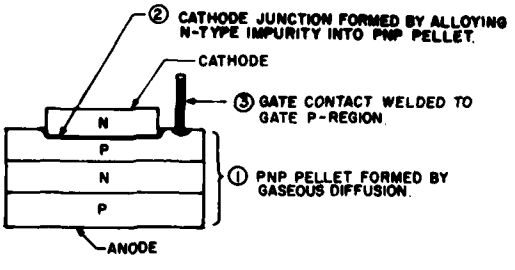


FIGURE 48. ALLOY-DIFFUSED PELLET FOR SCR

illustrated in Figure 49. The principal advantage of planar construction is that junction formation always takes place (reference Figure 49) underneath a thin layer of silicon dioxide grown over the silicon wafer before diffusion commences which prevents contamination of the silicon surfaces.

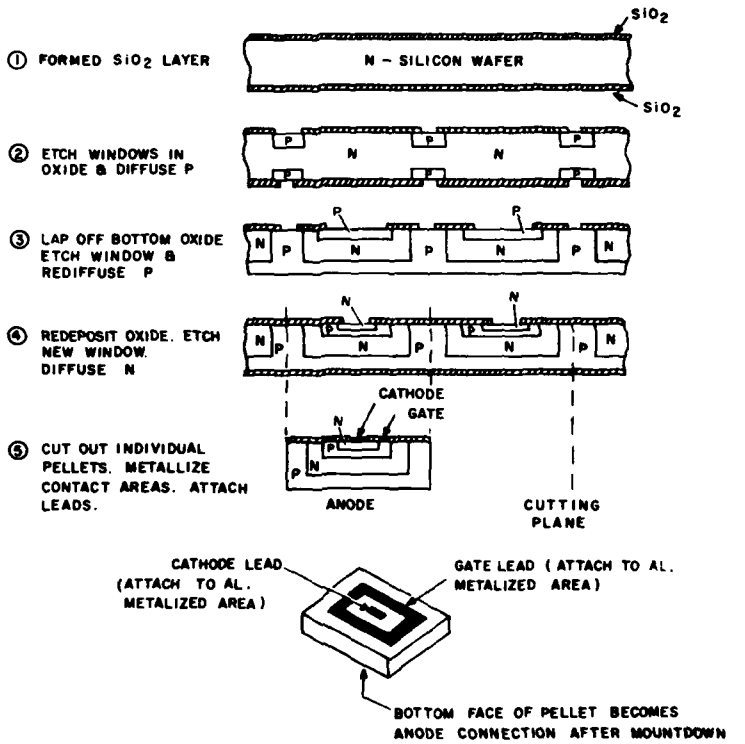


FIGURE 49. TYPICAL PLANAR PNPN PELLET FABRICATION (GEOMETRY EXAGGERATED FOR CLARITY)

The "TRIAC" is an acronym that has been coined to identify the triode (three-electrode) AC semiconductor switch which is triggered into conduction by a gate signal in a manner similar to the action of an SCR. The triac, generically called a Bidirectional Triode Thyristor, differs from the SCR in that it can conduct in both directions of current flow in response to a positive or negative gate signal. The basic triac structure is shown in Figure 50. The region directly between terminal MT_1 and terminal MT_2 is a p-n-p-n switch in parallel with an n-p-n-p switch. The gate region is a more complex

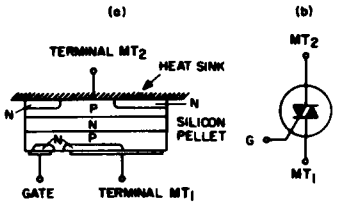


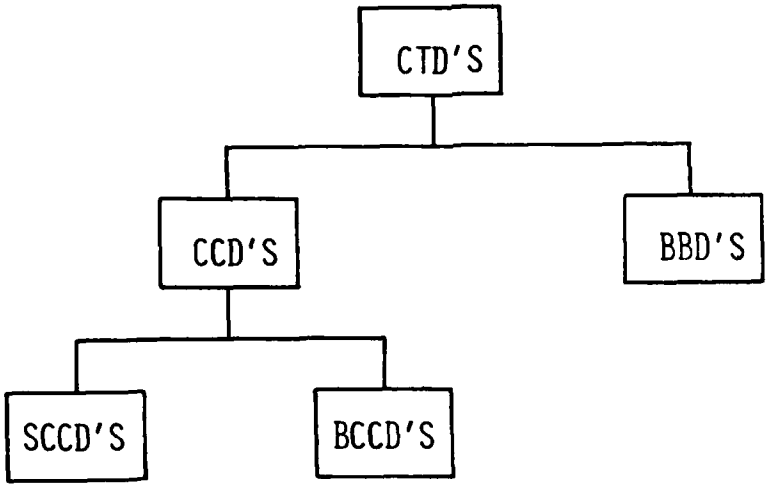
FIGURE 50. THE TRIAC; (a) SIMPLIFIED PELLET STRUCTURE
(b) CIRCUIT SYMBOL

arrangement which may be considered to operate in any one of four modes: direct gate of normal SCR; junction gate of normal SCR; remote gate of complementary SCR with positive gate drive; and remote gate of complementary SCR with negative gate drive. Terminal MT_1 is the reference point for measurement of voltages and currents at the gate terminal and at terminal MT_2.

Additional details on all semiconductor devices can be found in the bibliography at the end of this section.

5. Charge-Coupled Devices (CCD). Charge-coupled devices (CCD's) and bucket-brigade devices (BBD's) are subsets of a class commonly known as charge transfer devices (CTD's). The basic principle of charge transfer devices involves the movement of charge from one physical location of a semiconductor substrate to another in a controlled manner with the use of properly sequenced clock pulses. With properly designed charge injection and detection, CTD's are capable of performing numerous electronic functions such as image sensing, data storage, signal processing, and logic operations, since the CTD is an analog shift register in its basic form.

Charge-coupled devices can be classified (see Figure 51) as surface charge-coupled devices (SCCD's) in which the signal charge is transferred along the Si surface (or more accurately, the Si/SiO_2 interface), or bulk charge-coupled devices (BCCD's) in which the signal charge is transported within tne Si.



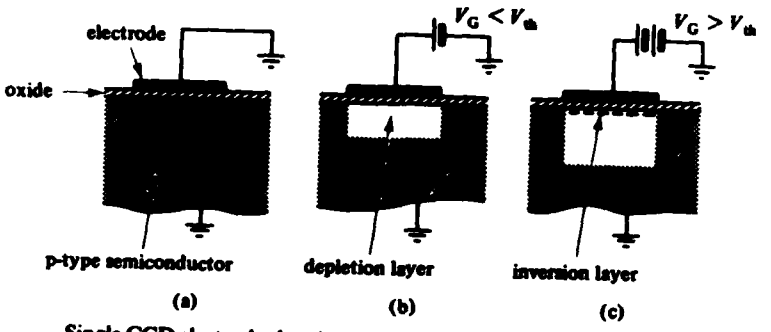
CTD'S - Charge Transfer Devices
BBD'S - Bucket Brigade Devices
CCD'S - Charge-Coupled Devices
SCCD'S - Surface Charge-Coupled Devices
BCCD'S - Bulk Charge Coupled Devices

FIGURE 51. FAMILY OF CHARGE TRANSFER DEVICES

The concept of storing information via charge in a capacitor is not new. The concept of connecting a series of storage capacitors with perfect switches was adapted to provide a variable analog delay line. However, the charge transfer concept lacked an effective vehicle to develop and utilize these ideas. With the recent significant process and material improvements associated with MOS technology, and control of Si/SiO_2 interface properties, it became possible to translate these ideas into physically realizable devices. The evolution of the charge transfer concept started with bipolar transistors as switches. The bipolar transistors were later replaced by MOS transistors and the form now known as bucket-brigade devices was developed.[11]

A basic understanding of charge storage can be obtained by examining what happens if an increasingly positive voltage is applied to the gate of the metal-oxide-semiconductor (MOS) structure shown in Figure 52. Prior to the application of a bias, there will be a

uniform distribution of holes (majority carriers) in the p-type semiconductor; as the gate electrode is made positive, however, the holes are repelled from the semiconductor immediately beneath the gate, thereby creating a depletion layer (see Figure 52b). As the gate bias is increased, the depletion region extends further into the bulk semiconductor and, as one would expect, the potential at the semiconductor/insulator interface (generally called the "surface potential" and designated by ϕ_s) becomes increasingly positive. Eventually a gate bias is reached at which the surface potential becomes so positive that electrons (i.e., minority carriers) are attracted to the surface where they form an extremely thin ($10^{-2}\,\mu$m) but very dense (i.e., in terms of charge per unit volume) "inversion layer" (see Figure 52c). The creation of the inversion layer corresponds to the establishing of a conducting channel in an MOS transistor and the CCD gate potential corresponding to the onset of inversion is called, as in the case of an MOS transistor, the threshold voltage, V_{th}. By analog with an MOS transistor, a CCD in which the inversion charge is negative is often called an n-channel CCD; likewise, a device in which the inversion charge comprises holes is called a p-channel CCD. There is one important difference, however, between the MOS capacitor structure of Figure 52 and an MOS transistor. In an MOS transistor, the application of a gate bias in excess of the threshold voltage results in the immediate formation of a channel because a copious supply of minority carriers is available from the transistor's source and also, perhaps, its . But in the structure of Figure 52 no ready supply of minority carrier exists and so, even if the gate voltage is suddenly pulsed well beyond the threshold voltage, an inversion layer cannot form immediately. In the absence of an inversion layer, the depletion region extends much further into the bulk semiconductor and most of the potential difference between the gate and the substrate is dropped across this depletion layer.



Single CCD electrode showing the creation of depletion and inversion layers under the influence of an increasingly positive electrode voltage.

FIGURE 52. CHARGE STORAGE

An almost linear relationship exists between the charge density in the inversion layer versus the surface potential. A family of curves can be plotted for different gate voltage levels. This almost linear nature of the relationship suggests a simple hydraulic model for the charge storage mechanism which is extremely useful in picturing the operation of all CCD structures. The application of a gate voltage in excess of V_{th} creates a "potential well," the depth of which is related, for a particular structure, to the magnitude of the gate voltage. Figure 54a, for example, depicts the empty well concept when various gate biases are applied to the 0.1 μm thick oxide structure of Figure 53. The introduction into the structure of an inversion layer brings about an almost linear reduction in the surface potential and is analogous to pouring liquid into the well, the depth of which (measured from the top of the well to the surface of the liquid) also decreases linearly with the amount of liquid introduced (See figure 54a and 54c). The well clearly has a maximum capacity governed by the "gate voltage" and the "oxide thickness," which determine the depth of the well (and hence the maximum depth of liquid, representing the charge per unit area, which can be introduced), and the "area of the electrode," which determines the area of the well's cross section.

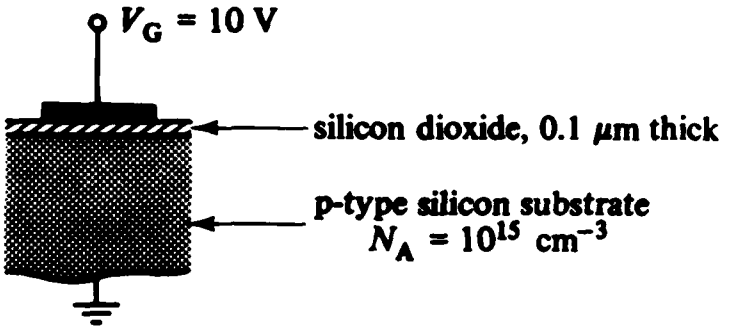
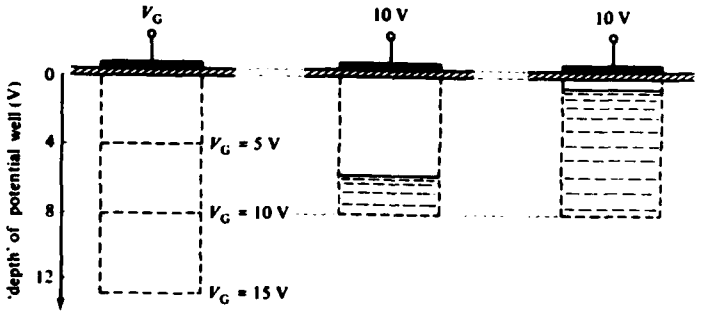


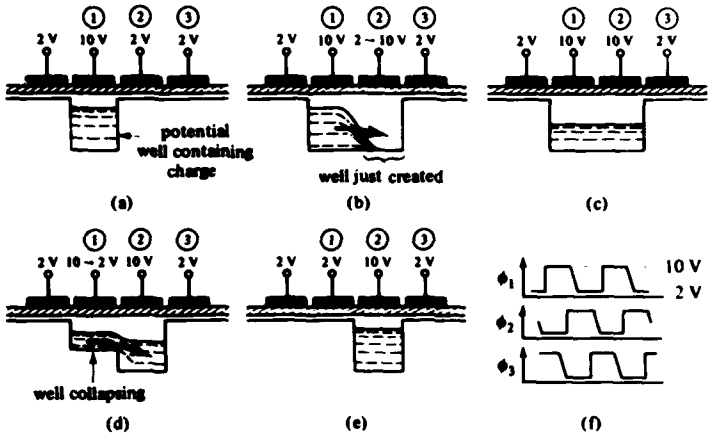
FIGURE 53. TYPICAL MOS STRUCTURE USED IN CCD'S



The potential well concept. (a) The depth of an empty well is approximately proportional to the gate voltage. (b) and (c) For a given gate voltage, the depth of the well (measured to the surface of the liquid) decreases linearly with increasing charge. Note that when V_G = 10, (a), (b) and (c) correspond to the structure and the situations depicted in Fig. 1.2.

FIGURE 54. POTENTIAL WELL CONCEPT

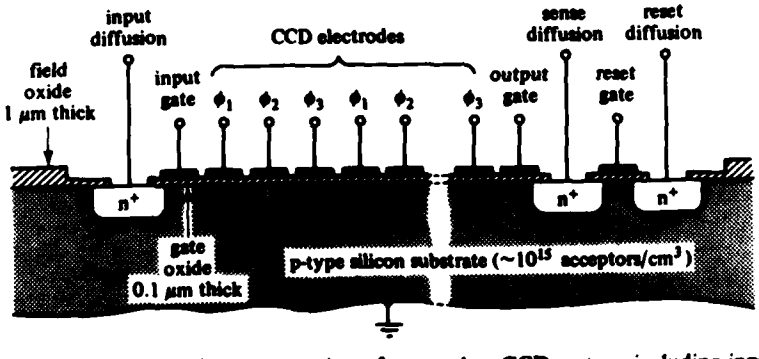
To understand how a potential well can be moved from one location to another in a CCD structure, consider the arrangement of four closely spaced electrodes shown in Figure 55a. We assume that some charge is stored initially in the potential well under the second electrode (from the left) which is biased to 10V. In Figure 55a, we have assumed V_{th} to be less than 2V, and so potential wells will be created beneath all the electrodes. The potential well under the 10V electrode will, of course, be much deeper than those under the 2V electrodes and so, providing that it is not "over-filled," it is only in this way that charge will be stored. Now suppose that the bias on the third electrode is increased to 10V. If the two 10V electrodes are very close together their respective potential wells will merge and so the charge packet originally under the second electrode becomes shared between the wells under the second and third electrodes (See Figure 55b and 55c). If now the potential on the second electrode is reduced to 2V, the remaining contents of its potential well will be shifted into the third well (see Figure 55d). We therefore end up with a situation (see Figure 55e) similar to that in Figure 55a but with the deep potential well and its associated charge packet moved one place to the right. By applying a succession of varying voltages to the CCD electrodes a charge packet can be propagated in a controlled manner just beneath the surface of the semiconductor. For a CCD structure consisting of more than a few electrodes, it would be quite impractical to have external access to each individual electrode. Fortunately this is not necessary: the electrodes can be grouped together and each group or phase connected to a different driving clock. A three-phase clocking system, such as that depicted in Figure 55f is required for a CCD structure of the type shown in Figure 55a-e. It is the CCD's ability to store and move around a variable amount of charge that gives the device its analogue and digital processing capabilities.



(a)–(e) Movement of potential well and associated charge packet by clocking of electrode voltages; (f) clocking waveforms for a three-phase CCD.

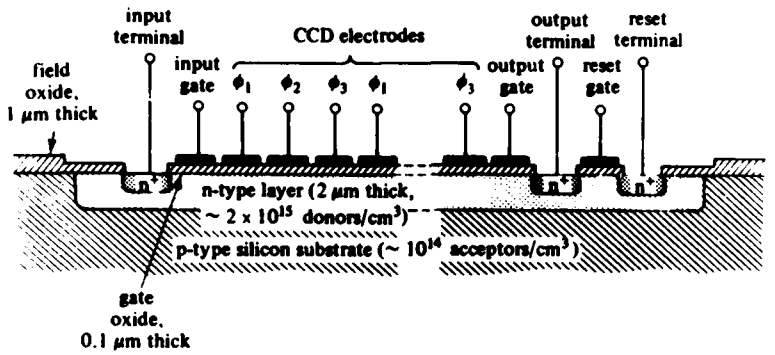
FIGURE 55. CHARGE MOVEMENT

Figure 56 shows a diagrammatic representation of a complete CCD system including input and output circuitry. Figure 57 shows a diagrammatic representation of a typical bulk-channel CCD fabricated in silicon.



Diagrammatic representation of a complete CCD system, including input and output circuitry (n^+ denotes heavily doped n-region).

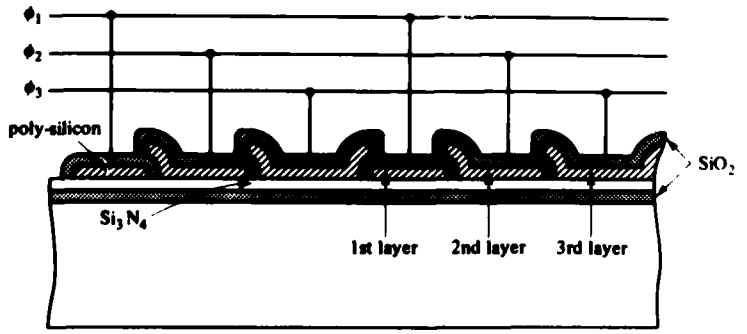
FIGURE 56. A COMPLETE CCD SYSTEM



Diagrammatic representation of a typical bulk-channel CCD fabricated in silicon (n^+ denotes heavily doped n-type regions).

FIGURE 57. A BBCD SYSTEM

One of the more complex approaches used to produce both narrow inter-electrode gaps and a completely enclosed surface is to use three separate metal layers to form the three sets of electrodes. The basic structure of the polycrystalline silicon version, which is now the most widely used three-phase technology, is shown in Figure 58. The silicon nitride layer shown in this diagram is used to protect the underlying oxide layer during etching of the polycrystalline silicon electrode pattern.

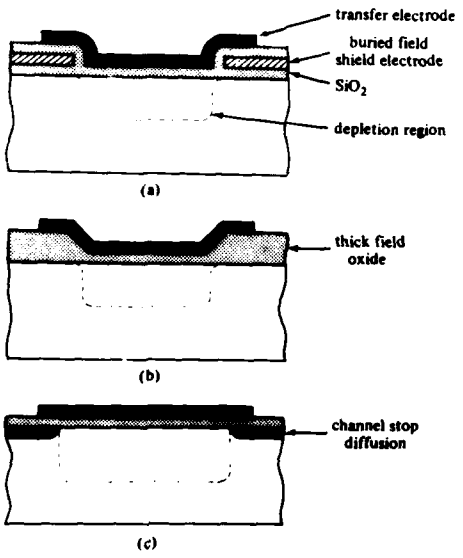


Three-phase structure employing three overlapping levels of oxidized polycrystalline silicon.

FIGURE 58. A THREE PHASE CCD STRUCTURE

There are three standard MOS techniques that can be used to confine the charge packet in a direction perpendicular to that of charge transfer. These three standard MOS techniques, at least in principle, limit the width of the channel. These techniques are illustrated in Figure 59 and are:

- o Field shield electrode
- o Oxide step
- o Channel-stop diffusion[12]



Techniques of lateral confinement. (a) buried field shield electrode. (b) thick field oxide; and (c) channel stop diffusion.

FIGURE 59. LATERAL CONFINEMENT

6. Metal-Nitride-Oxide-Semiconductor (MNOS)- The MNOS device is another type of charge-storage programmable structure. The basic structure is shown in Figure 60. An MNOS device consists of layers of aluminum, silicon nitride, silicon dioxide, and silicon. The

device can be switched between two distinct, more or less permanent, threshold voltage states by applying a voltage pulse to the gate. The device is usually programmed by applying a positive gate voltage pulse above a critical polarization level. Typically, a pulse of 50 volts for a duration of 10 to 20 microseconds will result in an inversion layer. A pulse in the opposite direction will remove the inversion layer.

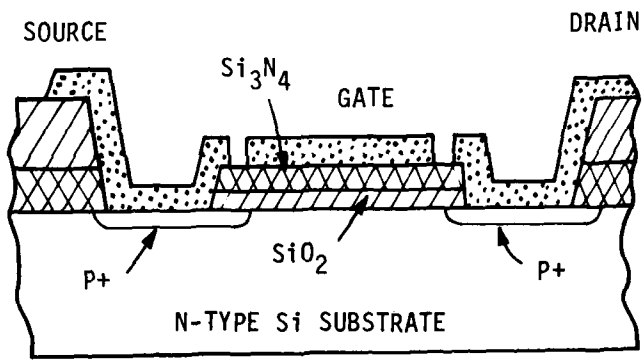


FIGURE 60. METAL-NITRIDE-OXIDE SEMICONDUCTOR

C. Failure Modes in Semiconductor Devices. The failure mode of a semiconductor device is defined as that characteristic of the device for which it has been classified a failure, i.e., deviation from specification or desired performance. A summary of the principal semiconductor failure modes are given in Table VI below:

TABLE VI

FAILURE MODE SUMMARY

FAILURE MODE	DEFINITION	EFFECT ON DEVICE OR IC
1. Internal Short	Short Circuit Between Metalized Leads or Across a Junction.	Short Circuit or Circuit Malfunction.
2. Internal Open	Open Circuit in the Metallization or Wire Bond.	Open Circuit
3. Parameteric Variation	Variation in Gain or Other Electrical Parameter.	Marginal Performance, Temp. Sensitivity, or No Effect.
4. Junction Leakage	Leakage Current Across P-N Junctions.	Effects Range from None to Malfunctions.
5. Threshold Shift	Shift in Turn-on Voltage.	Random Logic Malfunction
6. Seal Integrity	Ingress of Ambient Air, Moisture and/or Contaminants.	Effects Range from Degradation to Complete Malfunction.

D. Failure Mechanisms in Semiconductor Devices. A review of the principal failure mechanisms found in silicon semiconductor devices is presented over the next few pages. The presentation of failure mechanisms is that package defects are described first, then macro failures in the chips, chip attachment failure, bonding defects, metallization and conductor failures, failures in oxide or passivation layers, failures in interface between conductor and underlayer and at last design defects and faults in the bulk silicon.

1) Encapsulation Failures.

- o Degradation of solder glass causing insulation failures
- o Compatibility problems kovar-glass sealings
- o Humidity and impurity penetration
- o Imperfections in termination materials
- o Stress cracks in encapsulation or solder glass
- o Different thermal expansion coefficient of encapsulation, leads or chip

2) Macro Chip Failures.

- o Single cracks crossing larger part of chip
- o Small cracks at bondings
- o Cracks and imperfections because of poor scribing

3) Imperfect Chip Attachment to Substrate.

- o Incomplete thermal contact between chip and substrate because of solder leaching
- o Incomplete thermal contact between chip and substrate because of improper bond
- o Stress cracks in interface chip to substrate
- o Solder or epoxy material short circuit of chip edge

4) Wire Bonds.

- o Excessive bonding pressure
- o Misplaced bonds, crossed wires, excess tails, and over size bonds
- o Mechanical stress deformation of wire during bonding procedure
- o Microcracks at bonding heel. Heel breaking
- o Cracks in Si Alloyed Al wire (1% SiAl)
- o Silicon electromigration in aluminum wires
- o Gold-Aluminum intermetallic phases ("purple plagues")

5) Special Bonding Methods.

- o Failures in beam-lead bondings

6) Aluminum Conductors.

- o Cracks in the aluminum conductors due to stress-relief
- o Faults in metallization at contact windows
- o Puddling at contacts
- o Adhesion failures
- o Electromigration
- o Corrosion
- o Failure depending on grain size
- o Metal migration under passivation layers
- o Failures because of instability of metallization system
- o Hillock formation and cracks in connection with temperature cycling
- o Surface reconstruction of aluminum metallization
- o Failures in connection with underetching
- o Geometrical failures in connection with misalignment
- o Leaching of metallization by soldering
- o Flash-across short of "electrodes"

7) Gold Conductors.

- o Electromigration.
- o Gold metallization degradation at high temperatures
- o Whisker formation in two-layer gold metallization

8) Thermal Oxide or Passivation Layers.

- o Ionic impurities in the oxide
- o The fixed charge Q_{ss}
- o Ions at the oxide surface
- o Oxide step contour failures in multi-layer circuitry
- o Pinholes from etching processes
- o Geometrical failures in connection with misalignment or photoresisting and etching failures
- o Cracks or scratches in oxide surface
- o Electrical breakdown of oxide
- o Foreign substances attached (liquid, metallic particles, etc.)

9) Aluminum Conductor to Underlayer Interface.

- o Thermal interface reactions with Si
- o Porous Al layers in contact windows

10) Design Defects and Faults in Bulk Silicon.

- o Improper design
- o Defects in bulk material
- o Resistivity striations
- o Recombination-generation centers at the silicon-silicon dioxide interface of planar devices and trapped carriers in the silicon dioxide ("walk-out")
- o Diffusion faults

E. Product Evaluation. A number of techniques have been introduced over the last ten years for assessing a microelectronic device. Those techniques which the failure analyst may be required to perform from time to time are:

a) Scanning Electron Microscope (SEM) Wafer Analysis
b) Destructive Physical Analysis (DPA)
c) Constructional Analysis (CA)

All of these techniques rely on judging the population quality based on a small sample.

The utilization of the SEM to evaluate metallization step coverage was pioneered by NASA - Goddard personnel during the manned missile development period. This work led to the introduction of a test method 2018 which was added to MIL-STD-883B specifying the procedure for SEM wafer inspection. The requirement covers a procedure for judging the quality and acceptability of metallization on semiconductor die. This procedure examines the specific metallization defects that are batch process oriented.

Destructive Physical Analysis is a series of steps used on a small sample to judge the quality, workmanship, and general acceptability of a manufacturer's process for a production lot of devices. It is usually performed by lower skill personnel than normally used for in-depth failure analysis. The steps are established by a data sheet or procedure and limited latitude is allowed to the performing analyst in changing the steps.

On the other hand, Constructional Analysis is usually performed on a small sample to compare vendors' quality, workmanship, design approaches, thermal matching, and other design related aspects of the device. It is usually performed by a higher skill level analyst with considerable latitude in what is looked at and in what depth. Constructional Analysis is usually a one-time for a given device and vendor whereas Destructive Physical Analysis can and should be performed on each production lot and be made part of the lot acceptance criteria.

F. Failure Analysis Flow Sequence. The actual failure analysis flow sequence will be largely dependent on the type of device, expected failure mechanisms, observed failure modes, package construction, and technology utilized. Figure 61 illustrates the mental as well as general steps that a failure analysis progresses through in an orderly failure analysis. This simplified flow diagram is utilized to stress the importance of establishing the potential failure mechanisms, based on all data available, prior to any actual analytical steps or other destructive or non-destructive tests.

A more detailed generalized failure analysis flow diagram is illustrated in Figure 62. An attempt is made here to illustrate what is the usual location of each of the specialized failure analysis techniques in this procedural guide. This, in no way, precludes the use of some specialized technique in a different place in the analysis based on unique circumstances for that particular failure mechanism(s).

G. Failure Analysis Laboratory Requirements. The possible equipment available to the failure analyst is unlimited on the present market; however, most analysts have to start out with only a modest equipment budget and build up a capability over a number of years. Our approach in this guide will be to outline three levels of Failure Analysis Laboratories as a way of sizing up your present and future equipment needs for realizing your laboratory goals.

1. BEGINNING FAILURE ANALYSIS LABORATORY.

Item	Approx. Cost
1. Curve Tracer	$ 5 - 10K
2. Digital V-O-M	$750 - 1.5K
3. Stereo Binocular Microscope (10X-100X)	$750 - 1K
4. Package Opening Tools	$200
5. Miscellaneous Hand Tools	$500
6. Set of DUMAS Type Microprobes (Min. of three)	$200 - 500
TOTAL	$7.4 - $13.7K

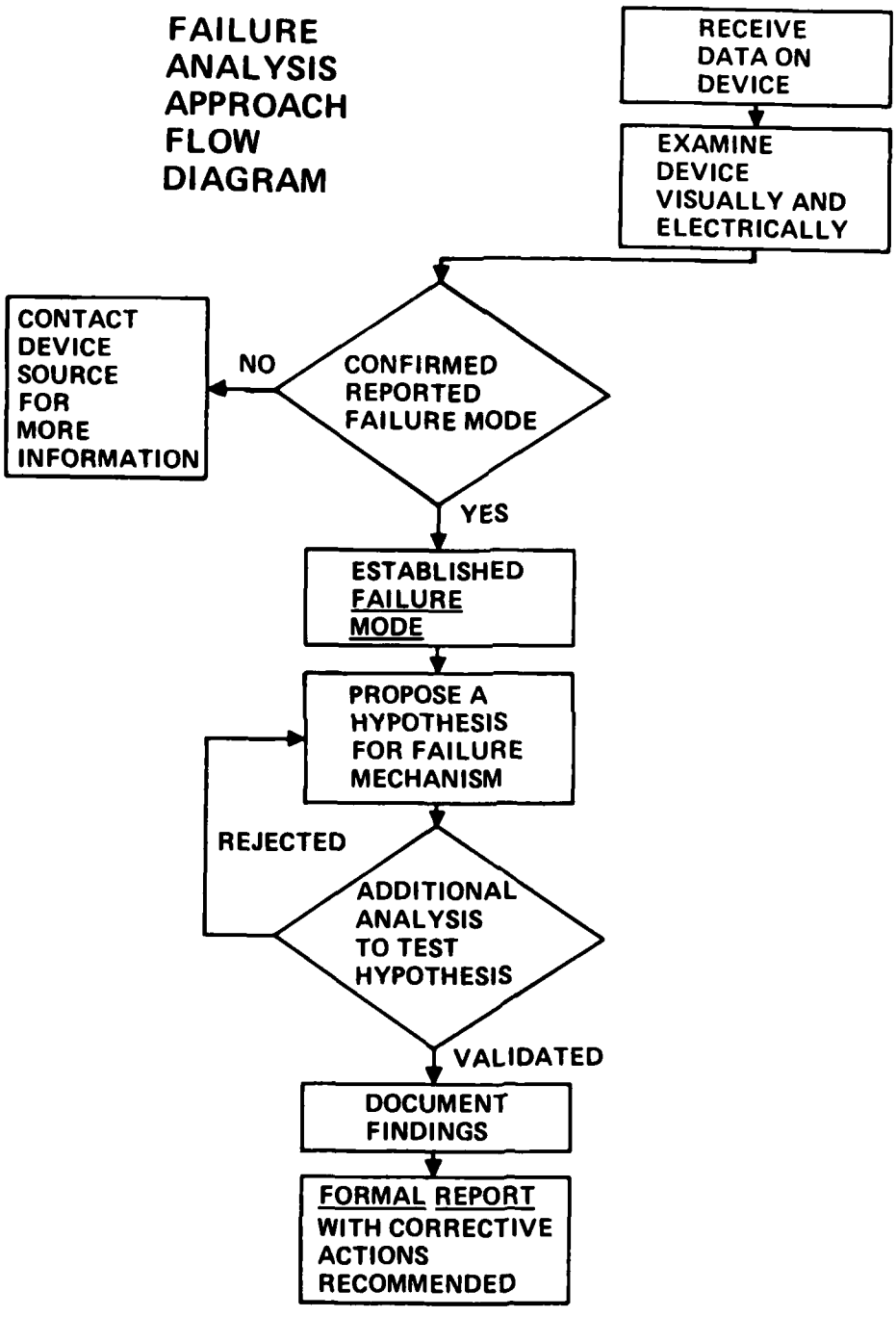


FIGURE 61. FAILURE ANALYSIS APPROACH FLOW DIAGRAM

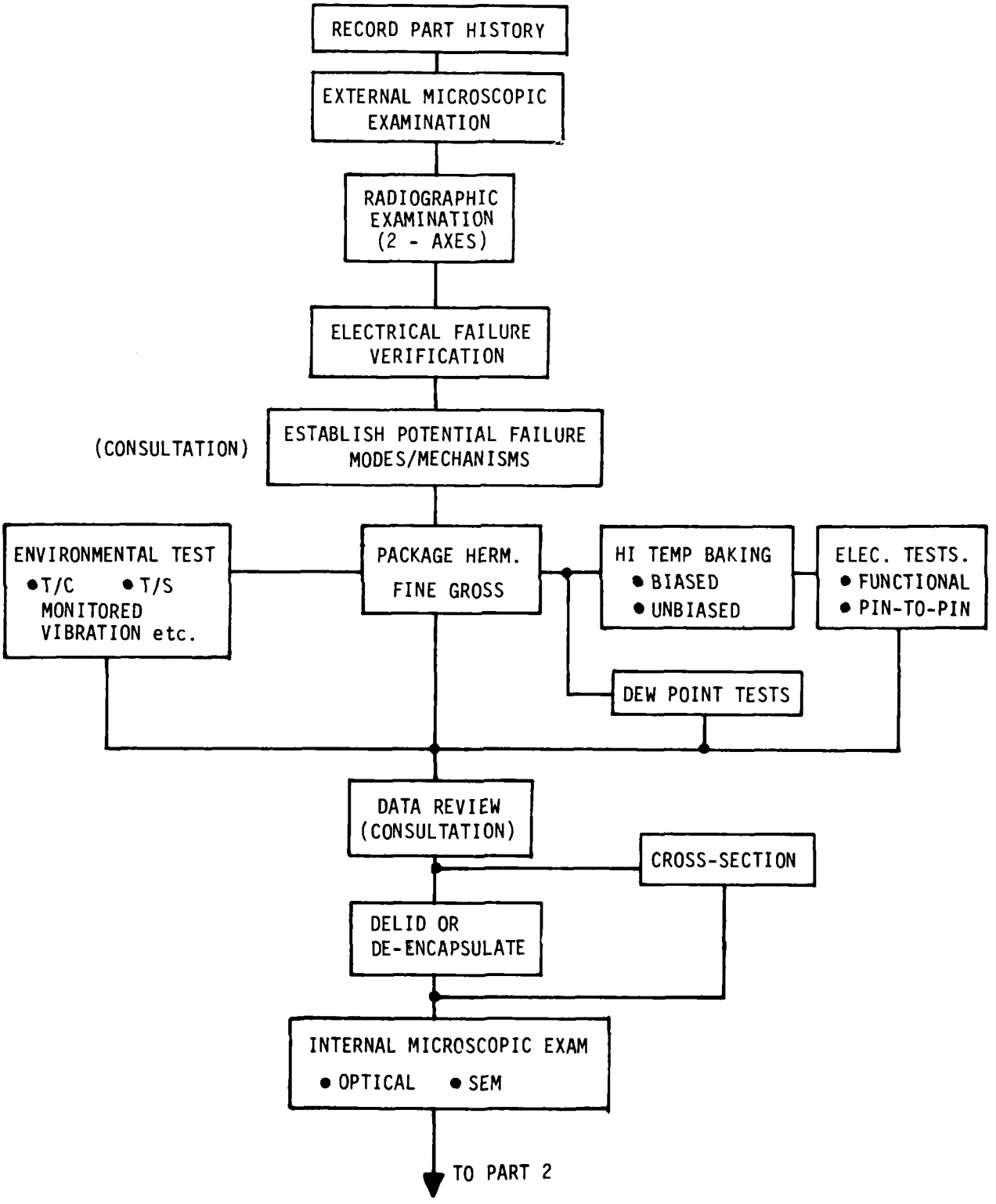


FIGURE 62. GENERALIZED FAILURE ANALYSIS FLOW DIAGRAM

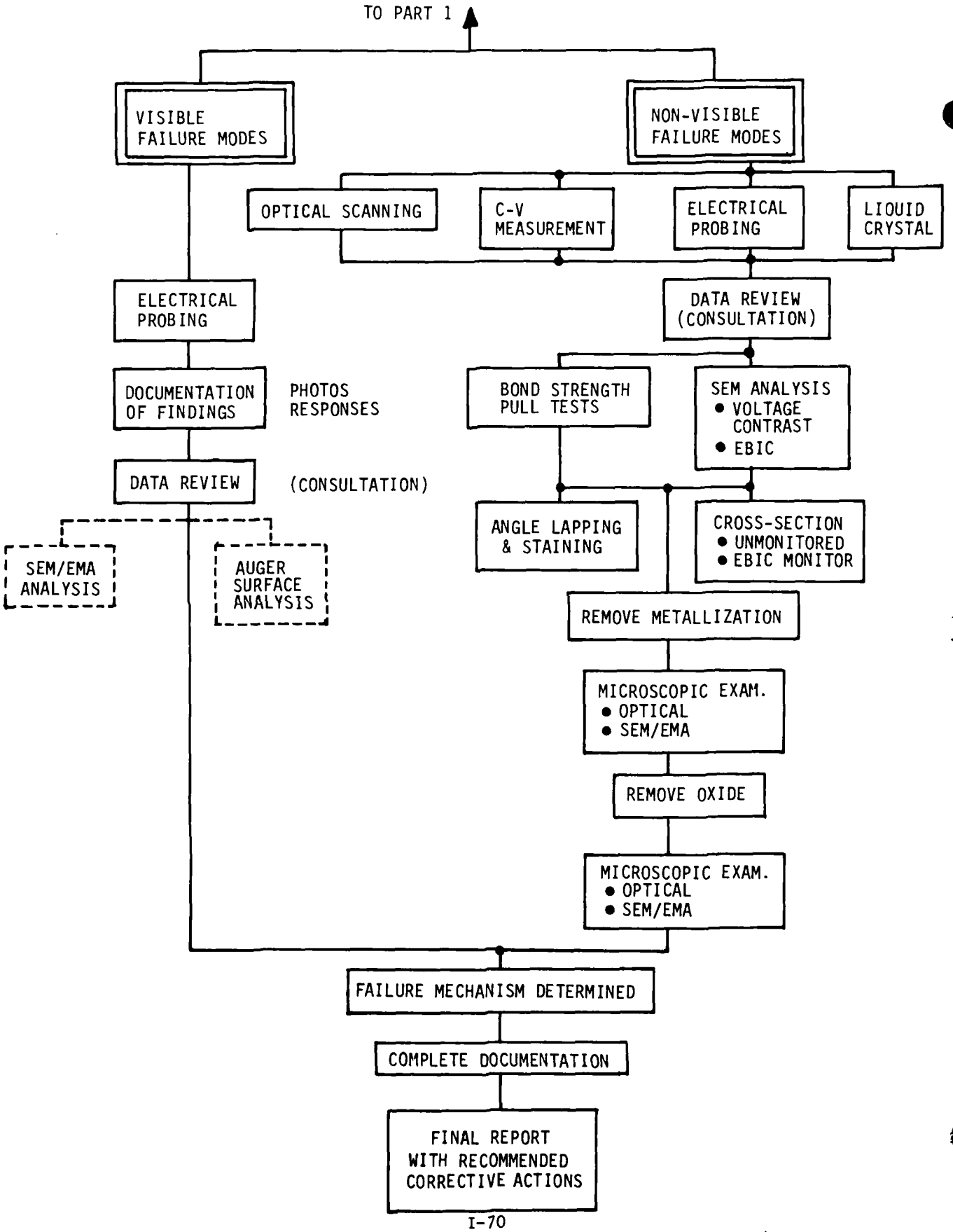


FIGURE 62. GENERALIZED FAILURE ANALYSIS FLOW DIAGRAM (cont'd)

2. GOOD FAILURE ANALYSIS LABORATORY.

	Item	Approx. Cost
1.	Curve Tracer(s)	$ 5 - 10K
2.	Manual Integrated Circuit Tester ° Linear ° Digital	$ 5 - 25K
3.	C-V Measurement/Recording Equipment	$ 5 - 10K
4.	Electrical Probe Station	$10K
5.	Environmental Test Chamber	$ 5K
6.	Stereo Binocular Microscope(s) (10X-100X) (Zoom)	$750 - 1K
7.	Metallurgical Microscope, Stereo Zoom (100X-800X) Bright field, dark field, phase contrast.	$ 3 - 5K
8.	Small Machine Shop (drill, grinders, lathe, etc.)	$ 5 - 10K
9.	Wet Chemistry Hood & Chemical Storage	$ 3 - 5K
10.	Oscilloscope, Power Supplies, etc.	$ 10 - 20K
11.	Scanning Electron Microscope (EDX capability)	$ 55 - 200K
12.	Cross-sectioning/Polishing Equipment	$ 15 - 25K
	TOTAL	$122 - 326K

3. ADVANCED FAILURE ANALYSIS LABORATORY

	Item	Approx. Cost
1.	Curve Tracer(s)	$ 5 - 10K
2.	Manual Integrated Circuit Tester	$ 5 - 25K
	° Linear	
	° Digital	
3.	Automatic Integrated Circuit Tester	$100 - 400K
	° Memory	
	° μP's	
4.	C-V Measurement/Recording Equipment	$ 5 - 10K
5.	Optical Scanning Equipment	$ 10 - 20K
6.	Metallurgical Microscope(s), Stereo Zoom Bright field, dark field, phase contrast. (100X-800X)	$ 3 - 5 K
7.	Machine Shop (drill press, grinders, lathe, etc.)	$ 10 - 15K
8.	Wet Chemistry Hood(s), Chemicals, Storage	$ 5 - 10K
9.	Oscilloscope(s), Power Supplies(s), Pulse Generators, etc.	$ 20 - 50K
10.	Scanning Electron Microscope(s)	$150 - 300K
	° Energy Dispersive X-Ray	
	° Wavelength Dispersive X-Ray	
	° Backscatter Detector	
	° Cathodoluminescence	
	° Specimen Current Amplifier	
	° Higher Beam Voltages (>30KV)	
11.	Auger Spectrometer	$ 50 - 75K
	° Ion Beam Etching	
12.	Mass Spectrometer	$150 - 200K
13.	Cross-sectioning/Polishing Equipment	$ 50 - 100K
14.	Infrared Radiometer (Scanning)	$ 35 - 50K
		$508 - 1,270K

H. Failure Analysis Documentation. Failure analysis documentation provides the technical basis for the decisions on the failure mode, failure mechanism(s), and possible corrective actions. The first form encountered by the failure analyst is the form requesting a failure analysis on a particular semiconductor device. A typical failure analysis request form is shown on pages I-73; and I-80/81; also note that this form has space for a short form report on the bottom half. There are a number of specialized data formats used by Failure Analysis Laboratories throughout the industry. Some of the special data formats used are:

a) DESTRUCTIVE PHYSICAL ANALYSIS DATA
b) HERMETICITY DATA
c) BOND STRENGTH PULL DATA
d) FAILURE ANALYSIS DATA

Examples of these data sheets are shown on pages I-74 to I-81.

Each failure analyst will develop his own methods and procedures for data collecting but there are a few general considerations that should be stressed. The principal points are listed below:

a) Record all initial electrical/physical characteristics prior to any tests or procedures being tried on the suspect device.

b) Always try out any potentially destructive electrical, chemical, mechanical procedures on a good reference unit first to determine the usefulness prior to committing the suspect device.

c) It is rare that an analyst will over-document, so beware of inadequate data on intermediate steps which greatly affect the final failure mechanism conclusion.

d) Although it seems obvious, it is vitally important to document the actual order of analysis procedures that the device has seen prior to any particular data observation.

SPERRY
FLIGHT SYSTEMS

FAILURE ANALYSIS LABORATORY
SHORT FORM

				JOB NO.
PROJECT NAME	AO OR PN	REQUESTED BY	DEPT	DATE RECEIVED
				DATE COMPLETED
DEVICE, P/N	MANUFACTURER	DATE CODE	QTY	MAN-HOURS:

BACKGROUND:

TESTS:

RESULTS:

PERFORMED BY _____

5232-015 (REV 11-77)

Copy 4 – Requester

TYPICAL FAILURE ANALYSIS REQUEST FORM

DESTRUCTIVE PHYSICAL ANALYSIS REPORT

DATE: INITIATED _____ COMPLETED _____ DPA REPORT NO. _____

PART TYPE _____ S/N: _____ P/N: _____

SUPPLIER: _____ P.O. NO. _____ DN NO. _____

LOT/DATE CODE: _____ QTY. PROCURED: _____ SAMPLE SIZE _____ PIA CHG. _____

DPA SPECIFICATION _____ REV _____

RESULTS OF ANALYSIS ANALYST: _____

DPA FINDINGS: _____

RECOMMENDATIONS: _____

CONTAINS DISCREPANT CONDITION: _____ YES/NO ____, RECOMMEND USE: _____ YES/NO _____

DISCREPANCIES (SPEC. PARA'S) _____

APPROVALS:

R&C COMPONENT PARTS ENG.	DATE	R&C PARTS ENGINEERING SUP.	DATE

PROJECT DISPOSITION: _____

SQA SIGNATURE	DATE	PROJ. REL. COORDINATOR	DATE

PROJECT LEADER	DATE

TYPICAL REPORT FORM

DPA CHECK SHEET

DPA NO._____

TRANSISTORS, SCR'S

SHEET NO._____

Part Type_____ Supplier_____ P/N_____

Date Started_____ Lot/Date Code_____

	Sample No.	1	2	3	4	5
	Serial No.					
CURVE TRACER EXAMINATION:						
Are junctions normal?						
DECAP UNITS & PHOTOGRAPH ONE DEVICE FOR RECORDS:						
Any evidence of intermetallics?						
Is lead dress normal?						
Is there any unattached foreign material?						
Does die meet the visual criteria?						
SEM INSPECTION, ONE SAMPLE, EXPANDED CONTACTS ONLY:						
Is step coverage adequate?						
WIRE BOND STRENGTH:						
Does wire pull meet criteria?						
DIE SHEAR:						
Is die attach adequate?						

COMMENTS OR ANOMALIES:_____

Analyst:_____ Date:_____

TYPICAL CHECK SHEET

GENERAL ELECTRIC

E-LAB
Technical Services

ADVANCED RELIABILITY REPORT

BLDG. 3 • ELECTRONICS PARK • SYRACUSE, NEW YORK 13221 • 315-456-2556

HERMETICITY SEAL MIL-STD-883B
METHOD 1014.2 TEST CONDITION _____
SUBJECT: FINE LEAK TEST
Feed-Through (Glass to Metal Seals)

Report Number AR-89-79

Date July 19, 1979

Requested by Fritz Viggiano Dept. HMED

Copy to: F. Viggiano
G. Trojanowski

Chg. No. 840632

Tests by J. Thrall

Signed J. Thrall Jr.

- Sensitivity Calibrator Type SC-4, For Helium Mass Spectrometer Leak Detector: Serial No. 13808, 4.3×10^{-8} STD. cc/sec.
- Calibrator Reading START/FINISH (units) 4.8×10^{-8} / 5.5×10^{-8}
- Helium Bomb Pressure/Time N/A PSIGA/ N/A HRS.
- Special Conditions: Seals were mounted over vacuum port and sprayed with helium externally.

Unit Serial No.	Reading in Units	Leak Rate atm/cc/sec.
E010	2.0 → 0.8	$>1 \times 10^{-8}$
E011	1.3 → 0.9	"
E012	2.0 → 0.6	"
E019	Background >0.08	$>1 \times 10^{-9}$
E039	0.7 → 0.15	"
E045	2.0 → 0.3	$>1 \times 10^{-8}$

/mvg

• RELIABILITY TESTS AND ANALYSES • SCANNING ELECTRON MICROSCOPE & MICROPROBE FACILITIES
• SEMICONDUCTOR FAILURE ANALYSIS • COMPONENT QUALIFICATION

Tensile Pull Test MIL-STD-883 Method 2011

Bond Wire Material:	Pkg. Pad Material:	Die Pad Material:
(X) Aluminum	( ) Aluminum	(X) Aluminum
( ) Gold	(X) Gold	( ) Gold
( ) _____	( ) _____	( ) _____

8 (Mils) Wire Dia. Part Type JANTXV2N4150

S/N 3595, 3619, 3628

PULL TEST DATA

Lead & I.D. No.	Wire Bond Type	Failure (grams)	Wire Break	Die Bond	Pkg. Bond	*	Remarks
S/N95							
Em 1	STITCH	15+					NO BREAK
Em 2		15+					" "
Bs 3		15+					" "
S/N19							
Em 1		15+					NO BREAK
Em 2		15+					" "
Bs 3		15+					" "
S/N28							
Em 1		15+					NO BREAK
Em 2		15+					" "
Bs 3		15+					" "

* NOTES:
(1) Wire break at neckdown point (due to bonding process).
(2) Wire break at point other than neckdown.
(3) Failure in bond (interface between wire and metallization).
(4) Lifted metallization (separation of metallization of bond pad from die or substrate).
(5) Fracture of die or substrate under the bond.

MICROELECTRONIC FAILURE ANALYSIS DATA SHEET
ENGINEERING FAILURE ANALYSIS LABORATORY
MARTIN MARIETTA DENVER

DATE: _____ PROGRAM: _____ I.D. NO: _____
PART NO: _____ NOMENCLATURE: _____ S/N: _____
LOT NO: _____ TEST NO: _____ MANUFACTURER: _____
REPORTED FAILURE/DEGRADATION MODE: _____

KEY: *Electrical Parameter(s) measurement required to detect change. Curve Tracer photographs required. Lab Data Sheet 102 required.

**Photomicrographs required in these steps.
○1 Standard steps required in obtaining a device "short finger print" (used to support Project Component evaluation programs).
○2 Standard steps required in obtaining a device "total finger print" (used to support Tech Ops support or research programs).

I. EXTERNAL ANALYSIS

○1,2 Electrical parameters (record on Lab Data Sheet 102) _____

○1,2 External microscopic exam _____

○1,2 X-Ray (photographs mandatory) _____

*○1,2 External rinse (D.I. water/HF) _____

○1,2 Hermetic seal check (fine/gross) _____

*○1,2 Environmental tests (specify) _____

○2 Gas Ambient Analysis _____
NOTE: Consultation mandatory before continuing.

II. INITIAL INTERNAL ANALYSIS

*○1,2 Decap device _____

**○1,2 Surface microscopic exam _____

○1,2 Photomicrograph (mandatory for abnormalities) _____

*○2 Vacuum bake and effluent analysis _____

○2 Surface rinse (D.I. water/HF) _____

NOTE: Consultation mandatory before continuing.

III. SURFACE ANALYSIS

( )1,2 Infra-Red topographical plot _____

** ( )1,2 Surface Profilometry _____

** ( )1,2 Functional mapping by SEM _____

** ( )2 EBIC Analysis by SEM _____

** ( ) Micromanipulator Probing _____

** ( )2 Die Passivation, Metalization, Thermal Oxide Preferential Removal _____

NOTE: Consultation mandatory before continuing.

IV. SUBSTRATE/SURFACE ANALYSIS

** ( )1,2 Microsection and Metallographic exam _____

** ( )2 Chemical Analysis _____

** ( )2 Scanninng Electron Microscopy - Energy Dispersive X-Ray Analysis _____

** ( )2 Electron Microprobe Analysis _____

** ( ) Auger, ESCA, Ion Microprobe _____

V. FAILURE MECHANISM (Consultation Required)

_____
Analyst

DATE: / / | RADC SYSTEM SUPPORT REQUEST | NO. ____

SYSTEM/EQUIP NO.: | GOV. CONTRACTOR:

RESP. GOV. AGENCY: | DATE OF REQUEST: / /

GOV. AGENCY CONTACT:

RADC SS CONTACT:

PART NOMENCLATURE

MANUFACTURER	PART TYPE NO.	SERIAL/LOT NO.	DATE CODE	PACKAGE TYPE	HER. TYPE:	PLASTIC TYPE:

PART TEST HISTORY

RADC IN-HOUSE PART FAILURE | | SYSTEM PART FIELD FAILURE |

PART SCREEN TESTED: | YES | | NO | | PART MFG. | | SYSTEM CONTRACTOR | | RADC |

TEST FAILED:

FAILURE MODE DATA

PART FAILURE MODE:

ADDITIONAL REMARKS:

RADC ENGINEER/S: | TELEPHONE:

DATE: / / | RADC FAILURE ANALYSIS REPORT | NO. ___

SYSTEM/EQUIP NO.: | GOV. CONTRACTOR:

RESP. GOV. AGENCY: | DATE OF REQUEST: / /

GOV. AGENCY CONTACT: | DATE FA STARTED: / /

RADC SS CONTACT: | DATE FA COMPLETED: / /

PART NOMENCLATURE

MANUFACTURER	PART TYPE NO.	SERIAL / LOT NO.	DATE CODE	PACKAGE TYPE	HER. TYPE:	PLASTIC TYPE:

PART TEST HISTORY

RADC IN-HOUSE PART FAILURE | | SYSTEM PART FIELD FAILURE |

PART SCREEN TESTED: | YES | | NO | | PART MFG. | SYSTEM CONTRACTOR | RADC

TEST FAILED:

FAILURE ANALYSIS DATA

PART FAILURE MODE:

FAILURE ANALYSIS SUMMARY:

ACTION TAKEN / RECOMENDATIONS:

DETAILED FA REPORT AVAILABLE: | YES | | NO | | RPT. TITLE/NO.

ADDITIONAL REMARKS:

RADC ENGINEER/S: | APPROX. MHRS. EXPENDED:

BIBLIOGRAPHY

1. Glaser, A.B., and G.E. Subak-Sharpe. Integrated Circuit Engineering, Addison-Wesley Publishing Company, Reading, Massachusetts, 1977. pp. 280 - 286, 618 - 629.

2. Hamilton, D.J., and W.G. Howard. Basic Integrated Circuit Engineering, McGraw-Hill Book Company, New York, 1975.

3. Verdnis, Andrew. Integrated Circuit Fabrication Technology, Reston Publishing Company, Incorporated, Reston, Virginia, 1979.

4. McWhorter, Gene. Understanding Digital Electronics, a text in the Texas Instruments Learning Series, Texas Instruments Incorporated, 1978.

5. (No Author). Manual Two - Integrated Circuit Devices and Components, part of McGraw-Hill Operation Update series, McGraw-Hill Book Company, 1978, pp. 2 - 72.

6. General Electric Staff. SCR Manual, Fifth Edition, General Electric Company, Syracuse, New York, 1972, pp. 15 - 183.

7. International Rectifier Staff. SCR Applications Handbook, International Rectifier Corporation, El Segundo, California, 1974.

8. Blood, W.R., Jr. MECL - System Design Handbook, First Edition, Motorola Semiconductor Products Incorporated, October 1971.

9. ICE Staff. Microcircuit Manufacturing Control Handbook, Volume I, Integrated Circuit Engineering Corporation, Scottsdale, Arizona.

10. Torrero, E.A. "The Multifacets of I^2L," IEEE Spectrum, Volume 14, Number 6, June 1977, pp. 28 - 36.

11. Meyer, David D., and William J. Laughton. "Evaluation of Charge-Coupled Device Technology," Class 2 General Electric Company document for General Electric Employees only, Syracuse, New York, November 1976.

12. Beynon, J.D.E., and D.R. Lomb. Charge-Coupled Devices and Their Applications, McGraw-Hill Book Company (UK) Limited, London, 1980.

13. Canon, Don L., Gerald Luecke, and G. Richard. MOS Integrated Circuits Course Lesson Summary, Texas Instruments Learning Center, Texas Instruments, Dallas, Texas.

SECTION II

REFERENCE DOCUMENTS AVAILABLE

II. REFERENCE DOCUMENTS AVAILABLE

A. Reliability Physics Notebook. Volume I was a discussion of significant reliability factors such as parts derating, parts screening, and general environmental considerations for high reliability devices.

Volume II of this document was the early reference source for the reliability engineer working in the semiconductor and hybrid microelectronics industry in the late 1960s. The document was the result of a contract to collect, analyze and interpret reliability data for updating the original parts failure rate data supplied by Rome Air Development Center (RADC). The part types covered are:

1. Resistors
2. Potentiometers (variable resistors)
3. Capacitors
4. Connectors
5. Relays
6. Switches
7. Magnetic Devices
8. Rotating Devices
9. Electronic Tubes
10. Semiconductors
11. Microelectronics
12. Wire and Cable
13. Low Population Parts

For each of these part types, a general information section, procedure for determining failure rates, and the prediction information and/or computational procedure were presented.

Document Summary

Title	RADC Reliability Physics Notebook Volumes I and II
Designation	RADC-TR-67-108
Contractor	Hughes Aircraft Company
Authors	Clifford M. Ryerson Sammie L. Webster Fred G. Albright
Date	September 1967
Total Pages	492

B. Integrated Circuit Engineering (ICE)/Rome Air Development Center (RADC) Microcircuit Manufacturing Control Handbook.

1. Introduction. This document was intended to be a reference guide to microcircuit manufacturing process engineers and to be primarily directed toward the semiconductor processing steps and their critical parameters and potential problem areas. The document has six major sections which are labeled:

a) Introduction
b) Processes
c) Process Control
d) Analytical Techniques
e) Problem Areas

There is also an appendix with major items of equipment described with model numbers, manufacturers and cost information. Emphasis in the document is in the problem area section with approximately one-third of the document covering this area. A good description of the processing steps for each of the following technologies is given in the processes section.

a) Linear or ECL
b) TTL or DTL Digital
c) Schottky Barrier Digital
d) Standard P-channel MOS
e) Ion Implanted PMOS
f) Complementary MOS (CMOS)
g) Silicon Gate NMOS
h) Silicon on Sapphire (Spinel)(SOS)
i) Integrated Injection Logic (I^2L)
j) Charge Coupled Devices (CCD)
k) Dielectric Isolation (DI)

Document Summary

Title	Microcircuit Manufacturing Control Handbook Volume I
Designation	None
Contractor	Integrated Circuit Engineering (ICE)
Authors	ICE/RADC
Date	July 1975
Total Pages	Contents Periodically Updated

C. Reliability Physics Symposium Proceedings.

1. Introduction. The major source of information on reliability physics phenomena of electron devices is the annual proceedings of the International Reliability Physics Symposium (IRPS). The symposium began in 1962 and at that time was called "Physics of Failure in Electronics." The first four symposia (1962 to 1965) were jointly sponsored by RADC and IITRI. The fifth (1966) was jointly sponsored by RADC and Battelle Memorial Institute. In 1967 (6th annual), the name was changed to "Reliability Physics Symposium" and the joint sponsorship by IEEE's Electronic Devices Society and IEEE's Reliability Group began and has continued to the present. This conference is generally held in April of each year.

Typically, the conference covers the technical areas of integrated circuit failure modes and mechanisms and the evaluation of failure models for these mechanisms. Even though the integrated circuit complexity has gone from SSI to VLSI, the principal failures are still related to the fundamental device and environmental factors of moisture, packaging materials and device metallization. These and many of the other traditional failure mechanisms are covered in the industry studies of state-of-the-art semiconductor devices.

2. Availability. The proceedings, starting with the 6th annual, are available from the IEEE on microfiche. The microfiche proceedings from 1967 to 1977 must be purchased as a complete set. Order Catalog Number 77CM1195-7 PHY. Starting with 1978, individual proceedings may be ordered on microfiche. There are, however, a few copies of the more recent proceedings still in print (soft bound or hard bound). Orders for microfiche or printed proceedings should be directed to: IEEE Service Center, Conference Publication Sales, 445 Hoes Lane, Piscataway, NJ 08854. To determine price and availability, call (201)981-0060.

The IEEE catalog numbers for the IEEE sponsored symposia proceedings are as follows:

a)	6th Annual 1967	-	Number 7-15C58
b)	7th Annual 1968	-	Trans, Elect. Devices, ED-16, No. 4, April 1969
c)	8th Annual 1970	-	Number 70C59-PHY
d)	9th Annual 1971	-	Number 71-C-9-PHY
e)	10th Annual 1972	-	Number 72 CH0628-8 PHY
f)	11th Annual 1973	-	Number 73 CH0755-9 PHY
g)	12th Annual 1974	-	Number 74 CH0839-1 PHY
h)	13th Annual 1975	-	Number 75 CH0931-6 PHY
i)	14th Annual 1976	-	Number 76 CH1072-8 PHY
j)	15th Annual 1977	-	Number 77 CH1195-7 PHY
k)	16th Annual 1978	-	Number 78 CH1294-8 PHY
1)	17th Annual 1979	-	Number 79 CH1425-8 PHY
m)	18th Annual 1980	-	Number 80 CH1531-3 PHY
n)	19th Annual 1981	-	Number 81 CH1619-6 PHY

3. Search and Retrieval Index to IRPS Proceedings. The Reliability Analysis Center (RAC), operated by IITRI under contract to RADC, has prepared an in-depth index of the papers contained in the International Reliability Physics Symposium (IRPS) (i.e., from 1968, 7th Annual to 1978, 16th Annual). This index is designed primarily for use by the failure analyst and researcher. It makes possible rapid information retrieval on reliability physics topics.

In addition to the technical terms index and the chronological list of papers three other sections are included:

a) Author Index. This is an alphabetical list of all authors cited in the proceedings, whether principal or secondary.

b) Corporate Index. This is an alphabetical list of all corporations, companies, institutions and government agencies with whom the authors were affiliated at the time the papers were prepared.

c) Keyword in Title Index. This is an alphabetical list of selected keywords in the title of the papers. Citations include paper number and title.

4. Index Availability. This index is available in print and may be purchased at the Symposium or from: Reliability Analysis Center, RADC/RBRAC, Griffiss AFB, NY 13441, Telephone (315) 330-4151 or Autovon 587-4151. Inquiries regarding updates should also be directed to the above address.

D. Advanced Techniques in Failure Analysis (ATFA) Symposium. The former ATFA Symposium was sponsored by the International Society for Testing and Failure Analysis in cooperation with the Institute of Electrical and Electronic Engineers and the International Metallographic Society. Meetings have been held in September or October of each year mainly in the Los Angeles, California, area. Renamed the International Symposium for Testing and Failure Analysis, under the sponsorship of the International Society for Testing and Failure Analysis, the symposium has a Failure Analysis Workshop which is held either a day earlier or a day later than the technical paper sessions. At these workshops, the beginning failure analyst can become acquainted with some of the basic procedures and techniques used in failure analysis and benefit from the experience of other analysts in the field. The symposium program typically lasts several days with papers covering areas such as:

1. Microelectronic Failure Analysis Techniques
2. Analysis of Structural Failures
3. Passive Components
4. Reliability Screening and Testing
5. Analytical Techniques
6. Large Scale Integration

Symposium is dedicated to the education and extension of techniques for failure analysis, screening and testing, and diagnostics. Copies of proceedings can be obtained from ATFA, Inc., 2882 Salmon Dr., Los Alamitos, CA 90720.

E. Scanning Electron Microscopy (SEM, Inc.). An international meeting usually held in Chicago, Illinois, but has been held in other major cities. Symposium is an international review of advances in techniques and applications of the Scanning Electron Microscope. The proceedings are published in two to three volume sets by Scanning Electron Microscopy, Inc., P.O. Box 66507, AMF O'Hare, Illinois 60666, USA.

F. Microbeam Analysis Society (MAS). Primarily a society of microbeam users founded in 1967. There are reported to be 700 members made up of persons or businesses who are interested in electron beam microprobe analysis, scanning electron microscopy, and other uses of electron and ion probes and surface analysis

techniques. Society publishes a journal entitled "Micronews" four times a year and annual abstracts. Annual convention/meeting was held in August 1979 at San Antonio, Texas. Contact Robert Myklebust at National Bureau of Standards in Washington, D.C. 20234 for additional information. Copies of the annual conference proceedings can be obtained from Ann Arbor Science Publishers, Inc., P.O. Box 1425, Ann Arbor, Michigan 48108.

G. Integrated Silicon Device Technology.

Research Triangle Institute (RTI)
Durham, North Carolina 27702

An extensive series exists on nearly every semiconductor processing step or related analytical technique. These documents are becoming somewhat dated from a chronological viewpoint but are still useful to the person with limited "hands-on" semiconductor processing experience. A list of document identification numbers with titles and preparation dates are provided below:

AD 408 961	Resistance (Vol. I, June 1963)
AD 423 148	Capacitance (Vol. II, Oct. 1963)
AD 603 715	Photoengraving (Vol. III, Jan. 1964)
AD 603 716	Diffusion (Vol. IV, Feb. 1964)
AD 605 558	Physical/Electrical Properties of Silicon (Vol. V, July 1964)
AD 613 951	Unipolar Transistors (Vol. VI, March 1965)
AD 618 704	Oxidation (Vol. VII, June 1965)
AD 630 894	Diodes (Vol. VIII, March 1966)
AD 624 520	Epitaxy (Vol. IX, Augus. 1965)
AD 626 985	Chemical/Metallurgical Properties of Silicon (Vol. X, Nov. 1965)
AD 632 556	Bipolar Transistors (Vol. XI, April 1966)
AD 643 610	Measurements Techniques (Vol. XII, Sept. 1966)
AD 655 081	Intraconnections and Isolation (Vol. XIII, May 1967)
AD 654 630	Interconnections and Encapsulation (Vol. XIV, May 1967)
AD 655 082	Reliability (Vol. XV, May 1967)
	Functional Design (Vol. XVI, May 1967)

H. Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium Proceedings.

1. Introduction. The EOS/ESD Symposium and Proceedings are a major source for information on the phenomena of electrical overstress and electrostatic discharge. Sponsored by IITRI, the symposium was first held in 1979; at present, it convenes yearly in September.

The symposium addresses all aspects of electrical overstress of electronic parts with emphasis placed on electrostatic discharge effects and problems. Microcircuit modeling, failure mechanism studies, susceptibility testing, failure simulation techniques, damage analysis, protective device structures and networks, sources of EOS, controlling the environment to prevent ESD exposure, human factors and case histories are applicable topics covered by this symposium.

2. Availability. The published Proceedings are available and can be purchased from the Reliability Analysis Center. Inquiries or orders for the EOS/ESD Symposium Proceedings should be directed to: Reliability Analysis Center, RADC/RBRAC, Griffiss AFB, NY 13441, or Telephone (315)330-4151 or Autovon 587-4151.

I. GIDEP Alert System.

1. Introduction. The Government-Industry Data Exchange Program (GIDEP) is a cooperative activity between Government and Industry participants seeking to reduce or eliminate expenditures of time and money by making maximum use of existing knowledge. The program provides a means to exchange certain types of technical data essential in the research, design, development, production and operational phases of the life cycle of systems and equipment.

Participants in GIDEP are provided access to four major data banks. The proper utilization of these data banks can assist in the

improvement of quality and reliability and reduce costs in the development and manufacture of complex systems and equipment.

The Engineering Data Bank (EDB) contains engineering evaluation and qualification test reports, nonstandard parts justification data, parts/materials specifications, manufacturing processes, failure analysis data, and other related engineering data on parts, components, materials, and processes.

The Reliability and Maintainability Data Bank (RMDB) contains failure rate/mode data on parts and components based on field performance information and reliability demonstration tests on operational systems and equipment.

The Metrology Data Bank (MDB) contains test equipment calibration procedures and related metrology engineering data on test systems, calibration systems, and measurement technology.

The Failure Experience Data Bank (FEDB) contains GIDEP ALERTs, consisting of objective failure information generated wherever significant problems are identified on parts and materials or safety.

The ALERT system provides the GIDEP participants with identification and notification of actual or potential problems on parts, components, materials, manufacturing processes, test equipment, or safety conditions. The initiator of the ALERT coordinates the ALERT with the manufacturers (vendors) when applicable, then forwards it to the GIDEP Operations Center for distribution to all participants.

The Urgent Data Request (UDR) system permits any participant with a technical problem to rapidly query the scientific and engineering expertise of all participant organizations. A UDR form is initiated by the member and sent to the GIDEP Operations Center for distribution to all participants. Responses are provided directly to the person making the query and are also incorporated into the appropriate data bank.

GIDEP has a rapid data retrieval system which makes the microfilmed information in the data banks immediately accessible to all participants through either hard-copy indexes or the use of remote computer terminal index searches.

Examples of a typical ALERT and all the forms associated with GIDEP are shown in pages II-11 through II-22.

2. Participation. Organizations may participate without charge in any or all of the above data banks by agreeing to abide by preestablished requirements for participation.

GIDEP participants are not subject to any fees or assessments. However, each participating organization must provide an internal program operation to include at least one Representative, a microfilm reader-printer, and adequate working area within its facility. In industry these expenses are not normally underwritten by the government, regardless of contract status, since the savings and cost avoidance accruing from proper program usage should far exceed the internal operating costs.

A GIDEP participant may be either a government or industry activity engaged in the design development, test, production, or support of major equipment and systems. Participants are primarily users of parts, components, and materials, rather than manufacturers of these items.

During one calendar year a major industrial participant was able to document in excess of 2 million dollars in savings/cost avoidance through the application of GIDEP data to all phases of its activities.

Participation requirements or additional information about GIDEP may be obtained by contacting the Director, GIDEP Operations Center, Corona, California 91720. Telephone: (714)736-4677 or Autovon: 933-4677.

(PLEASE TYPE ALL INFORMATION)

1. PART/MATERIAL TYPE
Integrated Circuit
J-K Master Slave
Flip Flop

ALERT

ALERT NO. F9-70-01

DATE 10-8-70 (DAY | MO. | YEAR)

2. MANUFACTURER & ADDRESS
Signetics Corporation
811 East Arques Avenue
Sunnyvale CA 94086

3. INDUSTRY/GOVT SPEC. NO.
Hazeltine Corp.
Part Number C6600J

4. REFERENCE
RADC Detailed Failure Analysis Report Available 15 August 1970

5. MANUFACTURER'S PART NO.
S5472J

6. PART RATING OR SIZE
14 Lead Metal-Ceramic "J" Package

7. MANUFACTURER'S LOT OR DATE CODE
6908 Thru 6914

8. MANUFACTURER'S SERIAL NO.
N/A

9. PROGRAM OR SYSTEM
ESD 416M/P/418L SPO
AIMS AN/GPA-124/125

10. SPECIAL REQUIREMENTS OR ENVIRONMENT
Coder-Decoder functional failures occurred during operational equipment testing at a 100°F ambient temperature due to S5472J IC failures.

11. LOCATION & FUNCTION
AIMS AN/GPA-124/125 Coder-Decoder Equipments at Hazeltine New York Plant and Operational Test Sites.

12. PROBLEM SITUATION AND CAUSE (FAILURE MODE & MECHANISM)
S5472J IC failures at elevated temperature. Circuit failure mode identified by Hazeltine and verified by RADC was output "inhibit" mode functional failure (i.e., output toggled under grounded "J" input conditions at elevated temperature). The ICs recover upon return to room ambient temperature. RADC failure analysis identified the two basic failure mechanisms:

a. A design error in the photolithographic diffusion masks used by Signetics to fabricate the S5472J die. The design error is a missing n^+ diffusion used for ohmic contact to the n-type resistor tub associated with the "J" inputs.

b. Surface inversion due to either bulk oxide or oxide surface contamination which was production lot dependent (i.e., date codes 6908 thru 6914).

13. ACTIONS TAKEN
Signetics Corp. was notified of RADC's failure analysis findings and verified the existence of the diffusion photomask omission and a surface inversion problem on S5472J circuits date coded 6908-6914. Signetics instituted a 125°C functional "inhibit" screen test on all Hazeltine S5472J products. However, this test was shown by RADC to pass marginal circuits. RADC developed two 25°C DC electrical tests (low cost) defined below which will reject all potentially unreliable S5472Js. Signetics accepted RADC's screens for the AIMS program, but currently does not conduct the 125°C "inhibit" test or the 25°C electrical parameter screens on other S5472J procurements. Signetics indicated that the redesign of their 8000 series circuits would correct the diffusion.

14. RECOMMENDATIONS FOR FURTHER ACTION
RADC recommends two DC 25°C electrical screen tests for subject ICs: (a) Vcc-to-Substrate Leakage Current: Vcc = +0.40 volts, I = 1.0 ua max, and (b) Clear-to-Substrate Leakage Current: Clear = +5.0 volts, I = 1.0 ua maz. In addition, RADC recommends the following High Temperature Screen implemented by Signetics for these circuits. This test is a 48 hour "Inhibit" Functional Test with Ta = 125°C.

15. SOURCE OF INFORMATION (ORGANIZATION/INDIVIDUAL)
EDGAR A DOYLE, JR./GERALD G. SWEET
RADC (EMNRP)
Griffiss AFB, NY 13440

TELEPHONE
(315) 330-2778

16. MANUFACTURER NOTIFIED DATE (DAY | MONTH | YEAR)
20 | 5 | 70

17. TYPED NAME OF ALERT COORDINATOR
GEORGE W. LYNE
RADC (EMNRC)
Griffiss AFB, NY 13440

TELEPHONE
(315) 330-4726

18. DATE (DAY | MO. | YEAR)
28 | 5 | 70

19. SIGNATURE OF ALERT COORDINATOR
G.W. LYNE

NASA FORM 993 OR DCS FORM 41 12 69

ALERT NO. F9-70-01

ITEM 12. PROBLEM SITUATION AND CAUSE (Cont'd)

The diffusion photomask omission is inherent to the S5472J, N5472A (-55°C to 125°C) and the lower temperature electrically equivalent S7472J, N7472A circuits. All Signetics current production lots contain the photomask fault.

The diffusion photomask omission results in a parasitic PNP transistor (open base) which can result in excessive leakage current from J tub resistors and cross-unders to the substrate and slight forward bias of all resistors to their n-type tub. Further, the fault enhances surface inversion when a contaminated bulk oxide or surface ions are present. Direct ohmic contact to the n-type tub with +Vcc applied is a standard IC design practice to prevent the above forward bias condition and minimize the effect of leakage currents on circuit functional failure. Failure of these S5472J circuits is the combined result of the omitted diffusion and the presence of surface inversion conditions. The diffusion photomask omission by itself is not sufficient to cause circuit failure. However, the surface inversion is lot dependent and can be a recurring problem in that production lots having oxide contamination are susceptible to failure at elevated temperature.

Item 13. Actions Taken (Cont'd)

photomask omission, however, the 5400 chips would not be redesigned. To our knowledge then, all current and future 5472 production chips will still contain the diffusion photomask omission.

Item 14. Recommendations for Further Action (Cont'd)

Input J's at +0.8 volts, +2.4-Clock Pulse and +5 volts Vcc applied. Under these test conditions output Q must remain stable at Logical "1" Level (~4 volts). The required 48 hour stress test period is based on RADC data on S5472J circuit failures. RADC further recommends that S5472J circuits in high reliability equipments be replaced with circuits screened as recommended. S5472Js date coded 6908 thru 6914 represent an extremely high reliability risk in view of the surface problem detected. All S5472J, N5472A, S7472J, and N7472A procurements should incorporate the screens delineated herein from maximum reliability of subject circuits.

OMB NO. 22-R0328

GOVERNMENT-INDUSTRY DATA EXCHANGE PROGRAM

ALERT

Please Type All Information – See Instructions On Reverse

1. NOMENCLATURE *(Part/Material/Hazard/Safety Problems)*	2. ALERT/SAFE-ALERT NO.
	3. DATE *(Day, Month, Year)*

4. MANUFACTURER AND ADDRESS	5. NSN	
	6. PROCUREMENT SPECIFICATION	7. REFERENCE
	8. MANUFACTURER'S PART NUMBER	9. LOT/DATE CODE OR SERIAL NO.

10. SPECIAL REQUIREMENTS OR ENVIRONMENT *(Requirements placed on, or extreme environment to which item was exposed)*

11. PROBLEM SITUATION AND CAUSE *(State facts of problem and cause–failure mode and mechanism–project and function)*

12. ACTIONS TAKEN *(State all actions taken to correct the problem situation and to prevent its recurrence)*

13. DATE MFR NOTIFIED *(Day, Month, Year)*	14. MANUFACTURER RESPONSE ☐ CORRESPONDENCE ATTACHED ☐ DID NOT REPLY	15. CONTACT POINTS FOR INFORMATION *(Name, Affiliation, Phone)*

16. ALERT COORDINATOR *(Name, Affiliation)*	17. SIGNATURE OF ALERT COORDINATOR

DD FORM 1 NOV 78 1938

ALL PREVIOUS EDITIONS ARE OBSOLETE

18. NOMENCLATURE

19. ALERT/SAFE-ALERT NO.

INSTRUCTIONS FOR PREPARING ALERT FORM

1. NOMENCLATURE – Enter major subject category classification and function information. This is obtained from Section 12 of the Government–Industry Data Exchange program (GIDEP) Policies and Procedures (P&P) Manual.

2. ALERT/SAFE ALERT NO. – Use originator's code assigned by GIDEP. Enter letter "A" for ALERTS or letter "S" indicating SAFE ALERT when subject or ALERT affects health or safety of personnel who may come in contact with defective part or unit it is assembled into. The letter is followed by last two digits of year and then by consecutive sequence number of all ALERTs submitted by the originator for that year. An addendum is indicated by adding a change letter (A, B, or C, as required) to the sequence number. For example: XX–A–77–02A is ALERT number for addendum to second ALERT in 1977 by an originator with code XX.

3. DATE – This is date ALERT is released by ALERT Coordinator. Note coordination procedures in 13. Each addendum should have new release date.

4. MANUFACTURER AND ADDRESS – List actual manufacturer of item. Also enter Manufacturer's Federal Code Number (MFCN) from Federal Handbook H4–1 or H4–2. When possible, also enter Contract Administration Service Code Number (CASN) from DOD 4105.59–H. If supplied from source other than manufacturer and this is pertinent, also list the source here or in Block 10. If ALERT is against a category or application, do not identify manufacturer.

5. NATIONAL STOCK NUMBER – (Formerly Federal Stock Number.) List applicable number. If several numbers are applicable and space is not available, place asterisk after last number and continue entry in Block 10. As a minimum, enter Federal Supply Class.

6. PROCUREMENT SPECIFICATION – List applicable procurement specification and name of issuing organization. Include, in Block 10, nearest government or industry specification and any exceptions or special recognized government or industry specification requirements which were imposed.

7. REFERENCE – List any applicable documentation not included as part of this ALERT, e.g., previous ALERT number, TWX, or report number.

8. MANUFACTURER'S PART NUMBER – List manufacturer's catalog identification/part number of item. If different than procurement specification identification, list nearest similar manufacturer's identification and list differences in Block 11.

9. LOT/DATE OR SERIAL NO. – When problem is applicable to only certain lot/date code or serial numbered items, list appropriate code or number. Use year purchased if other information is not available. Blank space indicates "all."

10. SPECIAL REQUIREMENTS OR ENVIRONMENT – State any special requirements placed on item or any special or extreme environment to which it was subjected. This would include any exceptions or requirements other than imposed in applicable procurement specification listed in Block 6.

11. PROBLEM SITUATION AND CAUSE – State facts of problem and cause, including failure mode and mechanism.

12. ACTIONS TAKEN – State all actions taken to correct problem situation and to prevent further occurrences. This will include any actions taken by manufacturer, if known.

13. DATE MANUFACTURER NOTIFIED – Release of ALERT requires that a copy be sent to manufacturer identified in Block 4 and fifteen (15) working days be allowed for a reply. When available, attach a copy of the reply to the ALERT.

14. MANUFACTURER RESPONSE – Item manufacturer must be notified. When manufacturer correspondence is included, check CORRESPONDENCE ATTACHED entry. When manufacturer does not reply, check DID NOT REPLY entry. If ALERT is against a category or application and manufacturer is not identified, enter N/A in CORRESPONDENCE ATTACHED entry.

15. CONTACT POINTS FOR INFORMATION – Enter name, affiliation, and telephone number of persons to contact for further information. This may include designated personnel from ALERT originator's organization, or any other organization.

16. ALERT COORDINATOR – Enter name and affiliation of the ALERT Coordinator.

17. SIGNATURE – Signature of ALERT Coordinator.

18. NOMENCLATURE – Same as in Block 1.

19. ALERT/SAFE–ALERT NO. – Same as in Block 2.

OMB NO. 22-R0336

GOVERNMENT-INDUSTRY DATA EXCHANGE PROGRAM

GENERAL DOCUMENT SUMMARY SHEET

1 OF

Please Type All Information – See Instructions on Reverse

1. ACCESS NUMBER	2. COMPONENT/PART NAME PER GIDEP SUBJECT THESAURUS	
3. APPLICATION	4. MFR NOTIFICATION ☐ NOTIFIED ☐ NOT APPLICABLE	5. DOCUMENT ISSUE (Month/Year)
6. ORIGINATOR'S DOCUMENT TITLE		7. DOCUMENT TYPE ☐ GEN RPT ☐ NONSTD PART ☐ SPEC
8. ORIGINATOR'S DOCUMENT NUMBER	9. ORIGINATOR'S PART NAME/IDENTIFICATION	
10. DOCUMENT (SUPERSEDES) (SUPPLEMENTS) ACCESS NO.	11. ENVIRONMENTAL EXPOSURE CODES	
12. MANUFACTURER	13. MANUFACTURER PART NUMBER	14. INDUSTRY/GOVERNMENT STANDARD NUMBER

15. OUTLINE, TABLE OF CONTENTS, SUMMARY, OR EQUIVALENT DESCRIPTION

16. KEY WORDS FOR INDEXING	
17. GIDEP REPRESENTATIVE	18. PARTICIPANT ACTIVITY AND CODE

DD FORM 1 NOV 78 2000

REPRODUCTION OR DISPLAY OF THIS MATERIAL FOR SALES OR PUBLICITY PURPOSES IS PROHIBITED

INSTRUCTIONS FOR COMPLETING THE GIDEP GENERAL DOCUMENT SUMMARY SHEET

NOTE: Completion of a Summary Sheet by the participant is not mandatory for document acceptance into GIDEP. A Summary Sheet will be prepared by the GIDEP Operations Center for document submittals received.

PAGE 1 OF — Enter the total number of summary sheet pages

BOX

1 — Leave blank--entry will be completed by GIDEP Operations Center.

2 — Enter standard nomenclature associated with GIDEP Subject Thesaurus selected from Section 12, Policies and Procedures Manual.

3 — Indicate application which the device was used (e.g., ground, missile, shipboard, spacecraft; refer to P & P Manual, Section 13).

4 — Device manufacturer must be notified of test results. Manufacturer approval of report is not required--include pertinent manufacturer correspondence with document submittal to GIDEP; check NOTIFIED entry. If document is for a nonstandard part or of a general nature and a manufacturer is not identified, check NOT APPLICABLE.

5 — Enter month and year of document issue.

6 — Enter complete document title exactly as it appears on originator document.

7 — Identify document type by inserting letter X by appropriate descriptor.

8 — Enter document number exactly as it appears on originator document.

9 — Enter part name and identification as assigned by organization/agency originating the report; if not specified, enter N/A (Not Applicable).

10 — Delete either SUPERSEDES or SUPPLEMENTS. If document supersedes/supplements an existing GIDEP document, enter GIDEP microfilm access number of appropriate document. If document neither supersedes nor supplements an existing GIDEP document, enter the word NONE.

11 — Enter the single symbol coding for environmental exposure as defined in Subject Thesaurus, Section 12, P&P Manual (e.g., C – Salt Spray; V – Vibration; % – Shelf Life); if not specified, enter N/A (Not Applicable).

12 — Enter manufacturer abbreviation and H–4 Code number listed in GIDEP Manufacturer List. If manufacturer is not listed, enter the phrase, SEE BOX 15; enter manufacturer's full name and division (if any) in Box 15. If more than one manufacturer, enter phrase, SEE BOX 15; enter additional manufacturers as appropriate. If manufacturer is not specified, enter N/A (Not Applicable).

13 — Enter complete part number. Use open O for alpha letter O, and use Ø for numeric zero. If more than one part number, enter phrase, SEE BOX 15; enter additional part number(s). If a part number is not specified, enter four dashes (----).

14 — Enter standard part number such as the 1N or 2N--diode and transistor designators. For GIDEP purposes, any military assigned number is considered as a government standard part number. If more than one standard number, enter phrase SEE BOX 15; enter additional standard number(s).

15 — If subject matter in document can be categorized into more than one major subject category, enter additional subject categories in upper right-hand corner. Briefly summarize test results or material detailed in text of document. Include any pertinent details or comments required for proper interpretation of material presented (e.g., peculiar environmental capabilities, unique electrical characteristics that may be "state-of-the-art," or characteristics that restrict part usage to particular applications or any other details that may aid a prospective user of the part).

16 — Enter appropriate words or phrases that enhance information retrieval on subject matter(s) contained in document. As a secondary data retrieval technique within each applicable Major Category (entry 2), the document is referenced in the computer data bank and Report Index according to each key word. Do not use abbreviations or words that are part of the subject category listed in Box 2. Key word phrases are limited to 60 total characters and blank spaces. Separate key words and/or phrases with commas.

17 — Enter signature or name of GIDEP Representative.

18 — Enter name, city, and state of participant activity or corporation and division submitting the document and GIDEP two-character code (e.g., X1).

DD FORM 2000 (1 NOV 78) (BACK)

GOVERNMENT–INDUSTRY DATA EXCHANGE PROGRAM

DOCUMENT SUMMARY SHEET

Completion of Summary Sheet is Optional – Please Type All Information – See Instructions On Reverse

1. ACCESS NUMBER (Leave Blank – To be Completed by OC)	2. ORIGINATOR'S DOCUMENT NUMBER	3. DOCUMENT ISSUE (Month/Year)

4. COMPONENT/PART NAME PER SUBJECT THESAURUS	5. ORIGINATOR'S DOCUMENT TITLE

6. APPLICATION	7. MFR NOTIFICATION ☐ NOTIFIED ☐ NOT APPLICABLE	8. THIS DOCUMENT (SUPERSEDES) (SUPPLEMENTS) GIDEP ACCESS NUMBER

	9 PARAMETERS	10 MANUFACTURER AND H4 CODE	11 MFR PART NUMBER	12 INDUSTRY/GOVERNMENT STANDARD NUMBER	13 TOTAL TESTED	14 TEST EXCEED MFR SPEC
A		- - - - - - - - -				
B		- - - - - - - - -				
C		- - - - - - - - -				

	15 SOURCE DATA REQUIRED TO UTILIZE DOCUMENT	ENCL	SUBMITTED AS/WITH GIDEP ACCESS NUMBER
A			
B			
C			

16 ITEM	TEST OR ENVIRONMENT	SOURCE DATA REF	SOURCE DATA PARA, METHOD/CONDITION	TEST LEVELS AND OTHER DETAILS	ENVIR CODE	NUMBER TESTED	NUMBER FAILED

17. SUMMARY

18. KEY WORDS FOR INDEXING

19. GIDEP REPRESENTATIVE	20. PARTICIPANT ACTIVITY AND CODE

DD FORM 1 NOV 78 1999

INSTRUCTIONS FOR COMPLETING THE GIDEP DOCUMENT SUMMARY SHEET

NOTE: Completion of a Document Summary Sheet by the participant is preferred but not mandatory for document acceptance into GIDEP. A Summary Sheet will be prepared by the GIDEP Operations Center for document submittals received.

PAGE 1 OF Enter total number of summary sheet pages

BOX

1 Leave blank – entry will be completed by GIDEP Operations Center.

2 Enter document number exactly as it appears on originator document.

3 Enter month and year of document issue.

4 Enter standard nomenclature associated with GIDEP Subject Thesaurus selected from Section 12, Policies and Procedures Manual.

5 Enter complete document title exactly as it appears on originator document.

6 Indicate application which device was used (e.g., ground, missile, shipboard, spacecraft; refer to P & P Manual, Section 13).

7 Device manufacturer must be notified of test results by copy of report. Manufacturer approval of report is not required--include pertinent manufacturer correspondence with document submitted to GIDEP; check NOTIFIED entry. If manufacturer not identified, check NOT APPLICABLE.

8 Delete either SUPERSEDES or SUPPLEMENTS. If document affects an existing GIDEP document, enter microfilm access number of appropriate document. If document neither supersedes nor supplements an existing GIDEP document, enter word NONE.

9 Each line entry is used to differentiate between groups of test samples. All test samples grouped as a single ITEM should be identical. Enter characteristics such as, Part Type, Size, Rating, Lot/Date code or serial number, as required to describe test sample(s) without requiring document review.

10 Enter manufacturer abbreviation and H4 Code number listed in GIDEP Manufacturer Abbreviation List. If manufacturer not listed, enter phrase SEE BOX 17; enter manufacturer's full name and division in Box 17. If more than one manufacturer, enter phrase MULTIPLE, SEE BOX 17; make appropriate entries in Box 17. If manufacturer not specified, enter word NONE. If document pertains to a material or raw stock, enter phrase STOCK MATERIAL.

11 Enter complete part number (P/N). Use open O for alpha letter O and use a Ø for a numeric zero. If more than one manufacturer, enter phrase MULTIPLE, SEE BOX 17; make appropriate entries in Box 17. If document pertains to raw stock, enter type designation and material (e.g., 2014–T6 Aluminum). If P/N not specified, enter four dashes (----).

12 Enter standard P/N such as the 1N and 2N--diode and transistor designators. For GIDEP purposes, any military assigned number is considered as a government standard P/N.

13 Enter total of each test sample type or group tested. If any control samples were tested, use footnote symbol 1/; enter applicable information in Box 17.

14 Enter word YES as appropriate whenever test sample(s) subjected to test(s) that exceeded manufacturer specifications; leave blank as appropriate.

15 Identify applicable specification(s), standard(s), and acceptance test procedure required for document interpretation (e.g., MIL–STD–202). If reference enclosed, check ENCL column. Any documents or applicable sections required to utilize report shall be included with report. EXCEPTION: Military specifications or generally available industry association specifications. If reference previously submitted as a GIDEP document, list microfilm access number in SUBMITTED AS/WITH GIDEP ACCESS NUMBER column. If a document is not enclosed or referenced, enter NONE in SOURCE DATA REQUIRED TO UTILIZE DOCUMENT column.

16 ITEM. This entry used in conjunction with Boxes 9 and 13. For documents that contain only one item (line entry) in Box 9 and total number of devices listed in Box 13 have seen subjected to TEST OR ENVIRONMENT entry, enter ALL. When a test sample or subset of total devices is less than total of Box 13, enter designator A1 to identify which of selected parts were tested to environment specified. Each different subset for subsequent test environments requires a separate line entry and identified A2, A3, etc.

TEST OR ENVIRONMENT. Enter test or environment that test sample was subjected (e.g., salt spray, vibration, shelf life).

SOURCE DATA REF. Enter letter from Box 15 which identifies applicable reference.

SOURCE DATA PARA METHOD/CONDITION. Enter specific document paragraph and test method or condition used as part of reported test(s) (e.g., if a Vibration Test was recorded as TEST OR ENVIRONMENT entry and test performed in accordance with MIL–STD–202, Method 205, associated entry would be: 3.3.3; Method 205).

TEST LEVELS AND OTHER DETAILS. Briefly define test levels, duration, etc. (e.g., for Method 205, associated entry would be: Condition C, 50G peak).

ENVIR CODE. Enter single symbol coding for environmental exposure as defined in GIDEP Subject Thesaurus (e.g., C – salt spray; V – vibration; % – shelf life).

NUMBER TESTED. Enter total number of test samples exposed to specific test or environment.

NUMBER FAILED. Distinguish between a failure to satisfy requirements and an intentional test to failure. Note the latter type by indicating design limits vs point of failure.

17 If subject matter can be categorized into more than one major subject category, enter additional categories in upper right-hand corner. Briefly summarize test results or material. Include pertinent details required for proper interpretation of material presented (e.g., unique electrical characteristics that may be "state-of-the-art," or characteristics that restrict part usage to particular applications or any other details that may aid a prospective user of part).

18 Enter appropriate words or phrases that enhance information retrieval. As a secondary data retrieval technique within each applicable Major Category (entry 4), document is referenced in computer data bank and Report Index according to each key word. Do not use abbreviations or words that are part of subject category listed in Box 4. Key word/phrases are limited to 60 total characters and blank spaces. Separate key words and phrases with commas.

19 Enter signature or name of GIDEP Representative

20 Enter name, city and state of participant activity or corporation and division submitting the document and GIDEP two-character code (e.g., X1).

NOTE: USE EITHER GIDEP FORM DD 1999–1 OR 1999–2 FOR CONTINUATION PAGE AS REQUIRED.

MICROFILM ACCESS NUMBER	GOVERNMENT–INDUSTRY DATA EXCHANGE PROGRAM **RELIABILITY–MAINTAINABILITY DATA SUMMARY** *Please Type All Information – See Instructions On Reverse*	1 OF

1. ACTIVITY	CITY/STATE	NAME	TELEPHONE

2. CODE	3. CHECK ONE	4. REPORT NUMBER	5. DATE
	☐ FAILURE RATES ☐ REPLACEMENT RATES		

6. PROGRAM OR SYSTEM	7. OBSERVED ENVIRONMENT	8. OBSERVATION PERIOD (Mo/Yr) START FINISH	9. UNIT OF MEASURE

10. ELECTRICAL STRESS CAT % OF	11. TEMPERATURE CAT °C	12. MECHANICAL STRESS CAT TYPE	13. SCREENING CLASS SPEC NO

LINE	14. ITEM NOMENCLATURE	15. APPLICATION
1		
2		
3		
4		
5		
6		

LINE	16. VENDOR & H4 CODE	17. ITEM NUMBER	18. OTHER ITEM NUMBER(S)	19. NO. OF ITEMS
1				
2				
3				
4				
5				
6				

LINE	20. DURATION	21. NO. FAILURES	22. FAILURE RATE	23. MEAN REPAIR TIME	25. PREDOMINANT FAILURE MODE(S)
1					
2					
3					
4					
5					
6					

25. ADDITIONAL COMMENTS AND INFORMATION

SIGNATURE

DD FORM 1 NOV 78 2001

REPRODUCTION OR DISPLAY OF THIS MATERIAL FOR
SALES OR PUBLICITY PURPOSES IS PROHIBITED

INSTRUCTIONS FOR PREPARING RELIABILITY–MAINTAINABILITY DATA SUMMARY

Completion of this summary sheet is optional but preferred. The GIDEP Operations Center will prepare a summary sheet if none is provided with data submittal. All data submitted should be accompanied with a copy of the complete original report.

Please type, as this sheet will be microfilmed.

For large submittals enter "See Attached Report" in Block 25.

Be sure the information below as essential (*) is contained in the submittal.

For line items of differing stress and screening levels, use separate sheets.

Any questions should be directed to Officer in Charge, GIDEP Operations Center, Corona, California 91720. Phone: (714) 736–4677, AV 933–4677.

BLOCK

1 Enter submitting activity, location, name of individual, and telephone number.

2 Enter GIDEP participant code, per Section 3, GIDEP P and P (Policies and Procedures) Manual.

* 3 Indicate if failure or replacement rates per definitions in P and P Manual.

4 Enter the in–house original report number.

5 Enterrthe date of the report.

6 Enter the name of the parent program or system.

* 7 Enter the observed environment category and modifiers (see GIDEP P and P manual). Categories include: GND, MBL, SHP, SUB, MSL, SPC, HLI, PRP, JET, SST, WET, LAB, ABN, DOR (Dormant).

* 8 Enter beginning and ending dates (Month–Year) of the observation period.

* 9 Enter the unit of measure (e.g., Hrs, Days, Miles, Cycs, Rnds, Revs, Acts).

Use L – Low; M – Medium; H – High; and S – Severe for the categorizations in Blocks 10, 11, and 12.

10 Categorize the electrical stress and indicate the percentage and rating factor.

11 Categorize the typical temperature and indicate its value in degrees centigrade.

12 Categorize the mechanical stress and indicate the type (vibration, acceleration, stress–strain, etc.)

13 Classify the screening as A – High Reliability; B – Good Reliability; C – Commercial Grade. Indicate to what specification the screening was done.

*14 Provide the most complete descriptions possible of the parts/components/assemblies being reported.

15 Indicate for what application the item was used (e.g., navigation, communication, check out, etc.).

16 Use manufacturer name abbreviation from the GIDEP abbreviation list. If not listed, give H–4 code or complete name and address.

*17–18 Enter a vendor item number with the vendor's name, industry/government standard number, military specification number, and/or federal (NATO) stock number.

*19 Enter the total observed population of the item.

20 Enter the quotient of the total item experience (e.g., part–hours) divided by the total number of items.

21 Enter the total number of failures (or replacements if replacement rates).

22 Enter the calculated failure rate.

23 Enter the mean repair time (MRT, MTTR) if known (see definitions in GIDEP P and P Manual).

24 Enter the predominant failure mode(s).

25 Enter additional pertinent amplifying information.

DD FORM 2001 (1 NOV 78) (BACK)

GOVERNMENT–INDUSTRY DATA EXCHANGE PROGRAM

URGENT DATA REQUEST

Please Type All Information – See Instructions On Reverse

1. REQUESTER (Complete Items 1 thru 13)	2. DATE (Day, Month, Year)
	3. UDR NO.

4. SUBJECT CATEGORY

5. TYPE OF DATA NEEDED *(Check as required)*

☐	TEST	☐	FAILURE RATE	☐	FAILURE MODE	☐	METHODOLOGY
☐	DESIGN	☐	FAILURE EXPERIENCE	☐	SPECIFICATION	☐	MAINTENANCE
☐	METROLOGY	☐	OTHER *(Specify)*				

6. COMPONENT / PART / MATERIAL / TEST EQUIPMENT / PROCESS DESCRIPTION

7. MANUFACTURER	8. MANUFACTURER PART NUMBER	9. IND/GOVT STD NO.
10. APPLICATION (Aircraft, Missile, Shipboard)	11. SPECIFICATION NO.	

12. PERFORMANCE REQUIREMENTS

13. DATA SOURCES SEARCHED

If you can in any way help this GIDEP participant, please contact hi.. ..ctly. Then complete the remainder of this form and return it for report submittal credit to:

Officer in Charge, GIDEP Operations Center, Corona, California 91720

☐ INFORMED REQUESTER OF ADDITIONAL DATA SOURCES	IF NO DATA IS AVAILABLE DO NOT RETURN THIS FORM	☐ DATA AVAILABLE AND TRANSMITTED TO REQUESTER
DATE	NAME	PARTICIPANT
LOCATION (City and State)	PHONE NUMBER	SIGNATURE

DD FORM 1 NOV 78 2002

NO CHARGE OR OBLIGATION EITHER TO THE PARTICIPANT OR TO THE GOVERNMENT IS INCURRED BY THE TRANSMITTAL OF, OR THE RESPONSE TO THIS INFORMATION REQUEST

GIDEP URGENT DATA REQUEST (UDR) SYSTEM

The GIDEP Operations Center initiated the UDR system to enable greater communication and exchange of needed reliability information among GIDEP participants who need data which other participants might have. This UDR system is intended solely for the use of GIDEP participants and is operated on an entirely voluntary basis. It is anticipated that UDR's will be submitted as a last resort after all known available sources of information have been searched. Generally UDR's submitted to the GIDEP Operations Center will be reproduced and mailed out to all program participants within 24 hours of their receipt. To submit a UDR for distribution to GIDEP participants, fill out the numbered blocks on the reverse of this form according to the instructions below and mail it to

Officer in Charge
GIDEP Operations Center
Corona, California 91720

INSTRUCTIONS

BLOCK

1 REQUESTER: Enter name, address, and phone number of GIDEP Representative requesting information. Complete only items 1 through 13.

2 DATE: Enter date of request.

3 UDR NO.: Leave blank – GIDEP Operations Center will assign UDR number.

4 SUBJECT CATEGORY: Enter the major subject category as listed in Subject Thesaurus, Section 12 Policies and Procedures Manual.

5 TYPE OF DATA NEEDED: Check the appropriate box(es). If Other is checked, specify what other type of data is needed.

6 COMPONENT/PART/MATERIAL/TEST EQUIPMENT/PROCESS DESCRIPTION: Enter a brief but specific definition of the information required.

7 MANUFACTURER: Enter name of manufacturer as applicable.

8 MANUFACTURER PART NUMBER: Enter part number as applicable.

9 INDUSTRY/GOVERNMENT STANDARD NUMBER: Enter Industry/Government Standard number as applicable.

10 APPLICATION: Define general end use application.

11 SPECIFICATION NUMBER: List applicable government or industry specification number.

12 PERFORMANCE REQUIREMENTS: *Specify any other special conditions or requirements needed to be given in order to obtain the desired information.*

13 DATA SOURCES SEARCHED: List data sources which have been researched to eliminate repetitive efforts.

NOTE: When UDR replies are received, submit the data to the GIDEP OC according to the GIDEP Policies and Procedures manual.

J. Reliability Predictions, MIL-HDBK-217.

1. Introduction. The purpose of the Military Standardization Handbook MIL-HDBK-217C is to provide the best available data for predicting the reliability of military systems. Two methods of reliability prediction are illustrated. They are:

a) Part Stress Analysis
b) Parts Count

These methods vary in degree of information needed to apply them. The Part Stress Analysis requires the greatest amount of detail and is applicable during the later design phase where actual hardware and circuits are being designed. The Parts Count Method requires less information, generally that dealing with quantity of different part types, quality level of the parts, and the application environment. This method is applicable in the early design phase and during bid proposal formulation.

The Parts Stress Analysis Prediction section provides failure rate models for the following major part categories:

a) Microelectronics
b) Discrete Semiconductors
c) Tubes
d) Lasers
e) Resistors
f) Wire and Printed Wire Boards
g) Miscellaneous
h) Capacitors
i) Inductors
j) Motors
k) Relays
l) Switches
m) Connectors
n) Connections

Principal factors that are considered in these models are quality of the parts as procured, temperature, and equipment use environment. There are also secondary factors that are peculiar to the part type. Most of the models make use of a base failure rate, λ_b, which is usually a function of the electrical and thermal stresses on the part. Models for microelectronic parts are somewhat more complex and do not use a "base failure rate" as such. Instead, the model comprises several additive terms, each of which is a function of microcircuit complexity i.e., number of gates, bits or transistors depending upon the device type. The present microcircuit models in MIL-HDBK-217C was revised May 1, 1980 to reflect the results of a recently completed study. This revision expanded the existing models to more accurately reflect observed failure data for the larger microcircuits and for new technologies.

RADC has available a computer program for performing MIL-HDBK-217C predictions. The program is resident on the RADC time-shared computer and is accessible to both Air Force agencies and their contractors through the ARPA computer network. A few of the many features included in the program are:

a) Updated parts failure rates
b) Automatic flatting of overstressed parts
c) System modeling, including redundance considerations
d) Iterations for examining impact of changes in parts, temperature, etc.

Use of the program reduces time for accuracy verification and eliminates the need for contractors to develop their own program. Further details and instructions for access to the program or user's manual can be obtained by contacting RADC/RBRT (Mr. George Lyne), Griffiss AFB, NY 13441, Autovon 587-3476 or Commercial (315)330-3476.

Document Summary

Title	Military Standardization Handbook Reliability Prediction of Electronic Equipment
Designation	MIL-HDBK-217C
Contractor	RADC Griffiss AFB, NY is the preparing activity (PA)
Authors	Air Force Contract - Mr. Lester J. Gubbins RADC/RBET Griffiss AFB, NY 13441 Autovon: 587-2951 Commercial: (315)330-2951
Date	9 April 1979
Total Pages	Handbook sections are periodically updated under contract

K. Military Specifications.

1. MIL-STD-781. MIL-STD-781 covers the requirements for reliability qualification tests (preproduction) and reliability acceptance tests (production) for equipment that experiences a distribution of times-to-failure that is exponential. These requirements include: test conditions, procedures, and various fixed length and sequential test plans with respective accept/reject criteria.

The application of this standard is intended to provide the procuring activity with decision information prior to award of a production contract, based on realistic test and evaluation of equipment performance and reliability, under severe environmental conditions. It is also intended that the standard provide guidelines for determining test conditions which should apply to production reliability acceptance testing. These tests should be accomplished under one of the following locations and conditions, selected from the listed order of priority and authorized by the procuring activity:

a) Test in government or commercial laboratory independent of the developing/producing contractor

b) Have prime contractor test subcontractor's products under government surveillance

c) Allow contractor to conduct these tests in his own facilities, under strict government surveillance, where such an arrangement is shown to be in the best interests of the government

Furthermore, it is the intent of this standard that both performance and reliability be assessed in a test program of statistically valid length under combined, cyclic, and time-varying environmental conditions which simulate those expected in service use.

This standard may be applied on a program requiring only the development of equipment where the final development model is to be used for reliability design qualification. However, this standard is not applicable to reliability growth testing. This standard may be applied on a pure production contract where the reliability design has already been qualified.

This standard is applicable to six broad categories of equipment, distinguished according to their field service applications.

a) Category 1 - Fixed Ground Equipment
b) Category 2 - Mobile Ground Vehicle Equipment
c) Category 3 - Shipboard Equipment
   - Sheltered
   - Unsheltered
d) Category 4 - Equipment for Jet Aircraft
e) Category 5 - Equipment for Turbo-prop and Helicopter
f) Category 6 - Air Launched Weapons and Assembled External Stores

The military standard also includes a number of useful appendices which are listed below with a brief description of their purpose :

- Appendix A - Reliability Program Overview and the Role of Reliability Testing

This appendix describes briefly a reliability program of the type desired by the implementation of MIL-STD-781, applicable to development and production, including the necessary environmental considerations and providing the program relationships to reliability qualification and acceptance testing.

- Appendix B - Reliability Qualification and Acceptance Test Conditions

This appendix discusses the test conditions for reliability qualification and acceptance tests, including the analyses necessary to establish conditions appropriate to the particular system or equipment.

- Appendix C - Statistical Test Plans

This appendix covers the statistical test plans and the selection and use of these plans. Operational characteristic curves are given for Probability Ratio Sequential Test (PRST), fixed length and all equipments tests. Also expected test time curves are presented for the PRST plans.

- Appendix D - Reliability Test Procedures

The purpose of reliability qualification and acceptance test procedures is to assure that adequate planning has been accomplished prior to commencement of testing and to provide a document that reflects an understanding or agreement between the government and the contracting activity as to what the intent of the tests are, what the procedural rules shall be, and what the criteria for acceptance shall be.

- Appendix E - Test Instruments and Facilities

The purpose of this appendix is to assure that adequate planning is accomplished and that appropriate and sufficient equipment and facilities have been provided, with necessary certifications and calibrations, acceptable to the procuring activity, prior to the commencement of reliability qualification and production acceptance tests.

- Appendix F - Notes on Data Requirements

Data requirements should be placed on contract only when review of the data by the procuring activity at the contractor's facility is not cost effective. When data requirements are included in the DD Form 1423, Contract Data Requirements List, the contractor's format should be used unless there are considerable cost savings to the procuring activity through the use of a specified format.

2. MIL-STD-202. MIL-STD-202 establishes uniform methods for testing electronic and electrical component parts, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military operations, and physical and electrical tests. This standard covers almost all components other than semiconductors, such as capacitors resistors, switches, relays, transformers and jacks. The standard is intended to apply only to small parts, such as transformers and inductors, weighing up to 300 pounds or having a root-mean-square test voltage up to 50,000 volts unless otherwise specifically invoked. A numerical index of test methods is supplied for easy reference on the following page.

Method Number	Date	Title
		Environmental Tests (100 Class)
101D	16 April 1973	Salt spray (corrosion)
102A	Cancel effective 31 December 1973 (See note on method 102.)	
103B	12 September 1963	Humidity (steady state)
104A	24 October 1956	Immersion
105C	12 September 1963	Barometric pressure (reduced)
106D	16 April 1973	Moisture resistance
107D	16 April 1973	Thermal shock
108A	12 September 1963	Life (at elevated ambient temperature)
109B	16 April 1973	Explosion
110A	16 April 1973	Sand and dust
111A	16 April 1973	Flammability (external flame)
112B	16 April 1973	Seal
		Physical-characteristics tests (200 Class)
201A	24 October 1956	Vibration
202D	16 April 1973	Shock (specimens weighing not more than 4 pounds) (Superseded by method 213.)
203B	16 April 1973	Random drop
204C	16 April 1973	Vibration, high frequency
205E	16 April 1973	Shock, medium impact (Superseded by method 213)
206	12 September 1963	Life (rotational)
207A	12 September 1963	High-impact shock
208C	16 April 1973	Solderability
209	18 May 1962	Radiographic inspection
210A	16 April 1973	Resistance to soldering heat
211A	14 April 1969	Terminal strength
212A	16 April 1973	Acceleration
213B	16 April 1973	Random vibration
215	9 November 1966	Resistance to solvents
216	Cancel effective 16 April 1973 . (See not on method 216)	
		Electrical-characteristics tests (300 Class)
301	6 February 1956	Dielectric withstanding voltage
302	6 February 1956	Insulation resistance
303	6 February 1956	DC resistance
304	24 October 1956	Resistance-temperature characteristic
305	24 October 1956	Capacitance
306	24 October 1956	Quality factor (Q)
307	24 October 1956	Contact resistance
308	29 November 1961	Current-noise test for fixed resistors
309	27 May 1965	Voltage coefficient of resistance determination procedure
310	20 January 1967	Contact-chatter monitoring
311	14 April 1969	Life, low level switching
312	16 April 1973	Intermediate current switching

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officers.)

3. MIL-STD-701. MIL-STD-701 establishes the requirements for the selection of semiconductor devices used in the design and manufacture of military equipment. It provides a standard parts list for semiconductor devices by functional use, such as silicon voltage reference diodes shown in the sample table below. The table provides device part number, reference voltage range, voltage temperature stability, dynamic impedance, maximum temperature, JEDEC outline, and the corresponding MIL-S-19500 specification slash number.

TABLE I.

SILICON VOLTAGE REFERENCE DIODES (listed in order of voltage range)

Device type no.	Reference voltage range		Voltage temp Stability	Dynamic impedance		Max temp	JEDEC outline 1/	Specification MIL-S-19500/
	$V_{(BR)}$ Min (V)	$V_{(BR)}$ Max (V)	$\Delta V_{(BR)}$ (V)	Z (ohms)	@I_Z (mA)	(°C)		
1N821	5.90	6.50	0.096	15	7.5	175	DO7	159
1N823	↕	↕	0.048	↕	↕	↕	↕	↕
1N825			0.019					
1N827			0.009					
1N829	5.90	6.50	0.005	15	7.5	175	DO7	159
1N4565A	6.08	6.72	0.100	200	0.5	175	DO7	452
1N4566A	↕	↕	0.050	↕	↕	↕	↕	↕
1N4567A			0.020					
1N4568A			0.010					
1N4569A			0.005	200	0.5			
1N4570A			0.100	100	1.0			
1N4571A			0.050	↕	↕			
1N4572A			0.020					
1N4573A			0.010					
1N4574A	6.08	6.72	0.005	100	1.0	175	DO7	452
1N3154	8.00	8.80	0.130	15	10.0	175	DO7	158
1N3155	↕	↕	0.065	↕	↕	↕	↕	↕
1N3156			0.026					
1N3157	8.00	8.80	0.013	15	10.0	175	DO7	158
1N935B	8.55	9.45	0.184	20	7.5	175	DO7	156
1N937B	↕	↕	0.037	↕	↕	↕	↕	↕
1N938B			0.018					
1N939B	8.55	9.45	0.009	20	7.5	175	DO7	156
1N941B	11.12	12.28	0.239	30	7.5	175	DO7	157
1N943B	↕	↕	0.047	↕	↕	↕	↕	↕
1N944B			0.024					
1N945B	11.12	12.28	0.012	30	7.5	175	DO7	157

1/ Mechanical configurations of devices are equal or similar to referenced JEDEC outlines.

4. MIL-STD-750. This military standard establishes uniform methods for testing semiconductor devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military operations, and physical and electrical tests. The standard uses the term "devices" in a way that includes such items as transistors, diodes, voltage regulators, rectifiers thyristors and tunnel diodes.

The document provides test methods for environmental, mechanical, electrical characteristics, thermal resistance, low frequency tests, high frequency tests, field effect electrical tests, diodes, microwave diodes, thyristor and tunnel diodes.

As a ready reference for the failure analyst, a numerical index of the test methods is provided on the following pages.

Numerical Index of Test Methods

Method Number	Title
1001.1	Barometric pressure, (reduced)
1011	Immersion
1016	Insulation resistance
1021.1	Moisture resistance
1026.3	Steady-state operation life
*1027.1	Steady-state operation life (LTPD)
1031.4	High-temperature life (nonoperating)
*1032.1	High-temperature (nonoperating) life (LTPD)
1036.3	Intermittent operation life
1037	Intermittent operation life (LTPD)
*1038	Burn-in (for diodes and rectifiers)
*1039	Burn-in(for transistors)
1041.1	Salt Atmoshpere (corrosion)
*1046.2	Salt spray (corrosion)
1051.1	Thermal shock (temperature cycling)
1056.1	Thermal shock (glass strain)
1061.1	Temperature measurement, case and stud
1066.1	Dew point
1071	Seal
	Mechanical Characteristics Tests (2000 Class)
2006	Constant acceleration
2016.2	Shock
2026.2	Solderablility
2031.1	Soldering heat
2036.3	Terminal strength
2046.1	Vibration fatique
2051.1	Vibration noise
2056	Vibration, variable frequency
2057.1	Vibration, variable frequency (monitored)
2066	Physical dimensions
2071	Visual and mechanical examination
2076	Radiographic inspection
	Electrical-characteristics Tests (for transistors) (3000 series)
	General
3001.1	Breakdown voltage, collector to base
3005.1	Burnout by pulsing
3011.1	Breakdown voltage, collector to emitter
3015	Drift
3020	Floating potential
3026.1	Breakdown voltage, emitter to base
3030	Collector to emitter voltage
3036.1	Collector to base cutoff current
3041.1	Collector to emitter current
3051	Safe operating area (continuous dc)
3052	Safe operating area (pulsed)
3053	Safe operating area (switching)
3061.1	Emitter to base cutoff current
3066.1	Base emitter voltage (saturated or nonsaturated)
3071	Saturation voltage and resistance
3076.1	Forward-current transfer ratio
3086.1	Static input resistance
3092.1	Static transconductance

Method Number	
	Circuit Performance and Thermal Resistance Measurements (3100 series)
3126	Thermal resistance (collector-cutoff-current method)
3131	Thermal resistance(forward voltage drop, emitter to base, didoe method)
3132	Thermal resistance (DC forwardd voltage drop, emitter base, continuous methods)
3136	Thermal resistance (forward voltage drop, collector base, diode method)
3141	Thermal response time
3146.1	Thermal time constant
3151	Thermal reisitance, general
	Low-frequency Tests (3200 series)
3201.1	Small-signal short-circuit input impedance
3206.1	Small-signal short-signal forward-current transfer ratio
3211	Small-signal open-circuit reverse-voltage transfer ratio
3216	Small-signal open-circuit output admittance
3221	Small-signal short-circuit input admittance
3231	Small-signal short-circuit output admittance
3236	Open circuit output capacitance
3240.1	Input capacitance (Output open-circuited or short-circuited)
3241	Direct Interterminal capacitance
3246.1	Noise figure
3251.1	Pulse response
3255	Large-signal power gain
3256	Small-signal power gain
3261.1	Extrapolated unity gain frequency
3266	Real part of small-signal short-circuit input impedance
	High Frequency Tests (3300 series)
3301	Small-signal short-circuit forward-current transfer-ratio cutoff frequency
3306.2	Small-signal short-circuit forward-current transfer ratio
331	Maximum frequency of oscillation
	Field-effect Transistor Electrical Tests (3400 series)
3401	Breakdown voltage, gate to source
3403	Gate to source voltage or current
3405	Drain to source "on"-state voltage
3407	Breakdown voltage, drain to source
3411	Gate reverse current
3413	Drain current
3415	Drain reverse current
3421	Static drain to source "on"-state resistance
3423	Small-signal drain to source "on"-state resistance
3431	Small-signal, common source, short-circuit, input capacitance
3433	Small-signal, common source, short-circuit, reverse-transfer capacitance
3453	Small-signal, common-source, short-circuit, output admittance
3455	Small-signal, common source, short-circuit, forward transadmittance
	Electrical-characteristics Tests (for diodes)(4000 series)
	General
4001	Capacitance
4011.3	Forward voltage
4016.2	Reverse current and reverse voltage
4021.2	Breakdown voltage (diodes)
4022	Breakdown voltage (voltage regulators and voltage reference diodes)
4026.1	Forward recovery time
4031	Reverse recovery time
4036	"Q" for variable capacitance diodes
4041.1	Rectification efficiency
4046.1	Reverse current, average

Method Number	General (cont'd)
4051.2	Small-signal breakdown impedance
4056.1	Small-signal forward impedance
4061.1	Stored charge
4066.2	Surge current
4071	Temperature coefficient of breakdown voltage
4076.1	Saturation current
4081	Thermal resistance for signal diodes, rectifier diodes, and controlled rectifiers
	Microwave Diodes (4100 series)
4101.2	Conversion loss
4106	Detector power efficiency
4111	Figure of merit
4116	Intermediate frequency impedance
4121.1	Output noise ratio
4126.1	Overall average noise figure and IF amplifier noise figure
4131	Video impedance
4136	Voltage standing wave ratio
4141	Burnout by repetitive pulsing
4146	Burnout by single pulse
4151	Rectified microwave diode current
	Thyristor(controlled rectifiers)(4200 series)
4201.2	Holding current
4206.1	Forward blocking current
4211.1	Reverse blocking current
4216	Pulse response
4219	Reverse gate current
4221.1	Gate-trigger voltage or gate-trigger current
4223	Gate-controlled turn-on time
4224	Circuit-commutated turn-off time
4225	Gate-controlled turn-off time
4226.1	Forward "on" voltage
4231.2	Exponential rate of voltage rise
	Tunnel Diodes (4300 series)
4301	Junction capacitance
4306.1	Static characteristics of tunnel diodes
4316	Series inductance
4321	Negative resistance
4326	Series resistance
4331	Switching time

5. MIL-STD-883. MIL-STD-883 is the military standard document outlining test methods and procedures for evaluating microelectronic devices and packages. The latest revision is MIL-STD-883B which is dated 31 August 1977. Revisions are issued as "Notices" during the time the particular issue is current. MIL-STD-883B currently has one notice, Notice 1 dated 21 July 1978. The document covers the test methods for environmental, mechanical and electrical (digital and linear). A listing of the test method numbers and test titles are given for ready reference on the following pages.

A detailed discussion is provided on a number of critical quality assurance procedures with which the failure analyst should be familiar. The principal areas covered are:

a) 5001 - Parameter Mean Value Control
b) 5002 - Parameter Distribution Control
c) 5003 - Failure Analysis Procedures for Microcircuits
d) 5004.4 - Screening Procedures
e) 5005.4 - Qualification and Quality Conformance Procedures
f) 5006 - Limit Testing
g) 5007.1 - Wafer Lot Acceptance
h) 5008 - Test Procedures for Hybrid and Multichip Microcircuits

TEST METHODS

Method Number	
	Environmental Tests
1001	Barometric pressure
1002	Immersion
1003	Insulation resistance
1004.2	Moisture resistance
1005.2	Steady state life
1006	Intermittent life
1007	Agree life
1008.1	High-temperature storage
1009.2	Salt atmosphere (corrosion)
1010.2	Temperature cycling
1011.2	Thermal shock
1012	Thermal characteristics
1013	Dew point
1014.2	Seal
1015.2	Burn-in test
1016	Life/reliability characterization tests
1017	Neutron irradiation
1018	Internal water vapor content
	Mechanical Tests
2001.2	Constant acceleration
2002.2	Mechanical shock
2003.2	Solderability
2004.2	Lead integrity
2005.1	Vibration fatigue
2006.1	Vibration noise
2007.1	Vibration, variable frequency
2008.1	Visual and mechanical
2009.1	External visual
2010.3	Internal visual (monolithic)
2011.2	Bond strength
2012.2	Radiography
2013	Internal visual
2014	Internal visual and mechanical
2015.1	Resistance to solvents
2016	Physical dimensions
2017.1	Internal visual (hybrid)
2018	Scanning electron microscope (SEM) inspection of metallization
2019.1	Die shear strength
2020	Particle impact noise detection test
2021	Glassivation layer integrity
2022	Meniscograph solderability
	Electrical Tests (Digital)
3001.1	Drive source, dynamic
3002.1	Load conditions
3003.1	Delay measurements
3004.1	Transition time measurements
3005.1	Power supply current
3006.1	High level output voltage
3007.1	Low level output voltage
3008.1	Breakdown voltage, input or output
3009.1	Input current, low level
3010.1	Input current, high level
3011.1	Output short circuit current
3012.1	Terminal capacitance
3013.1	Noise margin measurements for digital microelectronic devices
3014	Functional testing

TEST METHODS - Continued

Method Number	Electrical Tests (Linear)
4001	Input offset voltage and current and bias current
4002	Phase margin and slew rate measurements
4003	Common mode input voltage range Common mode rejection ratio Supply voltage rejection ratio
4004	Open loop performance
4005	Output performance
4006	Power gain and noise figure
4007	Automatic gain control range
	Test Procedures
5001	Parameter mean value control
5002	Parameter distribution control
5003	Failure analysis procedures for microcircuits
5004.4	Screening procedures
5005.4	Qualification and quality conformance procedures
5006	Limit testing
5007.1	Wafer lot acceptance
5008	Test procedures for hybrid and multichip microcircuits

6. MIL-STD-1562. MIL-STD-1562 is a military standard providing a list of standard microcircuits for use in military electronic systems. The document has the microcircuits grouped under functional headings in tabular form, such as:

a) TTL Shift Registers
b) TTL Decoders
c) TTL Counters
d) CMOS Flip Flops
e) CMOS NOR Gates
f) Bipolar Voltage Regulators

Table headings consist of the commercial or generic number, MIL-M-38510 slash sheet number, device type and a brief circuit description. Table I is a sample page from MIL-STD-1562A dated 11 January 1978.

Table II TTL SHIFT REGISTERS

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description
5495	9	01	4-bit, right shift, left shift
54LS95	306	03	4-bit, parallel-access
5496	9	02	5-bit
54LS96	306	04	5-bit
54164	9	03	8-bit, parallel-out, serial
54LS164	306	05	8-bit, parallel-out
54165	9	04	8-bit, parallel-load
54194	9	05	4-bit, bidirectional
54LS194	306	01	4-bit, bidirectional
54S194	76	01	4-bit, bidirectional
54195	9	06	4-bit, parallel access
54LS195	306	02	4-bit, parallel access
54S195	76	02	4-bit, parallel access
54LS295	306	06	4-bit, right shift, left shift register, 3-state outputs
54LS395	306	07	4-bit, cascadable shift register, 3-state outputs
9300	159	01	4-bit
9328	159	02	Dual, 8-bit

TABLE I-G. TTL Decoders

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description
5442	10	01	BCD to decimal
54LS42	307	03	BCD to decimal (low-power Schottky)
5443	10	02	Excess-3 to decimal
5444	10	03	Excess-3-gray-to-decimal
5445	10	04	BCD to decimal decoder/driver (open collector)
5446	10	06	BCD to 7 segment decoder/driver (open collector)
54LS47	307	04	BCD to 7 segment decoder/driver (open collector)(low-power Schottky)
5448	10	08	BCD to 7 segment decoder/driver
5449	10	09	BCD to 7 segment decoder/driver (open collector)
9317	158	02	7 segment decoder/driver
9321	158	01	1 of 4 decoder
54LS138	307	01	3 to 8 line decoder (low-power Schottky)
54LS139	307	02	Dual, 2 to 4 line decoder (low-power Schottky)
54145	10	05	BCD to decimal decoder/driver (30-volt, open collector output)

7. MIL-S-19500. This specification is entitled "General Specification for Semiconductor Devices" and covers the general requirements for semiconductor devices used in military equipment. Specific requirements for a particular type of semiconductor device are listed in the applicable device detail specification. This document provides the materials, marking and quality assurance requirements for semiconductor devices.

The document is best known for the appendixes which are very useful to the failure analyst.

a) Appendix A - Semiconductor Common Definitions
b) Appendix B - Abbreviations and Symbols
c) Appendix C - Statistical Sampling, Life Test, and Qualification Procedures

Appendix C provides LTPD sampling plans in table form for sample sizes 5 to 32,589 with corresponding acceptance number and the maximum percent defective LTPD. Table II illustrates the LTPD table used in MIL-S-19500 which is based upon the Poisson exponential binomial limit.

TABLE III

LTPD SAMPLING PLANS 1/ 2/

Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample).

Max. Percent Defective (LTPD) or λ	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
Acceptance Number (c) (r = c + 1)	Minimum Sample Sizes (For device-hours required for life test, multiply by 1000)																
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
4	16 (12.3)	27 (7.3)	39 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)	5327 (0.037)	7994 (0.025)
5	19 (13.8)	31 (8.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)	7019 (0.047)	10533 (0.031)
7	24 (16.6)	39 (10.2)	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)	832 (0.83)	1109 (0.62)	1664 (0.42)	2378 (0.29)	3325 (0.22)	5546 (0.12)	8319 (0.083)	11092 (0.062)	16638 (0.042)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)	890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.3)	3562 (0.22)	5936 (0.13)	8904 (0.086)	11872 (0.065)	17808 (0.043)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)	948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	403 (2.3)	672 (1.4)	1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)	1066 (0.94)	1422 (0.71)	2133 (0.47)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)	1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.240)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)	1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.344)	4728 (0.246)	7880 (0 148)	11819 (0.098)	15759 (0.074)	23639 (0.049)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (2.51)	826 (1.51)	1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8260 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)	1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	9638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)	1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5411 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27051 (0.052)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1086 (1.61)	1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6519 (0.269)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

1/ Sample sizes are based upon the Poisson exponential binomial limit.

2/ The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.

8. MIL-M-38510. This specification establishes the general requirements for monolithic, multichip, and hybrid microcircuits and the quality and reliability assurance requirements which must be met in the procurement of microcircuits. Detail requirements, specific electrical characteristics of microcircuits, such as electrical tests and sequence, and all other provisions which are sensitive to the particular use intended will be specified in the applicable slash sheets to MIL-M-38510, e.g., MIL-M-38510/XXX.

Multiple levels of product assurance requirements and control for monolithic and multichip microcircuits and a single level for hybrid microcircuits are provided for in this specification.

A number of critical quality assurance parameters and factors are defined with which the failure analyst should be familiar; these are:

a) Production Lot
b) Inspection Lot
c) Wafer Lot
d) Final Seal

A detailed discussion is given on qualification requirements for the various classes of microcircuits. It identifies those processing and manufacturing changes which constitute a change of a qualified product.

A section is provided on the general design and construction requirements for microcircuits including these characteristics:

a) Package Materials
b) Internal Moisture Levels
c) External Metal Surfaces
d) Die Topography
e) Die Intraconnection Pattern

f) Die to Terminal Interconnection

g) Internal Conductors

h) Internal Lead Wires

i) Glassivation

j) Marking of Microcircuits

Other areas covered are the definitions for inspection lot identification code and workmanship guidelines for rework and the rebonding of monolithic devices.

This document incorporates the information that previously was in MIL-STD-1313A, dated 8 December 1967 and MIL-STD-1331.

9. RADC Failure Analysis Documents. A series of six RADC Technical Memoranda entitled: "RADC In-Depth Failure Analysis Quick Reaction (QR) Reliability System Support Accomplishments", covering RADC failure analysis efforts involving microelectronic devices in direct support of Air Force electronic systems are listed below for reference. The reports are published periodically by RADC for dissemination of pertinent part reliability data on Air Force Systems and are available on a limited basis to authorized Department of Defense agencies only. Requests for any of these documents must be referred to Mr. Ed Doyle Jr., RADC/RBRP, Griffiss AFB, NY 13441. AV: 587-2735 or Commercial (315) 330-2735.

a) RADC-EEN-TM-70-1
"RADC In-Depth Failure Analysis Quick Reaction Capability (QRC) Reliability System Support Accomplishments" (January 1967- January 1970)
Edgar A. Doyle Jr. et al.

b) RADC-RC-TM-71-2
"RADC In-Depth Failure Analysis (QRC) Reliability System Support Accomplishments" (January 1970-January 1971)
Edgar A. Doyle Jr. et al.

c) RADC-TM-RC-72-3
"RADC In-Depth Failure Analysis (QR) Reliability System Support Accomplishments" (January 1971-January 1972)
Edgar A. Doyle Jr. et al.

d) RADC-TM-RB-73-8 (Two Volumes)
"RADC In-Depth Failure Analysis (QR) Reliability System Support Accomplishments" (January 1972-September 1973)
Edgar A. Doyle Jr. et al.

e) RADC-TM-76-13 (Two Volumes)
"RADC In-Depth Failure Analysis Quick Reaction Capability (QR) Reliability System Support Accomplishments" (September 1973-July 1976)
Edgar A. Doyle Jr. et al.

f) RADC-TM-79-4
"RADC In-Depth Failure Analysis Quick Reaction (QR) Reliability System Support Accomplishments" (July 1976-July 1979)
Edgar A. Doyle Jr. et al.

10. D.A.T.A. BOOKS (Reference Standards for Industry). D.A.T.A. Books on electronic devices are available from D.A.T.A., Inc., A Cordura Company, P.O. Box 26875, San Diego, CA 92126 which are useful to the failure analyst. The following is a list of current publications covering semiconductor technology devices:

a) Transistors
b) Diodes
c) Thyristors
d) Digital ICs
e) Interface ICs
f) Memory ICs
g) Linear ICs
h) Microcomputers
i) Power Semiconductors
j) Microwave Devices

These reference books are published and updated semi-annually and provide a complete listing of commercially marketed semiconductor device types including specifications, nominal electrical parameters, etc., which supplement available manufacturers' product catalogues. Publications also available are several D.A.T.A. Books covering discontinued device types.

SECTION III

FAILURE ANALYSIS TECHNIQUES

A.

FAILURE VERIFICATION AND FAULT ISOLATION TECHNIQUES

III. FAILURE ANALYSIS TECHNIQUES

A. Failure Verification and Fault Isolation Techniques.

1. Introduction. Failure verification is perhaps the most important step the failure analyst is called upon to perform. Reported failures are often due to something totally independent of the microelectronic device.

Laboratories that perform analyses on field failures typically report that as many as 30% of reported failures cannot be verified. Some of the ways in which this situation can come about are:

a) Contact resistance at socket pins can cause failure.
b) Incorrect device insertion (common problem with DIP packages).
c) Wrong device used, for example, PNP for NPN transistor.
d) Improper application of the device. For instance, a high gain linear integrated circuit may oscillate if used in an application which calls for a low gain device. Also, a device may have been used outside its specification range, such as improper power supply voltage, inadequate drive current, etc.

In general, there is an order which should be followed in verifying a failure. Some of the steps to be followed are:

a) Initial external examination of package
b) Bench top testing

- o Pin-to-pin tests with curve tracer
- o Curve tracer tests (diodes and transistors)
- o Commercially available logic test equipment (See EQUIPMENT Section)

- Commercially available linear test equipment (See EQUIPMENT Section)
- Breadboard test setups with oscilloscope, frequency generator, power supplies, DVM, etc.

c) Automatic test equipment evaluation
d) High-low temperature tests for temperature sensitivity
e) Tests for intermittent failure
f) Fault isolation

With the exception of step (a), there is no hard and fast rule about the order of these steps. For instance, if automatic test equipment, the appropriate test instructions, the appropriate test fixture, etc., are readily available, it may be desirable to do a quick test with this equipment before proceeding to pin-to-pin tests.

Obviously, not all these steps would be appropriate for every type of microelectronic device. For example, automatic test equipment would not normally be used to verify failures of discrete diodes and transistors. Pin-to-pin evaluation of a complex memory is unlikely to detect failures internal to the memory. Also, all failures will not be intermittent in nature.

2. Initial External Examination. This step is intended to be nondestructive. Particular care should be used in handling the device. Information that could be vital in determining the cause of a failure might be lost if the device is mishandled. For example, the failure might be due to a strand of wire adhering to the device surface shorting two or more pins together. Special care must be used with high impedance devices such as MOS, linear, low power Schottky TTL, etc., because of the danger of electrical overstress (electrostatic discharge). These devices should be stored and handled with the leads in a conductive foam or with a shorting clip. A grounding strap should be worn at any time when the device leads are not shorted.

All external markings such as part number, date code, and manufacturer should be recorded. Examination of the package exterior should proceed in sequential stages to include the naked eye, low power (1-30x) stereo zoom, and higher power microscopic examination if any anomaly is found. Notes should be taken regarding the package condition, and a photographic record of any significant condition should be kept. The following is a list of specific items for which the package should be checked during inspection:

a) Contamination, corrosion, stains, or attached foreign particles
b) Pin damage and condition of plating
c) Cracks in, and general integrity of, package, especially around leads
d) Condition of the lid seal
e) Evidence of package mismarking or remarking
f) Discoloration that might be due to electrical overstress
g) Possible inaccurate lead designation
h) General mechanical damage resulting from mishandling

3. Bench Top Testing. In verifying electrical failures, the failure analyst is faced with a major dilemma. This dilemma comes from the fact that the analyst must define failure. For example, a TTL bipolar NOR gate may switch properly and show the proper output voltage levels when the inputs are toggled, but it may require significantly higher input current than normal to produce the change. In this example, the TTL gate is "functional" in the sense that the truth table could be satisfied. On the other hand, the sample failed one set of "parametric" tests. That is, at one specific temperature, power supply voltage, current, etc., the unit failed because of high input current. By the same token, this sample may well pass all tests at, for instance, a lower power supply voltage or a different temperature.

Generally speaking, it is impossible to completely separate functional from parametric testing. This fact is particularly true of diodes, transistors, and linear integrated circuits. With logic circuits, as the example above shows, functionality might be said to have a different and separate meaning from parametric concerns.

The failure analyst must keep these facts in mind when attempting to verify failures. He must particularly keep in mind the fact that complete electrical testing requires a complex matrix involving many variables. As an example, consider Figure 1. Figure 1 gives the pin designation and electrical specifications for a 7402 TTL quadruple 2-input positive-NOR gates integrated circuit. The specifications for this relatively simple integrated circuit demonstrate the high degree of complexity in testing. To completely test this integrated circuit, it must be exercised through every possible combination of voltage, current, and temperature listed in the specification sheet.

a) Pin-to-Pin Electrical Evaluation. Conditions such as electrical shorts, low breakdown, excessive leakage, opens, etc., can all be detected during this test. An example of a typical data sheet for recording pin-to-pin electrical measurements is shown in Table I.

- Pretesting Procedure. The following steps should be accomplished and the precautions should be observed before beginning pin-to-pin tests:

  - Obtain manufacturer's specification sheet and circuit diagram for the device under test.

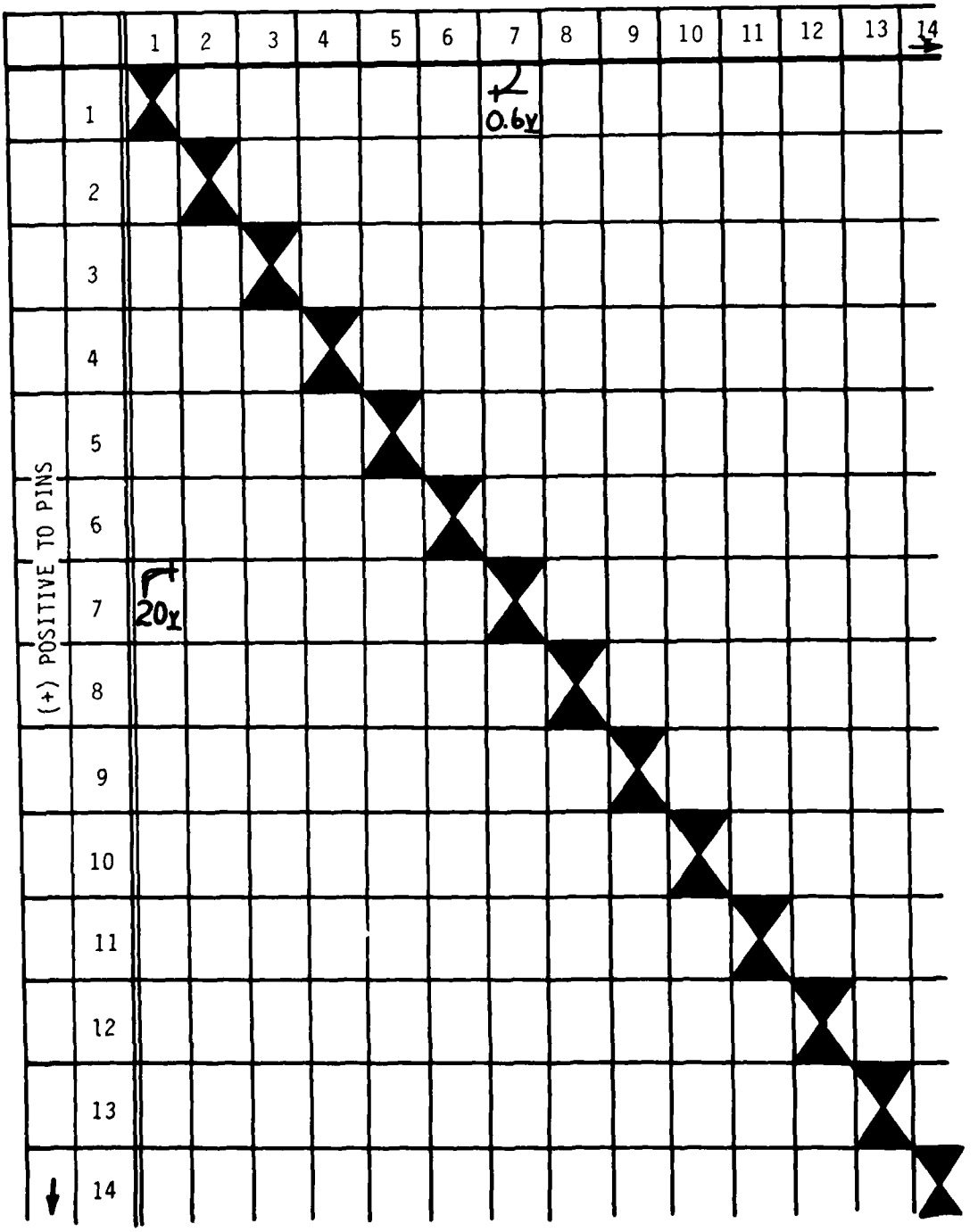
  - Obtain a known electrically good unit for purposes of comparison.

  - If high impedance devices are being handled, always wear a grounding strap. These devices should remain with the leads shorted together when not being handled.

TABLE I

TYPICAL DEVICE ELECTRICAL PIN-TO-PIN DATA SHEET

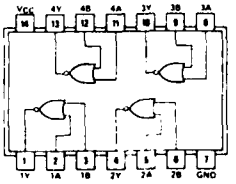
Device Type _____ (-) NEGATIVE TO PINS Date: _____



QUADRUPLE 2-INPUT POSITIVE-NOR GATES

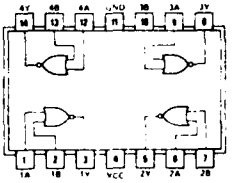
02

positive logic:
$Y = \overline{A+B}$



SN5402 (J)
SN54L02 (J)
SN54LS02 (J, W)
SN54S02 (J, W)

SN7402 (J, N)
SN74L02 (J, N)
SN74LS02 (J, N)
SN74S02 (J, N)



SN5402 (W)
SN54L02 (T)

a). Pin Designation

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '02 MIN	NOM	MAX	SERIES 54 / SERIES 74 '25, '27 MIN	NOM	MAX	SERIES 54L / SERIES 74L 'L02 MIN	NOM	MAX	SERIES 54LS / SERIES 74LS 'LS02, 'LS27 MIN	NOM	MAX	SERIES 54S / SERIES 74S 'S02, 'S260 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−800			−100			−400			−1000	μA
	74 Family			−400			−800			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			16			2			4			20	mA
	74 Family			16			16			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†			SERIES 54 / SERIES 74 '02, '25, '27 MIN	TYP‡	MAX	SERIES 54L / SERIES 74L 'L02 MIN	TYP‡	MAX	SERIES 54LS / SERIES 74LS 'LS02 'LS27 MIN	TYP‡	MAX	SERIES 54S / SERIES 74S 'S02, 'S260 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage		1, 2			54 Family			0.8			0.7			0.7			0.8	V
						74 Family			0.8			0.7			0.8			0.8	
V_{IK}	Input clamp voltage		3	V_{CC} = MIN, I_I = −18 mA					−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage		1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4		V
						74 Family	2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
						74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
					I_{OL} = 4 mA	Series 74LS								0.25	0.4				
I_I	Input current at maximum input voltage		4	V_{CC} = MAX		V_I = 5.5 V			1			0.1						1	mA
						V_I = 7 V									0.1				
I_{IH}	High-level input current	Data inputs	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			10							μA
		Strobe of '25							160										
		All inputs				V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	All inputs	5	V_{CC} = MAX		V_{IL} = 0.3 V						−0.18							mA
		Data inputs				V_{IL} = 0.4 V			−1.6						−0.4				
		Strobe of '25							−6.4										
		All inputs				V_{IL} = 0.5 V												−2	
I_{OS}	Short-circuit output current§		6	V_{CC} = MAX		54 Family	−20		−55	−3		−15	−20		−100	−40		−100	mA
						74 Family	−18		−55	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply current		7	V_{CC} = MAX			See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS' and SN54S/SN74S'.
¶Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of output short-circuit should not exceed one second.

b). Electrical Specifications

FIGURE 1. PIN DESIGNATION AND COMPLETE ELECTRICAL SPECIFICATIONS FOR A TTL 7402 NOR GATE INTEGRATED CIRCUIT

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'02	8	16	14	27	2.75
'25	8	16	10	19	2.25
'27	10	16	16	26	4.34
'L02	0.8	1.6	1.4	2.6	0.275
'LS02	1.6	3.2	2.8	5.4	0.55
'LS27	2.0	4	3.4	6.8	0.9
'S02	17	29	26	45	5.38
'S260	17	29	26	45	10.75

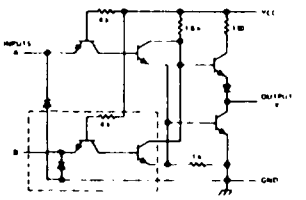
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'02	C_L = 15 pF, R_L = 400 Ω		12	15		8	15
'25			13	22		8	15
'27			10	15		7	11
'L02	C_L = 50 pF, R_L = 4 kΩ		31	60		35	60
'LS02, 'LS27	C_L = 15 pF, R_L = 2 kΩ		10	15		10	15
'S02	C_L = 15 pF, R_L = 280 Ω		3.5	5.5		3.5	5.5
	C_L = 50 pF, R_L = 280 Ω		5			5	
'S260	C_L = 15 pF, R_L = 280 Ω		4	5.5		4	6

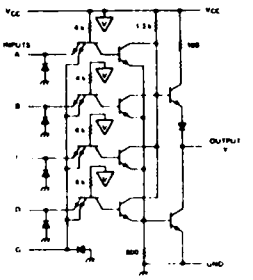
#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)



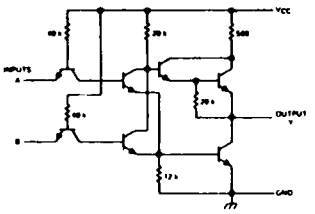
The portion of the schematic within the dashed lines is repeated for the C input of the '27

'02, '27 CIRCUITS



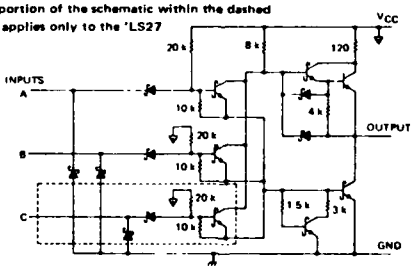
'25 CIRCUITS

Resistor values are nominal and in ohms

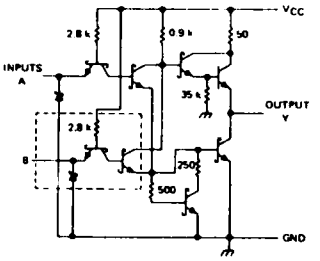


'L02 CIRCUITS

The portion of the schematic within the dashed lines applies only to the 'LS27



'LS02, 'LS27 CIRCUITS



The portion of the schematic within the dashed lines is repeated for each additional input of the 'S260, and the 0.9 kΩ resistor is changed to 0.6 kΩ.

'S02, 'S260 CIRCUITS

POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

b). Electrical Specifications (Cont'd)

FIGURE 1. PIN DESIGNATION AND COMPLETE ELECTRICAL SPECIFICATIONS FOR A TTL 7402 NOR GATE INTEGRATED CIRCUIT (CONT'D)

- Always disconnect the device under test when changing settings on the curve tracer. This is especially true of the POLARITY switch because transients of up to 60-70 volts can reach the device under test.

- The attachment of large clips, such as alligator clips, directly to package pins should be avoided because of the danger of electrical shorting and mechanical damage to leads. However, if necessary, miniature test clips can be used with proper care.

• Typical Results. Figures 2, 3, and 4 demonstrate some of the CRT displays that might be seen when performing pin-to-pin tests.

Note: The failure analyst must bear in mind that misleading breakdown and/or leakage measurements may result when some input or control pins are allowed to float at an arbitrary voltage level. Consider Figures 2h and 2i, for instance. The breakdown shown on the CRT display when only one input pin of a low power Schottky AND gate is unconnected reads higher (Figure 2h) than when both inputs are tied together (Figure 2i). Also, some MOS devices (such as analog switches) can give misleading breakdown voltages unless pins not being tested are tied to a specific voltage state, such as ground.

• Testing Procedure. Following is a description of procedures used in performing pin-to-pin testing with a 576 Tektronix curve tracer.

Note: Figure 5 shows an inexpensive but useful test fixture suitable for making pin-to-pin measurements on 40 pin DIP packages. Similar fixtures can be made for all types and sizes of packages at nominal costs.

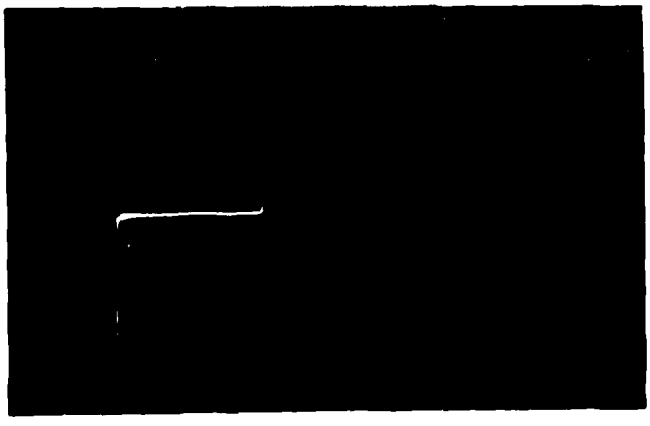


FIGURE 2a. TYPICAL TRANSISTOR BASE - EMITTER JUNCTION

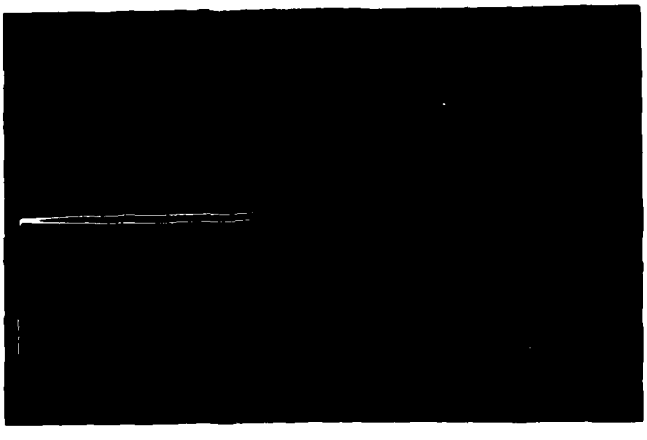


FIGURE 2b. TYPICAL TRANSISTOR BASE - COLLECTOR JUNCTION

FIGURE 2c. TYPICAL TRANSISTOR COLLECTOR - EMITTER JUNCTION

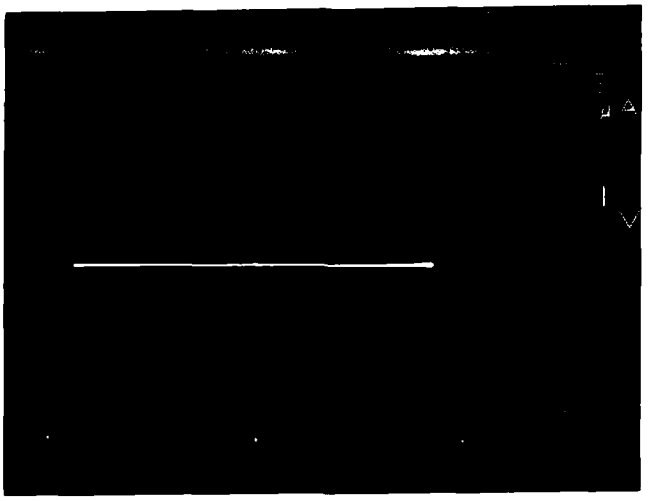


FIGURE 2d. TYPICAL MOS LINEAR OP AMP INPUTS TO GROUND JUST BEFORE BREAKDOWN OF INPUT PROTECTIVE DIODE

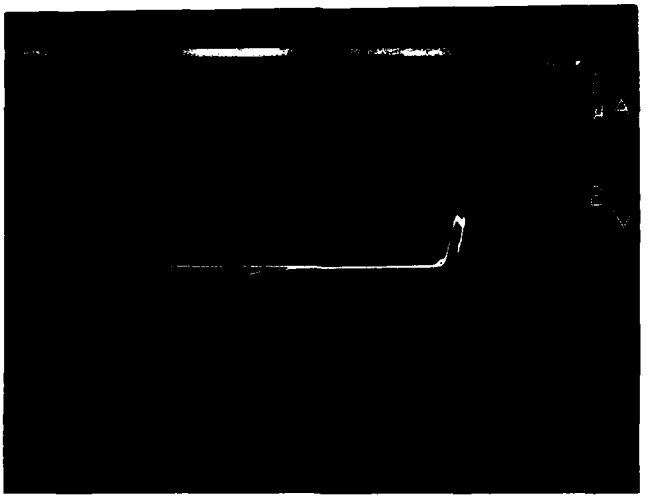


FIGURE 2e. TYPICAL MOS LINEAR OP AMP INPUTS TO GROUND AFTER BREAKDOWN OF INPUT PROTECTIVE DIODE

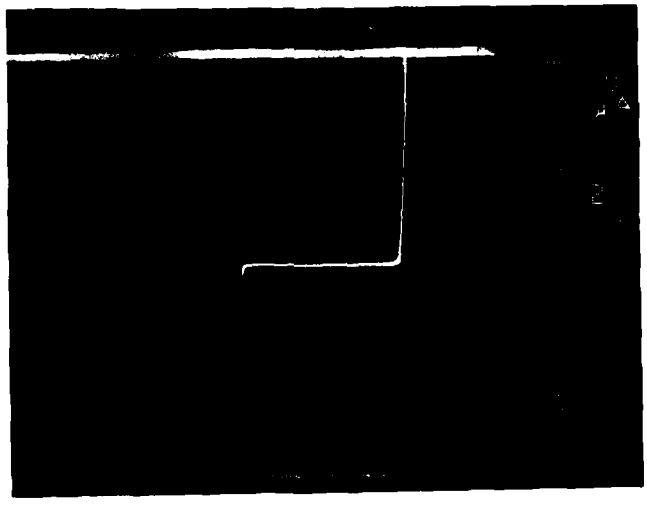


FIGURE 2f. TYPICAL BIPOLAR TTL AND GATE INPUTS TO GROUND

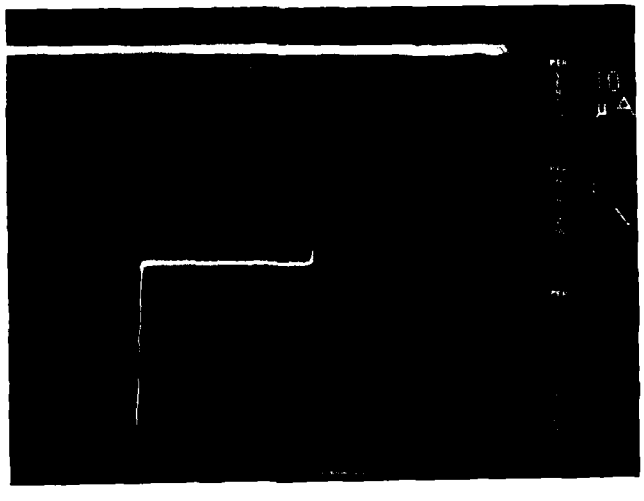


FIGURE 2g. TYPICAL BIPOLAR TTL AND GATE INPUTS TO V_{CC}

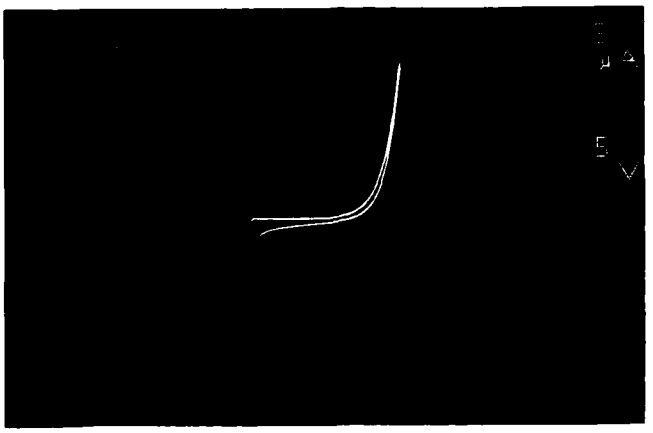


FIGURE 2h. TYPICAL BIPOLAR TTL LOW POWER SCHOTTKY AND GATE TO GROUND. ONLY ONE INPUT OF DUAL INPUTS CONNECTED.

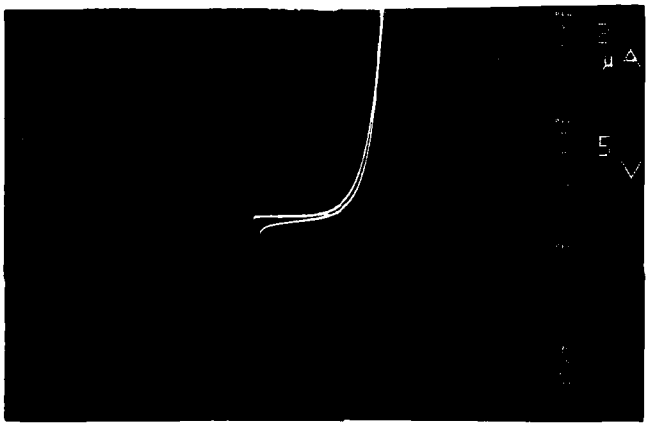


FIGURE 2i. TYPICAL BIPOLAR TTL LOW POWER SCHOTTKY AND GATE TO GROUND. ALL INPUTS ARE CONNECTED TOGETHER.

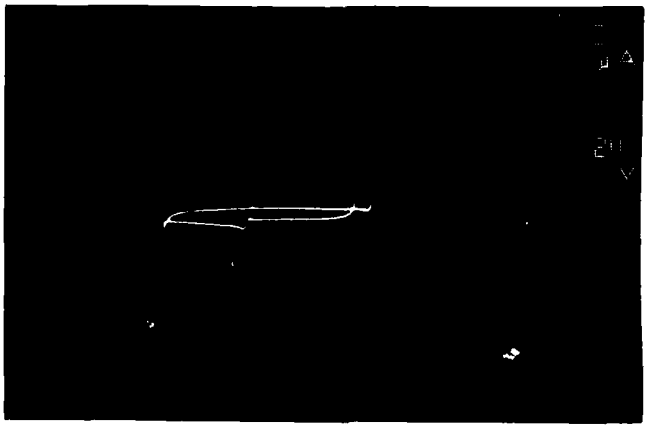


FIGURE 2j. TYPICAL BIPOLAR LINEAR OP AMP INPUT TO GROUND

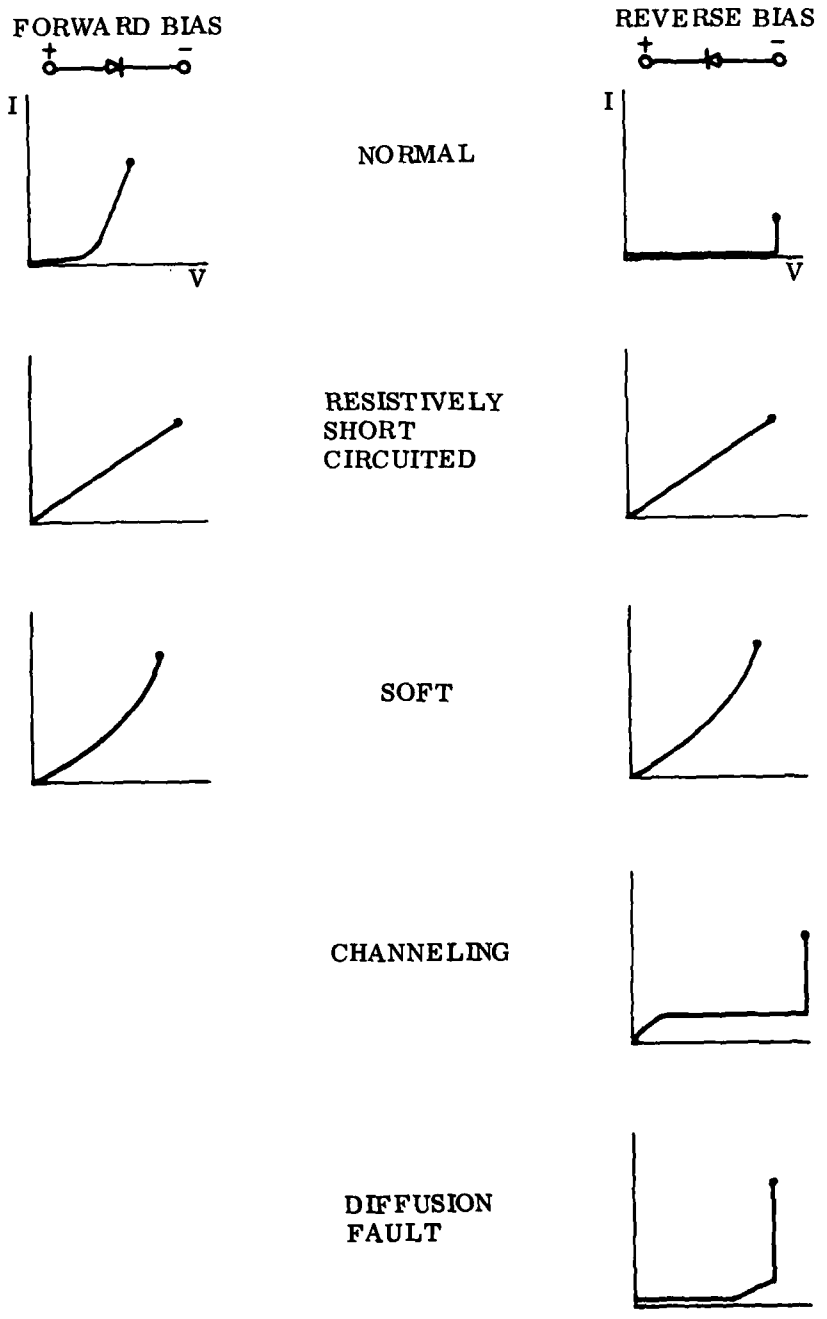


FIGURE 3. TYPICAL DIODE CURVE TRACER CRT DISPLAYS WHICH MIGHT BE SEEN DURING PIN-TO-PIN MEASUREMENTS.

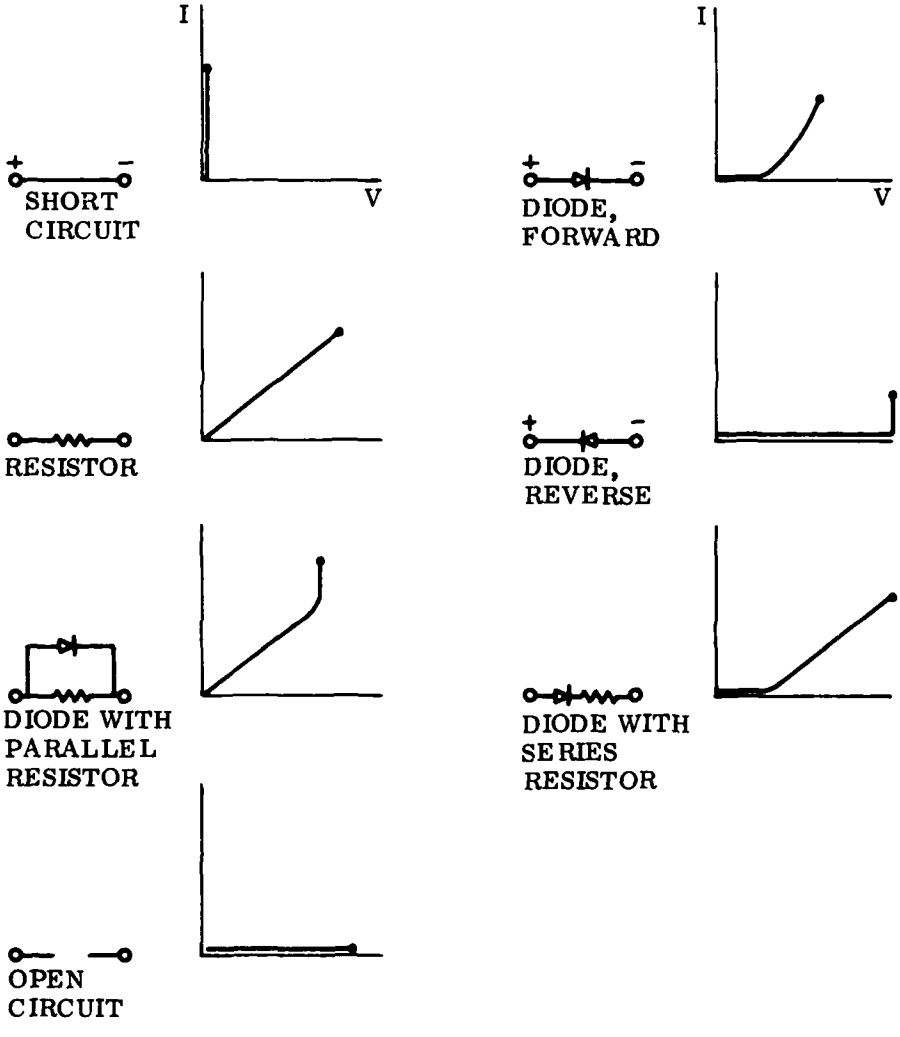
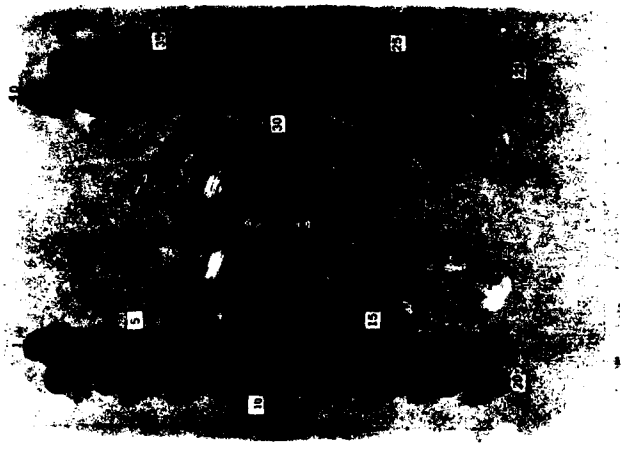
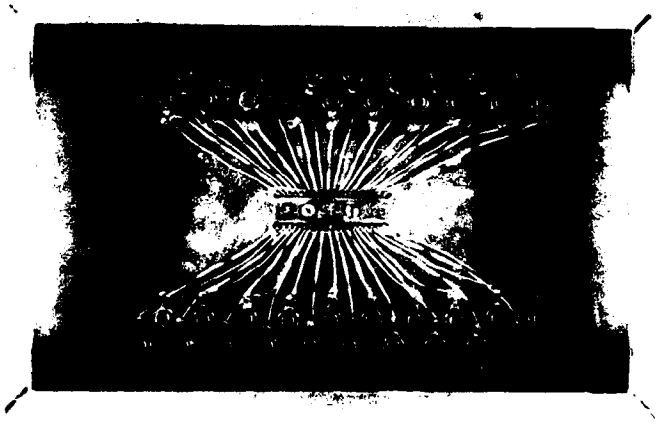


FIGURE 4. TYPICAL CURVE TRACER CRT DISPLAYS WHICH MIGHT BE SEEN DURING PIN-TO-PIN MEASUREMENTS.



a). TOP VIEW



b). BOTTOM VIEW

FIGURE 5. TEST FIXTURE FOR CURVE TRACER PIN-TO-PIN MEASUREMENTS OF A 40 PIN PACKAGE

- Verify that the LEFT-OFF-RIGHT switch connecting the curve tracer terminals to the unit under test is in the OFF position.

- Verify that the VARIABLE COLLECTOR SUPPLY is in the zero volts position.

- Place the MAX PEAK VOLTS switch into the lowest (15 volts) range and the SERIES RESISTORS switch into the highest (65k ohms) position.

- Place the POLARITY switch into the AC position. This will allow the failure analyst to observe both the forward and reverse current and voltage characteristics on the CRT.

Note: If an older curve tracer, Tektronix 575 for instance, is used, the POLARITY switch does not have the AC position. In this case, pin-to-pin measurements must be made twice - once with the POLARITY switch in the NPN position and once with the switch in the PNP position - in order to observe both forward and reverse directions.

- Insert the unit into a test fixture.

- Connect a wire from one (either LEFT or RIGHT) of the COLLECTOR terminals on the curve tracer to pin number 1 on the test fixture.

- Connect a wire from the corresponding side EMITTER terminal on the curve tracer to pin number 2 on the test fixture.

- Place the LEFT-OFF-RIGHT switch into either the LEFT or RIGHT position, depending on which side the COLLECTOR and EMITTER connections are being taken from.

- Slowly turn the VARIABLE COLLECTOR SUPPLY clockwise, applying voltage between the two pins.

- In this first series of measurements, the voltage and current should be limited to 10 volts and 10 microamps, respectively. Examination of the circuit diagram may indicate that a higher breakdown voltage should be applied between any two pins, and these measurements can be made after the initial 10 volt 10 microamp measurements.

Note: In the case where internal lead intermittency due to marginal contact is suspected, the initial voltage and current should be limited to 1 volt and 1 microamp, respectively. The voltage should be applied cautiously, beginning from zero volts, while the CRT display is monitored for intermittent continuity characteristics.

- The CRT display should be monitored for normal and for anomalous results. Any anomalous results should be documented by notes and photographs.

- Return the VARIABLE COLLECTOR SUPPLY to zero volts.

- Return the LEFT-OFF-RIGHT switch to the OFF position.

- Move the EMITTER terminal wire to pin 3 of the test fixture.

- Place the LEFT-OFF-RIGHT switch into the proper position.

- Apply voltage by advancing the VARIABLE COLLECTOR SUPPLY.

- Continue in this manner until all pins have been checked against pin number 1. Document any anomalous results.

- Verify that the applied voltage is returned to zero volts and that the test fixture has been isolated electrically from the curve tracer.

- Move the wire from the COLLECTOR terminal to pin number 2 position and the wire from the EMITTER terminal to pin number 3 position.

- Make the appropriate measurements and then sequentially advance the EMITTER terminal as previously described.

- Continue in this manner until all the pins, one at a time, have been measured against each other. Any suspicious or anomalous results should be documented.

b) Curve Tracer Measurements (Diodes and Transistors). A curve tracer is normally sufficient to measure the dc characteristics of diodes and transistors. Rise time, frequency response, etc., will require either more sophisticated equipment or breadboarded test circuits.

o Diodes. Figure 3 shows typical curve tracer displays that might be obtained when testing a single junction. Figure 6 shows typical dc specifications for a silicon switching diode. Techniques are available which can be used in conjunction with the curve tracer to to test dc characteristics at other than room temperatures. (See Tests for Intermittent Failures.)

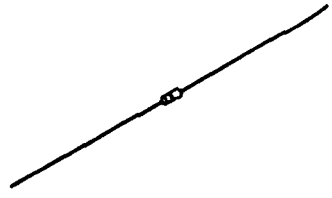
1N4829-30 SEE PAGE 266

Silicon Diodes

1N4863

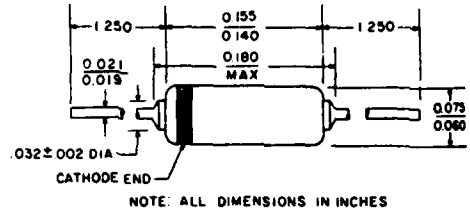
The General Electric 1N4863 Double Heatsink Diode is a high voltage, low capacitance diode for low- and high-current, high-speed switching circuits and general purpose applications. This diode incorporates an *oxide-passivated, planar structure built on a high resistivity*, epitaxial layer grown on a low resistivity silicon substrate. The 1N4863 offers controlled conductance, minimum and maximum forward voltage at four levels of forward current. This closely-controlled conductance is necessary for the design of clamping and logic circuits where tight tolerances on voltage levels are required.

All Double Heatsink Diodes receive a one-hour glass anneal bake at 425°C. This processing optimizes DHD hermetic integrity under temperature cycling and thermal shock conditions exceeding MIL-S-19 19500C requirements. All DHD's then receive a 300°C stabilization bake for 168 hours to assure parameter stability and reliability under maximum storage and operating junction temperature(s).



absolute maximum ratings:

	1N4863	
Voltage		
Reverse (Continuous)	50	volts
Current		
Average Rectified	200	ma
Recurrent Peak Forward	600	ma
Forward Steady-State DC	250	ma
Peak Forward Surge (1 μsec)	4	amps
Power		
Dissipation	500	mw
Temperature		
Operating	−65 to +200	°C
Storage	−65 to +200	°C
Lead, 1/16" ± 1/32" from case for 10 sec.	300	°C



NOTE: ALL DIMENSIONS IN INCHES

electrical characteristics: (25°C) (unless otherwise specified)

		1N4863 Min.	1N4863 Max.	
Forward Voltage				
(I_F = 0.1 ma)	V_F	440	550	mv
(I_F = 1.0 ma)	V_F	560	680	mv
(I_F = 10 ma)	V_F	690	820	mv
(I_F = 100 ma) (Note 1)	V_F	830	1200	mv
Breakdown Voltage				
(I_R = 5 μa)	B_V	70		v
(I_R = 100 μa)	B_V			
Reverse Current				
(V_R = 50 V)	I_R		50	na
(V_R = 50 V, T_A = +150°C)	I_R		50	μa
(V_R = 80 V)	I_R			na
(V_R = 80 V, T_A = +150°C)	I_F			μa

FIGURE 6. DC SPECIFICATIONS FOR TYPICAL SWITCHING DIODE

a Transistors. Figure 7 shows static dc parameters for a typical small signal silicon NPN transistor. Figure 8a). shows a curve tracer measurement of gain factor (β). Comparison of the data sheet and the curve tracer measurements shows:

SPEC. SHEET	CURVE TRACER
V_{CE} = 10 v	V_{CE} = 10 v
I_c = 1 ma	I_c = 1 ma
β = 50 min.	$\beta \simeq 200$

Figure 8b). shows the transistor family of V-I curves at breakdown. The curve tracer can be used to measure individual junctions in the transistor as well. Figures 2a, 2b, and 2c show typical V-I characteristics of the device junctions. As with the diode, the curve tracer can be used in conjunction with external forms of heating and cooling to monitor dc characteristics at other than room temperature (See Tests for Intermittent Failures).

c) Commercially Available Logic Test Equipment. Commercial equipment for bench top logic testing is available in the form of logic probes, clipon logic probes, and test systems. These range in complexity from the very simple to the very complex. The logic probes are little more than continuity checkers. A light on the probe indicates a high logic level, and low logic level corresponds to the light being off. These probes have little applicability in testing individual integrated circuits and find much more use when logic levels and signals are being traced on printed circuit boards.

Most logic circuits are highly specialized. Few bench top logic testers are available, at low price, with enough flexibility to test more than a few different logic functions. The Accutest circuit analyzer (see Equipment Section) is an example of one system available that is suitable for general failure analysis.

Silicon
Transistors

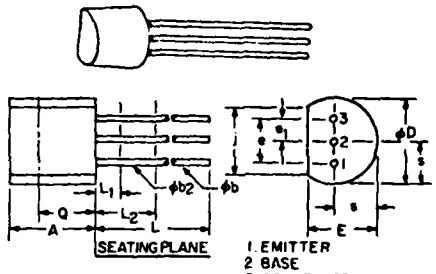
NPN

GES2221A,2A

The General Electric GES2221A and GES2222A units are silicon, NPN, planar passivated, epitaxial devices specifically developed for high speed switching, amplifier and core driver applications.

FEATURES:

- Performance comparable to hermetic units
- High gain
- Medium voltage
- Excellent switching speeds
- Low saturation voltages
- High frequency



1. EMITTER
2. BASE
3. COLLECTOR

TO-92

SYMBOL	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.	NOTES
A	4.320	5.330	.170	.210	
øb	.407	.550	.016	.022	1,3
øb2	.407	.482	.016	.019	3
øD	4.450	5.200	.175	.205	
E	3.180	4.190	.125	.165	
e	2.410	2.670	.095	.105	
e1	1.150	1.395	.045	.055	
J	3.430	4.320	.135	.170	
L	12.700	—	.500	—	1,3
L1	—	1.270	—	.050	3
L2	6.350	—	.250	—	3
Q	2.920	—	.115	—	2
s	2.030	2.670	.080	.105	

NOTES:
1. THREE LEADS
2. CONTOUR OF PACKAGE UNCONTROLLED OUTSIDE THIS SIDE.
3. (THREE LEADS) øb2 APPLIES BETWEEN L_1 AND L_2. øb APPLIES BETWEEN L_2 AND 12.70 MM (.500") FROM THE SEATING PLANE. DIAMETER IS UNCONTROLLED IN L_1 AND BEYOND 12.70 MM (.500") FROM SEATING PLANE.

absolute maximum ratings: ($T_A = 25°C$, unless otherwise specified)

		GES2221A GES2222A	
Voltages			
Collector to Emitter	V_{CEO}	40	Volts
Collector to Emitter	V_{CES}	40	Volts
Emitter to Base	V_{EBO}	5	Volts
Collector to Base	V_{CBO}	75	Volts
Current			
Collector	I_C	400	mA
Collector (peak, pulsed 10 μsec, ≦ 2% duty cycle)	I_C	800	mA
Dissipation			
Total Power ($T_C \leqq 25°C$)	P_T	1.0	Watts
Total Power ($T_A \leqq 25°C$)	P_T	0.360	Watts
Derate Factor ($T_C \geqq 25°C$)		10.0	mW/°C
Derate Factor ($T_A \geqq 25°C$)		3.6	mW/°C
Temperature			
Storage	T_{STG}	−65 to +150	°C
Operating	T_J	−65 to +125	°C
Lead ($\frac{1}{16}" \pm \frac{1}{32}"$ from case for 10 sec.)	T_L	+260	°C

electrical characteristics: ($T_A = 25°C$, unless otherwise specified)

STATIC CHARACTERISTICS	Symbol	GES2222A GES2221A Min.	Max.	
Collector-Emitter Breakdown Voltage				
($I_C = 10mA$, $I_B = 0$)	$V_{(BR)CEO}$*	40	—	Volts
Emitter-Base Breakdown Voltage				
($I_E = 10\mu A$, $I_C = 0$)	$V_{(BR)EBO}$	5	—	Volts
Collector-Base Breakdown Voltage				
($I_C = 10\mu A$, $I_E = 0$)	$V_{(BR)CBO}$	75	—	Volts
Collector-Emitter Breakdown Voltage				
($I_C = 10\mu A$, $V_{BE} = 0$)	$V_{(BR)CES}$	40	—	Volts
Collector-Emitter Saturation Voltage				
($I_C = 150mA$, $I_B = 15mA$)	$V_{CE(SAT)}$*	—	0.3	Volts
($I_C = 500mA$, $I_B = 50mA$)	$V_{CE(SAT)}$*	—	1.0	Volts
Base-Emitter Saturation Voltage				
($I_C = 150mA$, $I_B = 15mA$)	$V_{BE(SAT)}$*	0.6	1.1	Volts
($I_C = 500mA$, $I_B = 50mA$)	$V_{BE(SAT)}$*	—	2.0	Volts

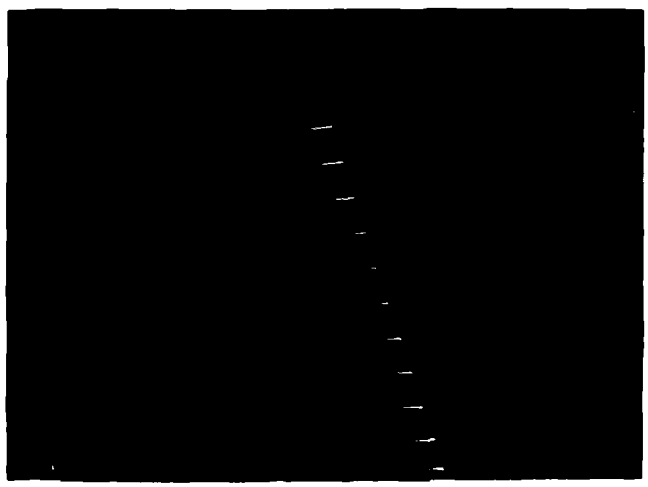
FIGURE 7. DC SPECIFICATIONS FOR TYPICAL SMALL SIGNAL TRANSISTOR

GES2221A, 2A

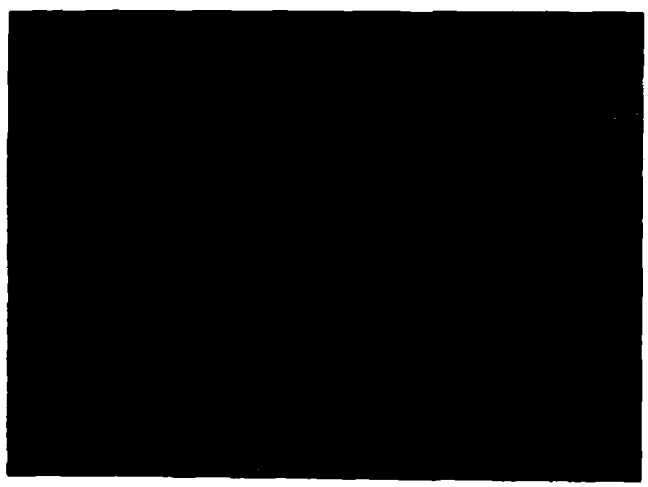
STATIC CHARACTERISTICS (Continued)	Symbol	GES2221A Min.	GES2221A Max.	GES2222A Min.	GES2222A Max.	
Forward Current Transfer Ratio						
(V_{CE} = 1.0V, I_C = 150mA)	h_{FE}*	20	—	50	—	
(V_{CE} = 10V, I_C = 0.1mA)	h_{FE}	20	—	35	—	
(V_{CE} = 10V, I_C = 1.0mA)	h_{FE}	25	—	50	—	
(V_{CE} = 10V, I_C = 10mA)	h_{FE}*	35	—	75	—	
(V_{CE} = 10V, I_C = 150mA)	h_{FE}*	40	120	100	300	
(V_{CE} = 10V, I_C = 500mA)	h_{FE}*	20	—	30	—	
Collector Cutoff Current						
(V_{CB} = 60V, I_E = 0)	I_{CBO}	—	10	—	10	nA
(V_{CB} = 60V, I_E = 0, T_A = 100°C)	I_{CBO}	—	10	—	10	μA
Emitter-Base Reverse Current						
(V_{EB} = 3.0V, I_C = 0)	I_{EBO}	—	50	—	50	nA

*Pulsed, 300 μsec, ≦ 2% duty cycle

FIGURE 7. DC SPECIFICATIONS FOR TYPICAL SMALL SIGNAL TRANSISTOR (Cont'd)



a). GAIN MEASUREMENT



b). V-I CHARACTERISTICS AT BREAKDOWN

FIGURE 8. CURVE TRACER FAMILY CHARACTERISTICS OF GES2222A TRANSISTOR

Several intermediate cost bench top logic test systems are generally used when evaluating circuit board logic functions that utilize many integrated circuits. Such systems are becoming highly sophisticated (See, for example, the Tektronix 7D01 Logic Analyzer and the attachments available).

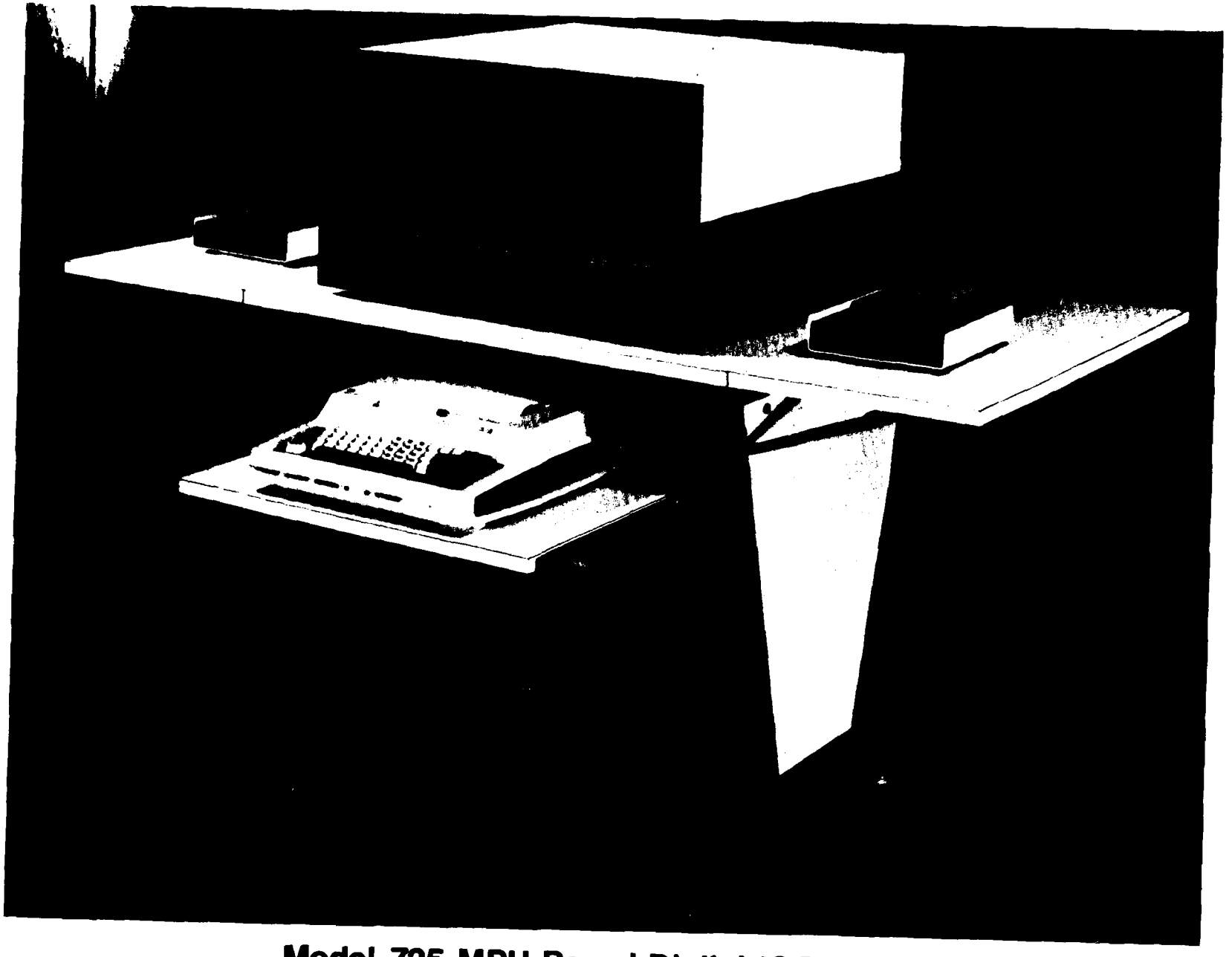
More complex IC logic test equipment, such as the system shown in Figure 9, requires extensive software and is relatively expensive (See Equipment Section). Such equipment is not normally common to the failure analysis laboratory unless failure analysis is performed on many circuits of the same or similar type.

d) Commercially Available Linear IC Test Equipment. Commercial equipment for bench top testing of linear IC's is available in the form of curve tracer accessories and more complex test systems (See Equipment Section). The curve tracer accessory system is sufficient for evaluating the dc characteristics of linear circuits, while the more expensive test systems will evaluate dynamic performance.

e) Breadboard Test Fixtures. Breadboard test fixtures are more commonly utilized by the failure analyst than is dedicated test equipment. Curve tracer and/or pin-to-pin electrical tests are generally used to determine dc characteristics such as gate input current to ground, breakdown from V_{ss} to ground, etc. Breadboard fixtures can be used to more completely characterize devices both in terms of dc and dynamic ac performance. Following are a few breadboard circuits that might prove useful in characterizing some specific types of devices:

e Diodes and Transistors. Usually, manufacturer's specification sheets will include typical test circuits for measuring such characteristics as turn-on and turn-off times, frequency of oscillation, diode reverse recovery time, etc.

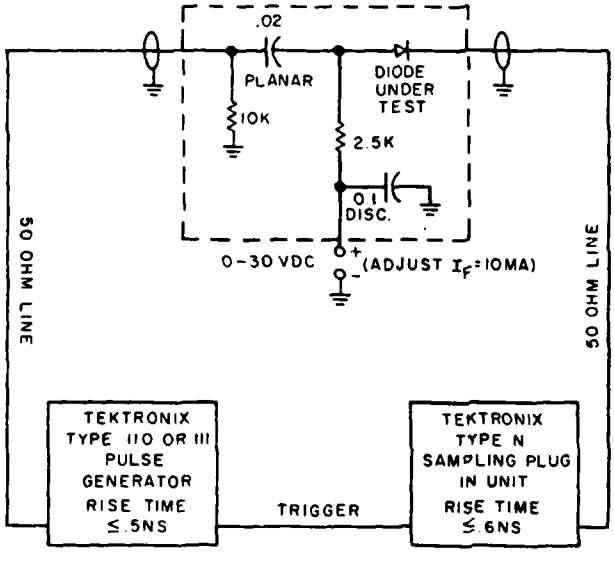
Figures 10 through 12 show, respectively, test circuits for measuring 1N4863 diode low and high current reverse recovery time, 2N3662 transistor turn-on and turn-off times, and 2N3662



Model 725 MPU Based Digital IC Tester

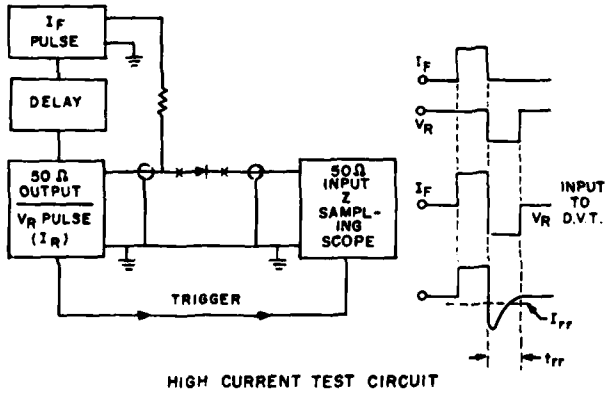
FIGURE 9. DIGITAL INTEGRATED CIRCUIT TEST SYSTEM

HERMALT COLOR CORP 11 RICHMOND ST CLIFTON N J (201) 772-2661



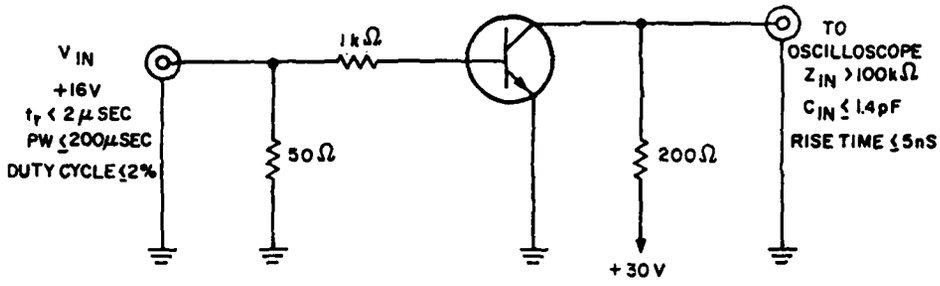
LOW CURRENT t_{rr} TEST CIRCUIT

FIGURE I

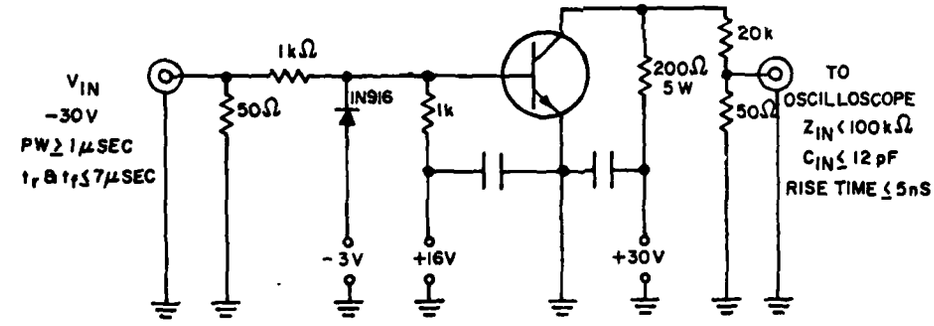


HIGH CURRENT TEST CIRCUIT

FIGURE 10. BREADBOARD CIRCUITS FOR MEASURING IN4863 REVERSE RECOVERY TIME



TEST CIRCUIT FOR DETERMINING TURN-ON TIME



TEST CIRCUIT FOR DETERMINING TURN-OFF TIME

FIGURE 11. BREADBOARD CIRCUITS FOR MEASURING 2N3662 TURN-ON AND TURN-OFF TIMES

TEST CIRCUITS

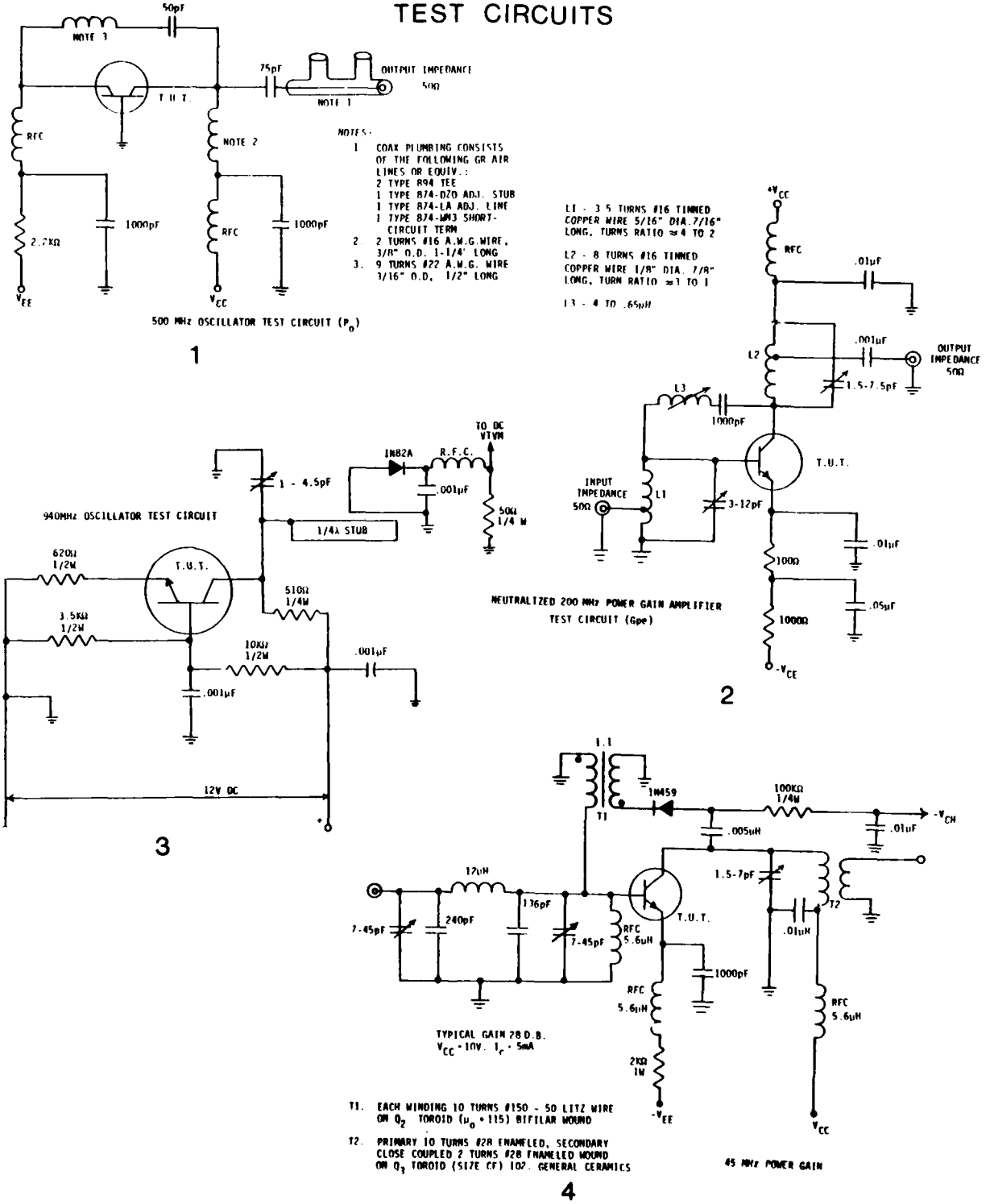


FIGURE 12. BREADBOARD CIRCUITS FOR MEASURING 2N3662 OSCILLATOR AND POWER AMPLIFIER CHARACTERISTICS

transistor oscillator and power amplifier characteristics. These circuits are typical of breadboard setups for diode and transistor evaluations.

o SSI/MIS Logic Integrated Circuits. Many of the logic functions are highly specialized, and, therefore, special breadboard test circuits are necessary for characterization. However, the simpler logic circuits such as AND, OR, J-K flip-flop, decade counters, etc., can be characterized with relatively simple equipment setups.

Figure 13 shows a breadboard circuit that will easily characterize simple gates and allow measurement of:

1) Verification of truth table
2) Input gate current
3) Input voltage level
4) Output voltage level
5) DC power supply current

Figure 14 shows a circuit that allows dynamic measurement of simple gates, J-K flip-flops, counters, etc., and will measure:

1) Input voltage level
2) Output voltage level
3) Signal transit time
4) Functionality
5) Power supply current

o Linear Integrated Circuits. A relatively simple test circuit for measuring dc characteristics of linear circuits is shown in Figure 15. This circuit will allow the failure analyst to measure the dc parameters:

1) Input offset voltage
2) Input bias current

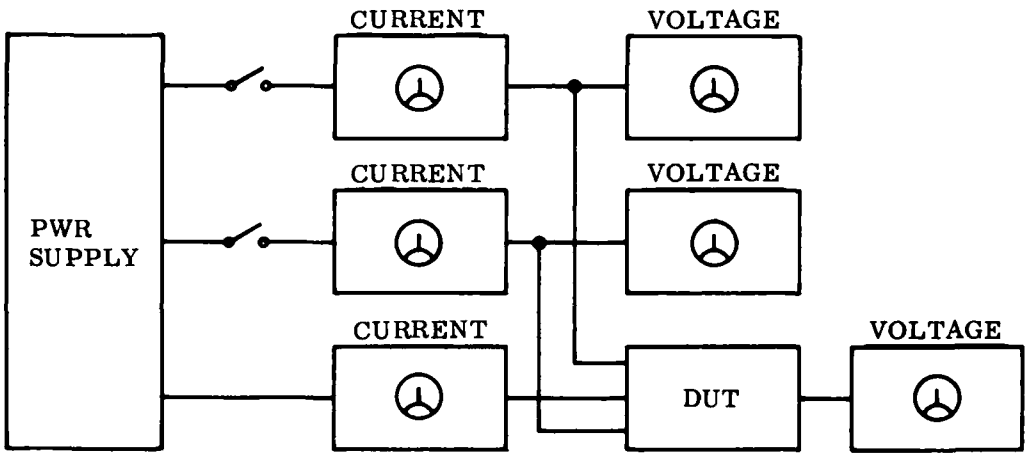


FIGURE 13. CIRCUIT FOR DC CHARACTERIZATION OF SIMPLE LOGIC GATES.

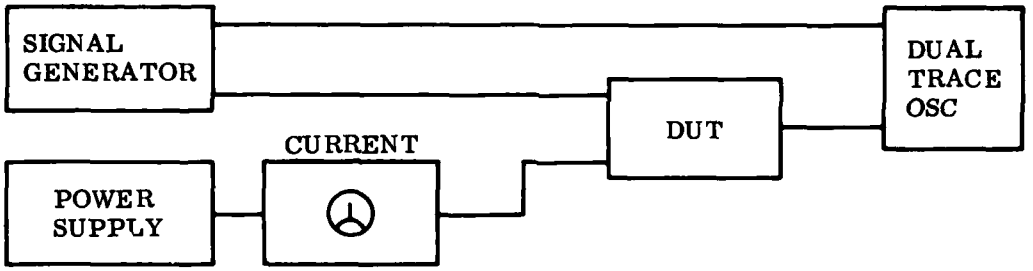


FIGURE 14. CIRCUIT FOR DYNAMIC CHARACTERIZATION OF SIMPLE LOGIC GATES.

3) Input offset current
4) High impedance composite input offset voltage
5) Voltage gain
6) Common mode rejection ratio
7) Power supply rejection ratio

The test setup shown in Figure 15 requires five separate power supplies. The circled numbers from 1 to 9 designate banana plugs, and the switches K1 to K3 designate toggle switches.

Use of the circuit in Figure 15 will allow the failure analyst to rapidly verify the majority of failures in linear circuits. Detailed explanations of how to use and interpret the circuit in Figure 15 can be found in Reference 4.

4. Automatic Test Equipment. Because of the increasing complexity of microelectronic devices, it is often impractical to attempt failure verification by bench top methods. For example, it would be a monumental task to locate and verify failure of a single bit in a complex memory using bench top equipment only. MOS/LSI digital circuits are many times the physical size of SSI circuits and are tremendously more complex. With such complexity, automatic test equipment becomes almost a necessity. Computerized test equipment can characterize failures such as voltage or timing sensitivity, parametric degradation, decoding malfunctions, single bit errors, voltage, pattern, output level sensitivities, etc.

One of the useful options available with automatic test equipment is the CRT display. Functional pass or fail information can be displayed on this screen. A keyboard input device allows access to the test information stored in memory. By use of the keyboard entry it is possible to make voltage, timing, or failure trip level changes in the test program without having to rewrite the test program. A hardcopy output can also be made available for documenting parametric readings.

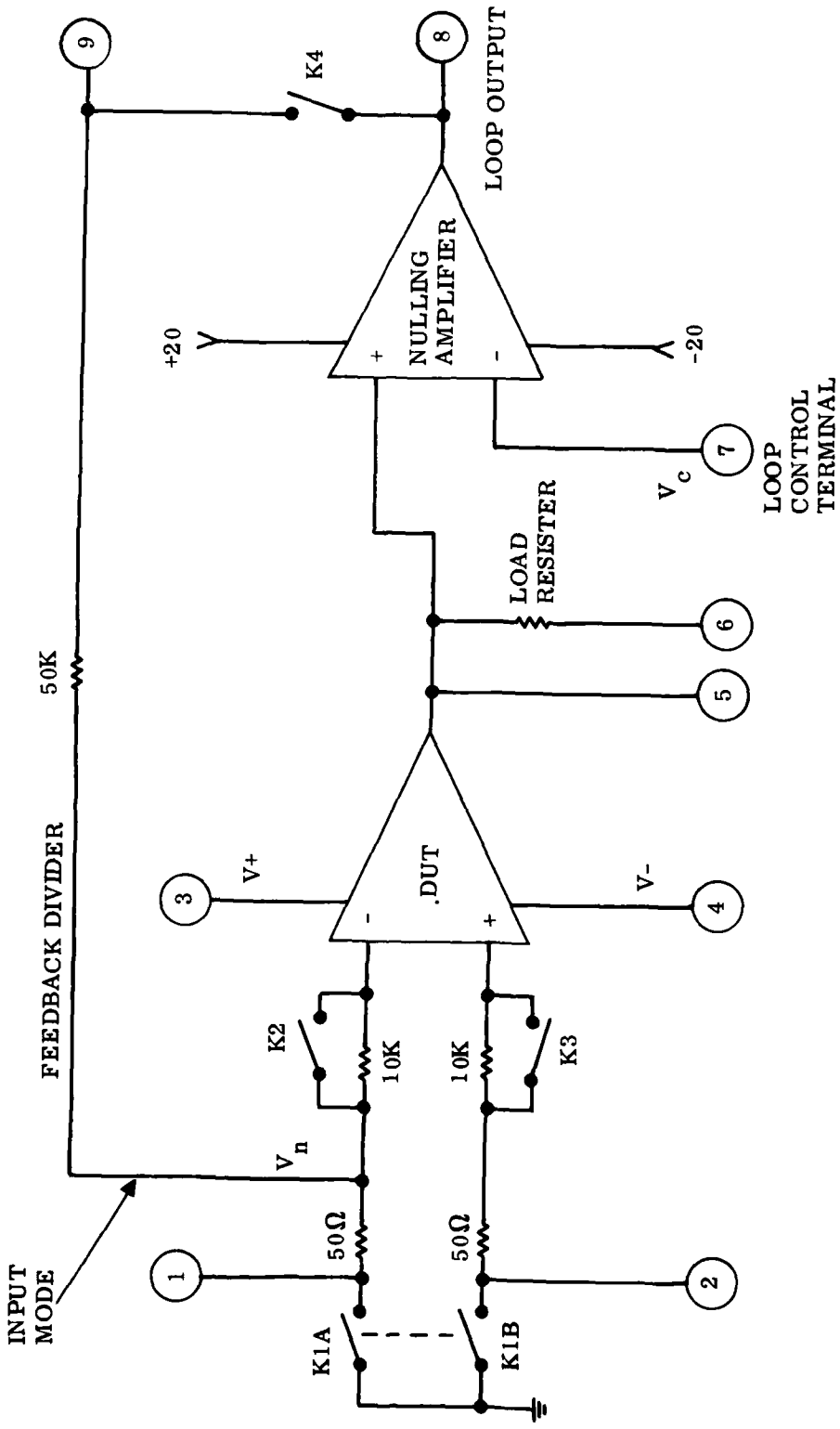


FIGURE 15a. BASIC LINEAR OP-AMP TEST CIRCUIT.

FIGURE 15b. TEKTRONIX S3270 AUTOMATED SEMICONDUCTOR ELECTRICAL TEST SYSTEM.

In verifying failures with automatic test equipment, the use of correlation samples is critical. These samples should consist of totally good samples, functionally bad samples, and parametrically bad devices to verify tester functions.

Temperature cycling attachments are also available whereby complex circuits can be fully tested while being put through full temperature cycling. Reported failures that pass room temperature tests should be retested with temperature cycling and at various power supply voltages.

Parametric failures can be degradational or they can be catastrophic. The data on these failures can be obtained by using the data log output format available with automatic test equipment.

Functional failures in LSI circuits are often more difficult to analyze than functional failures in less complex circuits because, for example, large amounts of complex circuitry exist between input and output pins. Functionality of simple logic circuits may depend on correct operation of one, two, or three gates between a given input and output. Functionality of LSI logic circuits such as microprocessors may depend on correct operation of 50 to 100 gates to produce a correct output for a given input.

Verification and isolation of a failure site along a given circuit path in complex circuits is virtually impossible using bench top equipment alone. Location of failure sites in complex integrated circuits is made much easier through the features available with automatic test equipment.

a) Functional Versus Parametric Tests. The concept of functional testing being uniquely separable from parametric testing was briefly discussed in Section 3 of this chapter. In Section 3 an example was given which showed that it is extremely difficult to separate failure causes into functional or parametric categories.

As circuits become more complex, some parametric tests may have little relevancy. For example, suppose that an input transistor to a gate far inside the interior of a microprocessor is excessively leaky. Suppose that this transistor leakage is sufficient to prevent the gate from functioning properly. In this event, it is unlikely that any parametric tests at the accessible circuit terminals will reveal useful data.

Note: In a case like this, some parametric values may, however, indicate that a problem exists. Parameters such as power supply current may show a significant increase if the transistor mentioned in the example is leaky enough. The point being made by the example is, however, that the failure analyst will probably have no idea where to look to isolate such a failure because parametric tests at the specific input which eventually leads to the faulty gate are unlikely to reveal a fault.

b) Shmoo Plots. In many cases a system engineer who designs microelectronic elements into systems will design using the manufacturer's data sheet "typical" values. The designer assumes that every element going into his system will have parameters that fall well within these narrow limits. This practice often results in a reported field failure which, after being retested, ends up as a non-verified failure or classified as "electrically retest good."

The fact that there are variations in device parameters must be taken into account. The so-called "typical" parameter values on specification sheets are actually the average value of the parameter as determined by the manufacturer.

The ability of automatic test equipment to produce Schmoo plots is a powerful tool in analyzing and characterizing many reported field failures. The Shmoo plot is a printout which quantifies the actual range of operation as a function of two or more parameters. The variables may be temperature and supply voltage, or temperature and input level. When compared to the conditions

existing at reported failure, the Schmoo plot may reveal that the device will not, in fact, work under those conditions. Figure 16 shows typical Shmoo plots of two and three parameters. These Shmoo plots are, respectively, for a microprocessor and a dynamic memory.

In obtaining the Shmoo plot shown in Figure 16a, the pulse width of input signals to a microprocessor was varied along with power supply voltage. The "plus" symbols indicate areas of functionality and the "minus" symbols indicate areas of non-functionality.

Clearly, electrical testing of the more complex devices becomes impossible on the bench. For example, testing a 4K semiconductor memory to even a single pattern would be difficult on the bench using even nominal test conditions. With bench techniques, one would not even attempt to perform any type of characterization testing such as that required to generate a three dimensional Shmoo plot of read access time as a function of supply voltage and ambient temperature. The 2000 to 10,000 complete functional tests required are just not possible manually, but using ATE this becomes routine and it is possible to generate and display this data (or any other performance data) with programming time of typically three to four hours.

A large chore using bench techniques is the task of testing the example 4K semiconductor random access memory with a single fixed timing. This might be possible using bench equipment if the proper associated circuitry were built to accomplish address sequencing, I/O control, and perform data comparisons. This, however, would require considerable set-up time and would not be usable with other types of memories. It would certainly be impossible to do with manual switching because of the large number of steps in most memory test patterns not to mention the factor introduced if one considers the refresh requirements of dynamic memories.

Next to impossible using bench techniques is the task of measuring worst case cell access time. Obtaining read access time, for example, requires that the memory first be checked for functionality,

using a specific pattern and known timing. For a 4K RAM this single test typically can take 10 to 15 seconds at the minimum cycle time (A typical n^2 type test on a 4K memory requires over 32×10^6 cell accesses, which, if done at a rate of 3 MHz, would require about 10 seconds). If the device passes on first try, the timing is incrementally modified and the test repeated until the timing at the point of failure is established. From this iterative testing and known timing, the read access time may be established. At least 5 complete functional tests are usually required to establish a single read access time. Using ATE, this requires about one minute at maximum speed for this example. This measurement probably wouldn't even be attempted using a bench technique.

Definitely impossible using bench techniques is the task of observing a critical performance characteristic such as read access time over a range of operating conditions such as supply voltage and temperature. This is the type of information most valuable for device characterization or failure analysis since it allows for the easy identification of regions of marginal operation. Relative to the testing itself, this requires the previous access time measurement to be performed at even combination of temperature and supply voltage. For a region of 20 voltage points by 20 temperature points, this requires 400 read access time measurements at 1 minute each or about 400 minutes using ATE. This is only one device during an eight hour work shift! This certainly is not too practical even on ATE, but it can be done with no operator intervention if the system has a mini-environmental chamber such as that shown in Figure 4. With this, the testing program has complete control over all DUT variables including ambient temperature.

To illustrate the value of a powerful data presentation capability, consider that the resulting data could then be printed on several pages and be almost impossible to interpret, or it could be displayed graphically in the form of a Shmoo plot where significant features are immediately obvious. In our example, this allows the read access time to be displayed as a function of two variables (temperature and supply

voltage) in a three dimensional format which can be viewed from any direction. Figures 16b and 16c are examples of this type of data presentation, illustrating the ease with which regions of marginal operation may be established and trends such as temperature sensitivities identified for characterization purposes. Without ATE, this type of information, which is necessary to ensure adequate device specification, probably would not be available during characterization testing or to assist the failure analyst in the identification of marginal device operation. Figure 16d shows a typical ATE system equipped with temperature control unit.

5. Verification of Intermittent Failures. If a device failure cannot be reproduced, and thus verified, by any of the methods described previously, the failure may be intermittent in nature. There are a number of conditions which might result in an intermittent failure. These conditions may range from gross faults to subtle ones. Some of the conditions existing in a microelectronic device which might result in intermittent failures are:

- Loose conductive particles inside a package cavity can cause intermittent shorts
- Bad design or layout on the device, printed circuit board, or system level might result in intermittent localized heating problems or in parasitic devices randomly causing parametric or functional problems (for example, triggering of a parasitic SCR in a CMOS logic circuit by a system transient)
- Surface leakage paths created by contaminants in the package ambient, such as water vapor
- Poor solder or weld joints that open during vibration, or temperature cycling

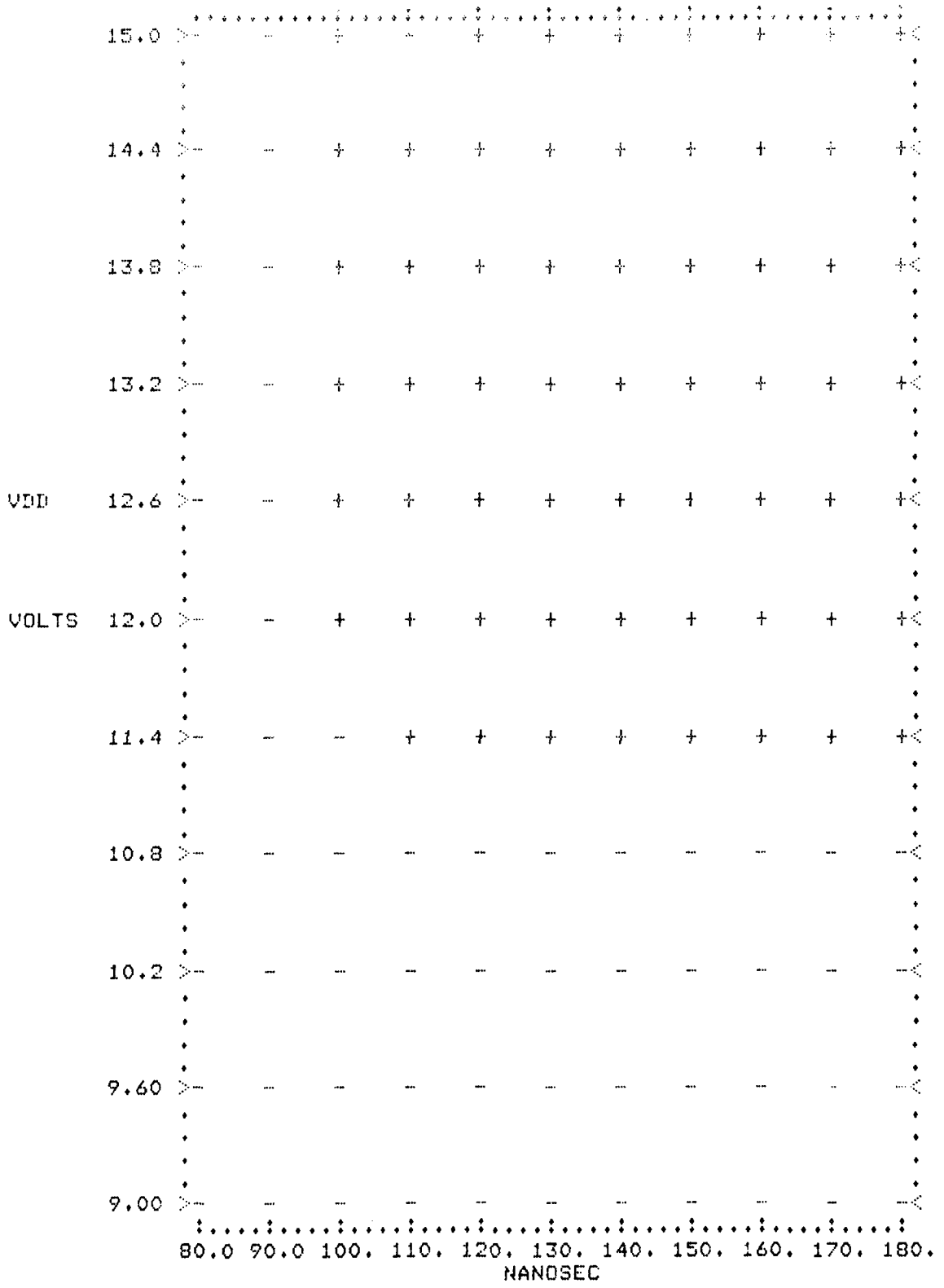


FIGURE 16a. TYPICAL SCHMOO PLOT OF MICROPROCESSOR OPERATION AS A FUNCTION OF INPUT PULSE WIDTH AND POWER SUPPLY VOLTAGE. "PLUS" AREAS INDICATE CORRECT OPERATION, AND "MINUS" AREAS INDICATE FAULTY OPERATION.

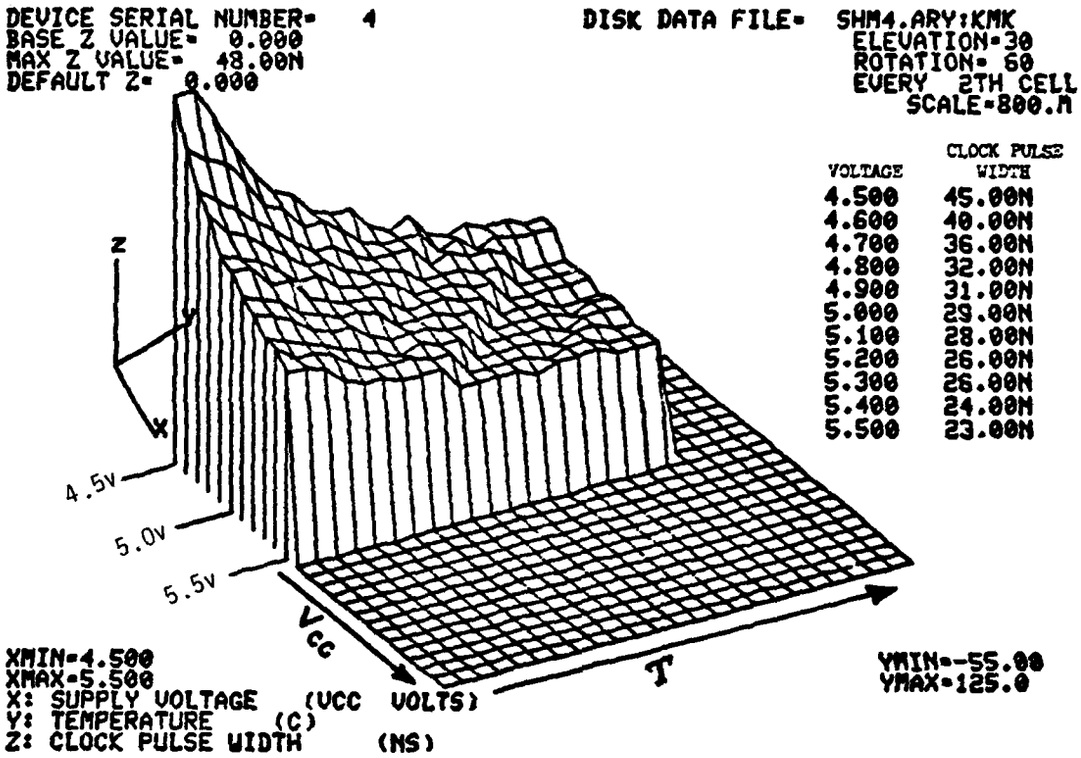


FIGURE 16b. THREE DIMENSIONAL SHMOO PLOT (GRAPHIC DISPLAY) OF CLOCK PULSE WIDTH VERSUS TEMPERATURE AND SUPPLY VOLTAGE Vcc.

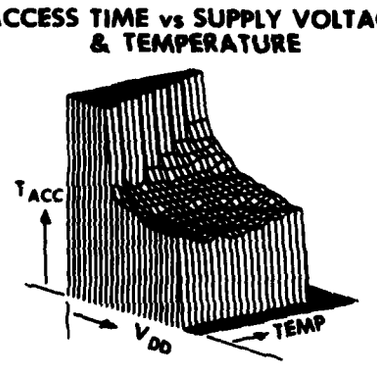


FIGURE 16c. THREE DIMENSIONAL SHMOO PLOT OF ACCESS TIME VERSUS SUPPLY VOLTAGE AND TEMPERATURE.

FIGURE 16c. TEKTRONIX S3260 AUTOMATED SEMICONDUCTOR ELECTRICAL TEST SYSTEM WITH TEMPTRONIC THERMOSTREAM® TEMPERATURE CONTROL UNIT.

- o Microcracks in thin film metallizations that might cause open circuits as a function of thermal cycling
- o High electrical resistance associated with wire bonds
- o Breaks in wire bonds on wires in plastic encapsulated devices
- o Cracked die

There are three test methods described below which may verify a suspected intermittent failure. All the tests are potentially destructive but should not be if conducted with appropriate care.

If the exact conditions under which a part failed are known, then the test corresponding to those conditions should be performed first. For instance, if the failure was reported to have occurred during temperature fluctuations, then the first test described, using temperature variation, should be used. If such specific information about conditions at failure are not known, then the tests should be performed in the order given.

a) Temperature Cycling with Monitoring. The initial electrical measurements will have already been made in room temperature conditions. If either an oscilloscope or curve tracer is being used, it would be advisable to make photographic records of the initial test results for purposes of comparison.

b) Heating. Some of the ways in which microcircuits can be heated while monitoring are:

- o Method I. The simplest way to heat a microelectronic device while monitoring the electrical characteristics is to use a heat gun. A thermocouple can be attached temporarily to the device surface for monitoring temperature. It will be necessary to hold the packaged device at a given temperature for several

minutes to insure that the enclosed devices have reached equilibrium with the indicated package case surface temperature. Care must be used with the heat gun because it is capable of heating devices well beyond the manufacturer's specifications.

o Method II. Another method of heating a device is to use the tip of a soldering iron. The thermocouple attachment can be used in this method also. Care must again be used to allow the enclosed elements to rise to the indicated package case surface temperature.

o Method III. Commercial environmental chambers are available for temperature cycling.

In all heating methods, it would be advisable to advance the operating temperature in steps of 5°C until failure is detected. Care must be used to avoid exceeding the manufacturer's maximum operating temperature.

c) Cooling. Some of the ways in which microcircuits can be cooled while monitoring are:

o Method I. The simplest way to cool microcircuits is through the use of a commercially available spray specifically intended for this use, for example, "Quick-Freeze" (See Equipment Section). The coolant can be applied directly to the unit or rapidly sprayed across the package surface. This spray is capable of achieving package case temperatures in the range of -40°C to -50°C.

o Method II. Another method is to bring dry ice into direct contact with the package. This method will also produce package temperatures in the range of -40°C to -50°C.

o Method III. Commercial environmental chambers are available which will produce the required low temperature.

Combinations of heating and cooling methods can be used to stress an element while monitoring electrically. Generally, if devices have intermittent failures which are affected by temperature cycling, a fault will be observed during the first few cycles.

Note: Intermittent failures which are temperature sensitive may often occur over a limited temperature range. The failure analyst must continually observe units under test and remain alert for this possibility because such failures may be difficult to document.

d) Vibration With Monitoring. A typical sequence that might be followed in this type of test is listed below:

- Consult the manufacturer's specification to obtain the maximum frequency and acceleration which the microelectronic device package should be able to withstand. Typically, the frequency range is 10 to 2000 Hz, and the acceleration in the range of 98 to 196 m/s^2.
- Select an acceleration. This value is held constant throughout the test.
- Select a frequency range; for instance, 10 to 1500 Hz.
- Select the length of the cycle; typically, a 10- or 20-minute cycle.
- Run the cycle while monitoring electrically.

Note: A 10-minute cycle is 20 minutes in length because of the actual run procedure. For example, the test is begun at the low frequency (typically 10 Hz) and run up to maximum frequency through a 10-minute period. The frequency is then lowered through another 10-minute period. Likewise, a 20-minute cycle is actually 40 minutes in length.

e) Shock with Monitoring. A typical sequence that might be followed in this type of test is listed below.

- o Consult the manufacturer's specification for the maximum shock allowable
- o Rigidly fix device to shock equipment monitoring apparatus
- o By beginning with lower than maximum shock conditions, shock the device while monitoring electrically by lifting the mounted device a sufficient height to achieve the required acceleration
- o Continue shocking/electrical monitoring cycles until failure is observed or until maximum shock conditions have been reached

Note: Before doing a shock test with shock equipment, the failure analyst may gently tap the unit while it is being tested. This has been known to be sufficient to verify an intermittent failure.

f) Uses of Centrifuge. The centrifuge is used as a screening test in product acceptance and often in failure analysis to identify bonding wire lead dress problems. If during wire bonding operations wire of insufficient length is used, an electrical short can result from the bonding wire coming in contact with the die edge. Electrical shorting can also result from a loose conductive particle that becomes trapped between bonding wire and die edge.

When microelectronic failure is suspected to be a result of one of the causes described above, the failure analyst might decide to document the failure cause by a test - centrifuge - retest cycle.

Note: Care must be used when centrifuging parts so as not to cause physical damage to the microelectronic package. That is, too much force during centrifuge operations can, for instance, cause the package to crack. See References 18 and 19 for more details.

g) Particle Impact Noise Test. (See Chapter III-F for details.) Intermittent failure might possibly be due to loose conductive particles inside a package. PIND tests will definitely indicate the presence or absence of particles inside a package.

h) Monitoring. The question of what and how to electrically monitor during the tests described above is obviously very important. The use of the words "electrical monitoring" in these tests assumes that some knowledge exists about what exactly should be monitored. Some of the sources from which knowledge might come are:

- The device type being tested
- Knowledge regarding internal components and structure, such as from a schematic
- Knowledge regarding the reported device failure

The last of these is by far the most important. The importance of obtaining as much information as possible about the reported failure cannot be stressed enough.

After deciding what to monitor, the question of how to monitor must be answered. For example, one would not use a relatively insensitive ammeter to monitor a minor change in the

input bias current of an operational amplifier. A more sophisticated instrument would have to be used. Similarly, an expensive digital voltmeter is not needed to monitor a T^2L output voltage transition.

6. Fault Isolation. Once electrical failure has been verified, further techniques become necessary to isolate the specific cause of failure. If obvious external causes and hermeticity have been eliminated, then it becomes necessary to open the package for further analysis. Chapter III-E contains details on package opening techniques for a variety of package types.

Probably the most valuable tool available to the failure analyst at this point in his investigations is visual observation. A number of failure modes and their manifestations have been tabulated previously in Section I. Many of these failure modes/mechanisms are obvious when viewed through the light microscope.

There are other failure modes which are more subtle in nature. These generally will require the more sophisticated techniques detailed in subsequent chapters and more in-depth circuit analysis. Whatever the approach used, once the fault is isolated to a small area of a complex device, individual active elements on the device may need to be electrically isolated from surrounding elements and tested further.

a) Die Isolation. This destructive technique is the final and definitive test for any package related electrical failure modes. The technique involves removing the package internal wiring from the die. Consult Chapter III-L for further information.

Once the wires are removed, the pin-to-pin tests described in this chapter should be repeated. If any leakage or shorts are noted during this test, they may explain electrical failure and should be documented. If anomalies are noted, then their relation to the observed failure must be judged. If no anomalies are recorded, then isolation should proceed.

b) Isolation by Micromanipulator Probe. Figure 17 shows typical micromanipulator apparatus. Isolation using this instrument is accomplished by scraping through die metallization lines breaking electrical contact. This method is the simplest because it requires the least investment in both time and equipment.

Most integrated circuits are manufactured with a passivating layer of silicon dioxide. It is possible to break through this dielectric layer and cut the metal underneath, but several passes with probe tip will probably be necessary. Thinning the oxide layer by chemical etch is recommended for dense circuits. See Chapter III-N for details of chemical processing.

When using this mechanical technique, care must be used when adjacent metallization is present because it is possible to cause shorts between metallization runs by smearing the metallization.

Cutting metallization in this way may leave thin strings of metal that still provide electrical continuity in the cut area. There may also be shorts caused by smearing action of the probe. There are a number of chemical methods avaible to remove these thin strips of metal. If the metal is aluminum, the same buffered mixture of hydrofluoric acid used to remove passivation oxide will attack and etch freshly scratched aluminum. See Chapter III-N for details on etching and acid handling.

c) Isolation Through Overstress of Metallization. This method requires three electrical probes. One probe tip is positioned where the metallization cut is desired. The other two probe tips are connected together and placed on the same metallization run on either

side of the first probe. A low voltage (about 5 volts) is then applied between these two probes and the center one. This procedure produces a controlled metal run zap at the center probe location. The procedure is commonly called the "controlled zap" or "capacitor discharge" method depending on the energy source. Figure 18 shows an opening made with this method. A curve tracer is usually sufficient to supply the current needed.

d) Isolation Through Spot Etching. There are two variations of this process. One involves a single probe tip, and the other involves a photoresist technique.

In the first method, a drop of a suitable metal etchant is placed on the tip of a probe. The probe tip is then lowered until it comes in contact with the metal to be separated. The etchant will etch its way through the metal, providing separation. Figure 19 shows a separation made in this way.

With the second spot etching technique, small, hard to access metal runs can be separated by exposing a spot of positive photoresist and subsequently etching the metal away. This method is time consuming and quite tedious.

A layer of positive photoresist is applied to the microcircuitry by a suitable dispenser, and uniformity is achieved by spinning. The photoresist is then treated to a precuring cycle in a convection oven at about 65°C for 15-20 minutes. Care must be used not to expose the photoresist from this point on to ordinary room white light. Yellow room lights are necessary.

The device is placed under an ordinary binocular field microscope equipped with a yellow filter in the light source. The area to be cut is located. A Nicholas Illuminator equipped with a black shield over the end lens is prepared. A small hole should be cut in the center of the black shield. This illuminator is then inserted, at low light level, in one eyepiece of the microscope. By turning down the microscope yellow filtered light source, the spot from the Nicholas light source can be seen near the center of the field of view. This spot will be used to expose the photoresist in the area where the cut is to be made. The X and Y controls of the microscope are used to locate the spot.

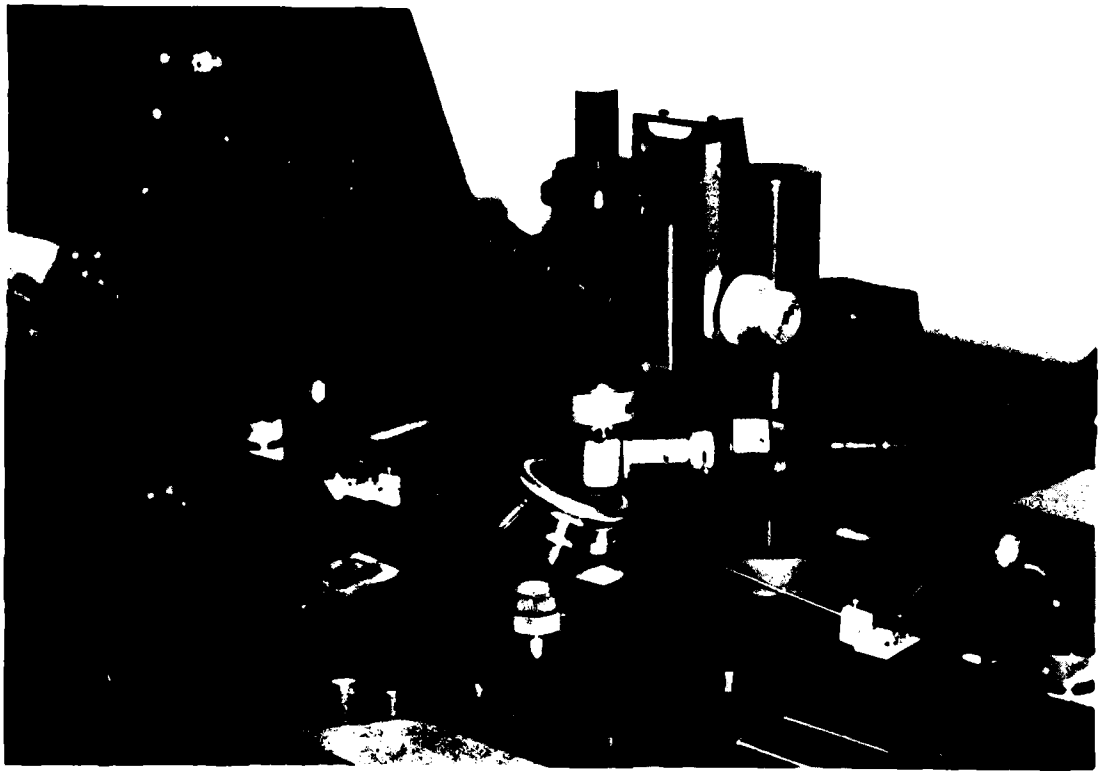


FIGURE 17. TYPICAL MICROMANIPULATOR TEST STATION

FIGURE 18. ELECTRICAL ISOLATION USING VOLTAGE OVERSTRESS

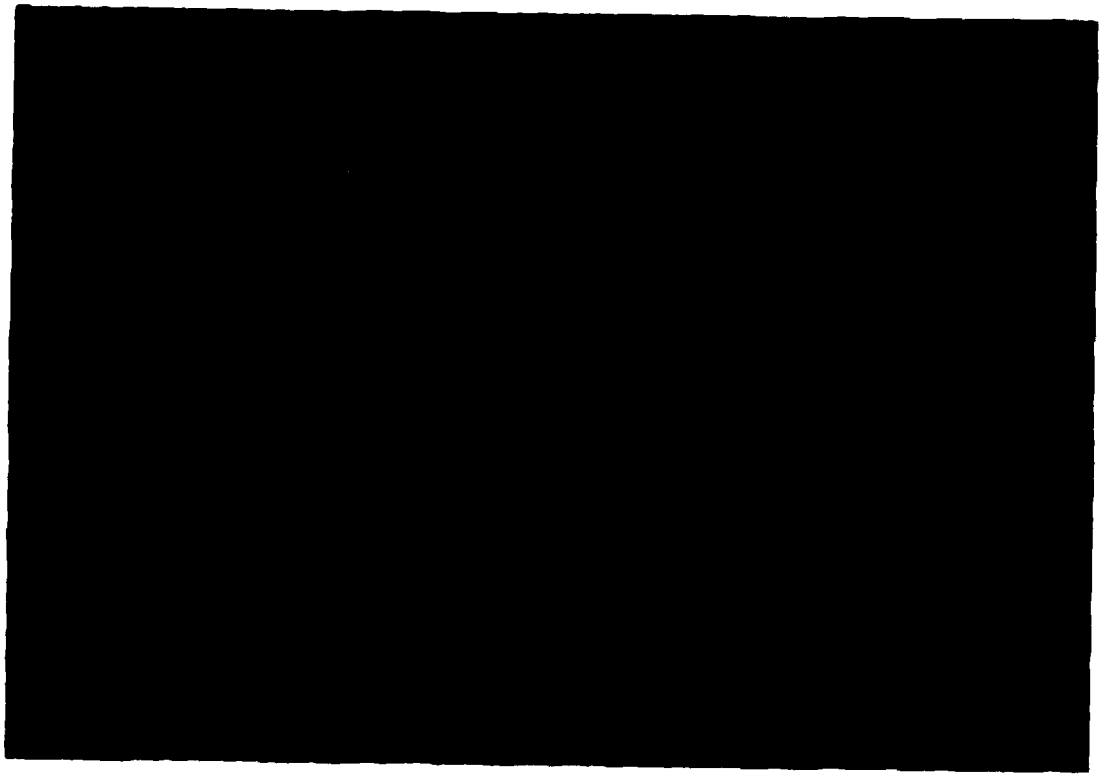


FIGURE 19. ELECTRICAL ISOLATION USING SPOT CHEMICAL ETCH

The photoresist is exposed by increasing the intensity of the Nicholas light source. Photoresist in the exposed area is removed by the appropriate developer solution. A solution of suitable metal etchant can then be used to etch the metal away. The photoresist is then removed, usually in acetone. The photoresist process described can be used with Shipley type positive photoresists but may vary with other types.

The resolution obtained with this type process is satisfactory with the more dense MSI and LSI circuits. Figure 20 shows cuts and two holes in a 0.001-inch (25.4um) wide aluminum stripe. The smaller hole is less than 0.0001 inches (2.54 um) in diameter.

This process causes the least damage to underlying and adjacent topography of the microcircuit. For instance, the underlying oxide is not damaged as with the cutting technique.

Aluminum metallization systems only have been described, but other metal systems can be effectively handled by using the appropriate chemical etches. See Chapter III-N for details on chemicals.

e) Isolation by Laser Cutting. With a good deal of practice, preferably on similar microcircuits, a laser may be used to cut metal stripes. This method is fast and quite accurate, but it obviously requires easy access to a laser.

f) Isolation by Ultrasonic Cutting. This technique utilizes a sharp probe fitted to an ultrasonic horn such as the type used in wire bonding equipment. Metallization lines can be accurately cut using this technique. This technique also allows the cutting of multilayer interconnects, a technique which is practically impossible by any other means. Figure 21 shows polycrystalline silicon cut through 2 μm of silicon diode, and Figure 22 shows an ultrasonically cut aluminum metal run.

FIGURE 20. HOLES CUT THROUGH 0.001 INCHES ALUMINUM METALLIZATION. ARROW POINTS TO HOLE LESS THAN 0.0001 INCHES IN DIAMETER

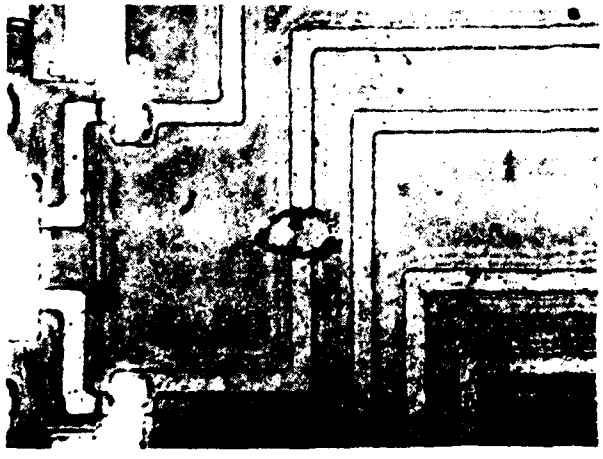


FIGURE 21. POLYCRYSTALLINE SILICON INTERCONNECTION (12.7 μm) CUT WITH AN ULTRASONIC PROBE

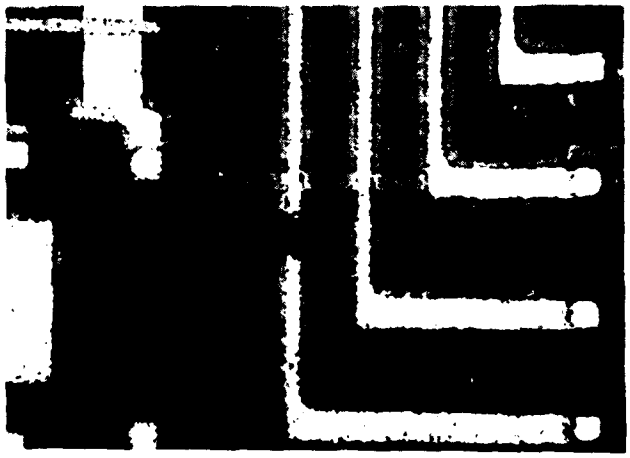


FIGURE 22. ALUMINUM METALLIZATION INTERCONNECTION CUT WITH ULTRASONIC PROBE

7. Die Probing Following Isolation. Once individual elements in a complex microcircuit have been successfully isolated from surrounding circuitry, micromanipulator microprobe apparatus similar to the one shown in Figure 17 can be used to electrically characterize the element.

Micromanipulator apparatus is capable of mechanically reducing hand movements to the fine geometric distances used in microcircuits. Movements of the probe tips are observed through the microscope and the probe tips are placed on metal connections of the isolated device in an appropriate manner to evaluate it.

Generally, most silicon devices will require four probes for characterization. For a bipolar device, these connections will be used on substrate, base, emitter, and collector. For a MOS device, they will be used to contact substrate, drain, source, and gate. A diode will require only two probes for anode and cathode.

Usually a curve tracer is sufficient for most electrical characterization, but combinations of power supplies, volt-ohm or current meters, and frequency generators may be used. High frequency measurements above 1 MHz are generally impractical because of loading problems, crosstalk, etc.

8. Metal Probe Making and Pointing Methods. Tungsten probes with the sharp tips needed in microelement probing are difficult to purchase. In addition, the probe tips are easily damaged during use. As a result, many laboratories make and sharpen their own probes.

Probes are not difficult to make and do not require much time if a flame technique is used. Etching probes from wire stock becomes a lengthy process if many probes are to be made.

In the flame technique, probes are cut from tungsten wire into lengths approximately 1 cm longer than the required length. These wire pieces are then oxidized by introducing them into the tip of a flame.

The wire is moved back and forth through the flame. As the tip is thinned into a sharp point, the oxidized metal will be discarded by the pressure of the gas from the flame.

Chemical methods exist for producing sharp points on new probes and for resharpening dulled or broken ones. An electrochemical cell using sodium hydroxide will satisfactorily sharpen probes in a short time. Figure 23 diagramatically demonstrates the apparatus. The tungsten metal is caused to dissolve into the electrolyte as a result of dc electric current. In order to produce a sharp tip, the probe must be cycled into and out of the electrolyte in approximately 1-second intervals for about 25-50 cycles.

Another chemical method exists that will produce probe tips as small as 0.5 μm in diameter. This method differs from the previously described one in the following respects:

a) Ac current is used, 60 Hz, obtained through suitable isolation transformer
b) Copper is purposely introduced into the electrolyte solution
c) The insertion and withdrawal cycle is increased to 3-5 times per second

This method uses an electrolyte solution of from 10% to 50% of either sodium hydroxide or potassium hydroxide. Probe tip sharpening depends heavily on the concentration of copper that is added to the electrolyte. If the copper concentration exceeds 1.1 mg per ml, tips will not sharpen. The copper may be added by dissolving cupric chloride or by substituting a copper electrode for the tungsten wire at 5 volts ac for about 1 minute.

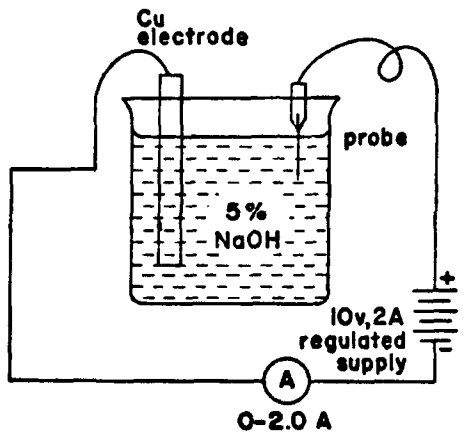


FIGURE 23. DIAGRAMMATIC REPRESENTATION OF METAL PROBE POINTING APPARATUS

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2. Anstead, R.J. "Failure Analysis of Electronic Parts: Laboratory Methods.," Nat. Tech. Info. Service N75-23853, 1975.

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17. Renaud, D.P., R.J. Ashton. "Failure Analysis Techniques Used to Physically Isolate LSI Circuits," Proc. Advanced Tech. in Fail. Analy. Symp., 1979, pp. 177-184.

18. Libove, C. "Rectangular Flat-Pack Lids Under External Pressure," RADC-TR-76-118, May 1976.

19. Libove, C. "Rectangular Flat-Pack Lids Under External Pressure: Improved Formulas for Screening and Design," RADC-TR-76-291, Sept. 1976.

EQUIPMENT

MOS Static Protection.

1. VELOSTAT Product Line

a.	Grounding strap with cord	$7 ea.
b.	Floor Mats	$30 - $100/sq.ft.
c.	Conductive foam	$30 - $70/sq.yd
d.	A full product line of conductive accessory products, price available on request.	

3M Company, Nuclear Prod. Div., St. Paul, MN

Microscopes. See Chapter III-M

Curve Tracer.

1.	576 Curve tracer with standard test fixture	$5975
2.	577/D1 storage curve tracer main frame	$3495
3.	577/D2 nonstorage curve tracer main frame	$3025
4.	177 standard test fixture for 577	$ 695
5.	178 linear IC test fixture for 577	$1860
6.	C95 camera and adapter	$ 910

Tektronix Company, Beaverton, OR

Power Supplies.

1.	LL series, single supply	$ 163
2.	LD series, dual supply	$ 480

LAMBDA Electronics, Melville, L.I., N.Y.

Multimeters.

1.	Model 2480/2480R Digital Multimeter	$ 245

Data Precision Corp., Wakefield, MA

2.	Model 3476A Digital Multimeter	$ 320

Hewlett-Packard, Palo Alto, CA

Oscilloscopes.

1.	Model 5440 with dual trace plug in	$2080

Tektronix Co., Beaverton, OR

2.	Model 180D with dual trace plug in	$2750

Hewlett-Packard, Palo Alto, CA

EQUIPMENT

Pulse Generators.

1.	Model 10526T hand held logic pulser	$ 115
2.	Model 8011A bench top generator Hewlett-Packard, Palo Alto, CA	$ 650

Automatic Test Equipment.

1.	S-3000 series system	$20,000 - $30,000
2.	S-3200 series system Tekronix Co., Beaverton, OR	Price depends on options

Bench Top Logic Test Equipment.

1.	Model 545A hand held logic probe with tip	$ 155
2.	Model 548A logic clip	$ 125
3.	Model 5045A digital IC test system Hewlett-Packard, Palo Alto, CA	$10,000 - $15,000
4.	Model P6401 hand held logic probe with tip Tektronix Co., Beaverton, OR	$ 105
5.	Model 308 Data Analyzer Sony/Tektronix Co., Beaverton, OR	$3000
6.	Model 7D01 Logic Analyzer	$3520
	a. DF1 Display Formatter	$1530
	b. DF2 Display Formatter	$2140
	c. DL2 Digital Latch	$1650
	d. 7603 Oscilloscope	$2260
	e. DD501 Digital Delay	$ 850
	f. R6501 Ramp Generator	$ 375
	g. DL502 Digital Latch	$1480
	h. WR501 Word Recognizer Tektronix Co., Beaverton, OR	$1650

Temperature Stress Equipment.

1.	"The Mite" hand held heat gun Master Appliance Corp., Racine, WI	$ 65
2.	MS-240 "Quik-Freeze" Miller-Stephenson Chemical Co., Los Angeles, CA	$ 3.18
3.	Model CO-160C-1 environmental chamber Blue M Electric Co., Blue Island, Ill.	$2500

Package Stress Equipment.

1.	Vibration Systems Unholtz-Dickie Corp., Hamden, Conn.	$5000 - $100,000
2.	Shock Systems Avco International, Cincinnati, OH	$2000 - $20,000

EQUIPMENT

Micromanipulator Test Station.

1.	6000 series base	$7315 - $8500
2.	Microscope	$ 633 - $2500
3.	Camera	$1200 - $1600
4.	Eye pieces, light sources, etc.	$ 400 - $ 800
5.	Micromanipulators with magnetic base	$165 ea.
6.	Ultrasonic probe The Micromanipulator Co., Escondido, CA	$2450

Capacitance-Voltage Apparatus.

1.	Model 868-1T C-V plotter, capacitance meter heat controller, heated chuck, and probe MSI Electronics Inc., Woodside, N.Y.	$8300

B.

RADIOGRAPHY TECHNIQUES

B. Radiography Techniques.

1. X-RAY RADIOGRAPHY.

a) Introduction. Radiography is a non-destructive testing method whereby a material or an assembly is subjected to penetrating radiation and the resulting image is produced on a screen or a photographic film. This radiograph is a shadow image which records differences in density brought about by the internal material variations in the object being examined.

This method of inspection is one of the means best suited to examine the internal condition of sealed electronic packages. It allows one to view internal leads or connections, their configuration, spacing and clearance, and the presence of any loose particles or those that possibly could break loose under shock or vibration. The only limitation is that the density and thickness be sufficient to record.

Producing a radiograph of an object necessitates the use of an X-ray or gamma ray source and a recording screen or film. The radiation obeys the laws of light; therefore, for the image to be of the same size as the object, the film is placed close to the object and the radiation source as far from the film as practical. You normally wish to produce a sharp image, and to accomplish this the radiation source should be small, the distance from the object to film should be minimal and the source to object distance should be great. Image distortion should be negligible which entails that the object and film should be parallel and that the radiation beam be perpendicular to the film.

The target which is bombarded by the electrons establishes the focal spot and is usually set at an angle. The projected size of this beam is the effective focal spot. Ideally, this focal spot would be a point source but in practice it does have a size limitation (See Figure 1).

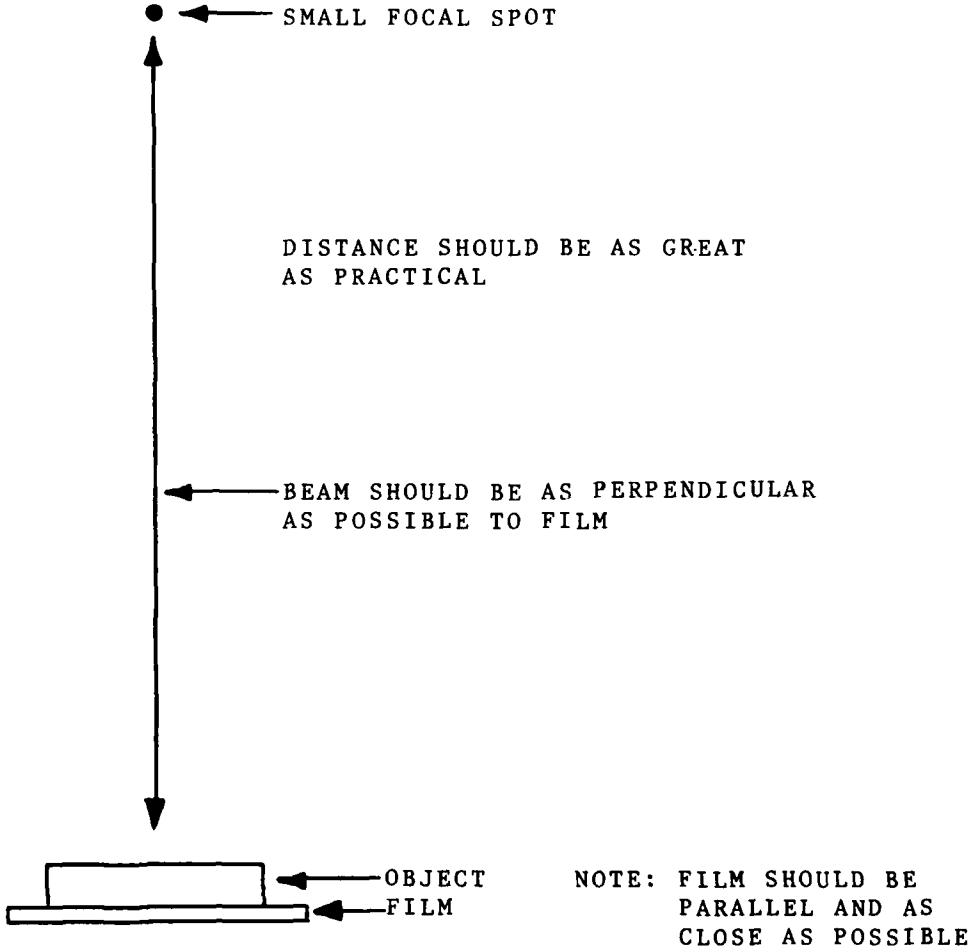


FIGURE 1. GRAPHIC SUMMARY OF X-RAY RADIOGRAPHY

1) Generation of X-rays. The most feasible generator of radiation in this application is X-rays. The intensity of the beam which varies inversely with the square of the distance from the source is dependent upon the number of available electrons which is proportional to the flow of electrons through the tube which can be expressed in milliamperes. This proportion establishes tube current as one of the exposure constants in radiography.

The radiation from an X-ray tube generates both characteristic and continuous rays. The characteristic rays are determined by the target material but the continuous waves which cover a wide band of wavelengths are the ones used in radiography. An increase in voltage will produce more energy which in turn produces X-rays of shorter wavelength which have greater penetration, and a variation in tube current varies the intensity of the beam but the wavelength is unchanged.

2) X-ray Film. To obtain good resolution which is required for this application, it is necessary to utilize a fine grain film which in turn means a relatively slow film speed. The speed of the film in turn is measured by the exposure required to obtain a desired film density. The density range used for transistors and rectifiers is approximately 2.

3) Film Processing. The exposed film can be either processed manually in tanks or by the use of an automatic processor if volume is sufficient.

In manual processing, cleanliness must be maintained, processing time adhered to within prescribed limits, solution temperatures and concentration followed. The tanks must be of sufficient depth whereby the film can be vertically suspended and of sufficient width to allow the solutions to totally incompass the film with allowable space to prevent contact with either the walls of the tank or adjacent film.

In automatic processing, all the required steps are performed mechanically and when the processor is properly maintained produces higher quality radiographs.

4) Penetrometers. A penetrometer is a device which is placed on the film and whose image on a radiograph is used to determine radiographic quality level or sensitivity. For electronic components, one usually employs what is known as an Image Quality Indicator (IQI) which is illustrated in Figure 2 and Table I. These penetrometers are made with increasing thicknesses of steel shim stock to match the thickness of the device enclosure. They contain tungsten wires and lead particles of varying diameters to enable one to measure distortion and to determine sensitivity. The distortion is defined as:

$$\text{Percentage distortion} = \frac{S_0 - S_1}{S_0} \quad 100$$

Where S_0 = actual wire spacing
S_1 = wire spacing as it appears on the film.

5) Safety. Paramount in the use of X-ray are safety precautions that must be strictly followed. Radiation cannot be detected by human senses and can be damaging to tissue. Safety interlocks must be employed which isolate the shielded area where exposures take place. Radiation surveys of the exposure room must be made periodically. Operators and/or personnel in close proximity to the radiation source must use film badges or pocket dosimeters to monitor possible exposure levels. The area should also be marked with warning labels to alert people that they are entering a radiation area.

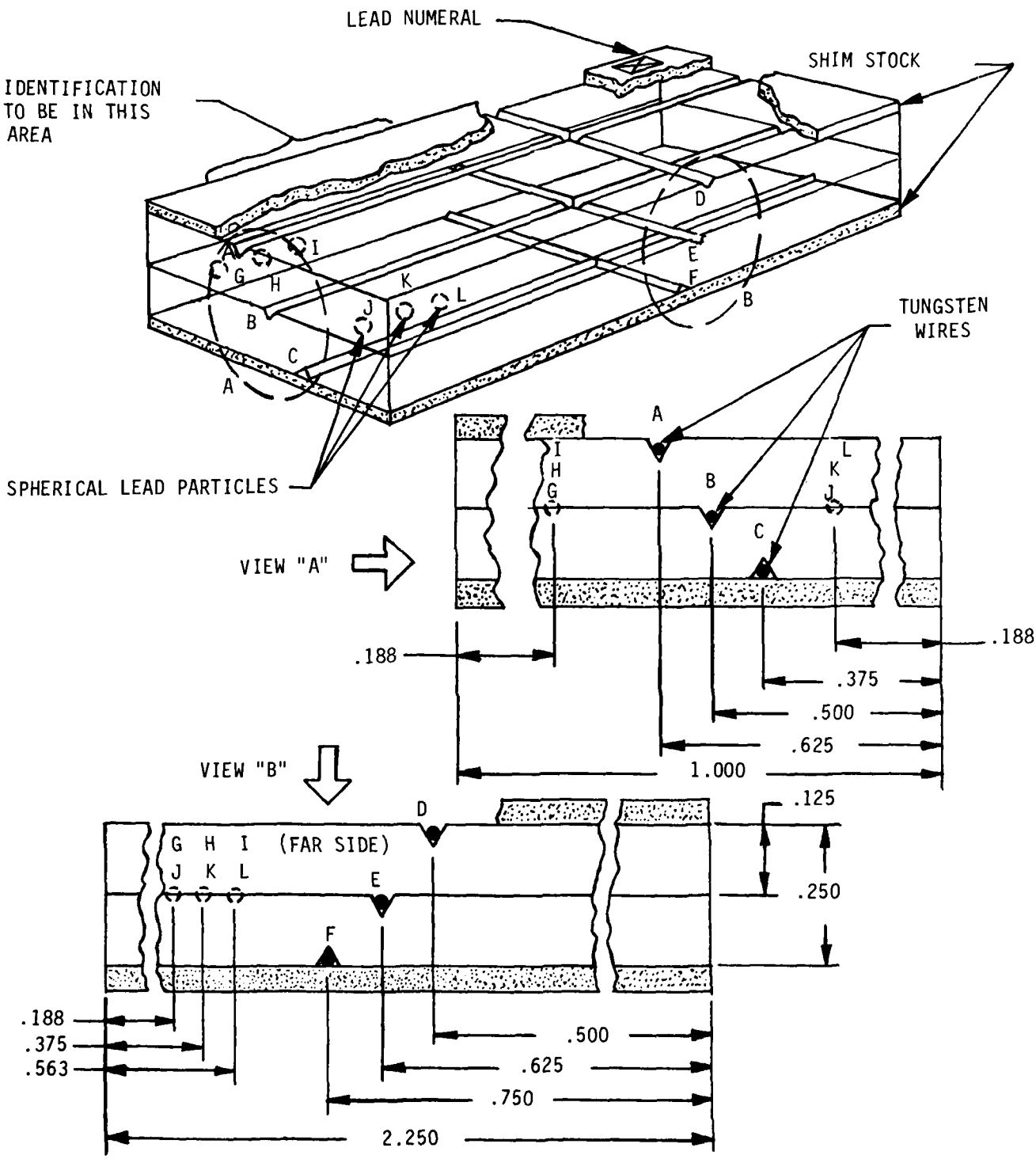


FIGURE 2. IMAGE QUALITY INDICATOR

TABLE I. INTERNAL WIRE DIMENSIONS

PEN (IQI) NO.	TUNGSTEN WIRE DIAMETERS						LEAD PARTICLE DIAMETERS						STEEL SHIM STOCK
	A	B	C	D	E	F	G	H	I	J	K	L	
1	.002	.001	.0005	.0005	.001	.002	.015	.010	.008	.006	.004	.002	NONE
2	"	"	"	"	"	"	"	"	"	"	"	"	.002
3	"	"	"	"	"	"	"	"	"	"	"	"	.005
4	"	"	"	"	"	"	"	"	"	"	"	"	.007
5	.003	.002	.001	.001	.002	.003	"	"	"	"	"	"	.010
6	"	"	"	"	"	"	"	"	"	"	"	"	.015
7	.005	.003	.002	.002	.003	.005	"	"	"	"	"	"	.025
8	"	"	"	"	"	"	"	"	"	"	"	"	.035

NOTES:

1. Wires to be tungsten, shim stock to be carbon steel, particles to be lead. Center section to be 1/8" layers of clear acrylic plastic, bonded with clear plastic cement of low X-ray density. Fasteners may be used within 0.250 or less from each corner but shall not interfere with end use of the penetrometer. Bottom surface shall be flush.

2. All dimensions shown are $\pm$ 0.005, except wires, and shim stock, which shall be within standard mill tolerances and lead particles which shall be $\pm$ 0.0002. Groove details are not critical except that wire must be embedded flush or below surface of plastic and centered at location shown. Particle-hole sizes are not critical but should not exceed 1/32" in diameter and depth and must be centered as shown ($\pm$ 0.005).

3. Additional layers of shim stock may be used as necessary.

4. Identification marking shall be permanent and legible. Location and size of characters is not critical but shall not interfere with or obscure the radiographic image details.

b) Standard Single Radiographs. In X-raying electronic components, the following criteria are usually employed :

- o KV should not exceed 150
- o Beryllium window in tube
- o Maximum focal spot of 3.5 millimeters
- o Focal film distance shall be at least 36 inches
- o Very fine grain single emulsion film
- o Capability of detecting particles of 0.001 inches (25.4 μm)
- o Film density of 1.8 to 2.5
- o Distortion shall not exceed 10 percent
- o Radiograph examination at a minimum of 10X

When exposing a single package or component, it is placed directly in the center of the beam with the specimen placed on the film which rests on a lead topped surface to minimize backscatter. Penetrometers are placed at opposite corners of the film.

If a number of items are to be exposed, it is important that each item in the X-ray beam fall on the circumference of a sphere whose diameter is determined by the target to film distance. Any deviation from this results in distortion of the X-ray image at the positions of the film which are not at the proper distance from the target.

This requirement means that an adjustment must be made for the curvature of the desired target to film distance according to Table II.

By the utilization of the standard 7 x 17 inch film size, the correction needs only to be made in the longitudinal direction which is easily accomplished by a properly formed sheet.

TABLE II

TARGET-TO-FILM DISTANCES

Perpendicular Distance from Centerline of X-Ray Beam, Inches	Displacement of 36" Curve from Perpendicular, Inches	Displacement of 48" Curve from Perpendicular, Inches	Difference Between 36" and 48" Curves, Inches
Centerline	Tangent	Tangent	Zero
1	.014	.009	.005
2	.05	.04	.01
3	.13	.10	.03
4	.22	.17	.05
5	.35	.26	.09
6	.50	.37	.13
7	.67	.51	.16
8	.88	.66	.22
9	1.11	.85	.26
10	1.36	1.02	.34

NOTE: Actual tests indicate that displacement limits for distortion-free images fall at about 0.250". Therefore, correction is required for distances of about 4.5" off the beam center. Correction for differences in curvature between 36" and 48" target distances is required when the film is about 9" off the beam center line.

1) Defect Types. The following defects are readily discernible and can be cause for rejection or further analysis.

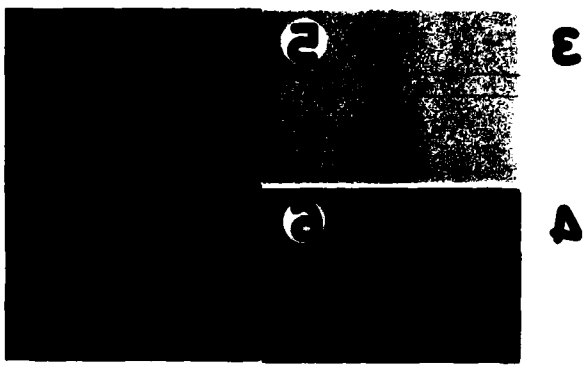
- o Expulsion
- o Poor Lead Connection (Broken, sharp bends, divided)
- o Missing Component Part
- o Metallic Particles
- o Extraneous Metal
- o Cracked Lead
- o Non-uniformity
- o Tilted Pellet
- o Contamination
- o Inadequate Clearance
- o Improper (voided) package lid seals/lead seals

It is also essential in some types of devices to X-ray in two or three directions to insure that defects are not masked by the internal construction.

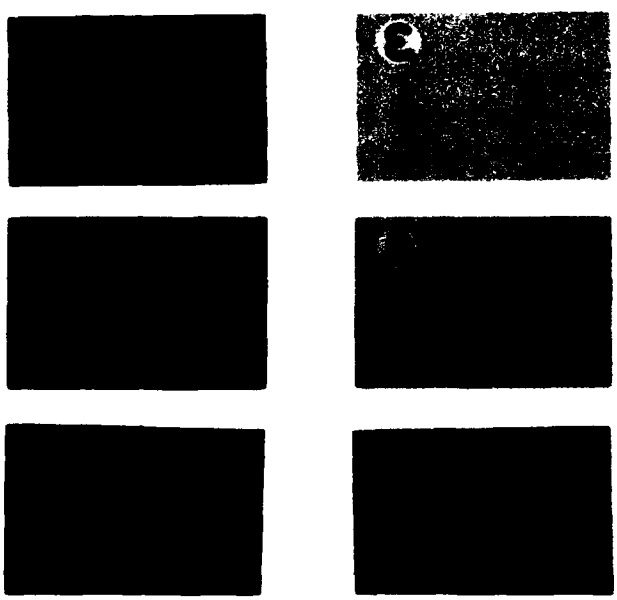
2) Typical Defects. ASTM E431 depicts defects for a number of packages which can be used for the interpretation of radiographs of semiconductors and related devices. See Figures 3, 4 and 5.

3) Sample Radiographs. Radiographs 1 and 2 show respectively Image Quality Indicators on X-ray and Polaroid Type 55 film. They demonstrate the approximate detail which can be expected with each of these films. Precise minute detail is lacking in the Polaroid Type film but it can be satisfactory for viewing gross defects.

Radiograph 3 shows foreign particles in a diode. This radiograph is a direct print from the film so the densities are reversed.



RADIOGRAPH 1. IMAGE QUALITY INDICATOR ON X-RAY FILM

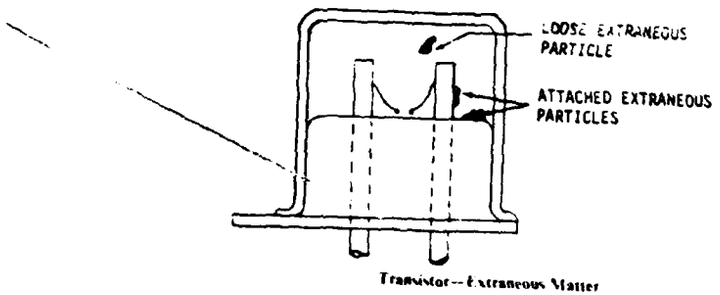


RADIOGRAPH 2. IMAGE QUALITY INDICATOR ON POLAROID FILM

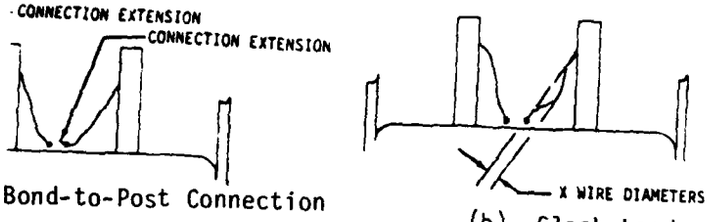
RADIOGRAPH 3. RADIOGRAPH OF PARTICLES IN DIODE

4) Typical Exposures. Nominal exposures for typical electronic devices are given below for a 48-inch target to film distance realizing that all X-ray units have some variation.

PART	Accel. Potential in KV	Beam Current in MA	Exposure TIME(MIN.)
Diodes	130	6	2
T05	120	6	3
Rectifiers (7/16)	140	6	6
Relays	140	6	6

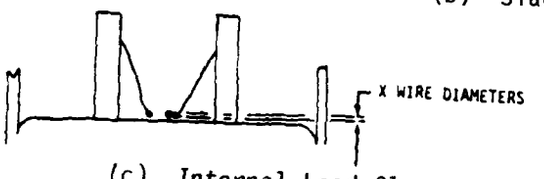


Transistor – Extraneous Matter



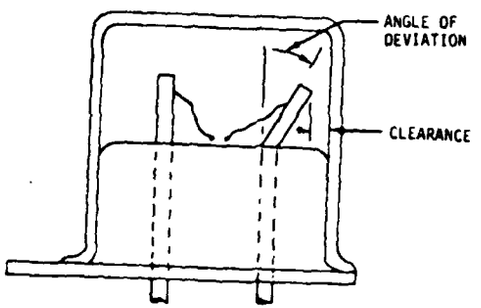
(a) Bond-to-Post Connection

(b) Slack Leads

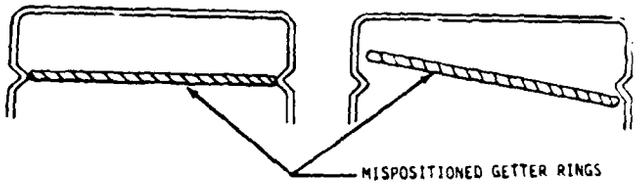


(c) Internal Lead Clearance

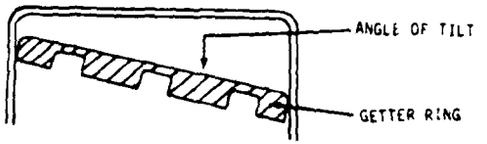
Transistor – Internal Lead Irregularities



Transistor – Post-Position Irregularities

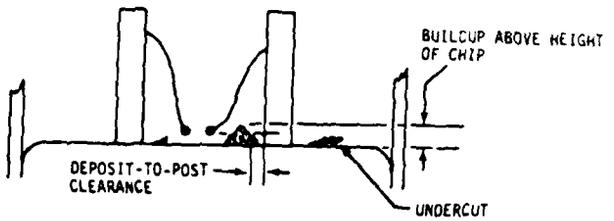


(a) Crimp Type

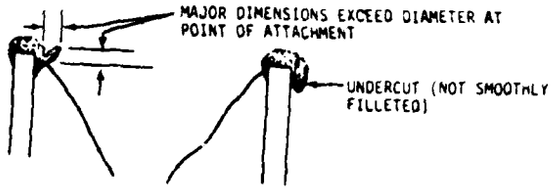


(b) Non-Crimp Type

Transistor – Getter Position Irregularities

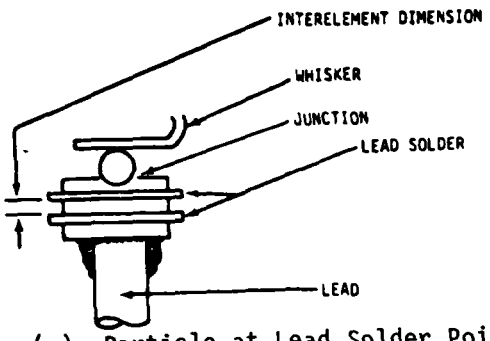


Transistor – Mounting Paste Buildup or Expulsion or Both

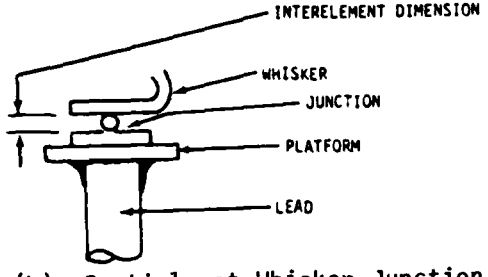


Transistor – Post-Connection Solder or Paste Buildup

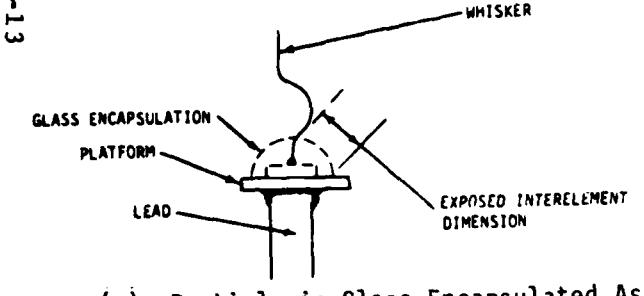
FIGURE 3. TYPICAL DEFECTS REVEALED THROUGH RADIOGRAPHY



(a) Particle at Lead Solder Points

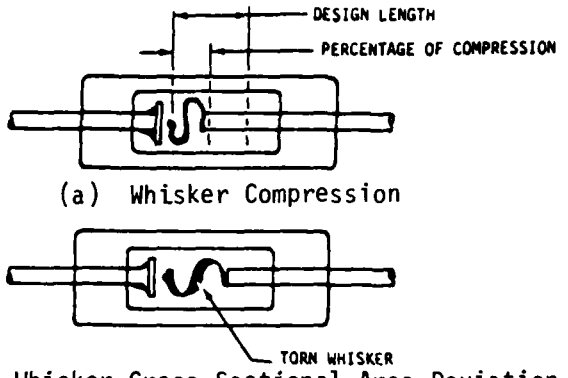


(b) Particle at Whisker Junction



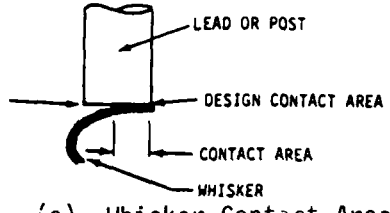
(c) Particle in Glass Encapsulated Assembly

Diodes, Low-Power Rectifiers (Whisker-Type)—Extraneous Matter



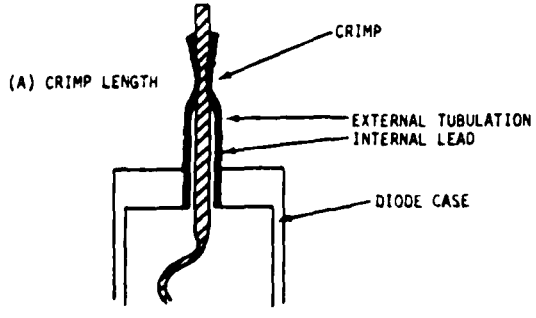
(a) Whisker Compression

(b) Whisker Cross-Sectional Area Deviation



(c) Whisker Contact Area

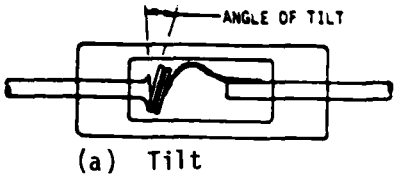
Diodes, Low-Power Rectifiers (Whisker-Type)—Whisker Irregularities



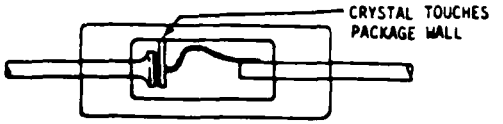
Diodes, Low-Power Rectifiers (Crimped Lead Devices)

This standard is subject to revision at any time by the responsible technical committee and must be reviewed every five years and if not revised, either reapproved or withdrawn. Your comments are invited either for revision of this standard or for additional standards and should be addressed to ASTM Headquarters. Your comments will receive careful consideration at a meeting of the responsible technical committee, which you may attend. If you feel that your comments have not received a fair hearing you should make your views known to the ASTM Committee on Standards, 1916 Race St., Philadelphia, Pa. 19103, which will schedule a further hearing regarding your comments. Failing satisfaction there, you may appeal to the ASTM Board of Directors.

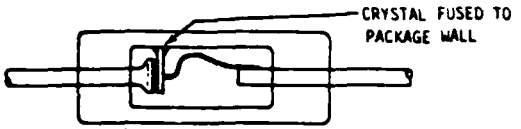
FIGURE 4. TYPICAL DEFECTS REVEALED THROUGH RADIOGRAPHY



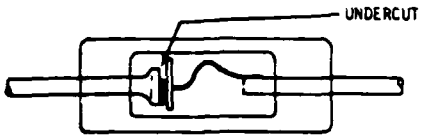
(a) Tilt



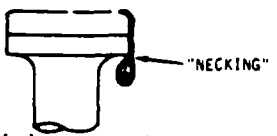
(b) Clearance



(c) Clearance

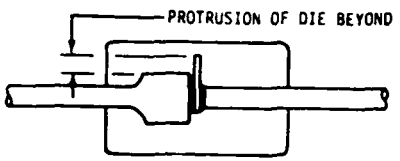


(d) Fusion

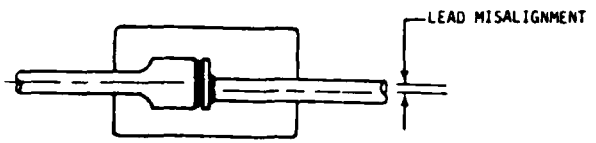


(e) Mounting Paste Expulsion

Diodes, Low-Power Rectifiers (Whisker-Type) – Crystal and Crystal Mounting Irregularities

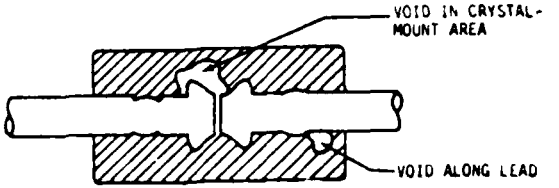


(a) Crystal Misalignment

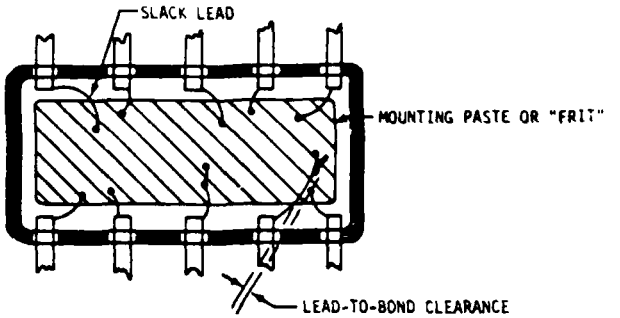


(b) Post Misalignment

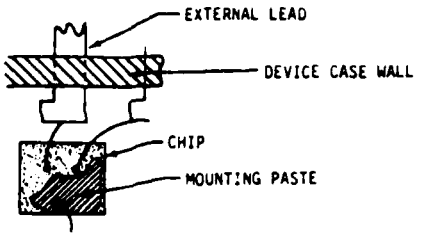
Diodes and Low-Power Rectifiers (Whiskerless-Type) – Misalignment



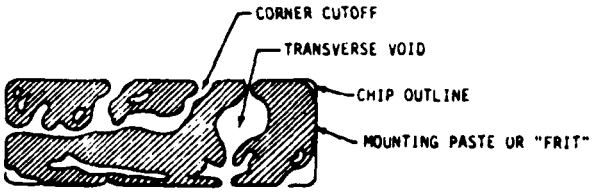
Diodes and Low-Power Rectifiers (Whiskerless-Type) – Voids



Integrated Circuits – Internal Clearances



(a) Mounting Paste Area



(b) Typical Voiding Configurations

Integrated Circuits – Chip Mounting

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FIGURE 5. TYPICAL DEFECTS REVEALED THROUGH RADIOGRAPHY

c) Stereo Radiographs. There are methods available to determine the depth of a flaw or the location of a defect within a section by the utilization of stereo radiography. A single radiograph shows no perspective since the entire view is a single plane, however. By double exposing a film or by the use of two films and a stereoscope, depth can be ascertained.

1) Double Exposure Method. Double exposure methods of determining flaw depth in a specimen are based on physical measurements of the radiographic image and do not depend on depth perception. One such method is illustrated in Figure 6. Lead markers M_1 and M_2 are respectively attached to the front and back surfaces of the specimen. Two exposures, each one approximately one-half the time required for a normal exposure, are made. The distance between F_1 and F_2 is predetermined, and the tube is located at F_1 for one exposure and at F_2 for the other. The position of the film image of the flaw and of M_1 will perceptibly change as a result of the tube shift, while the M_2 image shift will be small if not imperceptible. The distance of the flaw from the film plane is determined by the following equation.

$$d = \frac{bt}{a + b}$$

where d = distance of the flaw from the film plane
a = distance of tube position shift
b = change in position of the flaw image
t = focus-film distance

o If film fog, or the small size of the flaw, does not permit use of the double exposure technique, two separate radiographs may be made. The two radiographs are aligned by superimposing images of the M_2 markers, the change in position of the flaw image is measured, and the foregoing equation is applied.

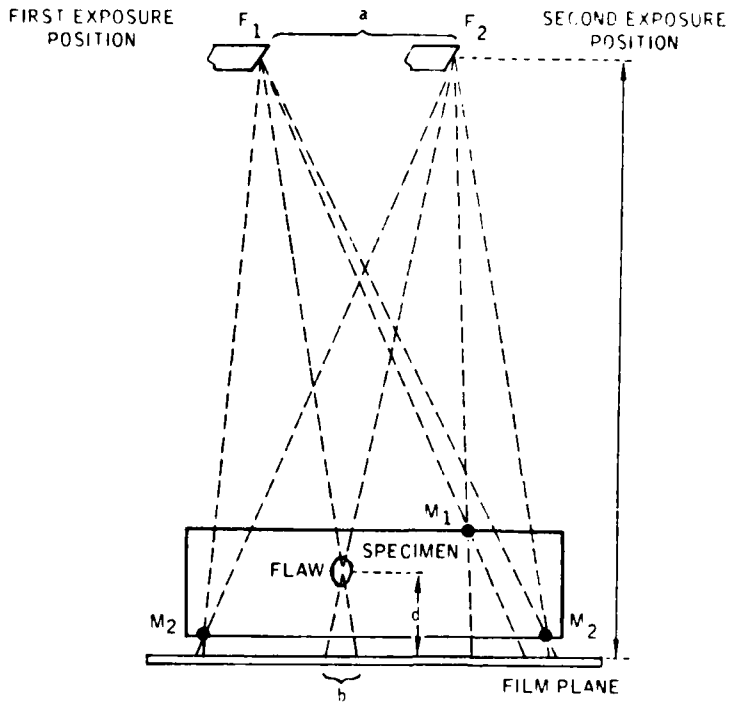


FIGURE 6. EXPOSURE POSITIONS

o For flaw depth determination when all that is required is knowledge of which specimen surface the flaw is nearer to, the relationship between the image shift of the M_1 marker and the image shift of the flaw provides the answer. If the flaw image shift is greater than half the shift of the M_1 image, the flaw is nearer the top surface of the specimen; if less than half, the flaw is nearer the bottom surface.

2) Stereoradiography. Stereoradiography gives the viewer a three-dimensional effect by use of two radiographs of the specimen and a stereoscope. The two radiographs are made with two different positions of the X-ray tube in relation to the specimen. The two positions are displaced from each other by a distance equal to the separation of a human's eyes. The stereoscope, through optical means, permits the viewer to view the two radiographs simultaneously while allowing each eye of the viewer to see only one of the radiographs. The right eye sees the image of the right shift position of the X-ray tube, and the left eye sees the image of the left shift position. The brain combines and merges the two images into one in which true perspective and spatial relationships are apparent. Stereography is little used in industrial radiography but is of value in flaw location or structural visualization (See Figure 7).

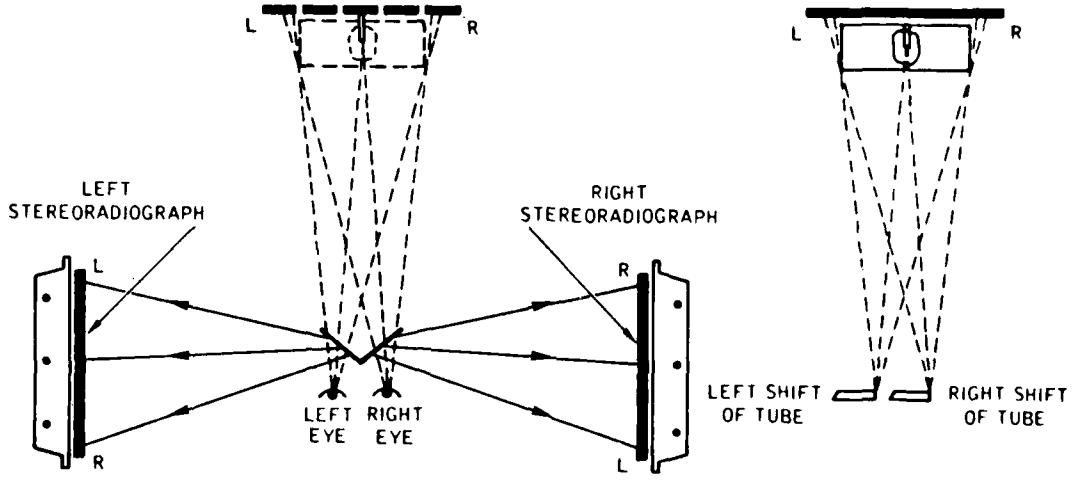
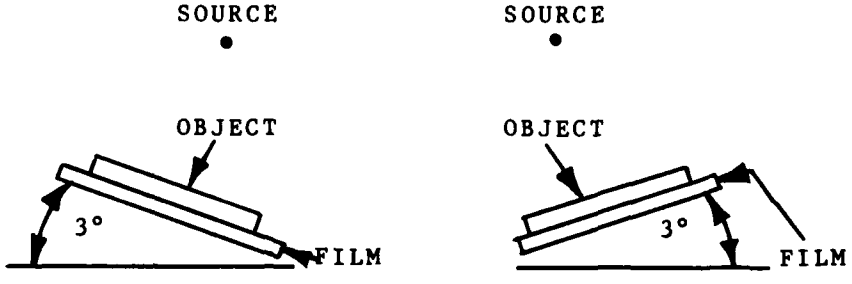


FIGURE 7. STEREOSCOPIC RADIOGRAPHY

3) Object Tilting. Another method makes use of tilting the object being radiographed approximately 3 degrees in each direction rather than moving the tube head and making the exposure. Viewing the two radiographs side by side under a stereomicroscope will allow one to view in three dimensions.



1 2

d) Video Monitor Systems. Methods have been developed using X-r· sensitive vidicon tubes rather than film to obtain radiographic images. In this system, the vidicon tube is placed behind the object and the image is transmitted to a remote receiver where viewing takes place. The image is not only reproduced but also magnified up to 50 diameters and resolution of 10 microns and high contrast sensitivities have been reported.

A typical system is illustrated in Figure 8 with the following schematic of the vidicon tube under the specimen shown in Figure 9.

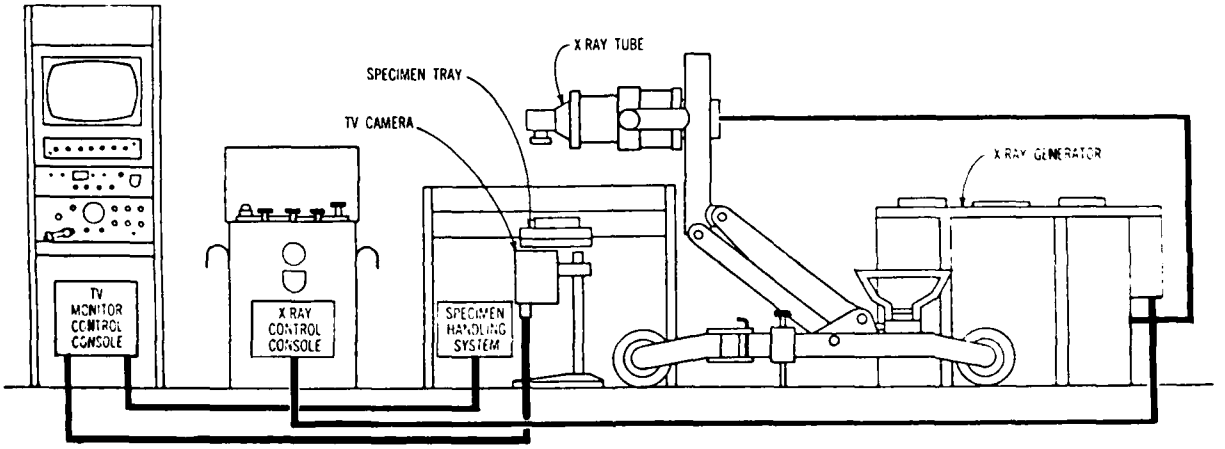


FIGURE 8. VIDEO MONITOR SYSTEM

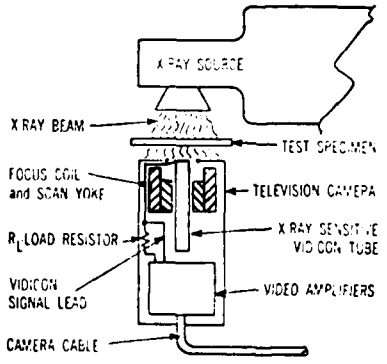


FIGURE 9. DETAILS OF VISUAL SIGNAL GENERATION

The three major components required are:

- o X-ray source and controls
- o Positioning and handling system for the test specimen
- o Closed circuit X-ray television system

1) X-Ray Source. The optimum image contrast and detail are obtained by the utilization of a very high intensity, a fine focal spot and a low inherent filtration of the X-ray source. The best performance has been obtained with a 150 kilovolt - constant potential source with fractional focus targets and beryllium windows. Such sources are commercially available with focal spot sizes as small as 0.4 mm.

High radiation outputs are required to provide high signal to noise ratios in the video signals from the vidicon tube and preamplifiers. The small focal spot is required to produce sharp images on the photoconductive layer of the vidicon tube and the beryllium window in the X-ray tube is needed to provide high specimen contrast.

2) Specimen Handling Unit. To enable one to selectively move the test specimen to desired areas of interest, precision movements in the X and Y direction must be attainable. The specimen must be located in the incident X-ray beam and as close as feasible to the vidicon tube surface, less than 1/8 of an inch. Distance from the X-ray source to the test specimen is relatively short, typically 5 to 10 inches rather than the 36 to 48 inches common with X-ray film. To permit variable scanning, controls must be provided to allow one to adjust specimen position from the remote viewing station to bring into view the various areas of the specimen which is subject to examination.

3) Television System. The main components of this system are the vidicon tube, the power supply, synchronizing and control unit and the monitoring screen. The viewing or control area contains all the necessary adjusting controls for X-ray kilovoltage, television current and contrast controls and positioning controls for the test specimen.

The X-ray image is transmitted through the vidicon window into a photoconductive layer. This layer is scanned by an electron beam, and capacitive coupling between the target face and signal plate produces a video signal that is amplified and transmitted to the monitor screen. The image area on the vidicon tube is relatively small; therefore, the enlargement or magnification is dependent on the monitor tube size.

The entire system should be of high quality and capable of continuous operation over extended time periods to minimize down time and component deterioration.

e) Photographic and X-ray Films. Radiographic films consist of a layer of an emulsion containing a silver compound coating one or both sides of a sheet of a cellulose derivative film. This emulsion is extremely sensitive to the amount of light or radiation to which it is exposed. After exposure and developing, it will produce an image whereby the density varies with the amount of radiation to which it has been subjected.

There are a number of manufacturers who produce different types of industrial film and the type used depends on the application or the specific results desired. These different types vary in sensitivity to radiation, which is film speed, and in quality of the image, which is grain size and contrast.

Sensitivity is the ability of the X-ray technique to reveal slight variations in density on the film and is determined by the contrast and definition. The radiographic contrast is the difference between the film densities of different areas on the film that depends upon the subject and film contrast. The definition is the sharpness of detail of the image.

Some facilities have used Polaroid film for radiographic purposes and have obtained varying results. They have employed Polaroid Type 52, 57 and Type 55 P-N. Using this method, darkroom facilities are not required but the resolution is questionable since resolution and contrast of these films are limited. For rapid evaluation of gross defects, however, this method does have merit.

In the application of the examination of microelectronics, it is essential to utilize a film that has an ultra fine grain even though the exposure time increases considerably. This is necessary because the finer the grain the higher the radiographic detail which is essential to differentiate small variations in density. It is also preferable to utilize a single coated film to avoid paralax because the film is ordinarily viewed under magnification to determine if any discrepancies exist.

We have utilized either KODAK R or GEVAERT-D2 for these types of applications. Both film types have a low speed but very high contrast and the finest possible grain. It is used with low or normal tube voltage where the finest possible rendering of detail is required.

FILM RATING

RATING	FILM TYPES				
1	KODAK R	or	GEVAERT	D2	- SINGLE EMULSION
2	" M		"	D4	
3	" T		"	D5	
4	" AA		"	D7	
5	POLAROID				

Decreasing image quality with increasing rating.

f) Photographic Darkroom Facilities.

1) Dark Room. This facility is usually divided into three distinct areas of operation and can be one large room or, if volume is large, individual adjoining compartments. One is usually a film storage area and work space where film cassettes are loaded and unloaded. The second is the processing section where the film is developed and washed, and the third will be the film drying area. Because of the heat involved in the last process, this area is usually somewhat removed from the processing area. Also a viewing room is needed where the finished radiographs are evaluated, and this area should have some control of lighting for proper viewing.

2) Manual Processing. The darkroom facility required for film processing must contain proper timers, safelights and controls to prevent fogging of the film. It is also essential to have precise temperature control of the solutions since time and temperature of the developing process must be strictly controlled.

The first three steps are normally carried out in a large temperature controlled water bath which contains the tanks, one each for the developer, stop bath fixer and a wash tank where the film is immersed in running water and held for a period of time equal to twice the fixing time. It is then placed in a wetting

agent to decrease the possibility of water marks and then dried.

The processing tanks must be made of a material able to withstand the chemical action of the solutions, not only to prevent any corrosion of the tanks but also so the solutions do not become contaminated. Cleanliness is paramount throughout the developing process, which entails that all tanks, film holders and related equipment be scrupulously clean.

It is essential that the level of developer solution be kept constant and therefore must be replenished periodically. This is necessary because of the dragout of the solution when changing the film from one tank to the next and also to replace the solution utilized on initial immersion.

To obtain uniformity of development, it is also necessary to agitate the film during the development state. This should be done not only to dislodge air bubbles which can retard developing but also to prevent reaction products from adhering to the lower portions of the film.

Film Processing Procedure.

- o Stir solutions
- o Check temperature
- o Load film on hanger
- o Set timer
- o Immerse film in developer
- o Agitate film
- o Drain outside developer tank
- o Place in stop bath
- o Fix adequately
- o Wash completely
- o Final rinse in Photo-Flo
- o Place in drier

3) Automatic Processing. If the volume of work is relatively high, processing automatically can be beneficial because not only is less manpower needed but more consistent and higher quality radiographs are produced. The only manual steps involved are the loading and unloading of the film from the machine. The process is rapid, and the dried film can be viewed within 15 to 20 minutes.

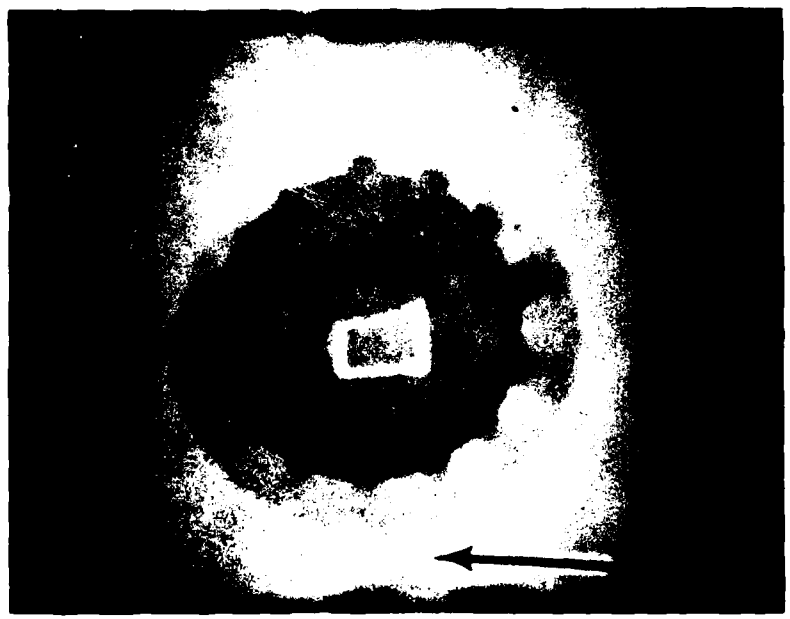
The film processing procedure in a machine is similar to those performed manually but special solutions, higher temperature, continual agitation and forced drying with heated air complete the process in a relatively short period of time and eliminate the human element.

4) Inexpensive X-ray Facility. The Faxtron Model 804 offers an inexpensive capability for the laboratory involved in only occasional use of X-ray radiographs of small electronic components. Figure 10 illustrates the small size and simple controls on the Faxtron equipment. A typical Faxtron X-ray is shown in Figure 11 illustrating a glass void in a flatpack package.

2. NEUTRON RADIOGRAPHY.

a) Introduction. Radiography with neutrons began shortly after the discovery of the neutron in 1932. The initial experiments in neutron radiography were performed in Germany in the late 1930's by H. Kallmann and E. Kuhn. A major advantage of using neutrons for radiography is that radiographic observation of certain material combinations is easy with slow neutrons but, because of attenuation differences, problems will arise with X-rays. For example, the high attenuation of slow neutrons in elements, such as hydrogen, lithium, boron, cadmium, and several rare earths means that these materials can be readily shadowed with neutrons even when they may be combined in an assembly with some high atomic weight material such as steel, lead, bismuth or uranium. Although, the heavy material would make

FIGURE 10. INEXPENSIVE X-RAY FACILITY (COURTESY OF FAXTRON)



HERMETICITY REJ.

FIGURE 11. TYPICAL FAXTRON X-RAY PACKAGE GLASS VOID

X-radiography difficult, neutron radiography should yield a successful inspection. Further, the differences in slow neutron attenuation often found between neighboring materials in the periodic table offer an advantage for neutron radiographic discrimination between materials that have similar X-ray attenuation characteristics. This advantage is illustrated in Figure 12, in which the mass-attenuation coefficients (μ/ρ) are plotted as a function of atomic number of the attenuating element for both X-rays and slow neutrons. Figure 12 demonstrates the differences in attenuation of neutrons and X-rays for the elements. Among the neutron radiographic applications suggested from Figure 12 are those involving hydrogenous and metallic assemblies, such as metal-jacketed explosives, adhesive-bonded assemblies, and components, such as rubber, plastic, wax, or paper in metal assemblies, and hydride deposits in metals. There are three areas of advantage that can be cited for neutron radiography:

- Contrast differences from X-radiography as determined by elemental attenuation differences
- Possibilities for isotopic differentiation
- Capability to radiographically examine highly radioactive material without the film fogging problem one would encounter with conventional radiography

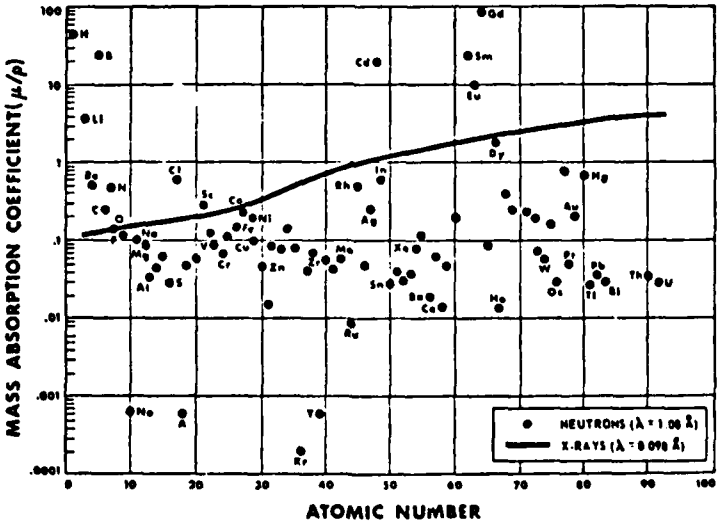


FIGURE 12. A COMPARISON OF MASS ABSORPTION COEFFICIENTS FOR THE ELEMENTS FOR BOTH X-RAY AND THERMAL NEUTRONS (COURTESY ARGONNE NATIONAL LABORATORY)

All of these advantages have led to useful applications for neutron radiography in nondestructive inspections of complex material assemblies. Very limited use of this technique has been made by semiconductor failure analysts.

b) Description of Technique. A neutron radiograph is produced by passing a beam of thermal neutrons (neutrons having energies less than 0.4 eV) which are well collimated through a test object as shown in Figure 13. The neutrons may interact with the atomic nucleus of the material and if they do will either be absorbed or scattered out of the beam. The beam emerges from the test sample containing information about elemental material and internal configuration of the object. The neutrons will not interact directly with the emulsion of the film. Therefore, information in this beam must be transformed into ionizing radiation by a converter plate. This secondary radiation then interacts with the emulsion on the film in much the same manner as X-rays, and an image is produced.

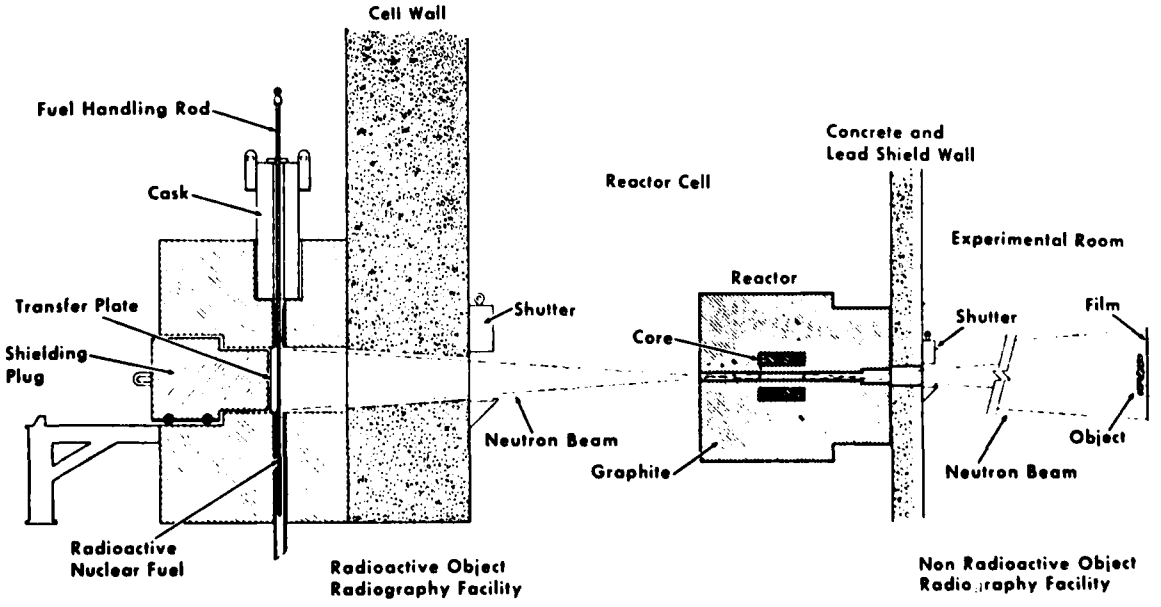


FIGURE 13. NEUTRON RADIOGRAPHY FACILITY

The biggest cause for interest in neutron radiography stems from the wide range in neutron attenuation coefficients. X-ray attenuation coefficients have a range of approximately thirty for any given energy, while thermal neutrons have a range of four hundred thousand. A table of absorption coefficients of the elements for neutrons and X-rays is shown in Table III. The various factors which affect the neutron radiograph sensitivity are shown in Flow Diagram form in Figure 14. Figure 15 is a plot of the resolution uncertainty as a function of part distance from the film.

c) Equipment Required. Early neutron-radiography research took place at various Government laboratories and at General Electric's Vallecitas Nuclear Center. The basic facility used at GE is a 30 kW uranium-fueled, water-cooled reactor. Engineered to produce a very intense, well-collimated beam of thermal neutrons, it is an ideal source of neutrons for radiography. It produces a nearly gamma-free beam having a neutron-to-gamma (mr) ratio of 2×10^5, enabling direct or indirect radiography.

In the early 1970's, neutron radiography was limited to a few, well-equipped centers. However, the availability of low cost neutron sources, such as

- o americium - beryllium - curium (ABC)
- o antimony - beryllium (AB)
- o californium - 252

has encouraged development of portable systems.

d) Cost of Neutron Radiographs. Typical cost for a neutron radiograph is in the range of $40 - 150 each.

e) Examples. The best way to appreciate the unique advantages of the neutron radiograph is to compare the image obtained with thermal neutrons with the same part being imaged using X-rays.

TABLE III

ABSORPTION COEFFICIENTS OF THE ELEMENTS FOR NEUTRONS AND X-RAYS

Element	Neutrons (λ = 1.08 Å)		X-Rays (λ = 0.098 Å)	
	(μ/ρ) total	μ total	μ/ρ	μ
Hydrogen	48.5		0.280	
Lithium	3.7	2.0	0.125	0.067
Beryllium	0.52	0.92	0.131	0.24
Boron	24‡	60‡	0.138	0.35
Carbon	0.26	0.60	0.142	0.33
Nitrogen	0.48		0.143	
Oxygen	0.15		0.144	
Fluorine	0.11		0.146	
Neon	0.006‡		0.148	
Sodium	0.099	0.097	0.150	0.15
Magnesium	0.093	0.16	0.152	0.26
Aluminum	0.036	0.97	0.156	0.42
Silicon	0.044†	0.10†	0.159	0.37
Phosphorus	0.062†	0.12†	0.162	0.32
Sulfur	0.029	0.058	0.166	0.33
Chlorine	0.59		0.176	
Argon	0.006†		0.184	
Potassium	0.049	0.042	0.191	0.16
Calcium	0.057	0.088	0.200	0.31
Scandium	0.27†	0.68†	0.208	0.52
Titanium	0.119	0.54	0.217	0.98
Vanadium	0.093	0.56	0.227	1.4
Chromium	0.065	0.46	0.238	1.7
Manganese	0.107	0.79	0.250	1.8
Iron	0.141	1.1	0.265	2.1
Cobalt	0.26	2.2	0.287	2.5
Nickel	0.213	1.9	0.310	2.8
Copper	0.095	0.85	0.325	3.0
Zinc	0.045	0.32	0.350	2.5
Gallium	0.015†	0.089†	0.380	2.3
Germanium	0.082	0.45	0.41	2.2
Arsenic	0.076	0.44	0.44	2.5
Selenium	0.132	0.59	0.48	2.2
Bromine	0.074		0.52	
Krypton	0.0002‡		0.56	
Rubidium	0.042	0.064	0.59	0.90
Strontium	0.070	0.18	0.61	1.6
Yttrium	0.0056‡	0.021‡	0.66	2.5
Zirconium	0.047	0.31	0.71	4.6
Niobium	0.044	0.37	0.75	6.4
Molybdenum	0.055	0.55	0.79	7.9
Ruthernium	0.009‡	0.11‡	0.90	11.1
Rhodium'	0.53‡	6.6‡	0.95	11.8
Palladium	0.050	5.7	0.99	11.3
Silver	0.24	2.5	1.05	11.0
Cadmium	11.2‡	97‡	1.09	9.4
Indium	0.60‡	4.4‡	1.13	8.2
Tin	0.027	0.20	1.17	8.5
Antimony	0.037	0.25	1.21	8.1
Tellurium	0.031	0.19	1.25	7.8
Iodine	0.036	0.18	1.33	6.6

TABLE III (CONTINUED)

ABSORPTION COEFFICIENTS OF THE ELEMENTS FOR NEUTRONS AN X-RAYS

	(μ/ρ) total	μ total	μ/ρ	μ
Xenon	0.083‡		1.40	
Cesium	0.109	0.20	1.46	2.7
Barium	0.018†	0.068†	1.52	5.7
Lanthanum	0.063	0.39	1.60	9.8
Cerium	0.014	0.097	1.68	11.6
Praseodymium	0.046	0.30	1.75	11.4
Neodymium	0.21	1.5	1.81	12.6
Samarium	25‡	195‡	1.95	15.2
Europium	10‡	52‡	2.02	10.5
Gadolinium	84‡	497‡	2.08	12.3
Terbium	0.09‡	0.75‡	2.13	17.7
Dysprosium	2.0‡	17.2‡	2.23	19.2
Holmium	0.015‡	1.3‡	2.33	21
Erbium	0.41	2.0	2.40	11.4
Thulium	0.25‡	2.3‡	2.48	23
Ytterbium	0.076‡	0.42‡	2.55	14.0
Lutetium	0.22‡	2.1‡	2.63	26
Hafnium	0.20‡	2.3‡	2.72	31
Tantalum	0.067	1.1	2.80	47
Tungsten	0.058	1.1	2.88	56
Rhenium	0.16‡	3.4	2.95	63
Osmium	0.028‡	0.63‡	3.02	68
Iridium	0.80‡	18‡	3.09	69
Platinum	0.050	11	3.15	68
Gold	0.20	3.9	3.21	62
Mercury	0.71	9.6	3.31	45
Thallium	0.027†	0.32†	3.41	41
Lead	0.034	0.39	3.50	40
Bismuth	0.029	0.28	3.57	35
Thorium	0.033*	0.37*	3.80	43
Uranium	0.028†	0.52	3.90	73
PETN		2.545		0.255
RDX		2.894		0.2666
DIPAM		1.640		0.198
Lead Azide		0.783		12.15
Lead Styphnate		0.6776		2.442
16% B Boron 84% KNO_3 Potassium-Nitrate		8.588		0.344
48% Ti Titanium 52% $KClO_4$ Potassium Perchlorate		0.569		0.607
70/30 57% Zirconium-Nickel 43% $KClO_4$ Potassium Perchlorate		0.618		1.612
Smokeless Powder (Bullseye)		2.15		0.225
Epoxy - Armstrong C-7/W		8.38		0.179
H_2O		5.53		0.150
Lucite		4.80		0.182

*Scattering only. † Incoherent scattering not included. ‡ Scattering not included.

Mass absorption coefficients (μ/ρ) for true, scattering and total attenuation, plus the linear absorption coefficient (μ) are given for thermal neutrons of wavelength 1.08Å. Mass absorption coefficients (μ/ρ) and linear absorption coefficients (μ) are given for X-rays of wavelength 0.098Å. Values are in cm^2/g for μ/ρ and in cm^{-1} for μ.

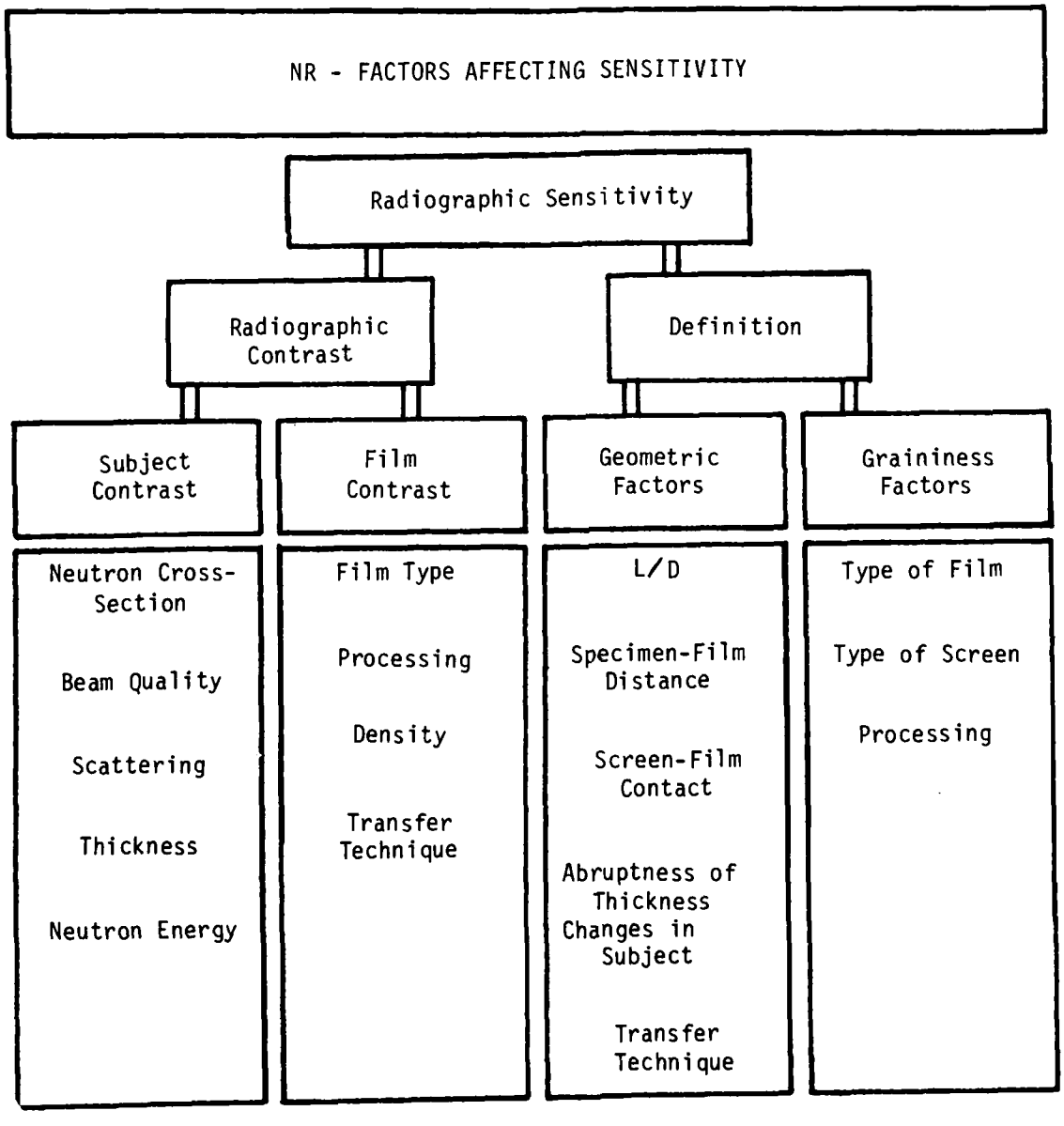


FIGURE 14. NR - FACTORS AFFECTING SENSITIVITY

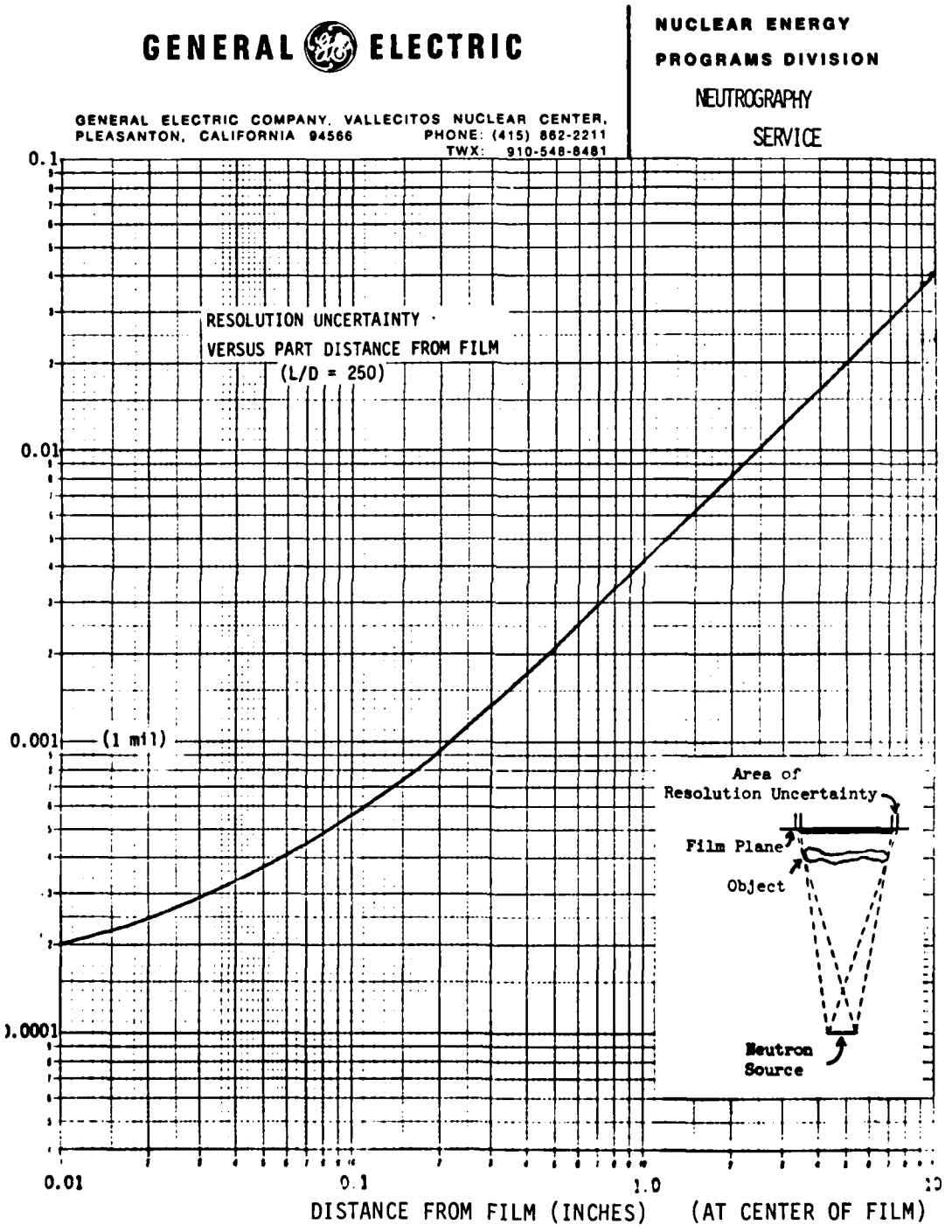


FIGURE 15. RESOLUTION UNCERTAINTY VERSUS PART DISTANCE FROM FILM

A group of component parts representing both electromechanical, electronic, potted assemblies, and printed circuit boards are imaged with X-ray and N-ray for comparison of material details observable with each method. Figure 16 shows the arrangement of the component parts for the radiograph analysis on the aluminum cassettes. Figures 17, 18, and 19 show an assortment of electronic assemblies and components analyzed with both X-ray and neutron radiography for comparisons. Each of these techniques has its own specific use and is somewhat complementary. The particular parameters used for each process are given below:

X-ray Parameters

120 KV at 12 mA for 1 1/2 minutes
distance to test cassette - 11 feet

Neutron Radiograph Parameters

Facility - General Electric 100 KW Nuclear Test Reactor
South Beam Port Neutrography Facility

L/D Ratio = 250
Flux 2 X 10^6 NV (neutrons/cm^2 - sec) for 8 minutes

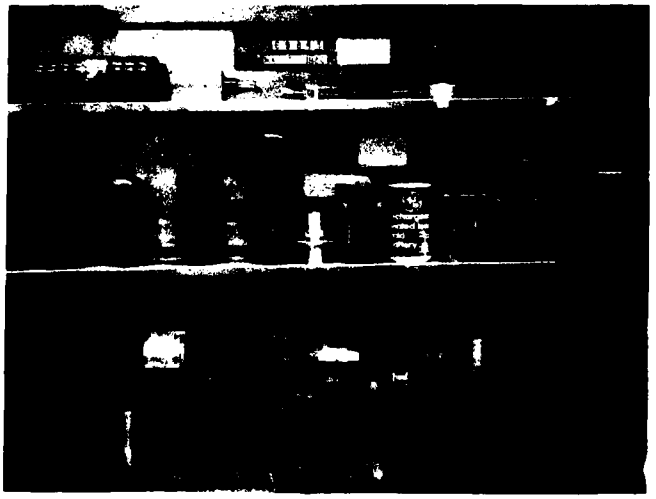
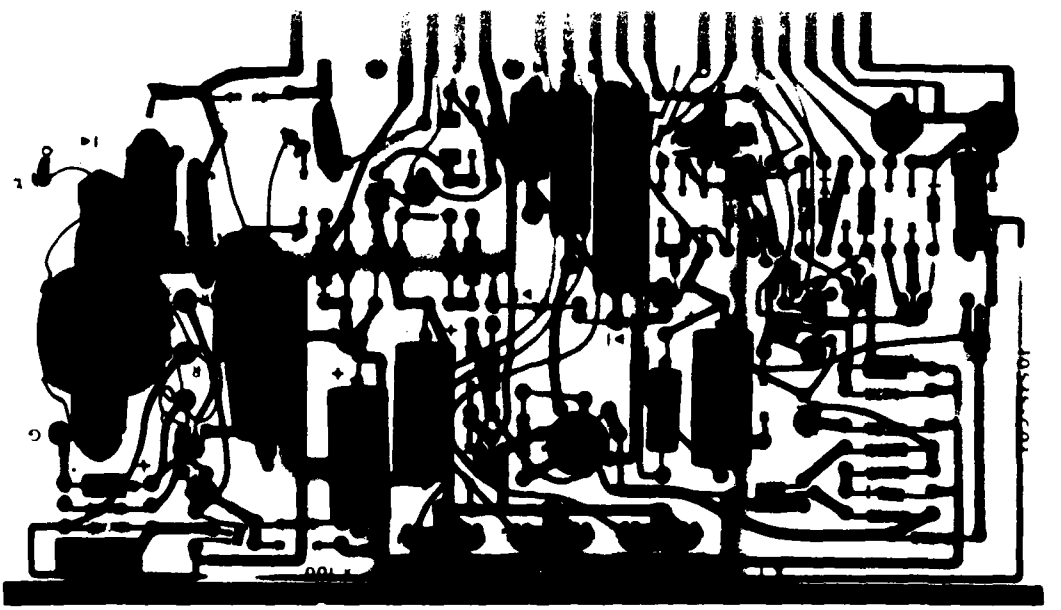


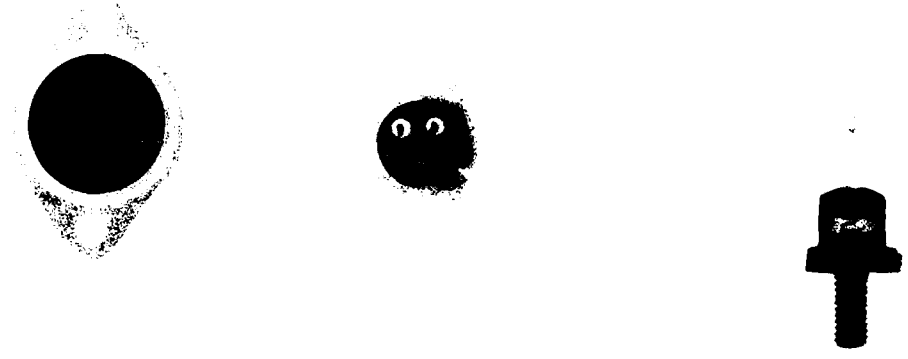
FIGURE 16. COMPONENT PARTS MOUNTED FOR RADIOGRAPH ANALYSIS

a) NEUTROGRAPH

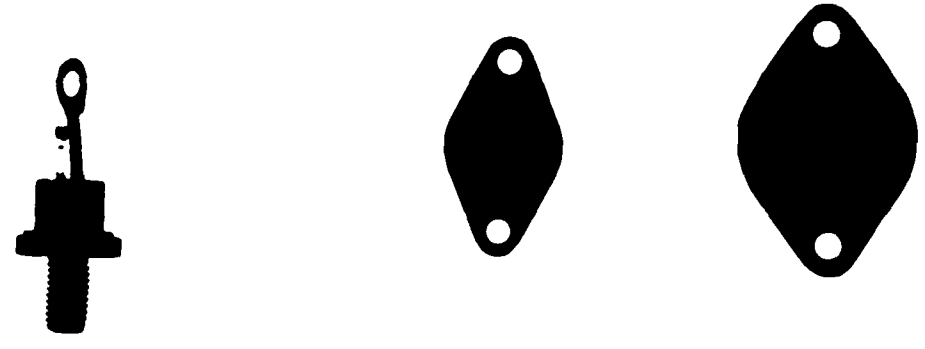


b) X-RAY

FIGURE 17. COMPARISON OF NEUTROGRAPH AND X-RAY OF PRINTED CIRCUIT BOARD

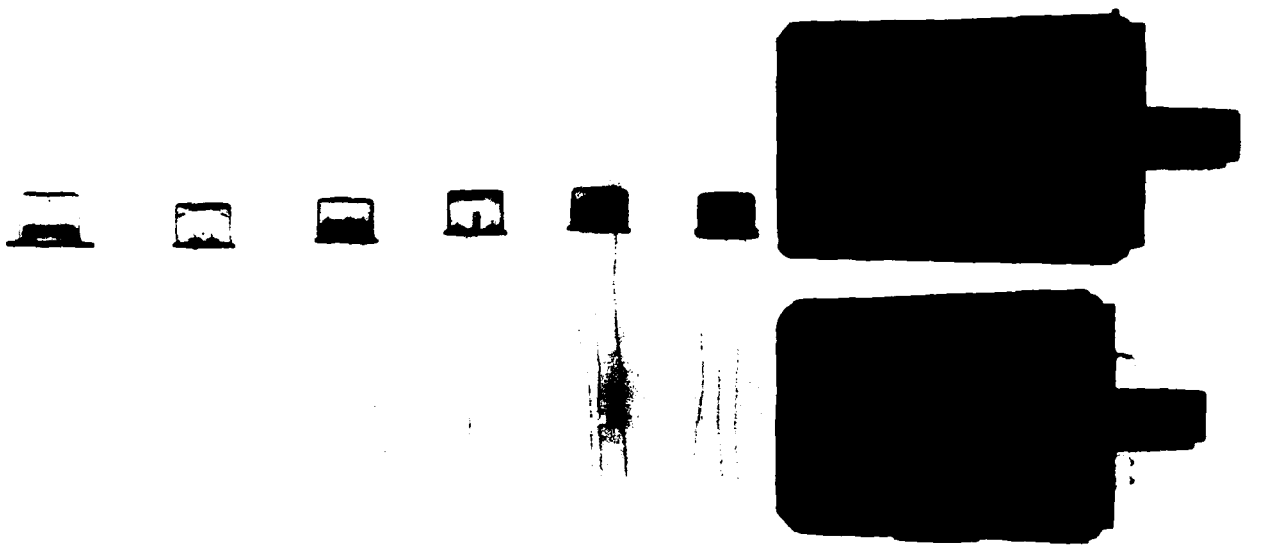


a) NEUTROGRAPH

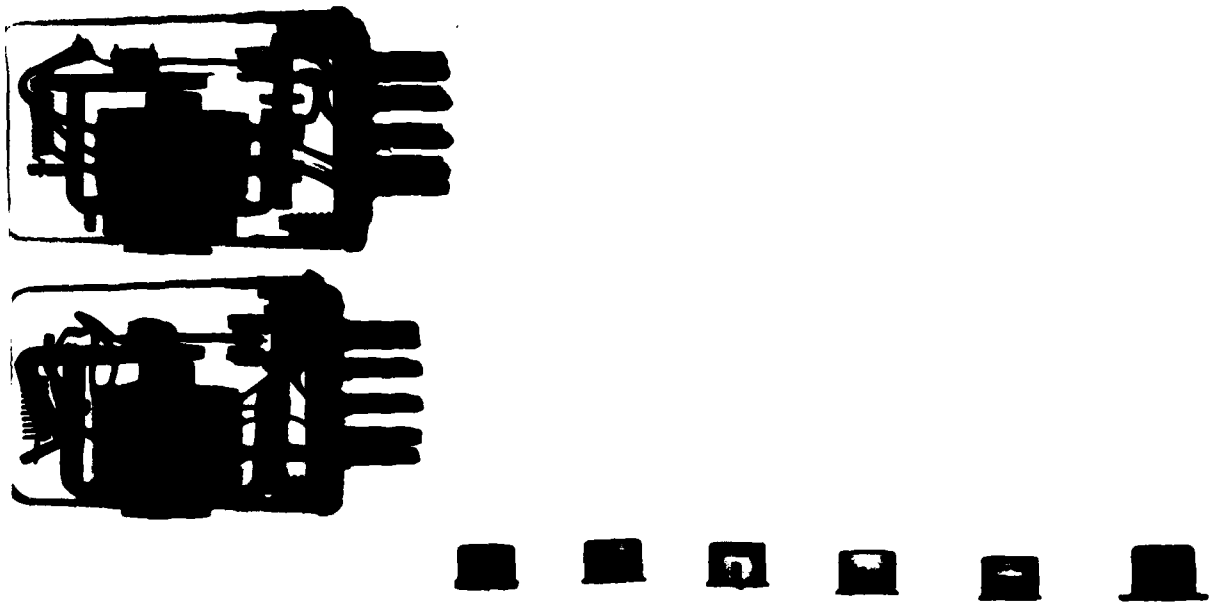


b) X-RAY

FIGURE 18. COMPARISON OF NEUTROGRAPH AND X-RAY OF SEMICONDUCTOR DEVICES



a) NEUTROGRAPH



b) X-RAY

FIGURE 19. COMPARISON OF NEUTROGRAPHS AND X-RAYS OF RELAYS AND POTTED ASSEMBLIES

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17. Brady, James A. Private Communication including Faxtron X-ray radiographs of component defects taken General Electric AESD in Utica, N.Y.

EQUIPMENT

X-ray Unit	
160 KVCP - Phillips Electronics	$22,500.00
FAXTRON 804 - Field Emission Corp.	5,900.00
N-ray Unit	
Neutron Radiographic Facility - General Electric Company	$1M - 15M
Automatic Processor	
X-O MAT - Model B - KODAK	$20,000.00
Guardian II - PAKO	$16,000.00
Densitometer	
Model 301 - X-RITE	900.00
Model 902 - MACBETH	900.00
Viewers	
Cat. #189 - S&S	695.00
Cat. #1851 - S&S	490.00
Manual Processing	
36" Processing Tank - Bar Ray	$2,175.00
Insert Tank and Cover - Bar Ray	100.00
Film Hanger - Bar Ray	16.50
Cassette - Bar Ray	11.00
Film Drier - S&S	450.00
Safe Light - KODAK	50.00

Not included are minor items such as thermometers, mixing paddles, timers, film cutter, etc. Most prices were obtained from Buffalo X-ray Company, Buffalo, N.Y.

C.

HERMETICITY TECHNIQUES

C. Hermeticity Techniques.

1. Introduction. The definitive document that specifies test methods and acceptance limits for microelectronic package seal effectiveness is MIL-STD-883, "Test Methods and Procedures for Microelectronics," Department of Defense, Washington, DC 20301. At this time of writing, Revision B (dated 31 August 1977) is current. The fine leak test acceptance limits in Revision B are five times more stringent than in the earlier Revision A. The user who desires to test a device against the acceptance levels of 883 should be careful to ascertain which revision applies to his particular procurement contract.

Method 1014 contained in the above Military Standard includes fine testing by helium and radioisotope tracer gases and gross testing by fluorocarbon bubbles, dye penetrant, and weight gain. These procedures are well written and specific and are designed for military acceptance. However, the failure analyst will often need additional techniques to determine whether functional failures are in fact related to hermeticity deficiency and what mechanism(s) may be responsible for hermeticity failure. The latter information is necessary in order to differentiate between one-of-a-kind freaks, handling overstress, and manufacturing lot rejection criteria. (See Appendix I at the end of this chapter for the current revision of Method 1014.)

Typical failure analysis techniques will depend on the nature of the package but in general should include these steps:

a) Localization of the leakage site(s)

b) External non-destructive examination by light microscope or Scanning Electron Microscopy (SEM). The SEM is particularly useful in package examination because of its superior depth of field. Figures 1 through 4 are SEM photographs of leaking glass-lead package seals, which indicated poor glass-to-metal oxide seals

FIGURE 1. 100X
SEM GLASS-TO-LEAD SEAL

FIGURE 2. 1000X
SEM GLASS-TO-LEAD SEAL

FIGURE 3. 100X
SEM GLASS-TO-LEAD SEAL

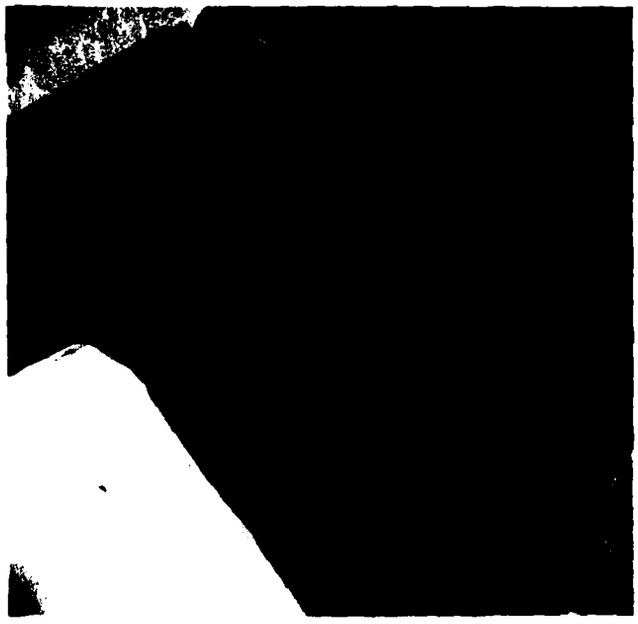

FIGURE 4. 1000X
SEM GLASS-TO-LEAD SEAL

c) Device dismantling (delidding) or cross-sectioning followed by metallurgical analysis

A very useful and comprehensive reference on all phases of leak detection is the Leakage Testing Handbook. This document describes 27 detector principles and 128 equipment manufacturers in July 1969. Obviously, any list of manufacturers rapidly becomes obsolete and should be supplemented by such current commercial listings as the Thomas Register, the VSMF microfilm file, or other industry buyers guides.

2. Methodology of Leak Testing. It is first necessary to distinguish between gross and fine leak rates. The quantitative definitions depend on package size and to some extent on device functional susceptibility, and these are spelled out in MIL-STD-883. There are additional distinctions:

a) Leak testing generally is applied to devices having designed cavities, as opposed to devices potted in epoxies, silicone rubber, dielectric fluids, or polymer cellular foams. In potted devices, the transmission rate or permeation rates of environmental contaminants may be a very important reliability consideration and can often be evaluated by leak detection-like methods. However, this section is limited to hermeticity problems related to cavity designs.

b) Leakage may involve both gases and liquids. "Fine" leak rates refer to gas leakage, because the surface tension of liquids generally restricts their passage to capillary sizes that are in the gross leakage category. However, very high pressure liquid environments (e.g., undersea operation) may overcome surface tension forces and necessitate special consideration. A detailed discussion of this effect is found in Section 6.4.2 of the Leakage Testing Handbook.

c) Not all gases behave alike in respect to their flow rates through capillaries. Helium is the most widely used tracer gas for leak detection, and its properties most nearly approximate those of an ideal gas. A practical value of 10^{-10} atm - cc/sec is the sensitivity to be expected under routine test conditions. However, water and halogenated compounds are among the most deleterious contaminants in microelectronic devices, and their rates of flow through leaks are generally quite different than that of helium. DerMarderosian, Hayashi , Stroehle , and Santeler are among those who have examined this problem. There is no simple correlation between the measured helium leak rate and the rate of moisture ingress because of unknown leak geometry effects and the difference between water liquid and water vapor. Nevertheless, helium leak testing by mass spectrometer detection is the most widely used method of leakage diagnosis.

Radioactive isotopes are used as tracers in the detection and measurement of leakage. Only a small quantity of the radioactive material is needed to load the item which is to be tested. The nuclear radiation from leakage of the radioactive material is detected by means of special electronic instruments. Sensitivity of this technique may be as high as 10^{-13} atm-cc/sec under ideal operating conditions. To attain these conditions, the soaking and counting time must be selected for high sensitivity, and the units being tested must be of a "clean" (i.e., unpainted metal or ceramic, no organic material) construction, with no possibility of adsorption of radioactive material on the outer surfaces. A practical value of 10^{-11} atm-cc/sec is the sensitivity to be expected under routine test conditions. The test procedure frequently used is that known as the "Radiflo" method. In this method of leakage testing, the following principal steps are involved:

- Components to be tested are placed in a tank, which is sealed and evacuated to about 2 torr.
- Diluted krypton-85, typically on the order of 1 percent diluted with N_2, is pumped into the tank under pressure.

- o After a prescribed "soaking" period, in which the radioactive gas diffuses into existing leaks in the components, the krypton is pumped out of the tank and stored for reuse.
- o An air wash is circulated over the components to remove any residual krypton from the external surfaces.
- o Components are then removed from the tank.
- o Those with leaks will retain some radioactive atoms, which emit gamma radiation.
- o This radiation is detected by a suitable radiation counter, the measured radiation being a function of the leak rate. Occasionally, components with very large leaks (10^{-5} atm-cc/sec) tend to slip through the leak test as acceptable. This is due to rapid escape of the radioactive gas through the large opening during the final pump-down phase of the test cycle.
- o Insert Leak Rate Equation for radiflow.
- o Usually, the components are bubble-tested after the Radiflo test to detect these gross leaks.

Disadvantages of Radiflo technique are:

- o Leaks cannot be localized.
- o If parts are leakers, a proscribed holding period of several days for radioactive decay is required before the failure analyst can perform other steps on the failed parts.

For these reasons, the Radioflo technique is more useful in high volume production testing where the disadvantages described above are not of primary interest. A more detailed test procedure for the Radiflo method can be obtained from MIL-STD-883 Test Method 1014.4, Test Condition B in appendix I of this section. Appendix II shows the deviation of Radiflo equation.

When samples are exposed to pressurized helium, the leak sites can often be located by probing the package exterior

with a very small diameter probe connected to the inlet of a mass spectrometer helium leak detector. The probe may consist of a hypodermic needle or a section of thick-wall polyethylene tubing drawn to a small diameter while heated. The latter is often used to form vacuum pickup nozzles for handling chips during device assembly. Nozzles can be formed that will fit over individual device lead wires and thus test each lead seal for leakage. The probe must be connected to the mass spectrometer inlet system, through a suitable throttle valve in order to maintain vacuum conditions in the spectrometer while the probe is at atmospheric pressure. Because of the unknown atmospheric dilution factor, the method cannot be quantitatively calibrated.

If the device package exterior is painted, the probability of locating leaks is diminished. Helium may diffuse along the interface between the paint and the package surface and emerge some distance from the actual leak site. If an attempt is made to remedy this problem by removing the paint with solvent, the result is likely to be even worse. Leaks may be plugged with solvent or softened paint.

This brings us to a very important precaution that is unfortunately widely overlooked. Devices must <u>never</u> be exposed to <u>any</u> liquid before performing tracer gas leak testing. Gross leak testing should always <u>follow</u> fine leak testing, never precede it. The reason is that liquids, even highly volatile solvents, will be held in capillaries by surface tension and will thus plug the leaks against the passage of tracer gas. Room temperature vacuum pumping will usually not remove the liquid. One case has been observed where a confirmed leak in stainless steel was intentionally plugged with water. A month of room temperature vacuum pumping failed to remove the water.

If a failure analyst suspects that this rule was violated before he acquired a sample, a vacuum bakeout may remove liquid blockages at the risk of introducing new factors in the analysis.

Painted samples or polymeric package constituents not only make difficult the loc ion of leak sites but they also

seriously compromise the quantitative measurement of overall fine leak rate by the Method 1014 procedure. Polymers will rapidly absorb quantities of tracer gas (either Krypton-85 or helium) during the pressure soak and subsequently deliver a large background signal to the detector from the outside surface, thus overshadowing small signals from leakage. This problem can sometimes be reduced by warming the sample for a short time after pressure soak and before the detection step. Tracer gas absorbed in the polymer may be desorbed faster than gas is lost by outflowing through leaks. It can be appreciated that quantitative calibration is difficult, depending as it does upon the relation between desorption by permeation through the polymer and the temperature dependence of gas flow in the transition mode through capillaries of unknown geometry. On a few occasions samples have been soaked twice, once followed by room temperature detections and the second time heated before detections. If heating reduced the tracer signal greatly and if no gross leak was subsequently found, then it is assumed that no fine leak existed. Confirmation can be obtained by a mass spectrometer gas analysis of the device interior. A background analysis before puncturing will separate sorbed gases on the package exterior from interior tracer gases, within certain leak-rate limits. Again, the precision of such an analysis is reduced because the relative rates of loss of tracer gas by desorption and by leakage during vacuum pumping are unknown. Davy has treated theoretical aspects of the problem.

3. Leak Rate Calculations. The equation in Test Method A2 may appear formidable at first encounter, and its development by Howl and Mann in 1966 and by Doyle in 1967 was accompanied by various graphical presentations. These were not notably successful in simplifying its use because nine quantities are involved, requiring sets of two-parameter curves over wide ranges of rates of change. Today it can be very quickly calculated with a student calculator for a single set of values, but even this can become time-consuming when evaluating the effects of varying parameters.

Probably the most satisfactory way of reducing the equation for all applications is to utilize programmable calculators with magnetic card recording. Two typical programs are included herein for Texas Instruments 59 and Hewlett Packard 67 calculators. But before applying these programs, it is appropriate to review the meaning of the basic equation, since confusion has been encountered in definition and physical significance of the quantities.

Expression for calculating the measured helium leak rate from MIL-STD-883B, METHOD 1014.2, "SEAL", Page 4, dated 31 August 1977:

$$R_1 = \frac{LP_E}{P_O}\left(\frac{M_A}{M}\right)^{1/2}\left\{1 - e^{-\left[\frac{Lt_1}{VP_O}\left(\frac{M_A}{M}\right)^{1/2}\right]}\right\}e^{-\left[\frac{Lt_2}{VP_O}\left(\frac{M_A}{M}\right)^{1/2}\right]}$$

The measuring of the basic equation is discussed first and then followed with a brief discussion of two of the nine other parameters. The remainder of the parameters in the equation are adequately self-explanatory.

a) R_1 = The Measured Leak Rate of Tracer Gas (He) Through the Leaks in (Units of) Atmosphere cc/sec He. This is the measured quantity actually determined by a properly calibrated mass spectrometer helium leak detector. The formula determines what combination of test conditions are necessary in order to prove that a particular sample passes the value for L specified by Method 1014 for its internal volume.

Modern commercial helium leak detectors have rated maximum sensitivities of the order of 10^{-10} to 10^{-11} atmos. cc/sec helium. If the leak detector available to the user is not this sensitive, then one can increase P_E or t_1, or decrease t_2. Each of these options has practical limits. t_2 can at best be reduced to a few seconds. t_1 may perhaps be increased to a weekend, or a week or month, but the point of diminishing returns is usually

reached in, say, overnight exposure. P_E will be limited by the strength of the pressure bomb but more likely by the strength of the device package. Large hybrid flatpacks, for example, may withstand a differential pressure of only one atmosphere or less. One or two destructive experiments on expendable samples may be necessary to establish this limit. In some cases it may not be that simple: glass soldered lids or metal soldered lids may develop microcracks during over-pressurized leak testing. The failure analyst must be alert to this possibility, not only to avoid false results but also to uncover a basically weak construction or a construction perhaps suitable for mild consumer applications but unacceptable for more heavily stressed military use. By now it should be evident that a rapid and flexible method of computing the leakage formula can be highly useful. The two included calculator programs are each written in two parts. The first part is a straightforward calculation of R_1 for the entered variables. P_o is assumed to be 1 and is permanently written in at that value. The ratio of M_A/M is also assumed constant. The remainder of the parameters are entered via user defined keys as described in the respective program instructions. There may be occasions when one would like to solve the formula "backwards"; that is, first to measure R_1 under some particular test condition and then calculate L to determine whether the device passes the acceptance limit. The formula cannot readily be solved for L mathematically, but it is easy to solve arithmetically to any desired accuracy by an iterative process. This is the second part of the calculator programs. 99% accuracy is usually adequate for most purposes, but the user may select any desired accuracy. The algorithm incorporates a procedure to ensure rapid convergence, and the running time for typical values is of the order of ten seconds (usually two or three iterations). The program is seeded with a starting L value of 10^{-12} atmos. cc/sec which is very conservatively chosen to be sure that the results converge on the positive slope side of Figure 7 in the Howl and Mann paper.

b) L = The Equivalent Standard Leak Rate in Atmosphere cc/second. This is a standard leak rate under test conditions of one atmosphere (absolute) pressure of air within the package and a vacuum surrounding the package, conditions which obtain in a mass spectrometer leak test apparatus. L is a quantity specified by Test Method 1014 and is different for different-sized packages. It is an acceptance standard only. The internal atmosphere is defined to be air in the derivation of the basic formula (Reference 11, page 2). If the package has zero leakage after pressure bombing in helium, then no helium will be detected by the mass spectrometer, an eminently satisfactory result.

c) P_E = The Pressure of Exposure in Atmospheres Absolute. Most pressure gages used for this pressure range are of the Bourdon-Tube type, or similar to mechanical aneroid barometers. They are usually calibrated to read zero at atmospheric pressure. P_E, however, is defined in terms of atmospheres absolute. Thus "gage pressure" readings, unless specified differently on the face of the gage, are 14.7 pounds per square inch (sea level) less than the absolute pressure. Zero on such a gage is actually one atmosphere absolute. If the gage reading is 4 atmospheres, then the absolute pressure is 5 atmospheres.

4. Gross Leak Testing. The three methods used in Method 1014 are liquid fluorocarbon bubble testing, dye penetrant, and weight gain in fluorocarbon liquid. The latter is not capable of locating leak sites, but the first two methods are readily capable of pinpointing most gross leaks. The techniques are explicitly described in Method 1014.

Figure 5a shows typical equipment used for performing gross leak testing, and Figure 5b shows several examples of packages with gross leaks.

Dye penetrant testing of gross leaks leaves a residue of dye and developer powder, and this residue can cause problems in subsequent microscopic examination. Accordingly, the liquid fluorocarbon bubble test would be the method of first choice when failure analysis is planned.

5. Some Pitfalls in Leak-Rate Measurement. A case history is described in the following section to illustrate methods of data treatment as well as some special problems. This case history is not claimed to be "typical", a meaningless description. It illustrates a number of lessons that all failure analysts should heed even though they may not expect ever to see the type of device described. The narrative style demonstrates how problems arise sequentially. In addition, information available to the analyst is frequently incomplete.

The problem was to determine the leak rate of some rather large ceramic hybrid flatpacks that had failed. The packages measure 9 cm x 4.8 cm x 0.6 cm. Internal package volume V was $12 cm^3$. The lids were metal, soldered to metallized-ceramic sidewalls. The bottoms were metal heat sinks soldered to the ceramic substrate (not a closure joint).

a.

b.

FIGURE 5. TYPICAL LEAK EQUIPMENT AND EXAMPLES OF MICROELECTRONIC PACKAGES WITH GROSS LEAKS.

The large surface area of the metal lids necessitated a low helium exposure pressure (P_E) to avoid excessive deflection stress. This was specified not to exceed one atmosphere "differential pressure." The pressure actually used was 13.7 pounds per square inch gage pressure. This was attained by first using a mechanical vacuum pump to exhaust the pressure vessel containing the sample to a pressure of about 50 millitorr. The pump was then valved off and the system backfilled with helium to a gage pressure of 13.7 pounds per square inch. The absolute helium pressure (P_E) in atmospheres was therefore

$$P_E = \frac{13.7}{14.7} + 1.0 = 1.93 \text{ atmospheres.}$$

Since the device was already filled with one atmosphere of dry nitrogen (an almost universal practice in microcircuit construction), it received a maximum differential pressure during exhaust of one atmosphere internal, and the helium soak was at a differential pressure of $\frac{13.7}{14.7} = 0.93$ atmosphere, or 1.93 atmospheres absolute. No correction was considered necessary for elevation above sea level or for barometric pressure variations.

The exposure time t_1 was 24 hours, or 86,400 seconds. At the end of that time the following data were taken:

Dwell time (t_2) = 125 seconds.

Elapsed Time Seconds	Leak Rate Arbitrary Units	
0	--	Start Leak De - Pump
65	10	
95	8	
130	6.7	
285	4	
415	3	

Standard Calibrator Leak Rate = 2.3×10^{-8} atmos. cc/sec. helium

Measured standard helium leak rate = 2.0 units

Sometimes devices exhibit an essentially constant mass spectrometer leak rate reading which, of course, simplifies calculations and conclusions. The relatively rapid decrease in leak rate in the above data can be interpreted in several ways:

a) Drift of the mass spectrometer sensitivity. This was ruled out by checking it against the calibrated helium leak before and after the test run.

b) Pump out of helium through a leak in the specimen

c) Desorption of surface helium on the outside of the specimen

As previously mentioned, item (c) is a serious problem when paint or organic polymers are present. A simple external flush with pressurized air or nitrogen is usually sufficient to eliminate surface sorption of helium or metals. Ceramics lie somewhere between metals and polymers in helium sorption. Ceramics usually have a greater specific surface area than metals, and the glassy phase may have a relatively high rate of helium permeation.

At this point, item (c) remained an unevaluated possibility, so the leak rate data were first calculated by the Method 1014 leak rate formula. Since the mass spectrometer signal declined significantly with time, it was necessary to extrapolate the data to time zero (when the vacuum pump was started). This can be done by plotting the data on semilog paper, with the time in seconds on the horizontal linear scale. A flexible curve can then be used to fit by eye to the y (leak rate) intercept at t = 0. Alternatively, a curve may be fitted by one of the standard library programs available for the TI59 or HP67 or other models. If these data are plotted directly on semilog paper the result is rather far from a

straight line, so an exponential curve would probably not fit well. However, a parabolic curve was fitted by a calculator program with the following results:

Time Sec.	Measured Leak Rate	Calculated Parabolic Leak Rate
0	--	12.5
65	10	9.5
95	8	8.3
130	6.7	7.1
285	4	3.6
415	3	3.1

Since we do not know what processes are generating the measured leak rates (i.e., surface desorption or capillary leakage or a mixture of the two), it would be unjustified to attach physical significance to the apparent parabolic fit. In any event, the precision is unknown, so we should simply accept it as an empirical convenience.

Using 12.5 scale units as the leak rate and 2 units for the calibrated helium leak,

$$R_1 = \frac{12.5}{2} \times 2.3 \times 10^{-8} = 1.44 \times 10^{-7} \text{ atmos. cc/sec helium.}$$

The remainder of the quantities needed to calculate L are, to summarize:

P_E = 1.93 atmos. absolute
P_0 = 1 atmos., already entered in the program
$(MA/M)^{1/2}$ = 2.679, already entered in the program
t_1 = 86,400 seconds
t_2 = 125 seconds
V = 12 cc

Note that with the calculator programs, we can arrive at a pass/fail conclusion in either of two ways:

a) Since the internal cavity volume V is greater than 0.4cc, then L must not exceed 1×10^{-6} atmos. cc/sec. air equivalent by 883B, or 5×10^{-7} by 883A. The appropriate value for L is plugged into the first half of the program and the resulting R_1 value is compared with the measured R_1. If the calculated (or permissible) R_1 is greater than the measured R_1, the device passes and conversely it fails.

b) The measured value of R_1 is plugged into the second half of the program. The calculated L is then compared directly with the statement in paragraph 3.1.1.2.1, "Failure Criteria." Because of the wording of this paragraph, it may be easier to understand the criteria if one calculates L by the programs. It is for this reason that we have included the iterative programs for calculating L. Either method, if properly applied, will lead to the same pass/fail conclusion, and it is hoped that this dual choice of methods will diminish rather than increase whatever confusion may have existed. The results of the calculations are as follows:

Max. Permissible L - atmos. cc/sec.	883A	883B
	5×10^{-6}	1×10^{-6}
Calculator Program Part 1 - Calculated R_1 For Max. Permissible L	2.4×10^{-6}	9.9×10^{-8}
Calculator Program Part 2 - Calculated L For Measured R_1	1.44×10^{-7}	1.21×10^{-6}

The conclusion is that the device passed 883A but failed 883B. The reasoning is as follows:

o If we used Part 1 of the program and calculated R_1, R_1 must have measured no greater than 2.4×10^{-6} to pass 883A. In fact, it measured 1.44×10^{-7} which passes 883A. However, 1.44×10^{-7} is greater than 9.9×10^{-8} and therefore it failed 883B.

o If we used Part 2 of the program, the same conclusions are reached by merely comparing the calculated L with the maximum permissible values. Incidentally, the failure analyst was not informed until later that 883A was the test criterion.

6. Discussion. The differences between pass and fail quantities in this example are not large, and it is legitimate to question the accuracy and precision of measurement. As previously mentioned, desorption of surface helium (background) was an unknown factor. Microscopic examination of the device revealed considerable porosity in the heat-sink solder. It was not easy to evaluate this porosity effect separately from the ceramic sorption, but a simple test was run to help estimate the magnitude of sorbed helium. An open (delidded) device was helium bombed under the same conditions as before and "leak" tested. The device interior contained monolithic ceramic capacitors and resistors and open-faced silicon chips, plus metallization runs. There was no organic material present and no sealed cavities.

An abbreviated tabulation of "leak" rate data follows, in arbitrary scale units:

Elapsed Time-Sec.	Leak Rate-Arb. Units
131	1000 (Just on scale)
175	600
221	400
570	200
2490	76
9070	26

This enormous increase over the sealed device leak test rate can only mean that the surface desorption background is a serious problem and could well account for most of the "leakage" used to arrive at the previous pass/fail conclusion. The revised conclusion is that the sealed device passed both 883A and 883B.

Unfortunately, it is not possible to state what leak rate would have had to be recorded to fail the device. The background must be reduced as far as possible by gentle and rapid heating during the swell period. Tests should be run on ceramic and solder samples to establish the minimum time and temperature to produce zero background (after normalizing to equivalent areas).

The failure analyst should at this point consider an alternate approach to the analysis; namely, a mass spectrometer analysis of the package atmosphere. If it contains helium, it was a leaker. If it does not (after adjusting for differences in instrumental sensitivities) then the composition of the gas may indicate a cause of failure other than package leakage. For example, sealed-in water may have been a basic cause of failure. This is discussed in the section on gas analysis.

This case history ends here on a somewhat inconclusive note. Additional work was done but it contains details inappropriate to this Procedural Guide. We deliberately refrained from searching out files for a happy ending example. They do exist, fortunately, but they are less instructive of pitfalls. The ultimate goal, that of a correct conclusion, should always be kept in sight, and it often requires tenacity and integrity on the part of the analyst to achieve it.

FIGURE 6 : TI CALCULATOR HERMETICITY PROGRAM

TITLE HERMETICITY, MIL-STD-883B PAGE 1 OF 3

PROGRAMMER WEL DATE 8-20-79

TI Programmable **Program Record**

Partitioning (Op 17) NORMAL Library Module NONE Printer _____ Cards 1

PROGRAM DESCRIPTION - TI59 CALCULATOR

MIL-STD-883B, METHOD 1014.4, "SEAL", Page 3

$$R_1 = \frac{LP_E}{P_0}\left(\frac{M_A}{M}\right)^{1/2}\left\{1 - e^{-\left[\frac{Lt_1}{VP_0}\left(\frac{M_A}{M}\right)^{1/2}\right]}\right\} e^{-\left[\frac{Lt_2}{VP_0}\left(\frac{M_A}{M}\right)^{1/2}\right]}$$

See reference above for definition of terms.

USER INSTRUCTIONS

STEP	PROCEDURE	ENTER	PRESS		DISPLAY
	To Compute R_1 from specified L:				
1.	L units - atmosphere cc/sec.	L		A	L
2.	P_E units - atmospheres	P_E		B	P_E
3.	t_1 units - seconds	t_1		C	t_1
4.	t_2 units - seconds	t_2		D	t_2
5.	V units - cc	V	2nd	A′	V
6.	Compute R_1			E	R_1
	To Compute L from measured R_1:				
1.	Units as above	P_E		B	P_E
2.	" " "	t_1		C	t_1
3.	" " "	t_2		D	t_2
4.	" " "	V	2nd	A′	V
5.	Measure Helium leak rate - atmos. cc/sec. He	R_1	2nd	B′	R_1
6.	Select relative accuracy, usually 0.99	.99	2nd	C′	.99
7.	Compute L		2nd	E′	L

USER DEFINED KEYS	DATA REGISTERS (INV ■)		LABELS (Op 08)
A L	0 A	0	
B P_E	1 B	1	
C t_1	2 C	2	
D t_2	3 D	3	
E	4	4	
A′ COMPUTE R_1	5 A′	5	
B′ V	6 B′	6	
C′ R_1 MEASURED	7 C′	7	
D′ ACCURACY	8	8	
E′ COMPUTE L	9	9	

FLAGS 0	1	2	3	4	5	6	7	X 8	X 9

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FIGURE 6:· TI CALCULATOR HERMETICITY PROGRAM (cont'd)

TITLE HERMETICITY, MIL-STD-883B PAGE 2 OF 3

TI Programmable Coding Form

PROGRAMMER WEL DATE 8-20-79

LOC	CODE	KEY	COMMENTS
000	76	LBL	
001	11	A	
002	42	STO	
003	00	00	
004	91	R/S	
005	76	LBL	
006	12	B	
007	42	STO	
008	01	01	
009	91	R/S	
010	76	LBL	
011	13	C	
012	42	STO	
013	02	02	
014	91	R/S	
015	76	LBL	
016	14	D	
017	42	STO	
018	03	03	
019	91	R/S	
020	76	LBL	
021	16	A'	
022	42	STO	
023	04	04	
024	91	R/S	
025	76	LBL	
026	17	B'	
027	42	STO	
028	05	05	
029	91	R/S	
030	76	LBL	
031	18	C'	
032	42	STO	
033	06	06	
034	91	R/S	
035	76	LBL	
036	15	E	
037	53	(	
038	53	(	
039	02	2	
040	93	.	
041	06	6	
042	07	7	
043	09	9	
044	42	STO	
045	10	10	
046	65	×	
047	43	RCL	
048	01	01	
049	65	×	
050	43	RCL	
051	00	00	
052	54	)	
053	65	×	
054	53	(	
055	01	1	
056	75	-	
057	53	(	
058	53	(	
059	53	(	
060	43	RCL	
061	00	00	
062	65	×	
063	43	RCL	
064	02	02	
065	65	×	
066	43	RCL	
067	10	10	
068	54	)	
069	55	÷	
070	43	RCL	
071	04	04	
072	54	)	
073	94	+/-	
074	22	INV	
075	23	LNX	
076	54	)	
077	54	)	
078	65	×	
079	53	(	
080	53	(	
081	53	(	
082	43	RCL	
083	00	00	
084	65	×	
085	43	RCL	
086	03	03	
087	65	×	
088	43	RCL	
089	10	10	
090	54	)	
091	55	÷	
092	43	RCL	
093	04	04	
094	54	)	
095	94	+/-	
096	22	INV	
097	23	LNX	
098	54	)	
099	54	)	
100	42	STO	
101	11	11	
102	87	IFF	
103	08	08	
104	10	E'	
105	92	R↓	
106	76	LBL	
107	10	E'	
108	86	STF	
109	08	08	
110	87	IFF	
111	09	09	
112	38	SIN	
113	53	(	
114	01	1	
115	52	EE	
116	01	1	
117	02	2	
118	94	+/-	
119	42	STO	
120	00	00	
121	54	)	
122	86	STF	
123	09	09	
124	15	E	
125	76	LBL	
126	38	SIN	
127	43	RCL	
128	06	06	
129	32	X↕T	
130	53	(	
131	43	RCL	
132	11	11	
133	55	÷	
134	43	RCL	
135	05	05	
136	54	)	
137	42	STO	
138	12	12	
139	22	INV	
140	77	GE	
141	39	COS	
142	43	RCL	
143	00	00	
144	91	R/S	
145	22	INV	
146	86	STF	
147	08	08	
148	22	INV	
149	86	STF	
150	09	09	
151	76	LBL	
152	39	COS	
153	53	(	
154	43	RCL	
155	12	12	
156	35	1/X	
157	34	√X	
158	65	×	
159	43	RCL	

MERGED CODES

62	72 STO	83 GTO
63	73 RCL	84
64	74 SUM	92 INV SBR

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TI-24181

FIGURE 6 : TI CALCULATOR HERMETICITY PROGRAM (cont'd)

TITLE HERMETICITY, MIL-STD-883B PAGE 3 OF 3

PROGRAMMER _____ DATE _____

TI Programmable **Coding Form**

LOC	CODE	KEY	COMMENTS	LOC	CODE	KEY	COMMENTS	LOC	CODE	KEY	COMMENTS
160	00	00									
161	54	)									
162	42	STO									
163	00	00									
164	15	E									

MERGED CODES

62	72 STO	83 GTO
63	73 RCL	84
64	74 SUM	92 INV SBR

TEXAS INSTRUMENTS INCORPORATED

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TI-24181

Program Description

FIGURE 7 : HP CALCULATOR HERMETICITY PROGRAM

Program Title LEAK HP67

Name **Date**

Address

City **State** **Zip Code**

Program Description, Equations, Variables, etc.

$$R_M = \frac{P_E}{P_A}\sqrt{\frac{M_A}{M}}\; L \left\{ 1 - \exp\left(-\sqrt{\frac{M_A}{M}\frac{L}{V}}\, T_1\right)\right\} \exp\left(-\sqrt{\frac{M_A}{M}\frac{L}{V}}\, T_2\right)$$

R_M = Leak Rate Measured (STD cc He/Sec)

P_E = Bomb Pressure, (Atmospheres Absolute)

P_A = 1 Atmosphere

L = Air Leak Size (STD cc Air/Sec)

V = Package Volume (cc)

T_1 = Bomb Soak Time (Sec)

T_2 = Dwell Time from Bomb Release to Measurement (Sec)

Program calculates the helium leak rate, R_M, given the air leak size, L, and other conditions.

It will also calculate the leak size L, given R_M and other conditions, by an iterative technique. A tolerance on the precision of L must be entered. The smaller the tolerance, the longer the running time. A tolerance of 0.01 will require about 30 sec.

Operating Limits and Warnings Solutions for L have two roots. This program finds the smaller root.

LABELS					FLAGS
A STO L	B STO P_E	C STO T_1	D STO T_2	E CALC R_M	0
a STO V	b STO R_M	c STO TOL	d	e CALC L	1
0	1	2	3	4	2
5	6	7	8	9	3

SET STATUS		
FLAGS	TRIG	DISP
ON OFF		
0 [ ] [ ]	DEG [ ]	FIX [X]
1 [ ] [ ]	GRAD [ ]	SCI [ ]
2 [ ] [ ]	RAD [ ]	ENG [ ]
		n 2

FIGURE 7 : HP CALCULATOR HERMITICITY PROGRAM (cont'd)

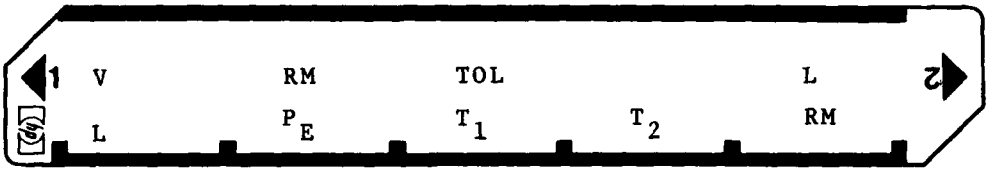
STEP	KEY ENTRY	KEY CODE	COMMENTS
001	*LBL A		
002	STO0		
003	RTN		
004	*LBL E		
005	STO1		
006	RTN		
007	*LBL C		
008	STO2		
009	RTN		
010	*LBL D		
011	STO3		
012	RTN		
013	*LBL a		
014	STO4		
015	RTN		
016	*LBL b		
017	STO6		
018	RTN		
019	*LBL c		
020	STO8		
021	RTN		
022	*LBL E		
023	2		
024	.		
025	6		
026	7		
027	9		
028	RCL0		
029	^		
030	STO5		
031	RCL2		
032	^		
033	RCL4		
034	÷		
035	CHS		
036	e^x		
037	CHS		
038	1		
039	+		
040	RCL5		
041	RCL3		
042	^		
043	RCL4		
044	÷		
045	CHS		
046	e^x		
047	^		
048	RCL5		
049	RCL1		
050	^		
051			
052	RTN		
053	*LBL e		
054	EEX		
055	CHS		
056	1		
057	Σ		
058	STO6		
059	*LBL 9		
060	GSBE		
061	STO7		
062	RCL6		
063	X≠Y?		
064	X≠Y		
065	÷		
066	1		
067	-		
068	RCL8		
069	X>Y?		
070	GTO1		
071	RCL9		
072	RCL7		
073	÷		
074	√x		
075	RCL0		
076	×		
077	FSE		
078	STO6		
079	GTO0		
080	*LBL 1		
081	RCL6		
082	RTN		
083	R/S		
090			
100			
110			

REGISTERS

0 L	1 P_E	2 T_1	3 T_2	4 V	5	6 R_M	7 R_C	8 TOL	9
S0	S1	S2	S3	S4	S5	S6	S7	S8	S9

A	B	C	D	E	I

FIGURE 7: HP CALCULATOR HERMETICITY PROGRAM (cont'd)



STEP	INSTRUCTIONS	INPUT DATA/UNITS	KEYS	OUTPUT DATA/UNITS
1	ENTER BOMB PRESSURE - P_E	ATM	B	
2	ENTER BOMB TIME - T_1	SEC	C	
3	ENTER DWELL TIME - T_2	SEC	D	
4	ENTER PACKAGE VOLUME	CC	a	
5	TO CALCULATE RM			
	ENTER L	STD cc/ sec	A	
	CALCULATE RM		E	STD cc/ sec
6	TO CALCULATE L			
	ENTER RM	STD cc/ sec	b	
	ENTER TOLERANCE (0<X<1)		c	
	CALCULATE L		e	STD cc/ sec

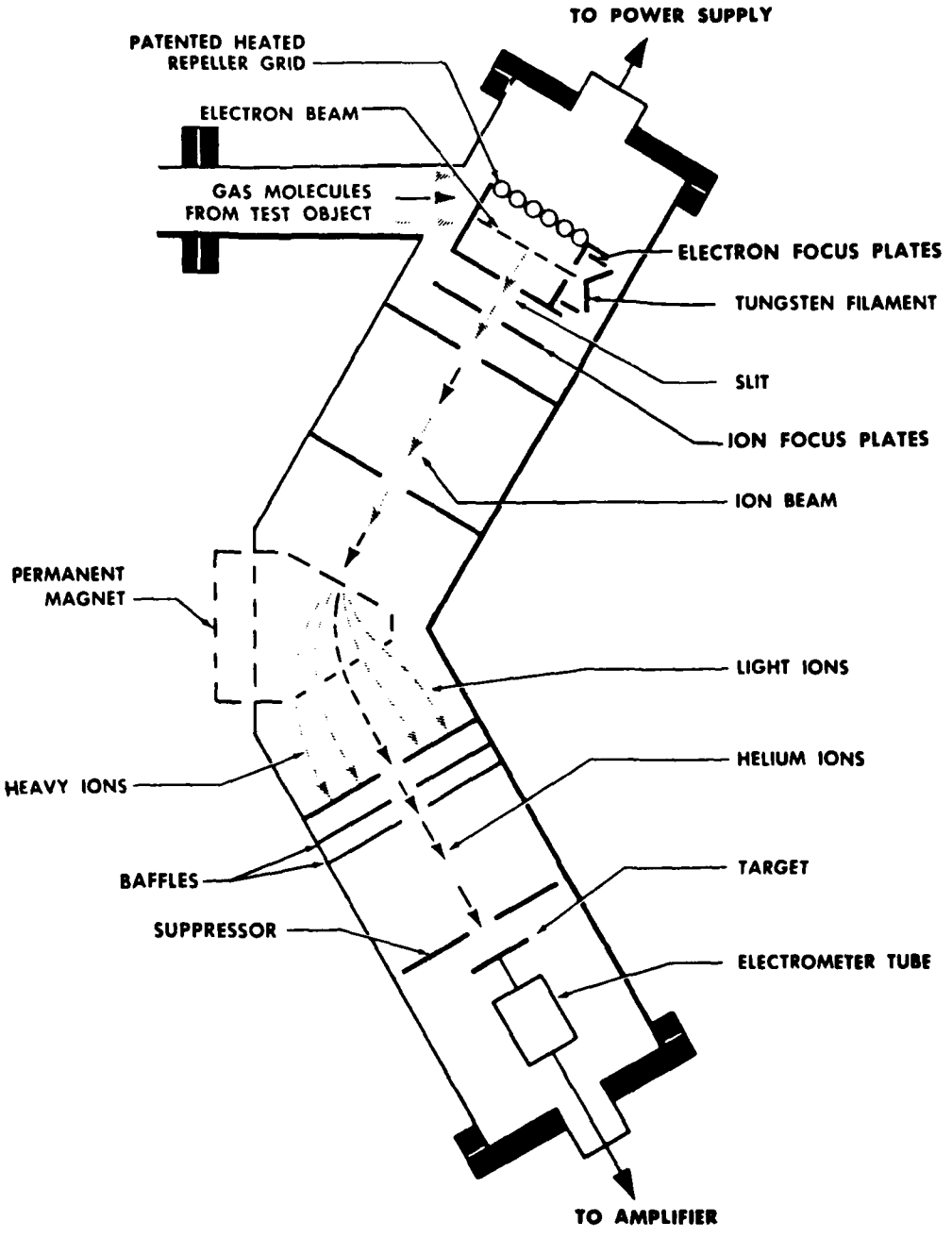
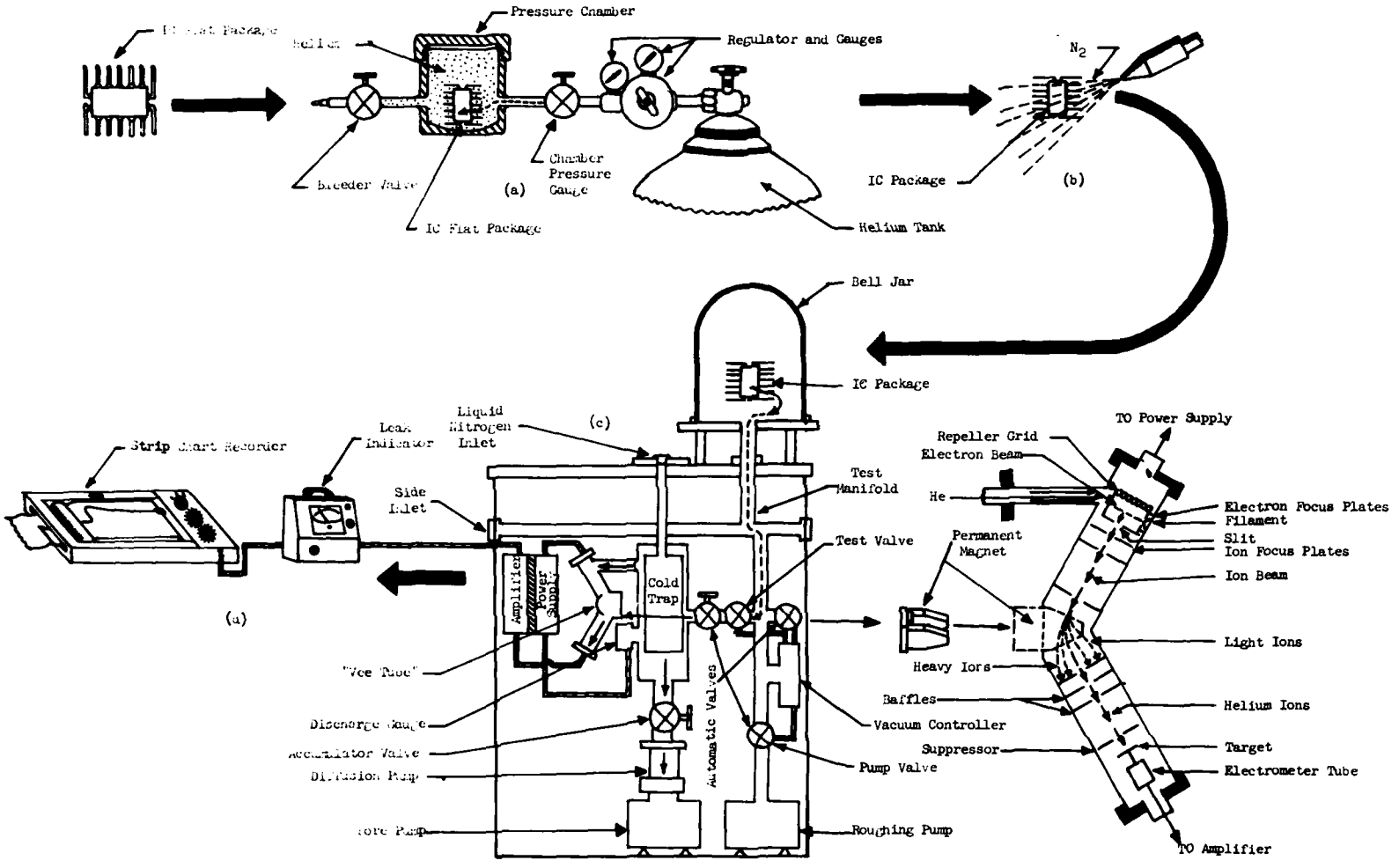


FIGURE 8. MAGNETIC SECTOR MASS SPECTROMETER
(COURTESY OF VEECO INSTRUMENT, INC.)



Package Leak Rate Measurement Flow Diagram Illustrating (a) Helium Pressure Bomb, (b) Nitrogen Flush, (c) Helium Leak Detector Showing Mass Spectrometer, and (d) Readout Electronics.

FIGURE 9. LEAK MEASUREMENT SYSTEM

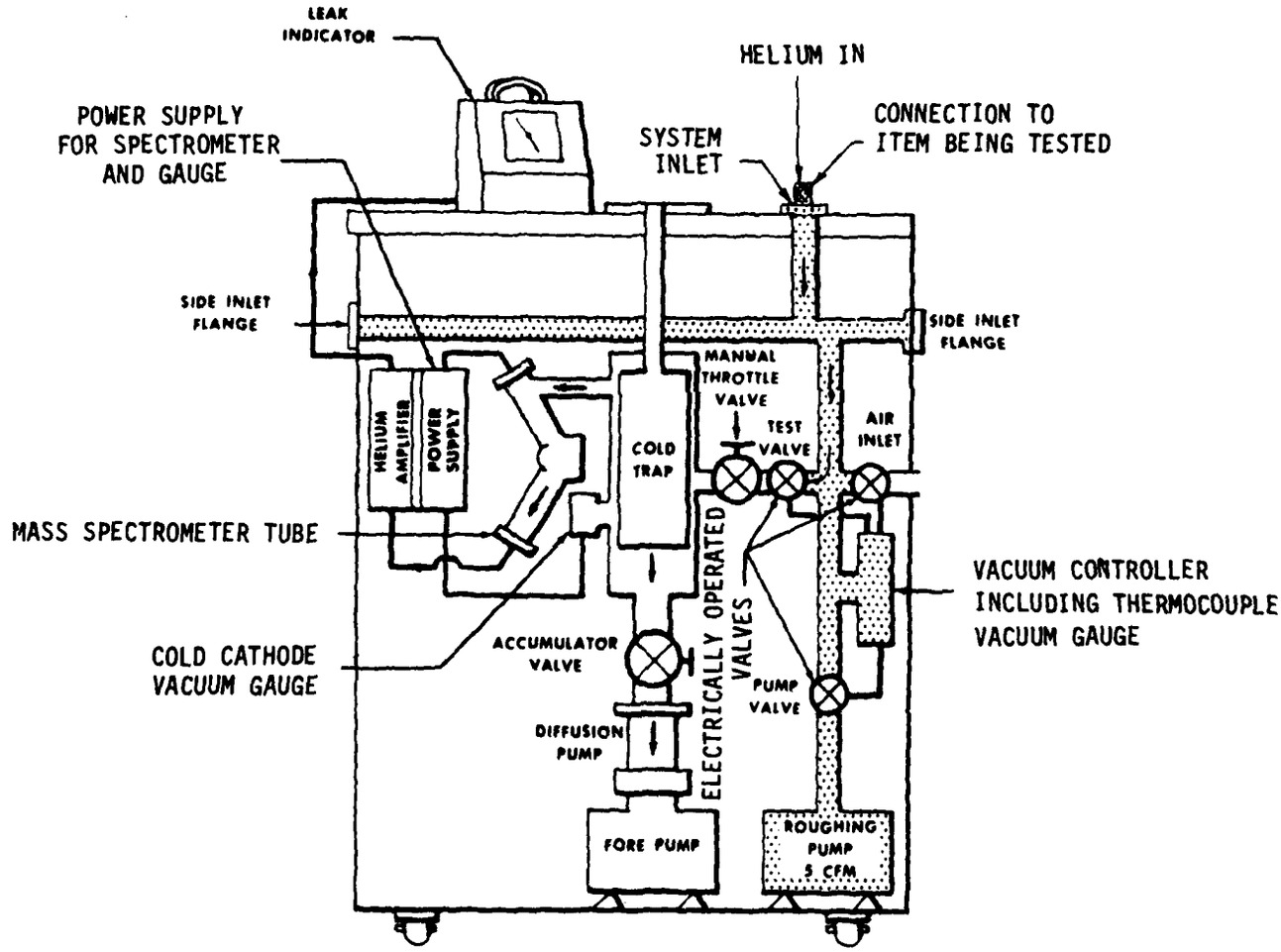


FIGURE 10. LEAK TEST STATION VACUUM SCHEMATIC

(COURTESY OF VEECO INSTRUMENT, INC.)

TABLE I

Glossary of terms used in leak detection

1. Leak — In vacuum technology a hole, or porosity, in the wall of an enclosure capable of passing gas from one side of the wall to the other under action of a pressure or concentration differential existing across the wall.

2. Gross Leak — A leak which exhibits a leak rate in the range of 10^{-4} to 1 atm cc/sec or higher.

3. Fine Leak — A leak which exhibits a leak rate in the range of 10^{-5} to 10^{-10} atm cc/sec or lower.

4. Leak Rate — In leak detection practice *leak rate* is defined as the rate of flow (in pressure-volume units per unit time) through a leak with gas at a specified high pressure (usually atmospheric pressure) on the inlet side and gas at a pressure on the exit side which is low enough to have negligible effect on the rate of flow.

5. Leak Detector — A device for detecting and locating leaks, and indicating the magnitude thereof.

6. Tracer Gas — A gas which, passing through a leak, can then be detected by a specific leak detector and thus disclose the presence of a leak. Also called *search gas*.

7. Probe Gas — A tracer gas which issues from a more-or-less fine orifice so as to impinge on a restricted test area.

8. Pressure Testing — A leak detecting procedure in which tracer gas is introduced under pressure into the encloser under examination, and detected as it is emitted from a leak.

9. Soap Bubble Test — A type of pressure testing in which the tracer gas is detected by bubbles formed in a layer of soap solution applied to the surface of the test object.

10. Vacuum Testing — A leak detecting procedure in which the enclosure under examination is evacuated, the tracer gas applied to the outside surface of the enclosure, and the gas detected after entering the enclosure.

11. Mass Spectrometer Leak Detector — A mass spectrometer adjusted to respond only to tracer gas. Helium is commonly used as the tracer gas, and thus the instrument is normally referred to as a *helium leak detector*.

12. Spectrometer Tube — The sensing element of a mass spectrometer leak detector.

13. Ion Source — That part of a spectrometer tube in which tracer gas is ionized preliminary to being detected.

14. Noise Level — In the case of a leak detector, the spurious output, expressed in suitable terms, exhibited by the detector in the absence of an output due to tracer gas.

15. Background — In the case of a leak detector, the spurious output, expressed in suitable terms, due to the response to other gases than the actual gas being used for probing. The background may be inherent in the detector, or accidental.

16. Minimum Detectable Pressure Change — The pressure producing an indication of three times the noise level.

17. Minimum Detectable Leak — a. The size of the smallest leak, expressed in terms of mass flow per unit time that can be unambiguously detected by a leak detector in the presence of noise and background.

b. The product of the minimum detectable pressure change and the pumping speed at the detector.

18. Probe Test — A leak test in which the tracer gas is applied by means of a probe (see below) so that the area covered by the tracer gas is localized. This enables the individual leaks to be located.

19. Probe — A tube having a fine opening at one end, used for directing a stream of tracer gas.

20. Sampling Probe — A device used in pressure testing and so designed as to collect tracer gas from a restricted area of the test object and feed it to the leak detector. Also called *pressure probe or sniffer*.

21. Hood Test — An overall test in which an object under vacuum test is enclosed by a "hood" which is filled with tracer gas so as to subject all parts of the test object to examination at one time.

22. Isolation Test — A method of determining whether a leak is present in a system, or of obtaining an estimate of its magnitude, by observing the rate of rise of pressure in the evacuated system when the system is isolated from the pump. Also called *rate of rise test*.

23. Masking — The covering of a section of a test object so as to prevent tracer gas from entering leaks that may exist in the covered section.

24. Flooded System — A system which, while being leak tested under vacuum, becomes so filled with tracer gas as to make impracticable further leak detection by means of a probe.

25. Helium Drift — In the case of leak detection with a helium probe, the drift of helium to a leak or permeable gasket located at a point sufficiently remote from the end of the probe to mislead the operator into suspecting the area near the probe.

26. Standard Leak — a. A device which permits leakage through it, at a specified rate, of a specified gas, with atmospheric pressure at one end of the device and a pressure on the other side sufficiently low to have negligible effect on the leak rate.

b. A capillary or porous wall leak, usually in a glass or metal tube, whose dimensions have been adjusted to give a conductance within specified limits for a specified gas at a standard reference temperature with specified inlet and exit pressures. Standard leaks for attaching to vacuum test manifolds with air at atmospheric pressure exposed to the inlet are usually protected by filters to avoid clogging by dust particles. Standard leaks for calibrating mass spectrometers are usually fused to a glass reservoir containing the specified gas at a known high pressure.

c. A device providing a known throughput into a vacuum system. Also referred to as a *calibrated leak*.

Veeco Instruments Inc.
Terminal Drive, Plainview, New York 11803

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12. Leyshon, W.E. "The New Importance of Moisture in Integrated Circuit Packages," Technical Information Bulletin R78ELSO26, General Electric Co., Syracuse, New York, August 1978.

SOME MANUFACTURERS OF HELIUM MASS SPECTROMETER LEAK DETECTORS

1. Alcatel Vacuum Products — $5,000 - $10,000
   60 Sharp Street
   Hingham, MA 02043

2. Edwards High Vacuum Inc.
   3279 Grand Island Blvd.
   Grand Island, N.Y. 14072

3. Leybold-Heraens Vacuum Products Inc.
   200 Seco Road
   Monroeville, PA 15146

4. Vacuum Instrument Corp.
   6 Stepar Place
   Huntington Station, N.Y. 11746

5. Varian Vacuum Division
   121 Hartwell Avenue
   Lexington, MA 02173

6. Veeco Instruments Inc.
   Terminal Drive
   Plainview, N.Y. 11803

APPENDIX I

METHOD 1014.4

SEAL

1. PURPOSE. The purpose of this test is to determine the effectiveness (hermeticity) of the seal of microelectronic and semiconductor devices with designed internal cavities.

1.1 Definitions.

a. Standard leak rate. Standard leak rate is defined as that quantity of dry air at 25°C in atmosphere cubic centimeters flowing through a leak or multiple leak paths per second when the high-pressure side is at 1 atmosphere (760 mm Hg absolute) and the low-pressure side is at a pressure of not greater than 1 mm Hg absolute. Standard leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm cc/sec).

b. Measured leak rate. Measured leak rate (R_1) is defined as the leak rate of a given package as measured under specified conditions and employing a specified test medium. Measured leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm cc/sec). For the purpose of comparison with rates determined by other methods of testing, the measured leak rates must be converted to equivalent standard leak rates.

c. Equivalent standard leak rate. The equivalent standard leak (L) of a given package, with a measured leak rate (R_1), is defined as the leak rate of the same package with the same leak geometry, that would exist under the standard conditions of 1.1 a. The formula (does not apply to test condition B) in 3.1.1.2 represents the L/R ratio and gives the equivalent standard leak rate (L) of the package with a measured leak rate (R_1) where the package volume and leak test conditioning parameters influence the measured value of (R_1). The equivalent standard leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm cc/sec).

2. APPARATUS. The apparatus required for the seal test shall be as follows for the applicable test condition:

2.1 Test conditions A_1, A_2, and A_4 1/ - Tracer gas helium (He) fine leak. Apparatus required shall consist of suitable pressure and vacuum chambers and a mass spectrometer-type leak detector preset and properly calibrated for a helium leak rate sensitivity sufficient to read measured helium leak rates of 10-9 atm cc/sec and greater. The volume of the chamber used for leak rate measurement should be held to the minimum practical, since this chamber volume has an adverse effect on sensitivity limits. The leak detector indicator shall be calibrated using a diffusion-type calibrated standard leak at least once during every working shift. In addition for test condition A_4, the following apparatus is required:

a. Fixture and fittings to mate the package to be tested to the leak detector.
b. Surgical rubber gasket.
c. Apeizon grease (type M or N) or equivalent.

2.2 Test condition B - Radioisotope fine leak. Apparatus for this test shall consist of:

a. Radioactive tracer gas activation console.
b. Counting equipment consisting of a scintillation crystal, photomultiplier tube, preamplifier, ratemeter, and krypton-85 reference standards. The counting station shall be of sufficient sensitivity to determine through the device wall the radiation level of any krypton-85 tracer gas present within the device. The counting station shall have a minimum sensitivity corresponding to a leak rate of 10-9 atm cc/sec of krypton-85 and shall be calibrated at least once every working shift using krypton-85 reference standards and following the equipment manufacturer's instruction.

1/ A_3 was intentionally omitted.

e. A tracer gas consisting of a mixture of krypton-85 and dry nitrogen. The concentration of krypton-85 in dry nitrogen shall be no less than 100 microcuries per atmospheric cubic centimeter. This value shall be determined at least once each 30 days and recorded in accordance with the calibration requirements of this standard (see 4.3.4 of MIL-STD-883).

2.3 Test condition C - Fluorocarbon gross leak. Apparatus for this test shall consist of:

a. A vacuum/pressure chamber for the evacuation and subsequent pressure bombing of devices up to 75 psig up to 10 hours.
b. A suitable observation container with provisions to maintain the indicator fluid at a temperature of 125°C and a filtration system capable of removing particles greater than 1 micron in size from the fluid.
c. A magnifier with a magnification in the range between 3X to 30X for observation of bubbles emanating from devices when immersed in the indicator fluid.
* d. Sources of FC-72, FE-2, or PP-1 fluorocarbon detector fluids, and FC-40, FC-43, PP-7, FE-4, or PP-9 fluorocarbon indicator fluids.
e. A lighting source capable of producing at least 15 thousand foot candles in air at a distance equal to that which the most distant device in the bath will be from the source. The lighting source shall not require calibration but the light level at the point of observation (i.e., where the device under test is located during observation for bubbles) shall be verified.
f. Suitable calibrated instruments to indicate that test temperatures, pressures, and times are as specified.
g. Suitable fixtures to hold the device(s) in the indicator fluid.

2.4 Test condition D - Penetrant dye gross leak. The following apparatus shall be used for this test:

a. Ultraviolet light source with peak radiation at approximately the frequency causing maximum reflection of the dye (3650 A for Zyglo; 4935 A for Fluorescein; 5560 A for Rhodamine B, etc.,).
b. Pressure chamber capable of maintaining 90 psig.
c. Solution of fluorescent dye (such as Rhodamine B, Fluorescein, By-check, Zyglo, FL-50, or equivalent) mixed in accordance with the manufacturer's specification.
d. A magnifier with a magnification in the range between 3X to 30X for dye observation.

2.5 Test condition E - Weight gain gross leak. Apparatus for this test shall consist of:

a. A vacuum/pressure chamber for the evacuation and subsequent pressure bombing of devices up to 75 psig up to 10 hours.
b. An analytical balance capable of weighing the devices accurately to 0.1 milligram.
c. A source of FC-72 or fluorocarbon fluid.
d. A filtration system capable of removing particles greater than 1 micron in size from the fluorocarbon fluid.
e. Suitable calibrated instruments to measure test pressures and times.
f. A source of Freon TF.

3. PROCEDURE. Fine and gross leak tests shall be conducted in accordance with the requirements and procedures of the specified test condition. Testing order shall be fine leak (condition A or B) followed by gross leak (condition C, D, or E). When specified (see 4), measurements after test shall be conducted following the leak test procedures. Where bomb pressure specified exceeds the microcircuit package capability, alternate pressure, exposure time, and dwell time conditions may be used provided they satisfy the leak rate, pressure, time relationships which apply, and provided no less than 30 psig bomb pressure is applied in any case. When test condition A4 is used, gross leak testing is not required. However A4 shall not be used in lieu of the required seal testing of lidded packages. When batch testing (more than one device in the leak detector at one time) is used in

performing test condition A or B and a reject condition occurs it shall be noted as a batch failure. Each device may then be tested individually one time for acceptance if all devices in the batch are retested within one hour after removal from the tracer gas pressurization chamber.

3.1 Test condition A_1, A_2, or A_4 - Tracer gas (He) fine leak. Test condition A_1 is a "fixed" method with specified conditions per table I that will ensure the test sensitivity necessary to detect the required measured leak rate (R_1). Test condition A_2 is a "flexible" method that allows the variance of test conditions in accordance with the formula of 3.1.1.2 to detect the specified equivalent standard leak rate (L) at a predetermined leak rate (R_1). Test condition A_4 is a method that will detect the required measured leak rate (R_1) of an unsealed package.

3.1.1 Test conditions A_1 and A_2 - Procedure applicable to "fixed" and "flexible" methods. The completed device(s), shall be placed in a sealed chamber which is then pressurized with a tracer gas of 100 +0, -5 percent helium for the required time and pressure. The pressure shall then be relieved and each specimen transferred to another chamber or chambers which are connected to the evacuating system and a mass-spectrometer-type leak detector. When the chamber(s) is evacuated, any tracer gas which was previously forced into the specimen will thus be drawn out and indicated by the leak detector as a measured leak rate (R_1). (The number of devices removed from pressurization for leak testing shall be limited such that the test of the last device can be completed within 60 minutes for test condition A_1 or within the chosen value of dwell time t_2 for test condition A_2.)

3.1.1.1 Test condition A_1 - Fixed method. The devices(s) shall be tested using the appropriate conditions specified in table I for the internal cavity volume of the package under test. The time t_1 is the time under pressure and time t_2 is the maximum time allowed after release of pressure before the device shall be read. The fixed method shall not be used if the maximum equivalent standard leak rate limit given in the procurement document is less than the limits specified herein for the flexible method.

TABLE I. Fixed conditions for test condition A_1.

Volume of package (cc)	Bomb condition			R1
	Psig	Exposure time hours	Maximum dwell hours	Reject limit (atm cc/secHe)
V < 0.40	60±2	2 +0.2, -0	1	5 x 10-8
V ≥ 0.40	60±2	2 +0.2, -0	1	2 x 10-7
V ≥ 0.40	30±2	4 +0.4, -0	1	1 x 10-7

3.1.1.2 Test condition A_2 - Flexible method. Values for bomb pressure exposure time, and dwell time shall be chosen such that actual measured tracer gas leak rate (R_1) readings obtained for the devices under test (if defective) will be greater than the minimum detection sensitivity capability of the mass spectrometer. The devices shall be subjected to a minimum of 2 atmospheres absolute of helium atmosphere. If the chosen dwell time (t_2) is greater than 60 minutes, graphs shall be plotted to determine an R_1 value which will assure overlap with the selected gross leak test condition. The chosen values, in conjunction with the value of the internal volume of the device package to be tested and the maximum equivalent standard leak rate (L) limit (as shown below or as specified in the applicable procurement document), shall be used to calculate the measured leak rate (R_1) limit using the following formula:

$$R_1 = \frac{LP_E}{P_0}\left(\frac{M_A}{M}\right)^{1/2}\left\{1 - e^{-\left[\frac{Lt_1}{VP_0}\left(\frac{M_A}{M}\right)^{1/2}\right]}\right\} e^{-\left[\frac{Lt_2}{VP_0}\left(\frac{M_A}{M}\right)^{1/2}\right]}$$

Where:

R_1 = The measured leak rate of tracer gas (He) through the leak in atm cc/secHe.
L = The equivalent standard leak rate in atm cc/sec.
P_E = The pressure of exposure in atmospheres absolute.
P_O = The atmospheric pressure in atmospheres absolute. (1)
M_A = The molecular weight of air in grams. (28.7)
M = The molecular weight of the tracer gas (Helium) in grams. (4)
t_1 = The time of exposure to P_E in seconds.
t_2 = The dwell time between release of pressure and leak detection, in seconds.
V = The internal volume of the device package cavity in cubic centimeters.

3.1.1.2.1 Failure criteria. Unless otherwise specified, devices with an internal cavity volume of 0.01 cc or less shall be rejected if the equivalent standard leak rate (L) exceeds 5×10^{-8} atm cc/sec. Devices with an internal cavity volume greater than 0.01 cc and equal to or less than 0.4 cc shall be rejected if the equivalent standard leak rate (L) exceeds 1×10^{-7} atm cc/sec. Devices with an internal cavity volume greater than 0.4 cc shall be rejected if the equivalent standard leak rate (L) exceeds 1×10^{-6} atm cc/sec.

3.1.2 Test condition A_4 - Procedure applicable to the unsealed package method. The fixture and fittings of 2.1a. shall be mounted to the evacuation port of the leak detector. Proof of fixturing integrity shall be verified by sealing a flat surfaced metal plate utilizing the gasket and grease of 2.1 and measuring the response of the leak test system. Testing shall be performed by sealing the package(s) to the evacuation port and the package cavity evacuated to 5×10^{-7} atm cc/sec. Care shall be taken to prevent contact of grease with package (seal ring not included) to avoid masking leaks. The external portion of the package shall be flooded with Helium gas either by the use of an envelope or a spray gun, at a pressure of 30 psig.

3.1.2.1 Failure criteria. Unless otherwise specified, devices shall be rejected if the measured leak rate (R_1) exceeds 1×10^{-8} atm cc/secHe.

3.2 Test condition B - Radioisotope fine leak test.

3.2.1 Activation parameters. The activation pressure and soak time shall be determined in accordance with the following equation:

$$Q_S = \frac{R}{skT\overline{P}t} \qquad (1)$$

The parameters of equation (1) are defined as follows:

Q_S = The maximum calculated leak rate allowable, in atm cc/secKr, for the devices to be tested.
R = Counts per minute above the ambient background after activation if the device leak rate were exactly equal to Q_S. This is the reject count above the background of both the counting equipment and the component, if it has been through prior radioactive leak tests.
s = The specific activity, in microcuries per atmosphere cubic centimeter, of the krypton-85 tracer gas in the activation system.
k = The overall counting efficiency of the scintillation crystal in counts per minute per microcurie of krypton-85 in the internal void of the specific component being evaluated. This factor depends upon component configuration and dimensions of the scintillation crystal. The counting efficiency shall be determined in accordance with 3.2.2.
T = Soak time, in hours, that the devices are to be activated.
P = $P_e^2 - P_i^2$, where P_e is the activation pressure in atmospheres absolute and P_i is the original internal pressure of the devices in atmospheres absolute. The activation pressure (P_e) may be established by specification or if a convenient soak time (T) has been established, the activation pressure (P_e) can be adjusted to satisfy equation (1).
t = Conversion of hours to seconds and is equal to 3,600 seconds per hour.

NOTE: The complete version of equation (1) contains a factor (P_O^2 - $(\Delta P)2$) in the numerator which is a correction factor for elevation above sea level. P_O is sea level pressure in atmospheres absolute and ΔP is the difference in pressure, in atmospheres between the actual pressure at the test station and sea level pressure. For the purpose of this test method, this factor has been dropped.

3.2.2 Determination of counting efficiency (k). The counting efficiency (k) of equation (1) shall be determined as follows:

a. Five representative units of the device type being tested shall be tubulated and the internal void of the device shall be backfilled through the tubulation with a known volume and known specific activity of krypton-85 tracer gas and the tubulation shall be sealed off.
b. The counts per minute shall be directly read in the shielded scintillation crystal of the counting station in which the devices are read. From this value, the counting efficiency, in counts per minute per microcurie, shall be calculated.

3.2.3 Evaluation of surface sorption. All device encapsulations consisting of glass, metal, and ceramic or combinations thereof, including coatings and external sealants, shall be evaluated for surface sorption of krypton-85 before establishing the leak test parameters. Representative samples of the questionable material shall be subjected to the predetermined pressure and time conditions established for the device configuration as specified by 3.2.1. The samples shall then be counted every 10 minutes, with count rates noted, until the count rate becomes asymptotic with time. (This is the point in time at which surface sorption is no longer a problem.) This time lapse shall be noted and shall determine the "wait time" specified in 3.2.4.

3.2.4 Procedure. The devices shall be placed in radioactive tracer gas activation tank. The activation chamber may be partially filled with inert material to reduce pumpdown time. The tank shall be evacuated to 0.5 torr. The devices shall be subjected to a minimum of 2 atmospheres absolute pressure of krypton-85/dry nitrogen mixture for a minimum of 12 minutes. Actual pressure and soak time shall be determined in accordance with 3.2.1. The R value in counts per minute shall not be less than 600 above background. The krypton-85/dry nitrogen gas mixture shall be evacuated to storage until 0.5 torr vacuum exists in the activation tank. This evacuation shall be completed within 3 minutes maximum. The activation tank shall then be backfilled with air (air wash). The devices shall then be removed from the activation tank and leak tested within 1 hour after gas exposure with a scintillation-crystal-equipped counting station. Device encapsulations that come under the requirements of 3.2.3 shall be exposed to ambient air for a time not less than the "wait time" determined by 3.2.3. In no case will the time between removal from the activation chamber and test exceed 1 hour. This exposure shall be performed after gas exposure but before determining leak rate with the counting station. Device encapsulations that do not come under the requirements of 3.2.3 may be tested without a "wait time." (The number of devices removed from pressurization for leak testing shall be limited such that the test of the last device can be completed within 1 hour.) The actual leak rate of the component shall be calculated with the following equation:

$$Q = \frac{(\text{ACTUAL READOUT IN NET COUNTS PER MINUTE}) \times Q_S}{R}$$

Where Q = Actual leak rate in atm cc/sec, and Q_S and R are defined in 3.2.1.

3.2.5 Failure criteria. Unless otherwise specified, devices that exhibit a leak rate equal or greater than the test limits of table II shall be considered as failures.

TABLE II. Test limits for radioisotope fine leak method.

Volume of package cc	Calculated Q
< 0.01	1 x 10-8
≥ 0.01	5 x 10-8

3.2.6 Personnel precautions. Federal, some state and local governmental regulations require a license for the possession and use of krypton-85 leak test equipment. In the use of radioactive gas, these regulations and their maximum permissible exposure and tolerance levels prescribed by law should be observed.

3.3 Test condition C - Fluorocarbon gross leak.

3.3.1 Procedure. The devices shall be placed in a vacuum/pressure chamber and the pressure reduced to 5 torr and maintained for 1 hour except that for devices with an internal volume ≥ 0.1 cc, this vacuum cycle may be omitted. A sufficient amount of FC-72 or equivalent detector fluid shall be admitted to cover the devices. When the vacuum cycle is performed, the fluid will be admitted after the 1-hour period but before breaking the vacuum. For devices with an internal cavity volume < 0.1 cc, the pressure shall then be increased to 60 +5, -0 psig for a duration of 2 hours minimum - also for devices with an internal cavity volume of less than 0.05 cc an acceptable alternate condition is a pressure of 75 +5, -0 psig for 1 hour minimum; for devices with an internal cavity volume ≥ 0.1 cc, if the package cannot be subjected to 60 +5, -0 psig, the pressure shall be increased to 30 +5, -0 psig (or 45 +5, -0 psig if the vacuum cycle was omitted) and maintained for a duration of 10 hours minimum. At the end of this time, the pressure shall be released and the devices removed from the pressure chamber and retained continuously immersed in a bath, of the detector fluid. When the devices are removed from the bath they shall be dried for 2 ±1 minutes in air prior to immersion in FC-40 or equivalent indicator fluid, which shall be maintained at 125° ±5°C. The devices shall be immersed with the uppermost portion at a minimum depth of 2 inches below the surface of the indicator fluid, one at a time or in such a configuration that a single bubble from a single device out of a group under observation may be clearly observed as to its occurrence and source. The device shall be observed against a dull, non-reflective black background through the magnifier, while illuminated by the lighting source, from the instant of immersion until expiration of a 30-second minimum observation period, unless rejected earlier.

3.3.2 Failure criteria. A definite stream of bubbles or two or more large bubbles originating from the same point shall be cause for rejection.

3.3.3 Precautions. The following precautions shall be observed in conducting the fluorocarbon gross leak test:

a. Fluorocarbons shall be filtered through a filter system capable of removing particles greater than 1 micron prior to use. Bulk filtering and storage is permissible. Liquid which has accumulated observable quantities of particulate matter during use shall be discarded or reclaimed by filtration for re-use. Precaution should be taken to prevent contamination.
b. Observation container shall be filled to assure coverage of the device to a minimum of 2 inches.
c. Devices to be tested should be free from foreign materials on the surface, including conformal coatings and any markings which may contribute to erroneous test results.
d. A lighting source capable of producing at least 15 thousand foot candles in air at a distance equal to that which the most distant device in the bath will be from the source. The lighting source shall not require calibration but the light level at the point of observation (i.e., where the device under test is located during observation for bubbles) shall be verified.
e. Precaution should be taken to prevent operator injury due to package rupture or violent evolution of bomb fluid when testing large packages.

3.4 Test condition D - Penetrant dye gross leak. This test shall be permitted only on transparent glass encased devices or for destructive verification of opaque devices (see 3.6). The pressure chamber shall be filled with the dye solution to a depth sufficient to completely cover all the devices. The devices shall be placed in the solution and the chamber pressurized at 90 psig minimum for 3 hours minimum. For device packages which will not withstand 90 psig, 45 psig for 10 hours may be used. The devices shall then be removed and carefully washed, using a suitable solvent for the dye used, followed by an air-jet dry. The devices shall then be examined under the magnifier using an ultraviolet light source of appropriate frequency.

3.4.1 Failure criteria. Any evidence of dye penetration into the device shall constitute a failure.

3.5 Test condition E - Weight gain gross leak.

3.5.1 Procedure. The devices shall be cleaned by placing them in a container of clean Freon TF at 25°C and allowed to soak for 2 minutes minimum. The devices shall then be removed and placed in an oven at 125°C for 1 hour minimum, after which they shall be allowed to cool to room ambient temperature. Each device shall be weighed and the initial weight recorded or the devices may be categorized into cells as follows. Devices having a volume of < 0.01 cc shall be categorized in cells of 0.5 milligram increments and devices with volume ≥ 0.01 cc shall be categorized in cells of 1.0 milligram increments. The devices shall be placed in a vacuum/pressure chamber and the pressure reduced to 5 torr and maintained for 1 hour except that for devices with an internal cavity volume ≥ 0.1 cc, this vacuum cycle may be omitted. A sufficient amount of FC-72 fluorocarbon or equivalent fluid shall be admitted to the pressure chamber to cover the devices. When the vacuum cycle is performed, the fluid shall be admitted after the 1-hour period but before breaking the vacuum. The devices shall then be pressurized to 60 psig except that 75 psig shall be used when the vacuum cycle has been omitted. The pressure shall be maintained for 2 hours minimum. If the devices will not withstand the 60 psig test pressure, the pressure may be lowered to 30 psig with the vacuum cycle and the pressure maintained for 10 hours minimum. Upon completion of the pressurization period, the pressure shall be released and the devices removed from the pressure chamber and retained in a bath of the fluorocarbon fluid. When the devices are removed from the fluid they shall be air dried for 2 $\pm$1 minutes prior to weighing. Transfer the devices singly to the balance and determine the weight or weight category of each device. All devices shall be tested within 4 minutes following removal from the fluid. The delta weight shall be calculated from the record of the initial weight and the post weight of the device. Devices which were categorized shall be separated into two groups, one group which shall be devices which shifted one cell or less and the other group which shall be devices which shifted more than one cell.

3.5.2 Failure criteria. A device shall be rejected if it gains 1.0 milligram or more and has an internal cavity volume of < 0.01 cc or 2.0 milligrams or more if the internal cavity volume is ≥ 0.01 cc. If the devices are categorized, and device which gains enough weight to cause it to shift by more than one cell shall be considered a reject. A device which loses weight of an amount which if gained would cause the device to be rejected may be retested after it is baked at 125°C for a period of 8 hours.

3.6 Retest. Devices which fail gross leak (test conditions C and D) may be retested destructively for verification purposes only. Devices which fail fine leak (test conditions A_1, A_2, A_4, or B) shall not be retested for acceptance unless specifically permitted by the applicable procurement document. Where fine leak retest is permitted, the entire leak test procedure for the specified test condition shall be repeated. That is, retest consisting of a second observation on leak detection without a re-exposure to the tracer fluid or gas under the specified test condition shall not be permissible under any circumstances. Preliminary measurement to detect residual tracer gas is advisable before any retest.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

a. Test condition letter when a specific test is to be applied (see 3).
b. Accept or reject leak rate for test condition A or B when other than the accept or reject leak rate specified herein applies (see 3.1.1.1, 3.1.1.2, 3.1.2, and 3.2.4).

c. Where applicable, measurements after test (see 3).
d. Retest acceptability for test conditions A and B (see 3.6).
e. Order of performance of fine and gross if other than fine followed by gross (see 3).
f. Where applicable, the device package pressure rating shall be specified if that rating is less than 60 psig.

APPENDIX II

Derivation of the Radiflo Equation

$$Q\ \frac{\text{atm cc}}{\text{sec}} = \frac{R\ (\text{cts/sec})}{S\left(\frac{\mu c}{\text{atm cc}}\right)\ K\left(\frac{\text{cts/sec}}{\mu c}\right) T(\text{sec})} \qquad \frac{(P_o^{\,2} - 0)}{(P_e^{\,2} - P_i^{\,2})}$$

All pressures are absolute and defined as follows:

P_o = atmospheric pressure

P_e = "exposure" pressure or pressure of radioactive gas in tank

P_i = internal pressure inside part being tested

If pressures are expressed in atmospheres, then:

$$P_o = 1;\ (P_o^{\,2} - 0) = 1$$

and the above equation becomes:

$$Q\ \frac{\text{atm cc}}{\text{sec}} = \frac{R}{SKT\ (P_e^{\,2} - P_i^{\,2})}$$

where:

P_e & P_i = "exposure" pressure and part internal pressure expressed in atm

R = net counting rate of tested part

S = specific activity of gas contained within the tested part

K = Counting efficiency of the system

T = "exposure" time

A. If we assume Poiseuilles (laminar/viscous) flow:

1. Reynolds number is less than critical for turbulent flow.

2. $\frac{T}{a} < 10; \frac{To}{a(Pavg)}$ where: T = mean free path of radioactive gas in cm

To = m.f.p. in cm at 1 atm

a = radius of flow channel in cm.

Pavg = Average pressure across the flow channel in atm

3. The flow is steady, which means that the changes in the pressure at either end of the flow channel are sufficiently small that no acceleration of flow exists in the flow channel.

B. Assume isothermal conditions (the viscosity of a gas is a function of its temperature and this consideration is necessary in comparing two Poiseuille flow rates at different pressures).

C. Define standard leak rate as that flow in atm cc/sec of air which would exist in a flow channel if the driving pressure remained constant at one atm absolute and the receiver pressure remained constant at zero atm absolute.

D. Let M = amount of gas (atm cc) which enters a part during exposure in the tank

T = time (sec) for M to enter part during exposure

Pe = exposure pressure (atm)

P_i = internal pressure of the part (atm)

a = effective radius of flow (leak) channel (cm)

ℓ = effective length of flow (leak) channel (cm)

Qt = flow rate of M into part during exposure $(\frac{\text{atm cc}}{\text{sec}})$

Qs = flow rate of M into part under conditions of standard leak defined in (C) above $(\frac{\text{atm cc}}{\text{sec}})$

Q_{avg} = average flow rate of M into part during exposure $(\frac{\text{atm cc}}{\text{sec}})$

E. $Q_{avg} = \frac{M}{T}$

F. $Q_t = K\frac{a^4}{\ell} (P_e^2 - P_i^2)$

G. $Q_s = K\frac{a^4}{\ell} (P_o^2 - 0^2)$

For any given part where Poiseuilles flow exists, it is true that:

H. $\frac{Q_s}{Q_t} = \frac{P_o^2 - 0^2}{P_e^2 - P_i^2}$

I. $Q_s = Q_t (\frac{P_o^2 - 0^2}{P_e^2 - P_i^2}) = Q_t (\frac{P_o^2}{P_e^2 - P_i^2})$

Now by the conditions of Poiseuilles flow and steady flow:

J. $Q_t = Q_{avg} = \frac{M}{T}$

$$Q_s = \frac{M}{T}\left(\frac{P_o^2}{P_e^2 - P_i^2}\right) = \frac{M}{T(P_e^2 - P_i^2)}$$

where pressures are in atm absolute.

K. Now the amount of gas M, present within the part can be determined by radiation counting if:

R = net counting rate of part $(\frac{counts}{sec})$ or $(\frac{cts}{sec})$.

S = specific activity of gas contained within part $(\frac{\mu\ curies}{atm\ cc})$.

K = Counting efficiency of system $(\frac{cts}{sec\ \mu\ curies})$.

so that,

L. $$M(atm\ cc) = \frac{R(\frac{cts}{sec})}{S\ (\frac{\mu\ c}{atm\ cc})\ K\ (\frac{cts}{sec\ \mu\ c})}$$

Consequently the expression for Qs becomes:

M. $$Q_s = (\frac{R}{SK})\ \frac{1}{T}\ (\frac{1}{P_e^2 - P_i^2})$$

$$Q_s = \frac{R}{SKT\ (P_e^2 - P_i^2)}\ (\frac{atm\ cc}{sec})$$

D.

PACKAGE AMBIENT GAS ANALYSIS TECHNIQUES

D. Package Ambient Gas Analysis Techniques

1. Introduction. Gas analysis of hermetic containers has been performed for more than 25 years using mass spectrometry. Some of the earliest work was done on relay cans and vacuum tubes. Because of the relatively large volumes (i.e., > 10 ccm) the techniques utilized straightforward leak valve sampling procedures. While these techniques are not accurate in an absolute sense, they do provide usable relative concentrations of the gaseous constitutents present inside these hermetic enclosures. They were, in fact, directly responsible for extending the operating life of relay contacts and vacuum tubes. It was not until 1970 that techniques for gas analysis of small volume enclosures were investigated. It was soon apparent that small volume analysis of moisture was a much more difficult problem. With proper care and calibration, it was possible to obtain better than 10% accuracy on all of the gases found in air with the exception of water vapor. As late as 1978, correlation between laboratories was, with respect to moisture determinations, sometimes worse than an order of magnitude. Since then a number of round robin tests have been conducted under carefully controlled conditions, i.e., MIL-STD-883, Method 1018.2 (Appendix A). As of June 1980, correlation has been established at 5000 ppm moisture (±20%) for packages with volumes between .01 ccm to .85 ccm at the four commercial gas analysis laboratories identified and RADC (Appendix B). It should be noted that correlation has not been demonstrated for lower moisture limits or for packages containing organic die attach material or dessicants. The ability to correlate moisture measurements at 500 ppm for small packages is still several years away. This does not imply that moisture measurements from gas analysis laboratories are not meaningful below 5000 ppm. On the contrary, the relative dryness or wetness of a package does provide guidance for process improvement. For these experiments the trend rather than absolute accuracy is important. A nomograph

relating microelectronic package ambient dew point (the temperature at which moisture will condense from vapor), the package internal pressure, and moisture concentration in ppm_v is shown in Figure 1.

2. Package Ambient Components and Their Interpretation. It will be useful to list various gaseous components often found in IC packages and the conclusions that can be drawn from their presence.

a) Moisture. Water provides mobility for ions in electrochemical reactions and electric charge transport. It is probably the most damaging contaminant because it plays a part in many failure mechanisms. In some cases, its presence is necessary and sufficient to cause failures; in others, it is necessary but not sufficient; that is, other contaminants or structural conditions must also be present. Moisture typically is brought into the package adsorbed on the walls of the enclosure or is due to loss of package hermiticity and subsequent transfer of external ambients into the internal package cavity. The dryness of the sealing environment has little effect on the final moisture contact of the package (i.e., more than enough moisture is adsorbed on the walls of the package to bring the ambient to a wet condition).

b) Failure Mechanisms Related to Moisture are:

- Corrosion
- Electrical surface leakage
- Electrochemical metal migration
- Electrical degradation of bulk oxide (gate turn-on) or polar inversion layers

c) Oxygen. Oxygen gas in packages can cause aluminum oxidation during high temperature burn-in or operation. This

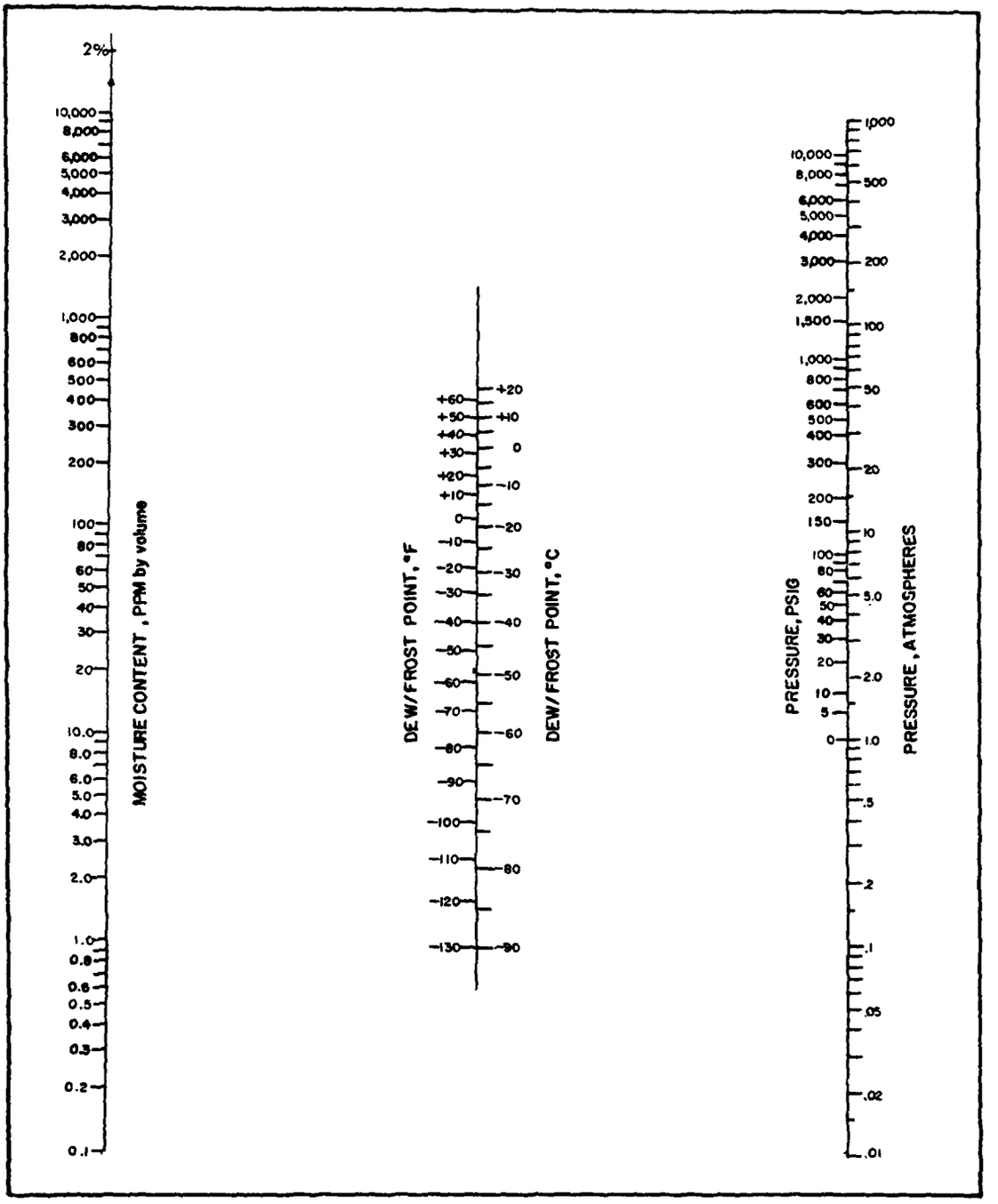


FIGURE 1. NOMOGRAPH FOR DEW POINT AND PPMV AS A FUNCTION OF P.

can lead to a beneficial passivation. It has been shown to be necessary in the case of solder glass sealed parts (CERDIPS) to have from 10 to 20% oxygen in the sealing furnace. Since oxygen is consumed at high temperature, the residual oxygen left in the package is very often less than half the amount specified in the sealing furnace. In a negative way, oxygen has been implicated in beta shift in some bipolar devices because of its polar effect on surface charge inversion.

d) Argon. Since argon is inert, it makes an excellent tracer gas for independent leak assessment. If the parts are sealed in nitrogen or nitrogen-oxygen mixtures, the detection of argon as a residual gas usually signifies that the packages became non-hermetic sometime after seal. Seal leakage may occur even though the package will pass fine and gross leak test since leakage paths can easily plug or dissimilar material seals may open temporarily during thermal excusions. Noting other gaseous components accompanying argon can often identify at what point in the package history that hermeticity was lost.

e) Carbon Dioxide. Carbon dioxide readily forms electron attachment (negative) ions which can affect surface charge status. When dissolved in water, it forms a weak acid that can promote galvanic corrosion. Finally, when CO_2 is found in a package, it can be interpreted as one of the end products in a sealing furnace ambient or the oxidation of a hydrocarbon residue associated with package materials or contamination, some of which may still be present on the chip or in the package.

f) Helium or Freon. Usually indicates a fine or gross leak condition is present or has occurred at some time prior to gas analysis, e.g., screen escapes. Correlate with argon, total pressure, oxygen or other contaminants to determine mechanism.

g) Methane. Often produced during analysis as the fractionated portion of some heavier hydrocarbon (i.e., grease or oil).

h) Pump Oil. From contaminated vacuum bakeout ovens (mass 55, 56, 57).

i) Chlorine. A fractionated ion formed from a chlorinated hydrocarbon. Free chlorine is too reactive to exist as a free molecule.

j) Halogen Compounds. Halogen compound residues are always cause for alarm because they can so readily initiate aluminum corrosion in the presence of traces of moisture. In this case, halogens do not usually become chemically bound in the reaction products. Instead, they play an intermediate role in breaching the normally protective aluminum oxide. The exposed aluminum metal then reacts with water to form hydrated aluminum oxide.

Since many process chemicals and solvents contain halogens (e.g., freons, trichloroethane), it is important to prevent these solvent residues from contacting water on the device surface. The resulting hydrolysis reaction (which is catalyzed by many metals) produces halogen acids directly from the supposedly inert solvents.

k) Hydrogen. Hydrogen gas is seldom found in significant amounts except when deliberately introduced as part of a "forming" gas mixture used to stabilize MOS type devices. It may outgas in small quantities from Kovar or ferrous metals or be entrapped in electroplated coatings. Hydrogen ions (protons) are highly mobile charge carriers in silicon oxide, with a mobility comparable to the notorious sodium ions.

l) Organic Vapors Many organic vapors have been found in semiconductor packages from sources such as solvent residues, photo resist processes, epoxy bonding, etc. Most of them are relatively harmless and have not been directly correlated with failures. They sometimes are indicative of sloppy processing and should be noted for that reason. Some organic residues that are detected by their vapors may contain impurity metal ions in the solid state which can be surface charge carriers.

m) Miscellaneous. In at least one case, acetic acid was detected during mass spectrometer analysis. It was traced to the use of single component silicone "bathtub" resin, which, of course, should never be used in microelectronic applications. In this instance, the acetic acid destroyed the Dumet seals on glass signal diodes.

Amines are sometimes detected from epoxy curing systems and may contribute to aluminum corrosion, since aluminum is amphoteric.

Device malfunction may occur in the presence of only trace amounts of the gaseous species discussed above. As seen in Table I, the volume of gas in a sealed package may be as low as 0.01 cm^3. This limits the quantity of gas available for analysis. In addition, the gas must be transferred from the opened package to the instrument used for analysis. These facts impose significant demands on the technique of analysis for the identification and quantification of the components of package ambient gas.

TABLE I PACKAGE VOLUMES

Packages	Typical Volumes, cm^3
TO-5	0.168-0.215
TO-18	0.034
CERDIPS, FLATPACKS	0.012-1.18
DIODES	0.01

3. Analytical Techniques. Since microelectronic packages are usually backfilled with dry nitrogen gas or air near atmospheric pressure before being hermetically sealed, a technique capable of identifying and mesuring very small amounts of gas in the presence of a large quantity of nitrogen is required. A technique eminently suitable for this task is mass spectrometry.

A word of caution to the neophyte in moisture analysis or the residual gas analysis technician: past experience has been that changing over an RGA or GC-MS system to obtain correlatable moisture readings usually requires a large amount of senior engineer manhours as well as technician time. Typical conversion time would be at least 6 months to sometimes more than a year. Even purchasing a turn-key system such as that available from Pernika Corp. will require months of training to understand how the many system variables affect the analysis results. Therefore, before embarking on setting up a moisture analysis system for microelectronic devices, a very careful and realistic cost trade-off analysis should be performed. Current system cost is approximately $120K to $150K.

a) Mass Spectrometric Method. A mass spectrometer is an instrument that produces gaseous ions from a sample, separates these ions, detects them, and records their relative abundances as a function of their mass-to-charge (m/z) ratios. This record is called a mass spectrum.

Types of Commonly Available Mass Spectrometers

- Quadrupole & Monopole
- Magnetic Sector
- Time-of-Flight

Of the three types of instruments generally available, the relatively small size and fast scan rates that can be achieved with the quadrupole have made it the most popular choice for gas analyzers.

The incorproation of a mass spectrometer in a package ambient gas analysis system has been described by Thomas in Reference 1. Figure 2 indicates the essential features of such a system.

This system is a batch type system in that several samples are loaded at one time on a rotary holder. The system is then vacuum-baked for a period of time necessary to insure low gaseous background levels.

Another system for package ambient gas analysis is the rapid cycle system. This system features a fifteen (15) minute cycle time from sample loading to gas analysis and then sample removal.

Each system has advantages in application to the users' gas analysis requirements. However, comparison of data from these two systems must consider the different thermal stresses each presents to the microelectronic package and its internal materials.

Pictures of commercially available batch and rapid cycle systems are seen, respectively, in Figures 3 and 4.

b) Package Opening System. The package opening system must do the following:

- Handle a variety of sample sizes
- Hold samples firmly in place
- Control sample temperature at 100°C prior to opening
- Employ a puncturing device that will not damage the package seal

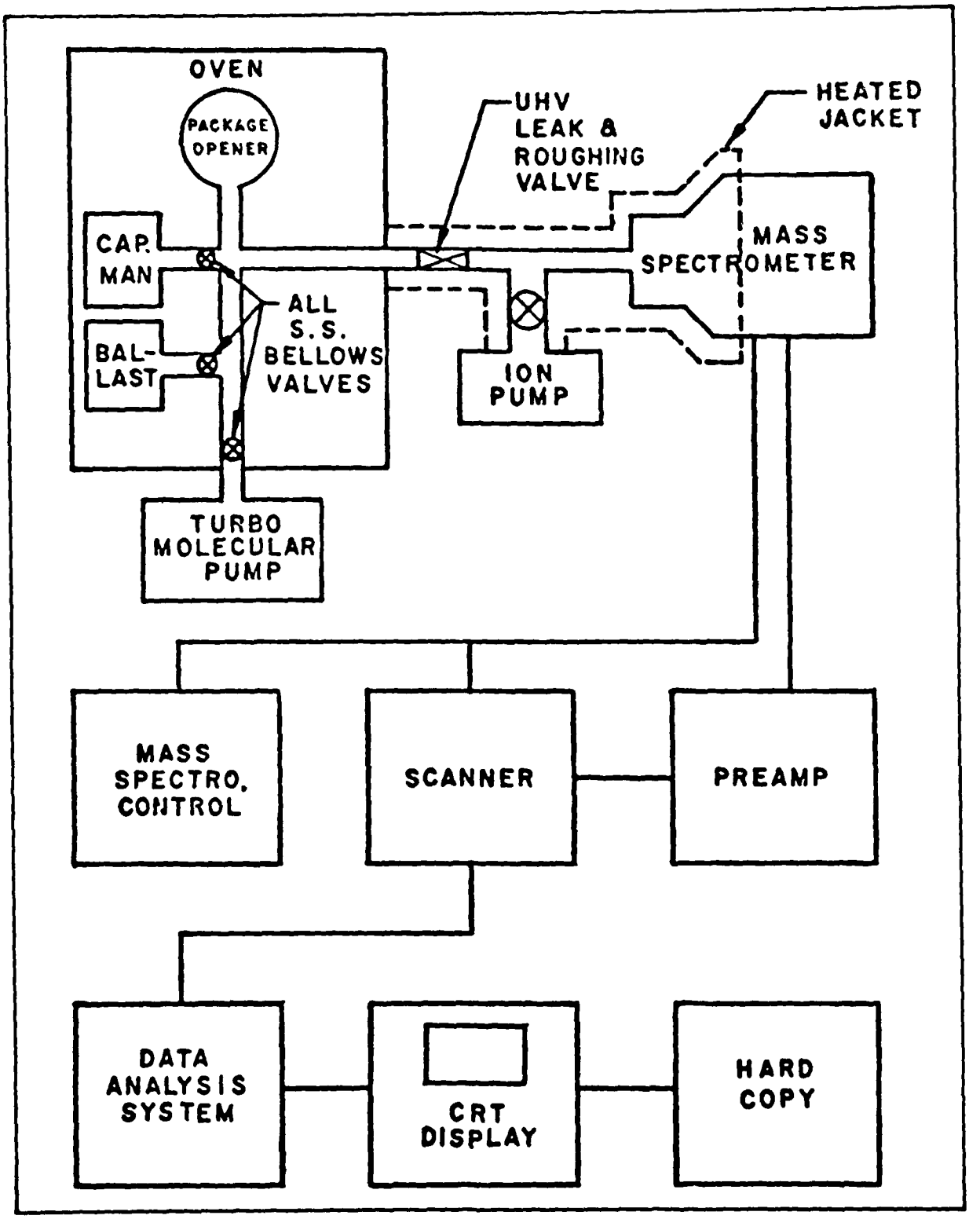


FIGURE 2. I.C. GAS ANALYSIS SYSTEM

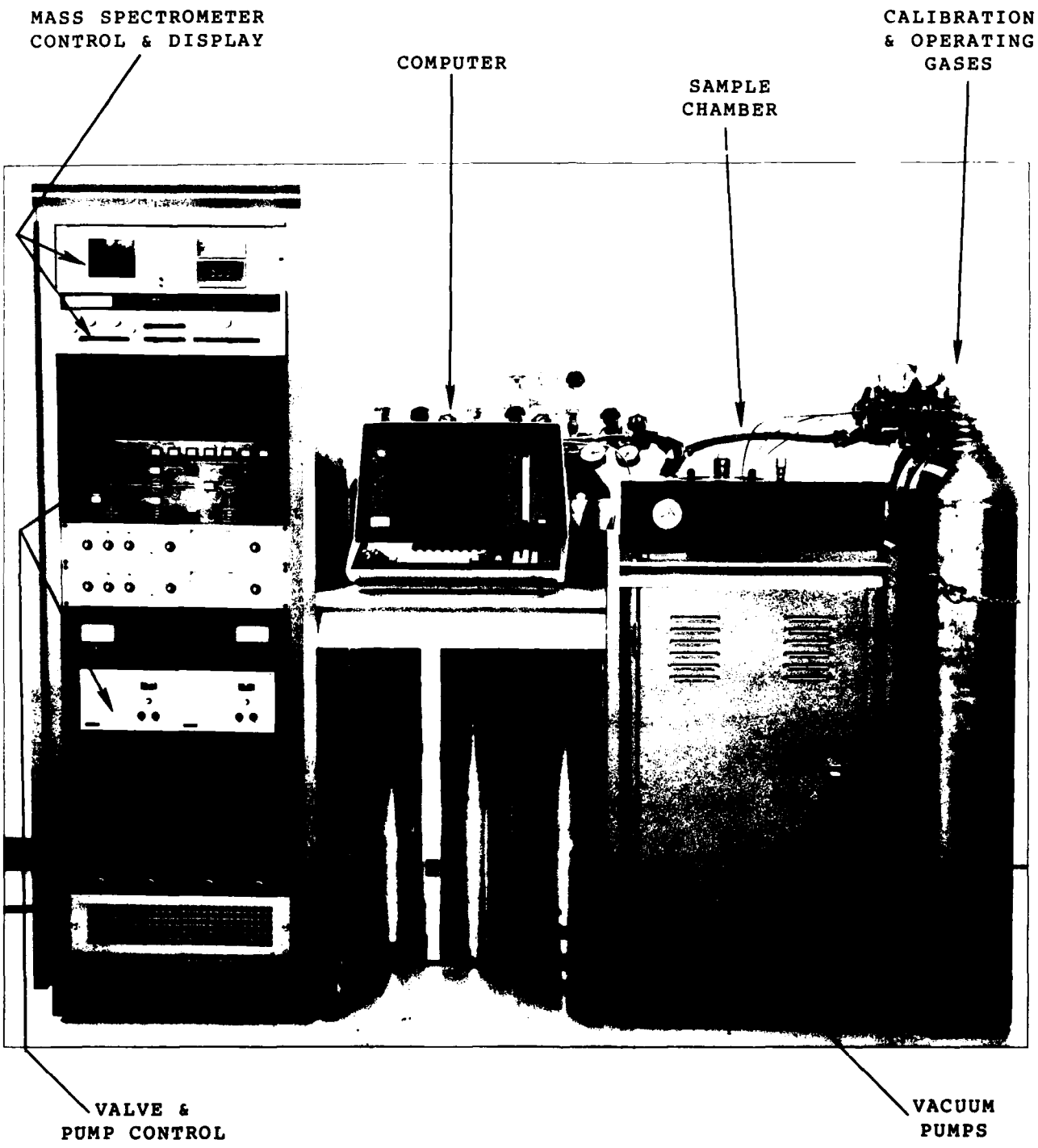


FIGURE 3. COMMERCIALLY AVAILABLE BATCH GAS ANALYSIS SYSTEM

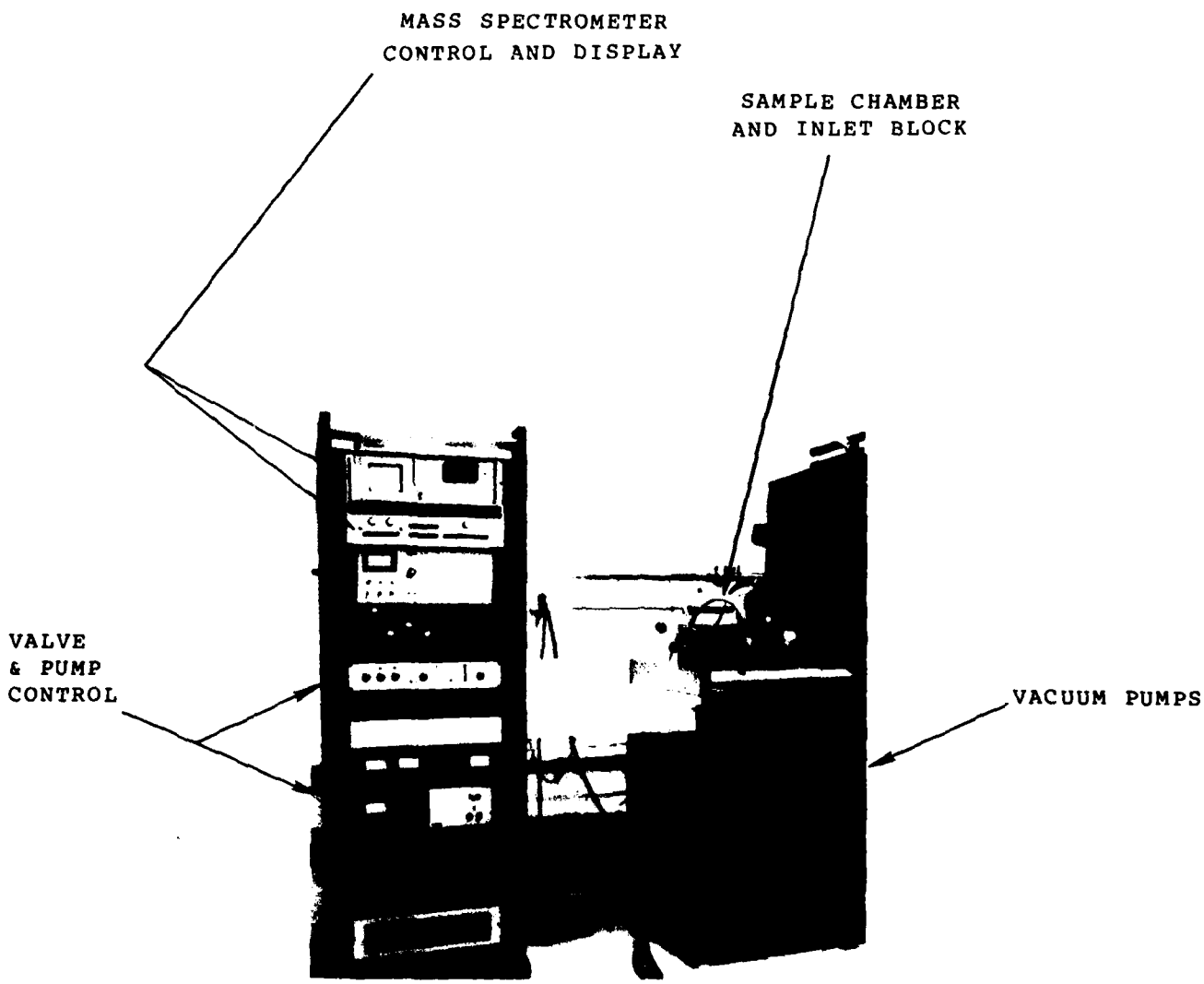


FIGURE 4a. COMMERCIALLY AVAILABLE RAPID CYCLE GAS ANALYSIS SYSTEM

FIGURE 4b. RADC RAPID CYCLE GAS ANALYSIS SYSTEM

- o Be evacuated by an oil-free pumping system (i.e., turbo-pump)
- o Contain a non-contaminating pressure sensor (i.e., diaphram type)
- o Provide options for either sampling through a fixed orifice or differential pumping mode prior to inserting sample into the mass spectrometer

c) Mass Spectrometer. The mass spectrometer should be capable of:

- o Having mass range of at least 2 to 100 (m/z)
- o Exhibiting unit resolution over this range (being able to distinguish clearly between two equally intense peaks one mass unit apart)
- o Utilizing a stable, rapidly recoverable detector (i.e., electron multiplier)
- o Being evacuated by an oil-free pumping system (e.g., turbomolecular pump)

d) Sample Analysis. The actual analysis requires three sets of data:

- o Background
- o Calibration
- o Sample

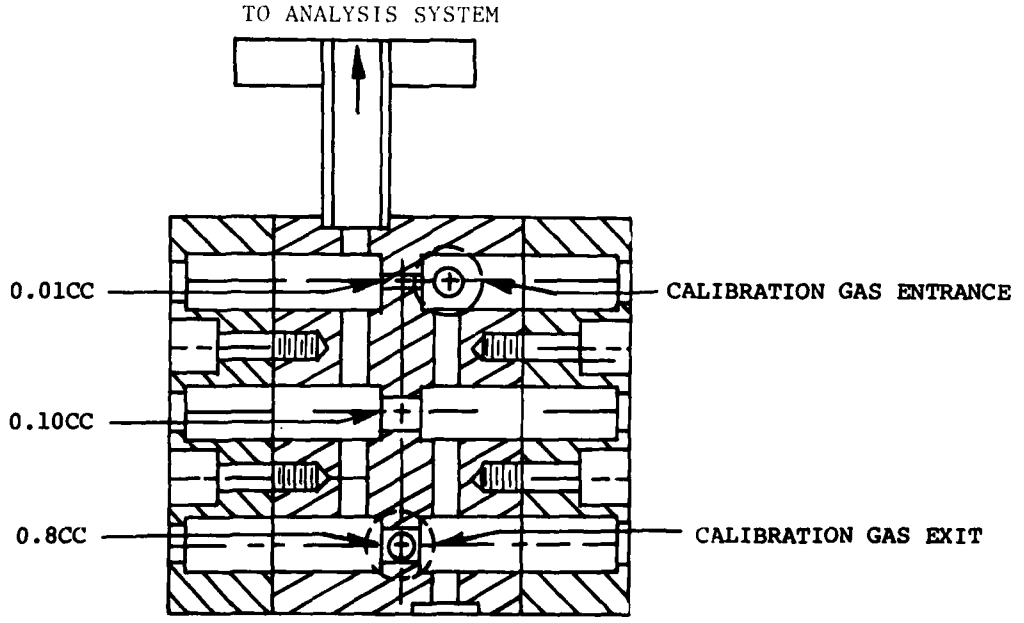
e) Background. The background spectrum allows correction for the signal in the system arising from hot filament reactions, desorption of gases from system walls, and those small but constant leaks to which every vacuum system is prone. Since small IC packages may have less than 1 microgram of moisture, it is absolutely necessary that the moisture

background due to leakage be eliminated from the background. Otherwise, it will completely swamp (mask the actual) the sample mositure content. System dryness can be measured by running an absolutely dry calibration burst. If the background moisture peak (mass 18) does not depress or increase during opening of the dry sample, the system is sufficiently leak-free for performing moisture analysis. The peaks commonly seen include m/z values 2, 18, 28, and 44.

f) Calibration. The key to success in any gas analysis system which is used to measure moisture lies in the ability to reproducibly generate constant volumes of gas containing known moisture content. Outwardly, this may seem very simple. However, it has proven to be a very difficult task. Recently a calibration system has been developed which accurately simulates small package volumes (.01, .1, .85 ccm) while at the same time making it possible to control the moisture content. This system coupled with a two-pressure moisture generator has now been in use at the four commercial gas analysis laboratories and RADC since November 1979 and has made it possible for all five laboratories to achieve analysis correlation to better than $\pm$20% at 5000 ppm for volumes between .01 ccm to .85 ccm. A picture of the system is shown in Figure 5. The key feature of the valve design is that it allows for continuous purging of the back side of the sampling valve and the sample chamber until just before insertion of the sample burst. The sample volume which is trapped between two toggle valves can be quickly toggled into the mass spectrometer system without excessive outgassing or time delay. Each of the calibration systems has been checked with an NBS calibrated dew point hygrometer and demonstrated an accuracy of better than $\pm 0.5^{\circ}C$ dew point.

g) Data Collection and Reduction. The simplest approach to package gas analysis is to record a mass spectrum after the package has been opened using a static sample method

a. MOISTURE CALIBRATION THREE VOLUME CALIBRATION VALVE AND GENERAL PURPOSE HUMIDIFIER



b. THREE VOLUME VALVE: CROSS-SECTIONAL VIEW

FIGURE 5. MOISTURE CALIBRATION SYSTEM

at a constant pressure. The difficulty with this approach is seen in Figure 6 where the relative abundance (labeled "intensity" in the figure) is recorded as a function of time after package opening. It is seen that the rates of escape of the various components of the ambient gas from the package and their detection is not uniform. On the contrary, except for the very anomalous behavior of the water vapor, there appears to be some fractionation effects, that is, a dependence on the molecular mass of the various species. This observation indicates the need for an integrated measurement of each gas component over a reasonable time period to give reproducible results. Of course, the practical way of achieving time-integrated mass spectrum intensity measurements is through a computer system.

With the appropriate interface unit and through the use of such programming techniques as MID (Multiple Ion Detection), Background Subtraction, and Quantitative Calibration Software, the accuracy and precision of measurement can be increased one hundredfold (two orders of magnitude).

h) Technique Flow Chart. A flow chart detailing a package ambient gas analysis is presented in Figure 7.

4. Application. The application of the mass spectrometric technique to the analysis of the backfill gas in a relatively large volume relay package is presented here.

A quadruple mass spectrometer was used to perform the analysis, and the data were (captured) by a computer. The figures are actual printouts of experimental data.

Four sets of data were obtained as depicted in Figures 8, 9, 10 and 11. Figure 8 represents the background spectrum of the instrument before room air, which was used as the calibration standard, was admitted to the ion source.

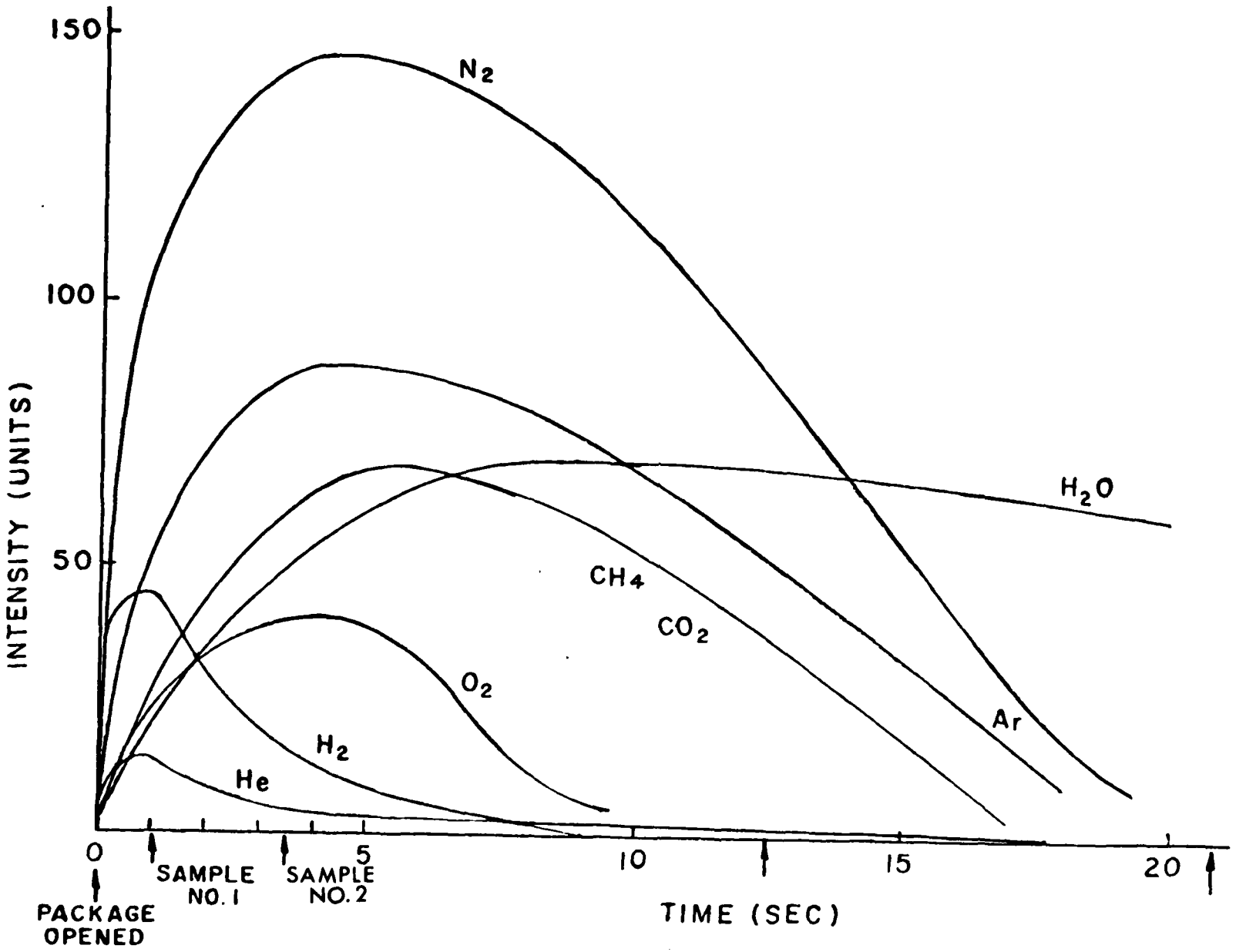


FIGURE 6. ANALYSIS SYSTEM PUMP-OUT CURVES.

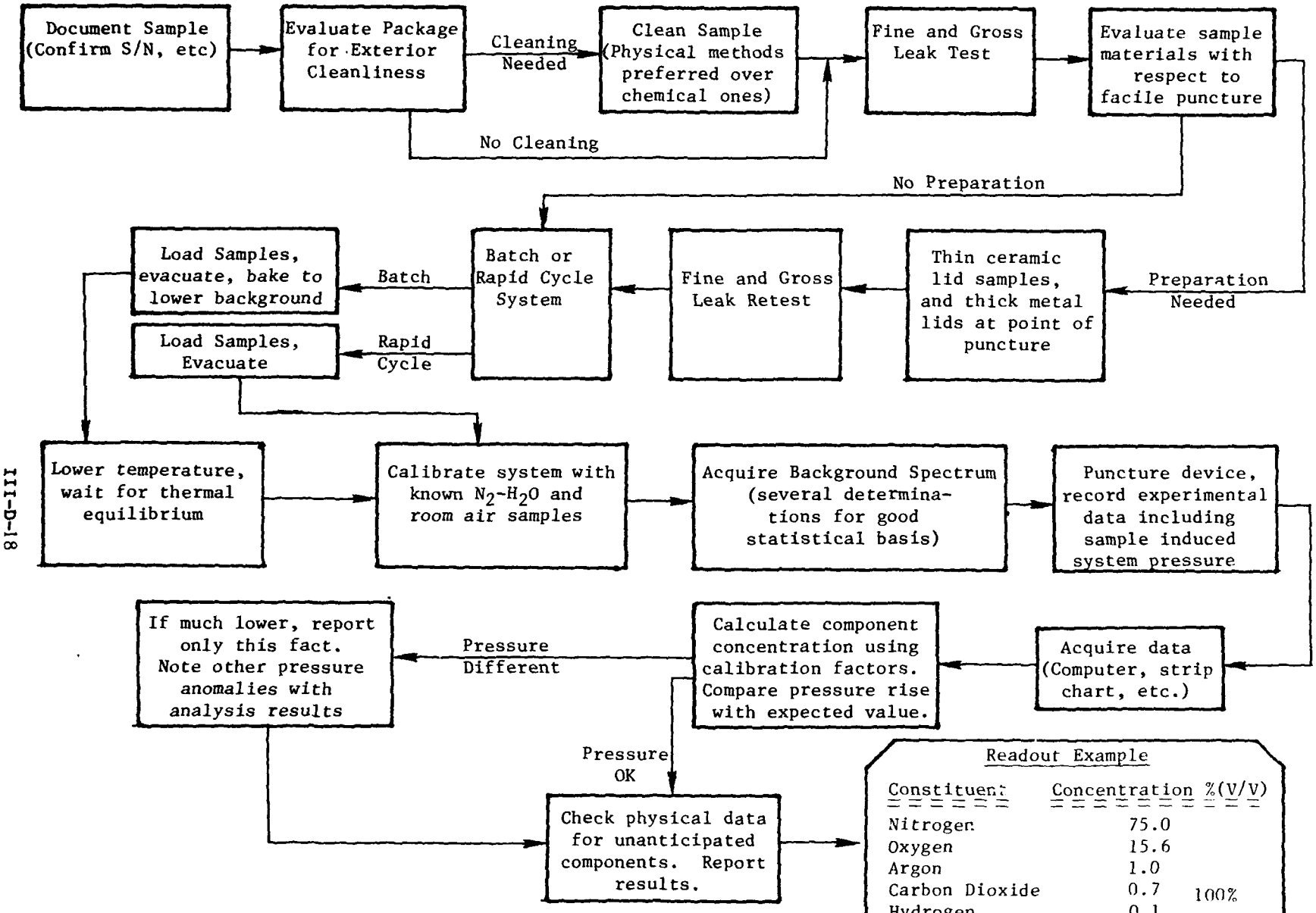


FIGURE 7. PACKAGE AMBIENT GAS ANALYSIS TECHNIQUE

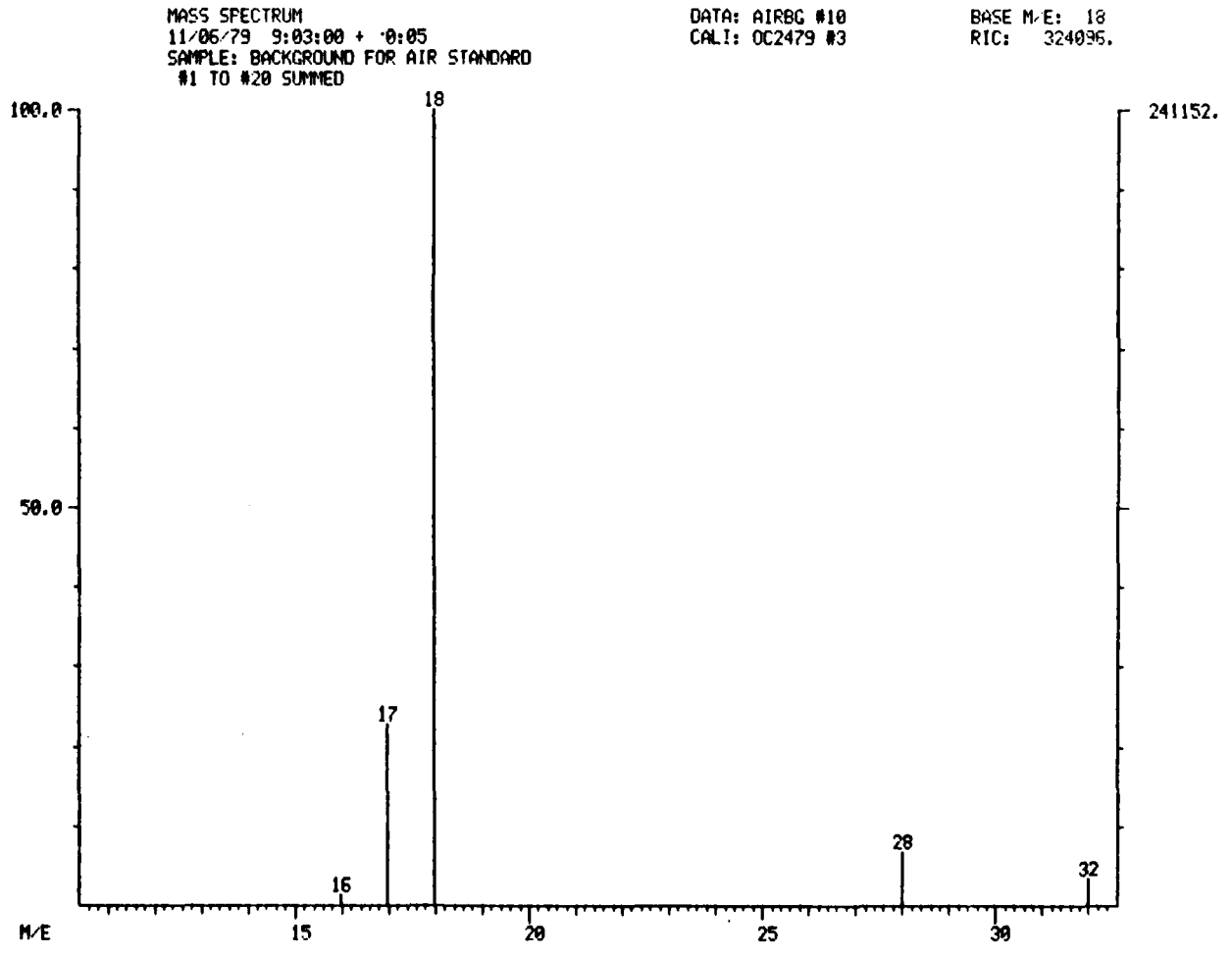


FIGURE 8. MASS SPECTRUM - SAMPLE: BACKGROUND FOR AIR STANDARD.

The assumption that is made throughout these calculations is that the itensity (= height) of any mass peak represents a summation of the contributions of all ions of a given m/z value, regardless of their origin. Also, the background contributions are assumed to be constant during the course of the experimental measurements.

The largest peak in the background arises from water, H_2O (m/z = 18), with its accompanying fragment peaks at (m/z = 17) and (m/z = 16). Peak 28 arises from both carbon monoxide (CO) and nitrogen (N_2) gases and, of course, m/z = 32 corresponds to oxygen gas (O_2).

In Figure 9, the mass spectrum of room air, one can easily recognize that the very small peaks at 40 and 44 (multiplied fifty fold (50X) for display purposes) represent argon (Ar) and carbon dioxide (CO_2), respectively. The peak at 14 is a composite derived from nitrogen, N_2^{2+} and N^+, while peak 29 is an isotope peak of N_2 ($N_{14}.N_{15}$).

Figure 10 is a background spectrum taken just before the relay package was punctured.

Figure 11 shows the mass spectrum of the relay package fill gas. Note the very low levels of O_2 compared to N_2. A multiplier of 500 was used in order to show their relative abundances in the spectrum. The instrument was scanned from mass 1 through mass 100; however, low molecular mass organic compounds appear to be absent. The mass-intensity data pairs for the air sample and background are presented in TABLE II.

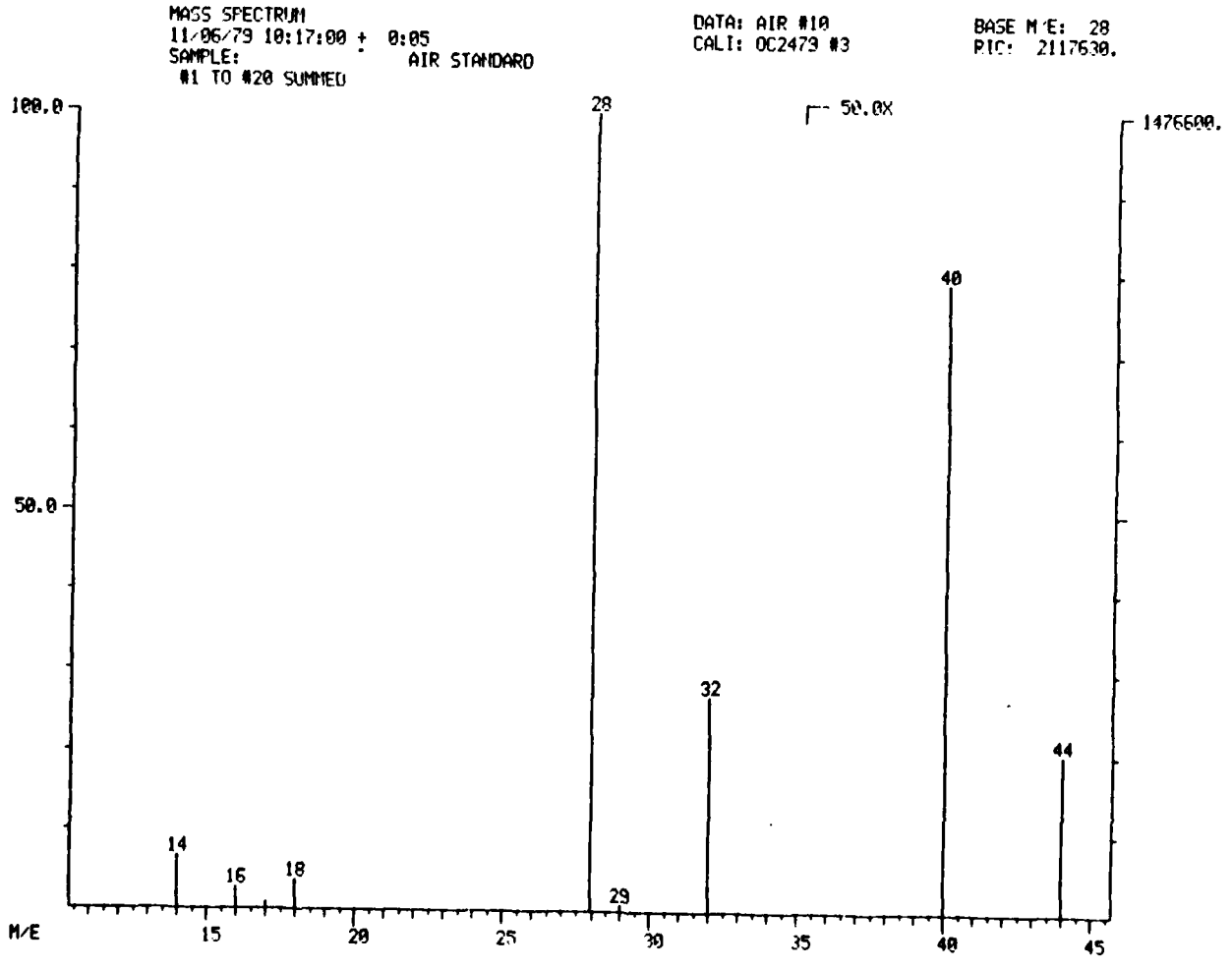


FIGURE 9. MASS SPECTRUM - SAMPLE: AIR STANDARD

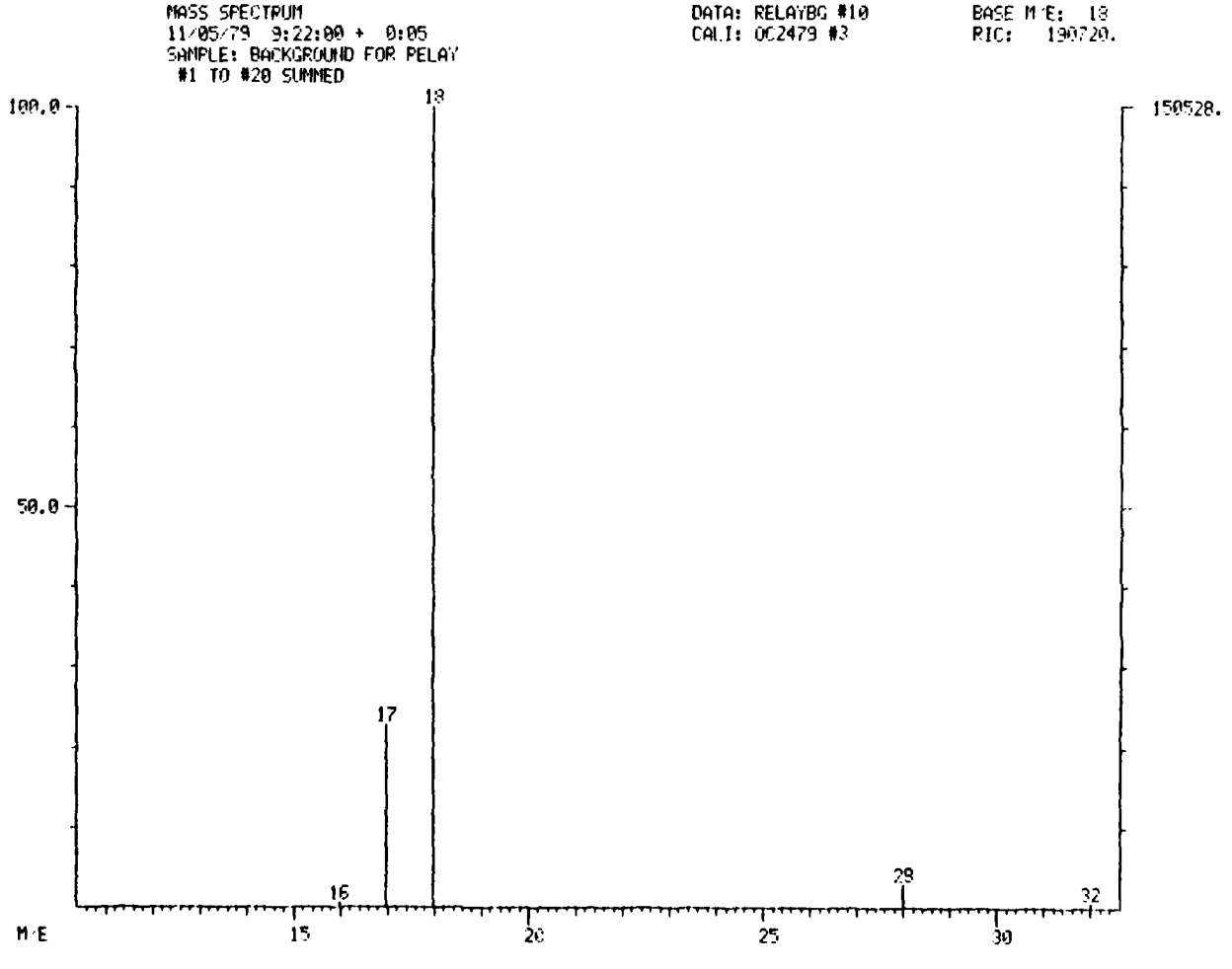


FIGURE 10. MASS SPECTRUM - SAMPLE: BACKGROUND FOR RELAY

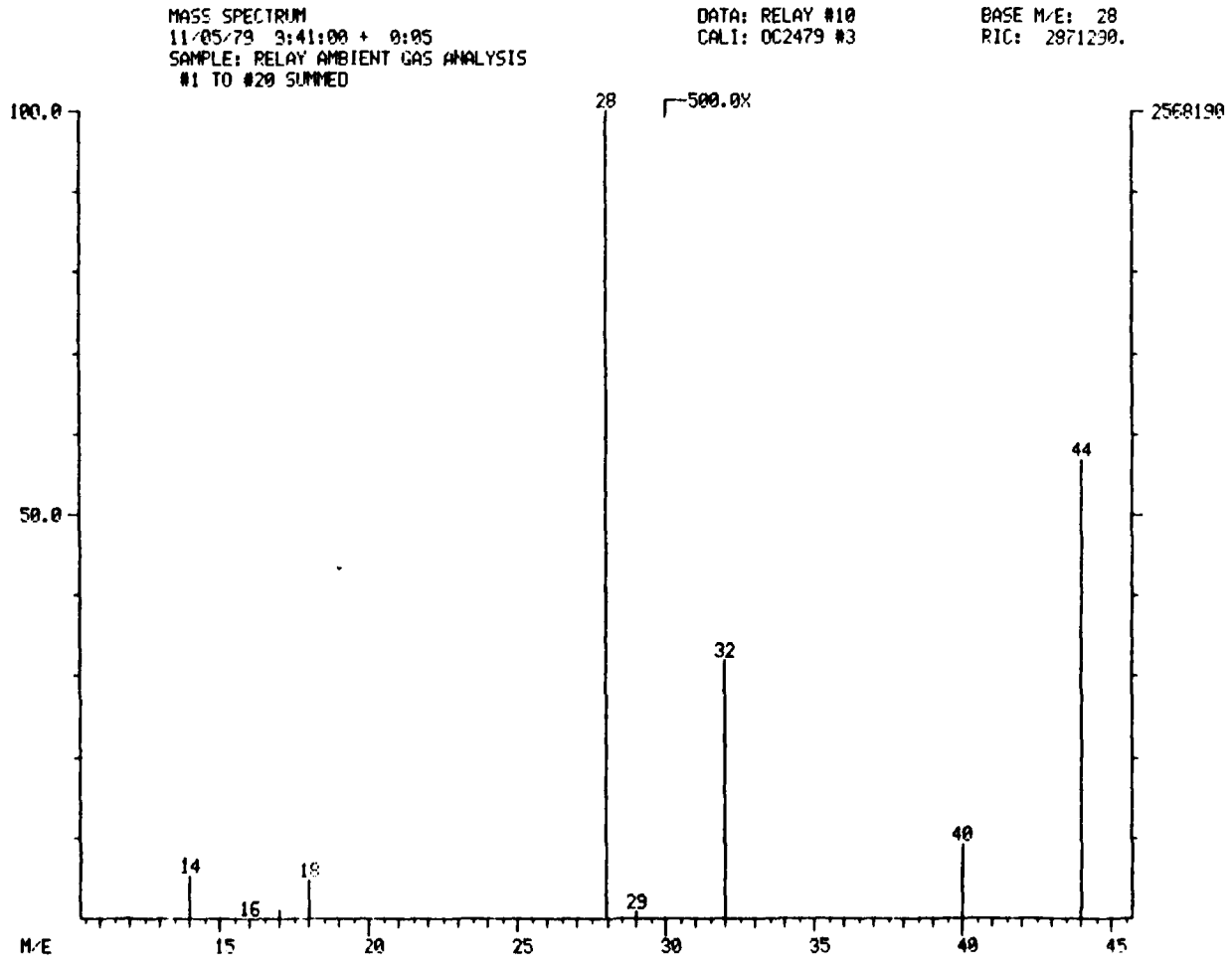


FIGURE 11. MASS SPECTRUM - SAMPLE: RELAY AMBIENT GAS ANALYSIS

TABLE II MASS INTENSITY DATA

Component	Molecular Peak, m/z	Intensity: Air	Intensity: Background	Intensity: Air (Corrected)	Sensitivity x 10^{13}
N_2	28	1476600	16256	1460334	2.20
O_2	32	398336	7968	390368	2.19
Ar	40	23264	-	23214	2.93
CO_2	44	5904	-	5904	21.10

5. Calculations.

a) Sensitivity. The sensitivity, S, of an instrument to a particular species is expressed as the peak intensity (= height) per unit of pressure,

$$S = \frac{I}{P}$$

where I = peak intensity
p = pressure

For the various species that comprise air, the pressure is the partial pressure of that species, that is:

$$P_C = F_C \times P_T$$

where P_C = partial pressure of component C
F_C = fraction of component c in air
P_T = total pressure of sample

The values of F_C for air are given in TABLE III.

TABLE III

Composition of Air

Component	F_c
N_2	0.7809
O_2	0.2095
Ar	0.00934
CO_2	0.00033

For example, the sensitivity of the instrument to N_2 is:

$$S_{N_2} = \frac{I_{N_2}}{P_T \times F_{N_2}}$$

Using the data in Table II,

$$S_{N_2} = \frac{1450344}{8.5 \times 10^{-8} \text{ torr} \times 0.7809}$$

$$= 2.20 \times 10^{13} \text{ intensity units/torr}$$

Note that the corrected intensity of N_2 is used in the calculation since the instrument background contributes to the intensity at m/z = 28.

The same approach is used for the other components of air, and the calculated sensitivities are recorded in TABLE II.

b) Sample Composition. The mass-intensity pairs for the relay and instrument background are given in TABLE IV. Rewriting the sensitivity equation, one obtains a relationship for calculating the fraction of component C in the sample:

$$F_C = \frac{I_C}{S_C \cdot P_T}$$

Thus, for N_2 in the relay

$$F_{N_2} = \frac{I_{N_2}}{S_{N_2} \cdot P_T}$$

TABLE IV: COMPOSITION OF RELAY PACKAGES

		Intensity				
Component	Molecular Peak, m/z	Relay	Background	Relay Corrected	$10^3 F_C$	%(V/V)
N_2	28	2568190	4416	2563774	1.371	99+
O_2	32	1644	729	915	0.491	0.036
Ar	40	475	-	475	0.191	0.014
CO_2	44	2916	-	2916	0.163	0.012

where P_T is the total pressure of the relay gas in the mass spectrometer

$$F_{N_2} = \frac{2563774}{2.20 \times 10^{13} \times 8.5 \times 10^{-8}}$$

$$F_{N_2} = 1.371$$

The rather absurd result points up a critical problem in these types of measurements: the actual pressure of the sample. Note that in a proper set-up, Figure 1, provision has been made for a gas pressure measurement via the capacitance manometer. However, the sensitivity of the instrument should be relatively unaffected by sample pressure differences over a wide range. The more important thing is that the pressure of the sample remain essentially constant during the measurement. If this is true, then the relative fractions of components in the sample should remain virtually constant.

To convert the values of F_c in TABLE IV to percent composition (volume/volume), normalization is used:

$$\% C = \frac{F_c}{\Sigma F_c} \times 100$$

$$i \quad i$$

For N_2:

$$\% N_2 = \frac{1.371}{1.371845} \times 100$$

$$\% N_2 = 99.94$$

c) Precision. The precision in measurements of this type in a quadrupole mass spectrometer is subject to many factors. Experience indicates that a precision of ±1% appears to be a lower limit.

Therefore, the calculated values for percent of each component must be adjusted to account for this precision level. These calculations were made ignoring the moisture content because there was very little difference between the background reading and the sample reading and points to the necessity of very accurate control over background measurements.

6. Dew Point Measurements.

a) Introduction. The gas ambient of a microelectronic package is not a static system. One of the most dramatic changes which occurs in the package ambient takes place immediately after seal. If the seal is made in dry nitrogen (5 ppm moisture) and parts are used which have not been baked out, the ambient in the package changes from 5 ppm to 5000 ppm moisture within a matter of seconds. This desorption of moisture from the ceramic or metal parts continues for several days, reaching moisture contents greater than 15,000 ppm even though the package was sealed in a dry atmosphere. The outgassing of moisture from the interior walls of the package also affects the interpretation of the reported moisture content. It is fair to say that the reported moisture at 100°C is always greater than the amount actually in the ambient. This fact becomes important if one wants to relate the measured moisture back to the dew point.

To calculate the dew point, several assumptions are required:

- o All the moisture in an enclosed volume must remain in the vapor state (since dew point concerns only the molecules of moisture in a volume of gas)
- o No moisture is removed from the ambient by the walls of the package

Figure 12 is a nomograph which converts parts per million (ppm) moisture to dew point at constant pressure.

b) Description of Technique. The purpose of the dew point test, a nondestructive test method, is to detect the presence of moisture trapped inside an integrated circuit or hybrid microelectronics package. The device is mounted in a suitable socket and the necessary leads to monitor some electrical parameter which would be sensitive to surface conductivity due to condensed moisture. Typical electrical parameters used are I_{CBO} leakage current on transistors and input offset voltage or supply current on operational amplifiers. Figure 13 shows a typical operational amplifier test circuit for performing the dew point test. The transient change in the observed electrical parameter as the device goes through the wet phase of the dew point is an effective indicator of entrapped moisture. This technique is a qualitative method only. The amount of change noted is dependent upon excitation, entrapped water and amounts of residual chemicals which are left on the die and may become conductive.

c) General Procedure:

- o Power fixture/device
- o Temperature chambers set to -45 to -65°C and 3 to 8°C
- o Place fixture/device in cold chamber and allow it to remain there until the recorder indicates the device has stabilized
- o Transfer fixture/device to other chamber (3 to 8°C)
- o Disregard initial observed transients due to thermal gradients across the die that may occur in the first couple of seconds
- o Allow device to warm.

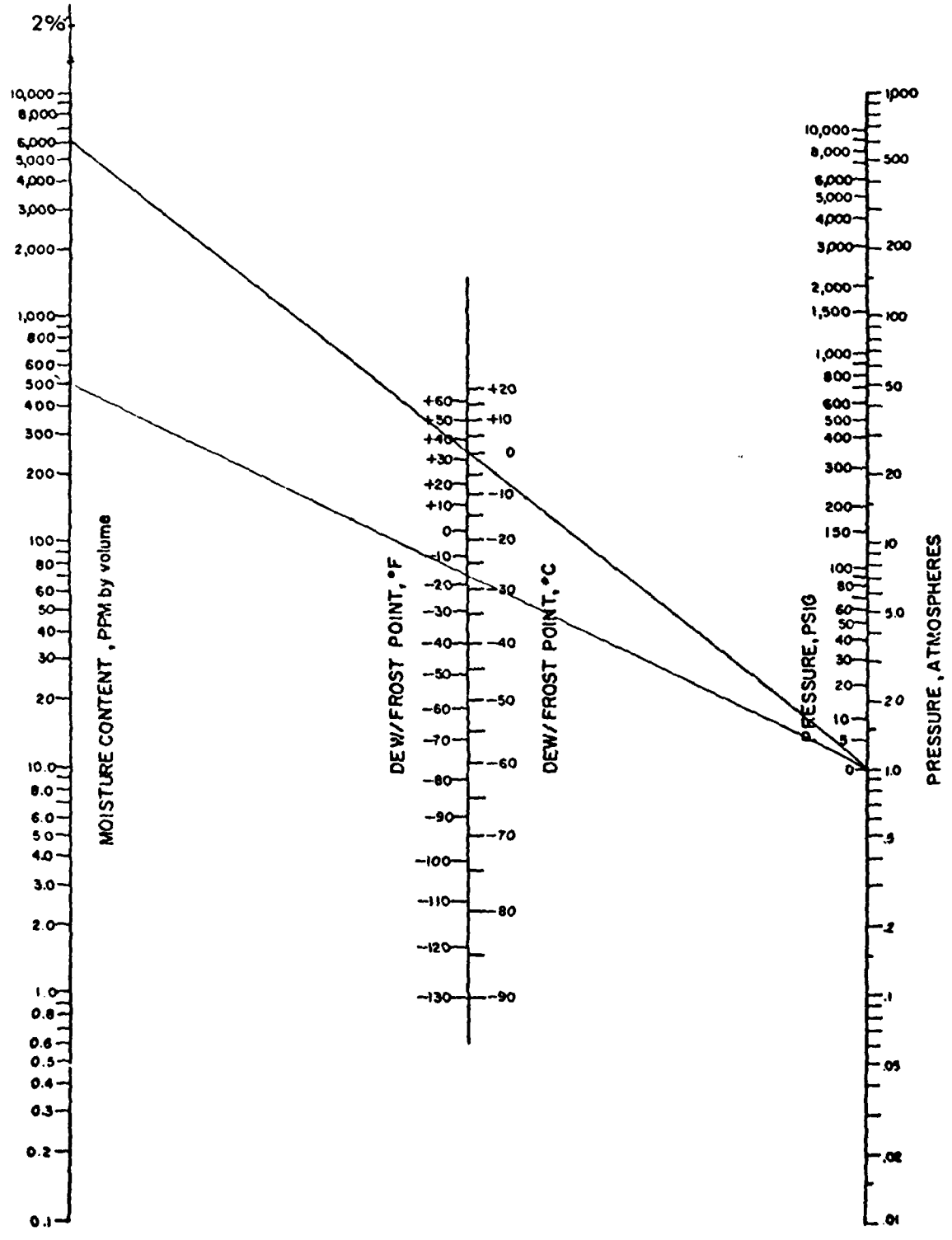
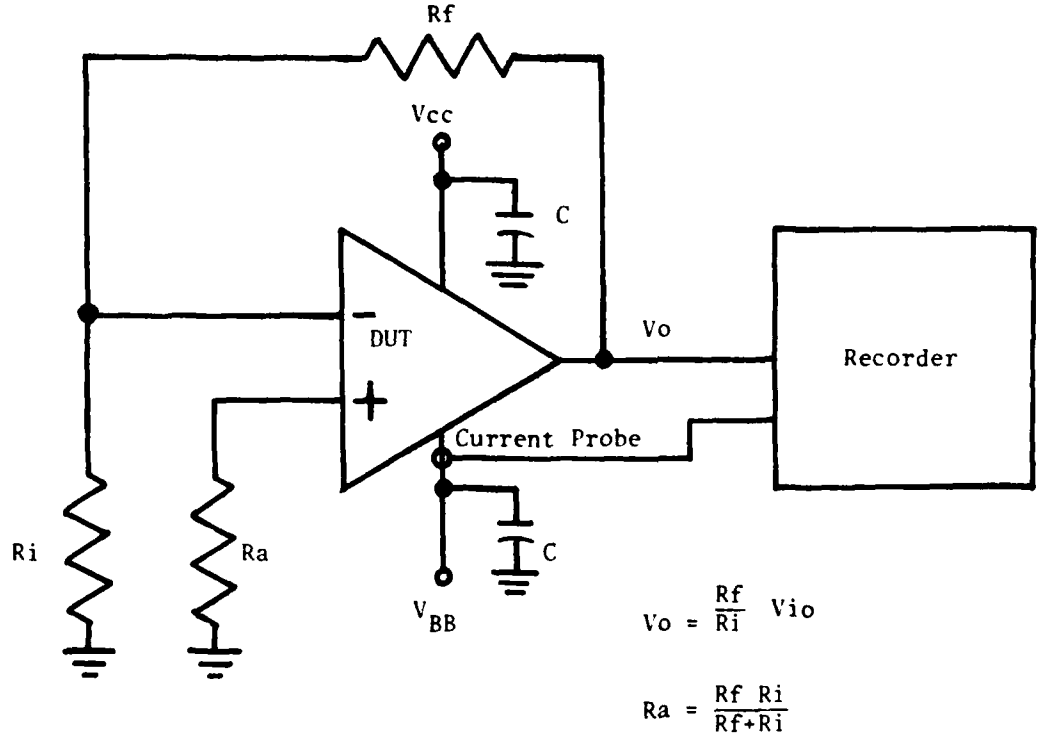


FIGURE 12. NOMOGRAPH FOR DEWPOINTS AND PPMV AS A FUNCTION OF P



Note: 1. Provide band pass and/or frequency compensation circuitry as required to make the DUT functional and stable.

2. Choose C to decouple power supply as necessary.

FIGURE 13. TYPICAL OPERATIONAL AMPLIFIER TEST CIRCUIT

- Any discontinuity or deviation from a normal thermal time constant is indicative of frost on the die going to a wet stage
- The wet leakage currents can flow to give an abnormal equivalent input offset voltage and an increase in excitation current
- This will continue until the die surface dries, then the device will return to normal conditions
- If the test is repeated, succeeding deviations become less pronounced until nothing is observed

If the part is then subjected to a gas analysis, water will still be detectable but so will hydrogen and oxygen which indicates that part of the water was electrolyzed into its elements.

d) Testing Check Points.

- Excitation voltage compatible with the device
- Gain is high to provide a good readable channel (A gain of 1000 is suggested for the op. amp.).
- Minimum time of monitoring is suggested as 30 seconds.

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EQUIPMENT

Temperature Chamber

Model CO-160C-1 environmental chamber Blue M Electric Co, Blue Island, IL	$2,500

Recorder

Model 7100 B strip chart recorder/plug-in Hewlett Packard, Palo Alto, CA	$3,000

Curve Tracer

576 Curve Tracer with standard test fixture Tektronix Co., Beaverton, OR	$5,975

Power Supplies

LD series, dual supply Lambda Electronics, Melville, LI, NY	$ 480

APPENDIX A

METHOD 1018.2

INTERNAL WATER-VAPOR CONTENT

1. PURPOSE. The purpose of this test is measuring the water-vapor content of the atmosphere inside a metal or ceramic hermetically-sealed device. It can be destructive (procedures 1 and 2) or nondestructive (procedure 3).

2. APPARATUS. The apparatus for the internal water-vapor content test shall be as follows for the chosen procedure:

2.1 Procedure 1. (Procedure 1 measures the water-vapor content of the device atmosphere by mass spectrometry.) The apparatus for procedure 1 shall consist of:

a. A mass spectrometer capable of reproducibly detecting the specified moisture content for a given volume package with a factor of ten sensitivity safety margin (i.e., for a specified limit of 5000 ppmv, .01 ccm, the mass spectrometer shall demonstrate a 500 ppmv or less absolute sensitivity to moisture for a package volume of .01 ccm). The smallest volume shall be considered the worst case. The calibration of the mass spectrometer shall be accomplished at the specified moisture limit (±20%) using a package simulator which has the capability of generating at least three known volumes of gas ±10% on a repetitive basis by means of a continuous sample volume purge of known moisture content ±10%. Moisture content shall be established by the standard generation techniques (i.e., 2 pressure, divided flow, or cryogenic method). The absolute moisture shall be measured by an NBS calibrated moisture dew point analyzer at least once every 2 years. The NBS calibrated dew pointer shall be returned to the Bureau of Standards at least once each year for recalibration. Calibration records shall be kept on a daily basis and made available to DCAS personnel. Gas analysis results obtained by this method shall be considered valid only in the moisture range or limit bracketed by at least two (volume or concentration) calibration points (i.e., 5000 ppmv between .01-.1 ccm or 1000-5000 ppmv between .01-.1 ccm). A best fit curve shall be used between volume calibration points. Corrections of sensitivity factors deviating greater than 10% from the mean between calibration points shall be required.

b. A vacuum opening chamber which can contain the device and a vacuum transfer passage connecting the device to the mass spectrometer of 2.1a. The transfer passage shall be maintained at 125°C ±5°C. The fixturing in the vacuum opening chamber shall position the specimen as required by the piercing arrangement of 2.1c, and maintain the device at 100°C ±5°C for a minimum of 10 minutes prior to piercing.

c. A piercing arrangement functioning within the opening chamber or transfer passage of 2.1b, which can pierce the specimen's housing (without breaking the mass spectrometer chamber vacuum and without disturbing the package sealing medium) thus allowing the specimen's internal gases to escape into the chamber and mass spectrometer.

NOTE: A sharp-pointed piercing tool, actuated from outside the chamber wall via a bellows to permit movement, should be used to pierce both metal and ceramic packages. For ceramic packages, the package lid or cover should be locally thinned by abrasion to facilitate localized piercing.

2.2 Procedure 2. (Procedure 2 measures the water-vapor content of the device atmosphere by integrating moisture picked up by a dry carrier gas at 50°C.) The apparatus for procedure 2 shall consist of:

a. An integrating electronic detector and moisture sensor capable of reproducibly detecting a water-vapor content of 300±50 ppmv moisture for the package volume being tested. This shall be determined by dividing the absolute sensitivity in micrograms H_2O by the computed weight of the gas in the device under test, and then correcting to ppmv.

b. A piercing chamber or enclosure, connected to the integrating detector of 2.2a, which will contain the device specimen and maintain its temperature at 100°C ±5°C during measurements. The chamber shall position the specimen as required by the piercing arrangement. The piercing mechanism shall open the package in a manner which will allow the contained gas to be purged out by the carrier gas or removed by evacuation. The sensor and connection to the piercing chamber will be maintained at a temperature of 50°C ±2°C.

2.3 Procedure 3. (Procedure 3 measures the water-vapor content of the device atmosphere by measuring the response of a calibrated moisture sensor or an IC chip which is sealed within the device housing, with its electrical terminals available at the package exterior.) The apparatus for procedure 3 shall consist of one of the following:

a. A moisture sensor element and readout instrument capable of detecting a water-vapor content of 300 ±50 ppmv while sensor is mounted inside a sealed device.

b. Metallization runs on the device being tested isolated by back-biased diodes which when connected as part of a bridge network can detect 2000 ppmv within the cavity. The chip shall be cooled in a manner such that the chip surface is the coolest surface in the cavity. The device shall be cooled below dew point and then heated to room temperature as one complete test cycle.

NOTE: Suitable types of sensors may include (among others) parallel or interdigitated metal stripes on an oxidized silicon chip, and porous anodized-aluminum structures with gold-surface electrodes.

Surface conductivity sensors may not be used in metal packages without external package wall insulation. When used, the sensor shall be the coolest surface in the cavity. It should be noted that some surface conductivity sensors require a higher ionic content than available in ultraclean CERDIP packages. In any case, correlation with mass spectrometer procedure 1 shall be established by clearly showing that the sensor reading can determine whether the cavity atmosphere has more or less than the specified moisture limit at 100°C.

3. PROCEDURE. The internal water-vapor content test shall be conducted in accordance with the requirements of procedure 1, procedure 2, or procedure 3. Devices containing desiccants or organics shall be prebaked for 12 to 24 hours at 100°C ±5°C prior to hot insertion into apparatus.

3.1 Procedure 1. The device shall be hermetic per test method 1014, and free from any surface contaminants which may interfere with accurate water-vapor content measurement.

After device insertion, the device and chamber shall be pumped down and baked out at a temperature of 100°C ±5°C until the background pressure level will not prevent achieving the specified measurement accuracy and sensitivity. After pumpdown, the device case or lid shall be punctured and the following properties of the released gases shall be measured, using the mass spectrometer:

a. The increase in chamber pressure as the gases are released by piercing the device package. A pressure rise of less than 50 percent of normal for that package volume and pressurization may indicate that (1) the puncture was not fully accomplished, (2) the device package was not sealed hermetically, or (3) does not contain the normal internal pressure.

b. The water-vapor content of the released gases, as a proportion (by volume) of the total gas content.

c. The proportions (by volume) of the other following gases: N_2, He, Mass 69 (fluorocarbons), O_2, Ar, H_2, CO_2, CH_4, and other solvents, if available, in the order stated. Calculations shall be made and reported on all gases present greater than 1% by volume. Data reduction shall be performed in a manner which will preclude the cracking pattern interference from other gas species in the calculations of moisture content. Data shall be corrected for any system dependent matrix effects such as the presence of hydrogen in the internal ambient.

3.1.1 Failure criteria.

a. A device which has a water-vapor content greater than the specified maximum value shall constitute a failure .

b. A device which exhibits an abnormally low total gas content, as defined in 3.1a, shall constitute a failure, if it is not replaced. Such a device may be replaced by another device from the same population; if the replacement device exhibits normal total gas content for its type, neither it nor the original device shall constitute a failure for this cause.

c. Data analysis on devices containing desiccants or organics shall be terminated after 95 percent of the gas has been analyzed in a dynamic measurement system or data shall be taken after pressure has stabilized for a period of 2 minutes in a static system or in any manner which approaches the true measurement of ambient moisture in equilibrium at 100°C within the cavity.

3.2 Procedure 2. The device shall be hermetic per test method 1014, and free from any surface contaminants which may interfere with accurate water-vapor content measurement.

After device insertion into the piercing chamber, gas shall be flowed through the system until a stable base-line value of the detector output is attained. With the gas flow continuing, the device package shall then be pierced so that a portion of the purge gas flows through the package under test and the evolved moisture integrated until the base-line detector reading is again reached. An alternative allows the package gas to be transferred to a holding chamber which contains a moisture sensor and a pressure indicator. System is calibrated by injecting a known quantity of moisture or opening a package of known moisture content.

3.2.1 Failure criteria.

a. A device which has a water-vapor content (by volume) greater than the specified maximum value shall constitute a failure.

b. After removal from the piercing chamber, the device shall be inspected to ascertain that the package has been fully opened. A device package which was not pierced shall constitute a failure, if the test is not performed on another device from the same population; if this retest sample or replacement is demonstrated to be pierced and meets the specified water-vapor content criteria, the specimen shall be considered to have passed the test.

c. A package which is a leaker in the purge case will be wet and counted as a failure. In the case of evacuation, a normal pressure rise shall be measured as in 3.1a.

3.3 Procedure 3. The moisture sensor shall be calibrated in an atmosphere of known water-vapor content, such as that established by a saturated solution of an appropriate salt or dilution flow stream. It shall be demonstrated that the sensor calibration can be verified after package seal or that post seal calibration of the sensor by lid removal is an acceptable procedure.

The moisture sensor shall be sealed in the device package or, when specified, in a dummy package of the same type. This sealing shall be done under the same processes, with the same die attach materials and in the same facilities during the same time period as the device population being tested.

The water-vapor content measurement shall be made, at 100°C or below by measuring the moisture sensor response. Correlation with procedure 1 shall be accomplished before suitability of the sensor for procedure 3 is granted. It shall be shown the package ambient and sensor surface are free from any contaminating materials such as organic solvents which might result in a lower than usual moisture reading.

3.3.1 Failure criteria. A specimen which has a water-vapor content greater than the specified maximum value shall constitute a failure.

4. IMPLEMENTATION. Suitability for performing method 1018 analysis is granted by the qualifying activity for specific limits and volumes. Method 1018 calibration procedures and the suitability survey are designed to guarantee ±20% lab-to-lab correlation in making a determination whether the sample passes or fails the specified limit. Water vapor contents reported either above or below the (water vapor content -volume) range of suitability are not certified as correlatable values. This out of specification data has meaning only in a relative sense and only when one laboratory's results are being compared. Suitability status has been granted for a specification limit of 5000 ppmv and package volumes falling between .01 ccm and .85 ccm. The range of suitability for each laboratory will be extended by the qualifying activity when the analytical laboratories demonstrate an expanded capability. Information on current analytical laboratory suitability status can be obtained by writing DESC/EQM, Dayton, OH 45440.

5. SUMMARY. The following details shall be specified in the applicable procurement document:

a. The procedure (1, 2, or 3) when a specific procedure is to be used (see 3).

b. The maximum allowable water-vapor content falling within the range of suitability as specified in test method 5005 or 5008.

APPENDIX B

Certified Laboratories

Gollob Analytical Services
47 Industrial Road
Berkely Heights, NJ 07922
(201) 464-3331

Oneida Research Sevices
1 Ellinwood Court
New Hartford, NY 13413
(315) 736-4722

Pernicka Corporation
450 East Middlefield Road
Mountainview, CA 94043
(415) 969-0220

West Coast Technical Services
17605 Fabrica Way, Suite D
Cerritos, CA 90701
(213) 921-9831

APPENDIX C

MIL-STD-750B
27 February 1970

METHOD 1066.1

DEW POINT

1. Purpose. The purpose of this test is to monitor the device parameter for a discontinuity under the specified conditions.

2. Apparatus. The apparatus used in this test shall be capable of varying the temperature from the specified high temperature to -65°C and return to the specified high temperature while the parameter is being measured.

3. Procedure. The voltage and current specified in the detail specification shall be applied to the terminals and the parameter monitored from the specified high temperature to -65°C and return to the specified high temperature. The dew point temperature is indicated by a sharp discontinuity in the parameter being measured with respect to temperature. If no discontinuity is observed, it shall be assumed that the dew point is at a temperature lower than -65°C and the device being tested is acceptable.

4. Summary. The following details shall be specified in the individual specification:

a) Test temperature (high) (see 2).
b) Test voltage and current (see 3).
c) Test parameter (see 3).

E.

PACKAGE OPENING/ENCAPSULATION TECHNIQUES

E. Package Opening/Encapsulation Techniques.

1. Introduction. Package opening techniques fall within a "semi-destructive" class of failure analysis procedures. In general, it is not possible to return a microelectronic device to its fully original state after package opening. Opening a package is, in this sense, destructive. However, with sufficient care, the internal contents of a package will not be damaged by the opening procedure and thus the procedure is considered nondestructive, except for negating package hermeticity and internal gas ambient analysis.

In failure analysis, to avoid loss of valuable information, package opening should come only after electrical failure verification has been made, and all possible external causes for the failure have been explored and rejected.

Further terminal electrical testing can be conducted after the package is opened provided the technique employed is nondestructive to the package leads. The more exotic test procedures (EBIC, Photoresponse, Liquid Crystal, etc.) described in other chapters can also be performed after package opening. The failure analyst's most powerful tool, visual observation, can be brought into play at this point. Device isolation and probing can also be accomplished after package opening to determine the location and cause of failure. These techniques are detailed in Chapter III-A.

Quite a broad range of microelectronic package types exists. The techniques necessary to open these packages, consequently, vary greatly in application and difficulty. Most microelectronic packages require mechanical and/or chemical techniques to open.

Several package types are standard in industry, and procedures for opening them have been developed. Other, nonstandard types may require different, individual techniques for opening. The following sections contain details on opening specific package types.

This listing is in no way complete because there are probably as many ways to open a specific package type as there are individuals who perform this task.

2. Hermetic Packages. In microelectronics a hermetic package is one which has been sealed in a gas atmosphere and which maintains that atmosphere without leaking gas either into or out of the package. In actual practice, microelectronic packages intended to be hermetic are not always so. Package leakage often leads to microelectronic failure. The techniques for hermeticity tests are detailed in Chapter III-C.

Table I lists procedures for opening hermetic packages.

3. Plastic Packages. There are several types of plastic packages on the market today. These plastic packaging materials are thermosetting. They are generally highly resistant to attack from either mild acid or mild basic (alkali) solutions. These plastic materials will decompose at temperatures of 300°C or higher. A removal process involving decomposition would, however, be harmful to the metallization systems used in semiconductor devices. Harm would come both from the high temperature and from the chemical products of decomposition.

Development of decapsulation procedures have been further handicapped by the fact that the chemicals used must not be harmful to the semiconductor elements. In spite of these restraints, several chemicals are available that will perform plastic decapsulation while not harming semiconductor elements unduly if established procedures are closely followed. Semiconductor elements can generally be electrically retested after decapsulation, but analysis of die contamination is not meaningful.

TABLE I: HERMETIC PACKAGE OPENING TECHNIQUES

PACKAGE TYPE	PROCESS NO.	PROCESS STEPS
Glass encapsulated diodes; whisker type, double-heat-sink (DHD) type	1.	Figure 1 shows a typical whisker diode. Figure 2 shows a typical DHD diode. The following steps describe a procedure for opening these packages. a. Prepare the sample for metallurgical cross sectioning along the length of the package (See Chapter III-N for details on specimen preparation). b. Begin grinding away the encapsulating material on emery paper until the glass package is being removed. Frequent checks under a low power (3-30X) stereo microscope should be made to monitor progress. Rough emery paper grinding should be given up in favor of lapping as the package cavity is approached (See Chapter III-O for details on grinding and lapping processes). c. When the interior cavity is just opened, epoxy can be carefully inserted by means of a hypodermic syringe. The epoxy will hold the semiconductor element and electrical connections in place. Further polishing may be necessary to completely open the package cavity. The semiconductor element and electrical connections can now be examined visually and probed electrically.
	2.	An alternate method of opening these packages is available. However, before using this method, the failure analyst must determine that a failure is not due in any way to the package or to the electrical connections interior to the package. a. Obtain a small sieve-like basket with holes no bigger than approximately 0.020 inches and which will not be destroyed by acid solutions. For instance, stainless steel mesh serves well for this purpose.

TABLE I: HERMETIC PACKAGE OPENING TECHNIQUES (CONT'D)

PACKAGE TYPE	PROCESS NO.	PROCESS STEPS
Glass encapsulated diodes; whisker type, double-heat-sink (DHD) type (Cont.)	2. (Cont.)	b. Place the sample in the basket, and immerse the basket into an acid solution to etch away the leads completely (See Chapter III-M for details on appropriate acid). This will allow the semiconductor element to be removed from the package. c. Carefully remove the basket and rinse thoroughly in water, being careful not to lose the semiconductor element. d. If the chip has not come out of the package, carefully lift the package with tweezers and dump the element into the basket. The chip can then be removed from the basket for analysis.
Stud mounted diode, SCR	1.	Figure 3 shows a typical stud mounted device. To open this type package: a. Anchor the sample firmly in a vise with the leads upward. b. With a hand-held grinding instrument (such as the Dremel tool), grind away all leads on top of the package. This frees the element internal electrical connections. c. Using the tool, grind around the base of the metal top, destroying the metal-to-metal seal. d. Carefully remove the top, exposing the active element. Care must be used to prevent damage to the active element from metal particles.
	2.	a. Repeat steps a. and b. above. b. Cut through the top by using the transistor can opener shown in Figure 4.

TABLE I: HERMETIC PACKAGE OPENING TECHNIQUES (CONT'D)

PACKAGE TYPE	PROCESS NO.	PROCESS STEPS
Stud mounted diode, SCR (Cont.)	2. (Cont.)	c. Carefully remove the top from the base. There is a danger of damage from metal particles generated by the can opener, and caution should be used.
	3.	A third method exists if the failure analyst has access to machine shop equipment. a. Repeat steps a. and b. in procedure 1 above. b. Mount the package in an appropriate fashion and remove the lid by using a metal lathe.
Metal can, TO-3, TO-5, etc.	1.	a. Using the can opener shown in Figure 4, cut through the metal top. b. Carefully remove the top from the base. Care must be used to prevent damage due to metal particles generated by the can opener. Figure 5 shows a can opened with the can opener.
	2.	a. Firmly mount the package in a vise with the top facing up. b. Grind away the top with a grinding tool (such as the Dremel tool). Particular care must be used to prevent damage from metal particles.
	3.	a. Place a sheet of abrasive paper (such as Buehler emery paper) on a flat surface. b. Grind through the top of the can by abrading the can against the abrasive paper. Frequent checks should be made during the grinding. Caution should be used to prevent damage to the semiconductor device from metal particulate material. NOTE: Although all these various forms of grinding can be used to open cans, it is strongly recommended that the can opener be used in preference to grinding.

TABLE I: HERMETIC PACKAGE OPENING TECHNIQUES (CONT'D)

PACKAGE TYPE	PROCESS NO.	PROCESS STEPS
Ceramic packages, all types	1.	NOTE: This technique is suitable for all types of ceramic packages, including those types where the lid seal is formed at the lead frame interface. a. Figure 6 shows the equipment used in this process. Position the package between the knife blades contacting the seal region. The physical condition of the seal regions, i.e., the determination of the optimum package sides exhibiting the maximum seal glass dimensional length (top lead frame surface to ceramic lid bottom/glass seal interface) to be clamped between the parallel cutters, will generally dictate the orientation. b. Apply sufficient pressure to just hold the package in place. c. Heat the package lid for approximately 5 seconds with a Butane-Oxygen Microflame Torch, remove the heat and slowly increase pressure on the package seal. d. Repeat the heat/pressure sequence until the entire lid, intact, is sheared off at the seal. NOTE: This technique thus assures minimal damage to the package and lead frame and prevents particles (seal material) entering the package cavity during opening.
	2.	a. Place abrasive paper (such as Buehler emery paper) on a flat surface. b. Abrade the package lid by repeated strokes across the paper. The sample may optionally be potted for ease in handling (See Chapter III-M for details on potting procedures).

TABLE I: HERMETIC PACKAGE OPENING TECHNIQUES (CONT'D)

PACKAGE TYPE	PROCESS NO.	PROCESS STEPS
Ceramic packages, all types (Cont.)	2. (Cont.)	c. Continue abrading, with frequent visual checks, until the lid is almost completely gone. d. Remove the remainder of the lid over the cavity by attaching a piece of tape and lifting off. Figure 7 shows packages opened by this method.
Ceramic flat packs	1.	a. Clamp the package in a vise as demonstrated in Figure 8. Care must be used in applying pressure so as not to crack the package. b. Using an implement, such as a 12 inch metal rule or something comparable in weight, tap upward lightly on the bottom of the package. The lid will generally come off quite easily. NOTE: There is a good bit of controversy about this technique. It has been reported that clamping this package in a vise will always result in cracking of the ceramic and that tapping the package will usually result in removal of some or all the internal leads.
	2.	a. Clamp the package in a vise as demonstrated in Figure 8. Care must be used in applying pressure so as not to crack the package. b. Using a sharp implement (such as an Exacto knife), scribe around the lid seal until the lid can be either pried off or lifted off.
	3.	a. Place a sheet of abrasive paper (such as Buehler emery paper) on a flat surface. b. Optionally pot the package in potting compound (See Chapter III - N for details on potting procedures).

TABLE I: HERMETIC PACKAGE OPENING TECHNIQUES (CONT'D)

PACKAGE TYPE	PROCESS NO.	PROCESS STEPS
Ceramic flat packs (Cont.)	3. (Cont.)	c. Grind the potting material away by abrading the lid surface. d. Continue abrading, with frequent visual checks, until the lid is almost completely gone. e. Remove the lid by attaching a piece of tape and lifting off.
Metal lid DIP packages	1.	a. Clamp the package in a vise as demonstrated in Figure 9. Care must be used in applying pressure so as not to crack the package. b. Using a sharp implement (such as an Exacto knife) scribe around the lid seal until the seal is broken. c. Remove the lid by attaching a piece of tape and lifting off.
	2.	a. Place a sheet of abrasive paper (such as Buehler emery paper) on a flat surface. b. Abrade the package lid by repeated strokes across the paper. The sample may optionally be potted for ease in handling. (See Chapter III-N for details on potting procedures). c. Continue abrading, with frequent checks, until the lid is almost completely gone. d. Remove the remainder of the lid over the cavity by attaching a piece of tape and lifting off.

TABLE I: HERMETIC PACKAGE OPENING TECHNIQUES (CONT'D)

PACKAGE TYPE	PROCESS NO.	PROCESS STEPS
Metal lid DIP packages (Cont.)	3.	a. Clamp the package in a vise. Care must be used in applying pressure so as not to crack the package. b. With a large tip soldering iron, heat the package lid until the solder around the lid edge melts. c. Remove the lid by picking up with a vacuum pick up. NOTE: Heating is not generally the preferred technique in opening packages because of the danger of contaminating the elements with solder flux and solder balls. There is additionally the danger that heating might alter the electrical characteristics of the failure.
Ceramic DIP packages	1.	a. Scribe around the top edge of the glass frit where the package and lid were joined together with a sharp implement (such as an Exacto knife). b. Grasp the package with a pair of end cutting pliers that have had the cutting faces ground flat. c. Apply pressure to the pliers until the package cracks open. It may be necessary to strike the pliers with a hammer to break open the package. This technique is demonstrated in Figure 10. NOTE: Technique number 1 often causes damage to the microelectronic chip and/or the internal wiring. The successful use of this technique requires a good bit of experience.
	2.	a. Place a sheet of abrasive paper (such as Buehler emery paper) on a flat surface. b. Optionally pot the package in potting compound (See Chapter III-N for details on potting procedures).

TABLE I: HERMETIC PACKAGE OPENING TECHNIQUES (CONT'D)

PACKAGE TYPE	PROCESS NO.	PROCESS STEPS
Ceramic DIP packages (Cont.)	2. (Cont.)	c. Grind the potting material away by abrading until the package top is exposed. d. Continue abrading, with frequent visual checks, until the outline of the cavity edges becomes visible. e. Remove the remainder of the lid over the cavity by attaching a piece of tape and lifting off.
Special microwave packages	1.	There is perhaps less standardization in these packages than in other types. The packages are generally small and therefore difficult to work with. To facilitate handling, the package leads can be soldered to a piece of copper clad circuit board, as demonstrated in Figure 11. These packages are generally ceramic with a metal lid. a. Mechanically anchor the package. b. Using a hand-held grinding tool (such as the Dremel tool) carefully grind away the lid. Care must be used to prevent damage to the microcircuit by metal and/or ceramic particles.
	2.	a. Mechanically anchor the package. b. Using a sharp implement (such as an Exacto knife) scribe around the lid seal until the seal is broken. c. Remove the lid by attaching a piece of tape and lifting off.

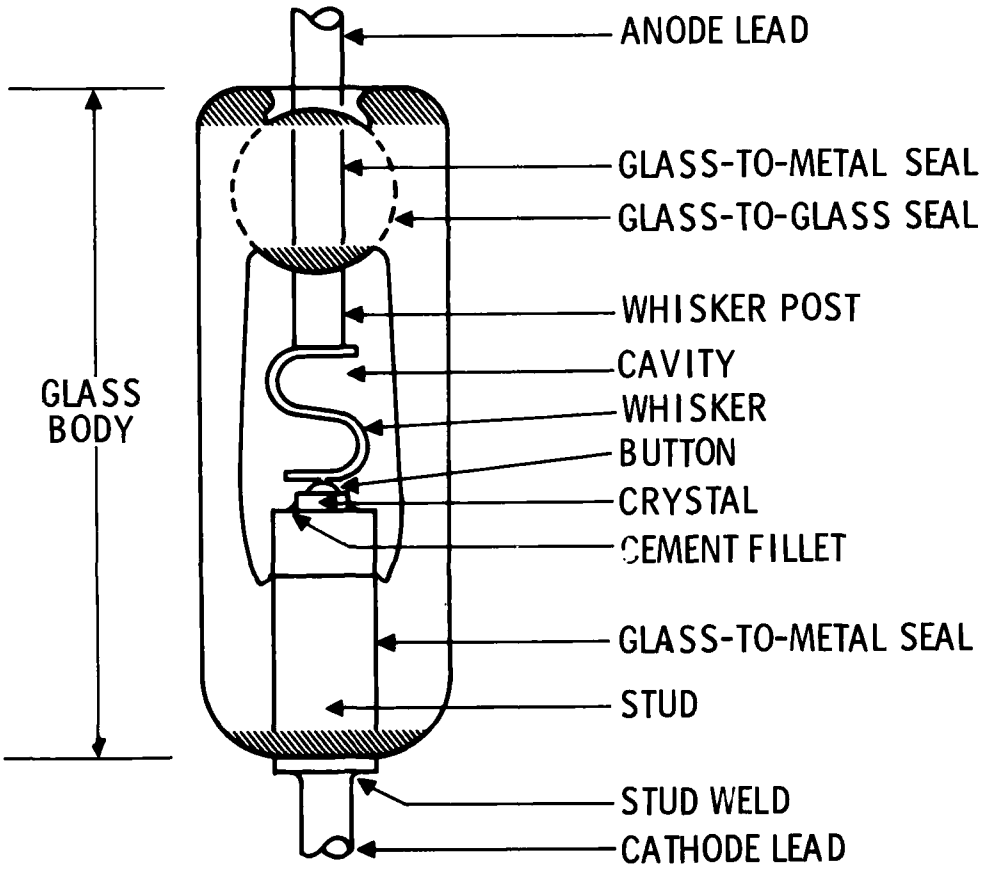

FIGURE 1. WHISKER DIODE (TYPICAL)

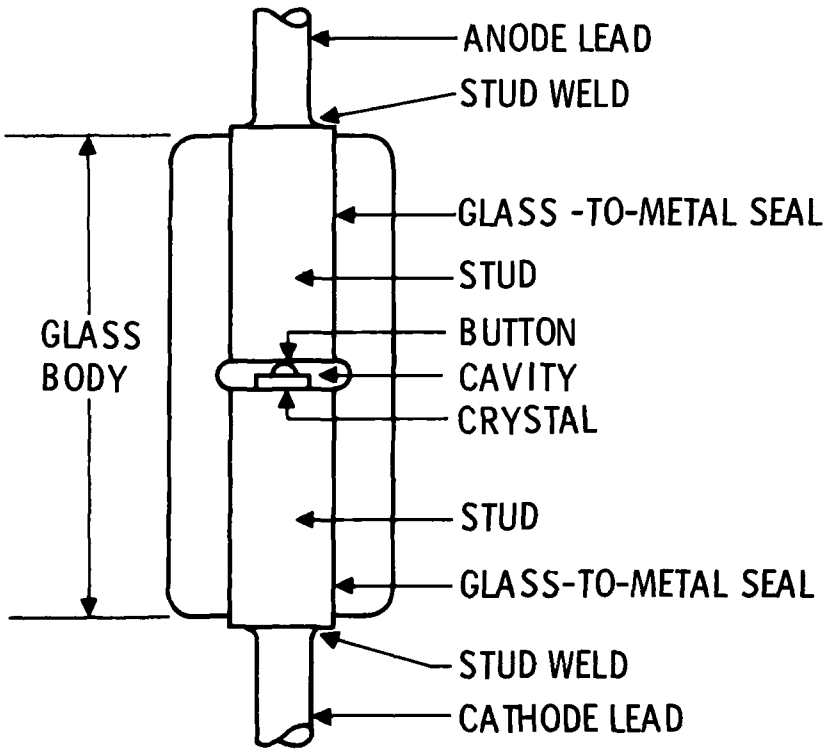

FIGURE 2. DOUBLE HEAT SINK (DHD) DIODE

STUD MOUNT DIODE (TYPICAL)

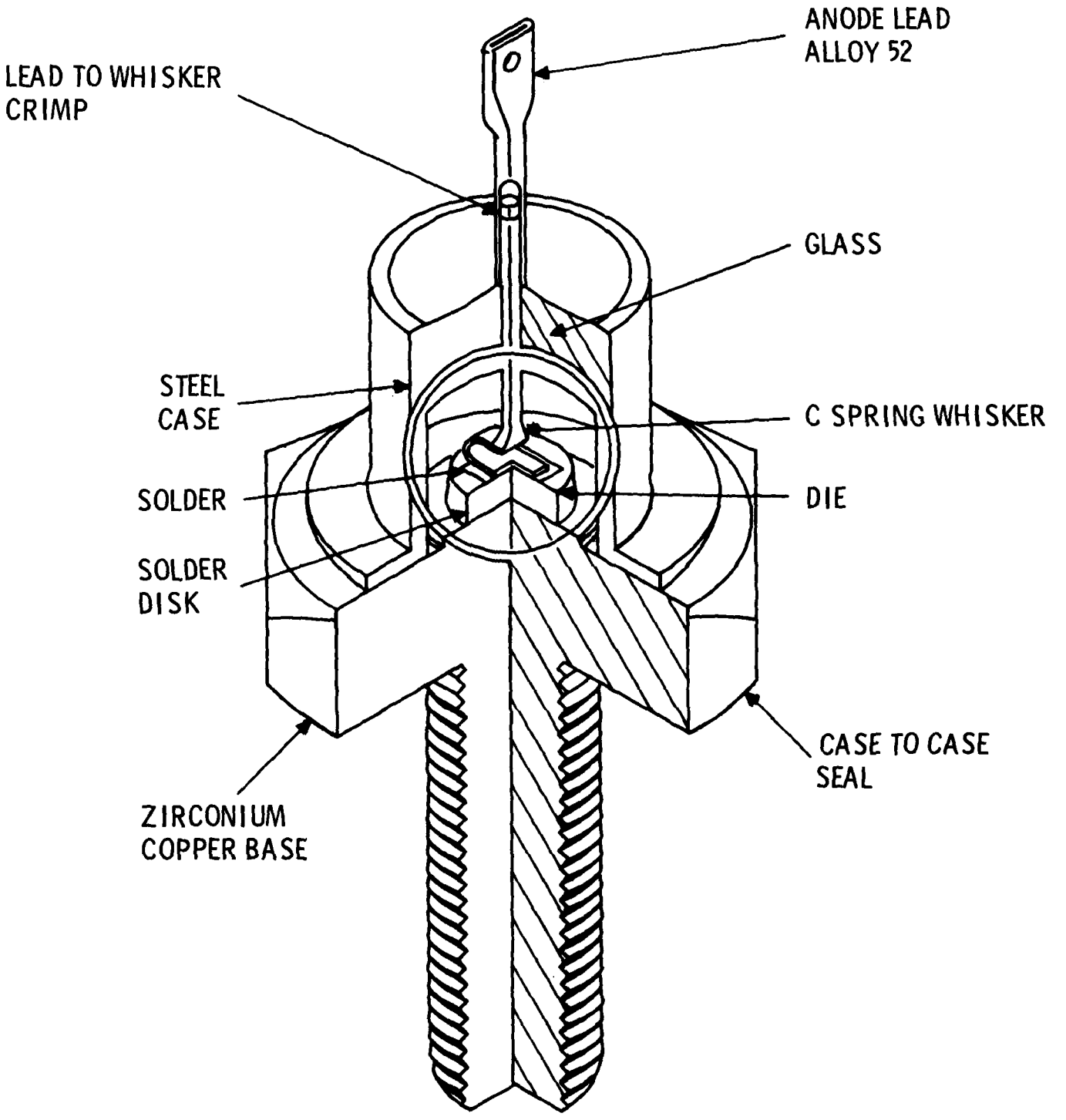

FIGURE 3. STUD MOUNT DIODE (TYPICAL)

FIGURE 4. TRANSISTOR CAN OPENER

FIGURE 5. TRANSISTOR OPENED WITH CAN OPENER

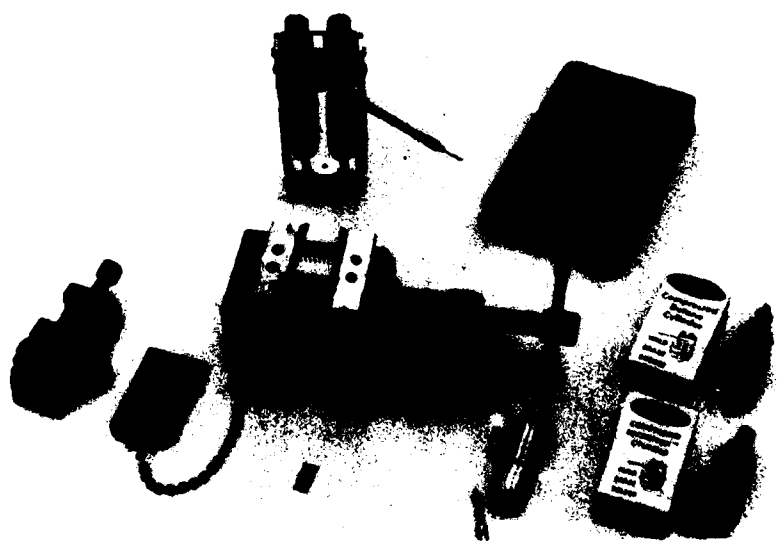

FIGURE 6. EQUIPMENT FOR OPENING CERAMIC PACKAGES

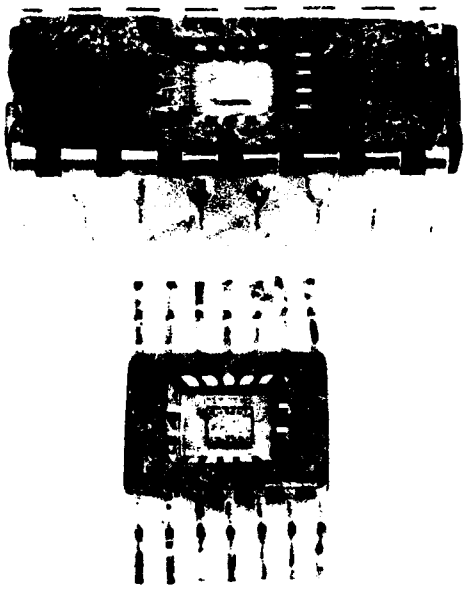

FIGURE 7. CERAMIC PACKAGES OPENED BY ABRADING

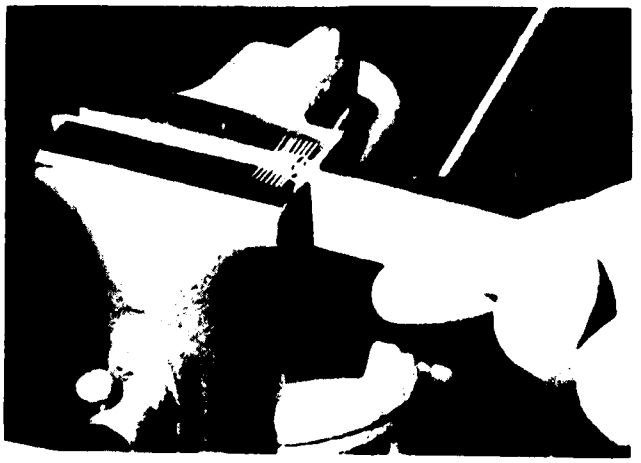

FIGURE 8. METHOD FOR OPENING CERAMIC FLAT PACK PACKAGES

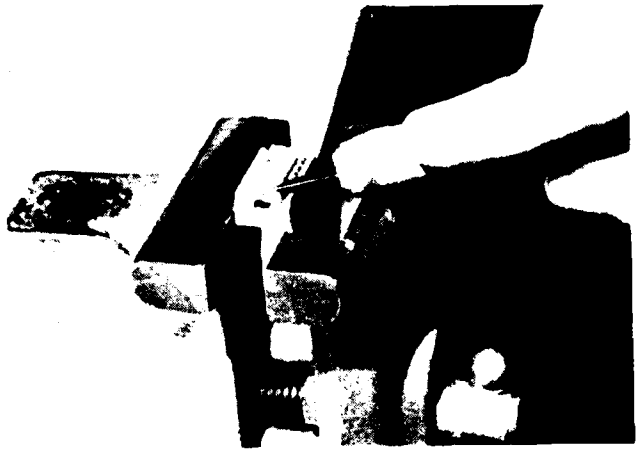

FIGURE 9. TECHNIQUE FOR OPENING METAL LID DIP PACKAGES

FIGURE 10. TECHNIQUE FOR OPENING CERAMIC DIP PACKAGES

FIGURE 11. MICROWAVE PACKAGE OPENED BY GRINDING TOP AWAY

All of the chemicals used in the procedures described below are extremely dangerous. The directions from the manufacturer, where applicable, should be followed explicitly. The use of fume hoods is mandatory, and strict adherence to laboratory safety procedures should be observed at all times. More information on chemicals and safety procedures can be found in Chapters III-M and IV, respectively.

Several methods, involving both wet and dry chemistry, have been developed for opening these packages. As it was mentioned previously, this is not intended to be a complete collection of methods for opening these packages or any other classification of package. This is due to the highly individualistic nature of many failure analysis techniques as performed in various laboratories.

Table II covers decapsulation chemical mixtures, the materials these chemicals will remove, and process steps which should be used as a guide in their use.

Before proceeding with decapsulation, many failure analysts use radiography techniques to pin point the exact locations of chip, header, and wires. Several of the techniques described in Table II involve milling slots or wells over the chip so as to reduce the thickness of material that must be etched through to expose the microcircuit. Radiography is extremely helpful in judging where this well should be located and how deep it should be. However, radiography is not always necessary. For instance, as experience in package opening grows, the failure analyst will become familiar with the locations of microcircuits in many of the parts he deals with routinely (See Chapter III-B for details on radiographic techniques).

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
1	Most molding compounds	a. Concentrated Sulfuric Acid H_2SO_4	In this process, the majority of the encapsulant directly over and surrounding the active device is removed before the etch. 1. Using a milling instrument (such as the Dremel tool) a small well can be milled in the package over the chip location. Radiography would be helpful in judging the depth and position of the well. 2. In a small beaker, boil the acid being used. It is recommended that concentrated sulfuric be boiled to about one half its original volume to remove as much water as possible. 3. To remove moisture from the unit, bake at 200°C for 30 minutes. 4. Immerse the unit in acid, using appropriate care, and monitor until the semiconductor element in the unit becomes visible. It will be necessary to remove the unit from the acid at intervals of 1-2 minutes to monitor because the acid will rapidly become dark in color. 5. Rinse in room temperature acid and then in methyl alcohol. 6. Follow with final DI water rinse, and carefully blow dry. Figures 12 and 13 show a unit before and after etch, respectively.

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES (CONT'D)

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
2	Most molding compounds	a. Fuming Sulfuric Acid b. Fuming Nitric Acid	This process is a selective etch where only the encapsulant directly over and surrounding the active element is exposed. It should be noted that of these acids, fuming nitric is in general the more potent. 1. Using a small milling instrument (such as the Dremel tool), mill a small well over the chip location in the package. See Figure 14 for example. Radiography would be helpful in judging the depth and position of the well. 2. To remove mositure, bake the unit at 200°C for 30 minutes. 3. Heat the unit on a hotplate to a temperature in the range of 60-80°C. 4. Using an eyedropper, and extreme care, fill the well with drops of acid. Allow the unit to remain on the hot plate for approximately 1 minute. 5. Rinse in methyl alcohol to wash away the dissolved plastic. 6. Examine the etched area for complete exposure of the die. 7. If necessary, repeat Steps 3 through 6 until the die is completely exposed. 8. Follow with DI water rinse, and gently blow dry. Figure 15 shows a package opened in this way.

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES (CONT'D)

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
3	Most molding compounds	a. Fuming Sulfuric Acid b. Fuming Nitric Acid	This process is a variant of the selective etch described in Process 2. Many workers in the field of failure analysis have observed that, in using Process 2, the lead frame is often damaged precluding the possibility of electrically retesting the device. This process, although more lengthy, allows more control in restricting the area of the etch to regions more directly above the active device. In this way, the lead frame is subjected to the acid for a reduced time period. In this process a Teflon TFE fixture is milled to hold a specific size package. For instance, a separate size fixture would be necessary for a 40 pin package, one for a 24 pin package, etc. This fixture is milled so that its top edges are level with the top surface of the unit to be etched. The unit and the holder are vacuum baked at 100°C for two hours. Type C FEP Teflon is used to make a seal across the top of the unit and the TFE carrier. This is done through the use of a press where the top platen only is heated to 350°C and 25 pounds of pressure is used. The specific process steps are: 1. Preheat press to 350°C. Set pressure to 25 pounds. 2. Lightly sand IC top and TFE fixture.

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES (CONT'D)

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
3 (Cont.)			3. Place FEP sheet over fixture, treated side down. Place aluminum foil over this. 4. Place fixture on press and lower platen. 5. Wait about 4 minutes, then turn heat off. 6. Remove assembly from press at 200°C. 7. When cool, peel off aluminum and inspect seal. 8. Trim away excess FEP. 9. With a razor blade or knife, cut a window over chip location. 10. Follow Process 1, Steps 2, 4, 5 and 6. Figures 17, 18, and 19 demonstrate this process. For more information, consult Reference 9.
4	Epoxy B/Novolac	Solution of: -Sodium Dichromate 20 pts. by wt. -Conc. Sulfuric Acid 300 pts. by wt. -Distilled Water 25 pts. by wt.	1. Using a small milling instrument (such as the Dremel tool), a well is milled out over the location of the chip in the unit to be opened. Radiography would be helpful in judging the depth and position of this well. 2. The external leads are cut as close to the body as possible. 3. The package is cleaned in DI water, followed by an alcohol rinse and drying. 4. Immerse in etching solution held at 160°C $\pm$ 10°C for approximately 15-25 min.

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES (CONT'D)

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
4 (Cont.)			5. Prepare a mixture of 1:1 concentrated hydrofluoric acid and glycerine. 6. When the internal circuit is revealed, pour the solution prepared in Step 5 over the chip area to remove decapsulation residue. 7. Rinse in DI water. 8. Dry at 40°C.
5	Phenolic Molding Compound	Nitric/Sulfuric Acid Solution	1. With a small milling instrument (such as the Dremel tool), grind away as much of the phenolic material as possible without damaging the chip or wiring inside. Radiography would be helpful in judging the depth and position of this well. 2. Into a small pyrex beaker pour 20 ml of concentrated sulfuric acid. Slowly (3-5 ml at a time) pour 20 ml of concentrated nitric acid into the beaker. 3. Suspend the unit into the solution until it is immersed but not touching the bottom of the beaker. 4. Heat the acid to the boiling point, then reduce the temperature until the bubbling action around the phenolic decreases to only mild action. Cover the beaker with a watch glass. 5. It is necessary to check the unit periodically until the chip is exposed.

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES (CONT'D)

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
5 (Cont.)			6. When etching is sufficient, rinse in acetone. 7. Rinse in DI water. 8. There may be a clear wax or a varnish coating remaining on the surface at this point. If so, immerse the unit in concentrated sulfuric acid for a few minutes at room temperature. 9. Rinse in DI water. 10. Gently blow dry.
6	Molded Silicones Silicone Varnish Urethane Foam Anhydride Expoxies Urethane Coatings	Uresolve Plus Dynaloy, Inc.	1. With a small milling instrument (such as the Dremel tool), a hole is milled over the chip in the unit to be opened. Radiography would be helpful in judging the depth and position of this well. 2. Pour a sufficient amount of Uresolve Plus into a beaker, and cover with a cover glass. 3. Heat the solution to 40°C. 4. Physically restrain the units with some kind of holder, or solder the leads and ends of chip substrate paddles to a length of wire. 5. Immerse the unit into the heated solution. 6. Remove the units from solution periodically to check the state of removal.

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES (CONT'D)

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
6 (Cont.)			7. When removal is complete over the chip, rinse in acetone. 8. Rinse in DI water. 9. Gently blow dry.
7	Potting Epoxies	Dynasolve 100 Dynaloy, Inc.	The procedure here is the same as with Uresolve Plus process number 6, only the solution is heated to 100°C.
8	Some Potting Epoxies	Dynasolve 160 Dynaloy, Inc.	The procedure here is the same as with Uresolve Plus process number 6, only the solution is used at room temperature.
9	Molded Compounds Silicone Epoxy	J-300 Depotting Agent Indust-R: - Chem Laboratory, Inc.	This procedure utilizes the same process steps as described in process number 6, except with regard to temperature and the method of holding the sample in solution. The chemical is heated to the range of 150°C-180°C. Since this is above the melting point of common solder, some other method of holding the sample in solution must be used. A small basket made from stainless steel mesh wire, for instance, makes a good sample holder.
10	Molded Compounds Epoxies	Oxygen Plasma	This is a dry chemistry process. Plasma etching has a dual advantage in that it causes minimum electrical damage or degradation while maintaining mechanical support of the lead frame and chip. The major disadvantage in plasma etching is that it usually requires several days to expose the package contents.

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES (CONT'D)

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
10 (Cont.)			1. With a small milling instrument (such as the Dremel tool), a hole is milled over the chip in the unit to be opened. 2. Areas not to be etched on the package are coated with silicone grease, which is not attacked by oxygen plasma. This masking will maintain mechanical integrity of the package. 3. The unit is then loaded into a plasma unit, and the plasma etch parameters adjusted. Various parameters have been used for the etch cycle. Some of the ranges reported in the literature are: Power Watts: 20 — Flow cc/min: 80-150 — Etch Temp.: 100°C-195°C NOTE: Reported for the Tegal System (#5). The exact etch conditions will vary with different systems. Generally, the higher the power, the higher the etch temperature. It is desirable to determine the proper set of etch conditions to match the equipment and material being etched. 4. The unit being etched is monitored and removed from the etch chamber when the die breaks through. 5. Rinse in DI water. 6. Rinse in isopropyl alcohol.

TABLE II: PLASTIC PACKAGE OPENING TECHNIQUES (CONT'D)

PROCESS NUMBER	PACKAGE MATERIAL	DECAPSULATION CHEMICALS	PROCESS STEPS
10 (Cont.)			7. Gently blow dry. NOTE: Addition of 20-30% Freon gas (CF_4) in the oxygen plasma will greatly enhance the etch rate. This mixture of Freon will also etch silicon dioxide passivation layers at approximately 50 Å per minute. For this reason, the sample must be monitored regularly to prevent damage to the microcircuit. The chamber in which Freon etching is done should be quartz glass. The Freon plasma will rapidly etch pyrex glass.
11	All Plastics	Sulfuric Acid	NOTE: An unconfirmed process for opening all types of plastic packages has been reported on in the literature (Reference 10). The process shows a great deal of promise but remains as yet unconfirmed.

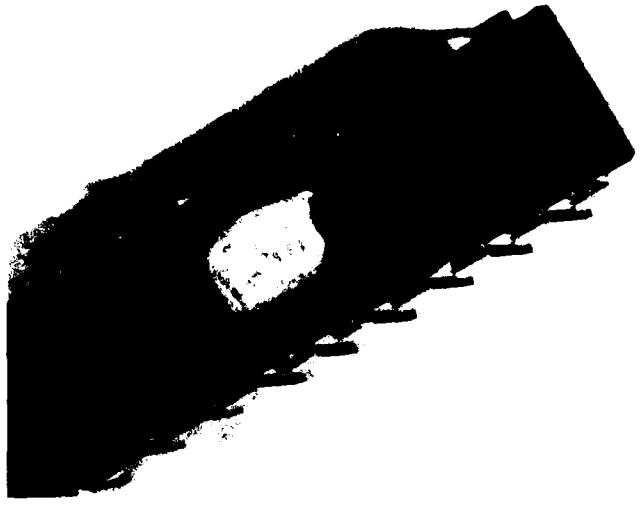

FIGURE 12. PLASTIC DIP PACKAGE WITH WELL MILLED OVER LOCATION OF CHIP, BEFORE ETCH

FIGURE 13. PACKAGE SHOWN ABOVE AFTER ETCH IN BOILING SULPHURIC ACID

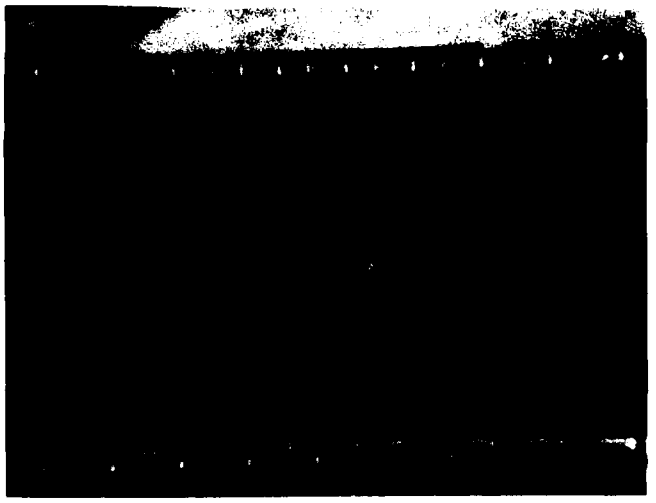

FIGURE 14. PLASTIC PACKAGE WITH WELL MILLED ABOVE CHIP LOCATION BEFORE ETCH

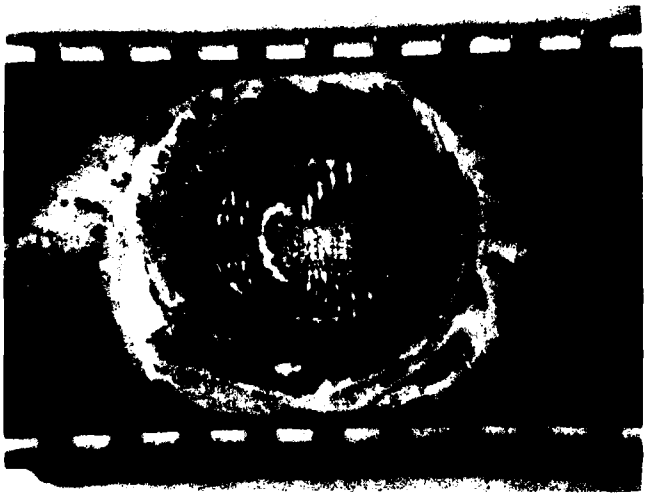

FIGURE 15. PACKAGE SHOWN ABOVE AFTER ETCHING WITH FUMING NITRIC ACID

FIGURE 16. FEP TEFLON ENCASED PACKAGE PRIOR TO ETCH

FIGURE 17. PACKAGE FROM FIGURE 16 AFTER ETCH AND REMOVAL OF FEP TEFLON

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EQUIPMENT

Cross Sectioning Equipment. See Chapter III-O.

Package Opening.

1. Transistor can opener $ 75 - $125
   Signet Tool & Die, Inc., Saugus, Mass.

2. Dremel Tool $ 45 - $ 55
   Emerson Electric Co., Dremel Mfg. Div., Racine, Wis.

3. Microflame Torch, Butane Cylinders, Oxygen (Micronox™) Cylinders
   Microflame Inc., 7800 Computer Ave., Minneapolis, Minn.

General Laboratory Supplies.

1. Graduates
2. Beakers
3. Thermometers
4. Hot plates
5. Tweezers
6. Face mask
7. Apron (See current catalog for pricing)
   Cole Parmer, Chicago, Ill.

Chemicals and Solvents. See Chapter III-N.

F.

THERMAL MAPPING (IR SCANNER) TECHNIQUES

F. Thermal Mapping (IR Scanner) Techniques.

1. Introduction. A primary cause of failure in semiconductor devices is excessive temperature at junctions, leading to thermal runaway or to degradation due to thermally accelerated mechanisms. Thus, it is important to have some means of determining temperatures of operating devices. In most devices that fail, one does not have direct access to junction terminals which would allow electrical measurements, so that the most direct measurement that can be made is the infrared radiation arising at the surface of a silicon chip directly over a junction. A measurement of total power radiated can be converted to absolute temperature if the surface spectral emissivity is known.

Infrared observations can also be used in some instances to examine phenomena interior to a silicon chip. This is possible because silicon is relatively transparent in the near infrared, so that an infrared image converter can sometimes be used to observe die bond quality, carrier recombination radiation, etc.

Although knowledge of surface emissivity may be lacking, one can still use infrared radiation measurements to locate hot spots on device surfaces. The spatial resolution of infrared instruments has absolute limits set by the wavelengths involved, which are some one to three micrometers. Modern LSI circuitry has surface detail coming close to these dimensions, so one should be aware of this in interpreting observations.

Infrared instruments suitable for thermal measurements in failure analysis are, in general, microradiometers or scanners. The former may be used to make spot temperature measurements, or, with mechanical motions may be used to make point-by-point maps of infrared radiance. Scanning instruments may be used for rapid mapping but have the disadvantage that variable surface emissivity renders quantitative measurements more difficult.

2. Thermal Resistance. The thermal behavior of a semiconductor device is often described by a single parameter called its "thermal resistance" or "thermal impedance." This parameter is defined as the rise in temperature of some prescribed point on a device above the temperature of some designated ambient reference point divided by the applied power. The interior point is often taken to be the hottest point of some output transistor on a chip. The reference point is often taken to be some point on the device case or the ambient air surrounding the device. This parameter is useful in describing thermal behavior because, at least for moderate applied power levels, the specified temperature rise is approximately proportional to applied power. Appropriate care must be exercised in selecting the reference point and in calculating the power that is applied to the device in order to obtain useful results. Often, in specific applications, the failure analyst must answer the question, "What was the maximum temperature that occurred at a certain junction when the device failed?" This answer may not be simply obtained by a low power measurement of thermal resistance to a specified reference point. Hot spotting and current crowding may have occurred in operation. Oftentimes, the analyst must attempt to duplicate service conditions to ascertain what actually occurred. Subject to these reservations, the concept of thermal resistance is a very useful entity in failure analysis. The units are usually stated in degrees celsius per watt, (^{o}C/W). Measurements must be taken simultaneously of a junction temperature with infrared techniques and of a reference temperature, usually with a thermocouple.

In a complex integrated circuit, the measurement of power dissipated in a specific junction is often impossible or, at best, difficult. About the best that can be done is to measure total power into the input terminals.

3. Emissivity Measurement and Control. The total radiated energy per unit area of a surface depends on the absolute temperature of the surface and on the spectral emissivity of the surface. Total emissivity of a surface is defined as the ratio of total radiated

energy from a surface to that which would be radiated from a "black body" at the same temperature. The emissivity is always less than or equal to unity.

Two methods may be used to determine the temperature of a point on the surface of a device. In the first, the device is heated to a known temperature by placing it on a hot plate, heated stage, controlled heat sink, etc. The radiomicrometer is focused on the spot in question, and the total radiated power measured. The emissivity can then be calculated from the known temperature. Power to the device is then applied, either with the heat sink at elevated temperature or after it has been allowed to cool. From the known emissivity and the measured radiated power, the temperature of this spot can be deduced.

In the second method, a thin coating of a material of known high emissivity is applied to the spot in question. A suitable material is "Krylon" black spray lacquer. A small amount of this lacquer is sprayed into a suitable receptacle. It may be thinned with toluol. A wooden sliver such as a match stick is sharpened to a fine chisel point. A drop of lacquer can be picked up and deposited where desired. Some experimentation will show the amount and consistency required to give a proper coating. Coatings a few μ meters thick are adequate and do not change thermal properties drastically. Once the coating is applied, it must be dried because cooling from evaporation will cause erroneous results.

The emissivity of the coating material should be measured to be sure that it is correct. This type of lacquer should have an emissivity of approximately unity.

A coating of this type can be applied successfully to a chip several millimeters square. If this is done, the search for emissivity is facilitated by removing the necessity for correcting for hot spots. It has the disadvantage that one can no longer see surface detail optically, and the lacquer may introduce surface electrical leakage.

4. Reference Point Measurement. When the reference point for a thermal resistance measurement can be seen with the radiometer (for example, when one is comparing the temperature rise of a transistor junction over that of the upper surface of a hybrid circuit), it is convenient to measure both the elevated temperature and the reference temperature with the infrared instrument. Black lacquer at both points will facilitate these measurements. This mode has the virtue that the same instrument is used to measure both temperatures, and the temperature elevation, which is a difference, can be more accurately measured since some calibration errors will tend to cancel.

In the event that the reference point is not accessible to the optics, then some other means must be used for its measurement. This case arises when, for example, the reference point is the lower surface of a package. Thermocouples may be used, but it is absolutely necessary that proper procedures be followed. The thermocouple element must be constructed of as fine wire as is feasible to avoid heat losses, and the junction must be properly bonded to the surface in question. The best method for a metal object is to drill a hole just equal in diameter to that of the thermocouple bead, whose depth is slightly more than the bead radius. The bead is then either peened into the hole or bonded with a suitable agent, such as epoxy. The thermocouple wires should, if at all possible, be laid down flat on the surface for at least 20 wire diameters and bonded thereon with a suitable material. This insures proper thermal contact, so that heat flow through the interface between the bead and the material does not cause false measurements. The thermocouple should be referred to a proper ice reference, or a stable automatic junction corrector should be used. The thermocouple voltage may be measured with a high impedance (10^{10} ohm) digital millivoltmeter or with an instrument expressly designed for this service. With proper precautions, temperature errors less than 0.05°C can be realized.

If a thermocouple is attached to this sample, its indication can be used to calibrate the radiometer reading by using a heated stage. This tends to minimize some of the errors inherent in taking the difference of two temperatures.

5. Applying Power to a Damaged Device. In performing failure analysis, the analyst is often confronted with the task of attempting to measure thermal properties of a transistor which has failed in service or which has several interconnections to other parts of a circuit. Ingenuity must be used to make such measurements. Even if a transistor is damaged and cannot be powered in the usual manner, it may be possible to run a single junction in breakdown. A constant current supply is useful in this case, or a large series resistor external to the circuit may be used to control the current.

Sometimes, a hybrid circuit may be rewired. It may be necessary to remove some leads, cut some current-carrying runs and bond new leads in order to isolate the device in question, if bonding facilities are available.

Even on a single integrated circuit chip, a device may occasionally be isolated by scribing some runs with a micromanipulator, or burning them out electrically. These measures are destructive and should be resorted to only when all available evidence has been collected and documented.

6. Case Opening. Infrared observations have the disadvantage that the device case must be open in order to make measurements. Case opening or delidding is always a partially destructive procedure and sometimes is totally destructive, in that unforeseen accidents may fracture microcircuits, obscuring evidence that may be important in failure analysis. In addition, if hermeticity tests or residual gas analysis are deemed advisable, they must

obviously be performed prior to attempts to open the case. It is also necessary to perform a thorough visual inspection before case opening or delidding, preferably with a microscope of adequate magnification to reveal any flaws that may exist. As complete electrical measurements as possible must also be completed prior to case opening, so that accidental damage does not preclude the obtaining of these data.

Although the thermal conditions that prevail in a device open to the atmosphere are different than those found in a hermetically sealed package, measurement errors due to convection cooling in any reasonable sized device are only a few percent, since the great bulk of heat removal is almost always accomplished by thermal conduction through the chip, chip bond, case bottoms, and package leads These remarks obviously do not apply to depotted plastic encapsulated devices where heat removal is primarily by thermal conduction through the lead frame. Conformal coatings may also be present, particularly in hybrids, and some judgement may be necessary in interpreting thermal test results in this case.

7. Typical Equipment. Two basic types of equipment are used in making infrared thermal measurements, the single-spot infrared radiometric microscope and the infrared scanning imager. Figure 1 shows a typical single-spot infrared microscope, a model RM-2A manufactured by Barnes Engineering Company. The optical diagram for a Barnes Engineering Company Model RM-2A is shown in Figure 2.

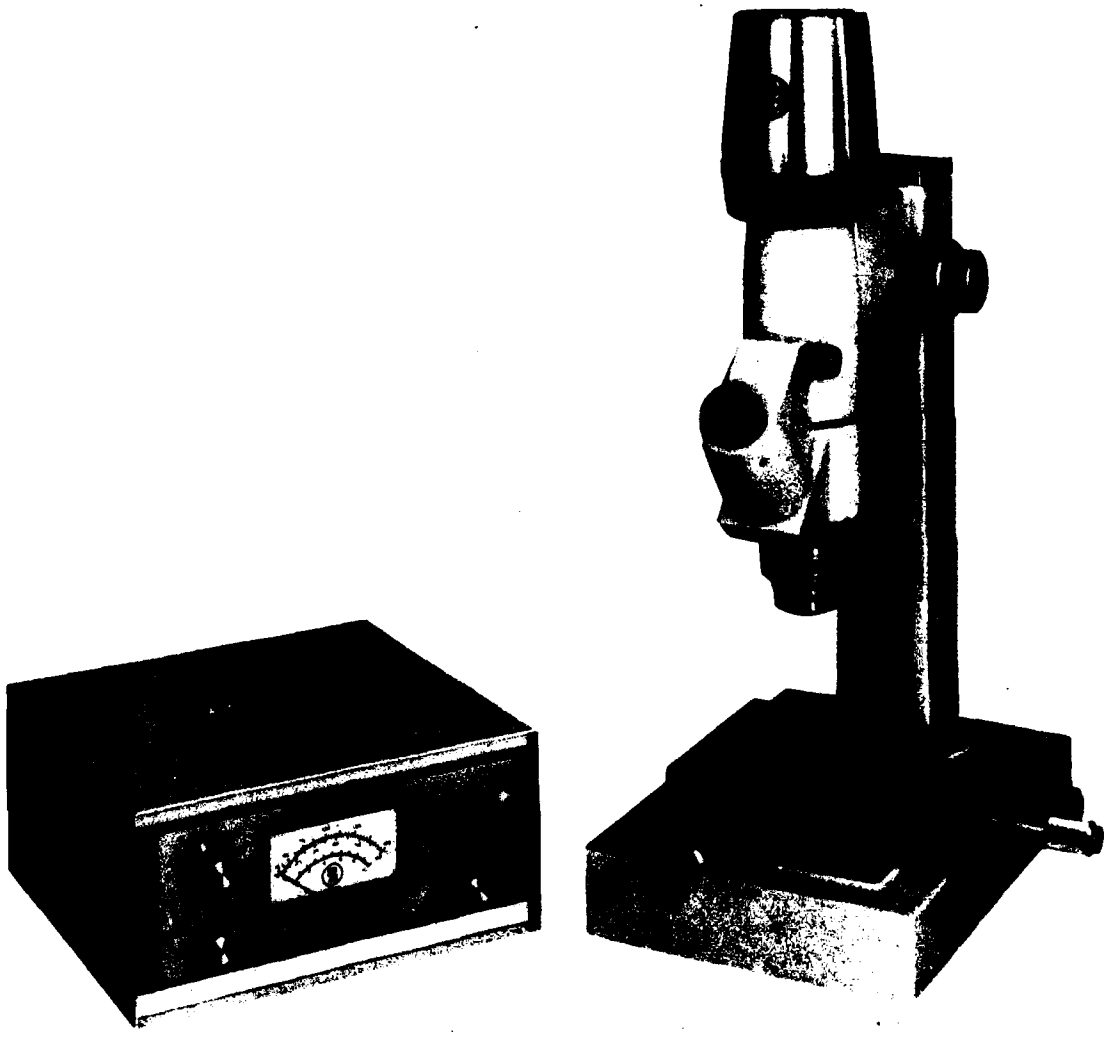

Figure 1. SINGLE-SPOT INFRARED MICROSCOPE
(Courtesy of Barnes Engineering Company)

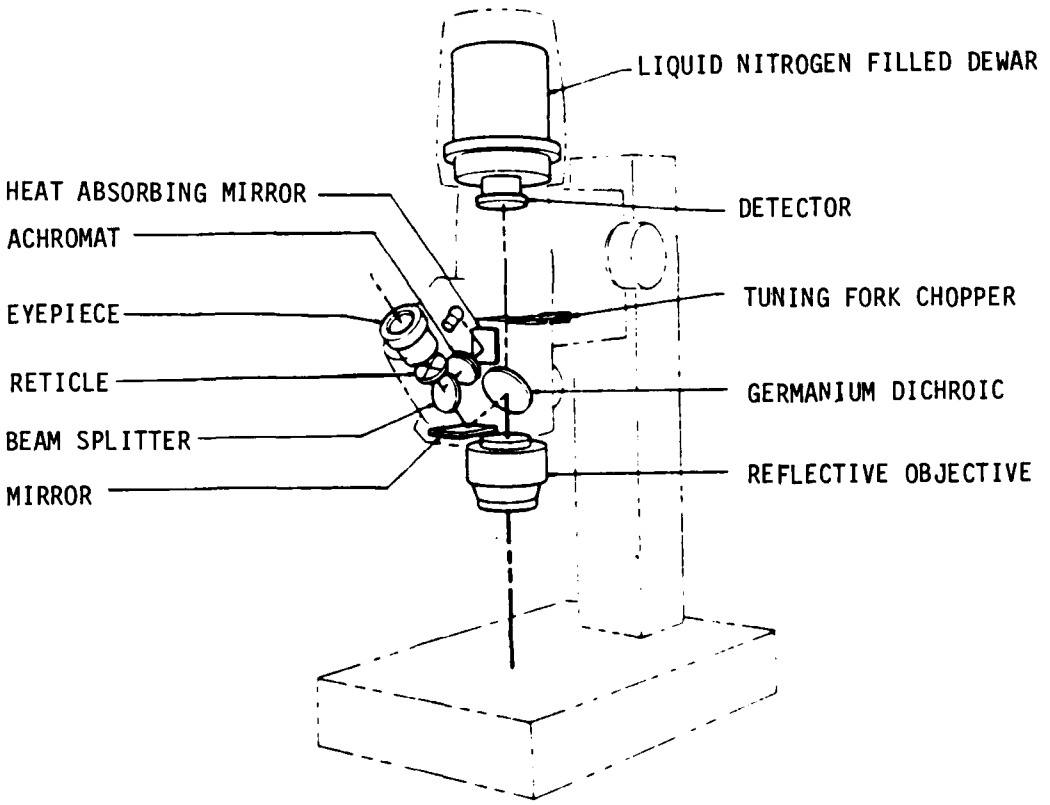

FIGURE 2. OPTICAL DIAGRAM FOR RADIOMETRIC MICROSCOPE

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EQUIPMENT

Radiometer

1. Single-Spot Infrared Radiometric Microscope
   Model RM-2A
   Barnes Engineering Company, Stamford, Conn. — $ 9,975

   Objective Lenses
   RM-164
   Barnes Engineering Company, Stamford, Conn. — $ 2,150

   Calibration Source
   RM-121
   Barnes Engineering Cmmpany, Stamford, Conn. — $ 915

   Specimen Heater
   RM-122
   Barnes Engineering Company, Stamford, Conn. — $ 915

   Microscope Stages
   RM-113 1" x 1" travel — $ 465
   Barnes Engineering Company, Stamford, Conn.

2. Infrared Radiometric Imager
   RM-50
   Barnes Engineering Company, Stamford, Conn. — $27,700

   Thermoelectric Sample Stage 1.25" x 1.25" — $ 1,600
   Barnes Engineering Company, Stamford, Conn.

   Specimen Heater
   Barnes Engineering Company, Stamford, Conn. — $ 865

G.

PHOTORESPONSE MEASUREMENT TECHNIQUES

G. Photoresponse Measurement Techniques.

1. Introduction. Photoresponse scanning is an effective non-destructive technique for analyzing devices which can be damaged by electron beam examinations. It is particularly useful in analyzing MOS devices which can be damaged by electron beam energies. Photoresponse scanning is non-destructive so it does not preclude the failure analyst from using other analytical procedures in subsequent steps. A number of implementation schemes have been used, and the resolution of the various approaches range from 10 μm to 1 μm.

Photoresponse scanning has been used to accomplish the following by various investigators:

a) Define the extent and location of any undesired inversion on the surface of an integrated circuit

b) Monitor the logical operation of digital devices and to change the state of individual logic elements with the light beam

c) Electronically map temperature in a transistor

d) Detect the location of hot spots that develop under certain operating conditions

e) Reveal areas of nonlinear operation in a device under optical scanning

f) Map dc and high frequency gains in transistors

g) Life time measurements

h) Reveal various anomalous effects in active junction regions

The photoresponse scanner can be used to determine the uniformity of a resistive area; if the resistor is in the base circuit of a transistor biased in its active region, this current can be amplified to give an enhanced photoresponse.

In FET transistors and integrated circuits, the light spot can cause an increase in the current in the channel. With proper interpretation one can tell which transistors in MOS arrays are on and which are off.

It is particularly useful to the failure analyst in a comparative manner, i.e., comparing a "good" unit optical scan response with the defective or suspect unit optical scan response. This approach allows the relatively inexperienced user to obtain some qualitative information.

2. Technique Description. A moving light spot, usually generated by a mechanically deflected laser beam, has the effect of generating current carriers in the semiconductor material. In the simplest case, this can cause a current in an unbiased junction if the light spot falls sufficiently close to the junction. This current can be measured in an external circuit connected to the device being scanned. As the light spot is swept across the device being scanned, the amplitude of this current will vary as the composition of the semiconductor device changes. This current variation is the information that is used to present a photoresponse map of the device being scanned. The current variations are simply amplified and fed to a cathode ray display which is driven in synchronism with the laser scan. The information is obtained by interpreting the map produced.

The system works equally well for mapping reversed-biased junctions. In this case the light spot, in generating carriers, causes the reverse current to increase. This change of current can be produced in the same manner as for the non-biased junction. If a

transistor biased in the active mode is observed using the laser scanner, a change in the base-collector junction current may be amplified by the transistor being scanned to give an enhanced photoresponse map.

Another category of studies that can lend itself to observation on the scanner is that of resistivity. In particular, a resistor in an integrated circuit can show a photoresponse when the circuit is scanned. Again, the light spot creates carriers in the semiconductor material, but in this case the semiconductor becomes more conductive and the current passing through the resistor increases. For the resistor to be detected on a photoresponse map of the device being scanned, the resistor must be carrying a current.

3. Equipment Required. A number of investigators have constructed systems capable of displaying photoresponses of semiconductor devices. At the *fifth annual* symposium on the Physics of Failure on November 15-17, 1966, Potter and Sawyer presented a description of a photoresponse scanning system using oscillating mirrors to scan a focused beam of laser light over the surface of the device. At the same symposium, Haberer illustrated a photoresponse system using a demagnified raster from an oscilloscope screen onto the device surface to obtain photoresponse mapping of semiconductors. Tihanyi and Pasztor have used a Nipkow disc to generate a raster on the device surface. The typical spatial resolution of these systems ranges from 5 to 10 microns because of the spot size usually obtained with these systems. Kasprzak has demonstrated a system with a spatial resolution of approximately 1 micron utilizing a Pockel cell to amplitude modulate the laser beam and a lock-in amplifier to produce the desired signal level and rejecting noise by amplifying only the modulation frequency.

Basically, all of the systems (with the exception of the Haberer demagnified raster from an oscilloscope screen) require a:

a) Laser Light Source
b) Scanning Capability (Light Source/Sample)
c) Reflected Light Imaging (Topographical Information)
d) Signal Processing Electronics

4. Skills Required. The analyst or user of the equipment should have sound fundamental training in these areas:

a) Laser Operation and Alignment
b) Optical Alignment Procedures
c) Electronic Signal Mixing
d) Display Electronic Instrumentation
e) Solid State Electronics

5. Procedure. The procedure that will be described in some detail is based on the National Bureau of Standards system outlined in excellent detail in NBS Special Publications 400-24 and 400-27.

This system incorporates two low-power, continuous wave helium-neon lasers. One of the lasers operates at a wavelength of 0.633 μm in the visible portion of the spectrum and the other at a wavelength of 1.15 μm in the near infrared. A movable slide in the optical paths of the lasers allows the user to select which of the lasers is to be used for a particular experiment. The chosen laser is sequentially reflected from two nodding scanning mirrors which oscillate in orthogonal directions. The moving light spot forms a raster on the specimen upon being directed through the camera tube of an optical microscope. The specimen is electrically connected to a cathode ray display which is deflected in synchronism with the scanning mirrors.

A complete block diagram of the dual-laser photoresponse scanner is shown in Figure 1.

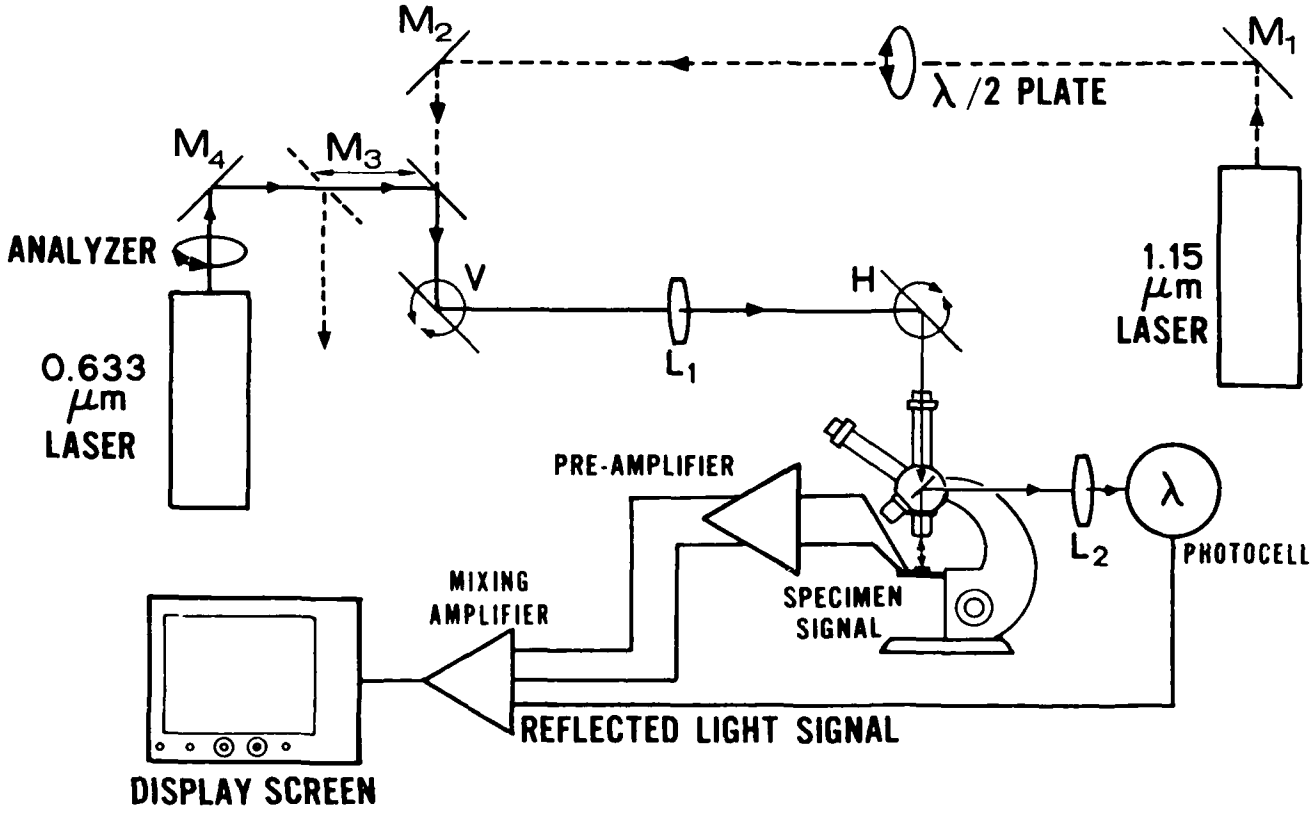


FIGURE 1. THE LIGHT AND SIGNAL PATHS OF THE DUAL-LASER SCANNER
(After Sawyer/Berning-N.B.S.)

The laser scanner incorporates a reflected light circuit to enable one to obtain a map of the topography of the specimen being scanned. This circuit makes use of a half-silvered mirror that is built into the microscope for vertical illumination purposes when the microscope is used in a normal manner. Some of the laser light that is reflected from the specimen as it is scanned is collected by the microscope's objective and subsequently reflected from the half-silvered mirror in the microscope. This light passes out of the microscope through the vertical illuminator. In order that the microscope could retain its vertical illumination capability, a second half-silvered mirror was placed in the vertical illuminator tube to direct the reflected light out of the tube and through a lens L_2 and onto a germanium photodiode. The second half-silvered mirror makes it possible to use either the vertical illumination or the reflected light circuit without changing any parts. The lens L_2 focuses the raster of the reflected light to a point on the photodiode. Refocusing to a point is necessary so that irregularities in the photodiode do not distort the electrical signal obtained from that device when the scanning mirrors V and H are driven to fairly high excursions. A germanium photodiode was chosen over a silicon photodiode because the germanium responds to both the 1.15 μm laser and the 0.633 μm laser.

The photocell provides an electrical signal which can be used to obtain a spatial map of the REFLECTANCE of the specimen being scanned by the laser radiation. Another electrical signal can be obtained from the specimen at the same time, and this signal is extracted by simple electrical connections to the device being scanned. This is the PHOTORESPONSE signal, and it can be used to display spatially the electrical response of the specimen to the laser radiation. This photoresponse signal is generally of greater importance in studying semiconductor devices than the reflected light signal, the reflected light signal being mainly used to identify areas on the specimen that give a photoresponse signal. Both the response signal and the reflected light signal are generated at the same time and are thus synchronized.

Electrical signals generated within the specimen as a result of the laser scanning the device, as well as the electrical signal developed by the reflected light photodiode, are amplified and modulate the electron beam of a cathode ray display. The electron beam of the display is deflected horizontally and vertically at the same rates and in synchronism to the deflection of the scanning mirrors. A point-to-point correspondence is thus established between the position of the laser spot on the specimen and the position of the electron beam on the display. As the light spot and the electron beam move, the electrical signals from the device and/or reflected-light photodiode, in modulating the electron beam, produce a picture of the response of the specimen on the display screen.

Figure 2 is a block diagram showing the important elements in the electrical section of the system. The MIXER is the heart of the electrical system. Its signal processing capabilities include signal amplification from up to three sources, addition and subtraction of these signals (mixing), and superimposing the signals onto the vertical deflection waveform driving the display for the vertical deflection type presentation. The mixer allows signals from the specimen and the reflected light photodiode to be mixed in any desired proportions so that a display of the specimen's photoresponse, for example, can be superimposed on a topological display generated by the photodiode. Any signal, or combination of signals from the specimen can be mixed with the deflection waveform that is used for vertical deflection of the electron beam on the display screen. This is a display technique which provides a picture which appears to have a three-dimensional quality. An advantage of this presentation mode is that it allows quantification of the specimen's photoresponse, since the deflection of the spot on the cathode ray tube display, as compared to a change in spot intensity, can more easily be measured. With the mixer, either the conventional spot intensity modulation or the vertical deflection modulation or both can be used. An overall view of the NBS Laser Scanner is shown in Figure 3.

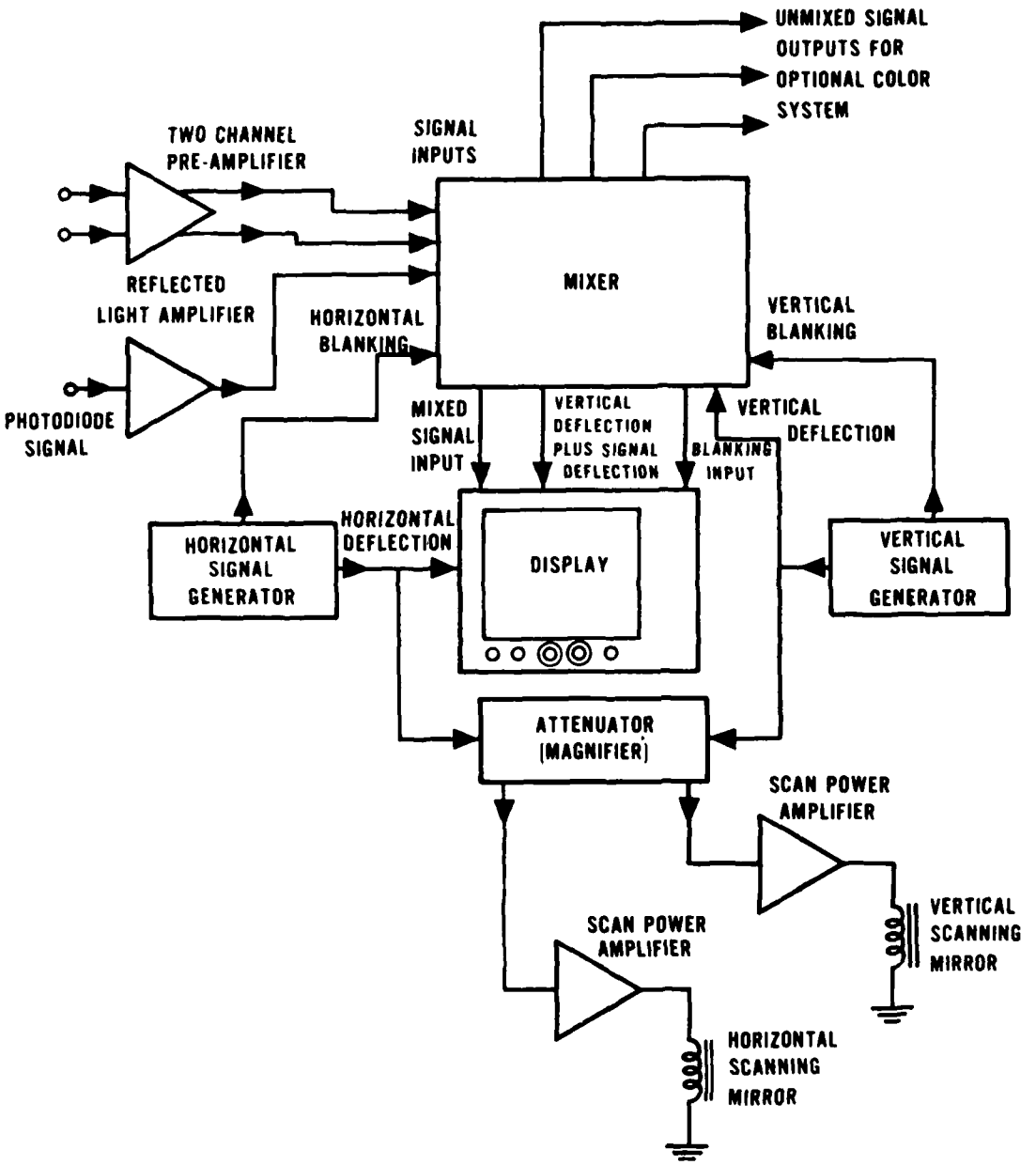


FIGURE 2. A BLOCK DIAGRAM OF THE ELECTRICAL INTERCONNECTIONS FOR THE SCANNER
(After Sawyer/Berning-N.B.S.)

FIGURE 3. OVERALL VIEW OF THE LASER SCANNER

In performing the photoresponse technique, a number of critical steps must be considered:

a) Specimen Connection
b) Magnification/Achievement of Optimum Definition
c) Optimizing Scanning Rates

A number of specimen connections to the electronics are illustrated in Figures 4 thru 7. The specimen must be placed under the scanning light spot so that it is as level as possible to obtain uniform focus on the chip area. Many specimens are sensitive to room light, and the lights should be kept dim, particularly if they are of the fluorescent type, as the line frequency modulation of the room light is readily transformed into a modulation of the specimen signal by the specimen. It is often desirable to terminate the inputs to a high-gain linear device with low resistances; otherwise,a very large signal is obtained from the input transistors.

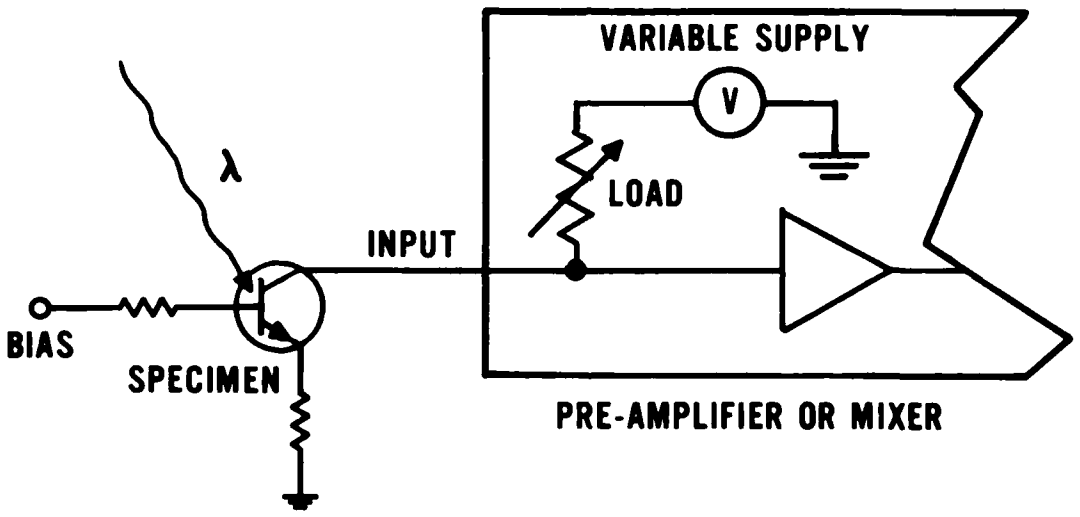


FIGURE 4. TYPICAL HOOKUP OF SPECIMEN TO ELECTRONICS

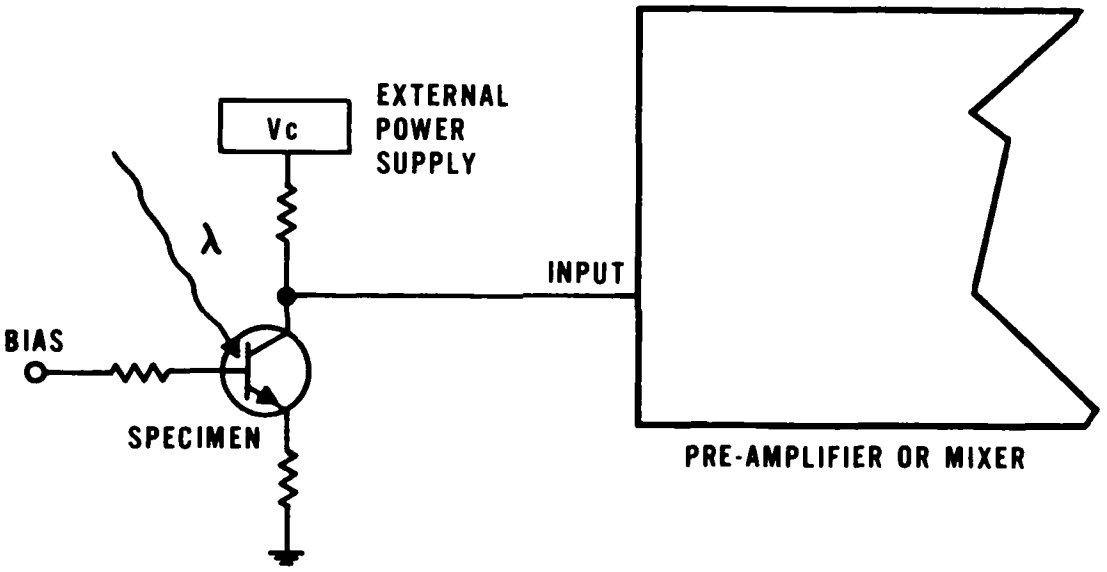


FIGURE 5. HOOKUP OF SPECIMEN TO ELECTRONICS WHEN AN EXTERNAL POWER SUPPLY IS USED

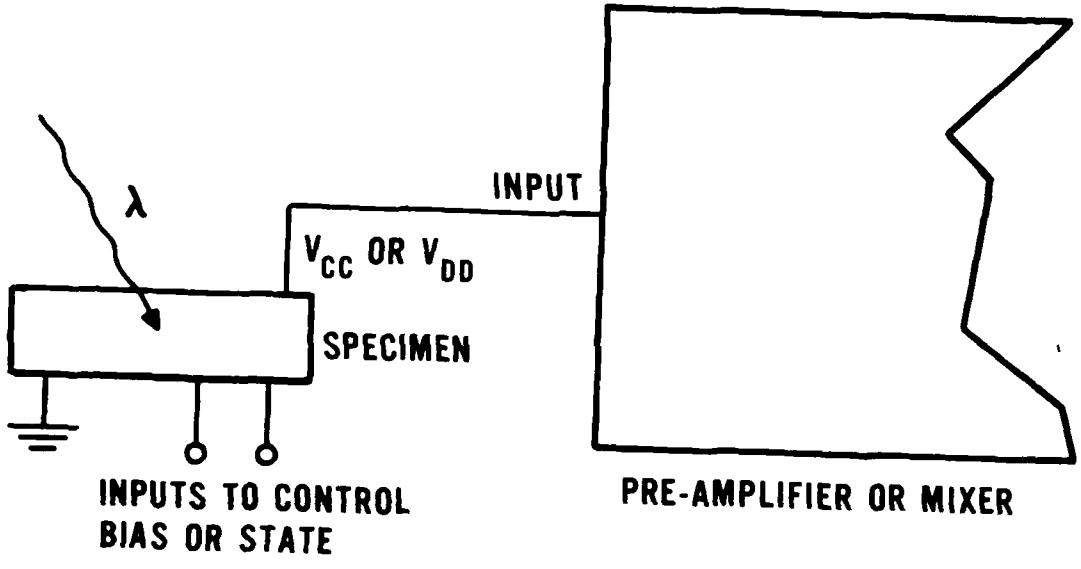


FIGURE 6. CONNECTION OF A TYPICAL INTEGRATED CIRCUIT SPECIMEN TO THE SCANNER'S ELECTRONICS

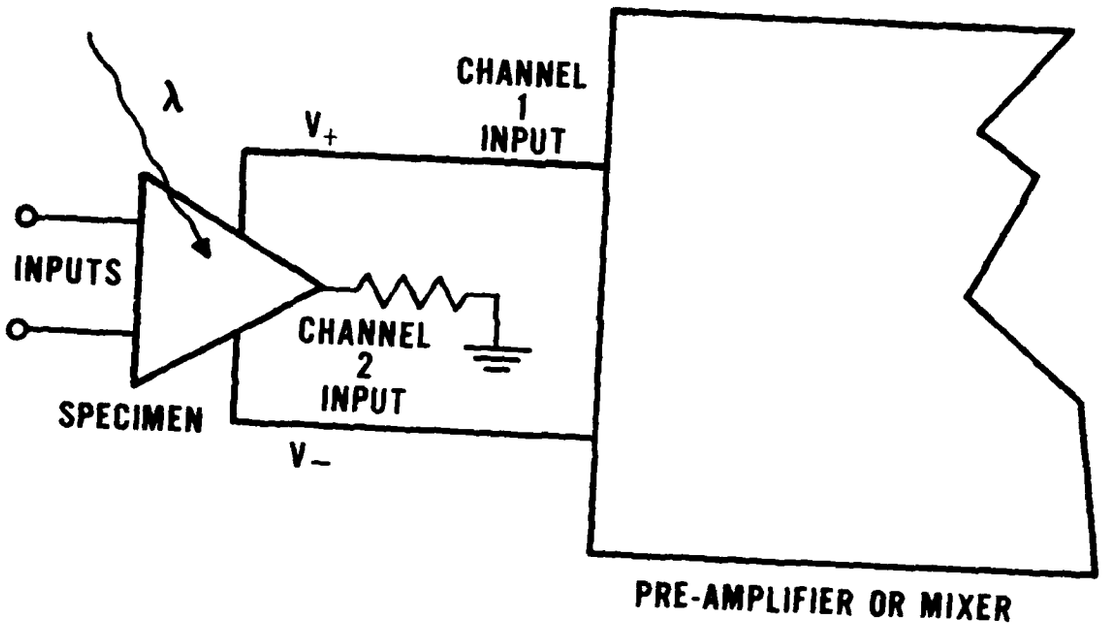


FIGURE 7. HOOKUP OF AN INTEGRATED CIRCUIT SPECIMEN WHEN THE CIRCUIT REQUIRES TWO POWER SUPPLIES

The optimum definition, that is, the maximum number of distinct objects that can be seen on the display, is obtained by setting the attenuator that controls the scanning mirror excursion so that the mirrors have the largest excursion without the light raster being vignetted by the microscope optics.

In general, it may be best to use the fastest scanning rates that the scanning mirrors will allow because it is important that a picture of the specimen is produced in the shortest possible time. This reduces the effects of drift in the specimen or electronics and is particularly appropriate when the display is being photographed. The fast scanning rates also make it easier to view the display in real time, especially the color display because fast-decay phosphors are used.

Many specimens have carrier storage effects which make it necessary to use slower scanning rates to maintain resolution. Situations where these storage problems occur are usually made apparent by blurring of vertical lines in the image. Solar cells are particularly susceptible to these storage problems.

6. Checklist for Getting the Picture. Some of the critical steps that need to be taken to obtain a monochromatic picture of a particular specimen as quickly as possible are as follows:

a) Adjust mixer/amplifier electronics as required.
b) Set brightness on display so that a dim raster can be seen.
c) Set magnifier/attenuator on 1000 μm.
d) Install 8X objective in microscope.
e) Locate specimen on microscope stage.
f) Verify that specimen connections are as required for device type.
g) Adjust movable slide in the microscope so that laser is blocked and the eyepiece is activated.

h) Energize the lamp in the vertical illuminator, and focus the microscope onto the specimen.

i) Reset the prism slide so that it allows the laser to impinge on the specimen; turn off the illuminator.

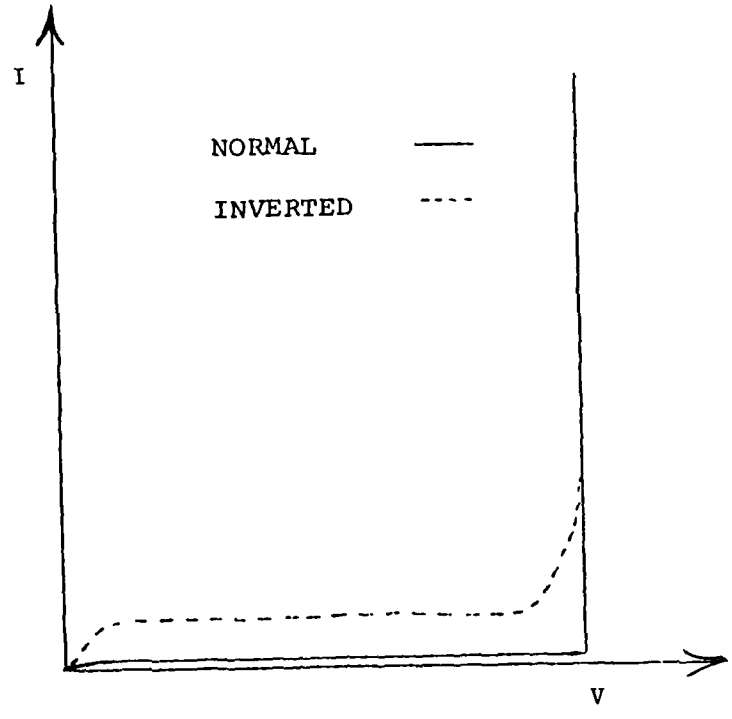
j) See that the scanner is working by using the reflected light signal.

k) Adjust offset, gain, load resistor controls to obtain the optimum photoresponse signal.

l) The photoresponse image can be superimposed on the reflected light image by use of the mixer controls.

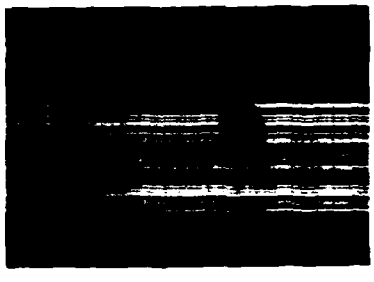
*CAUTION: Care must be exercised to avoid having either the infrared laser radiation or the visible laser light reflected into the eye.

7. Typical Photoresponse Analysis. Figure 8a illustrates the electrical curve tracer characteristics of a collector-base junction for a normal and an inverted junction. A topographical view of the collector-base region of the inverted transistor is shown in Figure 8b with the region labeled A as being suspicious. Utilizing the intensity modulation mode of the photoresponse scanner, the inverted area is clearly discernable in Figure 8c. In this case, the surface inversion in area A was a P type skin on the N type collector material.



a. CURVE TRACER CHARACTERISTICS

b. TYPICAL TRANSISTOR WITH A SLIGHTLY INVERTED CURVE TRACER CHARACTERISTIC ≃800X



c. INTENSITY MODULATION AREA SCAN OF INVERTED TRANSISTOR ≃800X INVERSION AT AREA A (AFTER KASPRZAK)

FIGURE 8. TYPICAL PHOTORESPONSE RESULTS

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EQUIPMENT

DESCRIPTION	ESTIMATED COST
1. Binocular Microscope Suitable for use with polarized light, including camera tube, vertical illuminator port, prism slide to change optical paths between specimen and camera tube. Needs large stage travel and a large working distance.	$ 3 - 5K
2. Lasers a) 0.633 μm, 3mW CW HeNe noise less than 2% b) 0.633 μm, 5mW CW HeNe noise less than 2%, mirrors changed to cause it to operate at 1.15 μm	$ 1 - 2K
3. Signal Generators a) Waveforms available simultaneously sine, square, triangle, ramp, sync pulse b) Frequency: .005 Hz to 1 MHz c) Output impedance: 600 Ω or lower	$500 - 1.5K
4. Analyzer Rotatable polarizing optical component	$ 1 - 2K

EQUIPMENT

	DESCRIPTION	ESTIMATED COST
5.	Half-Wave Plate	$500 - 1,000
	Mica-between-glass type for 1.15 μm radiation	
6.	Monochromatic Display	$ 1 - 2K
	a) Bandwidth: DC to 20 MHz on X, Y, and Z inputs b) Digital dc blanking, blanked +5V, unblanked -5V	
7.	Scanning Mirrors and Amplifier Systems	$ 2 - 3K
	a) Galvanometeric type nodding mirrors b) Frequency response dc to 1 kHz	
8.	Reimaging Lens System	$ 1 - 2K
	a) TV Camera Lens f_1 = 50 mm f_{number} = 2 f_2 = 25 mm f_{number} = 1.4	

H.

LIQUID CRYSTAL ANALYSIS TECHNIQUES

H. Liquid Crystal Analysis Techniques.

1. Introduction. The use of liquid crystals in failure analysis has increased a great deal recently. The applications of liquid crystals have grown from the relatively simple technique of identifying local hot spots to aiding in the more difficult tasks of locating submicron oxide defects and in circuit layout mapping. This latter technique is still in its infancy but nevertheless shows great promise. The following sections begin with the simplest liquid crystal technique and end with the more involved techniques.

WARNING: Particular care should be used when handling liquid crystal materials. The toxicity of some of these materials is listed as unknown. This should be kept in mind at all times when handling liquid crystal materials.

2. Hot Spot Location Technique. This technique uses cholesteric (heat sensitive) liquid crystals to locate areas of high power dissipation in microelectronic devices (Reference 1). Shorted junctions, metal lines with shorts to underlying structures, and oxide breakdown failures can be analyzed with this technique.

This type of liquid crystal responds to changes in temperature by changing color. The material that is most useful in failure analysis work responds in the temperature range of 30° - 32°C with color changes in this range from red to violet. The fact that this working temperature is just above room temperature eliminates the need for using a stage with heating and cooling capabilities (Kits are now available which allow tailoring a solution for a specific temperature range. See page III-H-14).

Before using liquid crystal material to locate a suspected short circuit, it will be necessary to expose the microcircuit element inside a packaged device (See Chapter III-E for details on package opening). Some means of making electrical contact to the device will be necessary.

FIGURE 4. CMOS MICROCIRCUIT WITH ELECTRICAL BIAS AND CHOLESTERIC LIQUID CRYSTALS APPLIED.

The liquid crystal material can be applied to a microcircuit with a fine tipped brush. It is necessary to dry the material by baking for several minutes at 50 °C. Indirect illumination is used while the microcircuit is observed under a stereo microscope. The short circuit is first forward biased and 100-200 mA of current is allowed to flow for a few seconds. A large area will be affected by the heat generated and will go through the color range to violet (hottest of all the visible colors).

After violet color level is reached, the current is reduced and the voltage bias reversed. This will force localized heating at the shorted area. The shorted area can be identified by its color, which will remain at or close to the violet end of the spectrum while the surrounding area will cool down and change color. Color rings will be visible around the area where the short is located. If the current through the shorted area is varied carefully, it may be possible to resolve small areas by observing the motion of opaque particles suspended in the liquid crystal material.

3. Oxide Defect Location Technique. This technique uses nematic liquid crystals in a current sensitive dynamic scattering cell to locate defects in insulating layers. Extremely small pinholes in MOS transistor gates and oxide defects or breakdown sites can be analyzed using this technique. Use of this technique in locating submicron oxide defects provides a fast, simple solution to what would be a lengthy series of failure analysis steps if other techniques were used (e.g., optical inspection, cleaning procedures, and reinspect for stationary point defects, then SEM analysis at high magnification).

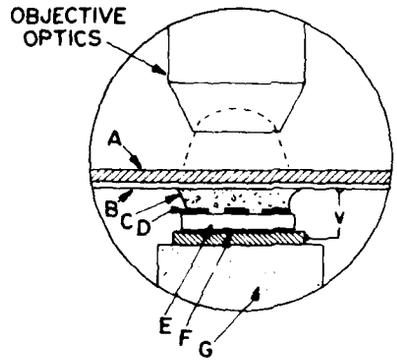
In using this technique, it is necessary to expose the microelectronic device by opening the package (See Chapter III-E for details on package opening). After exposing the microcircuit, the protective glassivation and the circuit metallization must be carefully removed. It has been reported that the prolonged use of

ultrasonic cleaning at this point is highly damaging and has even caused oxide pinholes to be formed. The microcircuit must then be removed from the package header, or the package material must be somehow removed such that the top of the microcircuit is the highest surface.

Figure 2 demonstrates the basic current sensitive cell required to locate oxide defects using liquid crystals. A drop of the liquid crystal, typically MBBA, is placed on the device surface. The top of the cell is formed by placing a glass slide with a thin transparent conductive coating such as SNO_2 or AU in its lower surface over the liquid crystal droplet. It is important that the glass cover plate and the microcircuit be parallel with one another and that the thickness of the liquid crystal between the two be carefully controlled in the range of 10 μm to 25 μm.

A dc voltage is then applied between the microcircuit substrate and the conducting surface of the glass cover. The resistivity of the liquid crystal is high, typically greater than 10^{11} Ω-cm, and very little current through the oxide defect results. This small current through the liquid crystal causes an electrohydrodynamic instability which is visible due to the anisotropic refractive index of the material. Vortices appear to extend laterally around the defect and make pinholes appear much larger than they actually are, thereby providing a magnification of the defect site. Because of the magnification effect, it is possible to detect isolated submicron pinholes which would be extremely difficult to detect optically. The polarity of the applied voltage and the optics employed (bright field vs. dark field) and the cell thickness must be chosen by the analyst to provide the optimum display of defects.

As the applied voltage is increased, the vortex activity will increase, and at about 7-9 volts turbulence will begin and cause vivid displays due to strong dynamic light scattering around partial pinholes (thin oxide areas). Vortex diameter is directly proportional to cell thickness. The current required for creating



A- COVER SLIDE
B- TIN OXIDE COATING
C- MBBA LIQUID CRYSTAL
D- SiO_2 DIELECTRIC LAYER
E- SILICON SUBSTRATE
F- ALUMINUM SLIDE & Ag EPOXY MOUNT
G- ELEVATOR MICROMETER

FIGURE 2. CURRENT SENSITIVE LIQUID CRYSTAL CELL FOR LOCATING OXIDE DEFECTS IN MICROCIRCUITS

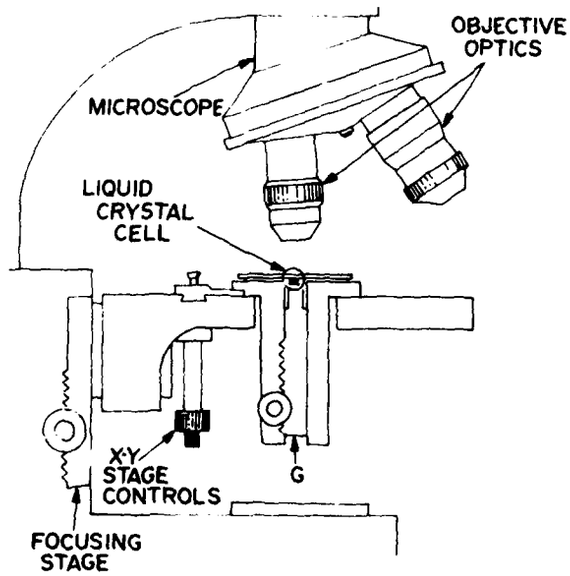


FIGURE 3. FIXTURE FOR PRODUCING CURRENT SENSITIVE LIQUID CRYSTAL DISPLAY ON A MICROCIRCUIT SURFACE

the display is very small, ~ 3 x 10^{-6} A/cm^2, and therefore dielectric layers can be nondestructively tested up to and beyond normal breakdown voltages. If it should be desirable to do further analysis, such as SEM, the liquid crystal is easily removed with acetone.

Figure 3 shows a fixture that may be used to create a liquid crystal cell. Figure 4 demonstrates diagrammatically the current induced formation of the vortex motion in the liquid crystal. Figure 4 shows a photomicrograph of a MOS capacitor structure with a pinhole which is made visible by the liquid crystal display.

This technique will not work with silicon gate devices unless a method is found for removing the polysilicon gate without damaging the gate oxide nor with silicon-on-sapphire devices because of the absence of a substrate connection once the metalization is removed.

4. Optical Voltage Contrast Technique. This technique uses nematic liquid crystals in a field effect display cell which responds to fringing electric fields associated with aluminum and polysilicon conductor lines on integrated circuits. The analyst can observe circuit operation using this technique and can detect logical "stuck at" and electrically open conductor faults.

This technique makes possible nondestructive fault isolation down to the gate or transistor level. It is a complementary optical technique to SEM voltage contrast and permits observation of devices in operation. It can additionally be useful in determining the physical location and implementation of circuit functional blocks in complex LSI circuits. The technique is also useful in locating hot spots which dissipate as little as 20-30 milliwatts.

The following steps are used to prepare a circuit for analysis:

a) Remove the package lid or otherwise do what is necessary to expose the microcircuit inside its package (See Chapter III-E for details on package opening). The electrical connections to the microcircuit should not be disturbed.

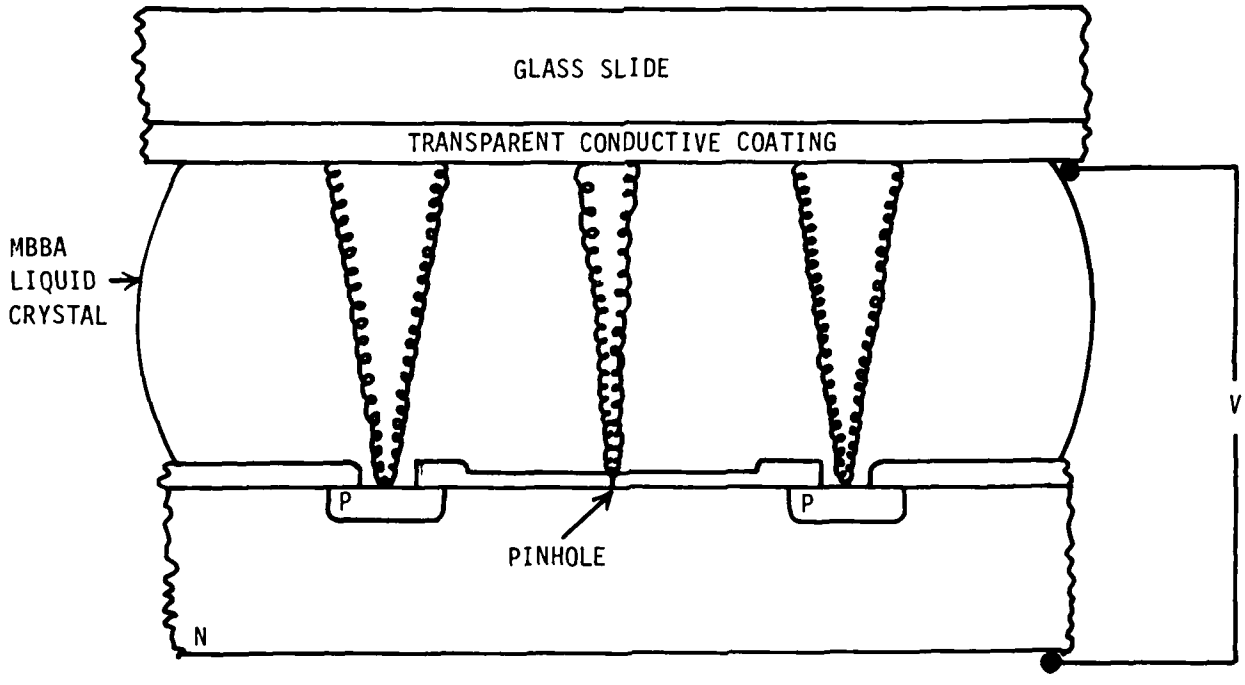
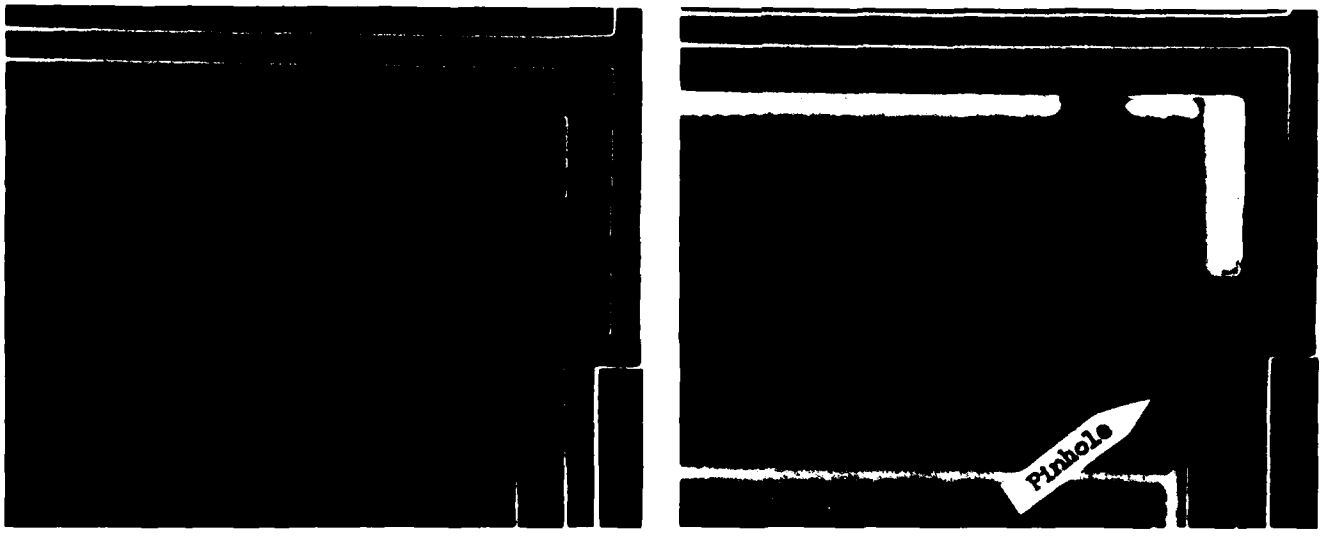


FIGURE 4. CREATION OF VORTEX MOTION IN LIQUID CRYSTAL MATERIAL



a b

FIGURE 5. APPARENT MAGNIFICATION OF OXIDE DEFECT BECAUSE OF VORTEX MOTION IN THE LIQUID CRYSTAL

b) Prepare the surface of a 0.1mm thick microscope cover glass. It is necessary to prepare the surface of this glass so that the liquid crystal molecules will assume an orientation perpendicular to the cover glass surface. It has been reported that the glass can be prepared by sputtering a thin (about 200Å) transparent gold layer onto the glass at a 90° angle from the glass surface (see Reference 10)

c) Prepare the microcircuit surface by applying a solution of 5% by weight lecithin dissolved in trichloroethylene, and spin the sample to obtain a uniform, thin coating. This preparation is necessary to produce the required orientation of liquid crystal molecules perpendicular to the microcircuit surface. The microcircuit protective glassivation is not removed for this technique.

d) Bake the prepared microcircuit for 1 hour at 100°C or allow it to dry overnight at room temperature, being careful not to allow dust to settle on the surface.

e) Scribe or cut a portion of the prepared cover glass to a size that will fit flat on the microcircuit surface but without causing damage to the wire bonds. This can be done by taping the cover glass to a standard laboratory glass slide and dicing with a wafer scriber.

f) Using tweezers, with gold sputtered (shiny) side down, carefully place the prepared glass onto the prepared surface of the microcircuit. Electrical contact to the gold coating is not required.

g) Introduce liquid crystals into the space between the cover glass and microcircuit. This can be done by dipping a small applicator brush (made from three or four acid brush bristles taped to a paper clip) or micropipette in liquid crystal and touching it to the side edge of the coverplate. Repeat this step until enough material has been drawn in to fill the entire cell area. Excess material can be absorbed with the edge of a tissue. Figure 6 shows a typical prepared cell, and Figure 7 demonstrates the cell cross section.

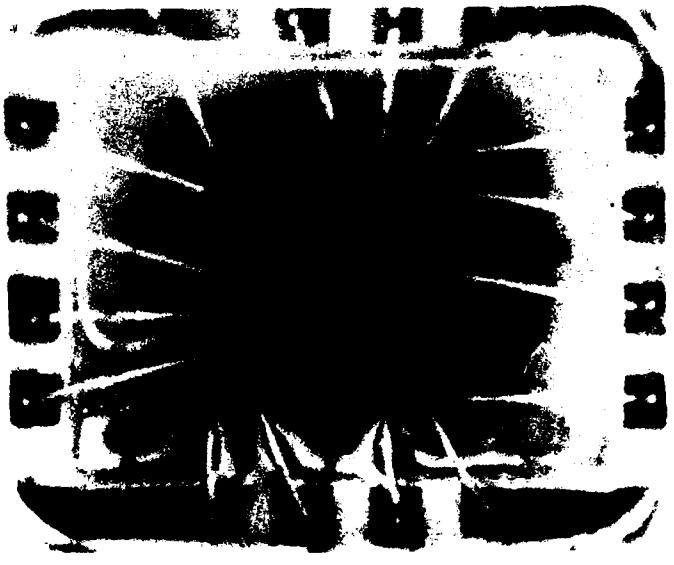


FIGURE 6. MICROCIRCUIT PREPARED WITH OPTICAL VOLTAGE CONTRAST CELL. LECITHIN TREATMENT, LIQUID CRYSTAL, AND GLASS COVER ARE IN PLACE

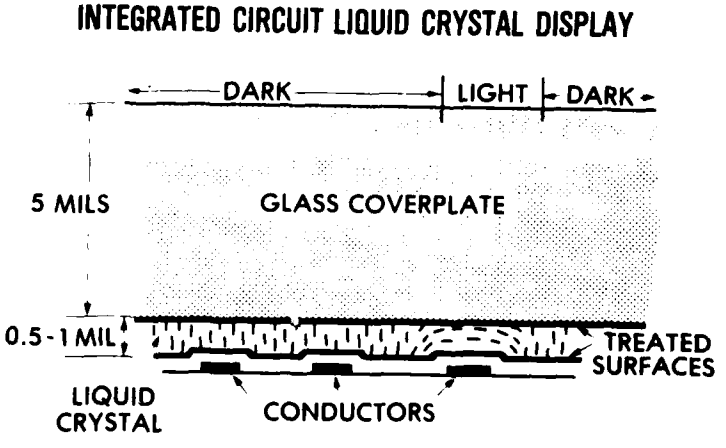


FIGURE 7. CELL CROSS SECTION FOR OPTICAL VOLTAGE CONTRAST LIQUID CRYSTAL TECHNIQUE

The prepared sample is placed in a fixture that allows electrical connection to the package leads and then placed under a standard microscope with vertical illumination. One polarizer is placed in the illuminator light path, and a second polarizer is placed in the microscope viewing path. The second polarizer is oriented 90° to the first. Vertical lighting and properly oriented polarizers are essential for observing the display effect.

The device will show no effect and will appear dark through the crossed polarizers when only dc voltages are present on the conductor metallizations. When the device is operated, the ac fields associated with toggling circuit nodes will cause a localized horizontal reordering in the liquid crystal above those conductor lines. The reordering results in an effective rotation of the direction of polarization of light reflected from those areas of the display. This "rotated" light is no longer stopped by the crossed polarizer in the viewing path, and those areas appear bright. There is an electric field dependent threshold for this effect; no effect for conductor voltages below 3.5 volts RMS, a weak brightening effect between 3.5 and 4.6 volts RMS, and a strong, high contrast effect above 4.6 volts RMS.

The displayed effect remains continuous at operating frequencies greater than over 500 Hz to over 10 MHz. Conductors toggling at 50% duty cycle have the highest intensity display. Figure 8 shows the display pattern of a CMOS microprocessor executing a register test program at a 2 MHz clock rate.

Because of the high frequency clock rate used with the processor shown in Figure 8, the display remains fixed, and no information about what logic levels are present at a given time during the execution of any single instruction in the register test program can be obtained. Rapidly changing logic levels are integrated by the RMS effect with a time constant on the order of 100 ms. When observing this type of display with normal device clocking, the analyst can

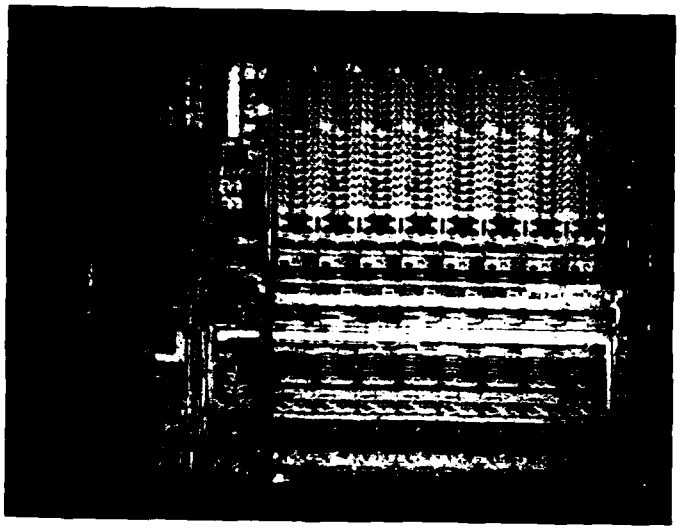


FIGURE 7. DISPLAY OBTAINED FOR A CMOS MICROPROCESSOR OPERATED AT 2 MHz WITH A REGISTER TEST PROGRAM

FIGURE 8 a. DISPLAY OF A FAILED PMOS SHIFT REGISTER WITH OPEN METALLIZATION LINES

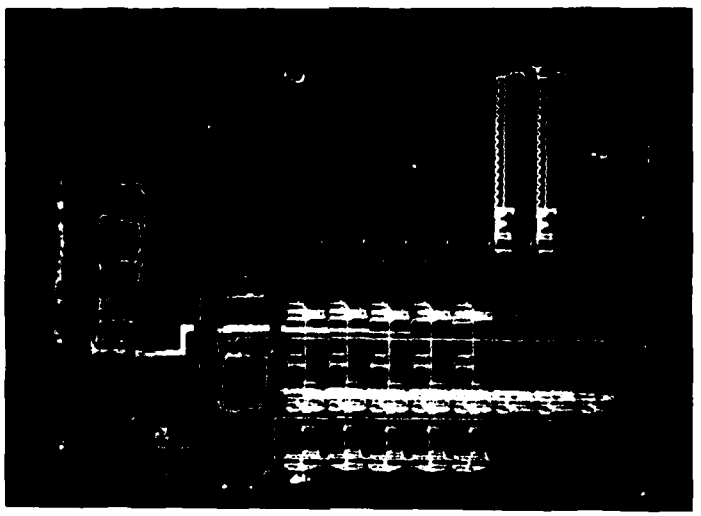


FIGURE 9. DISPLAY OBTAINED FOR A CMOS MICROPROCESSOR WITH TEST PROGRAM FOR THE ACCUMULATOR REGISTER

only detect "stuck at" and electrically open faults, both of which would cause a normally bright conductor to be dark. This interpretation usually requires comparison with the display of a good device. A typical liquid crystal display for microcircuit metallization line continuity verification is shown in Figure 8a. The arrows identify three on chip clock lines with obvious points of electrical discontinuity of an operating 1K MOS static shift register.

It has been reported that displays can be produced which do contain information about what specific logic levels are present at each circuit node for each state in a sequential electrical test. This is done by introducing a delay of about 400 μs in each of two separate states. Such a test procedure will cause the RMS voltage values of conductors to be effectively a function of the logic levels present during the delayed states. Only those conductors which are different for the two delayed states will light. By changing the second delay from one state to the next, the analyst can compare a reference state to many selected states and directly observe the logic level differences between the selected states. The propagation of data and operation of control signal paths in complex circuits can thus be analyzed. Figure 9a shows a CMOS microprocessor tested in this manner. Figure 9 a shows a display of conditions of Figure 10. The result is a comparison of the state of the processor after a load ØØ instruction with the state present after an instruction has been executed which loads hex FF into the accumulator. Figure 10 shows the test program being executed by the device under test. The required pauses in the master clock, Reset and Run Program signals are illustrated in Figure 11.

This technique results in displays which are often easier to interpret at low magnifications than those obtained with SEM techniques because dc voltage levels are not visible. Although there are also no electron charging problems as with the SEM, there are some circuits whose light sensitivity causes much the same reaction as SEM charging. The limited temperature operating range (22^0 - 45.5^0C) is a disadvantage as well. It is a technique which deserves more work.

FIGURE 9a. DISPLAY FOR CONDITIONS OF FIGURE 5. ARROW INDICATES HORIZONTAL ROW OF THE "INSTRUCTION" REGISTER

MICROPROCESSOR TEST PROGRAM

ADDRESS	CONTENTS	MNEMONIC	ACTION
—	—	—	INITIALIZATION
00	F8	LDI	D ← 00
01	00	00	← S0 = 32 CLOCKS
02	F8	LDI	D ← FF
03	FF	FF	← S1 = 48 CLOCKS
04	00	IDLE	STOP

FIGURE 10. TEST PROGRAM FOR OBSERVING LOAD IMMEDIATE CIRCUIT ACTIVITY

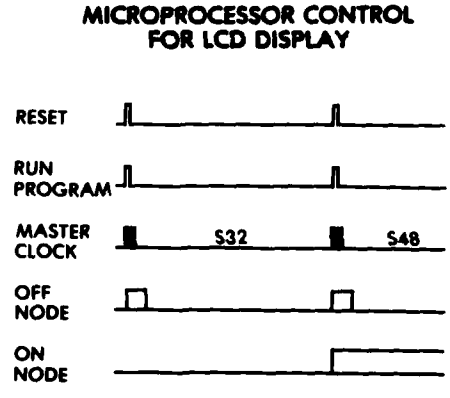


FIGURE 11. DEVICE UNDER TEST CONTROL SIGNALS AND INTERNAL NODE VOLTAGES

5. Low Threshold Voltage Liquid Crystal Display Technique. Preliminary experiments have been completed which were directed at implementing a lower threshold voltage LCD analysis technique. Several nematic liquid crystal materials are available which exhibit threshold voltages on the order of 1.50 volts and wide usable temperature ranges. At this writing these include only positive dielectric anisotropy materials which must be used in "twisted nematic" display cells (Reference 11). These cells require special surface treatments to promote molecular alignment parallel to the cell's bounding surfaces. The lecithin treatments used in the previously described MBBA technique cannot be used.

Two Liquid Crystal mixtures manufactured by Hoffman-LaRoche, Inc., Roche Chemical Division, Nutley NJ 07110, were used for these experiments: RO-TN-103 (V_{TH} = 1.46v, 22° tilt, T_{max} = 81°C) and RO-TN-132 (V_{TH} = 1.29v, 22° tilt, T_{max} = 60°C). The device and coverplate surface treatment used was a 300Å silicon monoxide layer evaporated from a source direction of 85° from normal, i.e., 15° grazing angle (Reference 10).

Several CMOS 1802 microprocessors and coverplates were surface treated and assembled with their respective directions of surface treatment deposit oriented at 90°, as required to produce a "twisted nematic" cell. These LC cells were tested using a microprocessor V_{DD} voltage level of +5v with usable results, as shown by Figures 11a and b. Improved contrast was obtained using parallel polarizers which resulted in a display with bright background and dark active device areas.

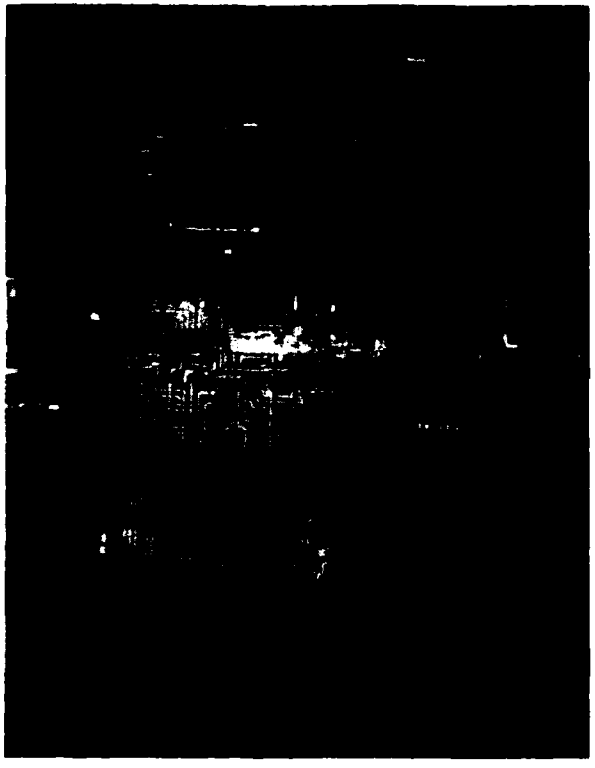
Additional experiments were conducted with no cell element surface treatments and other surface treatments such as rubbing with cotton, but none gave acceptable results. Although these initial experiments proved the feasibility of this low voltage LCD technique, the technique is quite difficult to implement because of the need to evaporate SiO on both the microcircuit under test and the cell coverplate surfaces.

TWISTED NEMATIC LIQUID CRYSTAL DISPLAY CELL

MATERIAL - RO-TN-103

DEVICE - CMOS MICROPROCESSOR

ILLUMINATION - BRIGHTFIELD (INCIDENT)



NO BIAS

5V/OPERATION

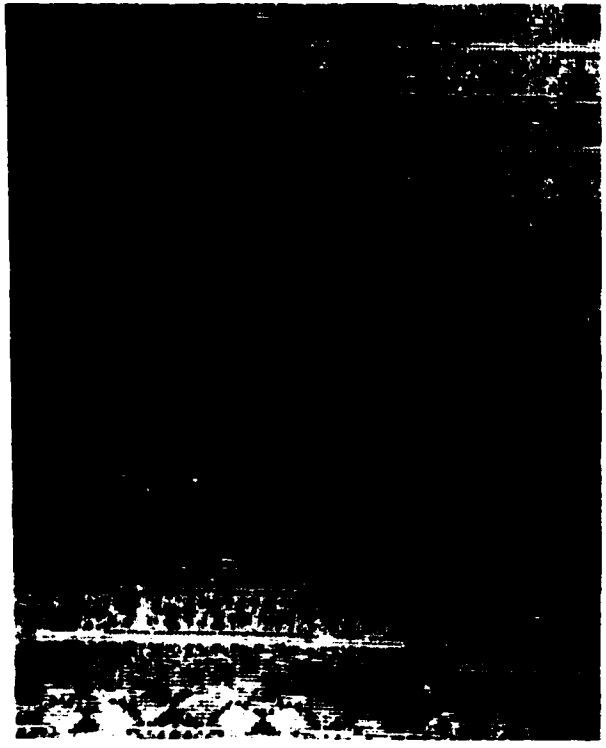
FIGURE 11a. LOW THRESHOLD VOLTAGE LIQUID CRYSTAL DISPLAY

TWISTED NEMATIC LIQUID CRYSTAL DISPLAY CELL

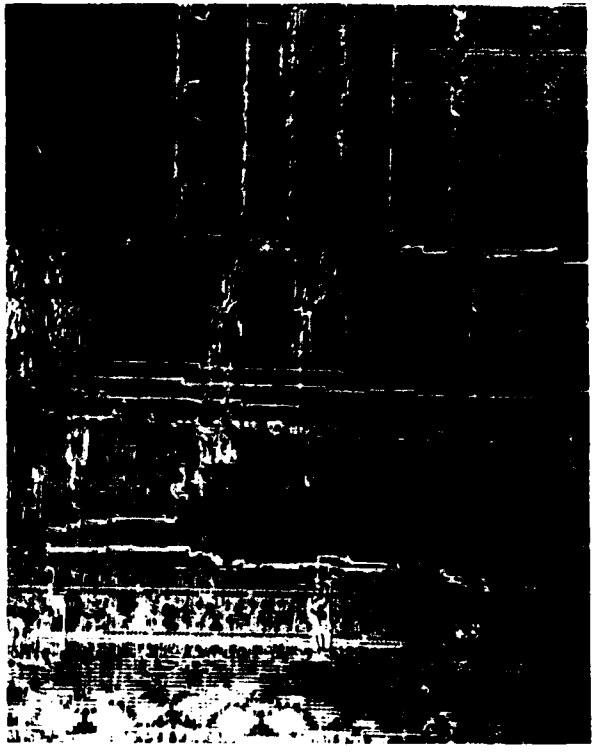
MATERIAL - RO-TN-103

DEVICE - CMOS MICROPROCESSOR

ILLUMINATION - DARKFIELD (OBLIQUE)



NO BIAS



5V/OPERATION

FIGURE 11b. LOW THRESHOLD VOLTAGE LIQUID CRYSTAL DISPLAY

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EQUIPMENT

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Mixture made to order for specific temperature range — $ 30/122cc

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Eastman Kodak Company, Eastman Organic Chemicals,
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MBBA: N-(p-Methoxybenzilidene)-p-butylaniline — $100/20g

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St. Paul, MN 55101 (616)733-0128
Ashley-Butter, Inc., 208 U.S. Highway 206S,
Somerville, NJ 08876 (201)359-5911

Lecithin

Vegetable, purified — $11/250g

Eastman Kodak Company, Eastman Organic Chemicals,
Rochester, N.Y. 14650

(May be purchased through Fisher Scientific Co.,
Pittsburgh, PA 15238 (412)781-3400
Scientific Products, Sunnyvale, CA 94086 (415)743-3100)

Low Threshold Voltage Liquid Crystal Materials

RO-TN-103 (V_{TH} = 1.46v, 22° tilt, T_{max} = 81°C) — $20/g
RO-TN-132 (V_{TH} = 1.29v, 22° tilt, T_{max} = 60°C) — $20/g

Hoffman-LaRoche, Inc., Roche Chemical Division,
Nutley, NJ 07110 (201)235-5000

I.

SURFACE EFFECTS

I. Surface Effects.

1. Introduction. Surface effects in semiconductor structures and packages, such as surface inversion ionic contamination, charge trapping, etc., are responsible for many microelectronic failures. Failures due to surface effects are often temporary or intermittent in nature. For instance, mobile ionic contamination can be moved through silicon dioxide by thermal energy and in the presence of an electric field. It is, therefore, sometimes possible to change the electrical characteristics of a microelectronic device by reversing the applied electric field and/or by baking at elevated temperatures causing ionic charges to move.

Another phenomenon concerns the activation energy associated with contaminants. That is, the effects of many contaminants in causing a failure are seen only after sufficient energy has been applied to the unit. Activation energy is generally reached by a time/temperature of operation function.

Most of the work done in investigating surface effect instabilities has been concerned with MOS type structures. However, bipolar structures are subject to the same phenomenon. Beta degradation, shifts in breakdown voltage, and leakage current drift are sometimes surface related effects in bipolar structures.

The presence of water and ionic contamination will invariably lead to current leakage problems. Generally, the role of these contaminants in microelectronic failure is difficult to quantify. The presence of the contaminants usually requires the use of expensive equipment and techniques such as the microbeam analysis techniques (See Chapter III P). Even then, the results are often questionable at best. For example, gas analysis techniques to quantify percentage of water in a particular atmosphere require the use of expensive equipment.

In this chapter, surface effects are presented, first from a theoretical viewpoint and following from a more practical viewpoint.

2. Theory of the Silicon - Silicon Dioxide Structure.

Most microelectronic devices in use today are silicon based structures. It is a well-demonstrated fact that the most successful method for passivating the surface in silicon device technology is thermally formed silicon dioxide (SiO_2).

Thermal SiO_2 layers are usually formed at high temperatures, 800° - 1200°C, in either a water vapor or an oxygen atmosphere. The growth of the oxide layer is a function of several variables, some of which are:

- Crystal orientation of silicon surface
- Condition of silicon surface
- Temperature
- Type and concentration of silicon doping
- Atmosphere
- Thickness of oxide present

Thermal oxidation occurs when oxygen enters the oxide layer present on the silicon surface, diffuses through that layer, and combines with silicon atoms at the silicon surface. It has been suggested that the reaction of forming SiO_2 is probably related to the energy required to break silicon-to-silicon atomic bonds.

As a result of the way in which SiO_2 is formed, there is always a thin layer at the silicon-SiO_2 interface where there are broken Si-Si bonds that are not attached atomically to any other atom. This condition is referred to as "dangling bonds" and adds to one type of charge that affects silicon device electrical performance. After thermal SiO_2 formation, it is common to remove the oxidizing atmosphere, while still at high temperature, and introduce an inert atmosphere such as nitrogen or helium. This is called the anneal step. Annealing allows bonds between Si-O_2 and Si-Si to become more complete, thus aiding in removing one source of fixed electrical charge. This is discussed more fully below.

a) Charges in Thermal Oxide. It is generally accepted that there are four (4) types of electrical charges that can be present in thermal SiO_2. These charge types are: fixed surface-state charge, Q_{SS}; mobile ionic impurity, Q_M; fast surface-states, N_{FS}; and oxide traps ionized by radiation, N_{IR}.

All these types of electrical charges affect the electrical performance at the surface of semiconductor devices. The effects usually appear in the form of threshold voltage shifts in the case of MOS structures and as leakage paths in all semiconductor structures.

The electrical effects are caused by the fact that any charges residing in the oxide will induce a charge of opposite polarity in the silicon below. The amount of induced charge in the silicon is inversely proportionaly to the distance of the oxide

charge from the silicon surface. Therefore, a charge located near the Si-SO_2 interface will reflect the total amount of its charge in the silicon. If this same charge were, however, located at the top surface of the oxide at maximum distance from the interface, there would be very little effect in the semiconductor.

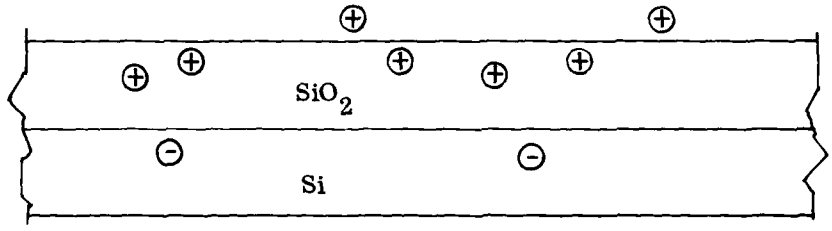
The effect of charge location is diagramatically represented in Figure 1.

Following is a more in-depth discussion of the four types of oxide charges described above.

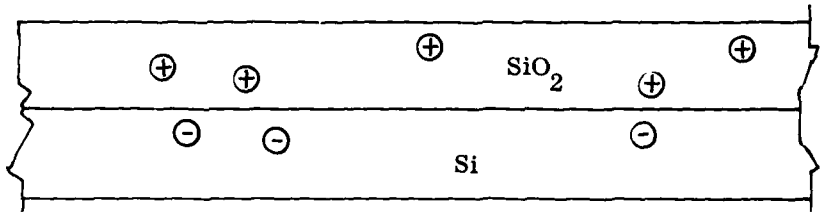
1. Fixed Surface-State Charge, Q_{SS}. This charge is a permanently fixed, positive charge. The existence of this charge has been well-established, particularly through studies made during the emergence of MOS semiconductor technology. It is thought to be related to the structure of oxide close to the area of interface between the SiO_2 and the silicon. This fixed charged cannot be discharged by varying the surface potential of the silicon. The final value of Q_{SS} during the fabrication cycle is dependent on both silicon surface orientation and upon the oxidation/anneal cycle used.

It is now in general agreement that Q_{SS} results from a nonstoichiometric silicon-oxygen structure in the interface region of Si-SiO_2. It can be looked on as either a result of excess silicon or of lack of oxygen. Whichever the case, a positive charge results.

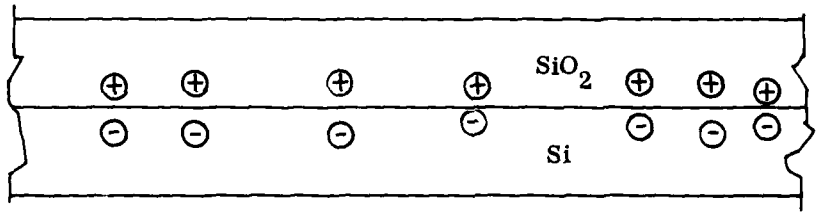
A phenomenon exists whereby the density of Q_{SS} charge can be increased. For instance, if a negative bias is applied to the gate of an MOS structure in the temperature range of 100° - $400^{\circ}C$, the Q_{SS} charge level will increase. The amount of Q_{SS} increase is proportional to initial values of Q_{SS} and on the negative applied field. Assuming that Q_{SS} is due to partially ionized silicon atoms such as Si^{+}, a possible explanation for this phenomenon exists. The application of a negative field might then break another already weakened silicon bond to produce Si^{++} or an additional positive charge.



a. LITTLE OR NO ELECTRICAL EFFECT FROM CHARGES IN OXIDE.



b. MORE PRONOUNCED ELECTRICAL EFFECT FROM CHARGES IN OXIDE.



c. SEVERE ELECTRICAL EFFECT FROM CHARGES IN OXIDE.

FIGURE 1. DIAGRAMMATIC REPRESENTATION OF EFFECTS OF CHARGES TRAPPED IN SILICON DIOXODE

2. Mobile Ionic Charges, Q_M. This type of charge was the first to be examined extensively. This is true because studies of other charge types could only be begun after mobile charges were minimized. Experimental evidence has shown that alkali ions (Na^+, K^+, Li^+) are the major source of ionic-induced instability. Mobile protons and immobile negative ions can also contribute to instability.

The positive alkali ions will drift in oxide under bias conditions when the temperature is greater than 100°C. There are, however, some cases where drift under room temperature conditions has been noted. Hydrogen ions (H^+ or H_3O^+) will drift under room temperature conditions, but negative ions will not drift at temperatures lower than 300°C. It is possible during the device fabrication stage to getter these ions at high temperatures above 900°C using phosphosilicate glass.

Ionic contamination is generally introduced during the semiconductor fabrication stage but can result from contamination of packaged microelectronic devices.

3. Fast Surface-State Charges, N_{FS}. Fast states were studied during the time when germanium was the technology of the day. Regardless of the length of time they have been studied, they are understood the least. Fast states are in direct electrical communication with the silicon, and charge transfer is effected rapidly as surface potential changes.

These fast states appear both at discrete energy levels in the forbidden band and as a continuous distribution throughout the forbidden band. The density of N_{FS} is initially proportional to Q_{SS} and seems to have the same silicon orientation dependence.

The presence of N_{FS} in semiconductor devices affects many device electrical characteristics. MOS device threshold and transconductance, and bipolar junction noise, leakage, low current beta, and breakdown characteristics are all affected.

There is general agreement that these states are a result of either defects in the interface region between silicon and the oxide or to impurities in this region. They may be due quite possibly to both. Whatever causes these states, holes and electrons are trapped at particular surface potential or energy levels.

The application of negative field conditions and ionizing radiation both increase the formation of N_{FS}. The use of high temperature annealing in an inert atmosphere also tends to increase the amount of fast states. This fact seems to support the surface defect explanation for fast state formation.

4. Radiation Induced Charge, N_{IR}. Gamma radiation, X-rays, high energy electrons, neutrons, etc., are all examples of radiation that causes a positive charge to be introduced in thermal SiO_2, usually near the interface of SiO_2-Si. Radiation will also increase the level of fast states, N_{FS}. The level of charge N_{IR} is a function of dose level, energy level, and the electrical field across an oxide during the radiation. It is possible to anneal out both N_{IR} and N_{FS} charges caused by radiation through the use of a low temperature, typically 300°C, bake in an inert atmosphere.

Depending on the dose level and rate, ionizing radiation can produce a sufficient positive space charge to shift the threshold voltage of an MOS device in the range of tens to more than one hundred volts.

Two possible explanations have been given regarding the mechanism by which radiation causes the positively charged N_{IR}. One of these models is based on the SiO_2 structure. It postulates that electron-hole pairs are produced as a result of the radiation. The resulting holes are trapped by broken silicon-oxygen bonds, and the electrons migrate away. The traps responsible for trapping the holes may or may not have been created by the radiation, but the result is the same. The second of the proposed explanations concerns the activation of such impurity ions as sodium. It is proposed that this ionized impurity then acts as a positive charge or acts indirectly to trap holes created by the radiation.

A number of techniques have been used in trying to solve the radiation problem. Some of these techniques have been:

- Modifying the SiO_2 structure such that strain on the silicon-oxygen bond is reduced to its lowest possible value
- Adding impurity species to compensate for trapping centers, or possibly to complex impurity ions
- To form SiO_2 of extreme purity so as to eliminate impurity trapping centers

Various proprietary techniques exist for radiation hardening oxide layers, and products are available commercially.

3. The Capacitance-Voltage (C-V) Measurement. The most useful method of studying the $Si-SiO_2$ system is the C-V measurement made on a metal-oxide-semiconductor structure or the polysilicon-oxide-semiconductor structure. A bias voltage applied between the gate and the semiconductor will create an electric field at the surface of the semiconductor. The small signal ac capacitance can then be measured as a function of bias, frequency, and bias sweep speed.

Figure 2 demonstrates the ideal MOS system. If a positive bias is applied between gate and semiconductor, the semiconductor energy bands will bend downward. This energy band bending will cause electrons in the semiconductor to be attracted to the surface. This condition is called ACCUMULATION, and the capacitance measured, Co, will be determined solely by the thickness of the oxide.

If a negative bias is applied, electrons in the semiconductor will be repelled from the surface. This will cause a DEPLETION layer to be formed in the semiconductor bulk material. A fixed volume charge density equal to the semiconductor doping N_D will exist, but no free carriers will be present. DEPLETION layer has the effect of widening the distance between capacitor plates, and thus lowering the total capacitance.

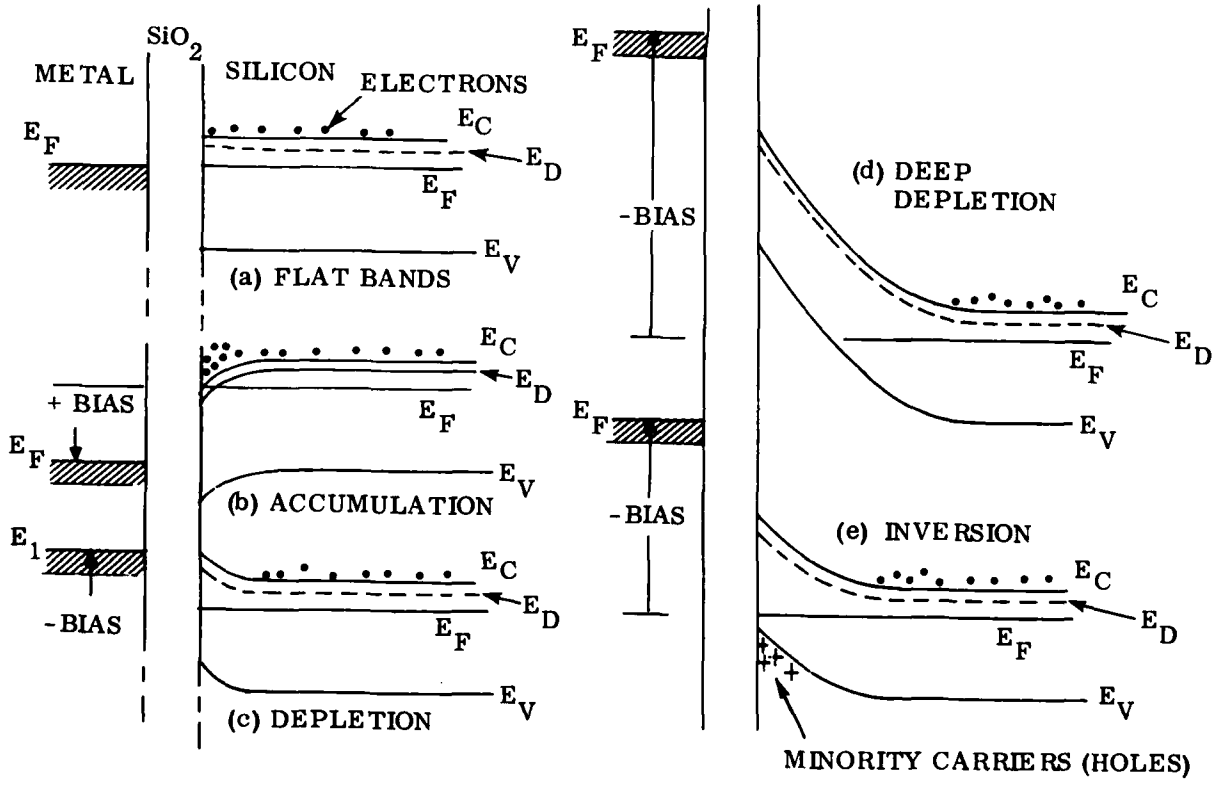


FIGURE 2. THE IDEAL MOS ENERGY BAND STRUCTURE UNDER VARIOUS BIAS CONDITIONS. BAND BENDING AND REDISTRIBUTION OF FREE CHARGE IN THE N-TYPE SEMICONDUCTOR ARE SHOWN

Further increasing negative bias widens the space charge layer until an INVERSION layer made of minority carriers (holes, in this example) is formed at the surface. Still further increased negative bias will increase the number of holes present in the inversion layer. The width of the space charge layer will not be affected by increasing negative bias, provided the bias is changed slowly.

Upon application of a very large negative bias, the space charge region will become very wide, producing the condition of DEEP DEPLETION. The capacitance will approach zero in this condition. If the bias is maintained, minority carriers will be generated and the semiconductor surface potential will come to equilibrium with the bulk. The space charge width will return to its equilibrium width, and an INVERSION layer will be formed.

The impurity concentration of the semiconductor material will determine the maximum width of the space charge layer. The capacitance minimum seen at inversion can be used to measure the doping of the semiconductor near the surface. If a small ac signal of sufficiently low frequency is applied at this point, the inversion layer concentration will follow the ac bias variation and will supply charge as readily as the accumulation layer. Under these conditions, the capacitance will rise toward the maximum capacitance Co as the surface is inverted. Figure 3 shows the resultant C-V curve obtained with the structure as diagramed in Figure 2.

Thus far an ideal structure has been assumed. However, because of the work function difference between the metal gate material and the semiconductor material, ϕ_{MS}, and because of the presence of oxide charges described previously, the actual C-V curve is shifted from the ideal case. Figure 4 demonstrates how the actual C-V curve is in relation to the ideal case.

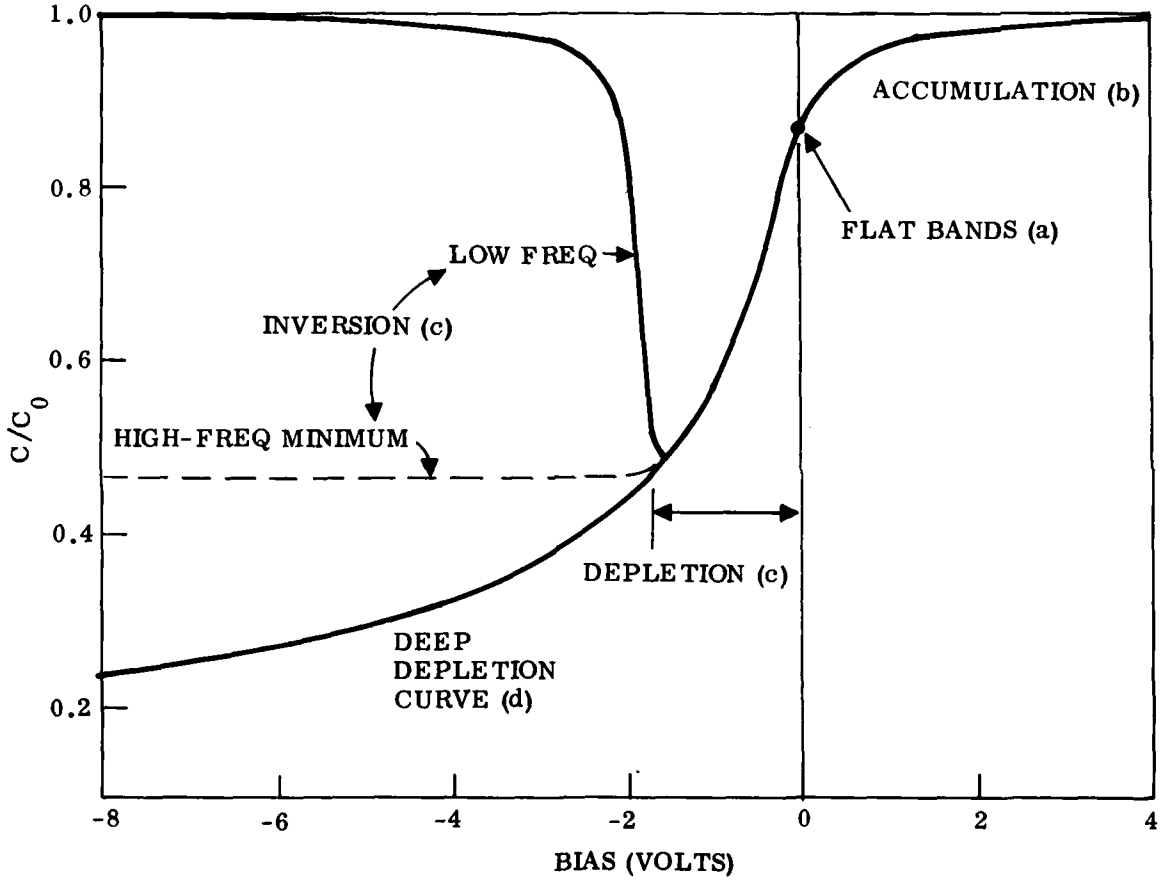


FIGURE 3. THEORETICAL C-V CURVE OF IDEAL MOS STRUCTURE SHOWN IN FIGURE 2

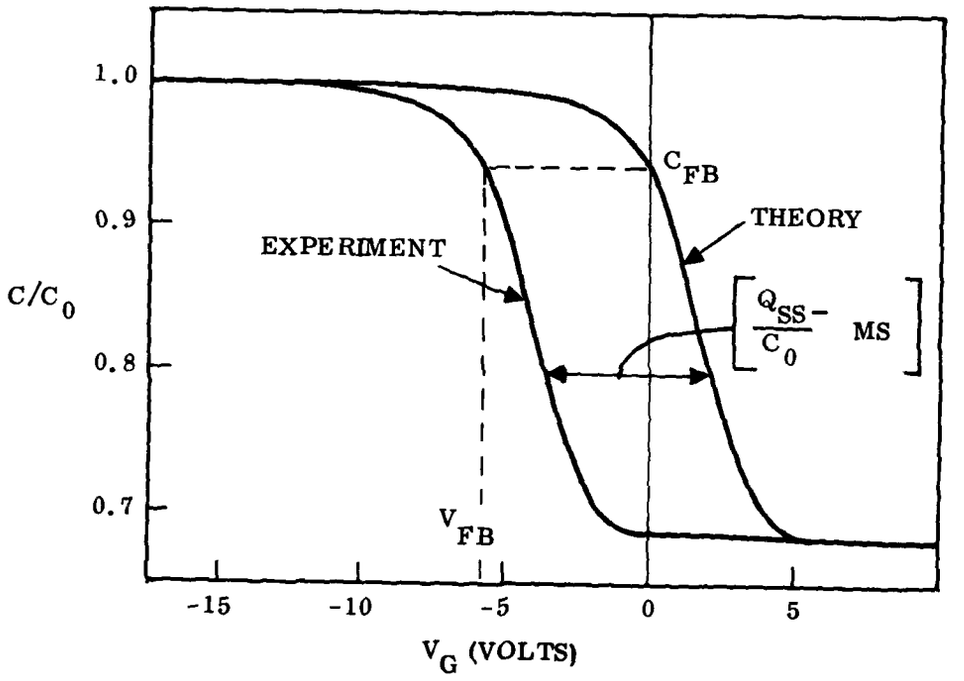


FIGURE 4. SHIFT OF ACTUAL C-V CURVE FROM THEORETICAL

a) Making the C-V Measurement. Equipment is commercially available for making C-V measurements. The apparatus applies an alternating voltage, typically at 1 MHz, superimposed on the dc bias voltage. The C-V trace is made by applying a positive bias, and by then sweeping the bias through zero volts and on into negative bias. The semiconductor surface during this measurement goes through the sequence of ACCUMULATION, INVERSION, and DEPLETION. The resulting change in capacitance with applied bias is recorded on an X-Y plotter.

The standard technique used in making C-V measurements begins with an "as-is" C-V plot as described above. The device is then stressed while under positive bias. The stage of the C-V apparatus is typically equipped with a heating element and thermocouple for controlling the temperature. The device temperature is raised, usually to 300°C, for 5-15 minutes while bias, usually 5-15 volts, is applied between gate and substrate.

The device is cooled down rapidly after the set time interval, with the bias remaining on the gate. A second C-V plot is made after the device has reached room temperature. By comparing the original curve with this one, the presence of mobile ionic contamination and fast surface-states will be revealed by shifts in the curve. Figure 5 shows possible before and after C-V curves.

A further C-V curve can be made after a negative stress bias with temperature cycle. The same procedure as outlined above is repeated, except that negative voltage is applied to the gate throughout the stress process. If mobile ions are present, the curve should be shifted back toward the original position.

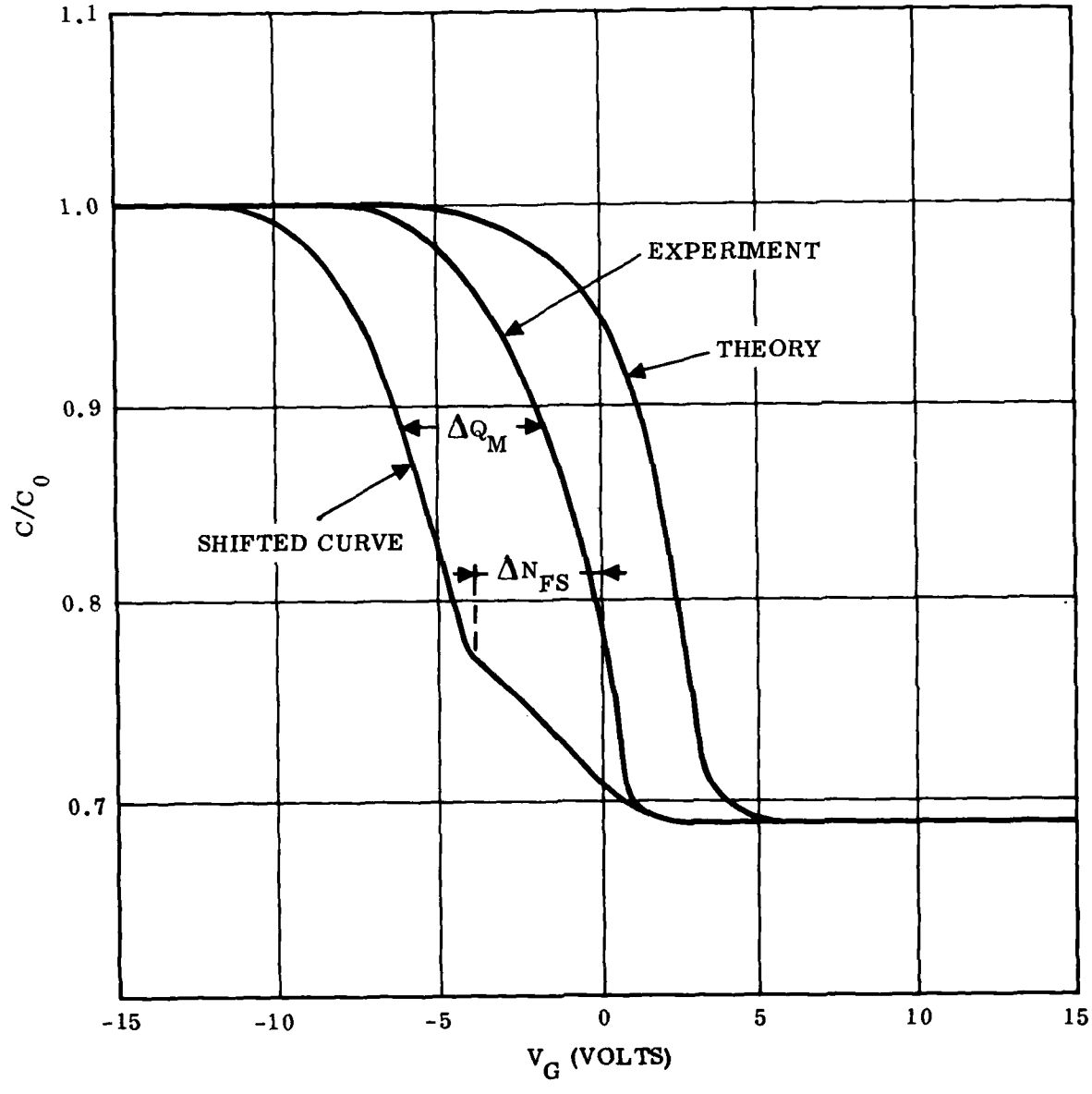


FIGURE 5. C-V CURVE SHIFT AFTER NEGATIVE VOLTAGE TEMPERATURE STRESS BIAS

4. Failure Mechanisms Due to Instabilities.

Performing failure analysis involving identification of inversion layers in MOS and bipolar circuits is usually extremely difficult. This is true because of the increasing complexity of microelectronic components and the complicated electrical potential distributions that exist during operation. It generally is necessary to isolate specific devices in a complex microcircuit before C-V analysis can be employed.

Electrical measurements to quantify inversion layers include measurement of leakage currents and capacity as a function of bias and frequency. The scanning electron microscope is very useful in identifying inversion layers and resultant leakage paths.

The failure analyst should always bear in mind when investigating suspected surface-related problems that leakage paths might easily be due to ionic contamination between package leads. For instance, ionic contamination on the surface of a transistor header might result in electrode leakage that is completely independent of the active device.

a) Instability Due to Surface Charge on the Silicon Dioxide.

Ionic contamination that comes into contact with the SiO_2 surface will, initially, remain unmoved on the surface. However, when a nearby PN junction is reverse biased the resulting fringing electric field will cause mobile charges to move on the SiO_2 surface.

These mobile charges will induce an area of charge in the semiconductor and cause leakage across a PN junction by causing excess electrons to gather near the top of the P region and excess holes to gather in the N region.

This type of instability is generally removed by a high temperature bake in the range of 170°C to 180°C for 10 minutes.

b) Conduction on Oxide Surfaces/Lateral Charge Spreading. This type of instability results in the formation of a parasitic MOS device. This phenonenon occurs when the SiO_2 surface becomes conductive as a result of injected charge and subsequent lateral charge spreading.

Higher levels of humidity and contamination on the SiO_2 surface aggravate the mechanism. This instability is generally removed with a high temperature bake in the range of 170°C to 200°C for several hours and re-established by a subsequent bake under bias.

This instability has been observed at insulator - insulator interfaces such as those formed by Si_3N_4, PSG, SiO_2, etc.

c) Instabilities Caused by Charges Within the Silicon Dioxide.

Four types of charges that can exist inside an oxide layer have been identified:

1) Mobile ionic charges (Na^+, Li^+, etc.)
2) Fixed positive charge
3) Interface (or fast) states
4) Radiation induced charges

Silicon dioxide is particularly susceptible to mobile charge contamination. These charges move under the influence of an electrical field and, when sufficient in density, can cause inversion of the silicon surface with resultant leakage.

A high temperature bake in the range of 170°C to 200°C for a few hours will remove the instability, and high temperature operating will cause this type of instability to reappear.

d) Instabilities in Double Layer Insulator Structures. This instability has been reported to be set up when a voltage is applied across the double layer structure. Because the electric fields are different in these layers, a charge will accumulate between the dielectric layers, resulting in charge conducting inversion layers.

The accumulated layer can be discharged by a high temperature bake in the range of 170°C to 200°C for several hours.

e) Instabilities Induced by External Stresses Avalanched Emitter-Base Junction. During the operating life of semiconductor devices, they often encounter electrical and thermal stresses that may cause damage ranging from degraded performance to complete nonfunctionality. NPN transistors have been reported to be susceptible to emitter-base junction degradation when reverse biased into the avalanche region.

The instability may or may not be reversible with a high temperature bake. The total amount of energy during the avalanche will determine how extensive and permanent the damage will be. For instance, high energy pulses can cause small highly localized hot spots that could melt an area of the Si - SiO_2 interface which would subsequently resolidify into an area of recombination/generation sites. These sites would then be areas of high leakage.

f) Instabilities Due to Parasitics. Parasitic devices may be responsible for anything from degraded parametric performance to complete failure. For example, parasitic SCR devices have been known to latch up, causing failure in some analog operational amplifiers.

Probably the most frequently encountered parasitic in bipolar circuits occurs when two adjacent areas, such as diffused resistors, are at different potentials in an N region, and metallization runs over the N region. If that metallization becomes negatively biased with respect to one of the P diffused regions, the N region could become inverted so as to form a channel through which current can flow between the P regions.

A common parasitic device found in MOS circuits is formed when the oxide over an N region becomes negative with respect to one of two adjacent P areas as a result of lateral charge spreading or ionic contamination.

5. Typical Failure Analysis Procedure for Identifying Instabilities. The following procedure may be useful in identifying probable causes of failure due to instability:

a) High temperature bake (170°C to 200°C). A typical bake time from 8 to 16 hours has been found sufficient.

b) Retest the unit. At this point, one of two results must be obtained:

1) The unit did not recover. If this is the case, the damage is probably a permanent, nonreversible damage, such as a condition of local diffusion spikes or over alloyed metallization.

2) The unit recovered. In this case, it can be concluded that the unit has reversible leakage but the probable cause cannot yet be identified. The failure analyst should proceed to the next step.

c) If at all possible, burn-in the device in a manner equivalent to the electrical configuration under which failure occurred. The temperature should be elevated, and one of two possible cases will to be used for burn-in.

1) No electrical bias is used. In this case, the burn-in ambient temperature should be 150°C.

2) Electrical bias is used. In this case, the junction should be operated at 150°C and the power dissipation should be adjusted to conform to this. One way in which to take this into account is to calculate:

$$T_{junction} = T_{ambient} + \text{Power} \times \text{Thermal Resistance}$$

The most commonly used conditions for achieving the burn-in are:

125°C for 168 hours.

d) Retest the unit. One of two results must be noted:

1) The instability cannot be reproduced. In this case, a low power avalanching of emitter-base junction or a surface charge inversion due to contamination by volatiles would be suspected.

When volatiles are suspected and the unit is hermetic, a gas analysis should be performed. Should this analysis show a high content of moisture or some other volatile, a surface charge on the surface of a microelectronic die would seem probable.

In the case of a plastic package, electrostatic damage and moisture contamination cannot be distinguished between because they will both disappear with high temperature bake.

2) The instability was reproduced. In this case, a die probe - layer removal - biased bake (drying) - probe procedure is called for (See Chapters III-A, III-E and III-M for more information on die isolation and probing, package opening, and chemical procedures, respectively).

6. Die Probe - Layer Removal - Biased Bake - Probe Procedure.

A microelectron unit suspected of having a contaminant in one or more layer (SiO_2, SiN_3, etc.) might use this procedure to locate and perhaps identify the contaminant.

The technique consists of sequentially removing the layers on a microcircuit and probing to discover whether the contaminant has been removed or not. The failure analyst must recognize the fact that degraded and leaky performance and light sensitivity will be shown by junctions.

Disappearance of abnormal curve tracer characteristics after a particular layer was removed will indicate that the source of the instability was either in that layer or located at the interface between that layer and the next. Removal of one half or one third of the layer, remeasuring, and removal of the remainder will help in determining where the contaminant was located.

Table I shows details on layer removal procedures (see also Chapter III-M) and Table II shows typical initial test results, procedures for subsequent layer removal, and typical conclusions.

TABLE I

LAYER REMOVAL PROCEDURES

LAYER TO BE REMOVED	MATERIAL	CHEMICAL PROCEDURE
Plastic	Epoxy	1) Drill hole over die until wires are reached. 2) Remove remaining plastic by exposing to red fuming nitric for 3-5 minutes at 125°C. 3) Wash in acetone in ultrasonic cleaner.
Glassivation	SiO_2	1 minute in HF to remove 5000A
		Plasma etching
	Si_3N_4	Phosphoric acid
		Plasma etch
Metallization	Aluminum	Solution B Nitric acid 5% Phosphoric acid 80% Acetic acid 5% 1 minute at 110°C-170°C (will not affect thermal oxide)
Undermetal Oxide	Si_3N_4	Plasma etch
		Phosphoric acid
	Thermal SiO_2	4:1 HF 2.5 minutes removes about 5000Å
		Plasma etch

TABLE II

FAILURE ANALYSIS BY LAYER REMOVAL METHOD

FAILED DEVICE ELECTRICAL MEASUREMENTS (PARAMETERS; LEAKAGES; BREAKDOWNS; I-V CHARACTERISTICS; THRESHOLDS)				CURVE TRACE - I-V CHARACTERISTICS AFTER DECAPSULATION FORWARD AND REVERSE BREAKDOWNS; hFE; THRESHOLD TEST. (SOMETIMES PINPOINTING OF AREA WITH ABNORMALITY OF PROBE IS DONE AFTER GLASSIVATION REMOVAL BECAUSE OF DIFFICULTY OF PROBING)						PROBABLE FAILURE CAUSE
INITIAL	AFTER HIGH TEMP BAKE	AFTER HIGH TEMP REVERSE BIAS OF LIFE	GAS ANALYSIS OF CAVITY PACKAGES	PINPOINT BY PROBE JUNCTION(S) WITH ABNORMAL I-V CHARACTERISTICS	I-V AFTER TOP HALF OF GLASSIVATION IS REMOVED	I-V AFTER COMPLETE GLASSIVATION REMOVAL	I-V AFTER METAL REMOVAL	I-V AFTER UNDER METAL PASSIVATION REMOVAL	I-V AFTER HIGH TEMP BAKE	
High leakages Low breakdowns High Offsets	Same or further degradation	Same or further degradation	Normal	Abnormal	---	---	---	---	---	Permanent damage due to excess forward current avalanched junction (ESD) (Microsection for identification)
High leakages* Low breakdowns High offsets	Recover	Will not recur	High content of volatiles i.e., H_2O	---	---	---	---	---	---	Package ambient contamination causes surface charge instability or lateral charge spreading; if no volatiles - avalanched junction due to transient
High leakages Low breakdowns High offsets	Recover	Recur	High content of volatiles i.e., H_2O	Abnormal	Recover	---	---	---	---	Ions in the glassivation bulk surface conduction of oxide lateral charge spreading at interface between glassivation and passivation.
High leakages Low breakdowns High offsets	Recover	Recur	Normal	Abnormal	Abnormal		Recover	---	---	Contamination due to metallization
Device tests good at room	Remained Good	Instability identified by monitoring at high temp	Normal	Instability shows unstable I-V at high temp; threshold test shows large shift	---	---	---	---	---	Parasitic MOS device action Dual dielectric instability
High leakages Low breakdowns High offsets	Recover	Recur	Normal	Abnormal	Abnormal	---	Abnormal	Recover	---	Thermal oxide contamination
High leakages Low breakdowns High offsets	Recover	Recur	Normal	Abnormal	Abnormal	---	Abnormal	Abnormal	Recover	Silicon bulk contamination Probably top layer

*May be bad one time and good when remeasured.

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EQUIPMENT

Capacitance-Voltage Apparatus

1. Model 868-IT C-V plotter, capacitance meter, heat controller, heated chuck, and probe.

   MSI Electronics Inc., Woodside, N.Y. $8300

J.

SURFACE TOPOGRAPHY MEASUREMENT TECHNIQUES

J. Surface Topography Measurement Techniques.

1. Introduction. Metallization line widths, spacing between adjacent patterns, thickness of thin film patterns, etc., are all physical dimensions often measured in failure analysis work. A broad range exists in both the complexity and in the cost of equipment available to make such measurements. The following sections describe some of the measurement techniques available.

2. Stylus Measurement Instruments. This type of measurement equipment is designed to determine vertical height differences between two or more surface layers. For example, the thickness of metallization on a microelectronic device can be determined by measuring the step height at the edge of the metallization. The instrument can be used with the aid of a strip chart recorder to record surface profiles as well.

This instrument operates by measuring and recording the vertical deflections of a stylus. The stylus tip is equipped with a diamond head and is drawn across the surface of the sample being measured. The deflections of the stylus are amplified and recorded on the strip chart recorder.

These instruments are typically capable of measuring elevation differences from less than 25 Å to 1,000,000 Å (100μm). The diamond stylus that comes in contact with the sample surface is on the order of 13 μm in radius and has a tracking force of approximately 50 milligrams. Even though this is a low pressure, measurement with this type of instrument should be considered as potentially destructive.

The sample being measured is placed on a stage beneath the sensing head containing the diamond tipped stylus. The sensing head is equipped with a microscope and light source so that the stylus can be lowered to the proper place for measurement. There is generally

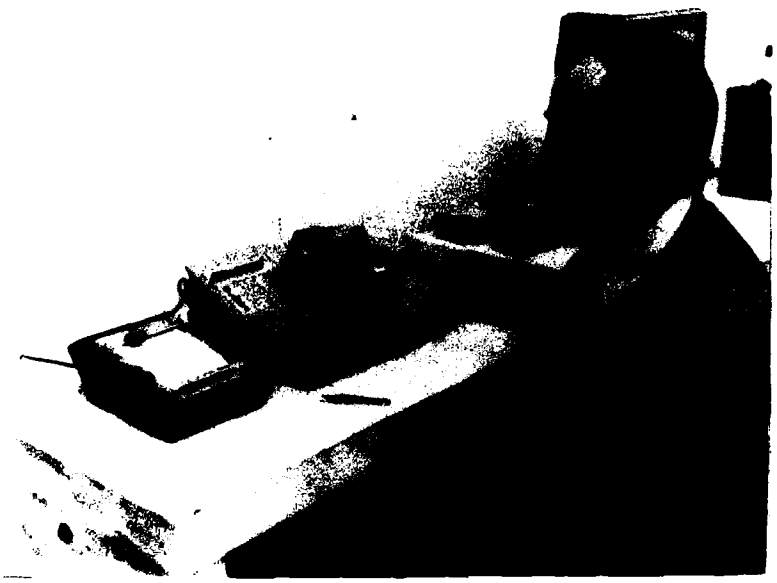
a series of scanning speeds to choose from and a selection of forward or reverse, rapid scan, and sample positioning. By choosing low scan speed along with high strip chart recorder speed, magnification of transverse horizontal scans can be obtained.

Because of the relatively large size of the diamond probe in comparison to many microelectronic dimensions, care must be used in choosing locations for making measurement, or erroneous results may be obtained. For instance, if metallization height is being measured, it would be unwise to try to accurately place a 13 μm diameter diamond probe onto a 2 μm wide strip of metallization. A more correct procedure would be to find a large metal pattern in the microelement to use for measurement. Care must also be used to insure that there is room between adjacent metal elements for the probe head to travel completely down to a lower surface and not be lodged between two metal patterns.

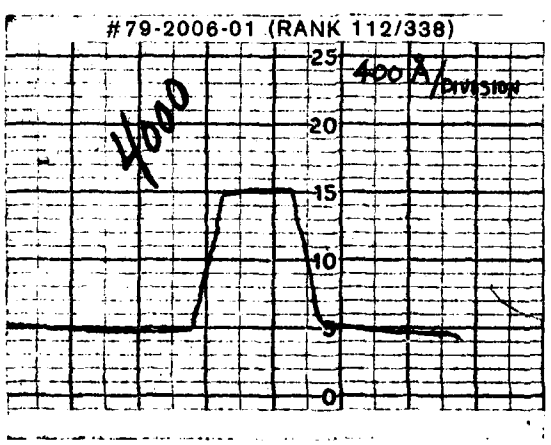
A typical stylus instrument and an example measurement are shown in Figure 1.

3. Interferometry Measurement Systems. Interference phenomena are used to measure thin film thicknesses in a nondestructive manner. Both double and multiple beam equipment are commercially available. Because the interference phenomenon is a function of the wavelength of light, the film thicknesses normally measured by these techniques vary between 30 and 20,000 Å. The type of instrument usually determines the measurement range.

The complete subject dealing with light interference is customarily divided into two subject classifications: diffraction and interference. Interference effects that are due to particular shapes of light wave fronts are grouped under the subject of diffraction. Light interference due to the effects of combining two or more separate beams that come from the same source are grouped under the classification of interference.



a) TYPICAL STYLUS MEASUREMENT EQUIPMENT



b) STRIPCHART RECORDING SHOWING OXIDE THICKNESS OF 4000Å BETWEEN TWO ADJACENT CONTACT OPENINGS

FIGURE 1.

Interference effects are observed only when the interfering beams originate at a common source. This fact is a practical consequence of the frequency of visible light (on the order of 10^{15} Hz) and the lack of homogeneity of known sources. Experiments have shown that the most nearly monochromatic light sources radiate unbroken wave trains for only about 10^{-8} seconds. After a given train is radiated, another train will begin that bears no definite phase relationship with the first. If photographs could be taken in this time period of 10^{-8} seconds, it might be possible to use separate light sources. However, because of the practical fact that much longer periods of time are required to register the effects of interference, the sources must be identical in all respects. To date, this is only possible when the beams originate from a common source.

a) Michelson Interferometer. The Michelson system makes use of two beams of monochromatic light originating from the same source to produce horizontal fringes across step heights. Figure 2 is a schematic of the Michelson interferometer system.

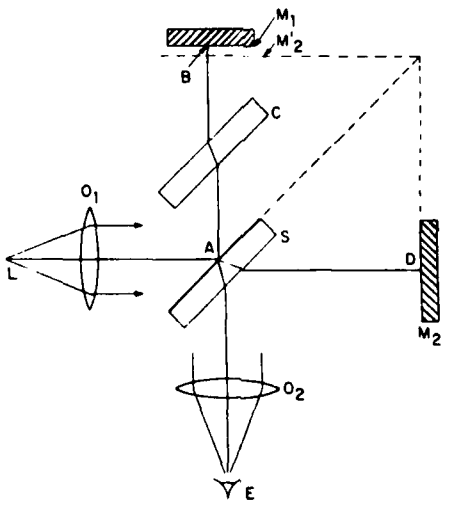


FIGURE 2. SCHEMATIC OF MICHELSON INTERFEROMETER SYSTEMS

In the explanation of how this system works, only the center beam of light will be considered. Referring to Figure 2, the objective O_1 collimates monochromatic light from the source L. The light beam is split at point A by the beam splitter S. The beam splitter may be a beam-splitting prism, a half silvered mirror, a 50% reflecting dielectric-film, or anything suitable, so long as the intensities of the split beams are equal.

The vertical split beam is reflected at point B on mirror M_1 back to point A and through the beam-splitter toward the viewing objective O_2.

The second split beam passes through the beam-splitter and is reflected back from point D on mirror M_2. Under proper conditions, these two beams will combine to give an interference pattern of fringes which will be observable through objective O_2. The interference pattern may either be observed by eye E, or the pattern can be recorded on photographic film.

In this example, the compensating plate C is of the same type of glass and is the same thickness as the beam splitter S. Reflections from mirror M_2 form a virtual image at M'_2. The translational position of one of the mirrors must be adjustable, and each mirror must have three tilting screws so that the relative positions of M_1 and virtual image M'_2 can be adjusted. By adjusting the two mirrors M_1 and M_2 in this way, fringes can be formed.

In actual operating conditions, mirror M_1 is replaced by a silvered sample with a step height to be measured. This step must not be too steep or the fringes across the step cannot be counted. Once fringes are produced with a sample, the step height can be calculated by the equation:

$$d = \frac{\Delta N \lambda}{2}$$ where: ΔN = number of fringes across step height.

λ = wavelength of monochromatic light.

d = step height.

Figure 3 shows diagramatically how the interferometer would be used in measuring the step height for a groove. In this example, the step height would be:

$$\Delta N = 0.5$$

$$d = \frac{0.5\lambda}{2}$$

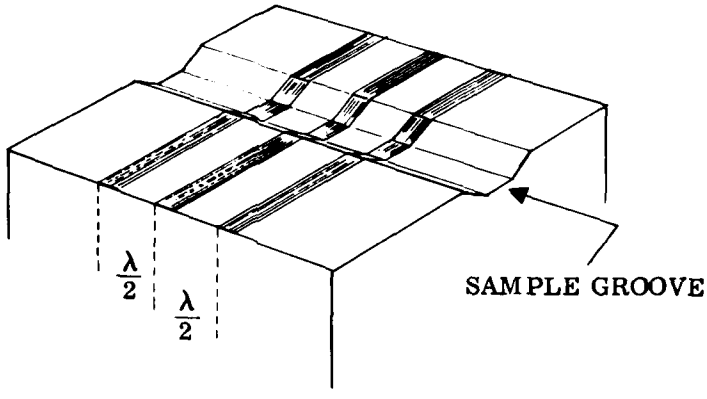
The step height could therefore be calculated when the wavelength of monochromatic light used is substituted into the above equation.

Two beam interferometry is capable of measuring thin film heights in the range of 300 - 20,000 Å with an accuracy of 150 - 300 Å.

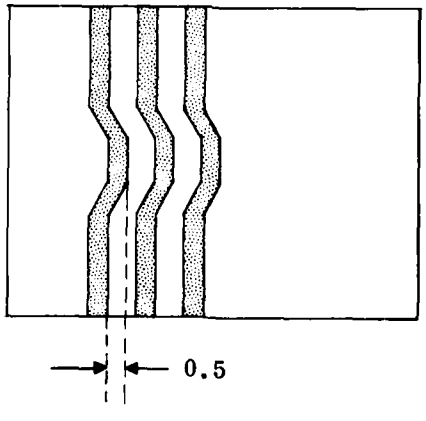
b) Multiple-Beam Systems. The sharpness of and, therefore, the ability to more accurately measure fringes across a step height is increased by using multiple-beams in the interferometer. In the Michelson (or Two Beam) interferometer, the source beam of monochromatic light is split and reflected only once by a 50% reflective beam-splitter (See S in Figure 2). In the multiple-beam system, multiple-beams are produced by using two glass plates with highly reflective coatings facing each other so that the incoming beam is alternately reflected and transmitted many times between the sample and the viewing objective. Figure 4 demonstrates this principle, and R and T denote the amplitudes of reflection and transmission.

Many multiple-beam interferometers employ optics that utilize the Fizeau Fringe method of generating multiple-beams. The use of Fizeau Fringe is commonly called the Tolansky technique.

Fizeau Fringes are generated by a monochromatic beam of light and represent contours of equal thickness arising in an area of varying thickness between two glass plates arranged in a manner similar to that



a. *FRINGE APPEARANCE ACROSS A GROOVE STEP*



b. FRINGE DISPLACEMENT ACROSS GROOVE STEP APPEARING AT INTERFEROMETER VIEWING OBJECTIVE

FIGURE 3. DIAGRAMMATIC REPRESENTATION OF HOW FRINGE DISPLACEMENT WOULD APPEAR ACROSS A STEP HEIGHT USING INTERFEROMETRY

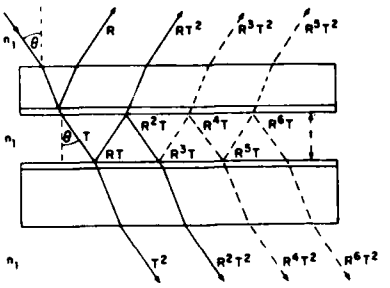


FIGURE 4. SCHEMATIC DIAGRAM OF MULTIPLE-BEAM INTERFERENCE BETWEEN TWO SILVERED GLASS PLATES

shown in Figure 4. In practical systems, multiple beams are produced by contacting the two plates such that they form a slight wedge at a low angle so that there is a gradient in the distance between their silvered surfaces. The slight angle between the plates causes consecutive fringes to be spaced as far apart as possible.

The angle of incidence of the collimated monochromatic light is typically kept very near 0°, and the medium between the plates is air so as to prevent additional beam bending between the plates. Therefore, the spacing between fringes corresponds to a thickness difference of $\lambda/2$. Figure 5 demonstrates diagrammatically the apparatus for producing multiple-beam interference images.

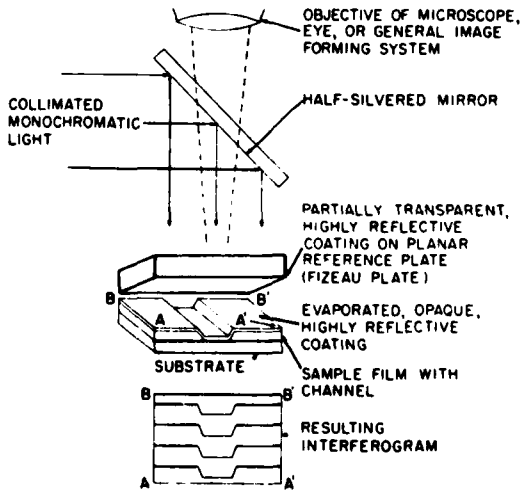


FIGURE 5. DIAGRAM OF APPARATUS USED TO PRODUCE FIZEAU FRINGES (TOLANSKY TECHNIQUE)

The step height is calculated using the same equation as in Michelson interferometry:

$$d = \frac{\Delta N \lambda}{2}$$

Accurate measurements with multiple-beam interferometers require careful evaluation of fringe fractions. The most accurate method of making these measurements is to make linear measurements from a photomicrograph. The accuracy of any measurement technique is highly dependent on the sharpness of the fringe definition. Two further prerequisites to producing sharp images are:

1) The sample surface must be extremely smooth and flat

2) Well-collimated, narrowband monochromatic light must be used

Thickness measurements are routinely made in the range of 30 - 20,000 Å with accuracy as good as $\pm$10 Å.

c) Polar Interferometer (Nomarski). As explained previously, interferometers produce interference patterns by splitting a single beam of monochromatic light into at least two beams which are recombined after traveling different optical paths.

With the Nomarski technique, a beam of light is linearly polarized, directed to the sample and reflected from it. This reflected beam is then split by a Wollaston prism into two equal-intensity beams with their electric vectors at right angles to one another.

The light beams are then passed through a second polarizer called the analyzer. This causes the electric vectors to be reoriented in the same direction. Passing the unsplit beam through the Wollaston prism causes the two split beams to form images which are displaced laterally to each other and also to have a phase difference between the two wave fronts. It is said, then, that the sample produces its own reference.

In making thickness measurements, fringes show along the step edge because of the lateral displacement and interference produced by the beams. The Nomarski equipment has two controls. One control varies the fringe spacing, and the second control varies optical path length. The second control, therefore, sets the position of the zero-order fringe, as well as other orders, within the field of view.

Nomarski fringes use the same equation to calculate step height as the Michelson interferometer, $d = \frac{\Delta N \lambda}{2}$. Likewise, the range of measurement is 300 - 20,000 Å, with accuracy of 150 - 300 Å. Attachments for microscopes are commercially available and relatively easy to use.

4. Ellipsometry. This technique provides a nondestructive way to measure thickness and refractive index of transparent films on reflective substrates. Ellipsometry has been called various polarization spectroscopy and polarimetry. This method is highly accurate for measuring very thin films but may also be used for thicker measurements. The range of thickness measurement is from a few Å to 2-3 μm, with an accuracy of 1 Å to 0.1% of total thickness. Ellipsometry is much more complex than the other techniques described throughout this section.

This technique is based on evaluating the change in state of reflected polarization of light. The state of polarization is determined by the relative amplitude of the perpendicular and parallel components of radiation, and on the phase difference between these two components. Upon reflection from the surface of a sample being measured, the ratio of the parallel and perpendicular amplitudes and the phase difference between them undergo changes that are dependent on the angle of incidence of the beam, the film thickness, and upon the various optical properties of the substrate.

If the optical properties of the film are known, and if the film is nonabsorbing, then the index of refraction and the thickness of the film can be calculated.

The practical use of the ellipsometer requires access to a digital computer and further access to a program that calculates film thickness and index of refraction. In operation, the ellipsometer polarizer and analyzer are rotated to obtain two null points (extinction of light) and, therefore, two sets of readings for polarized and analyzer. It is necessary to have a good idea of the range of film thickness before seeking the null points, because there are 32 possible sets of settings which will give null points. These readings are then fed into an appropriate computer program which calculates film thickness and index of refraction. Figure 6 shows the optical path in the ellipsometer.

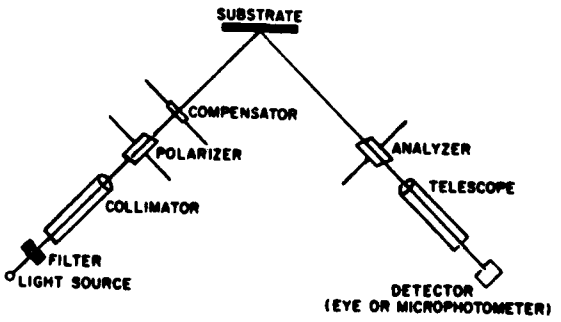


FIGURE 6. OPTICAL PATH IN THE ELLIPSOMETER

Mathematical equations pertaining to the theory of ellipsometry are available from a number of sources (see Reference 1), but are impractical without the use of a computer. However, fully automatic ellipsometers are presently available where one does little more than place a sample in the appropriate place (see Reference 13).

Ellipsometry is generally used much more in microelectronic fabrication work than in failure analysis.

5. Light Section Microscope. This instrument is limited to measurement of films thicker than 1μ. The instrument consists basically of two microscopes. An illuminating microscope projects a slit of light onto a sample at 45° to the sample, and an observing microscope forms an angle of 90° with the illuminating microscope and an angle of 45° with the sample. The image of the slit is observed through an eyepiece equipped with a reticle and micrometer.

If an opaque film is to be measured, the slit must be projected across a step in the film. The separation of the slit images across the step, due to reflection, is measured with the eyepiece micrometer. The accuracy in measuring films in the range of 1 - 400μ is reported to be 0.1μ.

If the film to be measured is transparent, a step is not needed. In the case of transparent films, two images are seen because of reflection from both interfaces involved. The true film thickness is given by the equation:

$$d = d^1(2n^2-1)^{1/2}$$

where:
- d = True film thickness.
- d^1 = Apparent film thickness as determined by micrometer measurement.
- n = Film index of refraction.

6. Linear Measurement Instruments. This class of instruments is used to make measurements of the physical dimensions, length and

width, of objects. The width of metallization lines, the separation between metallization lines, or the size of an integrated circuit chip are all measurements which are typically made in failure analysis work.

a) Filar Eyepiece. This is perhaps the most basic instrument available for physical measurement. The instrument consists of a movable reticule with a calibrated rotary thumbwheel. The apparatus is inserted in a monocular arrangement into a microscope. The instrument can be used with any microscope objective, and it requires a stage micrometer calibration slide. This stage micrometer has horizontal calibrated divisions generally of four types:

1) 2.2 mm long scale, with 0.2 mm of the scale divided into 0.01 mm divisions, with remaining 2.0 mm divided into 0.1 mm length, generally used at 200X magnification

2) Precision scale with twenty 0.01 mm divisions, $\pm$0.05 µm, with complete scale accumulated error no greater than 0.1 µm when used at 68°F (20°C)

3) 0.22 inches scale, with the smallest division 0.001 inches

4) 0.5 inches scale, with the smallest division 0.005 inches

Figure 7 shows an enlarged version of the fourth and third of the above listed scales, respectively.

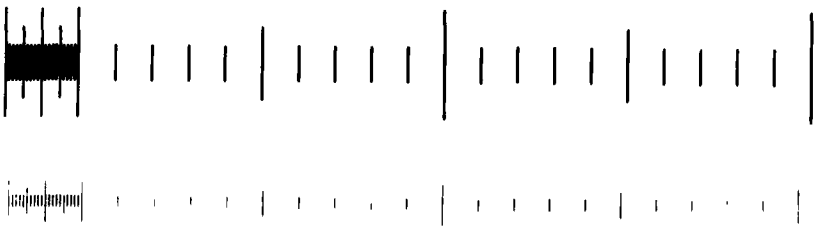


FIGURE 7. ENLARGED VERSION OF TYPICAL STAGE MICROMETER SCALES

Figure 8 shows a typical Filar Eyepiece.

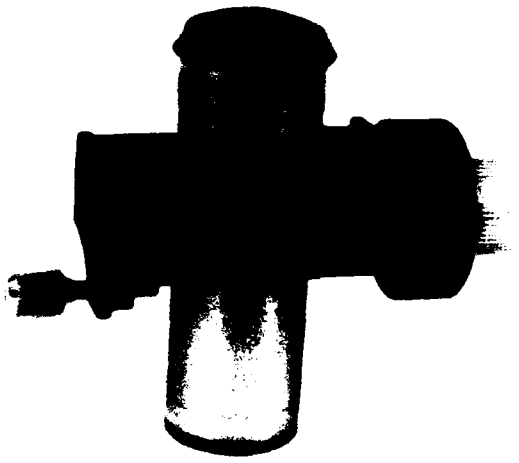


FIGURE 8. TYPICAL FILAR EYEPIECE

To calibrate the instrument, the appropriate objective is first chosen. For instance, if it is desirable to measure large objects, such as chip size, a low power objective is chosen. A high power objective would be used to measure such dimensions as metallization line width.

Looking through the eyepiece, the movable cursor should be moved so that it coincides with one of the calibration marks on the stage micrometer. The reading on the thumbwheel is next recorded. The thumbwheel should then be turned until the adjacent calibration mark is reached. The reading on the calibrated thumbwheel is then recorded a second time.

NOTE: Which adjacent mark should be used in calibration depends on the size object being measured and on the microscope objective being used. For instance, if a die size were being measured, one would not normally calibrate using the minimum spacing on the stage micrometer (see Figure 7), because excessive measurement error would be introduced over the relatively long distances involved.

The difference between the two readings will equal the number of divisions on the thumbwheel required to measure one unit of calibration distance. This will be true only for the specific microscope and objective being used. For example, on a Nikon microscope equipped with a 10X objective and 12.5X Filar Eyepiece, the following readings were made:

1) Calibration made over 0.001 inch marks
2) Initial reading 18
3) Final reading 60
4) 60 - 18 = 42 divisions per 0.001 inches

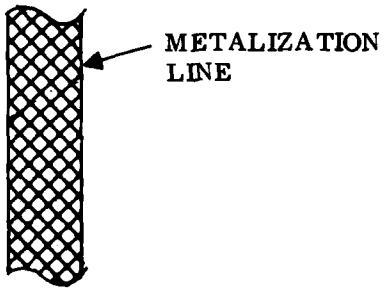
Measurements could then be made of any object visible with the 10X objective. If it becomes necessary to change the objective, the calibration procedure must be repeated.

For more precise filar measurements, digital readout filar eyepiece attachments are available. However, unless a large number of readings are taken routinely, the cost of this attachment may be prohibitive.

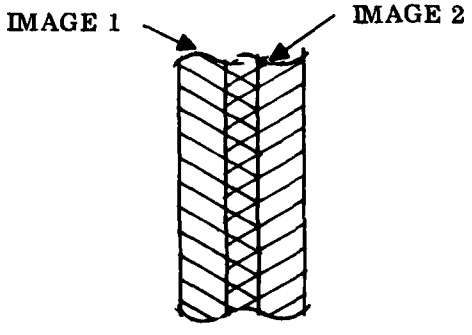
b) Image Splitting Measurement. This instrument is generally regarded as more accurate than the filar type of measurement. The image splitter does not rely on a reference line, the location of which is subject to the variabilities of judgement with each measurement.

The image splitter consists basically of a special prism assembly that can be used in conjunction with a normal metallurgical microscope. The instrument is used in a monocular arrangement in the microscope. Prisms are linked to a micrometer screw, such that their angular relation to each other can be varied. When the prism faces are parallel to each other, two images which are perfectly superimposed will be visible through the eyepiece. These two images will appear as one image only. As the micrometer screw is turned, these two images will move, or shear, across each other. This movement is continued until the object being measured is viewed as being two separate objects. Then, the two images are brought so as to be just touching. This is the correct measurement procedure. Figure 9 diagrammatically demonstrates the measurement procedure.

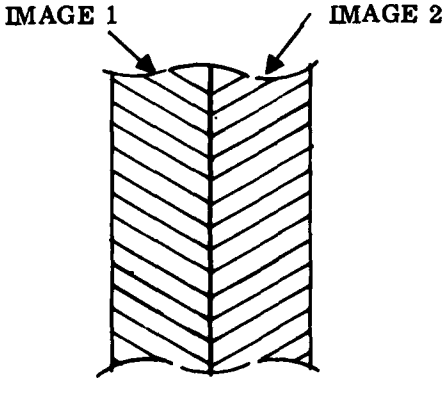
This instrument must be calibrated in the same way as the filar eyepiece. The same procedure is used as with the filar. A calibrated division on a stage micrometer is sheared, thus obtaining a dimensional value for each division on the measuring drum. As with the filar instrument, this calibration is valid only for the specific objective being used.



a. PREMEASUREMENT PERFECTLY SUPERIMPOSED IMAGE



b. INTERMEDIATE SHEAR IMAGE



C. PERFECT SHEAR FOR MEASUREMENT

FIGURE 9. DIAGRAMMATIC SCHEMATIC FOR CORRECT USE OF OPTICAL SHEAR MEASUREMENT

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11. Heavens, O.S. Optical Properties of Thin Solid Films, Butterworth Scientific Publications, London, 1955.

12. Mansour, T.M., Mater, Res. Std., Vol. 3, No. 33, 1959.

13. Bloem, H.H., et al. "Development of An Automatic Ellipsometer," Electro-Optical Systems Design March 1980, pp 38 - 45.

EQUIPMENT

Stylus Measurement

1.	Tallysurf Tallysurf Mfg. Co., Chicago, IL	$10,000
2.	Alpha-Step Tencor Instruments, Mountain View, CA	$ 9,500
3.	Dektak Sloan Technology Corp., Santa Barbara, CA	$ 9,000

Interferometry Systems

1.	(Michelson) Carl Zeiss, Inc., NY, NY	$ 1,500
2.	(Michelson) Gaertner Scientific Corp., Chicago, IL	$ 1,500
3.	Two Beam Attachment (Michelson) E. Leitz, Inc., Rockleigh, NJ	$ 1,500
4.	Sloan Angstrometer M-100 (Multiple Beam Fizeau) Sloan Technology Corp., Santa Barbara, CA	$ 4,000
5.	Varian Å-Scope (Multiple Beam Fizeau) Varian Vacuum Division, Palo Alto, CA	$ 4,000

Ellipsometry Systems

1.	RR 100 Routine Ellipsometer Rudolph Research, Fairfield, NJ	$ 4,500
2.	Ellipsometer Gaertner Scientific Corp., Chicago, IL	$ 4,500
3.	Automatic Ellipsometer, Model L-2 Rudolph Research, Fairfield, NJ	$20,000

Light Section Microscope

1.	Light Section Microscope Carl Zeiss, Inc., NY, NY	$19,000

Filar Eyepiece

1.	Filar E. Leitz, Inc., Rockleigh, NJ	$ 275
2.	Filar Bausch & Lomb Co., Rochester, NY	$ 275
3.	Digital Filar E. Leitz, Inc., Rockleigh, NJ	$ 2,800

K.

MECHANICAL ANALYSIS TECHNIQUES

K. Mechanical Analysis Techniques.

1. Introduction. These techniques are used in failure analysis to evaluate the integrity of some mechanical aspects of microelectronic assembly methods.

2. Ultrasonic Cleaning Methods. This cleaning procedure is quite efficient, but the failure analyst should proceed with appropriate care before using it. For example, weak or marginal wire or die bonds may break during cleaning as a result of the ultrasonic energy. Valuable data regarding failure may therefore be irretrievably lost. It has also been reported that ultrasonic cleaning has caused defects (cracks) in MOS gate oxide structures. Careful consideration should be given to the possible consequences before ultrasonic cleaning is used.

Ultrasonic cleaning systems consist of the following equipment:

a) Ultrasonic Generator. Produces high frequency electrical power output usually in the range of 20,000 - 50,000 Hz. These generators are of two types:

o Manual Tuning. This type of generator is equipped with a single "tuning" control and a meter indicating power delivered to the transducers. These generators are usually low power bench top models where the tuning control is readily accessible. Tuning is required because of change in liquid level, change in the work load, etc.

o Automatic Tuning. This type of generator is usually higher power than manual tuning models and is generally more permanently fixed. These generators are capable of self-adjusting the power output to compensate for changes in load, liquid level, etc.

b) Transducers. These will convert electrical energy from the generator into mechanical energy.

c) Tank. Container through which the mechanical energy is transferred to a liquid. The transducers are in physical contact with the tank through suitable attachments.

d) Cleaning Liquids. Used in the tank to transmit the ultrasonic energy to the part being cleaned. Usually, however, a beaker containing the part to be cleaned and a cleaning solution are placed in an energy-transmitting liquid, such as water, that fills the tank. A wire basket can also be fabricated to contain the part to be cleaned. This basket can be hung from the container's top rim.

Ultrasonic cleaning does not "shake off" solid contaminants but rather cleans as a result of cavitation. The energy from the transducers causes the generation of minute bubbles in the cleaning liquid. These bubbles collapse violently and the resulting impact against the immersed part results in erosion of surface contaminants.

The choice of a cleaning liquid depends on several factors:

- What is to be cleaned off. For example, to clean organic contamination, ionic contaminants, surface dirt, or any of many other possibilities, the proper solution, such as detergent, solvent, acid, etc., will be dictated by the contaminant (see Chapter III-M).

- What materials the sample is composed of. For example, if a sample has exposed metal, most acid solutions should be avoided.

- Cost and availability of cleaning solutions

- Possible fire and health hazards

3. Bond Pull Tests. The purpose of this test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable procurement document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead devices.

NOTE: Wire bond strength is a function of several variables, such as age, material used, wire diameter, wire doping, metal system used (gold-aluminum or aluminum-aluminum), temperature of bonding, annealing effects due to temperature of package sealing, and operation, etc. There are additional factors which the failure analyst must take into account when analyzing wire bond strength. Some of these factors are:

- Some microelectronic devices go through a wire bond pre-stress test in which the wire bonds are tested at a force which should be below their failure point.

- Conformal coatings are used on many microelectronic elements, such as on hybrid package boards and on printed circuit boards (e.g., silicones, epoxy, parylene). Therefore, a wire bond strength test may be greatly influenced by the presence of such a coating.

- Other factors concerning the history of the sample may be relevant, such as: environmental shock during lifetime; ultrasonic cleaning, etc.

All these factors may have some influence on wire bond pull tests and should be kept in mind at all times.

The apparatus for this test consists of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) at the point of failure shall be provided by equipment capable of measuring stresses up to and including 10 gf with an accuracy of ±0.25 gf, stresses between 10 and 50 gf with an accuracy of ±0.5 gf, and stresses exceeding 50 gf with an accuracy of ±2.5 percent of indicated value.

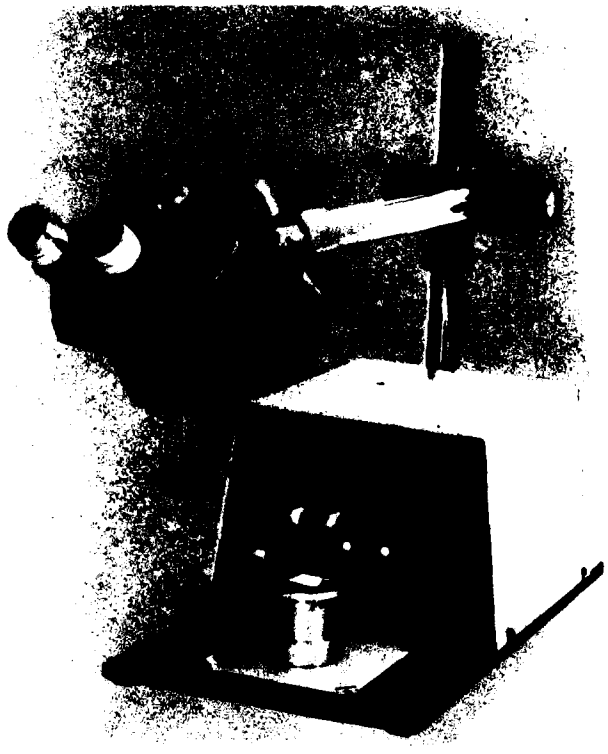
Figure 1 shows, respectively, typical equipment that might be set up in the laboratory and automatic equipment available for bond pull measurements. Figure 2 shows the manual equipment in use.

a) General Procedures

The test shall be conducted using the test condition specified in the applicable procurement document consistent with the particular device construction. All bond pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Unless otherwise specified, for conditions A, C, and D, detailed below, the LTPD specified for the bond strength test shall determine the minimum sample size in terms of the minimum number of bond pulls to be accomplished rather than the number of complete devices in the sample, except that the required number of bond pulls shall be randomly selected from a minimum of 10 devices. Unless otherwise specified, for conditions F, G, and H, the LTPD specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices (all conditions), a minimum of 10 die on a minimum of 2 completed devices shall be used. Where there is any adhesive, encapsulant or other material under, on, or surrounding the die such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

a) Manual Equipment Setup

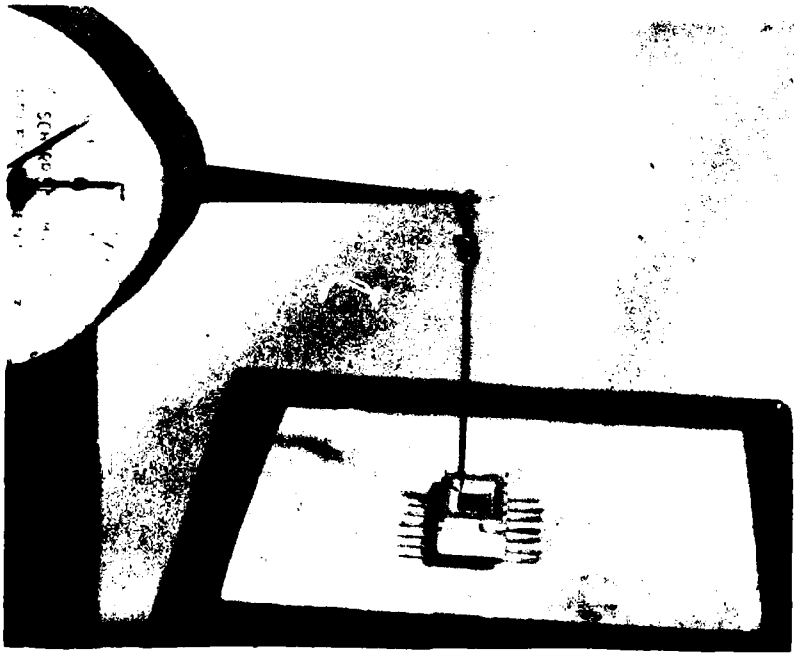
FIGURE 1. TYPICAL EQUIPMENT FOR PERFORMING BOND PULL TESTS IN THE LABORATORY (SHEET 1 OF 2)



b) Automatic Bond Pull Equipment

FIGURE 1. TYPICAL EQUIPMENT FOR PERFORMING BOND PULL TESTS IN THE LABORATORY (SHEET 2 OF 2)

a)



b)

FIGURE 2. BOND PULL TEST BEING PERFORMED

When flip chip or beam-lead chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

o The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

o The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

o The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

b) Test Conditions.

o Test Condition A - Bond Peel. This test is normally employed for bonds external to the device package. The lead or terminal and the device package shall be gripped or clamped in such a manner that a peeling stress is exerted with the specified angle between the lead or terminal and the board or substrate. Unless otherwise specified, an angle of 90 degrees shall be used. When a failure occurs, the force causing the failure and the failure category shall be recorded.

o Test Condition C - Wire Pull (Single Bond). This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. The wire connecting the die or substrate shall be cut so as to provide two ends accessible for pull test. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull test at the opposite termination. The wire

shall be gripped in a suitable device and simple pulling action applied to the wire or to the device (with the wire clamped) in such a manner that the force is applied within 5 degrees of the normal to the surface of the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

o Test Condition D - Wire Pull (Double Bond). This procedure is identical to that of test condition C, except that the pull is applied by inserting a hook under the lead wire (attached to die, substrate or header at both ends) with the device clamped and the pulling force applied approximately in the center of the wire in a direction within 5 degrees of the normal to the die or substrate surface or normal to a straight line between the bonds. When a failure occurs, the force causing the failure and the failure category shall be recorded.

o Test Condition F - Bond Shear (Flip Chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted. A suitable tool or wedge shall be brought in contact with the die (or carrier) at a point just above the primary substrate and a force applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate to cause bond failure by shear. When a failure occurs, the force at the time of failure and the failure category shall be recorded.

o Test Condition G - Push-off Test (Beam Lead). This test is normally employed for process control and is used on a sample of semiconductor die bonded to a specially prepared substrate. Therefore, it cannot be used for random sampling of production or inspection lots. A metallized substrate containing a hole shall be employed. The hole, appropriately centered, shall

be sufficiently large to provide clearance for a push tool but not large enough to interfere with the bonding areas. The push tool shall be sufficiently large to minimize device cracking during testing but not large enough to contact the beam leads in the anchor bond area. Proceed with push-off tests as follows: The substrate shall be rigidly held and the push tool inserted through the hole. The contact of the push tool to the silicon device shall be made without appreciable impact (less than 0.01 inch/minute [0.254 mm/minute]) and forced against the underside of the bonded device at a constant rate. When failure occurs, the force at the time of failure and the failure category shall be recorded.

o Test Condition H - Pull-off Test (Beam Lead). This test is normally employed on a sample basis on beam lead devices which have been bonded down on a ceramic or other suitable substrate. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a loop of nichrome or kovar wire) to make connection with a hard setting adhesive material (for instance, heat sensitive polyvinyl acetate resin glue) on the back (top side) of the beam lead die. Care should be taken to assure that no adhesive flows down the beam or under the die. The substrate shall be rigidly installed in the pull-off fixture, and the pull-off rod shall make firm mechanical connection to the adhesive material. The device shall be pulled within 5 degrees of the normal to at least the calculated force (see 3.2) or until the die is at 2.54 mm (0.10 inch) above the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

c) Failure Criteria. Any bond pull which results in separation under an applied stress less than that indicated in Table I as the required minimum bond strength for the indicated test condition, composition, and construction shall constitute a failure.

TABLE I

MINIMUM BOND STRENGTH

Test condition	Wire composition and diameter 2/	Construction 1/	Minimum bond strength (grams force)	
			Pre seal	Post seal and any other processing and screening when applicable
A	---	---	Given in applicable document	Given in applicable document
C or D	AL 0.0007 in AU 0.0007 in	Wire	1.5 2.0	1.0 1.5
C or D	AL 0.0010 in AU 0.0010 in	Wire	2.5 3.0	1.5 2.5
C or D	AL 0.00125 in AU 0.00125 in	Wire	Same bond strength limits as the 0.0013 in wire	
C or D	AL 0.0013 in AU 0.0013 in	Wire	3.0 4.0	2.0 3.0
C or D	AL 0.0015 in AU 0.0015 in	Wire	4.0 5.0	2.5 4.0
C or D	AL 0.0030 in AU 0.0030 in	Wire	12.0 15.0	8.0 12.0
F	Any	Flip-chip	5 grams-force x number of bonds (bumps)	
G or H	Any	Beam lead	30 grams force per linear millimeter of nominal, undeformed (before bonding) beam width. 3/	

NOTES:

1/ For ribbon wire, use the equivalent round wire diameter which gives the same cross-sectional area as the ribbon wire being tested.

2/ For wire diameters not specified, use the curve of figure 2011-1 to determine the bond pull limit.

3/ For condition G or H, the bond strength shall be determined by dividing the breaking force by the total of the nominal beam widths before bonding.

o Failure Category. Failure categories are as follows: (When specified, the stress required to achieve separation and the category of separation or failure shall be recorded.)

oo For Internal Wire Bonds:

- Wire break at neckdown point (reduction of cross section due to bonding process)
- Wire break at point other than neckdown
- Failure in bond (interface between wire and metallization) at die
- Failure in bond (interface between wire and metallization) at substrate, package post, or other than die
- Lifted metallization from die
- Lifted metallization from substrate or package post
- *Fracture of die*
- Fracture of substrate

oo For External Bonds Connecting Device to Wiring Board or Substrate:

- Lead or terminal break at deformation point (weld affected region)
- Lead or terminal break at point not affected by bonding process
- Failure in bond interface (in solder or at point of weld interface between lead or terminal and the board or substrate conductor to which the bond was made)
- Conductor lifted from board or substrate
- Fracture within board or substrate

oo For Flip-Chip Configurations:

- Failure in the bond material or pedestal, if applicable
- Fracture of die (or carrier) or substrate (removal of portion of die or substrate immediately under the bond)
- Lifted metallization (separation of metallization or bonding pedestal from die, or carrier, or substrate)

oo For Beam Lead Devices:

- Silicon broken
- Beam lifting on silicon
- Beam broken at bond
- Beam broken at edge of silicon
- Beam broken between bond and edge of silicon
- Bond lifted
- Lifted metallization (separation of metallization) from die, separation of bonding pad
- Lifted metallization

Table I lists the minimum bond strength allowable for the various test conditions.

Figure 3 shows minimum bond pull limits.

Figure 4 shows typical bond pull test data.

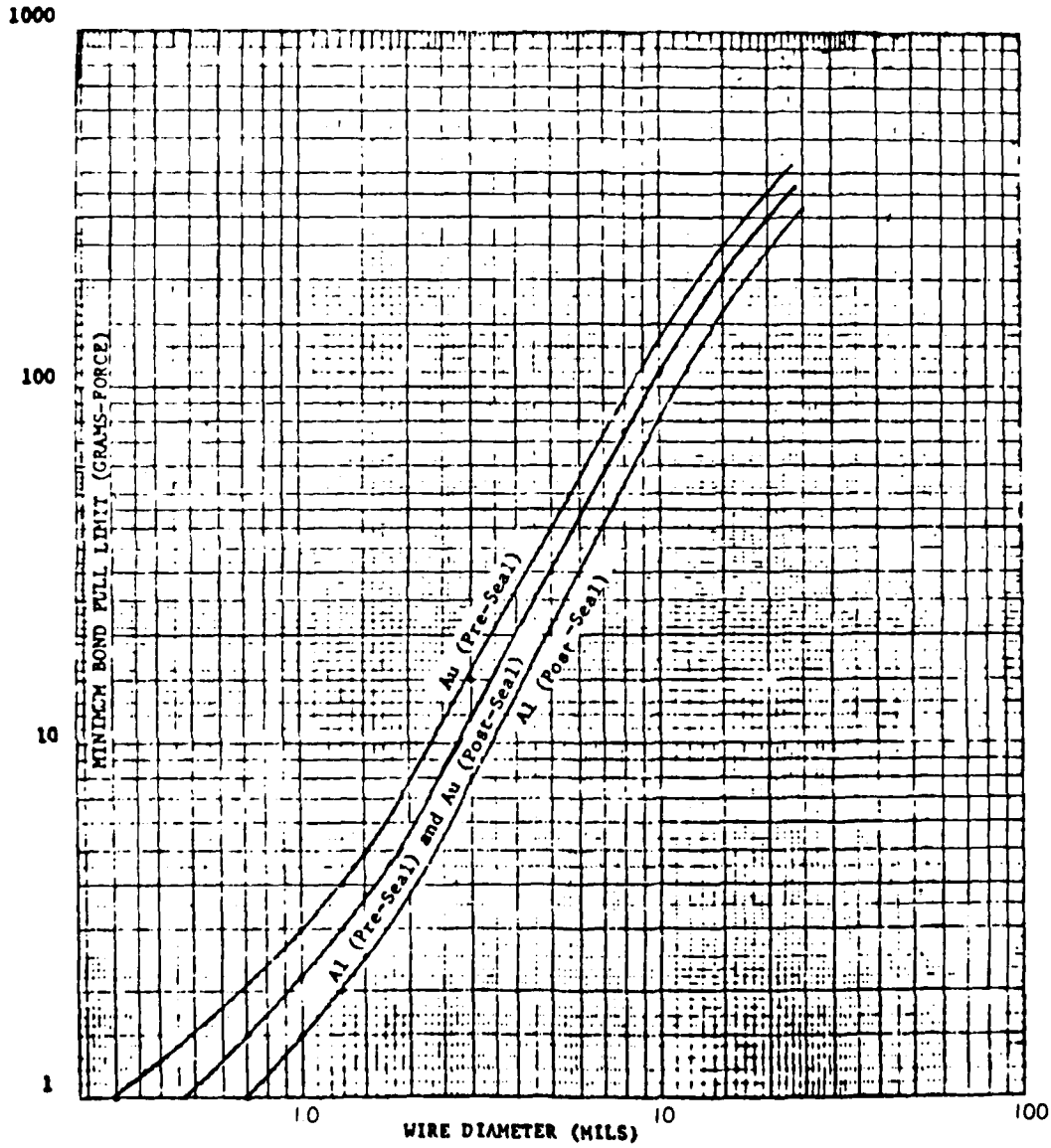


FIGURE 3. MINIMUM BOND PULL LIMITS

Tensile Pull Test MIL-STD-883 Method 2011

Bond Wire Material:	Pkg. Pad Material:	S/S Pad Material:
( ) Aluminum	( ) Aluminum	( ) Aluminum
(x) Gold	(x) Gold	(x) Gold
( ) _____	( ) _____	( ) _____

1.0 (Mils) Wire Dia. Part Type Miller Hybrid

S/N 0009

PULL TEST DATA Gold Wire Bonds: Pkg. feed thru to substrate

Lead & I.D. No.	Wire Bond Type	Failure (grams)	Wire Break	S/S Bond	Pkg. Bond	*	Remarks
Area 12 Lead 1	Wedge to Ball Bond	6.8	X			2	
Lead 2		6.2	X			2	
Area 13 Lead 1		6.5	X			2	
Lead 2		6.4	X			2	
Total Pull Tests = 30							
Average Pull Strength =		6.467 grams					
High Pull Strength =		7.5 grams					
Low Pull Strength =		5.5 grams					
Standard Deviation =		0.479					

* NOTES:
(1) Wire break at neckdown point (due to bonding process).
(2) Wire break at point other than neckdown.
(3) Failure in bond (interface between wire and metallization).
(4) Lifted metallization (separation of metallization of bond pad from die or substrate).
(5) Fracture of die or substrate under the bond.

FIGURE 4. TYPICAL BOND PULL TEST DATA

d) Summary. The following details shall be specified in the applicable procurement document:

- o Test condition letter (see a.)
- o Minimum bond strength if other than specified in c. or details of required strength distributions if applicable
- o LTPD or number and selection of bond pulls to be tested on each device, and number of devices, if other than 10
- o For test condition A, angle of bond peel if other than 90 degrees, and bond strength limit (see c.)
- o Requirement for reporting of separation forces and failure categories, when applicable (see failure category)

4. Die Shear Tests. The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die to package headers or other substrates. This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.

The test equipment consists of a load-applying instrument with an accuracy of ±5 percent of full scale or 50 grams, whichever is less. A circular dynamometer with a lever arm or a linear motion force-applying instrument may be used to apply the force required for testing. The test equipment shall have the following capabilities:

- o A die contact tool which applies a uniform distribution of the force to an edge of the die (see Figure 5)

o Provisions to assure that the die contact tool is perpendicular to the die mounting plane of the header or substrate

o A rotational capability, relative to the header/substrate holding fixture and the die contact tool, to facilitate line contact on the edge of the die, i.e., the tool applying the force to the die shall contact the die edge from end-to-end (see Figure 6)

o A binocular microscope with magnification capabilities of 10X minimum and lighting which facilitates visual observation of the die and die contact tool interface during testing

a) Procedure. The test shall be conducted as defined herein or to the test conditions specified in the applicable specific procurement document consistent with the particular part construction. All die strength tests shall be counted and the specific sampling, acceptance, and added sample provisions shall be observed, as applicable.

o A force sufficient to shear the die from its mounting or equal to twice the minimum specified shear strength (Figure 7), whichever occurs first, shall be applied to the die using the apparatus above (see also Figure 8).

o When a linear motion force-applying instrument is used, the direction of the applied force shall be parallel with the plane of the header or substrate and perpendicular to the die being tested.

o When a circular dynamometer with a lever arm is employed to apply the force required for testing, it shall be pivoted about the lever arm axis, and the motion shall be parallel with the

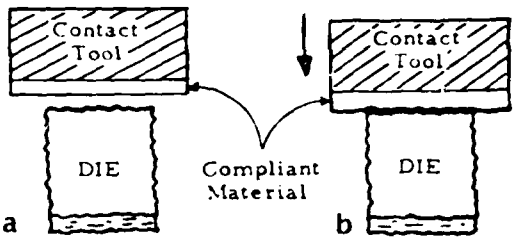


FIGURE 5. COMPLIANT INTERFACE ON CONTACT TOOL DISTRIBUTES LOAD TO THE IRREGULAR EDGE OF THE DIE.

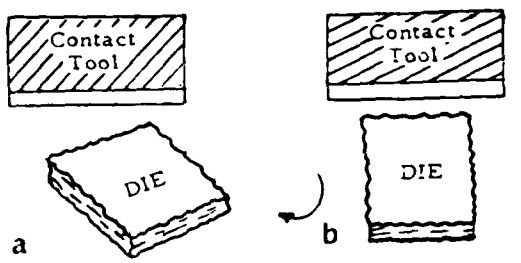


FIGURE 6. ROTATE THE DIE CONTACT TOOL FOR PARALLEL ALIGNMENT.

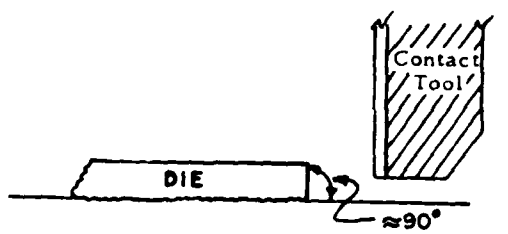


FIGURE 7. THE CONTACT TOOL SHALL LOAD AGAINST THAT EDGE OF THE DIE WHICH FORMS AN ANGLE ≈ 90° WITH THE HEADER/SUBSTRATE.

plane of the header or substrate and perpendicular to the edge of the die being tested. The contact tooling attached to the lever arm shall be at a proper distance to assure an accurate value of applied force.

o The die contact tool shall load against an edge of the die which most closely approximates a 90 degree angle with the base of the header or substrate to which it is bonded (see Figure 7).

o After initial contact with the die edge and during the application of force, the relative position of the contact tool shall not move vertically such that contact is made with the header/substrate or die attach media. If the tool rides over the die, a new die may be substituted or the die may be repositioned, provided that the requirements listed regarding angle of tool with die edge are met.

b) Failure Criteria. A device which fails any of the following criteria shall constitute a failure:

o Fails die strength requirements (1.0X) of Figure 8

o Separation with less than 1.25 times the minimum strength (1.0X) specified in Figure 8 and evidence of less than 50 percent adhesion of the die attach medium

o Separation with less than 2.0 times the minimum strength (1.0X) specified in Figure 8 and no evidence of adhesion of the die attach medium

NOTE: Residual silicon attached in discrete areas of the die attach medium shall be considered as evidence of such adhesion.

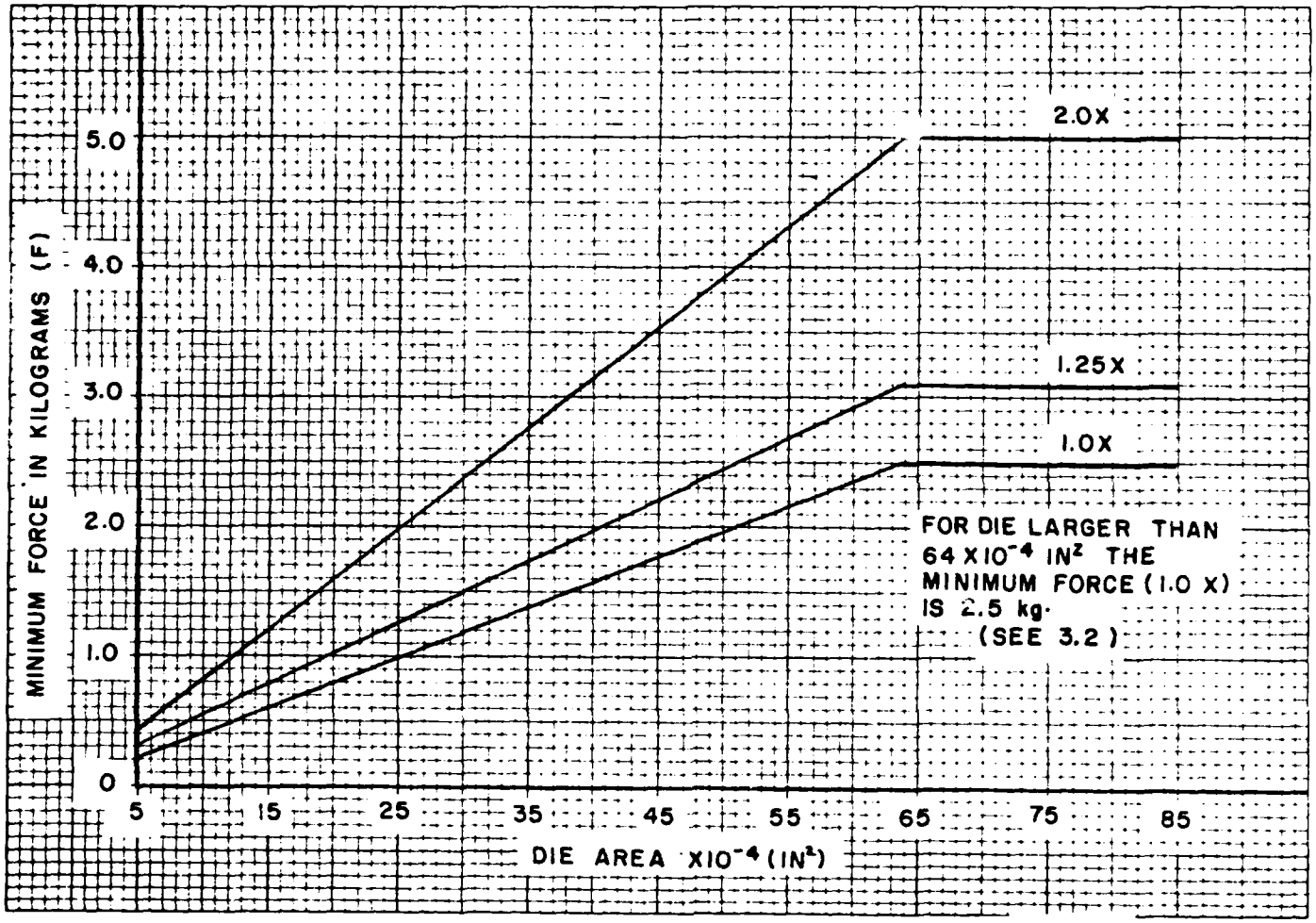


FIGURE 8. DIE SHEAR STRENGTH CRITERIA (MINIMUM FORCE VS. DIE ATTACH AREA)

c) Separation Categories. When specified, the force required to achieve separation and the category of the separation shall be recorded:

- o Shearing of die with residual silicon remaining
- o Separation of die from die attach medium
- o Separation of die and die attach medium from package

d) Summary. The following details shall be specified in the applicable procurement document:

- o Minimum die attach strength if other then shown in Figure 8
- o Number of devices to be tested and the acceptance criteria
- o Requirement for data recording, when applicable

5. Wire Rebonding. Gold and aluminum wire are used extensively throughout the microelectronics industry for electrically connecting microcircuits. The thickness of these wires usually lies between 17.8 μm and 50.8 μm, with the thicker wires most often used with high power devices.

Machines are commercially available for bonding either gold or aluminum wires. Figure 9 demonstrates how a 0.001 inch aluminum wire is bonded, and Figure 10 shows a typical wedge bond.

Gold wire is commonly bonded by either a thermocompression or an ultrasonic technique, both of which form a "ball" bond. In both techniques, a ball is formed by melting the gold wire at the end of a capillary tube prior to bonding. Melting is achieved by either burning hydrogen gas or by creating an electrical arc between

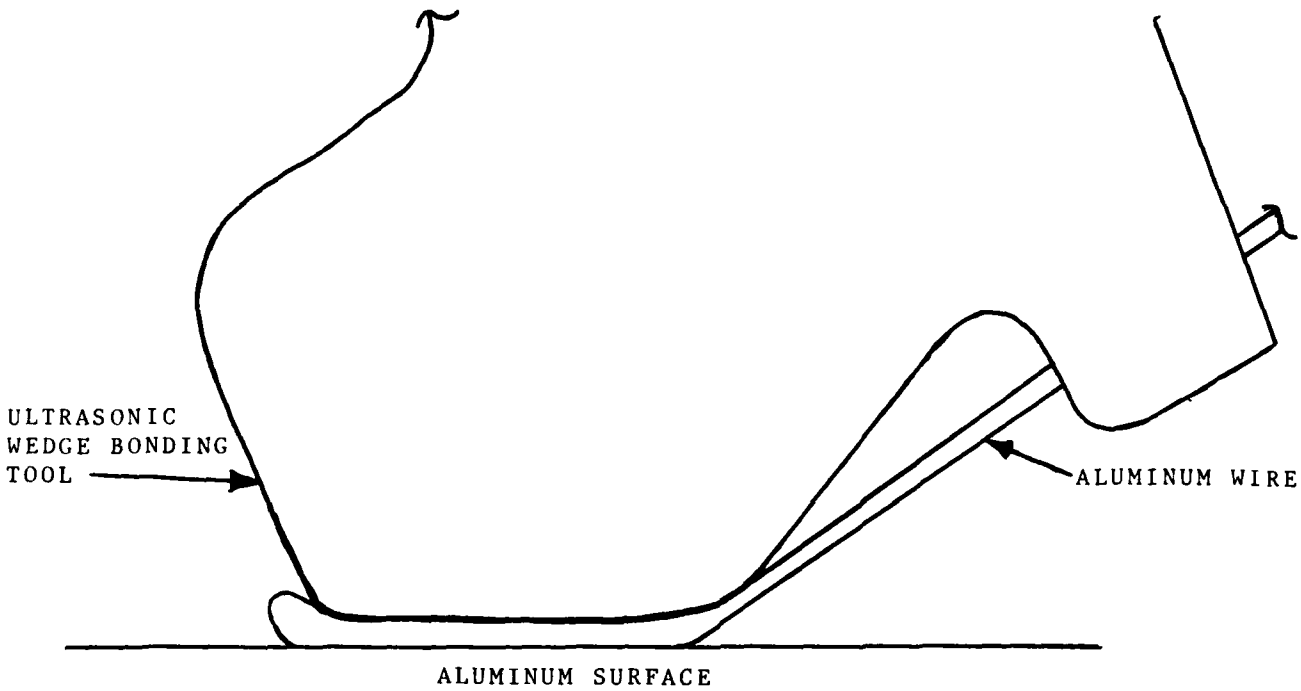


FIGURE 9. ULTRASONIC WEDGE BONDING

FIGURE 10. 0.001 INCHES ALUMINUM WIRE WEDGE BONDED TO INTEGRATED CIRCUIT PAD

the gold wire and a passing electrode. Figure 11 diagrammatically represents the ball forming process, and Figure 12 shows a ball bond.

During failure analysis, it is sometimes desirable to reconnect microcircuit electrical connections internal to a package. For example, internal wires are commonly removed during fault isolation, and after a fault has been either corrected or isolated from a circuit, it might be desirable to retest. In order to retest, the internal wiring of the package must be rebonded.

If wire bonding equipment such as that previously described is available, it is a relatively simple matter to rewire microcircuits, providing, of course, that microcircuit metallization pads have not been removed or irreparably damaged during package opening and/or subsequent processes.

6. Particle Impact Noise Test. The following procedure is extracted directly from MIL-STD-883B, Method 2020.1:

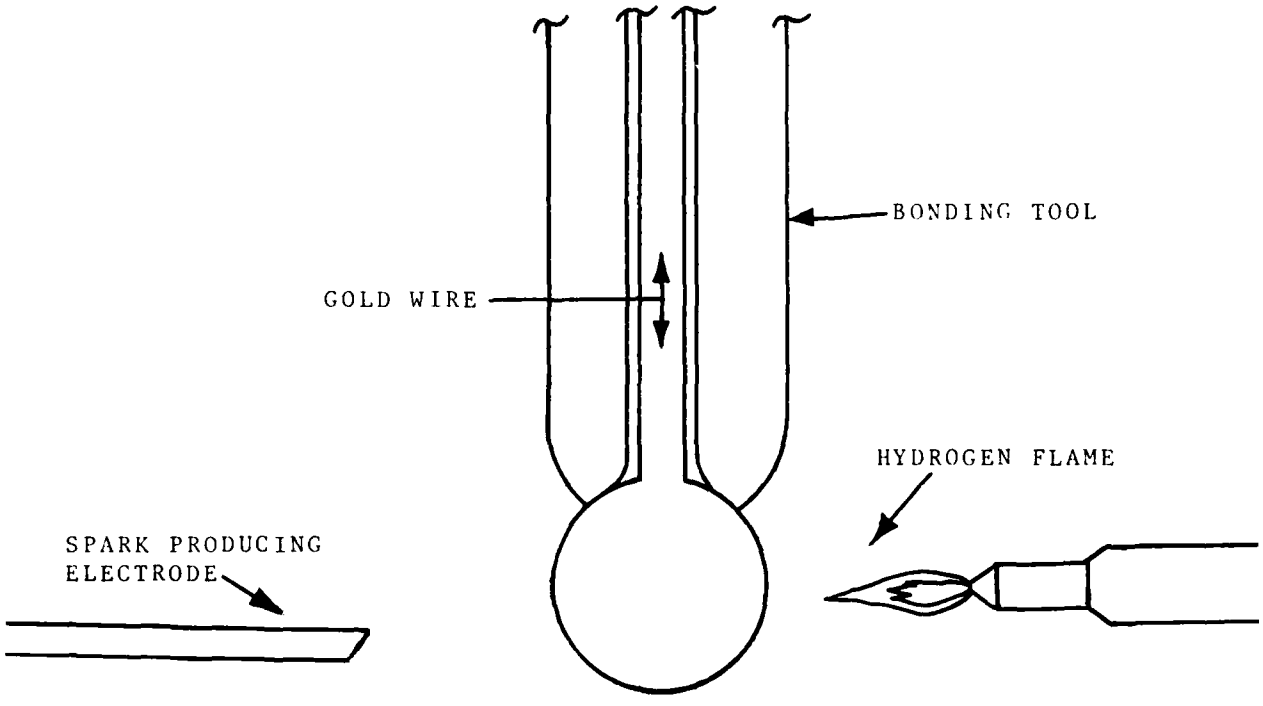


FIGURE 11. GOLD BALL FORMATION

FIGURE 12. GOLD BALL BOND ON AN INTEGRATED CIRCUIT BONDING PAD

PARTICLE IMPACT NOISE DETECTION TEST

1. PURPOSE. The purpose of this test is to detect loose particles inside a device cavity. The test provides a nondestructive means of identifying those devices containing particles of sufficient mass that, upon impact with the case, excite the transducer. Because of the limited efficiency of this test method, it may be desirable to subject devices to several sequences of this test in order to achieve desired confidence.

2. APPARATUS. The equipment required for the particle impact noise detection (PIND) test shall consist of the following (or equivalent):

a. A dual beam oscilloscope capable of 500 kHz response minimum, and a sensitivity of 20 mV/cm for visual display of the particle noise and of the threshold detector. Alternatively, a single beam oscilloscope may be used in conjunction with a lamp indicator for the threshold detection circuit.
b. A threshold detector to detect particle noise voltage exceeding a preset threshold of 5 ±1 millivolt peak above system peak noise. See figure 2020-4 for an acceptable circuit to perform the threshold detection function.
c. An audio system with speaker to monitor the audio signal from the PIND electronics. If headphones are used, the system shall provide safeguards against loud noise bursts.
d. A vibration shaker and driver assembly with a payload consisting of the DUT, (PIND) transducer, the transducer isolator, preamplifier (when included), co-test shock mechanism (when included), a portion of the transducer cable and its restraints, capable of providing essentially sinusoidal motion at:
   1. Condition A - 20g peak at 40 to 250 Hz.
   2. Condition B - 10g peak at 60 Hz.
e. PIND transducer, calibrated to a peak sensitivity of -77.5 ±3 dB re one volt per microbar at a point within the frequency of 150 to 160 kHz.
f. A sensitivity test unit (STU) (see figure 2020-3) for periodic assessment of the PIND system performance. The STU shall consist of a transducer with the same tolerances as the PIND transducer and a circuit to excite the transducer with a 250 microvolt ±20 percent pulse. The STU shall produce a pulse of about 20 mV peak on the oscilloscope when the transducer is coupled to the PIND transducer with attachment medium.
g. PIND electronics, consisting of an amplifier with a gain of +60 ±2 dB centered at the frequency of peak sensitivity of the PIND transducer to amplify the transducer signal to a usable level for threshold detection, audio detection and oscilloscope display. The noise at the output of the amplifier shall not exceed 10 mV peak.
h. Attachment medium. The attachment medium used to attach the DUT to the PIND transducer shall be either a viscous acoustic couplant such as Automation Industries No. 50A4084 (or equivalent) or double-faced tape such as Permacel P50 (or equivalent).
i. Co-test shock mechanism or tool, consisting of the integral co-test shock mechanism of 2.d. above (when included), or a six-inch solid AWG No. 10 copper rod with rounded end, or other mechanism capable of imparting shock pulses between 200 and 1500g to the DUT. The duration of the main shock shall not exceed 100 microseconds.
j. Special mounting adapters for devices which have irregular surfaces (see 3.3.2).
k. Isolator material between the PIND transducer and the vibration shaker and driver when required to reduce background noise. The isolator shall have no resonance within the test frequency range.

1. A pre-test shock fixture capable of imparting shock pulses between 500 and 1800g to the DUT. The duration of the main shock shall not exceed 100 microseconds. A co-test shock mechanism integral to the shaker and driver may be used for this purpose.

3. PROCEDURES.

3.1 Test equipment set-up. The test equipment shall be connected as indicated in figure 2020-1 and set-up in a low background noise area. Critical settings to provide proper detection sensitivity, unless otherwise specified, are as follows:

a. Audio output volume shall be adjusted to a comfortable noise level output.
b. Shaker drive frequency shall be adjusted in accordance with figure 2020-2 for condition A, or at 60 Hz for condition B.
c. Shaker drive amplitude shall be 20g (condition A) or 10g (condition B) with DUT and mounting adapter (if any) in place.
d. Oscilloscope vertical deflection primary beam sensitivity (displaying PIND electronics output) shall be 20 millivolts/centimeter. Secondary beam sensitivity (if displaying threshold detector output) shall produce approximately a 2 centimeter deflection difference between the two states of the threshold detector. The secondary beam display (without horizontal deflection) shall be centered vertically and approximately 1 centimeter to the left or right of the primary beam display.
e. Oscilloscope horizontal deflection shall be adjusted to 4 cm and shall obtain drive from the sine generator/amplifier, amplified accelerometer, or a time base (2 ms/cm) triggered from the accelerometer output.

3.2 Test equipment checkout. The test equipment checkout shall be performed to assure proper system operation, when any of the following occurs:

a. After a change of vibration frequency.
b. System shut-down for any reason.
c. Change of operators.
d. Work shift change.
e. Prior to and after testing group(s) of devices or every 4 hours during the test operating period, whichever comes first. System deficiencies shall be corrected prior to test. Failure of the system to meet checkout requirements shall require retest of all devices tested subsequent to the last successful system checkout.

3.2.1 Shaker drive system checkout. The drive system shall achieve the shaker frequency specified in 3.1 b. and the shaker amplitude specified in 3.1 c. If a visual displacement monitor is affixed to the transducer, it may be used for amplitudes between 0.04 and 0.12 inch (1.02 and 3.05 mm). An accelerometer may be used over the entire range of amplitudes and shall be used below amplitudes of 0.040 inch (1.02 mm).

3.2.2 Detection system checkout. With the shaker deenergized, the STU transducer shall be mounted face-to-face and coaxial with the PIND transducer using the recommended attachment medium. The STU shall be activated several times to verify low level signal pulse visual and threshold detection on the oscilloscope (approximately 20 millivolt peak or 10 millivolt peak above system noise).

NOTE: Not every application of the STU will produce the required amplitude but the majority of applications will do so.

3.2.3 System noise verification. For proper system operation, no extraneous noise can be permitted to exist in the system. During proper operation, the normal system noise, as observed on the oscilloscope, will appear as a fairly constant band and must not exceed 10 millivolts zero to peak. Extraneous noise is defined as noise in the system other than the permissible background noise that is present with no device on the transducer. Such noise can be due to a number of sources which must be eliminated or their effects guarded against, since those non-signal noise spikes can trigger the threshold detector and appear as signals on the other indicators. Common sources of external noise are fluorescent lighting, high voltage discharge and especially, less than optimum installation and support of the transducer cabling.

The latter source normally may be eliminated by redressing the cable, tightening or cleaning the connector at the transducer, or even replacing the transducer or transducer cable. To verify that no extraneous noise exists in the system, observe the oscilloscope while turning on the shaker and increasing the drive amplitude from zero to the desired acceleration level (see 3.1 c.) while applying the co-shock (see 3.3.4). This noise is usually present as pulses which remain in a fixed position on the oscilloscope trace. If extraneous noise is observed, correct the problem by shielding or other precautions, such as those suggested above and re-run the entire noise check.

3.3 Test sequence.

a. Pre-test shock.
b. Vibration 3-5 seconds.
c. Co-test shock.
d. Vibration 3-5 seconds.
e. Co-test shock.
f. Vibration 3-5 seconds.
g. Co-test shock.
h. Vibration 3-5 seconds.
i. Accept or reject.

3.3.1 Pre-test shock. Prior to vibrating the device, it shall receive a pre-test shock of 500 to 1500g (see 2.1).

3.3.2 Mounting requirements. Special precautions (e.g., in mounting, grounding of DUT leads, or grounding of test operator) shall be taken as necessary to prevent electrostatic damage to the DUT. All devices shall be mounted in an inverted position without adapters except for the following:

a. Stud-mounted devices shall be mounted in suitable adapters.
b. Axial diodes shall be mounted without adapters and with the leads in a horizontal plane.
c. Double-ended resistance welded packages (i.e., optical isolator) shall be mounted using a suitable adapter and with the leads horizontal. Most part types will mount directly to the transducer via the attachment medium. Parts shall be mounted with the largest flat surface against the transducer at the center or axis of the transducer for maximum sensitivity. When so mounted, the leads of the part will point up (e.g., TO-5) or horizontal (e.g., flat packs). Where more than one large surface exists, the one that is the thinnest in section or has the most uniform thickness shall be mounted toward the transducer, e.g., flat packs are mounted top down against the transducer. Small axial-lead, right circular cylindrical parts are mounted with their axis horizontal and the side of the cylinder against the transducer. Parts with unusual shapes may require special fixtures. Such fixtures shall have the following properties:

1. Low mass.
2. High acoustic transmission (aluminum alloy 7075 works well).
3. Full transducer surface contact, especially at the center.
4. Maximum practical surface contact with test part.
5. No moving parts.
6. Suitable for attachment medium mounting.

Leads on the parts shall be dressed, as necessary, so they will not strike each other or the transducer during vibration. Long or thin section leads shall be observed for signs of resonance, indicated by motion exceeding 3 or 4 diameters. Such resonance may give extraneous noise during test even though the leads do not strike each other. In these cases, the leads may have to be shortened (if permitted by the application) or special fixturing or frequency changes may be required.

NOTE: Some especially long-leaded TO-5 packages have been observed to be close to resonance at the test frequency.

3.3.3 Test monitoring. To avoid false indications, the DUT shall be inspected for any attached foreign matter or leads which are touching each other. The DUT shall be mounted on the center of the transducer using attachment medium and if

necessary, a mounting adapter. To provide maximum signal transmissibility with a viscous couplant, a sufficient amount of couplant shall be used and the DUT shall be firmly mounted so that any excess couplant can be squeezed out. When double-faced tape is used, it shall be changed at the start of a test group and after each 25 units or less thereafter. Devices shall be put on and removed from the attachment medium with a slight twisting motion. Device orientation for each package type shall be as specified in 3.3.2. The shaker input frequency shall be set in accordance with 3.1 b. and the shaker drive amplitude shall be increased to the level specified in 3.1 c. All detection systems shall be monitored for evidence of loose particles. Any device which gives a particle indication shall be considered a reject. Particle indications can occur in any one or combinations of the three detection systems as follows:

a. Visual indication of high frequency spikes which exceed the normal constant background white noise level.
b. Audio indication of clicks, pops, or rattling which is different from the constant background noise present with no DUT on the transducer.
c. Threshold detection shall be indicated by the lighting of a lamp or by deflection of the secondary oscilloscope trace.
d. If no particles are observed in 3 to 5 seconds, a co-test shock (see 3.3.4) shall be applied to the DUT while the shaker is operating. It is permissible to interrupt or perturb the vibration for a period not to exceed 250 milliseconds to provide for the application of an integral co-test shock. The audio, oscilloscope, and threshold detection systems are to be closely monitored during the time period immediately after each shock application as well as for an additional 3 - 5 seconds to detect particles which may lock up quickly. If no particles are detected with the first co-test shock application, the test shall be repeated two times. If there is no indication of particles within 5 seconds after the third co-test shock (see 3.3.4), the device is acceptable.

3.3.4 Co-test shock application. When using the copper rod shock tool (see 2.i.), the shock shall be applied to the DUT by bringing at least 1/4 to 1/2 inch of the free end of the shock tool into momentary contact with the vibrating DUT. The tool shall be held lightly and freely between the thumb and forefinger opposite the free end. Striking or hammering motions shall not be used. The shock shall be only the result of the mass inertia of the freely supported shock tool being struck by the vibrating DUT. The tool shall be held approximately horizontal and shall contact the DUT on a portion of the upper surface of its case. The duration of this contact is on the order of one-half second and results in several impacts of random shock to the DUT. The tool shall not contact the leads, other than minor accidental brushing of the leads along and parallel to their axis and shall not contact any glass portion of the case, except for all glass envelope diodes. If any other co-test shock device is used, its mode of operation shall be in accordance with procedures supplied by the equipment manufacturer. In systems that disable the threshold detector during the co-test shock, the period of time from shock pulse to reinitiation of threshold detection shall not exceed 100 milliseconds.

3.4 Failure criteria. Any noise bursts as detected by any of the three detection systems exclusive of background noise, except those caused by the shock blows, during the monitoring periods shall be cause for rejection of the device. Rejects shall not be retested (see 3.3.3) except for retest of all devices in the event of test system failure as provided in 3. If additional cycles of testing on a lot are specified, the entire test procedure (equipment set-up and checkout mounting, vibration, and co-shocking) shall be repeated for each retest cycle. Reject devices from each test cycle shall be removed from the lot and shall not be retested in subsequent lot testing.

4. SUMMARY. The following details shall be specified in the applicable detail specification:

a. Test condition letter A or B (see 2.d. and 3.1 c.).
b. Lot acceptance/rejection criteria (if applicable).
c. The number of test cycles, if other than one.
d. Attachment medium, if other than that specified (see 2.h.).
e. Pre-test shock level and co-test shock level, if other than specified in 2.i. and 2.i., respectively.

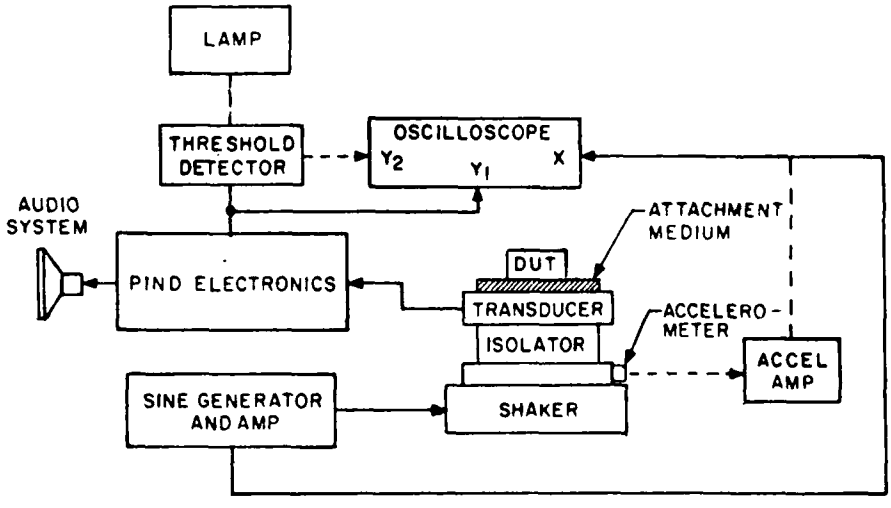


FIGURE 2020-1. Typical particle impact noise detection system.

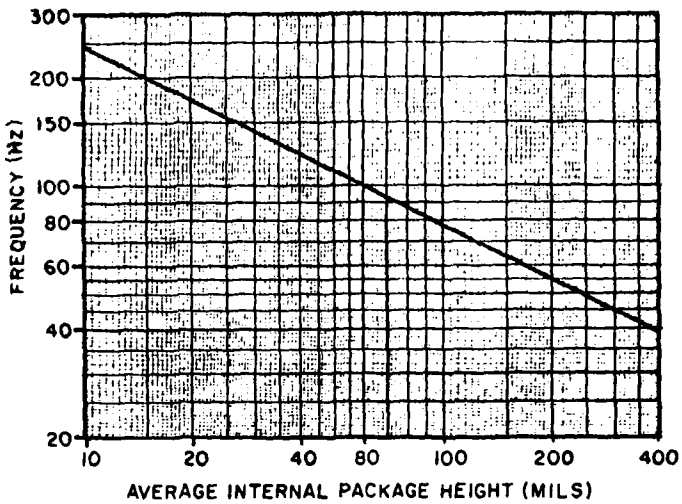
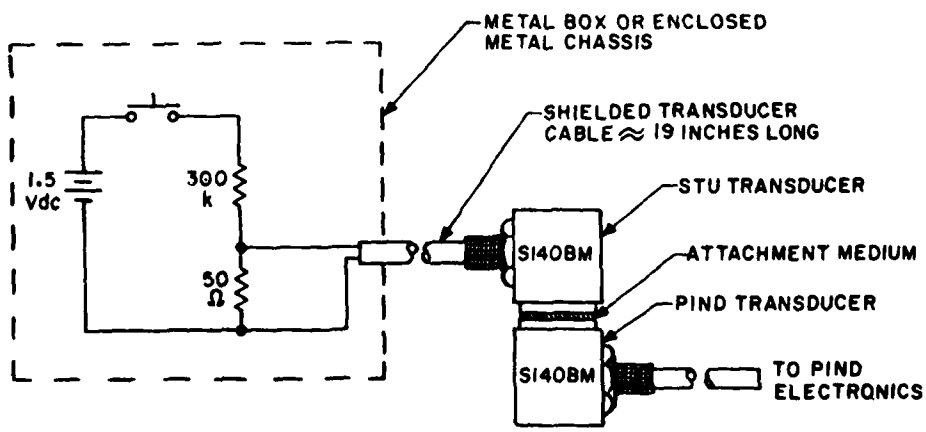
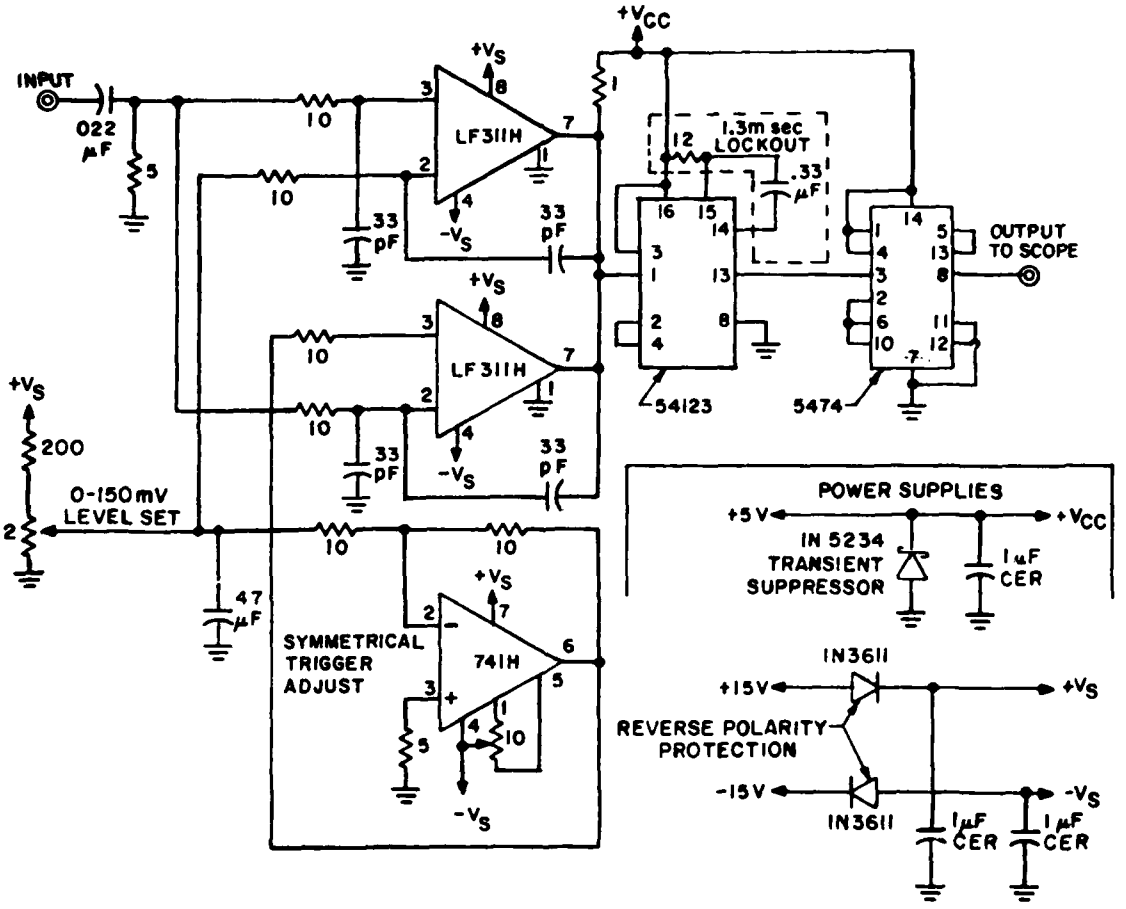


FIGURE 2020-2. Package height vs test frequency for 20G accleration (condition A).



NOTES:
1. Pushbutton switch: Mechanically quiet, fast make, gold contacts. E.G. T2 SM4 microswitch.
2. Resistance tolerance 5% non-inductive.
3. Voltage source can be a standard dry cell.
4. The coupled transducers must be coaxial during test.
5. Voltage output to STU transducer 250 microvolts, ±20%.

FIGURE 2020-3. Typical sensitivity test unit.



Resistance values are in kilohms unless otherwise specified.

FIGURE 2020-4. Typical threshold dectector schematic.

Figure 13 shows typical PIND equipment.

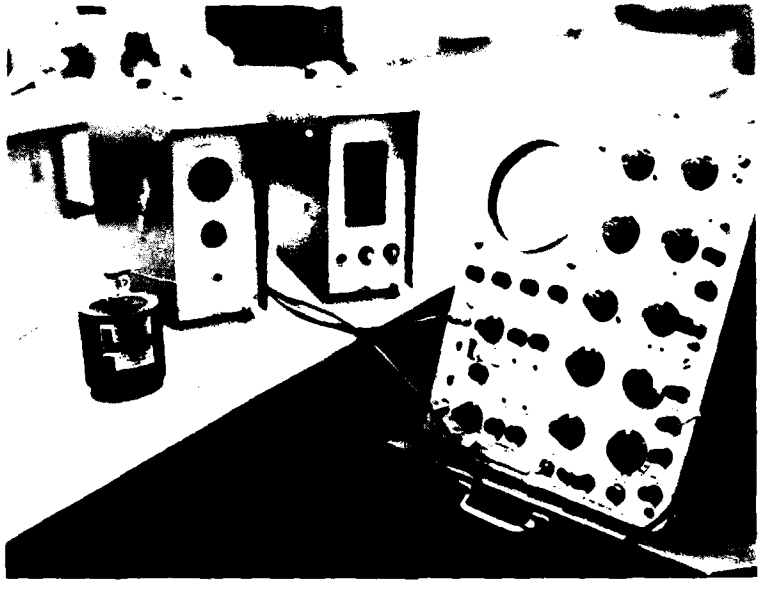


FIGURE 13. PIND EQUIPMENT

7. Pneumatic Impact Tester (Pneupactor). It has been reported that relatively high decelerations of comparatively short duration tend to excite resonant frequencies in microelectronic devices that can lead to failure of weak or improperly assembled devices. Such conventional screening methods as centrifuge testing do not normally detect these weaknesses.

Figure 14a shows one possible pneupactor apparatus set-up. Devices to be tested are loaded in specially made nylon projectiles. These projectiles are then accelerated down the tube, across a distance of approximately six (6) inches, and allowed to strike an aluminum striker plate. To prevent ringing from the impacted sample, a heavy (cast iron, for example) weight is fixed behind the striker plate.

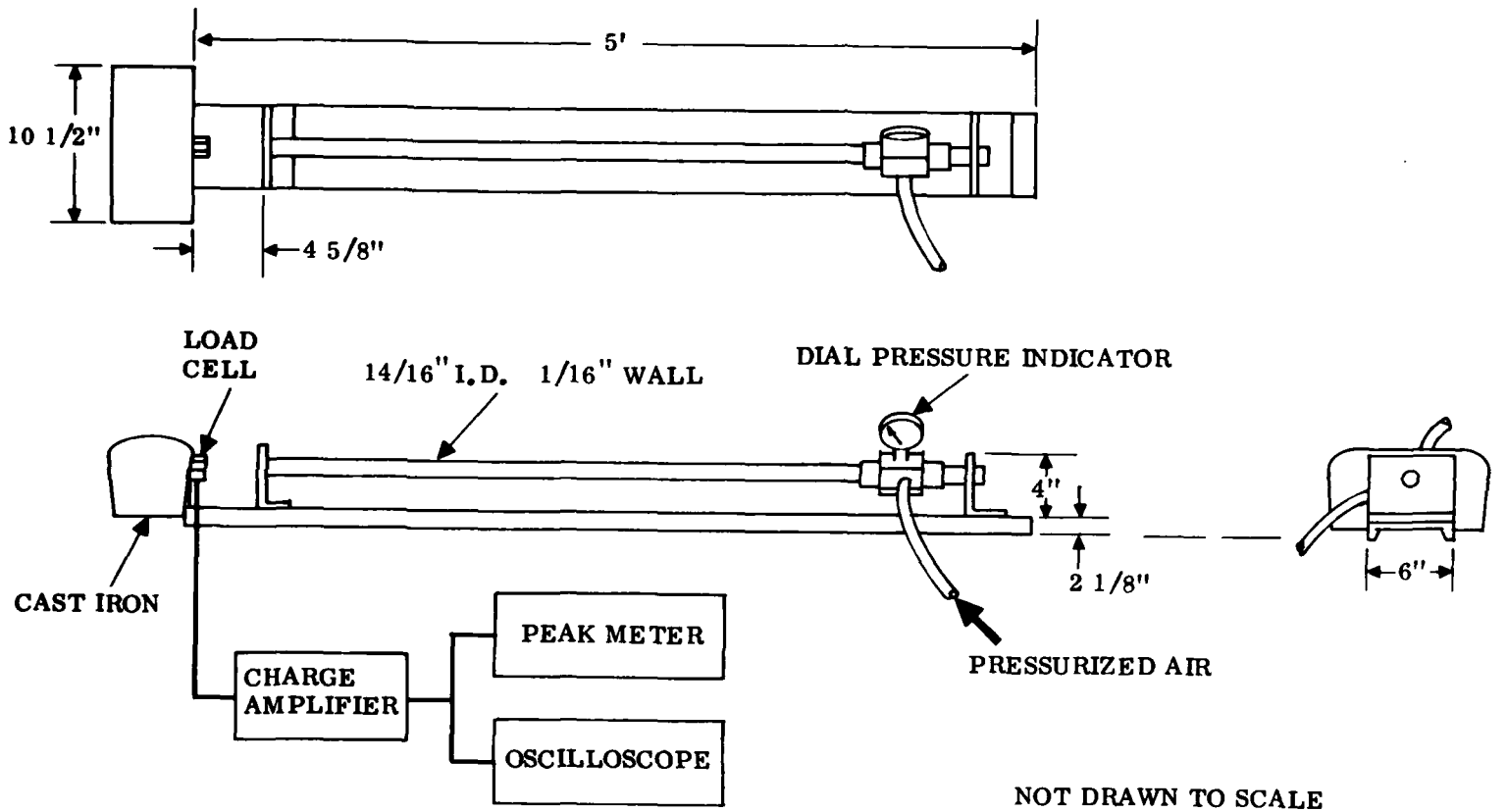


FIGURE 14. PNEUPACTOR APPARATUS

A piezoelectric quartz transducer (for instance, Kistler Model 912H, load cell) and a charge amplifier and peak meter (for instance, Kistler Model 593) can be used to measure the peak impact force upon impact. The load cell must be firmly attached to the impact plate (with, for instance, a beryllium - copper mounting stud).

In this setup, the peak meter registers only the peak signal from the charge amplifier. Therefore, to monitor ringing, an oscilloscope can be used to observe the output from the charge amplifier. If ringing should occur, the impact plate and the transducer mountings should be examined and adjusted for the closest possible physical contact.

A step-by-step procedure for calibrating the pneupactor and shocking a projectile is detailed below (Full details on calibration procedure can be obtained by consulting Reference 7):

- o Attach load cell to impact plate with Be-Cu stud.

- o Perform static calibration of charge amplifier:

  - Place impact plate with mounted load cell on a horizontal surface.

  - Using "T," connect both a Tektronics Model 454 oscilloscope (or equivalent) and peak meter to charge amplifier output.

  - With scope on "DC" mode, choose scope setting and charge amplifier range scale to measure a selected weight.

  - Set scope time base to 1 ms/div. or other suitable time base to display a shift in DC voltage level.

  - Set the charge amplifier time constant switch to "LONG," the polarity switch to "-", and the mode switch to "DC."

- Match a known weight to an appropriate charge amplifier range scale so that the full scale peak meter reading in lb/volt will be comparable to the expected deflection.

- For example, for a one-pound weight, set the transducer sensitivity to the lowest value provided by the manufacturer; set the range scale to 10 lb/volt (the range scale is divided by 10 if the transducer sensitivity is multiplied by 10); and set the scope sensitivity to 0.2 volt/cm. Choose an upper range scale, since it is more accurate than the lower scale. Place the weight on the load cell and allow enough time for thermal equilibrium to be established. Take the weight off the load cell and note the change in DC level of the scope trace. Adjust the charge amplifier gain so that a one-volt DC level shift is observed on the scope when the weight is taken off the load cell. Adjust the peak meter (zero and gain) so that it registers a one-pound force.

o Tighten tube mountings.

o Connect air hose to a continuous stream of air.

- Bolt the impact plate to the base and check during testing to be sure bolts are tight to prevent unwanted ringing.

- Attach 65 lb. cast iron block to impact plate with tapped hole in plate facing tube.

- Make electrical connections between the load cell, peak meter, and charge amplifier as shown in the Kistler manual.

- Select the proper transducer sensitivity from the calibration sheet accompanying the manual.

- Construct a three wall shock absorbent chamber to confine the rebounding particle.

- Set the charge amplifier range scale according to the peak force expected (see calibration curve in this report). Select the highest scale, if unsure of the peak force.

- Insert the circuit to be shocked into the proper projectile and hand-tighten the nylon projectile screw.

- Set the charge amplifier time constant switch to "short," the mode switch to "AC," and the polarity switch to "+."

- Zero the peak meter by pressing the reset button. If peak meter does not read "0," press button again.

- Set the air stream to the desired pressure on the dial pressure gauge.

- Insert the projectile into the tube end nearest the air jets and hand-release the projectile.

- Projectile will impact upon the load cell and be contained within the immediate vicinity of the load cell.

- Read the peak force in pounds off the peak meter and calculate:

$$\text{G-level} = \frac{\text{Peak force in pounds}}{\text{Weight of projectile in pounds}}$$

Figure 14b shows an improved pneumatic impact tester employing solenoid actuated has propelled projectile (nylon bullet device holder) for increased G-level impacts with reduced tube length.

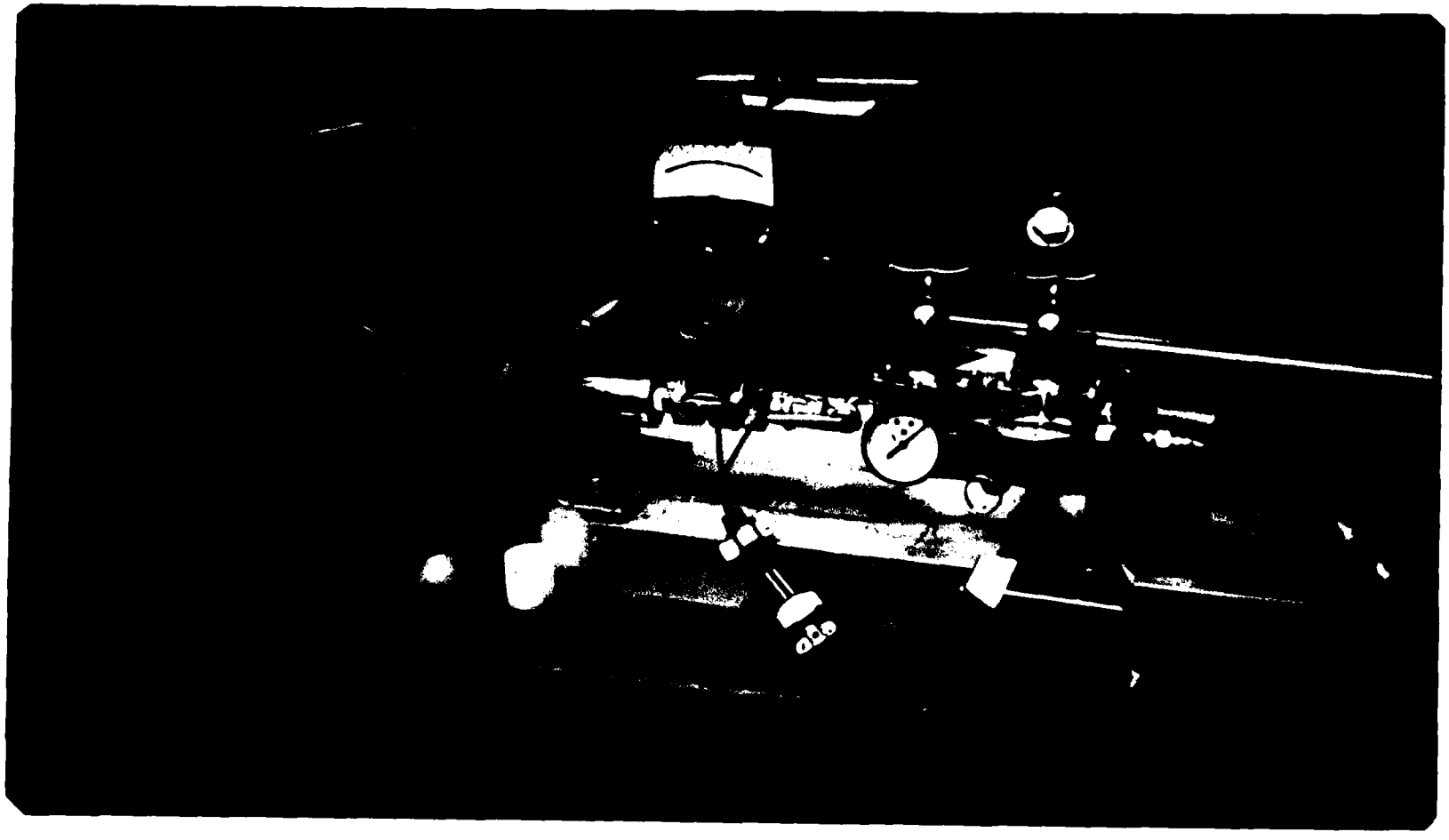


FIGURE 14b. PNEUMATIC IMPACT TESTER EMPLOYING SOLENOID ACTUATED GAS PROPELLED PROJECTILE (NYLON BULLET DEVICE HOLDER) FOR INCREASED G-LEVEL IMPACTS WITH REDUCED TUBE LENGTH

8. Package Stress Analysis. Microelectronic packages are routinely subjected to mechanical and thermal stresses in order to evaluate their strength and hermeticity. Some of the techniques used in evaluating electrical as well as mechanical properties of microelectronics are covered in Chapter III-A under Tests for Intermittent Failures. For example, vibration, shock, and centrifuge are covered in Chapter III-A.

A great deal of work has been done on the study of mechanical and thermal aspects of package integrity. More information can be found on this subject by consulting References 8, 9, and 10.

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9. Libove, C. "Rectangular Flat-Pack Lids Under External Pressure," RADC-TR-76-118, May 1976.

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EQUIPMENT

Ultrasonic Cleaning Equipment

1.	Buehler Ultramet Sonic Cleaners 50 watt unit, 1.3 liter	$135
2.	Fisher Ultrasonic Cleaner 100 watt unit, 2.8 liter	$150
3.	E/MC Ultrasonic Cleaner 40 watt unit, 473 ml Fisher Scientific Co., Pittsburgh, PA Cole Parmer, Chicago, Ill.	$ 68

Bond Pull Apparatus

1.	Stereo Zoom Microscope (See Chapter III-M)	
2.	X-Y Micromanipulator Movement Stage K & S Mfg. Co., Fort Washington, PA	$300
3.	Strain Gauge 5-50 Grams R. VanAlstine Tool Co., Schenectady, NY	$ 30
4.	Micropull III Bond Pull Tester Unitek Corp. Equip. Div., Monrovia, CA	$1500 - $3000

Wire Rebonding Apparatus

1.	Aluminum Wire Ultrasonic Bonder K & S Mfg. Co., Fort Washington, PA	$7000
2.	Gold Wire Ultrasonic Bonder Mech-ell Corp., Allentown, PA	$7000

L.

OPTICAL ANALYSIS TECHNIQUES

L. Optical Analysis Techniques.

1. Introduction. Optical analysis is perhaps the single most important and versatile tool available to the failure analyst. Most of the electrical and/or mechanical damage, either causing or resulting from a microelectronic failure, will be visible under some form of microscopic examination.

A broad range of types of optical equipment is necessary in failure analysis. Figures 1 and 2 provide a simple illustration of the truth of this statement. Figure 1 is a photograph of a 16K PROM taken at 8X magnification with a stereo microscope and Polaroid camera. Figure 1 shows that failure was due to a long piece of aluminum bonding wire loose inside the package cavity. Figure 2 shows nichrome fusible links at 600X magnification taken with a Nikon microscope with Polaroid camera attachments. Neither of the two microscope outfits used to produce Figures 1 and 2 is capable of producing both views. For instance, if only the high magnification microscope used for Figure 2 were available, it would have been much more difficult to locate the wire shown in Figure 1 because of the reduced area of view and shallow depth of field.

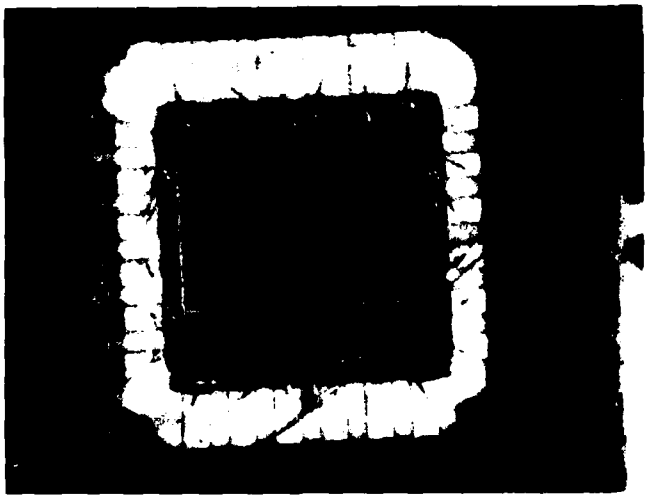


FIGURE 1. 16K PROM ELECTRICAL TEST FAILURE IN A CERAMIC PACKAGE WITH THE LID REMOVED. ARROW SHOWS THE CAUSE OF FAILURE TO BE A LOOSE ALUMINUM BONDING WIRE.

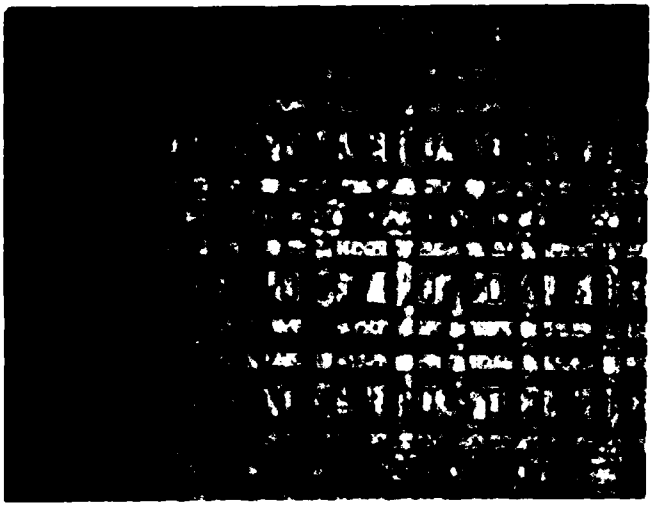


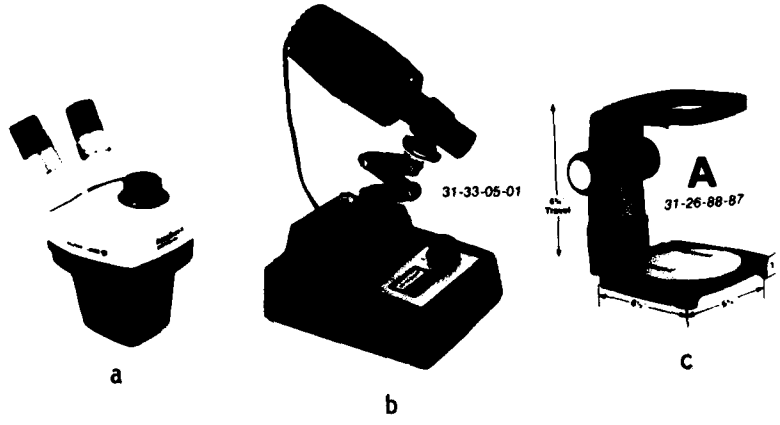
FIGURE 2. 600X MAGNIFICATION VIEW OF THE INTERNAL CELLS OF 16K PROM IN FIGURE 1. ARROWS POINT TO OPEN NICHROME LINKS.

2. Microscope Components. A microscope in its basic form consists of three elements: a magnifying system, a light source, and a viewing stage. Figure 3 demonstrates these three components for a stereo zoom microscope. As magnification increases and the more exotic microscope attachments are added, the complexity of the total system increases dramatically.

Brief descriptions of the three major microscope elements are listed below.

a) Magnification System. The magnification system consists of a number of individual components.

- Objective Lenses. The objective is the lens used closest to the sample under observation. These lenses are generally considered to be the most important part in the magnification system.



(a) MAGNIFYING SYSTEM, (b) LIGHT SOURCE and (c) VIEWING STAGE

FIGURE 3. BASIC COMPONENTS OF A MICROSCOPE SYSTEM.

Objective lenses are classified as:

- Achromatic: corrected for two colors, usually red and green
- Apochromatic: corrected for three colors, usually red, green, and violet
- Non-Achromatic: not corrected for any colors and yield color halos in the image they form

Other important properties of objective lenses are:

- Magnifying power: this number is generally printed on the side of the lens, and is the numerical value of lens magnification.

- Numerical Aperture Rating: This number is generally printed on the side of the lens, and it is a measure of the fineness of detail the lens can resolve. The higher this number, the greater the resolving power of the lens.
- Focal Length: The distance between the objective and the sample when the image is in focus. This property is especially important when integrated circuit chips are to be inspected at high power when still mounted in packages.

o Field Lens. This is the lens installed between the objective lens and the viewing eyepieces. It is often adjustable with typical values of 1.0, 1.25, 1.5, 2.0.

o Eyepieces. Eyepieces can be classified into three categories:

(a) Negative: Huggenian
(b) Positive: Ramsden
(c) True Negative: Amplifying

The magnification number is marked on the side of the eyepiece. A close approximation of the total microscope magnification power can be obtained by multiplying:

$$M_{TOTAL} \cong M_{OBJECTIVE} \times M_{FIELD\ LENS} \times M_{EYEPIECE}$$

b) Light Sources. There are a great many types of illumination sources available for use in microscopy. Table I lists technical data on several of the lamp types available.

TABLE I

TECHNICAL DATA OF TYPICAL LAMPS SUITABLE FOR MICROSCOPY ILLUMINATION

Lamp Type	Lamp Electrical	Approximate Color Temp (°K)	Approximate Life (hrs)
Low-Voltage	6V - 10W	~3300	50
Lamps	12V - 50W	~5500	50
	12V - 100W	~5500	50
Zenon	12V - 250W	~4500-5900	1200
Mercury Vapor Lamp	12V - 100W	~5000	200
Cesium-Iodide	12V - 250W	~4500	80

For work with stereo zoom type microscopes, the choice of an illumination source is largely a matter of personal preference. However, as microscope complexity increases, the more powerful sources become a necessity. For instance, the addition of Nomarski or other types of phase contrast optical systems to metallurgical microscopes requires much more light than simple incident light systems in the low wattage range are capable of providing. In addition, the use of color-correcting filters for photography will make the higher power light sources necessary.

c. Viewing Stages. Viewing stages are the simplest major component of a microscope. Stages are available from the simplest, as shown in Figure 3, to the more complex ones available for specific types of microscopes (see examples under specific type of microscope).

In general, there are two major types of stages: the regular and inverted stages. Inverted stages are most often used in metallographic work, where the sample area of interest can be placed face down on the flat surface of the stage. Regular stages are more common in general failure analysis work, where it may not be possible

or advisable to turn the sample upside down. For instance, the wire found inside the package shown in Figure 1 would have been lost if the package had been turned upside down.

Stages with X, Y, and rotational degrees of freedom are available, with the X-Y movement stages being the most popular. Stages that can be moved by hand in three degrees of freedom are useful, particularly when viewing samples under relatively low power stereo microscopes.

3. Types of Microscopes. Table II provides a listing of some of the types of microscopes and attachments available. Following Table II are more detailed discussions and examples of these various types of optical instruments and techniques in using them.

TABLE II

GENERAL INFORMATION ON MICROSCOPES

Microscope Type and Attachments	Magnification Range	Description and Use
Stereo	0.7 - 160X	Low power, large working distance, wide field, 3-dimensional viewing. Used to examine macro aspects of packages, for instance.
a. Photographic Attachments		Polaroid camera equipment is generally used with this microscope.
Metallurgical	25 - 1500X	Probably the most versatile microscope available for microelectronic work. Most commonly used with bright field incident illumination. Several special purpose attachments available.
Dark Field		Directs light along an acute angle so that surface irregularities are revealed.
Differential Interference Contrast System		Attachment which uses prisms and polarized light to produce colors that accentuate differences in sample surface topography.

TABLE II

GENERAL INFORMATION ON MICROSCOPES (CONT'D)

Microscope Type and Attachments	Magnification Range	Description and Use
Transmitted Light Source		"Bottom" illumination that allows light to be transmitted through optically transparent samples; for instance, silicon-on-sapphire samples.
Projection Screen		Useful chiefly for instructional purposes.
Field-of-View Diaphragm		Useful in excluding all light except that around area of interest.
Filters		Useful in enhancing resolution and in eliminating detrimental wavelengths of light in photography work.
Photographic Accessories		Polaroid and 35 mm cameras are available. Automatic shutter control devices are common.
Revolving Turret(multi-Objective)		Allows a change of magnification by changing objective lenses without changing focal distance.
Polarizing System		Uses two rotating polarizing filters that will highlight surface irregularities and defects.
Filar Eyepiece		Used to make linear measurements over the complete magnification range based on calibration with a stage micrometer. NOTE: Metallurgical microscopes are available with either regular or inverted stages.
Polarizing	50 - 700X	Useful in highlighting topographical features and strain areas.
Interferometer	25 - 500X	Uses monochromatic light source (such as sodium or thallium vapors) to produce interference fringes with which heights and thin film thicknesses can be measured over the range of 30 - 20,000 Å.

TABLE II

GENERAL INFORMATION ON MICROSCOPES (CONT'D)

Microscope Type and Attachments	Magnification Range	Description and Use
Hole Inspection	5 - 200X	Utilizes large working distance lenses so that holes through, for instance, printed circuit boards can be inspected.
Dimensioning	50 - 200X	Useful in measuring length, angle, profile, height, and shape of objects through precision stage movement.
Digital Unit		Available for precision measurements to 1 μm.
Infrared	50 - 200X	Generally used to examine bulk aspects of materials, such as silicon, which are transparent to infrared wave lengths, and in detecting local areas of high power dissipation.
Light Section	50 - 200X	Used to measure films greater than 1 μm in thickness.

a. Stereo Microscopes. Stereo microscopes are wide field, generally low power, long working distance microscopes that are available either with or without zoom capability. Figure 4 shows a typical stereo microscope.

Figure 5 shows the light path through a stereo microscope, and Table III gives typical optical data for a stereo microscope.

These illustrations and Table III in particular demonstrate the usefulness of the stereo microscope in failure analysis. The combination of low magnification, long working distance, and 3-dimensional image allows microcircuits to be examined for gross damage, such as package pin damage, broken or loose bonding wires,

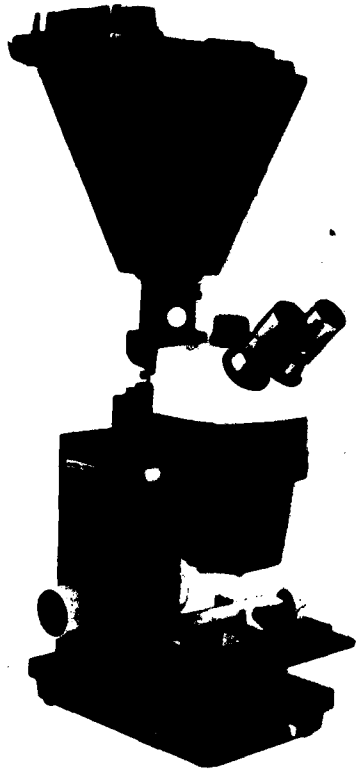


FIGURE 4. TYPICAL ZOOM STEREO MICROSCOPE WITH POLAROID CAMERA ATTACHMENT

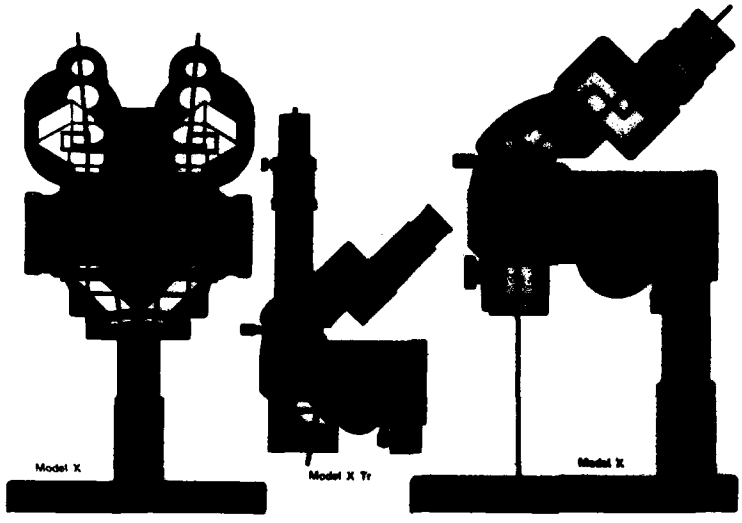


FIGURE 5. LIGHT PATH THROUGH A TYPICAL STEREO MICROSCOPE

TABLE III

OPTICAL DATA FOR A TYPICAL STEREO MICROSCOPE

Objectives	Working Distance	Eyepieces			
		G10X		G20X	
		Magnification	Field of view	Magnification	Field of view
1X	86 mm (3.39")	6.3X	32 mm (1.26")	12.6X	16.0 mm (0.63")
		10X	20 mm (0.79")	20X	10.0 mm (0.39")
		16X	12.5 mm (0.49")	32X	6.25 mm (0.25")
		25X	8.0 mm (0.31")	50X	4.0 mm (0.16")
		40X	5.0 mm (0.20")	80X	2.5 mm (0.10")
2X	45 mm (1.77")	31.5X	6.3 mm (0.25")	63X	3.15 mm (0.12")
		50X	4.0 mm (0.17")	100X	2.0 mm (0.08")
		80X	2.5 mm (0.10")	160X	1.25 mm (0.05")

foreign matter inside a package cavity, etc. As Table III shows, even at relatively high magnifications, the working distance can be 45 mm (1.77 inches). This versatility of the stereo microscope makes it an extremely valuable tool in failure analysis.

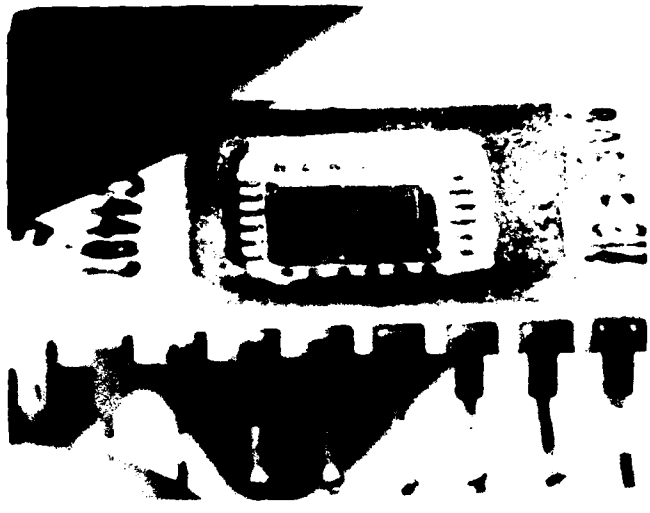
Figure 6 demonstrates the combination of high magnification range and large working distance. Figure 6a shows a microcircuit photographed at 4X, and Figure 6b shows a 120X photograph of a small area on the microcircuit.

b. Metallurgical Microscopes. These microscopes are by far the most versatile ones available to the failure analyst. The attachments available for the metallurgical microscope provide a broad range of versatility. These microscopes are available with either a regular or an inverted stage. The inverted stage microscope is most commonly used in metallurgical cross sectioning work, while the regular stage microscope is more common in general failure analysis. Figure 7 shows typical inverted stage and regular stage metallurgical microscopes that are available.

Figure 8 shows light paths through the inverted and regular stage metallurgical microscopes.

Microelectronic circuits can be examined while still mounted in most types of packages. However, one problem that the failure analyst frequently encounters with the metallurgical microscope is the generally short working distance between objective lens and sample. For instance, magnifications of 500 - 700X are required to adequately examine the metallization patterns on LSI circuits, and the working distance at that magnification is frequently insufficient to focus on a mounted sample.

Figure 6a gives some idea of the depth of field necessary to focus on the LSI microcircuit mounted in the ceramic package. Not all microscope objectives are capable of sufficient working distance



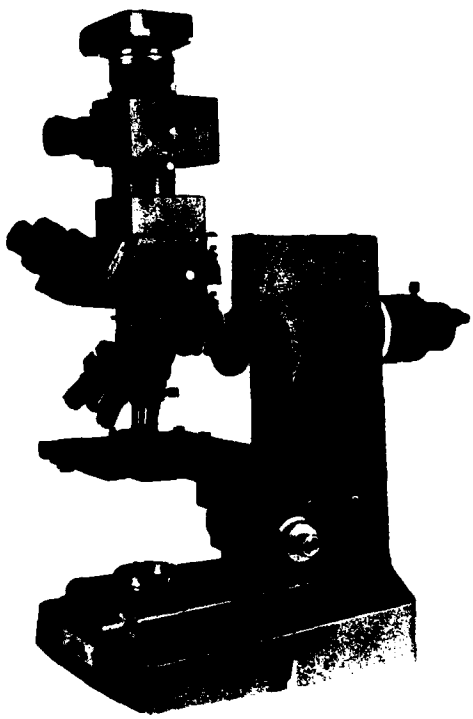
a. STEREO MICROSCOPE PHOTOGRAPH TAKEN AT 4X

b. STEREO MICROSCOPE PHOTOGRAPH TAKEN AT 120X

FIGURE 6. DEMONSTRATION OF STEREO MICROSCOPE VERSATILITY IN WORKING DISTANCE AND MAGNIFICATION RANGE

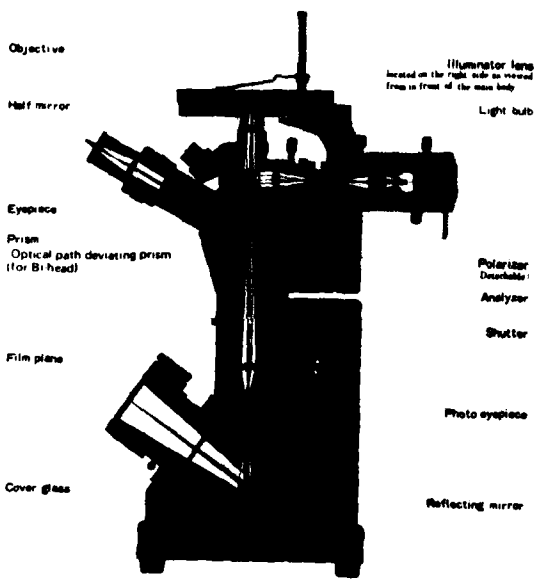
a. INVERTED STAGE METALLURGICAL MICROSCOPE

FIGURE 7. TYPICAL METALLURGICAL MICROSCOPES (SHEET 1 OF 2)

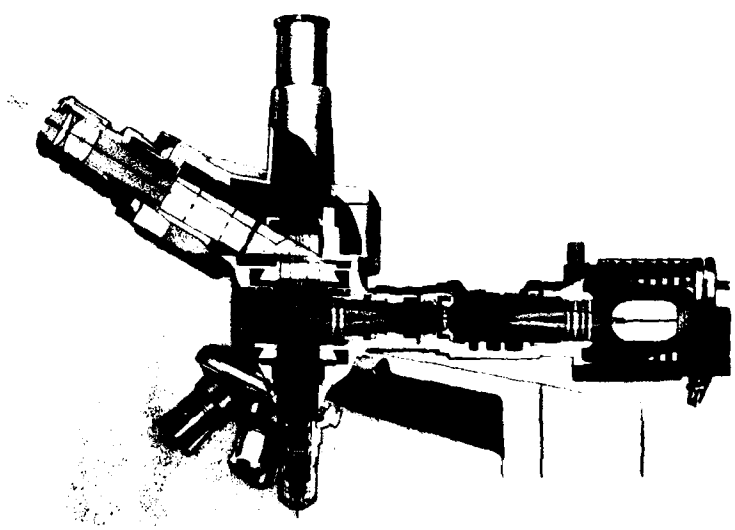


b. REGULAR STAGE METALLURGICAL MICROSCOPE

FIGURE 7. TYPICAL METALLURGICAL MICROSCOPES (SHEET 2 OF 2)



a. LIGHT PATH THROUGH INVERTED STAGE METALLURGICAL MICROSCOPE



b. LIGHT PATH THROUGH REGULAR STAGE METALLURGICAL MICROSCOPE

FIGURE 8. LIGHT PATHS THROUGH TYPICAL METALLURGICAL MICROSCOPES

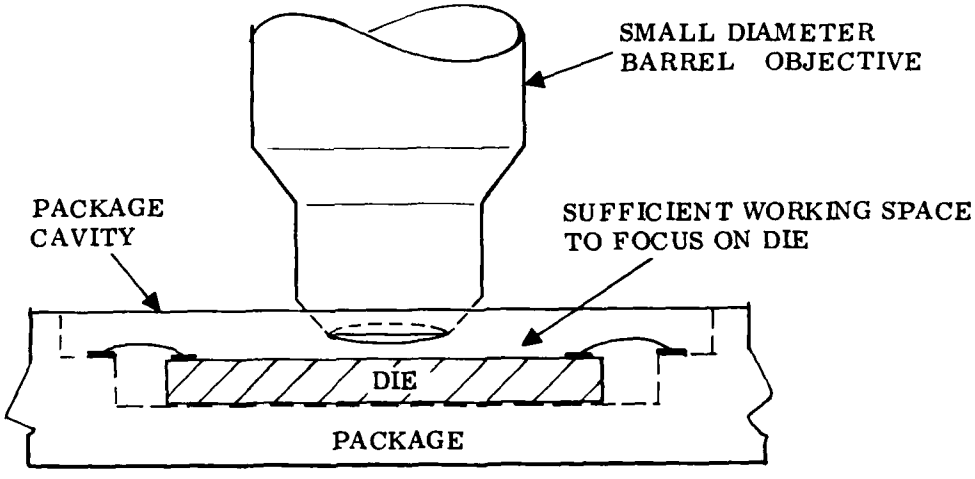
to focus within the package cavity. This is due in large part to the physical construction of some objective lenses. That is, objective lenses with larger diameter barrels tend to be flatter on the surface toward the sample and, therefore, often come into physical contact with the package surface before coming into focus on the microcircuit. Figure 9 diagrammatically demonstrates this problem.

Table IV gives some examples of typical working distance and magnification of objectives used in several of the attachments available for the metallurgical microscope. It should be noted that objectives with longer than normal working distance are available, and might be considered desirable by the failure analyst.

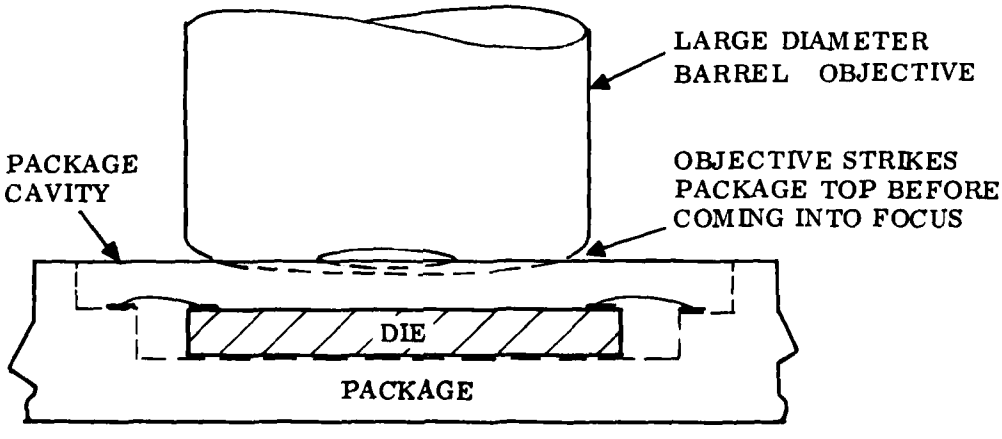
TABLE IV

WORKING DISTANCE AND MAGNIFICATION OF TYPICAL OBJECTIVES AVAILABLE FOR THE METALLURGICAL MICROSCOPE

Type	Initial Magnification	Numerical Aperture	Free Working Distance
Achromat	M5X	0.10	27.0mm
	M10X	0.25	7.6
	M20X	0.40	2.1
	M40X	0.65	0.5
	M100X (oil)	1.30	0.35
Plan Achromat	M Plan 1.3X*	0.03	48.99
	M Plan 2.5X*	0.05	42.0
	M Plan 5X	0.10	3.3
	M Plan 10X	0.25	7.1
	M Plan 20X	0.40	0.72
	M Plan 40X	0.63	0.39
	M Plan 100X (dry)	0.90	0.29
	M Plan 100X (oil)	1.25	0.16
Plan Achromat (long working distance)	LWD M Plan 20X	0.40	4.60
	LWD M Plan 40X	0.55	3.42
Metallurgical Darkfield Achromat	Neo 5X	0.10	22.3
	Neo 10X	0.25	7.5
	Neo 20X	0.40	1.7
	Neo 40X	0.65	0.62
Differential Interference Contrast Plan	M Plan 5X-N	0.10	2.65
	M Plan 10X-N	0.25	6.93
	M Plan 20X-N	0.40	0.68
	M Plan 40X-N	0.65	0.38
	M Plan 100X-N	0.90	0.29



a. SMALLER DIAMETER OBJECTIVE LENSES GENERALLY HAVE SUFFICIENT WORKING DISTANCE TO FOCUS ON MICROCIRCUITS MOUNTED IN PACKAGES, BUT AT THE EXPENSE OF RESOLVING POWER (MAGNIFICATION) *



b. LARGE DIAMETER OBJECTIVES OFTEN STRIKE THE PACKAGE BEFORE THE LENS IS BROUGHT INTO FOCUS

FIGURE 9. DIAGRAMMATIC REPRESENTATION OF LARGE VERSUS SMALL BARREL OBJECTIVE LENS FOCAL LENGTHS

*See Reference 12, p. 17.

Some of the typical defects the failure analyst might use the metallurgical microscope to examine are:

(a) Broken or missing wire bonds
(b) Metallization defects such as microcracks, discontinuity, missing areas, overalloy, etc.
(c) Oxide defects
(d) Evidence of electrical overstress
(e) Evidence of overheating

Some of the techniques which the metallurgical microscope and its attachments make available to failure analysis work are described below:

o Bright Field or Vertical Illumination*. This type of illumination is most commonly used with the metallurgical microscope. Figure 10 shows the light path through the objective lens when bright field incident illumination is used, and Figure 11 shows a typical bipolar integrated circuit when viewed under bright field illumination. It should be noted that the sample must be normal to the optical axis.

o Oblique Illumination. Surface detail can often be more easily revealed with the use of oblique illumination from a portable light source. For instance, the light source shown in Figure 3 would be suitable for use in oblique lighting. Figure 12 shows an oblique illumination photograph of the same bipolar integrated circuit shown in Figure 11. The enhanced surface detail is readily obvious.

o Dark Field Illumination. In this form of illumination, light is fed from the objective lens to the sample at an acute angle, so that most of the light is reflected away from the microscope.

*As opposed to "side" illumination generally used with stereo microscopes.

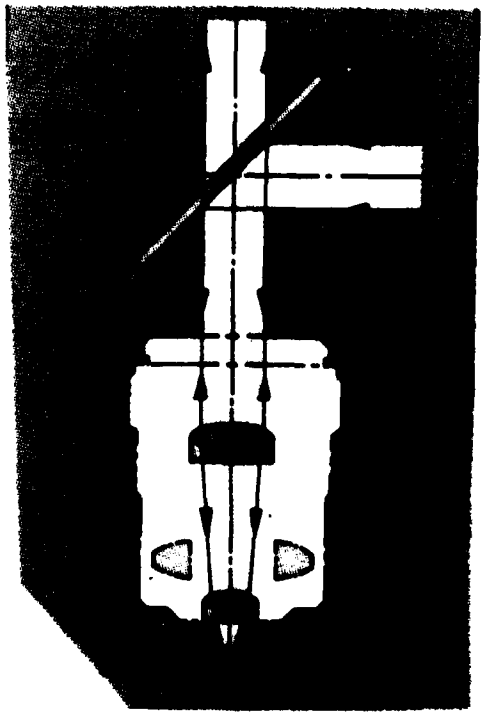


FIGURE 10. LIGHT PATH THROUGH OBJECTIVE LENS AT CONDITIONS OF BRIGHT FIELD ILLUMINATION

FIGURE 11. BIPOLAR INTEGRATED CIRCUIT VIEWED UNDER CONDITIONS OF BRIGHT FIELD ILLUMINATION

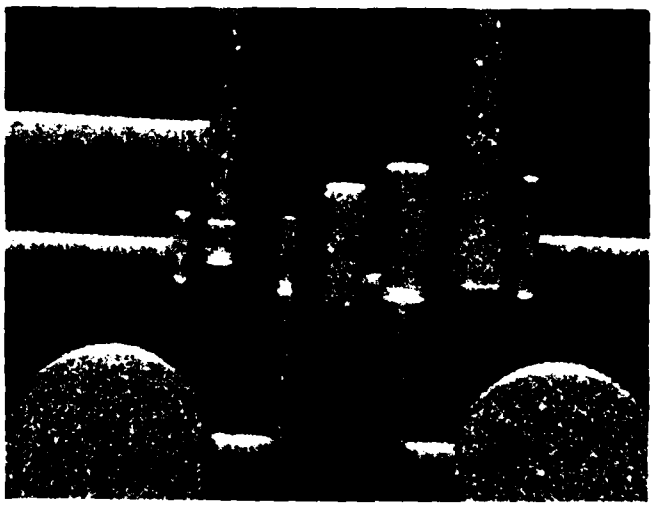


FIGURE 12. BIPOLAR INTEGRATED CIRCUIT VIEWED UNDER CONDITIONS OF OBLIQUE ILLUMINATION

Figure 13 shows the light path in dark field illumination.

Only light which strikes a protrusion or recession is reflected back into the objective lens. Holes or protrusions that show up as shadows under Bright Field Illumination will appear white against a dark background in Dark Field conditions.

Dark Field viewing, therefore, allows the failure analyst to accentuate surface irregularities that would not normally be visible in other lighting conditions. Figure 14 shows a Dark Field view of the bipolar integrated circuit shown in Figures 11 and 12.

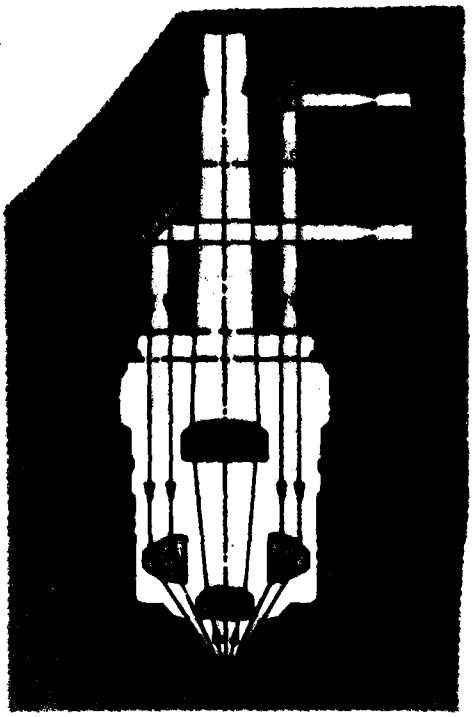


FIGURE 13. LIGHT PATH UNDER CONDITIONS OF DARK FIELD ILLUMINATION

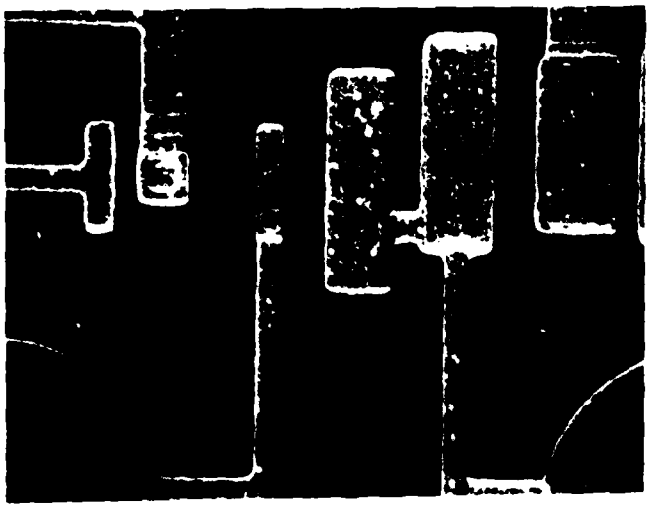


FIGURE 14. BIPOLAR INTEGRATED CIRCUIT VIEWED UNDER CONDITIONS OF DARK FIELD ILLUMINATION

o Differential Interference Contrast Systems. These systems employ a polarized light field which is then passed through a system of prisms. A display of colors accentuating surface contours is produced by rotating the prisms relative to the beam of polarized light.

The image produced by this interference contrast system is characterized by a definite relief effect and a shallow depth of field. The image is apparently three-dimensional in nature, and the recombination and interference produced by the beam splitting create a shadow effect. The shallow depth of field adds to the three-dimensional effect of the image.

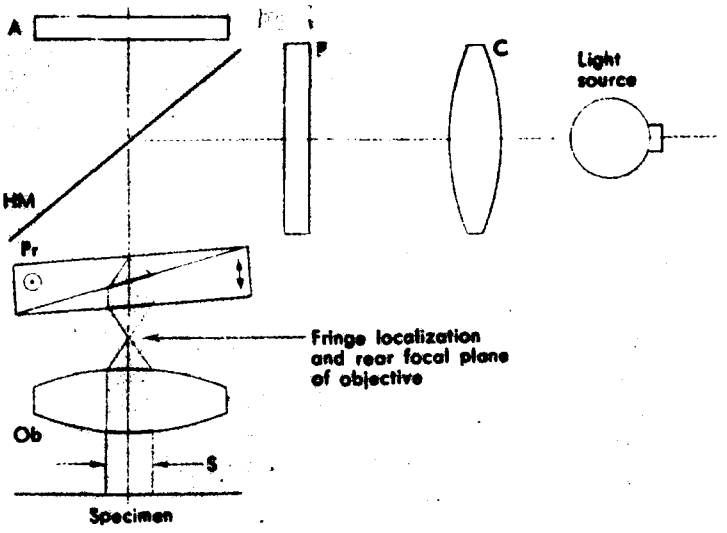
Figure 15 demonstrates the Nomarski type interference contrast system for transmitted light.

Figure 16 is a photograph of the bipolar integrated circuit shown in Figures 11, 12, and 14 using Nomarski interference system optics using reflected light.

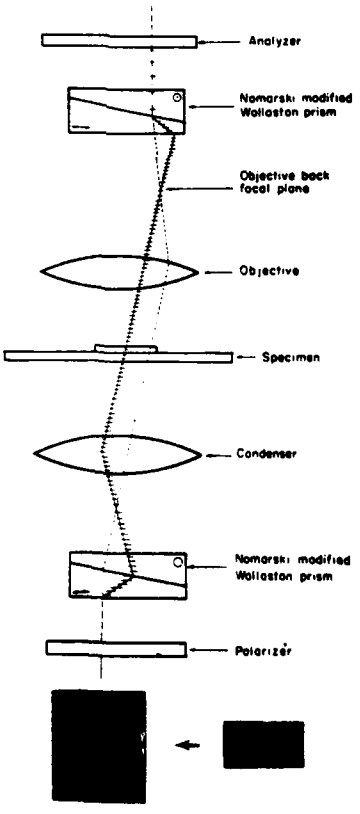
Care must be used in interpreting the image produced by this optical system. The apparent three-dimensional image is not a true and accurate representation of the sample. For instance, a "protrusion" may well not be an actual protrusion but might possibly be either an optical discontinuity in a flat film or a depression.

The differential interference contrast system is a two-beam instrument just as are other interference systems. It is, however, not a quantitative instrument because there is no visible separation of what would be a "reference beam" and a "specimen beam" as in, for instance, a Michelson-type interference microscope.

Differential interference contrast systems do produce interesting and effective images and are gaining a great deal in popularity over polarized light systems.



a. REFLECTED LIGHT OPTICS



b. TRANSMITTED LIGHT OPTICS

FIGURE 15. LIGHT PATH THROUGH NOMARSKI TYPE INTERFERENCE CONTRAST SYSTEMS

FIGURE 16. BIPOLAR INTEGRATED CIRCUIT VIEWED UNDER NOMARSKI INTERFERENCE CONTRAST OPTICAL SYSTEM USING REFLECTED LIGHT

o Transmitted Light Source. This method of illumination is not commonly used in most failure analysis work simply because most of the microelectronic packages and die encountered are opaque to transmitted light. However, revealing images are produced if transmitted light is used in examining silicon-on-sapphire circuits mounted in ceramic packages.

Figure 17 is a photograph of a silicon-on-sapphire logic cell taken using transmitted light.

Figure 18 shows a typical transmitted light microscope and the light path used.

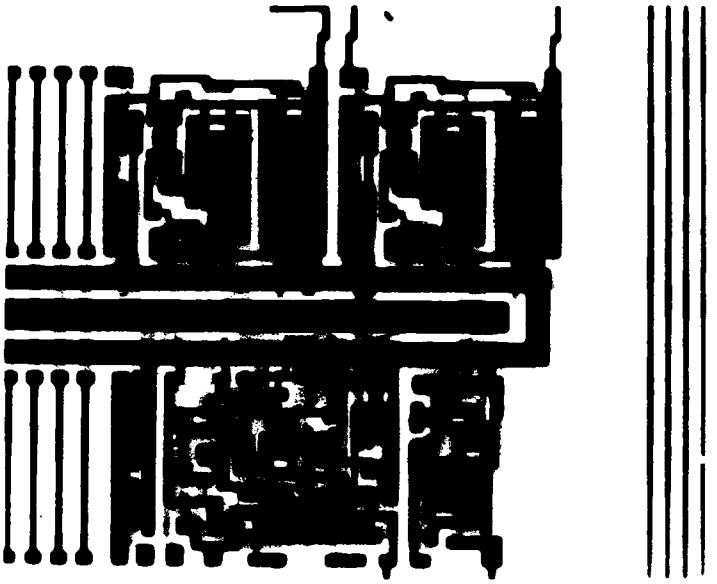


FIGURE 17. SILICON-ON-SAPPHIRE LOGIC CELL PHOTOGRAPHED USING TRANSMITTED LIGHT

o Projection Screen. The projection screen is a convenience chiefly when used as a teaching aid, so that several people at once can view a magnified image. It finds a great deal of use in semiconductor photomask inspection operations but is not often used in failure analysis.

Figure 19 shows an inverted stage metallurgical microscope equipped with a viewing screen. The light path in this form of instrument is the same as that shown in Figure 8a.

o Field View Diaphragm. This accessory for the metallurgical microscope is generally an integral part of the microscope illuminator. The diaphragm can be closed from its normally fully open position to reveal only a small area of interest on a microcircuit. Limiting the field of view to a small area in this way is useful, for instance, in teaching and in exhibiting small areas of interest in failure analysis reporting.

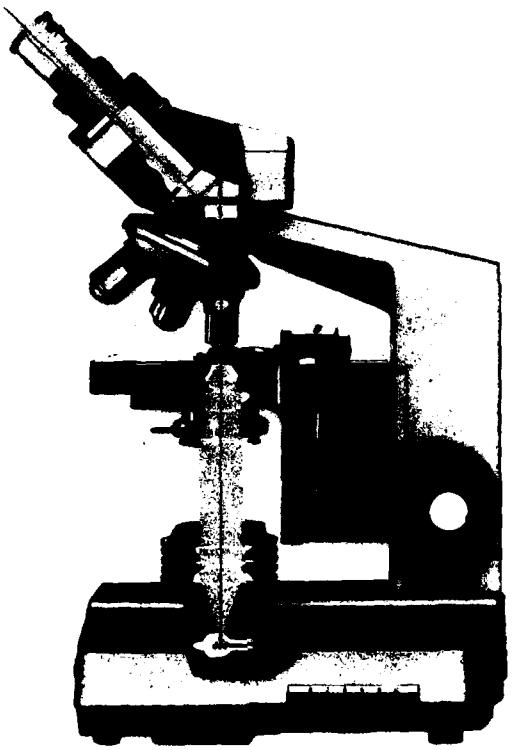


FIGURE 18. TYPICAL TRANSMITTED LIGHT MICROSCOPE AND LIGHT PATH

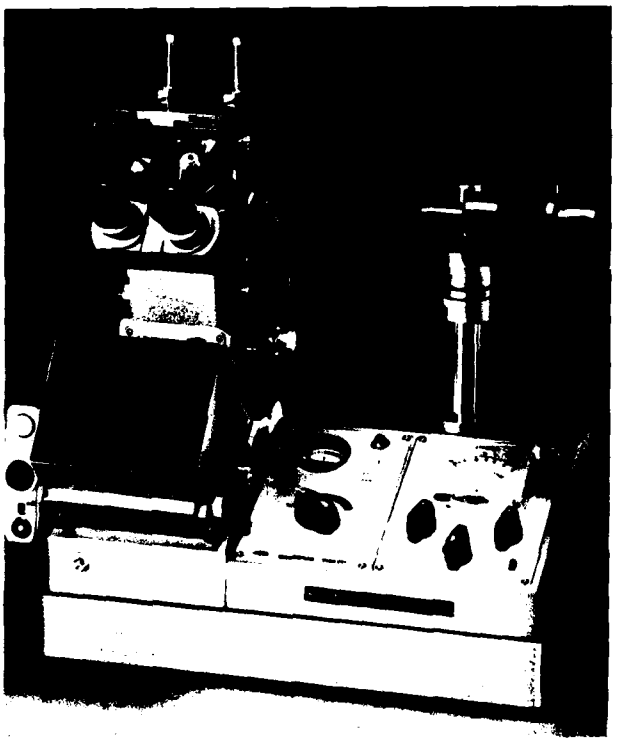


FIGURE 19. TYPICAL INVERTED STAGE METALLURGICAL MICROSCOPE WITH PROJECTION SCREEN

Figure 20 displays a small area of a bipolar integrated circuit.

o Filters. Various types of filters are either an integral part of the illuminator system for metallurgical microscopes or slots are usually provided for their insertion in the light path from the light source.

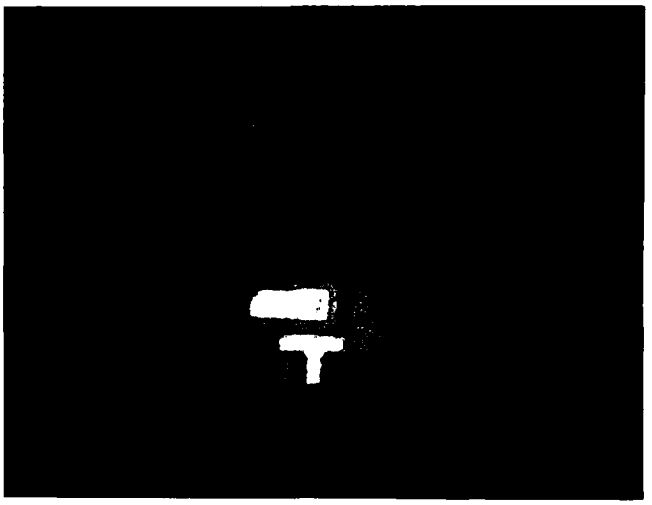


FIGURE 20. SMALL AREA OF BIPOLAR INTEGRATED CIRCUIT HIGHLIGHTED THROUGH USE OF FIELD OF VIEW DIAPHRAGM

In general, light filters are used in microscopy work for the following purposes:

(a) To improve image resolution
(b) To insure proper color identification
(c) To increase contrast
(d) To reduce glare and discomfort in viewing
(e) To reduce light intensity
(f) To cool the light beam (remove infrared heating effects)
(g) To alter or control spectral emission for photographic purposes

o Photographic Accessories. Proper attachments to fit either Polaroid or 35 mm film cameras are available for almost all metallurgical microscopes for photographic work. Photomicrography is an immensely complex subject and is unquestionably an artform unto itself (see the sections on Photomicrography, Photomacrography, and Photographic Films and Camera Systems for more details).

o Revolving Turret. The lengths of objective lenses and, therefore, the placement of the optical lens elements inside, are designed by manufacturers so that the objectives can be changed by means of a revolving turret without coarse refocussing. A set of lenses with this characteristic is called parfocal, and such a set is generally found on metallurgical microscopes in every failure analysis laboratory. Reference to illustrations of any metallurgical microscope will demonstrate the revolving turret.

o Polarizing System. Most metallurgical microscopes on the market can be fitted with two rotating polarizer plates to produce images which highlight surface characteristics and differences (see Polarizing Microscope).

o Filar Eyepiece. (See Dimensioning Microscope and Chapter III-J, paragraph 6.a, page III-J-7.)

c. Polarizing Microscope. Polarizing microscopes are generally used for transmitted light studies rather than for incident light studies. When polarized light is used in the incident light mode, it is most often used in crystallography studies rather than in general failure analysis.

More recently, however, new liquid crystal work is finding uses for polarized light in conjunction with dynamic operation of integrated circuits (see Chapter III-I).

d. Interferometer Microscopes. Interferometer microscopes are commonly used to measure film thicknesses in the range of 30 - 20,000Å. Film thicknesses are occasionally measured by the interferometer in failure analysis, but the equipment is more commonly used during semiconductor processing and during Destructive Physical Analysis (DPA).

For details on theory of interferometry and information on the types of interferometry, see Chapter III-J, paragraph 3. on page III-J-2.

Figure 21 shows typical interferometer equipment.

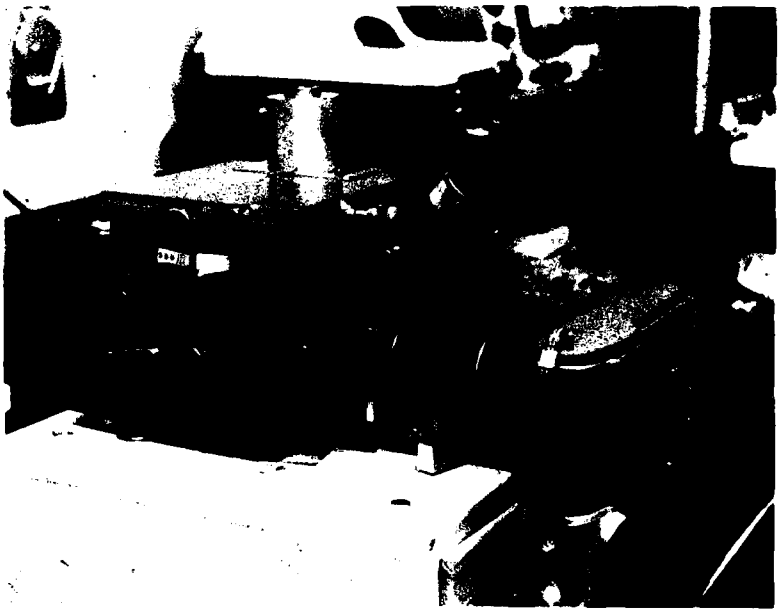


FIGURE 21. TYPICAL INTERFEROMETER EQUIPMENT

To use the interferometer in measuring film step heights, it is necessary to have sufficient slope at the step to be able to count the fringes across the step or else the measurements will be inaccurate. Some of the film heights that might be measured in failure analysis are:

- Metallization film thickness
- Oxide step heights
- Polycrystalline silicon film thickness
- Diffusion depths

The interferometer might find use in failure analysis to measure film thicknesses in areas where it may not be feasible to use other surface measuring equipment (such as Dektak or Tallysurf).

e. Hole Inspection Microscopes. Hole inspection microscope systems are generally built up from normal metallurgical microscopes with the addition of long working distance objectives. Table IV in this chapter shows that high magnification objectives (20X and 40X) are available with much longer than normal working distances.

Microscopes with long working distance can be used to inspect such things as plated-through holes in printed circuit wiring boards or to more readily inspect microcircuits mounted in package cavities.

f. Dimensioning Microscopes. Microscopes specifically designed for making measurements are capable of measuring in three dimensions accurately to within 0.0001 inches (2.5 μm). With special digital readout attachments, accuracy of measurement is increased to 0.00004 inches (1 μm). Figure 22 shows a typical measuring microscope, and Table V gives typical data on stage sizes and measurement ranges.

TABLE V

TYPICAL STAGE SIZE AND MEASUREMENT RANGES OF MEASURING MICROSCOPES

Models	CS-S Stage	CS-SR Stage	CS-D2 Stage
Stage area	170 mm x 170 mm	160 mm dia.	260 mm x 170 mm
Stage glass	90 mm dia.	90 mm dia.	130 mm x 80 mm
Stroke	X50 mm, Y50 mm	X50 mm, Y50 mm	X100 mm, Y50 mm
Minimum read-out	0.001 mm for both X and Y		
Rotation	—	Scale graduation 360°, reading up to 2' with vernier	—
Weight of specimen	Up to 3 kg		

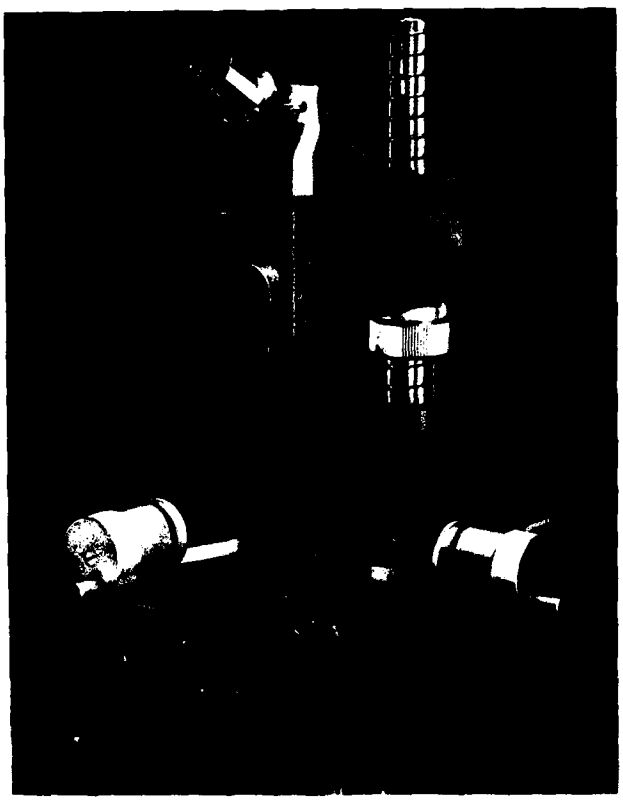


FIGURE 22. TYPICAL MEASURING MICROSCOPE

Some of the measurements that a failure analyst might wish to make with a dimensioning system are:

(a) Die size
(b) Package cavity size
(c) Bonding pad dimensions
(d) Metallization and other conductor widths and spacings
(e) Device dimensions (bipolar and MOS transistors, diode, resistor, etc.)
(f) Film heights
(g) Contour heights

Digital attachments are available for the dimensioning microscope that can increase measurement accuracy to within 1 μm. However, in general failure analysis, the dedicated dimensioning system would probably not find enough use to warrant its expense.

Relatively inexpensive alternatives are available for making X-Y measurements of equal accuracy to the dedicated measuring microscope. One such alternative is the filar eyepiece which is an attachment to a general purpose metallurgical microscope. The filar is capable of making most of the measurements used in failure analysis (see Chapter III-J, paragraph 6.a, page III-J-13 for details on calibration and use).

A second alternative is the beam splitter measuring apparatus. This is also an attachment to the general metallurgical microscope (see Chapter III-K, paragraph 6.b, page K-18 for details on calibration and use).

g. Infrared Microscope. Silicon is transparent to light with wavelengths greater than 1.1 μm. Therefore, possibilities exist for obtaining useful bulk material property information using infrared microscopy techniques and spectrophotometric analyses. In addition, bonding areas of semiconductor die in packages can be examined to some extent. The examination of die bonding areas is obviously limited by the fact that infrared light will not penetrate die metallization areas or areas of high doping concentration.

Figure 23 shows the components of an infrared microscope equipped with both transmitted and incident light.

The infrared microscope can be used in the transmission mode to examine semiconductor wafers during the processing cycle and to examine individual die before packaging. By using polarized transmitted infrared light, point defects can be located in silicon that are not visible by any other means (see Reference 8). The transmission mode, however, has little or no relevance in failure analysis work.

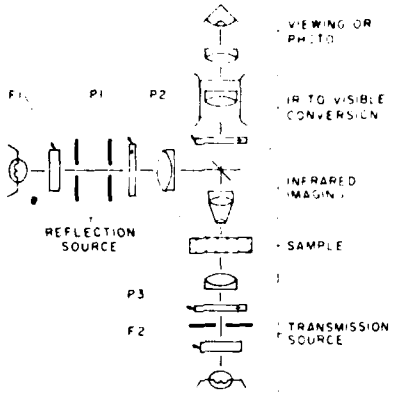


FIGURE 23. SCHEMATIC COMPONENTS OF INFRARED MICROSCOPE WITH BOTH TRANSMITTED AND INCIDENT LIGHT SOURCES

In the incident, or reflected, mode infrared microscopy can be used to examine the following: (see References 8 and 9).

(1) Contact damage occurring in weld areas used, for instance, in the assembly of solar cells.
(2) Semiconductor die bond areas

h. Light Section Microscope. This instrument is generally used in measurements of film thicknesses greater than 1 μm. The instrument consists of two microscopes. An illuminating microscope projects a slit of light onto a sample at 45° to the sample, and an observing microscope forms an angle of 90° with the illuminating microscope and an angle of 45° with the sample. The image of the slit is observed through an eyepiece equipped with a reticle and micrometer.

See Chapter III-J, page III-J-12 for further details.

4. Photomicrography. It is generally accepted that photomicrography is defined as being photographic work done through a compound microscope at a magnification of 10X or greater. The field of photomicrography is NOT severely limited or bounded by any of the following:

- o Make of microscope (Nikon, Zeiss, Olympus, etc.)
- o Type of camera (Polaroid, 35 mm)
- o Type of film (Polaroid paper and film negative,
- o 35 mm negative, large format Polaroid or negative type)
- o Type of light source (tungsten, xenon, etc.)
- o Type of lighting (bright field, dark field, differential interference, etc.)

NOTE: In one important sense, the type of film used in photomicrography is a limiting factor in failure analysis work. Failure analysis is generally completed in as short a time as possible, and therefore, results such as photographs are needed asas soon as possible. For this reason, Polaroid film and camera systems are used much more extensively than 35 mm or other negative systems.

Photomicrography requires techniques and experience that are far beyond comparison with ordinary photography. Some of the things which DO severely limit and bound the subject are:

- o Complete elimination of internal microscope reflection
- o Precise measurement of exposure time
- o Accurate focusing
- o Elimination of vibration (both sample and shutter)
- o Proper color temperature control (through filtration)
- o High quality optics

a. Practical Hints for Photomicrography. Following are some hints that should aid the failure analyst in his attempts to make high quality photomicrographs:

- (1) Finding the Best Location for Photomicrography. In order to take a good picture, a place must be chosen that is free from dust and humidity, vibration, and direct sunlight. It is also necessary to avoid places near air conditioners or heat outlets or any place where temperature frequently changes.

- (2) The Microscope. In photography work, it is preferable to have a microscope which focuses by moving the stage rather than the magnifying elements.

Microscopes with built-in illuminators are more convenient than external ones and generally provide more uniform lighting across the entire visible field.

Microscopes with large stands are generally stable and free from vibration.

Objective lenses, eyepieces, and photo eyepieces supplied by the same manufacturer are designed to complement each other optically. Therefore, in photography to produce the best quality photographs possible, different manufacturer's lenses should not be mixed.

Microscope objective lenses have a finite resolving power, and an eyepiece serves only to enlarge the resolved image. Therefore, no matter how high a total magnification is obtained by using a high magnification eyepiece, image detail not resolved by the objective will not be reproduced either optically or on film. For instance, the total magnification produced by 40X objective and 10X eyepiece is the same as that produced by 100X objective and 4X eyepiece, but the finer structural detail of a specimen will be revealed with the latter combination.

- (3) Photomicrographic Equipment. Even the slightest vibration at the moment of shutter release tends to cause blurred photographs. It would be advisable to utilize vibration-proof type equipment to prevent this. Pneumatic isolation monitoring or heavy stone tables are commonly used to minimize vibration.

A photomicrographic exposure meter designed to measure exposure time and color temperature in a position near the film plane is convenient.

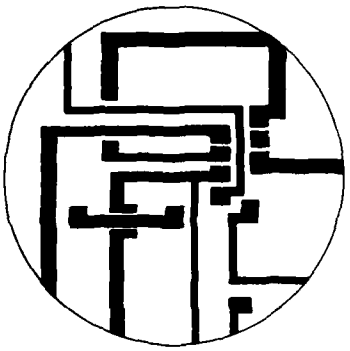
- (4) Centering the Illuminator. It is important to center the illuminator in order to ensure that the field of view is uniformly illuminated. The following procedure can be used to center the illuminator:

- oo Focus the microscope on a sample.
- oo Stop down the field iris diaphragm (the diaphragm located in the illuminator path).
- oo Center the field iris diaphragm.
- oo Open the diaphragm full open.
- oo Remove the photo eyepiece, look into the eyepiece tube and center the filament. This will be possible because the filament will appear in the field of view.

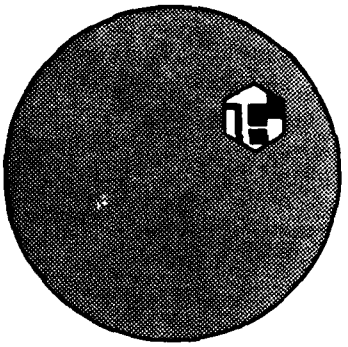
This procedure is diagrammatically represented in Figure 24.

- (5) Use and Effects of Aperture Iris Diaphragm and Field Iris Diaphragm. The field iris diaphragm controls the diameter of the total light bundle impinging on the sample. Stop down the field diaphragm while looking through the photo eyepiece, and an image of the iris diaphragm will appear within the field of view. The field diaphragm should now be opened to a diameter that is slightly larger than the diameter of the field of view.

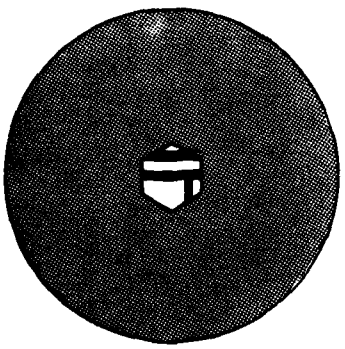
When an aperture diaphragm is opened too wide, the image contrast is impaired due to internal reflections. If the diaphragm is stopped down too much, resolution is reduced. In order to achieve maximum objective lens performance, it is a good practice to match the opening of the aperture iris diaphragm to the numerical aperture (NA) of the objective lens. This is a good practice in general photographic work, but often microscopic specimens are low in contrast, and their image will likewise be low in contrast if the objective is used with its full rated NA.



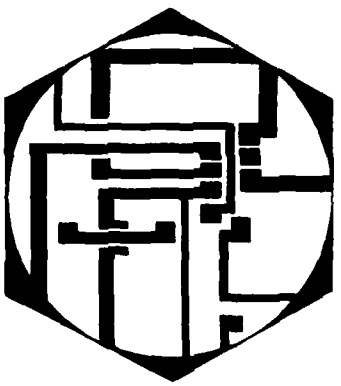
a. FOCUS THE MICROSCOPE



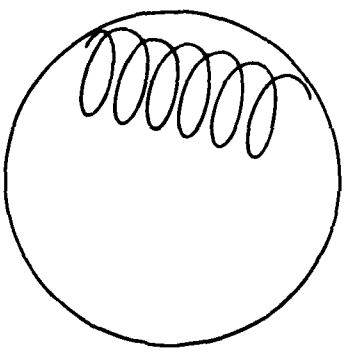
b. STOP DOWN THE FIELD IRIS DIAPHRAM



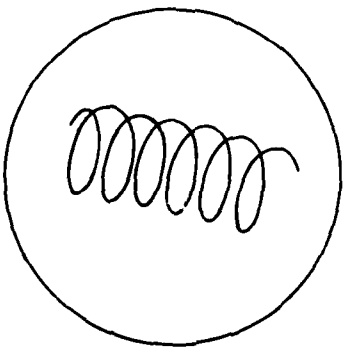
c. CENTER THE FIELD IRIS DIAPHRAM



d. OPEN THE DIAPHRAM FULL



e. REMOVE EYEPIECE AND LOOK AT FILAMENT



f. CENTER THE FILAMENT

FIGURE 24. DIAGRAMMATIC SEQUENCE IN CENTERING MICROSCOPE FILAMENT

It may, therefore, be occasionally preferable to stop down the aperture diaphragm slightly more than indicated by the objective NA. This practice will increase image contrast and result in larger depth of focus with a flatter field. An aperture setting of 0.7X of the objective lens NA is a good compromise.

- (6) Diopter Adjustment and Focusing. In focusing for photography, the eyepiece should first be corrected to the proper diopter setting for eye activity. The ability to bring the sample into sharp focus is an important aspect of photomicrography. Sharp focus is sometimes difficult to achieve, particularly when using objective lenses of 4X or lower because of the considerable depth of field. In cases such as this, use of a screen viewer on the camera will greatly improve focus.

- (7) Keep Optical Elements Clean. If the exposed surfaces of optical elements are stained or dirty, resolving power will be greatly reduced. It is good policy to keep instruments clean.

- (8) Black and White Photomicrography. Some of the considerations to be taken into account when taking black and white photographs are listed below:

oo Film. Photomicrography generally requires fine grain film. However, when the background is dark or when fluorescent lighting is being used, faster films are usually preferred. (see Photographic Films and Camera Systems for more details).

oo Filters. Green filters are usually used for photography, and blue filters are used for visual observation. Blue filters are not preferable for photographic work because their use impairs resolution over the entire picture. To increase contrast of a particular color, the filter to use should be a color which is complementary to that particular color to be enhanced. Table VI describes typical complementary color filters and the resultant colors emphasized.

TABLE VI

COMPLEMENTARY COLOR FILTERS

Complementary Colors	Colors Emphasized
Red	Blue-green
Yellow-green	Violet
Orange	Light blue
Green	Purple
Yellow	Ultramarine blue

oo Determination of Exposure. In photomicrography, it is essential to determine the optimum exposure time. The most simple and accurate means available is through the use of automatic exposure equipment.

- (9) Color Photomicrography. Some of the considerations to be taken into account when taking color photographs are:

oo Color Films. Several types of color film are available:

Polaroid (Sheet film, pack film, paper negative, positive-negative)
35 mm (color reversal, color negative)
(See Photographic Films and Camera Systems for more details.)

oo Color Temperature. Color temperature for the most commonly used films are in the range of:

Polaroid - approximately 5500°K, daylight
Polaroid - approximately 3500°K, tungsten
35 mm - approximately 4500°K, daylight
35 mm - approximately 2800°K, tungsten

oo Reciprocity Failure. Both extremely long and extremely short shutter speeds will lower the sensitivity of film. Both cases will result in underexposure, and the effect is called "reciprocity failure." Because of the long exposure times used in photomicrographic work, reciprocity failure often becomes a factor in the ability to produce good photographs. If a sample is photographed at several different magnifications, color rendition can change considerably even with accurate color temperature control. This situation comes about because of different shutter speeds. Due to reciprocity failure, color balance is different between a bright low magnification and a dark high magnification exposure. Shutter speeds should be kept constant, if at all possible, in order to avoid reciprocity failure.

5. Photomacrography. Photomacrography is generally defined as photographic work done at magnifications of 10X or less. Photographs of semiconductor die, microelectronic packages, test fixtures, etc., are all examples of uses of photomacrography. Because of the range of magnifications encountered (1:1, 1/2:1, 1/4:1, etc.), photomacrographic equipment requires long working distances.

Figure 25 shows four examples of photomacrography ranging in size from 180 x 225 mil^2 (4.6 x 5.7 mm^2) to 1.9 x 4.3 in^2 (4.8 x 11 cm^2).

The field of photomacrography is NOT SEVERELY limited or bounded by any of the following:

- Type of camera (Polaroid, 35 mm, large format negative, etc.)
- Type of film (Polaroid paper and film negative, 35 mm negative, large format Polaroid or negative type)
- Type of illumination (incident or oblique)

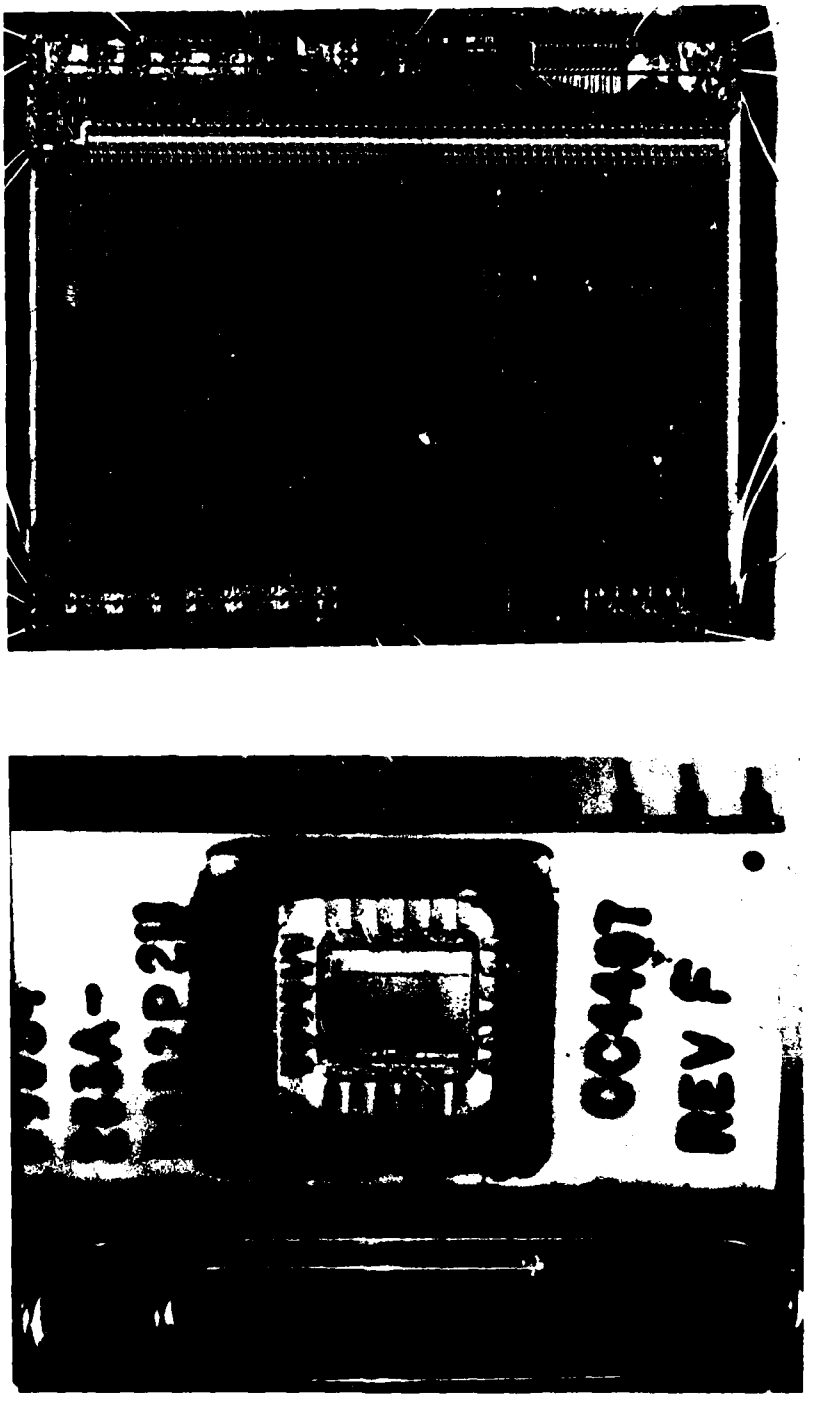
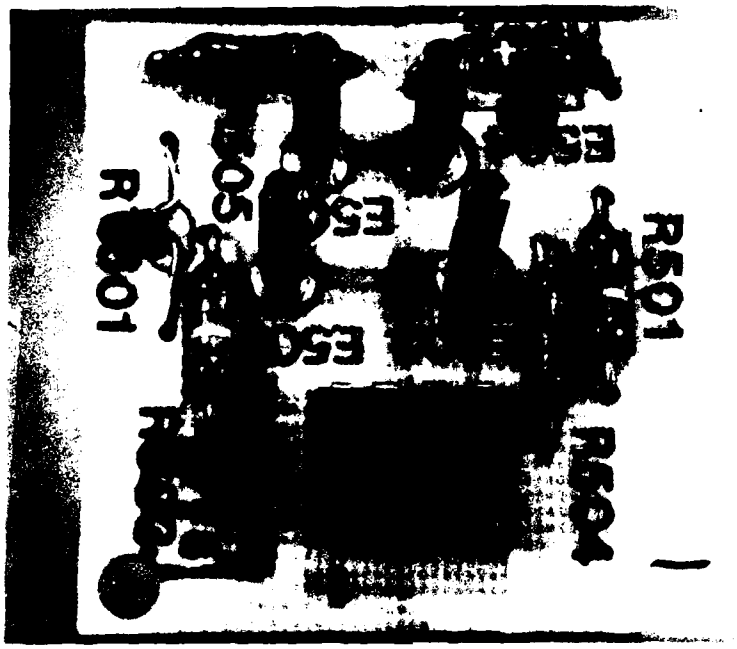


FIGURE 25. EXAMPLES OF PHOTOMACROGRAPHY (SHEET 1)



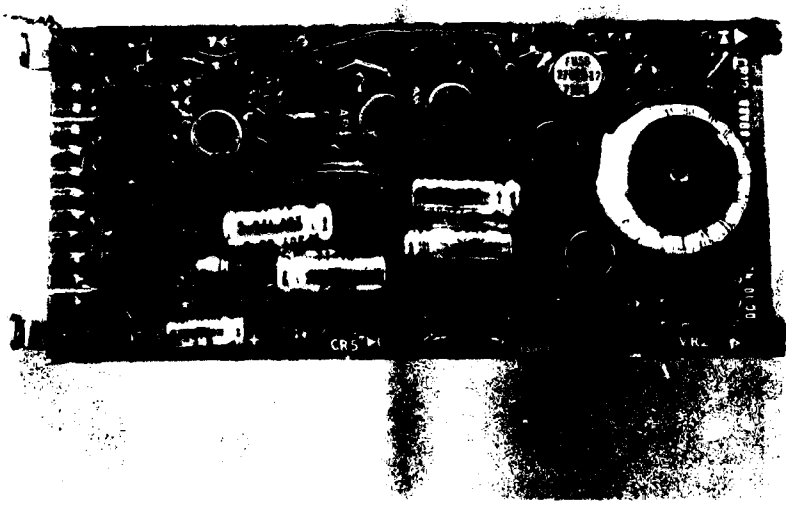


FIGURE 25. EXAMPLES OF PHOTOMACROGRAPHY (SHEET 2)

NOTE: Photomacrographic work in failure analysis is generally used to document an anomaly. Therefore, speed of results is important, and Polaroid film is most usually employed for this reason.

Photomacrographic work IS SEVERELY limited by the following:

- o Elimination of light source reflections
- o Precise measurement of exposure time
- o Accurate focusing
- o Elimination of vibration (both sample and shutter)
- o Proper color temperature control (through filtration)
- o High quality optics

a. Practical Hints for Photomacrography. Following are some hints that might aid the failure analyst in his attempts to make high quality photomacrographs:

- (1) Finding the Best Location for Photomacrography. In order to take a high quality picture, a location must be chosen that is free of dust, humidity, vibration, and direct sunlight. It is also advisable to avoid places near air conditioner or heat vents or any place where temperature frequently changes.

- (2) Photomacrographic Equipment. Any vibration at the moment of shutter release tends to cause blurred photographs. Therefore, equipment stands that are stable produce better pictures. Rubber feet on the bottom of the equipment stand is typical.

- (3) Illumination. Equipment is available with incident light illumination as an integral part. However, side illumination using illuminators such as the type demonstrated in Figure 3 is more common. A great deal of experience is necessary to place lighting equipment in the correct position to prevent shadows and to provide sufficient illumination.

- (4) Painted With Light Illumination Technique. A novel illumination technique is described which can provide shadowless and relatively uniform lighting of three dimensional subjects. The technique is quite useful for any subject that is prone to shadow generation under normal illumination. It is especially useful in macrophotography where close-up lens proximity prohibits uniform illumination. In practice the illumination is supplied by a single handheld floodlight which must be moved in a constant circular motion about its projection axis. During film exposure the camera shutter is held open while the floodlight is slowly and evenly (uniform speed) traversed to successively illuminate the entire topography of the subject. It is important to maintain a constant lamp-to-subject distance and to maintain the circular motion of the lamp during exposure. The camera lens aperture (f-stop) must be closed down to accommodate the long exposure time required. Obviously the depth of field increase resulting from the small aperture will enhance resolution in the photography of 3D subjects. Polaroid films are useful for experimental exposure determination. A typical exposure for Polaroid Type 58 (ASA 75) was found to be 50 seconds at f/32. The lamp, a 150 watt photoflood, was aimed at 45° and maintained at 20 inches to the subject. A typical equipment setup for macrophotography would consist of a Polaroid MP-4 photomacrographic and photomicrographic recording system shown in Figure 25A equipped with a 75mm lens for a magnification of 2.5X.

Typical results obtained using painted-with-light technique are shown in Figure 25B. The electronic module shown in Figure 25B (a and b) compare results using oblique strobe illumination with that obtained with the painted-with-light technique. Figure 25B (c) illustrates the lighting uniformity obtained with the painted light technique of a large electronic assembly.

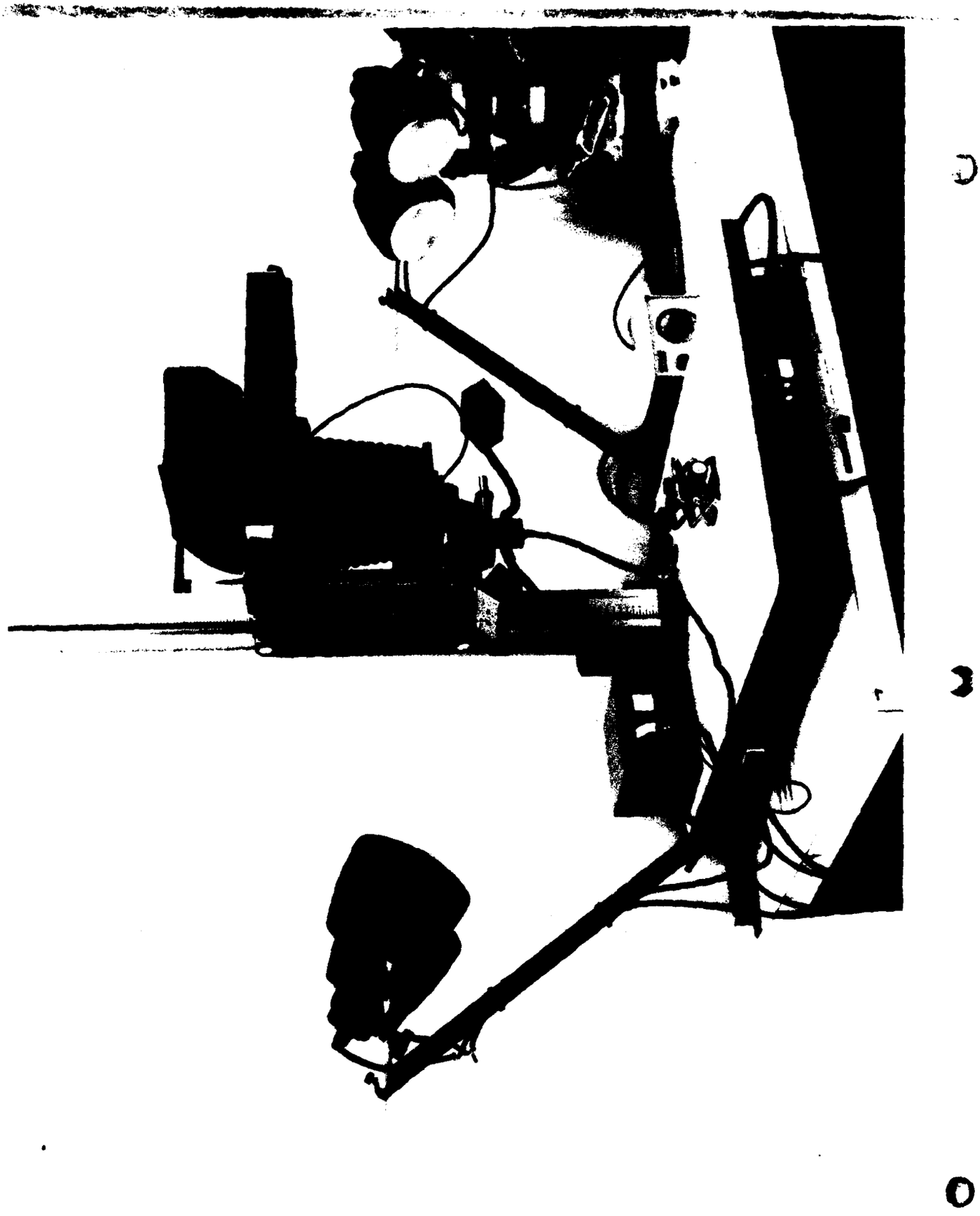


FIGURE 25A. POLAROID MP-4 PHOTOGRAPHIC RECORDING SYSTEM EQUIPPED WITH PHOTOFLOOD AND DUAL STROBE ILLUMINATION

(a) DUAL STROBE ILLUMINATION (BOWENS MACRO LITE)

(b) PAINTED WITH LIGHT ILLUMINATION

(c) PAINTED WITH LIGHT ILLUMINATION

FIGURE 25B. COMPARISON OF RESULTS OBTAINED USING THE PAINTED WITH LIGHT ILLUMINATION TECHNIQUES (b&c) VS. CONVENTIONAL ILLUMINATION METHOD (a)

b. Focus. Because of the depth of field usually available in photomacrography, focusing is not as critical as in photomicrographic work. However, as in any photographic work, care should be used to focus the equipment as well as possible.

The comments in paragraph 4.a of this chapter, Practical Hints for Photomicrography, regarding films, filters, and reciprocity failure are true also for photomacrographic work.

6. TV Camera Monitoring With Video Tape Recorder Systems. Systems employing TV camera monitoring and video tape recording may sometimes find application in failure analysis. These systems are, however, used more frequently as teaching aids or in semiconductor manufacturing inspection operations. TV camera and display images have become popular in semiconductor photomask inspections because of the ease of viewing and the reduction in eye strain achieved.

Of particular value is the TV display's ability to provide large image sizes of small dimensions thus enabling images to be measured more accurately than through normal microscope measurement means. The measuring ability of TV monitor systems has grown to a high degree of sophistication chiefly because of the nature of image recognition inherent in producing a TV image through electron beam scanning.

Image analyzing computers are available today which can almost immediately detect a light intensity change in a scanned image that might represent the edge of a dimension being measured. Using the same principles of "computer enhanced" photography that add detail to long-range satellite photographs, these image analyzing computers are capable of making highly accurate physical dimensional measurements that cannot be duplicated by optical techniques.

TV monitors and image analyzing computers have made possible high speed automatic inspection operations in which accept/reject decisions are made by computer.

Both black and white and color cameras and video monitors are available. Increased resolution has been obtained on more recent monitors by increasing horizontal line resolution at the picture center (500 lines in Hitachi VM-910). However, these monitors are not yet capable of producing colors and image quality comparable to optical methods.

7. Photographic Films. As any amateur photographer knows, the variety of films and types of equipment available on the market today are truly overwhelming. Equally overwhelming is the number of definitions and terms one must become familiar with to intelligently discuss photography. Things such as f-stop, ASA number, panchromatic, Tri-X pan, SLR, range finder, Polaroid, etc., are a few of the simpler terms one finds when discussing photography.

a. Polaroid Films. Obtaining speedy photographic documentation is an important requirement in failure analysis work. Because of the requirement for speed, Polaroid films are most often used in failure analysis work.

Table VII lists the technical characteristics and details of Polaroid film types available. This table provides sufficient information to allow the failure analyst to choose the proper film for use in any specific situation in either macro or microphotography.

NOTE: Table VII does not include Polaroid's latest film, Type 611 Video Image Recording Land Film. This film is panchromatic black and white in 3 1/4 x 4 1/4 inches (8.3 x 10.8 cm) pack. This film has extended gray scale for recording a greater range of display information and wide exposure latitude for improved recording of video display brightness range.

TABLE VII

DETAILS ON POLAROID FILM

	RESULT	PRODUCT NAME	FORMAT	PRINT SIZE	IMAGE AREA	SPEED[1]	NORMAL DEVELOPMENT TIME AT 75 F (24°C)	SPECIAL CHARACTERISTICS
COLOR	Color print	Polacolor 2 Type 808	Sheet	8" x10⅞in (22x27cm)	7½x9½in (19x23cm)	80 ASA (20 DIN)	60 seconds	Balanced for daylight and electronic flash
		Polacolor 2 Type 58	Sheet	4x5in (10.5x13cm)	3½x4½in (9x11.5cm)	75 ASA (20 DIN)	60 seconds	Balanced for daylight and electronic flash
		Polacolor 2 Type 108	Pack	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	75 ASA (20 DIN)	60 seconds	Balanced for daylight and flash cubes
		Polacolor 2 Type 668	Pack	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	75 ASA (20 DIN)	60 seconds	Balanced for daylight and electronic flash
		Polacolor 2 Type 88	Pack	3¼x3⅜in (8.3x8.6cm)	2¾x2⅞in (7x7.3cm)	75 ASA (20 DIN)	60 seconds	Balanced for daylight and flash cubes
		SX-70	Pack	3½x4¼in (8.7x10.5cm)	3⅛x3⅛in (8x8cm)		Self-timing 45°F (7°C) – 95°F (35°C)	Balanced for daylight
	Color movie	Phototape Type 608	Cassette		9⅝x7⅛in (24.5x18.1cm) projected on player screen		90 seconds	Running time 2½ minutes
	RESULT	**PRODUCT NAME**	**FORMAT**	**PRINT SIZE**	**IMAGE AREA**	**SPEED[1]**	**NORMAL DEVELOPMENT TIME AT 75°F (24°C)**	**SPECIAL CHARACTERISTICS**
BLACK AND WHITE	High speed print	Type 57	Sheet	4x5in (10.5x13cm)	3½x4½in (9x11.5cm)	3000 ASA (36 DIN)	15 seconds	General purpose high speed film
		Type 107	Pack	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	3000 ASA (36 DIN)	15 seconds	General purpose high speed film
		Type 084	Pack	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	3000 ASA (36 DIN)	15 seconds	For Cathode Ray Tube recording
		Type 667	Pack	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	3000 ASA (36 DIN)	30 seconds	General purpose high speed film. Prints do not require coating
		Type 87	Pack	3¼x3⅜in (8.3x8.6cm)	2¾x2⅞in (7x7.3cm)	3000 ASA (36 DIN)	30 seconds	General purpose high speed film. Prints do not require coating
		Type 47	Roll	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	3000 ASA (36 DIN)	15 seconds	General purpose high speed film
	Positive and Negative	Type 55	Sheet	4x5in (10.5x13cm)	3½x4½in (9x11.5cm)	50 ASA (18 DIN)	20 seconds	Negative requires brief clearing in sodium sulfite solution, washing and drying before use [2]
		Type 665	Pack	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	75 ASA (20 DIN)	30 seconds	Negative requires brief clearing in sodium sulfite solution, washing and drying before use [2]
	Fine grain print	Type 52 Polapan	Sheet	4x5in (10.5x13cm)	3½x4½in (9x11.5cm)	400 ASA (27 DIN)	15 seconds	Wide tonal range, superb detail
		Type 42 Polapan	Roll	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	200 ASA (24 DIN)	15 seconds	Wide tonal range, superb detail
	High contrast print	Type 51	Sheet	4x5in (10.5x13cm)	3½x4½in (9x11.5cm)	125 ASA (22 DIN) Tungsten 320 ASA (26 DIN) Daylight	15 seconds	Sensitive to blue light only
	Continuous tone transparency	Type 46L	Roll	3¼x4in (8.3x10.2cm)	2⅜x3¼in (6.2x8.3cm)	800 ASA (30 DIN)	2 minutes	Image must be stabilized and hardened in Dippit solution before use [3]
	High contrast transparency	Type 146L	Roll	3¼x4in (8.3x10.2cm)	2⅜x3¼in (6.2x8.3cm)	100 ASA (21 DIN) Tungsten 200 ASA (24 DIN) Daylight	30 seconds	Sensitive to blue light only. Image must be stabilized and hardened in Dippit solution before use [3]
	Ultra high speed print	Type 410	Roll	3¼x4¼in (8.3x10.8cm)	2⅞x3¾in (7.3x9.5cm)	10,000 ASA (41 DIN)	15 seconds, 60°F (15°C) – 90°F (32°C)	For Oscilloscope trace recording

Spectral sensitivity of all black and white films is panchromatic. Type B sensitization unless otherwise noted

Technical characteristics are subject to change without notice

NOTES

1. ASA and DIN equivalents
2. Polaroid Portable Negative Clearing Tank, #1051, provides convenient on-location clearing and storing of negatives
3. Polaroid projection film hardener #646 Polaroid Dippit for use with Types 46L and 146L films. Solution in easy-to-use container. Each Dippit processes 48 transparencies (6 rolls).

Polaroid snap-in plastic mounts #633 are available for 3¼x4" lantern slides, 16 mounts per box, 6 boxes per carton.

8. 35 mm, Sheet, Roll, Print, and Slide Films. Most commercially available photographic equipment used for micro and macrophotography utilizes either Polaroid, 35 mm, sheet, roll, print, or slide film camera systems. It would literally require volumes to cover all the important aspects of the types of films mentioned in this section and the photographic techniques available. Brief technical descriptions of some of the films available are contained in Tables VIII through X.

NOTE: The data for Tables VIII through X were taken from Kodak Photographic Materials Guide, Publication No. R-31. This publication is but one of the many available covering photographic techniques, films, developing, and generally anything one may wish to know about photography (see reference 13).

9. Camera Systems and Accessories. Several types and sizes of Polaroid cameras and several brand types of 35mm cameras are available for micro and macrophotographic work. Figure 26 demonstrates the light path through the photographic attachments mounted to a metallurgical or stereo microscope.

In actual use, one focuses the microscope by viewing the sample through the eyepiece between microscope and camera. In a properly adjusted and aligned system, the sample will be in focus when viewed through the normal microscope eyepieces as well as when viewed through the camera attachment eyepiece.

a. Polaroid Systems. Figure 27 demonstrates the simplest Polaroid camera system available, model NPC MF-10.

Figures 28 and 29 demonstrate, respectively, camera systems using pack and large format sheet Polaroid film.

Figure 30 demonstrates the highly versatile CU-5 camera system along with data on reduction and magnification ranges available. The system is generally used in macrophotography work.

TABLE VIII

KODAK COLOR FILMS

KODAK Color Films

KODAK Color Film (Code)	Balanced for	Film Speed and KODAK WRATTEN Filter Number									Processing	
		Daylight		Flash		Photolamps (3400 K)		Tungsten (3200 K)		Electronic Flash		
Roll Films		Speed	Filter	Bulb	Filter	Speed	Filter	Speed	Filter	Filter		KODAK Chemicals®
KODACHROME 25 (Daylight) (KM) For color slides[1]	Daylight, Electronic Flash, Blue Flash	25	None	Blue	None	8	80B	6	80A	None	Not for user processing	By Kodak labs and by photofinishers. Sent to Kodak by dealers or direct by users with KODAK Mailers
KODACHROME 40, 5070 (Type A) (KPA) For color slides[1] 135-36 only	Photolamps (3400 K)	25	85	Blue	85	40	None	32	82A	85		
KODACHROME 64 (Daylight) (KR) For color slides[1]	Daylight, Electronic Flash, Blue Flash	64	None	Blue	None	20	80B	16	80A	None		
KODACOLOR II (C) For color prints[2]	Daylight, Electronic Flash, Blue Flash	100	None	Blue	None	32	80B[6]	25	80A[6]	None	FLEXICOLOR® Process C-41	By Kodak, other labs or users. Sent to Kodak by dealers or direct by users with KODAK Mailers
KODACOLOR 400 (CG) For color prints[2]	Daylight, Electronic Flash, Blue Flash	400	None	Blue	None	125	80B[6]	100	80A[6]	None		
EKTACHROME 64 (Daylight) (ER) For color slides[1]	Daylight, Electronic Flash, Blue Flash	64	None	Blue	None	20	80B	16	80A	None[7]		
EKTACHROME 200 (Daylight) (ED) For color slides[1]	Daylight, Electronic Flash, Blue Flash	200	None	Blue	None	64	80B	50	80A	None[7]		
EKTACHROME 160 (Tungsten) (ET) For color slides[1]	Tungsten	100	85B	–	–	125	81A	160	None	–		
EKTACHROME 64 Professional (Daylight) (EPR)[1] 120, 135-36,[3] long rolls (5017)	Daylight, Electronic Flash, Blue Flash	64[4]	None	Blue	None	20	80B	16	80A	None[7]	Process E-6	By Kodak, other labs or users. Sent to Kodak by dealers or direct by users with KODAK Mailers
EKTACHROME 50 Professional (Tungsten) (EPY)[1] 120, 135-36,[3] long rolls (5018)	3200 K Tungsten	32 at 1 60 sec	85B	–	–	40 at 1 10 sec	81A	50[4] at 1 10 sec	None	–		
EKTACHROME 200 Professional (Daylight) (EPD)[1] 120, 135-36,[3] long rolls (5036)	Daylight, Electronic Flash, Blue Flash	200[4]	None	Blue	None	64	80B	50	80A	None[7]		
EKTACHROME 160 Professional (Tungsten) (EPT)[1] 120, 135-36,[3] long rolls (5037)	Tungsten	100	85B	–	–	125	81A	160[4]	None	–		
VERICOLOR II Professional, Type S (VPS)[2] 120, 135-20, 135-36, 220 Expose 1 10 sec or less	Electronic Flash, Daylight, or Blue Flash[8]	125	None	Blue[5]	None	40	80B	32	80A	None	FLEXICOLOR Process C-41	By Kodak user labs or professional finishers. Sent to Kodak by dealers or direct by users with KODAK Mailers. Type L film is not printed by Kodak
VERICOLOR II Professional, Type L (VPL)[2] 120 only Expose 1 50 to 60 sec	3200 K Tungsten	64 at 1 50 sec	85B	Not recom		64 at 1 sec	81A	80 at 1 sec[4]	None	Not recom		

TABLE VIII

KODAK COLOR FILMS (CONT'D)

KODAK Sheet Films	Balanced for	Daylight		Flash		Photolamps (3400 K)		Tungsten (3200 K)		Electronic Flash	Processing KODAK Chemicals®	
		Speed	Filter	Bulb	Filter	Speed	Filter	Speed	Filter	Filter		
EKTACHROME 64 Professional [1] 6117 (Daylight)	Daylight, Electronic Flash, Blue Flash	64 [4]	None	Blue	None	20	80B	16	80A	None [7]	Process E-6	By user labs or professional finishers, not by Kodak
EKTACHROME Professional [1] 6118 Tungsten	3200 K Tungsten	20 + CC 10G at 1 10 sec	85B	–	–	25 at 5 secs	81A	32 [4] at 5 secs	None	–		
VERICOLOR II Professional 4107 Type S [2] Expose 1 10 sec or less	Electronic Flash, Daylight, or Blue Flash	125	None	Blue [5]	None	40	80B	32	80A	None	FLEXICOLOR Process C-41	By user labs or professional finishers, not by Kodak
VERICOLOR II Professional 4108, Type L [2] Expose 1 50 to 60 sec	3200 K Tungsten	64 at 1 50 sec	85B	Not recom.		64 at 1 sec	81A	80 at 1 sec [4]	None	Not recom		
VERICOLOR Internegative 4112	3200 K Tungsten	– [4]	–	–	–	–	–	–	–	–		
VERICOLOR Print 4111	3200 K Tungsten	– [4]	–	–	–	–	–	–	–	–		

Long Rolls (Wider than 16 mm)		Balanced for	Daylight		Photolamps (3400 K)		Tungsten (3200 K)		Processing	
			Speed	Filter	Speed	Filter	Speed	Filter		
EKTACHROME MS 5256 (EMS)		Daylight	64	None	20	80B	16	80A	Process ME-4	By Kodak (35 mm only), other labs, or users. Sent to Kodak by dealers
EKTACHROME EF	5241, Daylight (EP)	Daylight	160	None	50	80B	40	80A		
	5242, Tungsten (EFB)	3200 K Tungsten	80	85B	100	81A	125	None		
VERICOLOR II Professional Type S (VPS), 2107 (On ESTAR Base), 5025 (On Acetate Base) Expose 1 10 sec or less		Electronic Flash, Daylight, or Blue Flash	125	None	40	80B	32	80A	FLEXICOLOR Process C-41	By Kodak, other labs, or users. Sent to Kodak by dealers
VERICOLOR Internegative 6011		3200 K Tungsten	– [4]	–	–	–	–	–		
VERICOLOR Slide 5072		3200 K Tungsten	– [4]	–	–	–	–	–		

Notes [1] Must be processed into slides or transparencies before prints can be made

[2] Must be developed to negatives before prints or slides can be made

[3] Also available in long rolls 35 mm perforated

[4] See film instructions

[5] Or clear bulbs with No. 80C Filter; use No. 80D Filter with zirconium-filled clear bulbs such as AG-1 and M-3

[6] Filter recommendations are for critical use in making negatives to be printed by photofinishers

[7] If results are consistently bluish, use a CC05Y or CC10Y Filter with EKTACHROME Films for Process E6; use a No. 81B Filter with KODACOLOR II Film. Increase exposure 1/3 stop when a CC10Y or No. 81B Filter is used

[8] Chemicals other than the KODAK Chemicals listed may be available

TABLE IX

KODAK BLACK-AND-WHITE FILMS

KODAK Black-and-White Films

KODAK Film (Code)	Properties and Purpose	Speeds	
Roll Films		Daylight	Tungsten
VERICHROME Pan (VP)—rolls and for Cirkut cameras	All-round use	125	125
PLUS-X Pan (PX)—135[1]	General-purpose film	125	125
TRI-X Pan (TX)[1]	Very fast. For limited light, action	400	400
PANATOMIC-X (FX)—135[1] PANATOMIC-X Professional (FXP)—120	Extremely fine grain, very high resolving power	32	32
PLUS-X Pan Professional (PXP)— 120 and 220 in 5-roll pro-pack	General-purpose film, retouching surface on emulsion side	125	125
TRI-X Pan Professional (TXP)— 120 and 220 in 5-roll pro-pack, film packs	Superior highlight brilliance, good contrast control, retouching surface on both sides	320	320
ROYAL-X Pan (RX)—120 only	Ultra-fast. For existing light	1250[3]	1250[3]
Recording 2475 (ESTAR-AH Base) (RE)—135-36[1]	Ultra-fast panchromatic. For adverse light conditions	–	1000-3200[3]
High Speed Infrared (HIE)—135-20 only	Haze penetration, special effects and purposes	–[3]	–[3]
Technical Pan 2415[1]	High to normal contrast, depending on development	25[3]	20
Sheet Films	**Properties and Purpose**	**Daylight**	**Tungsten**
EKTAPAN 4162 (ESTAR Thick Base)[2]	For portraits by electronic flash and general use	100	100
PLUS-X Pan Professional 4147 (ESTAR Thick Base)[2]	Excellent definition. For portrait and commercial work	125	125
SUPER-XX Pan 4142 (ESTAR Thick Base)	Long tonal gradation. Color-separation negatives	200	200
TRI-X Pan Professional 4164 (ESTAR Thick Base)[2]	Superior highlight brilliance, good contrast control	320	320
TRI-X Ortho 4163 (ESTAR Thick Base)	Superior body highlight brilliance. For portraits and commercial subjects	320	200
ROYAL Pan 4141 (ESTAR Thick Base)[2]	High Speed. General purpose	400	400
ROYAL-X Pan 4166 (ESTAR Thick Base)	Ultra-fast. For available-light exposure	1250[3]	1250[3]
Commercial 6127 and 4127 (ESTAR Thick Base)	Blue-sensitive. For continuous-tone copying, transparencies	50 (20[4])	8
Contrast Process Ortho 4154 (ESTAR Thick Base)	Extremely high contrast. For line copies	100[4]	50
Contrast Process Pan 4155 (ESTAR Thick Base)	Extremely high contrast. For copies of colored line originals	100[4]	80
Professional Copy 4125 (ESTAR Thick Base)	Retains highlight gradation in copies	25[4]	12
High-Speed Infrared 4143 (ESTAR Thick Base)	Haze penetration, special effects. Document copying	–[3]	–[4]
Long Rolls (Wider than 16 mm)	**Properties and Purpose**	**Daylight**	**Tungsten**
PLUS-X Pan Professional 2147 (ESTAR Base)	Good definition and excellent latitude	125	125
PLUS-X Portrait 5068	For portrait and school work. Retouching surface	125	125
Direct Positive Panchromatic 5246	For reversal processing to slides	80	64

NOTES [1] Also available in long rolls 35 mm perforated

[2] Also available in long rolls 3¼ in. wide

[3] See film instructions

[4] Speed to white-flame arc

TABLE I.

KODAK BLACK-AND-WHITE PAPERS

KODAK Black-and-White Papers

Texture	Smooth	Smooth	Smooth	Fine Grained	Fine Grained	Tweed	Tapestry
Brilliance	Glossy	Lustre	High Lustre	Lustre	High Lustre	Lustre	Lustre
KODAK Black-and-White Material							
AD-TYPE		A WH LW 2,3					
AZO	F WH SW 5			E WH SW 2,3 DW 2,3			
Dye Transfer	F WH DW			G CR DW			
EKTALURE				G CR DW	K WM-WH DW	R CR DW	X CR DW
EKTAMATIC SC	F WH SW, DW	N WH SW A WH LW					
KODABROME II RC	F WH MW S-UH*	N WH MW S-UH*		E WH MW			
KODABROMIDE	F WH SW 1-5 DW 1-5	A WH LW 2,3		E WH SW 2-4 DW 2-4			
MEDALIST	F WH SW 1-4 DW 2,3			G CR DW 2,3			
Mural						R, WRM† CR SW 2,3	
PANALURE	F WH SW						
PANALURE Portrait				E WH DW			
PANALURE II RC	F WH MW						
POLYCONTRAST	F WH SW, DW	N WH SW, DW A WH LW	J WH SW, DW	G CR DW			
POLYCONTRAST Rapid	F WH SW, DW	N WH SW		G CR DW			
POLYCONTRAST Rapid RC	F WH MW	N WH MW					
POLYCONTRAST Rapid II RC	F WH MW	N WH MW					
Portrait Proof						R CR SW	
RESISTO		N WH, SW 2,3					
Studio Proof	F WH SW						
VELOX	F WH SW 1-4						
VELOX PREMIER RC	F WH MW			E WH MW			
VELOX UNICONTRAST	F WH SW						

WH—White paper stock CR—Cream-white paper stock WM-WH—Warm-white paper stock

*Available in soft, medium, hard, extra-hard, and ultra-hard grades

†Available in rolls 54" wide

A: Smooth lustre on a white lightweight base. This paper is thin enough for the illustrative pages in a report or a manual. Folds without cracking.

E: Fine-grain lustre. This surface preserves fine detail and is suitable for illustrative work where a white base is desirable.

F: Smooth, glossy. The general favorite for photomechanical reproduction copying, and the rendering of final detail. F-surface RC papers must not be ferrotyped; they produce a high-gloss surface when air-dried. F-surface conventional papers can be ferrotyped to produce a high gloss.

G: Fine-grain lustre on a cream-white base. This is a popular surface for small- and medium-size portraits and for oil coloring.

J: Smooth, high-lustre white. Designed for the illustrator; preserves detail and produces highest quality photomechanical reproductions.

K: High-lustre counterpart of G although it imparts a feeling of greater brilliance and life to the picture. Not recommended for oils.

N: Smooth—between lustre and matte. Especially designed for retouching on the print. Accepts strong penciling and preserves fine detail.

R, WRM: Popular tweed surface. Minimizes need for fine retouching. Especially good for breaking up large areas. Popular in photomural work.

X: Lustre, tapestry surface, cream-white. Extremely coarse-textured and designed for heavy subjects. Effective for very large heads of men. Frequently colored with opaque oils, which gives effect of an oil painting on canvas.

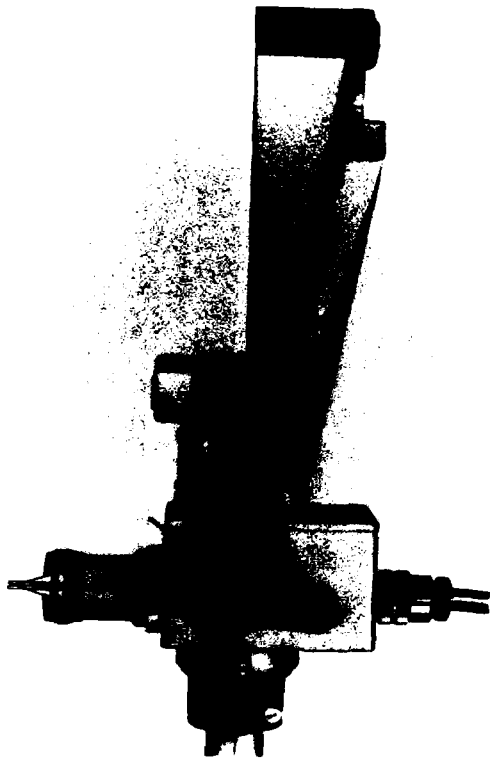


FIGURE 26. TYPICAL LIGHT PATH THROUGH PHOTOGRAPHIC ATTACHMENTS

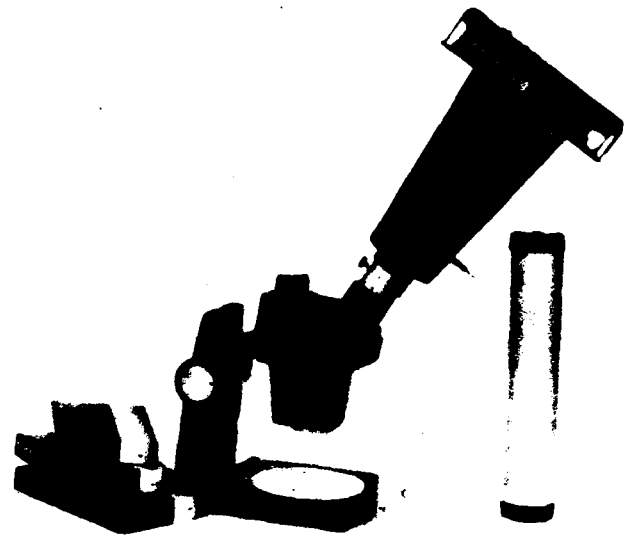


FIGURE 27. VERSATILE POLAROID CAMERA ATTACHMENT SUITABLE FOR INSTANTANEOUS PHOTOGRAPHY (MODEL NPC MF-10, $135)

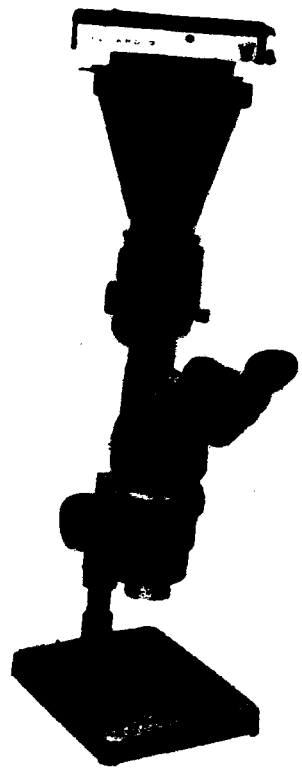


FIGURE 28. STEREO MICROSCOPE WITH PACK FILM POLAROID CAMERA ATTACHMENT

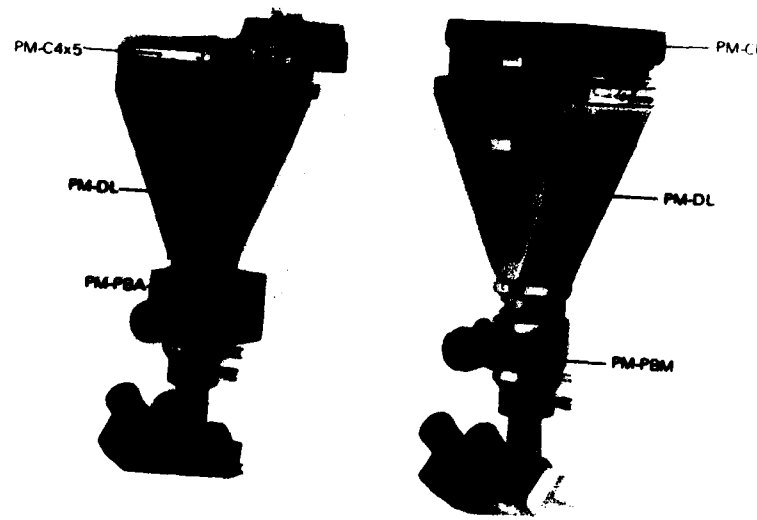


FIGURE 29. LARGE FORMAT POLAROID CAMERA EQUIPMENT

PICTURE RATIO AND FIELD SIZE WITH PACK FILM CAMERA BODY (88-1)

	REDUCTION			MAGNIFICATION				
Picture Ratio	1/4:1	1/3:1	1/2:1	1:1	2:1	3:1	4.5:1	10:1
Lens	88-5	88-5	88-5	88-3	88-3*	88-3**	88-35	88-17
Framing Accessory	88-25	88-52	88-53	88-11	88-21	88-31	FRAME BUILT-IN	
Field Size	29.2x38.1cm 11 1/2x15 in.	21.6x27.9cm 8 1/2x11 in.	15.2x19.7cm 6x7 3/4 in.	7.3x9.5cm 2 7/8x3 3/4 in.	3.6x4.2cm 1 7/16x1 5/8 in.	2.4x3.2cm 15/16x1 1/4 in.	1.6x2.1cm .63x.83 in.	.73x.95cm .29x.37 in.
Lens-to-Subject Distance	63.5cm 25 in.	45.4cm 17 7/8 in.	31.4cm 12 3/8 in.	11.7cm 4 5/8 in.	7.9cm 3 1/8 in.	6.7cm 2 5/8 in.	FRAME BUILT-IN	

*Add one 88-7 Ratio multiplier. **Add two 88-7 Ratio multipliers.

POLAROID LAND FILMS

POLAROID LAND FILM TYPES	88-1 Pack Film Camera Body	88-2 4x5 inch (9x12cm) Film Camera Body & Model 545 Film Holder
POLACOLOR 2 FILMS – finished, full color photos in 60 seconds. Film speed 75 ASA 20 DIN	Type 668	Type 58
HIGH SPEED FILMS – continuous-tone prints of medium contrast in 15-30 seconds. Film speed 3000 ASA 36 DIN	Type 667 Type 084	Type 57
POSITIVE/NEGATIVE FILMS – simultaneously produce continuous-tone prints and fully developed negatives in 30 seconds. Film speeds 75 ASA, 20 DIN., or 50 ASA, 18 DIN.	Type 665 (ASA 75)	Type 55 (ASA 50)
WIDE TONAL RANGE POLAPAN FILMS – continuous tone fine grain prints in 15 seconds. Film speed 400 ASA 27 DIN	-	Type 52
HIGH CONTRAST FILM – very high contrast print with highly saturated blacks and clean whites in 15 seconds. Film speed 125 ASA 22 DIN (Tungsten), 320 ASA 26 DIN. (Daylight)	-	Type 51

Film speeds are approximate ASA and DIN daylight equivalents unless otherwise noted.

HOODS FOR CRT RECORDING

Screen Size/ Approximate Coverage	Approximate Outside Hood Size	Hood	Lens
8x10 cm 3 1/16x3 15/16 in.	4 9/16x5 7/16 in.	88-13	88-3
8x10 cm 3 1/16x3 15/16 in.	5 29/32x5 29/32 in.	88-14	88-3
10.8x13.6 cm 4 1/4x5 3/8 in.	5 7/8x7 3/8 in.	88-46	88-5
12.7x16.5 cm 5x6 1/2 in.	5 7/8x8 1/8 in.	88-47	88-5
16.5x21.6 cm* 6 1/2x8 1/2 in.	6 1/4x8 1/8 in.	88-48	88-5
15.9x22.2 cm** 6x8 3/4 in.	6 1/4x9 in.	88-49	88-5

*For flat surface screens.
**For curved surface (convex) screens.

FIGURE 30. VERSATILE POLAROID CU-5 CAMERA AND ATTACHMENTS FOR BOTH REDUCTION AND MAGNIFICATION PHOTOGRAPHY

Text continued from page III-L-48.

Figures 31 and 32 demonstrate camera systems capable of being used in both micro and macrophotography work.

Reference to Table VII in this chapter shows the high degree of versatility achievable with Polaroid cameras, attachments, and films.

b. 35mm Systems. It has been stated in several places throughout this chapter that in general failure analysis work, Polaroid systems are used much more frequently than 35mm systems. However, when time is not of great importance, it may be desirable to take high quality photographs using 35mm camera attachments.

Figure 33 shows a 35mm camera equipped with automatic exposure control mounted on a metallurgical microscope.

Figure 34 shows a 35mm camera with bellows, lenses, filters, etc., that is capable of being used in both micro and macrophotography work.

c. Automatic Exposure Control. Equipment is available for attachment to both Polaroid and 35mm systems which will automatically control shutter speed to make correct and repeatable exposures.

Figure 33 shows an automatic exposure unit beside the microscope (Olympus PM-CBA) and its accompanying unit (Olympus PM-PBA) placed between the microscope and the camera.

To use the automatic equipment, the film speed being used (ASA rating) is dialed in on the automatic control unit. An exposure compensation setting is usually provided for normal, over, and under exposure (typically $\pm$ 1 f-stop). The microscope is focused, the desired illumination set, and to expose the film one need only activate the shutter control, preferably by cable release to minimize vibration. When this procedure is followed, a correctly exposed picture will result. A good deal of experience will greatly aid the failure analyst in his ability to make good quality photographs.

FIGURE 31. POLAROID CAMERA AND APPARATUS SUITABLE FOR BOTH MICROPHOTOGRAPHY AND MACROPHOTOGRAPHY (KENRO MP812 CAMERA HEAD, POLAROID MP-4 LENSES, SHUTTER, AND CAMERA STAND - $3200)

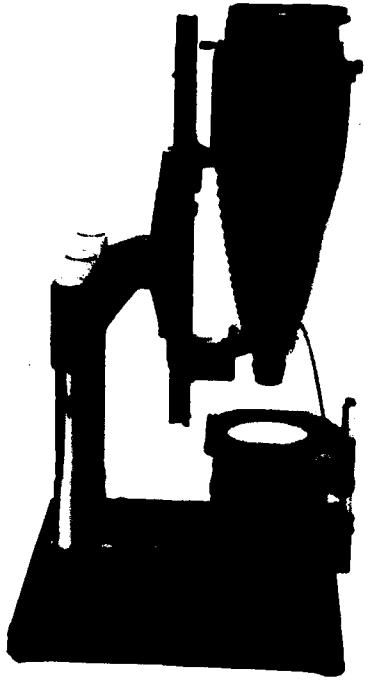


FIGURE 32. PHOTOGRAPHIC APPARATUS SUITABLE FOR BOTH MICROPHOTOGRAPHY AND MACROPHOTOGRAPHY WITH POLAROID FILM

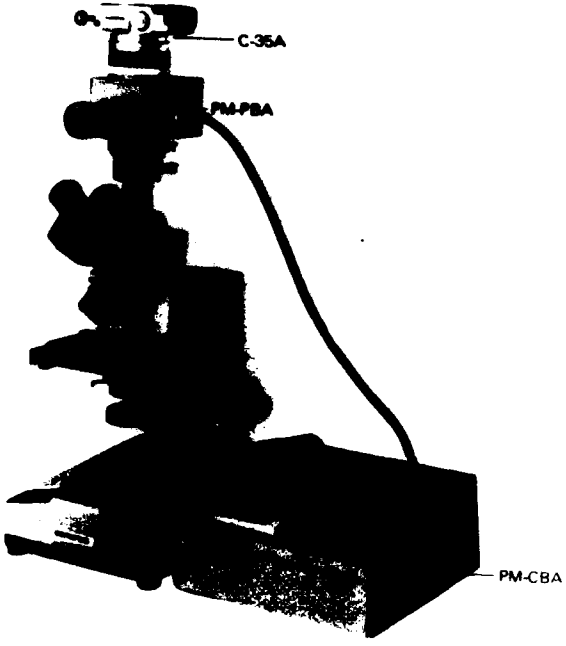


FIGURE 33. METALLURGICAL MICROSCOPE WITH 35MM CAMERA AND AUTOMATIC EXPOSURE CONTROL

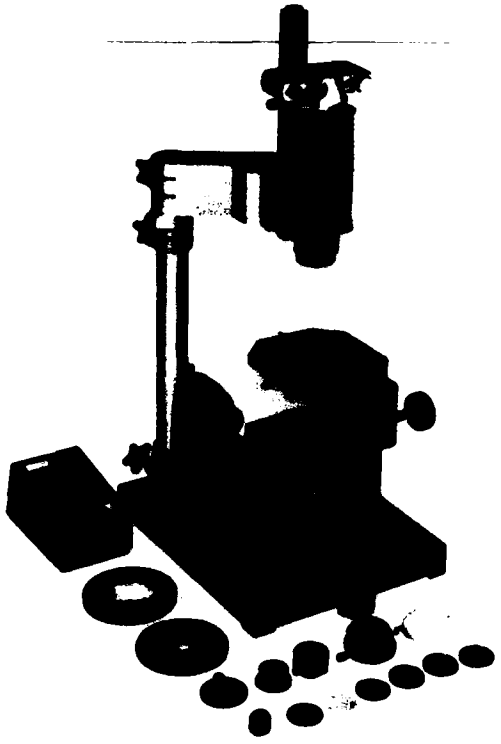


FIGURE 34. COMPLETE PHOTOGRAPHIC EQUIPMENT SUITABLE FOR BOTH PHOTOMICROGRAPHY AND PHOTOMACROGRAPHY WITH 35 MM FILM

Automatic exposure equipment works by sensing a proportion of the light reflected from the object being photographed. When enough light has been recorded by the sensing element, the control unit automatically closes the camera shutter. Typical location of the sensing element can be seen by referring to Figure 26. In Figure 26, it can be seen that the prism located in the automatic exposure unit directs a proportion of light from the microscope to the sensing unit (located to the right of the center prism in this particular Olympus microscope).

d. Filters. Filters are used to exclude undesirable light frequencies and/or to emphasize other light frequencies. Generally, the results of using filters with Polaroid films is neither well-known nor documented and is largely a matter of experimentation. On the other hand, filtration used in conjunction with 35mm photography is a well-established and documented procedure. Tables XI, XII, and XIII provide descriptions of some of the more common filters available for 35mm photography (information and filter numbers are from Vivitar Filter Guide).

TABLE XI

BASIC FILTERS FOR COLOR AND BLACK-AND-WHITE FILM

Filter and/or Number	Description
Skylight 1A	Most commonly used filter, chiefly to protect the camera lens. Also absorbs ultraviolet and reduces haze.
UV Haze	Primarily for lens protection. Also absorbs ultraviolet and slightly reduces haze.
Polarizing	Produces richer, more brilliant colors, increases contrast, eliminates or reduces reflections from non-metallic surfaces, penetrates haze. To use, open one f-stop daylight film, and open two f-stops with tungsten.
Neutral Density	Reduces the amount of light without changing color rendition. To use, open one f-stop for daylight or tungsten film.

TABLE XII

FILTERS FOR COLOR FILM

Filter Type and/or Number	Description
80A	Converts daylight film to 3200°K tungsten light sources. To use, open two f-stops.
CFD	Converts daylight film for use with fluorescent light. To use, open one f-stop.

TABLE XIII

FILTERS FOR BLACK-AND-WHITE FILM

Filter Type and/or Number	Description
No. 8 (K2) Yellow	Records blue and violet colors as dark shades of gray, &yellow as a light shade of gray. To use, open one f-stop with daylight film and 2/3 f-stop with tungsten.
No. 15(G) Deep Yellow	Records blue and violet colors as dark shades of gray, & red and yellow as light shades of gray. To use, open 1-2/3 f-stops with daylight film and one f-stop with tungsten.
02 Orange	Records blue, violet, and green colors as dark shades of gray, & red, orange, and yellow colors as light shades of gray. Has special applications in document copying. To use, open 2-1/3 f-stops with daylight film and two f-stops with tungsten.
25A Red	Records blue, violet, and green colors as dark shades of gray, & red and yellow colors as light shades of gray. To use, open three f-stops with daylight film and 2-1/3 with tungsten.
No. 11 (X1) Light Green	Records blue, violet, and red colors as dark shades of gray, yellow and green colors as light shades of gray. To use, open two f-stops with both daylight and tungsten films.

10. Film Developing and Dark Room Equipment. The subject of and the information available on film developing is probably as extensive as the list of details on photographic films available. Because of the need for a high degree of control over the variables involved, development of color film is not commonly done in facilities normally available to the failure analyst.

Development of black-and-white negatives and enlargement printing are relatively easy and inexpensive, especially when sheet negative film is used. Figure 35 shows simple equipment that can be used for developing sheet film negatives. Temperature control of developer chemicals can be achieved fairly simply over the short time it takes to develop small numbers of negatives. One way in which temperature can be controlled is simply to prepare a large pan of water at the specified temperature and then to place the pan(s) of developer chemicals into the prepared water. The pans into which water is placed should have sufficient volume so that placing the pan of developer chemical in does not cause rapid cooling of the water. It may also be desirable to preheat the developer chemicals. If both water in the large pan and developer chemicals are preheated, the proper temperature can be maintained for a significant length of time.

Tables XIV through XIX give technical details on developing many of the Kodak films and papers available (see the section on Photographic Films in this chapter). In addition, Reference 13 contains information available on everything from darkroom chemicals to darkroom layout and equipment (see Chapter III-B, page III-B-22 for more details on dark room procedures and equipment).

11. Photocopy Systems. It is often desirable to copy photographs in failure analysis. This situation comes about particularly when Polaroid paper negative film has been used to document various stages or results, and it becomes necessary to reproduce the original Polaroid picture for such reasons as duplicating failure analysis

(Text resumes on page III-L-73)

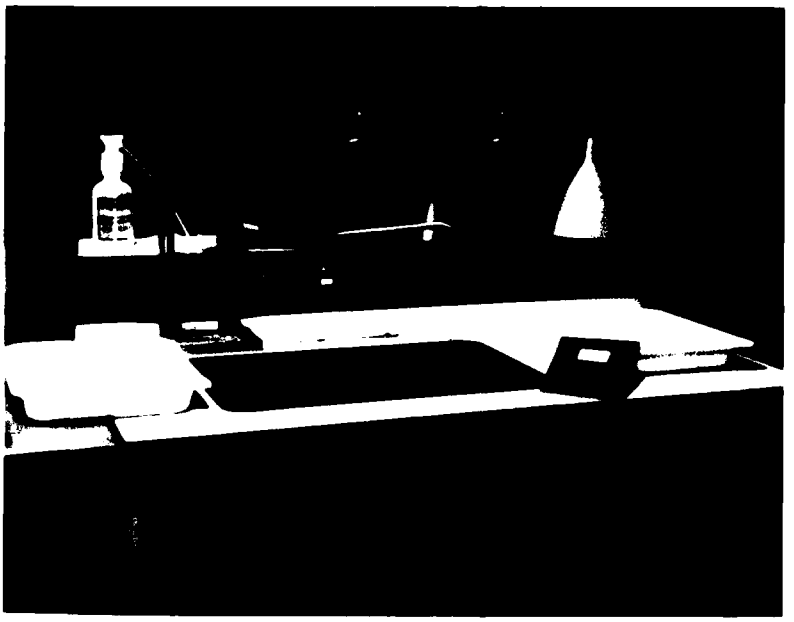


FIGURE 35. APPARATUS AND CHEMICALS FOR DEVELOPING BLACK-AND-WHITE SHEET FILM

TABLE XIV

MANUAL PROCESSING OF KODAK BLACK-AND-WHITE FILMS

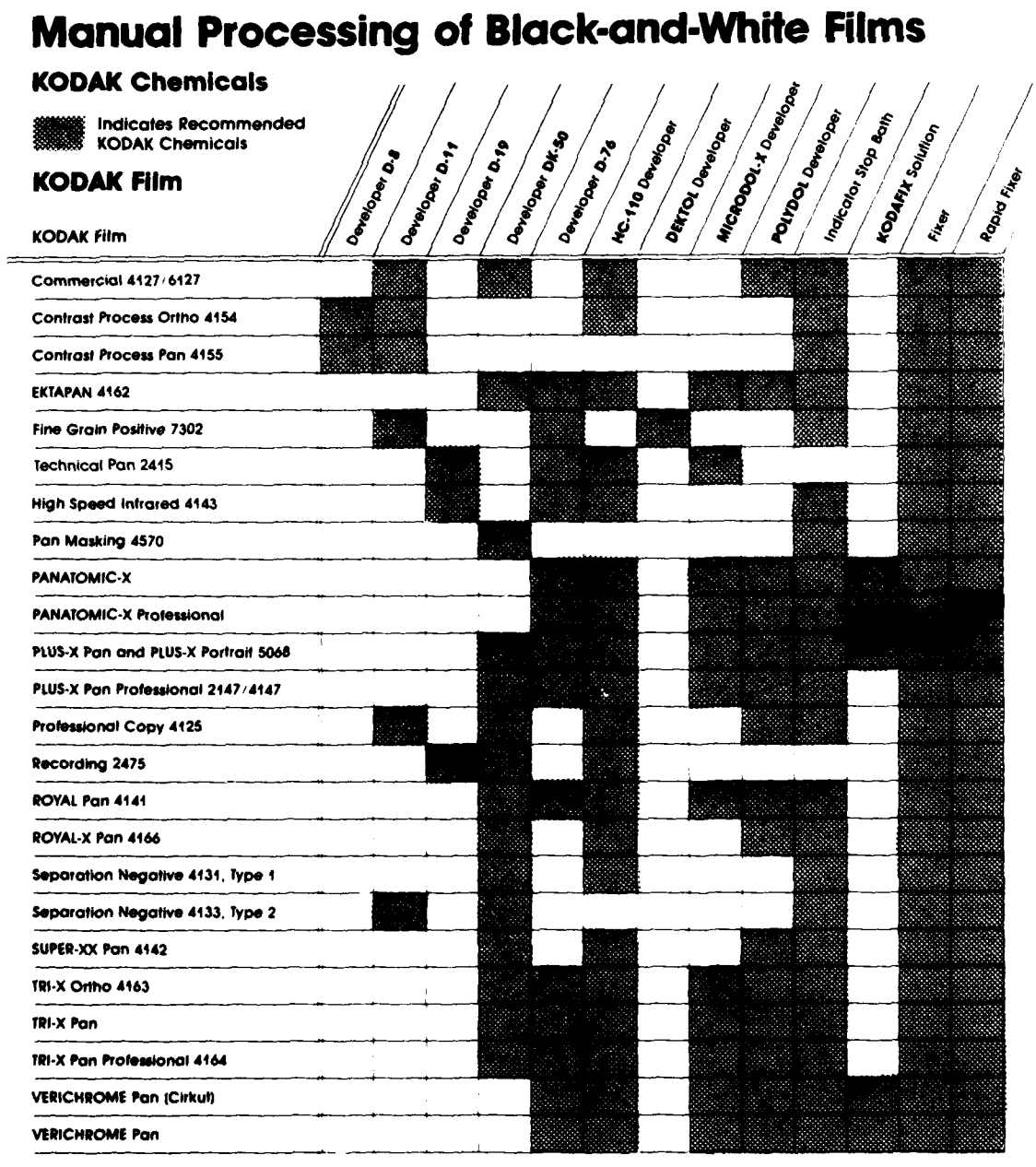


TABLE XIV

MANUAL PROCESSING OF KODAK BLACK-AND-WHITE FILMS (CONT'D)

KODAK Developers—major properties and uses

D-8	Extremely high contrast fast tray developer which produces high densities on process and continuous-tone films
D-11	High-contrast tray or tank developer for commercial and graphic arts work and for film positives and lantern slides
D-19	A high-capacity tank and tray developer that yields high-contrast negatives in short times. Suited to technical and scientific work
HC-110	A very versatile developer that comes in concentrated form. Dilution A provides short development times suitable for tray. Dilution B gives longer times with sharpness and grain similar to D-76 Developer. Other dilutions used in graphics arts
DK-50	Medium-activity, general-purpose developer for tank or tray with or without dilution. Excellent keeping characteristics and excellent tone reproduction with medium grain
POLYDOL	A long-life, high capacity, medium grain developer for sheet or roll films. Stable replenishment characteristics for consistent quality in sink line or production processing equipment
D-76	Produces maximum film speed and shadow detail with normal contrast and moderately fine grain. Gives long density scale and relatively low fog on forced development. Gives greater sharpness diluted 1:1. Excellent for roll films
MICRODOL-X	Gives finest grain with minimum speed loss with most films. Excellent choice for miniature films. Gives greater sharpness diluted 1:3; gives finer grain undiluted
VERSATOL	Handy, versatile, fast-working developer for films and papers. Good choice for small darkroom where finest grain is not required and exceptional keeping quantities are useful

TABLE XV

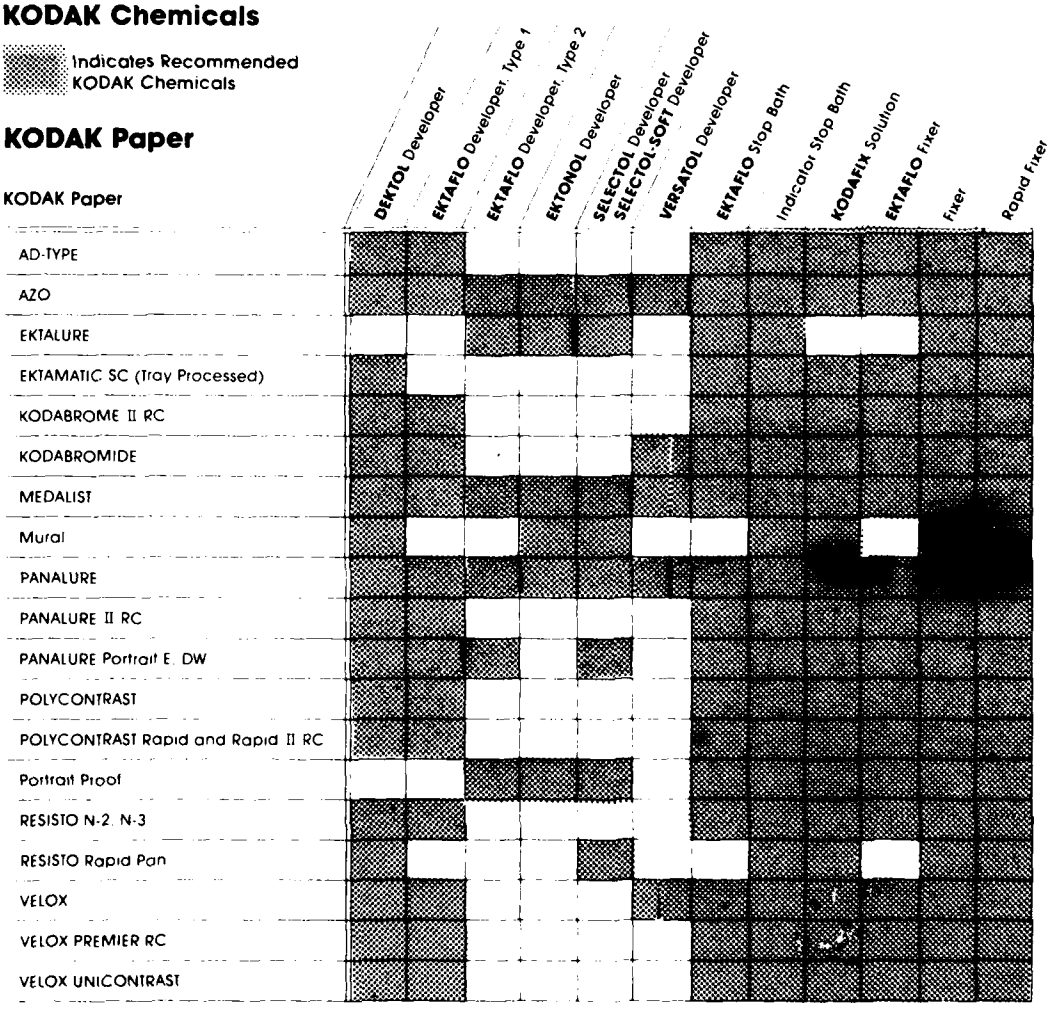
MANUAL PROCESSING OF KODAK BLACK-AND-WHITE PAPERS

Manual-Processing of KODAK Black-and-White Papers

KODAK Chemicals

Indicates Recommended KODAK Chemicals

KODAK Paper



KODAK Paper Developers—characteristics

DEKTOL	Yields neutral and cold tones on cold-tone papers
EKTAFLO, Type 1	A liquid concentrate with characteristics similar to those of DEKTOL
SELECTOL	For warm-tone papers and warmer tones on other papers
SELECTOL-SOFT	A companion to SELECTOL, gives lower contrast
EKTONOL	Specially designed for warm-tone papers which are to be toned
EKTAFLO, Type 2	A liquid concentrate with characteristics similar to those of EKTONOL
VERSATOL	An all-purpose developer for films, plates, and papers

TABLE XVI

KODAK EKTACHROME CHEMICALS AND PARAMETERS FOR PROCESS E-6

KODAK EKTACHROME Chemicals for Process E-6

Process E-6 was developed for the processing of KODAK EKTACHROME Films introduced in the past several years. The Process E-6 chemicals are available in convenient kit form.

The KODAK EKTACHROME Film Processing Kit, Process E-6, contains first developer, reversal bath, color developer, conditioner, bleach, fixer, and stabilizer.

All chemicals are supplied as easy-to-mix concentrates, ready to dilute and use. They are available separately in larger concentrate quantities.

Process E-6 offers uniformity and process stability for consistently high quality results without frequent adjustment of the process. It meets expected environmental requirements and, when operated to capacity, uses less water and energy than earlier processes.

Using Porcess E-6, roll films can be processed in 1 pint tanks, sink lines, and automatic processors. Sheet films can be processed in sink lines and automatic processors. Following is a Process E-6 summary of steps for 1 pint tanks:

Process E-6 Summary of Steps (for 1-Pint Tanks)

Solution or Procedure	Agitation and Remarks	Temperature		Time in Minutes	Total Time at End of Step
		°C	°F		
1 First Developer	First 4 steps in total darkness. Initial and subsequent agitation in first 3 steps	37.8 ± 0.3	100 ± ½	7	7[1]
2 Wash[2]		33-39	92-102	1	8
3 Wash[2]		33-39	92-102	1	9
4 Reversal Bath	Initial only	24-39	75-102	2	11
Remaining steps can be done in normal room light.					
5 Color Developer	Initial and subsequent agitation	37.8 ± 1.1	100 ± 2	6	17
6 Conditioner	Initial only	24-39	75-102	2	19
7 Bleach	Initial and subsequent agitation	33-39	92-102	7	26
8 Fixer	Initial and subsequent agitation	33-39	92-102	4	30
9 Wash (running water)	Initial and subsequent agitation	33-39	92-102	6	36
10 Stabilizer	Initial only	33-39	92-102	1	37
11 Dry	Remove film from reels. Temperature should not exceed 49 C (120 F)				

NOTES: [1] For initial films through a 1 pint set of solutions. See instruction sheet for times of subsequent films through the same set of solutions.

[2] Still water washes. Alternate wash in running water for 2 minutes.

TABLE XVII

KODAK FLEXICOLOR CHEMICALS AND PARAMETERS FOR PROCESS C-41

KODAK FLEXICOLOR Chemicals for Process C-41

Process C-41 is recommended for the processing of KODACOLOR II, KODACOLOR 400 and KODAK VERICOLOR II Professional Films. Developed to produce color negatives of uniformly high quality, it makes use of a number of KODAK FLEXICOLOR Chemicals, available either separately or in convenient kit form.

The KODAK FLEXICOLOR Processing Kit (for Process C-41) includes developer, bleach, fixer and stabilizer in quantities sufficient to make one pint of solution. The individual chemicals are available for larger amounts of solution.

The chemicals for Process C-41 can be used in small 1-pint tanks, rotary tubes, sink-line processing equipment, and continuous machines. Following is a summary of steps for processing KODACOLOR II, KODACOLOR 400, and KODAK VERICOLOR II Professional Films, using the processing kit.

Process C-41 Summary of Steps (for 1-Pint Tanks)

Solution or Procedure	Remarks	Agitation			Temperature		Time in Minutes②
		Initial①	Rest	Agitate	°C	°F	
1. Developer	Total darkness	30 sec	13	2	37.8 ± 0.15	100 ± ¼	3¼
2. Bleach		30 sec	25	5	24-40 ± 5	75-105	6½
Remaining steps can be done in normal room light.							
3. Wash	Running water③				24-40 ± 5	75-105	3¼
4. Fixer		30 sec	25	5	24-40 ± 5	75-105	6½
5. Wash	Running water③				24-40 ± 5	75-105	3¼
6. Stabilizer		30 sec			24-40 ± 5	75-105	1½
7. Dry	See instructions				24-43 ± 5	75-110	10-20

NOTES ① Rap the bottom of the tank firmly on the sink or table to dislodge any air bells. Be sure you have read the agitation recommendations elsewhere in these instructions.

② Includes 10-second drain time in each step.

③ Use fresh-water changes throughout the wash cycles. Fill the processing tank as rapidly as possible from a running water supply for about 4 seconds. When full, agitate vigorously for about 2 seconds and drain for about 10 seconds. Repeat this full wash cycle. If desired, use a running water inflow overflow wash with the cover removed from the tank.

TABLE XVIII

KODAK EKTAPRINT 2 CHEMICALS AND PARAMETERS FOR PROCESSING KODAK EKTACOLOR 74 AND 78 RC PAPERS

KODAK EKTAPRINT 2 Chemicals for Processing KODAK EKTACOLOR 74 and 78 RC Papers

These chemicals can be used in baskets, trays, and tanks for two-solution processing of EKTACOLOR 74 RC Paper. The KODAK EKTAPRINT 2 Processing Kit contains a developer and a bleach-fix in concentrated form to make 1- or 3½-gallon solutions. These and other EKTAPRINT 2 Chemicals are also available separately and in larger concentrate quantities.

Drum and tube-type processors used for processing EKTACOLOR RC Papers require KODAK EKTAPRINT 300 Developer.

Three-solution processing can be employed, if desired, with the addition of KODAK EKTAPRINT 3 Stabilizer and Replenisher.

Following is a summary of steps for tray and basket processing of KODAK EKTACOLOR 74 and 78 RC Papers. (Tube processing calls for a prewet step before developer step to help prevent streaking.)

Summary of Steps for Tray and Basket Processes

Solution or Procedure	Remarks	Temperature		Time in Minutes[1]	Time at End of Step	
		C	F			(w/optional steps)
1 Developer	No. 13 Safelight Filter (use 7½-watt bulb)	33 0 3	91 ½	3½	3½	
(Optional steps[2]) a. C-22 Stop Bath	Agitate as described	30-34	86-93	1		(4½)
b Wash	Running water			1		(5½)
2 Bleach-Fix	–	30-34	86-93	1½	5	(7)
Remaining steps can be done in normal room light						
3 Wash	Running water	30-34	86-93	3½	8½	(10½)
4 Dry	Air-dry—don't ferrotype!	Not over 107	Not over 225			

NOTES [1] Include a 20-second drain time in each process step. Baskets of complex design can be drained for 30 seconds to prevent excessive carry-over.

[2] The optional steps are suggested if marks or streaks are observed on the surface of prints. Excessive developer carry-over and inadequate agitation are usually responsible for such marks.

TABLE XIX

KODAK EKTAPRINT R-1000 CHEMICALS AND PARAMETERS
FOR PROCESSING KODAK EKTACHROME 2203 PAPER

KODAK EKTAPRINT R-1000 Chemicals for Processing KODAK EKTACHROME 2203 Paper

These chemicals are specifically intended for processing KODAK EKTACHROME 2203 Paper in tube-type or drum processors (such as KODAK Rapid Color Processors). They are available separately in sizes for making 1-gallon solutions.

KODAK EKTACHROME 2203 Paper can also be processed in continuous processing machines, using EKTAPRINT R-100 Chemicals.

Following is a summary of steps for processing EKTACHROME 2203 Paper in the KODAK Rapid Color Processor, Models 11 and 16-K.

Summary of Steps for Processing in the KODAK Rapid Color Processor, Model 11 or 16-K

Drum Temperature	First Developer Solution	38 ± 0.3 C (100 ± 0.5 F)
	Other Solutions	38 ± 1.0 C (100 ± 2 F)
	Washes and Presoak	36 to 40 C (97 to 104 F)

(Total wet processing time—12¾ minutes)

Processing Step	Remarks	Time in Min①	Total Min Used at End of Step	Total Min Left at End of Step
1. Prewet	In tray of water—total darkness②	1	1½	11¼
2. First Developer	Total darkness	1½	3	9¾
3. Stop Bath	Total darkness	½	3½	9¼
4. First Wash	Use safelight No. 10 or OA	2	5½	7¼
5. Color Developer	Use safelight No. 10 or OA	2	7½	5¼
Remaining steps can be done in normal room light				
6. Second Wash	—	½	8	4¾
7. Bleach-Fix	—	2½	10½	2¼
8. Final Wash	—	1½	12	¾
9. Stabilizer	—	½	12½	¼
10. Rinse	—	¼	12¾	0
11. Dry	See instructions 49 to 71°C (120 to 160°F)	—	—	—

NOTES: ① The time for each step, except the prewet, includes a 5-second drain time. The drain time after the prewet should be 30 seconds. In each case, start draining in time to end the processing step and start the next one on schedule.

② Agitate frequently. Do not handle the dry print with wet fingers or the wet print with dry fingers.

Important: After each process, rinse blanket, drum, and tray with running water to remove all traces of processing chemicals. Wipe excess water from drum and tray before starting next process.

Text continued from page III-L-64.

reports. An excellent reference that gives full details on techniques and setups can be found in reference 13, which directs the reader specifically to Kodak Publication No. M-1, Copying.

Copying setups consist basically of a copy board, with optional transmitted light source for copying transparencies or slides, light sources, an upright column, and a camera. The camera can be either 35mm or Polaroid. However, if Polaroid film is to be used, a ground glass should be used for the purposes of accurate focus.

Actually, the equipment described in the section on Photomacrography in this chapter is usually suitable for photocopying.

Figure 36 shows a copying setup arranged with the former Kodak Precision Enlarger, incorporating a camera back. Note the sheet of black paper used in this particular copying operation to prevent reflection from the opposing shiny page.

As mentioned above, focus is all-important in copying, and for this reason 35mm SLR cameras are most popular on copying setups. Polaroid cameras should employ a ground glass for sharp focus, generally necessitating the need for sheet film. If a range finder camera is the only camera available, there is a way to avoid the guesswork in focusing. If the camera back is opened, a piece of ground glass placed in the position normally occupied by the film, and the shutter set on time exposure, the image can be accurately focused.

If a copying stand is not available, an improvised setup can be made with a regular tripod. A plumb bob can be attached to the camera for centering the lens, and a small level can be used to keep the film plane parallel with the subject plane. Figure 37 shows such an apparatus.

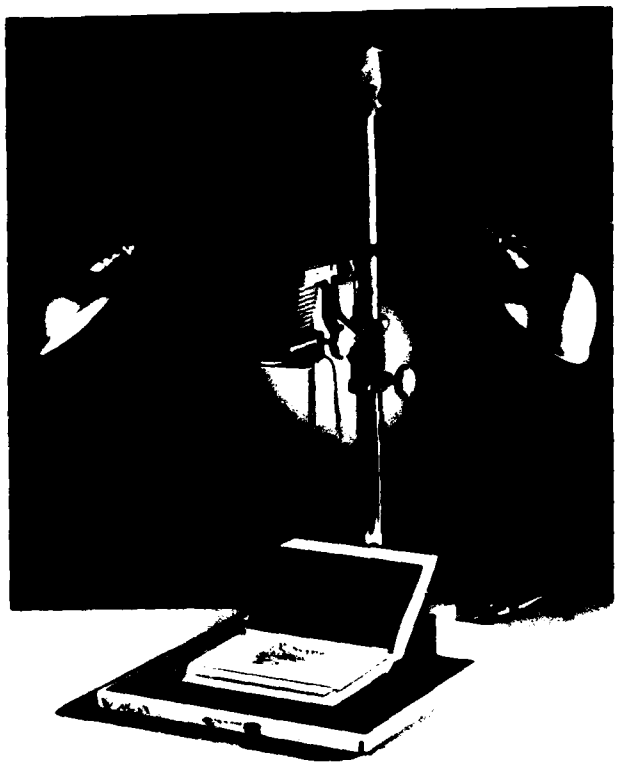


FIGURE 36. COPYING STAND UTILIZING THE FORMER KODAK PRECISION ENLARGER INCORPORATING A CAMERA BACK

Uniform illumination over the entire field is one of the most important considerations in copying. Improper lighting causes negatives to have uneven density, and such negatives are difficult to print. Small originals (up to 8 x 10 inches) can be satisfactorily illuminated by two lamps of equal intensity placed about 30 inches from the copyboard at an angle of 45 degrees to the lens axis. Figure 38 demonstrates this lighting setup.

a. Films for Copying. The nature of the material being copied must be taken into account when choosing a film. A distinction must be made between line copy and continuous-tone originals. The

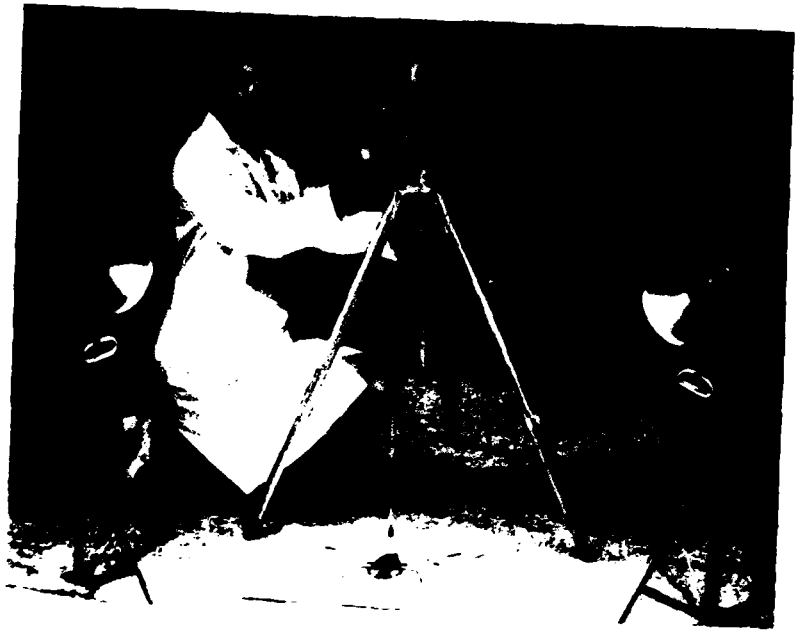


FIGURE 37. IMPROVISED COPY STAND USING REGULAR TRIPOD

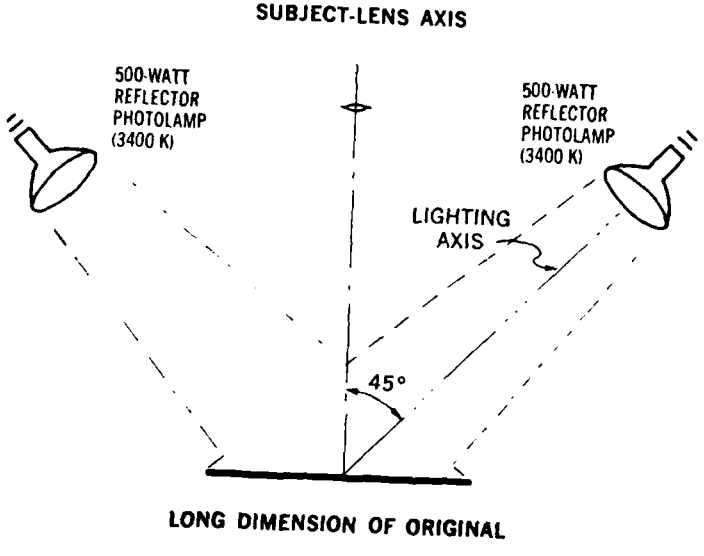


FIGURE 38. OPTIMUM ILLUMINATION SETUP FOR COPYING SMALL ORIGINALS

former requires a high-contrast film, while the latter requires a film more of the pictorial type. Table XX may be useful when making black-and-white copies.

TABLE XX

KODAK PANCHROMATIC BLACK-AND-WHITE FILMS FOR COPYING

Original	KODAK Sheet Film	KODAK Roll Film
Line*	Contrast Process Pan Film 4155 (ESTAR Thick Base)	High Contrast Copy Film 5069
Continuous Tone	Professional Copy Film 4125 (ESTAR Thick Base) PLUS-X Pan Professional Film 4147 (ESTAR Thick Base)	PLUS-X Pan Professional Film 2147 (ESTAR Base)
Combination	Professional Copy Film 4125 (ESTAR Thick Base)	PLUS-X Pan Professional Film 2147 (ESTAR Base)

*Overexposure must be avoided or the finest lines will not be recorded.

Color originals can be copied with regular color films, but the illumination must be of the proper color temperature for the chosen film.

Polaroid Types 46-L and 146-L transparency film can be used to make either transparencies or slides (by cutting the film down). The Polaroid Dippit #646 is used to develop and set the transparency.

12. External Visual Inspection (Method 2009.1, MIL-STD-883). See Appendix A.

13. Internal Visual Inspection (Methods 2010.3 and 2017.1, MIL-STD-883). See Appendix B.

APPENDIX A

METHOD 2009.1

EXTERNAL VISUAL

1. PURPOSE. The purpose of this examination is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. This test would normally be employed at the outgoing inspection from the device manufacturer's facility or as an incoming user inspection.

2. APPARATUS. Apparatus used in this test shall be capable of demonstrating device conformance to the applicable requirements, which may include optical equipment capable of magnification between 3X and 10X and a relatively large and accessible field of view such as an illuminated ring magnifier.

3. PROCEDURE. The device shall be examined under a magnification of between 3X and 10X (unless otherwise specified) with a field of view sufficiently large to contain the entire device in accordance with the requirements of the applicable procurement specification and the criteria listed in 3.1. Where adherence of foreign material is in question, devices may be subjected to a clean filtered air stream (suction or expulsion) of 88 feet per second maximum, and reinspected.

3.1 Failure criteria. Devices shall be considered to fail if they exhibit the following:

(a) Device design, lead identification, markings (content, placement, and legibility), materials, construction, and workmanship are not in accordance with the applicable specification.
(b) Defects or damage resulting from manufacturing, handling or testing.
(c) Visible evidence of corrosion, contamination or breakage (grossly bent or broken leads, cracked seals (except for glass meniscus)), defective (peeling, flaking, or blistering) or damaged plating. (Discoloration of the finish shall not be cause for failure unless there is evidence of flaking, pitting, or corrosion.)
(d) Leads which are not intact and aligned in their normal location, free of sharp or unspecified lead bends, and (for ribbon leads) free of twist outside the normal lead plane.
(e) Leads which are not free of foreign material such as paint or other adherent deposits, or dust.
(f) Other defects or features which will interfere with the normal application of the device.
(g) Evidence of any nonconformance with the detail drawing or applicable procurement document, absence of any required feature, or evidence of damage, corrosion, or contamination which will interfere with the normal application of the device.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Requirements for markings and the lead or pin identification (see 3).
(b) Detailed requirements for materials, design, construction, and workmanship (see 3).
(c) Magnification if other than specified in 3.

APPENDIX B

METHOD 2010.3

INTERNAL VISUAL (MONOLITHIC)

1. PURPOSE. The purpose of this test is to check the internal materials, construction, and workmanship of microcircuits for compliance with the requirements of the applicable procurement document. This test will normally be used prior to capping or encapsulation on a 100 percent inspection basis to detect and eliminate devices with internal defects, that could lead to device failure in normal application. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices. Complex microcircuits may require substitution of alternate screening procedures for visual inspection criterion pertaining to metal coverage, oxide, and diffusion faults that are difficult or impractical to perform. These alternate screening methods and procedures are documented in Method 5004, and their use shall be on an optional basis. Test condition A provides a rigorous and detailed procedure for internal visual inspection intended for high reliability class S microcircuits. Test condition B provides procedures for internal visual inspection intended for classes B and C microcircuits (classes of microcircuits refer to screening requirements of Method 5004).

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (gages, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

3. PROCEDURE.

a. General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable procurement document and the criteria of the specified test condition. For nonJAN devices if a specified visual inspection requirement is in conflict with circuit design topology or construction, it shall be documented and specifically approved by the procuring activity. For JAN devices there shall be no waivers. The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device process or technology, it has been indicated.

b. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Visual criteria specified in 3.1.1.2, 3.1.1.5, 3.1.1.7, 3.1.2, 3.1.7 e and f, 3.1.8, 3.1.9 a through d, and 3.2.1.2, 3.2.1.5, 3.2.1.7, 3.2.2, 3.2.7 e and f, 3.2.8, 3.2.9 a, b, and d may be examined prior to die attachment without required reexamination after die attachment. Visual criteria specified in 3.1.6.2, 3.1.6.3, 3.2.6.2, and 3.2.6.3 may be examined prior to bonding without reexamination after bonding. Visual criteria specified in 3.2.1.1 and 3.2.3 may be examined prior to die attachment at "high magnification" provided they are reexamined after die attachment at "low magnification." When inverted mounting techniques are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to attachment of the die.

c. Inspection control. In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections per 3 b, to insure that defects created during subsequent handling will be detected and rejected at final preseal inspection. During the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment. Devices examined to 3.1

criteria shall be inspected and prepared for sealing in a class 100 environment and devices examined to 3.2 criteria shall be inspected and prepared for sealing in a class 100,000 environment per Federal Standard 209, except that the maximum allowable relative humidity shall not exceed 65 percent. Devices shall be in covered containers when transferred from one controlled environment to another.

d. Magnification. "High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination normal to the die surface. "Low magnification" inspection shall be performed with either a monocular, binocular, or stereomicroscope, and the inspection performed within an angle of 30 degrees from the perpendicular to the die surface with the device under suitable illumination. The inspection criteria of 3.1.4, 3.2.4, and 3.2.6.1 may be examined at "high magnification" at the manufacturer's option.

e. Reinspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the procurement document. Where sampling is used rather than 100 percent reinspection, 6.4 of MIL-M-38510 shall apply.

f. Exclusions. Where conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.

g. Definitions:

1. Active circuit area includes all areas of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.
2. Controlled environment shall be in accordance with the requirements of Federal Standard 209 class 100 environment for air cleanliness and humidity, except that the maximum allowable relative humidity shall not exceed 50 percent. The use of an inert gas environment such as nitrogen shall satisfy the requirements for storing in controlled environment.
3. Diffusion tub is an isolated volume of semiconductor material, either "P" or "N" type, surrounded by isolation material.
4. Foreign material is defined as any material that is foreign to the microcircuit or any non-foreign material that is displaced from its original or intended position within the microcircuit package and shall be considered attached when it cannot be removed by a nominal gas blow (approximately 20 psig). Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles shall be considered embedded in the glassivation when there is evidence of color fringing around the periphery of the particle.
5. Functional circuit elements are diodes, transistors, crossunders, capacitors, and resistors.
6. Gate oxide bridge is the area lying between the drain and source diffusions of MOS structures. References to the metallization covering the gate oxide bridge shall include all materials that are used for the gate electrode.
7. Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area including metallization, except bonding pads and beam leads. Crazing is the presence of minute cracks in the glassivation.
8. Junction is the outer edge of a passivation step that delineates the boundary between "P" and "N" type semiconductor material.

9. Multilayered metallization (conductors) is two or more layers of metal or any other material used for interconnections that are not isolated from each other by a grown or deposited insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.
10. Multilevel metallization (conductors) is two or more layers of metal or any other material used for interconnections that are isolated from each other by a grown or deposited insulating material.
11. Operating metallization (conductors) is all metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.
12. Organic polymer (epoxy) vapor residue is the material that is emitted from the polymer, that forms on an available surface.
13. Original width is the width dimension or distance that is intended by design (e.g., original metal width, original diffusion width, original beam width, etc.,).
14. Passivation step is a change in thickness of the passivation for metal to metal or metal to silicon interconnection, by design, excluding lines on the surface where passivation layers have been removed as a result of normal device processing.
15. Passivation is the silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal.
16. Peripheral metal is all metal that lies immediately adjacent to or over the scribe grid.
17. Thick film is that conductive/resistive/dielectric system that is a film having greater than 50,000 angstroms thickness.
18. Thin film is that conductive/resistive/dielectric system that is a film equal to or less than 50,000 angstroms in thickness.
19. Substrate is the supporting structural material into and/or upon which the passivation, metallization and circuit elements are placed.

h. Interpretations. For inspections performed in the range of 75X to 100X, the criteria of "0.1 mil of passivation, separation, or metal" can be satisfied by a "line of separation" or a "line of metal." Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used for confirming that a reject condition does not exist, they shall be approved by the procuring activity.

3.1 Test condition A. Internal visual examination as required in 3.1.1 through 3.1.6 shall be conducted on each microcircuit and each integrated circuit chip. In addition, the applicable criteria contained in 3.1.7 through 3.1.9 shall be used for the appropriate microcircuit areas where glassivation, dielectric isolation or film resistors are used. The "high magnification" inspection shall be within the range of 100X to 200X, the "low magnification" within the range of 30X to 60X.

3.1.1 Metallization defects "high magnification." No device shall be acceptable that exhibits the following defects in the operating metallization:

3.1.1.1 Metallization scratches. A scratch is any tearing defect including probe marks in the surface of the metallization:

a. Scratch in the metallization excluding bonding pads and beam leads that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-1).
b. Scratch in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

c. Scratch in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.
d. Scratch in the metallization, over the gate oxide bridge (see figure 2010-3) (applicable to MOS structures).
e. Scratch in multilayered metallization excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 75 percent of the original metal width undisturbed (see figure 2010-1).

3.1.1.2 Metallization voids. A void is any region in the metallization where underlying metal or passivation is visible that is not caused by a scratch.

a. Void(s) in the metallization that leaves less than 75 percent of the original metal width undisturbed (see figure 2010-2).
b. Void(s) in the metallization over the gate oxide bridge that leaves less than 75 percent of the metallization length (L) and width (W) between source and drain diffusions undisturbed (see figure 2010-3) (applicable to MOS structures).
c. Void(s) that leave less than 75 percent of the metallization area over the gate oxide bridge undisturbed (applicable to MOS structures).
d. Void(s) in the bonding pad area that leaves less than 75 percent of its original unglassivated metallization area undisturbed.
e. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 75 percent of the narrowest entering interconnect metallization stripe width (see figure 2010-4).
f. Void(s) in the metallization area of a thin film capacitor that reduces the metallization area by more than 25 percent.

3.1.1.3 Metallization corrosion. Any metallization corrosion. Metallization having any localized discolored area shall be closely examined and rejected unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.

3.1.1.4 Metallization adherence. Any metallization lifting, peeling, or blistering.

3.1.1.5 Metallization probing. Criteria contained in 3.1.1.1 shall apply as limitations on probing damage.

3.1.1.6 Metallization bridging. Any metallization bridging where the separation between any two metallization paths is reduced to less than 50 percent of the original separation or 1.0 mil whichever is less. In no case shall this separation be less than 0.1 mil.

3.1.1.7 Metallization alignment.

a. Contact window that has less than 75 percent of its area covered by metallization.
b. Contact window that has less than a continuous 50 percent of its perimeter covered by metallization.
c. Contact window that has less than 75 percent of its perimeter on two adjacent sides covered by metallization (applicable to MOS structures)
NOTE: When by design, metal is completely contained in a contact window, criteria 3.1.1.7 b and c perimeter coverage can be deleted.
d. A metallization path not intended to cover a contact window that is separated from the window by less than 0.25 mil. When this requirement exceeds 50 percent of the original separation, the minimum separation shall be 0.1 mil.

e. Any exposure of the gate oxide bridge from source to drain diffusion (applicable to MOS structure) (see figure 2010-5).
f. Any exposure of the gate oxide bridge that leaves less than 75 percent of the metallization coincident with the source and drain diffusion junction line undisturbed (applicable to MOS structures).
g. Gate metallization not coincident with or extending over the diffused guard ring.
NOTE: Criteria 3.1.1.7 g applies to MOS structures containing a diffused guard ring. MOS devices that do not have a diffused guard ring shall have gate metallization extending not less than 0.1 mil beyond the gate oxide bridge (see figures 2010-3 and 2010-5).

3.1.2 Diffusion and passivation layer(s) faults "high magnification." No device shall be acceptable that exhibits the following:

3.1.2.1 Diffusion faults:

a. Any diffusion fault that allows bridging between diffused areas (see figure 2010-6).
b. Any isolation diffusion that is discontinuous or any other diffused area with less than 25 percent (50 percent for resistors) of the original diffusion width that remains (see figure 2010-6).

3.1.2.2 Passivation faults:

a. Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization (see figure 2010-7).
NOTE: Double or triple lines at the edge of the defect indicate it can have sufficient depth to penetrate down to bare silicon.
b. Active junction not covered by passivation, unless by design.
c. Contact window that extends across a junction, unless by design.

3.1.3 Scribing and die defects "high magnification." No device shall be acceptable that exhibits:

a. Less than 0.25 mil of passivation visible between operating metallization or bond periphery and edge of the die.
NOTE: Criteria of 3.1.3 a can be excluded for beam leads and peripheral metallization including bonding pads where the metallization is at the same potential as the die.
b. A chipout or crack in the active circuit area (see figure 2010-8).
c. A crack that exceeds 3.0 mil in length or comes closer than 0.25 mil to any operating metallization, or other functional circuit element (see figures 2010-8 and 2010-9).
d. Semicircular crack terminating at the die edge whose chord is equal to or greater than 75 percent of the narrowest separation between unglassivated metallization (see figure 2010-8).
e. Exposed silicon extending over the passivation edge at the point of the beam lead exit from the die (see figure 2010-9) (applicable to beam lead structures).
f. Die having attached portions of the active circuit area of another die.
g. A crack that exceeds 1.0 mil in length inside the scribe grid, scribe line. or silicon edge for beam lead devices that point toward operating metallization or functional circuit elements.
NOTE: Criteria of 3.1.3 b, c, and h can be excluded for beam lead devices where the chip-out or crack does not extend into the silicon material.
h. A crack that comes closer than 0.5 mil to operating beam lead metallization (see figure 2010-9).

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3.1.4 Bond inspection "low magnification." This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above.

NOTE: Wire tail is not considered part of the bond when determining physical bond dimensions (see figure 2010-10).

3.1.4.1 Gold ball bonds. No device shall be acceptable that exhibits:

a. Gold ball bonds on the die or package post wherein the ball bond diameter is less than 2.0 times or greater than 5.0 times the wire diameter.
b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.
c. Gold ball bonds where the wire center exit is not within the boundaries of the bonding pad.
d. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.

3.1.4.2 Wedge bonds. No device shall be acceptable that exhibits:

a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or more than 3.0 times the wire diameter in width, or are less than 1.5 times or more than 5.0 times the wire diameter in length (see figure 2010-10).
b. Thermocompression wedge bonds on the die or package post that are less than 1.5 times or more than 3.0 times the wire diameter in width or are less than 1.5 times or more than 5.0 times the wire diameter in length (see figure 2010-10).

3.1.4.3 Tailless bonds (crescent). No device shall be acceptable that exhibits:

a. Tailless bonds on the die or package post that are less than 1.2 times or more than 5.0 times the wire diameter in width, or are less than 0.5 times or more than 3.0 times the wire diameter in length (see figure 2010-10).
b. Tailless bonds where bond impression does not cover the entire width of the wire.

3.1.4.4 General (gold ball, wedge, and tailless). As viewed from above, no device shall be acceptable that exhibits:

a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area.
b. Wire bond tails that extend over or make contact with any metallization not covered by glassivation and not connected to the wire.
c. Wire bond tails that exceed two wire diameters in length.
d. Bonds on the package post that are not completely within the boundaries of the package post.
e. Rebonding.
f. Bonds placed so that the separation between bonds is less than 1.0 mil, excluding bonds connected by a common connector.
g. Bonds placed so that the separation between the bond and unglassivated metallization not connected to it is less than 1.0 mil. Where such requirements exceed the minimum unglassivated metal spacing and for glassivated metallization, the minimum separation between the bond and glassivated or unglassivated metallization not connected to it shall not be less than 0.25 mil.

h. Bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metallization visible between the periphery of the bond and at least one side of the entering metallization (see figure 2010-11).

NOTE: Criteria 3.1.4.4 h can be excluded when the entering metallization strip is greater than 2.0 mils in width and the bond pad dimension on the entering metal stripe side is greater than 3.5 mils.

i. Bonds where more than 25 percent of the bond is located in an area containing die preform mounting material.
j. Bonds placed so that the wire exiting from the bond crosses over another bond.
k. Any evidence of rebonding or repair of conductors by bridging with or addition of bonding wire or ribbon.

3.1.4.5 Beam lead. This inspection and criteria shall apply to the completed bond area made using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:

a. Bonds where the tool impression does not completely cross the entire beam width.
b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15 percent (10 percent for compliant bonds) or greater than 75 percent of the undeformed beam width.
c. Bonds where the tool impression length is less than 1.0 mil (see figure 2010-12).
d. Bonding tool impression less than 1.0 mil from the die edge (see figure 2010-13).
e. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see figure 2010-12).
f. Cracks or tears in the effective bonded area of the beam greater than 50 percent of the original beam width.
g. Bonds placed so that the separation between bonds and between bonds and operating metallization not connected to them is less than 0.1 mil.
h. Bonds lifting or peeling.

3.1.5 Internal leads "low magnification." This inspection and criteria shall be required inspection for the lead type(s) and location(s) to which they are applicable when viewed from above.

3.1.5.1 Wires. No device shall be acceptable that exhibits:

a. Any wire that comes closer than two wire diameters to unglassivated operating metallization, another wire (common wires excluded), package post, unpassivated die area, or any portion of the package, including the plane of the lid to be attached.
NOTE: Within a 5.0 mils spherical radial distance from the perimeter of the bond on the die surface, the separation can be 1.0 mil.
b. Nicks, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.
c. Missing or extra lead wires.
d. Tearing at the junction of the wire and bond.
e. Any wire making a straight line run from die bonding pad to package post that has no arc.
f. Wire(s) crossing wire(s), except common conductors.
g. Wire(s) not in accordance with bonding diagram.

3.1.5.2 Beams. No device shall be acceptable that exhibits the following:

a. Voids, nicks, depressions, or scratches that leave less than 50 percent of the beam width undisturbed.
b. Beam separation from the die.
c. Missing or partially fabricated beam leads unless by design.
d. Beam leads that are not bonded.
e. Bonded area closer than 0.1 mil to the edge of the passivation layer.
f. Less than 0.1 mil passivation layer between the die and the beam visible at both edges of the beam (see figures 2010-9 and 2010-12).

3.1.6 Package conditions (magnification as indicated). No device shall be acceptable that exhibits:

3.1.6.1 Foreign material. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psig). The device shall then be inspected and be rejected when it exhibits the following:

NOTE: Die inspections shall be at "high magnifications" while package and lid inspection may be at "low magnifications."

a. Foreign particles on the surface of the die or within the package or on the lid or cap that is large enough to bridge the narrowest unglassivated operating metal spacing.
NOTE: Silicon chips shall be considered as foreign particles.
b. Embedded foreign particles in the die that bridge two metallization paths.
c. Liquid droplets, chemical stains or photoresist on the die surface that bridge any combinations of unglassivated metal or bare silicon areas.
d. Ink on the surface of the die that covers more than 25 percent of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon areas.
NOTE: As an alternative to 100 percent visual inspection of lids or caps per the criteria of 3.1.6.1 a, the lids or caps may be subjected to a suitable cleaning process and quality verification approved by the qualifying activity (procuring activity for nonJAN) provided the lids or caps are subsequently held in a controlled environment until capping or preparation for seal.

3.1.6.2 Die mounting "low magnification."

a. Die mounting material buildup that extends onto the top surface of the die or extends vertically above the top surface of the die.
b. Die to header mounting material not visible around at least two complete sides or 75 percent of the die perimeter, except for transparent die.
c. Transparent die with less than 50 percent of the area bonded.
d. Flaking of the die mounting material.
e. Balling of the die mounting material.

3.1.6.3 Die orientation. Die not located or oriented in accordance with the applicable assembly drawing of the device.

a. Die not located or oriented in accordance with the applicable assembly drawing of the device.
b. Die not level within 10 degrees with respect to the package cavity.

3.1.7 Glassivation defects, "high magnification." No device shall be acceptable that exhibits:

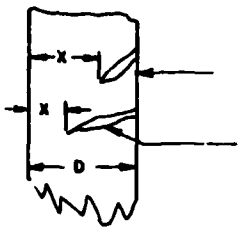
a. Glass crazing or glass damage that prohibits the detection of visual criteria contained herein.
b. Any lifting or peeling of the glassivation.
c. Two or more adjacent active metallization paths not covered by glassivation, excluding bonding pad cutouts.
d. Unglassivated areas greater than 5.0 mils in any dimension, unless by design.
e. Unglassivated areas at the edge of bonding pad exposing silicon.
f. Glassivation covering more than 25 percent of the bonding pad area.
g. Crazing over a film resistor.
h. Scratches in the glassivation that disturb metal and bridge metallization paths.
i. Cracks (not crazing) in the glassivation that form a closed loop over adjacent metallization paths.

3.1.8 Dielectric isolation "high magnification." No device shall be acceptable that exhibits:

a. A discontinuous isolation line (typically a black line) around each diffusion tub containing functional circuit elements.
b. Absence of a continuous isolation line between any adjacent tubs, containing functional circuit elements.
c. A diffused area which overlaps dielectric isolation material and comes closer than 0.1 mil to an adjacent diffusion tub; or an overlap of more than one diffusion area into the dielectric isolation material (see figure 2010-14).
d. A contact window that touches or overlaps dielectric material.
e. Metallization scratch and void defects over a dielectric isolation step shall be in accordance with criteria contained in 3.1.1.1 b and 3.1.1.2 b.

3.1.9 Film resistor, "high magnification." Rejection shall be based on defects found within the actively used portions of the film resistor. Metallization defect criteria of 3.1.1 shall apply. No device shall be acceptable that exhibits:

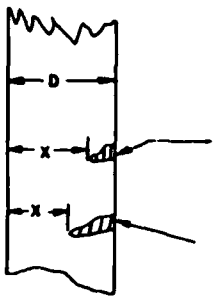
a. Any misalignment between the conductor/resistor in which the actual width X of the overlap is less than 50 percent of the original resistor width (see figure 2010-15).
b. Contact overlap between the metallization and film resistor in which the length dimension Y is less than 0.25 mil (see figure 2010-15).
c. Increase in resistor width greater than 25 percent of the original width.
d. Necking down that reduces the width of film resistor material at a terminal.
e. Void that leaves less than 75 percent of the film resistor undisturbed at a terminal.
f. Any sharp change in color of resistor material within 0.1 mil of the resistor/connector termination.
g. Inactive resistor inadvertently connected to two separate points on an active circuit.
h. Separation between any two resistors or a resistor and a metallization path that is less than 0.25 mil.
i. Any thin film resistor that crosses a substrate irregularity (e.g., dielectric isolation line, oxide/diffusion step, etc.,).



For single layer metal products

Accept - Scratch where the remaining undisturbed metal width (X) is greater than D/2. (50 PERCENT).

Reject - Scratch where the remaining undisturbed metal width (X) is less than D/2 (50 PERCENT).

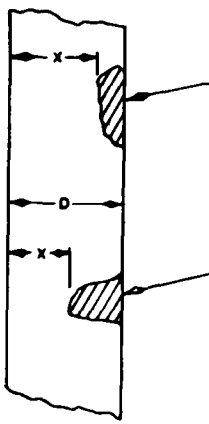


For multilayered metal products only.

Accept - Scratch exposing underlying metal or passivation where the remaining undisturbed metal width (X) is greater than 3/4 D (75 PERCENT).

Reject - Scratch exposing underlying metal or passivation where the remaining undisturbed metal width (X) is less than 3/4 D (75 PERCENT).

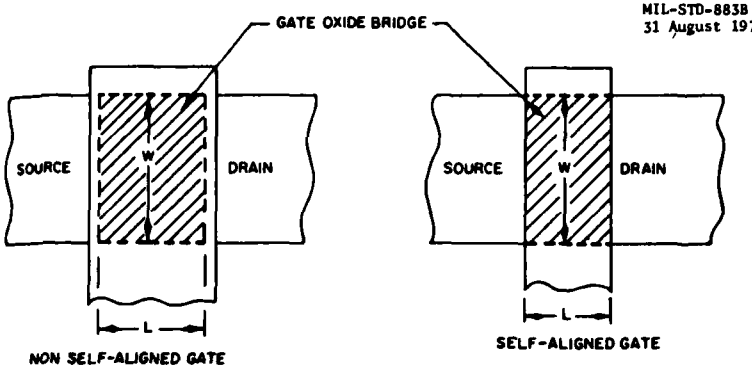
FIGURE 2010-1. Scratch criteria.



Accept - Void exposing underlying metal or passivation where the remaining undisturbed metal width (X) is greater than 3/4 D (75 percent)

Reject - Void exposing underlying metal or passivation where the remaining undisturbed metal width (X) is less than 3/4 D (75 percent)

FIGURE 2010-2. Void criteria.



NOTE: When standard metallization scratch and void criterion is applied to the gate area the dimension (W) and (L) shall be considered as the original channel width and length respectively.

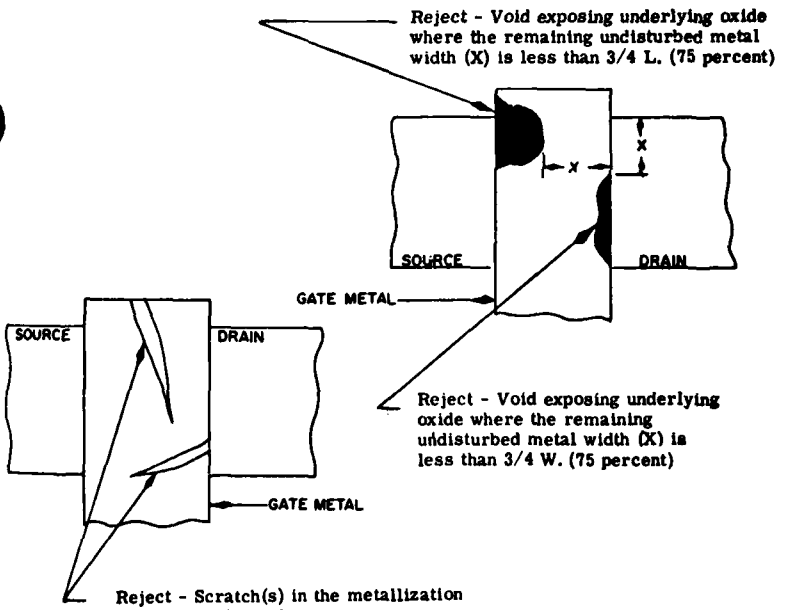


FIGURE 2010-3. MOS scratch and void criteria.

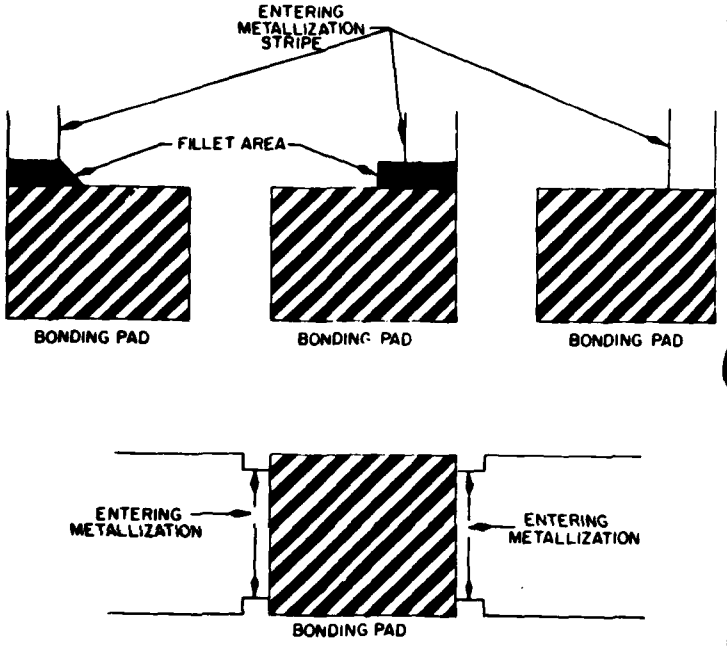


FIGURE 2010-4. Bonding pad areas.

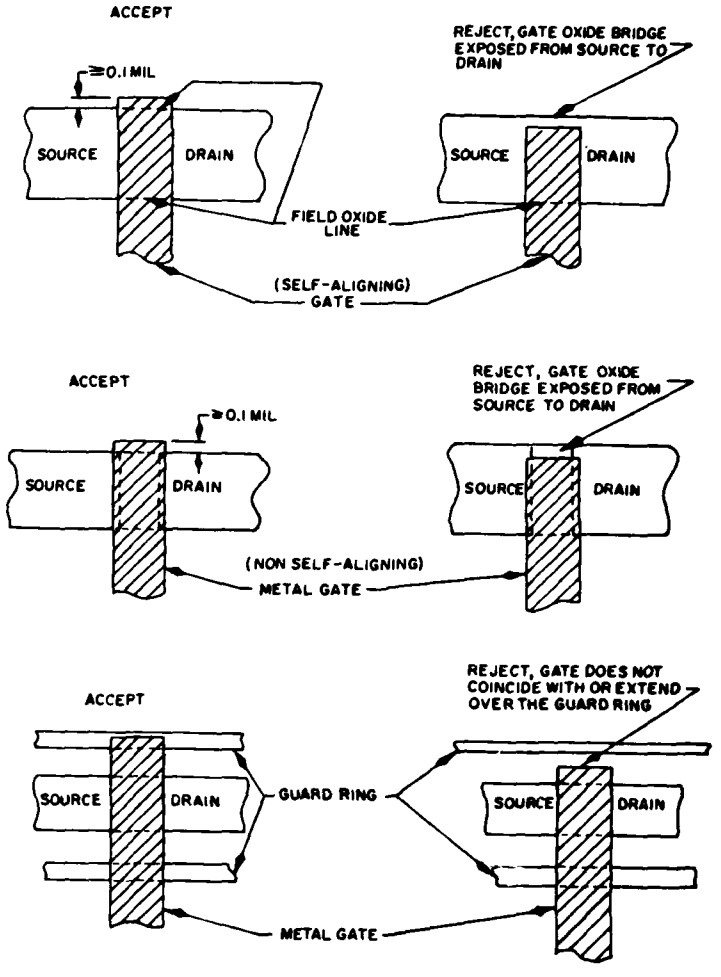


FIGURE 2010-5. MOS gate alignment.

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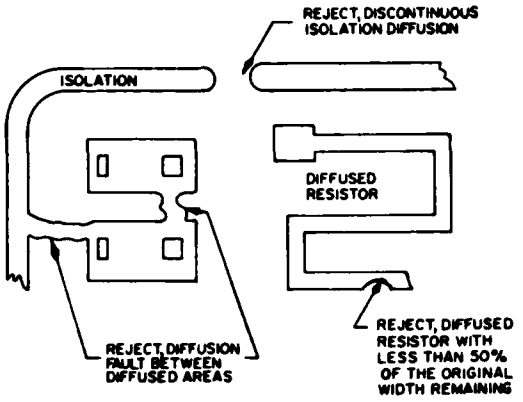


Figure 2010-6. Diffusion faults.

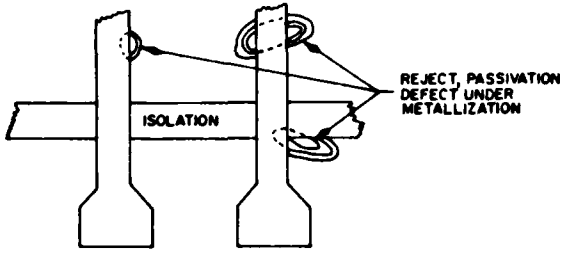


FIGURE 2010-7. Passivation faults.

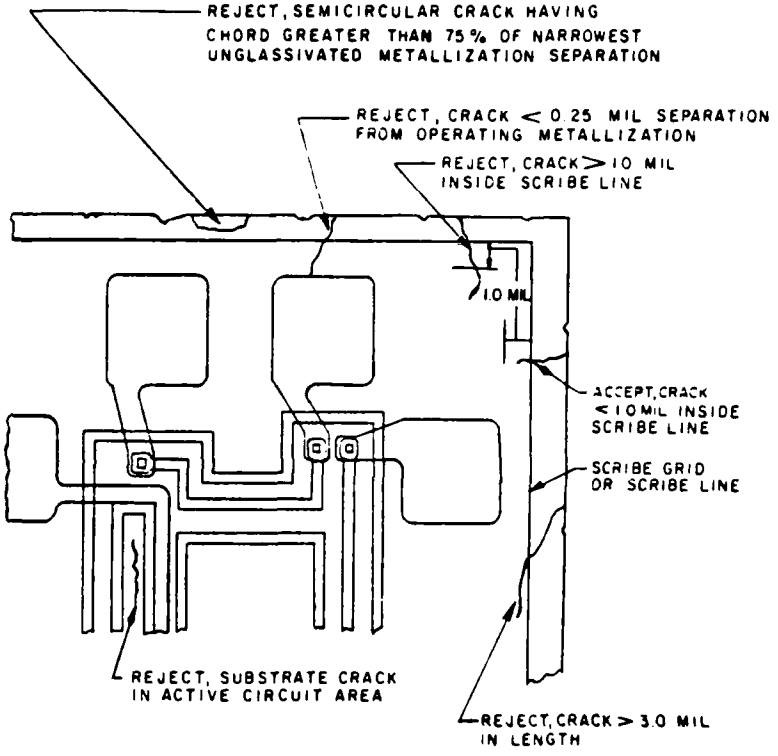


FIGURE 2010-8. Scribing and die defects.

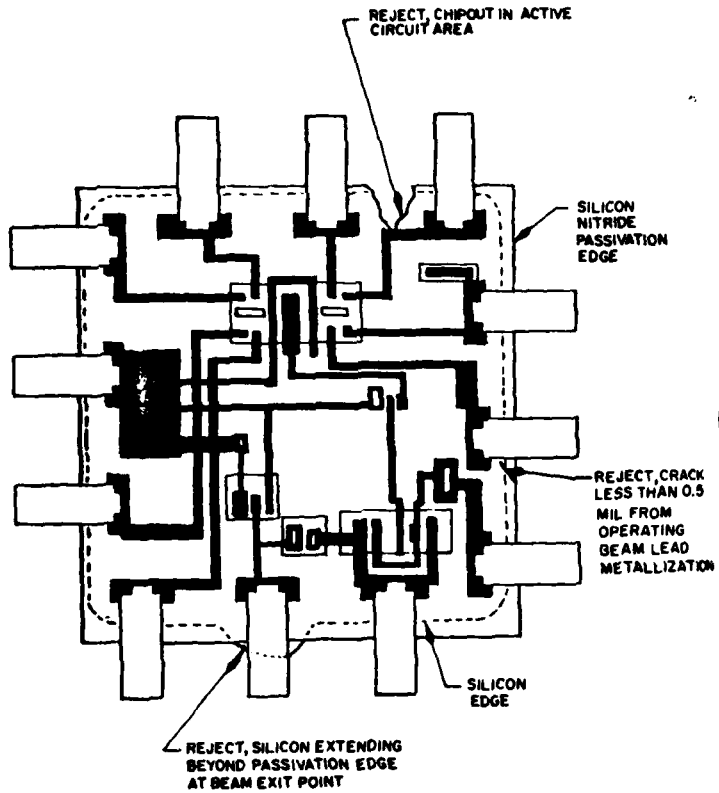


FIGURE 2010-9. Beam lead die faults.

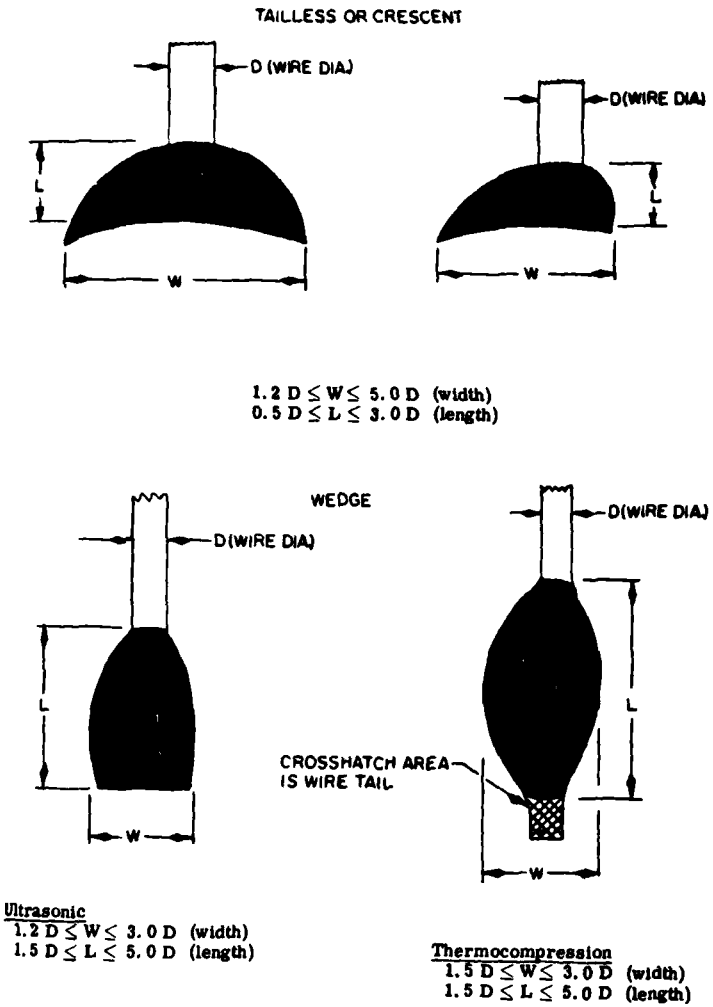
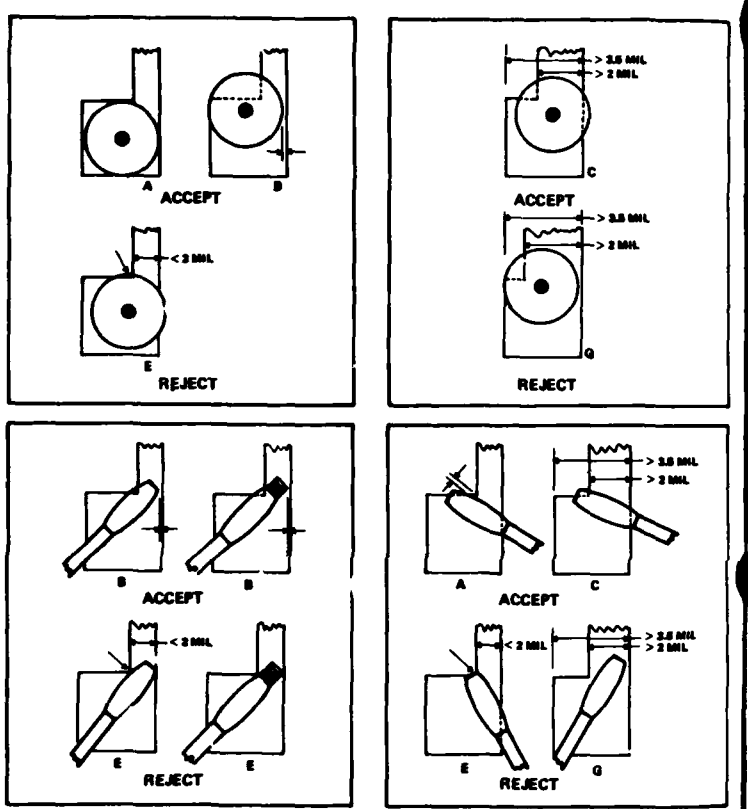


FIGURE 2010-10. Bond dimensions.



REASONS FOR ACCEPT OR REJECT DECISIONS:

A = ACCEPT, because ≥75% of the bond area is on the bonding pad, and there is no bond at the point where metal exits from the bonding pad.

B = ACCEPT, because ≥75% of the bond area is on the bonding pad, and there is a visible line of undisturbed connecting metal between the bond periphery and at least one side of the entering metal.

C = ACCEPT, even though no visible line of connecting metal exists, since the entering metal width is >2 mils and the bonding pad dimension is >3.5 mils on the entering metal side, and ≥75% of the bond area is on the bonding pad.

E = REJECT, due to a bond at the point where metal exits from the bonding pad without a visible line of connecting metal, and the entering metal width is not >2 mils (bond tails are considered part of the bond for Condition A).

G = REJECT, due to a bond area <75% on the bonding pad, even though all other criteria are met.

FIGURE 2010-11. BONDS AT METALLIZATION EXIT.

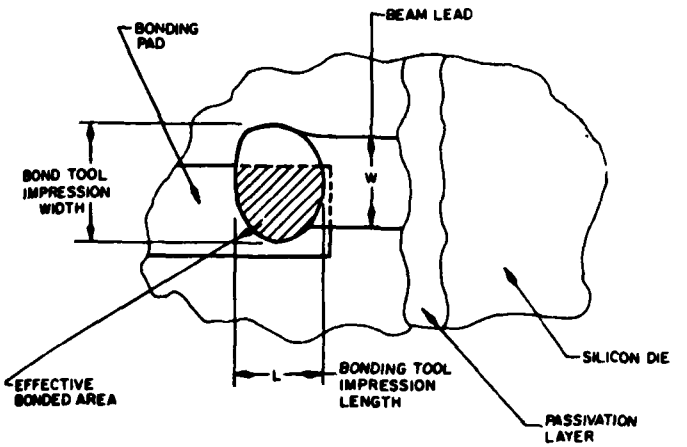


FIGURE 2010-12. Beam lead bond area.

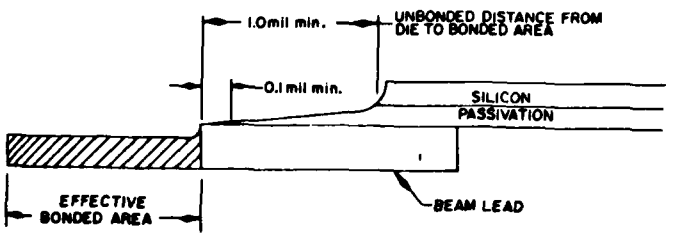


FIGURE 2010-13. Beam lead bond location.

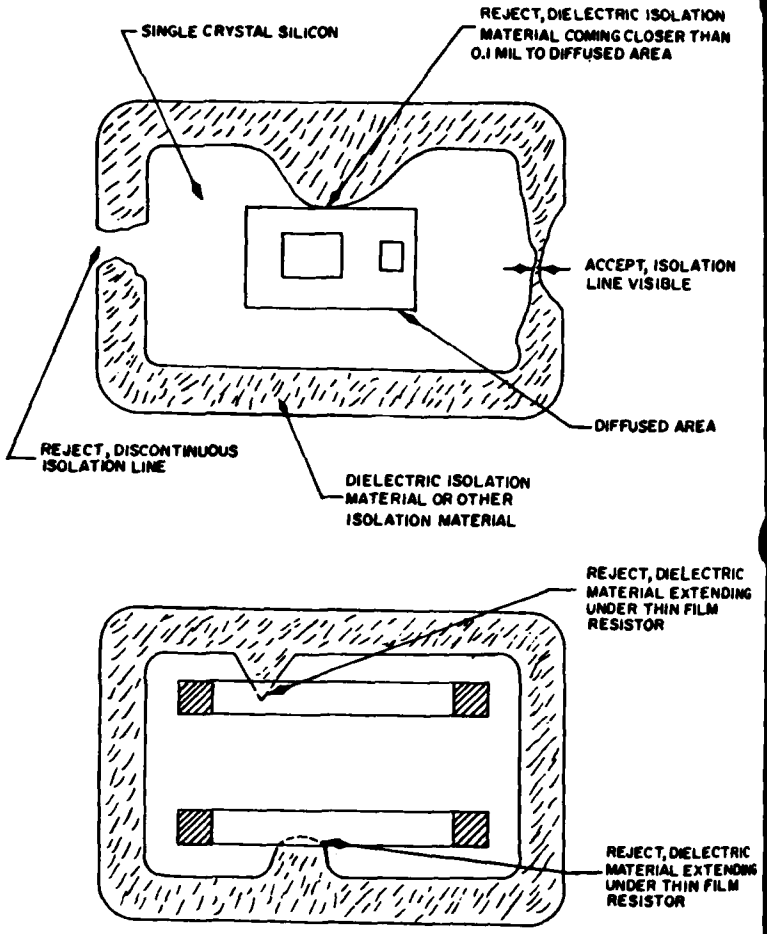


FIGURE 2010-14. Dielectric isolation defects.

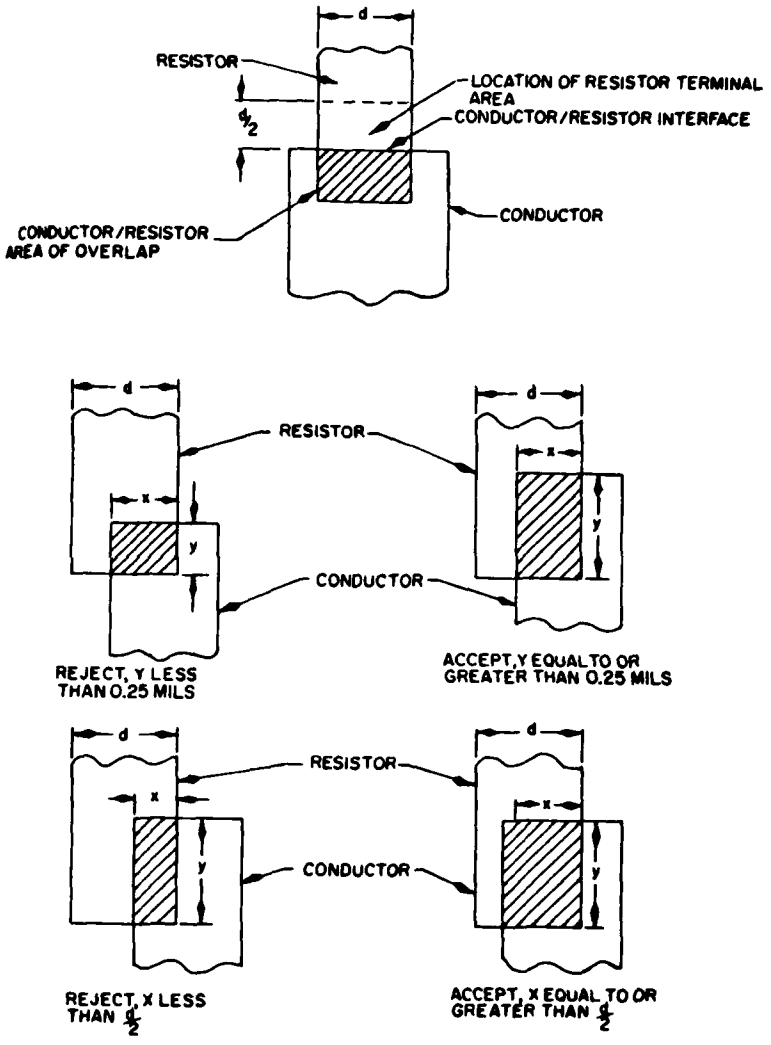


FIGURE 2010-15. Thin film resistor contact area.

3.2 Test condition B. Internal visual examination as required in 3.2.1 through 3.2.6 shall be conducted on each microcircuit and each integrated circuit chip. In addition, the applicable criteria in 3.2.7 through 3.2.9 shall be used for the appropriate microcircuits areas where glassivation, dielectric isolation or film resistors are used. The "high magnification" inspection shall be performed within the range of 75X to 150X and the "low magnification" within the range of 30X to 60X.

3.2.1 Metallization defects "high magnification." No device shall be acceptable that exhibits the following in the operating metallization.

3.2.1.1 Metallization scratches. A scratch is any tearing defect, including probe marks in the surface of the metallization:

a. Scratch in the metallization that exposes underlying passivation anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see figure 2010-16).
b. Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation on both sides. (For MOS devices, the path shall be the (L) dimension (see figure 2010-18).)
c. Scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 25 percent of the top-layer original metal width undisturbed (see figure 2010-16).

NOTE: Criteria of 3.2.1.1 a, b, and c can be excluded for peripheral power or ground metallization where parallel paths exist such that an open at the scratch would not cause an unintended isolation of the metallization path. When application of this exclusion causes or permits a device design to exceed the current density limitation imposed by the procurement document, this exclusion shall not apply. Current density shall be determined by design not visual inspection.

d. Scratch in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: Criteria of 3.2.1.1 a through d can be excluded for the last 25 percent of linear length of the contact cut and all metal beyond on the termination end(s) of the metallization runs. In these cases there shall be at least 50 percent of the contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-17).

e. Any scratch in the metallization, over the gate oxide bridge, that exposes underlying passivation and leaves less than 50 percent of the length or width of the metallization between source and drain diffusion undisturbed (see figure 2010-18) (applicable to MOS structures).
f. Scratch in the metallization that exposes the dielectric material of a thin film capacitor or crossover.

3.2.1.2 Metallization voids. A void is any defect in the metallization where underlying metal or passivation is visible and is not caused by a scratch.

a. Void(s) in the metallization that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-19).
NOTE: Criteria of 3.2.1.2 a can be excluded for peripheral power or ground metallization where parallel paths exist so that an open at the void(s) would not cause an unintended isolation of the metallization path. When application of this exclusion causes or permits a device design to exceed the current density limitation imposed by the procurement document, this exclusion shall not apply. Current density shall be determined by design, not visual inspection.

b. Void(s) in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: Criteria of 3.2.1.2 a and b can be excluded for the last 25 percent of linear length of the contact cut and all metal beyond on the termination end(s) of metallization runs. In these cases there shall be at least 50 percent of the contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-17).

c. Void(s) in the metallization over the gate oxide bridge that leaves less than 75 percent of the metallization length (L) between source and drain diffusions undisturbed (see figure 2010-18) (applicable to MOS structures).
d. Void(s) that leave less than 60 percent of the metallization area over the gate oxide bridge undisturbed (applicable to MOS structures).
e. Void(s) that leaves less than 75 percent of the metallization width coincident with the source or drain diffusion junction line, undisturbed (see figure 2010-18) (applicable to MOS structures).
f. Void(s) in the bonding pad area that leaves less than 75 percent of its original unglassivated metallization area undisturbed.
g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width (see figure 2010-20).
NOTE: if two or more stripes enter a bonding pad, each shall be considered separately.
h. Void(s) in the metallization of a thin film capacitor that reduces the metallization area by more than 25 percent.

3.2.1.3 Metallization corrosion. Any metallization corrosion.

3.2.1.4 Metallization adherence. Any metallization lifting, peeling, or blistering.

3.2.1.5 Metallization probing. Criteria contained in 3.2.1.1 shall apply as limitations on probing damage.

3.2.1.6 Metallization bridging. Any metallization bridging where the separation between any two metallization paths is reduced to less than 0.1 mil, unless by design.

3.2.1.7 Metallization alignment.

a. Contact window that has less than 50 percent of its area covered by metallization.
b. Contact window that has less than 40 percent of its perimeter covered by metallization.
NOTE: When, by design, metal is completely contained in a contact window, criteria 3.2.1.7 b perimeter coverage can be deleted.
c. A metallization path not intended to cover a contact window that is separated from the window by less than 0.1 mil.
d. Any exposure of the gate oxide bridge from source to drain diffusions (see figure 2010-21) (applicable to MOS structures).
e. Any exposure of the gate oxide bridge that leaves less than 75 percent of the metallization coincident with the source and drain diffusion junction line undisturbed (applicable to MOS structures).

f. Gate metallization not coincident with or extending over the diffused guard ring.
NOTE: Criteria 3.2.1.7 f applies to MOS structures containing a diffused guard ring. MOS devices that do not contain a diffused guard ring shall have gate metallization extending not less than 0.1 mil beyond the gate oxide bridge (see figures 2010-18 and 2010-21).

3.2.2 Diffusion and passivation layer(s) faults, "high magnification." No device shall be acceptable that exhibits the following:

a. A diffusion junction line that unintentionally crosses another diffusion junction line (see figure 2010-22).
b. Any isolation diffusion that is discontinuous except isolation walls around unused areas or bonding pads or any other diffused area with less than 25 percent of the original diffusion width remaining.
c. Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization (see figure 2010-23).
NOTE: Double or triple lines indicate that it can have sufficient depth to penetrate down to bare silicon; however, should the absence of glassivation in the defect area or the characteristics of the glassivation present allow verification of the presence or absence of passivation by color or color comparisons, respectively, then these techniques may be used.
d. An active junction not covered by passivation, unless by design.

3.2.3 Scribing and die defects, "high magnification." No device shall be acceptable that exhibits:

a. Less than 0.1 mil of passivation visible between operating metallization or bond periphery and edge of the die.
NOTE: Criteria of 3.2.3 a can be excluded for beam leads and peripheral metallization including bonding pads where the metallization is at the same potential as the die.
b. A chipout in the active circuit area (see figures 2010-24 and 2010-25).
NOTE: Criteria 3.2.3 b can be excluded for peripheral metallization that is at the same potential as the die. In these cases there shall be at least 50 percent of the peripheral metallization width undisturbed at the chipout.
c. Any substrate or passivation crack in the active circuit area or a crack that exceeds 5.0 mils in length (see figure 2010-24).
d. Any crack that comes closer than 0.1 mil to any operating metallization or other active circuit area on the die (see figure 2010-24).
NOTE: Criteria of 3.2.3 d can be excluded for peripheral metallization that is the same potential as the die.
e. A crack, that exceeds 1.0 mil in length, inside the scribe grid or scribe line that points toward operating metallization or functional circuit elements (see figure 2010-24).
f. Exposed silicon extending beyond the passivation edge at the point of the beam lead exit from the die (see figure 2010-25) (applicable to beam lead structures).
g. A crack that comes closer than 0.5 mil to operating beam lead metallization (see figure 2010-25).

3.2.4 Bond inspection, "low magnification." This inspection and criteria shall be required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above.

NOTE: Wire tail is not considered part of the bond when determining physical bond dimensions.

3.2.4.1 Gold ball bonds. No device shall be acceptable that exhibits:

a. Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 6.0 times the wire diameter.
b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.
c. Gold ball bonds where the wire center exit is not within the boundaries of the bonding pad.
d. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.

3.2.4.2 Wedge bonds. No device shall be acceptable that exhibits:

a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length (see figure 2010-26).
b. Thermocompression wedge bonds on the die or package post that are less than 1.5 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length (see figure 2010-26).
c. Wedge bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see figures 2010-20) and 2010-27).
NOTES: 1. Criteria 3.2.4.2 c can be excluded when the entering metallization strip is greater than 2.0 mils in width and the bond pad dimension on the entering metal stripe side is greater than 3.5 mils.
2. The requirements of 3.2.4.2 c for a visual line of metal can be satisfied when an acceptable wire tail obscures the area of concern, providing the following condition exists: Bond is located more than 0.1 mil from the intersecting line of the entering metallization stripe and the bonding pad, and there is no visual evidence of disturbed pad metallization at the bond and wire tail interface.

3.2.4.3 Tailless bonds (crescent). No device shall be acceptable that exhibits:

a. Tailless bonds on the die or package post that are less than 1.2 times greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length (see figure 2010-26).
b. Tailless bonds where the bond impression does not cover entire width of the wire.
c. Tailless bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see figure 2010-27).

3.2.4.4 General (gold ball, wedge and tailless). No device shall be acceptable that exhibits:

a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.
b. Bonds on the package post that are not completely within the boundaries of the package post.

c. Bonds placed so that the wire exiting from the bond crosses over another bond.
d. Bonds placed so that the separation between bonds or the bond and operating metallization not connected to it is less than 0.1 mil.
e. Wire bond tails that extend over or make contact with any metallization not covered by glassivation and not connected to the wire.
f. Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.
g. Bonds where less than 50 percent of the bond is located within an area that is free of die preform mounting material.
h. A bond on top of another bond.
i. Any evidence of repair of conductors by bridging with or addition of bonding wire or ribbon.
j. Any rebonding which violates the applicable rework limitations of MIL-M-38510.

3.2.4.5 Beam lead. This inspection and criteria shall apply to the completed bond area made using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:

a. Bonds where the tool impression does not completely cross the entire beam width.
b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15 percent (10 percent for compliant bonds) or greater than 75 percent of the undeformed beam width.
c. Bonds where the tool impression length is less than 1.0 mil (see figure 2010-28).
d. A bonding tool impression less than 1.0 mil from the die edge (see figure 2010-29).
e. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see figure 2010-28).
f. Cracks or tears in the effective bonded area of the beam greater than 50 percent of the original beam width.
g. Bonds placed so that the separation between bonds or between bonds and operating metallization not connected to them is less than 0.1 mil.
h. Bonds lifting or peeling.

3.2.5 Internal leads, "low magnification." This inspection and criteria shall be required inspection for the lead type(s) and location(s) to which they are applicable.

3.2.5.1 Wires. No device shall be acceptable that exhibits:

a. Any wire that touches another wire (excluding common wires), package post, unglassivated operating metallization, die, or any portion of the package.
b. Excessive loop or sag in any wire so that it comes closer than two wire diameters to another wire, package post, unglassivated operating metallization or die, or portion of the package after a spherical radial distance from the bond perimeter on the die surface of 5.0 mils for ball bonds, or 10 mils for ultrasonic and thermocompression bonds.
c. Nicks, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.
d. Attached extra wire greater than two wire diameters in length at the bonding pad or four wire diameters in length at the package post.
e. Tearing at the junction of the wire and bond.
f. Any wire making a straight line run from die bonding pad to package post that has no arc.
g. Wire(s) crossing wire(s) (except common conductors).
h. Wire(s) not in accordance with bonding diagram.

3.2.5.2 Beams. No device shall be acceptable that exhibits the following between the edge of the die and the bond area:

a. Voids, nicks, depressions, or scratches that leave less than 50 percent of the beam width undisturbed.
b. Beam separation from the die.
c. Missing or partially fabricated beam leads, unless by design.
d. Beam leads that are not bonded.
e. Bonded area closer than 0.1 mil to the edge of the passivation layer.
f. Lack of evidence of a passivation layer between the die and each beam (see figures 2010-25 and 2010-28).

3.2.6 Package conditions, "low magnification." No device shall be acceptable that exhibits:

3.2.6.1 Foreign material: All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psig). The device shall then be inspected and be rejected when it exhibits the following:

a. Unattached foreign material on the surface of the die or within the package.
b. Unattached foreign material on the surface of the lid or cap.
NOTE: Criteria of 3.2.6.1 b can be satisfied by a nominal gas blow (approximately 20 psig) or a suitable cleaning process providing that the lids or caps are subsequently held in a controlled environment until capping.
c. Attached conductive foreign material that bridges metallization paths, package leads, lead to package metallization, functional circuit elements or junctions, or any combination thereof.
NOTE: Glassivated areas of the die can be excluded from the criteria of 3.2.6.1 c when the particle or material is attached only at the top surface of the glassivation.
d. Ink on the surface of the die that covers more than 25 percent of a bonding pad area or that bridges any combination of unglassivated metallization or bare silicon areas.

3.2.6.2 Die mounting:

a. Die mounting material buildup that extends onto the top surface of the die.
b. Die to header mounting material not visible around at least 50 percent of the die perimeter or continuous on two full sides of the die, whichever is less, except for transparent die.
c. Transparent die with less than 50 percent of the area bonded.
d. Flaking of the die mounting material.
e. Balling of the die mounting material that does not exhibit a fillet, when viewed from above (see figure 2010-30).

3.2.6.3 Die assembly. Die not located and oriented in accordance with the applicable assembly drawing of the device.

3.2.7 Glassivation defects, "high magnification." No device shall be acceptable that exhibits:

a. Crazing that prohibits the detection of visual criteria contained herein.
b. Any lifting or peeling of the glassivation.
NOTE: Lifting or peeling of the glassivation may be excluded from the criteria above, when it does not extend more than 0.001 inch distance from the designed periphery of the glassivation, provided that the only exposure of metal is of adjacent bond pads or of metallization leading from those pads.

c. Two or more adjacent active metallization paths not covered by glassivation, excluding bonding pad cutouts.
d. Unglassivated areas greater than 5.0 mils in any dimension, unless by design.
e. Unglassivated areas at the edge of bonding pad exposing silicon.
f. Glassivation covering more than 50 percent of the bonding pad area.
g. Crazing over a film resistor.

3.2.8 Dielectric isolation, "high magnification." No device shall be acceptable that exhibits:

a. A discontinuous isolation line (typically a black line) around each diffusion tub containing functional circuit elements (see figure 2010-31).
b. Absence of a continuous isolation line between any adjacent tubs containing functional circuit elements.
c. A diffused area which overlaps dielectric isolation material and comes closer than 0.1 mil to an adjacent diffusion tub; or an overlap of more than one diffusion area into the dielectric isolation material (see figure 2010-31).
d. A contact window that touches or overlaps dielectric isolation material.
e. Metallization scratch and void defects over a dielectric isolation step shall be in accordance with criteria in 3.2.1.1 b and 3.2.1.2 b.

3.2.9 Film resistor, "high magnification." Rejection shall be based on defects found within the actively used portions of the film resistor. Metallization defect criteria of 3.2.1 shall apply. No device shall be acceptable that exhibits the following:

a. Any misalignment between the conductor/resistor in which the actual width X of the overlap is less than 50 percent of the original resistor width (see figure 2010-32).
b. Contact overlap between the metallization and film resistor in which the length dimension Y is less than 0.25 mil (see figure 2010-32).
c. Separation between any two resistors or a resistor and a metallization path that is less than 0.1 mil, unless by design.
d. Void or necking down that leaves less than 75 percent of the film resistor width undisturbed at a terminal.
e. Any sharp change in the color of resistor material, within 0.1 mil of the resistor/conductor termination.
f. Inactive resistor inadvertently connected to two separate points of an active circuit.
g. Any thin film resistor that crosses a substrate irregularity (e.g., dielectric isolation line, oxide/diffusion step, etc.,) (see figure 2010-31).

4. SUMMARY. The following details shall be specified in the applicable procurement document:

a. Test condition (see 3).
b. Where applicable, any conflicts with approved circuit design topology or construction.
c. Where applicable, gages, drawings, and photographs that are to be used as standards for operator comparison (see 2).
d. Where applicable, specific magnification (see 3).

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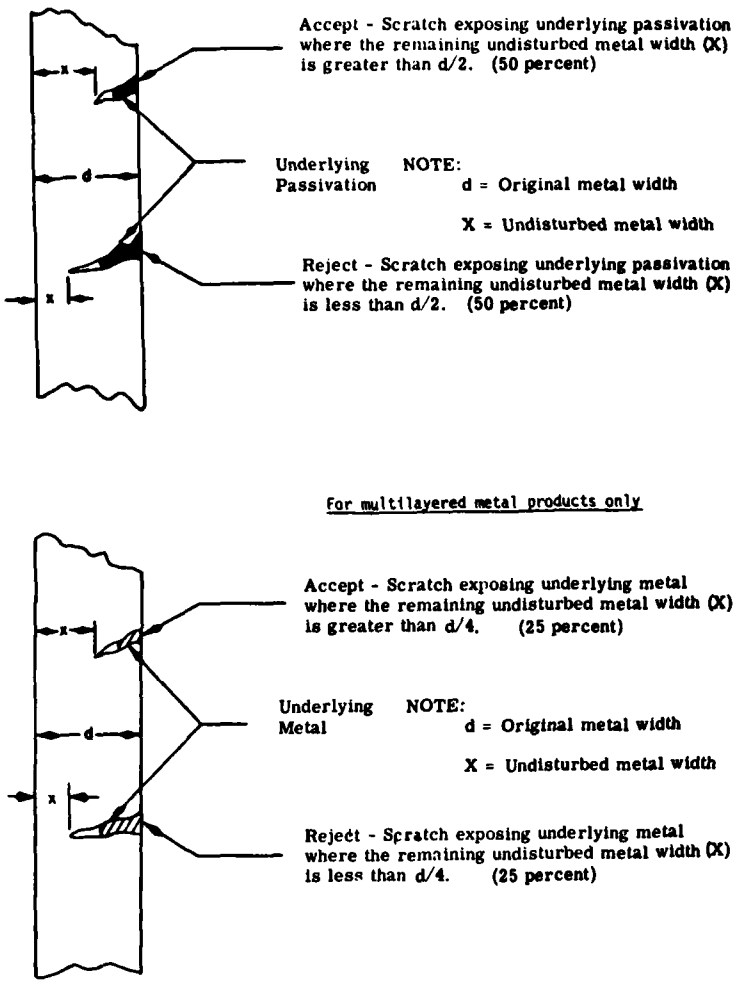

FIGURE 2010-16. Scratch criteria.

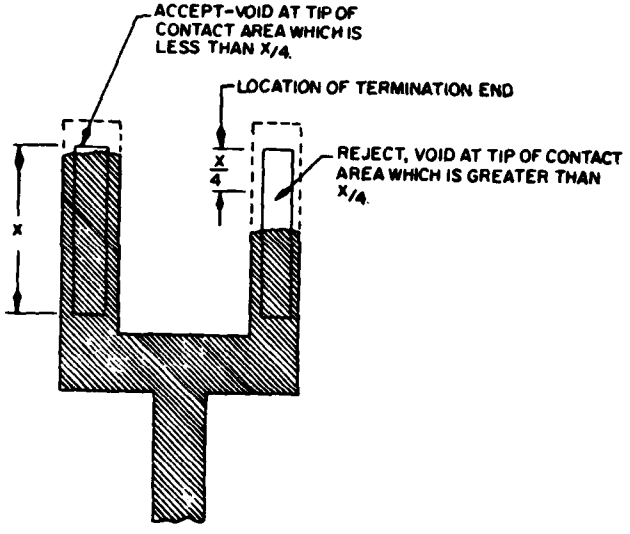

FIGURE 2010-17. Termination ends.

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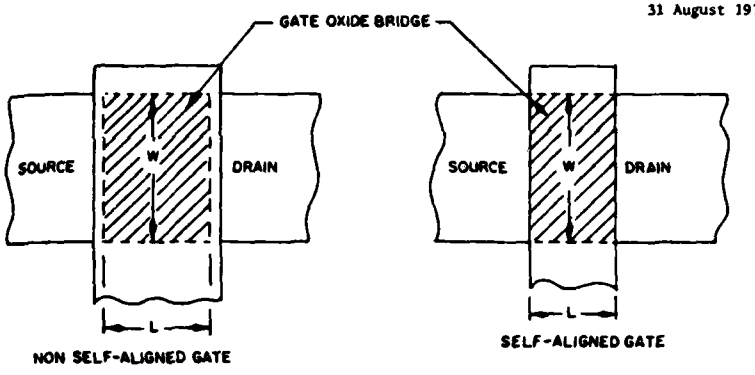

NOTE: When standard metallization scratch and void criterion is applied to the gate area the dimension (W) and (L) shall be considered as the original channel width and length respectively.

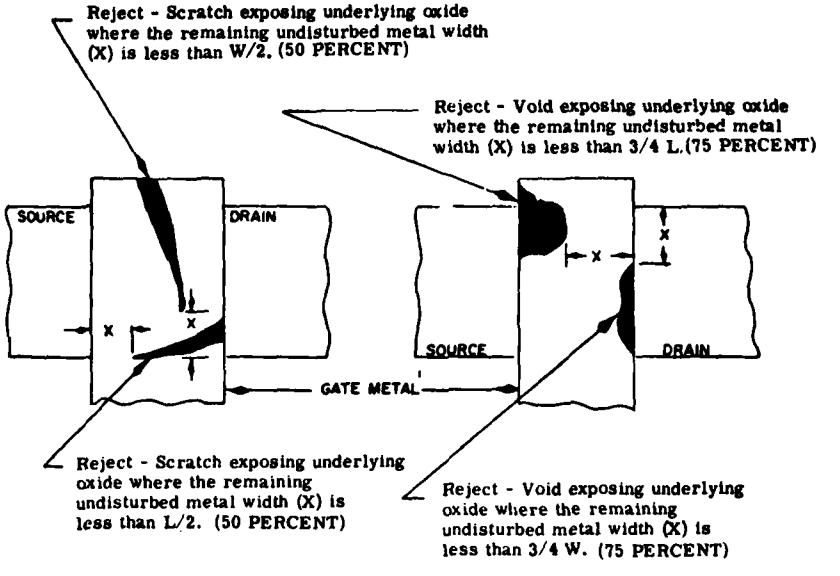

FIGURE 2010-18. MOS scratch and void criteria.

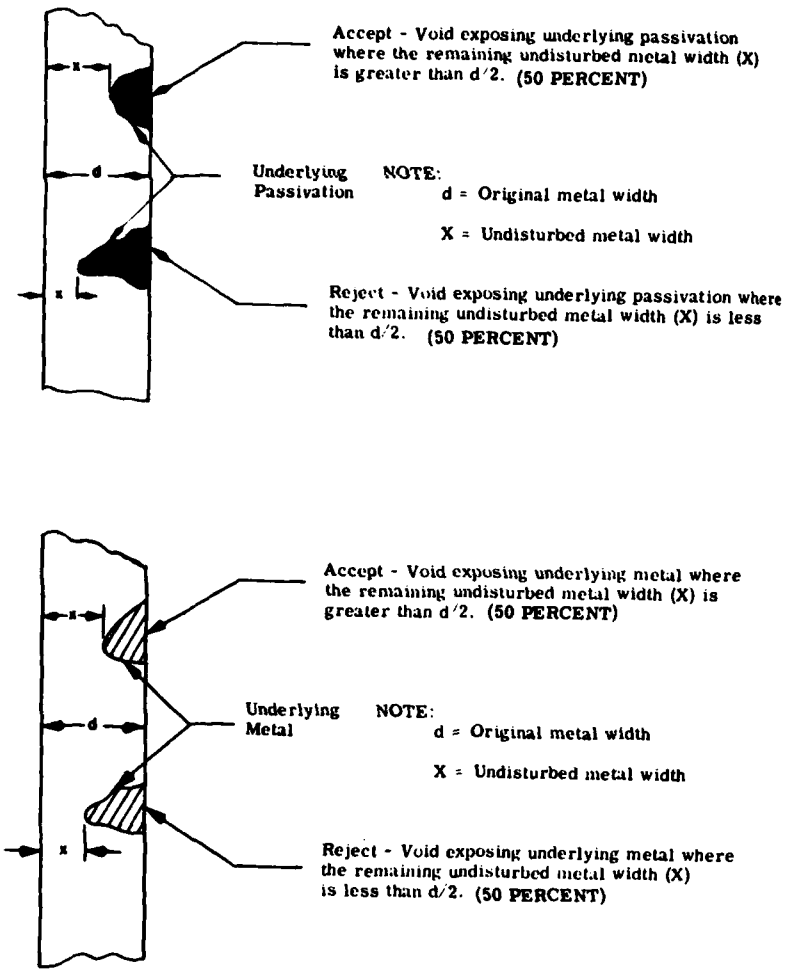

FIGURE 2010-19. Void criteria.

III-1-94

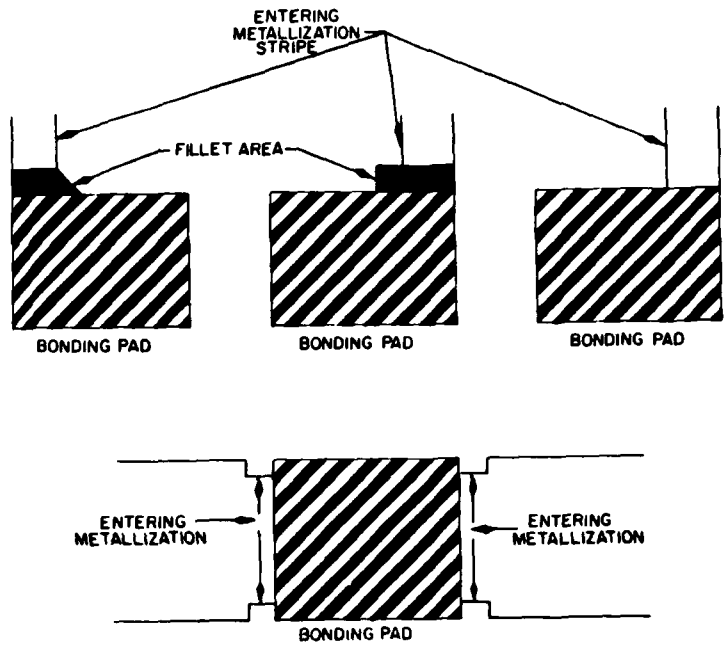

FIGURE 2010-20. Bonding pad areas.

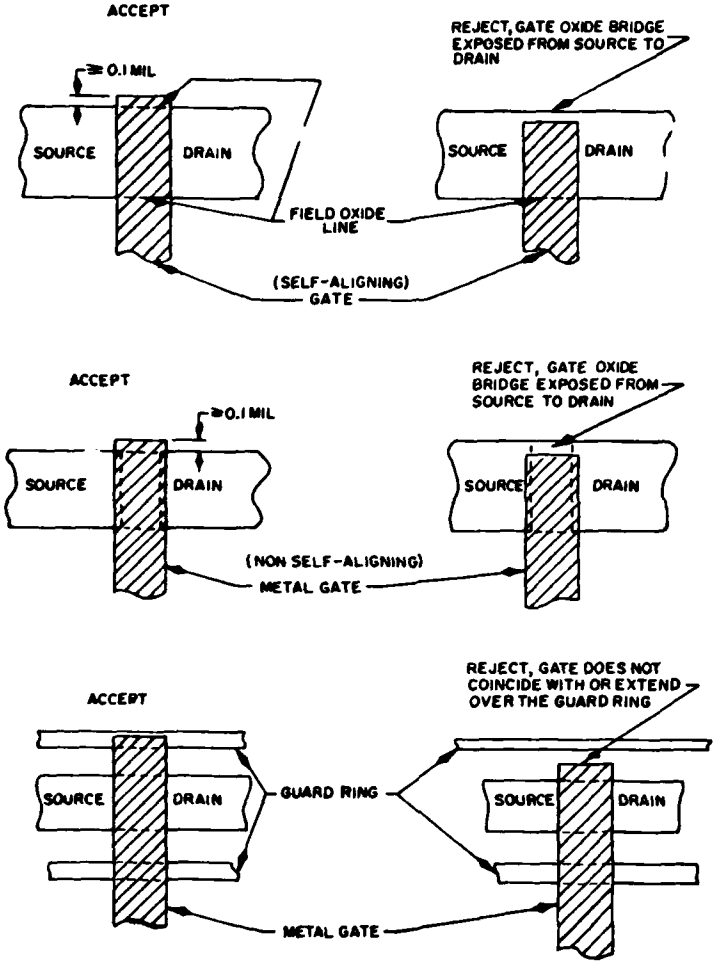

FIGURE 2010-21. MOS gate alignment.

III-1-95

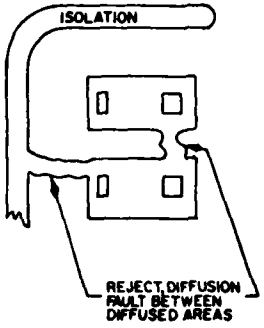

FIGURE 2010-22. Diffusion fault.

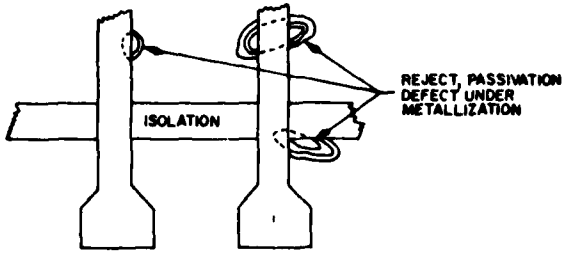

FIGURE 2010-23. Passivation fault.

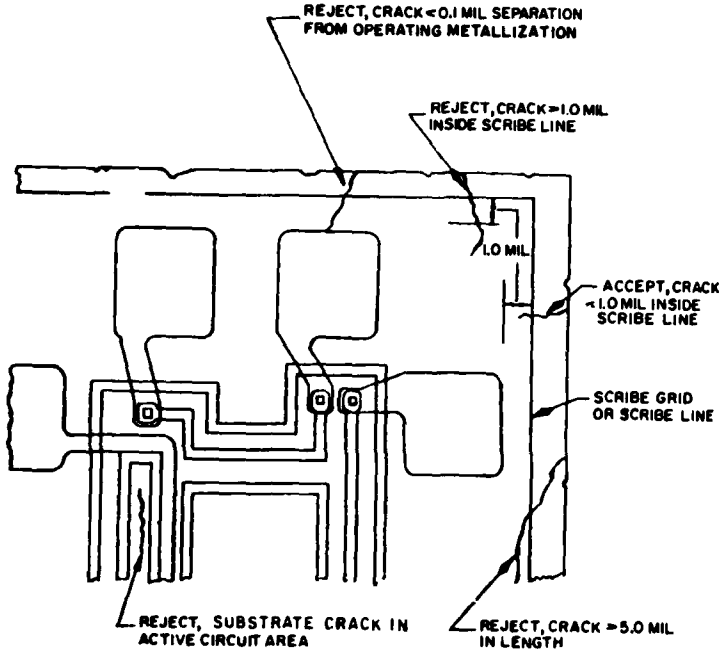

FIGURE 2010-24. Scribing and die defects.

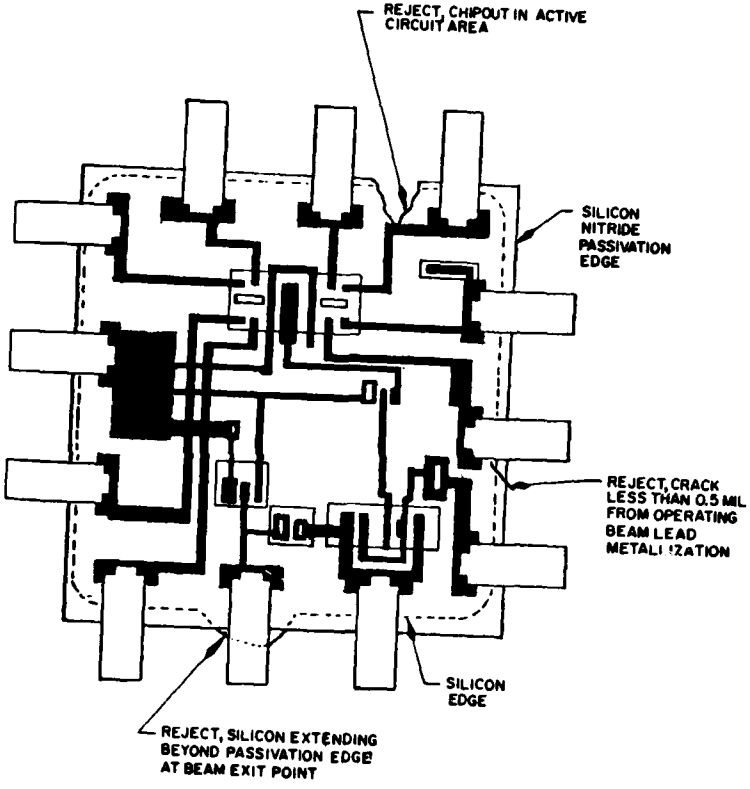

FIGURE 2010-25. Beam lead die faults.

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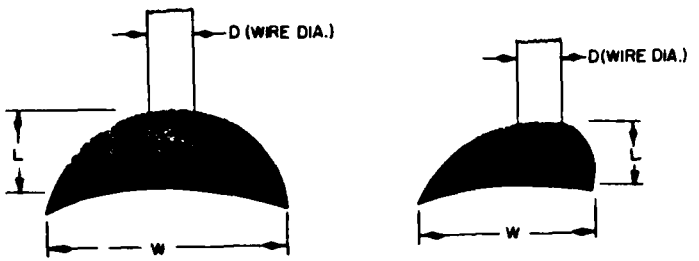
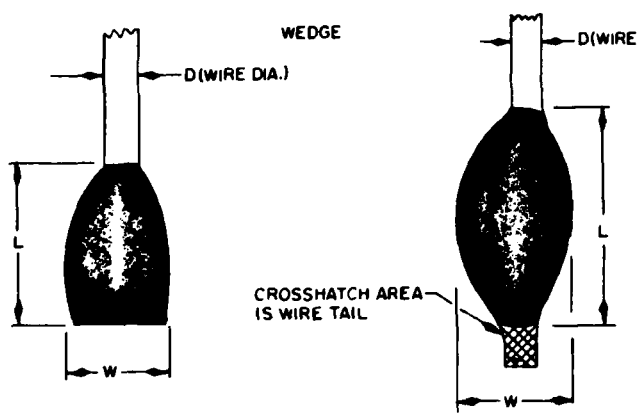
TAILLESS OR CRESCENT



$1.2\ D \leq W \leq 5.0\ D$ (width)
$0.5\ D \leq L \leq 3.0\ D$ (length)

WEDGE



Ultrasonic	Thermocompression
$1.2\ D \leq W \leq 3.0\ D$ (width)	$1.5\ D \leq W \leq 3.0\ D$ (width)
$1.5\ D \leq L \leq 5.0\ D$ (length)	$1.5\ D \leq L \leq 5.0\ D$ (length)

FIGURE 2010-26. Bond dimensions.

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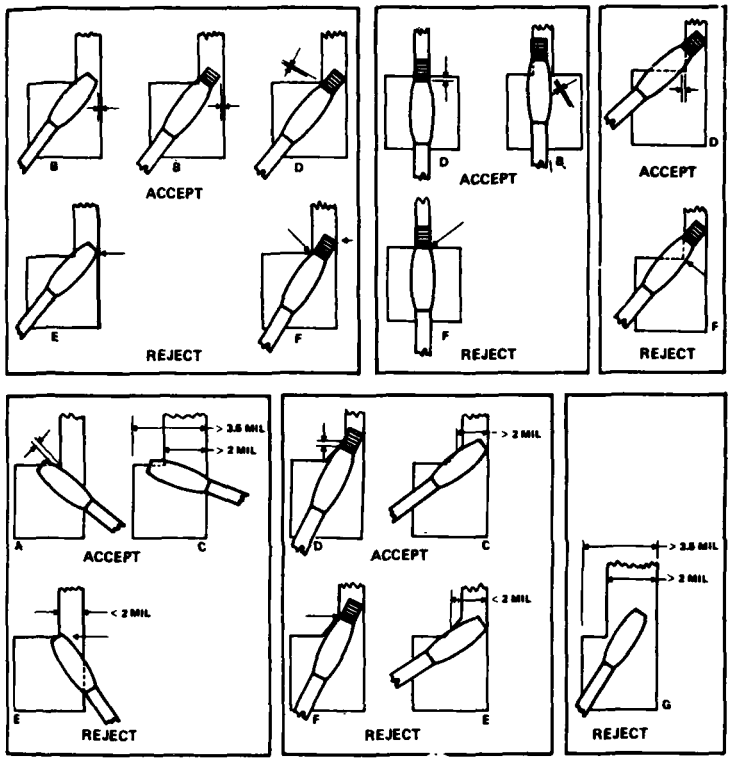

REASONS FOR ACCEPT OR REJECT DECISIONS:

A = ACCEPT, Because ≥50% of the bond area is on the bonding pad, and there is no bond at the point where metal exits from the bonding pad.

B = ACCEPT, Because ≥50% of the bond area is on the bonding pad, and there is a visible line of undisturbed connecting metal (≥0.1 mil) between the bond periphery and at least one side of the entering metal.

C = ACCEPT, even though no visible line of connecting metal exists, since the entering metal width is >2 mils and the bonding pad dimension is >3.5 mils on the entering metal side, and ≥50% of the bond area is on the bonding pad.

D = ACCEPT, even though the bond wire tail prevents the connecting line of metal from being visible, because, (1) the bond periphery excluding the tail, is located ≥0.1 mil from the intersection of the entering metal stripe and the bonding pad, and (2) there is no visual evidence of disturbed pad metal at the bond and wire tail interface, and (3) ≥50% of the bond area is on the bonding pad.

E = REJECT, due to a bond at the point where metal exits from the bonding pad without a visible line of connecting metal, and the entering metal width is not >2 mils.

F = REJECT, due to the bond periphery (omitting the bond wire tail) being within 0.1 mils of the intersection of the entering metal and the bonding pad, and the bond wire tail obscures the possible connecting line of metal.

G = REJECT, due to a bond area <50% on the bonding pad, even though all other criteria are met.

FIGURE 2010-27. BONDS AT METALLIZATION EXIT.

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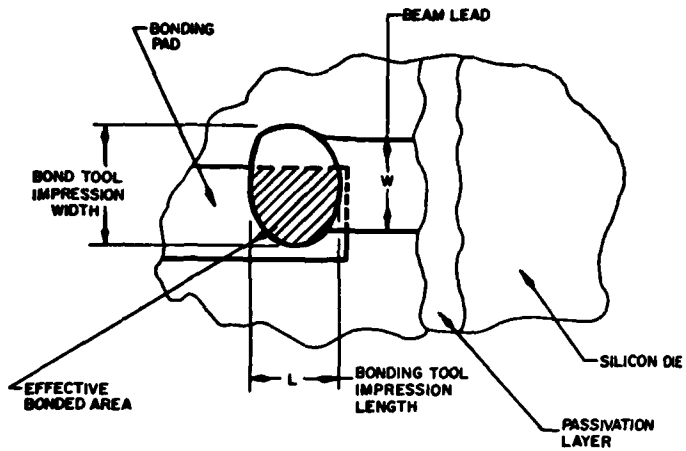

FIGURE 2010-28. Beam lead bond area.

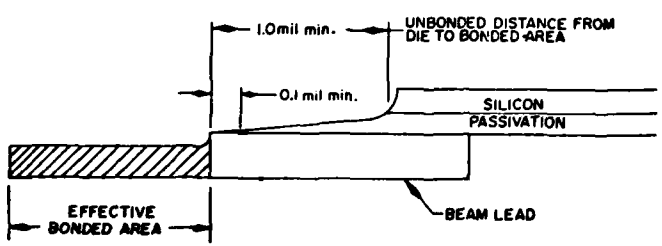

FIGURE 2010-29. Beam lead bond location.

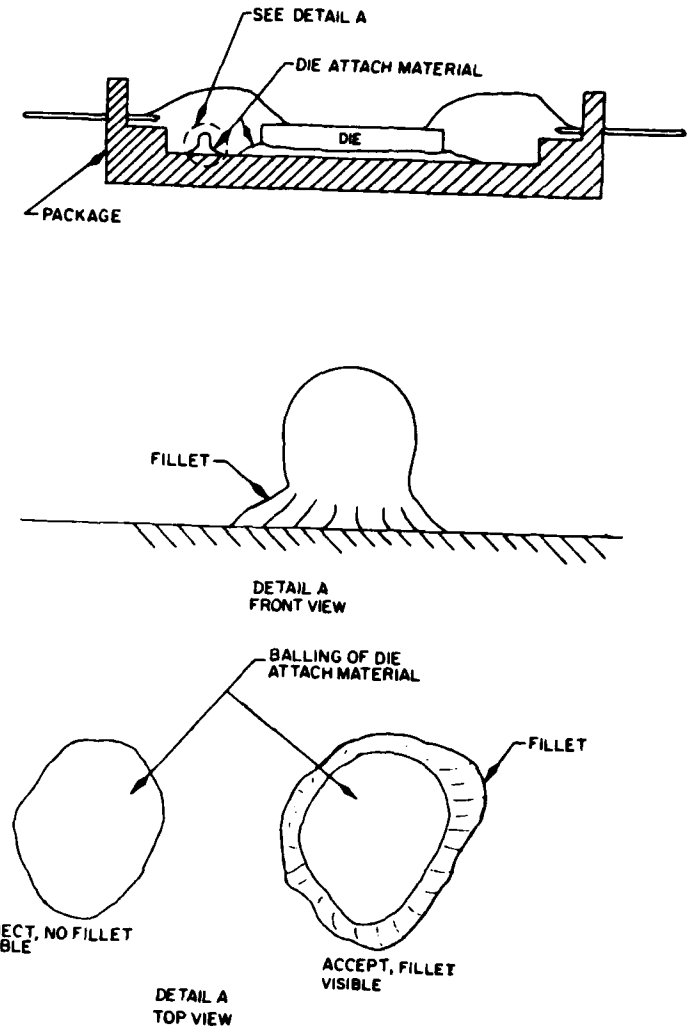

FIGURE 2010-30. Balling of die attach material.

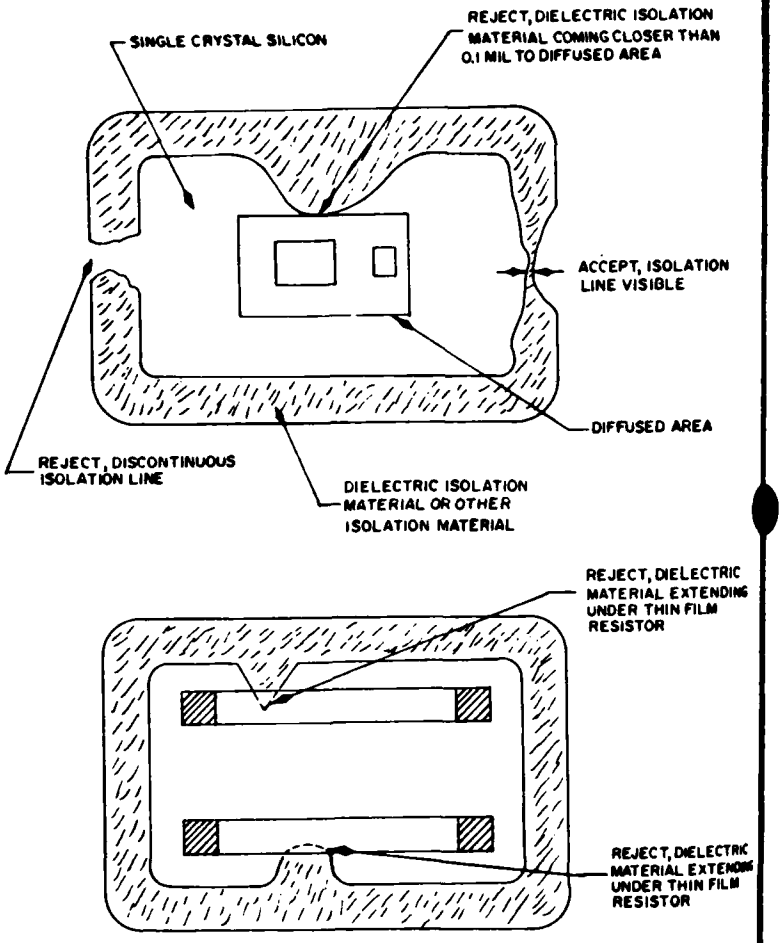

FIGURE 2010-31 Dielectric isolation defects.

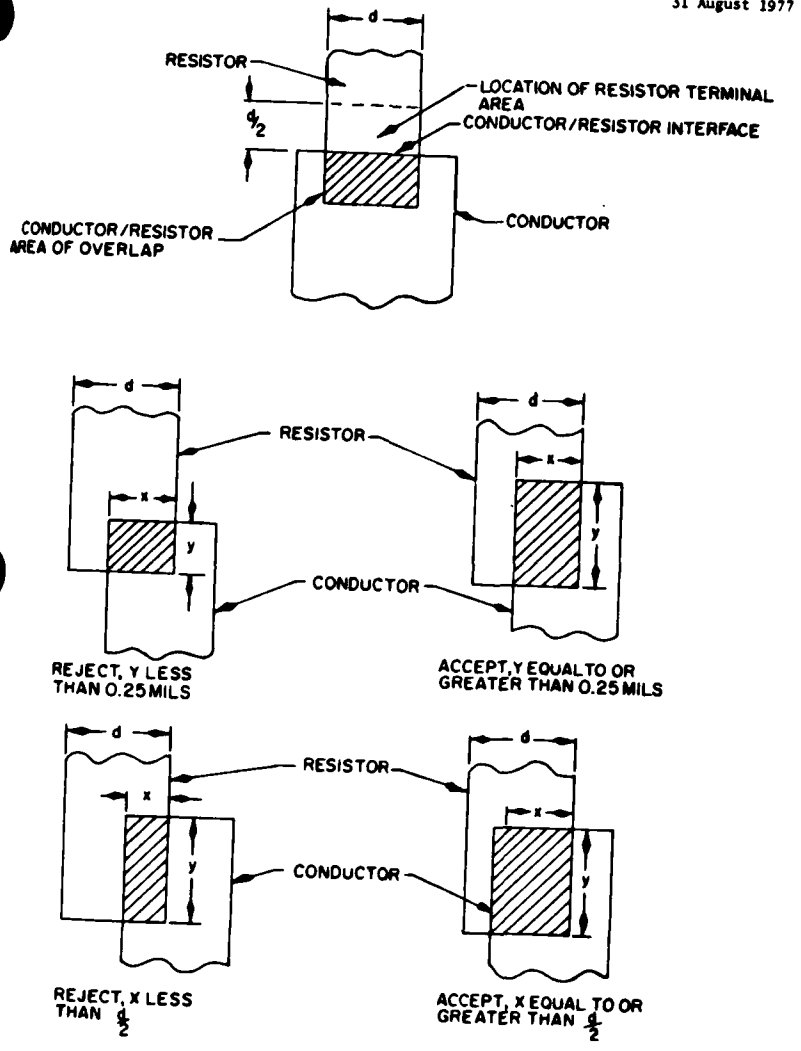

FIGURE 2010-32. Thin film resistor contact area.

METHOD 2017.1

INTERNAL VISUAL (HYBRID)

1. PURPOSE. The purpose of this test is to check the internal materials, construction, and workmanship of hybrid and multichip microcircuits that use a thin or thick film interconnection pattern on a supporting substrate for compliance with the requirements of the applicable procurement document. The following types of hybrid and multichip microcircuits may be inspected:

a. Passive thin and thick film networks.
b. Active thin and thick film circuits.
c. Multiple, including combinations, stacking or other interconnections of 1.a and 1.b.

This test will normally be used prior to capping or encapsulation on a 100-percent inspection basis to detect and eliminate devices with internal defects that could lead to device failure in normal application. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices. This test condition provides a rigorous and detailed procedure for internal visual inspection intended for hybrid microcircuits.

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (gages, drawings, photographs, etc.,) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

3. PROCEDURE.

a. General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable procurement document and the criteria of the specified test condition. Discrete active devices shall be examined in accordance with 3.1.1. For nonJAN devices, if a specified visual inspection is in conflict with circuit design topology or construction, that particular inspection criterion shall be designated; "excepted by design" in the design documentation and shall be specifically approved by the procuring activity. For JAN devices, there shall be no waivers. The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Resistor trimming may not cause or allow a device design to exceed maximum allowable current density requirement limitations imposed by the procurement document. Unused components or unused deposited elements need meet only the mechanical integrity criteria of this method as specified in 3.1.3.2.5, Metallization adherence, 3.1.4.1 a, b, d, e, f, and g, Solder or alloy component mounting and 3.1.4.2 a, b, c, e, and g, Organic polymer (epoxy) component mounting. Method 2012, Radiography, may be used to perform the inspection of 3.1.5.1 a except the reject criteria shall be less than 50 percent substrate attach area.

b. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Where obscuring mounting techniques, i.e., beam lead devices, stacked substrates are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to attaching the die or substrate. The inspection criteria of 3.1.1 may be performed at the option of the manufacturer, prior to die or chip attachment.

c. Inspection control. In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections (see 3.b), to insure that defects created during subsequent handling will be detected and rejected at final preseal inspection. During the time interval between internal visual inspection and preparation for sealing, devices shall be stored in a controlled environment. Devices examined to 3.1 criteria shall be inspected and prepared for sealing in a class 100,000 environment, as defined in Federal Standard 209, except that the maximum allowable relative humidity shall not exceed 65 percent. Devices shall be in covered containers when transferred from one controlled environment to another.

d. Magnification. "High magnification" inspection shall be performed perpendicular to the substrate surface with the device under illumination normal to the substrate surface. Other angles at which the inspection can be performed and at which the device can be illuminated may be used at the option of the manufacturer, if the visual presentation is the same as used in the originally specified conditions. "Low magnification" inspection shall be performed with either a monocular, binocular, or stereo microscope and the inspection performed within an angle of 30 degrees from the perpendicular to the substrate surface with the device under suitable illumination.

e. Reinspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the procurement document. Where sampling is used rather than 100 percent reinspection, 6.4 of MIL-M-38510 shall apply.

f. Exclusions. Where conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.

g. Definitions.

1. Active circuit area includes all areas of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.
2. Controlled environment shall be in accordance with the requirements of Federal Standard 209, class 100 environment for air cleanliness and humidity, except that the maximum allowable relative humidity shall not exceed 50 percent. The use of an inert gas environment such as nitrogen, shall satisfy the requirement for a controlled environment.
3. Foreign material is defined as any material that is foreign to the microcircuit or any non-foreign material that is displaced from its original or intended position within the microcircuit package and shall be considered attached when it cannot be removed by a nominal gas blow (approximately 20 psig). Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles shall be considered embedded in the glassivation when there is evidence of color fringing around the periphery of the particle.
4. Glassivation is the top layer(s) of transparent insulating material that covers the active chip area including metallization except bonding pads and beam leads. Crazing is the presence of minute cracks in the glassivation.
5. Insulating layer area is a dielectric layer used to isolate multilevel conductive and resistive material or to protect top level conductive and resistive material.
6. Multilayered metallization (conductors) is two or more layers of metal or any other material used for interconnections that are not isolated from each other by a grown or deposited insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.

7. Multilevel metallization (conductors) is two or more layers of metal or any other material used for interconnections that are isolated from each other by a grown or deposited insulating material.
8. Operating metallization (conductors) is all metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads and identification markings.
9. Organic polymer (epoxy) vapor residue is the material that is emitted from the polymer that forms on an available surface.
10. Original design separation is the separation dimension or distance that is intended by design.
11. Original width is the width dimension or distance that is intended by design (i.e. original metal width, original diffusion width, original beam width, etc.).
12. Passivation is the silicon oxide, nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of metal.
13. String is a filamentary run-out or whisker of organic polymer material.
14. Thick film is that conductive/resistive/dielectric system that is a film having greater than 50,000 angstroms thickness.
15. Thin film is that conductive/resistive/dielectric system that is a film equal to or less than 50,000 angstroms thickness.
16. Unused component or unused deposited element is one not connected to a circuit or connected to a circuit path at one and only one point. A connection may be made by design or by visual anomaly.
17. Substrate is the supporting structural material into and/or upon which the passivation, metallization, and circuit elements are placed.

h. Interpretations. References herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used to confirm that a reject condition does not exist, they shall be approved by the procuring activity.

3.1 Examination. Internal visual examination as required in 3.1.1 through 3.1.8.1 shall be conducted on each hybrid microcircuit. The magnifications required for each inspection shall be those identified in the particular test method used, i.e., 2010, 2017, and 2072.

3.1.1 Microcircuit and semiconductor die or chips. All microcircuit and semiconductor devices shall be examined in accordance with method 2010, 3.1.1 Metallization defects, 3.1.2 Diffusion and passivation layer(s) faults, 3.1.3 Scribing and die defects, 3.1.6.1 Foreign material and 3.1.7 Glassivation defects for class S hybrid microcircuits, 3.2.1 Metallization defects, 3.2.2 Diffusion and passivation layer(s) faults, and 3.2.3 Scribing and die defects, 3.2.6.1 Foreign material and 3.2.7 Glassivation defects for classes B and C hybrid microcircuits.

NOTE: The visual inspection requirements of method 2072 of MIL-STD-750 may be substituted for method 2010 of MIL-STD-883 for semiconductor devices as indicated below:

Visual inspection	MIL-STD-750 method 2072	MIL-STD-883 method 2010
Die metallization defects	3.1.1	3.1.1 or 3.2.1
Diffusion and passivation layer(s) faults	3.1.2	3.1.2 or 3.2.2
Scribing and die defects	3.1.3	3.1.3 or 3.2.3

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3.1.2 Passive chip components (capacitors, resistors, R-C elements, inductors, and transformers) "magnification 10 to 60X." No device shall be acceptable that exhibits the following:

a. Peeling or lifting of metallized terminals.
b. Bridging between metallized terminals that leaves less then 1.0 mil separation.
c. Nonconformance to outline drawing.
d. Lifting, blistering, or peeling of insulation.
e. Resistors, capacitors, and R-C elements fabricated using semiconductor technologies shall be inspected in accordance with MIL-STD-883, method 2010 or MIL-STD-750, method 2072 (see 3.1.1).

3.1.2.1 Thick film chip components. Conformance to the requirements of 3.1.3.

3.1.2.2 Ceramic chip capacitors. No device shall be acceptable that exhibits the following:

a. Crack or void in the body that exposes metal plates (see figure 2017-1A).
b. Crack that is more than 50 percent on a side and extends around a corner (see figure 2017-1B).
c. Evidence of separation (delamination) of capacitor plates (cracks along the plane of the plates) (see figure 2017-1C).

3.1.3 Substrate defects - "magnification 10 to 60X." No device shall be acceptable that appears to exhibit the following:

3.1.3.1 Basic substrate:

a. Less than 3.0 mils separation between any attached component and the edge of the substrate.
b. Holes through the substrate, except through lead holes, used or unused component mounting holes, or alignment holes.
c. Crack that exceeds 5.0 mils in length and points toward an operating portion of the circuit.
d. Chip out that reduces any active (metallized) circuit area to less than 50 percent of the original design width.
e. Crack that comes closer than 1.0 mil to an operating portion of the circuit.
f. Substrate having attached portions of another substrate that exceeds the substrate dimensions allowed by the assembly drawing.
g. Substrate having a section broken out around any substrate mounting hole greater than 25 percent of the mounting hole circumference when designed for substrate to post attachment.
h. Substrate that does not have 50 percent of the original design separation between operating metallization and the edge of the substrate.
NOTE: Substrates designed for wraparound conductors need not meet this criterion.
i. Any crack that does not originate at an edge.

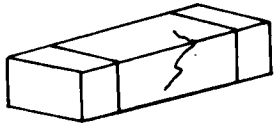
3.1.3.2 Metallization. No device shall be acceptable that exhibits the following in the operating metallization.

3.1.3.2.1 Metallization scratches. A scratch is any tearing defect, including probe marks, in the surface of the metallization:

a. Scratch in the metallization that exposes the substrate or underlying dielectric anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see figure 2017-2).
b. Scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 0.3 mil of the original top layer metal width undisturbed (see figure 2017-2).
c. Scratch in the metallization that exposes the dielectric material of a deposited thin film capacitor or crossover.

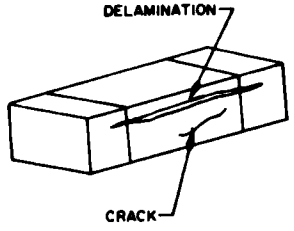
Reject - Crack or void that exposes metal plates.

FIGURE 2017-1A.



Reject - Crack that is more than 50 percent on a side and extends around a corner.

FIGURE 2017-1B.



Reject - Evidence of separation or delamination of capacitor plates.

FIGURE 2017-1C.

FIGURE 2017-1. Ceramic chip capacitor defects.

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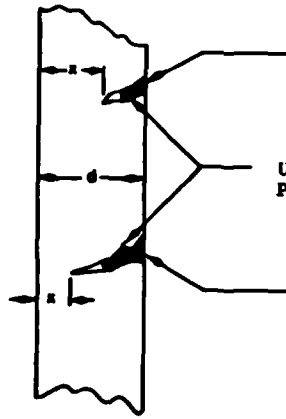


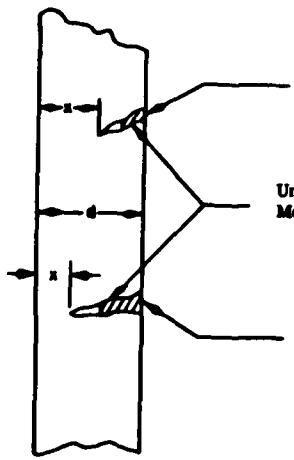
Accept - Scratch exposing underlying passivation where the remaining undisturbed metal width (X) is greater than d/2. (50 percent)

Underlying Passivation

NOTE:
d = Original metal width
X = Undisturbed metal width

Reject - Scratch exposing underlying passivation where the remaining undisturbed metal width (X) is less than d/2. (50 percent)

For multilayered metal products only



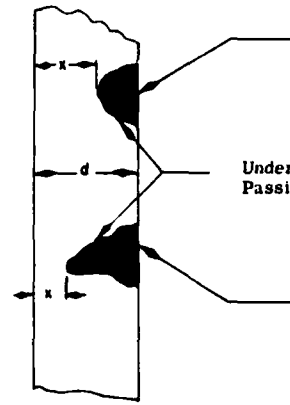
Accept - Scratch exposing underlying metal where the remaining undisturbed metal width (X) is greater than 0.3 mil.

Underlying Metal

NOTE:
d = Original metal width
X = Undisturbed metal width

Reject - Scratch exposing underlying metal where the remaining undisturbed metal width X is less than 0.3 mil.

FIGURE 2017-2. Scratch criteria.

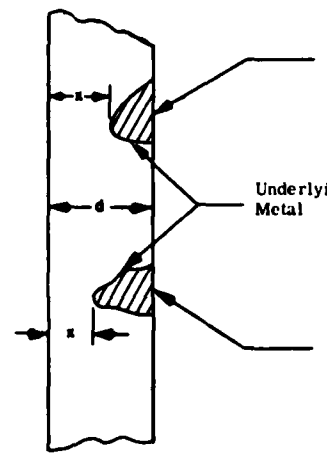


Accept - Void exposing underlying passivation where the remaining undisturbed metal width (X) is greater than d/2. (50 percent)

Underlying Passivation

NOTE:
d = Original metal width
X = Undisturbed metal width

Reject - Void exposing underlying passivation where the remaining undisturbed metal width (X) is less than d/2. (50 percent)



Accept - Void exposing underlying metal where the remaining undisturbed metal width (X) is greater than d/2. (50 percent)

Underlying Metal

NOTE:
d = Original metal width
X = Undisturbed metal width

Reject - Void exposing underlying metal where the remaining undisturbed metal width (X) is less than d/2. (50 percent)

FIGURE 2017-3. Void criteria.

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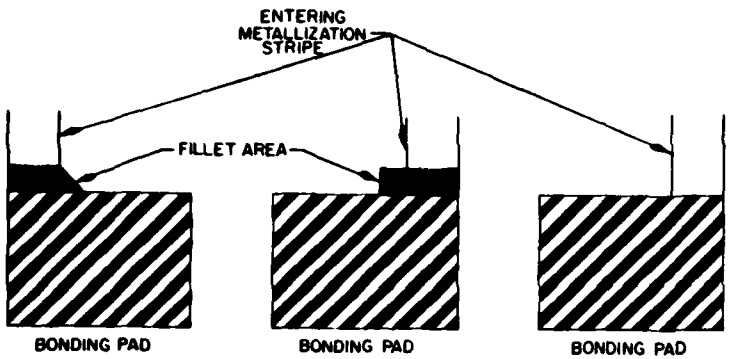
3.1.3.2.2 Metallization voids. A void(s) is any defect in the metallization where underlying metal or substrate is visible that is not caused by a scratch.

a. Void(s) in the metallization except for wire or beam lead bonding pads that leaves less than 50 percent of the original metal width undisturbed (see figure 2017-3).
b. Void(s) in the wire or beam lead bonding pad area that leaves an area less than twice the maximum allowable bond size undisturbed.
c. Void(s) in the wire or beam lead bonding pad, including fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width (see figure 2017-4).
   NOTE: If two or more stripes enter a bonding pad, each shall be considered separately.
d. Void(s) in the metallization of a thin film capacitor that reduces the metallization area by more than 25 percent.



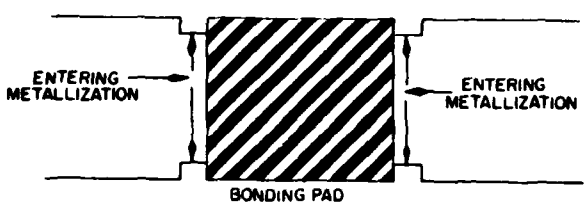


FIGURE 2017-4. Bonding pad areas.

3.1.3.2.3 Metallization bumps or indentations. Bump or indentation in the overlaying metallization of a deposited thin film capacitor or crossover.

NOTE: This criteria is excluded when multilayered dielectric material is used.

3.1.3.2.4 Metallization corrosion. Any metallization corrosion.

3.1.3.2.5 Metallization adherence. Any metallization lifting, peeling, or blistering.

3.1.3.2.6 Metallization probing. Criteria contained in 3.1.3.2.1 shall apply as limitations on probing damage.

3.1.3.2.7 Metallization bridging. Any metallization bridging where the separation between any two metallization paths is cumulatively reduced to less than 0.3 mil, whether caused by misalignment, photolithographic defects, screening defects, plating defects, smears, or other causes.

3.1.3.2.8 Metallization alignment:

a. Contact overlap between the metallization and film resistor that is less than 0.3 mil in length (see figure 2017-5).
b. Conductor and resistor overlap alignment width less than 75 percent of original resistor width (see figure 2017-5).
c. Any device in which the dielectric material of a film capacitor or a crossover does not extend beyond the width of the upper and lower metallization by 0.3 mil minimum.

3.1.3.3 Deposited resistors. Metallization defect criteria of 3.1.3.2 applies. In addition, no actively used device will be acceptable that exhibits:

3.1.3.3.1 General (thick and thin film).

a. Crack in resistor material longer than 0.3 mil.
   NOTE: Irregularities such as fissures in resistor material that do not expose the substrate that are created during resistor firing are not considered cracks.
b. Separation between any two resistors or resistor and conductor combination that is less than 0.3 mil, whether caused by misalignment, photolithographic defects, screening defects, smears, or other causes.
c. Void(s) or necking down that leaves less than 75 percent of the resistor width undisturbed at a terminal.
d. Resistor material left in the kerf (trimmed area) of a resistor.
e. Evidence of resistor repair.

3.1.3.3.2 Thin film resistor:

a. Any sharp change in color that indicates a change in thickness of the resistor material within 0.3 mil of the resistor/conductor termination.
b. Insulating layer that does not completely cover resistive material due to misalignment.
c. Less than 2.0 mils between any trimmed resistor area and conductor.
d. Trimmed resistor width less than 1.0 mil whether by trimming, voiding, or scratching or a combination thereof.

3.1.3.3.3 Thick film resistor:

a. Less than 5.0 mils between trimmed resistor area and conductor termination.
   NOTE: This criterion is excluded for laser trimmed resistors; however, 3.1.3.3.2c applies.

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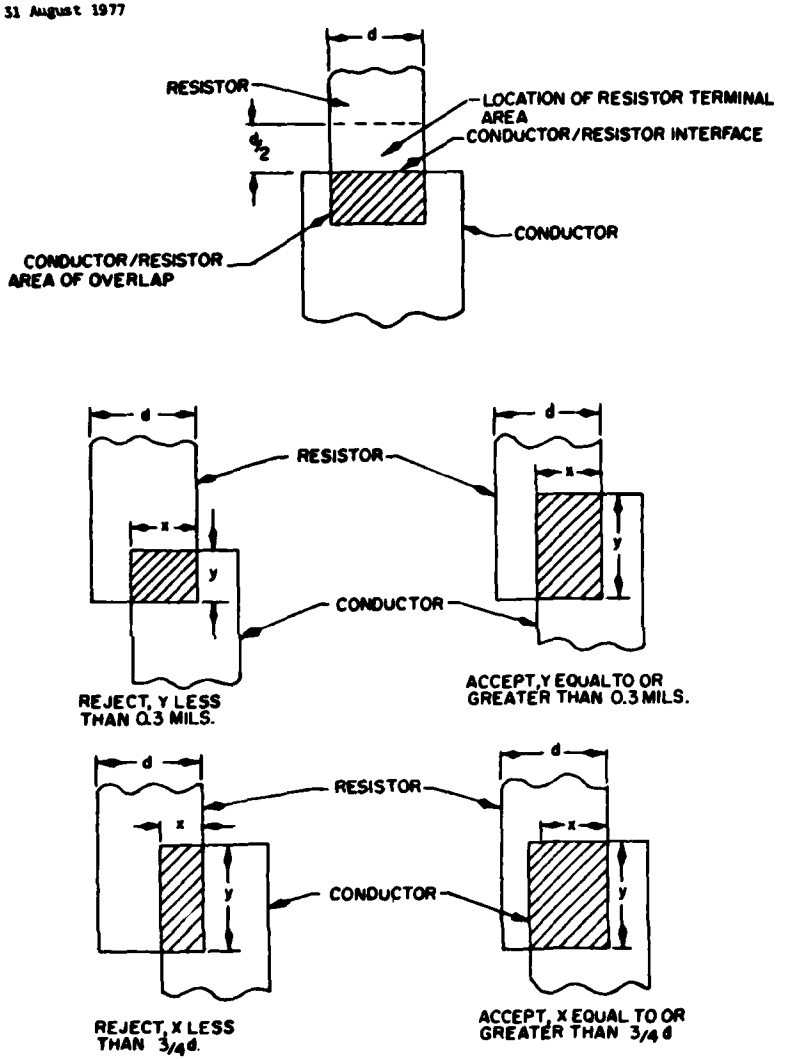

FIGURE 2017-5. Thin film resistor contact area

b. Trimmed resistor width less than 5 mils whether by trimming, voiding, or scratching or a combination thereof.

3.1.4 Component assembly to substrate, "magnification 10-60X." No device shall be acceptable that exhibits:

3.1.4.1 Solder or alloy component mounting (active and passive):

a. Solder or alloy not visible around at least 50 percent of the component perimeter or continuous on two sides of the component whichever is less.
   NOTE: End terminated components that have a fillet length less than 50 percent of the visible bonding perimeter on each end are not acceptable.
b. Component attach area less than 50 percent where the solder or alloy may be observed (i.e., glass substrate viewed from the bottom, transparent die).
   NOTE: This criterion may be employed in lieu of 3.1.4.1a.
c. Solder or alloy buildup that extends onto the top surface of the component.
   NOTE: End terminated components are excluded from this criteria.
d. Presence of any residual flux.
   NOTE: Use 10 to 15X magnification for passive components.
e. Foreign material in melt that does not exhibit a fillet.
f. Flaking of the solder or alloy material.
g. Balling of the solder or alloy material that does not exhibit a fillet (see figure 2017-6).
h. Solder or alloy material run out towards any isolated component or deposited element that leaves less than 0.3 mil separation.
   NOTE: Unused components or unused deposited elements are excluded from this criteria.
i. Solder or alloy material on wire or beam lead bonding pad that leaves an area less than twice the maximum allowable bond size free from such material.
j. Solder flow on end terminated components that reduces the original separation between end metallization contacts to less than 50 percent of the original separation or 1.0 mil whichever is greater.
k. End terminated ceramic chip capacitors that do not have a continuous metal conducting path composed of fillet and end termination metallization extending from the substrate mounting pad to the top of the capacitor.

3.1.4.2 Organic polymer component mounting (active and passive):

a. Organic polymer not visible around at least 50 percent of the die perimeter or continuous on two sides, whichever is less.
   NOTE: End terminated components mounted with a conductive organic polymer that have a fillet length less than 50 percent of the visible bonding perimeter on each end are not acceptable.
b. Component attach area less than 50 percent where the epoxy may be observed (i.e. glass substrate viewed from the bottom, transparent die).
   NOTE: This criterion may be employed in lieu of 3.1.4.2a.
c. Organic polymer buildup that extends onto the top surface of the die.
   NOTE: End terminated components are excluded from this criteria.
d. Crack in the organic polymer adhesive around the perimeter of the component greater than 5.0 mils in length or 10 percent of the contact periphery, whichever is greater.
e. Organic polymer run out toward any isolated component or deposited element that leaves less than 0.3 mil separation.
   NOTE: Unused components or unused deposited element are excluded from this criterion.
f. Organic polymer strings where the diameter of the string at the point of attachment is less than 50 percent of the maximum dimension of the string.

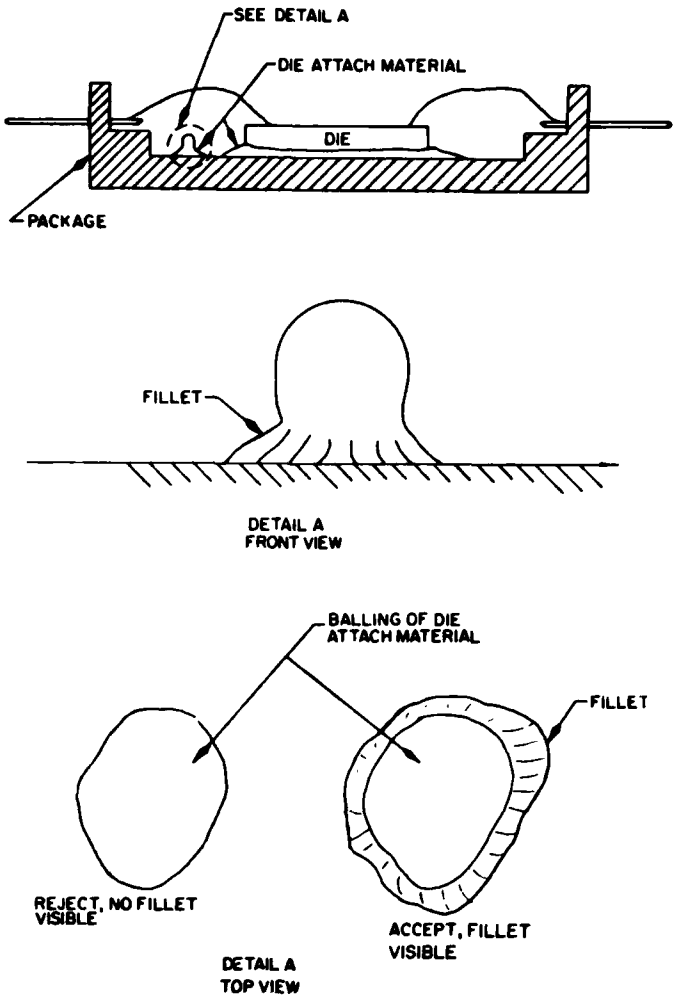

FIGURE 2017-6. Balling of die attach material.

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g. Organic polymer residue on a wire or beam lead bonding pad of a substrate or device, as evidenced by discoloration.
h. Organic polymer material on a wire or beam lead bonding pad.

3.1.4.3 Component orientation. Component not located or oriented in accordance with the applicable assembly drawing of the device.

3.1.5 Substrate mounting to package, "magnification 10 to 60X." No device shall be acceptable that exhibits:

3.1.5.1 Solder or alloy mounting:

a. Solder or alloy material not visible around at least 50 percent of the substrate perimeter or continuous on two sides of the substrate, whichever is less.
b. Solder or alloy material buildup that touches the top surface of the substrate and reduces the separation between the mounting material and operating metallization to less than 0.3 mil.
c. Presence of any residual flux.
NOTE: Use 10 to 15X magnification for passive components.
d. Foreign material in melt that does not exhibit a fillet.
e. Flaking of the solder or alloy material.
f. Balling of the solder or alloy material that does not exhibit a fillet (see figure 2017-6).
g. Less than 50 percent alloy or solder fillet around the circumference of the mounting posts when designed for substrate to post attachment.
h. Less than 25 percent fillet around the mounting post when substrate is mechanically attached by back side soldering or alloying.
i. Solder or alloy buildup that comes closer than 0.3 mil to package leads.
j. Solder or alloy material on substrate bonding pad that leaves an area less than twice the maximum allowable bond size free of such material.

3.1.5.2 Organic polymer mounting:

a. Organic polymer not visible around at least 50 percent of the substrate perimeter or continuous on any two sides of the substrate, whichever is less.
b. Organic polymer buildup that touches the top surface of the substrate or extends vertically above the edge of the substrate and reduces the separation between the mounting material and operating metallization to less than 0.3 mil.
c. Any crack in the organic polymer adhesive around the perimeter of the substrate greater than 5.0 mils in length.
d. Organic polymer strings where the diameter of the string at the point of attachment is less than 50 percent of the maximum dimension of the string.
e. Organic polymer residue on a bonding pad evidenced by discoloration.
f. Organic polymer material on bonding pad or substrate mounting posts.

3. 5.3 Substrate orientation. Substrate not located and oriented in accordance with the applicable assembly drawing of the device.

3.1.6 Bond inspection, "magnification 30 to 60X." This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above.
NOTE: Wire tail is not considered part of the bond when determining physical bond dimensions.

3.1.6.1 Gold ball bonds. No device shall be acceptable that exhibits:

a. Gold ball bonds on the die or package post where the ball bond diameter is less than 2.0 times or greater than 6.0 times the wire diameter.
b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.
c. Gold ball bonds where the wire center exit is not within the boundaries of the bonding pad.
d. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.

3.1.6.2 Wedge bonds. No device shall be acceptable that exhibits:

a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length (see figure 2017-7).
b. Thermocompression wedge bonds on the die or package post that are less than 1.5 times or greater than 3.0 times the wire diameter in width, or are less than 1.5 times or greater than 5.0 times the wire diameter in length (see figure 2017-7).
c. Wedge bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see figure 2017-8).

NOTES: 1. Criteria 3.1.6.2c can be excluded when the entering metallization strip is greater than 2.0 mils in width and the bond pad dimension on the entering metal stripe side is greater than 3.5 mils.
2. The requirements of 3.1.6.2c for a visual line of metal can be satisfied when an acceptable wire tail obscures the area of concern, providing the following condition exists. Bond is located more than 0.1 mil from the intersecting line of the entering metallization stripe and the bonding pad and there is no visual evidence of disturbed pad metallization at the bond and wire tail interface.

3.1.6.3 Tailless bonds (crescent). No device shall be acceptable that exhibits:

a. Tailless bonds on the die, substrate, component, or package post that are less than 1.2 times or greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater than 3.0 times the wire diameter in length (see figure 2017-7).
b. Tailless bonds where the bond impression does not cover the entire width of wire.
c. Tailless bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe (see figure 2017-8).

3.1.6.4 General (gold ball, wedge, and tailless). No device shall be acceptable that exhibits:

a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.
b. Bonds on the package post that are not completely within the boundaries of the package post.

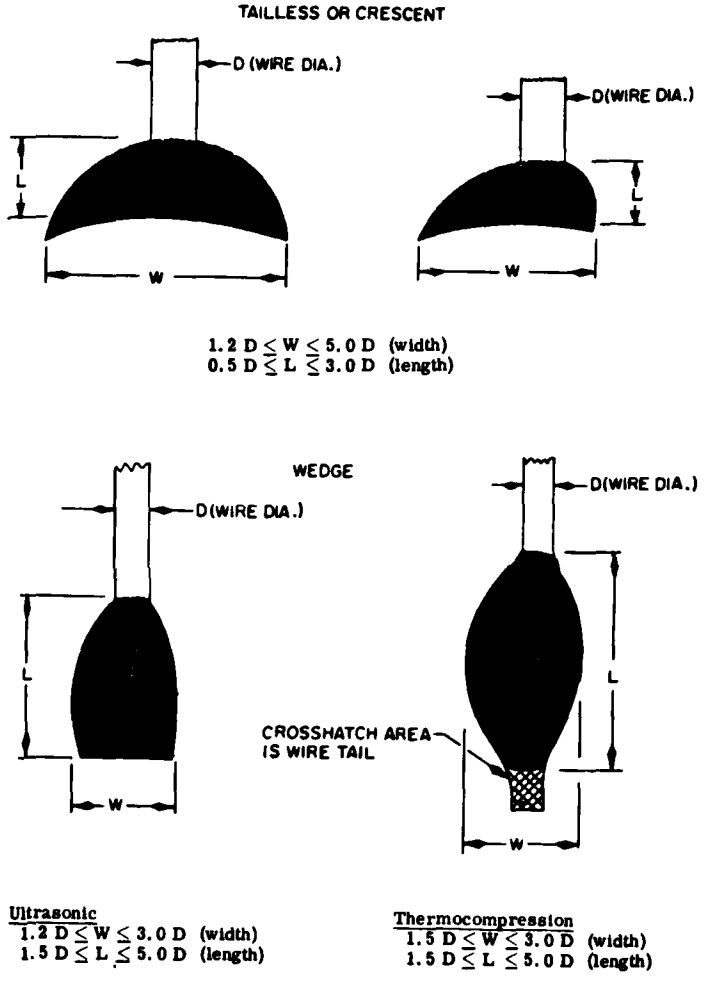
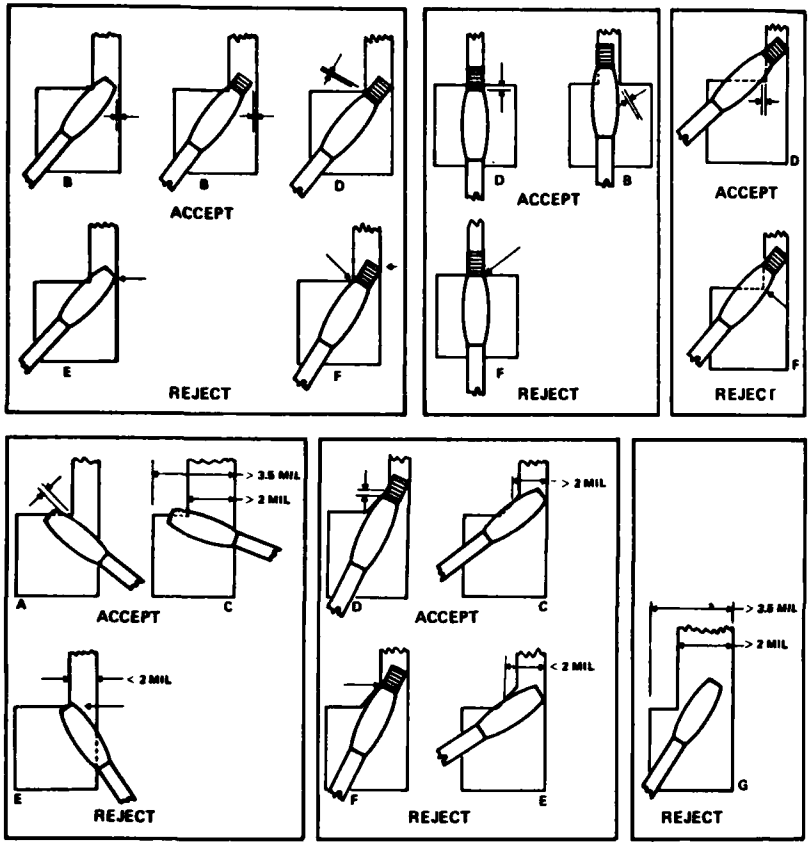


FIGURE 2017-7. Bond dimensions.



REASONS FOR ACCEPT OR REJECT DECISIONS:

A = **ACCEPT.** Because ≥50% of the bond area is on the bonding pad, and there is no bond at the point where metal exits from the bonding pad.

B = **ACCEPT.** Because ≥50% of the bond area is on the bonding pad, and there is a visible line of undisturbed connecting metal (>0.1 mil) between the bond periphery and at least one side of the entering metal.

C = **ACCEPT.** even though no visible line of connecting metal exists, since the entering metal width is >2 mils and the bonding pad dimension is >3.5 mils on the entering metal side, and ≥50% of the bond area is on the bonding pad.

D = **ACCEPT.** even though the bond wire tail prevents the connecting line of metal from being visible, because, (1) the bond periphery excluding the tail, is located ≥0.1 mil from the intersection of the entering metal stripe and the bonding pad, and (2) there is no visual evidence of disturbed pad metal at the bond and wire tail interface, and (3) ≥50% of the bond area is on the bonding pad.

E = **REJECT.** due to a bond at the point where metal exits from the bonding pad without a visible line of connecting metal, and the entering metal width is not>2 mils.

F = **REJECT.** due to the bond periphery (omitting the bond wire tail) being within 0.1 mils of the intersection of the entering metal and the bonding pad, and the bond wire tail obscures the possible connecting line of metal.

G = **REJECT.** due to a bond area <50% on the bonding pad, even though all other criteria are met.

FIGURE 2017-8. Bonds at metallization exit.

c. Bonds placed so that the wire exiting from the bond crosses over another bond.
d. Bonds placed so that the separation between bonds, or the bond and operating metallization not connected to it is less than 0.3 mil.
e. Wire bond tails that extend over or make contact with any metallization not covered by glassivation and not connected to the wire.
f. Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.
g. Bonds where less than 50 percent of the bond is located within an area that is free of die, chip, or substrate mounting material.
h. A bond on top of another bond.
i. Any rebonding which violates the applicable rework limitations of MIL-M-38510.

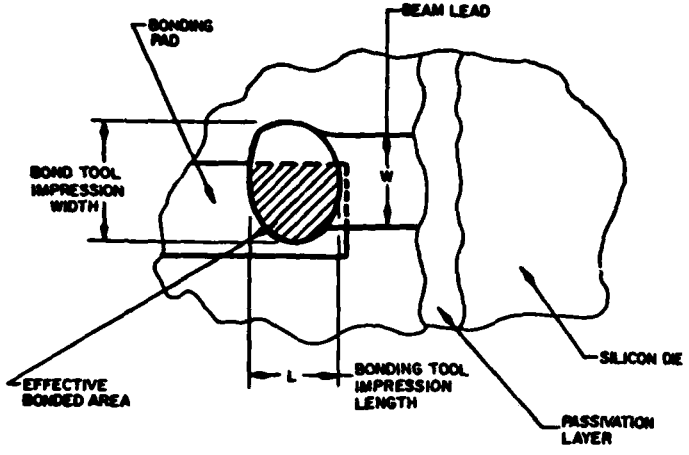
3.1.6.5 Beam lead. This inspection and criteria shall apply to the completed bond area made using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:

a. Bonds where the tool impression does not completely cross the entire beam width.
b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15 percent (10 percent for compliant bonds) or greater than 75 percent of the undeformed beam width.
c. Bonds where the tool impression length is less than 1.0 mil (see figure 2017-9).
d. Bonding tool impression less than 1.0 mil from the die edge (figure 2017-9).
e. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see figure 2017-9).
f. Cracks or tears in the effective bonded area of the beam greater than 50 percent of the original beam width.
g. Bonds placed so that the separation between bonds or between bonds and adjacent metallization not connected to them is less than 0.3 mil.
h. Bonds lifting or peeling.

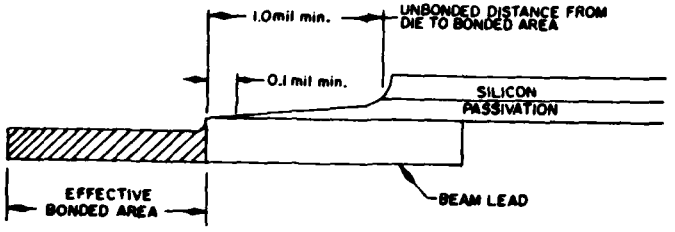
3.1.7 Internal leads, "magnification 10 to 60X." This inspection and criteria shall be required inspection for the lead type(s) and location(s) to which they are applicable.

3.1.7.1 Wires. No device shall be acceptable that exhibits:

a. Any wire that touches another wire (excluding common wires), package post, unglassivated operating metallization, die, or any portion of the package.
b. Excessive loop or sag in any wire so that it comes closer than two wire diameters to another wire, package post, unglassivated operating metallization, die, or portion of the package after a spherical radial distance from the bond perimeter on the die surface, of 5.0 mils for ball bonds, or 10 mils for ultrasonic and thermocompression wedge bonds.
c. Nicks, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.
d. Missing wires.
e. Wires not attached at both ends greater than two wire diameters in length at the bonding pad or four wire diameters in length at the package post.
f. Tearing at the junction of the wire and bond.
g. Any wire making a straight line run from die bonding pad to package post that has no arc.
h. Wire(s) crossing wire(s), except common conductors.
i. Wires not bonded in accordance with bonding diagram.



Beam lead bond area



Beam lead bond location

FIGURE 2017-9.

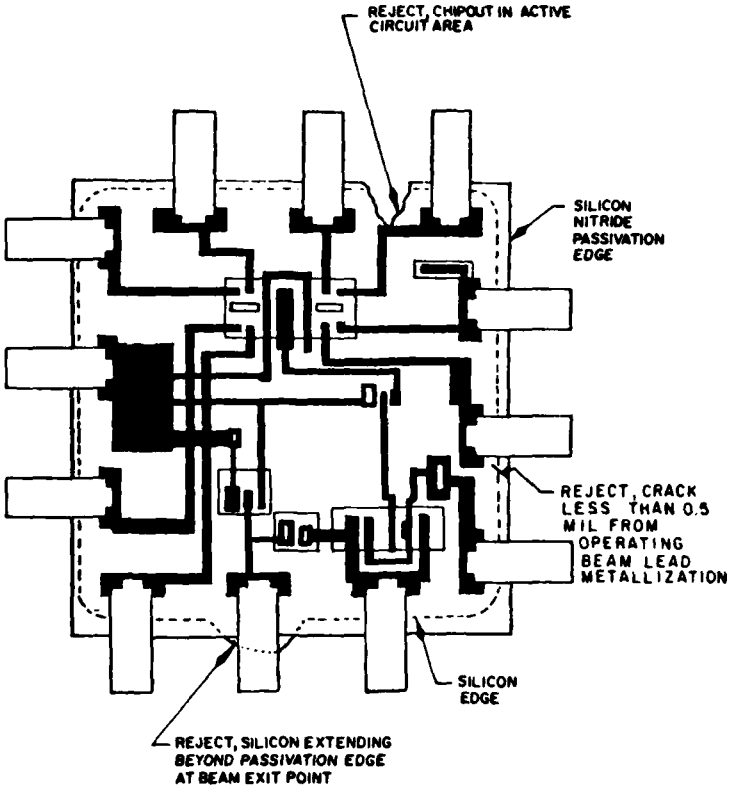


FIGURE 2017-10. Beam lead die faults.

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3.1.7.2 Beams. No device shall be acceptable that exhibits the following:

a. Voids, nicks, depressions, or scratches that leave less than 50 percent of the beam width undisturbed.
b. Beam separation from the die.
c. Missing or partially fabricated beam leads.
d. Beam leads that are not bonded.
e. Bonded area closer than 0.1 mil to the edge of the passivation layer.
f. Lack of evidence of a passivation layer between the die and each beam (see figure 2017-10).

3.1.8 Package conditions, "magnification 10 to 60X." No device will be acceptable that exhibits:

3.1.8.1 Foreign material:

a. Unattached foreign material on the surface of the die, substrate, or within the package.
b. Unattached foreign material on the surface of the lid or cap.
NOTE: Criteria of 3.1.8.1b can be satisfied by a nominal gas blow (approximately 20 psig) or a suitable cleaning process, providing the lids or caps are subsequently held in a controlled environment until capping.
c. Attached conductive foreign material that bridges metallization paths, two package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

a. Where applicable, any conflicts with approved circuit design topology or construction.
b. Where applicable, gages, drawings, and photographs that are to be used as standards for operator comparison (see 2).
c. Where applicable, specific magnification (see 3).

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EQUIPMENT

Microscopes

Metallurgical

Olympus Corp. of America, New Hyde Park, N.Y.	$1,600-2,140
Bausch & Lomb, Rochester, N.Y.	2,000-6,000
Nikon Inc., Garden City, N.Y.	2,600

Stereo (Brightfield)

Olympus Corp. of America	333-1,000
Bausch & Lomb	500-2,000
Nikon Inc.	675-2,200
Circon, Santa Barbara, California	2,257

Stereo (Darkfield)

Olympus Corp. of America	1,686-2,135
Bausch & Lomb	3,844-6,984
Nikon Inc.	3,300
Circon	3,530

Polarizing

Olympus Corp. of America	4,559
Bausch & Lomb	2,150
Nikon Inc.	4,900

Differential Interference Contrast

Olympus (attachments)	2,760
Bausch & Lomb	3,844-6,984
Nikon Inc. (attachment)	1,321
Circon	4,345

Hole Inspection

Bausch & Lomb (Stereo Zoom 4 Microscope with spot illuminator)	885
Nikon Inc.	750 & 850

Optical Microscopes

E. Leitz Inc. Rachleigh, NJ
Carl Zeiss Inc., New York, NY

EQUIPMENT (CONT'D)

TV Camera/Monitor with Video Tape/Cassette Recorder

RCA Camera/Electrohome Monitor; Micromanipulator Co., Escondido, California (with adaptors for 25 mm port trinocular microscope)	$1,090
Circon, Color Camera, Santa Barbara, California	
Model MV9270	7,950
MV9290	10,450
Circon MV9000 B&W Camera with 11" monitor	1,995
Circon MV9020 Color Camera with 9" monitor	7,650
Circon Video Cassette Recorder System for above cameras & monitors MV9469	2,375
Hitachi CCTV-100 9" monitor & B&W Camera, Woodside, New York	585
Sony Color Video Cassette Recorder, N.Y., N.Y.	850-7,500
Sony Color Video Tape Recorder	1,050-1,525
Sony B&W Cameras	430-1,395
Sony Color Cameras	1,400-4,900
Sony Monitors 8" B&W to 25" Color Trinitron	335-3,000
Motorola M4408-540, Shrewsbury, N.J.	549.53

Photomicrographic Equipment

Nikon Model HFM Camera and Adaptor	2,715
Olympus Cameras & Adaptors:	
35 mm system	2,963
4" x 5" Film System	3,101
3 1/4 x 4 1/4 Film System	3,004
Polaroid MP4 with monocular adaptor	1,300-3,800
Polaroid SX-70 and Adaptor; Available from Technical Enterprises, Gainesville, Florida	495
Bausch & Lomb (exclusively designed for Bausch & Lomb Cameras) Stereo Zoom 7®	
35 mm system	573
4" x 5" Film System	460
3 1/4 x 4 1/4 Film System	455
Polaroid MF-10 by Newton Plastics Corp., Newton Upper Falls, Mass.	135

Photocopy Systems

Polaroid CU-5 Hand Held System, Cambridge, Mass.	450
Polaroid Photo Copy Service, Cambridge, Mass.	
Rhedan Company (SX-70), New Haven Conn.	
Polaroid MP-4 Model XLR Photographic Recording System with Photofloods, 135mm lens and 4"x5" Film System	1,500
Bowens Macro-Lite Dual Strobe Illuminator	200
Kenro MP-812 Camera Head (8"x10" Film System)	800
Polaroid 8"x10" Processor	500
Polaroid 8"x10" Model 8105 Film Holder	100

Adolph Buehler Inc., Evanston, Illinois
(Dealer for Leitz, Reichert, Bausch & Lomb, American Optical, Unitron Microscopes)

M.

CHEMICAL ANALYSIS TECHNIQUES

M. Chemical Analysis Techniques.

1. Introduction. Acids, bases, special chemical solutions, and solvents are used heavily in failure analysis of microelectronics. Vital information about failure mechanisms can be obtained through cleaning procedures and through selective thin film and bulk material etches. These techniques involve several varieties of chemicals.

In general, all the chemicals used in failure analysis are potentially dangerous. However, some may be more harmful than others. For instance, the resulting burns to human skin from hydrofluoric acid and hydrochloric acid are vastly different. See Chapter IV, Laboratory Safety Procedures, for more information on safety measures and handling procedures.

2. Chemical Storage Requirements. Different classes of chemicals should be stored separately. Acids and bases should not be stored in the same location because of possibly violent reactions and dangerous gases that may be released when an acid and a base are brought together. Relatively small amounts of these materials can react to produce a large amount of gas accompanied by a significant quantity of heat. Likewise, acids and organic solvents should not be stored together because of the danger of fire when the two come in contact. Reactions may occur to produce sufficient heat to ignite certain solvents.

a) Acid Storage. Acids should be stored in an area designated strictly for this purpose. The containers used to store acid should be handled with extreme care, be kept closed, and be clearly labeled. The storage cabinet should be made of materials that are relatively impervious to attack from acids, such as the molded resin materials. The storage cabinets and surrounding area should be well-vented to prevent formation of pockets of toxic fumes. Any metal surfaces in the area should be painted and be checked periodically for corrosion.

No acid should be handled without proper protection. Rubber gloves, aprons, face mask, etc., should be worn when handling acids. Acid etching should be done in a fume hood equipped with proper venting of reaction products. Chapter IV, Laboratory Safety Procedures, contains more information on proper safety procedures.

b) Storage of Bases. The same type of container as described for storage of acids is applicable to storage of basic materials. Special care should be taken to keep water away from this storage area, because basic substances often are purchased and stored in solid form. When many of these solid bases are dissolved, very exothermic reactions may take place.

c) Solvent Storage. The use and storage of solvents present a constant fire hazard. This danger should be kept in mind at all times. Solvents should be stored in a double wall metal cabinet that is fireproof. Such containers are commercially available and contain vapor venting capability which should be used as specified by the manufacturer.

3. Chemical Lists. Following are tables listing acids, bases, solvents, and other chemical solutions commonly used in microelectronic failure analysis.

These lists, as indicated throughout this Guidebook, are by no means complete. It is felt, however, that a laboratory equipped with the chemicals listed can successfully perform most failure analysis techniques involving chemical procedures.

It is understood that, in addition to chemicals, a laboratory must be equipped with basic supplies. Equipment such as stainless steel tweezers, laboratory glassware, thermometers, hot plates, fume hoods, eyedroppers, etc., must be readily available to perform chemical procedures.

TABLE I

ACIDS

Name	Chemical Formula	Uses
Acetic, glacial	CH_3COOH	Etchant; buffering agent
Boric	H_3BO_3	Buffering agent
Chromic	CrO_3	Etchant, stain
Formic	HCOOH	Polar solvent
Fuming Nitric	HNO_3	Plastic package opening
Fuming Sulfuric (Oleum)	$H_2S_2O_7$	Plastic package opening
Hydrobromic	HBr	Metal etchant, stain
Hydrochloric	HCl	Metal etchant
Hydrofluoric	HF	Silicon dioxide and silicon etches
Nitric	HNO_3	Metal etchant; silicon nitride etchant; used in many silicon etchants as oxidizer
Oxalic	$HOOCCOOH \cdot 2H_2O$	Etchant; stain
Phosphoric	H_3PO_4	Metal etchant; polish
Sulfuric	H_2SO_4	Etchant; strong oxidizer

TABLE II

BASES

Name	Chemical Formula	Uses
Ammonium hydroxide	NH_4OH	General base
Potassium hydroxide	KOH	Silicon etchant
Sodium hydroxide	NaOH	Aluminum etchant

TABLE III

SOLVENTS

Name	Chemical Formula	Uses
Acetone	CH_3COCH_3	Polar solvent; solvent for plastics
Benzene	C_6H_6	Nonpolar solvent
Benzyl alcohol	$C_6H_5CH_2OH$	Polar solvent; solvent for plastics
Chloroform	$CHCl_3$	Polar solvent
Cyclohexane	C_6H_{12}	Nonpolar solvent
Dimethyl formamide	$HCON(CH_3)_2$	Polar solvent; solvent for plastics
Dimethyl Sulfoxide	$(CH_3)_2SO$	Solvent
Diethylether (Ethyl Ether)	$(C_2H_5)_2O$	Organic solvent
Ethanol (Ethyl Alcohol)	C_2H_2OH	Polar solvent
Ethylene dichloride	CH_2ClCH_2Cl	Solvent
Freon (Tetrachlorodi-fluoroethane)	$C_2F_2Cl_4$	Nonpolar solvent
Hexane	C_6H_{14}	Mild nonpolar solvent
Isopropyl alcohol	$(CH_3)_2CHOH$	Polar solvent
Methyl alcohol	CH_3OH	Polar solvent
Methylene chloride	CH_2Cl_2	Solvent for plastics & epoxies
Methyl Ethyl Ketone (Butanone)	$CH_3COC_2H_5$	Solvent; solvent for PVC
Toluene	$CH_3C_6H_5$	Nonpolar solvent
Trichloroethylene	$CHCl{:}CCl_2$	Nonpolar solvent
Xylene	C_8H_{10}	Nonpolar solvent

TABLE IV

OTHER CHEMICALS

Name	Chemical Formula	Uses
Ammonium bifluoride	$NH_4F \cdot HF$	Silicon dioxide etch; buffering agent
Ammonium chloride	NH_4Cl	Buffering agent
Ammonium fluoride	NH_4F	Buffering agent
Ammonium persulfate	$(NH_4)_2S_2O_8$	Buffering agent
Ammonium sulfide	$(NH_4)_2S$	Source of sulfide
Bromine	Br	Constituent preferential silicon etch
Calcium carbonate	$CaCO_3$	Buffering agent
Cupric sulfate (Copper Subsulfate)	$CuSO_4$	Stain
Cupric nitrate (Copper Nitrate)	$Cu(NO_3)_2$	Constituent preferential silicon etch
Ferric chloride	$FeCl_3$	Nichrome etch
Hydrogen peroxide	H_2O_2	Etchant; stain; oxidizer
Iodine	I	Constituent silicon etch
Nickel sulfate	$NiSO_4.6H_2O$	Stain
Potassium chloride	KCl	Buffering agent; electrolyte
Potassium cyanide	KCN	Etchant
Potassium ferricyanide	$K_3Fe(CN)_6$	Constituent molybdenum, tungsten etch
Potassium iodide	KI	Constituent gold etch
Pyrocatechol	$C_6H_4(OH)_2$	Constituent silicon stain
Sodium acetate	$NaCH_3COO \cdot 3H_2O$	Buffering agent; etchant
Sodium bicarbonate	$NaHCO_3$	Buffering agent; electrolyte
Sodium chloride	NaCl	Buffering agent; electrolyte

TABLE IV

OTHER CHEMICALS (CONT)

Name	Chemical Formula	Uses
Sodium citrate	$Na_3C_6H_5O_7 \cdot 2H_2O$	Buffering agent
Sodium cyanide	NaCN	Alkaline etchant
Sodium hypochlorite	NaOCl	Constituent silicon etch
Sodium hypophosphite	$NaH_2PO_2 \cdot H_2O$	Reducing agent
Sodium potassium tartrate	$NaKC_4H_4O_6 \cdot 4H_2O$	Buffer used in silicon crystal studies
Sodium silicate	$Na_2SiO_3 \cdot 9H_2O$	Etchant; coater
Sodium sulfide	$Na_2S \cdot 9H_2O$	Stain
Stannous chloride	$SNCl_2 \cdot 2H_2O$	Catalyst
Zinc Oxide	ZnO	Stain

TABLE V

PROPRIETARY MIXTURES

Name	Manufacturer	Use
FL-70, Industrial detergent	Fisher Scientific	Cleaning; wetting agent
Uresolve Plus	Dynaloy, Inc.	Removal urethane; silicones; varnishes
Dynasolve 100	Dynaloy, Inc.	Removal of potting epoxies
Dynasolve 160	Dynaloy, Inc.	Removal of some potting epoxies
J-300	Indust-Ri-Chem Laboratory, Inc.	Removal of molded compounds; silicone; epoxy
DECAP	Dynaloy, Inc.	Removal of some epoxies
ECCOSTRIP	Emerson & Cumming	Removal of some epoxies
Fluorinert Liquids	3M Company	Neutral cleaning; gross leak test; testing for high power spots

4. Cleaning Methods. The general purpose of any chemical cleaning in failure analysis is to remove visible residues or invisible contamination from the exterior or interior surfaces of the unit under investigation. Such contamination may be responsible for or may be a contributing factor in device degraded electrical performance.

Contamination may be polar, non-polar, ionic, or organic in nature, and therefore no single cleaning procedure is usually sufficient to remove all forms of contamination. For instance, strong bases such as potassium hydroxide are extremely difficult to remove in a water rinse alone, even though KOH dissolves quite readily in water. In this case, a mild acid rinse, followed by water, then a strong detergent rinse again followed by water will usually remove the basic contaminant.

Once the device being investigated has been thoroughly leak tested (see Chapter III-C) and no leaks found, the exterior surface can be cleaned. This is a nondestructive procedure. On the other hand, the package will have to be opened (see Chapter III-E) to clean the interior surfaces if this should be desired. Cleaning, under these circumstances, is at best a semi-destructive procedure.

Any external materials such as tape or lead insulation tubing should be removed from the package and kept. In the case of a leaky condition, it might be desirable to retest the unit to determine if the external material's removal in any way affected device electrical characteristics. If the same electrical characteristics exist, then the unit can be cleaned in a number of ways. The unit should be retested after each individual cleaning step to evaluate any electrical change that may occur as a result of the cleaning step.

There is a definite order in which cleaning mediums should be used. This is the case because it is possible to affect a contaminant in such a way that a cleaner which would normally remove it will no longer do so. Consider, for instance, the case of an oil film being

either on the exterior or interior surface. If this film were exposed to a water rinse first, there might result a gummy film that no longer exhibits the characteristics of the original oil film. The chances are that organic solvents would not remove the residue completely.

Cleaning should be done in steps designed to remove contaminants in the following order: organic materials, nonorganic and other non-water-soluble materials, water soluble materials. The reason for this order was illustrated by the above example of what could happen when rinsing an oil filter in water. In general, solvents for organic materials will have little effect on water soluble materials, while the reverse is not true. Care must be exercised in the choice of chemicals to be used in cleaning so as not to affect the package or any active elements inside. Special care must be taken when the packaging material is plastic.

a) Cleaning Steps for Organic Materials. An example of an organic contaminant is oil.

- Some of the solvents which may be used in this cleaning step are trichlorethylene, freon, toluene, xylene, hexane.
- Pour sufficient solvent to cover the unit into a beaker.
- Using locking tweezers or other appropriate implement, dip the unit into the solvent for several minutes, using a continuous stirring motion.
- Blow the unit dry with a stream of dry air or dry nitrogen.
- Retest the unit if appropriate. If the electrical parameters are unchanged, proceed to the next cleaning step.

b) Cleaning Steps for Polar Materials. Water, many compounds containing chlorine, and many nitrogen compounds are examples of polar substances.

- Some of the solvents which may be used in this cleaning procedure are acetone, propanol, methanol.
- Pour sufficient solvent to cover the unit into a beaker.
- Using locking tweezers dip the unit into the solvent for several minutes, stirring continuously.
- Blow the unit dry with dry air or dry nitrogen.
- Retest the unit if appropriate. If the electrical parameters are unchanged, proceed to the next cleaning step.

c) Cleaning Steps for Nonorganic and Ionic Materials. All salts belong to this category.

- The solvents that may be used in this step are deionized water, detergent in deionized water.
- Pour sufficient deionized water to cover the unit into each of two beakers.
- Add 2-3 drops of concentrated detergent solution to the second beaker and stir.
- Using locking tweezers, immerse the unit into the deionized water and then into the detergent solution for several minutes each.

- Rinse the unit in clean, preferably running deionized water for several minutes.

- Optionally, immerse the unit into one of the solvents from cleaning step b) to speed drying.

- Blow the unit dry.

- Retest the unit if appropriate. If the electrical parameters are unchanged, proceed to the next cleaning step.

d) Cleaning for Other Ionic Materials. Many carbonate compounds might possibly remain at this point.

- The solvents to be used here are the acids. Care must be used not to use an acid that will affect either the package material or the metallization systems present. Special care must be used if the package has been opened because of potential damage to the active device and interconnecting metallization systems.

- Mix the desired concentration of acid by slowly adding, with constant stirring, the concentrated acid to the appropriate amount of deionized water in a beaker.

- Using locking tweezers, immerse the unit into the beaker and stir. It may be desirable to limit the time to 1 minute or less.

- Transfer the unit to a beaker filled with clean deionized water for a quench of 1 minute.

- Further rinse the unit in clean, preferably running, deionized water.

- Optionally, immerse the unit into one of the solvents from cleaning step b) to speed drying.

- Blow the unit dry.

- Retest the unit if appropriate. If the electrical parameters are unchanged, proceed to the next cleaning step.

e) Cleaning for Remaining Ionic Materials. It is conceivable that some ionic species still remain at this point.

- The solvent used in this cleaning step is a basic solution. The same safety precaution as mentioned in step d) must be observed here as well, as basic solutions can potentially cause damage to packaging materials and metallization similar to acid reactions.

- Follow the procedure as outlined in step d) above, except that a basic solution is substituted for the acid solution.

If the electrical parameters remain unchanged and the package has not yet been opened, it might be desirable to open the package and repeat the cleaning procedures. If, after cleaning both the exterior and interior of the package and electrical parameters remain unchanged, it can be reasonably assumed that the electrical problem is not due to surface contamination. If, during some step in the cleaning procedures the electrical problem is cured, then some insight into what the source of the problem is will be gained.

The use of ultrasonic cleaners in conjunction with the cleaning methods discussed previously would greatly enhance the degree of cleaning. However, it must be kept in mind that ultrasonic energy during the cleaning could be detrimental to the mechanical integrity

of the device and/or internal wire bonds. The use of ultrasonic energy could alter the results of electrical testing, further complicating the failure analyst's task. For example, marginal wire bonds or die attachments may be sheared as a result of ultrasonic action. This detrimental aspect of ultrasonic cleaning must be weighed against the advantages when deciding whether ultrasonics should be used.

5. High Purity Water Systems. The need and the ability to remove sources of contamination during failure analysis is vital. Once having removed contamination, it is important to ensure that other sources of contaminants are not replaced during cleaning or other steps where rinsing is performed.

The Total Dissolved Solids (TDS) in water are ionizable solids in the form of cations and anions. Some of the materials that appear in the form of anions are chloride, nitrate, sulfate, silica, carbonate, and phosphate. Typical cations are magnesium, iron, sodium, and calcium.

There are a number of water purification systems in use throughout industry today. Some of these systems are ultrafiltration, reverse osmosis, ultraviolet sterilization, deionization, and distillation. All of these systems use filtration. Generally speaking, ultrafiltration, reverse osmosis, and ultraviolet sterilization are not, alone, capable of producing water of the quality needed in the field of microelectronic work.

The standard for water in the industry is on the order of 18 megohms. Water in the 2-20 ppm range, generally obtained with distillation, corresponds to resistivity of 2.5×10^5 ohms down to 2.5×10^4 ohms. This means that first stage distillation water should be double or triple distilled to meet industry standards. Distillation under these circumstances becomes quite expensive.

Deionization is an effective and relatively inexpensive alternative. The process of deionization involves two distinct reactions, whereby added ions are exchanged for the ions present in untreated water.

The selection of a water system depends on several variables, some of which are:

- o Solids content of source water
- o Organic colloid content
- o Desired resistivity
- o End use
- o Desired pressure
- o Amount of flow rate required

6. Material Removal. Listed below are etchants for specific materials that are encountered in microelectronic failure analysis work. Some of these etches are selective and will remove one specific material, while others will remove several materials. An example of this behavior is that some metal etches will attack more than one metal.

Unless otherwise specified, all the chemicals in this table represent the as-purchased "concentration" form. The symbol designation "W/W" means that mixtures are to be made by weight, while the symbol "V/V" indicates mixtures are to be made on the basis of volum measurements.

TABLE VI

MATERIAL REMOVAL

Material	Chemical Composition	Comments
Aluminum	1. Phosphoric acid	Heat to 50°C
	2. Hydrochloric acid	Room temperature
	3. 1g - Potassium hydroxide 100ml - Water	Slow etch
	4. 3 parts - Sulfuric acid V/V 2 parts - Hydrogen peroxide V/V	Rapid etch
	5. 2 Parts - H_2O V/V 1 part - HNO_3 V/V 1 part - HA_C V/V 16 parts - H_3PO_4 V/V	
	6. Plasma - BCl_3 gas mixture	Exact pressures, flow rates, and power to be determined for particular instrument
Copper, copper based alloys	1. 10ml - Water 10ml - Ammonium hydroxide 10ml - 3% Hydrogen peroxide	
	2. Nitric acid	Dilute to obtain desired etch rate
Gold	1. 1 part - 10% Potassium ferricyanide (aqueous) V/V 1 part - 10% Ammonium persulfate (aqueous) V/V	
	2. 4.6g - Potassium iodide 1.3g - Iodine 100ml - Water	Thin film etch
	3. 1 part - Hydrochloric acid V/V 3 parts - Nitric acid V/V	Aqua Regia (bulk etch)

TABLE VI

MATERIAL REMOVAL (CONT)

Material	Chemical Composition	Comments
Molydbenum	1. 100ml - Water 30g - Potassium ferricyanide 10g - Sodium hydroxide	
Nichrome	1. 2.25 - 3.75 Molar ferric chloride (aqueous) 2. 6g - Ceric sulfate 10ml - Nitric acid 90ml - Water	Heat to 55°C
Nickel based alloys	1. 60ml - Ethanol 15ml - Hydrochloric acid 5g - Ferric chloride	
Plastics, epoxies	See Table V and Chapter III-E	
Platinum	1. 1 part - Nitric acid V/V 3 part - Hydrochloric acid V/V	Aqua Regia
Poly silicon	1. 80ml - Nitric acid 60ml - Acetic acid 5ml - Hydrofluoric acid 2. Plasma with freon gas (CF_4)	Flow rates and power to be determined for particular machine
Silicon	1. 20% Potassium hydroxide in water W/W	Heat to 40 - 50°C. Can be used to remove die from package.
	2. 3 parts - Hydrofluoric acid V/V 5 parts - Nitric acid 2 parts - Water	Etches approximately 76 microns/min.
	3. 3 parts - Hydrofluoric acid V/V 5 parts - Nitric acid 2 parts - Acetic acid	Etches approximately 100 microns/min.
	4. Plasma with freon gas (CF_4)	Flow rates and power to be determined for particular instrument

TABLE VI

MATERIAL REMOVAL (CONT)

Material	Chemical Composition	Comments
Silicon dioxide	1. 25ml - Hydrofluoric acid 56g - Ammonium fluoride 75ml - Water	
	2. 1 part - Hydrofluoric acid V/V 10 part - Ammonium fluoride solution V/V	Ammonium fluoride solution: 1 lb. NH_4F in 680ml H_2O Etches SiO_2 7 - 10 Å/sec.
	3. 1 part - Acetic acid V/V 1 part - Ammonium fluoride solution V/V	Etches 700 - 900 Å/sec
Silicon monoxide	1. 40% Ammonium fluoride solution W/W (aqueous) 2% Sodium hydroxide solution W/W (aqueous)	Mix to give pH 9 Heat to 50°C
Silicon nitride	1. Phosphoric acid	Heat to 180°C in commercially available water cooled reflux condenser.
	2. Plasma with freon gas (CF_4)	Flow rates and power to be determined for particular instrument.
Soft solder	1. 1 part - Acetic acid V/V 1 part - 30% hydrogen peroxide	Selectively removes solder such as type used for die bonding without attacking backing metallization or heat sink.
Steel (carbon)	1. 98ml - Ethanol 2ml - Nitric acid	NOTE: May form explosive mixture
Steel (stainless)	1. 3 parts - Glycerol V/V 3 parts - Hydrochloric acid V/V 1 part - Nitric acid V/V	NOTE: May form explosive mixture
Titanium	1. Sulfuric acid	Heat to 80°C
Tungsten	1. 100ml - Water 30g - Potassium ferricyanide 10g - Sodium hydroxide	

TABLE VI (CONT'D)

Material	Chemical Composition	Comments
Gold (Preferential Etch)	1. Liquid Gallium (3-9's purity) a. DI Water b. Concentrated Hydrochloric acid	NOTE: Preferential gold etch using Gallium in the presence of refractory metals. Mount device on a glass slide using Apiezon W wax. Leave area to be etched clean. Fill a 50ml beaker with liquid gallium to sufficient depth that the mounted device can be immersed in it. The gallium should be about 3-9's or better. Heat the Ga to between 60°C and 80°C, using a Hg lab thermometer to measure the temperature. During the heating, cover the Ga with DI to a depth of 1cm. When the temperature is stabilized, add concentrated HCL acid to the beaker, a drop at a time until the Ga surface is clean and bright. Immerse the device into the Ga for about 3-5 minutes. Inspect the device to determine if the gold is removed. The Ga dissolves the gold if the device has been wetted by the Ga. To assure wetting, the device must be clean prior to immersion. Continue immersion until desired amount of gold is removed. Periodically add drops of HCL to the water, if the Ga surface oxidizes. Note that the device must be immersed in the metals. Dilute HCL will etch some metals, and even GaAs with prolonged immersion. Therefore, keep the device in the Ga, and upon removal rinse it with DI water.

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3. Anstead, R.J., et al. "Failure Analysis of Electronic Parts: Laboratory Methods," U.S. Dept. of Commerce, Nat. Tech. Info. Ser., N75-23853, 1975.

4. "NASA Failure Analysis Methods," Contract NAS 5-21444.

5. The Condensed Chemical Dictionary, Reinhold Publishing Corp., NY, NY.

6. Handbook of Chemistry and Physics, CRC Press, Inc. Cleveland, Ohio.

EQUIPMENT

Chemical Supplies

Prices available on request from:

Fisher Scientific Co, Pittsburgh, PA

Cole Parmer, Chicago, IL

Allied Chemical, Morristown, NJ

MCB Reagents, MCB Manufacturing Chemists, Inc., Cincinnati, Ohio

Transene Co. Inc., (Proprietary Etches-Stains) Rowley, Massachusetts

Eastman Organic Chemicals (Kodak), Rochester, New York

General Laboratory Supplies

Prices available on request from:

Fisher Scientific Co, Pittsburgh, PA

Cole Parmer, Chicago, IL

Macalaster Bicknell Co, Syracuse, NY

Water Control Systems

1. Corning "Mega-Pure" Stills
   1.4 - 11.4 liters/hour — $450 - $2,400

2. Barnstead Glass Stills
   3.8 - 19 liters/hour — $700 - $2,100

   Fisher Scientific Co, Pittsburgh, PA

3. Continental Automatic Deionization System
   2 - 50 gallons/minute — $10,000 - $40,000

   Continental Water Conditioning Corp., El Paso, TX

4. Automatic Deionizer System
   2 - 50 gallons/minute — $10,000 - $40,000

   Water Refining Co., Inc., Middletown, OH

5. Deionizer Water System
   2 - 60 gallons/minute — $10,000 - $40,000

   Culligan, Buffalo Water Specialists, Inc., Tonawanda, NY

N.

METALLURGICAL ANALYSIS TECHNIQUES

N. Metallurgical Analysis Techniques.

1. Introduction. The techniques described in this chapter allow the failure analyst to locate, observe, document, and measure semiconductor failure sites that are related to bulk semiconductor phenomena.

2. Cross Sectioning. Cross sectioning of semiconductor devices is used as a means of identifying causes of defects located by other methods, such as fault isolation. The process of sectioning and abrasively polishing specimens for microscopic examination has been referred to as a "metallographic technique." More recently the process has been widely expanded to include numerous applications in the electronic industry. Complex semiconductor devices contain highly dissimilar materials such as silicon, refractory metal alloys, silicon oxides, solders and ceramic substrates. These materials require modification of the basic technique to retain fragile interfaces and resolve microdefect areas. These areas are arbitrarily defined as being less than 25 μm in diameter. The technique necessary to reveal small defect areas is referred to as "Precision Metallography."

A great deal of patience and skill is required in performing these techniques. With sufficient practice, the failure analyst can section through a 25 μm wire bond or a 12 x 12 μm contact window.

It should be kept in mind at all times that precision metallography techniques are essentially a "one shot" operation. That is, if the area of interest is missed, there is no second chance.

a) Sample Preparation. Thorough preparation of the specimen is vital to achieve acceptable final results. Adequate knowledge of the sample, any unusual problems/materials, the area of interest, appearance, etc., all should be taken into account during sample preparation.

o Mapping. The microelectronic sample must be mapped and documented so the area of interest can be retained for future reference. Figure 1 is an overall die macro photograph of a typical sample. The arrow notes a base contact window to be cross-sectioned. The actual base contact window to be sectioned measures 7.6 by 33 μm. Since the section plane is to be parallel to the window's short dimension, the total depth of the target area exceeds 25 μm. Figure 2 is a higher magnification micrograph which details the target area.

o Encapsulation. Encapsulation must be in a transparent medium since the failure analyst must be able to view his progress as he grinds/polishes into the specimen. Any of a number of resins are available such as Buehler epoxide. If at all possible, the IC/semiconductor die should be removed from the substrate; otherwise it will greatly increase all aspects of sectioning difficulties. The specimen should be thoroughly cleaned in an ultrasonic bath; final wash can be FREON TF and methyl alcohol. This ensures adhesion between the epoxy and die surface.

- Encapsulation Method I. Buehler has available the "EPO-KWICK" epoxy kit which includes epoxy, mounting cups, release agent, and mixing tools, etc. The "Sampl-Kup"^{R} is a plastic 1 1/4" dia. x 1" high two-piece mounting form that facilitates rapid sample encapsulation. The sample cup is disassembled, coated inside with release agent, reassembled, and the epoxy mixture poured in half-way only. This is allowed to thoroughly cure before the specimen is encapsulated. HINT - It is best to have a few half-mounts prepared before hand to speed up the process. Next, place the specimen face-up on the half-mount and pour in the epoxy.

An alternative to the "Sampl-Kup"^{R} is the use of "Bakelite" (organic plastics) ring forms permitting standard size (1", 1 1/4" and 1 1/2" OD) ring forms to be used as specimen mounting molds. The epoxy and "Bakelite" ring forms used are AB EPO-MIX EPOXIDE (20-8133) and AB BAKELITE RING FORMS (20-8151 and 20-8152), BUEHLER LTD. The epoxy can be procured either in bulk quantities

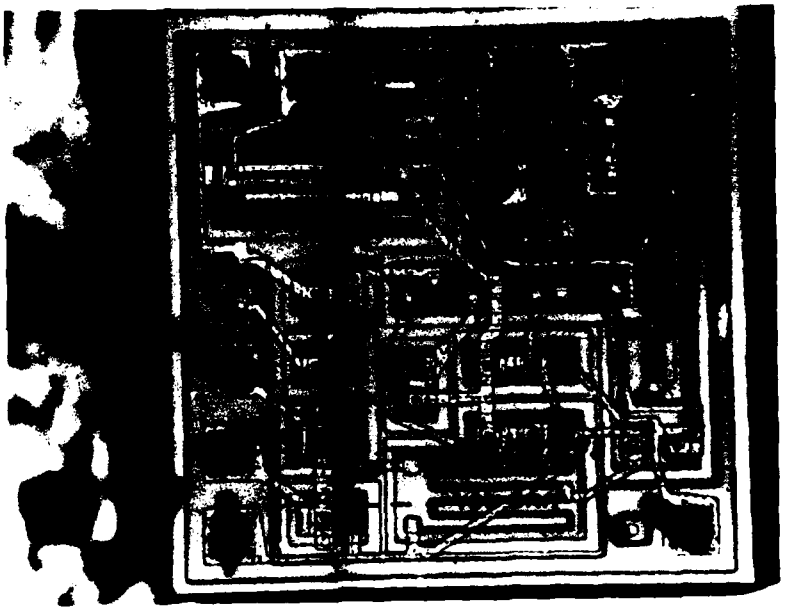


FIGURE 1. PHOTOMICROGRAPH OF BIPOLAR MICROCIRCUIT SAMPLE. ARROW POINTS TO AREA OF INTEREST. HORIZONTAL LINES AND MARKING INDICATE TO WHAT DEPTH THE GRINDING/POLISHING SHOULD BE DONE WITH WHAT ABRASIVE.

FIGURE 2. ENLARGED PORTION OF MICROCIRCUIT SHOWN IN FIGURE 1. ARROW POINTS TO BASE CONTACT WINDOW.

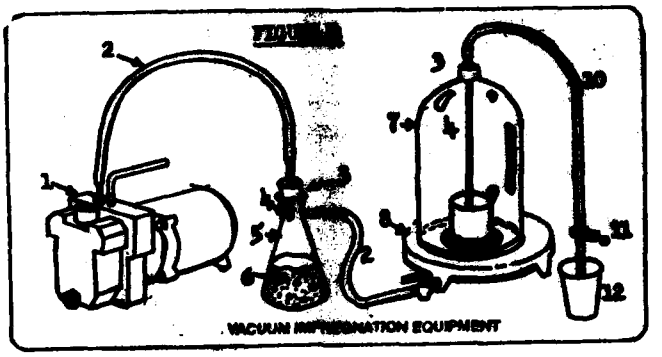
(resin and hardener) or in premeasured packets for convenient dispensing. The premeasured packets, containing both resin and hardener, use a separator which is removed prior to mixing in the package itself. Thus, the time consuming task of measuring (weight or volume) constituents, blending and dispensing the epoxy is eliminated. The mounting method uses a "Bakelite" ring form of proper diameter to accommodate the specimen size and is placed on a glass or Teflon plate (dimensions ∿4" x 4") which has been coated with silicone grease or other mold release compound. Two methods are commonly employed to position the specimen near the mold center. First, the specimen can be placed flat perpendicular to a pedestal (e.g. nylon or other plastic cylinders of proper height) and the mold subsequently filled with the premixed epoxy with care taken not to pour epoxy directly on the specimen to maintain specimen orientation. Plastic pedestals are preferred since they generally match the epoxy hardness and contain no metal. Metal pedestals result in metallic particles during sectioning which load the abrasive papers and cloth wheel covers excessively and can cause damage to delicate structures. Second, the mold can be partially filled with epoxy and allowed to cure. The specimen is then placed on the top surface of the cured epoxy in the proper orientation and the mold filled with additional epoxy. It should be noted that using either method the specimen can be orientated at any angle with respect to the original horizontal plane by either positioning the specimen at the desired angle during mounting or machining the completed mount to the desired angle after epoxy cure. The aforementioned epoxy type used cures at room temperature in 6-8 hours and curing can be accelerated by modified mixing and exposure at elevated temperatures as specified by the manufacturer.

One problem commonly encountered in epoxy cold mounting of microelectronic devices is air entrapment within the epoxy. This occurs during mixing of bulk material (resin and hardener) and to some degree with premeasured epoxy packets, as

well as during mold filling in either case. The entrapped air results in void formation within the mount and at the specimen surface itself. Voids at the specimen surface are particularly detrimental since specimen edge protection provided by the epoxy is essential for high quality metallurgical sections. These voids also produce pockets for abrasive material entrapment and subsequent edge damage to the specimen during sectioning. Voiding can be partially alleviated by allowing the mixed epoxy to settle for a short time prior to filling the mold. This procedure alone is insufficient for obtaining required specimen edge protection, i.e., 100% coverage of the specimen peripheral surface area; thus, vacuum impregnation must be employed when delicate structures not within the bulk specimen are to be sectioned. Two methods for vacuum impregnation are commonly used.

- Vacuum Impregnation of Epoxy Mounts, Method 1.

The equipment necessary for this technique and a suggested method of assembly are shown in Figure 3. To ensure success, the device should be thoroughly cleaned and dried to promote optimum penetration and adherence of the epoxy to the device. The device to be mounted is positioned in the desired orientation within a 1" or 1 1/4" Bakelite ring form sealed to a Teflon plate using silicone grease, and placed under the bell jar. HINT - See Buehler Ltd. Sample-Klip specimen support springs, No. 20-4000. Also, ordinary machine screw nuts, e.g., 6-32 hexagonal brass, serve well as convenient pedestals for devices when stood up on end in the center of the ring form. The glass portion of the entrance tube should be close to the top of the ring form but should not touch the device itself or extend into the ring form. At this point, the pinchcock is closed and evacuation begun. The amount of vacuum should be adjusted to stabilize just above the predetermined boiling point of the impregnation medium (i.e., if the boiling point of a specific medium is 20 mm of mercury, then the vacuum should be adjusted to about 22 mm). When the vacuum has stabilized, the free end of the entrance tube is placed in the disposable



1. Vacuum Pump
2. Vacuum Hose
3. Rubber Stopper
4. Glass Tubing
5. Erlenmeyer Flask
6. Dehydrating Agent
7. Bell Jar
8. Pump plate and Pad
9. Ring Form on Teflon Plate
10. Plastic Tubing
11. Hose Clamp
12. Disposable Paper Cup

FIGURE 3. VACUUM IMPREGNATION EQUIPMENT.

container holding the impregnating material. The pinchcock is opened slowly to draw the plastic into the disposable container. After the sample is completely covered, the pinchcock is closed and evacuation continued for a few moments longer.

The vacuum pump is then switched off and the pinchcock slowly reopened to allow pressure in the bell jar to return to normal. At this point the greatest penetration of plastic takes place, since the greater external pressure forces the impregnating material into the voids. The sample is then allowed to cure. The equipment should be cleaned immediately after use to avoid hardening of any residual plastic.

- Vacuum Impregnation of Epoxy Mounts, Method 2.

In this simplified method, the ring form containing the device (with Teflon back plate in place) is filled with epoxy and placed under the bell jar. The vacuum pump is connected to the jar by means of a valve which allows the selection of either evacuation of the jar or alternately a leak to atmosphere. Vacuum impregnation is effected by alternately evacuating and back leaking the system pressure while carefully observing the removal of air bubbles from the mount. This cyclic method is necessary to permit the generation of optimum vacuum pressure by allowing instant control to prevent boiling off the volatile constituents contained in the epoxy. The onset of boiling in the epoxy is usually disastrous to the mount since sudden eruption and instant localized or general hardening can occur. A possible improvement to this technique would be to limit the vacuum to a pressure just above the boiling point of the epoxy material used.

Method 2 is certainly simpler and also cleaner in use since the suction tube of Method 1 is not required. The choice between the two methods is debatable as to superiority of the cured mount. Method 1, which allows pre-evacuation of the device, should prove to be valuable in the removal of air entrapped in pockets and cavities of the device structure. However, additional air bubbles are carried to the mount from the free end of the entrance tube via the epoxy stream when the pinchcock of Figure 3 is opened. In Method 2, the rapid evacuation and pressurization cycle can efficiently produce relatively void free mounts if care is used. In any vacuum impregnation method there is a danger in maintaining the evaccuation cycle for an excessive duration. In this situation tiny bubbles (due to the boiling off of volatiles) will continue to escape with no apparent cessation. In time, however, they will become immobile, indicating that the epoxy has partially hardened. It is surmised that the removal of volatiles results in the premature hardening experienced. For best results, the evacuation cycle should be short. A number of experimental runs should be performed to determine the boiling

point of the epoxy used as described in techniques for Method 1. Then using a vacuum pressure above this predetermined boiling point, the cycle time to the escape of bubbles (volatile constituents) is determined. The vacuum pressure and evacuation cycle should be kept within the safe limits of the above findings.

- Encapsulation Method II. In this encapsulation method, Polyvinyl Chloride (PVC) $(-H_2CCHCl-)_n$, a synthetic thermoplastic resin compound, is used. This method can only be used when the sample can withstand the required temperatures and pressures for mount thermo-setting under applied pressure. Figure 4 shows the hydraulic press and mold assembly used in this method.

Because the three mold parts are machined to tight tolerances for close fit, each must be thoroughly clean (soft cloth only) and dry and care should be taken to avoid dropping these parts. Before starting be sure that the 2 1/2 inch long plunger will pass completely through the mold. Mold release (lubricant) can be used on the interior mold surfaces to facilitate removal of the PVC after cure; however, it is not essential.

Insert the 3/4 inch thick, 1 1/4 inch diameter base plug into the 1 1/4 inch (inner diameter) mold, until it is flush with the bottom of the mold, being sure that the dull side of the base plug is facing down. Fill the mold to 3/4 inch below the top with PVC powder. Place the specimen centered and horizontal on the leveled surface of the PVC and then pour in additional PVC to a level 1/8 inch below the mold top. Insert the 2 1/2 inch long plunger in the top of the mold, taking care to align the plunger with the molding bore and be certain that the recessed hole is facing up. The 2 1/4" deep hole serves as a receptacle for a (0 - 100°C) thermometer which measures the temperature of the mold. Open the pressure release valve on the press, and push the top plate of the hydraulic jack all the way

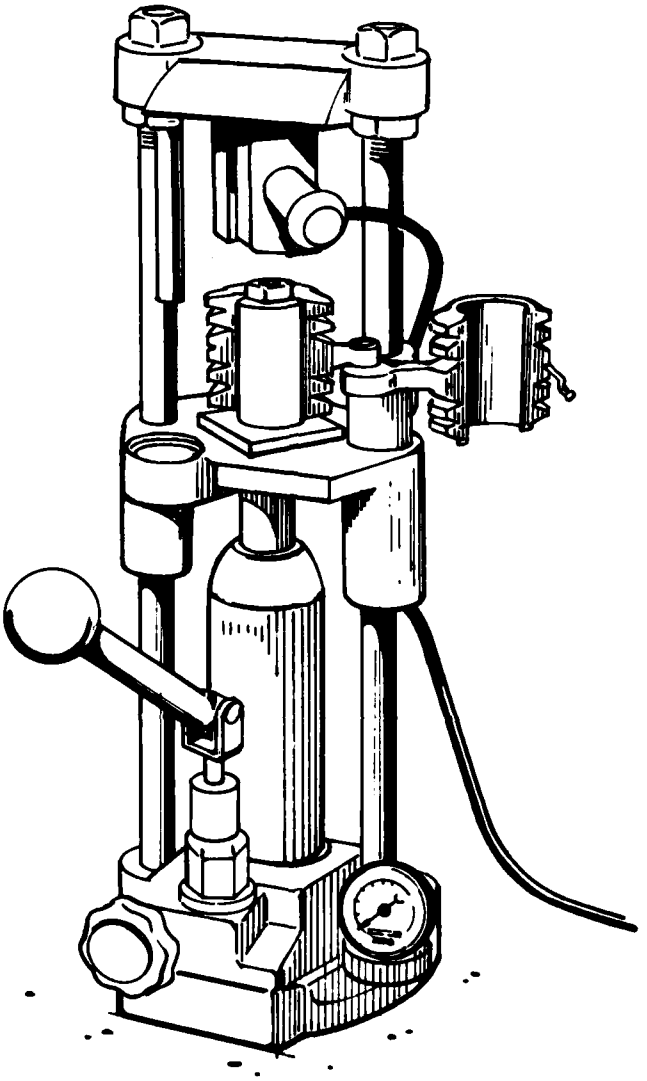


FIGURE 4. HYDRAULIC PRESS AND MOLD ASSEMBLY USED IN PVC MOLDING

*For definition of parts, refer to page III-N-65 in Appendix C.

down. Place the mold on the press insulating plate within the center markings and slide the heating collar over the mold. Then close the pressure release valve and snug up the mold to about 100 psig, being careful to align the pressure rod and plunger thermometer channels. A 5 ampere variac is used to regulate the temperature of the heater and the variac dial is set at 48-50 to establish and maintain a molding temperature of approximately 80-82°C as measured with a glass stem mercury thermometer inserted in the top plug.

Allow the mold temperature to reach ∿ 80°C, then pump the pressure up to 4000-4500 psig (measured on the outside scale of pressure gauge for 1 1/4 inch mold and inside scale for the 1" mold). Maintain the temperature and pressure for 30 minutes. Under compression the PVC mold temperature will rise; therefore, the variac voltage should be reduced to compensate for this and maintain proper temperature. It is essential throughout the process to maintain the temperature and pressure constant (80-82°C and 4000 psig, respectively). Higher temperatures will cause darkening of the PVC plastic and lower temperatures will result in fibrous pockets (cotton balls) within the mount interior. Low applied pressure will result in a soft plastic and voids within the mount. After 30 minutes at temperature under pressure, lift the heating collar to the collar hook adjacent to the pressure ram and turn off the variac. Allow the mold to cool to 40-45°C with the proper size cooling jacket placed around the mold before releasing the pressure. The latter is accomplished by opening the pressure release valve and with both hands forcing the lower plate to a full down position. The specimen is removed by placing the mold over the ejection opening on the left-hand side of the lower plates under the ejection stem and then applying hydraulic pressure. Catch the lower plug, PVC, and upper mold plug upon removal to avoid damage. The mold temperature at removal (40-45°C) is low so that asbestos gloves are not required as for higher temperature removal molds. Due to approximately 3:1 volume

shrinkage during melting of the PVC, the above method results in a mount 1 1/4" diameter and ∿ 3/4" thick. The specimen will be enclosed within the mount ∿ 1/4" below the top surface. Provided this procedure is followed, the PVC will be nearly transparent (amber color), allowing observation of the specimen surface and orientation to facilitate rough grinding at the proper angle to the region of interest. Prior to sectioning with abrasives, bevel the PVC mount edges with the belt sander for ease of handling and safety. If necessary to retrieve the specimen from the finished mount, Methyl Ethyl Ketone (MEK) can be used to dissolve the hardened PVC. Since this reaction is slow, it is advisable to remove (cut away) as much PVC material as possible.

o Viewing Window. The specimen, mounted in the epoxy which is subsequently cured, has a flat surface ground and polished onto it in such a manner that a clear, undistorted view of the die surface can be obtained with a binocular-zoom microscope. Figure 5 shows the mounted specimen after the upper surface has been ground and polished. Figures 6a and 6b illustrate the quality of the image obtainable through the epoxy of the sample surface. After the viewing window is formed, the sample should be oriented and marked to determine the plane of section and which portion is to be rough cut and ground away (Figure 6b).

b) Rough Grinding. This is a two-stage procedure which varies according to the material of the package surrounding the die.

Gross material removal can be accomplished with a fine slow speed diamond saw (i.e., Buehler-Isomet) before or after mounting in epoxy, by a more conventional cut-off tool, or by rough grinding with silicon carbide papers on a metallographic wheel. Figure 7 shows the Buehler-Isomet saw.

The prime rule in dealing with semiconductors is: THE DIE SHOULD NEVER BE TOUCHED BY SiC PAPERS COARSER THAN 600 GRIT.

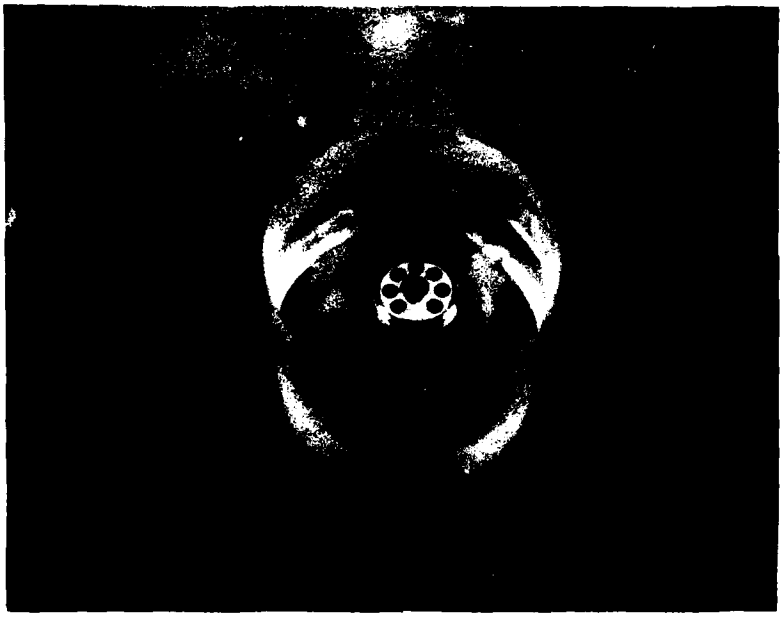


FIGURE 5. MOUNTED SPECIMEN WITH VIEWING WINDOW FORMED

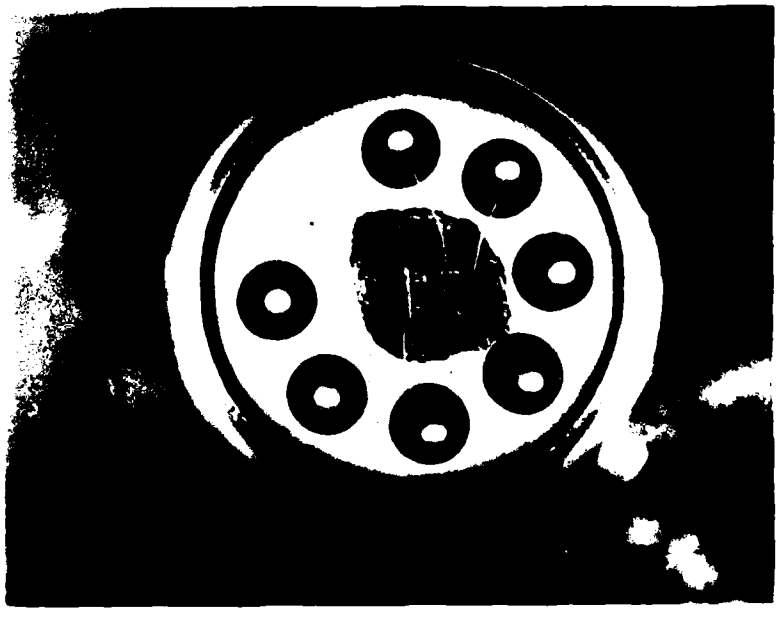


FIGURE 6a. DEMONSTRATES QUALITY OF OPTICAL IMAGE THROUGH EPOXY

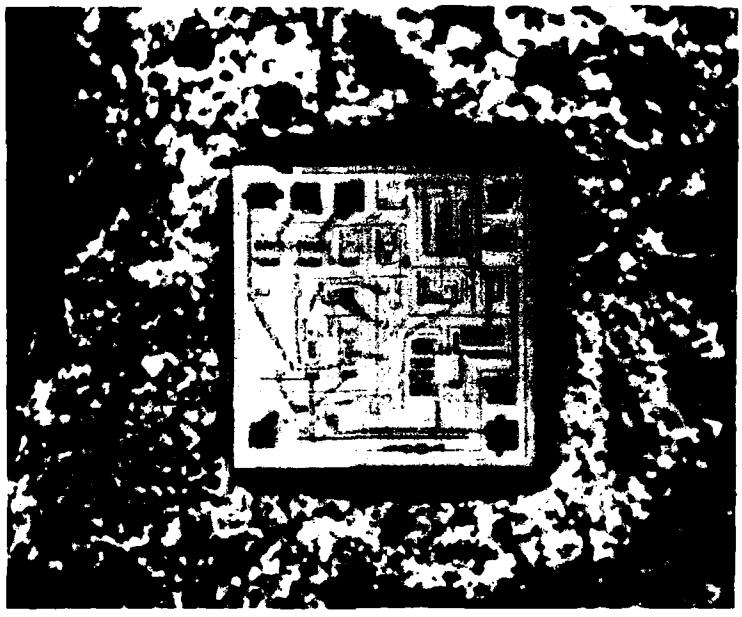


FIGURE 6b. SECTION OF PLANE ALONG WHICH GRINDING AND POLISHING OPERATIONS SHOULD BE DONE

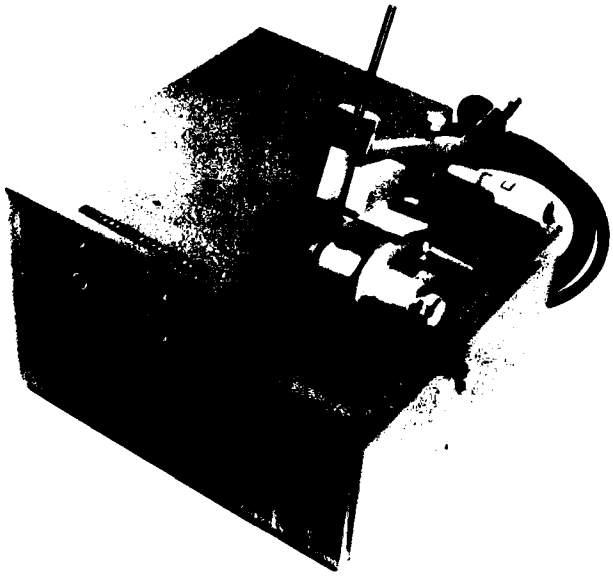


FIGURE 7. BUEHLER-IS[illegible]L' SPEED DIAMOND SAW

All coarse preparations should result in a section parallel to the plane of interest but not in contact with the die. Figures 8a and 8b illustrate the condition of the specimen after the first stage preparation with 240-grit paper. For continued ease of viewing through the top surface, the section plane should be undercut 5 to 10 degrees below the die surface (Figure 9). This will skew depth measurements by a small percent but on complex dice will tremendously aid in orientation.

Final rough grinding may be performed with 400-grit paper if good adhesion between epoxy and die surfaces exists. This is the process which will begin to cut away the silicon die material, and mistakes, even in the early stages, may result in shattering or cracking of the entire die. Best results are achieved with wet grinding at 500-700 rpm on ring-mount paper, i.e., there is no glue or adhesive on the back of the SiC paper to hold it down. The glue creates a slightly uneven and soft backing which tends to create control problems.

The specimen should be hand-held with even pressure onto the surface of the wheel in such a manner that the grinding action takes place from the top of the die downward. The cutting action should be kept perpendicular or only slightly angled to the die surface.

The 400-grit paper rough grinding is continued to within about 50 μm of the area of interest.

c) Fine Grinding. The final, fine grinding is accomplished with 600-grit SiC paper with copious water lubrication at low (500-700 rpm) speeds. Here again, ring-mount paper is preferred to the adhesive backed type. The grinding is accomplished by hand holding the specimen in contact with the grinding paper and the grinding action occurs from top to bottom of the die surface. This fine grinding proceeds to within about 7 μm of the area of interest, resulting in a specimen of the appearance shown in Figures 10a and 10b. The fine-grinding operation is the last opportunity to adjust the plane of the section with respect to the specimen geometry.

FIGURE 8a. TOP OF SAMPLE SEEN THROUGH VIEWING WINDOW AFTER ROUGH GRINDING

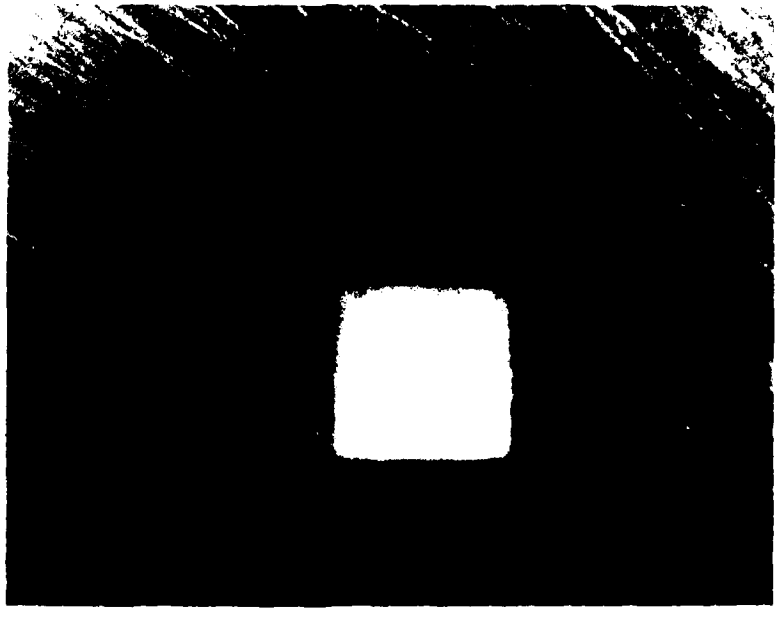


FIGURE 8b. CROSS SECTIONAL VIEW OF SAMPLE AFTER ROUGH GRINDING

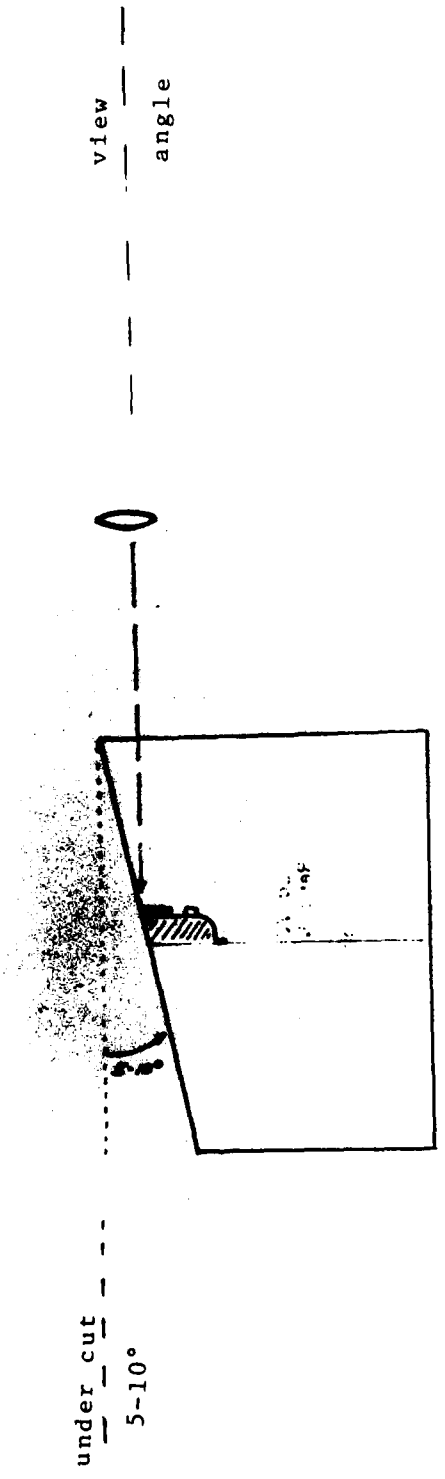


FIGURE 9. DEMONSTRATES UNDERCUT OF SECTION PLANE TO FACILITATE EASE OF VIEWING

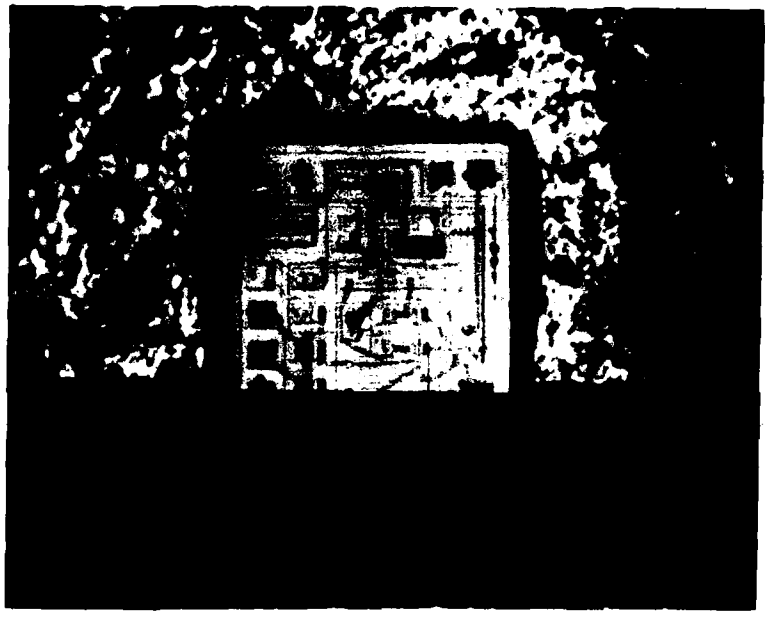


FIGURE 10a. TOP OF SAMPLE SEEN THROUGH VIEWING WINDOW AFTER FINE GRINDING

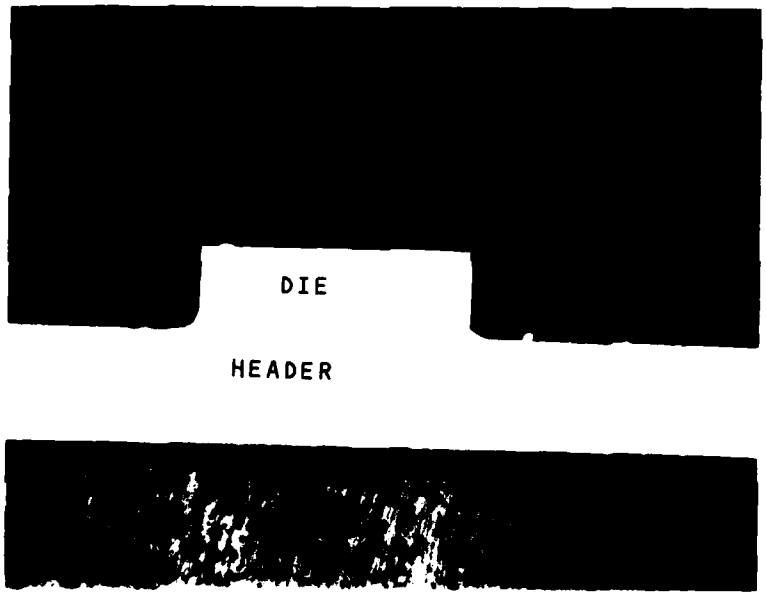


FIGURE 10b. CROSS SECTIONAL VIEW OF SAMPLE AFTER FINE GRINDING

d) Rough Polish. The specimen is thoroughly cleaned after the fine-grinding operation to prevent contamination of the diamond polishing cloth. Rough polishing is performed satisfactorily using 6-micron diamond paste on a synthetic material called Texmet (Buehler). This polishing uses very heavy pressure (~ 7 to 10 pounds) and is continued until all the 600-grit scratches are removed and the surface structures of the IC become visible (see Figures 11a and 11b).

e) Final Polish. The final finish of the specimen surface is achieved, utilizing very fine alumina powders, graded 1.0, 0.3, and 0.05 micron sizes and used on velvet-like cloth (Buehler) identified "microcloth." More recently, diamond abrasives graded in 6.0, 1.0, and 0.25 micron sizes and used on "Texmet" covered wheels have been popular. The foregoing are of polishing grade grit sizes and are used with water/oil lubricant extenders. The precautions of cleanliness must be adhered to even more carefully in the final polishing stages, since this is the final step wherein the true microstructure of the device is revealed. Once again, ring-mount cloths which allow free movement of the lubricant into the surface is found to give the best results. The sample is hand-held against the surface of the cloth, the wheel is used in a low-speed mode, and the hand(s) holding the sample are rotated counter to the rotation of the wheel. This causes multi-directional polishing action to occur, somewhat decreasing the preferential effect which is the bane of all metallographers. The cloth should be charged with polishing solution. First saturate the wheel-cloth with DI water and then charge the cloth with a polishing solution of 5 to 10 cc. Additional DI water from a squirt bottle will replenish the wheel during the polishing steps. The final polishing step (sample in contact with the polishing cloth) should never be more than 40-60 seconds. If all previous steps are properly executed, a 60-second final polish will result in a finished sample similar to that in Figures 12a and 12b. The sample is now ready for cleaning with cotton swab and liquid soap. Rinse and blow dry. This "as polished" surface is shown in Figures 13a and 13b.

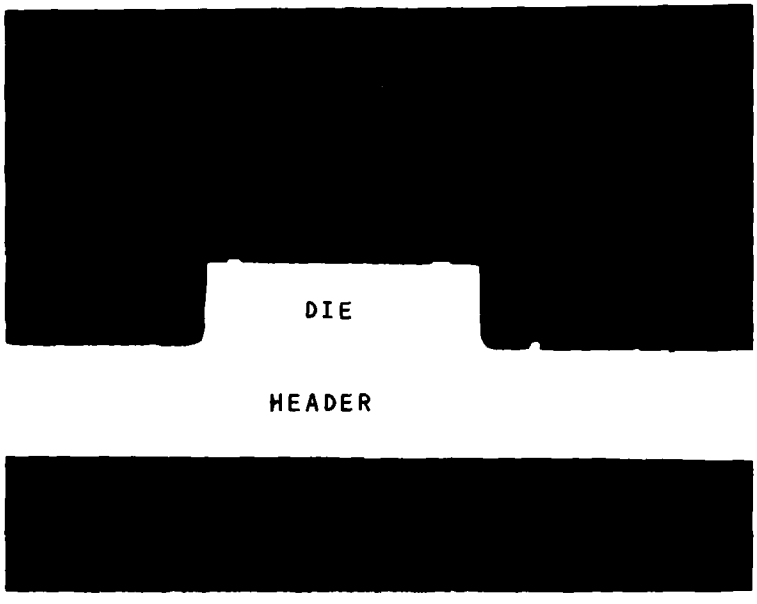


FIGURE 11a. CROSS SECTIONAL VIEW OF SAMPLE AFTER ROUGH POLISH: DETAILS ON TOP SURFACE OF MICROCIRCUIT BECOMING VISIBLE

FIGURE 11b. HIGHER MAGNIFICATION CROSS SECTIONAL VIEW AFTER ROUGH POLISH SHOWING FINER DETAIL OF MICROCIRCUIT SURFACE

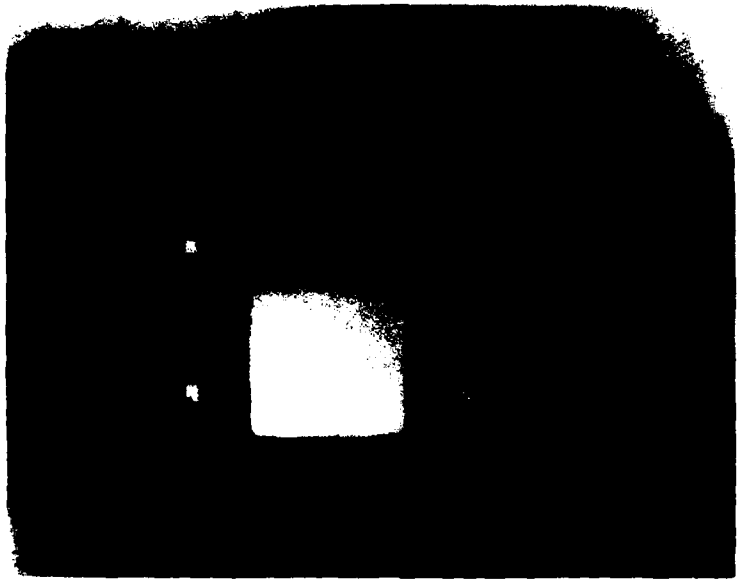


FIGURE 12a. CROSS SECTIONAL VIEW OF SAMPLE AFTER FINAL POLISH

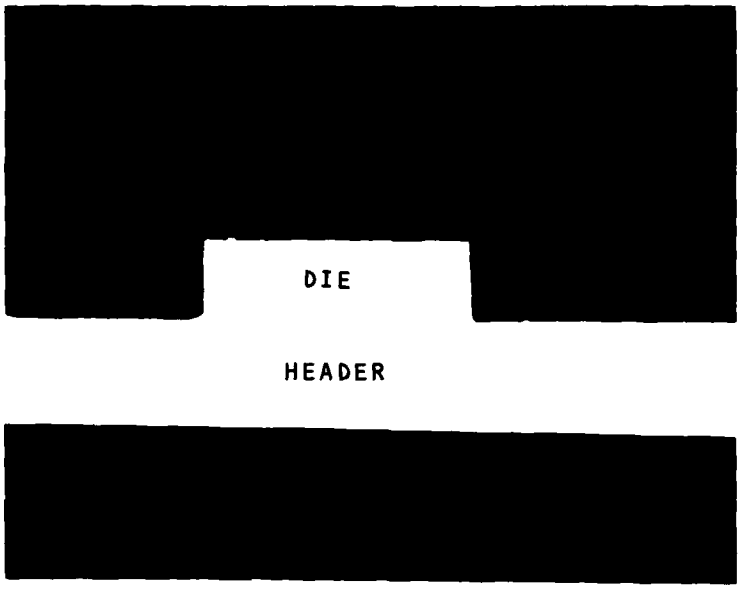


FIGURE 12b. HIGHER MAGNIFICATION CROSS SECTIONAL VIEW AFTER FINAL POLISH

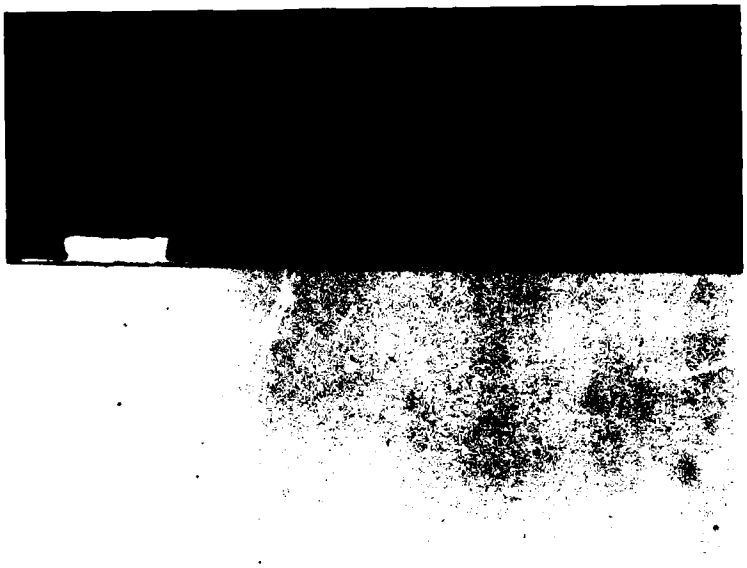


FIGURE 13a. THE "AS POLISHED" CROSS SECTIONAL VIEW SHOWING ALUMINUM METALLIZATION DETAILS ON THE MICROCIRCUIT SURFACE

FIGURE 13b. HIGHER MAGNIFICATION CROSS SECTIONAL VIEW SHOWING GREATER SURFACE DETAIL

A new instrument for cross sectioning, the "Minimet" (Buehler), has provisions for handling mounts singly through the full range of abrasives listed above. Moreover, cross contamination is minimized through the use of separate abrasive platens. The speed of oscillation of the mount to the platen and the pressure are fully adjustable. The grind or polish cycle may be timed at a constant pressure, or a gradually decreasing pressure may be set. A considerably finer degree of control may be exercised over the various stages of the section than is possible in hand-held methods.

f) Junction Delineation/Specimen Etching. The sample is now ready for staining. This operation will delineate diffusion areas (see the section in this chapter on junction staining for typical stains and procedures).

Figure 14a should be compared with Figure 12b to ascertain changes even in gross structure that a junction etch produced on the specimen. Figure 14b (an optical photo) of the etched specimen shows the diffusion tubs, isolations, emitter junctions, and N+ collector diffusions. The etch used is usually quite effective in removing smeared aluminum to show true structure. The etching/staining procedure will generally enhance/delineate any polishing damage and scratches on the sample.

Figure 15a is a SEM photomicrograph. At the lower 500 to 800 power magnification, the optical microscope often produces better images with more information, but as the required magnifications exceed 1200 to 1500 times, then the SEM comes into its own. Figure 15b should be compared to Figure 13b. In Figure 15b, the SiO_2 thickness can be easily discerned, slight thickness variations noted, and the contact interface between aluminum and silicon is easily examined. Of important note in the figure is the excellent adhesion of the epoxy to the aluminum stripe surface. On a good section, SEM examination is capable of providing dimensional information down to the 500 angstrom range.

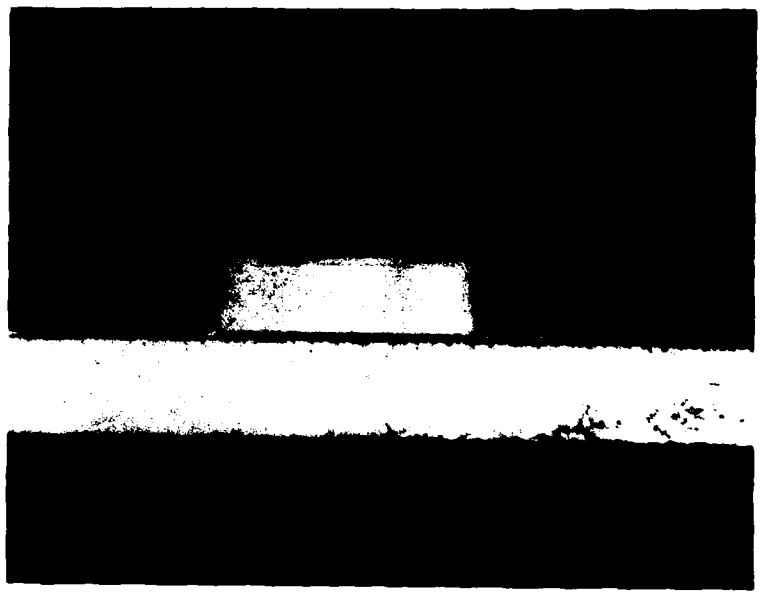


FIGURE 14a. CROSS SECTIONAL VIEW OF MICROCIRCUIT AFTER JUNCTION STAINING

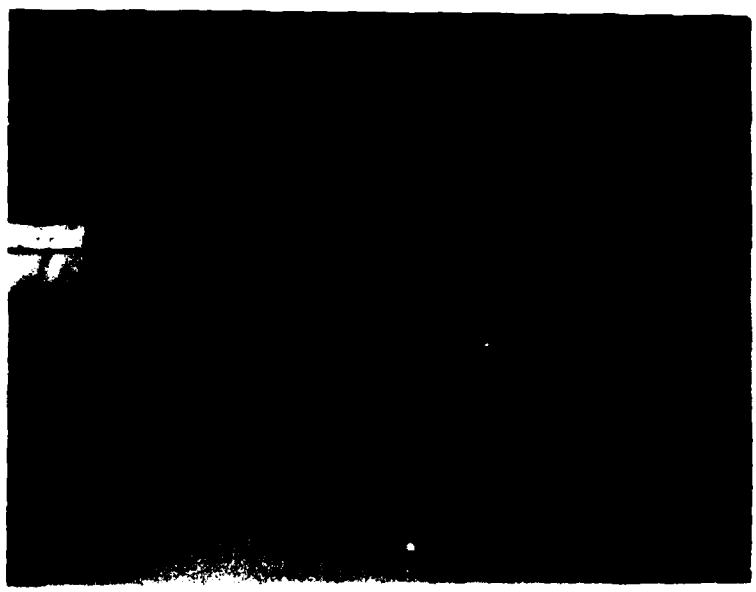


FIGURE 14b. HIGHER OPTICAL MAGNIFICATION SHOWING DIFFUSION AREAS

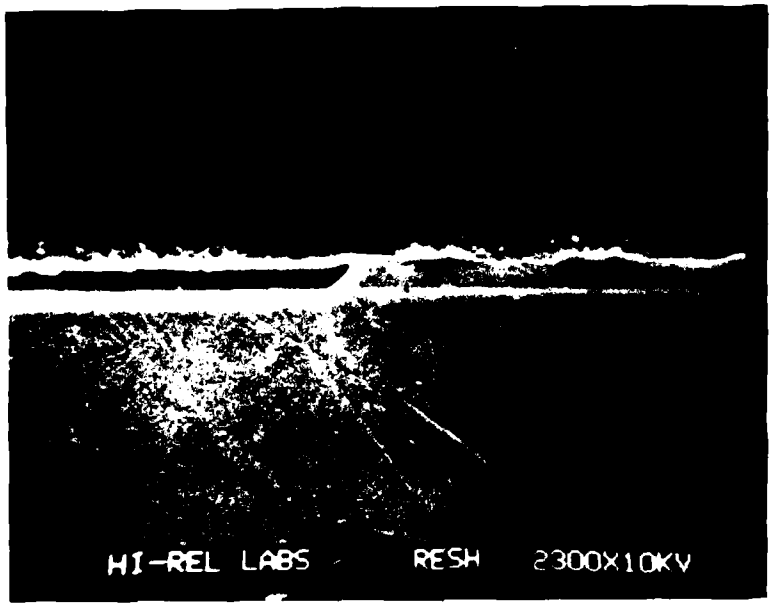


FIGURE 15a. SCANNING ELECTRON MICROSCOPE (SEM) PHOTOGRAPH SHOWING ALUMINUM CONTACT TO SILICON THROUGH THE BASE CONTACT WINDOW

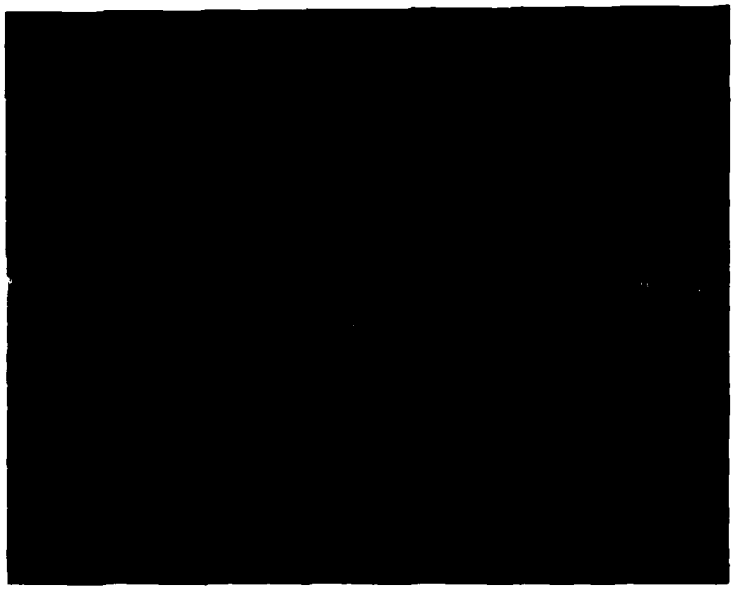


FIGURE 15b. HIGHER MAGNIFICATION IN WHICH OXIDE THICKNESS CAN BE SEEN AS WELL AS ALUMINUM - SILICON CONTACT AREA

3. Angle Sectioning. Angle sectioning as utilized in failure analysis involves mounting and lapping a die specimen at a shallow angle, generally 1° to 5°, for the purpose of revealing internal physical dimensions and defects, such as diffusion faults and electrical or electrostatic shorts. Measurements of internal structures in semiconductor devices are difficult to make in cross-section (90°) due to the very small dimensions involved. A typical diffusion depth in a silicon epitaxial layer is generally less than 10μ. Shallow diffusions approach 0.5μ in depth. Not only is the resolving power of light microscopy limited to ~0.25μ but conventional grinding/polishing techniques do not yield clean interfaces capable of resolving these dimensions.

Obviously, some method must be used to geometrically magnify these various layers in order to measure them. A beveled mount is used which has the desired angle machined into one half of the top surface where the specimen is mounted using Apiezon^{R} black wax. This mount is then secured in a cylindrical holder for the grinding/polishing operation. Figures 16-19 detail the tools that are used in the operation. This method will yield depth as a new dimension to the capabilities of failure analysis and provide information generally proprietary and not disclosed by the vendor.

a) Sample Preparation.

o Decap package to expose the chip (see Chapter III-E)

o Remove interconnecting wire leads between package/lead frame and the bonding pads on the chip using a pair of semiconductor grade tweezers.

o Remove passivation layer and surface metallization (see Chapter III-N). This step is optional. It will, however, aid in obtaining a scratch-free lapped surface. Individual

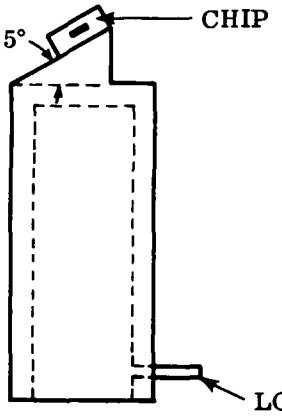


FIGURE 16.

BEVELING ROD - 1" ALUMINUM ROD WITH HOLE BORED THROUGH CENTER TO DECREASE WEIGHT

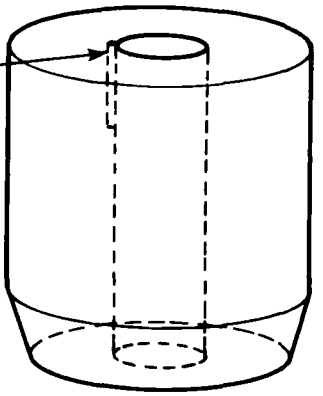


FIGURE 17.

BEVELING ROD HOLDER - USED FOR GRINDING WHEN USING SANDPAPER

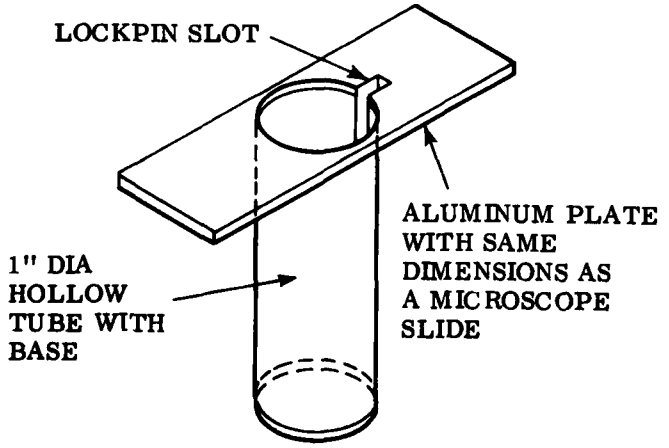
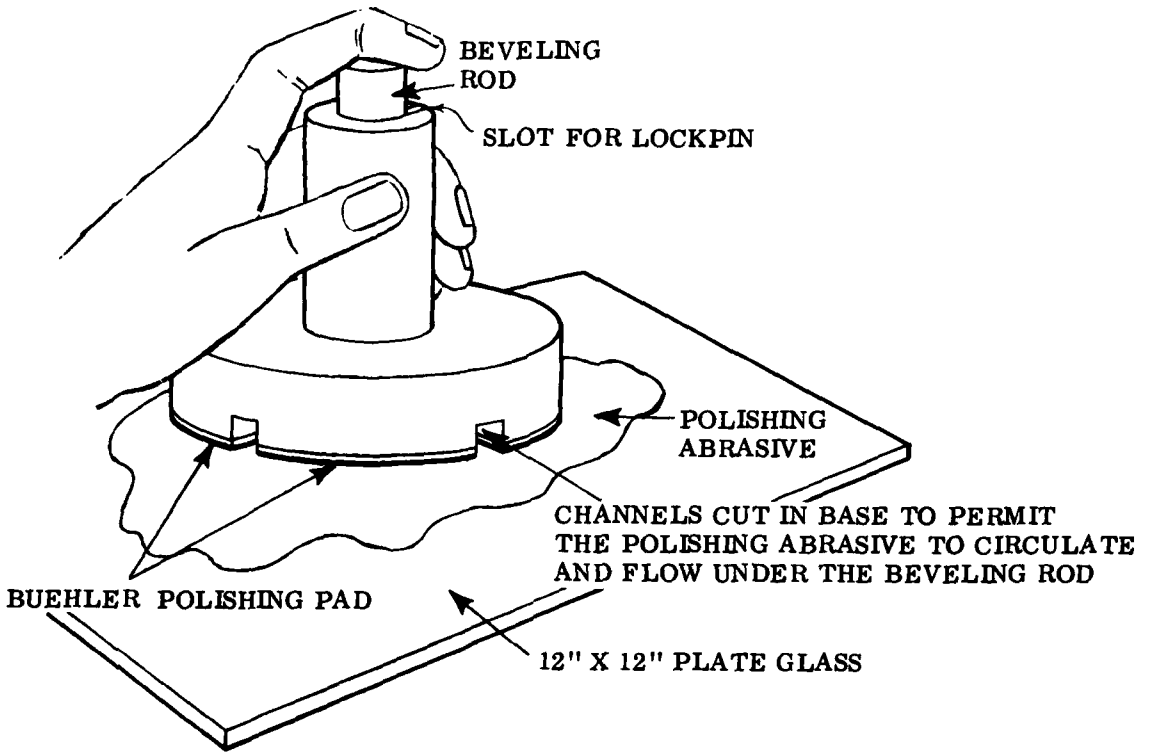


FIGURE 18.

MICROSCOPE HOLDER - BEVELING ROD IS INSERTED INTO AND SUPPORTED BY THIS HOLDER WHICH IS SUSPENDED BY THE MICROSCOPE PLATFORM. THE HOLDER PERMITS X AND Y VERNIER CONTROL OF THE CHIP.



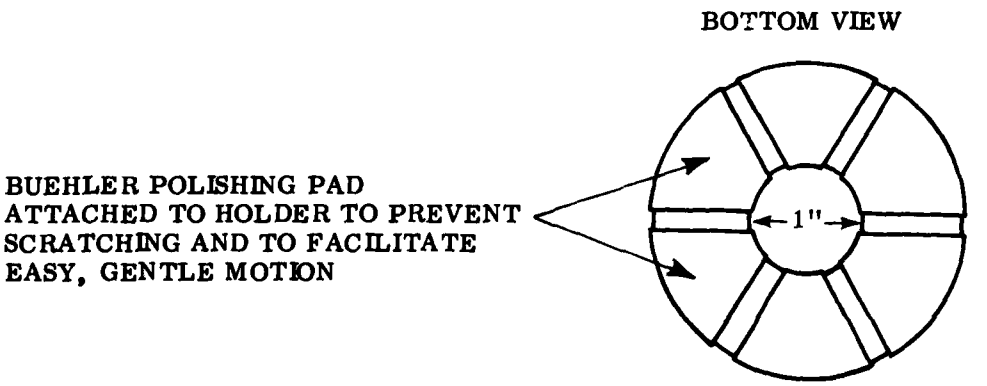
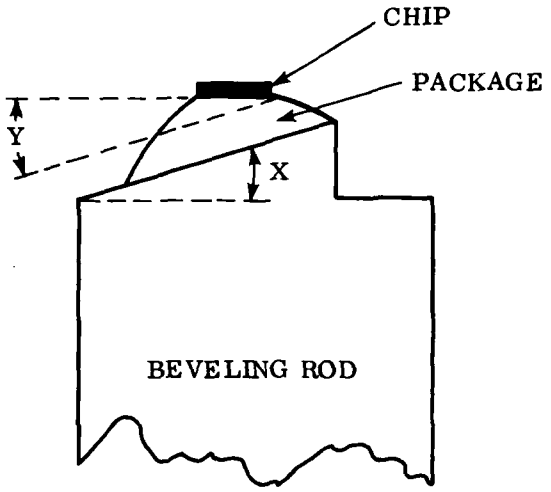
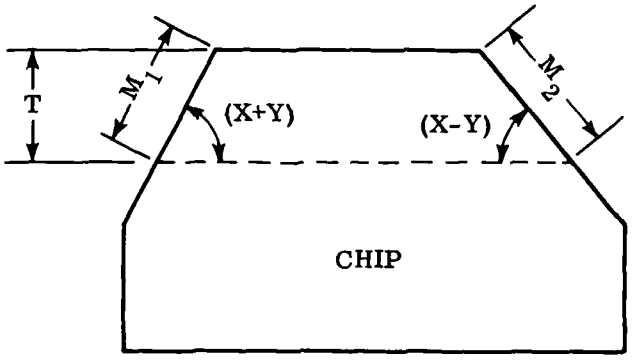


FIGURE 19a. BEVELING ROD HOLDER - MADE ACCURATELY TO ASSURE PERPENDICULARITY OF BEVELING ROD TO LAPPING SURFACE



X IS THE BEVELING ROD ANGLE

Y IS THE DEGREE TO WHICH THE CHIP IS NOT MOUNTED FLAT ON ITS HEADER



M_1 AND M_2 ARE THE TWO COMPARISON MEASUREMENTS WHICH ARE DEPENDENT UPON THE TWO ANGLE'S X, Y, AND THE DEPTH T

T IS THE DEPTH WHICH MUST BE ACCURATELY DETERMINED AND IN THIS CALCULATION IS USUALLY A MEASURE OF OXIDE THICKNESS

FIGURE 19b.

Diagrams for Junction Depth Measurement Technique Described in Appendix A

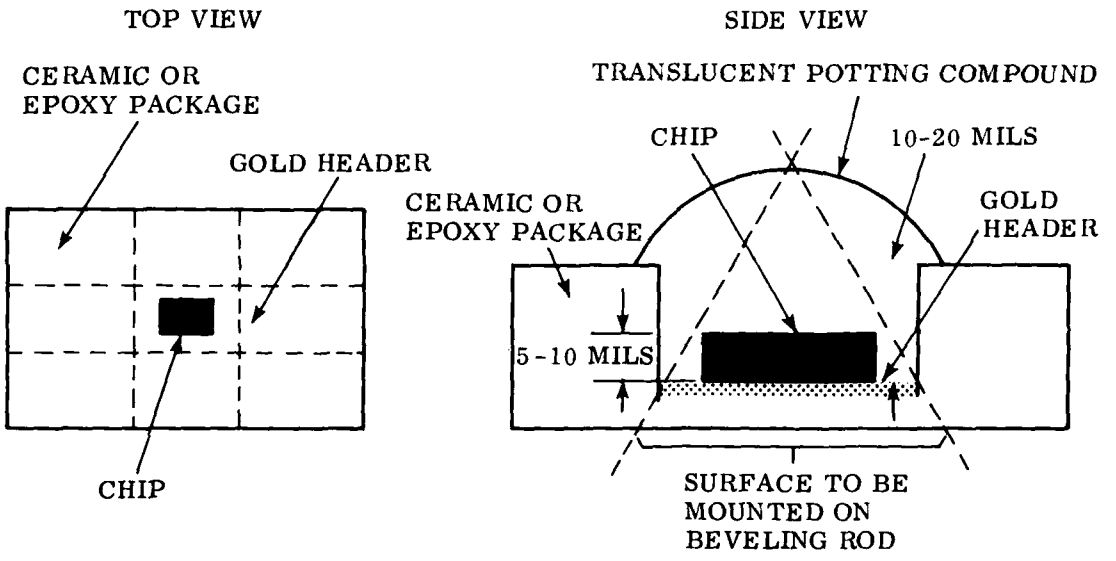
circumstances, however, may require that the metallization be left on because of a defect or region of interest near the surface or surface oxide passivation.

o Remove the case/IC frame: Most dies are mounted with a eutectic low-melting point solder. Gentle heating on a hot plate will usually facilitate die lift off from the case. For IC lead frames, using tweezers, apply a slight upward force on each lead. Only a slight force is required to separate leads from the ceramic or epoxy base material. An alternative method for both is to use a Dremel "Moto-Tool" and cut the package down with a cut-off wheel.

o Clean the package in an ultrasonic bath using a detergent cleaner, then a methanol rinse, followed by a gentle gas blast with dry nitrogen (30 PSI) or a freon dust-off can. Cleanliness is very important to achieve good surface bonding for the encapsulant.

o Encapsulate the chip with a transparent potting compound. The resin is placed directly over the chip but not allowed to flow over the ceramic or epoxy base. Its purpose is to protect the edges of the chip from breaking off and cracking during the angle lapping. It also serves to protect the chip surface from the harsh environment during the rough and fine grinding process. Vacuum debubbling is recommended to insure good bonding of the resin to the surface of the die. Heating gently (100°C) will hasten curing reaction.

o Grind away excess package material to enable an obstruction-free chip when angle lapping is performed. Grinding is absolutely necessary because of the hardness of the epoxy/ceramic package materials. Figures 20 and 21 illustrate a typical flatpak and relationship of chip and header to the potting material and parts of the package that must be removed. At this point, the 5°



(DASHED LINES SHOW WHERE THE PACKAGE IS CUT.)

FIGURE 20.

PACKAGE MATERIAL REMOVAL PATTERNS

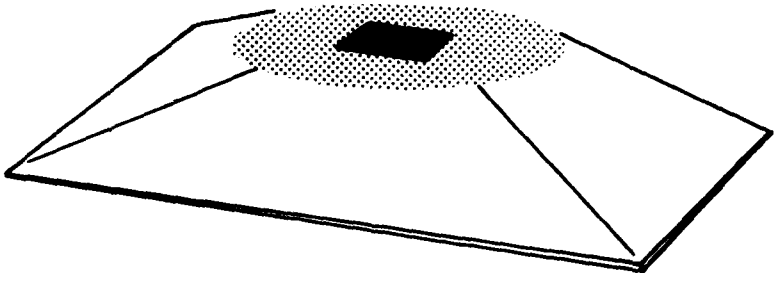


FIGURE 21.

PREPARED CHIP WITH ALL EXCESS PACKAGE MATERIAL REMOVED

beveling rod should be used together with a shim under the leading edge to support the package during the procedure. In this manner, the angle that the package is cut is greater than 5°. After the first cut, which is made perpendicular to one edge of the chip, the package is successively rotated 90° to remove all excess package material. Initially, a 240-grit silicon carbide wet proof paper is used. As the surface of the chip gets closer to the exposed grinding edge, a 320-400 grit paper is used. Package material is removed until the edge of the gold header is reached. If it appears further grinding will damage the chip surface, the package and shim should be moved and adjusted to increase the angle slightly. Under no condition should the surface or edge of the chip make contact with the grinding paper at this point.

o The package is supported in each of these grinding operations with a black wax (Apiezon W^{R}). This wax forms an air-water seal and bonds epoxy or ceramic and metal effectively. Melting point is from 80° - 90°C. It is insoluble in water, acetone, ether and alcohol but soluble in toluene and trichloroethane. It is hard at room temperature and comes in a molded cylindrical stick.

o The wax is applied by rubbing the stick on the heated angle rod, melting the wax. Use a hot-air blower or gas torch to heat the rod.

o When all excess package material has been removed, the surface of the prepared package is ready to be polished. Remove the package and shim from the rod with heat and clean off all the wax with trichloroethane. Thoroughly clean the package in an ultrasonic bath with methanol and insure the base of the package is flat and parallel with the surface of the die. If not, grind the base until it is smooth and flat and reclean in the ultrasonic bath. Cleaning and grinding guarantees that the lapped angle will be the same as the beveled rod angle, assuming that the chip was mounted flat in its package originally.

b) Sample Mounting.

o Ensure the beveling rod, holder and specimen are clean and free of all dirt and grinding particles (wash in DI water and blow with dry nitrogen - 30 PSI).

o Heat the beveling rod with a hot-air blower and continue the application of heat until completion of the mounting procedure.

o Apply a very small quantity of mounting wax to the beveling rod when hot.

o Smooth the wax to a thin even film with a micro spatula or similar tool.

o Mount the prepared package, using tweezers. Scrub the package into the wax. This ensures that the package and chip will be mounted flat and will result in the desired angle (assuming the chip is mounted flat in the package). Align the package so that the desired side of the chip to be beveled is on the high side of the beveling rod. Use the straight edge on the rod as a reference to obtain the desired angle and direction of bevel with respect to the chip surface plane.

c) Grinding.

o Place the beveling rod in the holder for grinding. Using 600-grit silicon carbide paper, grind into the chip until the leading edge of the beveled section is approximately 150-250 μm from the area of interest. Use only new-unused SiC paper. Be sure to use plenty of DI water to lubricate the grinding surface.

CAUTION

The beveling action is rapid. Check efforts after each stroke across the grinding paper to avoid destroying the chip or region of interest.

Make each stroke approximately two inches long. Grinding to the required area may take only four or five strokes.

o Thoroughly clean the beveling rod and device surface. Use a kimwipe moistened with DI water and a small quantity of 1.0 μm polishing alumina.

CAUTION

Never wipe an exposed chip or lapping surface with a dry kimwipe so as to avoid scratching the surface.

o This cleaning technique is necessary to remove any grit/particles embedded in the remaining encapsulating compound or exposed surfaces. It will also polish the surface, reestablishing the translucency, and enabling one to observe the chip surface.

d) Angle Lapping. The prepared device is now ready for rough (1.0 μm) and fine (0.3 μm) alumina polishing.

CAUTION

All of the following steps leading to completion of angle lapping are crucial in obtaining satisfactory results. Extreme care must be exercised to assure the cleanliness of the chip, package, rod, holder, and lapping surface. One mistake, one slip, or one foreign particle can destroy any evidence or area that was intended to be observed, rendering all previous efforts useless. In addition, one must be very gentle and exercise great care in handling and actual angle lapping to avoid destroying the area of interest.

o The angle lapping process requires extreme cleanliness. The specimen should be washed thoroughly after each lapping step and especially after structure delineation by chemical means to prevent contamination of the abrasive slurry and damage to microscope objectives used for observation and photomicrography. The lapping plate must be periodically rinsed and new abrasive added to remove specimen material particles which can cause scratching of the lapped surface. The lapping plate must also be pre-polished using the abrasive size intended for specimen lapping. Under no circumstances should a plate pre-polished with a specific grit size be used with a lapping abrasive larger or smaller in particle size. In the former case, the plate finish is obviously destroyed, whereas in the latter, the specimen will be damaged. Again cleanliness cannot be over emphasized.

o Any glass plate or other equal hardness material rigidly fastened can be used as a lapping surface. The dimensions of the plate should be 1' x 1' minimum for ease of lapping and to

avoid specimen damage due to accidental holding fixture motion over the plate edges. The plate should be inspected prior to pre-polishing for excessive scratches and/or high spots which cannot be removed with the intended grit size. Plate polishing is accomplished by using the mount holding collar only. Place the properly prepared abrasive slurry on the plate and slide the holding collar around the plate in a random pattern observing high spots and surface finish periodically until flatness and proper finish are achieved. In this manner, both the plate and holding collar bottom surface are polished uniformly. It should then be obvious that a separate plate and holding collar must be used for each grit size used.

o When cleanliness is assured, place a small quantity of 1.0 μm polishing alumina on the plate glass and dilute with approximately 20 cc DI water. Add a drop of liquid soap to lubricate the slurry.

NOTE: The 1.0 μm and 0.3 μm alpha alumina (aluminum-oxide) particles have a hexagonal crystal structure. They are very hard (9 on Moh scale) and fairly fast-cutting. Gamma alumina particles (0.05 μm) were found to be ineffective in cutting silicon. The particles have a cubic crystal structure and are somewhat softer (Moh 8).

o Thoroughly mix the slurry with the beveling rod holder before inserting the beveling rod.

NOTE: A Buehler polishing pad (Texmet^{R}) is attached to the beveling holder to facilitate easier motion on the lapping surface. *Optional - It is recommended that 6 micron diamond paste be rubbed into the polishing cloth before proceeding to the 1 micron alumina slurry. Only a small amount is used.

o Use extreme caution, gently sliding the beveling rod into the holder. This insertion will establish physical contact between the chip and the plate glass. Be certain the lock pin engages the alignment slot in the holder to prevent twisting.

CAUTION

If the beveling rod should accidentally strike the glass plate with even a slight downward force, it will crack or shatter the silicon chip. It might also nick or scratch the plate glass.

o Polish the silicon chip, using a gentle circular motion. Check the polishing efforts often (every few minutes). The polishing slurry should be discarded occasionally because it will pick up contaminating particles. As the water in the slurry begins to evaporate, add more DI water.

o When visual observation indicates that the leading edge of the beveled section is approximately 10-15 μm from the area of interest, polishing should proceed with the 0.3 μm alumina. When making this change, thoroughly clean the beveling rod and lapping plate. Replace the beveling rod holder and lapping plate. Polishing is then continued and is complete when the required area is reached.

o If a high degree of particles are observed on the lapped surface or the surface does not possess a mirror-like finish, final polishing may be performed on a Beuhler polishing pad instead of the glass plate, again using the 0.3 μm alumina.

o Thoroughly clean all equipment before proceeding to the staining/etching steps.

o After each series of laps, the specimen can be chemically treated to delineate internal structures. Prior to staining, wash the specimen thoroughly with distilled or deionized water followed by an isopropyl alcohol rinse and dry with a duster or dry nitrogen gas.

e) Staining. The purpose of staining is to identify the various zones of dopants in the semiconductor material. See the section in this chapter on junction staining for typical stains and procedures.

4. Junction Staining. In much of semiconductor failure analysis work, it becomes necessary to delineate the junctions on the polished silicon sample. The treatment procedure is to place an aqueous staining solution (commonly referred to as an etch or stain) in contact with the polished surface containing the junction. The solution functions by making silicon dioxide (SiO_2) soluble; in the presence of the solution, silicon monoxide, SiO, is relatively insoluble. The solution includes an oxidizing agent which stains by selectively forming over the silicon surface a layer of silicon monoxide.

The silicon monoxide forms mainly on the P-type material, giving it a darker appearance than the N-type material. This makes the demarcation between the two types of material clearly visible. It should be remembered that the P-N junction will appear as a contour. This is due to the fact that the higher concentration in P-type material will be more darkly colored. In some of the stains with higher total acid content, the N-type regions are more darkly colored the lower the concentration. Thus, it can be seen that concentration gradients show up as a difference in shading.

Evidence indicates that the staining process in the P-type material involves an electrochemical oxidation and reduction reaction which proceeds more quickly in P-type material because of its greater free energy of reaction. In this type reaction, the electrons given up by the P-type material must be balanced out by the flow of holes from the N-type material. Since this is in the high-resistance direction for the junction, surface leakage is the only path in which the current may flow. Also, surface leakage is enhanced by the mechanical polishing techniques previously described. This forms the basis for the most successful method of junction delineation.

Figure 22 shows a portion of a microcircuit that has been lapped and stained.

Table I lists a number of common silicon stains and the techniques employed in their use (see Chapter III-M for more details on chemicals and Chapter IV for details on safety in chemical handling).

NOTE: In general, the following rules regarding mixed stains should be followed:

- Do not store these solutions more than one month.
- Date each container and replace on a schedule based on thickness of the container wall.
- Put replacement date on each container.

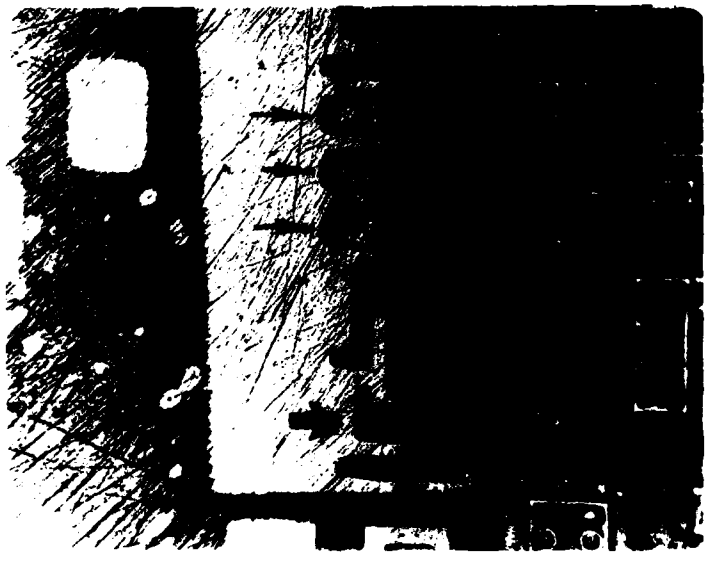


FIGURE 22. LAPPED AND STAINED MICROCIRCUIT

TABLE I

List of Junction Stains and Techniques

STAIN NO.	NAME	CHEMICAL COMPOSITION	TECHNIQUES
1	Dash Etch	3 parts by volume HNO_3 1 part by volume HF 12 parts by volume HAc (Acetic Acid)	A drop of the solution is applied to the sample, which is then exposed to a strong microscope light for a period of time varying from 1 to 20 seconds. Very heavily doped regions will become visible after several seconds, and as time progresses, the more lightly doped regions will appear. On epitaxial devices, usually the color of the heavily doped substrate will range from brown to blue after 10-to-15 seconds. This etch does not accentuate crystal flaws or defects due to polishing.
2	3-1 Stain	3 parts by volume HNO_3 1 part by volume HF 10 parts by volume HAc (Acetic Acid)	Within 4 to 5 seconds after a drop of the solution has been applied to the sample, the junctions will appear. Lightly doped regions can be brought out by using a light to speed up the reaction. Normally, this stain will, if used for an extended period of time, define all the junctions in a silicon wafer.
3	10-1 Stain	10 parts by volume HNO_3 1 part by volume HF 7 parts by volume HAc (Acetic Acid)	A drop of stain is placed on the sample and is immediately washed off as quickly as possible (within less than 1 second). This stain produces a fine line P-N junction but also greatly accentuates crystal damage or damages due to microsectioning.

TABLE I (CONT.)
List of Junction Stains and Techniques

STAIN NO.	NAME	CHEMICAL COMPOSITION	TECHNIQUES
4	20-1 Stain	20 parts by volume HNO_3 1 part by volume HF	This stain delineates the emitter, collector and vapor-grown junctions in silicon devices. For best results, a cotton swab saturated with the staining solution should be rubbed against the polished surface. Within 0.5 to 1 second after application of the stain, all junctions should appear. Because defects are emphasized by this stain, the prepared surface must be scratch free when viewed under 100X vertical illumination, if reproducible results are to be obtained. A semiconductor surface is attacked by the stain at a rate which is dependent upon impurity type and concentration, crystallographic orientation and residual stresses produced either by polishing or during the fabrication of the device. This solution will attack an N-type material at a faster rate than it will the corresponding P-type material. The emitter and collector junctions will appear as abrupt changes in the height of the surface. These steps are the junction positions and changes in the impurity gradient.
5	3-1 Stain With $CuSO_4$ Solution (See 5.a. below)	10 ml of Stain No.2 with 4 - 6 drops of solution 5.a. below.	This stain can be used in place of the 3-1 stain if the sample begins to show excessive staining burns (excessive material removal) before all of the junctions have been defined. Junction definition is enhanced by the deposition of metallic copper. Except for longer staining times, this stain is used in the same way as the standard 3-1 solution. (Stain No. 2)

TABLE I (CONT.)

List of Junction Stains and Techniques

STAIN NO.	NAME	CHEMICAL COMPOSITION	TECHNIQUES
5.a.	$CuSO_4$ Solution	10 ml of HF 200 g of $CuSO_4$ 1 liter of deionized water	Use with stain 5 above.
6	Safe-T-Stain	Propriety Mixture Philtec Inst. Co., Philadelphia, PA	This stain is noncorrosive to exposed skin. A drop of the solution is applied to the sample, and the sample is exposed to a light source. N+ areas are revealed with this stain. The length of time necessary to stain is a function of solution concentration and intensity of exposed light.
7	Fuller's Stain	99.5 - 99.9 parts by Volume HF 0.1 - 0.5 parts by Volume HNO_3	A drop of the solution is applied to the sample and then exposed to strong microscope light for a period of 20 - 30 seconds. This mixture stains highly doped P+ areas and moderately doped P areas after a longer period of time. These P areas are stained dark.
8	2-1 Stain	2 parts by Volume HF 1 part by Volume H_2O_2 17 parts by Volume DD Water	A drop of the solution is applied to the sample and then exposed to strong microscope light for at least 30 seconds. This mixture stains highly doped P+ and moderately doped P type areas dark.

5. Junction Depth and Other Subsurface Measurements. Several methods are available for measuring junction depth, epitaxial layer thickness, and other subsurface thicknesses.

a) Filar Eyepiece. Layer thickness can be measured in the following way:

- Angle section and stain the sample (see Section 3 of this chapter).
- Measure the stained area as demonstrated in Figure 23 with a filar eyepiece (see Chapter III-J).
- Calculate the desired layer thickness or depth by the formula:

$$d = L \sin \alpha$$

where: d = Layer thickness or depth
L = Measured distance
α = Angle at which lapping was done (usually 1° - 5°)

b) Interferometer. Measurements are made in the following way:

- Angle section and stain the sample (see Section 3 of this chapter).
- Illuminate with monochromatic light interferometer (for example, sodium or thallium light source).
- Count the number of fringes between the two boundaries of interest. Figure 24 demonstrates fringing.

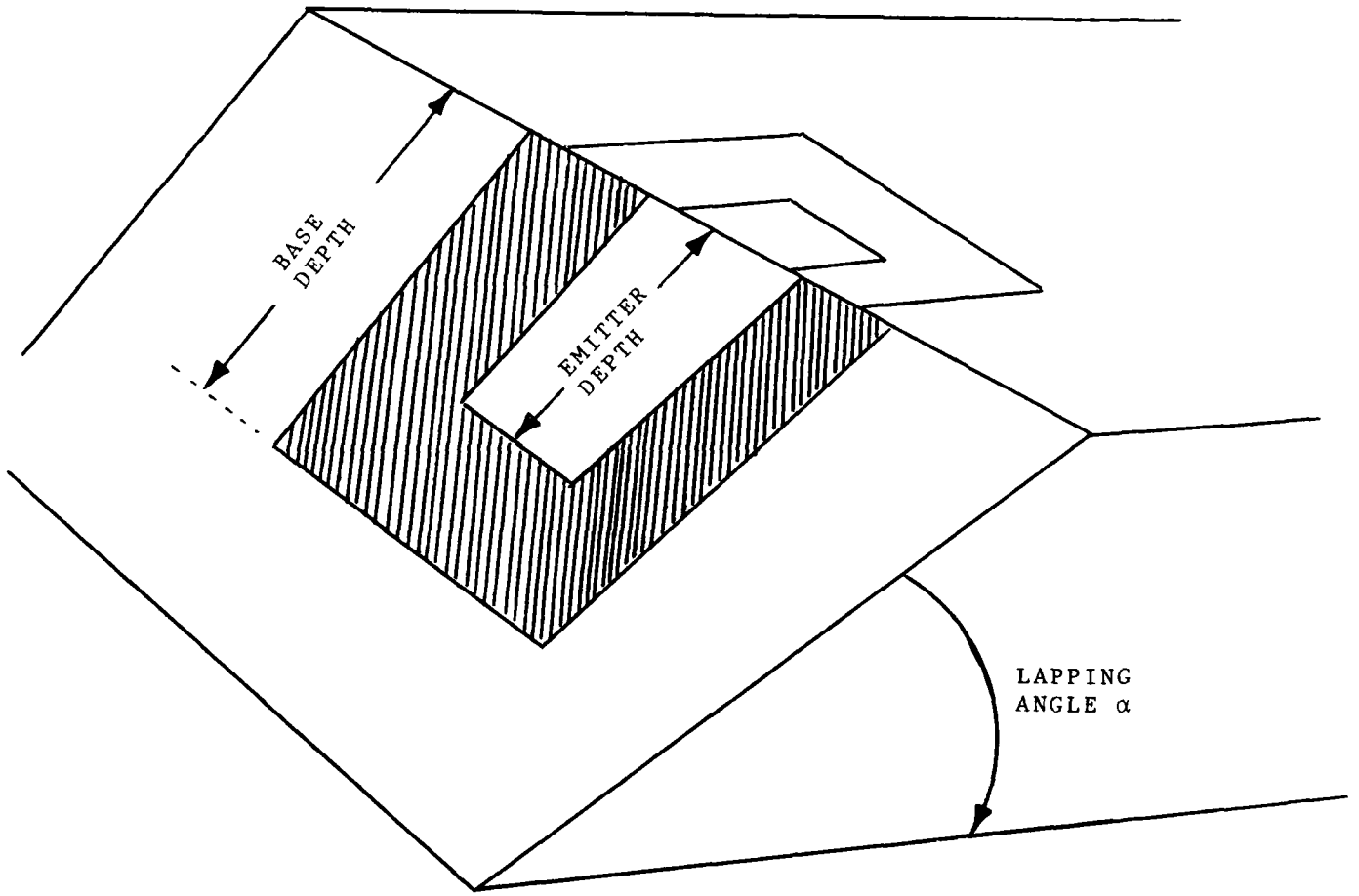


FIGURE 23. ANGLE SECTIONED AND STAINED BIPOLAR TRANSISTOR

o Calculate layer thickness by the formula:

$$d = N \frac{\lambda}{2}$$

where: d = Layer thickness or depth
N = Number of fringes
λ = Wavelength of monochromatic light

NOTE: In this method, the angle of lap does not effect the measurements, except in the sense that the shallower the angle, the easier the fringes are to count.

The sample may optionally be photographed to make fringe counting simpler.

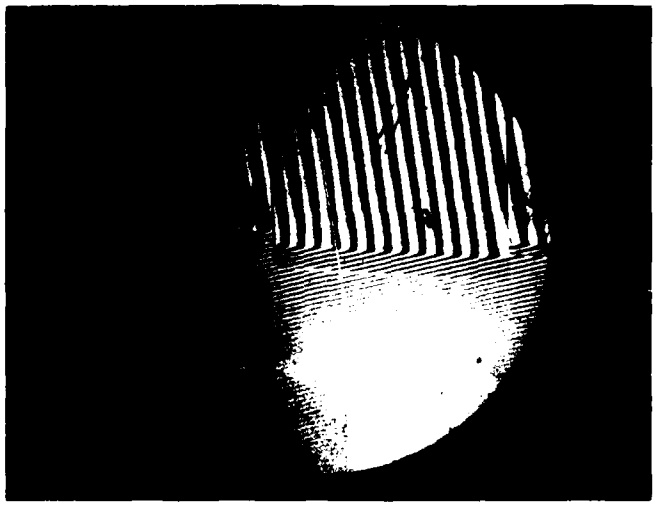


FIGURE 24. FRINGES PRODUCED BY MONOCHOMATIC LIGHT IN INTERFEROMETER, USED TO MEASURE BASE DIFFUSION DEPTH ON LAPPED AND STAINED MICROCIRCUIT

As an example, consider Figure 24. This figure demonstrates the technique of using interferometry to measure base diffusion depth on a microcircuit which has been lapped and stained. The sample was prepared by the steps listed below:

- Angle sectioned at 2° and stained with Stain No. 7 in Table I of section 4 of this chapter.
- Illuminated and photographed with thallium light source interferometer at 25X. λ = 0.54 µm.
- Draw a line parallel to the bottom of diffused area
- Draw a line parallel to one of the upper heavy fringes so that it intersects the other line drawn
- Count the fringes that cross the line parallel to the heavy fringes between the top and bottom surfaces of the delineated diffusion area, in this case 5 fringes

NOTE: If there should not be an even number of fringes, count whole fringes and add 1/2 more. It is possible to estimate more accurately than 1/2 fringe with higher magnification but is not normally recommended.

Calculate base depth:

$$d = 5 \times \frac{0.54\mu m}{2} = 1.35\ \mu m.$$

c) Grooving. This technique has little applicability in failure analysis because the failure analyst normally deals with individual semiconductor die, and the grooving equipment is intended more for wafer processing.

It is possible to expose junctions and subsurface layers more rapidly by groove methods than by hand angle sectioning. However, it is difficult to do so with a single die because of the small die size in relation to the large grinding wheel.

Groove apparatus employs a diamond impregnated rotating grinding surface lubricated by water. Apparatus options include choice of grinding wheel (cylindrical or spherical) and a series of grinding roughnesses. The sample is held rigidly against the grinding surface by a machine appliance.

The sample appears much as shown in Figure 22 after grinding and staining. This is true because of the very large radius of curvature of the grinding wheel in relation to the small microelectronic device size. Layer thicknesses are measured using the following steps:

- Grind and stain.
- Measurement of the layer thickness can be done in two ways
  - Measure the stained area from edge to edge with a filar eyepiece as in 5.a) above. Because of the slight curvature of the sample, a correction factor, supplied by the manufacturer, must be used in computing layer thickness.
  - Measure the stained area by interferometry as described in 5.b) above. Calculate thickness by the same equation.

$$d = N \frac{\lambda}{2}$$

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12. Platteter, D. "Basic Integrated Circuit Failure Analysis Techniques," Proceedings of the 14th Annual International Reliability Physics Symposium, 1978, pp. 248-255 (Reference for Appendix A).

13. Doyle, E.A. Jr., and G.G. Sweet. "Specimen Mounting and Metallurgical Angle Sectioning Technique for Microelectronic Devices," RADC Internal Document (Appendix B).

14. Doyle, E.A. Jr., and G.G. Sweet. "Specimen Mounting and Metallurgical Sectioning Techniques for Cross-Sectioning Microelectronic Devices," RADC Internal Document (Appendix C).

EQUIPMENT

1. Lapping surface (2) 12" x 12" plate glass — $10.00
   Available any hardware dealer.

2. Beveling rod(s), 1°-8° at 1° intervals (Figure 16).

3. Beveling rod holder for fine grinding (Figure 17).

4. Beveling rod holders (2) for fine polishing (Figure 19).

5. Microscope holder for holding beveling rod (Figure 18).
   Items 2 - 5 available at machine shops - prices will vary.

6. Apiezon Wax W 1 lb. packet (20-24 sticks) — $10.00
   James G. Biddle Co., Plymouth Meeting, PA (Minimum order)

7. Master Heat Gun - Cat. No. 3010 — $37.95
   Cole-Palmer Inst. Co., Chicago Ill. 60648

8. Potting Materials: Buehler, Evanston Ill.

   a) EPO-KWIK fast curve epoxy kit — $37.50
      Cat. No. 20-8128

   b) EPO-MIX (1 oz. packets) 2 part epoxide — $25/10 pk.
      Cat. No. 20-8133-001

   c) Epoxide (bulk)
      Resin - Cat. No. 20-8130-032 — $18/qt.
      Hardener - Cat. No. 20-8132-008 — $ 7.50/1/2 pt.

   d) TRANSOPTIC-Thermoplastic compression moulding power — $23/5 lbs.
      Cat. No. 20-3400-080

   e) RING FORMS - Phenolic mold form
      1" - Cat. No. 20-8151-010 — $ 2.75/10 pcs.
      1 1/4" - Cat No. 20-8152-010 — $ 3.50/10 pcs.
      1 1/2" - Cat. No. 20-8153-010 — $ 4.25/10 pcs.

   f) SAMPL-KLIP - Specimen support spring
      Cat. No. 20-4000-100 — $15/100 pcs.

   g) SAMPL-KUP - Reuseable plastic mold 1 1/4"
      Cat. No. 20-8180 — $11/12 pcs.

   h) Release Agent - for mold forms
      Cat. No. 20-8185-008 — $ 6.50/1/2 pt.

EQUIPMENT (CONT.)

9. GRINDING PAPER DISCS: Buehler, Evanston, Ill.

   a) CARBIMET - 8" Plain Back, 240 grit
      Cat. No. 30-5108-240-100 — $45/100 pcs.

   b) CARBIMET - 8" Plain Back, 400 grit
      Cat. No. 30-5122-400-100 — $45/100 pcs.

   c) CARBIMET - 8" Plain Back, 600 grit
      Cat. No. 30-5122-600-100 — $45/100 pcs.

10. POLISHING POWDERS: Buehler, Evanston, Ill.

   a) MICROPOLISH C - 1.0 micron Alpha
      Aluminum Oxide (Al_2O_3) Alumina
      Cat. No. 40-6310-016 — $32/1 lb.

   b) MICROPOLISH A - 0.3 micron Alpha
      Aluminum Oxide (Al_2O_3) Alumina
      Cat. No. 40-6305-016 — $32/1 lb.

   c) *Optional
      MICROPOLISH B - 0.05 micron Gamma
      Aluminum Oxide (Al_2O_3) Alumina
      Cat. No. 40-6301-016 — $32/1 lb.

11. METADI DIAMOND COMPOUND: Buehler, Evanston, Ill.
    6 micron paste
    Cat. No. 40-6172 — $40/5 grams

12. POLISHING CLOTHS: Buehler, Evanston, Ill.

   a) MICROCLOTH - Plain Back, 7"
      Cat. No. 40-7206 — $8.50/10 pkg.

   b) TEXMET - PSA back, 6"
      Cat. No. 40-7616 — $11.50/10 pkg.

13. Microscopes and illuminators - (see Chapter III-M)

14. Tissue, soft, lint free

   a) Kay-Pees — $1.38/box
      Sorg Paper Co., Middletown, Ohio

   b) Kimwipes - large size — $1.24/box
      Stock No. 34255
      Kimberly-Clark

EQUIPMENT (CONT.)

15. General Laboratory Supplies (Prices on request)

    a) Fisher Scientific Co., Pittsburgh, PA

    b) Cole-Palmer, Chicago, Ill.

16. Interferometry Equipment, filar eyepiece
    (see Chapter III-M)

17. GROOVE APPARATUS
    Signatone Corp., Santa Clara, CA — $2,000

18. DREMEL MOTO-TOOL KIT — $60
    Model No. 280
    Mill Factor Products Co.
    318 W. Pleasantview Ave.
    Hackensack, NJ 07601

APPENDIX A

JUNCTION DEPTH MEASUREMENT TECHNIQUE

ANGLE LAPPING

Junctions depths can be calculated using a standard optical microscope and the following procedure. Each measured distance must be multiplied by the sine of the lapping angle used. The accuracy of these measurements is dependent upon the die being mounted parallel to the lapping block. Figure 19b (p.III-N-28) illustrates the general case where the die is incorrectly mounted in its package. To compensate for this inaccuracy, an alternate technique is used. The package must be turned 180^{o} and beveled far enough to get a comparison of at least one measurement.

The two measurements, m_1 and m_2, depend on the angles X and Y, and on the junction depth T.

$$m_1 = T \csc (X + Y)$$

$$m_2 = T \csc (X - Y)$$

Eliminating the error angle, Y, from these equations gives the exact junction depth as

$$T = \frac{2\, m_1\, m_2 \cos X \sin Y}{\sqrt{(m_2 - m_1)^2 \sin^2 X + (m_1 + m_2)^2 \cos^2 X}} \qquad (1.1)$$

Since the angles X and Y are usually small, a useful approximation is found by expanding the trigonometric functions and retaining only terms of lowest order in X, yielding[6]

$$T \cong \tfrac{1}{2}\, r\, (m_1 + m_2) \sin X \qquad (1.2)$$

$$\text{where } r = 1 - \left[\frac{m_1 - m_2}{m_1 + m_2}\right]^2$$

Equation 1.2 introduces less than 1 percent error for lapping angles below 14 degrees. Because all depths cannot be compared by lapping from both sides of the die, these measurements are corrected by multiplying by the ratio T/m.

APPENDIX B

Specimen Mounting and Metallurgical Angle Sectioning Technique
for Microelectronic Devices

INTRODUCTION

Angle sectioning is employed routinely in establishing semiconductor device diffusion time/temperature schedules using control samples, device reliability characterization (physical analysis) and failure analysis. Like cross-sectioning, it is also a two step process involving mounting and subsequent lapping of a specimen at a desired angle, generally 1^{o} to 5^{c}, using fine alumina abrasives for the purpose of facilitating internal device physical measurements. Typical structures analyzed include diffusion depths, buried layer geometry, epitaxial layer and oxide thicknesses, nominal metal thickness, qualitative surface topography, dopant conductivity type (chemical staining-etching required), junction boundaries and profiles and other bulk structural anomalies. A beveled mount is used which has the desired angle machined into one half of the top surface where the specimen is attached using hot Apiezon wax (black). This beveled mount is then secured on a cylindrical slug and placed in a holding collar which maintains a constant specimen orientation with respect to the flat glass plate surface on which an abrasive slurry is placed for sequential lapping.

GEOMETRICAL MAGNIFICATION PROPERTIES OF ANGLE SECTIONING

Measurements of internal structures in semiconductor devices are difficult to make in cross-section (90^{o}) due to the dimensions involved. In today's microcircuit technology, a typical Si epitaxial layer into hich transistor, diode and resistor structures are fabricated is generally less than 10μ. Shallow diffusions approach 0.5μ in depth. Coupled with the fact that the resolution limit in light microscopy is on the order of 0.25μ it is obvious that a method for magnifying such structures for measurement purposes is required. In addition, since interferometer techniques are used for precision linear measurements and

require a plane tapered (sloped) surface for interference fringe generation, angle sectioning provides a means of specimen preparation amienable to direct measurement. This assumes that a suitable technique for delineating bulk structures for optical observation is employed prior to measurement. Angle sectioning can impart an apparent geometrical magnification to internal structures of any cross-sectional geometry by cutting through a vertical structure in a plane at some predetermined angle with respect to the vertical plane. This in effect is a mechanical method for elongating linear displacements proportional to the secant (sec) of the angle with respect to the vertical plane or the cosecant (cosec) with respect to the horizontal plane. Since the mount is beveled at a designated angle with respect to the horizontal plane the degree of apparent magnification can be calculated using the formula (1) which gives values of 11.5X and 57.3X for 5° and 1° respectively. The upper mechanical magnification, obtainable with reasonable repeatability and useable for maintaining a point of reference through a small geometry structure, corresponds to an angle on the order of $\sim 1^{\circ}$. At angles $< 1^{\circ}$, the lap will rapidly remove the material where the structures' geometry intersects the surface with resultant loss of reference plane for depth measurement. Also, since in mounting the specimen the actual final mounting angle depends on the quantity and uniformity of wax under the specimen, machining the mount with a bevel $< 1^{\circ}$ becomes impractical. At angles $> 5^{\circ}$ the amount of apparent magnification is not sufficient to allow accurate depth measurements using interferometry techniques and, in general, the rate of lap through the structure laterally can be time consuming using 0.3μ alumina abrasives.

STRUCTURAL DELINEATION AND MEASUREMENT

During the lapping sequence, various chemical delineation techniques including preferential acid etching and metal plating can be employed for

staining the angle lapped protion of the silicon to identify regions and/or boundaries of different conductivity and doping concentration or determine the position and depth of anomalies with respect to known internal or surface structures. Measurements of thickness/depth of internal regions or anomalies can then be made utilizing interferometry techniques. Instruments commonly used for such linear measurements include dual (non-contacting) and multiple (cont acting) beam interferometers or a metallurgical microscope equipped with a monochromatic filter and interference objective (dual-beam type).

CLEANLINESS REQUIREMENTS

The angle sectioning process requires extreme cleanliness. The specimen should be washed thoroughly after each lapping step and especially after structure delineation by chemical means to prevent contamination of the abrasive slurry and damage to microscope objectives used for observation and photomicrography. The lapping plate must be periodically rinsed and new abrasive added to remove specimen material particles which can cause scratching of the lapped surface. The lapping plate must also be pre-polished using the abrasive size intended for specimen lapping. Under no circumstances should a plate, pre-polished with a specific grit size, be used with a lapping abrasive larger or smaller in particle size. In the former case, the plate finish is obviously destroyed, whereas in the latter, the specimen will be damaged. Again cleanliness cannot be over emphasized.

LAPPING PLATE SURFACE PREPARATION

Any glass plate or other equal hardness material rigidly fastened can be used as a lapping surface. The dimensions of the plate should be 1' x 1' minimum for ease of lapping and to avoid specimen damage due to accidental holding fixture motion over the plate edges. The plate should be inspected

prior to pre-polishing for excessive scratches and/or high spots which cannot be removed with the intended grit size. Plate polishing is accomplished by using the mount holding collar only. Place the properly prepared abrasive slurry on the plate and slide the holding collar around the plate in a random pattern observing high spots and surface finish periodically until flatness and proper finish are achieved. In this manner, both the plate and holding collar bottom surface are polished uniformly. It should then be obvious that a separate plate and holding collar must be used for each grit size used.

MATERIALS

A. Apiezon Wax

Apiezon wax is used as the specimen bonding media since it is not soluble in acids or alkalies used for chemical delineation of specimen structures but readily dissolved with Toluene for removal purposes. Wax on the specimen surface may be helpful or harmful depending on the structures analyzed. Wax smeared over the lapped portion of the specimen during lapping results in improper chemical staining. Conversely, it forms a stronger wax-specimen-mount bond and protects specimen surface materials such as metals and oxides from unwanted etching during chemical staining of the lapped region. Removal of a thin wax layer on the specimen surface or lapped area can be accomplished using toluene by two methods. First, toluene can be applied with a dropper on the surface and immediately blown off using Freon or Nitrogen gas. This procedure is repeated until adequate cleanliness is obtained but not extended such that apiezon wax providing edge protection is removed. Secondly, a camel's hair brush soaked in toluene can be used to lightly brush the surface for dissolving the wax followed by gas blow drying. In either method it is difficult to completely remove all traces of wax, however, the translucency

of the unlapped surface can be made satisfactory and subsequent lapping should remove all traces on the lapped portion.

B. Al_2O_3 Abrasives

The abrasive commonly used for angle sectioning semiconductor materials, in particular Si microcircuits, is alumina (Al_2O_3). There are various commercial alumina powders available for metallurgical sectioning. Dry powders, powders in distilled water suspension and powders in special liquid suspensions producing an indefinitely suspended abrasive are available in a range of average particles sizes from Buehler Ltd. Average particle size is emphasized since some manufacturer's grading methods do not guarantee size uniformity, e.g. time controlled sedimentation separation, i.e., particle fall through a viscous fluid. As a result, these powders contain some large particles which cause deep scratches during lapping. Superior abrasives (alumina) exist which are graded for average particle size but with optical, SEM and/or TEM microscopy control of size distribution thereby eliminating scratch producing large particles. Past experience in evaluating optimum particle size for lapping Si material demonstrated that 0.3μ alumina yields a suitable smooth matte finish at an acceptable lap rate producing good chemical staining contrast when delineating internal structures. The matte finish results from abrasive rolling action rather than fixed (imbedded) particle grinding action. The use of larger particle size alumina results in a rougher finish and loss of boundary resolution optically and difficulty in interference fringe counting for displacement measurements. Smaller particle sizes produce a smoother finish but with reduced light scattering properties which inhibit the optical delineation of structures by conventional chemical methods. Surface wetting problems may also be involved with highly polished surfaces. Thus 0.3μ alumina, such as Buehler Ltd. No. 40-6352 AB Alpha No. 2, No. 40-6352-006 Alpha No. 2 Linde A or Micropolish Linde A,

are acceptable alumina abrasives for lapping Si. The Micropolish Linde A is the superior particle size distribution controlled alumina. The recommended distilled or deionized water to alumina powder volume ratio for lapping is approximately 10:1. When using water suspended alumina as supplied by Buehler Ltd., the solution is also diluted 10:1 prior to application. The final lapping solution should contain ∿1% by volume concentrated liquid soap for lubrication purposes. Thus, in a 500ml dispenser 5cc of soap provides proper lubrication and the resultant quantity of abrasive solution is sufficient for several weeks usage.

SPECIMEN MOUNTING

Place the beveled mount in the retainer on a hot plate and apply heat. The hot plate retainer provides a small mass holder for rapidly attaining the required wax melting temperature. Melt a small amount of Apiezon Wax (usable viscosity at ∿150°C) centered near the flat-beveled line on the angled surface of the mount. Remove the mount from the hot plate retainer with tongs and place in the aluminum slug holder. This slug is used to obtain a mount cool down rate compatible with the viscosity change of the wax (ΔT:fluid-solid) with decreasing temperature. It is also used as a mount media for the specimen during microscopic analysis due to the smaller axial length which is compatible with maximum microscope stage to objective distance. Place the specimen face up in the melted wax near the bevel line using Teflon tweezers or a small vacuum pickup, position under a stereo microscope for final orientation and carefully push the specimen down into the wax with a soft pointed tool (sharpened 1/8" Teflon rod or wooden Q-tip stick). The last step affects the resultant lap angle; i.e., maintaining the specimen bottom parallel to and flat on the beveled surface insures lap angle equal to bevel angle. Because of specimen thickness it is necessary to position the specimen offset slightly from the

bevel line (edge). This way the specimen top edge, which bears the beveled mount and slug weight during lapping, is less susceptible to breakage resulting from overhang (cantilevered chip). It is preferable to initially position the specimen back from the bevel line and slide forward to the final alignment even if remelting the wax is necessary. The specimen is generally mounted with an edge parallel to the bevel line. While the wax viscosity is still usable, wax should be pushed into the sides of the specimen using the pointed tool to provide maximum edge protection. Allow the mount to cool thoroughly before specimen lapping. After initial wax set, the mount cooling can be accelerated by running tap water on the steel mount surfaces. If minor reorientation is necessary, the wax can be remelted as before with the specimen in place, however, care should be taken not to overheat the wax such that its viscosity allows the specimen to slide excessively.

After the specimen is mounted properly, screw the mount into the threaded hole in the slug until finger tight.

LAPPING PROCEDURE:

Prior to lapping, the glass lapping plate surface must be rinsed thoroughly with distilled or deionized water and scrubbed with a clean lab brush. Shake the alumina abrasive solution to insure uniform abrasive particle mixture and apply a small amount on the appropriate glass lapping plate. Abrasive solution agitation is not necessary when using the abrasives with special suspensions for constant particle distribution. Rinse the holding collar with distilled/deionized water and place it face down on the plate in the abrasive slurry. Prior to specimen insertion and without exerting pressure on the holding collar, slide the collar around the plate in a random pattern (figure eight pattern is acceptable) until uniform distribution of abrasive is achieved and the collar slides freely without sticking. Spread additional abrasive solution on the

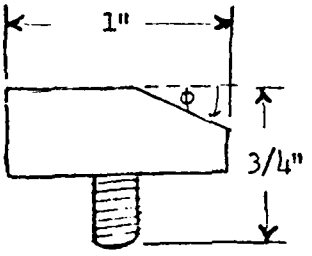
plate as required.

Leave the holding collar on the plate, spray water on the internal cylindrical surface and carefully insert the specimen mount and slug assembly into the holding collar using the recessed finger inset. The fingers should be dry to assure proper grip and to avoid accidental dropping of the assembly into the collar. If dropped, the specimen will strike the plate with sufficient force to destroy it. The close tolerance machining of the specimen mount and slug assembly to the holding collar results in a snug fit, thus prelubricating the holding collar with water minimizes the chance of binding and accidental droppage. Never force these parts into each other as the finely ground surfaces can be damaged beyond repair. Continuing, without exerting external pressure on the mated assembly, carefully slide the entire fixture in a slow random pattern (figure eight). The specimen should be checked for proper lap rate and orientation after traversing not more than three(3) figure eight patterns. This critical monitoring step can prevent specimen loss. If the angle is $< 1^{\circ}$, the specimen surface can be completely removed with only several laps. This check indicates whether the Apiezon wax mounting resulted in the proper angle with the desired specimen orientation. If improper specimen mounting is apparent, the mount must be reheated and the specimen repositioned using the previously described mounting procedure. If the rate of lap and orientation is acceptable, continue lapping adding water and/or abrasive solution as required until the region of interest is reached. After each successive lapping sequence, the specimen should be thoroughly cleaned with water and brushing. The lapping plate should be cleaned periodically with distilled/deionized water as dictated by excessive specimen scratching. After each series of laps, the specimen can be chemically treated to delineate internal structures. Prior to staining wash the specimen thoroughly with distilled or deionized water followed by an isopropyl alcohol rinse and

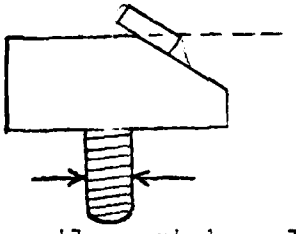
dry with an Effa Duster (Freon gas) or dry nitrogen gas. If necessary, DMSO (Dimethyl Sulfoxide), a superior organic solvent, can be used for specimen cleaning followed by the above cleaning and drying procedure. Care should be taken not to get DMSO in contact with body tissue since it is suspected to be carcinogenic in nature and is readily absorbed into the blood upon contact. Gloves (plastic) should be worn when using DMSO as a safety measure.

In general, specimens can be remounted in different orientations if necessary and relapped if the physical dimensions limit the lap laterally. Again cleanliness in angle sectioning cannot be overemphasized.

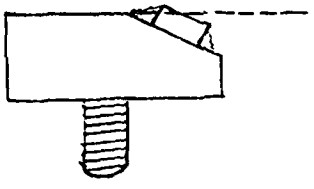
ANGLE SECTIONING



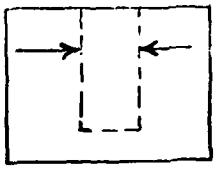
Beveled Polishing Mount



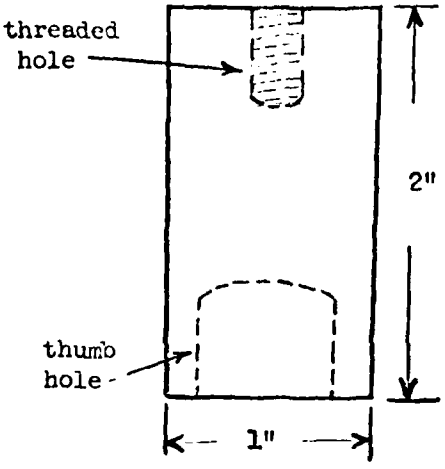
Incorrectly mounted sample



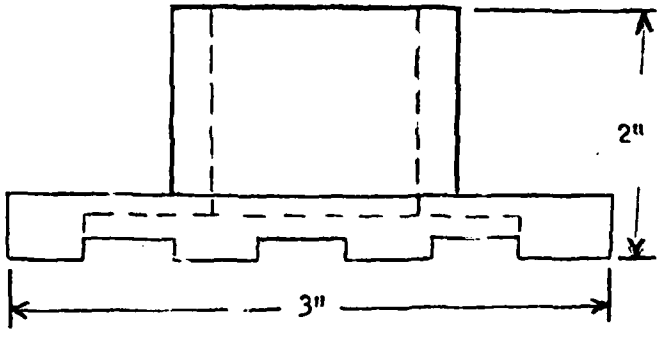
Correct position for sample secured to the Beveled Polishing Mount.



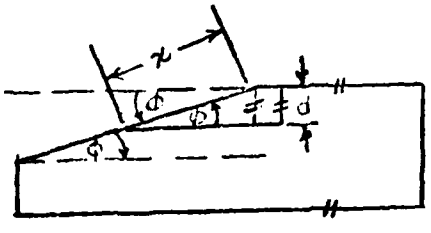
Aluminum Holding Fixture



Recessed Slug Design



Holding Collar Design



$\sin\phi = \frac{d}{x}$ where d = Actual Physical Depth
x = Viewed Image Normal to Lap Region

$x = d / \sin\phi = d \operatorname{cosec}\phi$

Geometrical Magnification of Chemically Stained Region at Lap Angle ϕ

$M = x / d = \operatorname{cosec}\phi$

$M\big|_{1^\circ} = 57.299 \qquad M\big|_{5^\circ} = 11.474 \qquad M\big|_{10^\circ} = 5.75$

APPENDIX C

Specimen Mounting And Metallurgical Sectioning Techniques For Cross-Sectioning Microelectronic Devices

INTRODUCTION

Cross-sectioning of microelectronic structures is a two step process consisting of specimen mounting in a suitable material and subsequent sectioning with abrasive materials. Two basic types of mounting material are used depending on device structure to be observed in cross-section. Polyvinyl Chloride (PVC) $(-H_2CCHCl-)_n$, a synthetic thermo-plastic resin compound, is used when the sample can withstand the required temperatures and pressures for mount thermo-setting under applied pressure. For deformable device structures several room temperature setting epoxys within "Bakelite" ring forms are used. Subsequent sectioning of the sample contained within the cylindrical mount is accomplished using graded abrasive materials. Several steps are involved including (1) rough grinding into the mount circumference to establish the proper angle and remove excess mounting media, (2) fine grinding with graded silicon carbide (SiC) papers to the approximate region of interest and (3) polishing using diamond pastes or graded aluminum oxide (Al_2O_3) or cerium (Ceric) oxide (CeO_2) abrasives. This procedure results in a highly polished surface which allows microscopic observation of the intrinsic microstructure. Sequential sectioning of the sample is also possible using steps 2 and 3 of the above procedure, and microstructure delineated when necessary by chemical etching.

PVC MOUNTING PROCEDURE (1½" and 1" ID MOLD)

Because the three mold parts are machined to tight tolerances for close fit, each must be thoroughly clean (soft cloth only) and dry and care should be taken to avoid dropping these parts. Before starting be sure that the 2½ inch long plunger will pass completely through the mold. Mold release

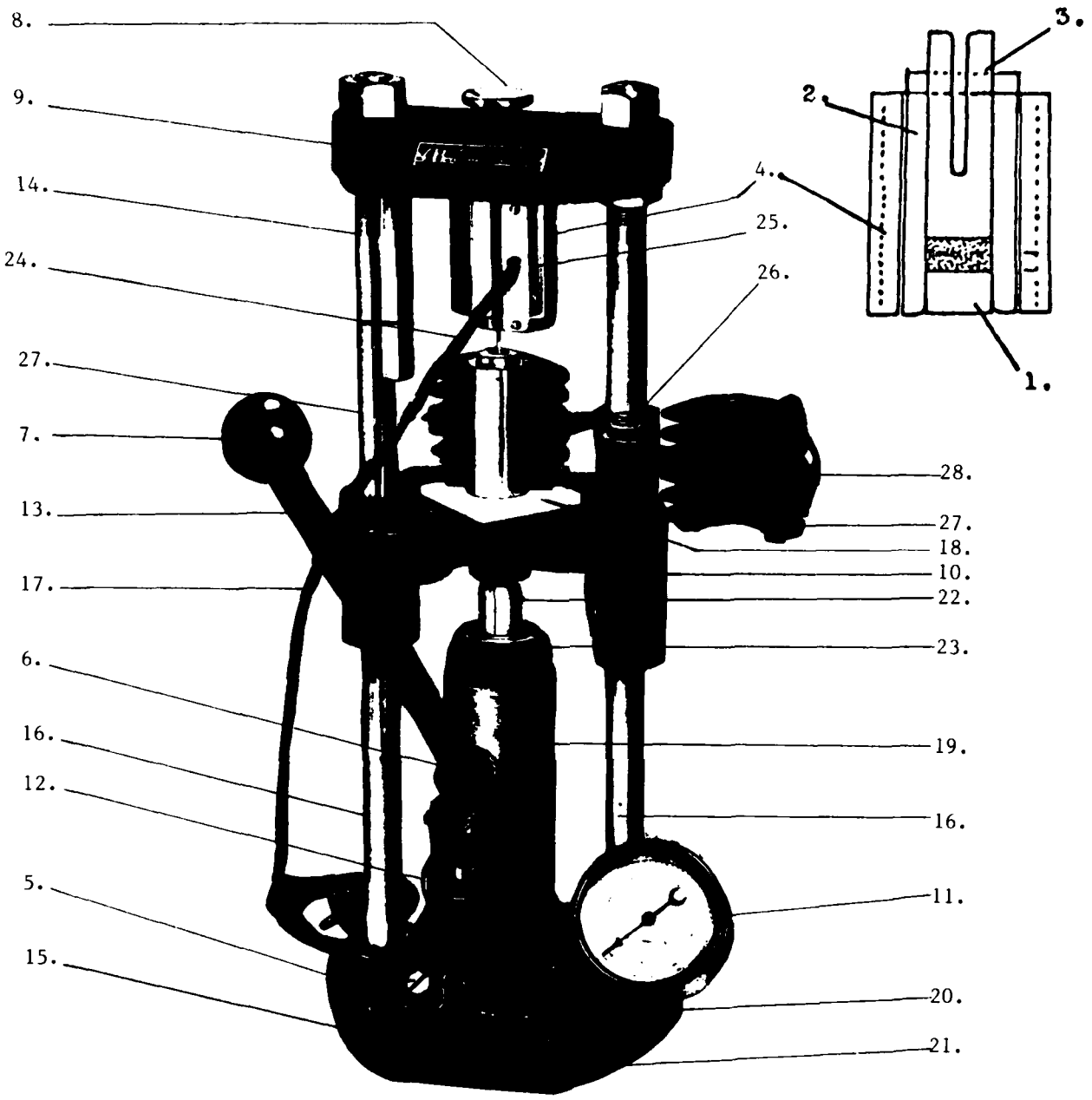
(lubricant) can be used on the interior mold surfaces to facilitate removal of the PVC after cure, however it is not essential.

Insert the 3/4 inch thick, 1¼ inch diameter base plug into the 1¼ inch (inner diameter) mold, until it is flush with the bottom of the mold, being sure that the dull side of the base plug is facing down. Fill the mold to 3/4 inch below the top with PVC powder. Place the specimen centered and horizontal on the leveled surface of the PVC and then pour in additional PVC to a level 1/8 inch below the mold top. Insert the 2½ inch long plunger in the top of the mold taking care to align the plunger with the molding bore and be certain that the recessed hole is facing up. The 2¼" deep hole serves as a receptacle for a (0 - 100°C) thermometer which measures the temperature of the mold. Open the pressure release valve on the press, and push the top plate of the hydraulic jack all the way down. Place the mold on the press insulating plate within the center markings and slide the heating collar over the mold. Then close the pressure release valve and snug up the mold to about 100 psig, being careful to align the pressure rod and plunger thermometer channels. A 5 amp. Variac is used to regulated the temperature of the heater and the variac dial is set at 48-50 to establish and maintain a molding temperature of approximately 80-82°C as measured with a glass stem mercury thermometer inserted in the top plug.

Allow the mold temperature to reach ∿ 80°C, then pump the pressure up to 4000-4500 psig (measured on the outside scale of pressure gauge for 1¼ inch mold and inside scale for the 1" mold). Maintain the temperature and pressure for 30 minutes. Under compression the PVC mold temperature will rise, therefore, the variac voltage should be reduced to compensate for this and maintain proper temperature. It is essential throughout the process to maintain the temperature and pressure constant (80-82°C and 4000 psig respectively).

Higher temperatures will cause darkening of the PVC plastic and lower temperatures will result in fibrous pockets (cotton balls) within the mount interior. Low applied pressure will result in a soft plastic and voids within the mount. After 30 minutes at temperature under pressure, lift the heating collar to the collar hook adjacent to the pressure ram and turn off the Variac. Allow the mold to cool to 40-45°C with the proper size cooling jacket placed around the mold before releasing the pressure. The latter is accomplished by opening the pressure release valve and with both hands, force the lower plate to a full down position. The specimen is removed by placing the mold over the ejection opening on the left-hand side of the lower plates under the ejection stem and then applying hydraulic pressure. Catch the lower plug, PVC, and upper mold plug upon removal to avoid damage. The mold temperature at removal (40-45°C) is low so that asbestos gloves are not required as for higher temperature removal molds. Due to approximately 3:1 volume shrinkage during melting of the PVC, the above method results in a mount 1¼" diameter and ∿ 3/4" thick. The specimen will be enclosed within the mount ∿ ¼" below the top surface. Provided this procedure is followed, the PVC will be nearly transparent (amber color) allowing observation of the specimen surface and orientation to facilitate rough grinding at the proper angle to the region of interest. Prior to sectioning with abrasives bevel the PVC mount edges with the belt sander for ease of handling and safety. If necessary to retrieve the specimen from the finished mount, Methyl Ethyl Ketone (MEK) can be used to dissolve the hardened PVC. Since this reaction is slow, it is advisable to remove (cut away) as much PVC material as possible. The included hydraulic press and mold assembly identify the apparatus used.

1315 SPECIMEN MOUNT PRESS



1. Base Plate
2. Cylinder
3. Plunger
4. Mold Heater
5. Pressure Release Valve
6. Oil Refill Hole (Not Shown)
7. Pump Handle
8. Thermometer
9. Upper Platen
10. Lower Platen
11. Gauge
12. Gauge Tube Connection
13. Ejector Opening
14. Ejector Stem
15. Base Casting
16. Support Columns
17. Heater Cord
18. Insulating Plate
19. Hydraulic Jack Body
20. Piston
21. Piston Packing Nut
22. Ram
23. Ram Packing Nut
24. Pressure Rod
25. Heater Support Hook
26. Cooler Support Sleeve
27. Cooler Blocks
28. Cooler Lock Lever

EPOXY COLD MOUNTING PROCEDURE (1 1/8" and 7/8" ID RING FORM)

In some cases the delicate structures of microelectronic devices to be examined in cross-sectioning, e.g. wire bonds, cannot withstand the temperature-pressure profiles of compression type mounting without deformation occurring. Thus, for deformable structures, a cold (room temperature) setting mounting media must be used. Epoxides designed for metallurgical specimen mounting material are translucent, clear (amber color), reasonably hard and exhibit excellent adherence and low volume shrinkage with proper curing. These epoxides also bond well to "Bakelite" (organic plastics) ring forms thereby permitting standard size (1", 1 1/4" and 1 1/2" OD) ring forms to be used as specimen mounting molds. The epoxy and "Bakelite" ring forms used are AB EPO-MIX EPOXIDE (20-8133) and AB BAKELITE RING FORMS (20-8151 and 20-8152), BUEHLER LTD. The epoxy can be procured either in bulk quantities (resin and hardener) or in premeasured packets for convenient dispensing. The premeasured packets, containing both resin and hardener, use a separator which is removed prior to mixing in the package itself. Thus, the time consuming task of measuring (weight or volume) constituents, blending and dispensing the epoxy is eliminated. The mounting method uses a "Bakelite" ring form of proper diameter to accommodate the specimen size and is placed on a glass or Teflon plate (dimensions ~4" x 4") which has been coated with silicone grease or other mold release compound. Two methods are commonly employed to position the specimen near the mold center. First, the specimen can be placed flat perpendicular to a pedestal (e.g. nylon or other plastic cylinders of proper height) and the mold subsequently filled with the premixed epoxy with care taken not to pour epoxy directly on the specimen to maintain specimen orientation. Plastic pedestals are

preferred since they generally match the epoxy hardness and contain no metal. Metal pedestals result in metallic particles during sectioning which load the abrasive papers and cloth wheel covers excessively and can cause damage to delicate structures. Second, the mold can be partially filled with epoxy and allowed to cure. The specimen is then placed on the top surface of the cured epoxy in the proper orientation and the mold filled with additional epoxy. It should be noted that using either method the specimen can be orientated at any angle with respect to the original horizontal plane by either positioning the specimen at the desired angle during mounting or machining the completed mount to the desired angle after epoxy cure. The aforementioned epoxy type used cures at room temperature in 6-8 hours and curing can be accelerated by modified mixing and exposure at elevated temperatures as specified by the manufacturer.

One problem commonly encountered in epoxy cold mounting of microelectronic devices is air entrapment within the epoxy. This occurs during mixing of bulk material (resin and hardener) and to some degree with premeasured epoxy packets, as well as during mold filling in either case. The entrapped air results in void formation within the mount and at the specimen surface itself. Voids at the specimen surface are particularly detrimental since specimen edge protection provided by the epoxy is essential for high quality metallurgical sections. These voids also produce pockets for abrasive material entrapment and subsequent edge damage to the specimen during sectioning. Voiding can be partially alleviated by allowing the mixed epoxy to settle for a short time prior to filling the mold. This procedure alone is insufficient for obtaining required specimen edge protection, i.e. 100% coverage of the specimen peripheral surface area, thus vacuum

impregnation must be employed when delicate structures not within the bulk specimen are to be sectioned. Two methods for vacuum impregnation are commonly used.

VACUUM IMPREGNATION OF EPOXY MOUNTS

First, there is a more elaborate technique which we will identify as Method I. The equipment necessary for this technique and a suggested method of assembly are shown in Figure 1. To ensure success, the device should be thoroughly cleaned and dried to promote optimum penetration and adherence of the epoxy to the device. The device to be mounted is positioned* in the desired orientation within a 1" or 1 1/4" Bakelite ring form sealed to a Teflon plate using silicone grease, and placed under the bell jar. The glass portion of the entrance tube should be close to the top of the ring form but should not touch the device itself or extend into the ring form. At this point, the pinchcock is closed and evacuation begun. The amount of vacuum should be adjusted to stabilize just above the predetermined boiling point of the impregnation medium (i.e. if the boiling point of a specific medium is 20 mm of Mercury, then the vacuum should be adjusted to about 22 mm). When the vacuum has stabilized, the free end of the entrance tube is placed in the disposable container holding the impregnating material. The pinchcock is opened slowly to draw the plastic into the disposable container. After the sample is completely covered, the pinchcock is closed and evacuation continued for a few moments longer.

The vacuum pump is then switched off, and the pinchcock slowly reopened to allow pressure in the bell jar to return to normal. At this point the greatest penetration of plastic takes place, since the greater external pressure forces the impregnating material into the voids. The

sample is then allowed to cure. The equipment should be cleaned immediately after use to avoid hardening of any residual plastic.

Method II

In this simplified method, the ring form containing the device (with Teflon back plate in place) is filled with epoxy and placed under the bell jar.* The vacuum pump is connected to the jar by means of a valve which allows the selection of either evacuation of the jar, or alternately a leak to atmosphere. Vacuum impregnation is effected by alternately evacuating and back leaking the system pressure while carefully observing the removal of air bubbles from the mount. This cyclic method is necessary to permit the generation of optimum vacuum pressure, by allowing instant control to prevent boiling off the volatile constituents contained in the epoxy. The onset of boiling in the epoxy is usually disastrous to the mount since sudden eruption and instant localized or general hardening can occur. A possible improvement to this technique would be to limit the vacuum to a pressure just above the boiling point of the epoxy material used.

Method II is certainly simpler and also cleaner in use since the suction tube of Method I is not required. The choice between the two methods is debatable as to superiority of the cured mount. Method I which allows pre-evacuation of the device should prove to be valuable in the removal of air entrapped in pockets and cavities of the device structure. However, additional air bubbles are carried to the mount from the free end of the entrance tube via the epoxy stream when the pinchcock of Figure 1 is opened. In Method II, the rapid evacuation and pressurization cycle can efficiently produce relatively void free mounts if care is used. In any vacuum impregnation method there is a danger in maintaining the

evacuation cycle for an excessive duration. In this situation tiny bubbles (due to the boiling off of volatiles) will continue to escape, with no apparent cessation. In time, however, they will become immobile indicating that the epoxy has partially hardened. It is surmised that the removal of volatiles results in the premature hardening experienced. For best results, the evacuation cycle should be short. A number of experimental runs should be performed to determine the boiling point of the epoxy used as described in techniques for Method I. Then using a vacuum pressure above this predetermined boiling point, the cycle time to the escape of bubbles (volatile constituents) is determined. The vacuum pressure and evacuation cycle should be kept within the safe limits of the above findings.

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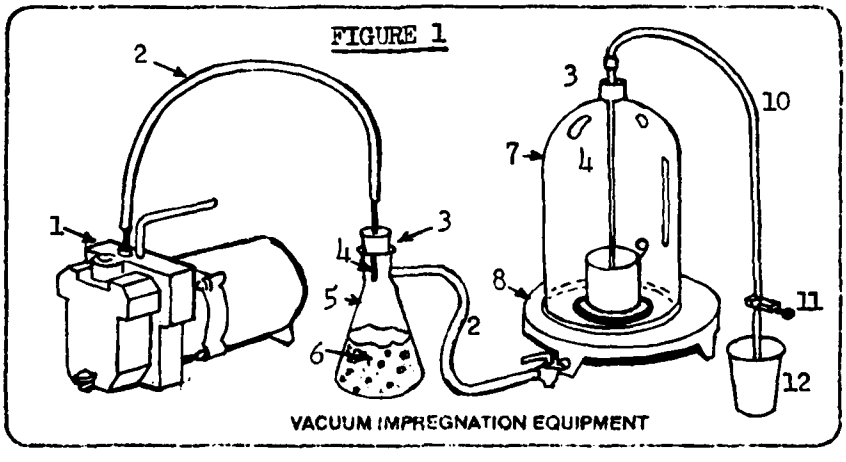
*See Buchler Ltd. Sample-Klip specimen support springs. No. 20-4000. Also, ordinary machine screw nuts, e.g. 6-32 hexagonal brass, serve well as convenient pedestals for devices, when stood up on end in the center of the ring form.

FIGURE 1



VACUUM IMPREGNATION EQUIPMENT

1. Vacuum Pump
2. Vacuum Hose
3. Rubber Stopper
4. Glass Tubing
5. Erlenmeyer Flask
6. Dehydrating Agent
7. Bell Jar
8. Pump Plate and Pad
9. Ring Form on Teflon Plate
10. Plastic Tubing
11. Hose Clamp
12. Disposable Paper Cup

METALLOGRAPHIC CROSS SECTIONING TECHNIQUE

In the sectioning of delicate microelectronic devices, it is first necessary to mould the devices in a mounting media to protect and permit the handling of these miniature structures. Several mounting methods suitable to particular device structures have already been described. The various techniques of 90^{o} sectioning of either the whole microelectronic package containing the semiconductor chip(s), etc., (or the chip itself after removal from the package), are described below.

The excess mounting plastic, at 90^{o} to the selected edge of the device, must first be removed close to this edge or to other selected regions of the device as desired. This excess plastic may be sawed away or abrasively removed using a coarse 60-80 SiC grit belt surfacer. It is imperative that the fragile regions of the device to be sectioned are not contacted with the saw or belt surfacer coarse cutters. These regions, the silicon chip and the glass to metal seals, etc., could be irreversibly damaged when cut or abraded by the coarse abrasives. When necessary, cuts in these brittle materials could be made with a low speed diamond saw close to the region of interest.

Following removal of the excess mounting material, coarse and fine grinding is performed using 180, 240, 400 and 600 grit (mesh size) SiC wet or dry abrasive papers, respectively. These are used on a hand surfacer lubricated with water. As usual, in grinding the surface to successively finer abrasive finishes, it is necessary to remove all traces of coarser abrasive particles before proceeding to a finer abrasive. To prevent cross contamination of abrasives, the mount is thoroughly scrubbed,

or the use of ultrasonic cleaning methods are used. The surface of the section is ground using the coarser grits for a time necessary to bring the face of the mount very close to the region of interest. At no time should the silicon chip be ground with an abrasive coarser than 400 grit. Failure to follow this precaution could result in excessive damage to the silicon. With care, it is possible to section right to the region of interest using successively finer grits. Each abrasive grit size is used for a duration long enough to remove the damage (coarser scratches) due to the proceeding abrasive size. When it is judged that all of the 400 grit scratch damage has been removed by use of the 600 grit abrasive, one can then proceed to one of the rough polishing abrasives. These consist of alumina powders, graded in 1.0, 0.3, and 0.05 micron size and are used on cloth covered wheels for rough to fine polishing, respectively. More popular are the diamond abrasives graded in 6.0, 1.0 and 0.25 micron size and used on a Texmet covered wheel. The foregoing are of polishing grade grit size and are used with water and/or oil lubricant extenders. The precaution of cleanliness cited above must be adhered to even more carefully in the polishing stages since this is the final step, wherein the true microstructure of the device is revealed. Layers measuring less than 1 micron in thickness will be visible and the surface finish necessary to delineate defects within these regions is difficult to achieve.

A new instrument for cross sectioning, the Minimet by Buehler, has provisions for handling mounts singly through the full range of abrasives listed above. Moreover, cross contamination is minimized through the use of separate abrasive platens. The speed of oscillation of the mount to the platen and the pressure are fully adjustable. The grind or polish

cycle may be timed out at either a constant pressure, or a gradually decreasing pressure may be set. A considerable finer degree of control may be exercised over the various stages of the section than is possible in hand held methods.

In hand held methods a motor driven variable speed wheel covered with special cloth disks are charged with the appropriate abrasives. A suitable lubricant is mixed with the abrasive and the mount with the specimen imbedded is pressed against the rotating wheel. The optimum hand pressure and wheel rotational speed (RPM) are governed by several factors; e.g. abrasive type, mounting media, nap of cloth covering etc. The abrasive type used has the greatest influence on the pressure and wheel speed variables. Diamond abrasives generally perform well under heavy hand pressure and high rotational speeds. In general, heavier pressures are recommended for coarse polishing and light pressure for short duration during final polishing. Normally the optimum selection of these variables can be determined experimentally and are not too critical. In all polishing methods, both manual and automatic, it is important to avoid prolonged polishing with any given abrasive in order to prevent undesirable relief cutting, i.e. preferential cutting of softer materials. In manual polishing, to obtain a more uniform polishing action, it is recommended the mount be moved slowly around the wheel in a direction counter to the wheel rotation. Again, specimen mount cleaning between each polishing stage as described previously is of utmost importance in achieving a scratch free metallurgical section.

0.

SCANNING ACOUSTICAL MICROSCOPY

0. Scanning Acoustical Microscopy.

1. Introduction. The acoustical microscope is an analytical tool whose course of development and importance to the scientific community may parallel that of the scanning electron microscope. Though in a relatively early stage of development compared with electron microscopy, the acoustic microscopy field is demonstrating its importance in a broad spectrum of applications, such as:

- Distinguishing between different materials of a solid surface
- Determining the thickness of different material layers
- Displaying variations in the elastic constants on a microscopic scale
- Examining alloying spikes of aluminum and silicon
- Examining regions surrounding dislocations and faults in single crystals that are highly stressed
- Detecting subsurface defects, flaws, inclusions and disbonded areas

Scanning acoustical microscopy has been used by the reliability engineer and analyst to evaluate the construction of passive and active electronic components.

Out of the research efforts of a number of groups over the last five years essentially two techniques have emerged as viable practical acoustic microscopes, the SLAM and the SAM.

2. Scanning Acoustic Microscopy (SAM). In the SAM, an incident acoustic wave is launched into a water medium by a piezoelectric transducer bonded onto one end of a cylindrical sapphire rod. The other end of the rod has a concave spherical surface ground into it, causing the acoustic beam to be focused a short distance away. A receiver rod, geometrically the same as the transmitter rod, is colinearly and confocally aligned with the transmitter to achieve maximum signal and resolution. For visualization, a thin sample is placed at the focal zone and it is systematically indexed mechanically. Variations in the sonic transmission are used to brightness modulate a CRT display. The position output signal of the sample drive mechanism is synchronized to the X and Y axes of the display. Horizontal scanning is accomplished by a rod attached to a vibrating loudspeaker cone. The vertical mechanism is a small precision hydraulic piston. A block diagram of the acoustic system is shown in Figure 1 after Lemons and Quate.

Regarding the focusing of waves, in an optical system lens designs are usually quite sophisticated in order to compensate for spherical aberrations. Multi-element lenses are usually necessary. In the acoustic system, however, the situation is much less involved for two reasons. In the first place, the lens in the SAM is always used "on axis" rather than in an imaging mode; here, the sample is moved through the focused beam. In the second place, the spherical aberrations which preclude the use of simple lenses in an optical system are minimal in the acoustic system because of the larger refractive index ratio between lens material and the fluid space in which the rays come to focus. As a comparison, in typical optical systems, a light beam is focused from glass of index 1.5 to air of index 1.0. In the acoustic system the velocity of sound ratio (the reciprocal of the index of refraction ratio) is 7.5 between the sapphire rod and water. Thus, the rays from the paraxial region and the far region join focus in a more precise manner than they would if the index of refraction ratio was smaller.

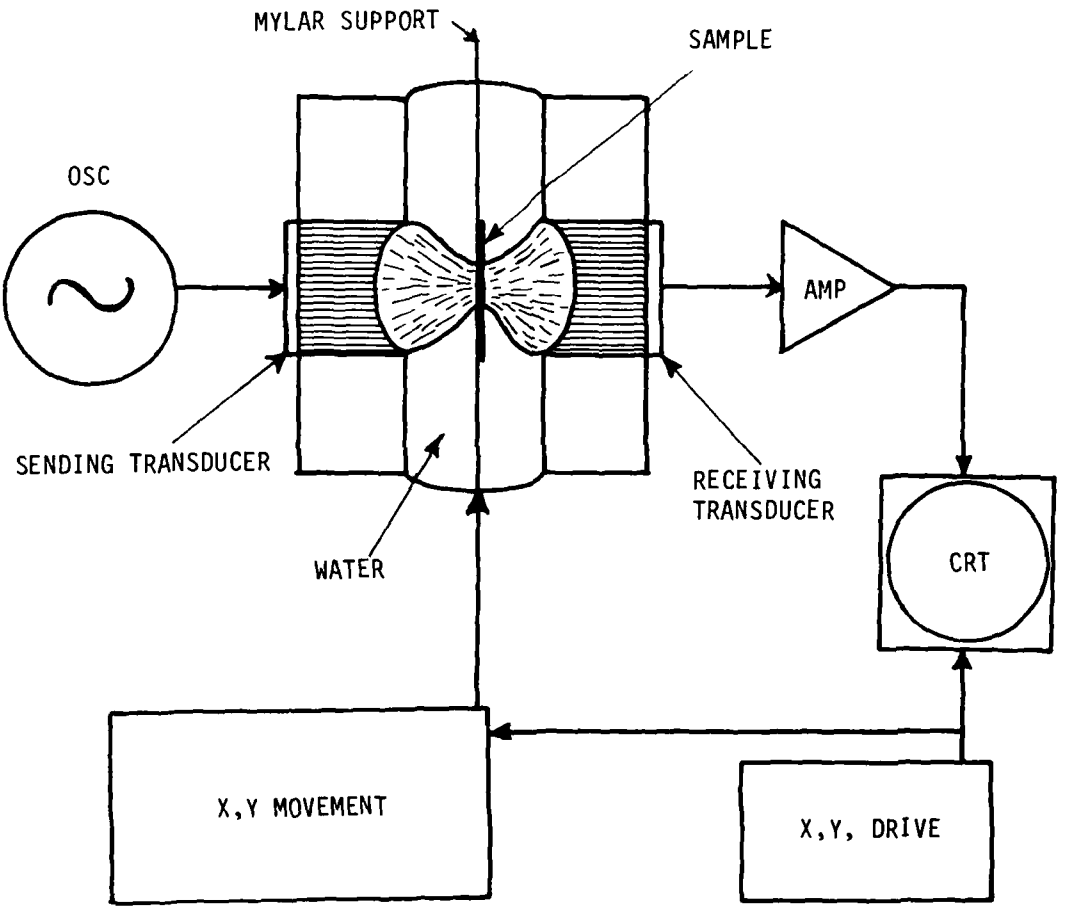


FIGURE 1. SCHEMATIC DIAGRAM OF THE SCANNING ACOUSTICAL MICROSCOPE (SAM) (AFTER LEMONS AND QUATE)

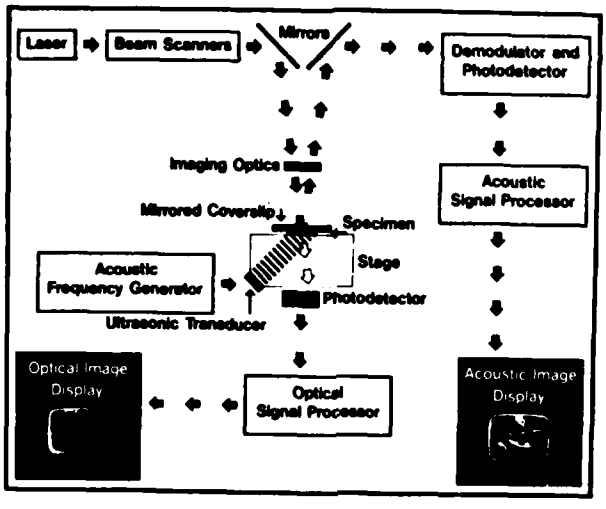
The frequency of operation of the SAM is limited by the ultrasonic attenuation in the fluid (usually water) between the transmitting and receiving rods. The attenuation of signal depends upon the separation distance between the lens surfaces; this in turn depends upon the lens radius of curvature. The distance can be decreased if the lens radius is made smaller. Because of the high velocity of sound ratio, the focal zone is located about 13 percent farther out than the center of curvature of the lens. Therefore, the lens-to-lens separation is about 3.6 mm, and the consequent attenuation loss in the water path, excluding that due to the specimen, is 20 dB at room temperature. In the most recent experiments the reported operating frequency is 3 GHz where the wavelength of sound n water (0.5 μm) is comparable to visible light. However, because of the extremely high ultrasonic absorption in water, viz. 8000 dB/cm at 60°, the lens-to-lens distance must be considerably reduced. Thus, Jipson and Quate have achieved microscope operation at 3 GHz with a lens whose radius is only 40 μm.

The basic advantage of piezoelectric acoustic detection is that it is capable of very high sensitivity. Unfortunately, however, the fluid space between the sample and the lenses must be long enough to achieve acoustic focus, and significant signal is lost in traversing the path. The possibilities of further increases in frequency and, therefore, resolution are based upon finding suitable low-loss fluids as well as fabricating precise lens surfaces with still smaller radii of curvature. A very interesting approach to achieving high resolution in the SAM, suggested by Quate, is to operate the instrument with the samples in liquid helium where the wavelength of sound is much shorter than in water, and the absorption losses are orders of magnitude lower.

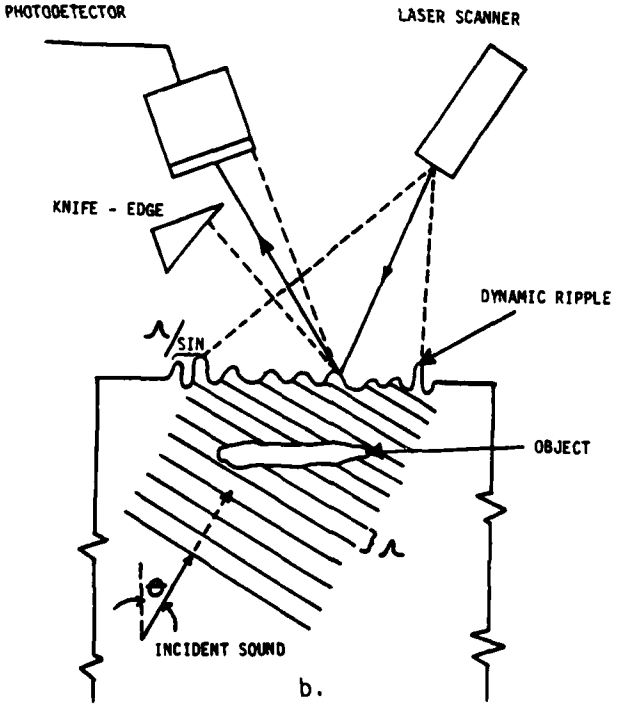
3. Scanning Laser Acoustic Microscope (SLAM). In the SLAM, a specimen is viewed by placing it on a stage where it is insonified with plane acoustic waves (instead of focused waves as in SAM) and illuminated with laser light. The block diagram of this

system is shown in Figure 2. Within the sample, the sound is scattered and absorbed according to the internal elastic microstructure. The principle upon which the laser beam is employed as a detector is based upon the minute displacements which occur as the sound wave propagates. As shown in Figure 2, an optically reflective surface placed in the sound field will become distorted in proportion to the localized sound pressure. The distortions are dynamic in that the pressure wave is periodic and the mirror displacements accurately follow the wave amplitude and phase. At every instant of time, the mirror surface is an optical phase replica of the sound field. The laser is used to measure the degree of regional distortion. By electronically magnifying the area of laser scan to the size of the CRT monitor and by brightness modulating the display, the acoustic micrograph is made visible. If the sample is made of a solid substance which can be optically polished (as for metallurgical examination), the sample is viewed directly with the laser. However, if the sample is not polished (for example, biological tissue or unprepared solid material), a plastic mirror (coverslip) is placed in contact with the sample to relay the sonic information into the laser beam. The laser detection process is further explained with reference to Figure 3.

A light beam incident upon the mirror will be reflected at an angle equal to the incident angle. When the surface is tilted by an amount proportional to the sound pressure, the reflected light is angularly modulated (spatially). If all the reflected light is captured by a photodiode, its electrical output signal will be a dc level only because the light power reaching the detector will not change as a function of angle. However, if part of the light beam is blocked by an obstacle (or knife-edge) then the amount of light reaching the photodiode will depend upon the instantaneous angular position of the beam. Thus, the electrical signal output will now consist of a dc component plus a small ac term coherent with the acoustic amplitude.



a.



b.

FIGURE 2. SCANNING LASER ACOUSTIC MICROSCOPE (SLAM)

a. Schematic Diagram
b. Detection of Acoustic Energy

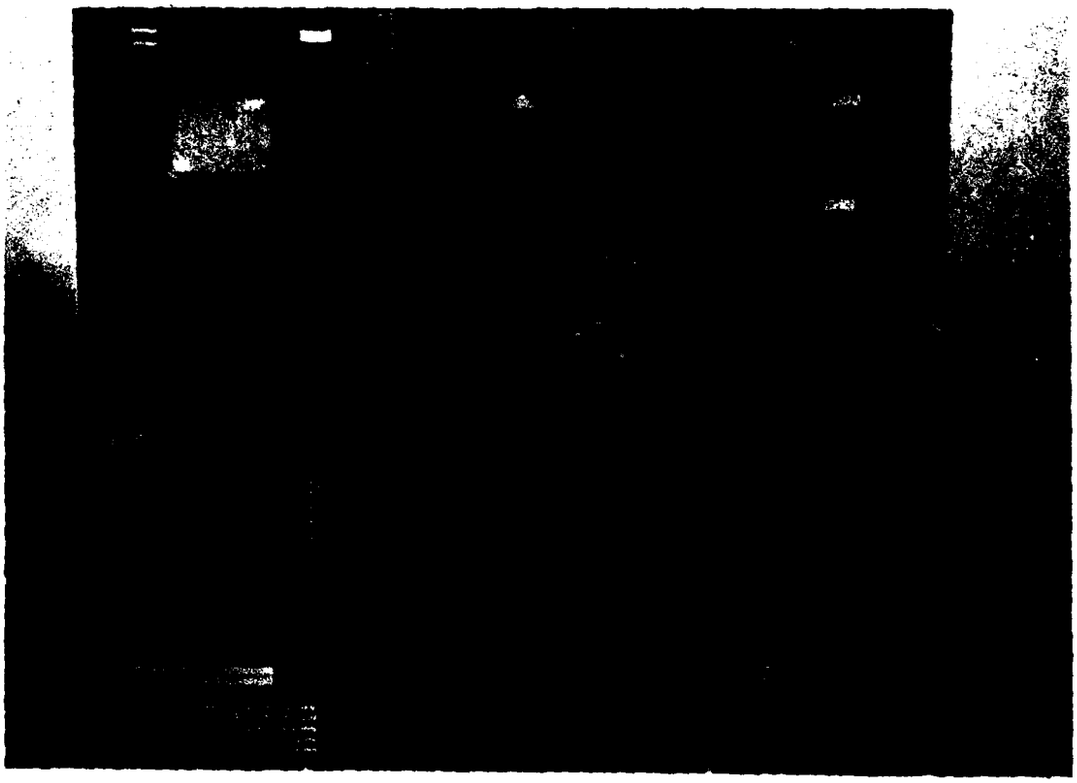


FIGURE 3. SCANNING LASER ACOUSTIC MICROSCOPE (SLAM)
TYPICAL COMMERCIAL EQUIPMENT, SONOMICROSCOPE 100

As a byproduct of the laser scanning technique, a corresponding optical image of the sample is obtained simultaneously, as shown in Figure 3. In the case of optically translucent samples, such as biological material and some solid materials, a "partially silvered" coverslip is employed. Now, a fraction of the probing laser light can penetrate the mirror and sample. This transmitted light is detected and the resulting signal fed to an adjacent CRT monitor, thus constituting an optical image. In the case of a reflective polished specimen such as a metal prepared for metallographic examination, an optical reflection image is produced. The importance of the simultaneous optical image is very great to the user, for it permits information obtained by acoustical microscopy to be immediately compared to a familiar optical frame of reference. This is accomplished without repositioning the sample or disturbing its environmental circumstances.

The laser beam scanning technique is based upon the use of an acousto-optical diffraction cell originally developed for a "laser TV" projection scheme in the late 1960's. This was developed because of the difficulties associated with linear mechanical scanning of mirrors for the horizontal deflection at "TV" frequencies, viz. 15.75 kHz. In an acousto-optical cell a traveling ultrasonic wave serves as a diffraction grating for the laser beam. If the interaction distances are sufficiently long, efficient Bragg diffraction occurs and virtually all of the light is diffracted into a single side order whose angular position is a function of the grating spacing. By changing the acoustic frequency to the cell, the output laser beam is made to scan over a range of angles limited by the bandwidth of the transducers. The vertical scanning of the laser beam is accomplished by linearly moving a mirror which is attached to a servo controlled galvanometer. The frame rate of the system is identical to that of standard TV, i.e., 30 frames per second.

The frequency of operation of the SLAM is usually between 100 and 500 MHz, the frequency of choice being dictated by intrinsic

attenuation of signal in the sample. Comparing to the SAM, wherei a lossy fluid path is needed to establish focus prior to entering the specimen, the SLAM needs only a thin fluid film to couple the sound from the stage to the sample. Also, thick samples are not as much of a problem with the SLAM except for losses within the samples themselves. Another basic advantage of the SLAM is that the sample remains stationary; the light beam does the scanning and produces acoustic and optical images simultaneously. Like the SAM, the SLAM can be pushed upwards in frequency and down in temperature to liquid helium in order to achieve higher resolution. Unlike the SAM whose resolution limit depends upon the quality of a lens, the limit of resolution in SLAM is governed by the wavelength of the laser light.

4. Imaging Techniques. A number of imaging modes and acoustic microscopy techniques are available:

- o Acoustical amplitude transmission images (SLAM and SAM)
- o Acoustical phase contrast imaging
- o Acoustical interferograms
- o Acoustical reflection images (SAM)
- o Acoustical dark-field images (SLAM)
- o Non-linear acoustic imaging
- o Polarization sensitive acoustic imaging (SLAM)
- o Acoustic line scan mode
- o Acoustic reflectivity profile

Acoustic microscopy, like all microscopic techniques, is primarily a qualitative technique. The information contained in acoustic amplitude or phase micrographs constitute characteristic material signatures.

Thus, much of the useful information obtained with acoustic microscopy is purely morphological in nature. These data can be

used to classify and sort materials, detect and localize flaws and defects in optically opaque samples, and map compressibility and density variations on a microscopic scale.

In addition to the qualitative aspects, techniques have been developed to quantitatively measure elastic properties on the microscopic scale. These techniques include graphic analysis of the acoustic interferograms to obtain velocity data as well as measurement of acoustic transmission levels through samples to obtain quantitative attenuation data. Additional techniques include stereoscopy, acoustic line scan, and acoustic reflectivity profiling. The last two are not true imaging modes or image analysis methods but instead are new characterization capabilities which have arisen from the microscope technology.

Stereo viewing is an accepted method of depth determination; it also enhances the information gathering process within the eye-brain complex. The technique is commonly used for observing the terrain from aerial photographs as well as for understanding the features of a sample visualized in a scanning electron microscope. The acoustic microscope employs relatively straightforward applications of the standard technique; namely, a set of images is made with the source of insonification at different angles. Depth determination can also be made by simple axial translation of the sample. This method can be used to determine defect locations in joints of various materials.

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EQUIPMENT

SONOMICROSCOPE 100

SCANNING LASER ACOUSTIC MICROSCOPE

Standard Features

Ultrasonic frequency 100 MHz nominal
Single and swept frequency insonification modes
Simultaneous acoustic and optical imaging
Dual 11" diagonal TV displays
Electronically activated interference mode of operation
Real time output - 30 frames per second
Standard composite video signal outputs for video tape recording or computer interface
Overall size - 76" wide x 34 3/4" deep x 60" high
110 volt line service 60 Hz

F.O.B. Bensenville, Illinois $97,038.00

Optional Features

Alternate frequency of operation
Accessory insonification stage
35 mm camera and mounting brackets
Polaroid camera and precision display for photography
Video tape recorder installed
Customized accessories
50 Hz power

P.

MICROBEAM ANALYSIS
TECHNIQUES

P. Microbeam Analysis Techniques.

1. Introduction. Microbeam analysis has practically become synonymous with Scanning Electron Microscopy (SEM) because of its rapid growth in popularity in the past 12 years and, in particular, its universal use in the microelectronics industry. But there has also emerged an imposing and growing list of exotic analytical instruments that exploit the information in interactions between specimens and energetic beams of ions, alpha particles, X-rays, lasers, ultraviolet visible light, microwaves, and acoustic waves, as well as a whole energy spectrum of electrons. In general, the interactions are not new in a theoretical sense but their analytical usefulness has only recently become accessible through advances in solid-state circuitry, computer data processing, ultra sensitive detectors, and the commercial practicality of reliable sophisticated mechanical and electronic systems.

Few, if any, organizations have a complete and up-to-date collection of all the available analytical equipment, and no individual analyst can master them all. However, time can be rented on most of the commercial analytical machines through service organizations, and sometimes feasibility work can be done on some of the developing systems. The problem of the analyst is to know which techniques or instruments are most likely to yield maximum relevant information at minimum cost and to avoid being limited by using only the tools that happen to be at hand.

Microbeam analysis equipment suitable for microelectronic failure analysis can be listed in two groups on the basis of extent of usage:

a) Scanning Electron Microscopy (SEM), which with the appropriate commercially available accessories at present dominate microelectronic failure analysis:

- o Topographic or Microstructure Analysis
- o X-ray Emission Elemental Analysis (EDS-Energy
- o Dispersive, WDS-Wavelength Dispersive)
- o Voltage Contrast Imaging
- o Electron Beam-Induced Voltage and Current (EBIV
- o and EBIC)
- o Cathodoluminescence (CL)

b) Other techniques of surface analysis:

- o Auger Electron Spectroscopy (AES)
- o Scanning Auger Microscopy (SAM)
- o Secondary Ion Mass Spectrometry (SIMS)
- o Scanning Secondary Ion Mass Spectrometry (SSIMS)
- o Ion Surface Scattering Spectroscopy (ISSS)
- o Electron Spectroscopy Chemical Analysis (ESCA)
- o Scanning Electron Spectroscopy for Chemical
- o Analysis (SESCA)
- o Scanning Electron Stimulated Desorption (SESD)
- o Scanning Transmission Electron Microscopy (STEM)
- o Automated Scanning Low Energy Electron Probe (ASLEEP)
- o Ultraviolet Photoelectron Spectroscopy (UPS)
- o Ion Microprobe Mass Analysis (IMMA)
- o Electron Energy Loss Spectroscopy (EELS)

See summaries on next page.

The commercial embodiments of these instrumental techniques are continually changing, with a trend toward combining several functions in one instrument. Many of the techniques require common components such as vacuum systems, beam-focusing magnetic lenses, picoampere current amplifiers, cathode ray imaging, and digital data processors. The advantages of commonality include obtaining several kinds of information from the same site on the specimen. However, as T.L. Barr has cautioned, "most surface-analysis tools are very complex electronic systems with sizeable downtimes . . .

TABLE I

SUMMARY

CHARACTERISTICS OF MICROANALYSIS TECHNIQUES

Technique	Primary Radiation	Secondary Radiation	Constituents Measured	Lateral Resolution	Depth Resolution	Typical Detection Limit
(1) X-ray Microanalysis	Electron	X-ray	Elements $Z \geqslant 11$ (EDS) $Z \geqslant 4$ (WDS)	1 μm	1 μm	750 ppm (EDS) 100 ppm (WDS)
(2) Auger Microanalysis	Electron	Electron	Elements $Z \geqslant 3$	0.1 - 1 μm	1 nm	0.1 percent
(3) Cathodo-luminescence	Electron	Photon	Molecules, other	1 μm	1 μm	1 - 1000 ppm varies strongly
(4) Secondary Ion Mass Spectrometry	Ion	Ion	All elements Molecules	1 μm	1 nm	1 ppm
(5) Ion Scattering Spectrometry	Ion	Ion	Elements $Z \geqslant 3$	100 μm	1 atom layer	100 ppm - 0.1 percent
(6) X-ray Fluorescence	X-ray	X-ray	Elements $Z \geqslant 11$ (EDS)	1 mm - 1 cm	100 μm	1 - 10 ppm
(7) Laser Raman Microprobe	Photons	Photons	Molecules	1 μm	1 μm	1 percent
(8) Laser Microprobe Mass Analyzer	Photons	Ions	All elements *(Molecules)*	1 μm	1 - 10 μm	1 ppm
(9) Electron Energy Loss Spectroscopy	Electron		Elements $Z > 3$	$\lesssim 10$ nm	Specimen Thickness $\leqslant 100$ nm	1000 ppm

SUMMARY

QUANTITATIVE MICROANALYSIS TECHNIQUE CHARACTERISTICS

	Quantitation Technique	Relative Accuracy	Characteristic Signal Images	Non-Conducting Samples	Vacuum Requirements
(1)	ZAF	1 - 5 percent ($Z \geqslant 11$)	Yes	Yes, coated	$< 10^{-2}$ Pa
(2)	Sensitivity Factors	10 - 25 percent	Yes	Difficult	$< 10^{-6}$ Pa
(3)	Working Curve	10 percent	Yes	Yes, coated	$< 10^{-2}$ Pa
(4)	Sensitivity Factors	20 percent	Yes	Yes	$< 10^{-5}$ Pa
(5)	Working Curve	20 percent	Yes	Yes	$< 10^{-7}$ Pa
(6)	Working Curve	5 percent	No	Yes	$< 10^{-1}$ Pa
(7)	Under Development	-	Yes	Yes	Atmospheric Pressure
(8)	Working Curve	5 percent	No	Yes	$< 10^{-3}$ Pa

'interlocked' systems will suffer from multiples of the separate downtimes." The failure analyst is apt to encounter a variety of instrumental combinations of different vintages and performance.

2. Microstructural Analysis in the SEM. SEM pictures of microelectronic devices are generally spectacularly more informative than light microscope pictures. The reasons are:

- o Superior depth of field (about 500 times greater than light pictures)
- o Higher resolution magnifications up to about 100,000X
- o Greater working distance, so that package cavities generally present no problem
- o The ability to accommodate tilt angles up to 90° (This is the result of 1) and 3). Dynamic or real-time focusing
- o The contrast mechanism of secondary electron emission accurately images surface topography which in a light microscope merely scatters light that is lost to the image-forming lens system

On the other hand, there are instances where the light microscope retains significant advantages over the SEM:

- o Multilayer thin films, such as silicon oxide or nitride on silicon or aluminum, are low in contrast in the SEM, and gradual variations in thickness are very difficult to image. Vertical illumination in a light microscope produces well-defined interference colors of good contrast that readily reveal passivation defects.

- o Light will penetrate glassivation layers and often allow inspection of the substrate. The SEM (in the secondary electron emission mode) derives most of its information from very near the surface.

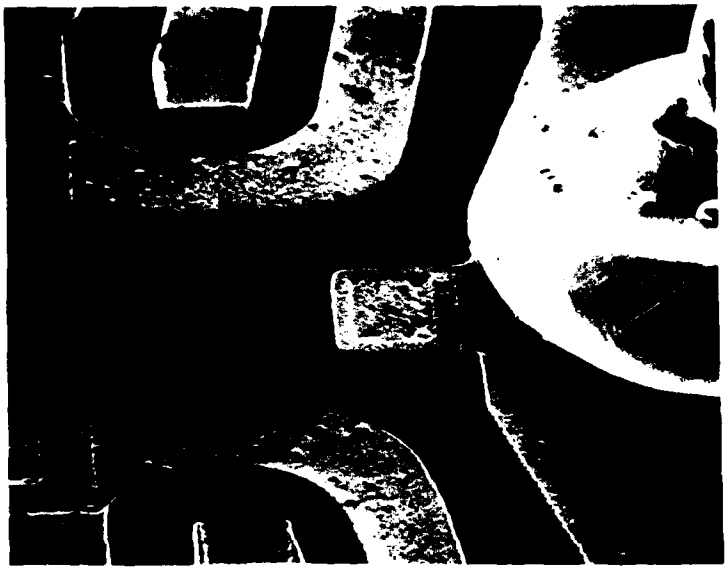
- In some SEMS, it is difficult to photograph an entire device at low magnification, e.g., below 20X, whereas this is no problem with light microscopy or macroscopy (see Chapter III-L, Optical Analysis Techniques).

The techniques of SEM operation have been exhaustively documented since 1967, particularly in the proceedings of the Scanning Electron Microscope Symposia published annually since 1968.

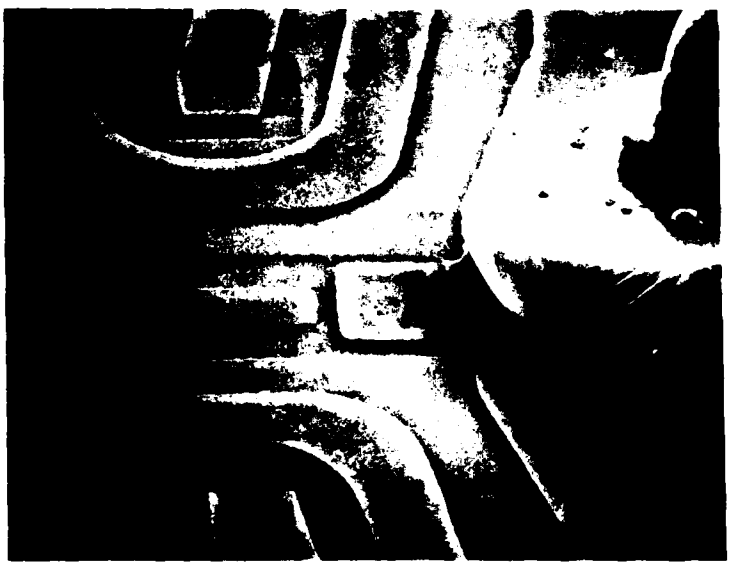
3. General SEM Operating Procedure. There are today many high quality SEM's available for the failure analyst to use which are usually supplied with information on normal equipment adjustment and operation entirely suitable for routine analysis; however, there are a number of significant factors affecting image contrast and quality which should be remembered:

a) Influence of Accelerating Voltage on Image Quality. In the SEM, generally, finer surface structural images can be obtained with lower accelerating voltages. At high accelerating voltages, the beam penetration and diffusion area becomes larger, resulting in unnecessary signals (e.g., backscattered electrons) being generated from within the specimen. These signals reduce the image contrast and obscure the fine surface structures. It is especially desirable to use low accelerating voltage for observation of low-concentration substances. Examples of the effect on image quality due to accelerating voltage are illustrated in Figure 1. This figure illustrates the image quality variation due to accelerating voltage during the examination of a microcircuit.

One of the disadvantages of low accelerating voltage is the deterioration of the resolution, but resolutions of 300Å to 500Å can be readily obtained through compensating adjustments. One method is to strongly excite the condenser lens, set the working distance to 13mm, and fully perform astigmatism correction.



1a) ACCELERATING VOLTAGE 3KV



1b) ACCELERATING VOLTAGE 30KV

FIGURE 1. MICROCIRCUIT, ACCELERATING VOLTAGE EFFECT ON IMAGE QUALITY

In general, the higher the accelerating voltage, the better is the resolution; however, there are unnegligible disadvantages in increasing the accelerating voltage, such as:

- Lack of detailed structure of specimen surface
- Larger edge effect (i.e., edge brightening)
- Higher probability of charge-up
- Greater specimen damage by electron beam

b) Influence of Charge-up on Image Quality. If the specimen is a nonconductive material, it is negatively charged up by the electron beam, and this disturbs normal secondary electron emission. This charge-up causes some unusual phenomena, such as:

- Abnormal contrast
- Image deformation and streaking
- Image shifts

There are a number of ways to minimize these effects some of which are fairly common knowledge, such as:

- Ground all device leads to stub
- Evaporate or sputter carbon or gold overcoatings

Often neglected are the effects of charging nearby insulators outside the immediate picture area. Examples are:

- Sidewalls of ceramic packages
- Insulators in the SEM specimen stage
- Plastic-covered wires to sample stage
- Non-conductive surfaces in the SEM specimen chamber

c) Contamination of the Specimen. When the electron beam irradiates the specimen for a long time in a vacuum, the residual organic compounds in the column build up as contamination at the beam irradiation spot on the specimen surface. This contam-

ination layer produces a number of effects on the secondary electron images and elemental analysis results, such as:

- o Image becomes darker because of decreased secondary electron emission
- o Resolution becomes lower because the contamination layer covers microstructures of the specimen surface
- o Detectability of elemental analysis with EDS or WDS becomes lower, especially for the lighter elements

The contamination rate can be effectively decreased by cooling the surroundings of the specimen. Many SEM's offer a cold finger or liquid nitrogen trap to provide this cooling near the specimen. This trap reportedly decreases the rate of contamination buildup to 1/10~1/20, the usually encountered rate.

d) Specimen Tilt Angle. Samples to be examined in a SEM must first be mechanically and electrically secured to a holder designed to be mechanically attached to the SEM specimen stage. The ability of a stage to incline the specimen surface toward the electron detector by means of an external control is termed specimen tilt. The angle of inclination (θ) formed by specimen tilting is defined as the angle between the plane normal to the path of the primary electron beam and specimen surface as illustrated in Figure 2. The primary function of tilt is to obtain a favorable position for viewing the specimen. Advantages obtained by proper adjustment of specimen tilt include:

- o Increased electron emission
- o Improved contrast
- o Reduced electrostatic charging

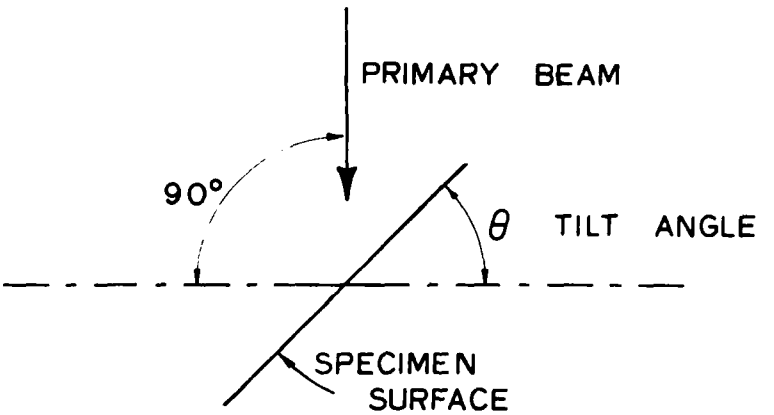


FIGURE 2. DIAGRAM ILLUSTRATING SPECIMEN TILT ANGLE

e) Summary. SEM operation procedures must not become stereotyped for all semiconductor device applications if optimum images are to be obtained. The failure analyst must recognize the need for flexibility in selecting and using SEM parameters and analytic procedures to yield the maximum information from semiconductor devices. The primary consideration in topographical analysis of semiconductor devices in the SEM is the reduction of primary electron beam penetration. The methods for accomplishing this are low accelerating voltage and high specimen tilt. These techniques result in improved signal-to-noise ratio (SNR) and contrast, less charging and, in general, good resolution. Table II summarizes the results of varying significant SEM operating parameters.

f) Image Problems. It is possible to classify various poor images into some general groups:

- o Images lacking sharpness and contrast
- o Unstable images
- o Generally poor quality images
- o Noisy images
- o Images showing jagged edges
- o Unusual contrast images
- o Distorted or deformed images

These image disturbances, besides being attributed to defects in the instrument itself, are occasionally caused by the operator's lack of experience, improper specimen preparation, and external influences such as installation room conditions. Tables III and IV show typical image disturbances and their causes. It is always a good idea to run through these tables before calling on the SEM maintenance engineer.

TABLE II – Results of Varying Significant SEM Operating Parameters

	Increasing Accelerating Voltage	Increasing Beam Current	Increasing Specimen Tilt	Increasing Number Lines/Frame	Increasing Time/Frame	Removal of the Passivating Layer	Coating Specimen
Beam Penetration	Increase		Decrease			Increase*	Decrease*
SNR	Decrease	Increase	Increase		Increase	Increase	Increase
PPR	Increase	Decrease		Increase		Increase	Decrease
Contrast			Increase			Increase	Increase
Charging	Sample Dependent	Increase	Decrease			Decrease	Decrease
Contamination Due to Beam	Increase	Increase					

*With reference to the active region of the device.

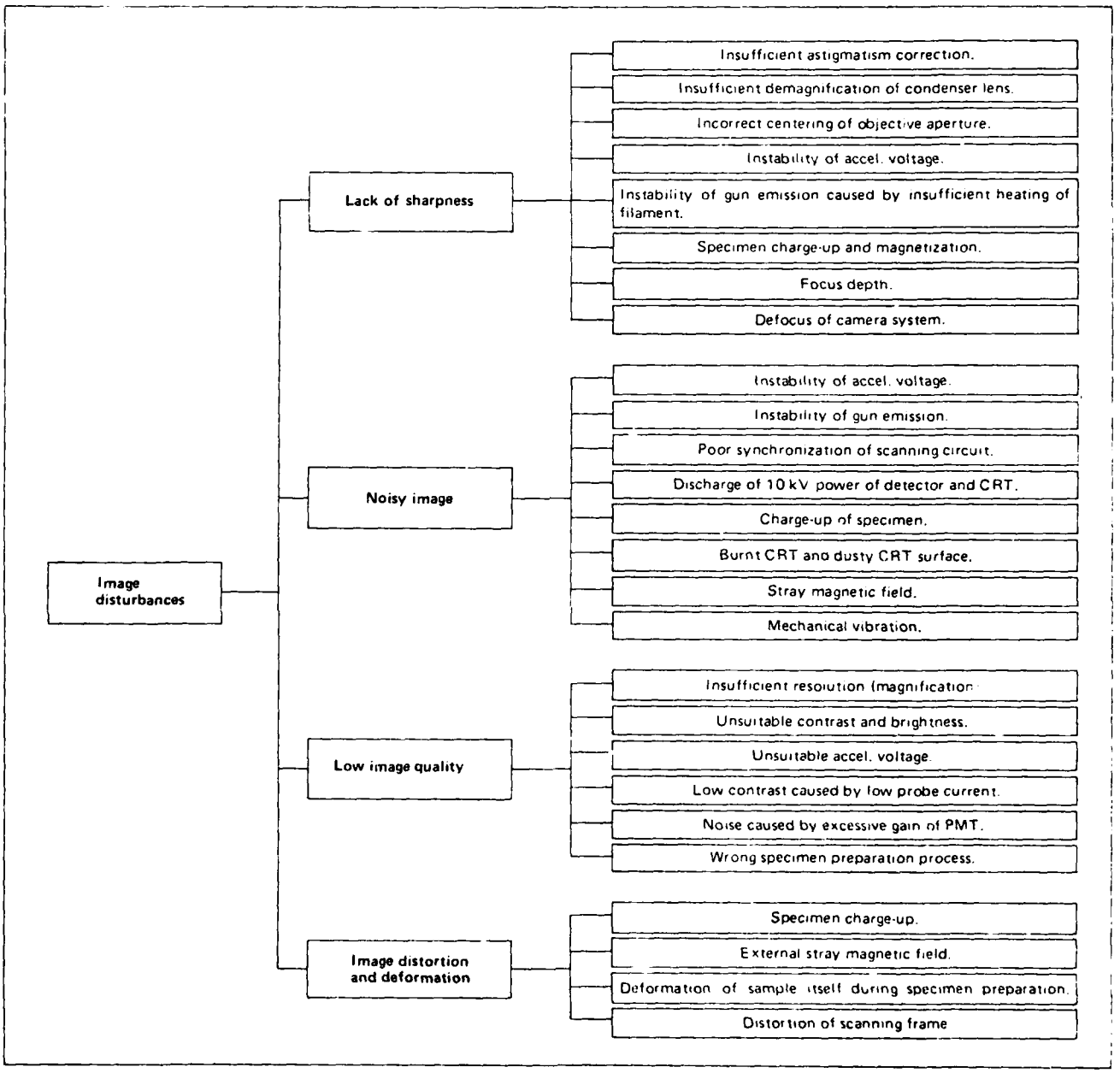


Table III. **Image Disturbances and Their Causes**

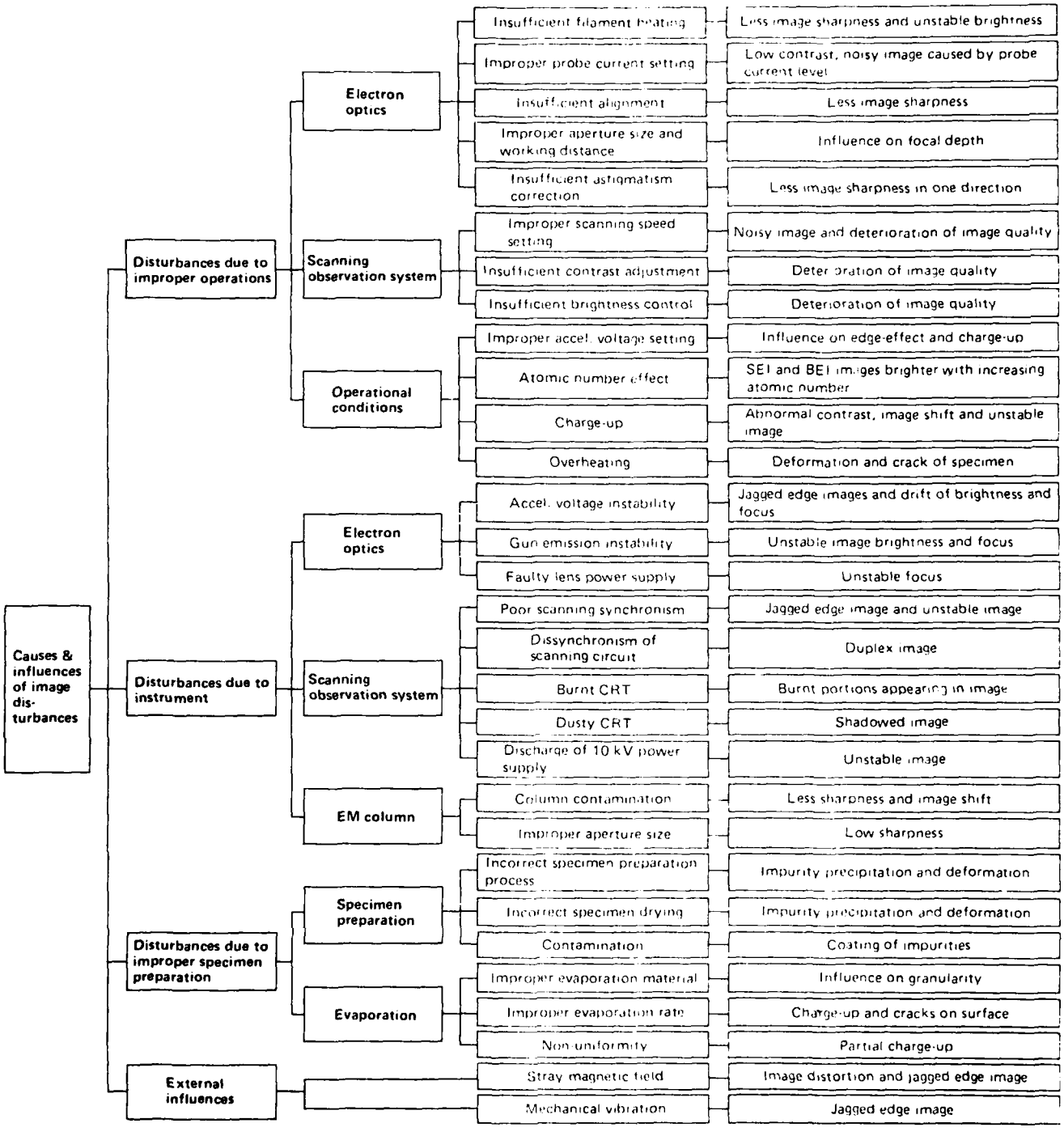


Table IV. **Detailed Image Disturbances and Their Causes**

4. Elemental Analysis by Electron-Stimulated X-ray Emission in the SEM. Historically, this type of analysis originated with the electron microprobe developed by Castaign. This instrument used fully focusing X-ray optics, and by SEM standards a rather large-diameter beam, and a rudimentary imaging capability. The small dimensions of microelectronic devices have prompted the more widespread use of X-ray spectrometers attached to the specimen chamber of the SEM. Since the maximum beam current of a typical SEM is of the order of one microampere (considerably less than that of a microprobe), the signal-to-noise ratio is less with the SEM but still adequate for most purposes.

Two basic types of X-ray detectors are in use on electron-beam instruments:

o Solid-state detectors such as lithium - drifted silicon crystals, coupled to multichannel analyzers. All detectable X-ray energies are presented simultaneously in a spectrum readout so that qualitative identification of elements is possible in a matter of seconds. These are generally called energy-dispersive spectrometers, or EDS. Figure 3 is a typical EDS spectrum plot of a semiconductor contact structure. The horizontal axis is in electron-volts (eV), and the vertical axis is a relative amplitude based on the number of X-ray counts. Each element has a characteristic energy spectrum which enables the analyst to identify elements but not compounds. This particular spectrum contains the characteristic energy lines for the silicon base, silver, chromium, and nickel.

o Diffraction crystals obeying Bragg's Law, coupled to gas-flow proportional counters. Spectral peaks are scanned sequentially by changing the crystal angle. These systems are wavelength dispersive spectrometers or WDS. The spectra peaks can be recorded on a strip-chart recorder to allow optimization of crystal setting for each element, or the change in X-ray counts from background can be used. Figure 4 is an example of a WDS spectra recording for a silver standard. The spectrum is made up of a large $L\alpha$ double peak, and the remainder are $L\beta$ peaks.

X-Ray Spectrum Lines

(Reading Left to Right)

Element	Line	KeV
Nickel	$L\alpha$	.86
Silicon	$K\alpha_{1,2}$	1.74
Silver	$L\alpha_1$	2.98
Silver	$L\beta_1$	3.16
Chromium	$K\alpha_{1,2}$	5.40
Chromium	$K\beta_1$	5.96
Nickel	$K\alpha_{1,2}$	7.48
Nickel	$K\beta_1$	8.26

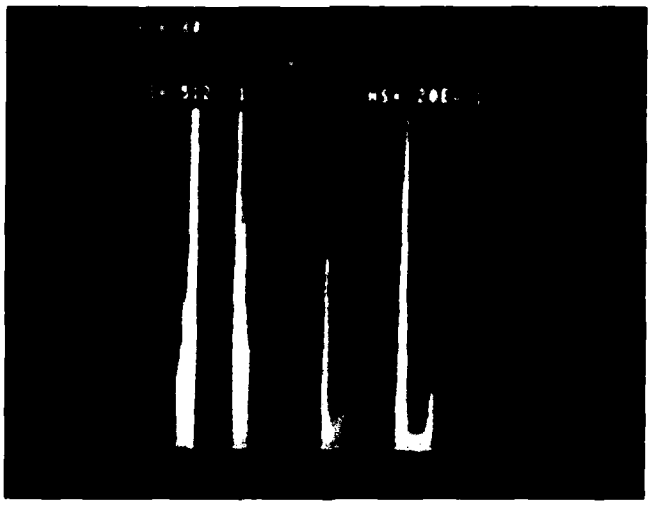


FIGURE 3. EDS SPECTRUM AND X-RAY LINE IDENTIFICATION

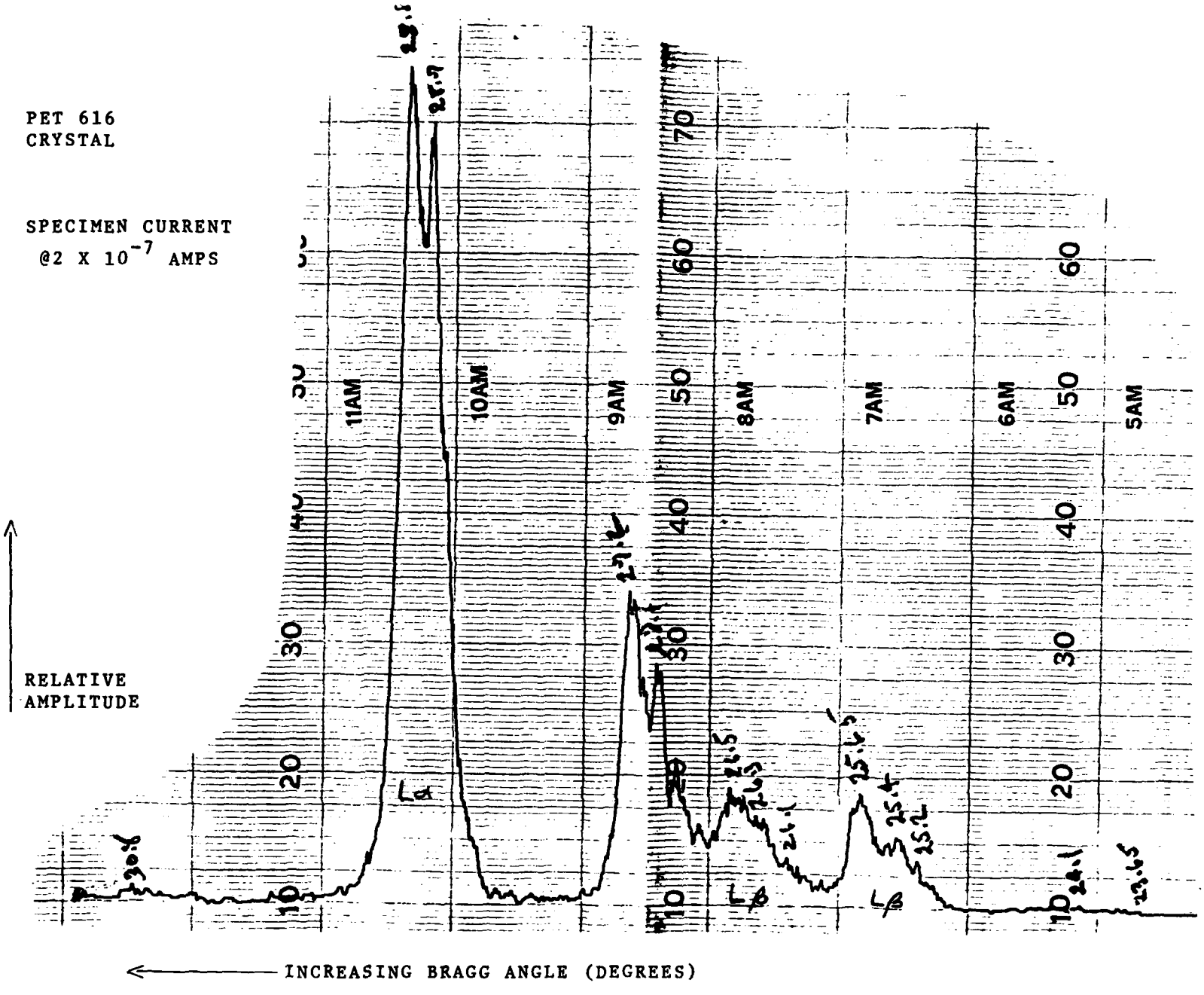


FIGURE 4. TYPICAL WDS SPECTRA SILVER STANDARD

For microelectronic failure analysis the solid-state or EDS systems are much more widely used, even though equipment costs are of the same order. EDS systems have two important disadvantages relative to WDS: poorer resolution of overlapping lines, and the inability to detect elements below fluorine without very restrictive windowless detectors. There are other important differences, particularly in research applications, and arguments about which system is "best" are futile. The two systems complement each other nicely and a dual installation on a SEM can be a very valuable solution if funds permit. Figure 5 is a SEM equipped with EDS and WDS systems.

5. Voltage-Dependent Contrast in the SEM. Voltage-dependent contrast in the SEM refers to a modulation of the secondary electron image by the electric field of the specimen. Information may be extracted in the form of a time- or voltage-varying image, or a waveform from selected points on the specimen.

The electric field to be analyzed is a complex resultant of several effects:

- The intentional applied operating voltage
- Charge injection by the SEM electron beam resulting in carrier injection into the active regions
- Stray fields impressed upon the specimen by charging insulators in the specimen package and in the SEM specimen chamber
- Topography variations of the specimen
- Accumulated charge in specimen oxide layers, the result of time-varying operating parameters (e.g., capacitor charging)

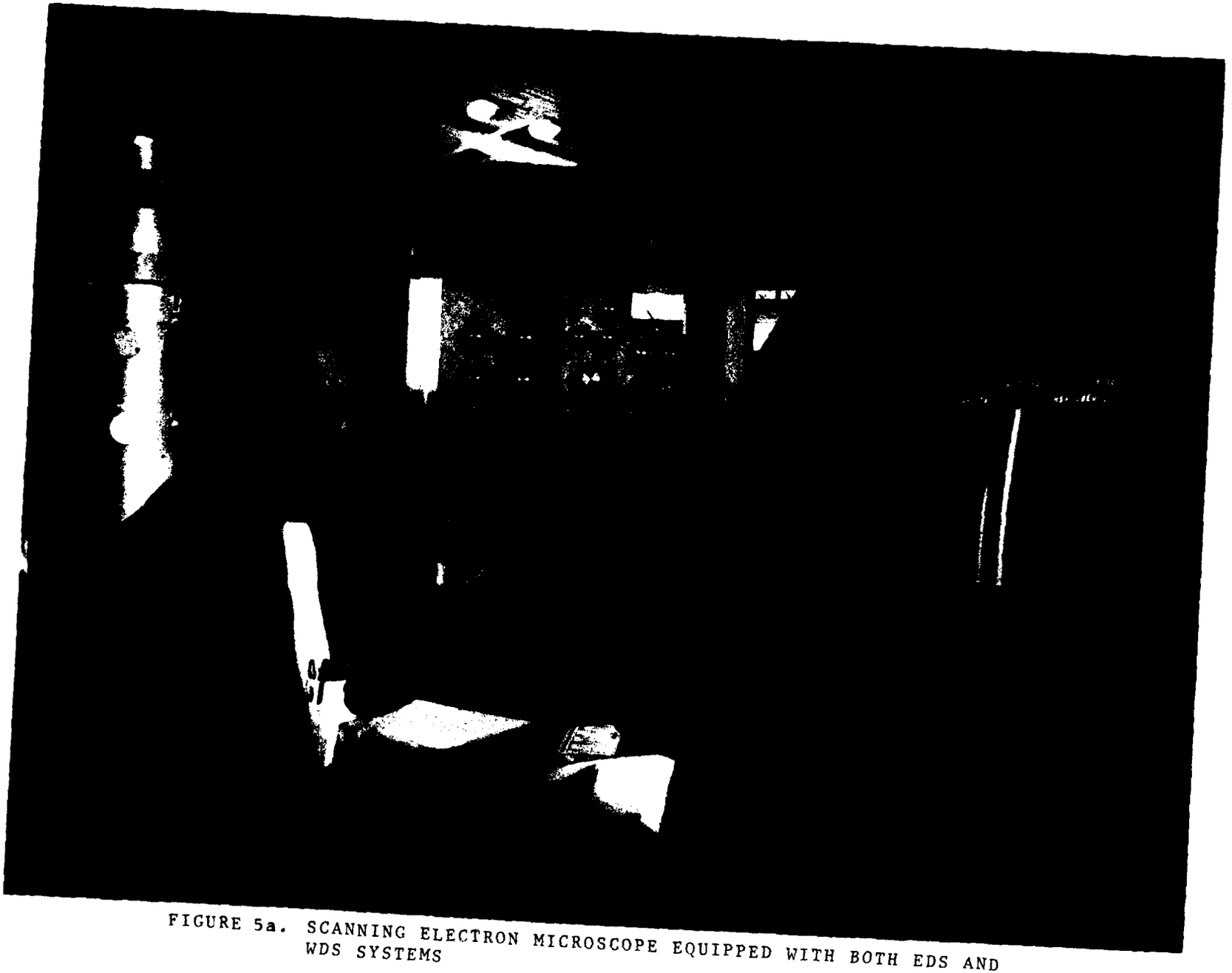


FIGURE 5a. SCANNING ELECTRON MICROSCOPE EQUIPPED WITH BOTH EDS AND WDS SYSTEMS

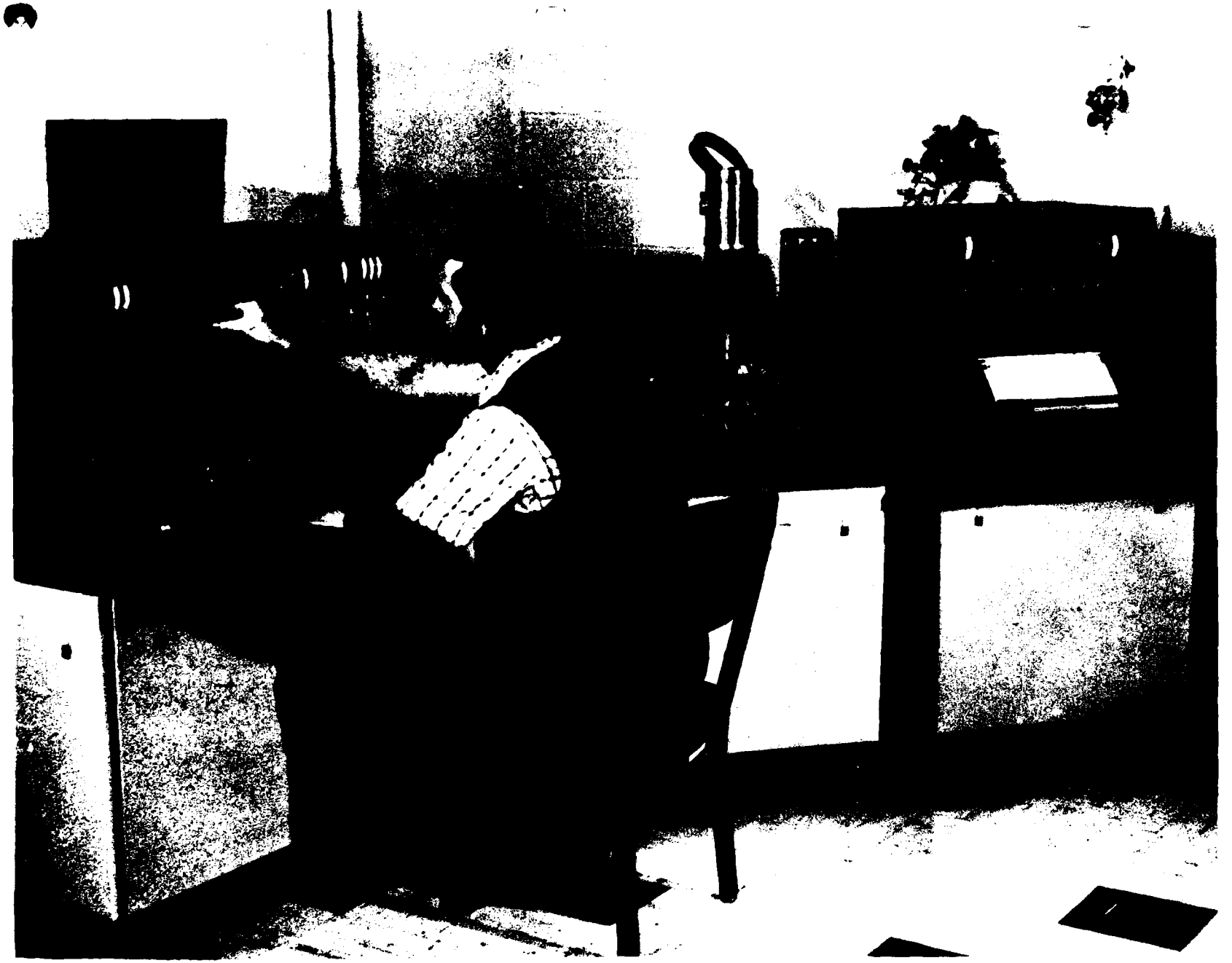


FIGURE 5b. SCANNING ELECTRON MICROSCOPE SYSTEM EQUIPPED WITH WDS SPECTROMETERS, RAPID SAMPLE EXCHANGE AIRLOCK AND ELECTRON BEAM MULTIPLE APERTURING CAPABILITY

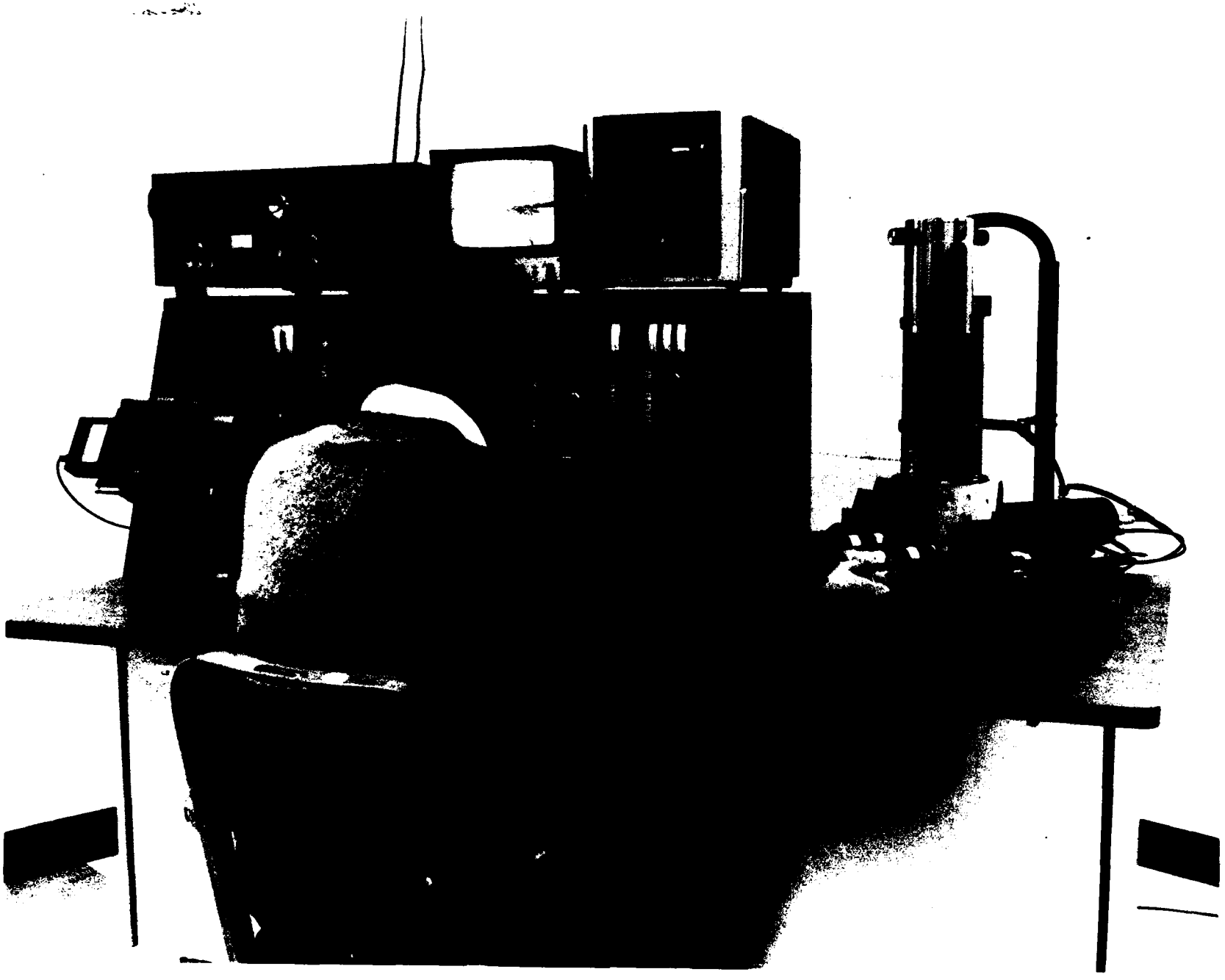


FIGURE 5c. SEM INCORPORATING (1) SCAN CONVERSION MEMORY SYSTEM AND (2) ELECTRICAL FEEDTHROUGH DEVICE EXCITATION, BEAM BLANKING AND TV SCAN RATES FOR VOLTAGE CONTRAST ANALYSIS.

- o Accumulated charge in specimen passivation layers resulting from non-unity secondary emission ratio during beam scanning

- o Voltage bleedover from adjacent bond wires

These effects may all have different relaxation times during time and voltage dependent exposure. Obviously, the total information content may be high in redundancy, irrelevance, and artifacts. This information must be sorted out and used to construct a hypothesis of the failure mechanism that fits the observed failure mode.

The pattern seen in most "voltage contrast" images is a superposition of topography, materials contrast, and voltage contrast. Some successes have been achieved in separating this information by computer processing, although the techniques and equipment are largely experimental at present. Although the microelectronic applications for the various "voltage imaging" techniques are expanding rapidly, there is little standardization in methodology or interpretation. Quantitative measurements are made with difficulty and are mostly done on special laboratory equipment. Nevertheless, operating images that compare good and bad devices can contain much easily recognized information not obtainable by other analytical methods.

6. Techniques.

a) DC Voltage Applied to Various Specimen Leads. This is the simplest method, which can reveal metallization defects and some forms of surface leakage. The contrast effects are usually transient because of surface charge rearrangement. It is limited to those areas of a circuit that are electrically accessible to DC.

b) Observation at Normal Specimen Operating Frequencies and Voltages. Secondary electron images observed under these conditions are difficult to interpret because of picture banding caused by frequency differences between scanning and operating cycles. Nevertheless, it is sometimes possible to localize and identify failure sites and nonoperation due to metallization opens by comparing failed and good units by means of video tape recordings. An example of multifrequency picture banding in a memory circuit is shown in Figure 6.

c) Stroboscopic Beam Scanning of Dynamically Operating Specimens. This technique permits visualization of the entire operating pattern of the device and is thus a very useful rapid screening method. The beam is gated by a beam-blanking accessory produced by most SEM manufacturers. Additional accessories needed are a signal generator triggered by the specimen clock pulses, and a dual-channel oscilloscope. SEM beam voltage must be less than 3 KV to avoid permanent changes in the specimen, particularly CMOS devices.

Signal-to-noise ratio is a basic limitation of the stroboscopic technique because of the shortened duty cycle or residence time of the beam on an element of specimen area. Maximum beam current is necessary, consistent with resolution and radiation damage limitations.

The basic advantage of stroboscopic operation is that it permits detection of time-varying voltage contrast as well as spatial variations. In addition, many failures are dynamic; that is, failure may occur only during a specific sequence of functions. Transient effects can be observed by synchronizing the specimen bias with the beam scanning period on certain specimen areas. Other techniques use time-varying signals that are not synchronized with raster scanning. Phase relationships between the applied dynamic voltages and the observed SEM signals can provide information on design failures by helping to trace the origins of potentials that appear at a given location. It is important to investigate such parameters in each type of application to avoid obscuring the effects being sought.

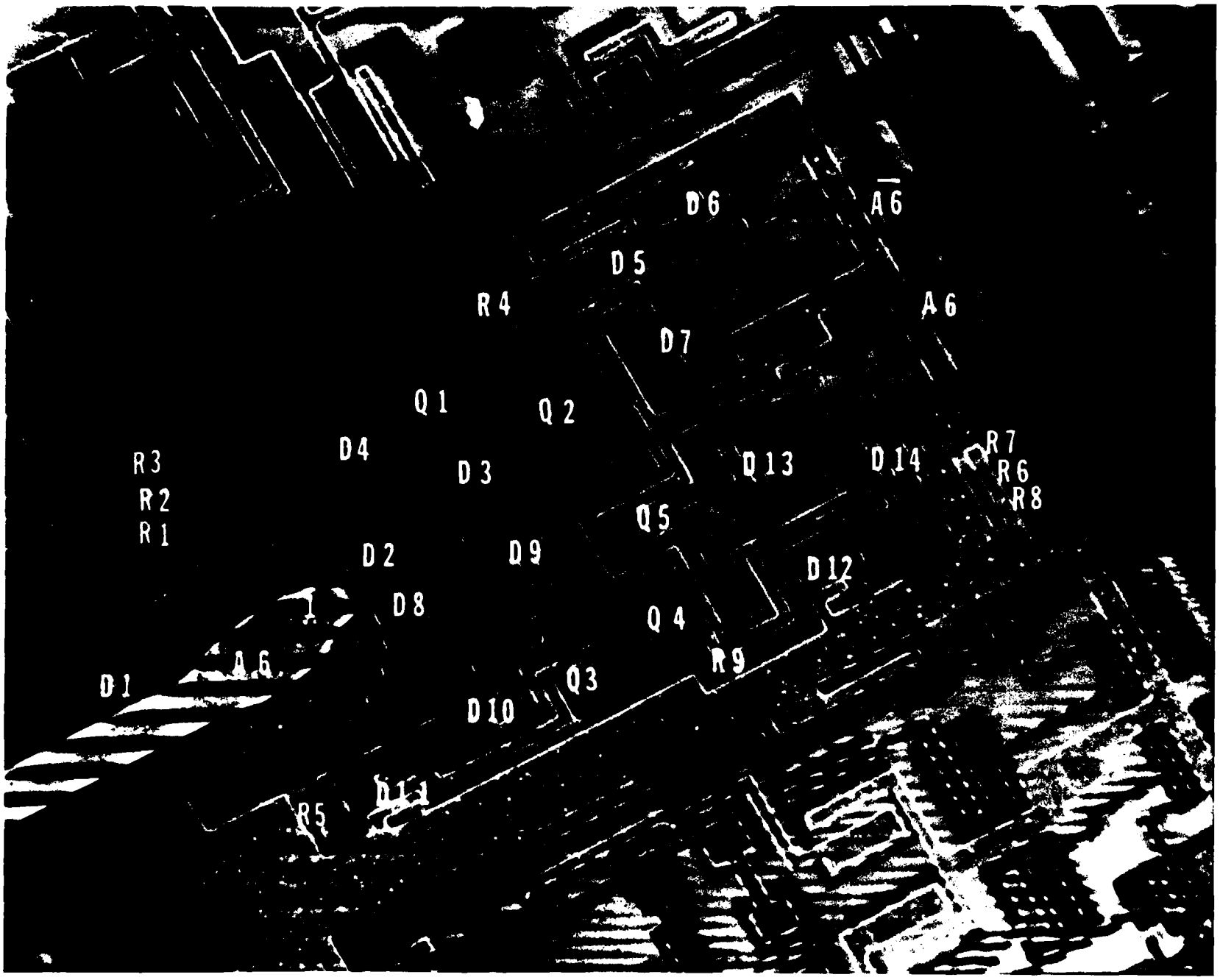


FIGURE 6. EXAMPLE OF PICTURE BANDING IN AN OPERATING CIRCUIT (BEALL MM)

d) Waveform Analysis at a Fixed Point. If the beam is left at a fixed point rather than scanned, a waveform is obtained from the secondary electron detector that varies with the dynamic waveshape of the input voltage. The beam may be pulsed (gated) in synchronism to vary the duty cycle and to observe phase relationships. Linearity problems preclude quantitative measurements without elaborate equipment modifications. With a stationary beam, radiation damage to the device is an important consideration.

e) Electron Beam-Induced Currents (EBIC). Instead of observing the secondary electron signal from the device surface, the image is formed by hole-electron pairs induced in the device by the SEM electron beam. The free carriers created in the depletion layer itself will be collected by the field inherent in the depletion layer. The holes will drift towards the p-type region, and the electrons will be pulled by the field towards the n-type region. This charge movement leads to current flow in an external circuit of the p-n junction. Information concerning the junction, such as depth, defects like diffusion spikes or pipes, can be obtained by this technique which cannot be obtained by other methods. The technique has been proven useful in detecting defects such as EDS damage, breakdown sites, and crystallographic defects. The depth of information depends on primary beam voltage. The device is usually scanned with the SEM beam. EBIC images can be obtained both in the biased and unbiased conditions.

The EBIC amplifier must have good bandwidth characteristics to allow reasonable scan times, such as the Model 427 current amplifier by Keithley Instruments.

An example of the usefulness of the EBIC mode of the SEM can be seen by viewing the secondary electron and electron beam induced images of a gate-drain junction region of a 2N3921 die (see Figure 7). In the upper photograph using the secondary electron image, no defect can be detected, but the EBIC image, with the gate to drain-

SE Micrograph Area (Evidence of a damage site is visible. Mag x 1500.)

a) SECONDARY ELECTRON IMAGE

EBIC Micrograph Showing Damage Site at Increased Magnification. (Same conditions as above. Mag x 1500.)

b) ELECTRON BEAM INDUCED CURRENT (EBIC) IMAGE

FIGURE 7. APPLICATION OF EBIC TO DEVICE FAILURE ANALYSIS

source junctions reverse biased at V_{GS}= -10 volts, reveals a damage site. The decreased EBIC current indicates a decreased carrier lifetime that is probably due to aluminum diffusion. This type of damage is characteristic of electrostatic discharge damage. Examination of the damage site by light microscopy and SE imaging failed to disclose any visible evidence of damage.

f) Miscellaneous Techniques. Various means have been used to enhance voltage contrast sensitivity by separating voltage information from the topographic signal. The methods include computer processing of the digitized signals, processing a difference signal with and without back bias, and various switching and subtraction techniques.

The properties of surface passivation can be evaluated by injecting carriers with the beam and simultaneously measuring surface inversion and lateral charge spreading. Ionic contamination and leakage sites can be identified and located. High sheet resistance of thin films can be measured by a similar technique.

7. Parameters to be Investigated. In order to evaluate various voltage contrast techniques as applied to specific microcircuits, the SEM operating parameters must be optimized with special attention to certain known limitations.

a) Beam Voltage. For surface voltage contrast, the beam voltage must be near the value for unity secondary electron emission ratio, which is about 870 volts for a typical microcircuit chip. Some SEMS may require circuit modifications to reach this value.

In some cases, surface charging can be avoided by penetrating the surface passivation to the underlying silicon. The ability to see meaningful surface voltage information is often a sensitive function of beam voltage, and this must be explored for

various types of microcircuits, especially bipolar devices which may be less sensitive to carriers induced by the beam. MOS device characteristics may be permanently altered by the beam, particularly above 3 kV.

b) Beam Current. Current must be explored with voltage because of its effect on tolerable duty cycle, signal/noise ratio, and radiation dosage particularly with MOS devices.

c) Specimen Chamber Conditions. The effects of shielding all surrounding insulators (including those in the specimen package) should be evaluated. If shielding is ineffective, coating unused insulators with conducting paint can help. It is important to standardize the electrical environment within the SEM for reproducible results when quantitative measurements are attempted.

d) Duration of Tests. Voltage contrast has, from experience, been found often to be transitory and volatile. The reasons include charging of nearby insulators, accumulation of charge in or on device passivation layers, charging of surface states at the Si/SiO_2 interface, "raster burn" of polymerized oil vapors within the SEM. Both beam exposure time and vacuum exposure time should be logged and standardized.

e) Surface Passivation. The types and thickness of surface passivation should be noted (e.g., oxide, nitride) as an aid in correlation with previous results. Thinning the passivation by etching may enhance the signal/noise, but such destructive tests should only be attempted if the failure mechanism is known. For example, etching may destroy impurity ions or introduce new ones.

f) SEM Detectors. The type of secondary electron detector can be a factor in the detection sensitivity. There may be trade-off advantages between light pipe/Farraday cages and silicon diode detectors. If so, these are relatively minor equipment modifications that would probably be acceptable to SEM users if significant advantages could be shown. The same remarks apply to the modulation of collector voltages: too much voltage will "wipe out" the small field variations that are sought on the specimen, while too little voltage will reduce detection sensitivity. In sophisticated systems energy analyzers or filters are effective, but they are not in general use.

8. Cathodoluminescence. Cathodoluminescence in microsites can be observed with relatively inexpensive accessories on the SEM. Its usefulness in microelectronics is at present limited primarily to compound semiconductors. This is perhaps the only temperature-dependent solid state phenomenon that can be directly observed in the SEM. A considerable body of literature relates to light emitting diodes but it has also been applied to GaAs Gunn devices.

9. Auger Electron Spectroscopy (AES). Auger electrons are low-energy electrons (20 to 2500 eV) that are ejected from a sample when it is scanned by an electron beam of up to 3000 volts. The energy spectrum is characteristic of the atomic number of the sample. The low energy of the Auger electrons limits their escape depth from the sample to only a few monolayers of the surface, just as in the case of secondary electrons used to form the image in a SEM. A shift in energy of Auger electrons can be interpreted in terms of local potential variations on devices.

Thus, Auger spectroscopy is a sensitive analyzer of elemental surface monolayers, particularly in the light-element range. It complements X-ray emission spectroscopy which has low sensitivity for light elements.

Since Auger spectrometry derives its information from the top monolayers, the samples must be analyzed in an ultra-high

vacuum - generally better than 10^{-9} Torr. Even so, carbon, oxygen, and nitrogen are nearly always found. It has become common practice to first sputter the surface with argon ions to reduce background. By sputtering and analyzing sequentially, a depth profile of composition can be obtained.

If an Auger spectrometer is attached to an ordinary SEM, carbon from backstreamed pump oil obscures other surface constituents. Some alleviation from pump oil carbonization has been achieved with special pump oils and cold wall specimen environments, but in general special ultra-high vacuum SEM construction is necessary and this is not commercially available at present. Instead, commercial Auger spectrometers have improved their scanning electron imaging capabilities: 500 Å spot size is presently available in at least one scanning system.

If a sample is examined in a conventional SEM, the hydrocarbon "raster burn" generated in the SEM will interfere with subsequent Auger analysis. Argon sputtering will remove this, but it may also remove the surface contaminants that one seeks. It is, therefore, important to perform Auger analysis first in this case and to forego other chemical preparation such as acid etching.

10. Sputtered Ion Mass Spectrometry (SIMS). Sputtering is the ejection of ions or neutral molucules when a surface is bombarded by energetic ions. The ejected particles may then be identified by mass analyzers. The original instruments were called ion microprobes and embodied both electrostatic and magnetic "double focusing" in order to resolve the large energy spread and overlapping lines of the ejected ions. This made it possible to obtain element and compound information both from the surface and from depth profiles. Sensitivity is extremely high; fractions of monolayers are easily detected. Spatial resolution of the SIMS is less than that of Auger spectroscopy and considerably less than X-ray emission spectroscopy in the SEM.

Recently, single focusing quadruple mass analyzers have been coupled to SEMs and Auger spectrometers. The single mass resolution is less than that of the double focusing ion microprobe, the cost is of the order of one tenth. Such instruments also can analyze the gases desorbed from surfaces by electron bombardment in the SEM.

Excellent review articles for ISS and SIMS are references 6 and 7 in the ISS, SIMS section of the bibliography on page III-P-41 and reference 6 in the Miscellaneous bibliography on page III-P-42 (reference entry #109 in the General Reference, page V-11).

11. Ion Scattering Spectrometry (ISS). In this ion beam technique, the bombarding beam is a monoenergetic noble gas ion beam of lower energy than is needed for sputtering. Instead of sputtering surface material off the specimen and mass-analyzing it as in SIMS, the energy lost by the low energy bombarding beam is measured in ISS. It has its greatest sensitivity in the higher atomic numbers and produces mostly elemental identification. It may be combined in the same instrument with a SIM's beam, both using a quadruple mass analyzer.

12. Electron Spectroscopy for Chemical Analysis (ESCA). ESCA is an analytical technique based on Einstein's photoelectric theory. It measures the energy of electrons ejected from a surface by a beam of X-rays or ultraviolet light. It is essentially nondestructive and can yield compound information on surface chemistry. The primary radiation was for a time limited to a spot size of about 2 millimeters, and thus it was thought that ESCA was unsuited for microanalysis. Then Hovland succeeded in generating a point source of X-rays by focusing a beam of electrons on the back of a thin metal foil. This technique was used at least thirty years previously in a commercial X-ray microscope. Although this point-source technique is not yet "commercial," it illustrates how rapidly evolving microbeam technology requires constant updating in our evaluations.

13. Other Microbeam Analysis Techniques.

a) Laser Microprobe Mass Analyzer. This instrument, termed "LAMMA," combines a laser microscope and a time-of-flight mass spectrometer. It combines spatial resolution of less than 1 micrometer, trace element sensitivity, and identification of nomogram quantities of organic materials.

b) Alpha-Induced X-ray Emission. This is a commercial instrument in which X-ray emission spectra are excited by alpha particles instead of an electron beam. Lower limits of detectability are claimed because of reduced bremsstrahlung background.

c) Automated Scanning Low Energy Electron Probe (ASLEEP). This technique (no commercial version available at this time) is to complement SEM and scanning Auger in imaging structural defects in silicon and III-V compound semiconductors.

d) Scanning Electron Stimulated Desorption (ESD). This technique mass-analyzes the relatively volatile surface contaminants (including water) that are desorbed by a relatively low energy Auger primary beam. It has been used in a combined Scanning Auger Microprobe (SAM) and Secondary Ion Mass Spectrometer (SIMS), but the technique should not be limited to this hardware. It should be useful in identifying many of the surface residue contaminants from process solvents, such as halogens.

e) Transmission Electron Microscopy (TEM). TEM requires either very thin specimens (a few micrometers at most) or carbon replicas which are time-consuming and difficult to prepare. The reward is the highest resolution of all beam instruments and fundamentally different contrast mechanisms.

In recent years hybridization has led to the Scanning Transmission Electron Microscope (STEM) and to SEMS temporarily converted to transmission imaging. The advantage is, besides

adding new contrast capability, the ability to perform Micro Area Scanning Transmission Electron Diffraction (MASTED) and micro-crystallographic analysis. In some cases diffraction information has been obtained on particles only 30 Å in dimensions. Because specialized electron optics are required to achieve best performance, commercial STEM instruments are optimized for maximum capability, but it is possible to obtain useful transmission results with relatively simple modifications to a conventional SEM.

f) Summary of Microbeam Analysis Applications. It is unfortunately impractical in most cases to attempt to reduce all aspects of failure analysis to detailed tabulated lists or to fault trees. Procedural strategy must be governed by the effects each step has on subsequent steps as well as on probabilities and cost. Failure mechanisms that formerly were only conjectures are rapidly becoming clarified through the judicious use of the newest analytical methods. Although failure analysis costs are rising, even the most exotic techniques may be very cheap compared with that of the downtime or loss of a major system. The analyst has a responsibility to preserve appropriateness in his procedures and avoid complexity in trivial problems, but results are often remembered after costs are forgotten.

We can summarize microbeam analysis techniques by association with some characteristic failure mechanisms that each can help to identify. Most of the microbeam techniques require skilled specialists for operation and interpretation of results, and these specialists are not always skilled in microelectronics failure problems. "Hybrid" individuals with experience in both camps are very desirable.

14. Some Typical Applications of the SEM.

a) General. The failure analyst should consider a number of other steps prior to analyzing a device with an SEM.

If the analyst has only a one-of-a-kind specimen, such as a single device that failed a major system, then the destructive nature of the various techniques must be considered. There can be no second guessing if the first analysis destroyed the sample. The question of analytical strategy is difficult to generalize, but a few comments may illustrate a useful way of thinking.

o Electrical testing to confirm failure should provide clues as to whether failure is catastrophic (opens or shorts) or whether degradation of parameters is the cause of trouble. If degradation is present, then step b) should be done (and possibly also even with catastrophic failure).

o If the device has a hermetic package (instead of plastic encapsulation) it probably should be helium leak-tested, and possibly gas-analyzed by mass spectrometer before delidding. Both of these procedures, if done with care, should not physically damage the chip or its leads.

o After delidding, the failure site should be sought by light microscopy. This will help to localize metallization abnormalities - corrosion, electromigration and physical damage.

o At this point the SEM is often employed to examine suspicious areas of surface topography. The various forms of voltage contrast can be very helpful in confirming the electrical failure site, particularly with LSI chips. Alternatively, the

liquid crystal techniques can be used to locate electrical failure. But here it becomes necessary to consider the effects of each technique as it may influence subsequent analyses. For example:

Most SEMs, even those with liquid nitrogen traps, will slowly deposit a "raster burn" comprised of polymerized vacuum pump oil vapor. Subsequent monolayer analytical techniques such as AES, ISS, SIMS will then see this carbon overlayer unless it is sputtered off.

A liquid nitrogen "cold finger" very close to the specimen will often alleviate this SEM problem. But sometimes voltage contrast searches may be quite prolonged and carbon will still be deposited. In this case, it may be necessary to choose in advance between a microsearch for the failure site versus a "shotgun" surface analysis.

If both AES and SEM are planned, AES should be done first since it is "cleaner." But suppose the electrical analysis leads to the suspicion that sodium contamination is present and causing electrical degradation. Sodium migrates so readily that it usually eludes electron beam analysis at room temperature. Cooling the specimen to about 110°K has been found to reduce mobility sufficiently to permit electron beam detection by EDX but at the expense of condensing greater amounts of pump oil. AES and SIMS have been shown to be effective in sodium analysis.

Sputtering techniques are, of course, destructive to the microstructure of surface morphology. A "clean" SEM is desirable to record surface features prior to sputtering, but the radiation damage and surface condensation associated with prolonged voltage contrast should again be considered.

Very thin films of organic contamination have led to bonding problems, and their detection and identification have always been very difficult. The SEM-EDX-WDX will see only carbon and even that with poor sensitivity. SIMS and ESCA are perhaps the best for this problem. ESCA is much less destructive but until recently has not been considered as a microanalysis tool. The simpler forms of SIMS have poor spatial resolution (large spot size), but the ion microprobe begins to approach useful resolutions. SAM has fair resolution (1 μm), but chemical bonding interpretation is in its infancy. Chemical identification of microareas of thin organic films remains one of the most difficult of all analytical problems, yet it is a relatively common problem in microcircuit fabrication and failure analysis.

A completely passive (nondestructive) analytical method is rare or nonexistent as dimensions become smaller and techniques more sensitive. An analytical strategy is necessary to avoid destroying a sample before the answer is obtained. It is less important if one has the luxury of many samples and can try each of the new techniques.

b) Loss of Package Seal Integrity. This condition may or may not be directly related to the device functional failure, but since leak testing or gas analysis cannot be performed retroactively after package opening, the leak site(s) should be located if possible. An external examination of the site in a SEM may disclose poor lead seals or lid attachment. This is a rapid and non-destructive examination compared with metallurgical cross sectioning and is often a good investment. If a lid solder seal leaks, an EDX element map may disclose lead-tin segregation or poor solder wetting. This is an example of a straightforward diagnosis that is relatively easy to perform in the SEM but considerably harder to confirm by classical methods.

c) Electrical Failure in the Chip. The sites of the failure must first be found. Probing combined with computerized function analysis may localize or even pinpoint the failure. If not, one of the electron beam methods may be needed (voltage contrast, EBIC, etc.). Before this is undertaken, the possible effects of the beam on the device should be carefully reviewed. For example, pump oil raster burn may not only quickly obscure failure observations but may also interfere with subsequent surface analysis. The injection of electrons by the beam may alter CMOS gate thresholds, or decrease the gain in bipolar devices, or increase surface leakage (see especially Ref. 6, III-P-41). These effects can be minimized by low beam voltages and good vacuum practice (clean, well-trapped systems) and by trial runs and rehearsals with good devices. In general, a failed device should be treated with great care because the information it contains may be fragile and volatile, and preliminary conclusions may not be confirmable.

d) Wire Bonding Problems. Early problems with gold-aluminum wire bonds usually centered around excessive formations of gold-aluminum intermetallic compounds ("purple plague") or aluminum corrosion concentrated on bonding pads by halogen contaminants held by liquid surface tension at some stage in manufacturing. Both of these problems were originally elucidated by the SEM microprobe instruments.

Other wire bonding problems, however, have not yielded so easily and some of them are beyond reach of the SEM microprobe. Typical examples are incompletely removed silicon oxides and nitrides on the bonding pads and insoluble polymer residues from manufacturing processes.

Auger analysis can give a good indication of oxides and nitrides by elemental identification, and progress has been reported in detecting peak shifts due to chemical bonding. Auger analysis of polymer residues would mainly yield carbon peaks.

ESCA would yield more information on the polymer composition, and since it is nondestructive it could be followed by SIMS or Auger to confirm the existence of oxides or nitrides. However, if Auger analysis were performed first, it may have partly volatilized any polymer layers because of its high energy beam (or if sputtering were used). A careful light microscope examination preceding all these methods is advisable to search for coloration or other indications of refractive index information.

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Founded: 1878. **Members:** 855. Professional society of microscopical biologists and microscopists. To foster biological research which employs the microscope and to publish results of microscopical research in all branches of learning. **Committees:** Reprinting Back Numbers; 80-Year Index. **Publications:** Transactions of the AMS, quarterly. **Convention/ Meeting:** annual.

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Founded: 1942. **Members:** 2500. **Local Groups:** 20. Persons interested in the electron microscope, including medical, biological, metallurgical, and polymer research scientists and technicians, as well as physicists interested in instrument design and improvement. Seeks to increase and diffuse knowledge of electron microscopes and related instruments and results obtained through their use. Maintains traveling scientific exhibit. Presents annual scholarships to graduate students. Also presents other awards for outstanding scientific contributions, including Burton Award to scientist under 35 years of age. **Committees:** Educational Radiation Safety. **Publications:** (1) Bulletin, 3/year; (2) Directory, annual; (3) Proceedings of Annual Meeting; also publishes Handbook of X-ray Safety for Electron Microscopists, 1973. **Affiliated with:** American Association for the Advancement of Science; American Institute of Physics. **Formerly:** (1964) Electron Microscope Society of America. **Convention/ Meeting:** annual - always August. 1979 San Antonio, TX; 1980 San Francisco, CA; 1981 Atlanta, GA; 1982 Washington, DC.

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Founded: 1967. **Members:** 700. Persons or businesses who are interested in electron beam microprobe analysis, scanning electron microscopy, and other uses of electron and ion probes and surface analysis techniques. **Publications:** (1) Micronews, 4/year; (2) Abstracts, annual. **Formerly:** Electron Probe Analysis Society of America. **Convention/ Meeting:** annual - 1979 August, San Antonio, TX; 1980 San Francisco, CA; 1981 August, Atlanta, GA, 1982 Washington, DC.

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Founded: 1868. **Members:** 200. Goal is to promote the proper use of the microscope and the advancement of applied and theoretical microscopy with emphasis on all phases of microscopy, including electron microscopy and advanced special instrumentation. Seeks to provide a forum for the dissemination of information by holding lectures, courses, exhibits, field trips and workshops. Keeps informed about, and encourages development of new instruments and techniques. Maintains archives of historical instruments, literature and work. Sponsors three "Young Peoples Courses" each year. Bestows annual award for outstanding work in the field. **Committees:** Education. **Publications:** Micro Notes II, monthly. **Convention/ Meeting:** annual - always June.

Q.

ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE EFFECTS AND FAILURE ANALYSIS TECHNIQUES

Q. ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE EFFECTS AND FAILURE ANALYSIS TECHNIQUES

1. Introduction. One of the most common causes of catastrophic or parametric failures of microelectronic devices is damage resulting from electrical overstress (EOS), which may occur from device manufacture through system test, deployment and operation. The most obvious form of EOS is the inadvertent application of a relatively continuous power source to a device without sufficient current or voltage limiting to prevent the absolute maximum ratings of either power, current or voltage from being exceeded. This EOS type frequently occurs as a secondary failure event resulting from a primary failure of some other microelectronic device or from a test or procedural error (such as cable reversals). There are some designs such that when individual or known parts fail, other parts are electrically overstressed. After field equipment has been serviced for any length of time, field service personnel learn that when specific parts fail certain other parts should be removed and replaced as preventive maintenance to prevent repeated repair actions. For this reason, where practical, a circuit analysis should be conducted and corrective action implemented for eliminating latent secondary failures as part of the failure investigation associated with any primary failure (see Reference 1).

There is another type of EOS failure which occurs from natural and man-made electrical and electromagnetic environmental stresses in which ostensibly the equipment was designed to function. This is the transient EOS with durations ranging from nanoseconds to hundreds of microseconds. Only rarely do microelectronic device specifications identify maximum transient tolerance and none specify transient tolerance levels over the entire transient pulse time domain. The susceptibility of microelectronic

devices to transients (especially bipolar integrated circuits to ESD) has emerged as an overlooked aspect of new designs which cause exorbitant life cycle cost in military applications and financial losses from product failure in commercial applications. It is therefore important that the failure analyst identify transient EOS failures when they occur and notify the users to control the use environment and/or the designers to improve the device and/or equipment design to harden it against transient EOS.

2. Sources and Nature of Transient EOS. The designer's goal should be to nullify the effect from all sources of transient EOS. Transient EOS is defined as any brief electrical or electromagnetic phenomenon, either natural or human induced, which causes degradation of the performance of electrical or electronic parts (see Reference 2).

a) Natural Electrical and Electromagnetic Environmental Stresses. Natural sources of transients are from electrostatic discharge (ESD). Lightning is the most formidable ESD, so much so that there is a technical community involved in lightning protection studies. Since 1974, annual Grounding and Lightning Technology Workshops have been held, jointly sponsored by FAA, NASA, the Florida Institute of Technology and Georgia Institute of Technology. When equipment experiences direct or near-miss lightning strikes, the power surge channel or the electromagnetic radiation can induce electrical transients in equipment cables (see Reference 3).

The most frequently occurring, least noticeable, and most ignored ESD are discharges from human bodies where the potential is too small to feel or hear (< 2500V) but when passed directly through sensitive electronic equipment and

microelectronic devices transient EOS failures occur. Parts, equipment and cables, especially tranmission lines, can become electrified (i.e., build up static charges) during periods of isolation from ground by (1) induction from nearby fields or by (2) contact and separation charging/triboelectrification and less frequently by (3) corona charging (contact with a highly charged object). Sudden movements and/or capacitance decreasing changes in orientation while electrified and with pins floating can produce very subtle transient EOS in highly sensitive microelectronic devices. This phenomenon can occur while the parts, assemblies or equipment are in plain polyethylene packaging material. Rapid discharges by connecting charged cables or by connecting charged parts and equipment to ground will produce subtle transient EOS that is usually neither seen nor heard, but sufficient energy and/or voltage is available to cause degradation or even catastrophic failures (see Reference 4). Recently, a technical community has developed around the EOS/ESD Symposium with the common goal to prevent failures from this subtle ESD phenomenon (see II-H).

b) Man-made Electrical and Electromagnetic Environmental Stresses. Sources of man-made transient EOS can be grouped by the following classifications:

- o Inadvertent equipment-generated transients
- o Electromagnetic radiation (EMR) signals
- o Electromagnetic pulse (EMP)

Sources of inadvertent equipment-generated transients are varied and complex and include everything from equipment switching transients to radiated and conducted emissions from a wide variety of sources (see References 2 and 5). Table III-Q-1 is a listing of some of the potential sources of inadvertent equipment-generated transients.

TABLE III-Q-1: POTENTIAL SOURCES OF INADVERTENT EQUIPMENT-GENERATED TRANSIENTS

Susceptibility Process	Source Identification
Direct Injection from Internal or External Power, Control and Signal Lines	o Switching (mechanical and solid state) of reactive loads; opening and closing of switches and relays o Fuse and circuit breaker interruptions and resettings/current inrush o Generator and motor operation (overspeed and hunting, start-up, control and shutdown)
Coupling of Radiated Magnetic, or Electric or Electromagnetic Field	o All of the above o Cable radiated emissions o Equipment radiated emissions o Flourescent lights o Ignition system, arc welder, particle precipitation operation
Coupling of Conducted Noise and Interference	o All of the above o Reflected waves

Many of these sources are repetitive and/or predictable and therefore are source identifiable. For example, switching of known reactive loads, energizing and deenergizing transformers, and control of industrial dc motors generate high level transients that fall into the source identifiable category. But transients on power and signal lines are virtually impossible to predict, and prudent damage analysis is necessary to establish a basis for device protection levels.

A common source of transient EOS especially in UHF receivers is high power electromagnetic radiation (EMR) signals incident upon the antenna which causes damage to the semiconductor components in the RF stage (see References 6, 7 and 8). Radar systems generate two distinct types of RF pulses:

- o Short pulses with $\leq$ 50ns pulse widths from high-power systems.
- o Longer pulses with pulse widths greater than 100ns to CW signals from low to medium power radar systems

Intense EMR incident upon equipment can shine (radiate) through and be conducted directly into the sensitive microelectronic devices. The term RF pulse refers here to a pulse-amplitude modulated RF carrier.

EMP of concern in military equipment stems from nuclear detonation (see References 2, 9 and 10). Large chemical explosions might also be a source of EMP. Nuclear EMP is particularly severe from high (200 km or more) detonation altitudes above the earth because of the extensive surface area that is exposed to the intense fields. Nuclear EMP and lightning have similar transient EOS characteristics.

c) Waveforms and Parameter Values. The basic waveforms of transient EOS are shown in Figure III-Q-1. The double exponential (Figure III-Q-1a) is characterized by the following parameters:

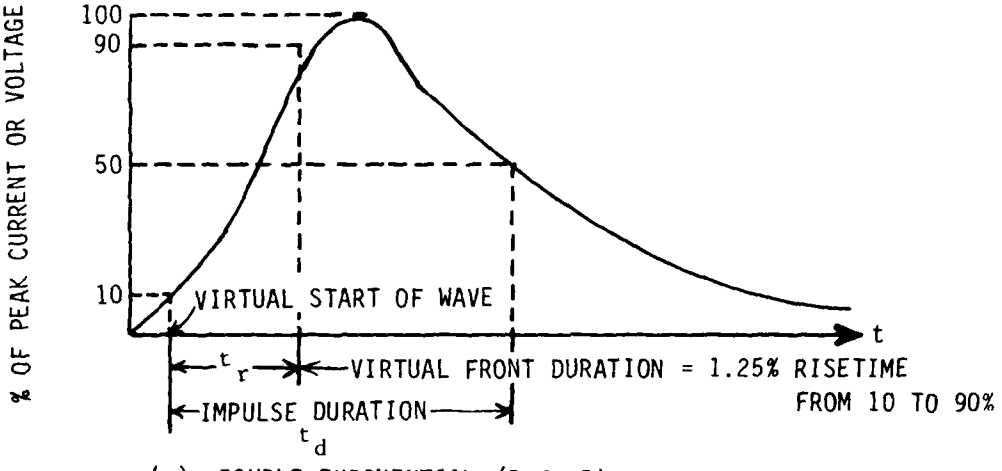
- Amplitude (A_p; V_p or I_p) - the peak voltage or current reached by the pulse
- Rise time (t_r) - standard 10% to 90% interval of peak current or voltage
- Duration (t_d) - time measured from initial impulse to the peak amplitude decayed to 50% or from peak amplitude to 50% decayed which is the definition used for t_d on Table III-Q-2
- Decay time constant - the time for the pulse amplitude to decrease 1/e of its peak value

The double exponential derivative (Figure III-Q-1b) has an additional parameter:

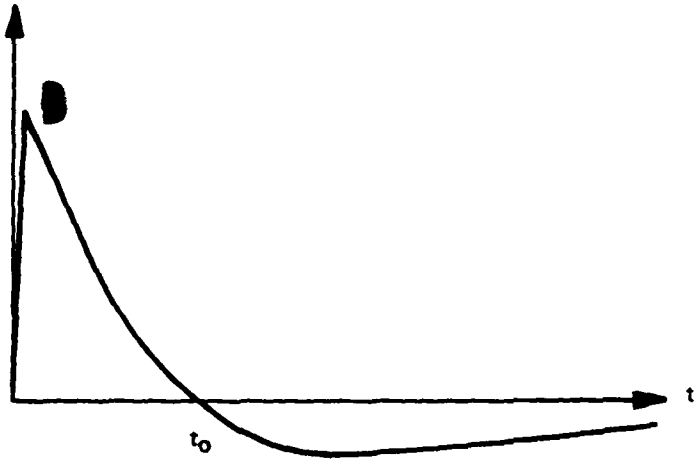
- Zero crossover time (t_0) - from peak pulse amplitude until the waveform crosses zero.

The damped sinusoid (Figure III-Q-1c) parameters needed are the frequency and the damping function.

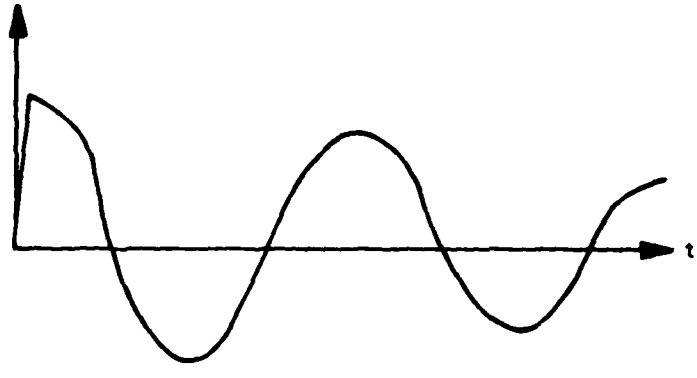
Although magnitudes and shapes of transient EOS vary widely, Table III-Q-2 represents some typical values for some of the most common sources of transient EOS.



(a) DOUBLE EXPONENTIAL (Ref. 5)



(b) DOUBLE EXPONENTIAL DERIVATIVE (Ref. 3)



V or I = A(t) SIN ($\omega t+\theta$)

WHERE A(t) IS A FUNCTION DECREASING IN TIME

(c) DAMPED SINUSOID (Ref. 3 and 10)

FIGURE III-Q-1 BASIC WAVEFORMS OF TRANSIENT EOS

TABLE III-Q-2

TYPICAL TRANSIENT MAGNITUDES AND WAVEFORMS/SHAPES

SOURCE	SUSCEPTIBILITY MODE	WAVE SHAPE	PARAMETER VALUES	REFERENCE
Human ESD	Fingertip direct injection	Double exponential	$t_r \leq 10ns$ $t_d = 150ns$ for RC equivalent $R = 1500\Omega$ $C = 100pf$ Carpets: $V_{CAP} = 12,000V$ $I_p = 8$ amps Vinyl Tile: $V_{CAP} = 4,000V$ $I_p = 2.67$ amps	(11, 12)
	Enhanced field (hand-held metal tool) direct injection	Double exponential	$t_r \leq 10ns$ $t_d = 50ns$ for RC equivalent $R = 550\Omega$ $C = 100$ pf Carpets: $V_{CAP} = 12,000V$ $I_p = 22$ amps Vinyl Tile: $V_{CAP} = 4,000V$ $I_p = 7.3$ amps	(12, 13, 14)
	o EMR shine-through o Conducted discharge causing radiated magnetic, electric or electromagnetic field	Damped sinusoid	Transmission and coupling efficiency depends on equipment structures - no clearly defined values	(12, 15, 16)
Device ESD or Assembly ESD	Contact with ground	Double exponential derivative or damped sinusoid	$t_r \leq 0.5ns$ $t_o = 1ns$ for RLC equivalent $R = 10\Omega$ $L = 10nH$ $C = 3.6pf$ (18 pin DIP) $V_{device} = 1000V$ $I_p = 15$ amps	(4, 17)

TABLE III-Q-2 (Cont'd)

TYPICAL TRANSIENT MAGNITUDES AND WAVEFORMS/SHAPES

SOURCE	SUSCEPTIBILITY MODE	WAVE SHAPE	PARAMETER VALUES	REFERENCE
Lightning	Channel current flowing in structure or EMR from return stroke	Double exponential (Figure III-Q-1a)	Older version (slow rise): t_r = 710 to 1070 nsec t_d = 38 to 58 µsec New version (fast rise): t_r = 44 to 60 nsec t_d = 40 to 60 µsec Amplitude is cable and/or system dependent with 20,000 amps considered in the upper range	(3, 17)
	Coupled magnetic field when load impedances are high and cable lengths short	Double exponential derivative (Figure III-Q-1b)	t_r = 100nsec max t_o = 1.6 to 2.4 µsec Source impedance = 5Ω Amplitude = 50V to 1600V (peak)	(3, 17)
	Coupled EMR when cable lengths are long	Damped sinusoid (Figure III-Q-c)	Older version (slow rise): f = 0.8 to 1.2 mHz t_r = 50 nsec max Source impedance = 20Ω Amplitude = 100V to 3200V (peak) Newer version (faster rise): f = 8 to 12 mHz t_r = 5nsec max Source impedance = 20Ω Amplitude = 100V to 3200V (peak)	(3)
Equipment generated	Direct injection	Double exponential derivative (Figure III-Q-1b)	t_r < 5µsec t_o = 10 µsec Source impedance = 100Ω Amplitude = 5V to 300V	(11)
	o Coupling of radiated magnetic, electric or electromagnetic field o Coupling of conducted noise and interference	Damped sinusoid (Figure III-Q-1c)	Transmission and coupling efficiency depends on equipment structure (See Table III-Q-3 for frequency spectrum)	(2)

TABLE III-Q-2 (Cont'd)

TYPICAL TRANSIENT MAGNITUDES AND WAVEFORMS/SHAPES

SOURCE	SUSCEPTIBILITY MODE	WAVE SHAPE	PARAMETER VALUES	REFERENCE
EMR signals (Radar)	Coupling of EMR	RF pulse	o short pulses < 50ns o long pulse > 100ns to CW f = 50kHz to 400 mHz	(6, 7, 8)
EMP	Coupling of EMR	Damped sinusoid (Figure III-Q-1c)	A = 500V to 1000V f = 0.01 to 50 mHz Source impedance = 100Ω I_p = 0.1A to 1000A	(2, 9, 10, 18)

TABLE III-Q-3

CONDUCTED AND RADIATED TRANSIENT SPECTRUM
(REFERENCE 2)

Conducted Emissions on Powerlines, Control and Signal Leads	30Hz - 50mHz
Radiated Emissions from Equipment and Cables	14kHz - 10GHz
Conducted Susceptibility - Noise on Power Lines	
Audio	30Hz - 50kHz
RF	50kHz - 400mHz
Transient	10µsec pulse (1 µsec rise time)
Conducted Susceptibility - Interference of Receivers	
Cross and Intermodulation	30Hz - 10GHz
Signal Rejection	30Hz - 10GHz
Radiated Susceptibility	
Magnetic Field	Steady State 400Hz Transient Broadband
Electric Field	100kHz - 40GHz

3. EOS/ESD Effects

a) General. The EOS from a relatively continuous power source will cause severe destruction of the device, i.e., lead wires will burn open; chip metalization will be evaporated; the semiconductor doped Si junctions on the chip will degrade or in some cases become totally destroyed due to melting and recrystallization. Circuit analysis should be performed to determine if a transient EOS could have caused an initial degradation condition leading to a subsequent sequence of events causing greater destruction of the device, (e.g., ESD caused degradation followed by equipment turn-on and subsequent hard failure). Otherwise the true cause of the failure will be unknown.

It is also possible that the failed device is exceptionally sensitive to successive degradation from multiple exposures to transient EOS. Figure III-Q-2 illustrates this concept of accumulative damage.

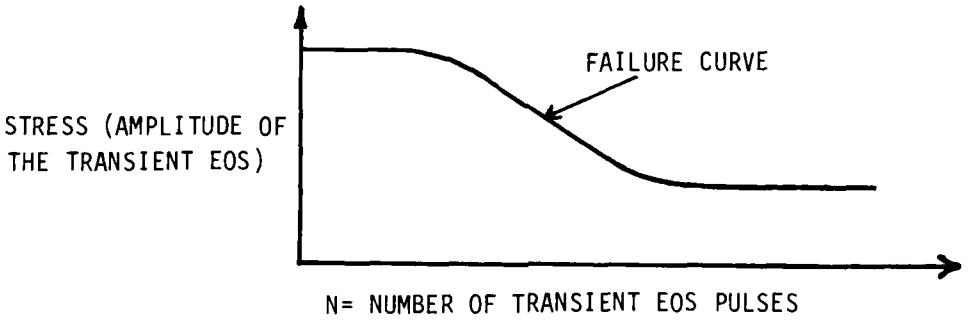


FIGURE III-Q-2 S-N CURVE FOR TRANSIENT EOS PULSES

Equivalent device physical damage may result from either a single large amplitude transient or from repetitive smaller amplitude transients. Another compound failure sequence is that from a latent failure where a critical transient EOS degradation level in the device application is reached (e.g., high power supply drain current), without causing a malfunction, but subsequent operating stresses of the circuit application cause the degradation process to continue or another failure process (e.g., electro-migration), to develop until a malfunction occurs (e.g., metalization stripe developes an open circuit).

Transients may also cause upset (data loss) or logic errors (stuck at) that may not cause any permanent device damage such that equipment turn-off and resetting is all that is necessary. In some designs a transient of insufficient amplitude by itself to cause damage can generate failures by placing the equipment into an operating mode that in turn causes EOS and permanent damage. SCR "latch-up" in microcircuit structures, i.e., the creation of a low resistance path between power supply and ground during an electrical pulse, and runaway oscillators are examples of this failure process.

b) Common Electrically Overstressed Part Structures. As bipolar devices preceded the development of MOS devices, EOS effects studies in the mid '60's were related to junction shorts. The second breakdown mechanism was extensively studied. Schafft (Reference 20) in 1967 published a comprehensive survey which summarized and critically reviewed the theories presented at the time. As the '70's arrived, researchers such as Wunsch and Bell (Reference 21), Budenstein (Reference 22), Sunshine and Lambert (Reference 23), Smith (References 24 and 25) and Domingos (Reference 26) delineated the dependence of junction EOS shorts on the pulse time domain, thermal behavior, geometry and doping level. Figure III-Q-3 is a

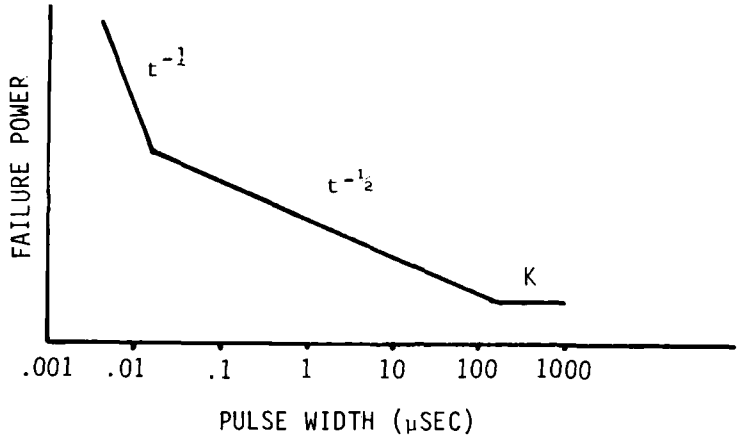


FIGURE III-Q-3

plot illustrating three regions which have been modeled for predicting damage threshold power (or energy) for semiconductor junctions. For very short pulse times where large currents are required to reach failure temperature, the bulk device is heated approximately adiabatically and the failure power approaches a dependence of t^{-1} (i.e., constant energy). For continuous operation the failure power approaches a constant (K) while in the region where thermal gradients are forming due to some heat loss a time dependence of $t^{-\frac{1}{2}}$ has been an accepted model. These models are all related to a thermal dependent process.

The reverse biased breakdown process is more of a growth process in the sense that the longer the transient, the more developed the short. The short starts at the junction, grows toward the base (high resistivity material) contact and then grows toward the emitter contact at which time total second breakdown occurs. If pulse widths are longer than 50 μsec, Lane (Reference 27) found aluminum contact metalization will start to migrate through the short. DeChiaro (Reference 28) has found that aluminum will move through the short by a process termed electro-thermal migration (ETM) with multiple exposures of transients less

than 1.0 μsecs. Thus, the challenge is to determine if shorts with aluminum in them are the result of one long transient as might come from an equipment-generated transient or from multiple exposures to ESD as might come from improper packaging or handling. In both cases researchers (References 24, 27 & 28) have found the distance between the metalization contacts is a major factor in determining the transient EOS sensitivity of the structure. Smith (Reference 25) also found that the contact sintering process variation could have a pronounced effect on the junction susceptibility to shorts.

Metalization, thin film resistor and flying lead wire burn-out are other classifications besides junctions which are affected by transient EOS. The failure models for these structures are dependent upon current density and time. The thermal conductivity of the substrate or glassivation can influence the failure process on metalization and thin film resistors. Being colocated to other heat generating structures will also influence the failure process as Smith (Reference 24) identified on long metalizition strips melting open and forming a puddle where the metal crossed over heat-generating diffused resistors. Smith classified this as "heat sinking metalization burnout" while calling the other "current conduction burnout."

Flying lead wires can only conduct appreciable amounts of heat through the bonding pads which means the middle of the wire will be the hottest. Thus the flying lead wire which has no nicks should burn out in the middle of the span between the bonding pads. Models and useful prediction equations for metalization and flying lead wire failure have been given by Smith (Reference 29) and Wunsch (Reference 30).

All the structures affected by transient EOS discussed to this point have been affected by the thermal overstress as a result of the electrical overstress. The MOS structure with a low breakdown gate oxide is more voltage sensitive. The failure process is dielectric breakdown when the transient voltage creates a field greater than the dielectric strength of the gate oxide. Unlike junction shorts the dielectric breakdown of gate dielectrics has not been an extensively studied failure process. Yang, Johnson and Lambert (Reference 31) identified some of the visual effects of dielectric breakdown from hot electron conduction producing different effects depending on polarity and substrate silicon dopant type (P or N). More recent researchers Li, Maserjian and Prussin (Reference 32) have introduced a field-time-dependent breakdown for MOS devices which holds for the field encountered below the dielectric strength of the oxide. The challenge is to identify the failure as transient EOS activated or oxide defect activated from the field strengths of normal operation. It is further a challenge to distinguish between a transient EOS dominant failure and a pinhole dominant failure.

c) Part Structures Susceptible to ESD. Different parts are susceptible to ESD in various degrees. These variations are due to different part designs and different structures that go into making the part. Table III-Q-4 is a summary of structures that are incorporated into various parts which are sensitive to ESD. Table III-Q-4 also lists the part types in which some of these structures are found and the associated failure processes involved.

o MOS Structures. A MOS structure is a conductor and a semiconductor substrate separated by a thin dielectric. Thus the acronym MOS for metal-oxide-semiconductor is

TABLE III-Q-4

PART STRUCTURES SUSCEPTIBLE TO ESD

PART STRUCTURE	PART TYPE	FAILURE MECHANISM	FAILURE INDICATOR
MOS Structures	o MOS FET (Discrete) o MOS ICs o Semiconductors with metalization cross-overs Digital ICs (Bipolar and MOS) Linear ICs (Bipolar and MOS) o MOS Capacitors Hybrids Linear ICs	o Dielectric breakdown from excess voltage and subsequent high current (Reference 35)	o Short (high leakage)
Semiconductor Junctions	o Diodes (PN, PIN, Schottky) o Transistors, Bipolar o Junction Field Effect Transistors o Thyristors o Bipolar ICs, Digital and Linear o Parasitic Transistors and Input Protection Circuits on: Discrete MOS FETs MOS ICs	o Microdiffusion from microplasma-secondary breakdown from excess energy or heat (References 20, 22 24, 25, 26) o Current filament growth by silicon and aluminum diffusion (electro-thermomigration References 28 and 33)	o Short (high leakage)
Film Resistors	o Hybrid ICs Thick Film Resistors Thin Film Resistors o Monolithic IC-Thin Film Resistors o Encapsulated Film Resistors	o Dielectric breakdown, voltage dependent-creation of new current paths (References 36 and 37) o Joule heating-energy dependent-destruction of minute current paths	o Resistance shift o Open (extremely thin films)
Metalization Strips	o Hybrid ICs o Monolithic ICs o Multiple Finger Overlay Transistors	o Joule heating-energy dependent metalization burnout (References 24 and 25)	o Open
Piezoelectric Crystals	o Crystal Oscillators o Surface Acoustic Wave Devices	o Crystal fracture from mechanical forces when excessive voltage is applied (Reference 34)	o Operational degradation
Closely Spaced Electrodes	o Surface Acoustic Wave Devices o Thin metal unpassivated, unprotected semiconductors and microcircuits	o Arc discharge melting and fusing of electrode metal (Reference 34)	o Operational degradation

derived. A more general acronym for this structure is MIS for metal-insulator-semiconductor. Dual dielectric systems such as MNOS (metal-nitride-oxide-semiconductor) are included in this susceptible structure classification.

- Part Types. Integrated circuit MOS technologies are NMOS (N-channel MOS), PMOS (P-channel MOS) and CMOS (Complementary MOS). Variations on these technologies are metal gate, silicon gate and silicon on sapphire (SOS technology). Differences in the susceptibility of these MOS technologies are dependent on the oxide or oxide-nitride gate dielectric breakdown and input protection circuitry to the external connections. The breakdown of the gate dielectric is mostly dependent on its thickness. Typically this has been 1100Å and with a dielectric strength ranging from 1×10^6 volts per centimeter (V/cm) to 1×10^7 V/cm. This results in breakdowns between 80 and 100 volts. Newer technology variations, however, like HMOS (high density MOS) which have thinner gate dielectric have much lower breakdowns (25 to 80V) and therefore require more care in the design of the input protection circuitry.

Certain bipolar linear integrated circuit operational amplifiers incorporate capacitors on their monolithic chip. These capacitors are MOS structures and are susceptible to dielectric breakdown from ESD. Those operational amplifiers such as the 741 whose capacitors do not have apparent direct contact to external pins are less vulnerable than parts such as the HA2520 whose capacitors are placed directly across an external pin combination.

Hybrid circuits can incorporate a chip capacitor which is a MOS structure with a dielectric vulnerable to ESD. MOS chip capacitors have the advantage of size and ease of attachment but the disadvantage of being highly susceptible to EOS should not be ignored.

Many monolithic integrated circuits have metalization runs which cross over active semiconductor regions or low resistivity semiconductor regions with field oxide between them serving as the insulator. These are sometimes referred to as parasitic MOS transistors. Typically field oxide is 15,000Å thick with breakdowns around 1,000 volts, but when oxide is etched away for diffusion, subsequent regrowth of oxide before metalization may be less than 3,000Å. In this case, breakdown could occur at 100 volts because of field intensification at the bottom corners of the metalization step and weak dielectric strength at the thin-thick oxide interface. When external pins are directly connected to such metalization runs, susceptibility to ESD occurs.

- Failure Mechanism: Dielectric Breakdown. ESD can damage the oxide in MOS structures because their breakdown voltage is low in comparison to voltage levels encountered with ESD. Permanent damage is done when the oxide is broken down, since it is the dielectric breakdown process associated with insulators, not the semiconductor junction breakdown process. The dielectric breakdown process is voltage and time dependent where the electric field associated with the applied voltage accelerates available free electrons with sufficient energy to dislodge other electrons to an "avalanche" condition which produces a punch-through (plasma-arc) short if the voltage is applied for sufficient duration.

For very short duration overvoltages some lattice damage might occur such that subsequent breakdown and therefore avalanche occurs at a lower value than the initial breakdown.

- Failure Indicators. As the punch-through short occurs the metalization will flow through the dielectric to create a low resistance path (short). However, in

some instances where there is particularly thin metalization such as 4,000Å, or there is sufficient energy passed through the short, the metal will be vaporized and the short will clear but leave a cratered hole in the dielectric. Degraded performance may result but not a catastrophic failure. There is conjecture that the short in some circumstances might reappear or performance might continue to degrade.

o Semiconductor Junctions. Included in this structure classification are PN junctions, PIN junctions and Schottky barrier junctions. Their sensitivity to ESD depends on geometry, size, resistivity, impurities, junction capacitance, thermal impedance, reverse leakage current and reverse breakdown voltage. The energy required to damage a junction in the forward bias direction is generally ten times that required in the reverse bias direction. Junctions with high breakdown voltage of greater than 100 volts and low leakage currents of less than 1 nanoampere are generally more susceptible to ESD than junctions of comparable size with low breakdown, such as 30 volts and leakage greater than 1 microampere.

- Part Types. The emitter-base junctions in bipolar transistors, whether incorporated in integrated circuits or a discrete transistor, are usually more susceptible to ESD damage than collector-base or collector-emitter junctions. This is primarily due to size and geometry where the emitter side wall experiences large energy densities during reverse bias ESD. Because of larger areas the collector-base and collector-emitter do not experience the same energy densities, although with the collector-base and collector-emitter it is possible to laterally forward bias the base-emitter, in which case a current crowding at the emitter side wall will occur.

Junction field effect transistors which have high impedance gates are particularly sensitive to ESD. They have extremely low gate-to-drain and gate-to-source leakage current in the order of less than 1 nanoampere and relatively high breakdown voltage of greater than 50 volts. Therefore the gate-to-drain and gate-to-source are usually the most sensitive ESD paths.

Schottky barrier junctions such as the 1N5711 diode and TTL Schottky integrated circuit structures are particularly sensitive to ESD because they have very thin junctions and the presence of metal which may be carried through the junction.

Not all diodes, transistors and thyristors contain semiconductor junctions that are considered sensitive to ESD. Transient suppressor diodes, zener diodes, power rectifiers, power transistors and power thyristors have been found to be insensitive to ESD. Semiconductor junctions as sensitive ESD structures are found not only in diodes, transistors, and bipolar integrated circuits but also in MOS integrated circuits as parasitic transistors and input protection clamps. Although a part's input protection junctions are designed to provide protection from ESD damage, the size of the protective junctions are limited due to cost and performance tradeoffs. Thus ESD pulses of sufficient energy can damage the input protection network junctions.

- Failure Mechanisms. The temperature coefficient of extrinsic semiconductors is positive, i.e., the higher the temperature, the higher the resistance. This characteristic prevents current crowding and hot spots from forming at low temperatures. However, in the reverse bias mode all the energy is being dissipated by the relatively narrow depletion layer width of the junction. Due to

geometry effects, local resistance variations, and crystal defects perfectly uniform current distribution does not occur across the junction. As an ESD occurs across the junction the temperature at the depletion region increases quickly and the extrinsic semiconducting material becomes an intrinsic semiconducting material, causing a sharp decrease in resistance, resulting in thermal secondary breakdown. As this process does not occur uniformly across the junction a hot spot develops into which all the remaining energy is concentrated, causing the silicon in the hot spot to become molten (1415°C). If sufficient energy is available the hot spot then grows as a filament short across the junction.

The more rapid the discharge, the more uniform is the increase in temperature and therefore current across the junction. This means that for short duration discharges of less than 10 nanoseconds the resultant filament short is wide compared to longer duration discharges. It is possible for hot spots to develop but not grow completely across the junction such that at low bias voltages they do not cause a failure condition. However, during operation at certain bias conditions, locally high current densities may exist with a corresponding highly localized large increase in temperature at the previously formed hot spot locations. In this case, continued growth of a filament short may occur or silicon and metalization may diffuse through the junction via the electro-thermomigration process at temperatures greater than 200°C.

The low-leakage high-breakdown JFET and Schottky barrier junctions seem to be particularly susceptible to this failure process. It is this same failure process that requires that the breakdown test on JFETs be performed as a leakage test rather than force the junction into breakdown. With low leakage junctions, highly localized currents can

occur during junction reverse breakdown. With Schottky barrier junctions, metalization is immediately available to migrate through the junction at localized hot spots.

- Failure Indicators. The current filament that develops across a semiconductor junction is analogous to a parallel resistor of the same value as the short across the junction. However, in some marginally formed hot spots it may be similar to connecting a zener diode and a resistor in parallel with the junction. High leakage will be the failure indicator description when the filament developed is a high resistance short.

o Film Resistors. Resistor material adhering to an insulating substrate comes under the ESDS structure classification of film resistor. The degree of sensitivity will depend on the composition and formulation of the resistor material and size-power considerations.

- Part Types. Hybrid microcircuits frequently contain either thin film or thick film resistors. Hybrid designs which cannot tolerate large changes in resistance such as precision voltage regulators are sensitive to ESD. Thick film resistors consist of: a conductive metal oxide as the resistive element; a metal additive to improve electrical performance; and a glass frit to provide a support matrix, adhesion to the substrate, and resistivity control. Such parts are particularly sensitive to ESD. Since the resistance change is almost always negative (subtractive) for thick films, electric discharge has been considered as a possible trimming procedure when conventional trimming methods overshoot the desired resistance tolerance. It has also been found that the thick film resistance changes are heavily dependent on voltage rather than energy. Himmel (Reference 38) has reported on a new generation of thick film materials which have a high tolerance for high voltage transients.

Thin film resistors, on the other hand, are more energy-dependent and do not have changes greater than 5 percent in resistance until the energy of discharge is sufficient to cause film rupture. In addition to linear and hybrid microcircuits, some monolithic integrated circuits may also contain encapsulated thin film resistors, such as polysilicon resistors, as part of an input protection circuit.

Discrete encapsulated resistors which contain the film resistor structures are also sensitive to ESD. Carbon film, metal oxide, and metal film resistors are somewhat sensitive to ESD, especially at low tolerance and low wattage ratings. A frequently occurring ESD problem with resistors is with the 0.05 watt metal film, part RNC50, specified at 0.1 percent tolerance. Placing these parts in a polyethylene bag and rubbing the bag on another bag is sufficient to shift the tolerance of these resistors.

- Failure Mechanisms. The ESD failure mechanisms of film resistors are not well defined. This is partly the result of not knowing the compositions and formulations of the resistor material which are often held proprietary by the manufacturer.

For thick film resistors the failure mechanism has been modeled as the creation of new shunt paths in a matrix of series-parallel resistors and infinitesimal capacitors isolating metallic islands. With the application of high electric fields the dielectric breakdown of the glass frit or other isolating dielectric material is exceeded and the ensuring rupture welds metallic particles together in a conducting path. Since this model involves a dielectric breakdown process it is mostly voltage dependent.

It appears that the ESD behavior of resistive materials is very much a function of the number of parallel current paths or the number of capacitive couplings between parallel paths in the film structure. The nature of the glass used in the material also appears to be quite important, both because it influences the distribution of the resistive elements and because it can act itself as a resistive element. Thus the behavior of different thick film resistor structures to ESD can vary greatly.

For thin film resistors and encapsulated metal film, metal oxide and carbon film resistors, the failure mechanism is primarily a thermal, energy dependent process modeled as the destruction of minute shunt paths. This mechanism is associated with an increasing resistance. At a lower ESD voltage, there is some small negative resistance shift on the thin film and metal film type resistor which appears to be voltage dependent. This negative resistance shift is usually not more than 5 percent and is typically less than 1 percent before changing to positive resistance shifts as ESD voltage increases.

- Failure Indicators. Some thin film resistors such as deposited tantalum nitride on SiO_2 substrates, may be so small and power limited that ESD voltages greater than 5,000 volts e.g., from a charged human body, can fuse the resistor open. For most cases, however, a shift in resistance will be the failure indicator. For circuit designs tolerant of large resistance changes, no failure will occur.

Generally, after exposure to ESD the stability of the resistor is reduced and the degree of instability is directly related to the level of ESD. Temperature coefficient changes have been known to result from ESD exposure.

For thick film resistors the resistance shift is negative. The resistance change can easily exceed 50 percent with some thick film pastes. Some exceptions to this may occur, especially at low resistance values.

For thin film, metal film, metal oxide and carbon film resistors at lower ESD levels, small negative resistance shifts of less than 5 percent can be experienced. At higher ESD levels, large positive shifts greater than 10 percent can be experienced, depending on the power rating.

o Metalization Stripes. Relatively narrow thin metalization on a substrate such as SiO_2 which carries current between terminals without any other energy absorbing element in the path are susceptible to ESD. These metalizations may consist primarily of aluminum or gold but can also be multi-layered. The failure mechanism is burnout from joule heating. This susceptible metalization structure is often used in monolithic integrated circuits, hybrid microcircuits and multiple-finger overlay transistor construction found in switching and high frequency transistors. Joule heating is most likely to occur when: (1) the ESD source has very low contact resistance, resulting in high currents over short time durations; and (2) a low resistance large area diode is connected by the metalization path between the two terminals, resulting in large currents due to the low voltage drop in the diode forward biased direction. Increasing the width or thickness of the stripe will decrease ESD sensitivity. The use of glassivation and thinner SiO_2 between the stripe and the silicon also reduces sensitivity to ESDS. The failure indicator from this failure mode is an electrical open.

o Piezoelectric Crystals. Part types such as quartz crystal oscillators and surface acoustic wave (SAW) devices can fail from being subjected to ESD with an operational degradation failure indicator. The electrical parameter

stability is damaged by subjecting the piezoelectric crystals they contain to excessive driving current. The piezoelectric effect causes mechanical stress and movement to be generated in the crystal plate when a voltage is applied to two opposite sides. When the voltage is too high, mechanical forces cause motion in excess of the elastic limit of the crystal and crystal fracture occurs. The fracture may occur as a lifted platelet which has been experienced in lithium niobate SAW delay lines. Such fractures, when occurring in sufficient quantity will cause enough change to the operating electrical characteristics to cause failure.

o Closely Spaced Electrodes. When employing thick metalization such as 13,500Å, gaseous arc discharge in an arc gap 50 µm wide can be used as a protection device to dissipate incoming high voltage spikes. For parts with closely spaced unpassivated thin electrodes, however, gaseous arc discharge can cause degraded performance. Parts that employ thin, closely spaced electrodes include surface acoustic wave (SAW) devices. Other parts such as high frequency multiple-finger transistors and new technology such as very large scale integration (VLSI) and very high speed integration circuits (VHSIC) could also be degraded to failure from arc discharge between metalization runs.

The arc discharge generally causes vaporization and metal movement away from the space between the electrodes. The melting and fusing do not move the thin metal into the interelectrode regions, but the metal pulls together and flows or opens along the electrode lines. There can be fine metal globules in the gap region itself but not in sufficient quantities to cause bridging. Shorting is not considered a major problem with unpassivated thin metal electrodes. ESD failures have been experienced on surface acoustic wave (SAW) band pass filters with 4,000Å of metal and 3.0 µm electrode spacing.

d) Virtual Electrical Overstress Effects. Certain device malfunctions are associated with EOS but in reality no EOS occurs. This occurs because the malfunction is activated by similar electrical stresses that produce EOS.

o Upset. Transient pulses similar to those that cause transient EOS can cause intermittent or upset failures. Such failures usually occur when equipment is in operation and is characterized by a loss of information or temporary distortion of its functions. No apparent hardware damage occurs and proper operation resumes automatically after the ESD exposure or, in the case of some digital equipment, after re-entry of the information by resequencing the equipment. Upset can be the result of an ESD spark in the vicinity of the equipment. The electromagnetic pulse (EMP) generated by the spark causes erroneous signals to be picked up by the equipment circuitry. Upset can also occur by the capacitive or inductive coupling of an ESD pulse or by the direct discharge of an ESD through a signal path providing an erroneous signal.

Parts that are very susceptible to transient upset are any logic family that requires small energies to switch states or small voltage changes in high impedance lines. Examples of families that are sensitive would be NMOS, PMOS, CMOS and low power TTL. Linear circuits with high impedance and high-gain inputs would also be highly susceptible along with RF amplifiers and other RF parts at the equipment level; however, design for RFI immunity can protect these parts from damage due to ESD high voltage spark discharge. To protect parts sensitive to ESD, high spark discharge at the equipment level requires good RFI/EMC design, buffering of busses, proper termination of busses, shielding of bus conductors and the avoidance of field penetrations of the equipment cabinet that lead to internal sensitive parts.

o ESD Activated Surface Inversion and Gate Threshold Voltage Shifts. Various NMOS and PMOS integrated circuit designs have been found to fail from very localized high concentrations of positively charged ions on the upper passivated surface of the die. NMOS designs fail due to excessive leakage in the microampere range from field-induced inversion between nearby N+ diffusions such as (1) thick field parasitic transistors, (2) intermediate field parasitic transistors, (3) EPROM transistors and (4) normal select transistors. PMOS designs such as the floating gate, EPROM or depletion type field-effect transistors fail when the negative charge on the floating gate is overcompensated by positive charge accumulation on the upper surface of the die. This causes the part to turn off, giving an erroneous unprogrammed indication. The effective field from the positively charged ions needed to create this inversion has been found to exceed 85 volts. Hermetic packages which have exhibited this failure mode have nonconductive lids made from non-transparent ceramic, transparent sapphire and transparent borosilicate glass. These failures can be prevented by grounding the bottom surface of the lid over the internal die or by instituting preventive measures to avoid electrostatic charging of the nonconductive lid.

Woods and Gear (Reference 39) found this failure mechanism on NMOS and PMOS UV EPROMs having transparent lids. NMOS static RAMS in a ceramic package were also found to fail from this ESD failure mechanism. Unless testing shows otherwise, any LSI integrated circuit with nonconductive lids could conceivably have field-effect structures which are susceptible to failure from undesirable field induced inversion or gate threshold voltage shifts.

This failure mechanism involves positively charged ion clusters deposited on the die as a result of air breakdown in the air gap between the die top surface and the bottom of

the package lid. Charging of the bottom of the lid can be induced by several means, one of which is by freeze spraying the package with canned coolant. The positive charging rate of the freeze spray impinging on the top of the lid depends on the flow rate of the coolant from the can. At low flow rates the charging is negative and does not induce failure; at high flow rates, sufficient positive charging can occur to induce failure. The localized air breakdown in the air gap of the package causes ionized streamers to form from the lid to the die surface. The positive charge on the bottom of the lid drives the positive charge in the streamer toward the die surface and attracts the negative charge toward the lid. This results in very localized clusters of positive ions on the die surface. Because of the nature of the air breakdown for certain package ambients this charge is probably identical in type to the very large $(H_2O)_nH^+$ ions that can be experimentally created by positive corona discharge in air.

These localized positive charges also cause the formation of inversion layer leakage paths between N+ diffusions and shift the gate threshold voltage on PMOS depletion type transistors. The formation of leakage paths and the gate threshold shifts gives rise to isolated circuit failures.

This failure mechanism is recoverable by neutralizing the positive charge on the outer surface of the die. On UV EPROMs with transparent lids, recovery is nondestructive when 2537Å ultraviolet light, with a minimum photon energy of 4.3eV is applied to the chip for as short as 3 to 5 seconds.

The failure indicators for this failure mode come under the general classification of operational degradation. This

operational degradation will take the form of a functional failure. In the case of NMOS UV EPROMs, certain programmed bits appear unprogrammed and certain unprogrammed bits appear programmed. In one group of failure indicators, bit failures have been organized in columns where programmed bits appeared unprogrammed. In another group of failure indicators, bit failures were organized in rows where unprogrammed bits appeared programmed.

The failure indicators for PMOS UV EPROMs are random single bit failures throughout the memory on bits which should read as programmed and instead read as unprogrammed.

The failure indicators for an NMOS static RAM have been reported as random bits stuck in a "1" or "0" logic state and the adjacent cell also stuck, but in the opposite logic state.

o Electrostatic Charges in Silicone Encapsulants. DerMarderosian and Rideout (Ref. 40) reported signal dropouts during system qualification testing in a cyclic gaseous pressure/vacuum environment. The problem was found to be caused by the charge generation from silicone potting material movement. Specifically, the problem was isolated to poorly adhered interfaces between the silicone encapsulant and electrically sensitive areas of the high impedance circuitry on a crystal oscillator module. The mechanism of the sporadic electrical interruptions was found to be associated with the generation of triboelectric charges at the poorly bonded interfaces during the depressurization cycle of the pressure/vacuum testing.

4. Failure Analysis Techniques. In practice the depth or level of applying failure analysis techniques in assessing suspect EOS/ESD part failure varies depending on part criticality or the failure pattern type and frequency.

There is no guarantee that the investment in the device failure analysis will produce accurate and definitive information. Misinformation from failure analysis can be costly. The application of appropriate electrical test and failure analysis techniques and accurate interpretation of the findings is not a straightforward process and requires experienced personnel.

Failure analysis activities are heavily results-orientated. Because of the difficulty and ambiguity of finding the EOS source, there is a tendency for part failure analysis to end abruptly when the analyst concludes the part was electrically overstressed. The analyst must recognize the need to determine whether a suspect EOS failure is related to part design errors/processing defects or application/environment induced. EOS part failures in equipment can be minimized only when the source or sources of EOS is isolated and eliminated through appropriate corrective action implementation.

a) General Procedure. To prevent future failure occurrences part analysis alone is usually not sufficient. On critical failures, to maximize the information feedback from the failure analysis process, McAteer (Reference 41) states the procedure should include the following major elements,especially if EOS is suspected:

- o Notification
- o Fact Gathering
- o Part Analysis
- o Failure Cause Identification
- o Corrective Action

o Notification. This is the documentation of the failure event. All the appropriate information should be conveyed. This event cannot be overdescribed. Ambiguous terminology should be avoided.

o Fact Gathering. The failure history and other appropriate part information concerning the failure should be gathered. A thorough examination of the failure circumstances should be conducted. The following types of questions should be answered by this fact gathering:

- o Is the part generally considered highly or moderately ESDS?
- o Did the device work under powered conditions and then fail while the power was still applied, or did the device fail immediately at turn-on?
- o Was there a handling operation performed prior to failure discovery?
- o Did the device pass a previous test?
- o Is there a source of high voltage-low energy transients in the equipment (other than ESD)?
- o Did the circumstances of failure and subsequent testing and handling confound the failure evidence?

o Part Analysis. The laboratory examination must be a step-by-step process with the results of each step reviewed to determine the next step in the analysis process. Table III-Q-5 depicts a failure analysis step-by-step sequence that might be necessary to detect and identify the parameters of an electrical overstress failure of an integrated circuit. All the techniques listed in this table would rarely be necessary for isolating the failure site but are listed to illustrate the alternate techniques that can be employed. Documenting the failure site and its defective conditions is the prime objective of the part analysis.

o Failure Cause Identification. With the result of the fact gathering and part analysis available the source of EOS must be identified and failure duplication testing performed.

TABLE III-Q-5
PART ANALYSIS SEQUENCE

Technique Sequence	MFATPG Section
Failure Verification:	
External visual examination	III-A-2 & III-L
Curve tracer pin-to-pin check (photo or sketch)	III-A-3
Circuit analysis	- - -
Electrical measurements, DC and function	III-A-4
Annealing processes	III-I
X-ray/hermeticity (optional)	III-B
Decap	III-E
Internal visual examination (photo)	III-L
Reverify	III-A-3 & 4
Fault Isolation:	
Glassivation removal	III-M
Visual examination, 400X (photo)	III-L
Reverify	III-A-3 & 4
Voltage contrast mode SEM	III-P-6a,b,c,d
Photoresponse	III-G
Electrical probe station	III-A-7
Isolation of circuit element	III-A-6
Electrical probe of isolated element	III-A-7
Metalization removal	III-M
Visual examination, 400X (photo)	III-L
SEM verification (photo)	III-P
Copper decoration	- - -
Liquid crystals	III-H
EBIC	III-P-6e
Chemical etch (Sirtl)	III-M
Metallurgical sectioning	III-N

o Corrective Action. In order to prevent future recurrence of the EOS failure certain measures must be implemented. Typical measures are the addition of protection circuitry, improved packaging and improved handling controls.

b) Visual Characteristics. Smith (Ref. 29 and 42) has pioneered in developing damage analysis physical criteria to determine the characteristics of the electrical transient causing failure. Smith's approach is to first identify the pulse width with an overriding assumption that the transient occured as a single event. Given the pulse width, the current, voltage, power and energy can then be established.

Smith's pulse width criteria for junction shorts, metalization burnout and flying lead wire vaporization are summarized as follows:

Criteria	Pulse Width
JUNCTION SHORTS:	
Width of short greater than 25% of contact width (see Figure III-Q-4)	≤ 200ns
Narrow short with no metalization damage at contact (see Figure III-Q-5)	200ns to 2μs
Narrow short with some metalization damage at the contact (see Figure III-Q-6)	2μs to 50μs
Somewhat wider short with aluminum alloyed in the short (white spear) (see Figure III-Q-7)	> 50μs
METALIZATION BURNOUT:	
Entire stripe damaged uniformly with the exception of distinct cornering effects (see Figure III-Q-8)	≤ 200ns

Bonding pad heat sinking with pulse width proportional to the distance between melt edge and bonding pad (see Reference 29)	> 200ns
Without damage to flying lead wire (see Reference 29)	< 200µs

FLYING LEAD WIRE BURNOUT:

Estimate minimum pulse width by assuming one half the length of undisturbed wire is proportional to the pulse width (see Reference 29)	> 100µs

With the pulse width determined, the power is determined by examining the electrical overstress path. The damage threshold of the power dissipating elements in the circuit path is then calculated. For junction shorts use the Wunsch-Bell equation (see References 21 and 30). The minimum power is determined from one tenth of the junction area and the pulse width. For metalization burnout it is simpler to estimate the current to cause failure by knowing the cross-sectional area of the metal stripe. For pulse widths less than 1µs, adiabatic conditions can be assumed and the heat loss through the oxide can be ignored. References 29 and 30 give equations for both conditions (adiabatic and heat loss through the oxide). Geometry effects such as current crowding at 90° turns and reduced cross-sectional areas at oxide steps must also be considered. The fundamental point the analyst should keep in mind is that the entire damage observed is related to power dissipation and heat flow.

Visual effects from short-duration, low-energy ESD pulses are usually not discernable on junction filament shorts. Speakman (Reference 43) shows an example in Figure III-Q-9 of the physical damage that occurs as a result of ESD through the emitter-base junction of one of the differential input transistor pairs on an operational amplifier. Speakman reported this to be an extreme case of ESD damage with most failed devices exhibiting no visible damage.

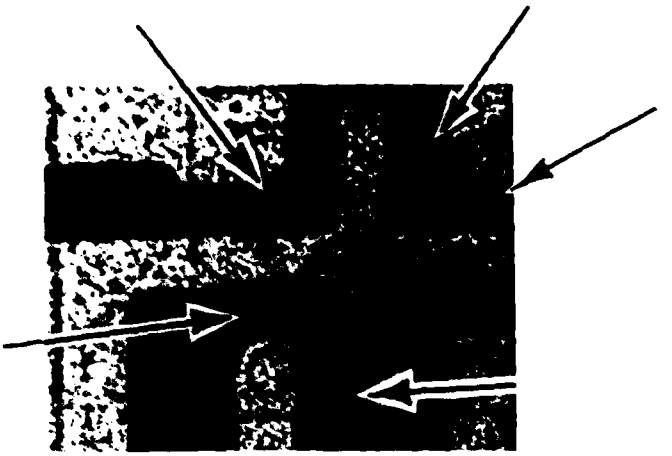


FIGURE III-Q-4: JUNCTION SHORTS CAUSED BY PULSE WIDTHS LESS THAN 200 ns.

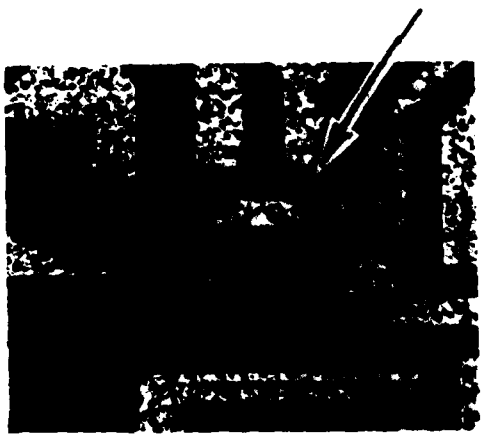


FIGURE III-Q-5: JUNCTION SHORT CAUSED BY A PULSE WIDTH BETWEEN 200 ns and 2 μs.

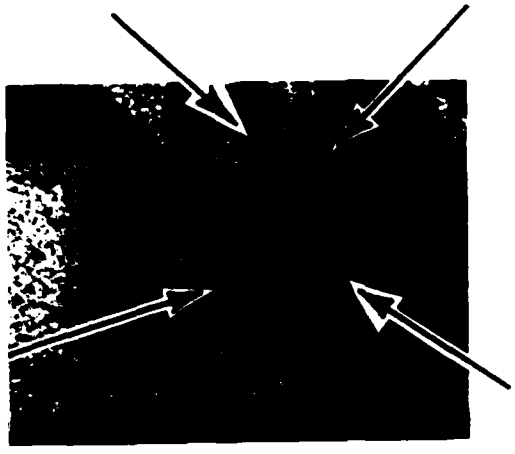


FIGURE III-Q-6: JUNCTION SHORTS TYPICAL OF PULSE WIDTHS BETWEEN 2 μs and 50 μs.

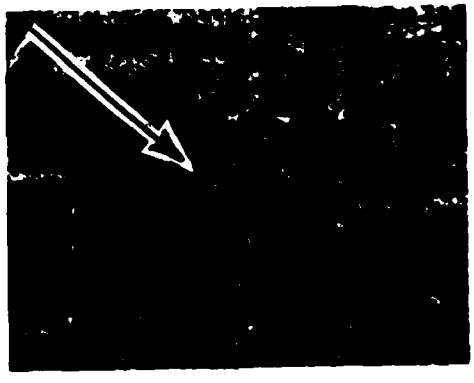


FIGURE III-Q-7: JUNCTION SHORT TYPICAL OF PULSE WIDTH LONGER THAN 50 μs.

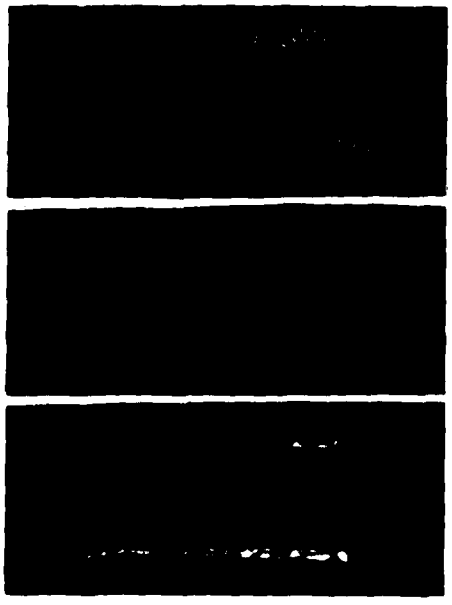


FIGURE III-Q-8: METALLIZATION DAMAGE AS A FUNCTION OF PULSE WIDTH.

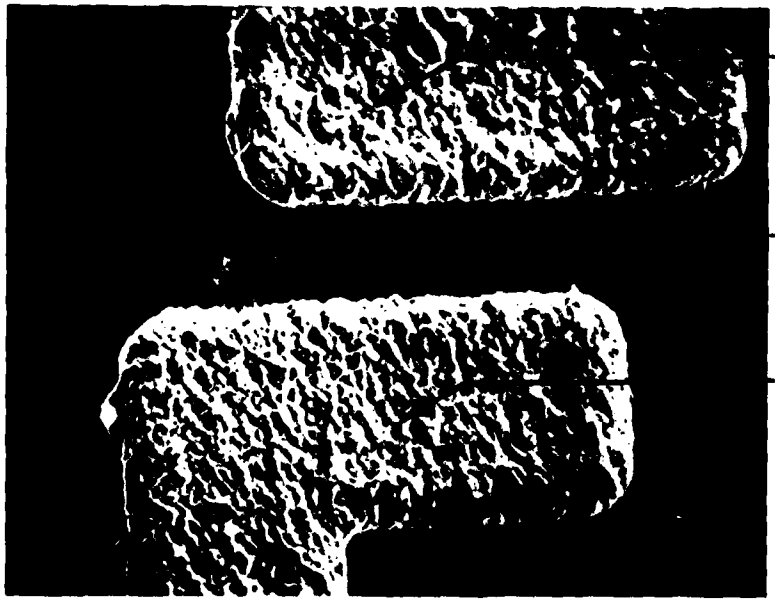
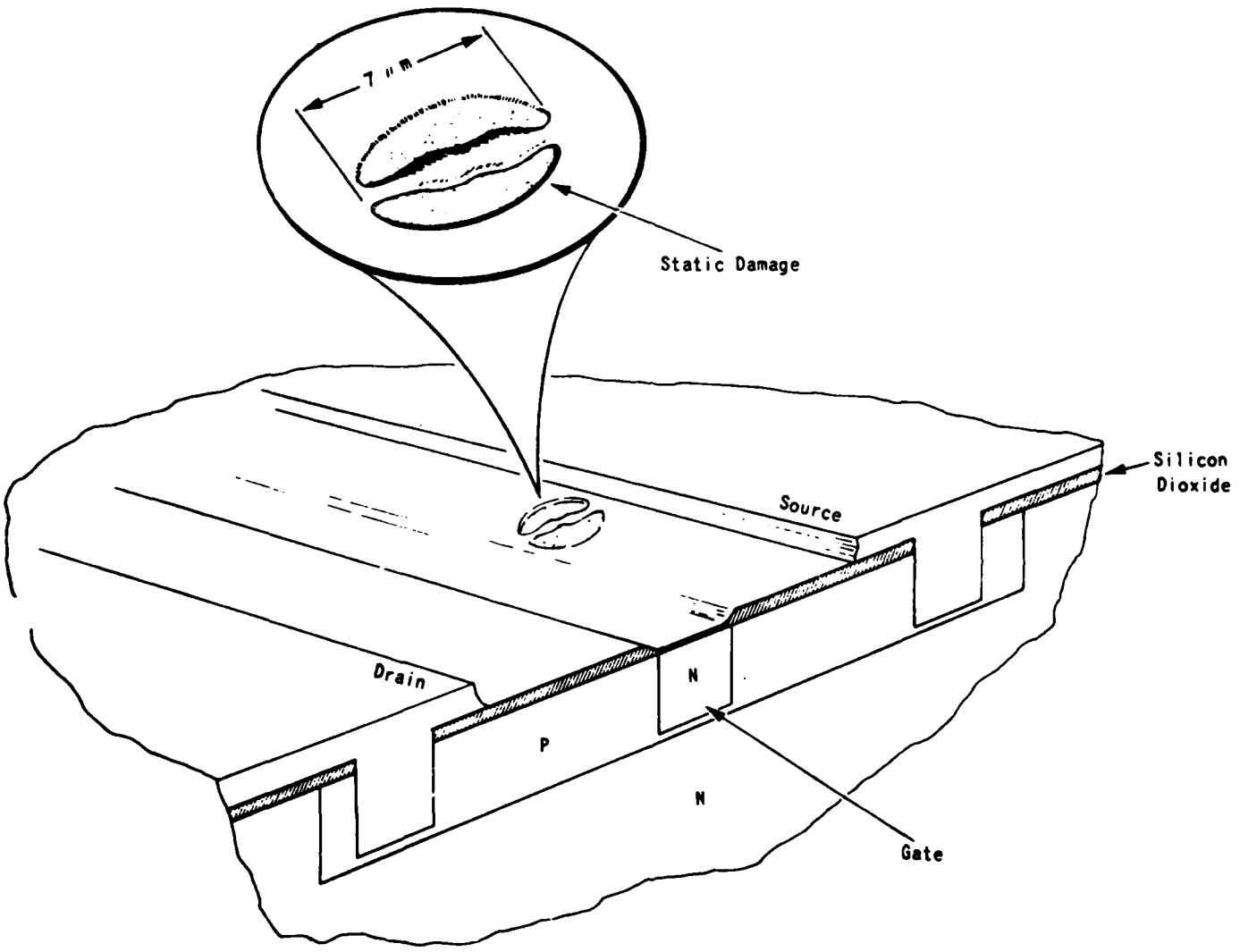


FIGURE III-Q-9: EXAMPLE OF THE PHYSICAL DAMAGE THAT SOMETIMES RESULTS FROM ESD THROUGH AN EMITTER-BASE JUNCTION (SEM AT 2000X)

Figure III-Q-10 is a schematic of the solidified melt region (puddle effect) near the gate-to-source junction depletion region of the 2N3112 JFET. Kirk, et al., reported (Reference 44) this damage trait was created by ESD but produced only degraded electrical characteristics and would have functioned in some circuits. Beall and Hamiter (Reference 45) and Trigonis (Reference 46) found that ESD damage effects on junctions which were not visible employing ordinary SEM techniques could be made visible by using EBIC techniques. See Figure III-Q-11a, b and c taken from Reference 45. Sirtl etches may also bring out these shorts.

ESD failures of gate dielectric and MOS capacitors on linear ICs are discernable as a cratered hole in the dielectric. Figure III-Q-12 is a SEM photo from Reference 47 and shows a punch-through on a CMOS gate at the thick-thin oxide interface. Figure III-Q-13 is a SEM photo from Reference 48 and shows a shorted capacitor in a internally compensated operational amplifier. The cratered hole was not visible until the metalization was removed. In some cases the crater is visible without removing the glassivation on the metalization (see Reference 46). Figure III-Q-14 a and b shows transient EOS caused metalization crossover shorts on a custom linear IC. In distinguishing transient EOS dielectric failures from pinholes the smoothness of the hole, the physical location and the frequency of the holes have a direct bearing on the determination. Pinholes which are caused by foreign particles during the photolithographic process will be smooth at the outer edge of the hole. An EOS short will be rough and have material expelled from the hole. In some cases the EOS hole will have hot electron tracks emanating from the hole along the crystaline plane (see Figure III-Q-13 and Reference 31).



Degraded 2N3112 JFET

FIGURE III-Q-10

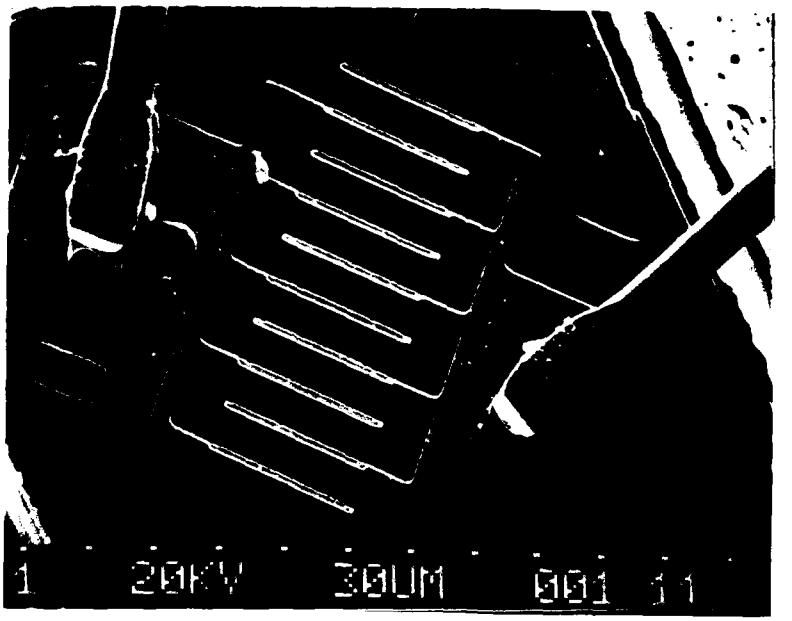


FIGURE III-Q-11 (a): SEM MICROGRAPH OF THE 2N3921 FET DIE. (MAG X 350)

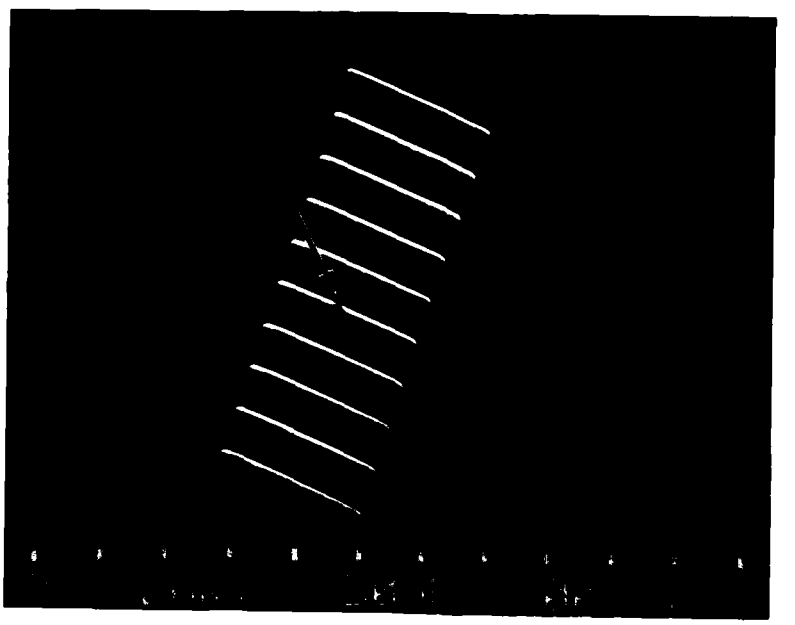


FIGURE III-Q-11 (b): EBIC MICROGRAPH OF THE SAME AREA SHOWN IN THE FIGURE 10. (V_{GS} = -10V. DAMAGE SITE IS VISIBLE (ARROW). (EB = 20 kV, I_B = 1 x 10-10A, MAG X 350.)

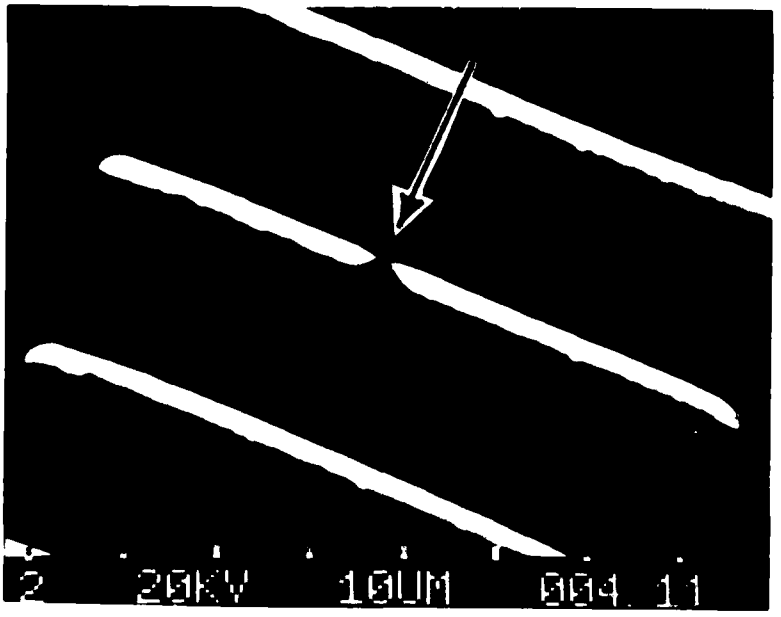


FIGURE III-Q-11 (c): EBIC MICROGRAPH SHOWING DAMAGE SITE AT INCREASED MAGNIFICATION (MAG X 1500.)

FIGURE III-Q-12: GATE OXIDE SHORT AT 20,000X OBSERVED AT 400X. PART AS RECEIVED HAD INPUTS SHORTED TO V_{SS}.

SEM PHOTO OF CAP FAILURE SITE

FIGURE III-Q-13: LIC CAPACITOR SHORT

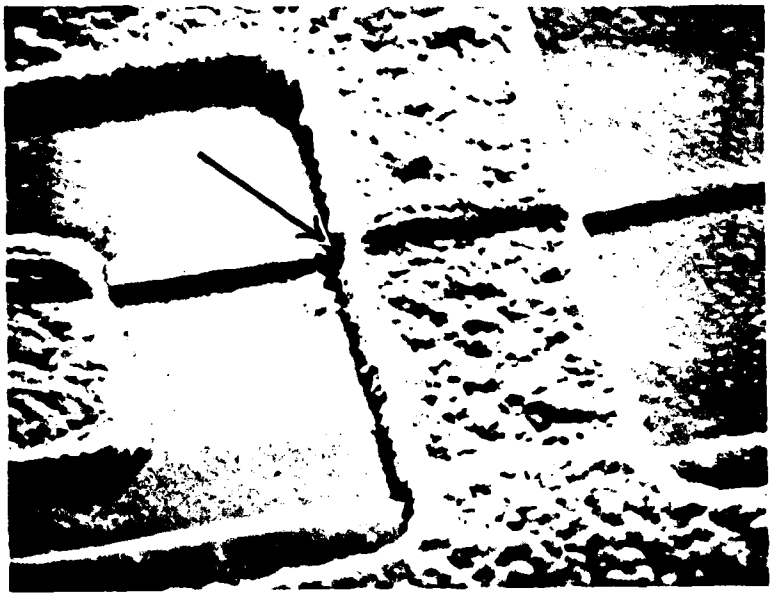


FIGURE III-Q-14 (a): V_{DD} SHORT TO Q_{15} BASE WHERE V_{DD} METALIZATION STRIP CROSSES OVER Q_{15} BASE ON CUSTOM LINEAR IC (SEM AT 3500X)

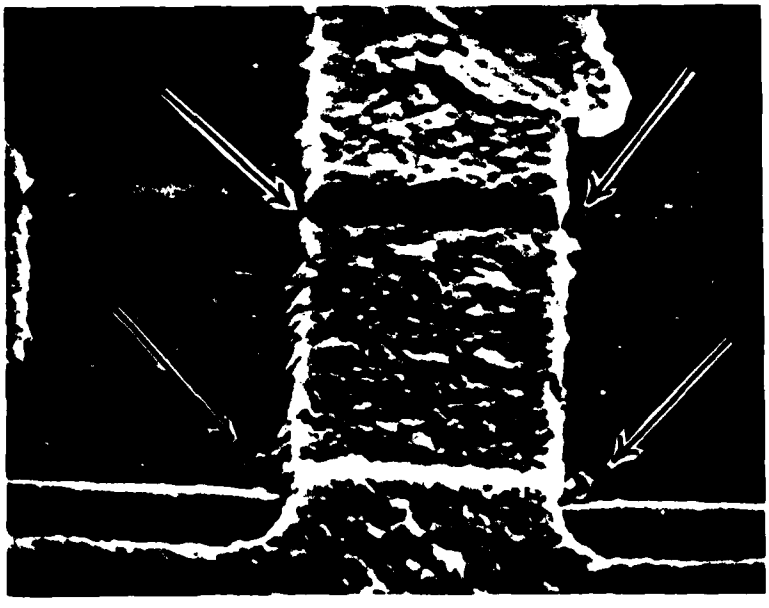


FIGURE III-Q-14 (b): SAME AS ABOVE WITH MULTIPLE SHORTS AT EDGE AND POINTS OF METALIZATION (SEM AT 3500X)

EOS-generated holes will tend to occur at the points of highest field intensification while oxide pinholes will be located more randomly. In some cases, pinholes of very small diameter (less than 1μm) will occur at the thick-thin oxide interface (Reference 49).

Table III-Q-6 is set up to facilitate review of photos of typical visual characteristic traits of EOS failures. Device types along with failure characteristics are identified in the table for easy cross referencing to the applicable source document. The analyst is encouraged to examine the photos and findings of the authors listed in the table. By locating a similar failure characteristic during analysis, he can reinforce his determination of the failure cause.

c) Failure Duplication Testing. When the part analysis has been completed and the failure traits identified, the final step in drawing a conclusion regarding the nature of the EOS is to duplicate the failure. A list of possible test waveforms is given in Table III-Q-2. An additional list is published in Reference 5. From the application and the damage analysis of the part, the likely source and magnitude of the transient must be estimated. It has been shown (References 7 and 43) that square pulses can be correlated to both RF pulses and double exponential pulses with respect to energy content to create damage. To identify the transient shape, the most plausible source and susceptible mode must be searched out to duplicate.

To typify equipment-generated transients and human body ESD, Antinone (Reference 11) specified a double exponential pulse from a capacitor resistor discharge circuit.

TABLE III-Q-6

SOURCE GUIDE TO FAILURE TRAIT PHOTOGRAPHS

Source	Year & Page	Authors	No. Appl. Photos	Device Types	Failure Traits	Ref.* No.
EOS-2	80/17	Bossard Chemelli Unger	3	I^2L CMOS	Contact window severe damage Metalization crossover failure	17
	80/87	Hart, Teng	6	CMOS	Metal-to-polysilicon contact resistance Polysilicon resistor	60
	80/95	Turner, Morris	11	NMOS	Gate oxide Deposited glass breakdown Vaporized metal Vaporized polysilicon resistor Alloying metal through junction	59
	80/104	Schwank Baker Armendariz	6	CMOS	Gate oxide ruptures	58
EOS-1	79/64	Rutherford Perkins	26	TTL	Oxide damage at pad Junction damage	54
	79/88	Uetsuki Mitani	4	TTL LIC Power IC	Junction damage Burned metalization Diffused resistor damage	55
	79/97	Anand Morris Higgins	7	Schottky Barrier Diodes (X-band)	Junction shorts	6
	79/147	Whalen Thorn Rastefano Calcatera	10	MESFET	Metal migration Massive channel damage	8
	79/168	Teng Hart McKenna	2	MOS	Filament shorts	56
	79/176	Soden	2	CMOS	Oxide breakdown	57
IRPS	71/163	Smith	5	Bipolar	Metalization burnout Thin film resistor burnout Junction shorts	25
	73/105	Smith	3	Bipolar	Metalization burnout Junction shorts	42

*All references refer to subsection III-Q.

TABLE III-Q-6 (Cont'd)

SOURCE GUIDE TO FAILURE TRAIT PHOTOGRAPHS

Source	Year & Page	Authors	No. Appl. Photos	Device Types	Failure Traits	Ref.* No.
IRPS (Cont'd)	78/41	Smith	9	Bipolar	Metalization damage Junction shorts	29
	78/47	Wunsch	1	IC	90° turn metalization damage	30
	74/60	Speakman	1	LIC	Op amp input e-b short	43
	74/30	Gajda	12	MOS	Process generated pinholes (Not EOS)	49
	74/304	Freeman Beall	14	JFET LIC T^2L	Junction shorts Capacitor oxide short Junction shorts	48
	77/61	Beall Hamiter	3	JFET	Junction damage	45
	77/144	Hickernell	4	SAW	Metalization damage Crystal surface rupture	34
	77/138	Minear & Dodson	1	LIC	Input transistor short	61
	75/10	Yang Johnson Lampert	4	SiO_2	Dielectric breakdown traits	31
	81/212	Fisch	3	MOS	Thick oxide rupture Gate oxide	62
	81/193	Unger	7	I^2L MOS	Contact window damage Dielectric breakdown	4
	81/223	DeChiaro	2	NMOS	Parasitic output transistor short	28
R&M Symposium	70/386	Lytle McAteer	14	Microcircuits Transistors	Junction shorts/white spear Metalization damage/burnout Fly leadwire burnout	50
	78/434	McAteer	25	Hybrids LIC ECL CMOS	Op amp input short Metalization crossover Junction short Gate oxide short	53
	76/162	Trigonis	30	LIC	MOS capacitor short Junction short	46

*All references refer to subsection III-Q.

TABLE III-Q-6 (Cont'd)

SOURCE GUIDE TO FAILURE TRAIT PHOTOGRAPHS

Source	Year & Page or Dash No.	Authors	No. Appl. Photos	Device Types	Failure Traits	Ref.* No.
RADC-TR-	71-59	Smith	19	Microcircuits	Junction shorts Metalization burnout	24
	72-148	Lane	22	Test pattern	Surface breakdown	27
	73-87	Domingos	23	Microcircuit	Junction shorts Metalization damage/burnout	26
	76-72	Whalen	26	CMOS	Gate oxide shorts Junction shorts Metalization crossover	47
	78-28	Antinone	1	CMOS	System transient simulated Metalization burnout	11
Microcircuit Manufacturing Control Handbook	5A-14		1	Analog Switch	N+ guard ring crossover short	II-B
	5J-3		1	LIC	Input transistor short	
	5J-1		1	UHF Xistor	Junction degradation	
	5I-1		1	Schottky TTL	Junction shorts	
ATFA Symposium	77/75	Shumka Miller Piety	6	CMOS	Gate oxide short Pinholes shorts	52
	77/99	Riga	2	LIC	Capacitor edge short Input transistor short	51

*All references refer to subsection III-Q.

Figure III-Q-15 is the test circuit for equipment-generated transients, and Figure III-Q-16 is the human body ESD generator. By varying the voltage on the capacitor the energy delivered to the part under test is varied. For ESD simulation, voltages as high as 15KV may need to be generated. The usual procedure is to have all the pins floating except the terminal pair believed to be the discharge path. However, it has been found (References 62 and 64) that certain ESD failure modes are not duplicated by this procedure. To successfully duplicate some failures all the pins except the pin receiving the ESD must be tied together and either grounded or left floating. Floating of all the pins is the state of the device when the pins are not in contact with a conductor but may have some mutual capacitance in addition to its self-capacitance.

By connecting a grounded 10 to 50 pf capacitor in series with the pins tied together the mutual capacitance effect may be simulated under controlled conditions. Unger (References 4 and 17) has shown significant energy variations depending on the orientation of the device to a ground plane.

For thick-film resistors that are highly voltage sensitive, Patterson (Reference 63) suggests that the resistance as a function of voltage be swept across the face of a storage oscilloscope (or photographed). The voltage level at which there is an inflection in the rate of change in resistance is the voltage amplitude of the transient EOS which produced the degradation in resistance.

5. Handling and Storage of ESD Sensitive Failed Devices. Suspect EOS failed devices may be even more sensitive than in their unfailed state because they may be

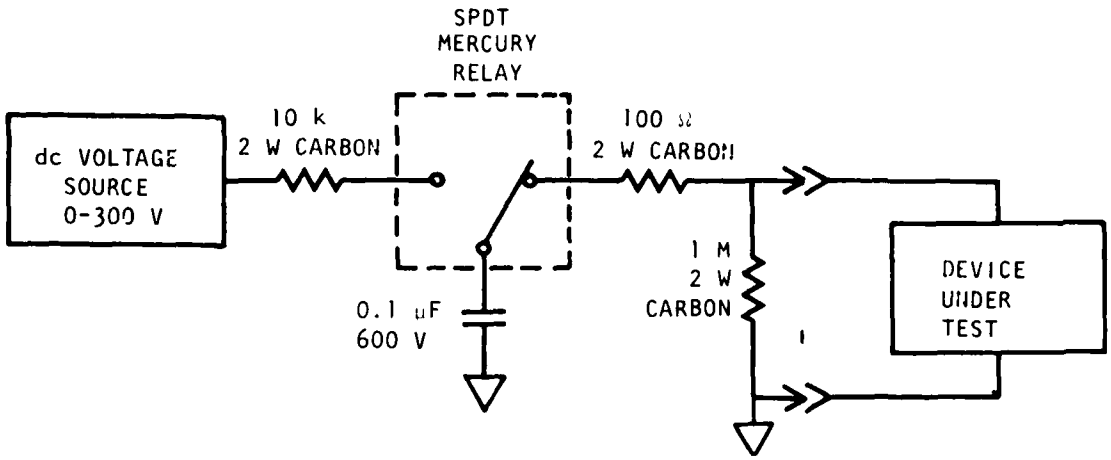


FIGURE III-Q-15: SYSTEM TRANSIENT SOURCE GENERATOR

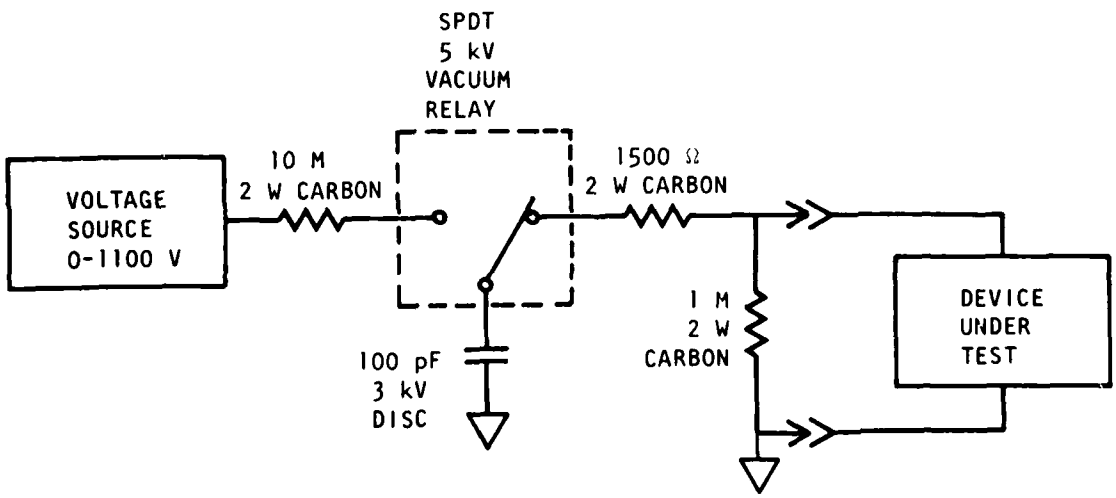


FIGURE III-Q-16: STATIC DISCHARGE SOURCE GENERATOR

in a partially degraded state. Thus to avoid confounding the analysis results, additional damage-causing stresses should be avoided. For example, an IC which is relatively insensitive may have a microfracture resulting in an intermittent open bond at the die pad. Careless handling which subjects the device to ESD could anneal the bond by microwelding the bond to the pad, eliminating the failure condition. Thus not only is it important to protect failed devices from mechanical, chemical and temperature stresses but ESD stresses as well. DOD-STD-1686 and DOD-HDBK-263 (References 64 and 65) should be used as a guide in the protection of devices from ESD. The two basic rules for ESD protection are (a) handle ESDS devices only at ESD protected work stations and (b) cover or package ESDS devices in ESD protective packaging when not being handled.

a) Protected Work Station. The purpose of the protected work station is to eliminate all the sources of ESD at the work station. The primary method of achieving this objective is by the grounding philosophy. Electrically bonding all the surfaces, tools and furnishings of the work station together not only eliminate voltage potential differences but also prevents the use of insulators which can retain static electricity.

A recommended protected work station should contain the following control elements:

- Protective work surface such as the Charleswater Micastat CPF201 table top laminate
- Personnel grounding devices such as wrist straps, model A5691-2 (SIMCO)
- Protective floor such as can be achieved through proper chemical treatments with staticide from Analytical Chemical Laboratories

- o Protective stool such as can be achieved through a stool cover, model 2050 from 3M Static Control
- o Air ionizers such as those available from SIMCO, 3M, Wescorp, Scientific Enterprises and Controlled Static to neutralize charge on insulated objects which have to be at the work station such as personnel clothing.

b) Protective Packaging. Three electrostatic principles are invoked to achieve protective packaging:

(1) equipotential bonding
(2) prevention of electrification through contact separation and triboelectric charging
(3) Faraday cage shielding.

Shunts such as 3M's conductive foam for radial leads and L. Gordon's conductive foil cardboard for axial leads use the principle of equipotential bonding to prevent an ESD between sensitive elements of the device. Note: shunts are not adequate by themselves as protective packaging, especially on highly sensitive devices.

Cushioning material placed next to an ESDS device can cause triboelectric charge when in intimate contact with the device. Thus, styrofoam and polyethylene bubble wrap can not be used. Conductive or antistatic foam, antistatic bubble wrap or antistatic treated urethanes must be used as cushion material next to the device.

Bags such as the Richmond 3600 and the 3M static shielding 2100 bag utilize two electrostatic principles to achieve protection. By having an antistatic inner surface which comes in contact with the device these bags prevent triboelectric charging. By having a conductive outer layer,

the bag forms a Faraday cage, such that contact with static charge in uncontrolled areas will not cause any ESD stresses on the device inside. When an ESDS device is in one of these bags providing a Faraday cage, no further ESD protective packaging is necessary.

For interim protection, handling containers that are conductive or antistatic and satisfy the prevention of the triboelectric charging principle and the Faraday cage principle are acceptable. The conductive Velostat tote boxes with the cover in place satisfies this criterion, provided no insulators are allowed in the container with the part.

c) Miscellaneous Precautions and Controls. A static meter such as the portable field scanner from Scientific Enterprises should be used to test for static charge build-up on surfaces and objects. Special attention to tools and processes in the lab must be taken to avoid inadvertent ESD.

Solder suckers should be the conductive tip type. Cold spray should be the MS240 type. When devices are received in the lab incorrectly packaged, discharge the packages and device slowly in ionized air.

Refer to DOD-HDBK-263 for additional precautions.

d) Awareness Training. Failure analysts should have ESD Awareness Training to the extent of understanding the electrostatic control principles discussed above and knowing the importance and the use of the static meter. Refer to DOD-HDBK-263, paragraph 10.0, for a comprehensive ESD training course outline. The analyst is reminded of the following:

- o ESD is not intuitively obvious
- o People destroy devices and never know it
- o ESD can be very subtle

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EOS/ESD CONTROL EQUIPMENT

Wrist Strap	
1. Controlled Static (Fred Strap 30113)	$ 16.85 ea.
2. Simco (Simco-Stat A5691-2)	7.75 ea.
3. Semtronics (EN5603-4)	8.80 ea.
4. Controlled Static (30112)	7.75 ea.
Work Surface	
1. Charleswater (Micastat) Table Top Laminate	$ 8/sq. ft.
2. 3M Table Mat (8210) 2'x4'x1/16"	42.00 ea.
3. Simco Table Mat (Simco-Stat A4726-2) 27"x48"x1/8"	36.00 ea.
Floor Control	
1. 3M Floor Mat (Velostat-1834) 4'x8'x1/8"	$120.00
2. Walter's Legge (Legsure-7102) Cleaner & Polisher	7.33/gal
3. Analytical Chemical Labs (Staticide) fine spray or damp mop	9.99/gal
Stool/Chair Control	
1. Semtronics (Enstat-EN5101) Stool Covers 10"-15"	$ 3.00 ea.
2. 3M (2050) Stool Covers 10"-15"	32.00/25
3. Simco (Neutro-stat) antistatic spray, 15OZ	4.00 ea.
Air Ionizers	
1. 3M (909)	$250.00/yr.
2. Wescorp (WD-100)	265.00
3. Simco (APMA-1)	327.30
4. Scientific Enterprise (100)	330.00
Protective Bags	
1. 3M Static Shielding Bags (2100) 6"x10"	$ 38.86/100
2. Richmond (RCAS 3600) bags	236.10/1000
3. Simco Carbon Loaded Bags (A4692) 6"x10"	25.30/100
4. 3M Velostat Bags (2004) 6"x10"	32.48/100
Protective Covering	
1. 3M Velostat Tote Boxes (4030) 8¼"x6¼"x2¼"	$ 16.40
Cushioning Material	
1. 3M Conductive Foam (2900) 24"x36"x¼"	$ 16.75/sheet
2. Kimberly-Clark Antistatic Bubble Wrap (Kimcel) 26"x250"x¼"	39.35
Conductive Shunts	
1. 3M Conductive Foam (2910) 24"x36"x¼"	$ 16.75/sheet
2. L. Gordon Conductive Foil Cardboard	70.00/100
Static Voltmeters	
1. Scientific Enterprises (Field Scanner 2B)	$595.00
2. Sargent Industries (1127E)	750.00
3. Simco (SS-2)	457.65
4. Anderson Effects (DCA-1200-1)	295.00

R.

MISCELLANEOUS ANALYSIS TECHNIQUES

R. Miscellaneous Analysis Techniques.

1. Introduction. Some of the techniques occasionally used by the failure analyst are briefly described below.

2. Electrical Circuit Tracing and Die Element Layout Mapping. To track down and identify failures, it is often necessary for the failure analyst to identify specific elements in a failed circuit. This procedure involves destructive techniques. For instance, failure in the output stage of a T^2L circuit may not have been due to the output transistor itself but to failure in some stage preceding the output. In this instance, it would be necessary to trace the electrical path backward from the output transistor. This technique is accomplished by first opening the package to reveal the topography of the microelectronic device (see Chapter III-E).

There are definite steps to be followed in performing failure analysis through circuit tracing. The steps are:

a) Trace and Identify Individual Circuit Elements. Several methods may be used to do this:

o Tracing by Visual Inspection. Some of the less complex microcircuits can be successfully mapped by visual inspection through a microscope in conjunction with device schematics. Package pin designation will provide a reference point for tracing circuits by identifying inputs, outputs, chip enable, V+, V-, substrate ground, etc. The following steps might be used in mapping the elements in a microcircuit:

- Obtain, if available, the manufacturer's circuit diagram

- Open the package (see Chapter III-E).

- Identify the desired starting point; input or output pins, for instance

- Using a metallurgical microscope, locate the proper metal pad on the microcircuit

- Trace the metal from the pad to the first device electrode encountered for instance, the base of an input device

- Consulting the circuit diagram, determine what element should be encountered next, and trace metallization patterns to the next device

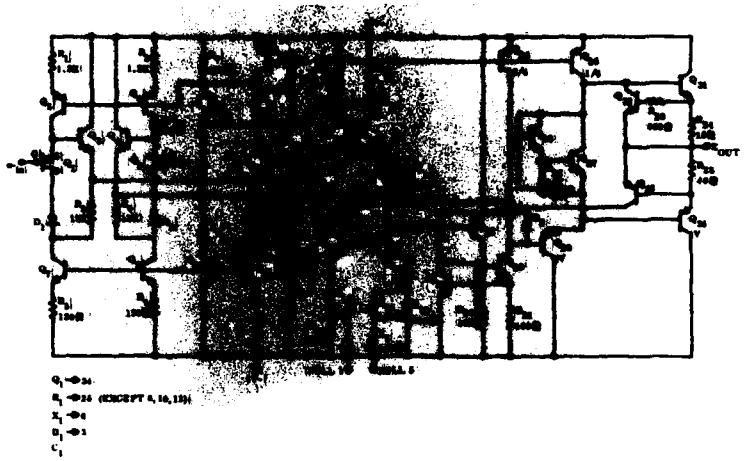
- Continue in this way until all circuit elements are identified or until the failure site is located visually

Figure 1 shows a circuit diagram and a photograph of a microcircuit that was mapped using this technique.

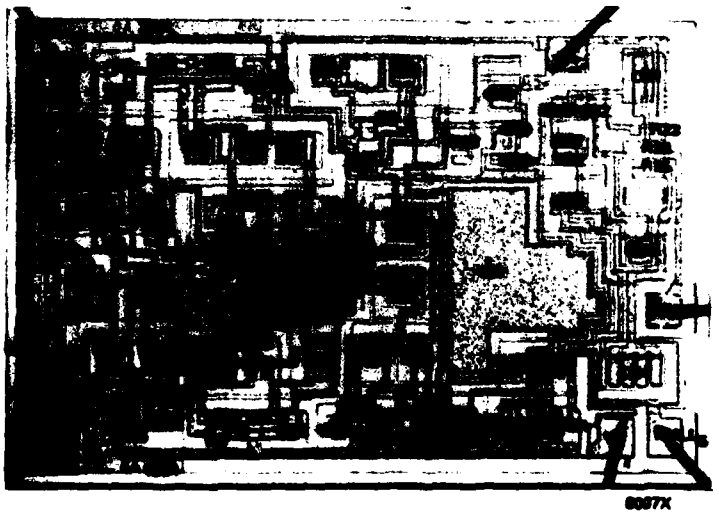
o Tracing by Visual Inspection With Chemical Staining. Due to multiple metallization layers and thick dielectric layers, it is often difficult to identify circuit elements, such as diffused resistors and other diffusion areas. Figure 2 demonstrates the difficulty in tracing electrical paths in such microcircuits. This bipolar emitter coupled logic circuit has two-layer aluminum metallization and a thick dielectric layer that prevents identification of diffused areas. Destructive techniques exist through which these circuit elements can be identified. The following steps detail one such technique:

- Obtain, if possible, the manufacturer's circuit diagram

- Open the package (see Chapter III-E)

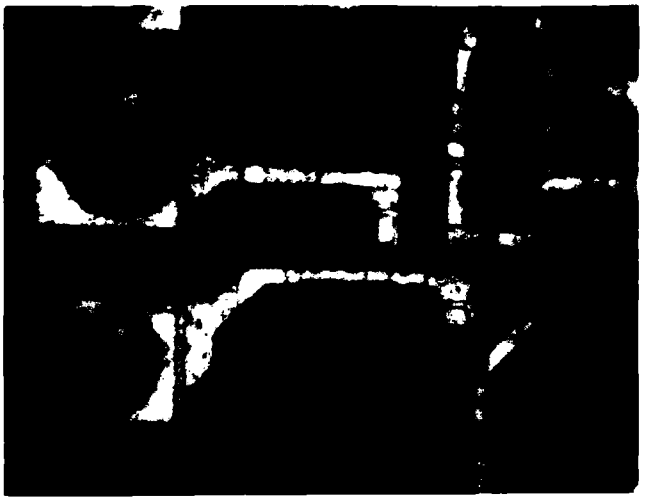


a) Circuit Diagram



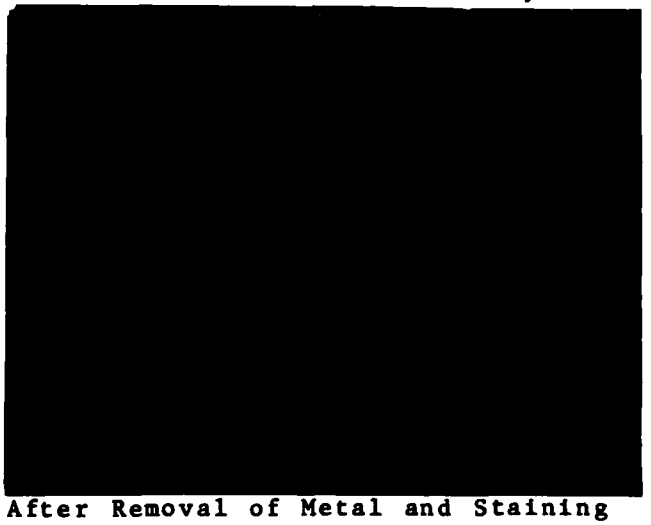
b) Photograph of Microcircuit

FIGURE 1. BIPOLAR LINEAR CIRCUIT MAPPED BY VISUAL INSPECTION



a) Before Removal of any Layers

b) After Removal of Dielectric Layers



c) After Removal of Metal and Staining

FIGURE 2. BIPOLAR ECL CIRCUIT SHOWING DIFFUSION AREAS

- Identify the desired starting point; input or output pins, for instance.

- Using a metallurgical microscope, locate the proper metal pad on the microcircuit

- Photograph the area of interest; preferably the entire microcircuit

- Remove the passivating and interdielectric layers so that the bare silicon surface is exposed (see Chapter III-N)

- Remove the metallization layers (see Chapter III-N)

- Remove any remaining dielectric layers that may be under the metallization areas (see Chapter III-N)

- Stain the diffusion areas on the surface of the silicon (see Chapter III-N) referring to Figure 2.c., it can be seen that staining reveals diffused areas

- Photograph the stained microcircuit

- Comparison of the "before" and "after" photographs will enable the failure analyst to trace the electrical interconnections on the microcircuit

o Tracing by Field Effect Liquid Crystal. It is virtually impossible to completely trace and map out electrical signal paths through many complex microcircuits, such as microprocessors.

A technique exists, though still in its infancy, involving a liquid crystal procedure by which it is possible to identify function blocks in complex microcircuits. See Chapter III-H for a description of this procedure.

° Tracing by Microbeam Techniques. Circuit tracing can be done through the use of the scanning electron microscope (see Chapter III-P for details).

b) Locate the Failure Site. During circuit tracing, a failure site may become obvious. Figure 3 shows an output transistor failure that was located using visual techniques. The output pad on the microcircuit was identified, and the metallization traced back to the output device. The failure was a collector-emitter short, and the failure area in the emitter can be seen where the metal was vaporized due to heat generation.

Often, however, failure sites are not so obvious visually. In this case, circuit performance must be analyzed in order to localize the most probable area in which to look for a failure.

c) Isolate the Failure Area. Once having located the probable failure area, it becomes necessary to isolate individual devices in the circuit. For details on isolation techniques, see Chapter III-A.

d) Element Probing. Individual circuit elements must be probed to determine their electrical parameters and thus verify failure. For details on element probing, see Chapter III-A.

FIGURE 3. BIPOLAR ECL FAILURE SITE. SHORTED AREA FROM EMITTER TO COLLECTOR CAN BE SEEN

3. Die Handling and Storage Methods and Equipment. At times the failure analyst is called upon to handle microcircuit die, or chips, that have not been individually packaged. For instance, many hybrid packages employ more than one microcircuit, and failed microcircuits are routinely replaced in these hybrid modules. Some of the things that should be kept in mind when dealing with microcircuits in chip form are:

- Always handle die with vacuum pickup equipment to avoid mechanical damage
- Store and transport die in specially compartmentalized containers
- Die should be kept in desiccator when not being analyzed to prevent contamination from, for instance, humidity

When dealing with individual die, the failure analyst will commonly mount the die on a laboratory microscope glass slide using such materials as epoxy, RTV, silicone adhesive double sided tape, apiezon wax, Eastman 910, etc. This provides several advantages during analysis, such as:

- Ease in microscope examination
- Allows chemical cleaning or etching to be done simply without losing die
- Allows die to be probed with micromanipulator probes easily
- Generally facilitat[e] die h[a]ndling and transport during analysis

It should be kept in mind that chemical cleaning and etching procedures may cause degradation of the bonding material used to adhere a die to a glass slide. There is, therefore, a danger of losing a die during chemical procedures if precautions are not taken. For instance, chemical etching solutions containing hydrofluoric acid (HF) are extremely harsh and will eventually weaken almost any bonding material. In addition, HF etches glass and if die bonding material is itself not weakened, the acid could still etch the glass from under a bond area, resulting in loss of the die.

4. Precision Weight Measurement (Analytical Balances). Precision weight measurements sometimes become necessary in failure analysis. Epoxy mixing for sample mounting, hermeticity weight gain tests, dielectric loss in electrolytic capacitors, etc., are all examples where precision weight measurements are necessary. Precision instruments are generally of two types:

a) Conventional Two Pan. These balances are typically used for measurement in the range of 0.1 to 200 grams with sensitivity of 0.1 mg. Standard weights are carefully placed on one of the pans with the sample to be weighed in the other pan. Additional small weight increments are either added or subtracted by means of a calibrated scale located on the balance arm until balance is achieved. The sample weight is then the sum of the reference weights plus the incremental small weight indicated on the balance arm.

b) Single Pan. Single pan instruments are considerably more expensive than two pan instruments. These balances utilize a substitution method which provides constant sensitivity at all loads and an accuracy free from beam length errors. The standardized weights are an integral part of the instrument and are changed by means of front panel controls. The measurement range is typically 0.1 mg to 150 grams, with 0.1 mg sensitivity. Figure 4 shows a typical single pan balance.

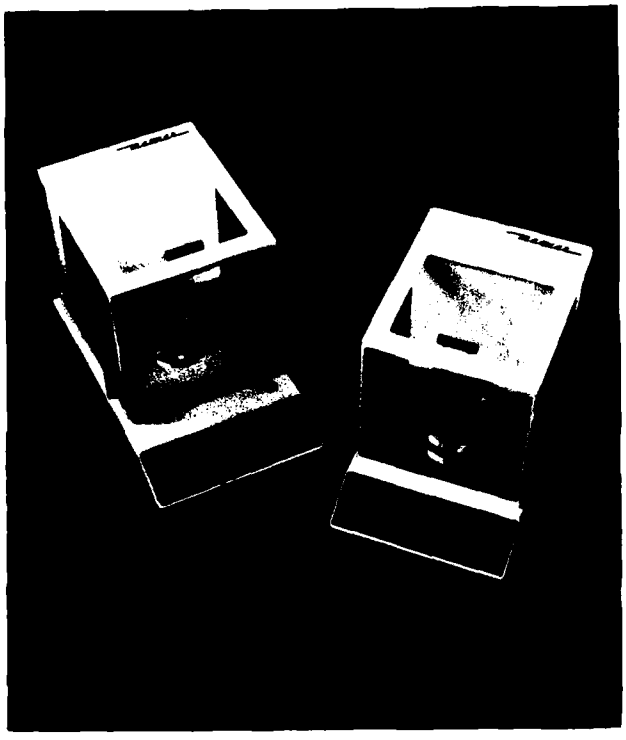


FIGURE 4. TYPICAL SINGLE PAN BALANCE

FIGURE 5. X-RAY DIFFRACTION EQUIPMENT

5. X-ray Diffraction. X-ray diffraction is frequently necessary to identify crystalline compounds present in deposits found on various parts of electronic circuits. Corrosion products formed as a result of exposure of a metal surface to a reactive chemical is a typical example. Knowledge of the composition of the compound formed can help to identify the reactive material involved. In most cases, the deposit is removed from the circuit under observation of a low power microscope and mounted on a 0.25 mm glass rod using a thin layer of amorphous grease. The minimum volume of material which may be reliably analyzed is equivalent to a sphere approximately 1 mm in diameter. A reference file of JCPDS data consisting of thousands of X-ray diffraction patterns aids in the identification (see Reference 2). Typical X-ray diffraction equipment is shown in Figure 5.

6. Emission Spectrograph. When the presence of trace amounts of metallic elements in a material is suspected, the emission spectrograph is a very useful instrument. The material to be analyzed is burned in a carbon arc, and the emission lines of any element present are recorded on a photographic plate. Elements may be detected in the parts per million range in most matrices with sample sizes as small as 0.5 mg. Quantitative analysis is possible by comparison with the proper standards. Due to the nature of the analysis, the test is destructive to the material being analyzed.

In some instances, a laser microprobe for analyzing a spot as small as 0.25 mm may be used to vaporize the desired material into the arc for analysis. The laser microprobe makes possible the generation of a spectral emission without direct contact with or preparation of the sample, the derivation of a spectrum from a precisely selected area of the sample, and the direct analysis of both non-conductors and conductors.

Typical equipment used in emission spectrograph measurements is shown in Figure 6.

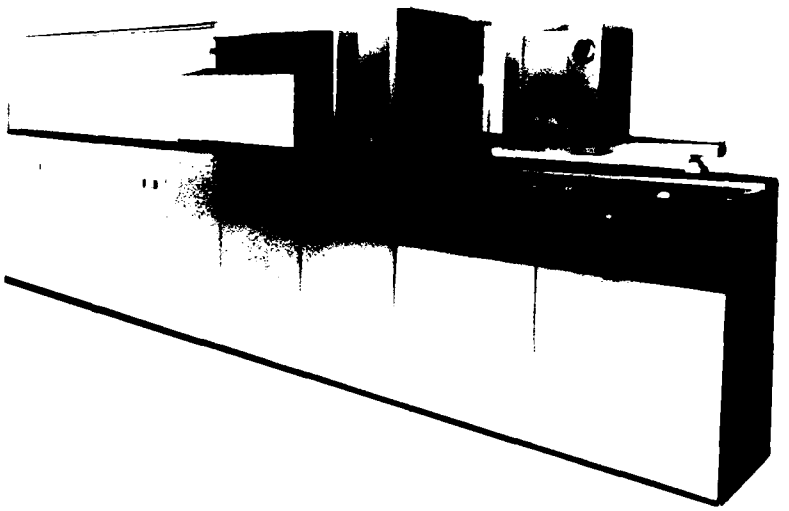


FIGURE 6. TYPICAL EMISSION SPECTROGRAPH EQUIPMENT

7. Atomic Absorption Spectroscopy. Quantitative determination of metallic elements can be made in water or other suitable liquid solution in the 10-100 parts per billion range using the standard flame technique of atomic absorption. By adding the graphite furnace attachment, several orders of magnitude improvement in the sensitivity is possible with many elements. Since each element has a separate lamp, it is desirable that the identity of the elements, whose quantitative level is sought, be predetermined by an alternate technique. Figures 7 and 8 show typical equipment.

In a typical application to electronics, traces of sodium may be determined in polymer packages or protective layers by first igniting the material in air to remove the organic content followed by solution of the residue in a small amount of water. It is also possible to introduce a solid sample directly into the graphite furnace. The level of the element detected is compared with the level of the same element in a standard solution of accurately known concentration, thereby giving very quantitative data.

8. Thermal Analysis. Several of the thermoanalytical techniques are useful in characterizing polymers, laminated boards and other materials which might be found in an electronic circuit package. For instance, matching expansion coefficients among the several materials in a package is one of the important contributions to the reliability of a circuit. Thermomechanical Analysis (TMA) provides a continuous trace of the change in dimension of a sample as a function of temperature. From this trace, the linear expansion coefficient may be calculated and the glass transition detected. Since at the glass transition a polymer becomes more flexible, it is often important to have the glass transition occur above the normal operating temperature. Increases in the temperature at which the glass transition occurs in a polymer with repeated heating cycles indicates a lack of cure. Samples from 1 mm to about 15 mm in length and about 10 mm in diameter may be measured. Typical equipment is shown in Figure 9.

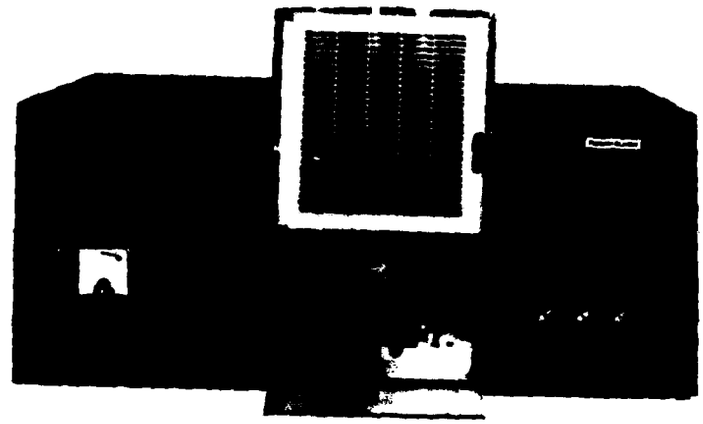


FIGURE 7. ATOMIC ABSORPTION SPECTROMETER
(Standard Flame Technique)

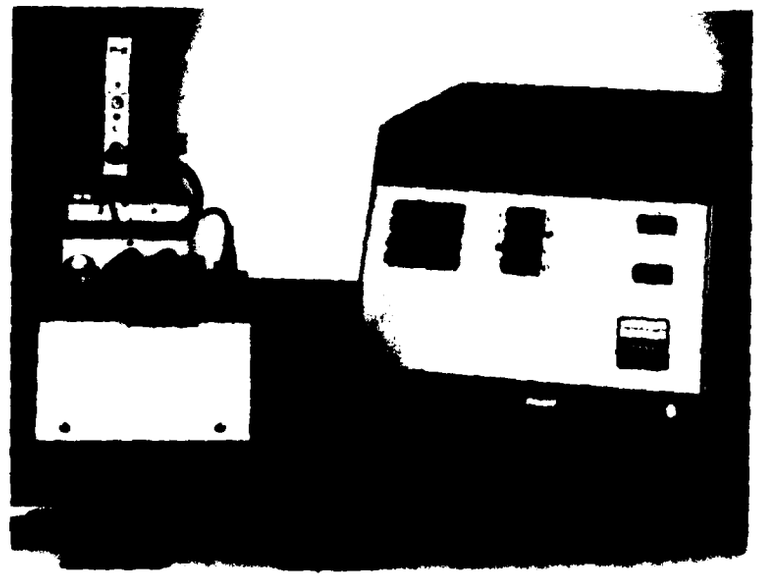


FIGURE 8. GRAPHITE FURNACE ATTACHMENT WITH PROGRAMMER
(Perkin-Elmer)

Differential Scanning Calorimetry (DSC) (see Figure 10) also will detect the heat associated with the glass transition or other transitions that occur during a heating cycle by comparing the heat flow into or out of a sample compared to that of a standard such as alumina. Severely undercured materials will also show an exotherm at the cure temperature. One milligram or more of most materials is needed for reproducible results.

Thermogravimetry (TGA) (see Figure 11) is useful in detecting the presence of low temperature volatiles particularly in polymers by continuously weighing the sample as a function of temperature. A sample of material weighing 1 mg or more is placed in a platinum basket on the end of a quartz rod attached to an electro balance. The basket with a thermocouple adjacent is inserted into a furnace with a programmed temperature cycle.

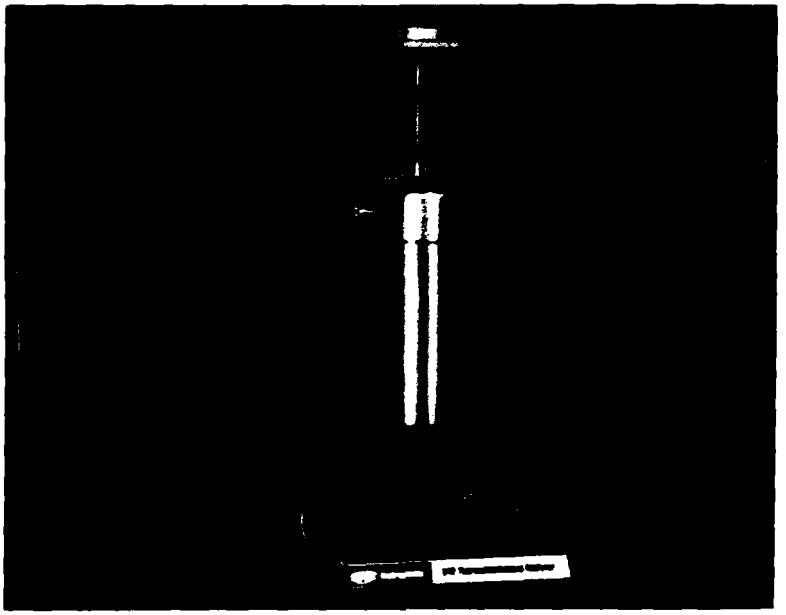


FIGURE 9. THERMOMECHANICAL ANALYZER MEASURES EXPANSION COEFFICIENT AND GLASS TRANSITION (DuPont)

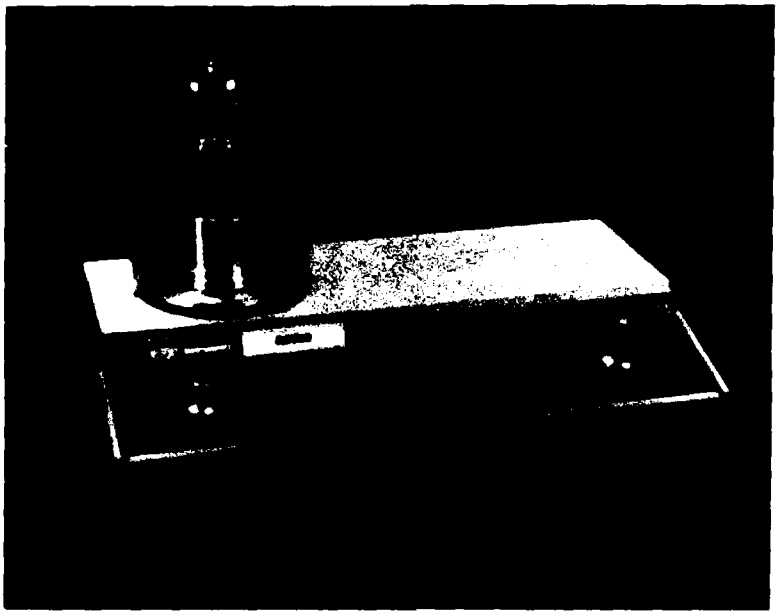


FIGURE 10. DIFFERENTIAL SCANNING CALORIMETER MEASURES TRANSITIONS AND LACK OF CURE (DuPont)

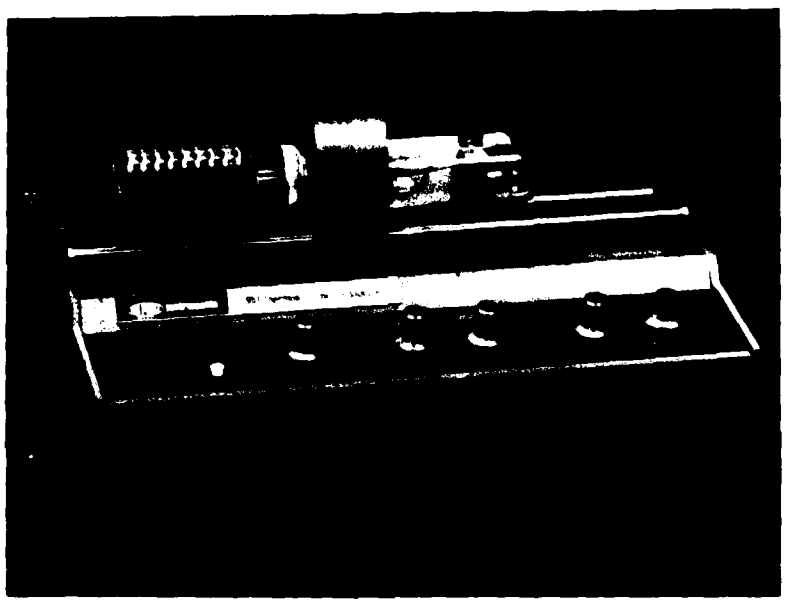


FIGURE 11. THERMOGRAVITY EQUIPMENT

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EQUIPMENT

Vacuum Die Handling Equipment	$ 25
Cole Parmer Inst. Co., Chicago, Illinois Sargent-Welch Scientific Co., Springfield, NJ	
Storage Desiccator	$ 150
Fisher Scientific Co., Pittsburgh, PA Scientific Products, McGraw Park, Ill. Sargent-Welch Scientific Co., Springfield, NJ	
Two Pan Analytical Balance	$ 690 - 900
Fisher Scientific Co., Pittsburgh, PA Scientific Products, McGraw Park, Ill. Sargent-Welch Scientific Co., Springfield, NJ Mettler Inc., Princeton, NJ	
Single Pan Automatic Balance	$1500 - 3000
Fisher Scientific Co., Pittsburgh, PA Scientific Products, McGraw Park, Ill. Sargent-Welch Scientific, Co., Springfield, NJ Scientech Optical Corp., Whippany, NJ	
Atomic Absorption Equipment	
Atomic Absorption Spectrometer	$14,000
Graphite Furnace for AAS	$ 8,000
Perkin Elmer Co., Norwalk, Conn.	
X-Ray Diffraction Equipment	$50,000
Diano Corp., Woburn, Mass.	
Emission Spec, Equipment	
Basic Equipment	$35,000
Laser Probe Attachment	$25,000
Jarrell-Ash, Neutonville, Mass.	
Thermal Analyzer Equipment	
Programmer/Recorder	$14,000
DSC Module	$ 8,000
TGA Module	$10,000
TMA Module	$ 8,000

9. Environmental/Mechanical Accelerated Stress Testing Facilities and Test Methods.

Whether performing analysis on existing failures or stressing devices to accelerate failures, environmental/mechanical stress facilities are important to support device failure analysis activities. Thermal, electrical, and humidity factors are most often used to accelerate device failure mechanisms which normally occur under use conditions; however, care must be taken to avoid generating non-typical problems at high stress levels. In addition to environmental and mechanical factors, many failure mechanisms are time dependent. Thus, failure analysis often requires a facility to simulate stress conditions over a period of time. Selected stress conditions and durations vary according to such things as the device technology, design, packaging, and suspected or anticipated failure mechanisms.

A formalized description of standard environmental and mechanical stress and test procedures is given in MIL-STD-883B Series 1000 Methods and selected Series 2000 Methods (Table I). It is sufficient here to list those factors most frequently employed. They are (1) electrical, (2) elevated temperature, (3) humidity, (4) temperature cycle, (5) thermal shock, (6) simultaneous combinations of these factors, and (7) sequential combinations of these factors.

Electrical bias can be either static or dynamic exercise. While static bias is easiest, for microelectronic devices of moderate complexity or inherently dynamic devices there is considerable concern regarding static bias effectiveness, i.e., the percentage of internal circuit nodes excercised. Dynamic testing is the alternative; however, it need not fully exercise all possible device states nor operate at maximum device frequency. Equipment required to bias/exercise microelectronic devices is generally commercially available or can be built in a general components lab.

Thermal acceleration at elevated temperature requires special materials. Operational life of wire insulation, sockets, and printed circuit boards of normally employed materials soon degrades. Materials that are currently available such as teflon insulated wire, silicone

TABLE I

MIL-STD-883B TEST METHODS

Method No.	
	Environmental tests
1001	Barometric pressure, reduced (altitude operation)
1002	Immersion
1003	Insulation resistance
1004.2	Moisture resistance
1005.2	Steady state life
1006	Intermittent life
1007	Agree life
1008.1	High-temperature storage
1009.2	Salt atmosphere (corrosion)
1010.2	Temperature cycling
1011.2	Thermal shock
1012	Thermal characteristics
1013	Dew point
1014.2	Seal
1015.2	Burn-in test
1016	Life/reliability characterization tests
1017	Neutron irradiation
1018	Internal water-vapor content
	Mechanical tests
2001.2	Constant acceleration
2002.2	Mechanical shock
2003.2	Solderability
2004.2	Lead integrity
2005.1	Vibration fatigue
2006.1	Vibration noise
2007.1	Vibration, variable frequency
2008.1	Visual and mechanical
2009.1	External visual
2010.3	Internal visual (monolithic)
2011.2	Bond strength
2012.2	Radiography
2013	Internal visual
2014	Internal visual and mechanical
2015.1	Resistance to solvents
2016	Physical dimensions
2017.1	Internal visual (hybrid)
2018	Scanning electron microscope (SEM) inspection of metallization
2019.1	Die shear strength
2020	Particle impact noise detection test
2021	Glassivation layer integrity
2022	Meniscograph solderability

sockets, and polyimide printed circuit boards allow reasonable life to 250°C. A choice of wire, socket, board and associated conductor materials is available from a number of manufacturers. This is also true of low temperature operation where typical materials experience performance problems.

Thermal shock temperature extremes frequently involve temperatures from -65°C to +150°C or more, requiring special fluids and bath equipment. As in thermal acceleration tests, equipment and supplies are available to perform these shock tests.

There are trade magazines which specifically address reliability testing such as "Electronics Test" or "Evaluation Engineering" and seminars and symposia which provide media for product announcement, description and exchange of techniques and testing experiences. Individual manufacturers also make available literature offering good information to users.

Stress testing techniques for semiconductor technology devices is undergoing dramatic changes both required and forced by the complexity and increased functional capabilities of modern devices. Integration of minicomputers with test beds will enable tremendous strides in gathering and analyzing functional and parametric data during actual stressing. For digital devices in particular, computers will also lead to greater flexibility and reduced set-up time by virtue of the fact that digital microprocessors and microcomputers are basically software programmable pattern generators. Figure 1 shows the application of a microprocessor evaluation kit to exercise and monitor semiconductor memories during a thermal stress test. Figure 2 illustrates the usage of a microprocessor evaluation kit to exercise devices while a minicomputer monitors and controls the testing and data acquisition/analysis. Such control will allow functional characterization to be performed at the chamber instead of requiring periodic device removal for precision automated test equipment (ATE) testing. It will also enable monitoring of additional parametric data to indicate when more extensive precision ATE measurements need to be performed. These systems are expected to be commercially available in the next few years.

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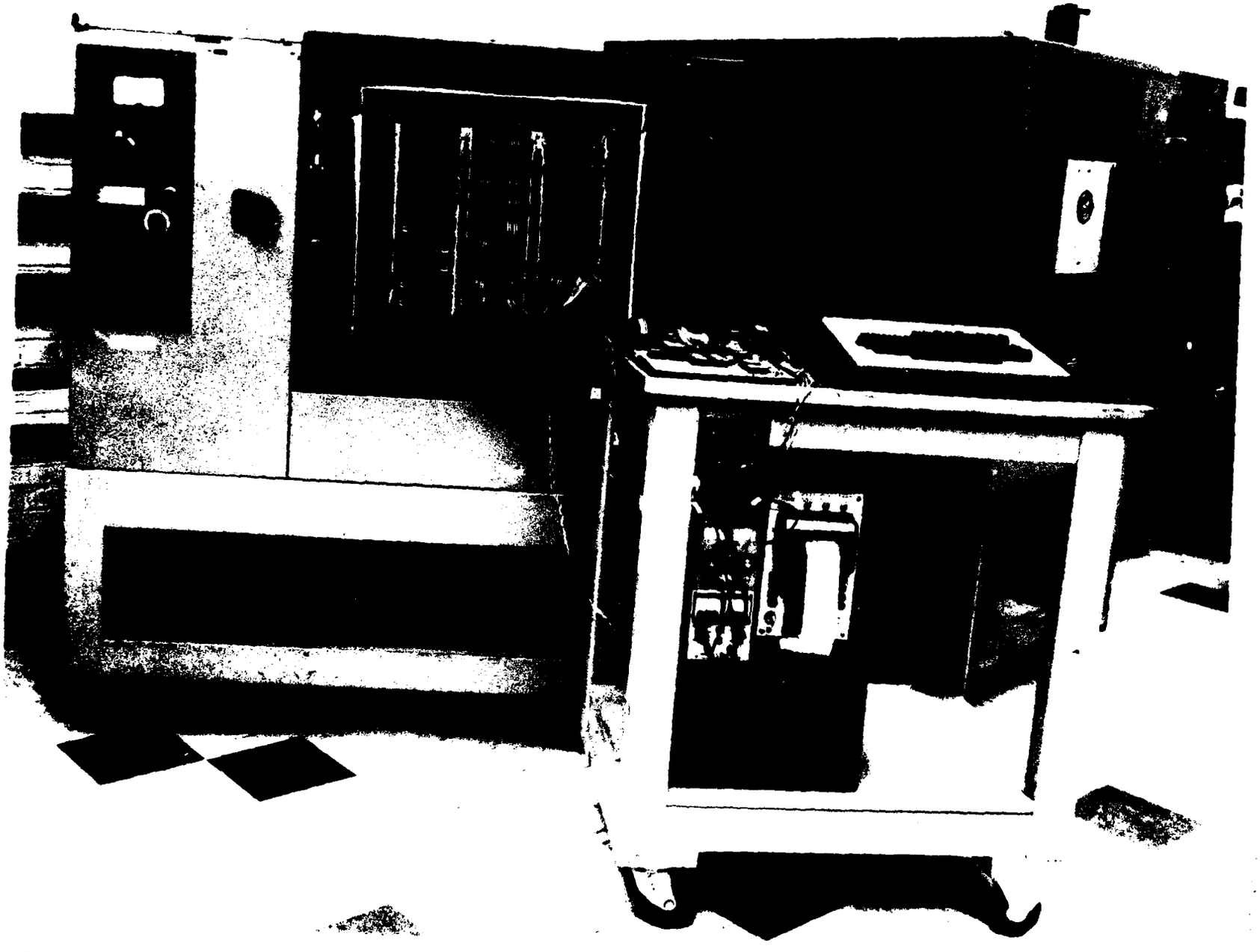

Figure 1. Accelerated temperature test utilizing a microprocessor evaluation kit for stimulus and monitoring

Figure 2. Accelerated temperature test utilizing a microprocessor evaluation kit for stimulus and minicomputer for monitoring and control

SECTION IV

LABORATORY SAFETY PROCEDURES

IV. LABORATORY SAFETY PROCEDURES

A. Chemical Usage Precautions, Disposal and Emergency Actions. Neglect of adequate safety procedures and precautions is one of the most common errors found in the laboratory today. Generally, small quantities of dangerous chemicals are stored and used in the failure analysis laboratory. This fact seems to contribute largely to the laxity often found in some laboratories.

Listed below are some of the general guidelines that should be followed in the handling and use of chemicals:

- Never remove chemicals from storage areas or handle chemicals without proper protective items:
  - Protective gloves - rubber, neoprene, etc.
  - Eye protection - safety glasses or face shield
  - Body protection - chemically resistive laboratory coat or apron
- Never transport breakable chemical containers unless enclosed in specially designed plastic carrying containers.
- Never dispense, mix, use, or dispose of laboratory chemicals without proper ventilation hoods and chemical sinks.
- Be aware of the potential dangers of the chemicals being handled or used. Table I lists excerpts from a reference source giving useful information on the dangers presented by some of the chemicals normally found in the failure analysis laboratory (Reference 2).

Regardless of strict adherence to safety regulations and practices, human error almost invariably leads to accidents. Listed below are some of the safety equipment items that are vital to a

chemical laboratory and some of the emergency actions that should be followed in the event of an accident:

- A respirator should be available in the immediate vicinity in the event that the atmosphere outside ventilation hoods is exposed to toxic fumes, such as large amounts of spilled acids.

- A full body deluge shower should be available in the laboratory in the event that large amounts of skin area are exposed to corrosive chemicals.

- Easily activated flowing water eye wash stations and/or plastic squeeze bottle portable eye wash equipment should be positioned by chemical handling and use locations.

- Fire extinguishers should be available, particularly around solvent storage and use areas.

- Kits containing spill cleanup and disposal materials should be available. These kits contain materials for controlling acid, caustic, and flammable solvent spills.

- First aid kit, stretcher, and blanket should be available.

- Individuals should not work alone in chemical laboratories.

- Emergency procedures are largely governed by common sense. For instance, if acid splashes into someone's eyes, then a companion should get the victim to an eye wash station as quickly as possible.

- Notify medical personnel, fire fighting personnel, etc., as appropriate.

The majority of laboratories in operation at present employ outside contracting firms to dispose of used chemicals. This is particularly true due to recent Environmental Protection Agency requirements. For example, it is now mandatory that units or containers of waste be labeled carefully not only as to contents but also to include percentage of contents.

The procedures in collecting and storing used chemicals should perhaps be more definitive and more stringently adhered to than dispensing because of the inherent dangers of producing toxic or flammable byproducts when mixing chemicals. Knowledgeable chemists should be consulted before waste chemicals are mixed.

B. Toxic Materials Handling. Generally speaking, all the chemicals, liquid and solid form, used in failure analysis are either themselves directly toxic or are capable of producing toxic byproducts under the proper conditions. Perhaps a more meaningful designation would be a division of materials into "more" or "less" toxic.

Table I lists dangerous properties of some of the chemicals commonly found in the failure analysis laboratory (see Reference 2).

NOTE: The numerical Toxic Hazard Ratings given in Table I correspond to:

0 - NONE (a) No harm under any conditions; (b) Harmful only under unusual conditions or overwhelming dosage.

1 - SLIGHT: Causes readily reversible changes which disappear after end of exposure.

2 - MODERATE: May involve both irreversible and reversible changes; not severe enough to cause death or permanent injury.

3 - HIGH: May cause death or permanent injury after very short exposure to small quantities.

U - UNKNOWN: No information on humans considered valid by authors of Reference 2.

As an example of the "more" or "less" toxic nature of chemicals, consider the difference in toxic ratings for hydrochloric and hydrofluoric acids. A comparison of these acids in Table I shows that hydrofluoric acid is considerably more dangerous than hydrochloric acid. A further example from Table I shows that the cyanide salts, such as potassium cyanide, sometimes used in failure analysis work, are not extremely dangerous unless they are directly ingested or are allowed to come in contact with an acid. Contact with an acid will produce hydrocyanic acid, which is deadly.

Therefore, degrees of toxicity do exist among the chemicals used in the laboratory, and appropriate special handling precautions should be observed for the more toxic materials. OSHA and any of several industrial handbooks are sources of toxicity of chemicals.

TABLE I
DANGEROUS PROPERTIES OF SOME OF THE CHEMICALS FOUND IN THE FAILURE ANALYSIS LABORATORY

ACETIC ACID
General Information
Synonyms: Methane carboxylic acid, vinegar acid, ethanoic acid.
Description: Clear, colorless liquid, pungent odor.
Formula: CH_3COOH
Constants: Mol wt: 60.05, mp: 16.7°C, bp: 118.1°C, flash p: 109°F (C.C.), lel = 5.4%, uel = 16.0%, ai: 212°F, d: 1.049 at 20°/4°C, autoign. temp.: 800°F, vap. press.: 11.4 mm at 20°C, vap. d: 2.07.
Hazard Analysis
Toxic Hazard Rating:
Acute Local: Irritant 3, Ingestion 3, Inhalation 2.
Acute Systemic: U.
Chronic Local: Irritant 2.
Chronic Systemic: U.
TLV: ACGIH, 10 ppm in air, 25 milligrams per cubic meter of air.
Toxicology: Caustic, irritating, can cause burns, lachrymation and conjunctivitis. It attacks the skin easily and can cause dermatitis and ulcers. Inhalation causes irritation of mucous membranes. In case of contact with skin, eyes or clothing, immediately flush skin or eyes with plenty of water and remove all contaminated clothing. If swallowed give magnesia, chalk or whiting in water (Section 1).
Note: It is a miscellaneous and/or general purpose food additive which can migrate to food from packaging materials. A common air contaminant (Section 4).
Fire Hazard: Moderate, when exposed to heat or flame; can react vigorously with oxidizing materials (Section 6).
Spontaneous Heating: No.
Caution: Particularly dangerous in contact with chromic acid, sodium peroxide, nitric acid.
Explosion Hazard: Moderate, when exposed to flame.
Disaster Hazard: Dangerous; when heated to decomposition, emits toxic fumes.

ACETONE
General Information
Synonyms: Dimethyl ketone; ketone propane; propanone.
Description: Colorless liquid; fragrant mintlike odor.
Formula: CH_3COCH_3.
Constants: Mol wt: 58.08, mp: −94.6°C, bp: 56.48°C, ulc = 90, flash p: 0°F (C.C.), lel = 2.6%, uel = 12.8%, d: 0.7972 at 15°C, autoign. temp.: 1000°F, vap. press.: 400 mm at 39.5°C, vap. d: 2.00.
Hazard Analysis
Toxic Hazard Rating:
Acute Local: Irritant 1; Ingestion 2; Inhalation 2.
Acute Systemic: Ingestion 2; Inhalation 2, Skin Absorption 2.
Chronic Local: Irritant 1.
Chronic Systemic: Ingestion 1, Inhalation 1, Skin Absorption 1.
TLV: ACGIH; 1000 parts per million in air, 2400 milligrams per cubic meter of air.
Toxicology: Acetone is narcotic in high concentrations. In industry, no injurious effects from its use have been reported, other than the occurrence of skin irritations resulting from its de-fatting action or headache from prolonged inhalation. A food additive permitted in food for human consumption (Section 10). A common air contaminant. See Section 4.
Fire Hazard: Dangerous, when exposed to heat or flame.
Explosion Hazard: Moderate, when vapor is exposed to flame.
Disaster Hazard: Dangerous, due to fire and explosion hazard; can react vigorously with oxidizing materials.

AMMONIUM BIFLUORIDE
General Information
Synonym: Ammonium hydrogen fluoride.
Description: White crystals.
Formula: NH_4FHF.
Constants: Mol wt: 57.05, d: 1.21 at 12°C/12°C (liquid).
Hazard Analysis
Toxicity: See fluorides.
Disaster Hazard: See fluorides.

AMMONIUM CHLORIDE
General Information
Synonym: Sal ammonia.
Description: White crystals.
Formula: NH_4Cl.
Constants: Mol wt: 53.50, mp: 520°C, bp: 337.8°C, d: 1.520, vap. press.: 1 mm at 160.4°C (sublimes).
Hazard Analysis
Toxic Hazard Rating:
Acute Local: Irritant 1, Ingestion 1, Inhalation 1.
Acute Systemic: U.
Chronic Local: Irritant 1.
Chronic Systemic: Ingestion 1.
Toxicology: A substance migrating to food from packaging materials. Large doses cause nausea, vomiting and acidosis.

AMMONIUM FLUORIDE
General Information
Description: White crystals.
Formula: NH_4F.
Constants: Mol wt: 37.04, mp: sublimes, d: 1.315.
Hazard Analysis and Countermeasures
See fluorides.

AMMONIUM HYDROXIDE
General Information
Synonyms: Aqua ammonium; water of ammonia; aqua ammonia; ammonium hydrate.
Description: Colorless liquid.
Formula: NH_4OH.
Constants: Mol wt: 35.05, mp: −77°C.
Hazard Analysis
Toxic Hazard Rating:
Acute Local: Irritant 2; Ingestion 3; Inhalation 2.
Acute Systemic: U.
Chronic Local: Irritant 2.
Chronic Systemic: U.
A general purpose food additive which migrates to food from packaging materials (Section 10).
Fire Hazard: Slight; when heated, it emits toxic fumes; can react with oxidizing materials (Section 6).
Disaster Hazard: Dangerous; emits irritating fumes and liquid can inflict burns. Use with adequate ventilation.

AMMONIUM PERSULFATE
General Information
Synonym: Ammonium peroxydisulfate.
Description: White crystals.
Formula: $(NH_4)_2S_2O_8$.
Constants: Mol wt: 228.20, mp: decomposes at 120°C, d: 1.982.
Hazard Analysis
Toxic Hazard Rating:
Acute Local: Irritant 1, Ingestion 1, Inhalation 1.
Acute Systemic: U.
Chronic Local: Irritant 1.
Chronic Systemic: U.
Fire Hazard: Moderate, by chemical reaction with reducing agents (Section 6).
Caution: A powerful oxidizer.
Explosion Hazard: Slight; oxygen released quietly in a fire, probably at a low temperature.
Disaster Hazard: Dangerous. See sulfates. Can react vigorously with reducing agents.

AMMONIUM SULFIDE
General Information
Synonym: Ammonium polysulfide.
Description: Yellow, hygroscopic crystals.
Formula: $(NH_4)_2S$.
Constants: Mol wt: 68.2, mp: decomposes.
Hazard Analysis
Toxicity: See sulfides. Evolves hydrogen sulfide on contact with acid or acid fumes. Fatal poisoning has been reported from use in hair waving lotions.
Fire Hazard: See sulfides.
Explosion Hazard: See sulfides.
Disaster Hazard: See sulfides.

BENZENE

General Information

Synonyms: Benzol, phenyl hydride; coal naphtha.

Description: Clear colorless liquid.

Formula: C_6H_6.

Constants: Mol wt: 78.11, mp: 5.51°C, bp: 80.093°-80.094°C, flash p: 12°F (C.C.), d: 0.8794 at 20°C, autoign. temp.: 1044°F, lel: 1.3%, uel: 7.1%, vap. press.: 100 mm at 26.1°C, vap. d.: 2.77.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 2; Ingestion 1; Inhalation 1.

Acute Systemic: Ingestion 2, Inhalation 2; Skin Absorption 2.

Chronic Local: 0.

Chronic Systemic: Ingestion 3; Inhalation 3; Skin Absorption 3.

TLV: ACGIH (recommended): 25 parts per million in air; 80 milligrams per cubic meter of air. May be absorbed via the skin.

Toxicology: Poisoning occurs most commonly through inhalation of the vapor, though benzene can penetrate the skin, and thus contribute to poisoning.

Locally, benzene has a comparatively strong irritating effect producing erythema and burning, and in more severe cases, edema and even blistering (Section 9). Exposure to high concentrations of the vapor (3,000 ppm or higher) results from accidents such as failure of equipment or spillage. Such exposure, while rare in industry, may result in acute poisoning, characterized by the narcotic action of benzene on the central nervous system. The anesthetic action of benzene is similar to that of other anesthetic gases, consisting of a preliminary stage of excitation followed by depression and, if exposure is continued, death through respiratory failure.

The chronic, rather than the acute form of benzene poisoning is important in industry; it has a toxic action on the blood-forming tissues. There is no specific blood picture occurring in cases of chronic benzol poisoning.

The bone marrow may be hypoplastic, normal, or hyperplastic, the changes being reflected in the peripheral blood. Anemia, leucopenia, macrocytosis, reticulocytosis, thrombocytopenia, high color index, and prolonged bleeding time may be present. Cases of myeloid leukemia have been reported. For the supervision of the worker, repeated blood examinations are necessary, including hemoglobin determinations, white and red cell counts and differential smears. Where a worker shows a progressive drop in either red or white cells, or where the white count remains below 5,000 per cu. mm., or the red count below 4.0 million per cu. mm., on two successive monthly examinations, he should be immediately removed from exposure. With this method of supervision of the worker, no permanent damage will result to the blood-forming system.

Following absorption of benzene, elimination is chiefly through the lungs, when fresh air is breathed. The portion that is absorbed, is oxidized, and the oxidation products are combined with sulfuric and glycuronic acids and eliminated in the urine. This may be used as a diagnostic sign. Benzene has a definite cumulative action, and exposure to relatively nigh concentrations are not serious from the point of view of causing damage to the blood-forming system, provided that the exposure is not repeated. On the other hand, daily exposure to concentrations of 100 ppm or less will usually cause damage if continued over a protracted period of time.

In acute poisoning, the worker becomes confused and dizzy, complains of tightening of the leg muscles and of pressure over the forehead, then passes into a stage of excitement. If allowed to remain in exposure, he quickly becomes stupefied and lapses into coma. In nonfatal cases, recovery is usually complete and no permanent disability occurs.

In chronic poisoning the onset is slow, with the symptoms vague; fatigue, headache, dizziness, nausea and loss of appetite, loss of weight, and weakness are common complaints in early cases. Later, pallor, nosebleeds, bleeding gums, menorrhagia, petechiae and purpura may develop. There is great individual variation in the signs and symptoms of chronic benzene poisoning. Note: Benzene is a common air contaminant.

Fire Hazard: Dangerous; when exposed to heat or flame; can react vigorously with oxidizing materials.

Spontaneous Heating: No.

Explosion Hazard: Moderate, when its vapors are exposed to flame. Use with adequate ventilation.

Disaster Hazard: Dangerous; highly flammable.

BENZYL ALCOHOL

General Information

Synonyms: Hydroxytoluene; phenyl carbinol.

Description: Water-white liquid; faint aromatic odor.

Formula: $C_6H_5CH_2OH$.

Constants: Mol wt: 108.13, mp: −15.3°C, bp: 205.7°C, flash p: 213°F (C.C.), d: 1.050 at 15°/15°C, autoign. temp.: 817°F, vap. press.: 1 mm at 58.0°C, vap. d.: 3.72.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 1; Allergen 1; Ingestion 1; Inhalation 1.

Acute Systemic: Ingestion 1; Inhalation 1; Skin Absorption 1.

Chronic Local: Irritant 1; Allergen 1.

Chronic Systemic: U.

Toxicology: In addition to local irritation of skin and mucous membranes it can cause headaches, vertigo, nausea, vomiting and diarrhea.

Fire Hazard: Slight, when exposed to heat or flame; can react with oxidizing materials.

Spontaneous Heating: No.

BORIC ACID

General Information

Synonyms: Boracic acid; o-boric acid.

Description: White crystals or powder.

Formula: H_3BO_3.

Constants: Mol wt: 61.84, mp: 185°C (decomp.) $-1\frac{1}{2}H_2O$ at 300°C, d: 1.435 at 15°C.

Hazard Analysis

Toxicity: See boron compounds.

BORON COMPOUNDS

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Ingestion 2; Inhalation 2.

Acute Systemic: U.

Chronic Local: 0.

Chronic Systemic: Ingestion 2; Inhalation 2; Skin Absorption 2.

Toxicology: Not highly toxic and therefore not considered an industrial poison. Used in medicine as sodium borate, boric acid, or borax, which is also a common cleaner. Fatal poisoning of children has been caused in some instances by the accidental substitution of boric acid for powdered milk. The medical literature reveals many instances of accidental poisoning due to boric acid, oral ingestion of borates or boric acid, and presumably absorption of boric acid from wounds and burns. The fatal dose of orally ingested boric acid for an adult is somewhat more than 15 or 20 grams and for an infant 5 to 6 grams.

Boron is one of a group of elements, such as lead, manganese and arsenic, which affects the central nervous system. Boron poisoning causes depression of the circulation, persistent vomiting and diarrhea, followed by profound shock and coma. The temperature is subnormal and a scarletina-form rash may cover the entire body. Boric acid intoxication can come about from absorbing toxic quantities from ointments applied to burned areas or to wounds involving loss or damage to such areas of skin, but it is not absorbed from intact skin. When a 5% boric acid solution is used to irrigate body cavities most of the boric acid is absorbed by the tissues. Continuous irrigation of the body cavities with solutions containing boron can be dangerous.

BROMINE

General Information

Description: Rhombic crystals or dark-red liquid.
Formula: Br_2.
Constants: Mol wt: 159.83, fp: −7.3°C, bp: 58.73°C, d: 2.928 at 59°C; 3.12 at 20°C, vap. press.: 175 mm at 21°C; 1 atm at 58.2°C, vap. d.: 5.5.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: U.
- Chronic Local: Irritant 2.
- Chronic Systemic: Ingestion 2; Inhalation 2.

TLV: ACGIH (recommended): 0.1 parts per million in air; 0.7 mg/cubic meter of air.
Toxicology: The action of bromine is essentially the same as that of chlorine, being an irritant to the mucous membranes of the eyes and upper respiratory tract. Severe exposures may result in pulmonary edema. Usually, however, the irritating qualities of the chemical force the workman to leave the exposure before serious poisoning can result. Chronic exposure similar to therapeutic ingestion of excessive bromides. See also bromides. Regular physical examinations should be made upon people who work with bromine.
Radiation Hazard: Section 5. For permissible levels, see Table
- Artificial isotope ^{82}Br, half life 36 h. Decays to stable ^{82}Kr by emitting beta particles of 0.44 MeV and others. Also emits gamma rays of 0.55–1.47 MeV.

Fire Hazard: Moderate; in the form of liquid or vapor by spontaneous chemical reaction with reducing materials (Section 6).
Caution: May ignite a combustible material upon contact. A very powerful oxidizer.
Disaster Hazard: Highly dangerous; when heated, it emits highly toxic fumes; it will react with water or steam to produce toxic and corrosive fumes; and it can react vigorously with reducing materials.

2-BUTANONE

General Information

Synonym: Methylethyl ketone.
Description: Colorless liquid, acetone-like odor.
Formula: $CH_3COCH_2CH_3$.
Constants: Mol wt: 72.10, bp: 79.57°C, fp: −85.9°C, lel: 1.8%, uel: 10%, flash p: 22°F (T.O.C.), d: 0.80615 at 20°/20°C, vap. press.: 71.2 mm at 20°C, autoign. temp.: 960°F, vap. d.: 2.41.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 1; Ingestion 1; Inhalation 1.
- Acute Systemic: Inhalation 2.
- Chronic Local: Irritant 1.
- Chronic Systemic: U.

Toxicology: Produces local irritation and narcosis. See ketones.
TLV: ACGIH (recommended): 200 parts per million in air; 590 milligrams per cubic meter of air.
Fire Hazard: Dangerous, when exposed to heat or flame; it can react with oxidizing materials.
Underwriters Lab Classification: 85 90.
Spontaneous Heating: No.
Disaster Hazard: Highly dangerous upon exposure to heat or flame.
Explosion Hazard: Moderate, when exposed to flame (Section 7).

CALCIUM CARBONATE

General Information

Synonyms: Calcite; aragonite.
Description: White powder.
Formula: $CaCO_3$.
Constants: Mol wt: 100.09, mp: decomposes at 825°C; 1339°C at 1025 atm., d: 2.7 2.95.

Hazard Analysis and Countermeasures

See calcium compounds. A nutrient and/or dietary supplement food additive. Also a general purpose food additive (Section 10). Calcium carbonate is a common air contaminant (Section 4).

CALCIUM COMPOUNDS

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 1; Ingestion 1; Inhalation 1
- Acute Systemic: U
- Chronic Local: Irritant 1.
- Chronic Systemic: U.

Toxicology: The fumes evolved by burning calcium in air are composed of calcium oxide (quick lime). This material is irritating to the skin, eyes and mucous membranes. Many calcium compounds are used medicinally. Generally speaking, calcium compounds should be considered toxic only when they contain a toxic component (such as arsenic, etc.) or as calcium oxide or hydroxide. Calcium compounds are common air contaminants (Section 4).

CHLOROFORM

General Information

Synonym: Trichloromethane.
Description: Colorless liquid; heavy, ethereal odor.
Formula: $CHCl_3$.
Constants: Mol wt: 119.39, mp: −63.5°C, bp: 61.26°C, fp: −63.5°C, flash p: none, d: 1.49845 at 15°C, vap. press.: 100 mm at 10.4°C, vap. d.: 4.12.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 1.
- Acute Systemic: Inhalation 3.
- Chronic Local: U.
- Chronic Systemic: U.

TLV: ACGIH (accepted): 50 parts per million in air; 240 miligrams per cubic meter of air.
Toxicology: Chloroform causes irritation of the conjunctiva. Upon inhalation, it causes dilation of the pupils with reduced reaction to light, as well as reduced intraocular pressure (experimental). The material is well known as an anesthetic. In the initial stages there is a feeling of warmth of the face and body, then an irritation of the mucous membranes and skin followed by nervous aberration. Prolonged inhalation will bring on paralysis accompanied by cardiac and respiratory failure and finally death.

It has been widely used as an anesthetic. However, due to its toxic effects, this use is being abandoned. 68,000 to 82,000 ppm kill most animals in a few minutes. 14,000 ppm is dangerous to life after an exposure of from 30 to 60 minutes. 5,000 to 6,000 ppm can be tolerated by animals for one hour without serious disturbances. The maximum concentration tolerated for several hours or for prolonged exposure with slight symptoms is 2,000 to 2,500 ppm. The harmful effects are narcosis, and damage to the liver and heart. Prolonged administration as an anesthetic may lead to such serious effects as profound toxemia and damage to the liver, heart and kidneys. Experimentally prolonged but light anesthesia in dogs produces a typical hepatitis. Inhalation of the concentrated chloroform vapor results in irritation of the mucous surfaces exposed to it. The narcosis is ordinarily preceded by a stage of excitation which is followed by loss of reflexes, sensation, and consciousness.

Fire Hazard: Slight, when exposed to high heat; otherwise practically nonflammable (Section 6).
Disaster Hazard: Dangerous; see phosgene.

CHLORIDES

Hazard Analysis

Toxicity: Varies widely. Sodium chloride (table salt) has very low toxicity, while carbonyl chloride (phosgene) is lethal in small doses.
Disaster Hazard: Dangerous; when heated to decomposition or on contact with acids or acid fumes they evolve highly toxic chloride fumes. Some organic chlorides decompose to yield phosgene.

CHROMIC ACID

General Information

Synonyms: Chromic anhydride; chromium trioxide.
Description: Dark, purple-red crystals.
Formula: CrO_3.
Constants: Mol wt: 100.01, mp: 196°C, d: 2.70.

Hazard Analysis

Toxicity: See chromium compounds.
Toxicology: It is a common air contaminant (Section 4).
Caution: This material is usually caustic in its action on skin, mucous membranes or organic matter in general.
TLV: ACGIH (accepted); 0.1 milligrams per cubic meter of air.
Fire Hazard: Dangerous; a very powerful oxidizing agent. In contact with organic matter or reducing agents in general it causes violent reactions (Section 6).
Explosion Hazard: Upon intimate contact with powerful reducing agents it can cause violent explosions.

COPPER COMPOUNDS

Hazard Analysis

Toxic Hazard Rating:
Acute Local: Irritant 1; Allergen 1; Ingestion 1; Inhalation 1.
Acute Systemic: Ingestion 2; Inhalation 2.
Chronic Local: Allergen 1.
Chronic Systemic: Ingestion 1; Inhalation 1.

Toxicology: As the sublimed oxide, copper may be responsible for one form of metal fume fever. Inhalation of copper dust has caused, in animals, hemolysis of the red blood cells, deposition of hemofuscin in the liver and pancreas, and injury to the lung cells; injection of the dust has caused cirrhosis of the liver and pancreas, and a condition closely resembling hemochromatosis, or bronzed diabetes. However, considerable trial exposure to copper compounds has not resulted in such disease.

As regards local effect, copper chloride and sulfate have been reported as causing irritation of the skin and conjunctivae which may be on an allergic basis (Section 9). Cuprous oxide is irritating to the eyes and upper respiratory tract. Discoloration of the skin is often seen in persons handling copper, but this does not indicate any actual injury from copper.

"In man the ingestion of a large quantity of copper sulfate has caused vomiting, gastric pain, dizziness, exhaustion, anemia, cramps, convulsions, shock, coma and death. Symptoms attributed to damage to the nervous system and kidney have been recorded, jaundice has been observed and, in some cases, the liver has been enlarged. Deaths have been reported to have occurred following the ingestion of so little as 27 g of the salt, while other victims have recovered after having taken much larger amounts up to 120 g." "Copper: The Metal, Its Alloys and Compounds," ed. Allison Butts, p. 857, Reinhold, 1954.

Many copper containing compounds are used as fungicides.

COPPER NITRATE

General Information

Synonym: Cupric nitrate.
Description: Blue, deliquescent crystals.
Formula: $Cu(NO_3)_2 \cdot 3H_2O$.
Constants: Mol wt: 241.63, mp: 114.5°C, d: 2.047.

Hazard Analysis and Countermeasures

See copper compounds and nitrates.

CYANIDES

Hazard Analysis

Toxic Hazard Rating:
Acute Local: Irritant 1.
Acute Systemic: Ingestion 3; Inhalation 3.
Chronic Local: Irritant 2.
Chronic Systemic: Ingestion 1; Inhalation 1.

TLV: ACGIH (recommended); 5 milligrams per cubic meter of air. Absorbed via intact skin.

Toxicology: The volatile cyanides resemble hydrocyanic acid physiologically, inhibiting tissue oxidation and causing death through asphyxia. Cyanogen is probably as toxic as hydrocyanic acid; the nitriles are generally considered somewhat less toxic, probably because of their lower volatility. The non-volatile cyanide salts appear to be relatively nontoxic systemically, so long as they are not ingested and care is taken to prevent the formation of hydrocyanic acid. Workers, such as electroplaters and picklers, who are daily exposed to cyanide solutions may develop a "cyanide" rash, characterized by itching, and by macular, papular, and vesicular eruptions. Frequently there is secondary infection. Exposure to small amounts of cyanide compounds over long periods of time is reported to cause loss of appetite, headache, weakness, nausea, dizziness, and symptoms of irritation of the upper respiratory tract and eyes. See also specific compounds.

Fire Hazard: Moderate, by chemical reaction with heat, moisture, acid; emit hydrocyanic acid (Section 6).
Caution: Many cyanides evolve hydrocyanic acid rather easily. This is a flammable gas and is highly toxic. Carbon dioxide from the air is sufficiently acidic to liberate hydrocyanic acid from cyanide solutions. See also hydrocyanic acid.
Explosion Hazard: See hydrocyanic acid.
Disaster Hazard: Dangerous; on contact with acid, acid fumes, water or steam, they will produce toxic and flammable vapors.

CYCLOHEXANE

General Information

Synonyms: Hexahydrobenzene; hexamethylene.
Description: Colorless mobile liquid, pungent odor.
Formula: C_6H_{12}.
Constants: Mol wt: 84.16, mp: 6.5°C, bp: 80.7°C, fp: 4.6°C, flash p: −4°F, uic: 90-95, lel: 1.3%, uel: 8.4%, d: 0.7791 at 20°/4°C, autoign. temp.: 500°F, vap. press.: 100 mm at 60.8°C, vap. d.: 2.90.

Hazard Analysis

Toxic Hazard Rating:
Acute Local: Irritant 2.
Acute Systemic: Inhalation 2.
Chronic Local: U.
Chronic Systemic: Inhalation 1.

Toxicology: Can cause skin irritation.
TLV: ACGIH (recommended) 300 parts per million of air, 1050 milligrams per cubic meter of air.
Caution: May act as a simple asphyxiant. See also cycloparaffins.
Fire Hazard: Dangerous; when exposed to heat or flame, it can react with oxidizing materials.
Spontaneous Heating: No.
Explosion Hazard: Moderate, in the form of vapor when exposed to flame (Section 7).

DIMETHYL FORMAMIDE

General Information

Description: Colorless, mobile liquid.
Formula: $(CH_3)_2NCHO$.
Constants: Mol wt: 73.1, bp: 152.8°C, lel: 2.2% at 100°C, uel: 15.2% at 100°C, flash p: 136°F, fp: −61°C, d: 0.9445 at 25°/4°C, autoign. temp.: 833°F, vap. press. 3.7 mm at 25°C, vap. d.: 2.51.

Hazard Analysis

Toxic Hazard Rating:
Acute Local: Irritant 2; Inhalation 2.
Acute Systemic: Ingestion 1; Inhalation 2; Skin Absorption 2.
Chronic Local: Irritant 2.
Chronic Systemic: Ingestion 3; Inhalation 3; Skin Absorption 3.

Toxicology: Highly irritating. Prolonged inhalation of 100 ppm has produced liver damage in experimental animals.
TLV: ACGIH (recommended) 10 parts per million of air; 30 milligrams per cubic meter of air. May be absorbed via the skin.
Fire Hazard: Moderate, when exposed to heat or flame; can react with oxidizing materials.
Explosion Hazard: Moderate, when exposed to flame.
Caution: Avoid contact with halogenated hydrocarbons and inorganic nitrates.

DIMETHYL SULFOXIDE

General Information

Synonym: DMSO.
Description: Clear, water-white, hygroscopic liquid.
Formula: $(CH_3)_2SO$.
Constants: Mol wt: 78.13, mp: 6°C, bp: decomp. at 100°C, flash p: 203°F (O.C.), d: 1.100 at 20°C, vap. press.: 0.37 mm at 20°C, lel: 2.6%, uel: 28.5%.

Hazard Analysis
Toxic Hazard Rating:
Acute Local: Irritant 2; Allergen 2; Inhalation 1.
Acute Systemic: Ingestion 2; Skin Absorption 2.
Chronic Local: Irritant 1; Allergen 2.

Chronic Systemic: Ingestion 1; Skin Absorption 2.
Freely penetrates skin. Acts as a primary irritant on skin causing redness, burning, itching, and scaling, also causes urticaria: systemic symptoms are nausea, vomiting, chills, cramps, and lethargy. A case of anaphylactic reaction has been reported. Has caused corneal opacity in experimental animals.
Fire Hazard: Moderate, when exposed to heat or flame.
Disaster Hazard: Moderately dangerous; when heated to decomposition, it emits toxic fumes; can react with oxidizing materials.

ETHYL ALCOHOL

General Information
Synonyms: Ethanol, methyl carbinol, spirit of wine.
Description: Clear, colorless, fragrant liquid.
Formula: CH_3CH_2OH
Constants: Mol wt: 46.07, bp: 78.32°C, ulc: 70, lel: 4.3%, uel: 19%, fp: −114.1°C, flash p: 55°F, d: 0.7893 at 20°/4°C, autoign. temp.: 793°F, vap. press.: 40 mm at 19°C, vap. d.: 1.59.
Hazard Analysis
Toxic Hazard Rating
Acute Local: Irritant 1.
Acute Systemic: Ingestion 2; Inhalation 2; Skin Absorption 1.
Chronic Local: Irritant 1.
Chronic Systemic: Ingestion 1; Inhalation 1; Skin Absorption 1.
TLV: ACGIH (recommended): 1000 parts per million in air; 1880 milligrams per cubic meter of air.
Toxicology: The systemic effect of ethyl alcohol differs from that of methyl alcohol. Ethyl alcohol is rapidly oxidized in the body to carbon dioxide and water, and in contrast to methyl alcohol, no cumulative effect occurs. Though ethyl alcohol possesses narcotic properties, concentrations sufficient to produce this effect are not reached in industry. Exposure to concentrations of 5,000 to 10,000 ppm results in irritation of the eyes and mucous membranes of the upper respiratory tract. If continued for an hour, stupor and drowsiness may result. Concentrations below 1,000 ppm usually produce no signs of intoxication. There is no concrete evidence that repeated exposure to ethyl alcohol vapor results in cirrhosis of the liver. The main effect of ethyl alcohol is due to its irritant action on the mucous membranes of the eyes and upper respiratory tract.

Exposure to concentrations of over 1,000 ppm may cause headache, irritation of the eyes, nose and throat, and, if long continued, drowsiness and lassitude, loss of appetite and inability to concentrate.
Fire Hazard: Dangerous, when exposed to heat or flame; can react vigorously with oxidizing materials.
Disaster Hazard: Dangerous, when exposed to heat or flame.
Spontaneous Heating: No.
Explosion Hazard: Moderate, when exposed to flame.

ETHYLENE DICHLORIDE

General Information
Synonyms: Ethylene chloride, 1,2-dichloroethane
Description: Colorless liquid
Formula: CH_2ClCH_2Cl
Constants: Mol wt: 99.0, bp: 83.5°C, ulc: 60/70, lel: 6.2%, uel: 15.9%, fp: −35.7°C, flash p: 56°F, d: 1.257 at 20°/4°C, autoign. temp.: 775°F, vap. press.: 100 mm at 29.4°C, vap. d.: 3.35.
Hazard Analysis
Toxic Hazard Rating
Acute Local: Irritant 3, Ingestion 3, Inhalation 3.
Acute Systemic: Ingestion 3, Inhalation 3.
Chronic Local: Irritant 2.
Chronic Systemic: Ingestion 3, Inhalation 3, Skin Absorption 2.
TLV: ACGIH (recommended): 50 ppm of air; 200 milligrams per cubic meter of air.
Toxicology: Ethylene dichloride has a distinctive odor and strong local irritating effects, which give warning of its presence in relatively safe concentrations. There is irritation of the eyes and upper respiratory passages. Ethylene dichloride has a specific effect on the cornea. Exposure to the vapor, or, in animals, injection under the skin, produces a clouding which may progress to endothelial necrosis and infiltration of the cornea by lymphocytes and connective tissue cells. The narcotic action of the compound is strong, probably of the same order as chloroform. Its toxic effects upon the liver and kidneys are less than that of carbon tetrachloride, but animal experiments indicate that these organs may show congestion and fatty degeneration. Edema of the lungs has also been reported in animals. Dermatitis in man has been observed (Section 9).

In short exposures to high concentrations, the picture is one of irritation of the eyes, nose and throat, followed by dizziness, nausea, vomiting, increasing stupor, cyanosis, rapid pulse, and loss of consciousness.

Chronic poisoning, where exposure has occurred over a period of several months, may cause loss of appetite, nausea and vomiting, epigastric distress, tremors, nystagmus, leucocytosis, low blood sugar levels, and possibly dermatitis if there has been skin contact. A soil fumigant. Used as a food additive permitted in food for human consumption.
Fire Hazard: Dangerous, if exposed to heat or flame.
Spontaneous Heating: No.
Explosion Hazard: Moderate, in the form of vapor when exposed to flame (Section 7).
Disaster Hazard: Dangerous; when heated to decomposition, it emits highly toxic fumes of phosgene; can react vigorously with oxidizing materials.

ETHYL ETHER

General Information
Synonyms: Sulfuric ether; anesthesia ether; ether; ethyl oxide.
Description: A clear, volatile liquid.
Formula: $C_2H_5OC_2H_5$.
Constants: Mol wt: 74.12, mp: −116.2°C, bp: 34.6°C, ulc: 100, lel: 1.85%, uel: 48%, flash p: −49°F, d: 0.7135 at 20°/4°C, autoign. temp.: 356°F, vap. press.: 442 mm at 20°C, vap. d.: 2.56.
Hazard Analysis
Toxic Hazard Rating:
Acute Local: Ingestion 2; Inhalation 1.
Acute Systemic: Inhalation 2; Skin Absorption 2.
Chronic Local: U.
Chronic Systemic: U.
TLV: ACGIH (recommended); 400 parts per million in air; 1212 milligrams per cubic meter of air.
Toxicology: Ether is not corrosive or dangerously reactive. However, it must not be considered safe for individuals to inhale or ingest. It is not toxic in the sense of being a poison. It is, however, a depressant of the central nervous system and is capable of producing intoxication, drowsiness, stupor, and unconsciousness. Death due to respiratory failure may result from severe and continued exposure.
Fire Hazard: Dangerous, when exposed to heat or flame; can react vigorously with oxidizing materials. See ethers.
Explosion Hazard: Severe, when exposed to heat or flame.
Disaster Hazard: Highly dangerous, in the presence of heat or flame. See ethers.

FERRIC CHLORIDE

General Information
Description: Black-brown solid.
Formula: $FeCl_3$.
Constants: Mol wt: 162.2, mp: 282°C, bp: 319.0°C, d: 2.804 at 11°C, vap. press.: 1 mm at 194.0°C.
Hazard Analysis
Toxic Hazard Rating:
Acute Local: Irritant 1; Ingestion 1.
Acute Systemic: U.
Chronic Local: Irritant 1.
Chronic Systemic: U.
Note: Used as a trace mineral added to animal feeds. (Section 10).
Disaster Hazard: Dangerous; when heated to decomposition, it emits highly toxic fumes of hydrochloric acid; will react with water to produce toxic and corrosive fumes.

FERRICYANIDES

Hazard Analysis

Toxic Hazard Rating
- Acute Local: Irritant 1.
- Acute Systemic: Ingestion 1.
- Chronic Local: U.
- Chronic Systemic: Ingestion 1.

Toxicology: Ferricyanides as such are of low toxicity since the CN is bound. It has been stated but not conclusively proven that HCN can be liberated in the stomach as a result of contact with gastric acidity.

Disaster Hazard: Dangerous; when heated to decomposition or on contact with acid or acid fumes, they emit highly toxic fumes of cyanides.

FLUORIDES

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: Ingestion 3.
- Chronic Local: Irritant 1.
- Chronic Systemic: Ingestion 3; Inhalation 3.

TLV: ACGIH (recommended); 2.5 milligrams per cubic meter of air.

Toxicology: Inorganic fluorides are generally highly irritant and toxic. Acute effects resulting from exposure to fluorine compounds are due to hydrogen fluoride. Chronic fluorine poisoning, or "fluorosis," occurs among miners of cryolite, and consists of a sclerosis of the bones, caused by fixation of the calcium by the fluorine. There may also be some calcification of the ligaments. The teeth are mottled, and there is osteosclerosis and ostemalacia. The bony and ligamentous changes are demonstrable by x-ray.

Loss of weight, anorexia, anemia, wasting and cachexia, and dental defects are among the common findings in chronic fluorine poisoning. There may be an eosinophilia, and impairment of growth in young workers.

Organic fluorides are generally less toxic than other halogenated hydrocarbons.

Common air contaminants (Section 4).

Disaster Hazard: Dangerous; when heated to decomposition or on contact with acid or acid fumes, they emit highly toxic fumes.

FORMIC ACID

General Information

Synonyms: Methanoic acid; hydrogen carboxylic acid.

Description: Colorless, fuming liquid; pungent penetrating odor.

Formula: HCOOH.

Constants: Mol wt: 46.03, bp: 100.8°C fp: 8.2°C, flash p: 156°F (O.C.), d: 1.2267 at 15°/4°C; 1.220 at 20°/4°C, autoign. temp.: 1114°F, vap. press.: 40 mm at 24.0°C, vap. d.: 1.59, flash p (90% solution): 122°F, autoign. temp. (90% solution): 813°F, lel (90% solution): 18%, uel (90% solution): 57%.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: Ingestion 3.
- Chronic Local: Irritant 2.
- Chronic Systemic: Ingestion 1.

TLV: ACGIH (recommended) 5 parts per million of air; 9 milligrams per cubic meter of air.

Toxicity. Note: A substance migrating to food from packaging materials (Section 10).

Fire Hazard: Moderate, when exposed to heat or flame.

n-HEXANE

General Information

Synonym: Hexyl hydride.

Description: Colorless liquid.

Formula: $CH_3(CH_2)_4CH_3$.

Constants: Mol wt: 86.17, bp: 68.7°C, ulc: 90-95, lel: 1.2%, uel: 7.5%, fp: −95.6°C, flash p: −7°F, d: 0.6603 at 20°/4°C, autoign. temp.: 500°F, vap. press.: 100 mm at 15.8°C, vap. d.: 2.97.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 1.
- Acute Systemic: Ingestion 1; Inhalation 1.
- Chronic Local: Irritant 1.
- Chronic Systemic: U.

Note: Use as a food additive permitted in food for human consumption (Section 10).

TLV: ACGIH (recommended); 500 parts per million in air; 1760 milligrams per cubic meter of air.

Fire Hazard: Dangerous, when exposed to heat or flame.

Spontaneous Heating: No.

Explosion Hazard: Moderate, when exposed to heat or flame.

Disaster Hazard: Dangerous; when heated or exposed to flame; can react vigorously with oxidizing materials.

HYDROBROMIC ACID

General Information

Synonym: Hydrogen bromide.

Description: Colorless gas or pale yellow liquid.

Formula: HBr.

Constants: Mol wt: 80.92, mp: −87°C, bp: −66.5°C, d: 3.50 g/liter at 0°C.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: Ingestion 2; Inhalation 2.
- Chronic Local: Irritant 2.
- Chronic Systemic: Ingestion 2; Inhalation 2.

TLV: ACGIH (recommended); 3 parts per million in air; 10 milligrams per cubic meter of air.

Disaster Hazard: Dangerous; see bromides; will react with water or steam to produce toxic and corrosive fumes.

HYDROCHLORIC ACID

General Information

Synonyms: Muriatic acid; chlorohydric acid; hydrogen chloride.

Description: Colorless gas or colorless, fuming liquid; strongly corrosive.

Formula: HCl.

Constants: Mol wt: 36.47, mp: −114.3°C, bp: −84.8°C, d: 1.639 g/liter (gas) at 0°C; 1.194 at −36°C (liquid), vap. press.: 4.0 atm at 17.8°C.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: U.
- Chronic Local: Irritant 2.
- Chronic Systemic: U.

TLV: ACGIH (recommended); 5 parts per million in air; 7 milligrams per cubic meter of air.

Toxicology: Hydrochloric acid is an irritant to the mucous membranes of the eyes and respiratory tract, and a concentration of 35 ppm causes irritation of the throat after short exposure. Concentrations of 50 to 100 ppm are tolerable for 1 hour. More severe exposures result in pulmonary edema, and often laryngeal spasm. Concentrations of 1,000 to 2,000 ppm are dangerous, even for brief exposures. Mists of hydrochloric acid are considered less harmful than the anhydrous hydrogen chloride, since the droplets have no dehydrating action. In general, hydrochloric acid causes little trouble in industry, other than from accidental splashes and burns. It is used as a general purpose food additive (Section 10). It is a common air contaminant (Section 10).

Disaster Hazard: Dangerous; see chlorides; will react with water or steam to produce toxic and corrosive fumes.

HYDROFLUORIC ACID

General Information

Synonyms: Hydrogen fluoride; fluorhydric acid.

Description: Clear, colorless, fuming corrosive liquid or gas.

Formula: HF.

Constants: Mol wt: 20.01, mp: −92.3°C, bp: 19.4°C, d: 0.921 g/liter (gas), 0.987 (liquid), vap. press.: 400 mm at 2.5°C.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: Ingestion 3; Inhalation 3.
- Chronic Local: Irritant 2.
- Chronic Systemic: Ingestion 2; Inhalation 2.

TLV: ACGIH (recommended); 3 parts per million in air; 2 milligrams per cubic meter of air.

Toxicology: It is extremely irritating and corrosive to the skin and mucous membranes. Inhalation of the vapor may cause ulcers of the upper respiratory tract. Concentrations at 50 to 250 ppm are dangerous, even for brief exposures. Hydrofluoric acid produces severe skin burns which are slow in healing. The subcutaneous tissues may be affected, becoming blanched and bloodless. Gangrene of the affected areas may follow. See also fluorides. It is a common air contaminant. (Section 4).

Disaster Hazard: Dangerous, when heated, it emits highly corrosive fumes of fluorides; will react with water or steam to produce toxic and corrosive fumes.

HYDROGEN PEROXIDE

General Information

Synonym: Hydrogen dioxide, T-Stuff.

Description: Colorless, heavy liquid or at low temperatures a crystalline solid.

Formula: H_2O_2.

Constants: Mol wt: 34.016, bp: 107°C for 35 wt%, d: 1.71 at −20°C, 1.46 at 0°C, vap. press.: 1 mm at 15.3°C.

Hazard Analysis

Toxic Hazard Rating: For concentrated solutions:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: U.
- Chronic Local: U.
- Chronic Systemic: U.

TLV: ACGIH (recommended); 1 part per million of air; 1.4 milligrams per cubic meter of air (90 wt% solution).

Toxicology: Pure H_2O_2, its solutions, vapors and mists are irritating to body tissue. This irritation can vary from mild to severe depending upon the concentration of H_2O_2. For instance solutions of H_2O_2 of 35 wt% and over can easily cause blistering of the skin. Irritation caused by H_2O_2 which does not subside upon flushing of the affected part with water should be treated by a physician. The eyes are particularly sensitive to irritation by this material. It is used as a general purpose food additive; it is a substance which migrates to food from packaging materials (Section 10). It is a common air contaminant (Section 4).

Fire Hazard: Dangerous by chemical reaction with flammable materials. H_2O_2 is a powerful oxidizer, particularly in the concentrated state. It is important to keep containers of this material covered because (1) uncovered containers are much more prone to react with flammable vapors, gases, etc.; (2) because if uncovered, the water from an H_2O_2 solution can evaporate, concentrating the material and thus increasing the fire hazard of the remainder.

For instance, solutions of H_2O_2 of concentrations in excess of 65 wt% heat up spontaneously when decomposing to $H_2O + \frac{1}{2}O_2$. Thus 90 wt% solutions, when caused to decompose rapidly due to the introduction of a catalytic decomposition agent, can get quite hot and perhaps start fires.

Explosion Hazard: Severe, when highly concentrated or pure H_2O_2 is exposed to heat, mechanical impact, detonation of a blasting cap, or caused to decompose catalytically by metals and their salts, dusts and alkalies.

Although many mixtures of H_2O_2 and organic materials do not explode upon contact, the resultant combination is detonatable either upon catching fire or by impact.

The detonation velocity of aqueous solutions of H_2O_2 has been found to be about 6500 meters/second for solutions of between 96 wt% and 100 wt% H_2O_2.

Another source of H_2O_2 explosions is from sealing the material in strong containers. Under such conditions even gradual decomposition of H_2O_2 to $H_2O + \frac{1}{2}O_2$ can cause large pressures to build up in the containers which may then burst explosively. See also Schumb, Satterfield, and Wentworth "Hydrogen Peroxide," pp. 174, 453.

Disaster Hazard: Highly dangerous because when heated, or shocked or contaminated, the concentrated material can explode or start fires.

HYPOCHLORITES

General Information

Description: Salts of hypochlorous acid.

Hazard Analysis

Toxic Hazard Rating
- Acute Local: Irritant 2; Ingestion 2; Inhalation 2.
- Acute Systemic: U.
- Chronic Local: U.
- Chronic Systemic: U.

Fire Hazard: Moderate, by chemical reaction with reducing agents. These are powerful oxidizers particularly at higher temperatures when chlorine and then oxygen are evolved, or in the presence of moisture or carbon dioxide.

Disaster Hazard: Dangerous; when heated or on contact with acid or acid fumes, it emits highly toxic fumes of chlorine and chlorides; will react with water or steam to produce toxic and corrosive fumes; it can react vigorously with oxidizing materials.

IODINE

General Information

Description: Rhombic, violet-black crystals, metallic luster.

Formula: I_2.

Constants: Mol wt: 253.84, mp: 112.9°C, bp: 183°C, d: 4.93, vap. press.: 1 mm at 38.7°C.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: U.
- Chronic Local: U.
- Chronic Systemic: Ingestion 3; Inhalation 3.

TLV: ACGIH (recommended); 0.1 part per million in air; 1 milligram per cubic meter of air.

Toxicology: The effect of iodine vapor upon the body is similar to that of chlorine and bromine, but it is more irritating to the lungs. Serious exposures are seldom encountered in industry, due to the low volatility of the solid at ordinary room temperatures. Signs and symptoms are irritation and burning of the eyes, lachrymation, cough, irritation of the nose and throat.

Radiation Hazard: Section 5. For permissible levels, see Table 5, p. 150.

Artificial isotope ^{125}I, half life 60 d. Decays to stable ^{125}Te by electron capture. Emits gamma rays of 0.035 MeV and X-rays.

Artificial isotope ^{126}I, half life 13 d. Decays to stable ^{126}Te by emitting positrons (51%) of 0.46 1.13 MeV. Also decays to stable ^{126}Te by emitting beta particles of 0.38-1.25 MeV. Also emits gamma rays of 0.39–0.86 MeV.

Artificial isotope ^{129}I, half life 1.6×10^7y. Decays to stable ^{129}Xe by emitting beta particles of 0.15 MeV. Also emits gamma rays of 0.04 MeV.

Artificial isotope ^{131}I, half life 8.1 d. Decays to stable ^{131}Xe by emitting beta particles of 0.33 (9%), 0.61 (88%) MeV. Also emits gamma rays of 0.08 0.72 MeV.

Artificial isotope ^{132}I, half life 2.3 h. Decays to stable ^{132}Xe by emitting beta particles of 0.80-2.14 MeV. Also emits gamma rays of 0.24-2.0 MeV.

Artificial isotope ^{133}I, half life 21 h. Decays to radioactive ^{133}Xe by emitting beta particles of 1.22 MeV. Also emits gamma rays of 0.53 MeV.

Artificial isotope ^{134}I, half life 53 m. Decays to stable ^{134}Xe by emitting beta particles of 0.5-2.4 MeV. Also emits gamma rays of 0.12 1.8 MeV.

Artificial isotope ^{135}I, half life 6.7 h. Decays to radioactive ^{135}Xe by emitting beta particles of 0.47 (35%), 1.0 (40%), 1.4 (25%) MeV. Also emits gamma rays of 0.42-1.69 MeV.

Disaster Hazard: Dangerous; when heated, it emits highly toxic fumes of iodine and iodine compounds; can react vigorously with reducing materials.

ISOPROPYL ALCOHOL

General Information

Synonyms: Dimethyl carbinol; sec-propyl alcohol; isopropanol.

Description: Clear, colorless liquid.

Formula: $CH_3CHOHCH_3$.

Constants: Mol wt: 60.09, mp: −88.5 to −89.5°C, bp: 82.3°C, lel: 2.0%, uel: 12%, flash p: 53°F, d: 0.7854 at 20°/4°C, autoign. temp.: 750°F, vap. press.: 33.0 mm at 20°C, vap. d.: 2.07, ulc: .70.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 1; Ingestion 1; Inhalation 1.

Acute Systemic: Ingestion 2; Inhalation 2.

Chronic Local: U.

Chronic Systemic: Ingestion 1; Inhalation 1.

TLV: ACGIH (recommended); 400 parts per million in air; 980 milligrams per cubic meter of air.

Toxicology: Acts as a local irritant and in high concentrations as a narcotic. It can cause corneal burns and often eye damage. It has good warning properties because it causes a mild irritation of the eyes, nose and throat at concentration levels of 400 ppm. It may induce a mild narcosis, the effects of which are usually transient, and it is somewhat less toxic than the normal isomer, but twice as volatile. It is not considered an important toxic hazard. There is some evidence that personnel can acquire a slight tolerance to this material, and single or repeated applications of it on the skin of rats, rabbits, dogs or human beings induced no untoward effects. It acts very much like ethanol in regard to absorption, metabolism and elimination but with a stronger narcotic action. Chronic injuries due to it have been detected in animals. Humans have ingested up to 20 ml diluted with water and noticed only a sensation of heat and slight lowering of the blood pressure. There are, however, reports of serious illness from as little as 10 ml taken internally. A food additive permitted in food for human consumption (Section 10). A common air contaminant (Section 4).

Fire Hazard: Dangerous, when exposed to heat or flame.

Spontaneous Heating: No.

Explosion Hazard: Moderate, when exposed to heat or flame.

Disaster Hazard: Dangerous! Keep away from heat and open flame; can react vigorously with oxidizing materials.

METHYL ALCOHOL

General Information

Synonyms: Methanol.

Description: Clear colorless very mobile liquid.

Formula: CH_3OH.

Constants: Mol wt: 32.04, bp: 64.8°C, lel: 7.3%, uel: 36.5%, fp: −97.8°C, flash p: 52°F, d: 0.7913 at 20°/4°C, autoign. temp.: 867°F, vap. press.: 100 mm at 21.2°C, vap. d.: 1.11.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 1; Inhalation 1.

Acute Systemic: Ingestion 3; Inhalation 2; Skin Absorption 2.

Chronic Local: Irritant 1; Inhalation 1.

Chronic Systemic: Ingestion 2; Inhalation 2; Skin Absorption 2.

TLV: ACGIH (recommended); 200 parts per million in air; 262 milligrams per cubic meter of air.

Toxicology: Methyl alcohol possesses distinct narcotic properties. It is also a slight irritant to the mucous membranes. Its main toxic effect is exerted upon the nervous system, particularly the optic nerves and possibly the retinae. The effect upon the eyes has been attributed to optic neuritis, which subsides but is followed by atrophy of the optic nerve. Once absorbed, methyl alcohol is only very slowly eliminated. Coma resulting from massive exposures may last as long as 2 to 4 days. In the body the products formed by its oxidation are formaldehyde and formic acid, both of which are toxic. Because of the slowness with which it is eliminated, methyl alcohol should be regarded as a cumulative poison. Though single exposures to fumes may cause no harmful effect, daily exposure may result in the accumulation of sufficient methyl alcohol in the body to cause illness.

Severe exposures may cause dizziness, unconsciousness, sighing respiration, cardiac depression, and eventually death. Where the exposure is less severe, the first symptoms may be blurring of vision, photophobia and conjunctivitis, followed by the development of definite eye lesions. There may be headache, gastrointestinal disturbances, dizziness and a feeling of intoxication. The visual symptoms may clear temporarily, only to recur later and progress to actual blindness. Irritation of the mucous membranes of the throat and respiratory tract, peripheral neuritis, and occasionally, symptoms referable to other lesions of the nervous system have been reported. The skin may become dry and cracked due to the solvent action of methyl alcohol.

Methyl alcohol is a common air contaminant (Section 4). It is used as a food additive permitted in foods for human consumption. Section 10.

Fire Hazard: Dangerous, when exposed to heat or flame.

Spontaneous Heating: No.

Explosion Hazard: Moderate, when exposed to flame.

Disaster Hazard: Dangerous, upon exposure to heat or flame; can react vigorously with oxidizing materials.

METHYLENE CHLORIDE

General Information

Synonyms: Dichloromethane.

Description: Colorless, volatile liquid.

Formula: CH_2Cl_2.

Constants: Mol wt: 84.94, bp: 40.1°C, lel: 15.5% in O_2, uel: 66.4% in O_2, fp: −96.7°C, d: 1.326 at 20°/4°C, autoign. temp.: 1224°F, vap. press.: 380 mm at 22°C, vap. d.: 2.93.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 2; Ingestion 2; Inhalation 2.

Acute Systemic: Ingestion 2; Inhalation 3; Skin Absorption 2.

Chronic Local: U.

Chronic Systemic: Ingestion 1; Inhalation 1; Skin Absorption 1.

TLV: ACGIH (recommended); 500 parts per million in air; 1740 mg per cubic meter of air.

Toxicology: This material is very dangerous to the eyes. Except for its property of inducing narcosis, it has very few other toxic effects. Its narcotic powers are quite strong, and in view of its great volatility, care should be taken in its use. It will not form explosive mixtures with air at ordinary temperatures. However, it can be decomposed by contact with hot surfaces and open flame, and it can then yield toxic fumes, which are irritating and will thus give warning of their presence. It has been used as an anesthetic in Europe and is still used there for local anesthesia. Experiments have shown that 25,000 ppm concentrations for 2 hour exposures were not lethal. Concentrations of 7,200 ppm after 8 minutes caused paresthesia of the extremities; after 16 minutes, acceleration of the pulse to 100 and during the first 20 minutes, congestion in the head, a sense of heat and slight irritation of the eyes. At a level of 2,300 ppm, there was no feeling of dizziness during one-hour exposures, but nausea did occur after 30 minutes of exposure. The limit of perception by smell is set at 25-50 ppm concentrations. Can cause a dermatitis upon prolonged skin contact (Section 9). A gas mask for organic vapors and fumes should be worn to avoid excessive inhalation.

Note: Used as a food additive permitted in food for human consumption (Section 10).

Fire Hazard: None.

Explosion Hazard: None under ordinary conditions, but will form explosive mixtures in atmosphere having high oxygen content.

Disaster Hazard: Dangerous; when heated to decomposition, it emits highly toxic fumes of phosgene.

Countermeasures

Ventilation Control: Section 2.

Personnel Protection: Section 3.

Storage and Handling: Section 7.

Shipping Regulations: Section 11.

MCA warning label.

IATA: Other restricted articles, class A, 40 liters (passenger), 220 liters (cargo).

NICKEL COMPOUNDS

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 1; Allergen 1; Ingestion 1; Inhalation 1.
- Acute Systemic: Ingestion 1; Inhalation 1.
- Chronic Local: Irritant 2; Allergen 1.
- Chronic Systemic: Inhalation 2.

TLV: ACGIH (recommended); 1 milligram per cubic meter of air.

Toxicology: Nickel and most salts of nickel are not generally considered to cause systemic poisoning. Ingestion of large doses of nickel, as a nickel compound, (1 to 3 mg per kg of weight) has been shown to cause intestinal disorders, convulsions and asphyxia in dogs. Nickel has been found in the hair of persons exposed to nickel oxide dust, but no systemic effects which could be attributed to nickel alone have been reported. In 1938, the British described 10 cases of lung cancer and numerous cases of cancer of the nose and nasopharynx occuring in workers in a nickel refinery. The exact cause of the malignancies was never completely explained but arsenic was involved. The most common effect resulting from exposure to nickel compounds is the development of "nickel itch." This form of dermatitis occurs chiefly in persons doing nickel-plating. There is marked variation in individual susceptibility to the dermatitis. It occurs more frequently under conditions of high temperature and humidity when the skin is moist, and chiefly affects the hands and arms (Section 9). Nickel carbonyl is highly irritating to the lungs and also can produce asphyxia by decomposing with the formation of carbon monoxide. These compounds are common air contaminants (Section 4).

NICKEL SULFATE

General Information

Description: Cubic, yellow crystals.

Formula: $NiSO_4$.

Constants: Mol wt: 154.76, mp: $-SO_3$ at 840°C, d: 3.68.

Hazard Analysis and Countermeasures

Used as a food additive permitted in the feed and drinking water of animals and/or for the treatment of food producing animals; also permitted in food for human consumption (Section 10). See nickel compounds and *sulfates*.

NITRIC ACID

General Information

Synonyms: Aqua fortis; hydrogen nitrate; azotic acid.

Description: Transparent colorless or yellowish, fuming, suffocating, caustic and corrosive liquid.

Formula: HNO_3.

Constants: Mol wt: 63.02, mp: −42°C, bp: 86°C, d: 1.502.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3
- Acute Systemic: Inhalation 3.
- Chronic Local: Irritant 2.
- Chronic Systemic: U.

TLV: ACGIH (recommended); 2 parts per million of air, 5 milligrams per cubic meter of air.

Toxicology: The exact composition of the "fumes" or vapor produced by nitric acid depends upon such factors as temperatues, humidity, and whether or not the acid comes in contact with other materials such as heavy metals or organic compounds. Depending upon these factors, the vapor will consist of a mixture of the various oxides of nitrogen and of nitric acid vapor. Nitric acid vapor is highly irritant to the mucous membranes of the eyes and respiratory tract and to the skin. It is corrosive to the teeth. Because of its irritant properties, chronic exposure to dangerous concentrations of the acid vapor seldom occur.

Fire Hazard: Moderate, by chemical reaction with reducing agents. It is a powerful oxidizing agent.

Explosion Hazard: Slight, by chemical reaction to evolve oxides of nitrogen, can explode on contact with powerful reducing agents.

Disaster Hazard: Dangerous, when heated to decomposition, it emits highly toxic fumes of oxides of nitrogen and hydrogen nitrate, will react with water or steam to produce heat and toxic and corrosive fumes.

NITRIC ACID, FUMING

General Information

Synonym: Nitric acid, anhydrous.

Description: Colorless to yellow to red corrosive liquid.

Formula: $NHO_3 + N_2O_4$.

Constant: D: > 1.480.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: Inhalation 3.
- Chronic Local: Irritant 2.
- Chronic Systemic: Inhalation 3.

Fire Hazard: Dangerous; very powerful oxidizing agent (Section 6).

Explosion Hazard: Moderate; can react explosively with many reducing agents.

Disaster Hazard: Dangerous; when heated to decomposition, it emits highly toxic fumes of oxides of nitrogen; will react with water or steam to produce heat and toxic, corrosive and flammable vapors.

OLEUM

General Information

Synonym: Fuming sulfuric acid.

Description: Heavy, fuming yellow liquid.

Formula: H_2SO_4 and up to 80% SO_3.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: U.
- Chronic Local: U.
- Chronic Systemic: U.

Fire Hazard: Dangerous, by chemical reaction with reducing agents and carbohydrates (Section 6).

Explosion Hazard: Severe, by chemical reaction with moisture and some organics.

Disaster Hazard: Dangerous, when heated to decomposition, it emits highly toxic fumes of oxides of sulfur, will react with water or steam to produce heat and toxic and corrosive fumes; can react vigorously with reducing materials.

OXALIC ACID

General Information

Synonym: Ethanedioic acid.

Description: Transparent, colorless crystals.

Formula: $COOHCOOH \cdot 2H_2O$.

Constants: Mol wt: 126.1, mp: 101°C, 189°C (anh.), bp: sublimes at 150°C, d: 1.653.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: Ingestion 3; Inhalation 3.
- Chronic Local: Irritant 3; Ingestion 3; Inhalation 3.
- Chronic Systemic: Ingestion 2; Inhalation 2.

TLV: ACGIH (recommended); 1 milligram per cubic meter of air.

Toxicology: Acute oxalic poisoning results from ingestion of a solution of the acid. There is marked corrosion of the mouth, esophagus and stomach, with symptoms of vomiting, burning abdominal pain, collapse and sometimes convulsions. Death may follow quickly. The systemic effects are attributed to the removal by the oxalic acid of the calcium in the blood. The renal tubules become obstructed by the insoluble calcium oxalate, and there is profound kidney disturbance. The inhalation of the dust or vapor may cause symptoms of irritation of the upper respiratory tract, gastro-intestinal disturbances, albuminuria, gradual loss of weight, increasing weakness and nervous system complaints. Oxalic acid has a caustic action on the skin and may cause dermatitis (Section 9); a case of early gangrene of the fingers resembling that caused by phenol has been described.

The chief effects of inhalation of the dusts or vapor are irritation of the eyes and upper respiratory tract, ulceration of the mucous membrane of the nose and throat, epistaxis, headache, irritability and nervousness. More severe cases may show albuminura, chronic cough, vomiting, pain in the back and gradual emaciation and weakness. The skin lesions are characterized by cracking and fissuring of the skin and the development of slow-healing ulcers. The skin may be bluish in color, and the nails brittle and yellow.

PHOSPHORIC ACID

General Information

Description: Colorless liquid or rhombic crystals.
Formula: H_3PO_4.
Constants: Mol wt: 98.04, mp: 42.35°C, $-\frac{1}{2}H_2O$ at 213°C, fp: 42.4°C, d: 1.864 at 25°C, vap. press.: 0.0285 mm at 20°C.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 2; Ingestion 2; Inhalation 2.
- Acute Systemic: U.
- Chronic Local: Irritant 2; Inhalation 2.
- Chronic Systemic: U.

Note: Used as a general purpose food additive (Section 10). It is a common air contaminant (Section 4).
TLV: ACGIH (recommended): 1 milligram per cubic meter of air.
Disaster Hazard: Dangerous; when heated to decomposition, it emits toxic fumes of oxides of phosphorus.

POTASSIUM CHLORIDE

General Information

Synonyms: Potassium muriate; potash muriate.
Description: Colorless or white crystals or powder; soluble in water; slightly soluble in alcohol; insoluble in absolute alcohol.
Formula: KCl.
Constants: Mol wt: 74.5; d: 1.987; mp: 790°C; sublimes at 1500°C.

Hazard Analysis and Countermeasures

Toxic Hazard Rating: U. A nutrient and or dietary supplement food additive (Section 10). See chlorides.

POTASSIUM CYANIDE

General Information

Description: White, deliquescent crystalline solid; faint odor of bitter almonds.
Formula: KCN.
Constants: Mol wt: 65.11; mp: 634.5°C; d: 1.52 at 16°C.

Hazard Analysis and Countermeasures

See cyanides.

POTASSIUM FERRICYANIDE

General Information

Synonyms: Red prussiate of potash; red potassium prussiate.
Description: Bright red, lustrous crystals or powder.
Formula: $K_3Fe(CN)_6$.
Constants: Mol wt: 329.24; mp: decomposes; d: 1.894 at 17°C.

Hazard Analysis

Toxicity: See ferricyanides. This is not a powerful poison as are the simple cyanides.
Disaster Hazard: Dangerous; when heated to decomposition or on contact with acid or acid fumes, it emits highly toxic fumes of cyanides.

POTASSIUM HYDROXIDE

General Information

Synonym: Potassium hydrate.
Description: White, deliquescent pieces, lumps or sticks having crystalline fracture.
Formula: KOH.
Constants: Mol wt: 56.11; mp: 360°C ± 7°C; bp: 1320°C; d: 2.044; vap. press.: 1 mm at 719°C.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Ingestion 3; Inhalation 3.
- Acute Systemic: Ingestion 3.
- Chronic Local: Irritant 3.
- Chronic Systemic: U.

Toxicity: Highly caustic. Used as a general purpose food additive (Section 10). See potassium.
Fire Hazard: Moderate.
Disaster Hazard: Dangerous; will react with water or steam to produce caustic solution and heat.

POTASSIUM IODIDE

General Information

Description: Colorless or white granules.
Formula: KI.
Constants: Mol wt: 166.02; mp: 723°C; bp: 1420°C; d: 3.13; vap press.: 1 mm at 745°C.

Hazard Analysis and Countermeasures

See iodides. A trace mineral added to animal feeds; a nutrient and or dietary supplement food additive.

PYROCATECHOL

General Information

Synonyms: 1,2-Benzendiol; catechol; pyrocatechin; o-dihydroxybenzene.
Description: Colorless crystals.
Formula: $C_6H_4(OH)_2$.
Constants: Mol wt: 110.11; mp: 105°C; bp: 240°C; flash p: 261°F (C.C.); d: 1.371 at 15°C; vap press.: 10 mm at 118.3°C; vap d: 3.79.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 3; Allergen 1.
- Acute Systemic: Ingestion 3; Inhalation 3; Skin Absorption 3.
- Chronic Local: Allergen 2.
- Chronic Systemic: Ingestion 3; Inhalation 3; Skin Absorption 3.

Toxicology: Can cause convulsions and injury to blood. See also phenol.
Fire Hazard: Slight; when exposed to heat or flame.
Spontaneous Heating: No.
Disaster Hazard: Dangerous; when heated, it emits highly toxic fumes; can react with oxidizing materials.

SODIUM ACETATE

General Information

Description: White crystals.
Formula: $NaC_2H_3O_2$.
Constants: Mol wt: 82.0; mp: 324°C; d: 1.528.

Hazard Analysis

Toxic Hazard Rating:
- Acute Local: Irritant 1; Ingestion 1.
- Acute Systemic: 0.
- Chronic Local: 0.
- Chronic Systemic: U.

Note: Used as a general purpose food additive (Section 10). It is a substance which migrates to food from packaging materials.

SODIUM BICARBONATE

General Information

Synonyms: Baking soda; sodium acid carbonate.
Description: White powder or crystalline lumps; soluble in water; insoluble in alcohol.
Formula: $NaHCO_3$.
Constants: Mol wt: 84; d: 2.159; mp: loses CO_2 at 270°C.

Hazard Analysis

Toxicity: Unknown. Used as a general purpose food additive; it is a substance which migrates to food from packaging materials (Section 10).

SODIUM COMPOUNDS

Hazard Analysis

Toxicity: Variable. Sodium ion is practically nontoxic. The toxicity of sodium compounds is frequently, though not always, due to the anion involved. The hydroxide is very corrosive, being strongly basic. Even here it is the concentration of hydroxyl ion which is responsible for the caustic action of this material.

SODIUM CHLORIDE

General Information

Synonyms: Salt, halite; sea salt

Description: Colorless, transparent crystals or white crystalline powder.

Formula: NaCl.

Constants: Mol wt: 58.45, mp: 801°C, bp: 1413 C, d: 2.165, vap. press.: 1 mm at 865°C.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 1; Ingestion 1.

Acute Systemic: 0.

Chronic Local: 0.

Chronic Systemic: 0.

Toxicology: When bulk sodium chloride is heated to high temperature, a vapor is emitted which is irritating to the eyes, particularly. Ingestion of large amounts of sodium chloride can cause irritation of the stomach. Improper use of salt tablets may produce this effect. A substance which migrates to food from packaging materials (Section 10).

SODIUM CITRATE

General Information

Synonym: Trisodium citrate.

Description: White crystals or granular powder; odorless; soluble in water; insoluble in alcohol.

Formula: $C_6H_5O_7Na_3 \cdot 2H_2O$.

Constants: Mol wt: 258, mp: loses water at 150°C, bp: decomposes at red heat.

Hazard Analysis

Toxic Hazard Rating: U.

Toxicity: Used as a sequestrant and general purpose food additive (Section 10).

SODIUM HYDROXIDE

General Information

Synonyms: Caustic soda, sodium hydrate, lye; white caustic.

Description: White, deliquescent pieces, lumps or sticks.

Formula: NaOH.

Constants: Mol wt: 40.01, mp: 318.4°C, bp: 1390°C, d: 2.120 at 20°/4°C, vap. press.: 1 mm at 739°C.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 3; Ingestion 3, Inhalation 2.

Acute Systemic: U.

Chronic Local: Irritant 2.

Chronic Systemic: U.

TLV: ACGIH (recommended): 2 milligrams per cubic meter of air.

Toxicology: This material, both solid and in solution, has a markedly corrosive action upon all body tissue. The symptoms of irritation from this material are frequently evident immediately. Its corrosive action on tissue causes burns and frequently deep ulceration, with ultimate scarring. Prolonged contact with dilute solutions has a destructive effect upon tissue. Mists, vapors, and dusts of this compound cause small burns, and contact with the eyes, either in the solid or solution form, rapidly causes severe damage to the delicate tissue. Ingestion either in the solid or solution form causes very serious damage to the mucous membranes or other tissues with which contact is made. It can cause perforation and scarring. Inhalation of the dust or concentrated mist can cause damage to the upper respiratory tract and to lung tissue, depending upon the severity of the exposure. Thus, effects of inhalation may vary from mild irritation of the mucous membranes to a severe pneumonitis. It can cause an irritant dermatitis (Section 9). It is a general purpose food additive, it migrates to food from packaging materials (Section 10).

Disaster Hazard: Dangerous; will react with water or steam to produce heat and will attack living tissue.

SODIUM HYPOCHLORITE

General Information

Formula: NaClO.

Constants: Mol wt: 74.45, mp: decomposes, bp: decomposes.

Hazard Analysis and Countermeasures

See hypochlorites.

SODIUM HYPOPHOSPHITE

General Information

Description: Colorless, pearly, crystalline plates or white, granular powder; bitter sweet, saline taste.

Formula: $NaH_2PO_2 \cdot H_2O$.

Constant: Mol wt: 106.01.

Hazard Analysis

Toxicity: Moderate. See hypophosphites.

Fire Hazard: Moderate. See hypophosphites.

Explosion Hazard: Moderate, when exposed to heat. Sodium hypophosphite may detonate if heated. It must be kept cool, and stored in a cool, ventilated place, away from acute fire hazards. It may be disposed of by dissolving in water (Section 7).

Disaster Hazard: Dangerous; see phosphates.

SODIUM POTASSIUM TARTRATE

General Information

Synonyms: Rochelle salt; potassium sodium tartrate.

Description: Colorless, transparent, efflorescent crystals or white powder; soluble in water; insoluble in alcohol.

Formula: $KNaC_4H_4O_6 \cdot 4H_2O$.

Constants: Mol wt: 282, mp: 70–80°C, d: 1.77.

Hazard Analysis

Toxicity: Unknown. A sequestrant and general purpose food additive. (Section 10).

SODIUM SILICATE

General Information

Synonym: Water glass.

Description: Amorphous or colorless, deliquescent crystals.

Formula: $Na_2O \cdot xSiO_2$ ($x = 2.5$).

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 1; Ingestion 1.

Acute Systemic: U.

Chronic Local: Irritant 1.

Chronic Systemic: U.

A substance which migrates to food from packaging materials (Section 10).

SODIUM SULFIDE

General Information

Synonym: Sodium monosulfide.

Descriptions: Amorphous, yellow-pink or white deliquescent crystals.

Formula: Na_2S.

Constants: Mol wt: 78.06, mp: 1180°C, d: 1.856 at 14°C.

Hazard Analysis and Countermeasures

See sulfides.

STANNOUS CHLORIDE

General Information

Synonyms: Tin crystals, tin salt, tin dichloride; tin protochloride.

Description: Colorless crystals, soluble in less than its own weight of water, very souble in hydrochloric acid (dilute or concentrated), soluble in alcohol, ethyl acetate, glacial acetic acid, and sodium hydroxide solution.

Formula: $SnCl_2 \cdot 2H_2O$.

Constants: Mol wt: 225.65, d: 2.71 mp: 37–38°C.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 2; Ingestion 2; Inhalation 2.

Acute Systemic: U.

Chronic Local: U.

Chronic Systemic: U.

Toxicity: A chemical preservative food additive. (Section 10).

Disaster Hazard: See chlorides.

SULFIDES

Hazard Analysis

Toxicity: Variable. The alkaline sulfides (potassium, calcium, ammonium and sodium) are similar in action to alkalies. They cause softening and irritation of the skin. If taken by mouth they are corrosive and irritant through the liberation of hydrogen sulfide and free alkali. Hydrogen sulfide is especially toxic and should be specially referred to (see hydrogen sulfide).

Sulfides of the heavy metals are generally insoluble and hence have little toxic action except through the liberation of hydrogen sulfide.

Sulfides are used as fungicides.

Fire Hazard: Moderate, when exposed to flame or by spontaneous chemical reaction. Many sulfides ignite easily in air at room temperature. Others require a higher temperature or the presence of an oxidizer. Upon contact with moisture or acids, hydrogen sulfide is evolved. Many powerful oxidizers on contact with sulfides ignite violently. See also hydrogen sulfide (Section 6).

Explosion Hazard: Many sulfides react violently and explosively on contact with powerful oxidizers. Hydrogen sulfide evolved can form explosive mixtures with air. See also hydrogen sulfide.

Disaster Hazard: Dangerous; when heated to decomposition, they emit highly toxic fumes of oxides of sulfur; they react with water, steam or acids to produce toxic and flammable vapors of hydrogen sulfide.

SULFURIC ACID

General Information

Synonyms: Oil of vitriol; dipping acid.

Description: Colorless, oily liquid.

Formula: H_2SO_4.

Constants: Mol. wt.: 98.08, mp: 10.49°C, bp: 330°C, d: 1.834, vap. press.: 1 mm at 145.8°C.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 3; Ingestion 3; Inhalation 3.

Acute Systemic: U.

Chronic Local: Irritant 2; Inhalation 2.

Chronic Systemic: U.

TLV: ACGIH (recommended): 1 milligram per cubic meter of air.

Toxicology: Contact with the body results in rapid destruction of tissue, causing severe burns. No systemic effects due to continual ingestion of small amounts of this material have been noted. There are systemic effects secondary to tissue damage caused by contact with it. However, repeated contact with dilute solutions can cause a dermatitis, and repeated or prolonged inhalation of a mist of sulfuric acid can cause an inflammation of the upper respiratory tract leading to chronic bronchitis. Sensitivity to sulfuric acid or mists or vapors varies with individuals. Normally 0.125 to 0.50 ppm may be mildly annoying and 1.5 to 2.5 ppm can be definitely unpleasant. 10 to 20 ppm is unbearable.

Workers exposed to low concentrations of the vapor gradually lose their sensitivity to its irritant action. Inhalation of concentrated vapor or mists from hot acid or oleum can cause rapid loss of consciousness with serious damage to lung tissue. In concentrated form it acts as a powerful caustic to the skin destroying the epidermis and penetrating some distance into the skin and subcutaneous tissues, in which it causes necrosis. This causes great pain and if much of the skin is involved, it is accompanied by shock, collapse and symptoms similar to those seen in severe burns. The fumes or mists of this material cause coughing and irritation of the mucous membranes of the eyes and upper respiratory tract. Severe exposure may cause a chemical pneumonitis, erosion of the teeth due to exposure to strong acid fumes has been recognized in industry.

Used as a general purpose food additive, it migrates to food from packaging materials (Section 10). It is a common air contaminant (Section 4).

Fire Hazard: Moderate, by chemical reaction, a powerful oxidizer; can ignite upon contact with combustibles.

Disaster Hazard: Dangerous; when heated, it emits highly toxic fumes, will react with water or steam to produce heat, can react with oxidizing or reducing materials.

TETRACHLORODIFLUOROETHANE

General Information

Description: Liquid.

Formula: $C_2F_2Cl_4$.

Constants: Mol. wt.: 203.8, bp: 92.8°C, d: 1.6447 at 25°C, vap. d: 7.03.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: 0.

Acute Systemic: Inhalation 2.

Chronic Local: U.

Chronic Systemic: Inhalation 1.

TLV: ACGIH (recommended): 500 parts per million, 4170 milligrams per cubic meter of air.

Disaster Hazard: Dangerous; when heated, it emits highly toxic fumes of fluorides and chlorides.

TRICHLOROETHYLENE

General Information

Synonyms: Ethinyl trichloride; ethylene trichloride.

Description: Stable, colorless, heavy, mobile liquid, chloroform-like odor.

Formula: $CHClCCl_2$.

Constants: Mol. wt.: 131.40, mp: −73°C, bp: 87.1°C, fp: −86.8°C, d: 1.45560 at 25°/4°C, autoign. temp.: 770°F, vap. press.: 100 mm at 32°C, vap. d: 4.53, flash p: 90°F, lel: 2.5%, uel: 90%.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 1; Ingestion 1; Inhalation 1.

Acute Systemic: Ingestion 2; Inhalation 3; Skin Absorption 2.

Chronic Local: Irritant 1.

Chronic Systemic: Inhalation 1; Skin Absorption 1.

TLV: ACGIH (recommended): 100 parts per million of air, 535 milligrams per cubic meter of air.

Toxicology: Inhalation of high concentrations causes narcosis and anesthesia. A form of addiction has been observed in exposed workers. Prolonged inhalation of moderate concentrations causes headache and drowsiness. Fatalities following severe, acute exposure have been attributed to ventricular fibrillation resulting in cardiac failure. There is some question as to damage to liver or other organs from chronic exposure. Cases have been reported but are of questionable validity. Determination of the metabolities trichloracetic acid and trichloroethanol in urine reflects the absorption of trichloroethylene.

NOTE: A food additive permitted in food for human consumption (Section 10). A common air contaminant (Section 4).

Fire Hazard: Slight, when exposed to heat or flame. High concentrations of trichloroethylene vapor in high-temperature air can be made to burn mildly if plied with a strong flame. Though such a condition is difficult to produce, flames or arcs should not be used in closed equipment which contains any solvent residue or vapor.

Spontaneous Heating: No.

Disaster Hazard: Dangerous, See chlorides.

TOLUENE

General Information

Synonyms: Methylbenzene; phenylmethane; toluol.

Description: Colorless liquid; benzol-like odor.

Formula: $C_6H_5CH_3$.

Constants: Mol. wt.: 92.13, mp: −95°C to −94.5°C, bp: 110.4°C, flash p: 40°F (C.C.), ulc: 75-80, lel: 1.27%, uel: 7.0%, d: 0.866 at 20°/4°C, autoign. temp.: 947°F, vap. press.: 36.7 mm at 30°C, vap. d: 3.14.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Ingestion 2.

Acute Systemic: Ingestion 2; Inhalation 2; Skin Absorption 1.

Chronic Local: Irritant 1.

Chronic Systemic: Ingestion 2; Inhalation 2; Skin Absorption 2.

TLV: ACGIH (recommended): 100 parts per million in air; 750 milligrams per cubic meter of air.

Toxicology: Toluene is derived from coal tar, and commercial grades usually contain small amounts of benzene as an impurity. Acute poisoning, resulting from exposures to high concentrations of the vapors, are rare with toluene. Inhalation of 200 ppm of toluene for 8 hours may cause impairment of coordination and reaction time; with higher concentrations (up to 800 ppm) these effects are increased and are observed in a shorter time. In the few cases of acute toluene poisoning reported, the effect has been that of a narcotic, the workman passing through a stage of intoxication into one of coma. Recovery following removal from exposure has been the rule. An occasional report of chronic poisoning describes an anemia and leucopenia, with biopsy showing a bone marrow hypoplasia. These effects, however, are less common in people working with toluene, and they are not as severe.

Exposure to concentrations up to 200 ppm produces few symptoms. At 200 to 500 ppm, headache, nausea, loss of appetite, a bad taste, lassitude, impairment of coordination and reaction time are reported, but are not usually accompanied by any laboratory or physical findings of significance. With higher concentrations, the above complaints are increased and in addition, anemia, leucopenia and enlarged liver may be found in rare cases.

A common air contaminant (Section 4).

Fire Hazard: Dangerous, when exposed to heat or flame.

Spontaneous Heating: No.

Explosion Hazard: Moderate, when exposed to flame.

Disaster Hazard: Moderately dangerous; when heated, it emits toxic fumes; can react vigorously with oxidizing materials.

ZINC COMPOUNDS

Hazard Analysis

Toxicity: Variable, generally of low toxicity.

Toxicology: Zinc is not inherently a toxic element. However, when heated, it evolves a fume of zinc oxide which, when inhaled fresh, can cause a disease known as "brass founders' ague," or "brass chills." It is possible for poeple to become immune to it. However, this immunity can be broken by cessation of exposure of only a few days. Zinc oxide dust which is not freshly formed is virtually innocuous. There is no cumulative effect to the inhalation of zinc fumes. Fatalities, however, have resulted from lung damage caused by the inhalation of high concentrations of zinc chloride fumes. Soluble salts of zinc have a harsh metallic taste; small doses can cause nausea and vomiting, while larger doses cause violent vomiting and purging. So far as can be determined, the continued administration of zinc salts in small doses has no effect in man except those of disordered digestion and constipation. Exposure to zinc chloride fumes can cause damage to the mucous membrane of the nasopharnyx and respiratory tract and give rise to a pale gray cyanosis. Workers in zinc refining have been reported as suffering from a variety of non-specific intestinal, respiratory and nervous symptoms. Ulceration of the nasal septum and eczematous dermatosis are also reported.

It has been stated that zinc oxide dust can block the ducts of the sebaceous glands and give rise to a papular, pustular eczema in men engaged in packing this compound into barrels. Sensitivity to zinc oxide in man is extremely rare. Zinc chloride, because of its caustic action, can cause ulceration of the fingers, hands and forearms of those who use it as a flux in soldering. This condition has even been observed in men who handle railway ties which have been impregnated with this material. It is the opinion of some who work with it that it is carcinogenic.

A common air contaminant (Section 4).

ZINC OXIDE

General Information

Synonyms: Zincite, Chinese white, zinc white, flowers of zinc.

Description: White or yellowish powder.

Formula: ZnO.

Constants: Mol wt: 81.38, mp: > 1800°C, d: 5.47.

Hazard Analysis

Toxicity: A seed disinfectant. See zinc compounds. A fungicide. A trace mineral added to animal feeds. Also a dietary supplement food additive (Section 10).

TLV: ACGIH (recommended): (fume) 5 milligrams per cubic meter of air.

m-XYLENE

General Information

Synonym: m-Xylol.

Description: Colorless liquid.

Formula: $C_6H_4(CH_3)_2$.

Constants: Mol wt: 106.2, mp: −47.9°C, bp: 139°C, lel: 1.1%, uel: 7.0%, flash p: 84°F, d: 0.864 at 20°/4°C, vap. press.: 10 mm at 28.3°C, vap. d: 3.66, autoign. temp.: 982°F.

Hazard Analysis

Toxic Hazard Rating:

Acute Local: Irritant 1.
Acute Systemic: Inhalation 1.
Chronic Local: Irritant 1.
Chronic Systemic: Inhalation 1; Skin Absorption 1.

TLV: ACGIH (recommended): 100 parts per million in air, 435 milligrams per cubic meter of air.

Note: A common air contaminant (Section 4).

Fire Hazard: Dangerous, when exposed to heat or flame; can react with oxidizing materials.

Explosion Hazard: Moderate in the form of vapor when exposed to heat or flame.

Disaster Hazard: Dangerous. Keep away from open flame.

C. Electrical-Mechanical Equipment. A great deal of electrical and electronic equipment is used in failure analysis work. In general, the most common dangers found in the use of electrical equipment is in electrical shock and in fire. Some general guide lines to follow in the use of electrical equipment are listed below:

- o Observe proper grounding procedures for all equipment. For instance, when multiple power supplies are used it is possible to have floating potentials in a hookup that might prove dangerous.

- o Insure that all equipment is properly fused.

- o Observe all manufacturer's suggestions regarding safe equipment usage.

- o Keep flammable materials away from electrical equipment when there could be a danger of sparks or arcing.

Some guidelines regarding the use of purely mechanical equipment in failure analysis are listed below:

- o Never operate pneumatic equipment without proper retainers to prevent ejection of the tool.

- o Do not use compressed gas for cleaning or open drying unless the gas pressure is reduced to less than 30 psi, and then only with proper personal protection against flying debris (safety glasses, faceshields, etc.).

- o Observe safety precautions when using pressurized equipment, such as pressure bombs.

- o Protect fingers, hands, eyes, etc., when using any hand or bench top mechanical equipment (shears, files, saws, vice, etc.).

Suggestions regarding safety in the use of electromechanical equipment in failure analysis are listed below:

- Portable circular saws with blade diameter greater than 2 inches must have blade guards above and below base plate.

- Circular saws with blade diameter greater than 2 inches, hand-held power drills, grinders, belt sanders, and similar type hand-held power tools must have constant pressure switches that turn equipment off when pressure is released.

- Ensure that portable equipment meets grounding requirements; that is, the equipment be either double insulated and plainly marked as such or be provided with a three-prong electrical plug.

- Care should be used at all times to insure that articles of clothing be kept clear of moving parts in electromechanical equipment.

In general, safety with electrical and mechanical equipment is largely a matter of common sense. As with handling dangerous chemicals, there is a danger in the small laboratory of becoming careless, allowing accidents to occur that would normally be easily prevented.

D. Radiation Dose Monitoring. Establishing standards for acceptable exposure levels to ionizing radiation has been at best a guess. This is true because it is impossible to predict the results of even minimal exposure over the long term. OSHA Code of Federal Regulations (CFR) number 1910.96 covers the subject of ionizing radiation.

Ionizing radiation covers alpha, beta, gamma rays, x-rays, neutrons, high-speed electrons, high-speed protons, and any other atomic particles. A radioactive material is defined as any material which spontaneously emits any one or a combination of the particles listed above. Dose is defined as the quantity of ionizing radiation absorbed per unit mass by the body or any portion of the body during such period of time an exposure takes place.

Several units of dose measurement are in use currently. The unit used and the relationships among the units depends generally on the biological effect under consideration and on the conditions for irradiation.

Federal law provides that any employer is responsible for making such surveys as will be necessary for him to comply with OSHA Standards regarding ionizing radiation. "Survey" means an evaluation of radiation hazards present in the use, release, disposal, or presence of radioactive materials, or any other source of ionizing radiation under specific conditions that might exist.

It is the responsibility of the employer to provide personnel monitoring equipment and to require the use of this equipment by any employee who enters an area where he receives or is likely to receive a dose of greater than twenty-five percent of the OSHA applicable dose in any calendar quarter (three month period as determined in OSHA regulations). Personnel monitoring equipment means devices designed to be worn or carried by individuals. This monitoring equipment will be capable of monitoring the radiation dose received by an individual through, for instance, film badges, pocket chambers, pocket dosimeters, etc.

It is also the responsibility of the employer to provide speedy examination of personnel monitoring devices and to maintain current records of employee radiation exposure levels.

E. Checkout of Potential X-ray Sources. Failure analysis laboratories commonly make use of high-voltage analysis equipment such as scanning electron microscopes and x-ray radiographic equipment. All of this equipment can be a source of dangerous x-ray leakage, and should be monitored on a regular basis.

OSHA regulations specify acceptable doses, and individual states commonly have their own regulations regarding dose levels, rates, and schedules for monitoring. For example, New York State Code Rule 38 details regulations regarding x-ray radiation.

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EQUIPMENT

1.	Protective Gloves Fisher Scientific Co., Pittsburgh, PA Best Mfg. Corp., Menlo, GA	$ 5/pair
2.	Face Shield Dockson Corp., Detroit, Mich. General Scientific Equip. Co., Philadelphia, PA	$20/ea.
3.	Safety Glasses Bachmann Brothers, Philadelphia, PA Bausch & Lomb, Rochester, NY	$ 3/ea.
4.	Chemical Safety Apron B. F. Goodrich, Akron, OH Uniroyal Inc., New York, NY	$18/ea.
5.	Laboratory Coat Industrial Products Co., Langhorne, PA Safety Services & Supply Co., Houston, TX	$14/ea.
6.	Eye Wash Station, Hand or Foot Actuated Guardian Equipment, Chicago, IL Speakman Co., Wilmington, Del.	$195/ea.
7.	Emergency Shower Haws Drinking Faucet Co., Berkeley, CA Bradley Corp., Menomonee Falls, WI	$100/ea.
8.	Fire Extinguisher, Electrical and Chemical Fires, 10 lb. Charge Graviner Inc., Berkley Heights, NJ Fire-Chem Mfg. Co., Inc., Philadelphia, PA	$70/ea.
9.	Collapsible Stretcher Bullard Co., Sausalito, CA Lima Medical Supplies Inc., Lima, OH	$45/ea.
10.	Safety Bottle Carrier Bel-Art Products, Pequannock, NJ Morse Mfg. Co., E. Syracuse, NY	$22/ea.

EQUIPMENT (CONT)

11.	Respirator for Organic and Acid Gases Scott Aviation, Div. of A-T-O Inc., Lancaster, NY Willson Products Div., ESB Inc., Reading, PA	$ 20/ea.
12.	Laboratory First Aid Kit Acme Cotton Products, Valley Stream, NY Devco Engineering Inc., Fairfield, NJ	$ 70/ea.
13.	Spill Clean-up Kits - Acid, Caustic, and Flammable Solvent Fisher Scientific Co., Pittsburgh, PA J. T. Baker Co., Phillipsburg, NJ	$260/3 kits
14.	Dosimeter Badges Applied Health Physics, Inc., Bethel Park, PA Nuclear Equipment Chem. Corp., Chicago, IL	$ 5/ea.
15.	Radiation Survey Meter Applied Health Physics, Inc., Bethel Park, PA Nuclear Equipment Chem. Corp., Chicago, IL	$350

SECTION V

FAILURE ANALYSIS TECHNIQUE REFERENCES

V. FAILURE ANALYSIS TECHNIQUE REFERENCES

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SECTION VI

GLOSSARY OF TERMS AND MATERIALS

VI. GLOSSARY OF TERMS AND MATERIALS

1. Activation Energy - The energy level at which a specific microelectronic failure mechanism becomes active.
2. Amine - A derivative of ammonia in which hydrogen atoms have been replaced by radicals containing hydrogen and carbon atoms.
3. C-V Measurement - Capacitance versus voltage measurement commonly used to evaluate silicon dioxide (SiO_2) purity and some surface properties of silicon.
4. Cholesteric Liquid Crystal - A heat sensitive liquid crystal material that changes color with varying heat.
5. Dangling Bonds - Condition that exists at silicon - silicon dioxide interface where silicon bonds are not attached atomically to any other atom.
6. Functional Testing - Generally thought of as electrical testing that determines if a microelectronics device has the proper output for a given output.
7. Halogenated Compounds - Chemical compounds formed by any of the five very active, nonmetallic elements (fluorine, chlorine, bromine, astatine, or iodine).
8. Ionizing Radiation - Particulate radiation (X-ray, gamma, alpha, etc.) capable of causing ions to be created upon striking neutral atoms.
9. Lecithin - A mixture of the diglycerides of fatty acids linked to the choline ester of phosphoric acid. The approximate chemical formula is: $C_{43}H_{88}NO_9P$.
10. Light Interference - Phenomenon occuring when two or more light beams from the same source are recombined and consequently interfere with each other in an additive and subtractive manner to produce bands of light and dark.
11. Nematic Liquid Crystal - A current flow sensitive liquid crystal material that can be used to locate small pinholes in silicon dioxide.
12. Parametric Testing - Electrical tests that evaluate parameters such as voltage and current levels, current leakage levels, gains, etc.

13. Permeation Rate - Rate at which a gas or liquid is capable of moving through a given medium
14. Radiograph - Image produced on photographic film by X-rays, gamma rays, or neutrons.
15. Thermal Silicon Dioxide - Silicon dioxide (SiO_2) formed on a silicon wafer at high temperatures (>800^{o}C) by diffusing oxygen to the silicon surface.
16. Tracer Gas - A gas which is forced into a package under high pressure and is subsequently used to measure a leak rate. Helium is typically used.
17. Velocity of Sound Ratio - Reciprocal of the index of refraction ratio.