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NAVAL OCEAN SYSTEMS CENTER SAN DIEGO CA  
EHF SATCOM TECHNOLOGY WORKSHOP, 4-6 AUGUST 1981.(U)  
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NOSC/TD-457

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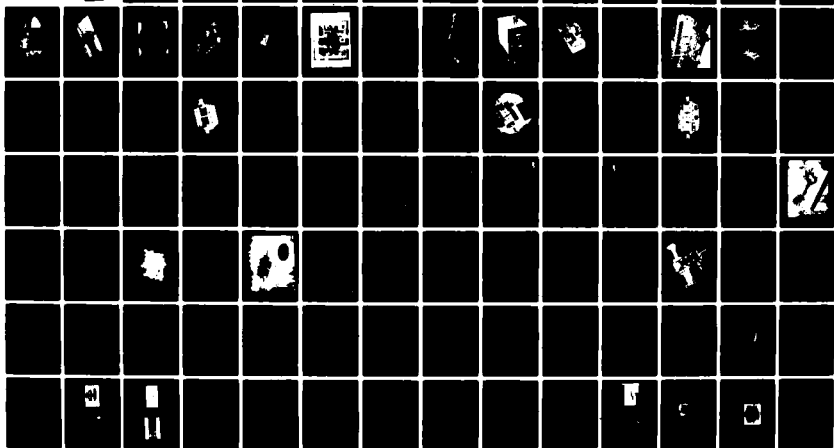
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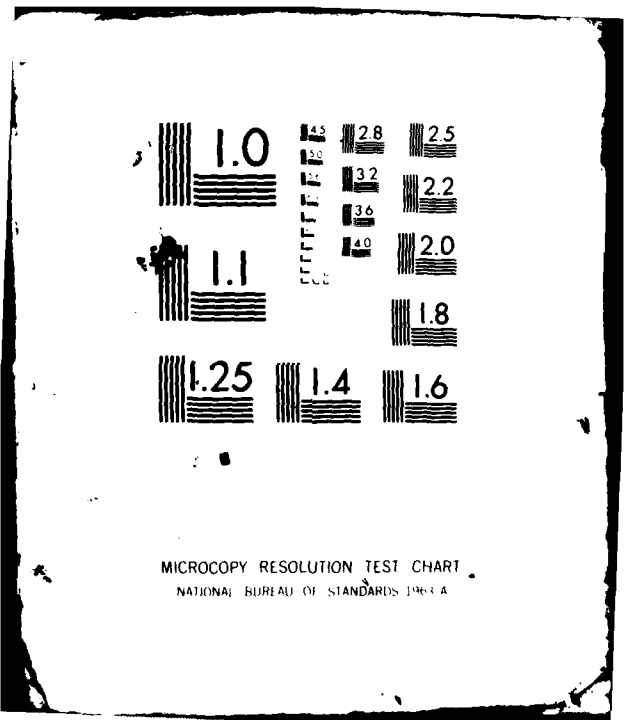
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MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS 1963-A

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# NOSC

NOSC TD 457

NOSC TD 457

Technical Document 457

**EHF SATCOM TECHNOLOGY WORKSHOP  
4-6 AUGUST 1981**

**KA Brodeur  
KR Casey**

September 1981

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**NAVAL OCEAN SYSTEMS CENTER  
SAN DIEGO, CALIFORNIA 92152**



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AN ACTIVITY OF THE NAVAL MATERIAL COMMAND

SL GUILLE, CAPT, USN

Commander

HL BLOOD

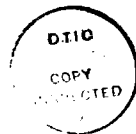
Technical Director

ADMINISTRATIVE INFORMATION

Work was performed under program element 62712N subproject XF12143555 (NOSC 814-CM03), by the EHF Communications Systems Program Branch (Code 8143).

Released by  
H. J. Wirth, Head  
SATCOM & HF Communications  
Systems Division

Under authority of  
H. D. Smith, Head  
Communications Systems  
and Technology Department



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K-BAND TECHNOLOGY DEVELOPMENT FOR EHF SATELLITE APPLICATION

M. I. T. - Lincoln Laboratory

C. Berglund

# K-Band Technology Development For EHF Satellite Application

C. D. BERGLUND, R. J. LENDER, M. L. STEVENS

MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
LINCOLN LABORATORY

# K-Band Technology Development For EHF Satellite Application

C. D. BERGLUND, R. J. LENDER, M. L. STEVENS

## INTRODUCTION

20 - 21 GHz RECEIVER FRONT END DESIGNS  
SPECIFICATIONS

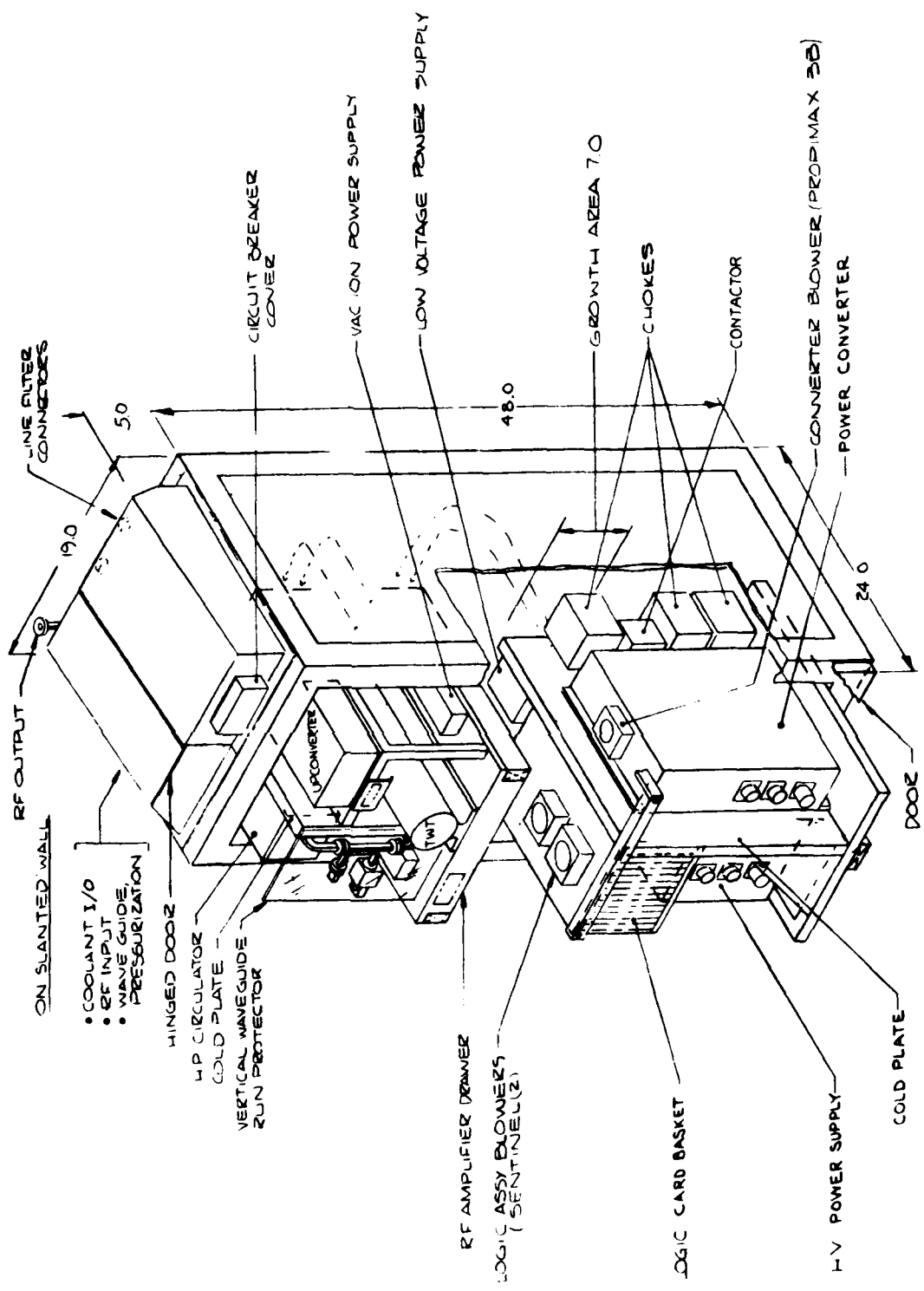
DEVICE CHARACTERIZATION  
AMPLIFIER PERFORMANCE

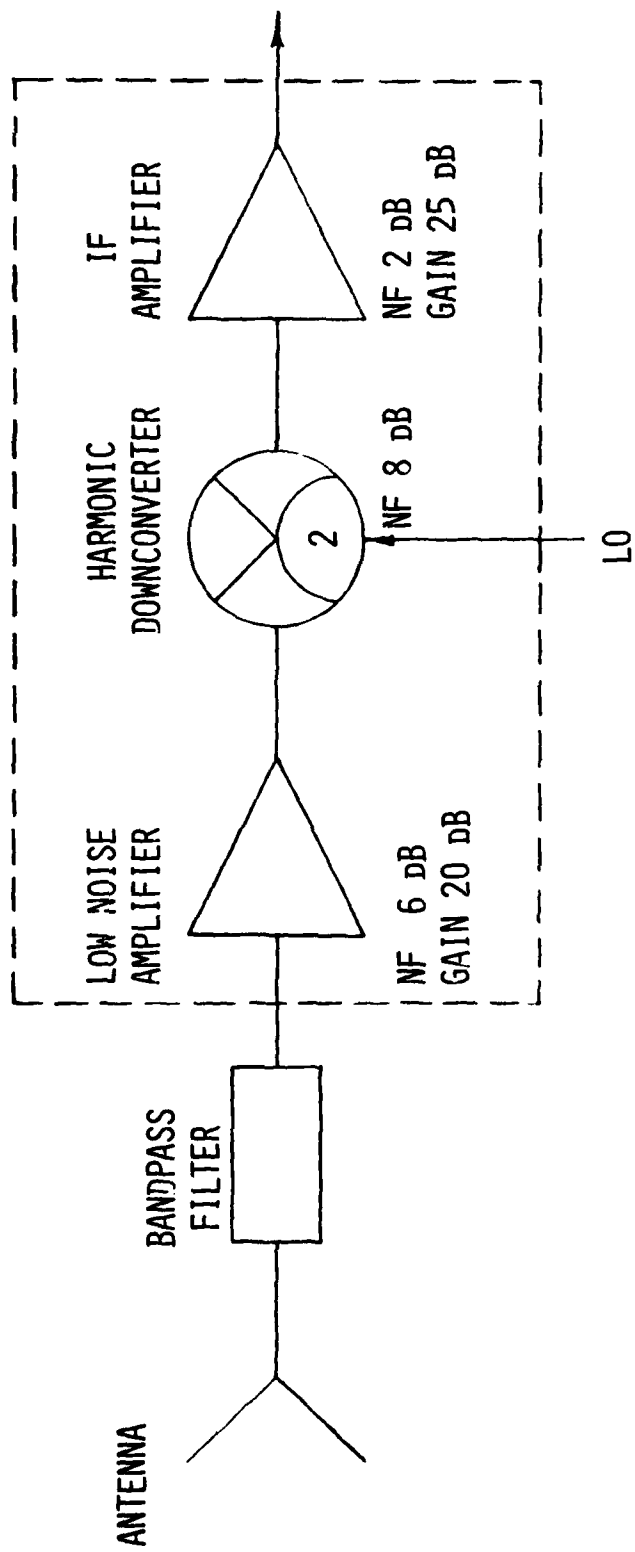
20 - 21 GHz GALLIUM ARSENIDE MESFET AMPLIFIER DEVELOPMENT  
DEVICE DEVELOPMENT  
DEVICE CHARACTERIZATION

LOAD PULL TECHNIQUE/TUNEABLE SLABLINE CIRCUIT  
LARGE SIGNAL "S-PARAMETER"/FIXED MICROSTRIP CIRCUITS  
DEVICE PERFORMANCE  
AMPLIFIER DESIGN AND PERFORMANCE

CONCLUSION

# Q-BAND HPA CABINET





- NOISE FIGURE  $\approx 6.5$  dB
- SMALL SIZE, VOLUME =  $6 \text{ IN}^3$
- LOW COST

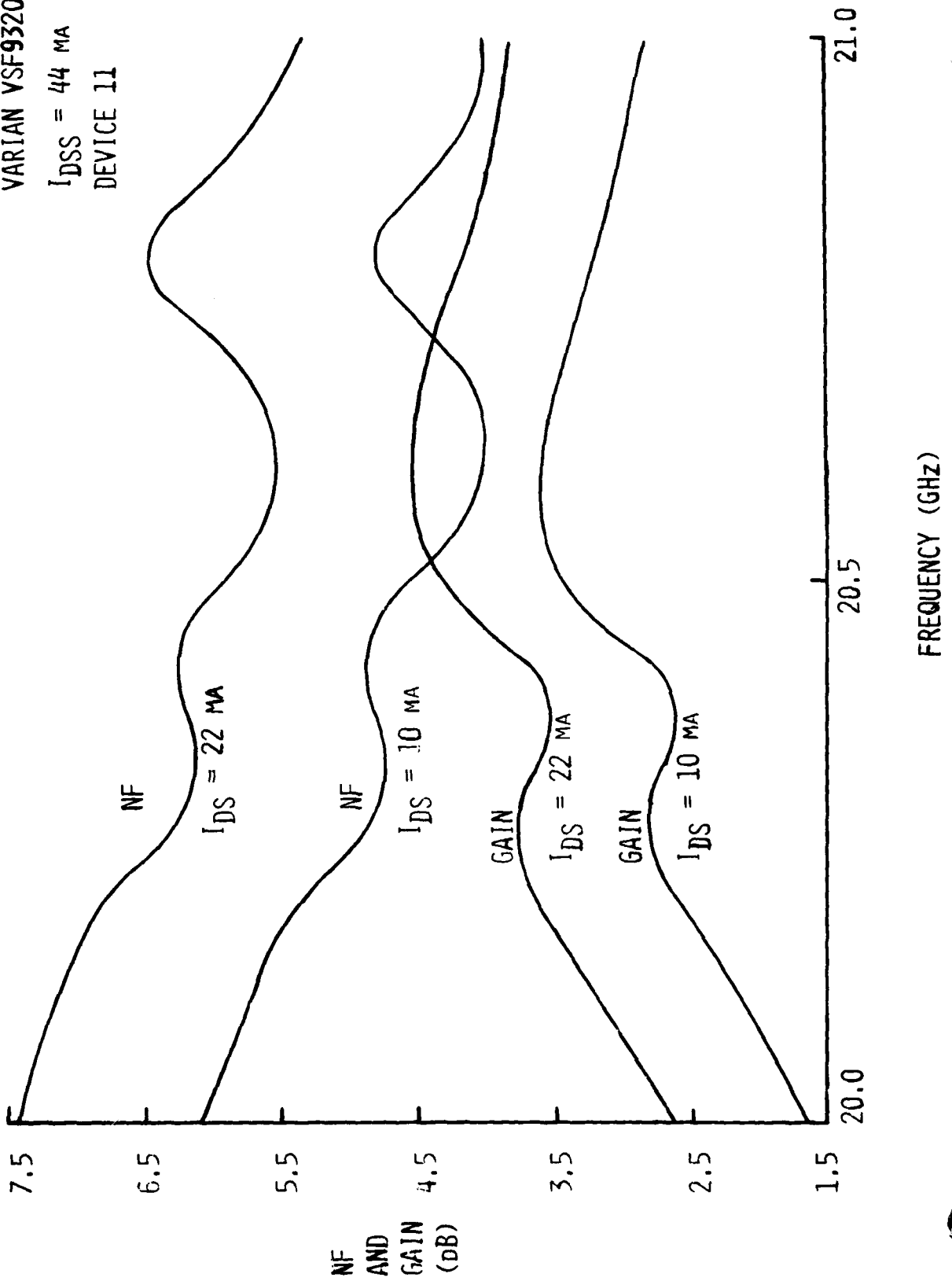
Block Diagram - 20 -21 GHz Receiver Front-End

# Performance of Low Noise Amplifier vs Bias

VARIAN VSF9320

$I_{DSS} = 44 \text{ MA}$

DEVICE 11

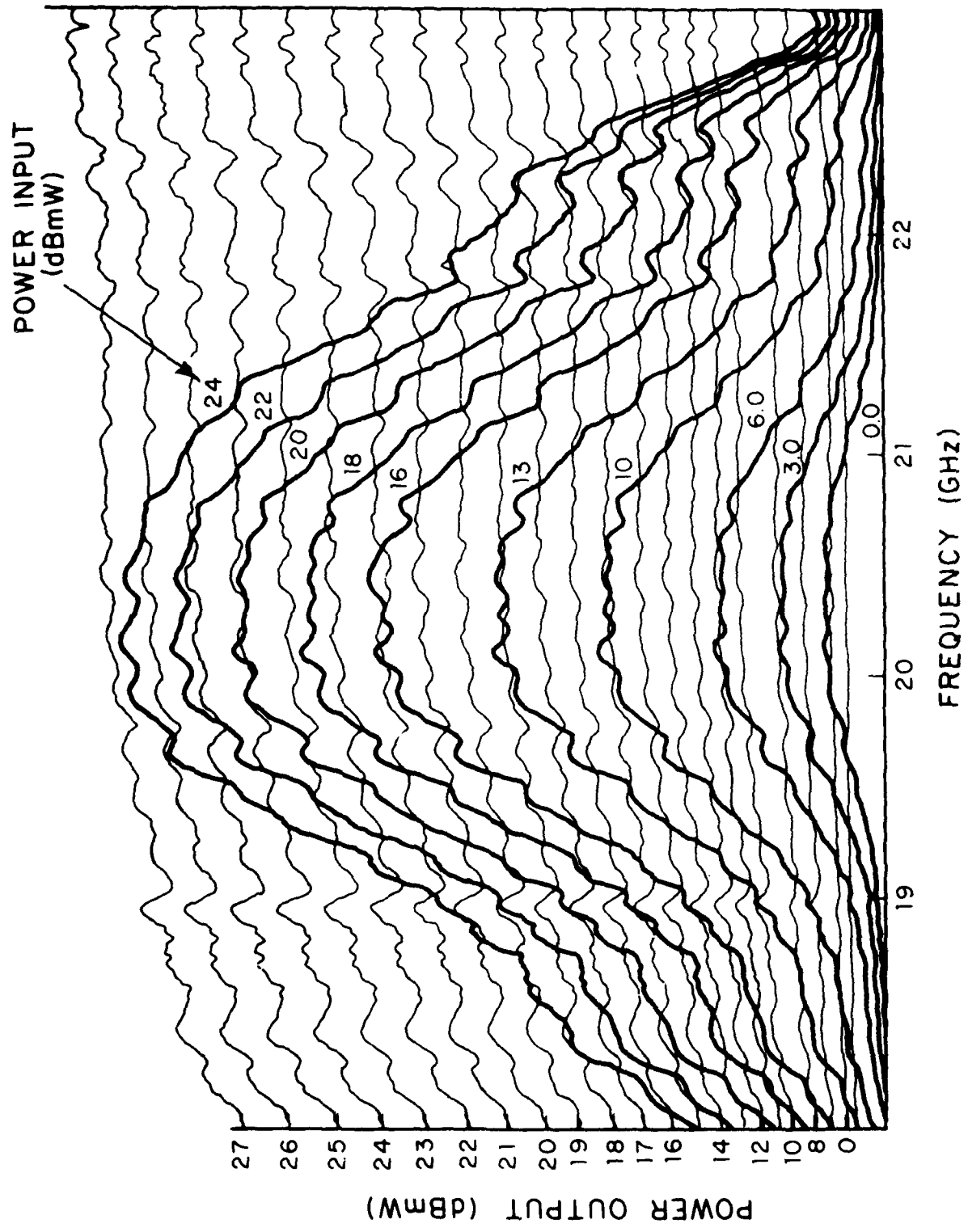


## K-Band FET Development Specification

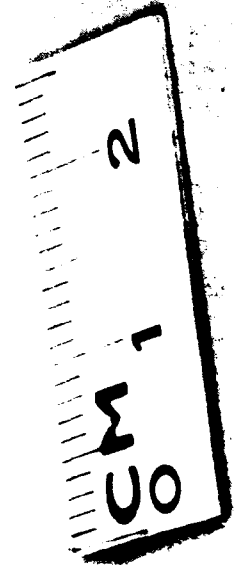
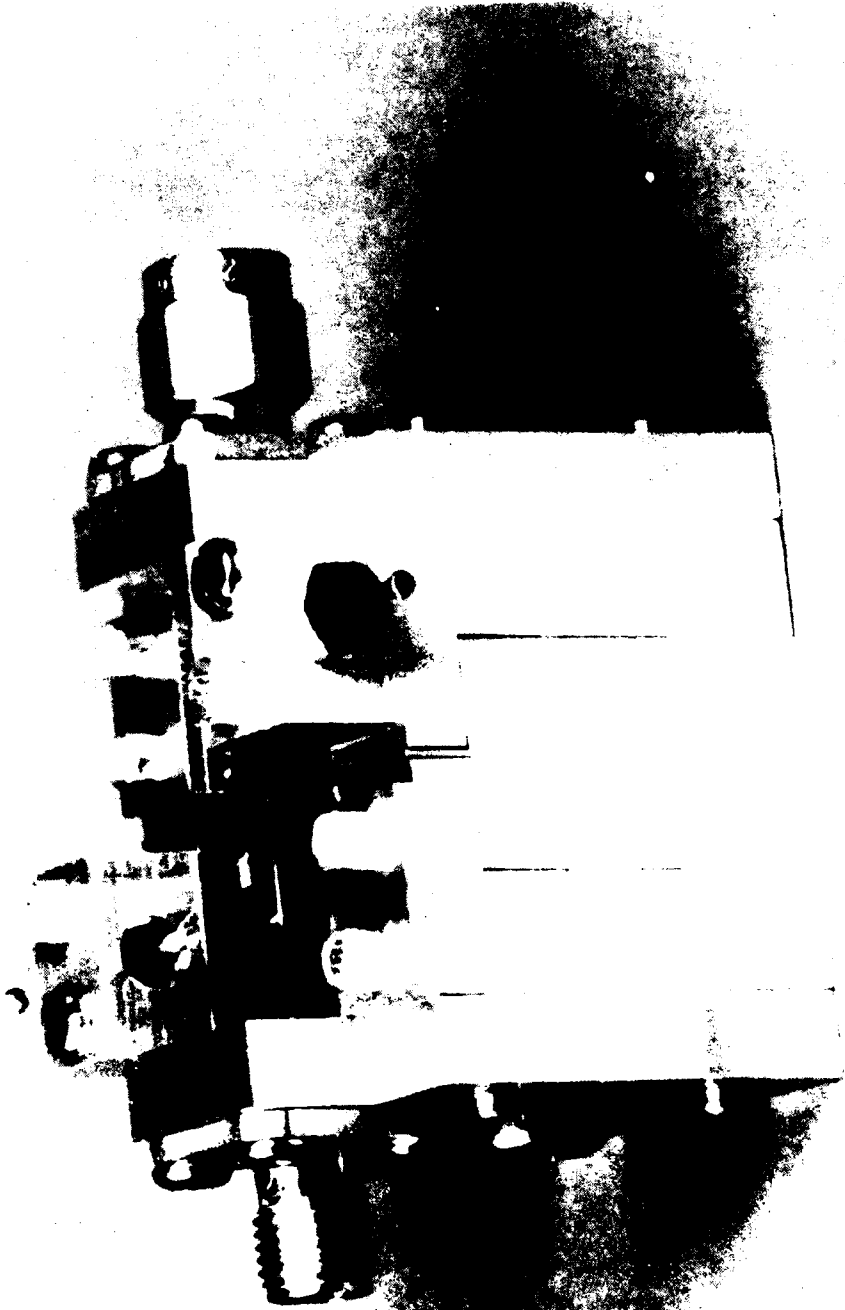
PERFORMANCE AT 21 GHz	I		II		III	
	GOAL	MINIMUM	GOAL	MINIMUM	GOAL	MINIMUM
POWER OUTPUT	1.0 W,	0.5 W.	--	1.0 W.	--	0.1 W.
POWER ADDED EFFICIENCY	20%	15%	20%	15%	20%	--
GAIN	5.0 dB	4.0 dB	5.0 dB	4.0 dB	10 dB	8 dB
CHANNEL TEMPERATURE RISE	< 100°C		< 100°C		< 100°C	
DELIVERABLES	50		60		100	
CONTRACTOR	MSC		MSC		MSC	

STATUS	COMPLETED	SCHEDULED COMPLETION
	AUGUST 1980	OCTOBER 1981

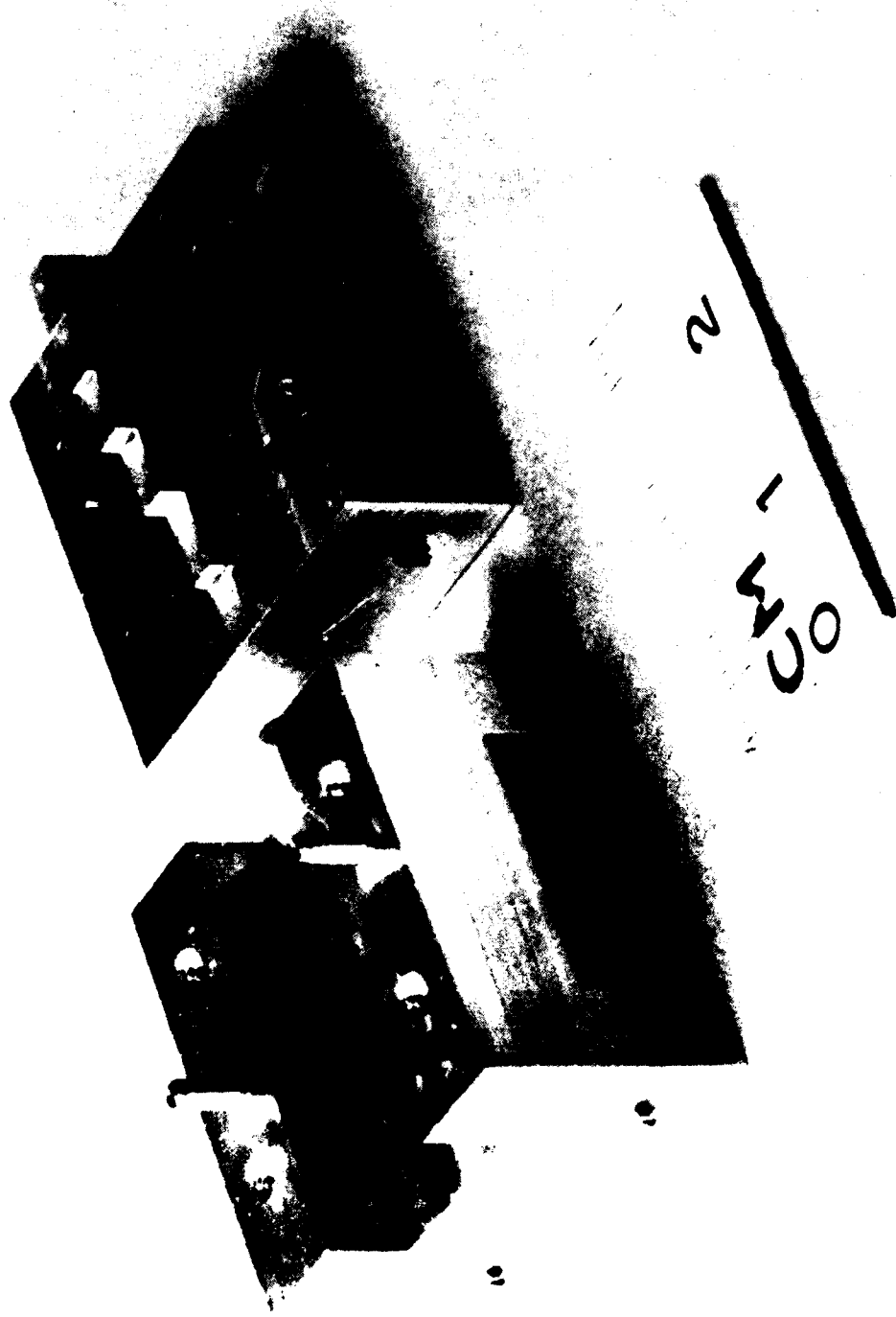
DEXCEL  
HUGHES



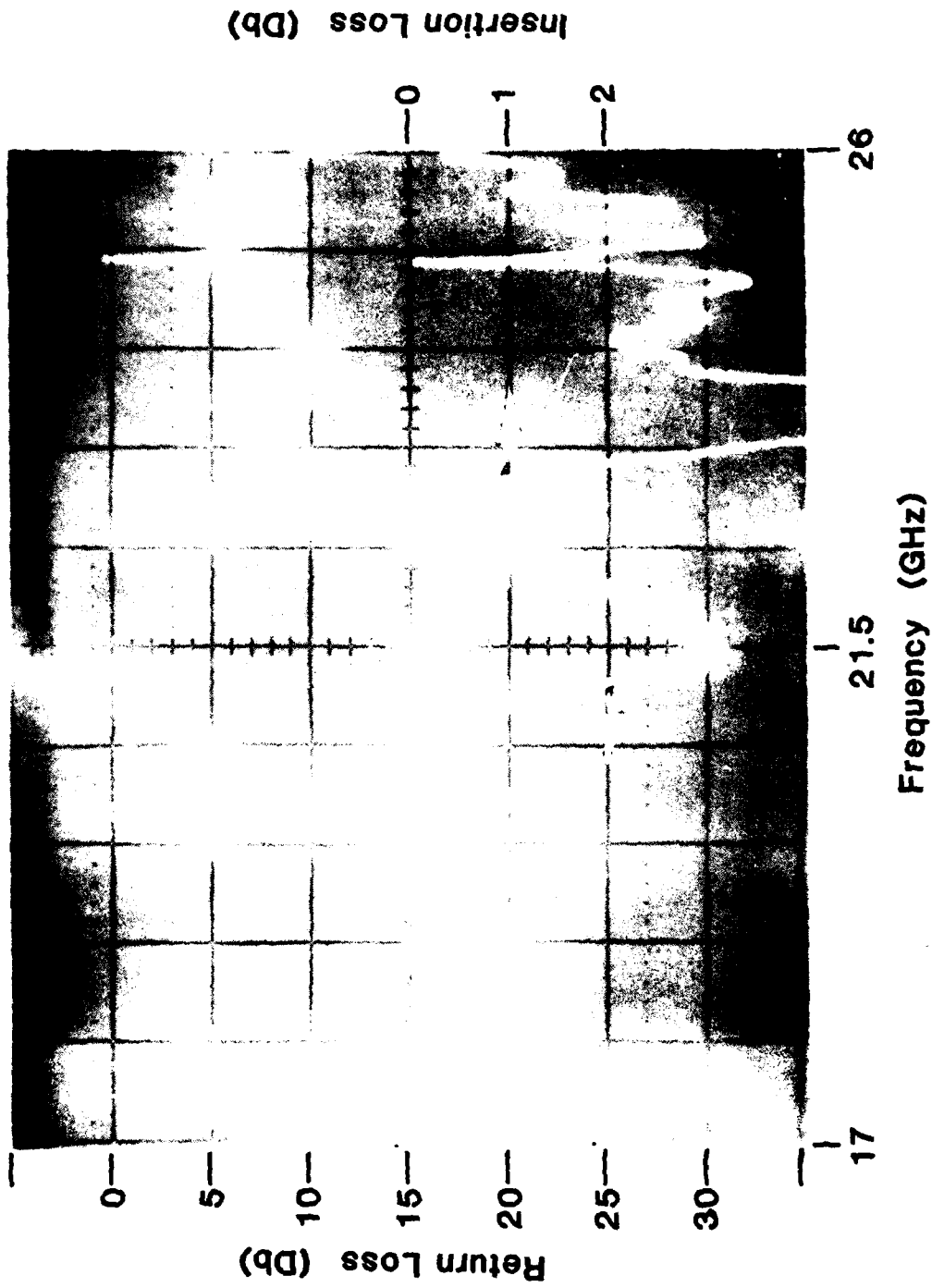
Microstrip Amplifier Power-Bandwidth Response.



Low Frequency FET Test Fixture



Ridge-Transformer Waveguide to Microstrip Transition



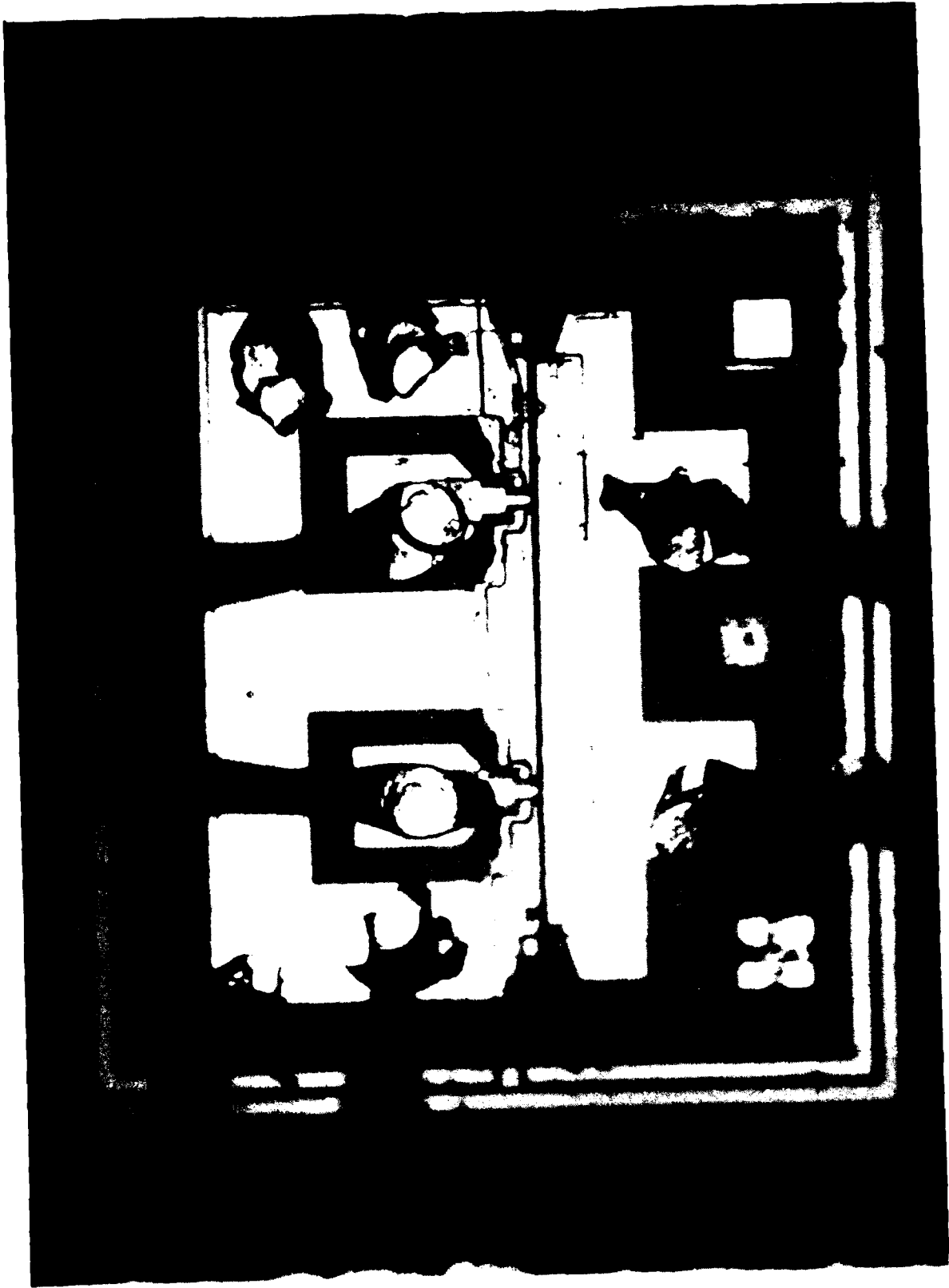
Ridge-Transformer Performance



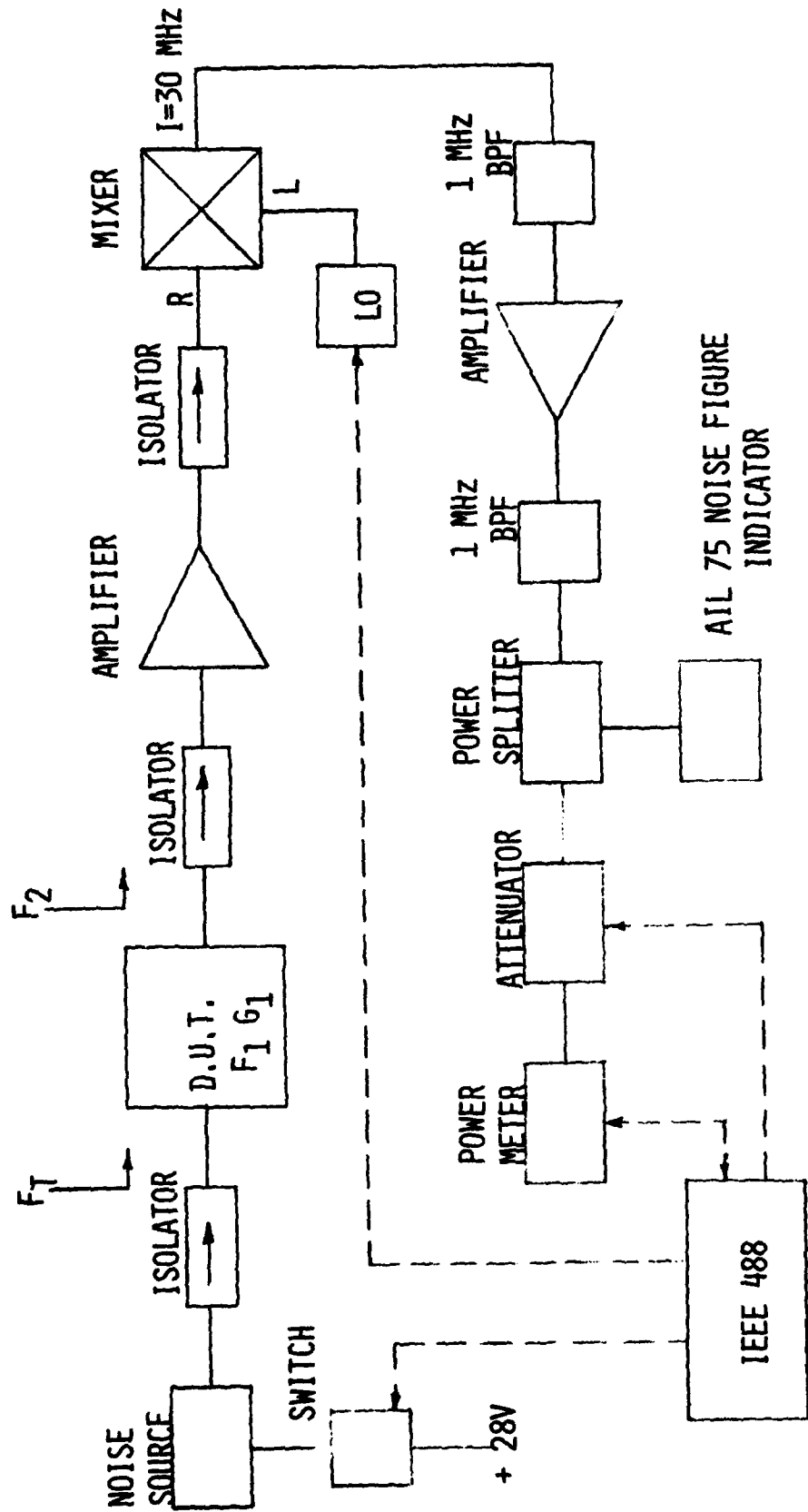
K-Band Low Noise Amplifier ( with cover )



K-Band Low Noise Amplifier ( without cover )



NEC 13700 Transistor



$$F_T = F_1 + \frac{F_2 - 1}{G_1}$$

Block Diagram - Automatic Noise Figure Measurement System



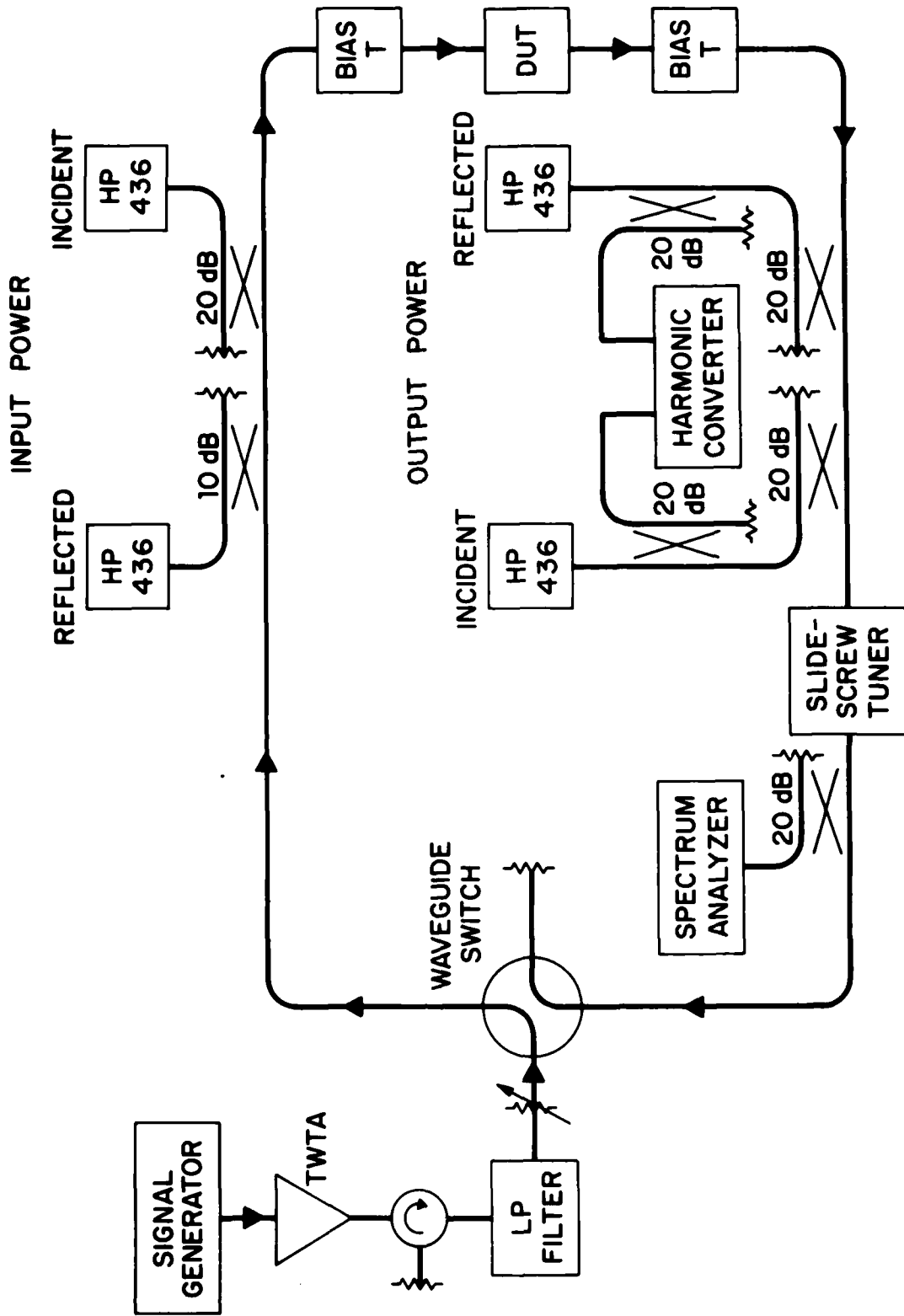
**Noise Figure Measurement Instrumentation**



Hot/Cold Waveguide Load



**K-Band 0.5W. GaAs MESFET**

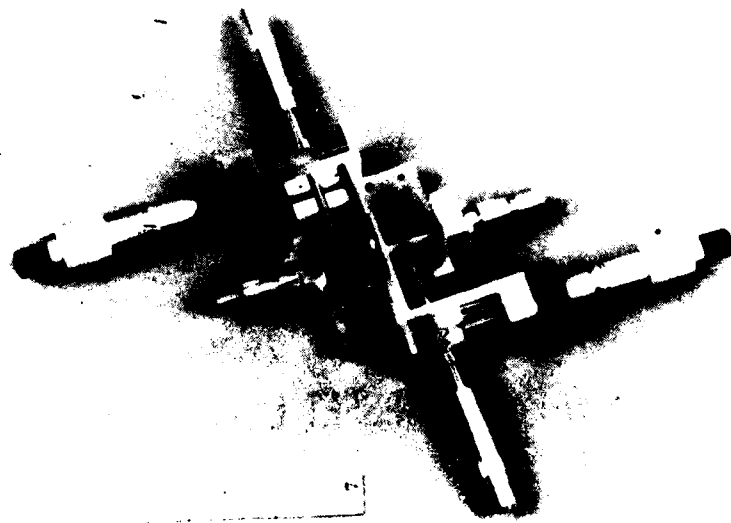


Block Diagram of Load-Pull Measurement Set-Up.

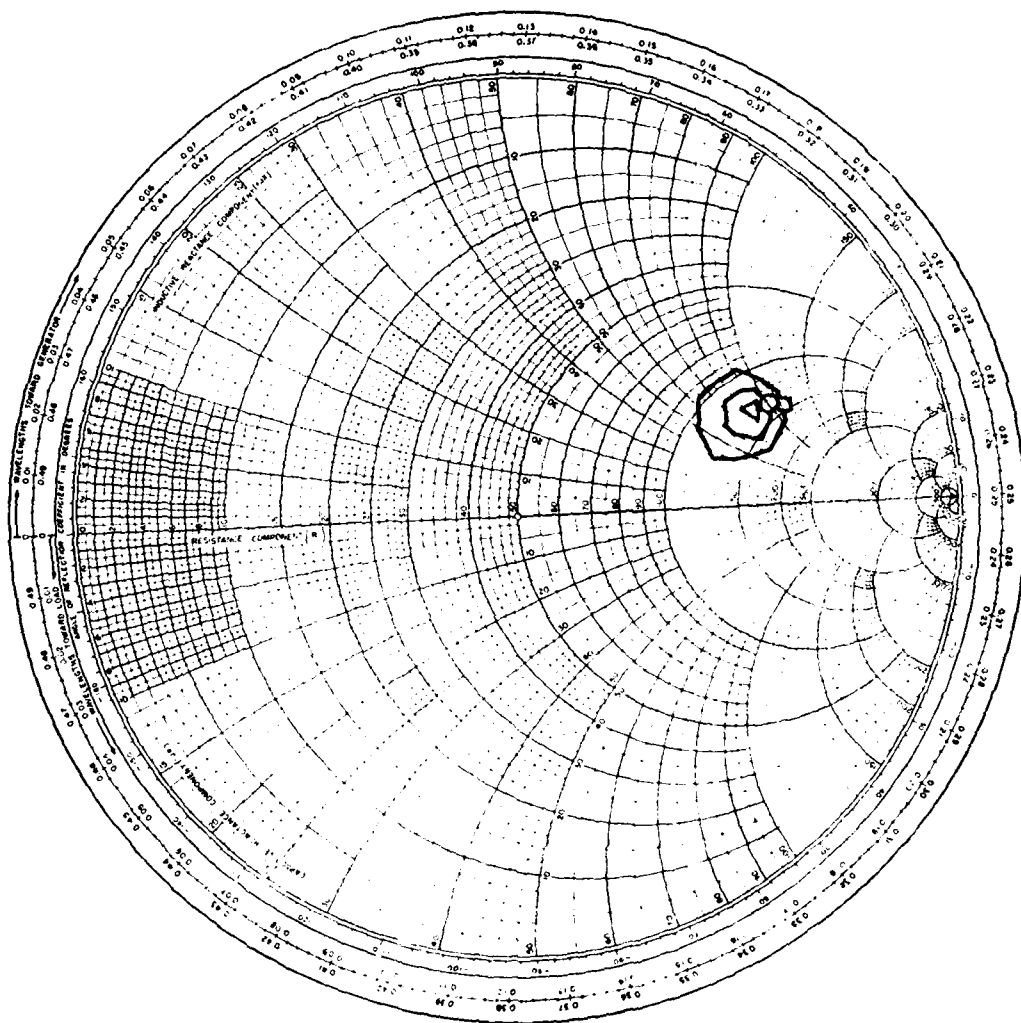




Slabline Transistor Holder



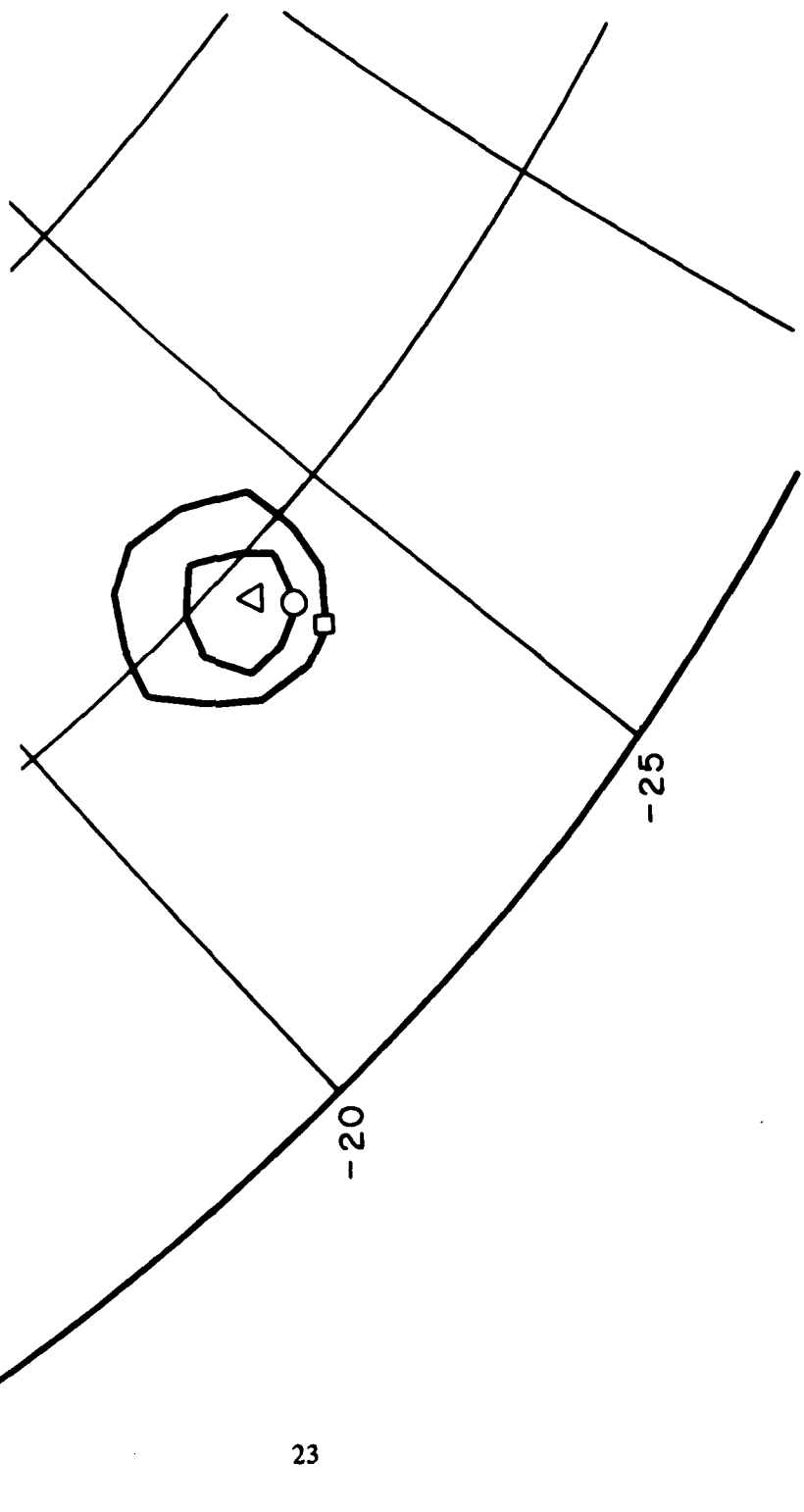
Transistor Holder (with side removed)



RING	P OUT (W)	GAIN (dB)	EFF	DC (A)
△	0.284	3.56	0.304	0.095
○	0.281	3.52	0.304	0.093
□	0.274	3.41	0.300	0.091

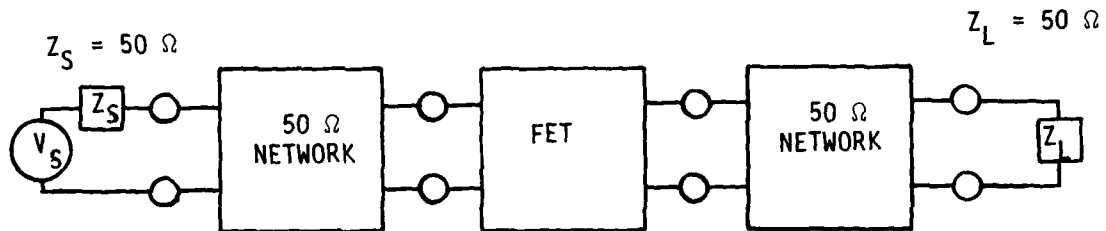
0.5 W Power MESFET Load-Pull Measurement.

RING	P OUT (W)	GAIN (dB)	EFF	IDC (A)
△	0.284	3.56	0.304	0.095
○	0.281	3.52	0.304	0.093
□	0.274	3.41	0.300	0.091



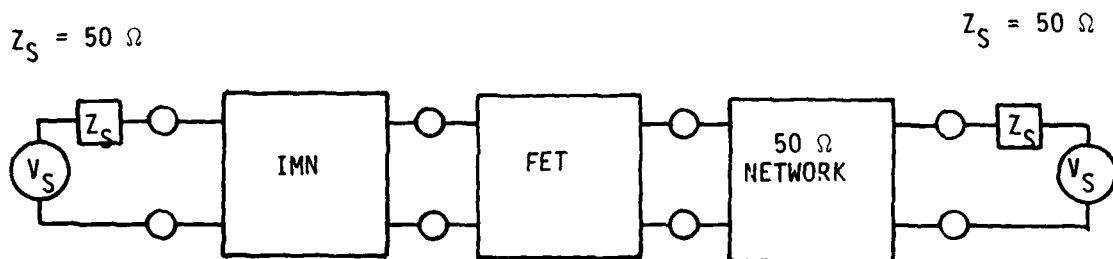
De-Embedded Load-Pull Data.

# Large Signal FET Characterization Procedure



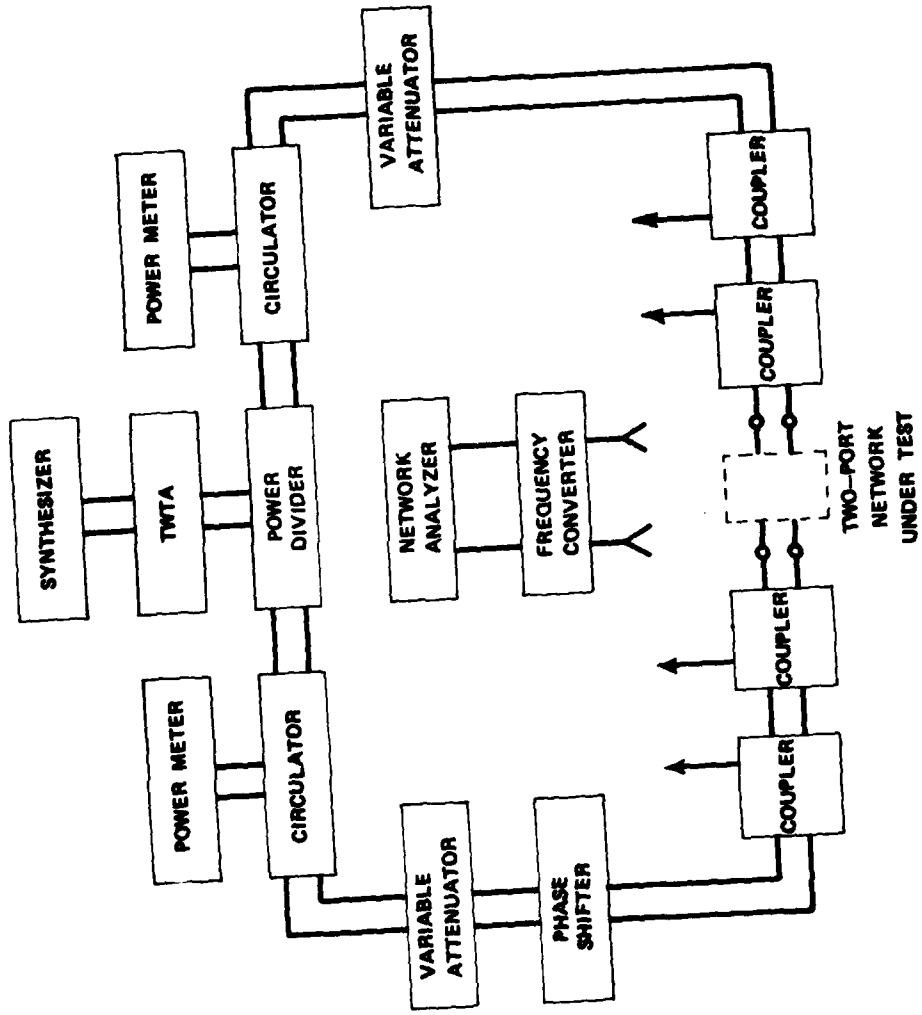
## I. CONVENTIONAL ONE-SIGNAL S-PARAMETER MEASUREMENT

- MEASURE  $S_{11}$  UNDER LARGE SIGNAL CONDITIONS
- ITERATE TO ESTABLISH DESIRED INPUT LEVEL
- DESIGN MATCHING NETWORK (IMN) FOR FET INPUT



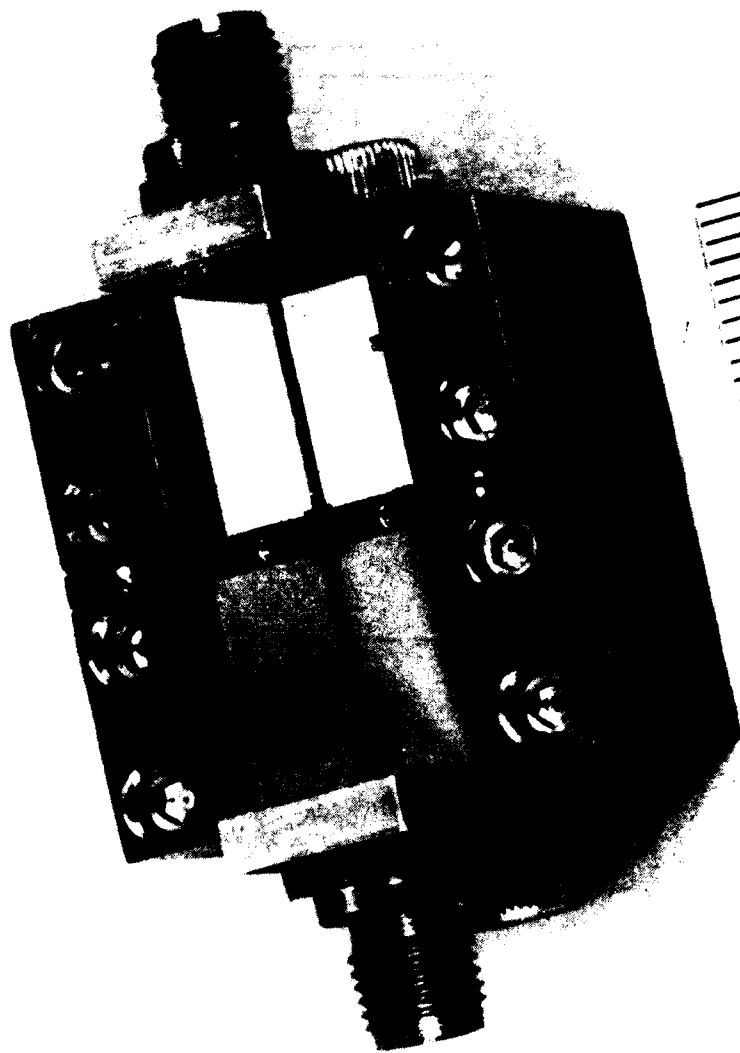
## II. TWO-SIGNAL S-PARAMETER MEASUREMENT

- INSTALL IMN AND MEASURE  $S_{11}$  TO DETERMINE INPUT MATCH
- MEASURE  $S_{22}$  UNDER LARGE SIGNAL CONDITIONS
- DESIGN OUTPUT MATCHING NETWORK

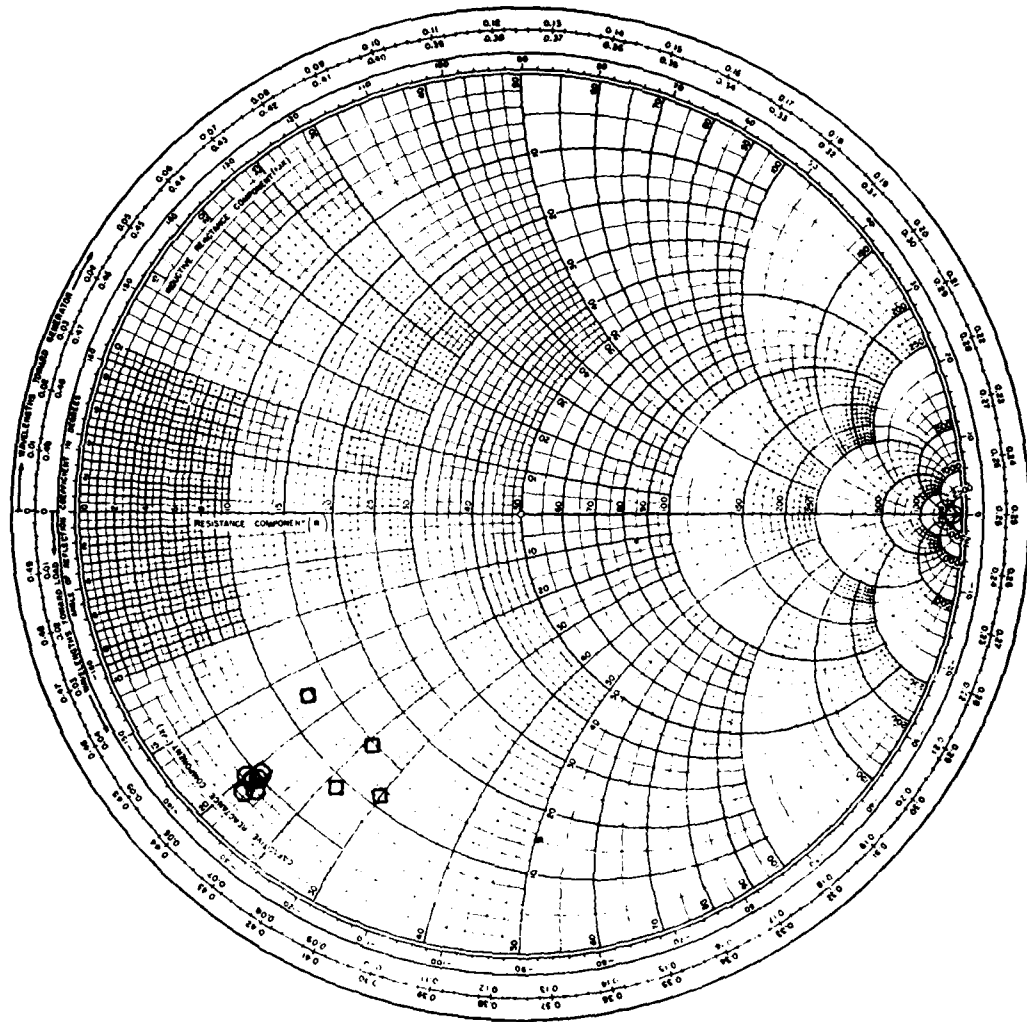


Test Configuration For Two Signal Measurement

Figure 19.

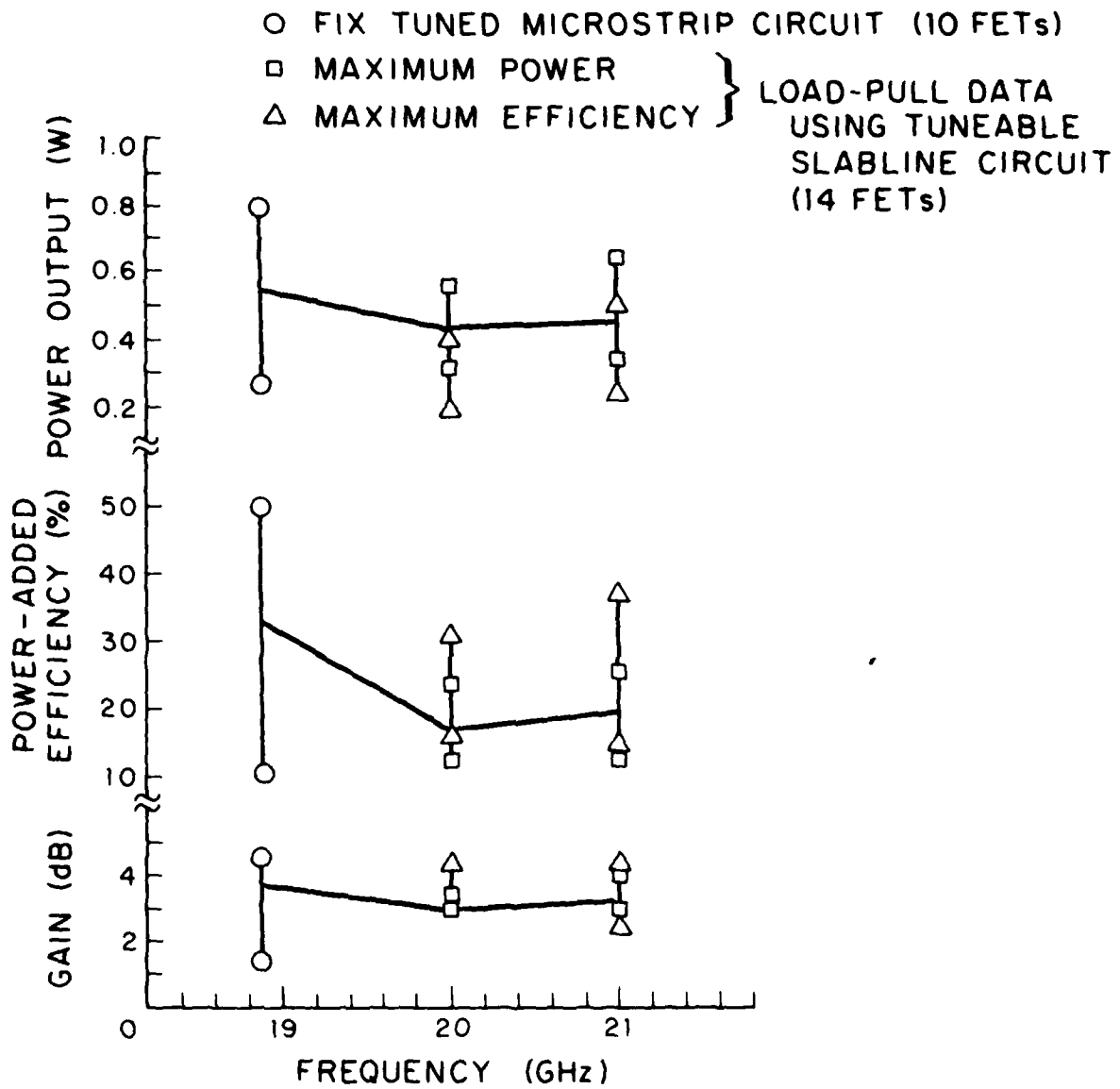


Microstrip Test Fixture

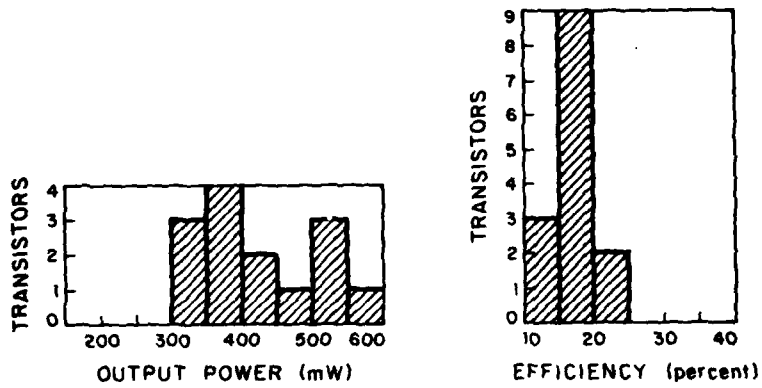


- LOAD-PULL DATA
- S-PARAMETER DATA

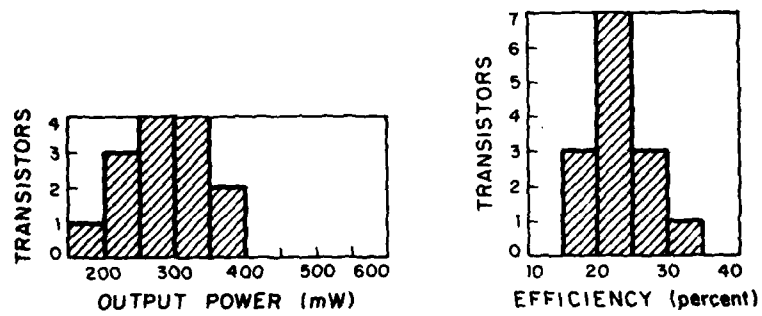
Comparison of Load-Pull and S-Parameter Data.



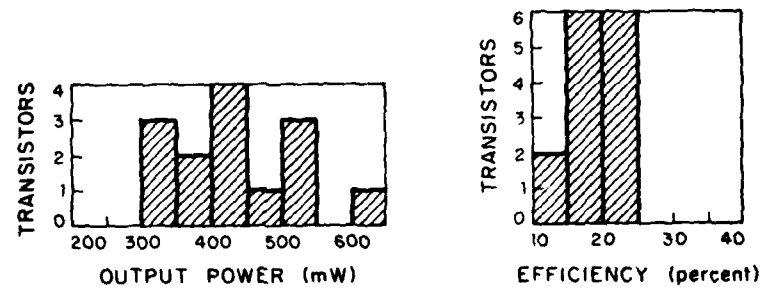
0.5 W FET Performance Versus Frequency.



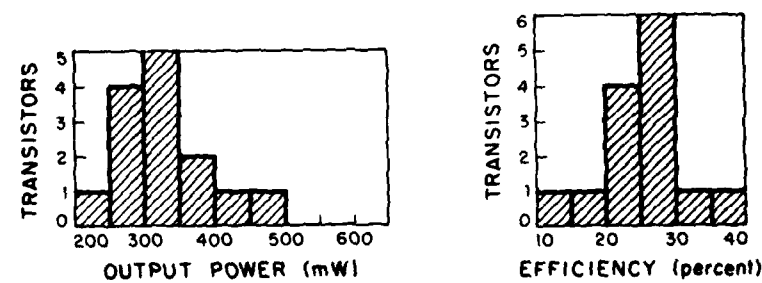
20 GHz Optimum Power Bias and Tuning.



20 GHz Optimum Efficiency Bias and Tuning.

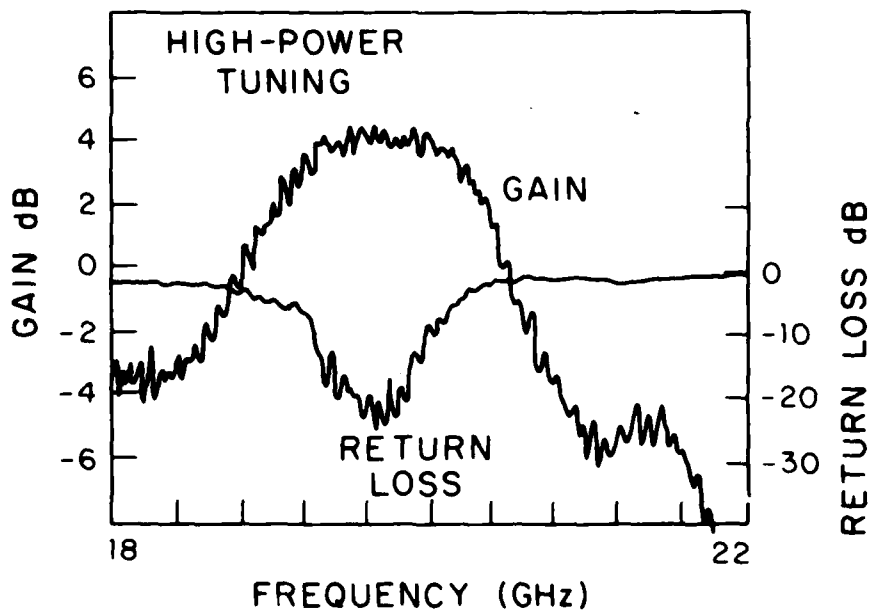
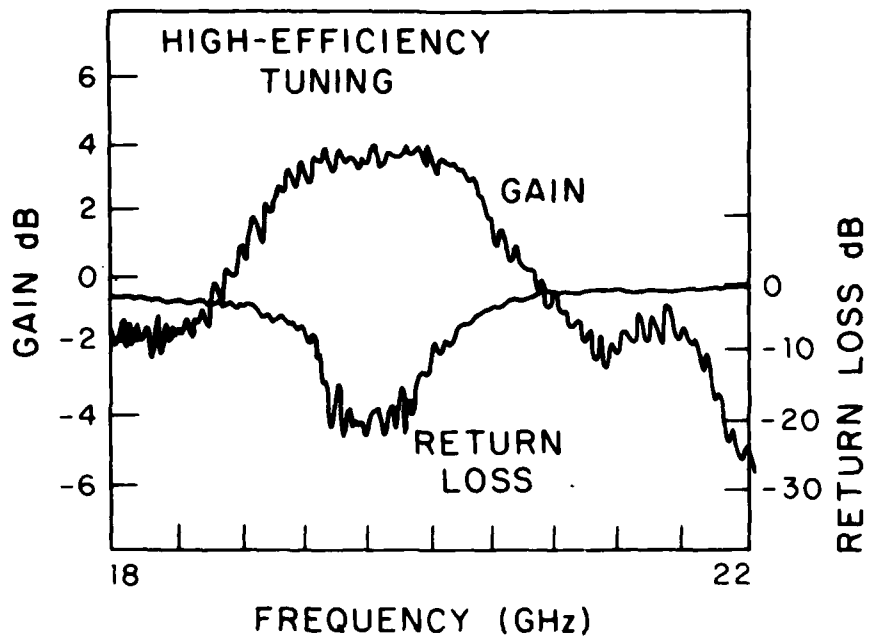


21 GHz Optimum Power Bias and Tuning.

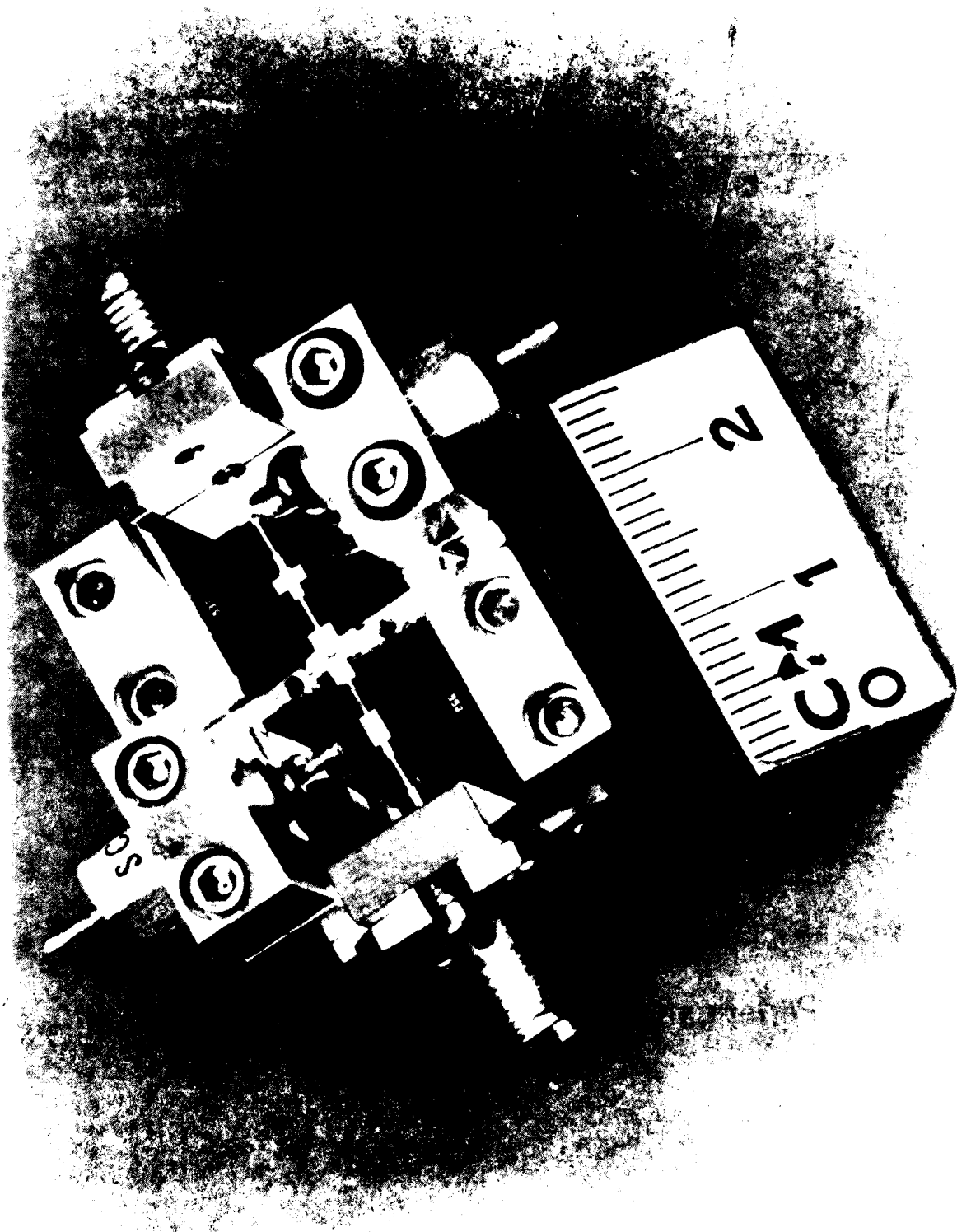


21 GHz Optimum Efficiency Bias and Tuning.

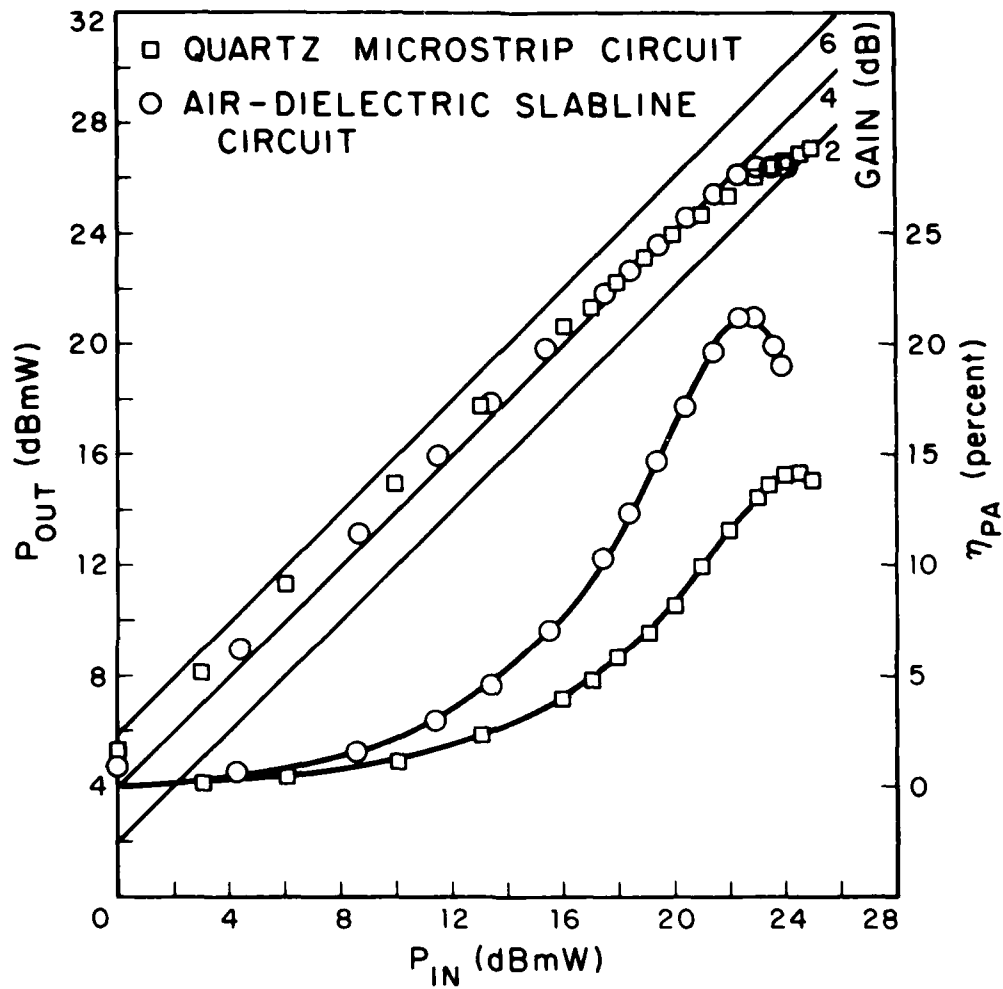
0.5 W Power MESFET Performance Summary.



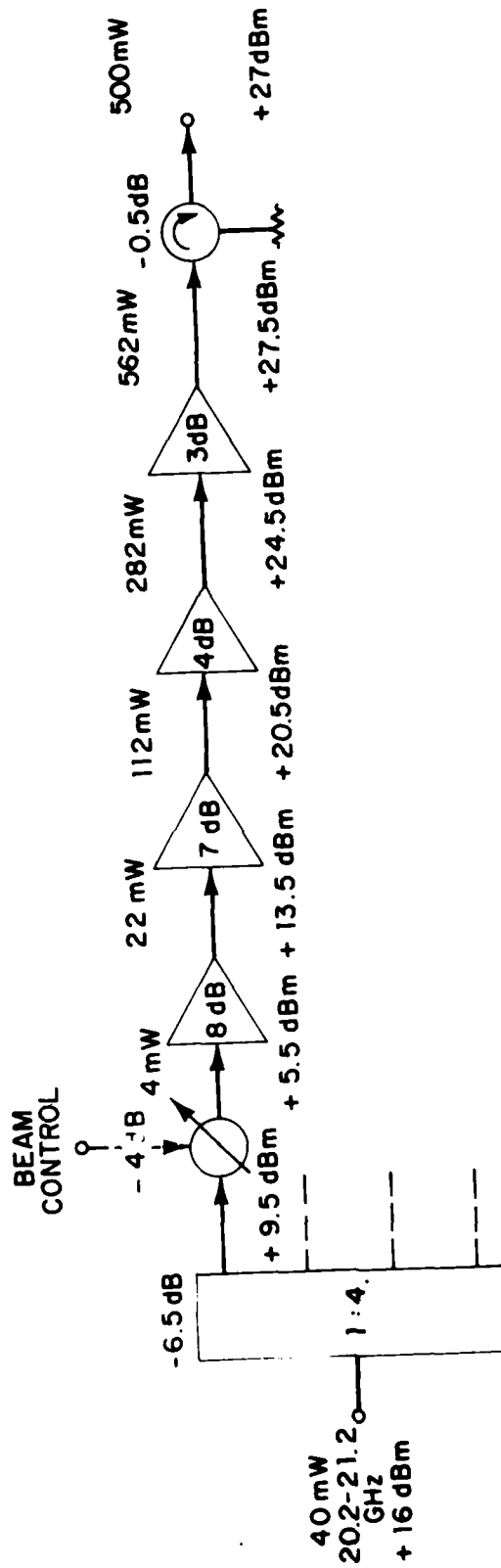
Swept Response of Slabline Amplifier.



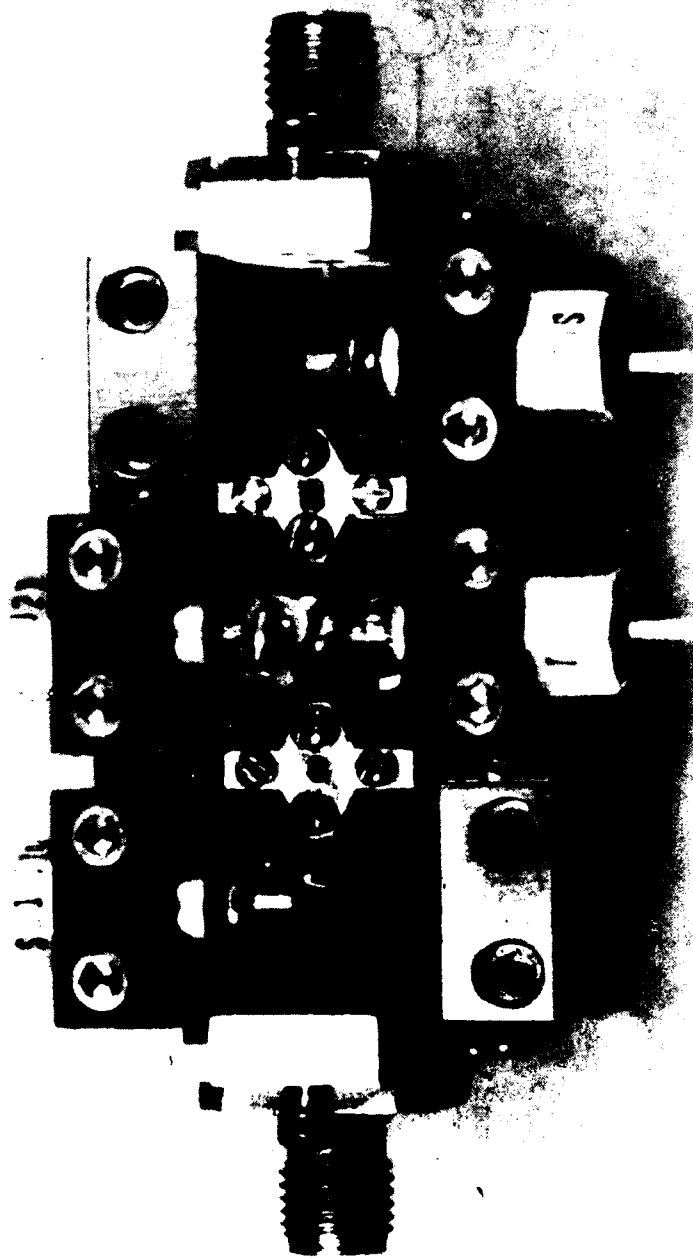
Microstrip Amplifier



Performance of Slabline and Microstrip Amplifiers.



20 GHz Transmitter Test-Bed.



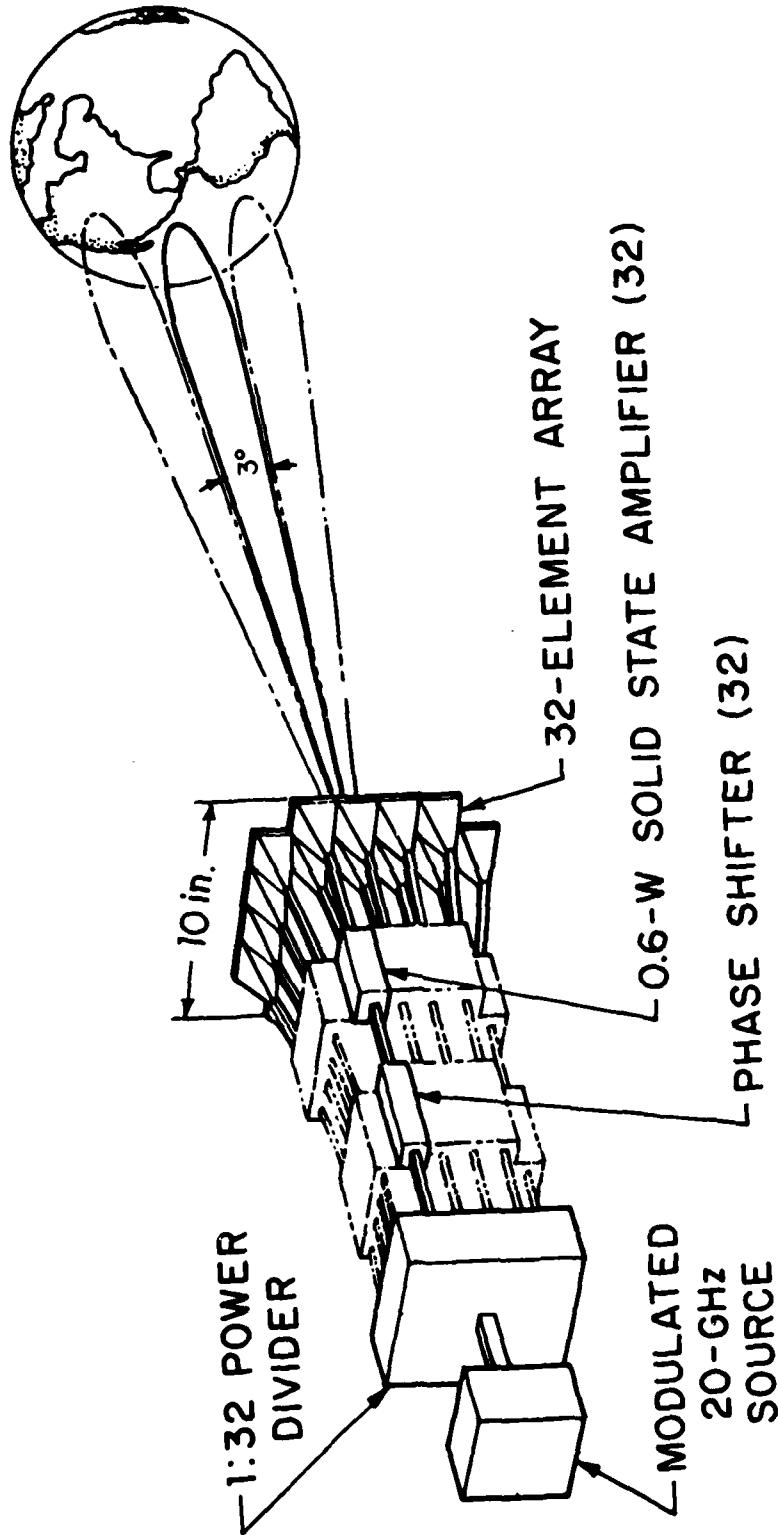
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Two-Stage Microstrip Amplifier



Artist's Conception of a Beam-Hopped Downlink Transmitter.

# Conclusion

## K-Band Receiver Development

- LOW-NOISE FET CHARACTERIZATION TECHNIQUES
- RIDGE-TRANSFORMER WAVEGUIDE/MICROSTRIP TRANSISTION
- LOW NOISE AMPLIFIER:

4.5 dB NOISE FIGURE WITH 6 dB OF GAIN

## K-Band Transmitter Development

- GaAs POWER MESFETS  
0.5 W POWER OUTPUT AT 20% POWER-ADDED EFFICIENCY
- LARGE SIGNAL FET CHARACTERIZATION TECHNIQUES  
LOAD-PULL/TWO-SIGNAL S-PARAMETERS
- FET PERFORMANCE EVALUATED IN SLABLINE AND MICROSTRIP CIRCUITRY
- COMPLETE AMPLIFIER STAGE  
0.4 W POWER OUTPUT/15% EFFICIENCY/3.0 dB GAIN

## Countinuing Development

- HIGH-GAIN (8 dB) 0.1 W FETS
- HIGH-POWER 1.0 W FETS

DESIGN AND OPTIMIZATION OF LOW NOISE AND POWER  
FETs FOR EHF APPLICATIONS

Hughes Aircraft

H. Yamasaki

(Document not available)

HIGH PERFORMANCE LOW COST MIXERS  
FOR COMMUNICATION APPLICATIONS

HUGHES AIRCRAFT

H. Yamasaki

(Document not available)

IMPATT POWER BUILDING BLOCKS FOR 20 GHz  
SPACEBORNE TRANSMIT AMPLIFIER

LNR Communications

H. C. Okean

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IMPATT POWER BUILDING BLOCKS FOR 20 GHz  
SPACEBORNE TRANSMIT AMPLIFIER

by

J. Asmus, Y. Cho, J. deGruyl, A. Giannakopoulos  
and  
H.C. Okean

presented at:

EHF SATCOM Technology Workshop  
San Diego, California  
August, 1981

IMPATT POWER BUILDING BLOCKS FOR 20 GHz

SPACEBORNE TRANSMIT AMPLIFIER\*

by

J. Asmus, Y. Cho, J. deGruyl, A. Giannakopoulos  
and  
H.C. Okean  
LNR Communications, Inc.

---

Single-stage circulator coupled IMPATT "building block" constituents of a 20 GHz solid state power amplifier (SSPA) currently under development for spaceborne downlink transmitter usage has been demonstrated as providing  $\sim 1.25$  to 1.5W RF power output at 3 to 5 dB operating gain over a 1 GHz bandwidth. Using either commercially available or recently developed in-house GaAs Schottky Read-profile IMPATT diodes, DC/RF power added efficiencies of 11 to 15 percent were achieved. A two stage IMPATT driver amplifier with similar RF output power capability exhibited  $13 \pm 0.5$  dB operating gain over a 1 GHz bandwidth. A companion 20 GHz FET driver preamplifier is also under development. Extension of the above to the development of a "full-up" 20W IMPATT transmitter is currently in progress.

---

\*This effort is sponsored in part by NASA Lewis Research Center and the Air Force Avionics Laboratory under Contracts No. NAS3-22491 and F33615-80C-1182, respectively.

20 GHz SOLID STATE TRANSMITTER DESIGN OBJECTIVES

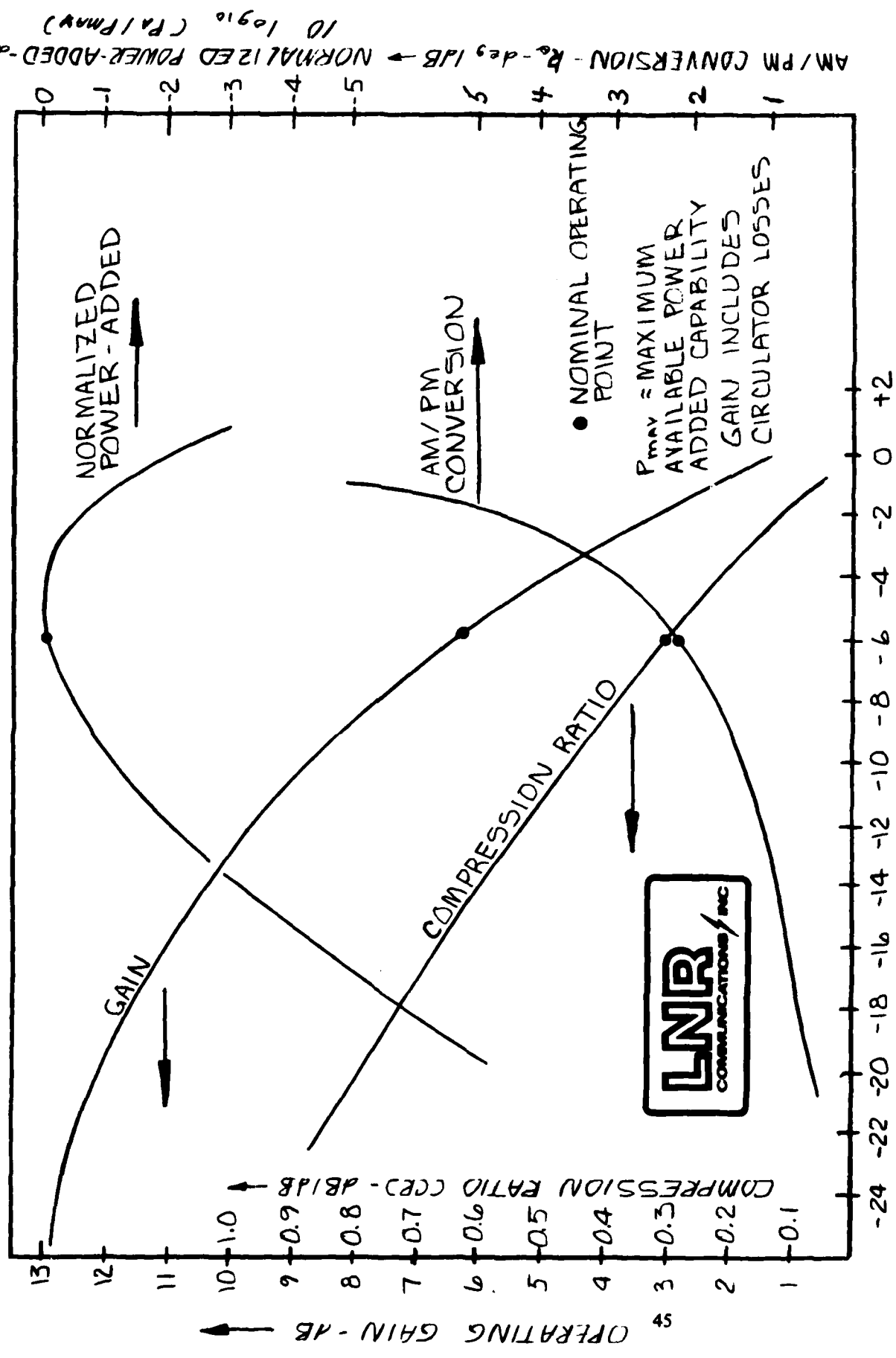
DESIGN OBJECTIVE (OVER PASSBAND)

PARAMETRIC

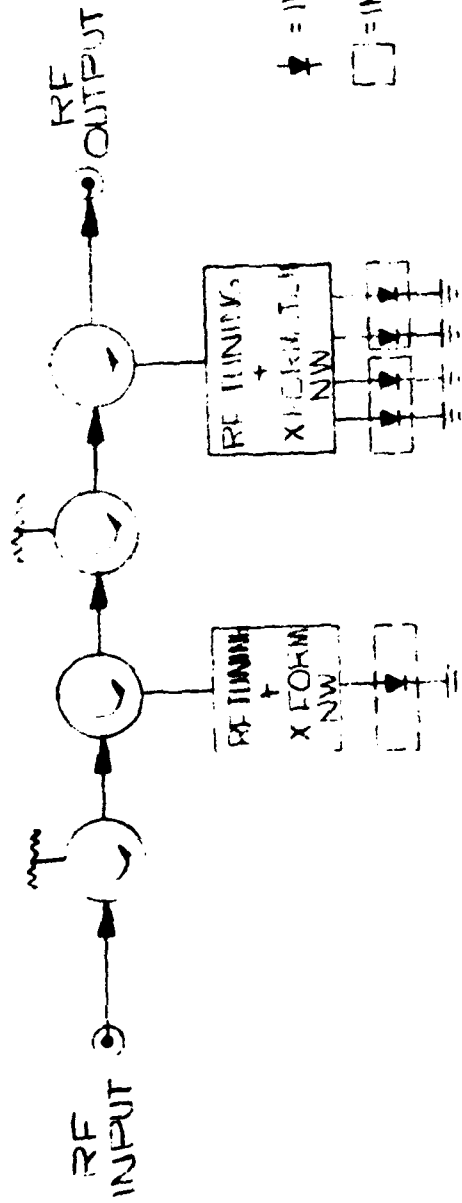
INPUT SIGNAL FORMAT	ANGLE MODULATED, SINGLE CARRIER
CENTER FREQUENCY	20 GHz
RF BANDWIDTH	1.0 GHz
SATURATED RF OUTPUT POWER	20 WATTS (MIN)
RF POWER OUTPUT VARIATION WITH FREQUENCY AND TEMPERATURE	0.6DB (P-P) @ NOMINAL DRIVE LEVEL 1.2DB (P-P) OVER NOMINAL +2DB DRIVE LEVEL RANGE
RF GAIN @ SATURATION	30 DB (MIN)
IN BAND OVERDRIVE SURVIVABILITY	5 DB ABOVE NOMINAL INPUT LEVEL
GAIN SLOPE	0.1 DB/MHz (MAX)
INPUT VSWR	1.25:1 (MAX)
OUTPUT VSWR	1.5:1 (MAX)
GROUP DELAY VARIATION	0.5 ns P-P (MAX) OVER 50 MHz SLOT
AM/PM CONVERSION	6°/DB (MAX)
DEVIATION FROM PHASE LINEARITY	10° (MAX)
SPURIOUS RESPONSE (SUM OF HARMONIC COMPONENTS)	17 DB BELOW CARRIER
SPURIOUS RESPONSE (NON-HARMONIC COMPONENTS)	60 DB BELOW CARRIER/20 MHz BAND
NOISE FIGURE	25 DB (MAX)
DC-RF EFFICIENCY	15 PERCENT (MIN)
PRIME DC VOLTAGE INPUT	28 V (NOM)
BASEPLATE TEMPERATURE	0 TO 50°C



TRANSFER CHARACTERISTICS OF "BUILDING BLOCK" IMPATT AMPLIFIER STAGE



NORMALIZED INPUT POWER  $10 \log_{10} (P_{in} / P_{max})$  - dB



⚡ = IMPATT MESA

[ ] = IMPATT PACKAGE

PROJECTED PERFORMANCE

- FREQUENCY RANGE:
- RF OUTPUT LEVEL:
- RF INPUT LEVEL:
- OPERATING GAIN:
- DC POWER CONSUMPTION:
- RE/DC POWER-ADDED EFFICIENCY:
- GAIN COMPRESSION:
- AM/PM CONVERSION:
- NOISE FIGURE:
- GAIN FLATNESS:
- PHASE LINEARITY:

PREAMP

-----19.5-20.5 GHz-----	6.25W
1.56W	0.36W
0.02W	12.3dB
18.9dB	25W
10W	23.5%
15.4%	0.09dB/dB
0.18dB/dB	3.4 deg/dB
2.5 deg/d	32.5dB
30.5dB	+0.2dB
+0.3dB	+2 deg
+3 deg	

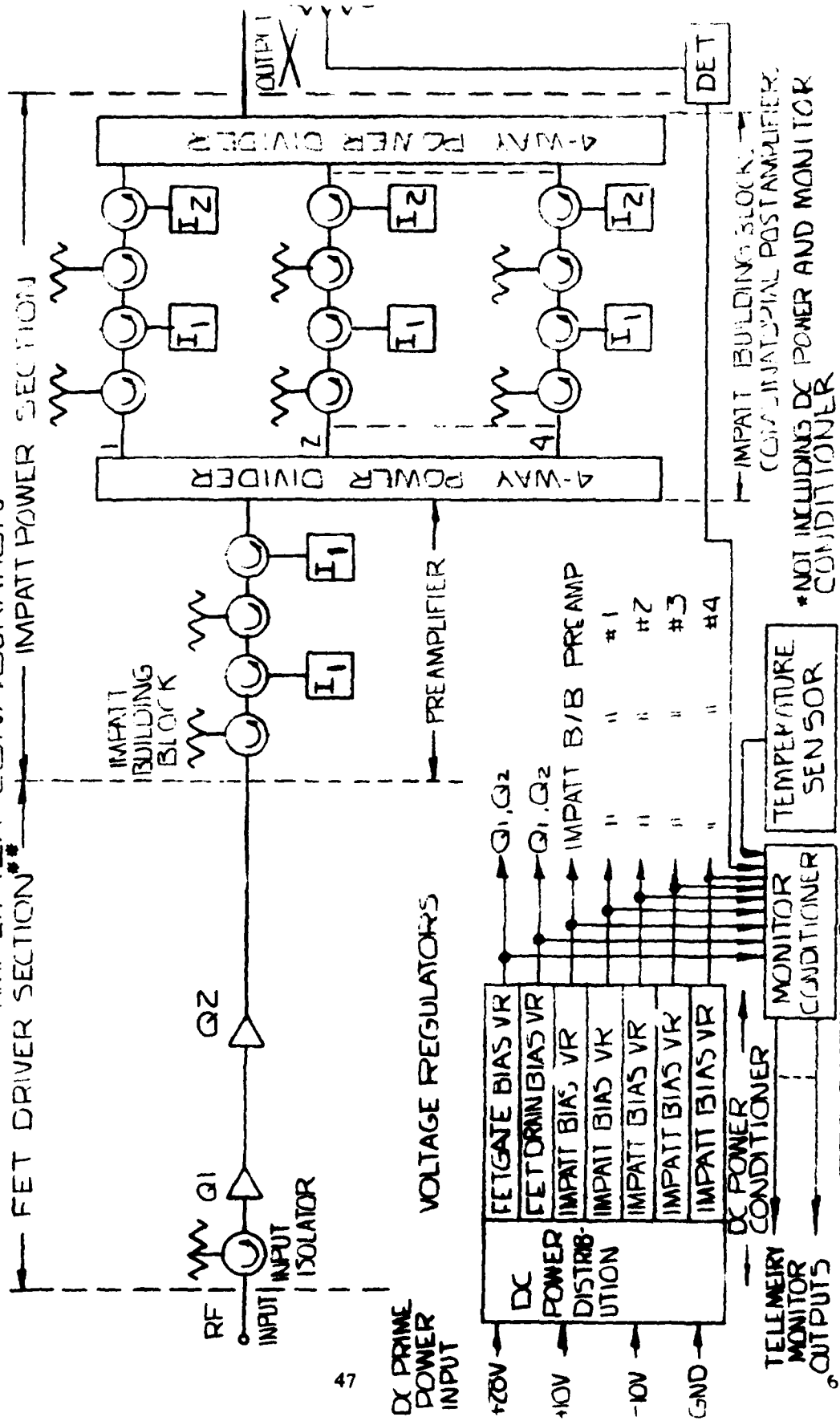
COMBINATORIAL POSTAMP

-----19.5-20.5 GHz-----	6.25W
1.56W	0.36W
0.02W	12.3dB
18.9dB	25W
10W	23.5%
15.4%	0.09dB/dB
0.18dB/dB	3.4 deg/dB
2.5 deg/d	32.5dB
30.5dB	+0.2dB
+0.3dB	+2 deg
+3 deg	

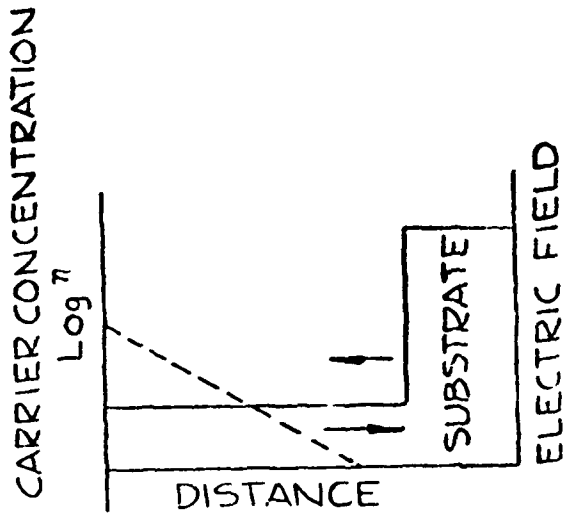
PREFERRED 20 GHz IMPATT POWER SECTION  
 "BUILDING BLOCK" AMPLIFIER DESIGN



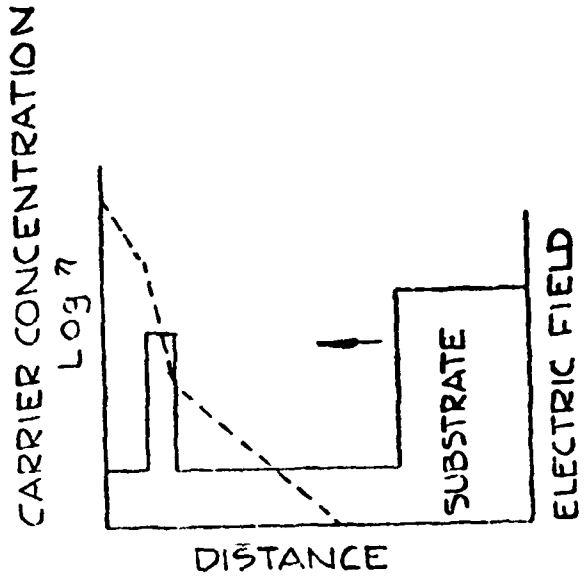
PREFERRED 20 GHz TRANSMITTER  
AMPLIFIER CONFIGURATION



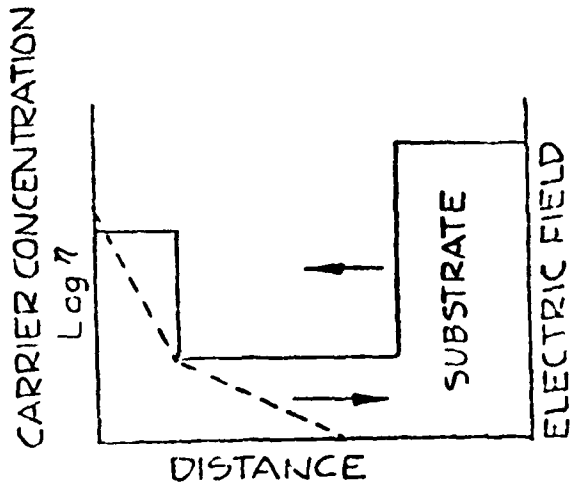
- PROJECTED CHARACTERISTICS
- RF OUTPUT LEVEL: 22.5 W (MIN) • POWER-ADDED EFFICIENCY: 20.4 PERCENT (MIN)\*
  - RF INPUT LEVEL: 27 W (NOM) • GAIN COMPRESSION: 0.016 dB/dB (MAX)
  - OPERATING GAIN: 39.5 dB (NOM) • AM/PM CONVERSION: 5.9 dB/dB (MAX)
  - DC PRIME POWER: 120 W (MAX)\* • NOISE FIGURE: 22.5 dB (NOM)
- \* NOT INCLUDING DC POWER AND MONITOR CONDITIONER



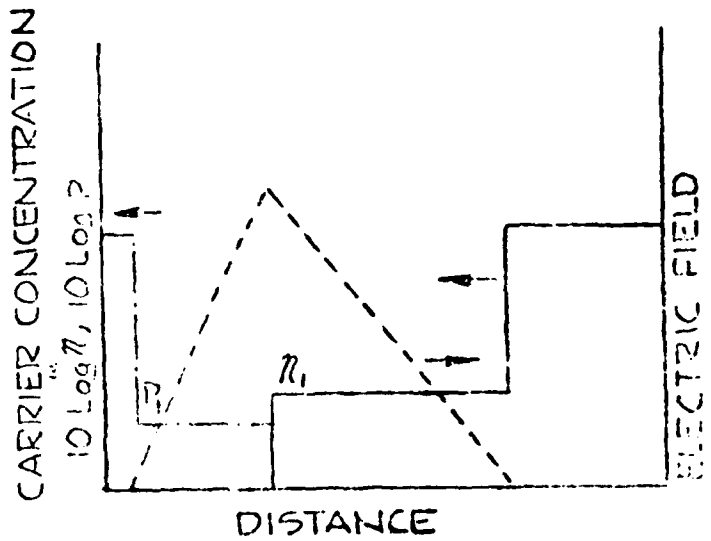
A. SDR FLAT DOPING PROFILE



C. SDR LHL DOPING PROFILE (MODIFIED READ)



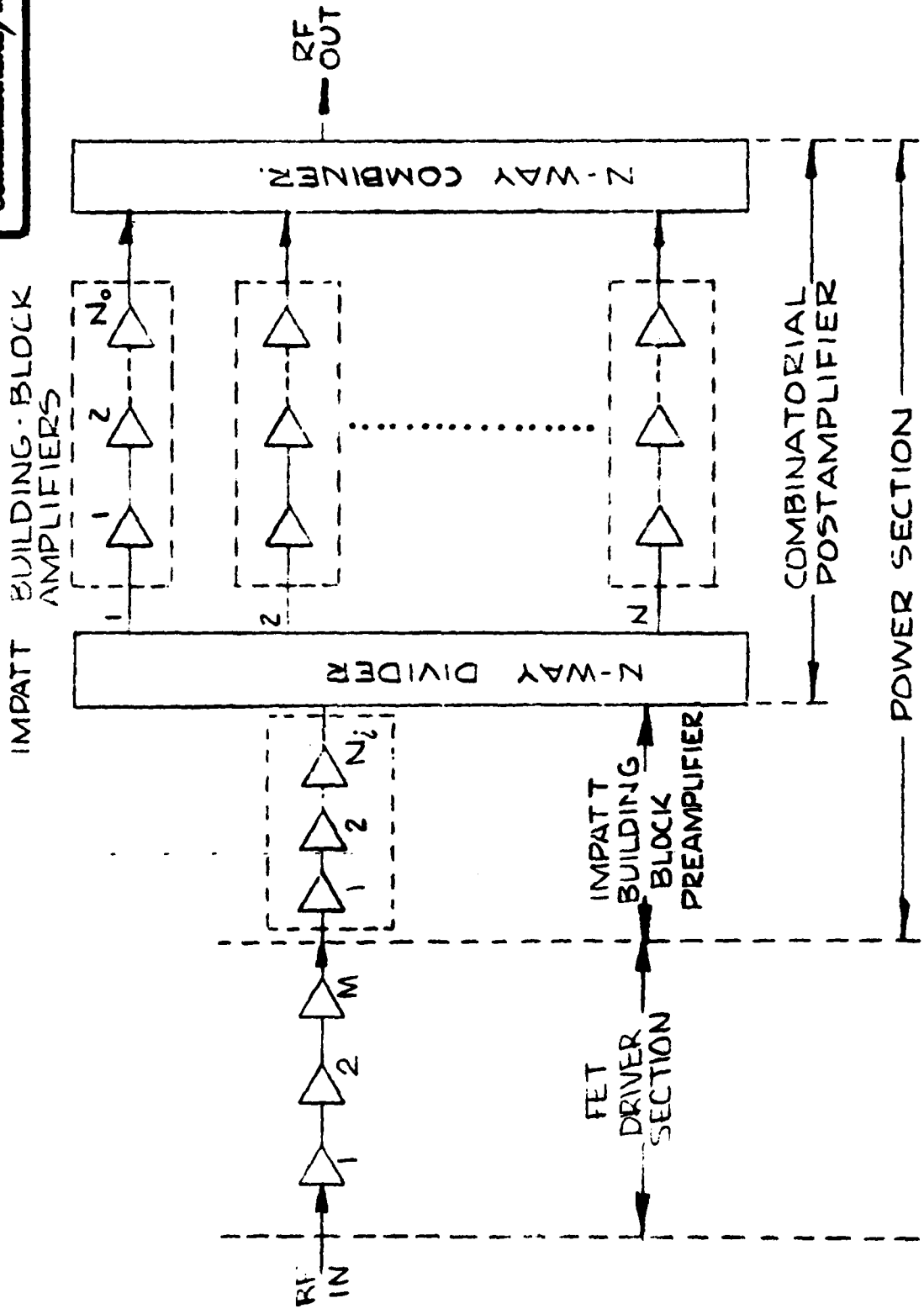
B. SDR HI-LO PROFILE (MODIFIED READ)



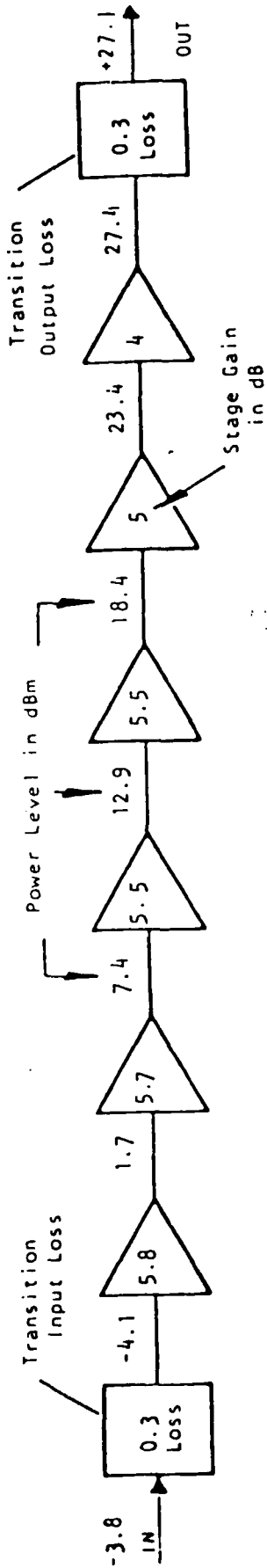
D. DDR FLAT PROFILE

ALTERNATIVE IMPATT DIODE DOPING PROFILES





FUNCTIONAL RF TOPOLOGY OF 20GHz IMPATT TRANSMITTER



Gain Stage	1	2	3	4	5	6
Gate Width ( $\mu\text{m}$ )	150	150	300	600	1350	2x1350
Current (mA)	30	30	60	120	250	500
Voltage (V)	7	7	7	7	7	7
Efficiency (%)	0.5	1.9	3.3	5.9	8.5	9.4

Total Module Gain - 30.9 dB  
 Module Output Power - 513 mW  
 DC Input Power - 6.93 W  
 Module Efficiency - 7.4%

Modified Block Diagram of 31 dB Amplifier Module Including Bias Schedule  
 (Linear Amplifier)

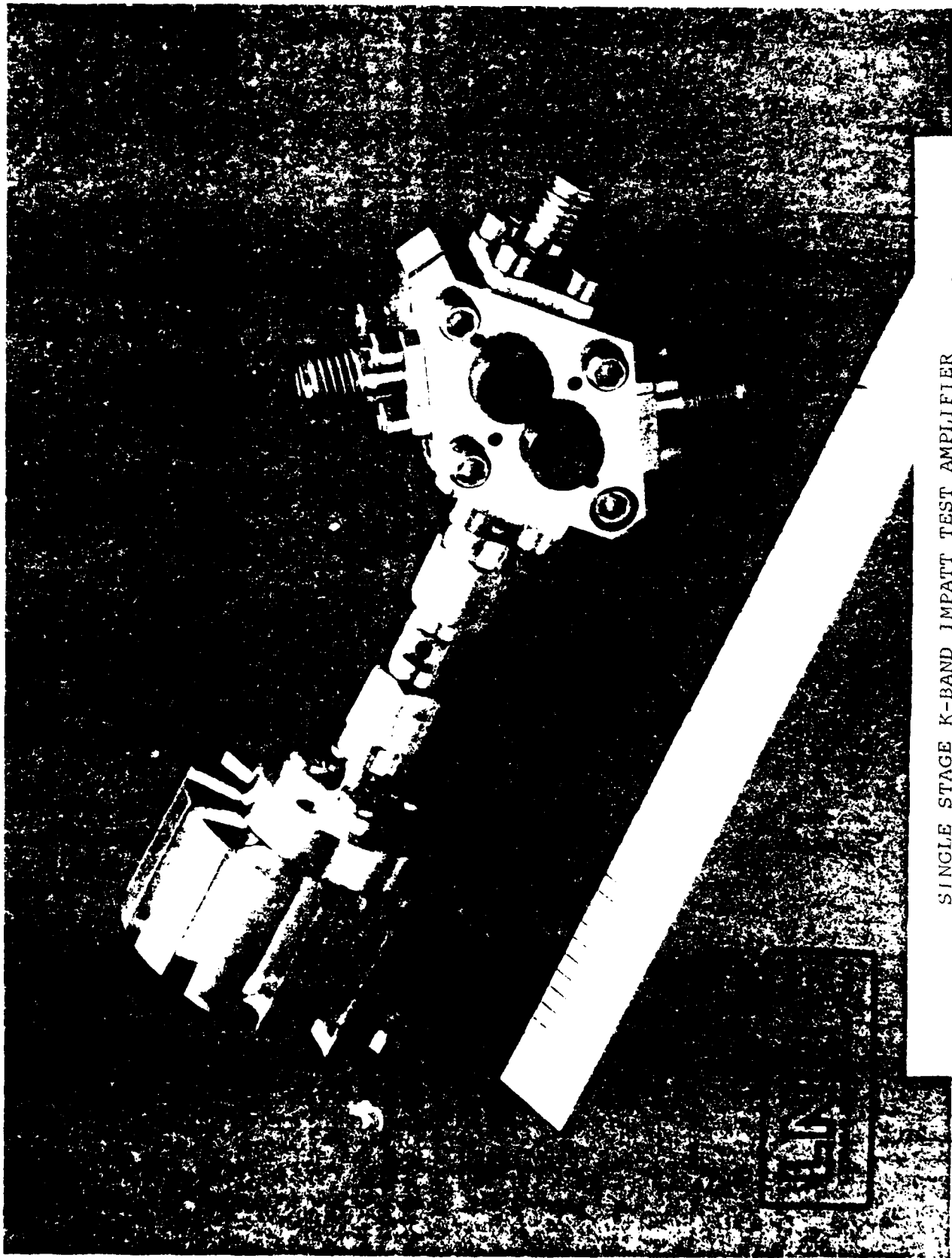
IN-HOUSE K-BAND IMPATT DIODE DEVELOPMENT STATUS

1) TYPE:

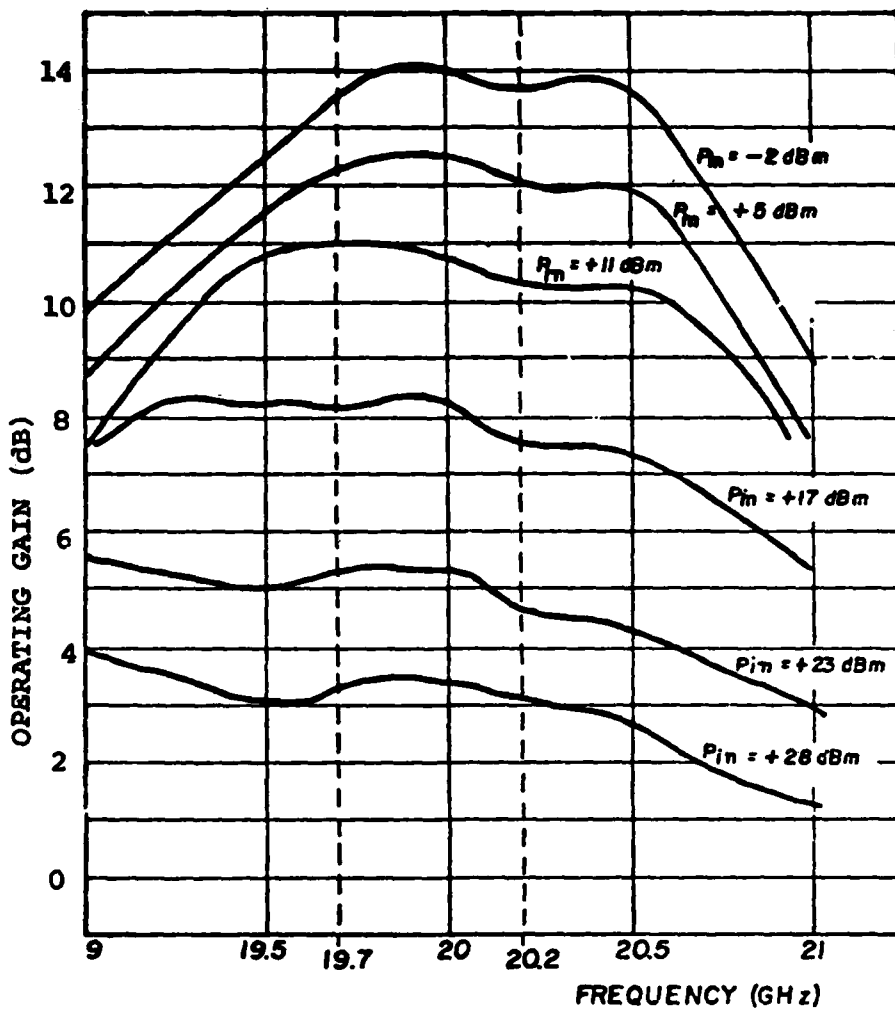
- GaAs MODIFIED READ-PROFILE (LHL)
- SINGLE DRIFT

2) SUMMARY OF RESULTS TO DATE

• FREQUENCY GHz	16-18	18-20
• RF POWER OUTPUT-W (TEST OSC.)	1.5-3.0	1.25-1.75
• DC/RF EFFICIENCY-PERCENT	15-20	10-15
• THERMAL RESISTANCE °C/W	20	20-22

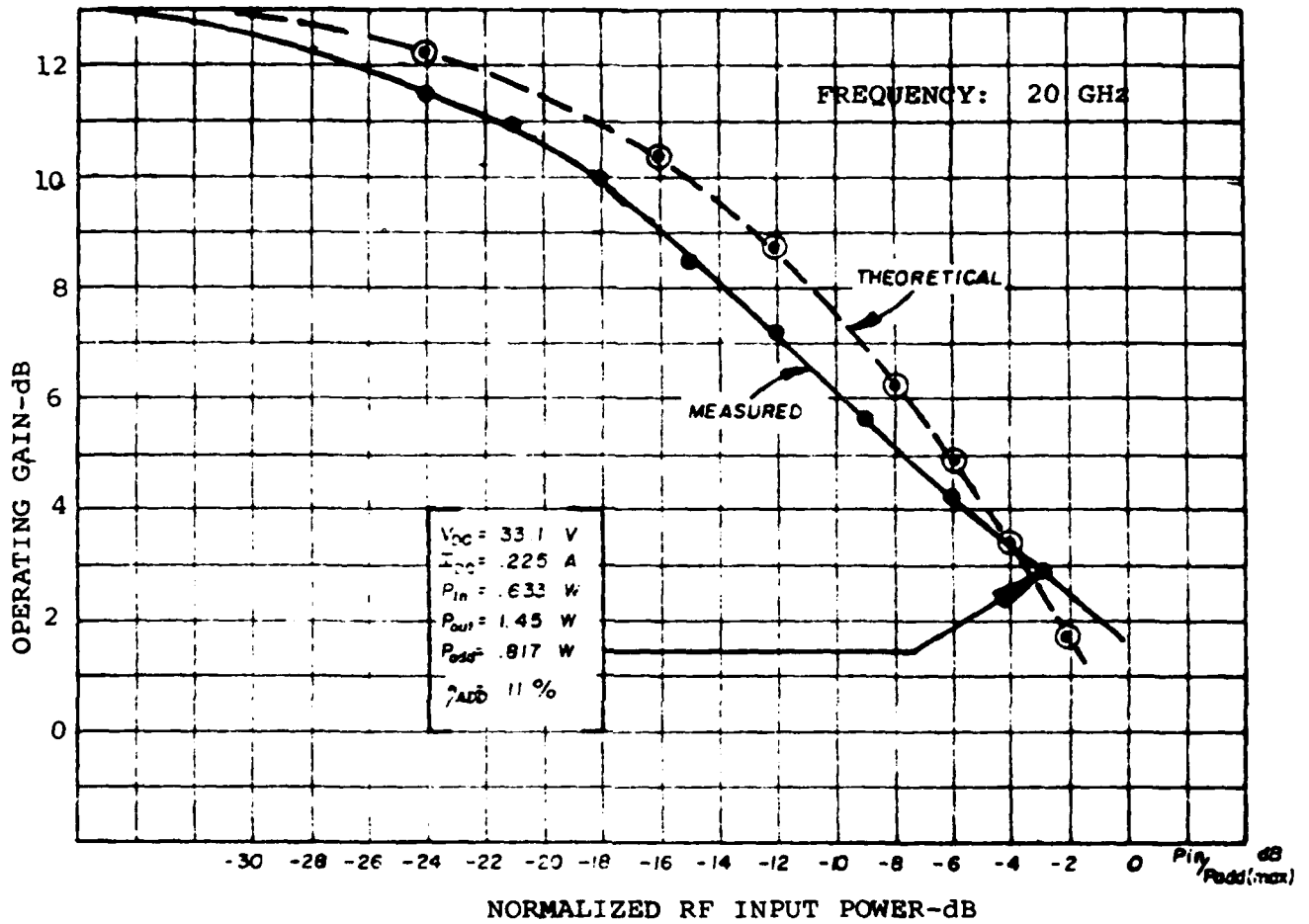


SINGLE STAGE K-BAND IMPATT TEST AMPLIFIER



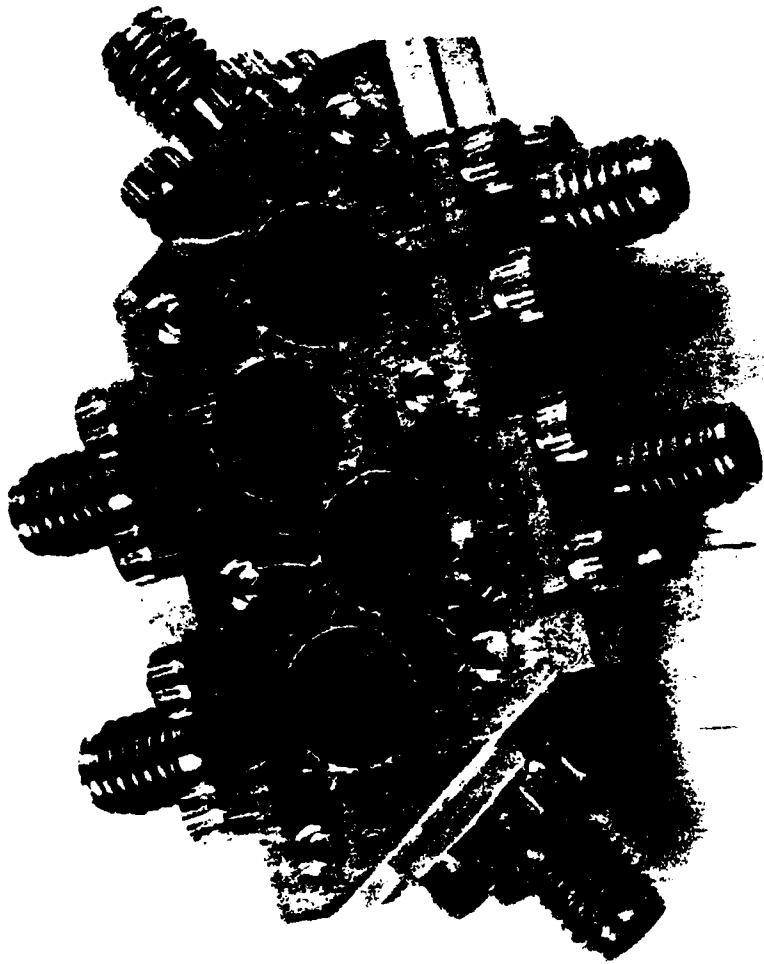
MEASURED GAIN OF SINGLE-STAGE IMPATT AMPLIFIER  
UTILIZING LNR IMPATT DIODE



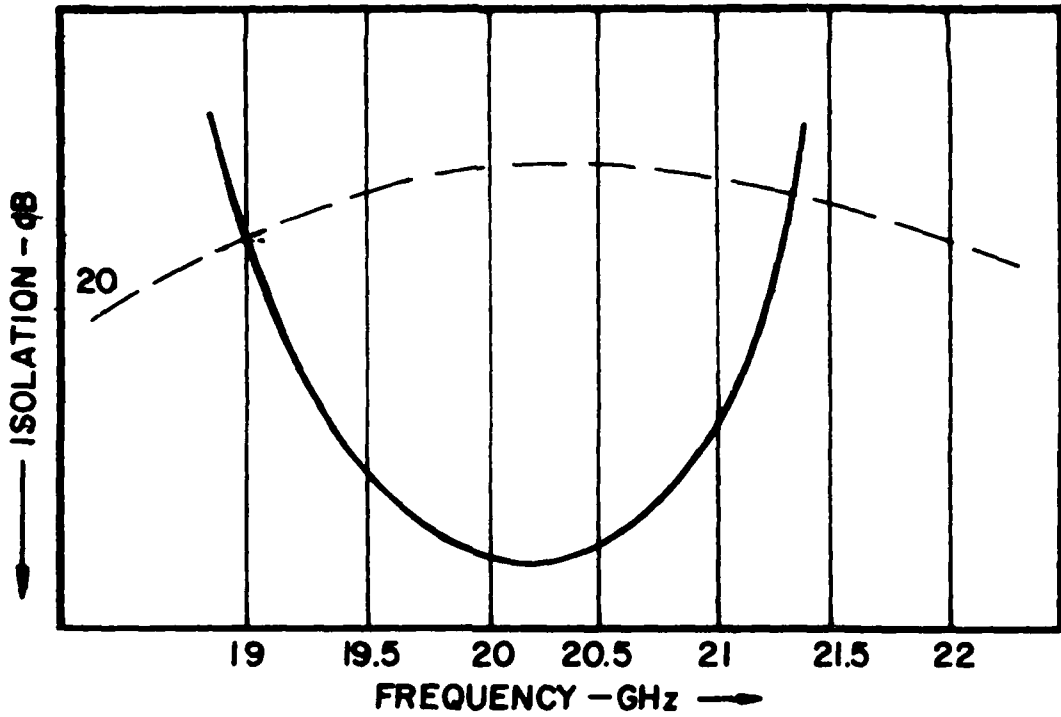


RF TRANSFER CHARACTERISTIC OF SINGLE-STAGE  
AMPLIFIER UTILIZING LNR IMPATT DIODE

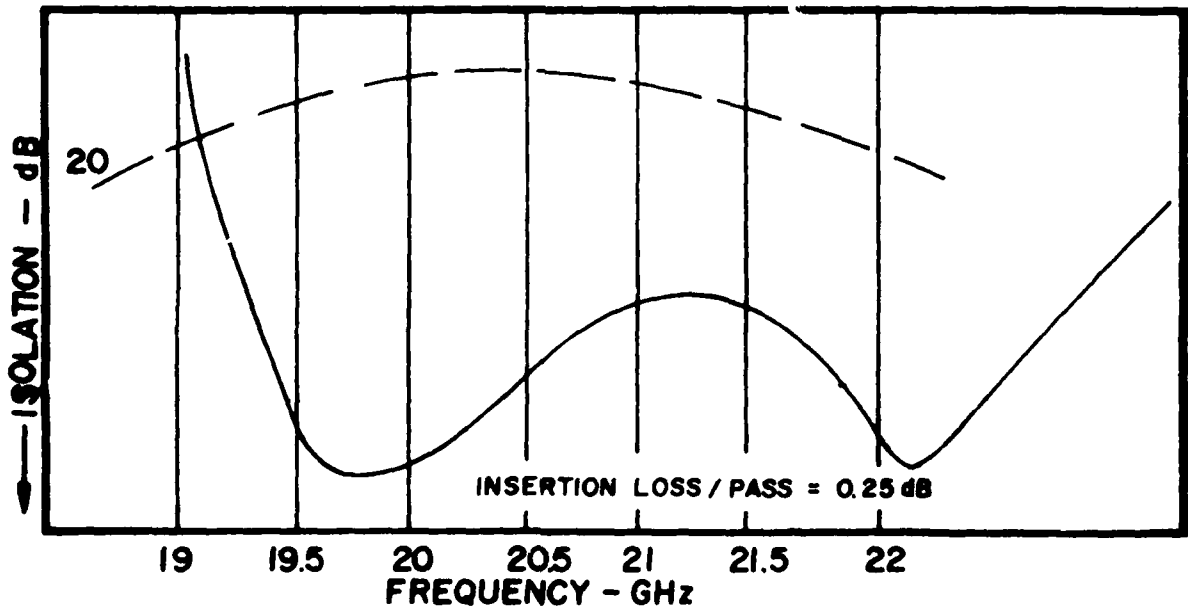




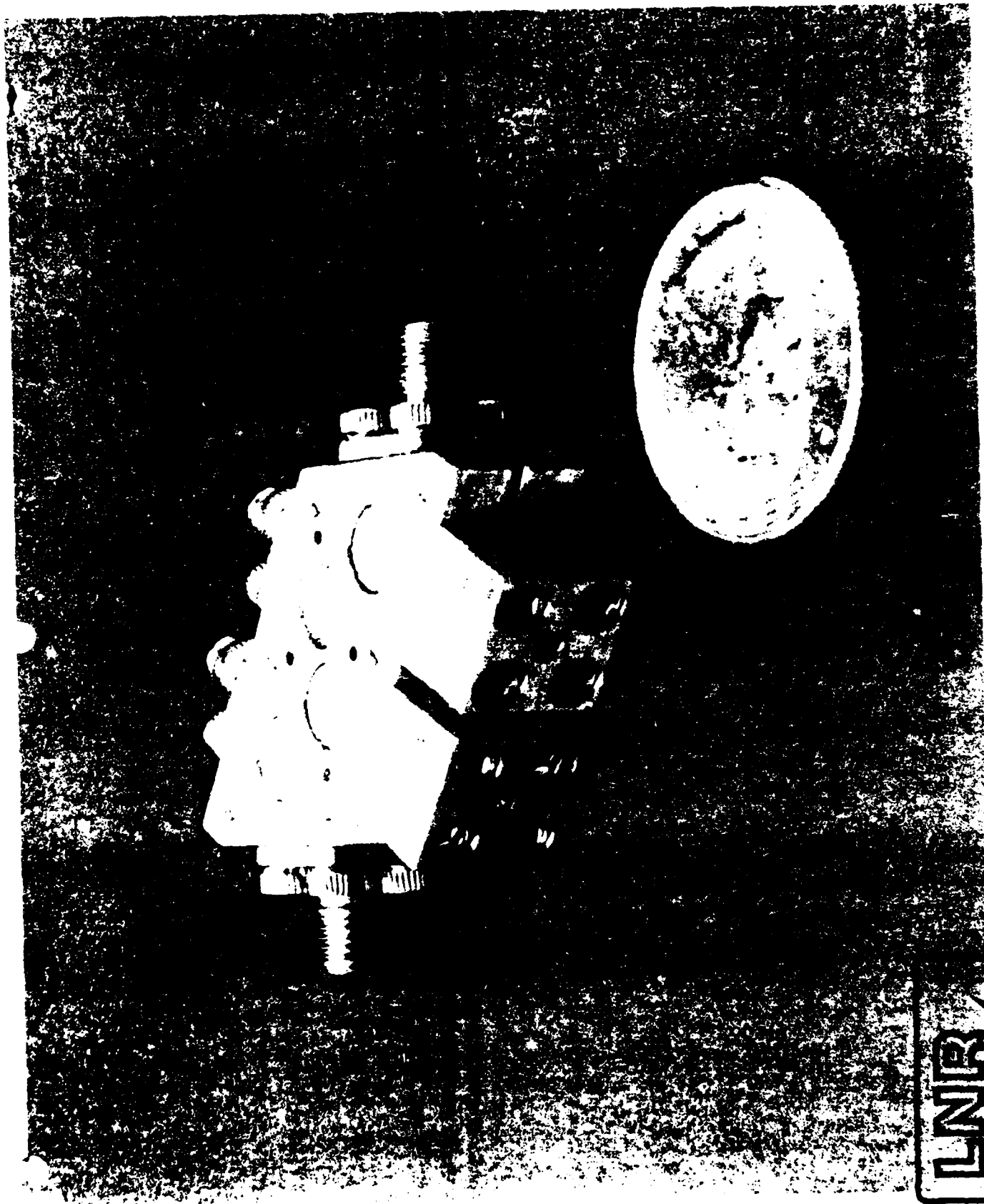
K-BAND 6-PORT STRIPLINE CIRCULATOR



TYPICAL EXTERNAL PORT ISOLATION OF BREADBOARD K-BAND  
6-PORT CIRCULATOR

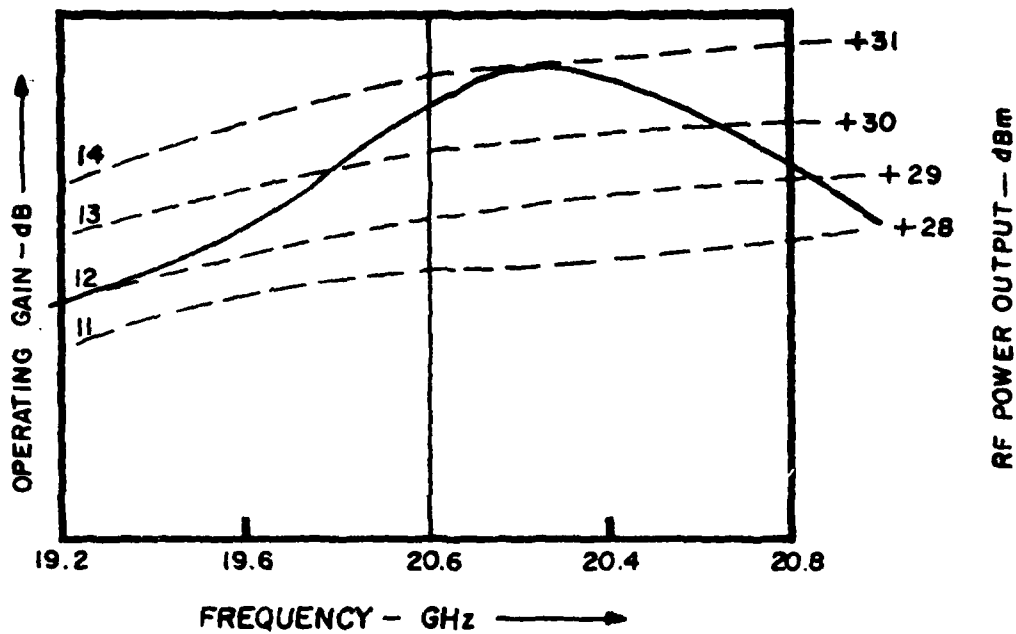


TYPICAL INTERJUNCTION ISOLATION OF BREADBOARD K-BAND  
6-PORT CIRCULATOR



INTEGRATED TWO-STAGE K-BAND IMPACT AMPLIFIER

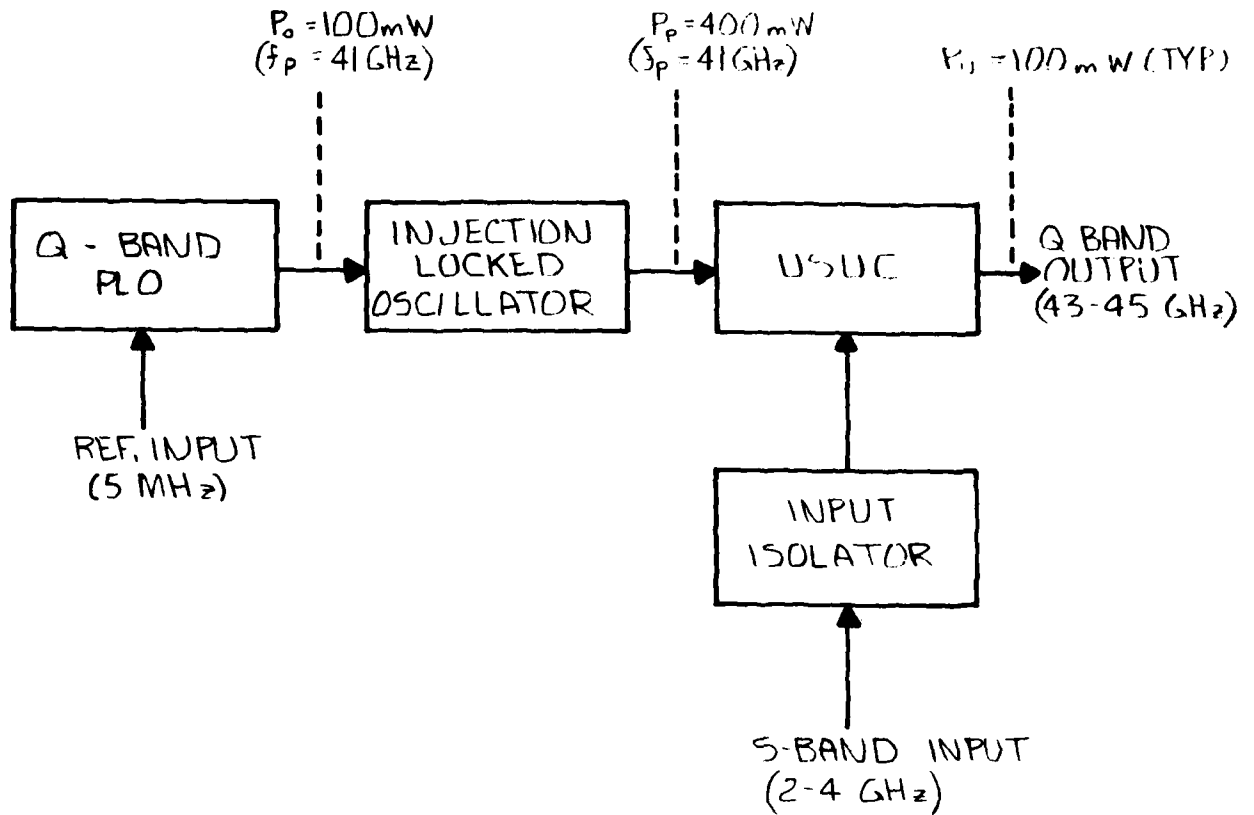




INPUT DRIVE LEVEL : + 17 dBm  
 OPERATING GAIN COMPRESSION RATIO : 0.2 dB/dB  
 IMPATT DEVICE POWER ADDED EFFICIENCY : 18 % (MAX)  
 DC POWER / STAGE : 6 W  
 (◆ COMM. AVAIL. )

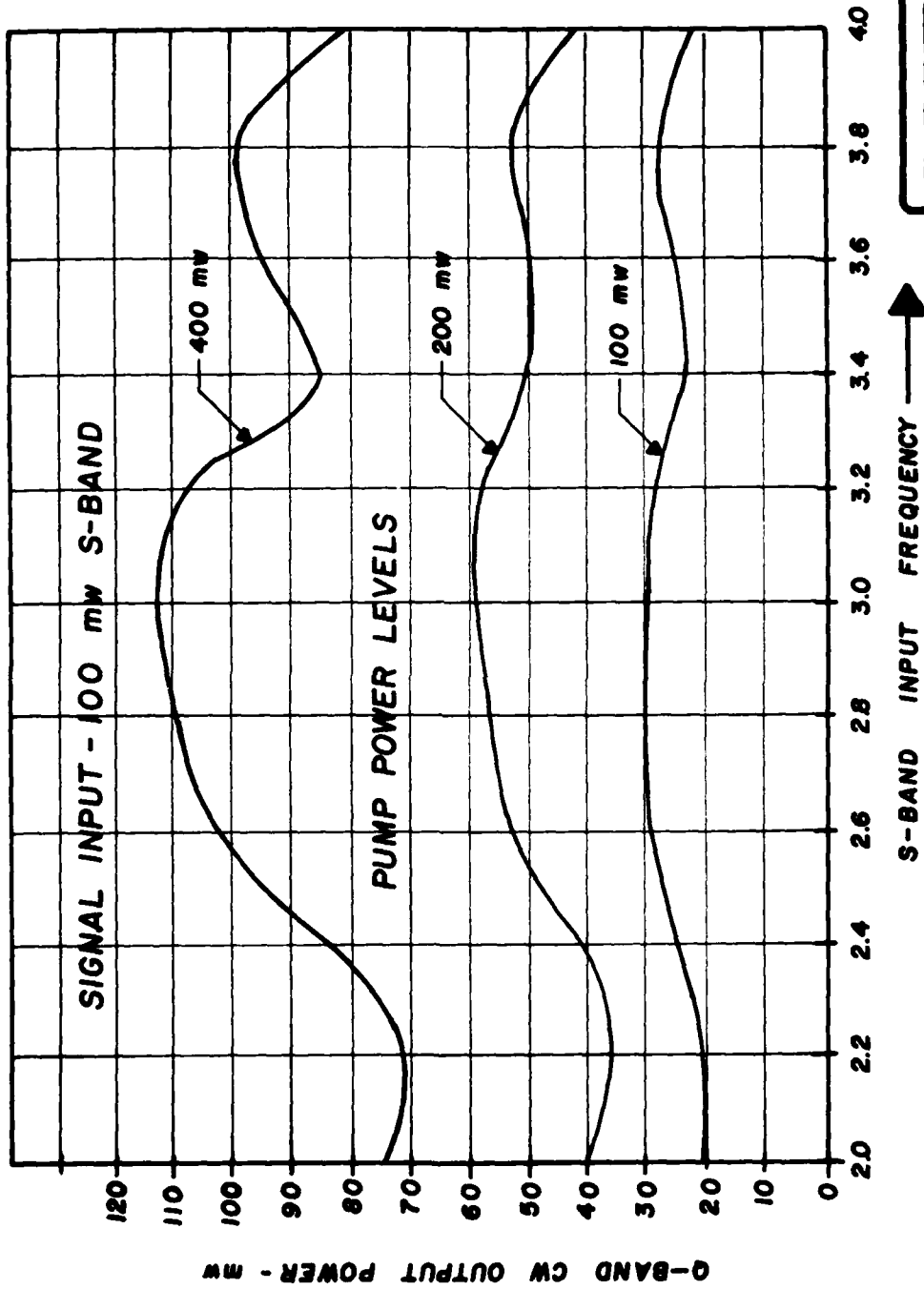
**MEASURED PERFORMANCE  
 OF  
 TWO-STAGE IMPATT PREAMPLIFIER**





FUNCTIONAL BLOCK DIAGRAM OF S/Q BAND POWER UPCONVERTER





SIGNAL INPUT - 100 mw S-BAND

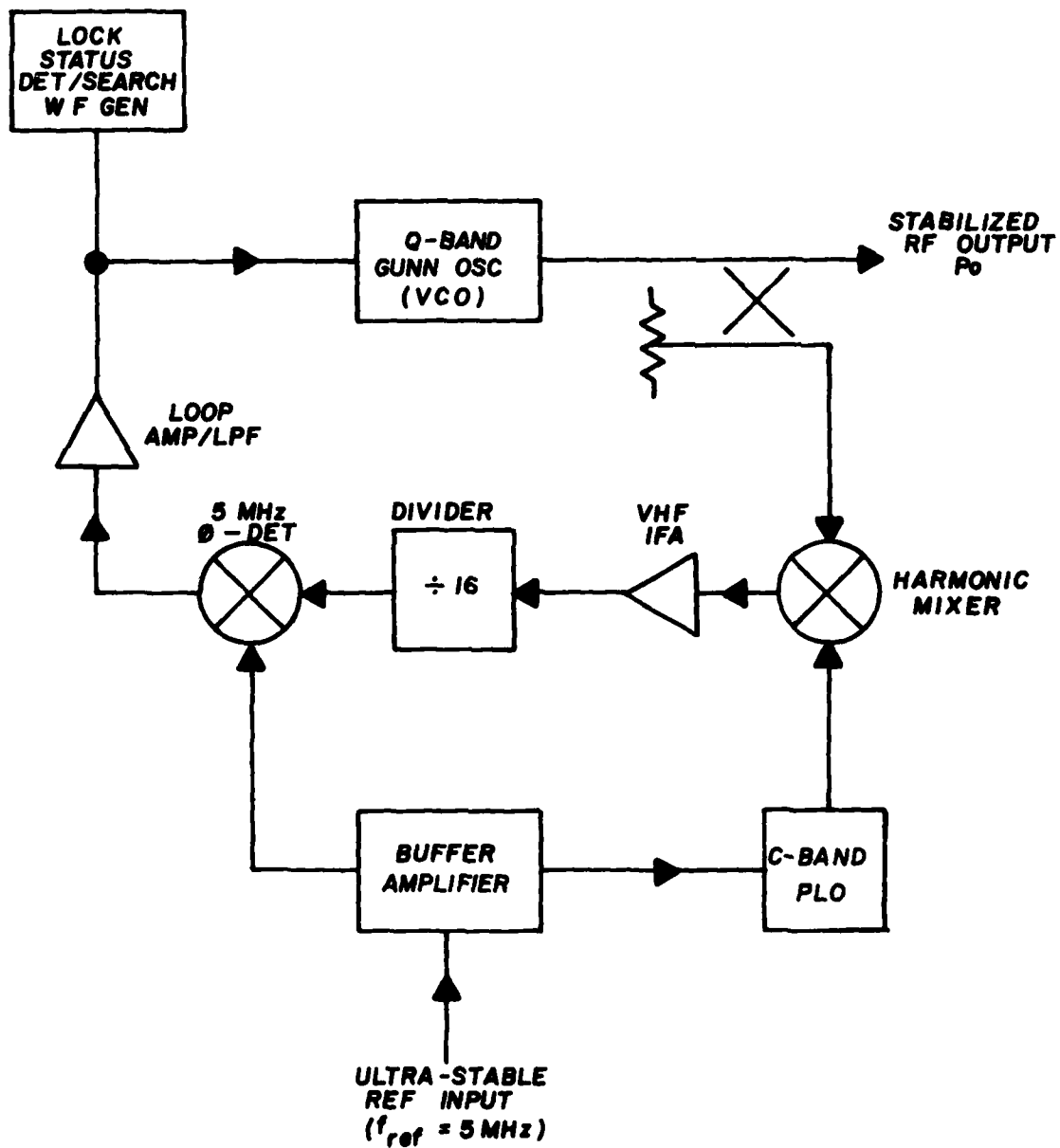
PUMP POWER LEVELS

Q-BAND CW OUTPUT POWER - mW

S-BAND INPUT FREQUENCY

MEASURED POWER OUTPUT - FREQUENCY RESPONSE OF S/Q-BAND USUC





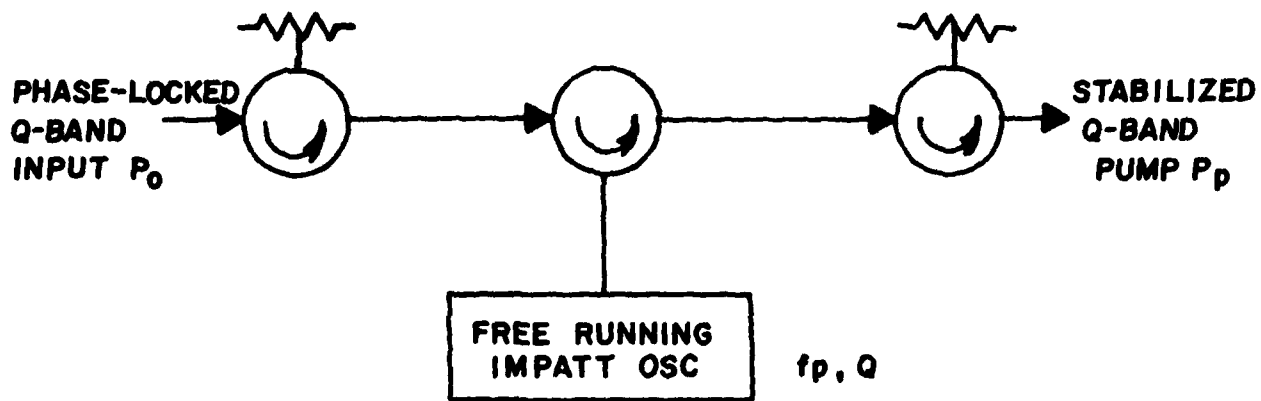
FUNCTIONAL BLOCK DIAGRAM OF THE Q-BAND PHASE LOCKED SOURCE



MEASURED POWER UPCONVERTER CHARACTERISTICS

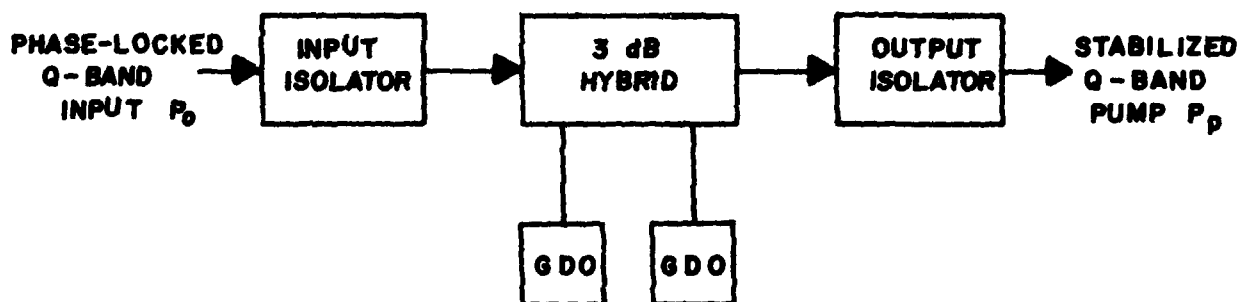
• Input frequency range	2-4 GHz
• Pump frequency	41 GHz
• Output frequency range	43-45 GHz
• Upper sideband output power	95mW (avg.)
• Passband output ripple	2 dB max. (P-P)
• Lower sideband rejection	> 40 dB
• S-band input power	100mW
• Q-band pump power	400mW
• S-band input VSWR	1.3:1 (max)
• Q-band output VSWR	1.5:1 (max)
• Q-band PLO output power	105mW
* • Projected ILO output power	450mW





$$B_{\text{LOCK}} = \frac{2f_p}{Q} \sqrt{\frac{P_0}{P_p}} > \Delta f_{o p-p} \quad (\text{DRIFT})$$

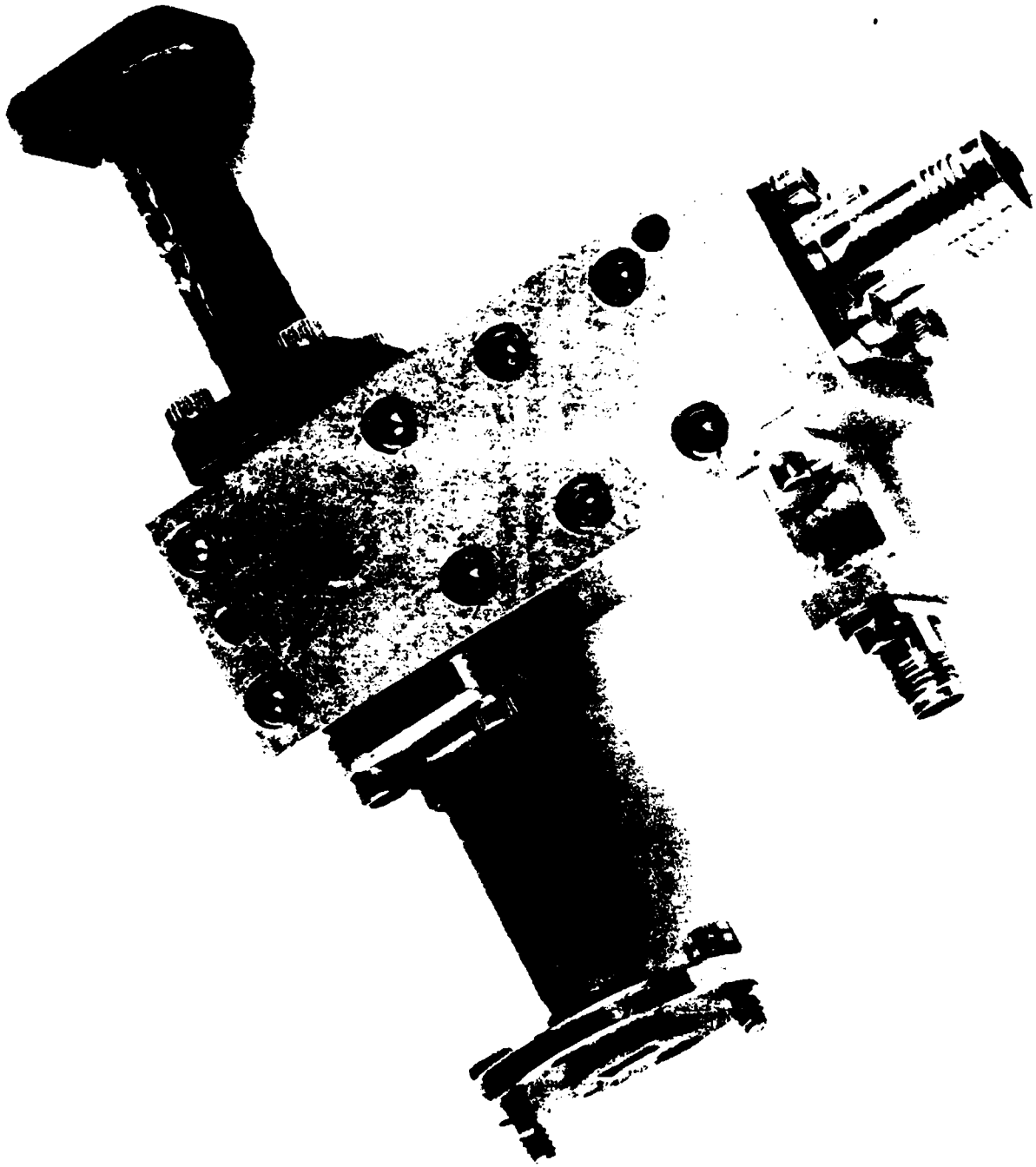
a) CIRCULATOR COUPLED IMPATT OSCILLATOR



b) HYBRID COUPLED GUNN DIODE OSCILLATORS

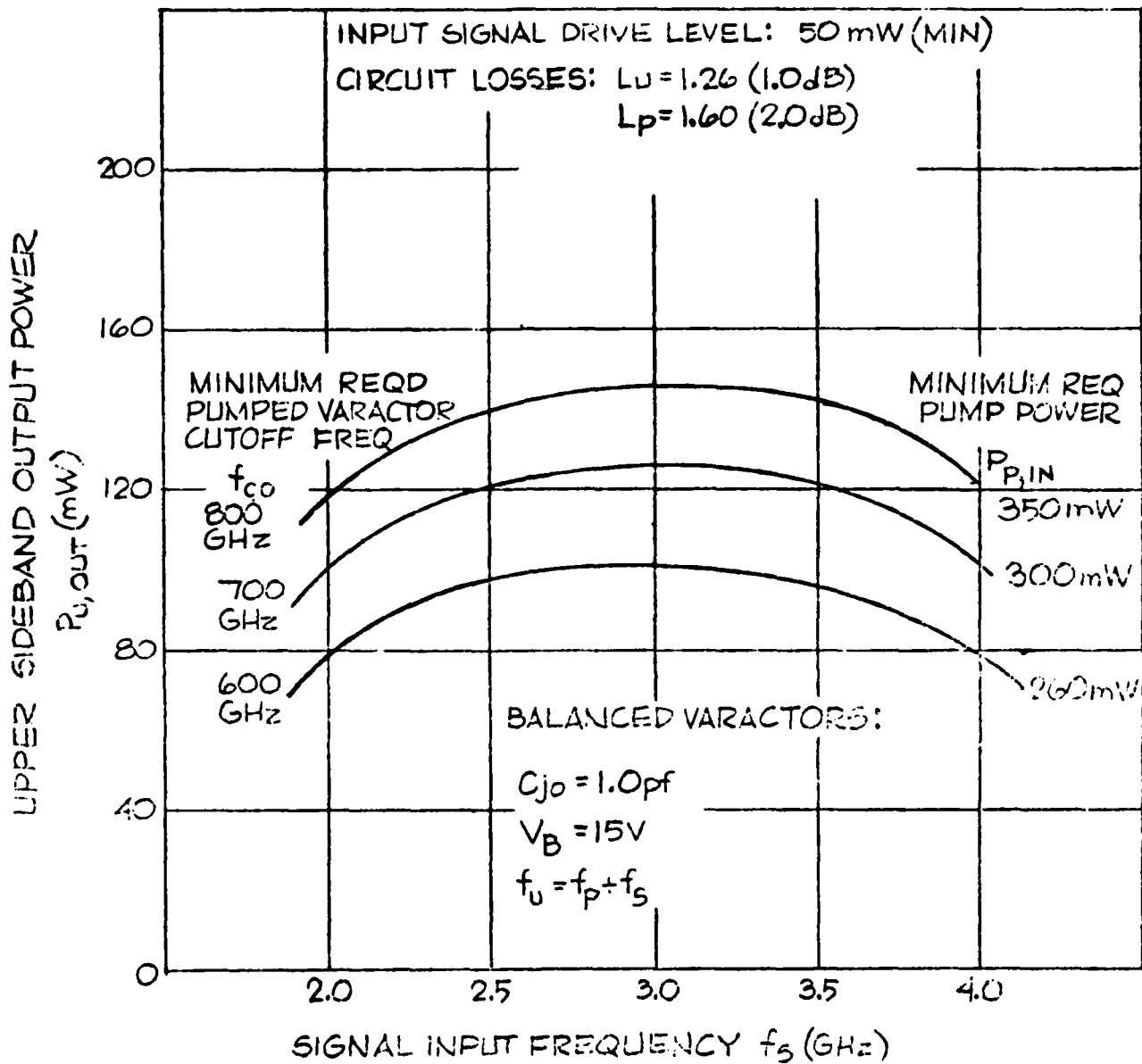
ALTERNATIVE INJECTION LOCKED OSCILLATOR CONFIGURATIONS





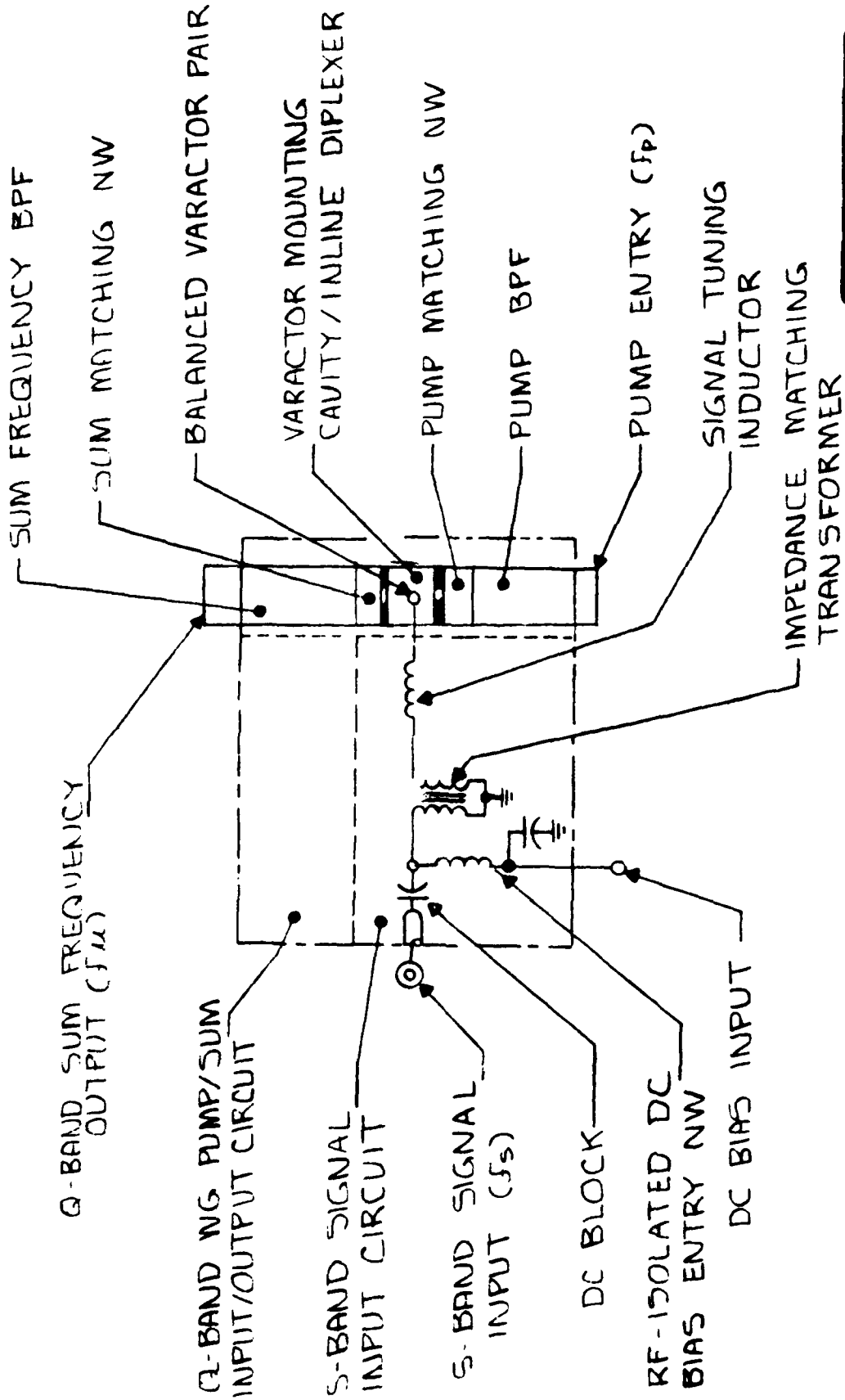
PHOTOGRAPH OF S/Q BAND USUC, INCLUDING IN-LINE PUMP/SUM DIPIEXER





THEORETICAL S - TO - Q - BAND HIGH POWER  
 USUC OUTPUT POWER-FREQUENCY RESPONSE  
 CURVES





86

SCHEMATIC LAYOUT OF S/Q-BAND USUC



PERFORMANCE GOALS OF HIGH POWER S/Q-BAND UPCONVERTER

- Input frequency range 2-4 GHz
- Pump frequency 41 GHz
- Output frequency range (USB) 43-45 GHz
- Upper sideband output power 100mW (Nom.)
- Passband output ripple  $\pm 1.5$  dB (Max.)
- Lower sideband rejection 40 dB (Min.)
- S-band input power 100mW (Max.)
- Q-band pump self-contained phase @ 41 GHz
- Q-band pump power 300mW (Nom.)
- Pump source phase locked loop (PLL) bandwidth 20 KHz (Nom.)
- Reference input frequency 5 MHz
- Pump source FM noise within PLL BW of carrier (fm 20 KHz)  $8.2 \times 10^3 \frac{\Delta f_{ref.}}{\sqrt{Mz}}$  (rms Hz/ $\sqrt{Mz}$ )

HIGH POWER S/Q BAND SATCOM UPLINK TRANSMITTER UNCONVERTER

LNR Communications

H. C. Okean

PRECEDING PAGE BLACK-OUT FILM

HIGH POWER S/Q BAND SATCOM UPLINK

TRANSMITTER UPCONVERTER

BY

H. DeGruyl, H.C. Okean and L.J. Steffek

Presented At

EHF SATCOM TECHNOLOGY WORKSHOP

San Diego, California  
August, 1981

HIGH POWER S/Q BAND SATCOM UPLINK

TRANSMITTER UPCONVERTER\*

by

H. deGruyl, H.C. Okean and L.J. Steffek  
LNR Communications, Inc.

-----

A 100mW output S-to-Q band varactor upper sideband up-converter (USUC), including associated phase locked solid state Q-band pump source, is being developed for use in the 44 GHz uplink transmitter sections of the 44/20 GHz Navy SATCOM ground terminals. Utilizing a balanced pair of in-house GaAs Schottky varactors embedded in a composite waveguide/TEM structure, said USUC translates a 2 GHz wide digitally modulated signal spectrum from the 2-4 GHz input to the 43-45 GHz upper sideband output bands. At 400 mW pump power at 41 GHz and 50 mW signal input level, the upper sideband output power ranges between 60 and 110 mW over 43-45 GHz, with better than 40 dB lower sideband rejection.

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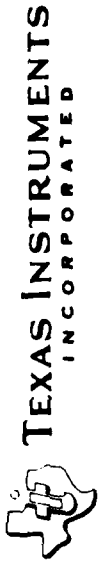
\*This effort was sponsored by the Naval Ocean Systems Center under Contract No. N00123-79-C-1529.

**DEVELOPMENT STATUS FOR A 20 GHz FET  
SPACECRAFT TRANSMITTER**

**Texas Instruments**

**V. Sokolov**

**PRECEDING PAGE BLANK-NOT FILMED**



DEVELOPMENT STATUS FOR A 20 GHz FET SPACECRAFT TRANSMITTER\*

BY

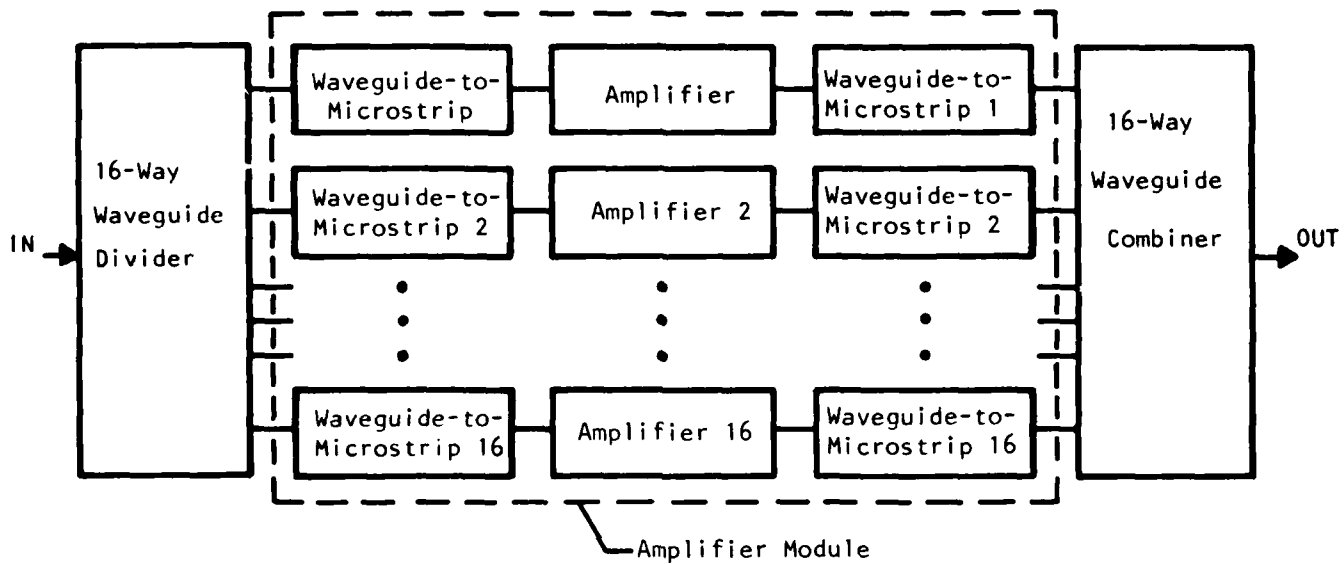
V. SOKOLOV, R.C. BENNETT, P. SAUNIER,  
R.P. LINDSLEY, C.H. MOORE, AND R.E. LEHMANN

TEXAS INSTRUMENTS INCORPORATED  
CENTRAL RESEARCH LABORATORIES  
P.O. Box 225936  
MAIL STATION 134  
DALLAS, TEXAS 75265

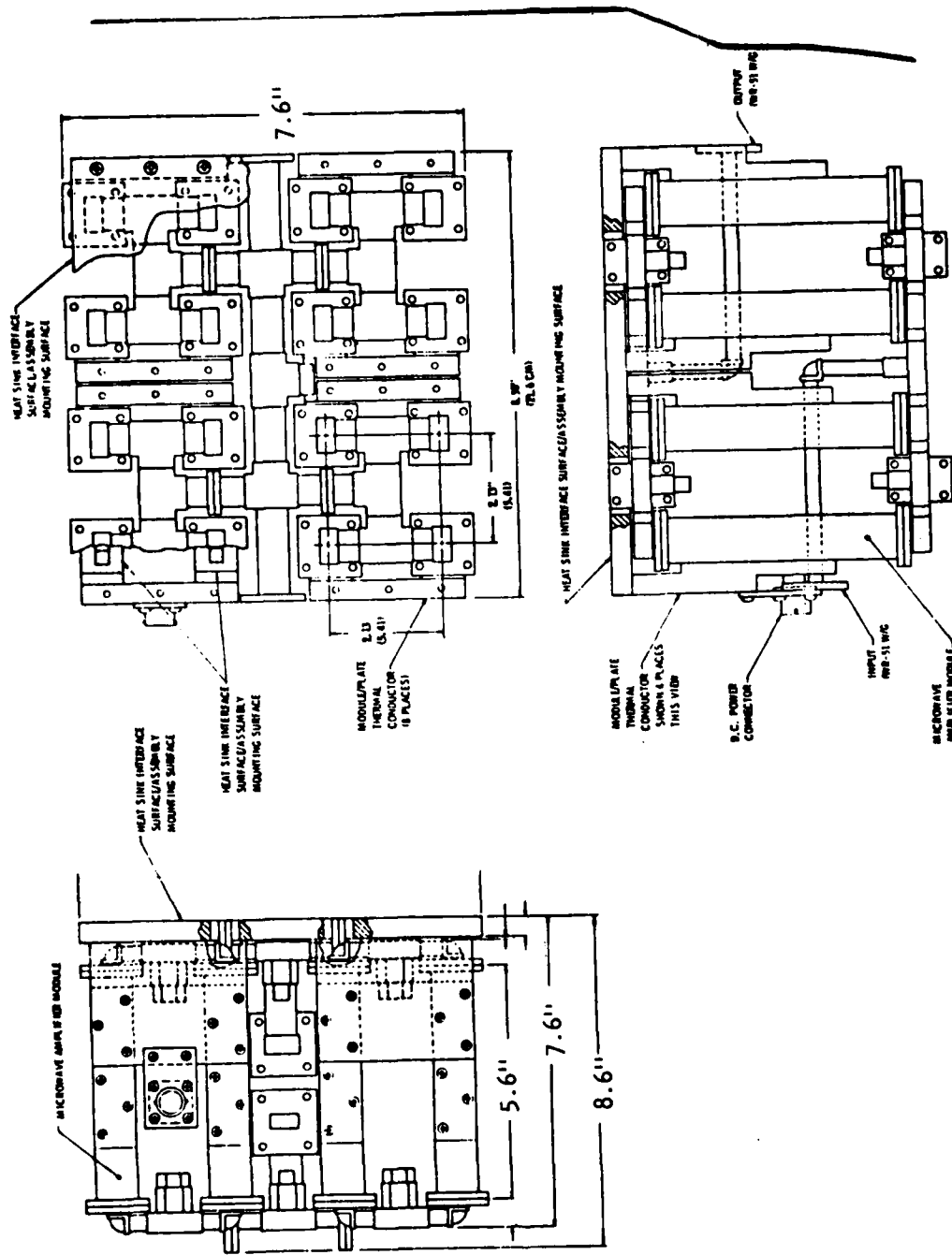
\* THIS WORK IS SUPPORTED BY NASA (LERC) UNDER CONTRACT No. NAS3-22504

BASIC PERFORMANCE SPECIFICATIONS  
(GOALS)  
INTEGRATED POC MODEL POWER AMPLIFIER

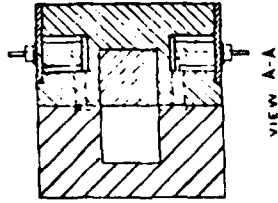
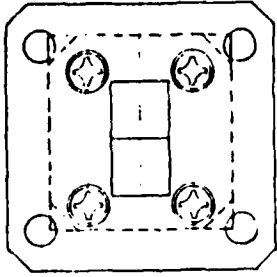
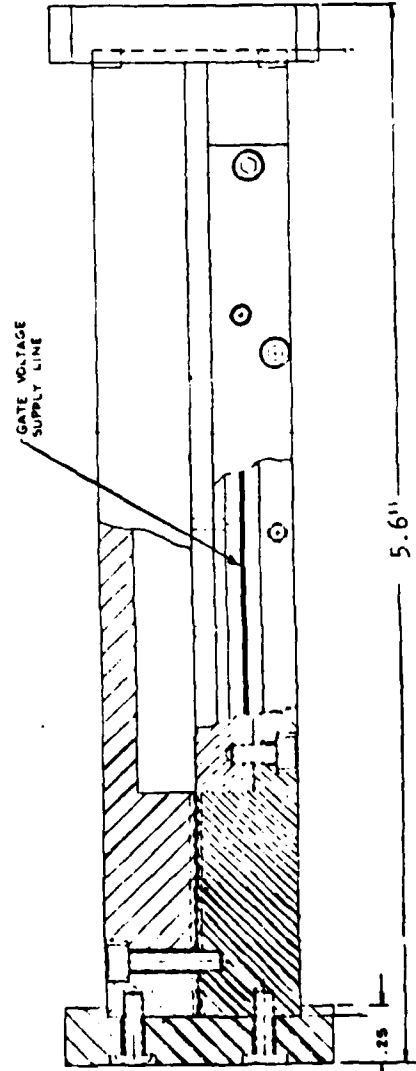
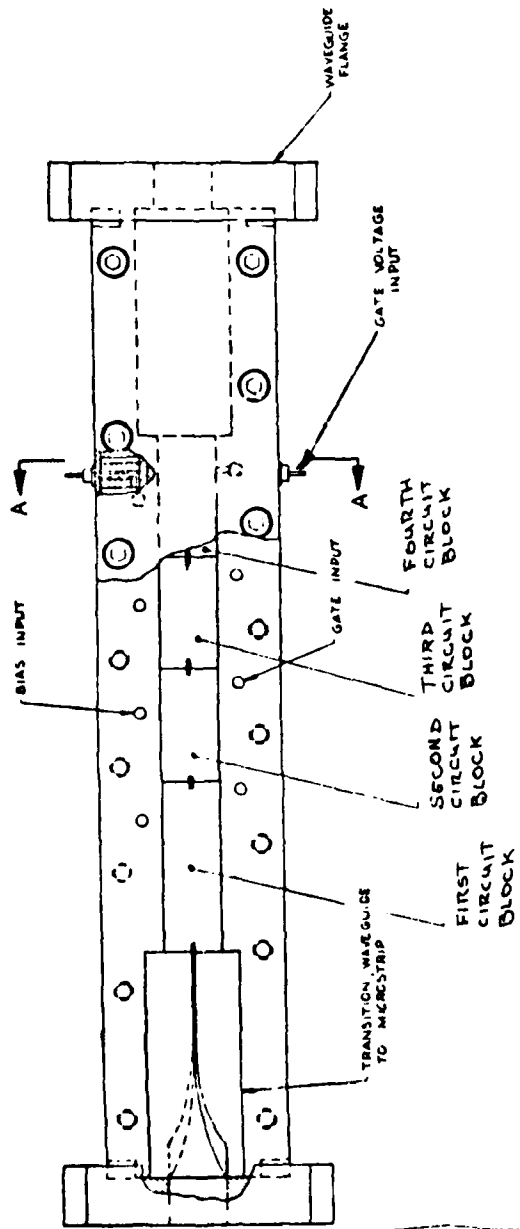
- CENTER FREQUENCY: 19 GHz ( $F_0$ )
- RF GAIN AT  $F_0$ : 30 dB
- OUTPUT POWER AT  $F_0$ : 7.5 W ( $P_0$ )
- 1 DB BANDWIDTH: 17.7-20.2 GHz
- EFFICIENCY AT  $P_0$ : 10%
- THIRD ORDER INTERMODULATION PRODUCTS: AT LEAST 20 DBC AT  $P_0$
- RF CONNECTORS: WR-51 WAVEGUIDE
- OPERATION OF POC MODEL OVER 0°-75°C BASEPLATE TEMPERATURE RANGE



Block Diagram of General Design Approach



20 GHz Amplifier Assembly Single Surface for Mounting and Heat Transfer



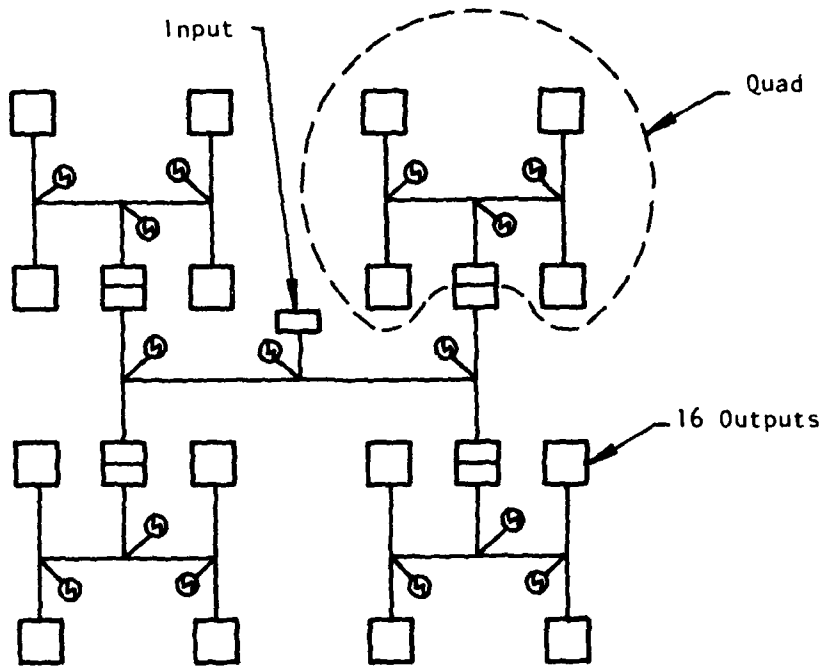
Amplifier Module Assembly

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DEVELOPMENT STATUS FOR A 20 GHZ  
FET SPACECRAFT TRANSMITTER

OUTLINE

- AMPLIFIER PERFORMANCE GOALS
- AMPLIFIER BLOCK DIAGRAM
- 20 GHZ FET DEVICES
- WAVEGUIDE DIVIDER/COMBINER DEVELOPMENT AND AMPLIFIER ASSEMBLY DRAWINGS
- AMPLIFIER MODULE DEVELOPMENT
- STATUS AND SUMMARY

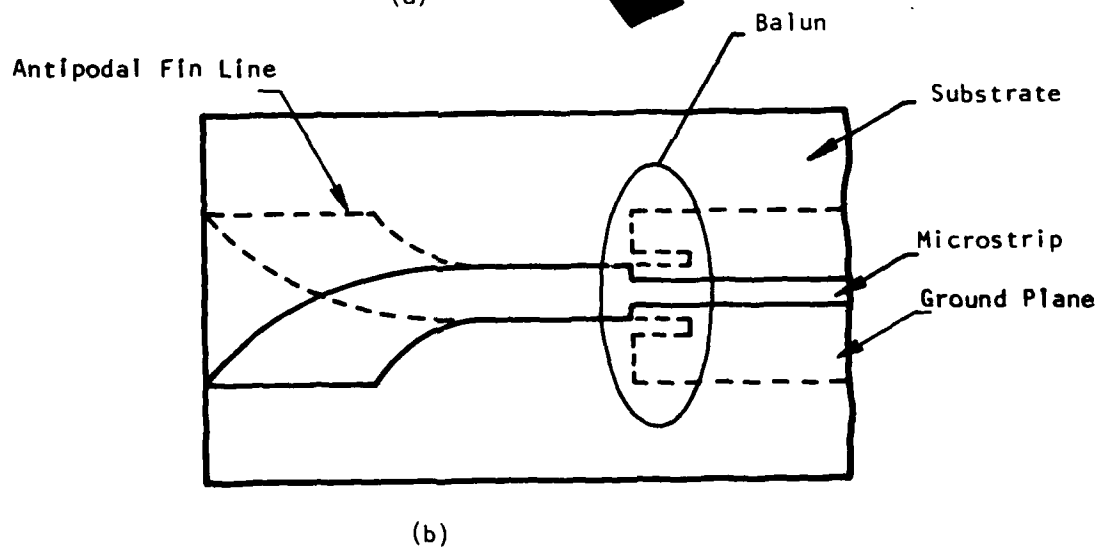
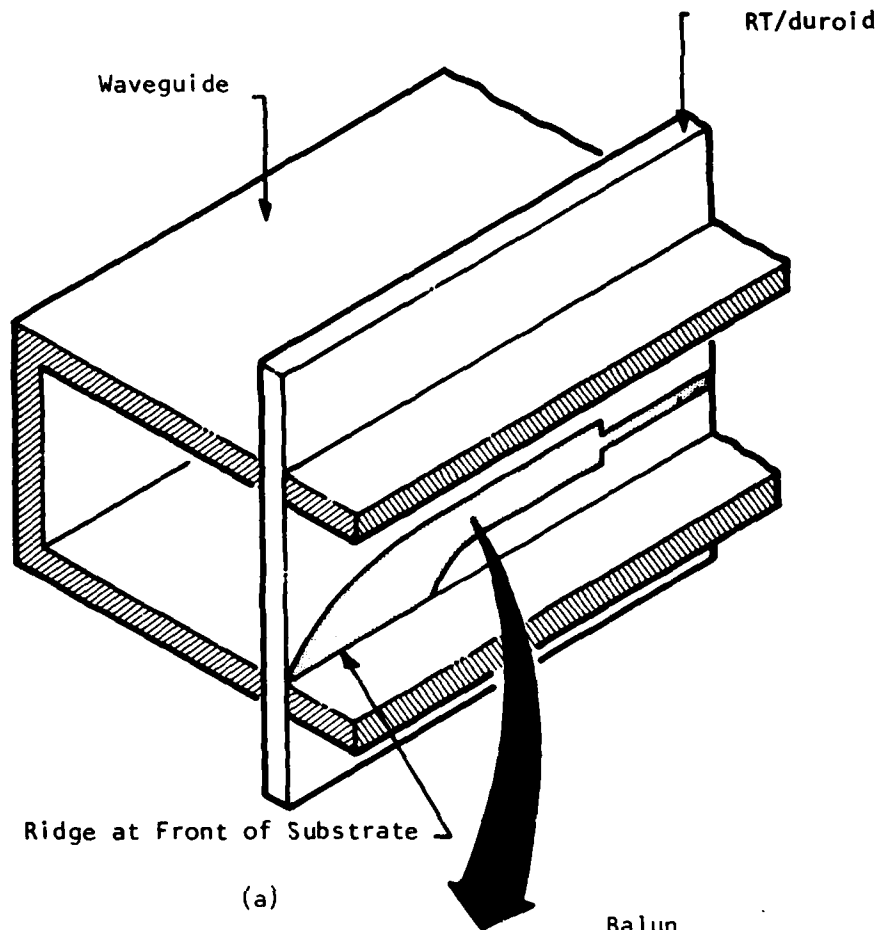


□ WR-51 Flange and E-Bend

▭ WR-51 Flange

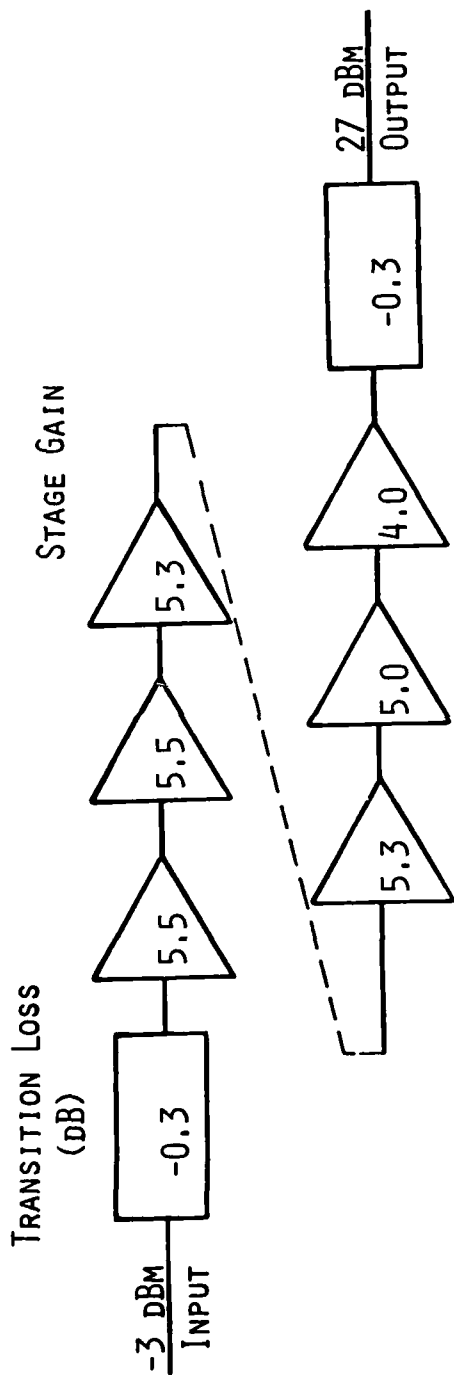
⊥ WR-51 Magic Tee with Loaded Fourth Port

Block Diagram of Power Divider/Combiner



A Low-Loss Transition from Waveguide to Microstrip  
 (a) Outline of the substrate inserted in the waveguide. (b) Position of the planar circuit in the waveguide.

MODULE AMPLIFIER BLOCK DIAGRAM  
(BREADBOARD VERSION)



{ 150 150 150 } FET GATE WIDTH (MICRONS)  
 { 300 1350 2x1350 }

{ 30 30 30 } NOMINAL DRAIN CURRENT (mA)  
 { 60 250 500 }

NOMINAL DRAIN VOLTAGE ~7 V

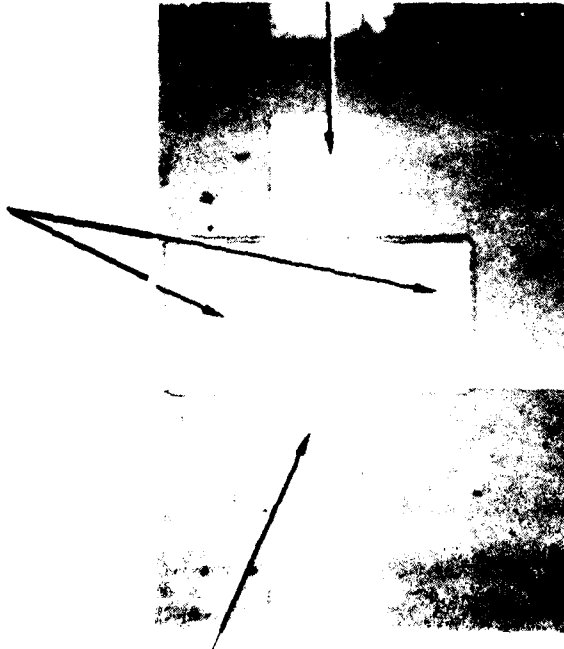
GAAs FET DESIGN AND FABRICATION

● DEVICE TYPE

● PERFORMANCES

● STATUS OF DEVICE SUPPLY

SOURCE

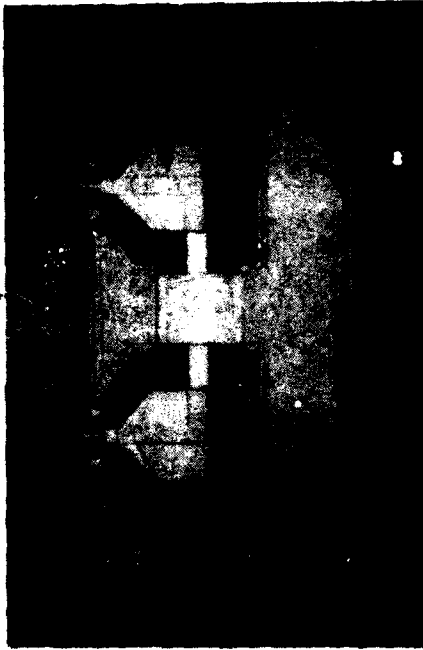


DRAIN

GATE

150 μm Gate Width Device

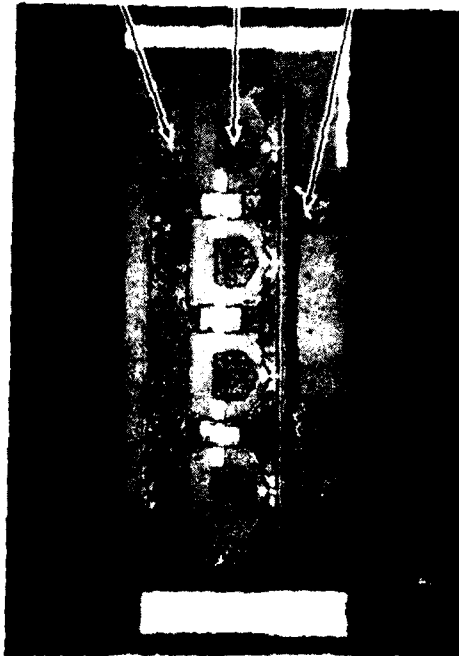
DRAIN



GATE

SOURCE

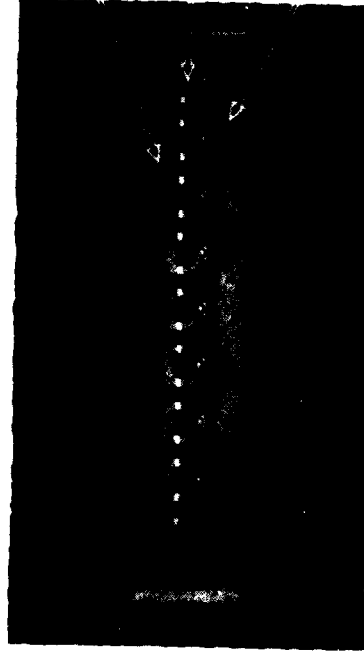
300 μm Gate Width Device



SOURCE  
GATE  
DRAIN

600  $\mu\text{m}$  Gate Width FET

CHIP DIM: 0.76 x 0.3 MM



SOURCE  
GATE  
DRAIN

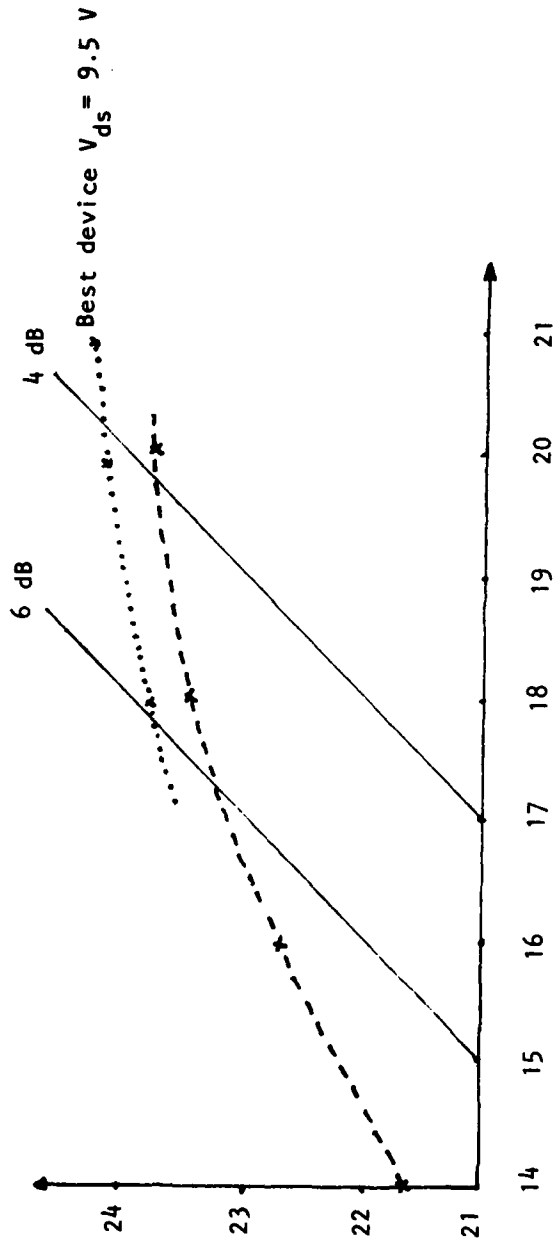
1350  $\mu\text{m}$  Gate Width FET

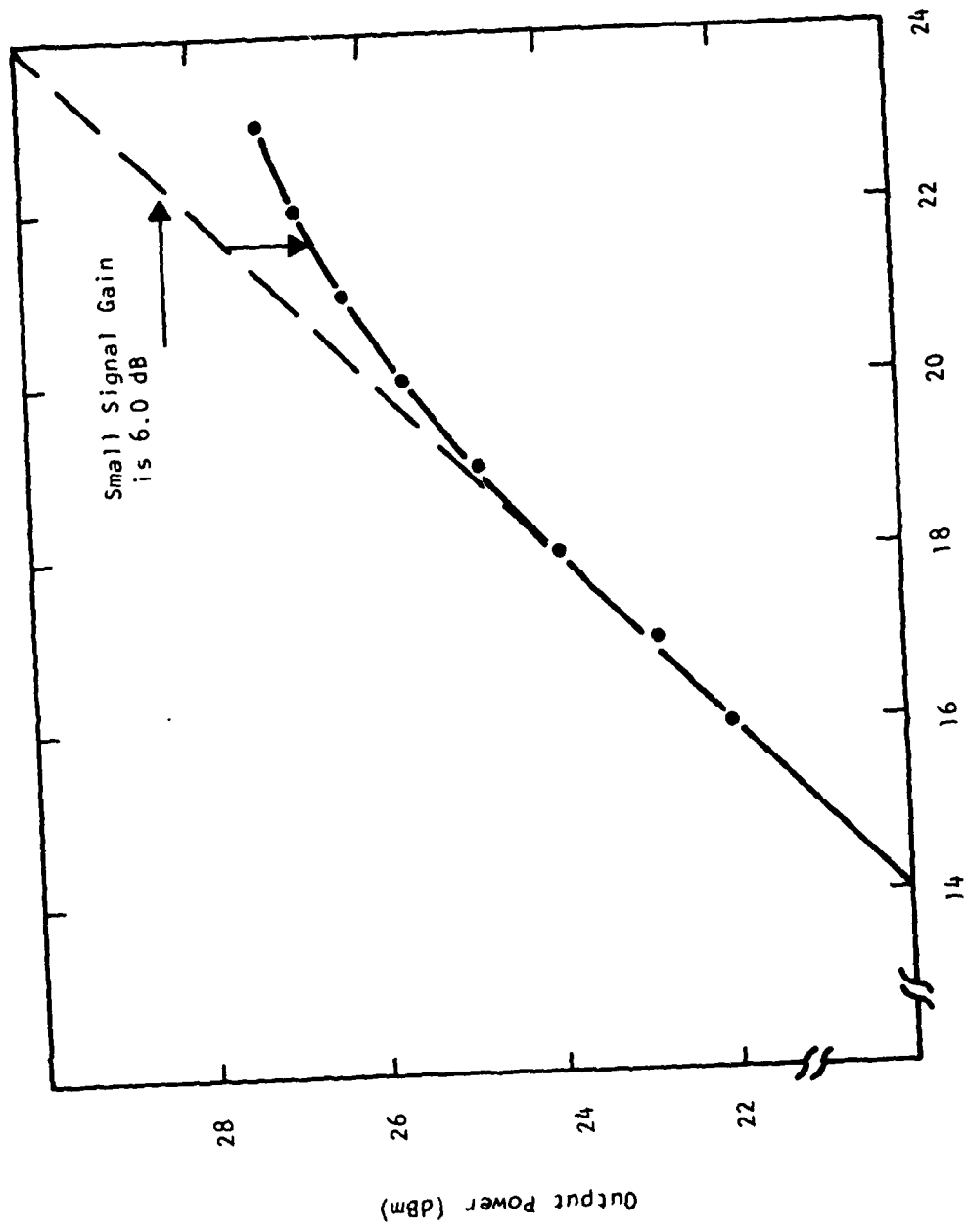
CHIP DIM: 1.5 x 0.3 MM

20 GHz FETS

# PERFORMANCES

- TESTS ARE PERFORMED ON 300  $\mu$ M GATEWIDTH DEVICES AT 15 GHz
- SMALL SIGNAL GAIN WITH 5 V ON THE DRAIN (5 DBM INPUT POWER)  
9 TO 10.5 DB
- INPUT POWER VERSUS OUTPUT POWER WITH 8 V ON THE DRAIN





1 dB Gain Compression  
Point is +26.6 dBm

F = 19.0 GHz  
 $V_D = 8.0$  V  
 $V_G = -1.34$  V  
 $I_D \approx 270$  mA  
 Device: 1350  $\mu$ m (80E13)

Small Signal Gain  
is 6.0 dB

Gain Compression Curve for 1350  $\mu$ m  $\pi$ -Gate FET  
(In 5th Stage Amplifier Circuit)

DEVICES

STATUS

- ABOUT 150 π GATE 1350 μM DEVICES ARE AVAILABLE
- A SUFFICIENT NUMBER OF 150 μM AND 300 μM DEVICES HAVE BEEN FABRICATED FOR IMMEDIATE NEED



**TEXAS INSTRUMENTS**  
INCORPORATED

**16-WAY MANIFOLD REQUIREMENTS**

**PURPOSE: THE POWER DIVIDER/COMBINER WILL PROVIDE UNIFORM AMPLITUDE AND PHASE TO EACH OF 16 AMPLIFIER MODULES, AND WILL RECOMBINE THE OUTPUT POWER OF THE 16 MODULES FOR MAXIMUM EFFICIENCY**

**ELECTRICAL**

**PARAMETER**

**DESIGN GOAL**

**FREQUENCY**  
**VSWR, INPUT**  
**AMPLITUDE VARIATION**  
**PHASE VARIATION**  
**INSERTION LOSS**  
**ISOLATION (BETWEEN OUTPUTS)**

**17.7 TO 20.2 GHZ**  
**1.25:1 MAX**  
**± 0.2 DB**  
**± 5.0 DEGREES**  
**0.8 DB MAX**  
**20 DB MIN**

**MECHANICAL**

**WEIGHT**  
**SIZE**  
**INPUT PORT**  
**OUTPUT PORT**

**1.6 POUNDS MAX**  
**COMPATIBLE WITH OVERALL**  
**PACKAGING CONCEPT**  
**1, WR-51 WAVEGUIDE**  
**16, MODULE COMPATIBLE**  
**WR-51**



**TEXAS INSTRUMENTS**  
INCORPORATED

---

20 GHZ MANIFOLD DESIGN

- A SINGLE MANIFOLD CONSISTS OF A 16-WAY MATCHED WAVEGUIDE POWER DIVIDER.
- LIGHT WEIGHT, DIP-BRAZED ALUMINUM CONSTRUCTION OFFERS LOW LOSS PERFORMANCE.
- FOUR "QUADS" PER MANIFOLD ASSEMBLY OFFERS MODULAR CONSTRUCTION.
- THE MODULAR HEAT SINK DESIGN PROVIDES EASY INTERFACE WITH A COLD PLATE.
- A PAIR OF MANIFOLDS FOR EACH PROOF-OF-CONCEPT TRANSMITTER ALLOWS POWER DIVISION AT THE INPUT AND LOW LOSS POWER COMBINING AT THE OUTPUT.
- STANDARD TEST EQUIPMENT FLANGES (HEWLETT PACKARD STYLE) ARE PROVIDED ON THE INPUT/OUTPUT PORTS.

MECHANICAL DATA

RF INPUT INTERFACE	WR-51 WAVEGUIDE FLANGE (HEWLETT PACKARD VERSION)
RF OUTPUT INTERFACE	WR-51 WAVEGUIDE FLANGE (HEWLETT PACKARD VERSION)
D.C. POWER INPUT	MS TYPE CONNECTOR MS3101R-20-16P
MOUNTING	INTERFACE SURFACE ACTS AS MOUNTING SURFACE AS WELL AS THERMAL CONDUCTOR
WEIGHT	13.8 LBS.
SIZE (CLEARANCE)	8.60 IN. X 8.50 IN. X 7.60 IN.
VOLUME (MAX)	556 IN. <sup>3</sup>

THERMAL DESIGN

REQUIREMENTS (WORST CASE)

- A. MAXIMUM DEVICE TEMPERATURE - 100°C
- B. MAXIMUM TEMPERATURE VARIATION BETWEEN MODULES - 10°C
- C. OPERATE IN A 75°C ENVIRONMENT

ANALYSIS DATA

AMPLIFIER CARRIER TEMPERATURE

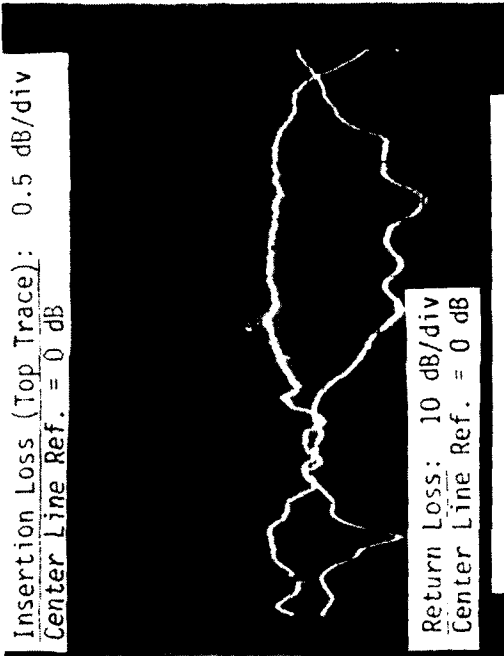
FIRST AMPLIFIER ASSEMBLY (.72W)	90°C
SECOND AMPLIFIER ASSEMBLY (.48W)	90°C
THIRD AMPLIFIER ASSEMBLY (2.0W)	94°C
FOURTH AMPLIFIER ASSEMBLY (4.0W)	99°C

HEAT SINK/MOUNTING PLATE

75°C



Insertion Loss (Top Trace): 0.5 dB/div  
Center Line Ref. = 0 dB



Return Loss: 10 dB/div  
Center Line Ref. = 0 dB

Frequency Range: 17.7-20.2 GHz

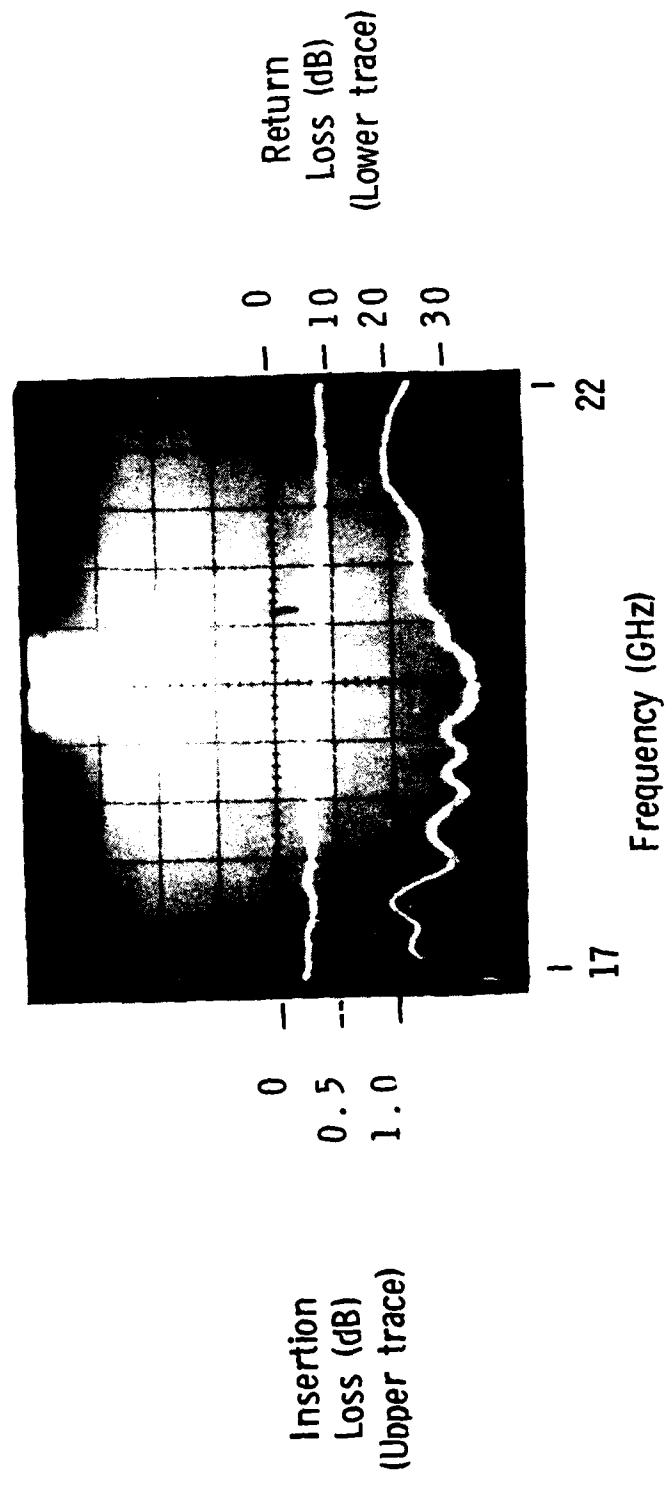
TWO QUAD ASSEMBLIES TERMINATION BLOCK, AND  
FLANGE ADAPTORS

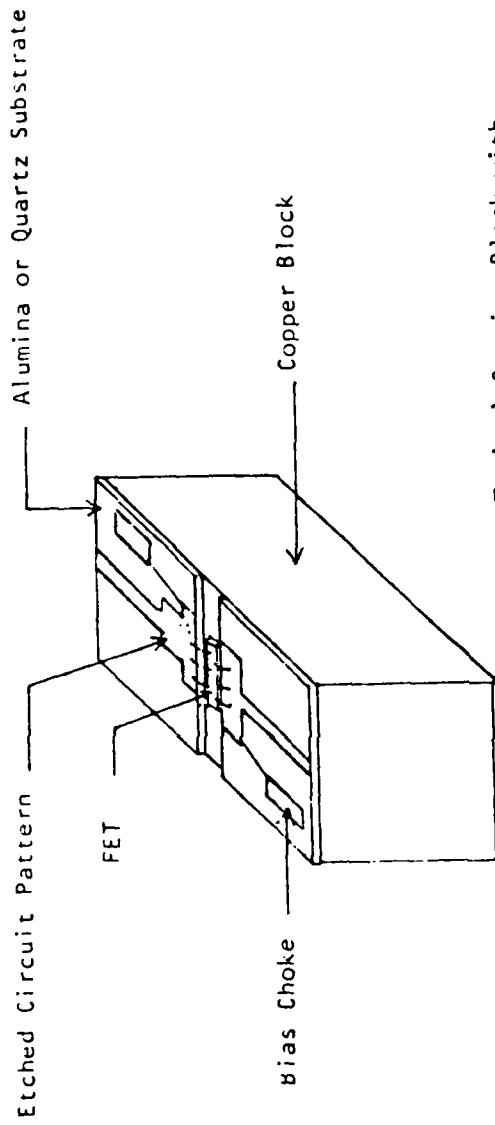
RF PERFORMANCE OF A PAIR OF BACK TO BACK  
QUAD ASSEMBLIES (FIRST ASSEMBLY,  
PRELIMINARY RESULTS ONLY)



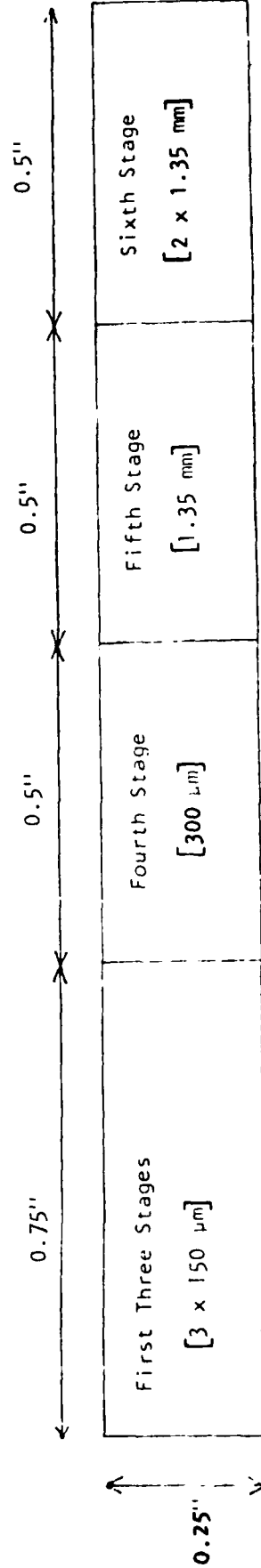
Waveguide-to-Microstrip Transition  
Test Fixture and Test Circuit

FREQUENCY RESPONSE  
OF  
TWO WAVEGUIDE-TO-MICROSTRIP TRANSITIONS  
(BACK-TO-BACK)





Typical Carrier Block with  
Microstrip Impedance Matching  
Circuit



Length of Four Blocks - 2.25"

Transition Length -  $\sim$  1.50" each

Total Module Length -  $\sim$  5.25"

FET Carrier Blocks Used in Breadboard Amplifier