

**1981 ELECTRONICS  
MINISYMPOSIUM  
PROCEEDINGS** TECHNICAL  
LIBRARY

**AS PRESENTED AT THE DOD MANUFACTURING  
TECHNOLOGY ADVISORY GROUP CONFERENCE  
SAN DIEGO, CA., 2, 3 DECEMBER 1981**

**ARRANGED BY THE ELECTRONICS SUBCOMMITTEE  
WORKING GROUP:**

- SESSION I HYBRID CIRCUITS  
II COMPONENTS AND PACKAGING  
III ELECTRONICS CAD/CAM  
IV SEMICONDUCTORS AND INTEGRATED CIRCUITS  
V MICROWAVE DEVICES  
VI ELECTRO-OPTICS**

**ELECTRONICS SUB COMMITTEE  
MANUFACTURING TECHNOLOGY ADVISORY GROUP  
C. E. MC BURNEY, CHAIRMAN**

**ASSEMBLED AND PRINTED AT  
US ARMY INDUSTRIAL BASE ENGINEERING ACTIVITY**

**DECEMBER 1981**

Electronics Subcommittee  
Manufacturing Technology Advisory Group  
Attn: DRXIB-MT  
Rock Island, Illinois 61299

30 December 1981

SUBJECT: MINISYMPOSIUM PROCEEDINGS

TO: ELECTRONICS SUBCOMMITTEE MEMBERS  
ELECTRONICS INDUSTRY REPRESENTATIVES

Proceedings of the Electronics Minisymposium held at San Diego on 2-3 December 1981 are published pursuant to paragraphs VD 3, 4 and 5 of the Manufacturing Technology Advisory Group Charter.

The papers are being published in response to requests from many conference participants. High quality of the papers dictate that they be widely disseminated to aid in technology transfer.

The contribution of the many Industry and Government authors and presenters is recognized and acknowledged.

Sincerely,



CHARLES E. MCBURNEY  
Chairman, Electronics Subcommittee  
Manufacturing Technology Advisory Group





# **MAJOR THRUSTS OF THE HYBRID CIRCUITS WORKING GROUP MTAG**

By DR. DEAN MCKEE,  
NAVAL OCEAN SYSTEMS CENTER



# **HYBRID CIRCUITS WORKING GROUP**

**Is concerned with the development of hybrid related materials and process technologies for the enhancement of productivity in the manufacture of DOD high reliability electronic systems.**

# **CURRENT THRUSTS**

- **Substrate fabrication**
- **Hybrid assembly processing**
- **Hybrid packaging**
- **Hybrid technology enhancement**

# **SUBSTRATE FABRICATION**

- **High density multilayer thick film hybrid microcircuit substrates**
- **Ceramic substrates for hybrid electronics**
- **Computerized thick film printer**

# **HYBRID ASSEMBLY PROCESSING**

- **Production methods for tape automated bonding**
- **Automatic polymer attachment production methods**
- **Bumped tape automatic bonding**
- **Hi rel wirebonding in hybrid circuits**

# **HYBRID PACKAGING**

- **Integrated circuit ceramic chip carrier packages**
- **Hermetic chip carrier packaging**

# **HYBRID TECHNOLOGY ENHANCEMENT**

- **High power thick film hybrids**
- **Manufacturing techniques for large scale hybrid microelectronics**
- **Hybrid computer-aided integration**
- **Hybrids for high power rf applications**
- **Delidding and resealing of hybrid microcircuits**



# **EXPECTED ACCOMPLISHMENTS OF CURRENT THRUSTS**

- **Improved productivity**
- **Improved assembly processes**
- **Packaging flexibility**
- **Improved quality and reliability**
- **Cost reduction**

## **FUTURE THRUSTS**

- **Hybrid components and materials**
- **Packaging applications**
- **Automated processes and procedures**
- **Microwave integrated circuits**
- **Hybrid testing**

# **HYBRID COMPONENTS AND MATERIALS**

- **Non noble metals for ceramic metal substrates and interconnection**
- **Metallic-organic materials**
- **Improved chip capacitors and inductors**
- **High temperature devices**

# **PACKAGING APPLICATIONS**

- **High reliability nonhermetic hybrid packages**
- **Saw packaging techniques**
- **Optical packaging techniques**
- **High speed VLSI packaging techniques**
- **Power hybrid packages**
- **Advanced hermetic repairable packages**

# **AUTOMATED PROCESSES AND PROCEDURES**

- **Hybrid computer-aided integration**
- **Rapid programmable laser trimming**
- **Automatic wire bonder**
- **Optimized automated heavy wire bonding**
- **Optical selection by pattern recognition**

# **MICROWAVE INTEGRATED CIRCUITS**

- **Ion beam milling for MIC's**
- **Automated assembly and fabrication of microstrip bonds**
- **Low cost thick film microwave circuits**
- **Hybrid rf power modules**

## **HYBRID TESTING**

- **Hybrid electronic repair capability**
- **Multipurpose chip test holder**
- **Mechanical testing of large hybrid packages**
- **Qualification procedures for hybrids**

# **RESULTS EXPECTED FROM FUTURE THRUSTS**

**A more producible hybrid for hi rel military applications through the optimization of**

- **Materials**
- **Packages**
- **Devices**
- **Fabrication and assembly**
- **Test and screening**
- **Repair capability**

**For cost effective hi rel hybrid microcircuits**

SESSION I - 2

HICADAM INTRODUCTION

HUGHES

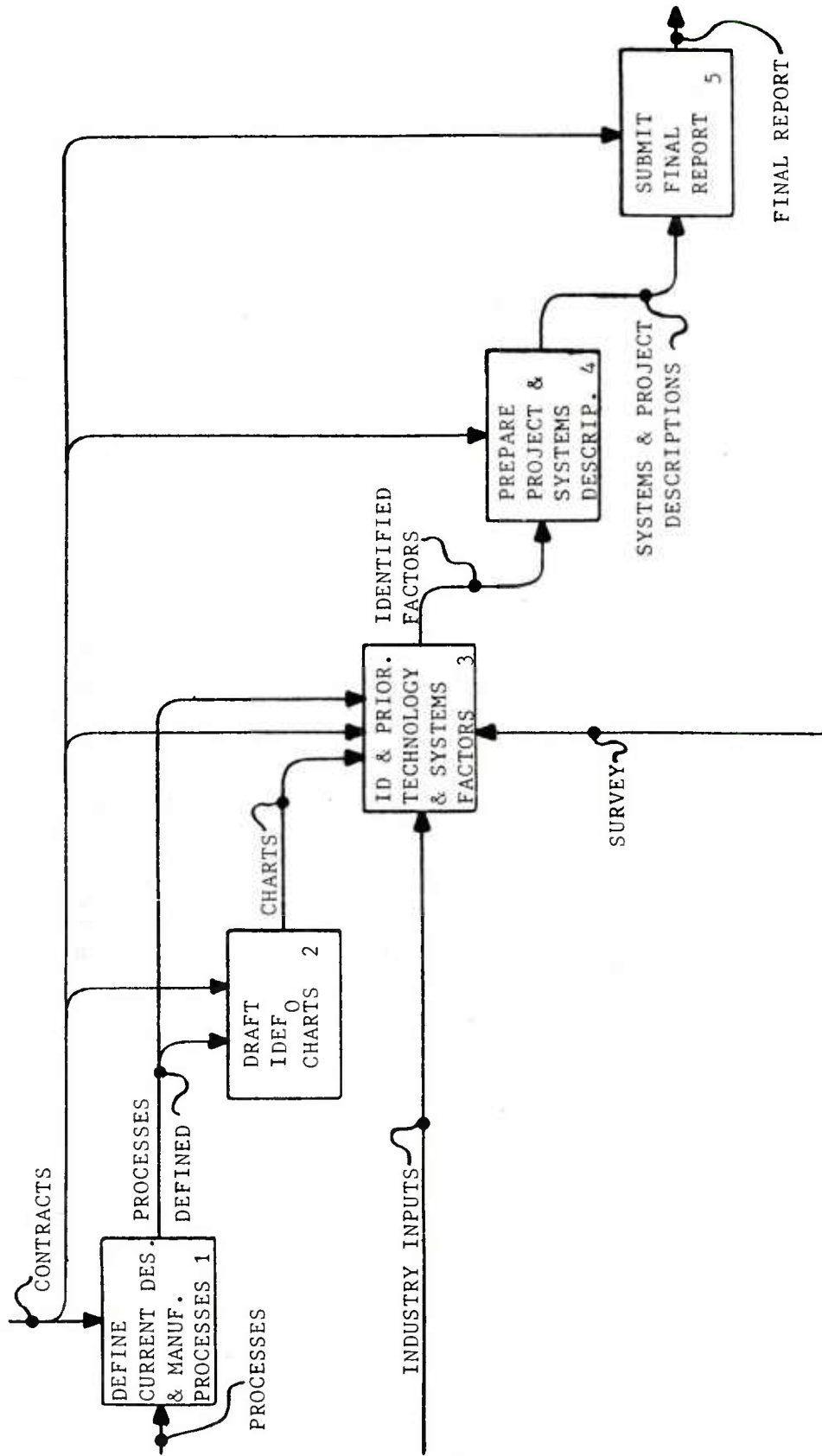
by Mr. Dean A. Keller  
HUGHES AIRCRAFT COMPANY

Hybrid Integrated Computer Aided Design And Manufacturing

PURPOSE: To reduce the manufacturing costs of hybrid microelectronics through the integration of CAD, CAM, and CAT.

PROGRAM MANAGER: MR. GORDON LITTLE

APPROACH MODEL



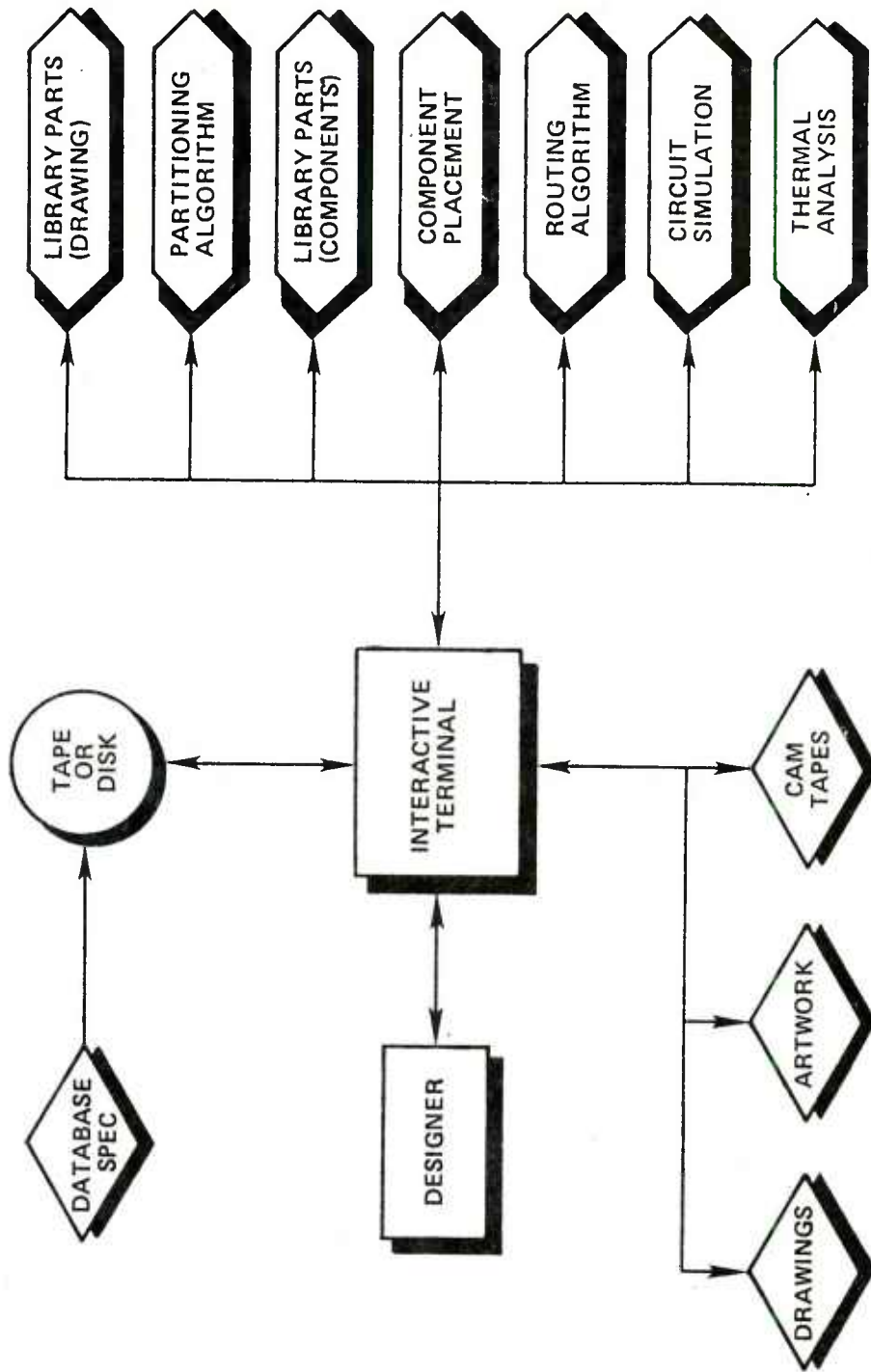
## DESIGN PROCESSES

HUGHES

- Technology Selection
- Circuit Simulation/Analysis
- Component Placement
- Interconnect Routing
- Test Requirements
- Die Topographies
- Releasable Database

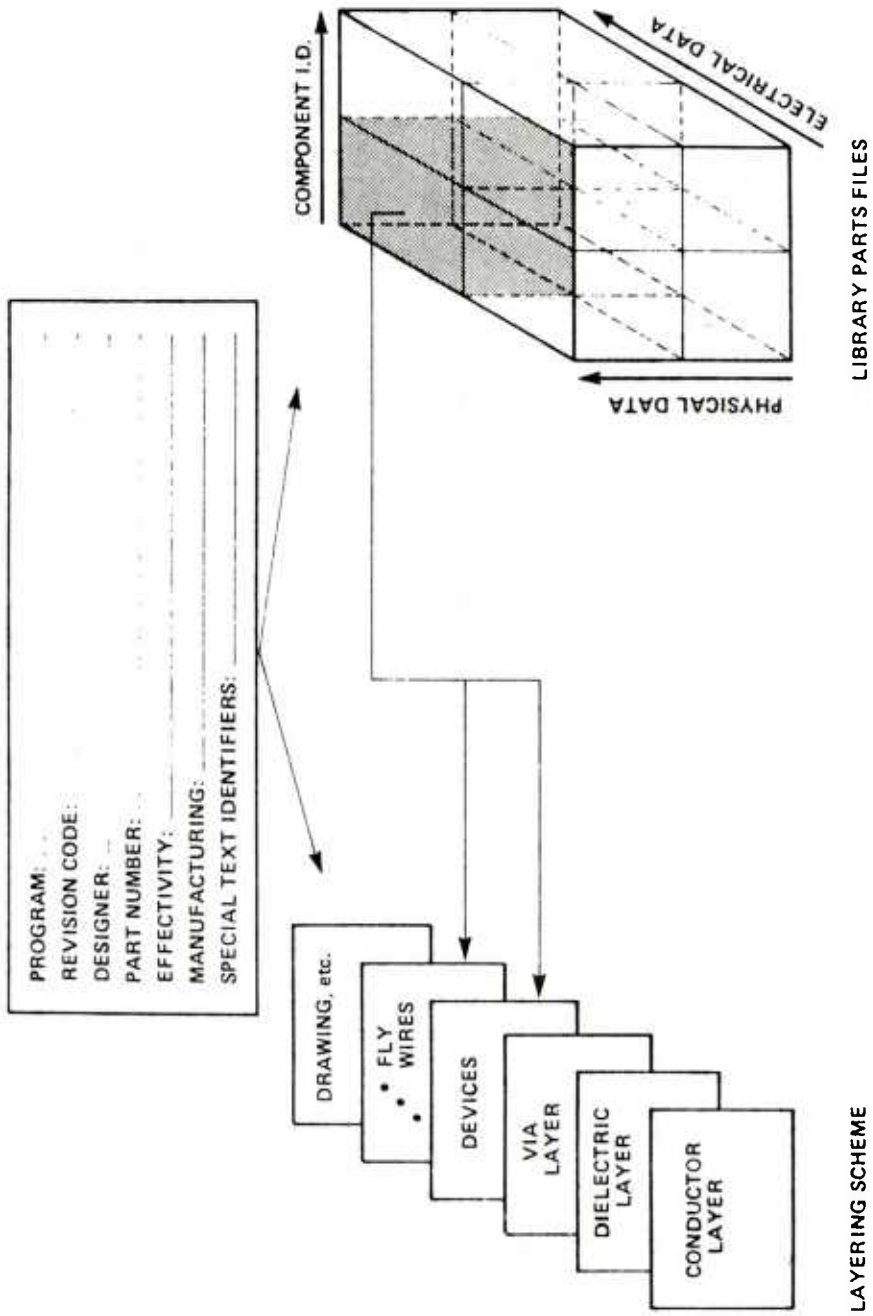
# CAD/CAM SYSTEM ATTRIBUTES

**HUGHES**



# ILLUSTRATIVE DATABASE INTERFACES

HUGHES



## MANUFACTURING PROCESSES

HUGHES

### Substrate Fabrication

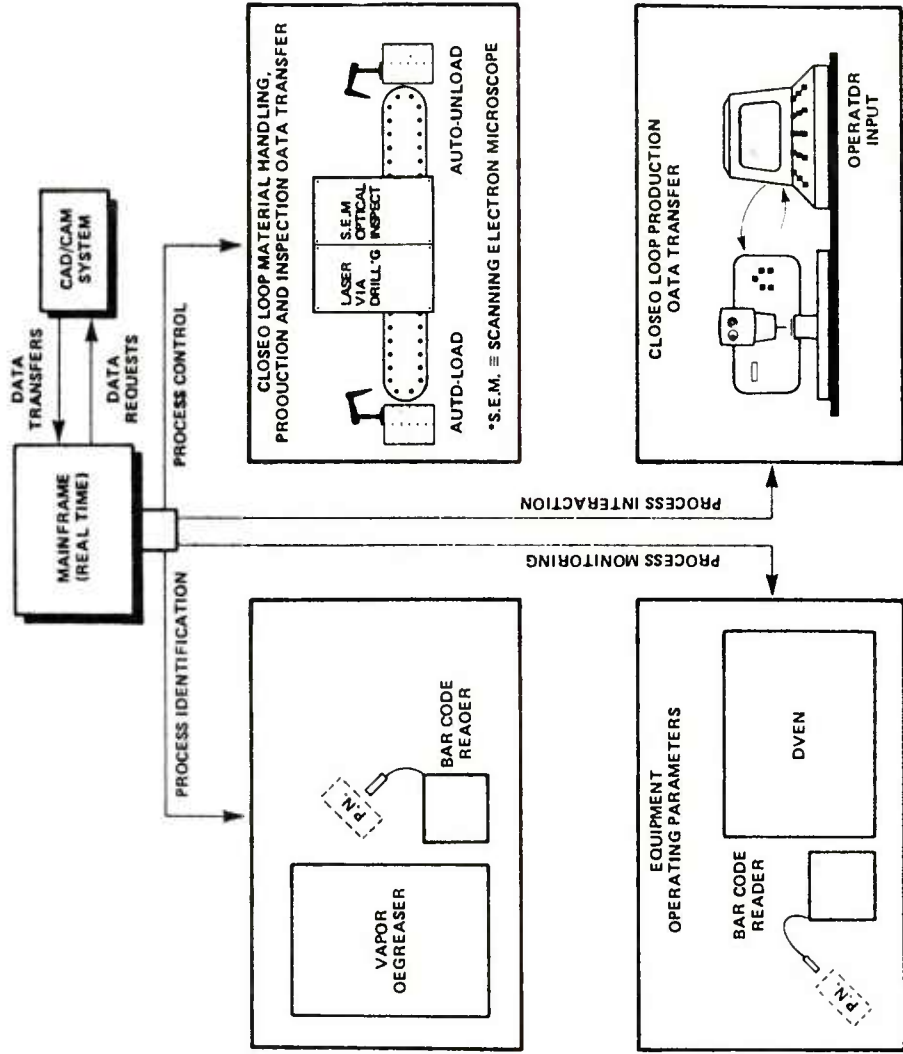
Thin Film  
Thick Film  
Cofired Ceramics  
Other Materials/Technologies  
Adjust Components

### Hybrid Assembly

Chip and Wire Technology  
Tape Automated Bonding  
Chip Carrier Technology  
Hybrid Packaging  
Process Inspection

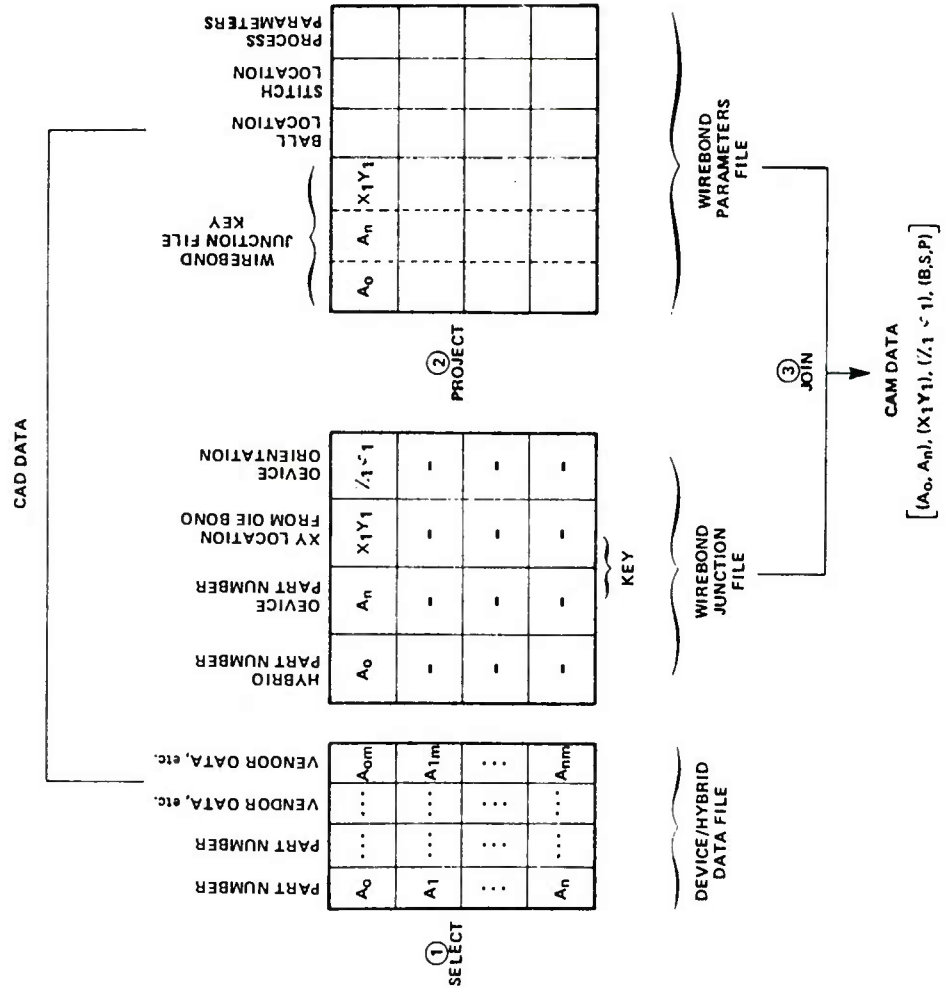
# "CAM ILLUSTRATIONS"

HUGHES

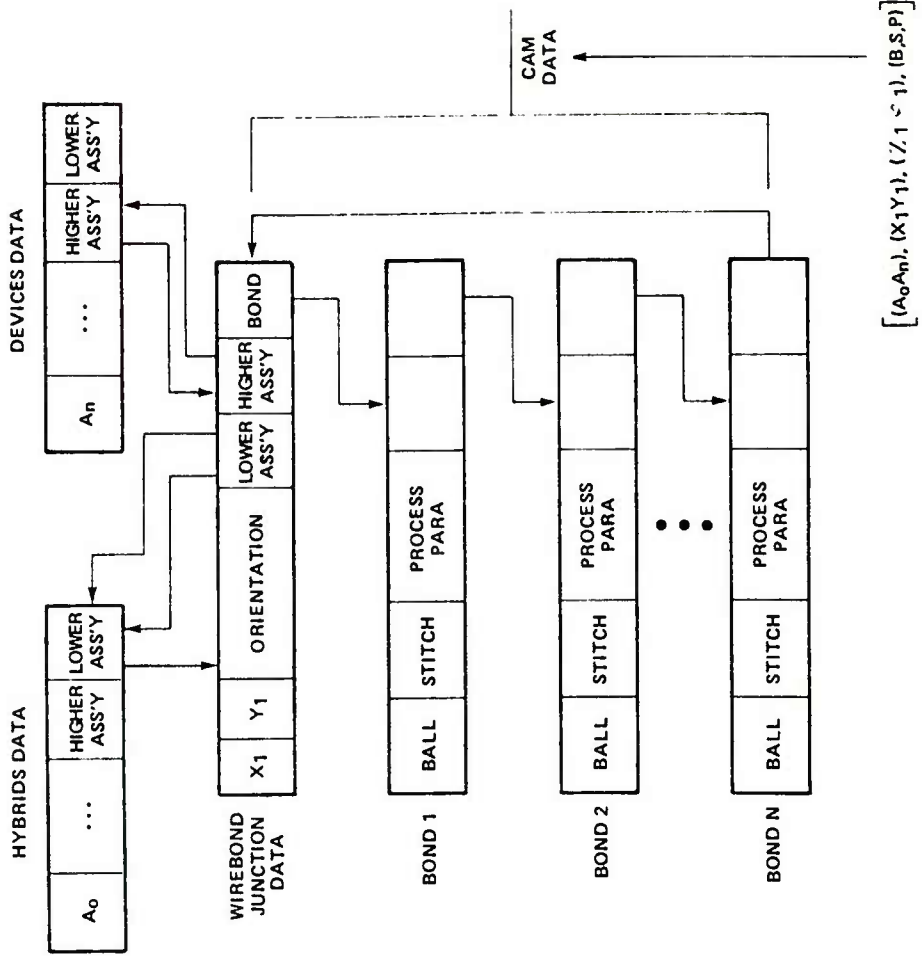


# "RELATIONAL DBMS ILLUSTRATION"

HUGHES



# "CODASYL DBMS ILLUSTRATION"



## SYSTEMS INTERFACES

HUGHES

- Material Requirements Planning
- Procurement Activity
- Production Control
- Process Control
- Quality/Test Information
- Configuration Control
- Administrative Support
- Financial Support

## TESTING PROCESSES

HUGHES

### Hybrid Testing

Functional

( low, high, and ambient temperature )

Environmental

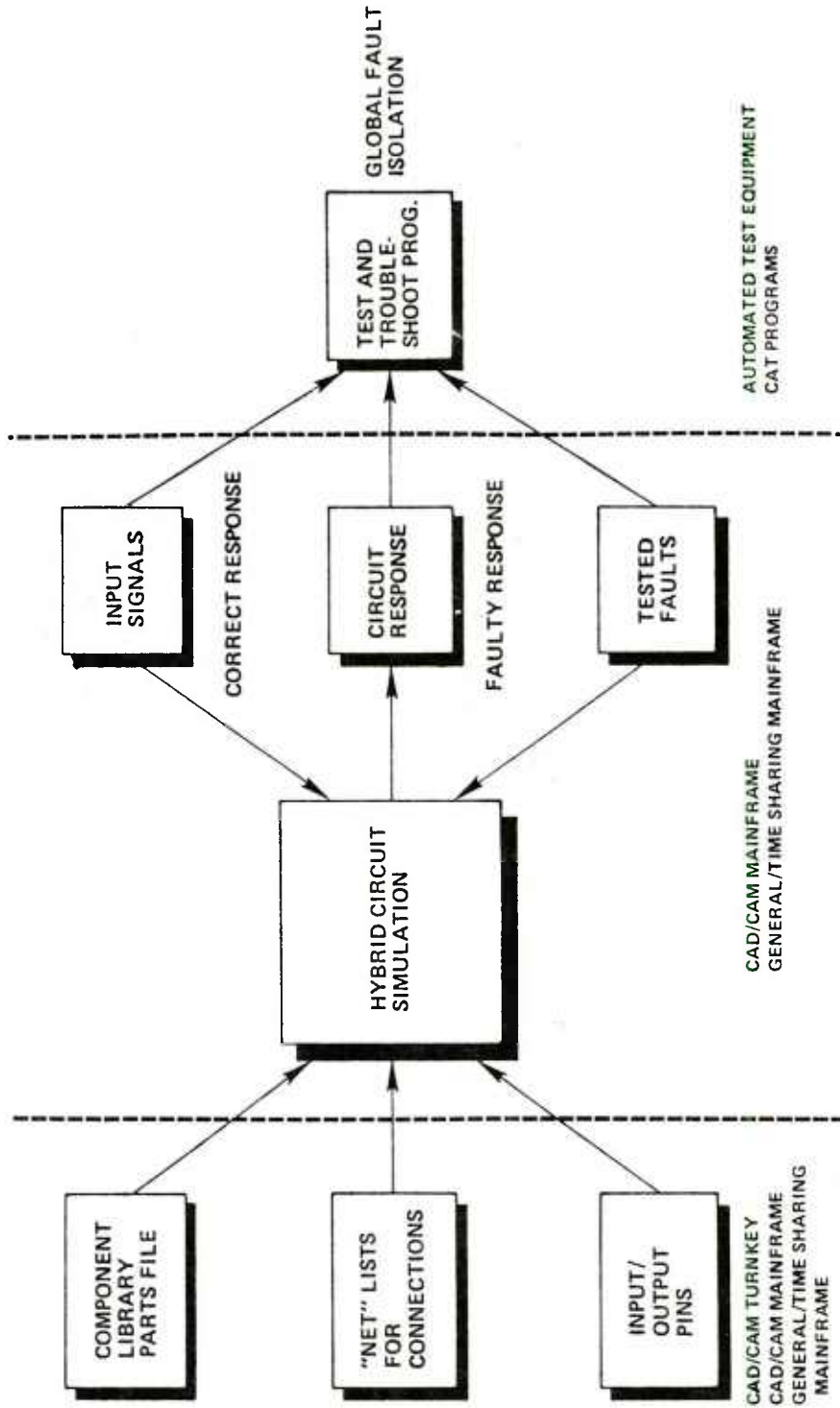
( leak, shock, temperature cycle, burn-in, etc. )

Fault Isolation

Failure Analysis

# ILLUSTRATIVE TEST PROGRAM GENERATION

HUGHES



## SYSTEMS AND TECHNOLOGY ASPECTS

HUGHES

### Systems Requirements

Physical Communications Interfaces  
Hybrid Database Specifications  
Component Placement & Routing Software

### Technology Needs

Automated Parts Identification  
Automated Material Handling  
Thick Film Ink Characterization w/IR Furnace  
Semi-automatic Probe Pre-screening of Die  
Automatic Camera & Test Probe System  
Automatic Substrate Inspection  
Microbridge Production Technology

## HICADAM SUMMARY

HUGHES

- Initial Functional Flow Defined
- Initial Systems Architecture Drafted
- Initial Technology Assessment Made
- Preliminary Systems Requirements
- Preliminary Technology Needs
- Established A Common Reference Point
- Reviewed by the ECAM Hybrid Commodity Group

## SESSION I-3

### CHIP CARRIERS; WHERE DO WE GO FROM HERE

By: JON S. PROKOP  
Texas Instruments Incorporated  
Equipment Group  
Dallas, Texas

The chip carrier has been around since about 1970. It was not until approximately the mid to late 1970's however, that it began to reach prominence in the world of electronic packaging. Two critical things happened in this time frame. The first was that the JEDEC Council undertook a strong thrust in standardizing chip carriers. The second was the Department of Defense took a leadership position in establishing chip carriers as a reality by funding three major Manufacturing Technology programs. The results of these programs are typified by Figure 1. Today we have available both 40 mil center and 50 mil center chip carriers in a wide variety of configurations suitable for the majority of integrated circuit and memory devices available on the open market. So, through these Manufacturing Technology programs, a development idea has been translated into a production reality. This is exactly what MMT programs are designed to do.

So much for history. Let's discuss the future for a few moments. Chip carriers are available today from a number sources in terminal counts ranging generally from 16 to 84. There are a few parts tooled with 120 terminals, but typically, parts are not available in terminal counts higher than 84. On the other hand, the advent of gate arrays and the VHSIC program has created a need for efficient device packaging with terminal counts in the order of 100 to 300. There is even some discussion about terminal counts reaching as high as 600. Chip carrier packages in terminal counts greater than 84 become increasingly less efficient as terminal counts increase. Clearly, chip carriers, as they exist today, are not the correct answer for packaging devices of this nature.

New packaging concepts could be used to solve this problem, and work is going on with fine pitch chip carriers with 20 and 25 mil terminal centers, pin grid array packages and the open-via chip carrier. However, physical device packaging is not the only approach to solving this particular problem. Figure 2 is a generic plot of pin-outs versus gates per function for any device or system. It indicates that as the number of gates per function increases, the number of pinouts increases as well. However, this figure also indicates that there is a tendency for devices and/or systems to "peel off" from this curve. This "peel off" results from the consideration of packaging economics at the time when device and/or system design is occurring.

An example of this can be found in Texas Instruments' approach to VHSIC packaging. Figure 3 is a comparison of the packaging approaches taken by the six VHSIC contractors. The most significant thing to notice in this comparison is that Texas Instruments' VHSIC devices will be packaged using standard chip carriers with terminal counts peaking at 84, while the other contractors are using a variety of packaging technologies with terminal counts reaching as high as 244.

There is no "magic" in what was done to keep Texas Instruments' VHSIC terminal counts low. Packaging economics and potential risk was incorporated into the initial system design trade-off matrix. This systems' perspective resulted in the concept of "programmation" being used on these devices. This is a partitioning scheme involving the incorporation of I/O, RAM and microcontrol ROM directly onto gate array devices, which not only keeps terminal counts low, but allows four different devices to be configured from one gate array.

System partitioning can be used to resolve a large percentage of the packaging problems we, as an industry, face today and will face in the near future. Looking further into the future, it is clear that something other than the problem resolution approaches discussed above must be used to minimize system packaging costs and related problems. What is needed is improved synergistic interaction between all industry and DoD factions.

Overall, this is the cornerstone of the MT program, and I what think, as the future unfolds, will be recognized as the key contribution of this program. Industry's challenge is to embrace this concept and learn to properly work with it.

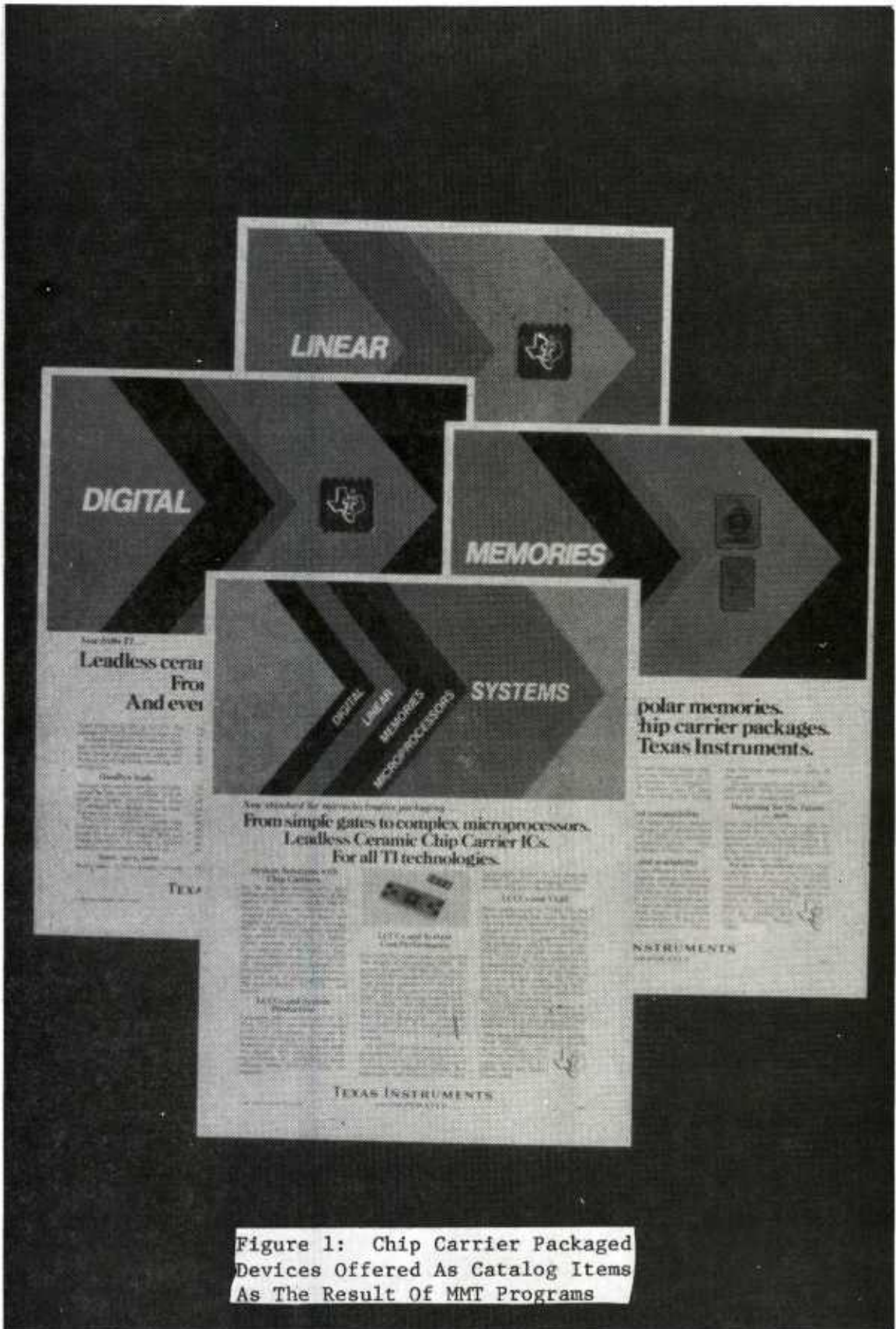


Figure 1: Chip Carrier Packaged Devices Offered As Catalog Items As The Result Of MMT Programs

# PINOUT "PEEL OFF"

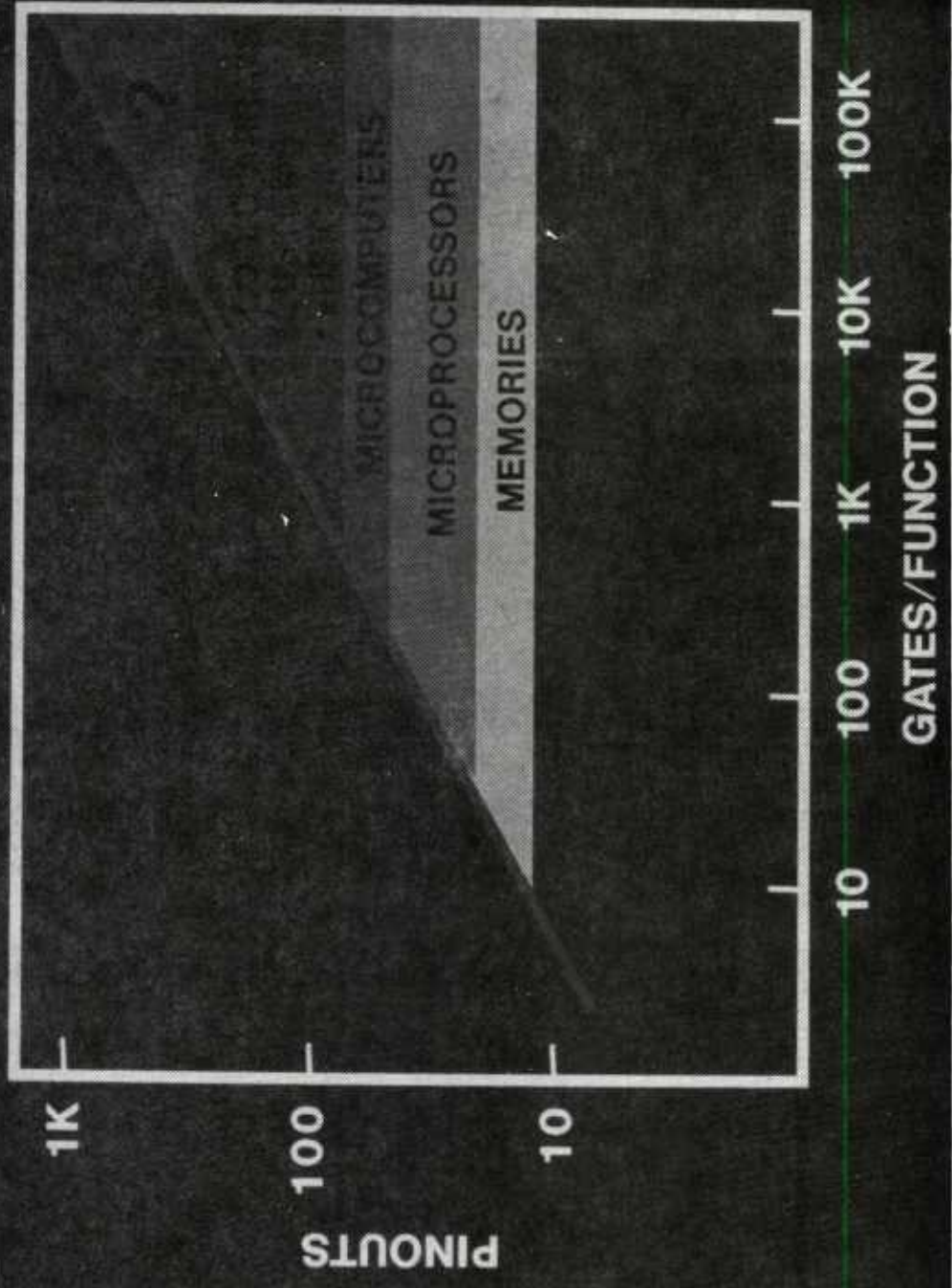


Figure 2

# CONTRACTOR SUMMARY

CONTRACTOR	MAXIMUM CHIP DISS.	MAXIMUM TERM. REQ'D	MAXIMUM C-C SPACING	DIE TO PKG. INTERCONNECT	TYPE
HONEYWELL/3M	1.9W	160	100 MILS	TAB	PIN GRID ARRAY
HUGHES	0.7	148	25	WIRE BONDS	FLATPACK
IBM	3.0	244	100	DECAL Cu TO BUMP	PIN GRID ARRAY
TRW/MOTOROLA	3.0	132	25	WIRE BONDS	LEADED CHIP CARRIER
WESTINGHOUSE	1.3	200	12.5	WIRE BONDS	LEADED CHIP CARRIER
TI	1.6	84	50	WIRE BONDS	LEADLESS CHIP CARRIER

Figure 3: VHSIC Device Packaging

## SESSION I-4

### ELIMINATION OF NOBLE METALS IN HYBRID MICROCIRCUITS

by

John O. Crist

Laser & Optical Materials Branch  
Electromagnetic Materials Division  
Materials Laboratory  
Air Force Systems Command  
Wright-Patterson Air Force Base, Ohio 45433

1. Thick film hybrid microcircuits, as their name implies, consist of a variety of discrete components such as capacitors and resistors as well as digital and analog integrated circuits (ICs). These components are electrically connected together through the use of conductor paths, historically gold (Au), that have been previously screen printed on a ceramic substrate and fired between 800°C and 1000°C. To complete the electrical connections, Aluminum (Al) wires are ultrasonically bonded from the ICs to the Au thick film conductors. These miniature interconnection systems have been used for many years in commercial and government applications alike. However, the reliability of the hybrid interconnection system is a particular concern for military applications due to the harsh environments in which these devices are used. One such reliability issue involves the Au conductor/Al wire interface which can physically separate due to the migration of Al molecules into the Au conductor material. This migration leaves physical voids, or holes, within the Al called Kirkendall voids, thus leaving a weak wire bond that can fail in a military environment.
2. To solve this interface problem, one of three fundamental approaches may be taken: (1) deposit a layer of a metal such as Nickel over the gold conductor, thus forming a barrier between the Al and Au; (2) improve the Au/migration inhibitor alloying; (3) replace Au conductors with an alternate material. All three options are potential solutions. The first approach has already been considered by many in industry. However, this option does incur the additional costs of another deposition layer. Approaches 2 and 3 are presently being investigated in the Materials Laboratory through a Manufacturing Technology (Man Tech) contract, # F33615-80-C-5010, and a Research and Development (R&D) contract, #F33615-81-C-5001, respectively.
3. The Man Tech effort is utilizing existing furnace technology with an improved Au alloy thick film conductor designed to reduce metal migration. Some of the basic advantages of this approach include (1) no modifications to existing furnace equipment, (2) the resulting Au thick film paste is expected to be available from a major thick film vendor, and (3) present resistor technology and wire bonding techniques will still apply. However, despite the definite advantages of the new Au thick film alloys, it is evident that industry is clearly advancing toward the use of non-noble metal systems such as copper (Cu) for future applications. The use of Cu instead of Au has two obvious advantages (1) unlike Platinum (Pt) and Palladium (Pd), which are commonly used in Au alloys, Cu is not considered a strategic material. (2) Cu does not fluctuate in price as dramatically as Au.

If military weapon systems are to take advantage of this new technology, the reliability of these new copper conductor/dielectric/resistor systems must be proven in military environments. The R&D effort mentioned previously is clearly focused on this issue and is expected to provide a firm R&D base for this technology.

4. To date, the Man Tech effort is showing strong promise for a Au/Pd thick film material (AVX 555). Reliability data is expected to be published soon by the contractor, Boeing Aerospace Co., Seattle, Washington (J. W. Bieber). The R&D contract with Rockwell International Corp., Anaheim, Ca (J. J. Licari), has thus far shown strong promise for copper thick film materials. Prior to this contract, Rockwell demonstrated the initial feasibility of using copper conductors for Al chip and wire applications (Fig. 1). The present contract involves the evaluations of DuPont 9923 and Cermalloy 7029D copper thick film conductors with compatible dielectric and resistor families (10 ohms/sq. - 100K ohm/sq.). The interim results of this effort are expected to be made publicly available within the next six months.

5. In summary, the Materials Laboratory is striving to improve wire bond reliability in hybrid microcircuits through the use of both improved and new thick film materials. A potential solution using an improved Au/Pd alloy is showing strong promise in eliminating present Au/Al metal migration problems in hybrid chip and wire applications. For future applications, the use of copper thick film systems in hybrids appears to be a promising approach in view of current results.

Fig. 1

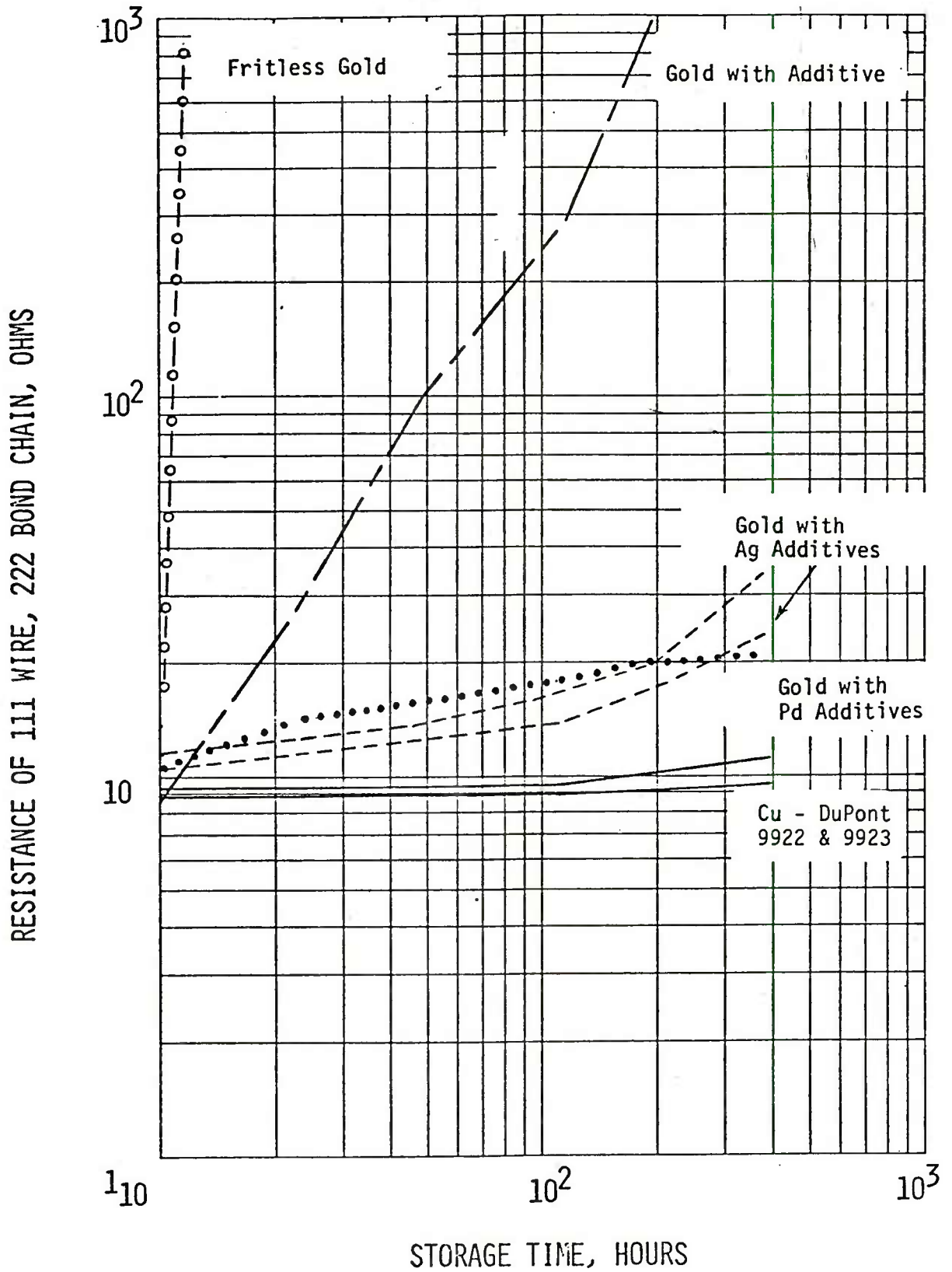


FIGURE 1 RESISTANCE CHANGE OF 1.0 MIL ALUMINUM WIRE BONDS AT 350°C IN N<sub>2</sub>

## SESSION II - 1

### Thrust Areas for Components & Packaging Working Group

by

GORDON D. LITTLE  
USAMICOM

The Components and Packaging Working Group, in addition to its general coordinating activities, has established two thrust areas for Printed Circuit Board manufacture. The first thrust area is concerned with improvements in military printed circuit board quality and manufacture. The second thrust area is for a high density printed circuit to meet the anticipated requirements of the Very High Speed Integrated Circuit (VHSIC) effort and the continuing requirements for smaller volume, less weight and higher reliability as, for example, is required in missile and avionics applications. Both these thrust areas have been established for technological guidance, discussion and the synergistic effect that can be generated by tri-service involvement and do not represent official DoD policy.

The thrust area concerned with Printed Circuit Board (PCB) manufacture and quality, was initiated in February 1979 at a Tri-Services planning conference in Tampa, Florida for Components and Packaging. A list of problem areas and anticipated future requirements (projects) for PCB were submitted by industry and government personnel at the conference, which included a joint session with the Electronic Industries Association and representatives from the Institute for Interconnecting and Packaging for Electronic Circuits (IPC). During the conference the proposed projects were discussed, additional projects were proposed and the projects were ranked by ballot action. The results of that ranking is shown in Figure 1. The IPC also agreed that they would prepare a ranking by survey letter of IPC members and submit it for publication in the proceedings of the conference. This was accomplished and the results of this action is also shown in Figure 1.

As a result of the identification of problem areas and future requirements several of the projects are either completed, ongoing or planned for future action. Some examples of this will be cited below. The Air Force and Army both have coordinated plans for (IPC Rank #1 in Figure 1) immediate large projects that are concerned with the Dimensional Stability of Materials, and miniature components mounting for PCB. The Army has completed a project on Laser Scan of PCB which accomplishes a major portion of the visual inspection of PCB. (IPC Rank #4 in Figure 1). The Army has completed two projects on Rigid Flex Cables, one concerned with the manufacture and the other concerned with connector attachment and molding.

The Army is nearing completion of a Printed Circuit Board cleanliness project and has already completed a project for automated Printed Circuit Board Digital Testing (IPC Rank #8). The Air Force has a completed project concerned with direct pattern generation for PCB. There are other examples of activity in the proposed thrust area, but a listing of all are beyond the scope of this paper. Some of the above cited examples were planned before the conference, but it is felt that the ranking helped to solidify and encourage ongoing and planned efforts in these areas.

A less formal meeting of the Components and Packaging Working Group was held at Redstone Arsenal in mid 1980. This group addressed a US Army Missile Command proposed program for high density printed circuit boards utilizing miniature hybrid type components. The High Density Printed Circuit Board Thrust Area was thus established to meet anticipated requirements concerned with Large Scale Integrated (LSI) circuits, the similar VHSIC requirements, and established requirements for small volume, light weight, highly dense military electronic applications. The thrust area includes a compatible high density packaging system for substrates (PCB type), miniature components, conductors, heat transfer, assembly and test. A partial list of the proposed projects for high density packaging is shown in Figure 2. There has been progress made in the thrust area. A completed US Army Missile Command program for semi-additive conductors shows promise as the conductor system technology for 2 mil lines and spaces and possibly smaller dimensions. Also considered important are miniature passive components and a hermetically sealed chip. The hermetically sealed chip requirement could initially be met by presently available ceramic chip carriers, should progress to a miniature ceramic chip carrier and ideally would include a tri-metal (or other) hermetically sealed semiconductor chip with dimensions no larger than the bare chips. Other proposed projects as in Figure 2, are being considered by the Tri-Services.

Another thrust area proposed by the group is in the area of military batteries. No concrete actions have been taken to date, but this may be established as a future additional thrust area.

IPC & MTAG  
PRINTED CIRCUIT BOARD THRUST AREA  
MM&T SURVEYS

<u>IPC RANK</u>	<u>MTAG RANK</u>	<u>PROPOSED PROJECTS</u>
1	8	Dimensional Stability of Dielectric Material
2	10	Active Flux Removal (Cleaning Procedures)
3	-	PTH Cleaning (Plasma, Etch, Laser)
4	5	Automatic Visual Inspection
5	6	Production of Rigid/Flex Circuits
6	-	Automatic Nondestructive Testing of Clad Lam.
7	1	DOD Standard Repair Procedures
8	2	Automatic Cleaning and Testing of PWB
9	3	Low Cost Laminates for Military Use
10	-	High Frequency Laminates
11	-	Direct Pattern Generation
12	4	Automatic Assembly
13	9	Elimination of Photo Image Tooling
14	7	Multi-Lead Component Removal

Figure 1. Printed Circuit Board Projects for Thrust Area 1

THRUST AREA FOR COMPONENTS AND PACKAGING W.G.

VERY HIGH DENSITY PRINTED CIRCUIT BOARDS

---

1. Thin film Semiconductors
2. Thin film Passive Devices for PWB's
3. Thin film Printed Wiring Boards
4. Automatic Assembly of VHD PWB's
5. Printed Wiring Boards with 2 mil Conductor and Spaces
6. High Density Multilayer PWB's
7. Design Standards for High Density PWB's
8. Heat Removal for High Density PWB's
9. Miniature Passive Devices for PWB's
10. Hermetically Sealed Chips for PWB's

FIGURE 2. Components & Packaging  
Thrust Area 2

## SESSION II-2

### NICKEL CADMIUM BATTERY PROGRAM

BY

DR. GLEN R. BUELL

AFWAL

The paper will describe MM&T Contract Work at Eagle Pitcher, Colorado Springs, Co., on nickel cadmium battery production processes with emphasis on positive plate construction. The new electro-chemical production process for impregnation of the positive plate will be described along with solutions to several unanticipated problems. In this process, a nickel slurry is picked up on a nickel wire screen and baked on in an oven thereby sintering the powder into the screen. MM&T process development follows several years work at the Propulsion Lab at Air Force Wright Aeronautical Labs.



## FLEXIBLE CB PROCESSES

FLEXIBLE PCBs WITH MOLDED CONNECTORS

NON-PLANAR PCBs

SEMI-ADDITIVE REEL TO PEEL PROCESSES

MULTI-LAYER FOLDED CIRCUITS

## PWA TESTING

INFRARED TESTING OF PWAs

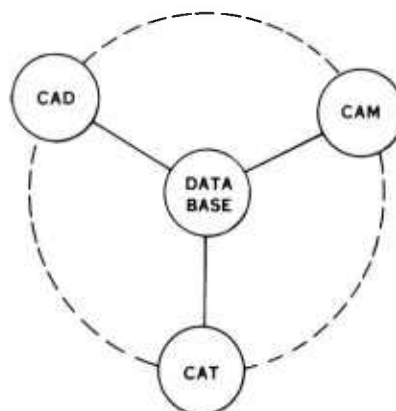
OPTICAL (LASER) INSPECTION OF PCBs

DIGITAL FAULT TESTING

The work is divided into several areas of interest including design, manufacturing processes for PCBs and for flexible CBs, and board testing. The first chart lists design and manufacturing processes covered herein, generally in the sequence applied. The second chart shows flexible circuit manufacturing processes and testing methods for either configuration. The lists do not cover all the processes needed to make a circuit board, but only those elected for study by the Army within its manufacturing technology program. Other processes have been studied by the Navy and Air Force but they are not the subject of this paper.

The text following consists of brief descriptions and illustrations of work performed on the contracts listed. The descriptions are arranged in the sequence shown in the two previous charts and listed with their complete titles in the Index.

## ECAM



380,81 1075

ELECTRONICS COMPUTER AIDED MANUFACTURING (ECAM)

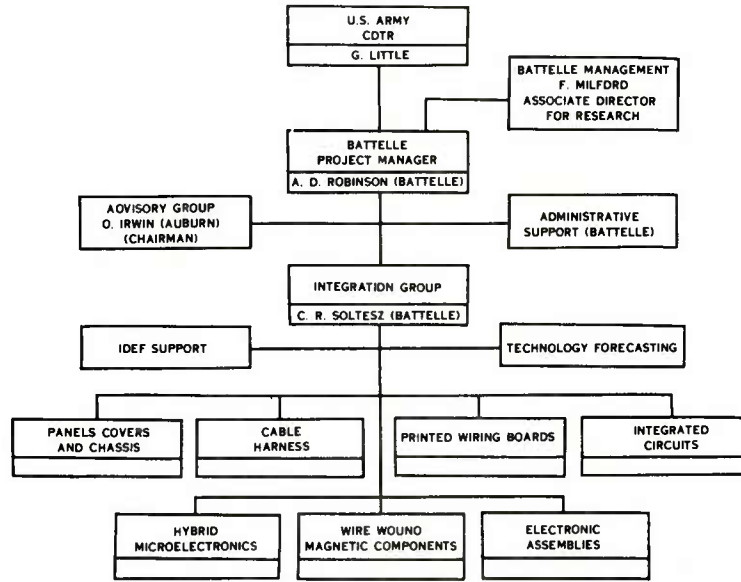
Battelle Laboratories, Cleveland, OH, in conjunction with a consortium of twelve electronics firms, is developing the architecture for a complete computer-aided-design/computer-aided-manufacturing and testing capability for seven types of electronics commodities.

A portion of the work will be to define the present capability in computer aided design, manufacture and test of printed wiring assemblies. A firm having a Calspan system, for example, for

design layout of circuit boards rarely uses the same data base to drill, route, plate or test the boards. This project is intended to bridge the gap between circuit board design and manufacture, and arrive at a common data base that is usable for all three areas.

The following firms form the consortium called for in the contract: AULT, Boeing, General Dynamics, General Electric, Honeywell, Hughes, IBM, Magnavox, McDonnell-Douglas, Microelectronics Engineering Corporation, RCA and Rockwell.

PROJECT ORGANIZATION



Funding for the Battelle contract is coming from Air Force and Navy as well as Army. Army Missile Command (MICOM) provided the contracting officer's representative, Mr. Gordon Little, and Army Materiel Development and Readiness Command (DARCOM) provided the funding. At DARCOM, Mr. George Schuck is project officer. The support structure, integration group, and commodity areas covered are shown here. A matrix illustrating activity areas to be supported by the various coalition members is also provided.

ACTIVITY AREAS OF COALITION MEMBERS

	INTEGRATION	ADVISORY	PANELS, COVERS	CABLE & HARNESS	PRINTED WIRING BOARD	I.C.	HYBRID	WIRE-WOUND	ASSEMBLIES
AULT								●	
BOEING	●	●		●	●				●
GD	●				●				●
GE	●								
HONEYWELL	●	●	●				●	●	
HUGHES	●	●	●	●	●	●	●	●	●
IBM	●	●	●	●	●	●	●	●	●
MAGNAVOX	●	●				●	●	●	●
MCDONNELL DOUGLASS	●	●	●	●	●	●	●	●	●
MEC						●	●	●	
RCA	●	●	●				●	●	●
ROCKWELL	●	●	●	●	●	●	●	●	●

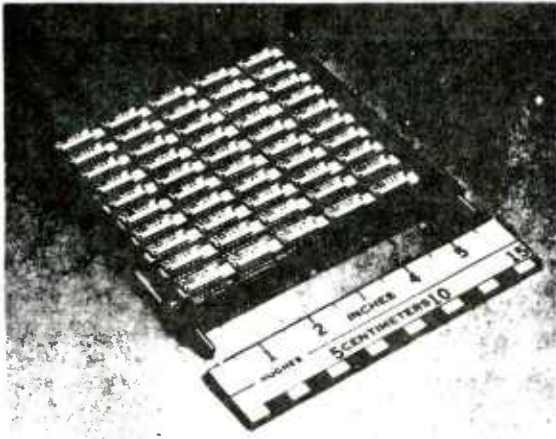
The end result of the work will be a Master Plan showing efforts required to bring about this technology. Leading into that plan is a broad study of present architecture, and an outline of



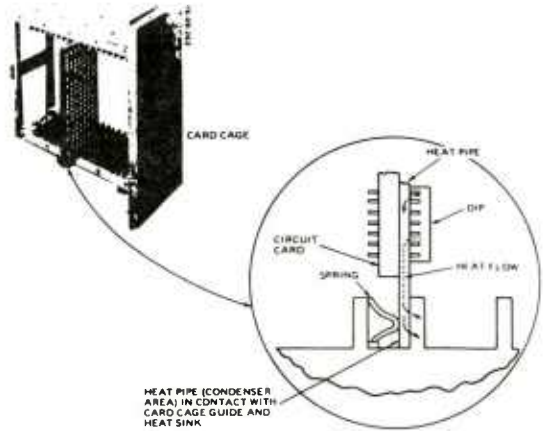




4000 heat pipes per week was designed and its cost estimated at \$500K.



**HEAT PIPE CARD WITH  
DIPS INSTALLED**



**REPRESENTATIVE HEAT PIPE  
APPLICATION**

Shell material selected was cartridge brass, CDA260; wick material was sintered stainless steel fiber, Dynalloy X-11; brazing alloy for wick-to-cover was silver braze foils, H&H 505; brazing alloy for cover to base was silver braze foil, H&H 560; fluid was Acetone.

Proponent: Mr. William Hoft, US Army Missile Command, Huntsville, AL 35898, (205) 876-2077.

Contract number is FR79-12-292. Dr. Kal Sekhon and Mr. Lloyd NeVow were principal investigators.

382,83 1103

**STABLE MATERIALS AND MANUFACTURE FOR MULTILAYER PWBS**

A contractor will establish a relationship between material variables and dimensional stability because interlayer misregistration increases with thinner base materials.

Will apply R&D data to improve materials and board fabrication methods to reduce registration failures. Work will result in improved specifications for copper-clad laminates, and pre-preg materials. Improved materials are available but not yet covered by Military Specifications.

Also, manufacturing parameters will be altered to reduce Z axis stress caused by the bonding process.

378 3171

**AUTOMATIC MONITORING AND CONTROL OF WAVE SOLDERING MACHINE**

Westinghouse Electric Corporation, Baltimore, MD, analyzed the variables involved in wave soldering of circuit boards and determined that a number of improvements could be made to the equipment and methods. The combination of interacting conditions and materials studied included solderability, flux activity, flux application, preheat temperature, conveyor speed, solder temperature, solder wave shape, area of contact, solder wave surface conditions, heating rate of the assembled board.

The entire process and equipment was analyzed for ways to improve and simplify it. A wave soldering machine was modified to incorporate these concepts:

- a. Fixturing that better protects the board and reduces sensitivity to wave flow variations.
- b. Airless spray fluxing to apply fresh, thinner flux.



Flexible printed wiring can save 80% of the weight, 20% of the volume, and 30-50% of the cost of military interconnection assemblies.

Proponent: Mr. Gordon Little, US Army Missile Command, Huntsville, AL 35898, (205) 876-3604.

Contract number is DAAK40-79-C-0212.

R80,81,82 3411  
MANUFACTURE OF NON-PLANAR PRINTED CIRCUIT BOARDS

General Dynamics, Pomona, CA, is developing methods for making curved or cylindrical circuit boards.

A glass-reinforced plastic cylinder would be built up of successive layers of circuit board material. After drilling and through-hole plating, components would be assembled from the inside and the tube rotated through a hot solder wave. To prove the process, ten eight-layer boards of moderate complexity will be built.

Proponent: Mr. Robert Brown, US Army Missile Command, Huntsville, AL 35809, (205) 876-5742.

Contract number is DAAH01-81-C-A777.

381,82 1063  
SEMIADDITIVE REEL TO REEL FLEXPRINT PROCESS

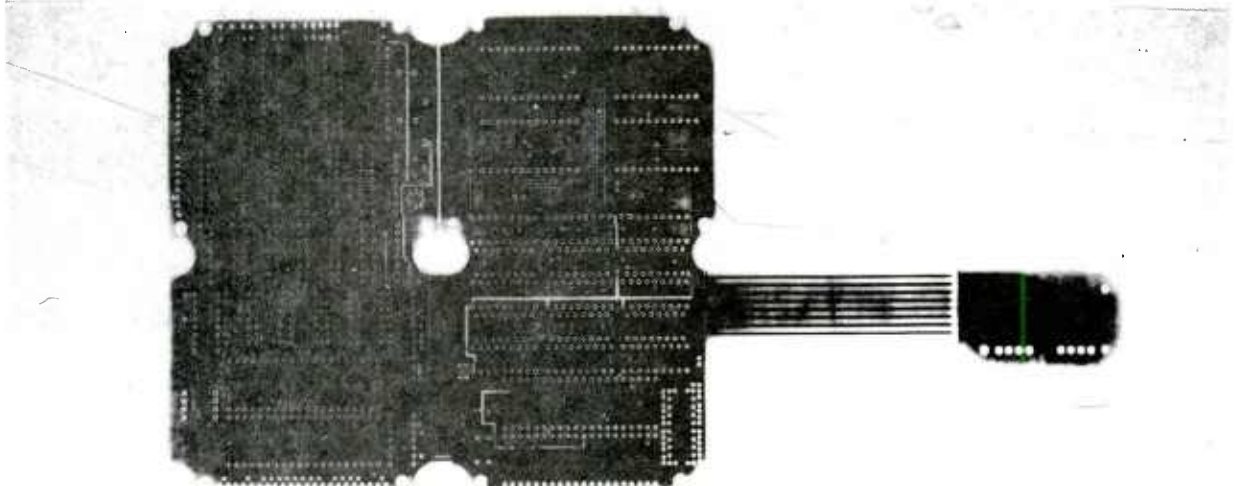
A contractor will assemble reel-to-reel equipment for making flexible circuits. Process steps will include stations for drilling, deburring, cleaning and applying electroless copper in the through-holes, and for plating up copper therein, and then for cleaning, rinsing, and drying single or double clad flex strip.

Also, for applying film photoresist, pattern exposure, and resist development. Then for copper etching, cleaning, drying and re-reeling. A hot solder dip may precede the rollup step. Flexible cables or circuits processed by this equipment will comply with MIL-P-5524(EL).

Proponent: Mr. Robert Brown, US Army Missile Command, Huntsville, AL 35809, (205) 876-5742.

F80 3054  
PRODUCTION METHODS FOR MULTI-LAYER FOLDED CIRCUITS

Hughes Aircraft Company, Ground Systems Group, Fullerton, CA, is establishing materials and processing specifications and standards for multilayer, multifolding rigid-flex circuit boards. Fabrication and testing will be automated and circuit board etching and plating will be optimized.



Rigid-flex folding circuit boards will be built for first application in the Position Location Reporting System (PLRS).

Proponent: Mr. J. G. Johnstone, US Army Communications and Electronics Command, DRCPM-PL-BC, Fort Monmouth, NJ 07703, (201) 532-1688.

378 3075  
INFRARED TESTING OF PRINTED WIRING ASSEMBLIES

Hughes Aircraft Company, Los Angeles, designed and built an inspection system for identifying and isolating printed wiring assembly flaws. The system uses infrared sensing and scanning techniques to locate hot spots and temperature abnormalities on operating circuit boards.

The system first makes a thermal profile of a good board and files this data in a computer; it represents a standard against which similar boards are compared. Locations of anomalies or faults are detected by an IR sensor and read by a computer and recorded. Thus, poor solder joints, marginal components, overloads, imbalances, neglected or improper heat sinks, and other flaws are identified. Correction of these errors eliminates trace pulling and peeling, board blistering, and component failure.

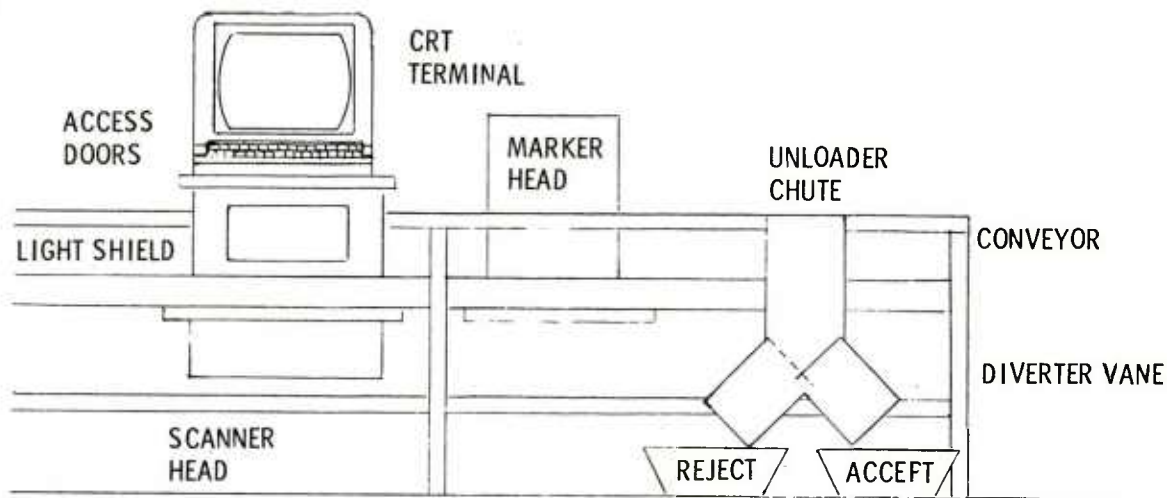
Hughes Aircraft Company is now marketing the system. The project engineer at Hughes was Mr. Donald Keever.

Proponent: Mr. Gordon Little, US Army Missile Command, Huntsville, AL 35898, (205) 876-3604.

Contract number is DAAK40-78-C-0276. Final report number is E-79-10.

377,80 3169  
AUTOMATIC OPTICAL INSPECTION FOR PRINTED CIRCUIT BOARDS AND COMPONENTS

Chrysler Electronics Division, Huntsville, AL, designed and built a production-oriented inspection system for evaluating populated circuit boards. The system uses a laser beam scanned across the bottom side of a bare board, a populated board, or a populated and soldered circuit board to obtain defect data. Defects may be printed out on a label that is affixed to the circuit board. The system is best used after lead clinching and before wave soldering as the rework cost is lowest at that time.



Chrysler plans to market the inspection systems. It should sell well because it has an economic payback period of only 2-1/2 to 3 years.

Proponent: Mr. Robert Brown, US Army Missile Command, Huntsville, AL 35898, (205) 876-5742.



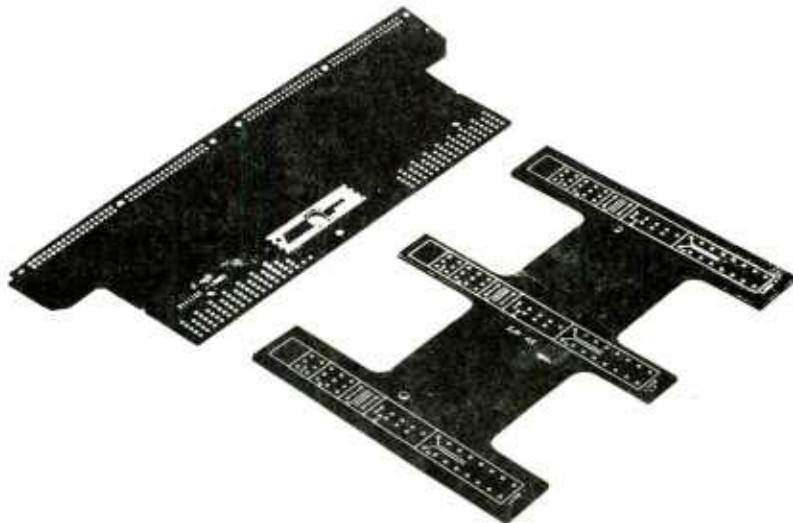


EXHIBIT 1. Deliverable Rigid-Flex Cables of Polyimide Construction.  
N00123-77-C-1192

#### **Rigid-Flex Printed Circuit Manufacturing Processes**

**Contractor: General Dynamics, Pomona Division, Pomona, CA**

**Project Engineers: Mr. Joseph A. Reavill, Mr. R. W. Aubert, and Dr. Marvin Abrams**

**NAVSEA Contract No. N00123-77-C-1192**

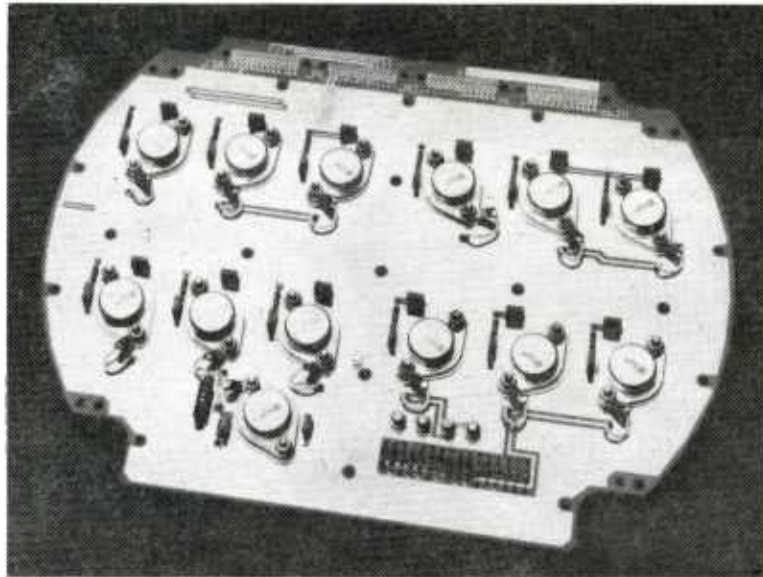
**Project No. DNS-77479**

**NOSC Project Monitor: Mr. C. Spurlin, Code 748, 271 Catalina Blvd, San Diego, CA 92152**

General Dynamics developed a fully documented manufacturing process for fabricating rigid-flex printed wiring cables with polyimide glass laminate stiffeners and copper/kapton/acrylic adhesive flexible layers.

They substituted polyimide glass laminate stiffeners for epoxy glass laminate stiffeners to improve drilling characteristics, prevent thermal damage caused by Z-axis expansion, and increase processing uniformity. The polyimide laminate cut Z-axis expansion by 54% and improved compatibility with individual processes. Process optimization gave a 25 percentage point yield increase, from 60% to 85%. Also, the previously observed bulging and tilting of the laminate which caused innercircuit separation appears to be overcome. Substitution of acrylic adhesive for the previously used phenolic butyral adhesive provided a yield increase in an earlier project. Material suppliers can now concentrate on providing materials needed for this type of construction.

The Report also includes extensive materials specifications and processing data. Report number NAVSEA MT S-479-77 (NOSC TR 531).



Auto-Pilot Regulator Board

**Metal Core Printed Wiring Board Fabrication**

**Contractor:** General Dynamics, Pomona, CA

**Project Engineer:** Dr. Marvin Abrams

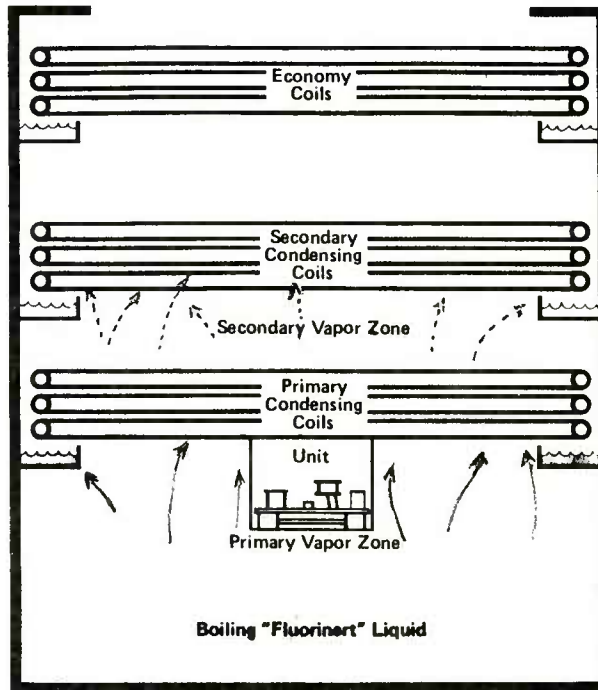
**Contract No.** N00123-80-C-0970

**Navy Project No.** DNS 80695

General Dynamics developed a method for producing metal core circuit boards for applications requiring high heat conductivity. Several layers of insulator material and copper substrate are laminated to one side of the aluminum panel while absorbent cloth is available on the other side to absorb the B-stage material that oozes through the holes in the aluminum panel. After cure, the absorbent cloth is removed and B-stage insulator material and copper laminate applied in a similar laminating operation. This makes for a double sided board.

Metal core printed wiring boards can be fabricated in any facility having the capability of producing standard multilayer boards to military specifications. The aluminum is treated as any other layer to be laminated except for the drilling operation for component lead insertion and two step laminating process.

At the time this project was initiated, the metal core boards were approximately ten times more expensive than a standard board. They are still approximately twice the cost but production boards made by this method are expected to cost only 20% more than a normal multilayer board.



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## Vapor Phase Soldering

Contractor: General Dynamics, Pomona, CA

Project Engineer: Dr. Marvin Abrams, et al

Contract No. N66001-80-C-0054

Navy Project No. DNS 80695

General Dynamics developed a procedure for batch soldering connectors onto flexible printed wiring harnesses. This replaces the current method which calls for hand soldering each connector pin to the pad on the flexible printed circuit, a costly and time consuming procedure. The contractor developed fixturing for mounting the connectors and solder preforms in place on the harness and for immersing the entire assembly into a heated vapor bath.

The vapor phase soldering equipment has means to regulate and control vapors in different temperature zones and for time controlled insertion and removal of the parts. Some modification was done to execute this process. The contractor also worked out a post solder joint evaluation procedure.

A savings of approximately 10 to one is estimated for typical standard missile harnesses and connectors. This amounts to over \$2 million in a five year period.

# **GENERAL DYNAMICS**

*Pomona Division*

20 October 1981

Results of Manufacturing Technology Contract N00123-80-C-0970  
Metal Core Printed Wiring Board Fabrication Process and  
N66001-80-C-0054, Vapor Phase Soldering.

Presentations on both of the subject contracts were made on September 22, 1981 to an invited audience of Department of Defense and military contractor personnel at the Pomona Division of General Dynamics. The presentations consisted of a detailed account of the process parameters and methods involved in the fabrication process, and a description of the verification testing and results, on prototype hardware produced to the process specification as well as projected cost avoidance/reduction analysis.

Both programs used SM-2 Block II hardware for their prototype parts. In the case of the Metal Core PWB program a process was established, which allows these components to be fabricated in a standard printed circuit facility that produces multilayer PWB's to military specifications. The aluminum metal sheet is treated like another layer to be laminated into the basic material sandwich. The only significant additional step that is added to the overall process is a second drilling operation for component lead insertion into the board. At the time this program was initiated metal core printed wiring board were only available from producers of specialty products employing patented processes. Prices typically ranged from \$1500 to \$2500 per board. Although other metal core PWB processes have since become available at more reasonable prices, they feature a fluidized bed approach which in our case would introduce non standard techniques with a resulting cost increase estimated at a minimum of 2:1. The resultant boards produced by the process developed here are estimated to cost only about 20% over that of a normal multilayer printed wiring board (\$150-\$250). Due to the success of the program one such part, the auto pilot regulator board in Standard Missile 2, Block II, has been designed to incorporate this style component. This regulator board has to dissipate considerable thermal energy which is confined in a small volume. In order to allow the design engineers to evaluate and design the bench model and flight test hardware during the development contract phase, manufacturing technology personnel who were conducting the manufacturing development program fabricated engineering parts by the process as it evolved. This close liaison allowed the design and product process development to evolve together into a cost effective component ready for release to production.

# **GENERAL DYNAMICS**

## *Pomona Division*

20 October 1981

Page 2

The Vapor Phase Soldering program developed a process for batch soldering connectors onto flexible printed wire harnesses. The present production process calls for hand soldering each pin of each connector to the component pad on the flexible printed circuit. The process developed here demonstrated a procedure for mounting the connectors together with solder preforms all held in place, and immersing the entire assembly into a heated vapor bath. Thus, solder joining all the pins on all the connectors simultaneously. The program involved establishing a capability to regulate and control vapors of different temperature zones, time controlled insertion and removal of parts, tooling and fixturing for mounting connectors and solder in place on the harnesses, and proper precleaning and post solder joint evaluation. A cost saving of approximately 10.2 to 1 is estimated for typical Standard Missile 2 Block II harnesses and connectors. This would amount to over \$2M savings over a five year period. Commercially available vapor soldering equipment require some custom modifications to be able to properly execute this process. Facilities have been identified for the FY82 procurement plan at General Dynamics to implement vapor phase soldering into the production factory.

Fig. 1

# CROSS-SECTION VIEW

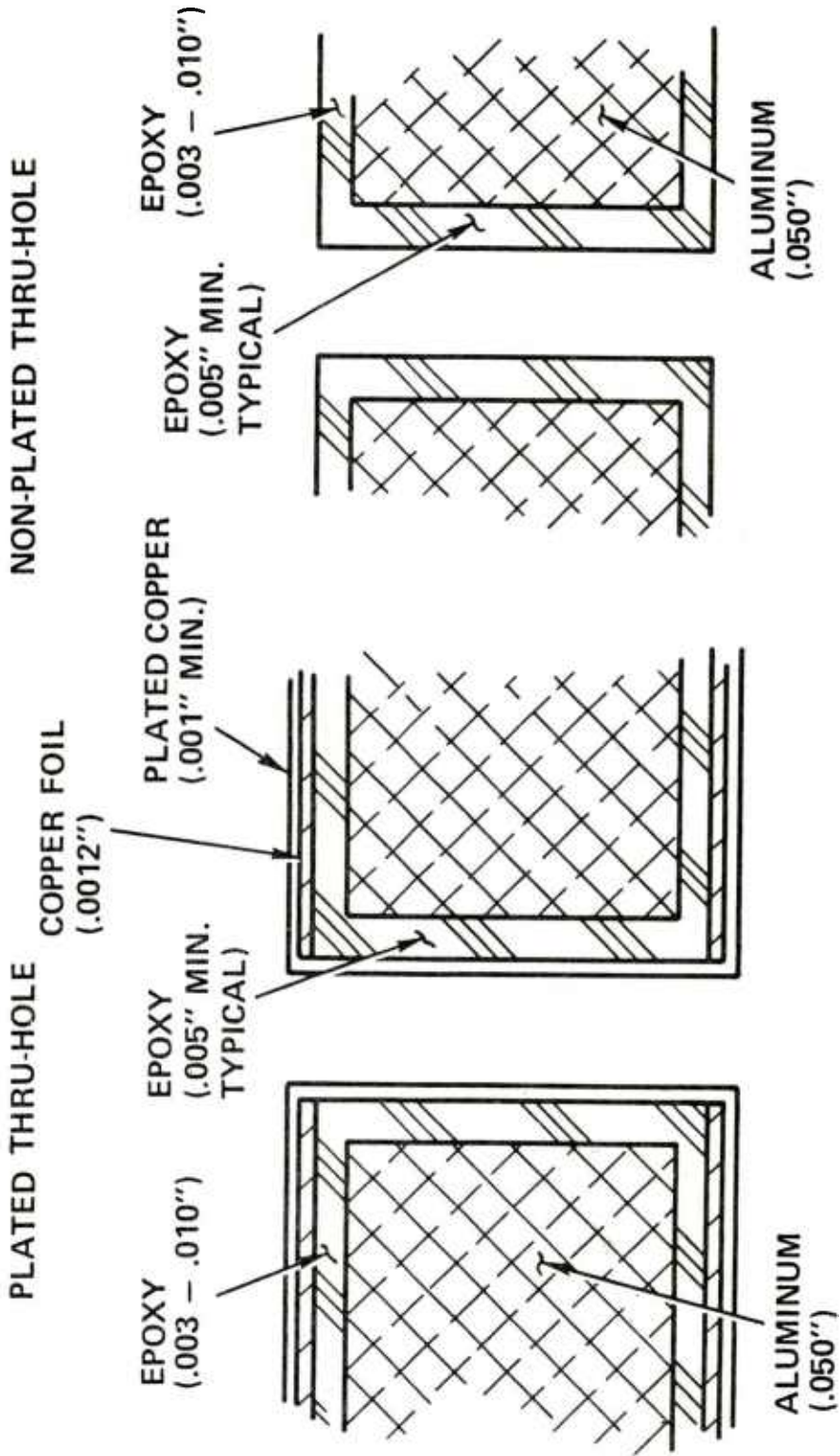


Fig. 2

# GENERALIZED PROCESS SEQUENCE

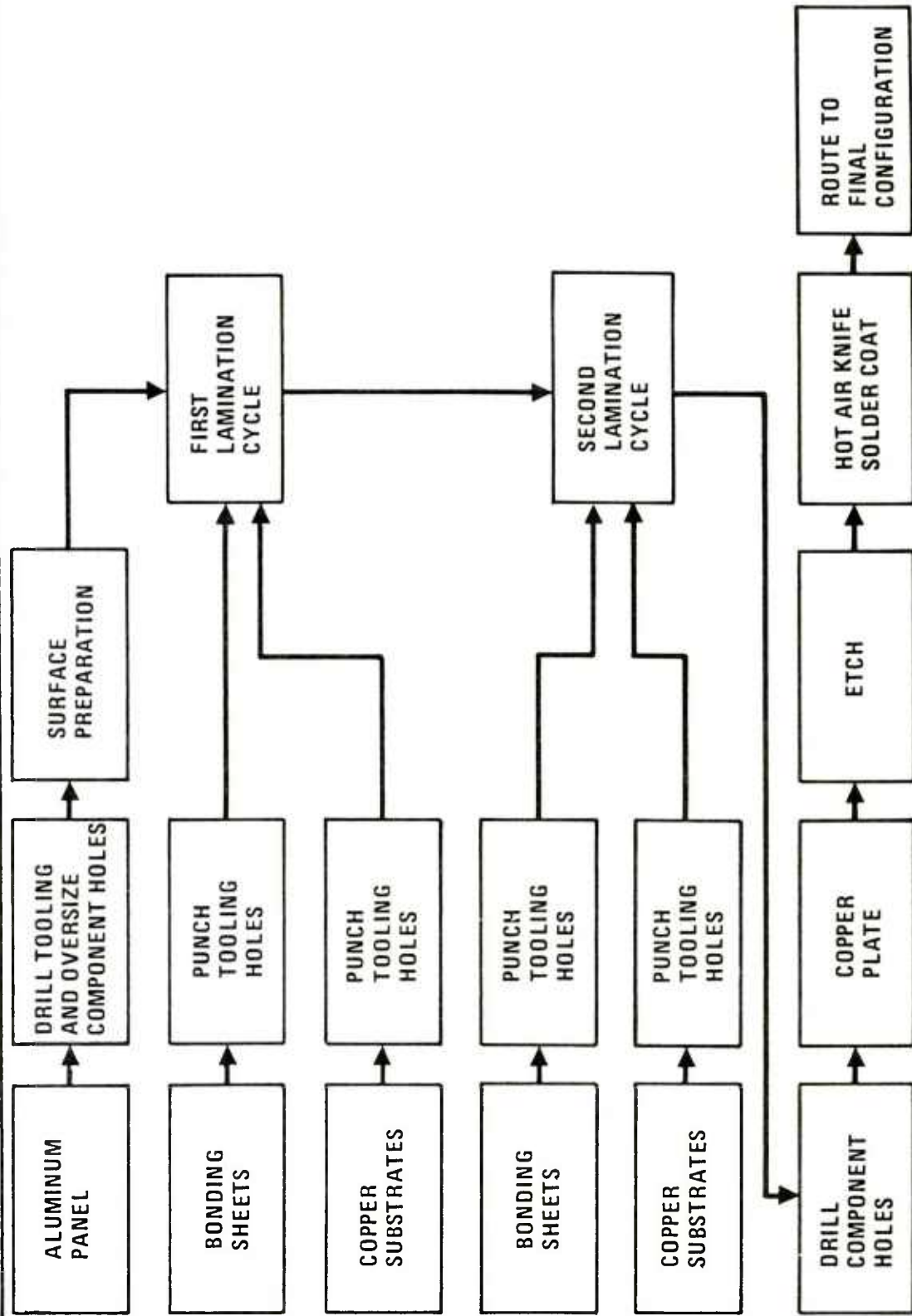
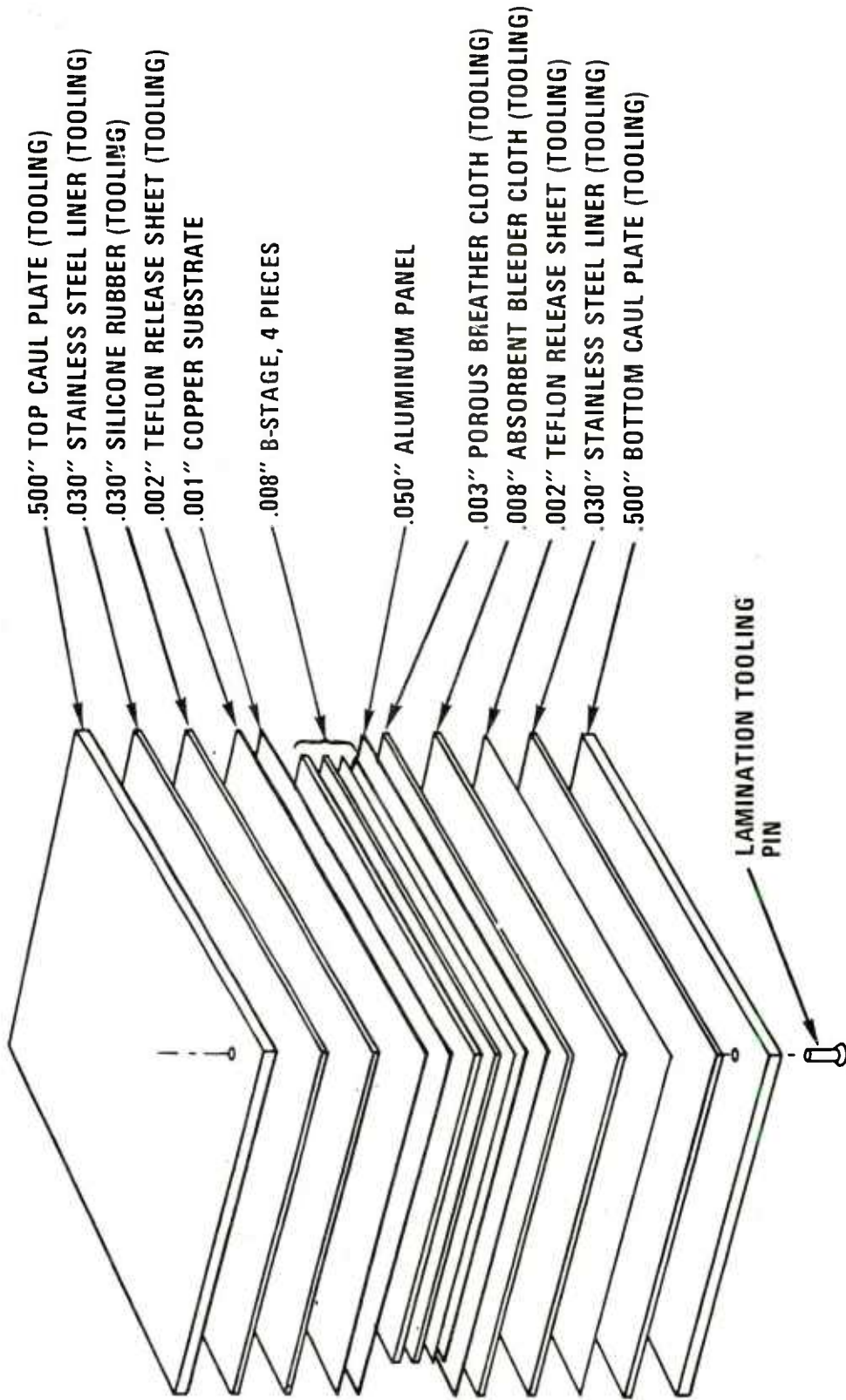


Fig. 3

# SHOWING LAMINATION TOOLING & PANEL LAYERS FOR 1ST LAMINATION CYCLE



"A Review of Air Force Manufacturing Technology Programs Directed at  
PWB Manufacturing Problems"

by  
Donald H. Knapke  
AFWAL/MLTE  
Wright-Patterson AFB, Ohio

Introduction

Manufacturing and maintenance costs of Air Force electronics hardware are escalating rapidly and the magnitude is such that it is a major cost driver in new weapon systems. The unique military demands of high performance and reliability coupled with low volume production requirements are considerably different than those issues that confront the current high volume commercial electronics manufacturing industry. The Air Force Manufacturing Technology (Man Tech) Program is addressing some of the critical issues which contribute to the high cost of fabricating and maintaining sophisticated AF electronics hardware. This paper will specifically discuss past, present, and planned program thrusts and achievements in the packaging and interconnection technology area. The AF Man Tech packaging and interconnection program sponsored by AFWAL/MLTE has been generically oriented with primary emphasis on reducing the manufacturing, assembly, and testing costs of printed wiring board (PWB) assemblies. Technology transfer and production implementation of Man Tech program results are successfully achieved via technical paper publication/presentation, end of contract debriefings/demonstrations, on-site technical interchanges, and publications of technical reports. A short synopsis of several past, current, and future USAF Man Tech programs in the packaging and interconnecting technology are described below.

MT for Conformal Coatings

This program was performed by Rockwell International Corporation, Electronic Devices Division, Anaheim, CA under the technical direction of Dr. James J. Licari. The objectives of the program were to improve the manufacturability and maintainability of conformally coated PWB assemblies by using a solvent soluble conformal coating in conjunction with a permanent solder mask.

Program performance objectives were demonstrated which showed that PWB assemblies which are coated with a solvent soluble conformal coating/solder mask system provide environmental protection equivalent to or better than coatings qualified to Mil-I-46058. Program emphasis was directed toward simple, cost effective, and automatic coating processes to improve coating maintainability and performance and reduce coating costs. Two solvent soluble (Humiseal's 1B31 acrylic and Dow Corning's DC-X9-6326 siloxane-polystyrene block copolymer)/solder mask (Wornow's SR-1000 and Haven Chemical's PC-401) coating systems were identified and optimized. Unique substrate and electrical test pattern configurations were utilized to screen materials and demonstrate coating system performance. Production implementation of program results was accomplished at Rockwell's Cedar Rapids PWB production facility. Project results are contained in AFWAL-TR-80-4139 dated September 1980.

#### MT for Repair of Conformally Coated PWB Assemblies

This program was performed by Hughes Aircraft Company, Technology Support Division, Culver City, CA under the technical direction of Mr. Robert A. Dunaetz. The objectives of the program were to reduce AF Logistics Center costs associated with maintenance and repair of conformally coated PWB electronic assemblies. Specific program achievements were: 1) the establishment of low cost simplified conformal coating identification procedures, 2) simplified/standardized coating removal and replacement techniques, materials and processes, 3) streamlined techniques for component removal and replacement, 4) improved soldering processes/techniques, 5) establishment of appropriate PWB assembly cleaning procedures, and 6) extensive verification of repair integrity, reliability, and conformance to applicable Mil-Specs. Program results have been implemented and are currently being utilized in AF Air Logistics Center electronics repair depots. Also, the AF Technical Order documentation covering PWB assembly repair is being updated to include Man Tech Program results. Project results are contained in AFWAL-TR-80-4086, Vols. I and II.

#### MT for Nickel-Boron Plating

This program was performed by General Electric Company, Electronics Laboratory, Syracuse, NY under the technical direction of Mr. Louis Zakraysek.

Technical guidance and Air Force program interaction/coordination was provided by Mr. John E. McCormick of Rome Air Development Center located at Griffiss AFB, NY. The initial objectives of this program were to establish effective high-volume low cost manufacturing processes, procedures, and controls for electroless nickel-boron (Ni-B) plating of electronic component leads/lead frames and to demonstrate the solderability, shelf life and reliability improvements/enhancements of the Ni-B metallurgical system over existing lead finish systems. The electroless nickel-boron deposit was found to be inadequate as a primary lead finish system for microelectronic package leads due to unacceptable solderability, corrosion protection and formability. After the manufacturing processes for plating electroless Ni-B on both Kovar and copper base metals were established, program emphasis was redirected to an extensive evaluation of Mil-M-38510 lead finish systems to determine the optimum combinations of both primary and secondary lead finishes required to improve solderability and reliability of the microelectronic package lead finish. Program results indicate that the hot solder dip and fused electrolytic tin plate over electrolytic sulfamate nickel are the preferred lead finish systems. Gold deposits exhibited poor solderability and corrosion protection especially if the underplate was discontinuous. Both electroless nickel-boron and electroless nickel-phosphorous are undesirable secondary lead finish materials due to their stressed deposits. Program results were incorporated in the recently revised RADC specification Mil-M-38510. Project results are contained in AFWAL-TR-81-4056 dated June 1981.

#### MT for Direct Pattern Generation of PWBs

This program was performed by Westinghouse Electric Corporation, Systems Development Division, Baltimore, MD under the technical direction of Mr. Richard W. Decker. The objective of the program was to demonstrate that the dynamic on-line laser exposure of PWB photoexist images was feasible and could reduce complex multilayer PWB fabrication times. Program accomplishments were summarized by an on-line industry demonstration of the Laser Pattern Generator (LPG). The LPG operates directly from a digitally encoded data base and has the capability to image intricate PWB circuit patterns on an 18 inch x 24 inch pattern area. Some of the benefits of direct laser imaging by raster laser scanning include: 1) eliminating many processing steps and reducing the time and costs associated with conventional artwork techniques,

2) exposure times are independent of pattern complexity, 3) switching the pattern polarity instantaneously, 4) reducing the design change turnaround time, and 5) improving the accuracy of pattern resolution and registration capability. Also, the use of the LPG enhances future PWB fabrication automation. Westinghouse has implemented the LPG into their PWB production facility. Project results are contained in AFWAL-TR-81-4052.

#### MT for PWB Electrodeposition Process Control

This program was performed jointly by two Rockwell International Corporation divisions, Electronics Research Center at Thousand Oaks, CA and Interconnect Systems Division at Cedar Rapids, Iowa. Primary technical responsibility for the program direction was shared between Dr. Dennis Tench at Electronics Research and Mr. Al Evans at Interconnect Systems. The overall objective of this program was to establish effective, efficient and dynamic process controls for analyzing and controlling electroplating processes used in PWB electroplating operations. Emphasis of the program included the optimization of the cyclic voltammetric stripping (CVS) and rotating cylinder (RC) technologies for analyzing and controlling the copper pyrophosphate plating system. Parameters such as bath composition, additive concentrations, and critical copper deposit properties were established. The CVS and RC techniques were coupled with a novel plated-through hole agitation evaluation technique to define optimum PWB plated-through hole production conditions. The major production accomplishments attained under this program may be summarized as follows: 1) CVS was fully implemented for production control of copper pyrophosphate baths and demonstrated that the additive concentration, the contaminant level, and a "fingerprint" do control plating bath performance, 2) an additive replenishment procedure based on CVS analysis was developed and shown to provide control of the additive concentration to within  $\pm 0.05$  ppm, 3) carbon treatment schedules were streamlined, based on CVS feedback, to efficiently maintain acceptable bath purity under operating conditions, 4) the value of CVS for monitoring bath purity was firmly established by the timely detection of detrimental contaminants sporadically introduced from faulty filter cartridges and contaminating anodes, 5) based on distorted CVS "fingerprints", hydrogen peroxide lingering in the bath after carbon treatment was shown to cause extremely poor through-hole deposits, 6) bath agitation within circuit board through-holes provided by air sparging and board motion was thoroughly charac-

terized and the data was used to improve the production agitation system. Based on pilot-line and production results demonstrating its utility, the RC method was implemented on-line to monitor the deposit tensile properties of PWB production baths. The overall production yield improvement resulting from implementation of this technology was shown to be greater than 10% for complex circuit boards. Rockwell has licensed UPA Technology, Inc. of Soyosset, NY to market the CVS technology to the PWB industry. Project results are contained in AFWAL-TR-81-4027 dated May 1981.

#### MT for PWB Electrodeposition Processes

This program was recently awarded to Rockwell International, Electronics Research Center, Thousand Oaks, CA and is under the technical direction of Dr. Dennis M. Tench. This program is a follow-up to the previous Air Force Man Tech program and requests an expansion of the CVS and RC technologies to PWB acid copper, tin/lead, and tin electroplating baths as well as electroless copper plating baths. The objectives of the program are to characterize acid copper plated through-hole (PTH) electrodeposit properties relative to Mil-P-55110C reliability requirements. Primary program emphasis is directed at multiple site on-line PWB production implementation of CVS and RC technologies for dynamic analysis and control of PWB acid copper electrodeposition processes. This will be coupled with a comprehensive cost analysis and documentation of the resulting technological impact on process yields, product quality and reliability, and improved PWB production rates.

#### MT for PWB Processes and Controls

This program is currently being performed by Martin Marietta, Orlando Aerospace Division, Orlando, Florida, under the technical direction of Mr. Walter S. Rigling. The objectives of the program are to improve PWB process yields and reduce manufacturing costs by optimizing the PWB design-manufacturing-productibility interface. Program emphasis is directed at establishing a real-time PWB manufacturing/productibility index (MPI) and effective manufacturing information feedback loop for the PWB designers utilization. The program's three tasks are: 1) to establish the interrelationships required in the PWB design data base to attain a dynamic PWB-MPI for complex multi-

layer board structures, 2) to integrate these data base elements and assemble the necessary prototype equipment to demonstrate the MPI concept, 3) to operationally demonstrate and verify a dynamic/real-time feedback loop for MPI utilization by the PWB designer; and 4) analyze and documentation of the cost impact and PWB manufacturing yield improvements resulting from MPI technology vs current design techniques and manufacturing methods. The completion date for this contract is December, 1982.

#### MT for High Reliability Packaging Using Hermetic Chip Carriers with Compatible PWBs

This is a planned FY82 new start Air Force Man Tech program to address specific packaging and interconnection issues surrounding the utilization of the high density leadless hermetic chip carrier (HCC) packages. The objectives of this planned Man Tech program are to establish fabrication techniques for printed wiring boards (PWBs) which are thermally, mechanically, and electrically compatible with the standard HCC packages. The program will emphasize the optimization of PWB materials, substrate fabrication and assembly techniques, and manufacturing process controls required to reduce and/or eliminate any thermal or mechanical incompatibility with this interconnection structure. The program will also include a comprehensive analysis (identification and quantification) of the stress factors which cause structural incompatibilities and the engineering tradeoffs required to accomplish a reliable HCC/PWB electronic assembly. An industry coalition type approach to achieve program objectives and to enhance technology transfer/industry implementation is planned.

#### Summary

Hopefully, this brief program review has provided an insight into some of the accomplishments of the Air Force Man Tech packaging/interconnection program. The programs described above represent an Air Force investment of approximately \$3.6 million dollars over four (4) years. Widespread industry implementation and utilization of Man Tech program results is needed to continue to insure maximum return on investment of this Air Force seed money. To enhance the benefits and implementation of future Air Force investments, the trend is toward Technology Modernization (Tech Mod) type programs which couple emerging technology developments with an Air Force business/acquisition strategy.

## SESSION II - 4

### GRID WIRE COATING MACHINE FOR POWER GRID VACUUM TUBES

E. J. Dutkowski  
Naval Weapons Support Center  
Crane, Indiana

#### ABSTRACT

The purpose of this MANTECH Program is to improve the process control of a grid-wire-coating machine. This should result in a more controllable process leading to a higher yield in vacuum tube production. The grid-wire-coating machine consists of coating molybdenum wire through electroplating and sintering operations. This process was developed by EIMAC/Division of Varian twenty to thirty years ago and much of the same techniques and equipment is still in use today.

In order to provide better control over this process, a new machine will be built using today's techniques and equipment.

## INTRODUCTION

Military high-power radar and communications systems in use today, in general, use power-grid vacuum tubes for radio frequency amplification, switching, and/or high voltage regulation. The power-grid vacuum tube normally consists of a cathode, an anode and one or more grids. The grids for these tubes require finely controlled characteristics to function correctly in the different applications.

The EIMAC Y633C is a power-grid tetrode vacuum tube, shown in figure 1, being utilized in the Navy's AEGIS Weapons System. This tube is used as a series dc switch for a Crossed-Field Amplifier (CFA) in the AN/SPY-1A Radar Transmitter and as a high voltage regulator in the MK-99 Continuous Wave Illuminator (CWI). This tube, in production, has had a history of low yield due to difficulty in meeting grid drive specifications. This parameter is primarily controlled by the properties of the grid wire.

Investigation into the grid wire problem has led to a Manufacturing Technology Program to improve the controls over this process and the machinery involved. The grids used in the Y633C, as well as many power-grid tubes, are made of coated molybdenum welded into cage shaped assemblies as shown in figure 2. Molybdenum is used because of the high strength requirements due to the large size and high temperature operation. The electrical properties of the grid wire are strongly dependent on the coating that is applied to the wire and how it is processed. In general, the grid wire coating can affect the primary electron emission, thermal emissivity and other parameters.

## BACKGROUND

The grids, both control grid and screen grid, that are used in the AEGIS Switch Tube are constructed of molybdenum wire coated with platinum black, zirconium,

and carbon. The process by which the coating is applied was developed by EIMAC thirty years ago and later patented by EIMAC. The process is known by the trade name Y3. EIMAC manufactures this coated wire today at their Salt Lake facility for use in tubes constructed by EIMAC and the coated wire is sold commercially as Y3 Coated Wire.

#### EXISTING FACILITY

The existing machine at EIMAC's Salt Lake City facility, as shown in figure 3 is twenty to thirty years old. The techniques used to operate this machine are again the same age. The process is highly dependent on skill and judgment of the individual operator. For this reason, Y3 manufacturing is not a dependable process by modern standards. In the past, the process has been plagued by widely varying wire performance characteristics resulting in unpredictable yields in tube production.

As we can see in figure 4, the existing process starts with molybdenum wire passing through an electrolytic acid etch to clean the wire, followed by a deionized (DI) water rinse to remove acid residue. A coating of platinum black is electro-deposited on the wire, the wire is rinsed with DI water and dried, then a slurry powdered carbon plus finely divided particles of zirconium is applied by passing the wire through a fountain at the zero velocity point. The wire is then passed through a controlled atmosphere furnace, to sinter the coating on the surface of the wire. After this process, the wire is spooled, stored, unspooled, inspected, surface processed which consist of wiping the excess material off of the surface and inspecting with a microscope.

#### PROCESS CONTROLS

A high degree of process control is required to maintain control of the wire characteristics. The primary characteristics affecting the tubes' electrical operation are shown in figure 5.

WIRE DIAMETER/PLATING THICKNESS: The wire diameter is primarily controlled by the original molybdenum diameter but is added to by the plating thickness of the platinum. There is a minimum thickness that can be maintained and still have the correct metalurgical composition and electrical characteristics. Since the platinum used in the process is the major cost of producing this wire, keeping this plating thickness to a minimum is desirable.

THERMAL EMISSIVITY: Thermal emissivity is primarily controlled by the particle size in the coating and the surface texture of the finished wire.

PRIMARY EMISSION: This parameter is directly related to the platinum coverage and the mix in the sintered coating. Consistent plating is subject to both temperature, plating current, plating contact and bath purity. The mix in the sintered coating is controlled by the particle size and viscosity of the slurry.

SECONDARY EMISSION: Secondary Emission is a surface roughness phenomenon and is directly controlled by particle size, firing temperature and polish.

WELDABILITY: The wire coating has a substantial effect on welding characteristics.

Other factors that affect the useability of the wire are impurities in the coating, the chamber or curvature of the wire and the ductility of the wire.

#### IMPROVED FACILITY

The improved Y3 machine will eliminate many of these problems and reduce reliance on human judgments. The improved facility will consist of three separate sections. The wire cleaning area, the plating/coating area and the spooling/inspection area.

The cleaning section, as shown in figure 6, will consist of two controlled atmosphere furnaces, electrolytic acid etch tank and a rinse tank. This machine will prepare the wire for the plating process. The wire will be fired in a wet hydrogen furnace to remove chemicals left from the drawing process. The wire is then power rinsed in a deionized water and electrochemically etched. The wire is again

power rinsed in deionized water and passed through a dry hydrogen furnace to dry the wire. The wire will then be spooled and stored, ready for use in the coating machine.

The coating machine, shown in figure 7, will contain a laser micrometer to measure the wire diameter before passing into the plating bath. The wire will again be measured after the plated wire is dried and the two diameter measurements will be compared and the difference used to control the plating power supply and therefore the plating thickness. The laser micrometer will measure the wire diameter to one-hundredth of a mil (.00001") and the plating thickness will be controlled to three-hundredths of a mil (.00003"). The wire is again tensioned to maintain a level run through the rest of the machine.

The wire will then pass through a fountain of a zirconium slurry (at the zero velocity point) with a constant viscosity, flow, pressure and specific gravity controls. From there the wire will pass through a Hydrogen reducing furnace. This furnace will have a preheat zone to slowly heat the wire and prevent thermal shock which can knock the zirconium coating off the wire. The hot zone will have separate heat monitors and controls for maintaining correct reaction temperature. The wire will exit through a cool down zone so that the wire will be cool enough not to react with the atmosphere. An exit tensioner is required to maintain a level wire through the furnace while the angle of the wire to the take-up spool varies.

A continuous measurement will be made of the wire diameter in the wiping and inspection station shown in figure 8. The diameter read-out will be recorded for future analysis.

## SUMMARY

The improvements made on the Y3 machine will reduce the cost of wire production through minimization of the use of platinum, reduce skilled labor for machine operation and increased useable finished wire, i.e. less wire requiring reprocessing. More importantly, the wire will be made with consistent and controllable characteristics required for high yields and long life in vacuum tubes in which it's used. The proposed completion date for this project is July 1984. The demonstration of this project will be held at EIMAC's Salt Lake City facility.

## LIST OF FIGURES

- Figure 1.....EIMAC Y633C Tetrode
- Figure 2.....EIMAC Y633C Grid Assemblies
- Figure 3.....Present Y3 Grid Coating Machine
- Figure 4.....Present Y3 Machine - Block Diagram
- Figure 5.....Process Characteristics
- Figure 6.....Proposed Cleaning Station
- Figure 7.....Proposed Coating Operation
- Figure 8.....Proposed Spooling/Inspection Station

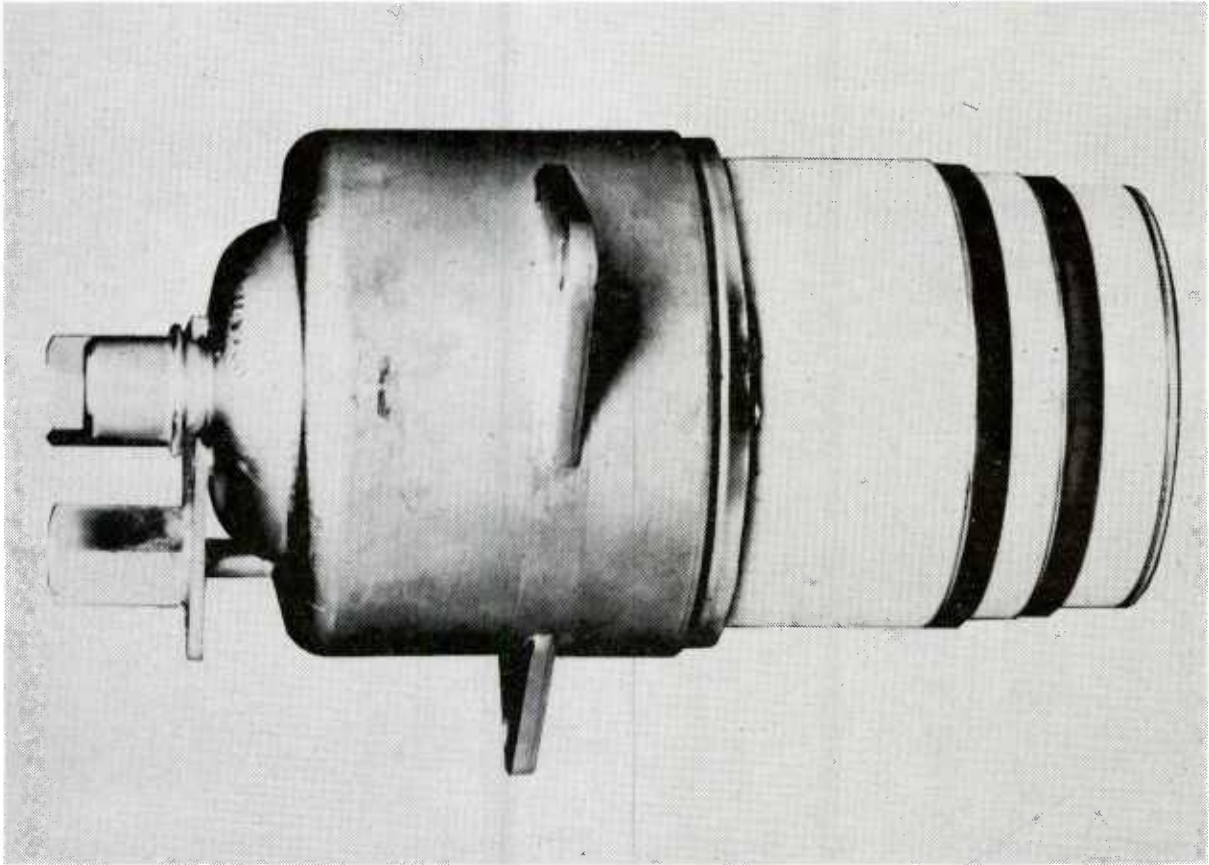


Figure 1 EIMAC Y633C Tetrode

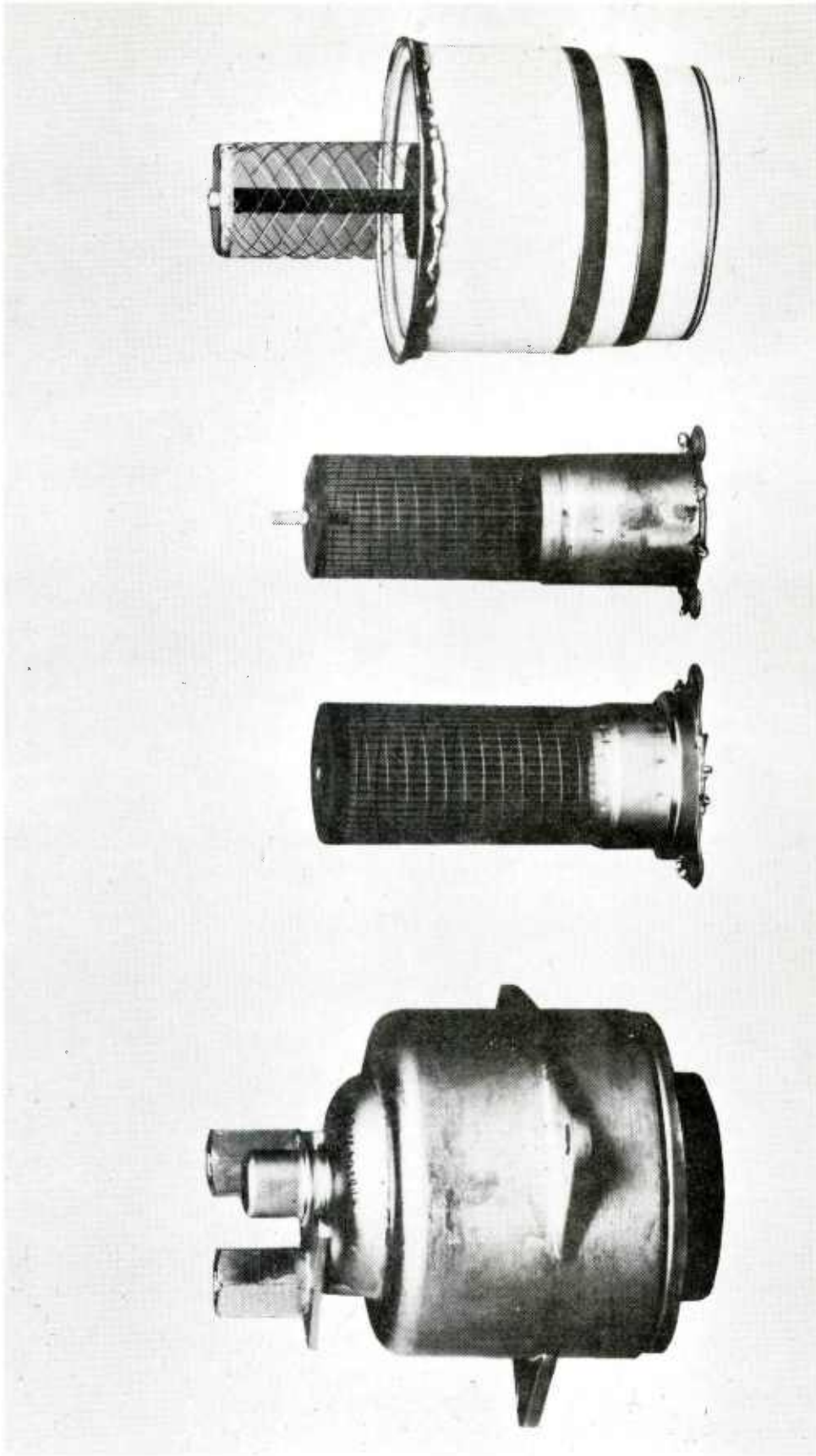


Figure 2 EIMAC Y633C Grid Assemblies

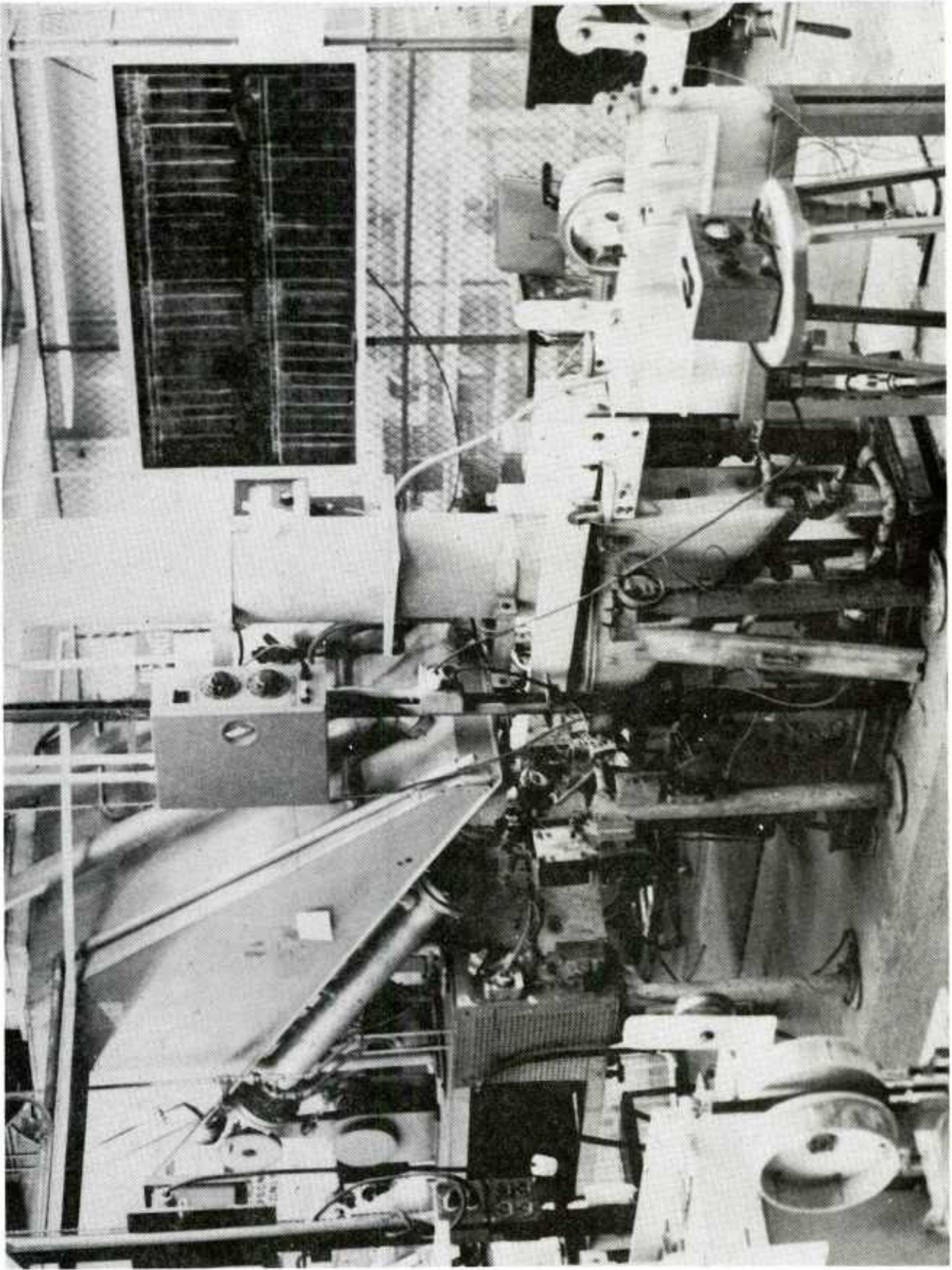


Figure 3 Present Y3 Grid Coating Machine

# EXISTING Y3 MACHINE

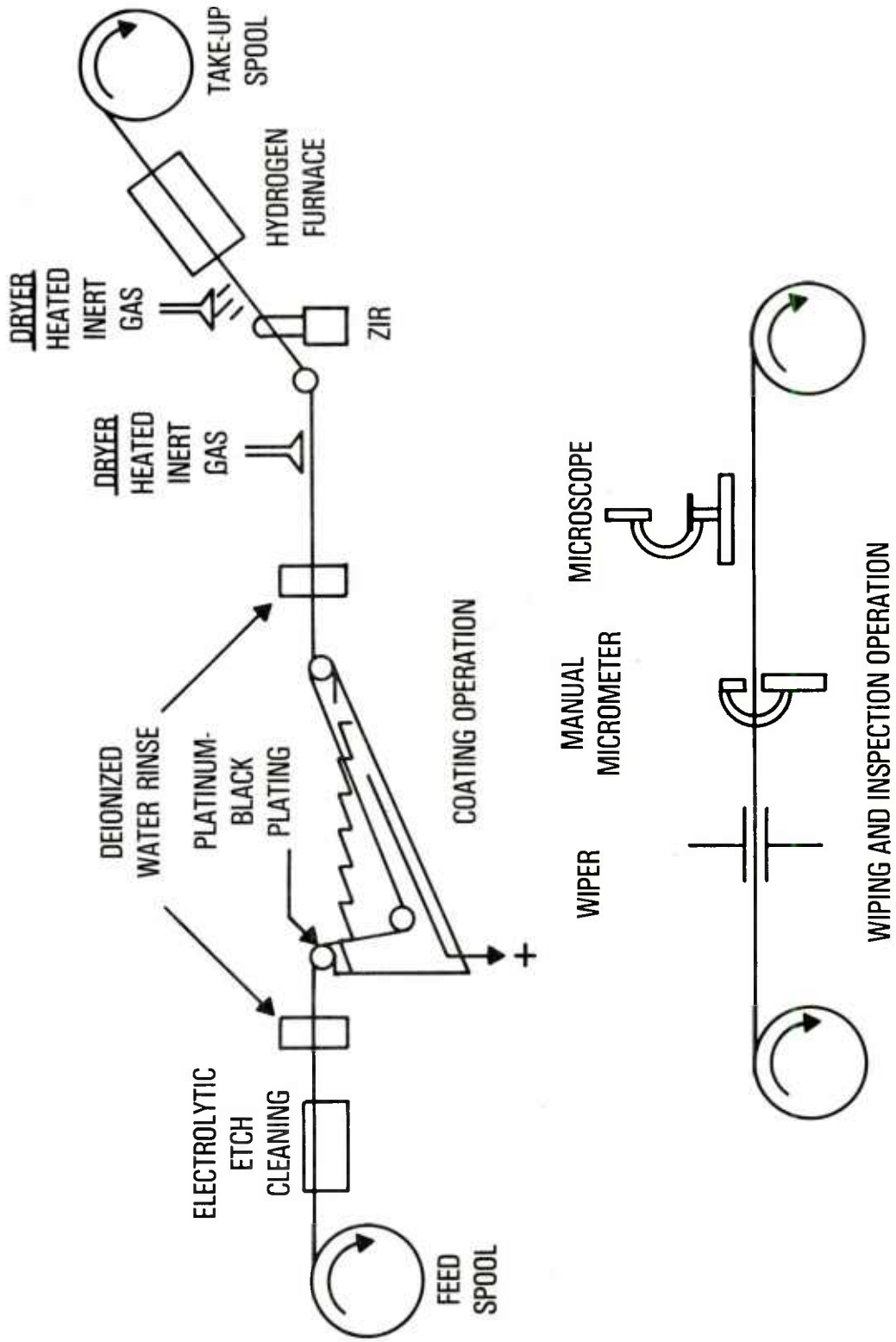


Figure 4 Present Y3 Machine - Block Diagram

- **WIRE DIAMETER**
- **THERMAL EMISSIVITY**
- **PRIMARY EMISSION**
- **SECONDARY EMISSION**
- **WELDABILITY**
- **IMPURITIES**
- **CAMBER**
- **DUCTILITY**

Figure 5 Process Characteristics

# PROPOSED CLEANING OPERATION

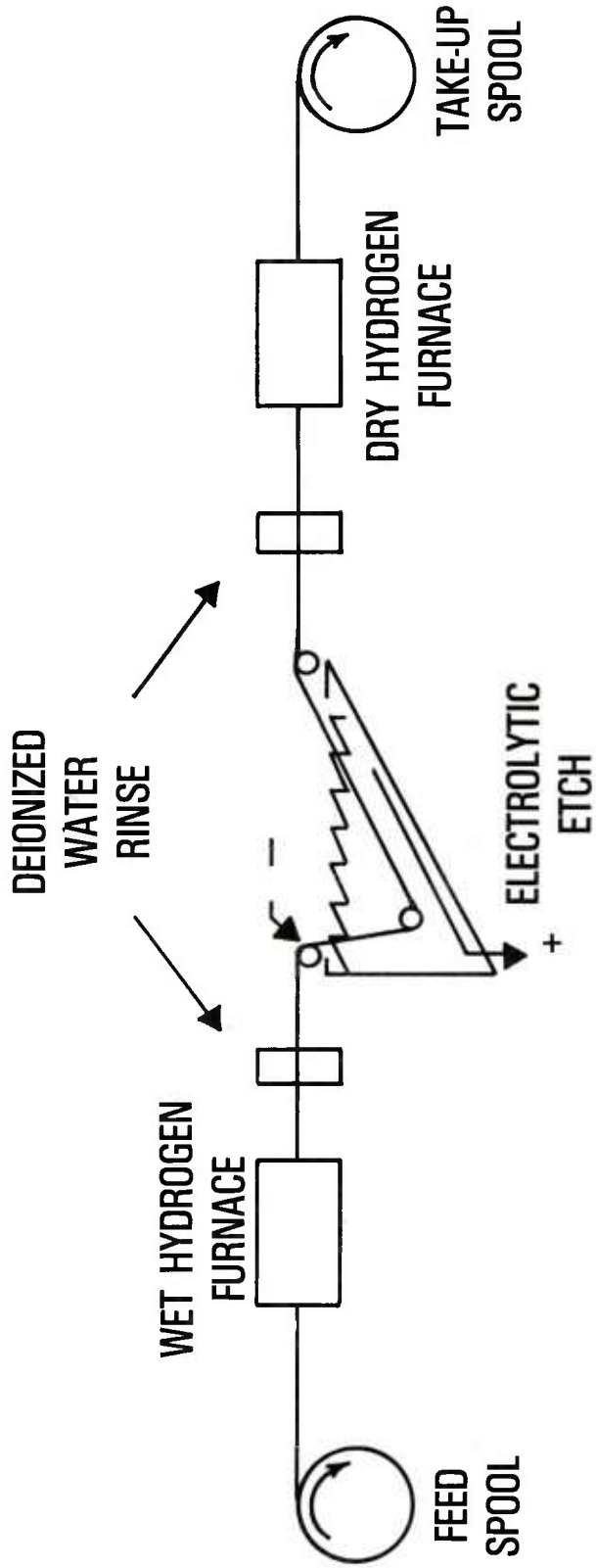


Figure 6 Proposed Cleaning Station

# WIRE MACHINE

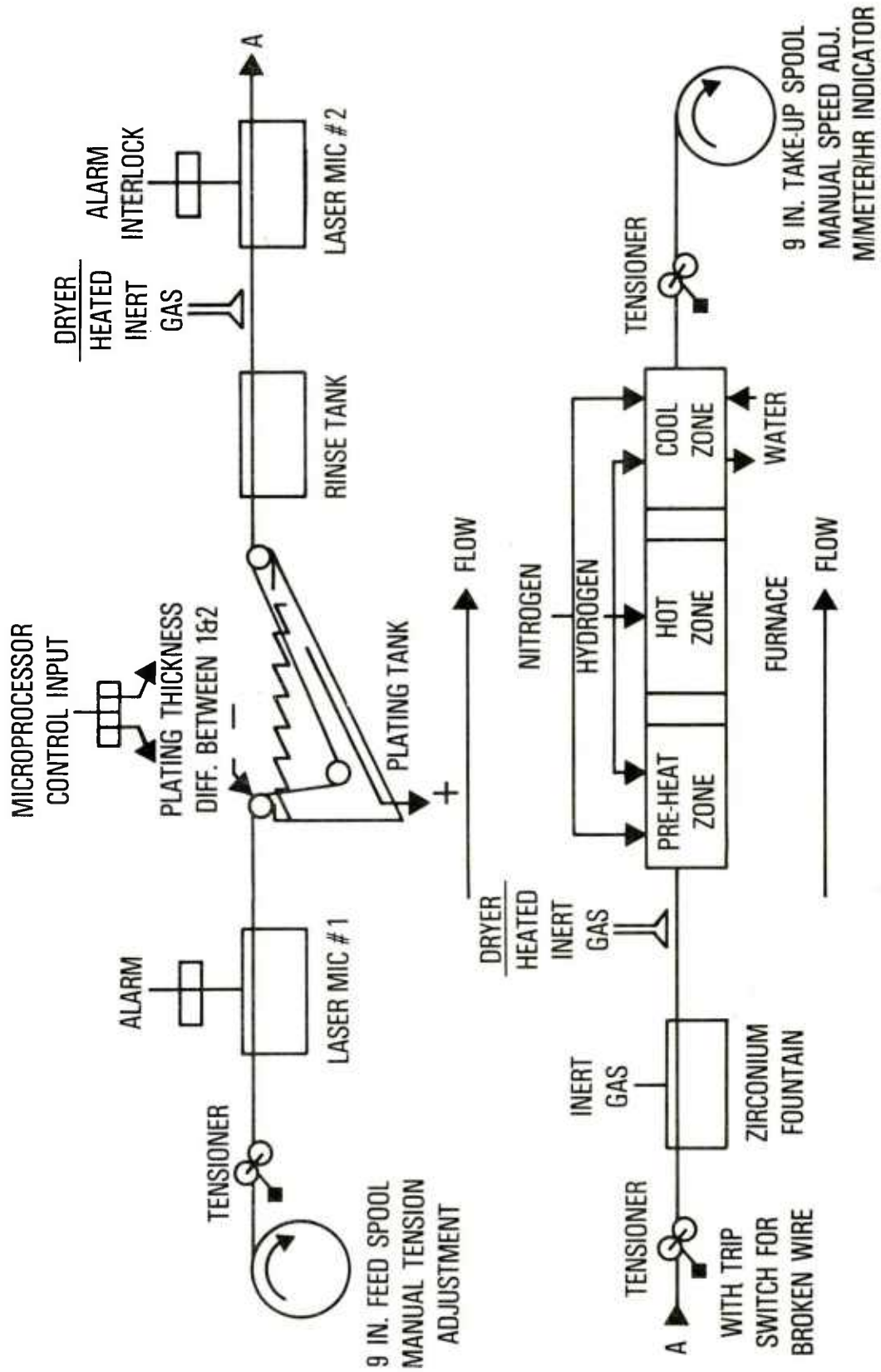


Figure 7

Proposed Coating Operation

# PROPOSED WIPING AND INSPECTION STATION

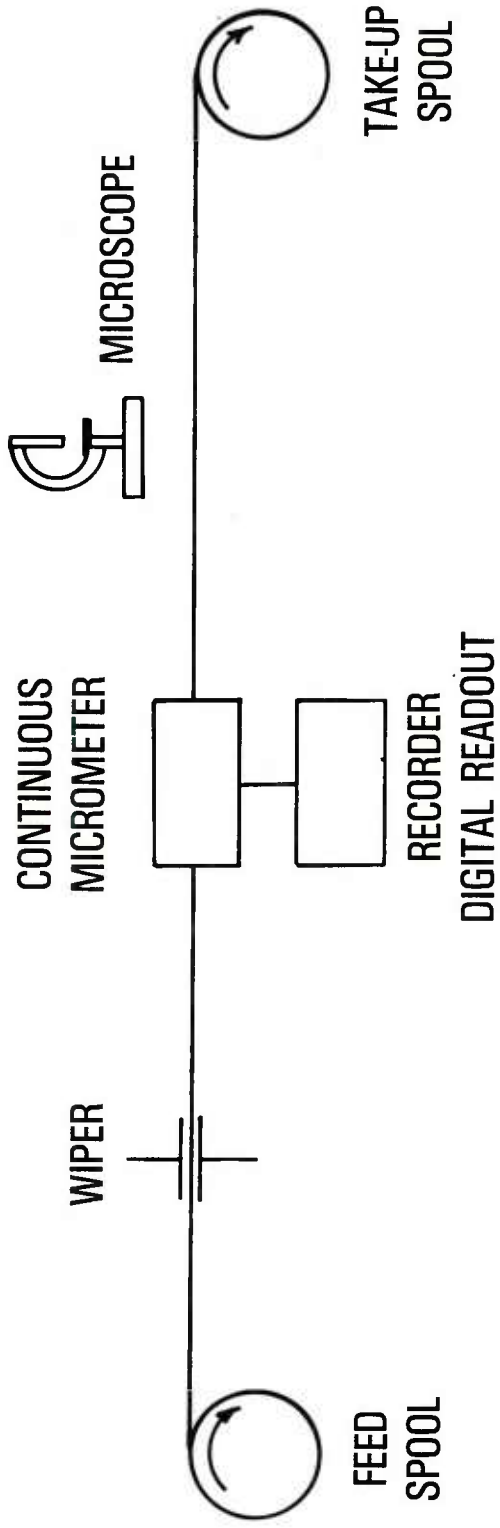


Figure 8 Proposed Spooling/Inspection Station

## SESSION III - 1

### MAJOR TRUSTS IN THE ELECTRONICS CAD/CAM PROGRAM

MR. FREDERICK MICHEL

MR. GILBERT WAGNER

OFFICE OF MANUFACTURING TECHNOLOGY

US ARMY DEVELOPMENT AND READINESS COMMAND

Mr. Fred Michel explained that his recent promotion to Chief of the Manufacturing Technology Division and other duties required him to ask Mr. Gilbert Wagner to manage the Electronics CAD/CAM working group. Mr. Wagner then stated that the group reviewed twelve FY83 project proposals and determined that ten met the definition for computer aided design and manufacture: The work must involve a manufacturing process, a means to monitor one or more parameters, a microprocessor or minicomputer to measure the parameter against a standard, and a feedback system to control and treat the process.

Mr. Wagner reported that ten projects met the criteria and were coordinated among Army, Navy and Air Force participants. No apparent duplication was found among the seven Army, three Air Force and single Navy proposals. The Major tri-Service thrusts consist of a multi-year contract with Battelle Labs, Columbus, Ohio, to develop a Master Plan outlining areas requiring further DOD attention in this technology. Current activity is described in the following paper.

## SESSION III - 2

### ELECTRONICS COMPUTER AIDED MANUFACTURING

#### ABSTRACT

The objective of the ECAM program is to produce a MASTER PLAN for government investment in technology development to support computer-aided design, manufacture and test of electronic equipment. This Plan, when completed, will be used to assist in managing the Army, Navy, and Air Force Manufacturing Technology programs in electronics over the next few years. The implementation of the programs will lead to improved productivity, reduced system costs, improved surge capacity and improved product quality.

The MASTER PLAN will include descriptions of specific technology development projects to be undertaken, approximate costs and duration, relative priorities of the projects, time phasing of projects, implementation requirements, and recommended labor requirements. The electronic commodities to be addressed are integrated circuits, wire wound components, printed wiring boards, panels covers and chassis, cables and harnesses, hybrid microelectronics, and electronic assemblies.

The PLAN is being developed by a broad coalition of military electronics manufacturers in cooperation with Battelle's Columbus Laboratories. These are:

- o AULT, INC
- o BOEING
- o COMPUTERVISION
- o GENERAL DYNAMICS
- o HONEYWELL
- o HUGHES AIRCRAFT
- o IBM
- o MAGNAVOX
- o MCDONNELL DOUGLAS  
ELECTRONICS
- o MICROELECTRONICS  
ENGINEERING CORP.
- o RCA GOVERNMENT SYSTEMS
- o ROCKWELL INTERNATIONAL
- o TECH TRAN CORPORATION

The MASTER PLAN will be developed by comparing fully automated factory models to the current state of the art and generating a list of the technology developments required to achieve the fully automated factories. The list will be prioritized, costed, and evaluated for risk, resource requirements and government return on investment.

The management challenge is to coordinate the activities of the Battelle personnel, 13 subcontractors and other members of the technical community so as to emerge with an industry consensus on the effort required to fully automate the design manufacturing and test functions within the defense electronics industry.

The program has a 19 month duration terminating in 1982.

# ELECTRONICS COMPUTER AIDED MANUFACTURING

by

Carl R. Soltesz  
Battelle Columbus Laboratories  
Columbus, Ohio

## Introduction

Automation and computer control have been used extensively in the manufacture of high volume consumer products. They have been applied to a much lesser extent to the manufacturing of military equipment because of the low production volumes involved. As a result, little work has been done on integration of the design and manufacturing processes. The automation and integration of inspection and test will bring about early identification of defects and defect trends, thus minimizing the continued addition of value to a defective product. Accordingly, it appears that there were major opportunities for cost savings and quality improvement in close integration of the functions of design, manufacture, and test by means of expanded use of computers adapted to batch manufacturing of electronics.

Based on these findings, the government initiated the present Electronics Computer Aided Manufacturing (ECAM) program. The planning phase of this program is now under way under the supervision of the working group. The planning phase, a triservice supported activity, is being done by a group of contractors managed by the U.S. Army Missile Command. In this paper, major emphasis will be on this planning phase and its expected products.

## Objective

The objective of the present study is to produce a MASTER PLAN for government investment in technology development to support computer aided design, manufacture and test of electronic equipment. This plan, when completed, will be used to assist in managing the Army, Navy, and Air Force Manufacturing Technology programs in electronics over the next few years. The implementation of the programs will lead to improved productivity, reduced system costs, shorter lead time, improved surge capacity and improved product quality.

The MASTER PLAN will include descriptions of specific technology development projects to be undertaken, approximate costs and duration, relative priorities of the projects, time phasing of projects, implementation requirements, and recommended labor requirements. The electronic commodities to be addressed are integrated circuits, wire wound components, printed wiring boards, panel covers and chassis, cables and harnesses, hybrid microelectronics, and electronic assemblies.

### Approach

The PLAN is being developed by a broad coalition of military electronics manufacturers coordinated by Battelle's Columbus Laboratories, the prime contractor.

The MASTER PLAN will be developed by (1) analyzing and describing present practices in design, manufacture, and test for each commodity, (2) developing conceptual designs of future, fully automated facilities for design, manufacture, and test for each commodity, (3) determining the new technology required to realize those fully automated facilities, and (4) development of a recommended plan for developing the required technologies.

The program has a 19-month duration, starting in May 1981, terminating in December 1982.

### The Coalition

Battelle formed the coalition, under guidelines set forth by MICOM, to be broadly representative of the U.S. military electronics manufacturing industry. It is important to have representation from major aerospace contractors from electronic equipment suppliers, from specialty firms, and from academia. It is also important that the coalition members be interested in the objectives of the program and who are able to work closely together to produce the required products. It is obviously desirable to have firms currently employing advanced CAD, CAM, and CAT techniques. Furthermore, it is necessary to have several organizations with expertise in each of the commodities specified for the program.

During the program, Battelle plans to make use of a coalition of fifteen organizations involved in design, manufacture, and test of military electronics and three universities.

These organizations are listed below in alphabetical order.

Auburn University

Ault, Inc.

Boeing Military Airplane Company and  
Boeing Aerospace Company

Computervision

General Dynamics Electronics Division and  
Stromberg-Carlson Corporate Division

General Electric Corporate Consulting Services

Honeywell Avionics Division

Hughes Missile Systems Group,  
Electro-Optical and Data Systems Group,  
Industrial Electronics Group, and the  
Government Systems Group

International Business Machines Federal Systems Division

Magnavox Government and Industrial Electronics Company

McDonnell Douglas Electronics Company

Microelectronics Engineering Corporation

Ohio State University

RCA Government Systems Division

Rockwell International, Missile Systems Division,  
Interconnect Systems Division, and  
Collins-Rockwell Division

The University of Alabama

The activity areas for each of the coalition members are indicated in Figure 1.

### Program Organization

The program is organized around the electronic commodities, with provision for integration, coordination, and support. The program structure is shown in Figure 2. The principal elements are seven commodity groups, the Integration Group, and the Advisory Group.

	INTEGRATION	ADVISORY	PANELS, COVERS	CABLE & HARNESS	PRINTER WIRING BOARD	I. C.	HYBRID	WIRE-WOUND	ASSEMBLIES	SUPPORT SYSTEMS	DATA BASE
AULT								●			
BOEING	●	●		x	●				●		
COLLEGE CAD/CAM	●										
COMPUTERVISION	●										
GD	●				●			x		x	●
GE	●										
HONEYWELL	●	●		●					x	●	
HUGHES	●	●	●	●	x	x	x	●	●	●	x
IBM	●	●		●	●	●	●		●	●	●
MAGNAVOX	●	●				●	●		●		
McDONNELL DOUGLAS	●	●	●		●	●			●		
MEC						●	●				
RCA	●	●		●						●	
ROCKWELL	●	●	x		●		●		●	●	●

- - Indicates participation
- x - Indicates technical leadership

FIGURE 1. ACTIVITY AREAS OF COALITION MEMBERS

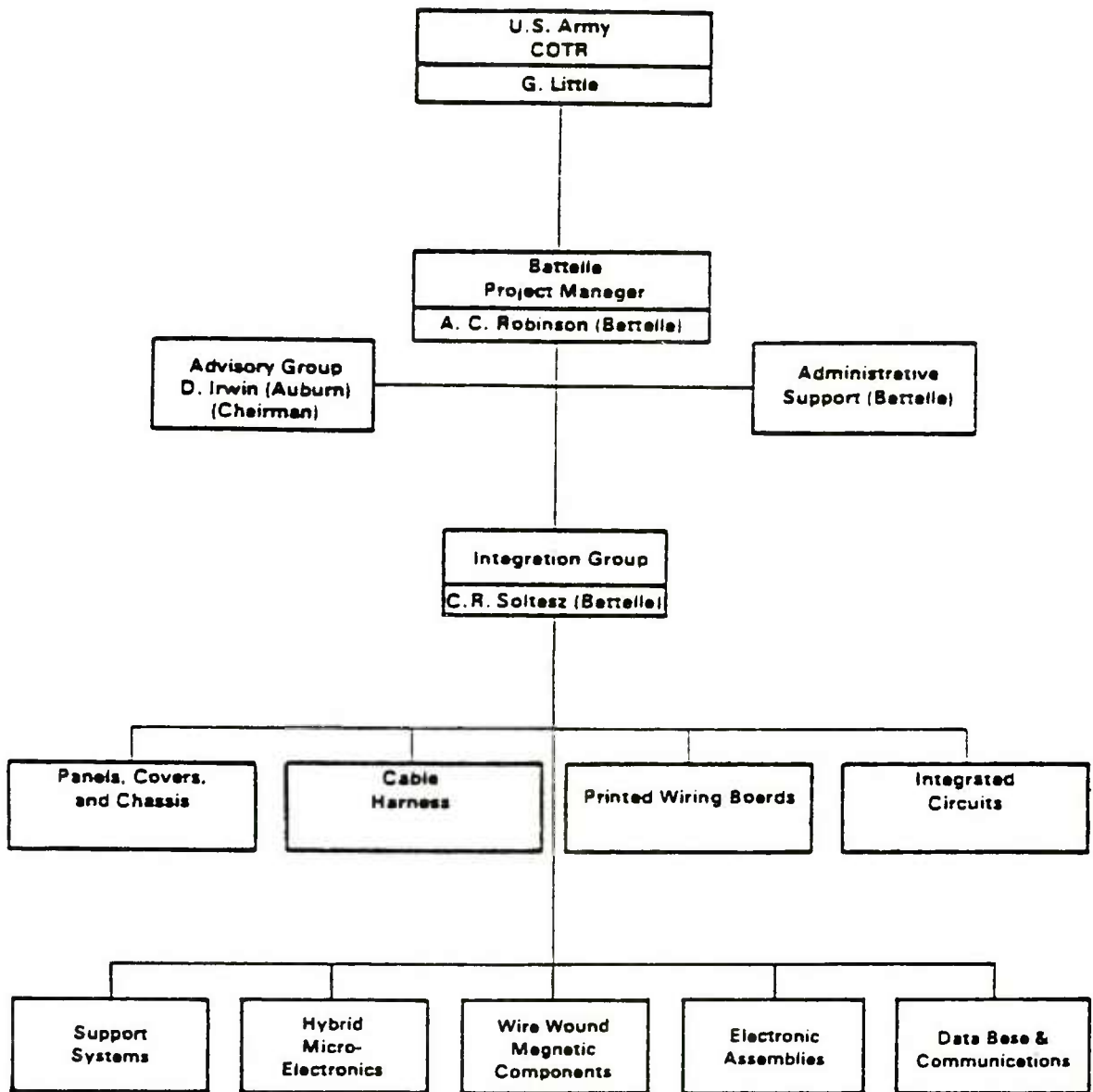


FIGURE 2. PROJECT ORGANIZATION

The Battelle Program Manager has overall responsibility for quality of results, schedule compliance, cost control and the technical deliverables. The Advisory Group is composed of representatives of top management from the major electronic manufacturing members of the coalition companies. This group will meet several times during the program to review activities from the standpoint of the electronics industry corporate management. The Integration Group will consist of ECAM Project Managers from the major electronics manufacturing companies along with certain cross-commodity specialists whose interests include human factors, group technology, data base management, technology transfer, system reliability, and software. The responsibilities of the Integration Group will include: (1) monitoring and integrating activities of the Commodity Groups, (2) ensuring that the entire program makes full use of the results of related work done elsewhere, and (3) carrying out those tasks that cut across commodity lines, especially the preparation of the MASTER PLAN.

The electronic commodities activities have been allocated to Commodity Groups. Each Commodity Group will be concerned with design, manufacture, and test for the commodity. Each group will be involved in developing the "AS IS" architecture, the "TO BE" architecture and proposing elements for the MASTER PLAN.

### Project Plan

The program has been divided into 4 tasks: (1) organize the coalition and prepare a program plan for operation, (2) analyze the current state of the art by use of the Air Force's IDEF methodology and create "AS IS" architecture (current practice description), (3) generate future factory functional models; "TO BE" architectures, and develop a list of technologies required for realization of the future factories, and (4) create the MASTER PLAN for government investment to develop those technologies which will result in the implementation of the computer aided manufacturing of electronics.

Full use will be made of related past and ongoing work including: (1) Manufacturing Technology projects of all three services, (2) the Air Force Integrated Computer Aided Manufacturing (ICAM) program, (3) the NASA Integrated Program for Aerospace-Vehicle Design (IPAD) program, and (4) company-funded CAD, CAM, and CAT projects, insofar as information can be made available.

In particular, substantial use will be made of the architectures of design and manufacture as developed under the ICAM program. Much of the project work will make use of the IDEF methodologies developed in the same program. Training courses

covering these methodologies will be provided for all project personnel.

### Project Results

The principal results to be obtained from the current phase are:

- "AS IS" Architectures. These are descriptions of current practice in design, manufacture, and test for each commodity. These descriptions will represent an integration of the coalition members' approaches and will be portrayed in IDEF<sub>0</sub> (one of the ICAM methodologies).
- "TO BE" Architectures. These will be descriptions (also using IDEF<sub>0</sub>) of future, fully automated factories, including some definition of the mechanisms to be utilized. There will be at least one such architecture for each commodity.
- The MASTER PLAN. This will consist of (1) a recommended group of project descriptions and (2) rationale for selection of these projects and priorities, project groupings and other relationships between projects. The project descriptions will include an outline of objectives, approximate cost and duration, possible technical approaches and type of organization best suited to carry out the development.

### Concluding Remarks

The overall objective of the ECAM program is very ambitious: it is to make a major improvement in the manufacture of military electronics equipment through a thoroughgoing application of computers and advanced automation. The present planning phase is being done in cooperation with the manufacturing industry. This approach to planning is itself a significant innovation. It may be five to ten years before we see major effects of this plan on the factory floor, but when we do see these effects they will be revolutionary.

## SESSION III - 3

### AIR FORCE ICAM "MANUFACTURING COST DESIGN GUIDE" FOR ELECTRONICS

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Cedar Rapids, Iowa

#### ABSTRACT

A "Manufacturing Cost/Design Guide (MC/DG) for Avionics" is under development for the Computer Integrated Manufacturing Branch (AFWAL/MLTC), Materials Laboratory, Wright-Patterson AFB, Ohio. The MC/DG is being developed by a team: Battelle's Columbus Laboratories (BCL), as prime contractor, Honeywell, Inc., and Rockwell International's Collins Avionics and Missile Group. Lockheed-California is participating in a critique role.

The data analysis methodologies established for the "MC/DG for Airframes" are being employed. General and detailed ground rules are required. These include specifications of electronic discrete parts, designer-influenced cost elements (DICE), materials, assemblies, manufacturing methods, etc. Examples of assemblies are power supplies, hybrids, and chassis. Examples of discrete parts are substrates and printed wiring boards.

An overview of the aerospace electronic design processes is given, indicating how the MC/DG will be utilized to conduct trade studies at both the conceptual and detailed design phases for circuitry and chassis. The paper discusses the manufacturing cost data requirements to achieve affordable performance in avionic systems. The data is provided to designers using MC/DG formats and these enable cost-trade studies to be conducted with little impact on scheduling.

ELECTRONICS

MANUFACTURING COST/DESIGN GUIDE  
(MC/DG)

KEY PARTICIPANTS

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AFWAL, WRIGHT PATTERSON AFB

COALITION PROGRAM MANAGER: BRYAN R. NOTON  
BATTELLE COLUMBUS LABORATORIES

SUBCONTRACTORS

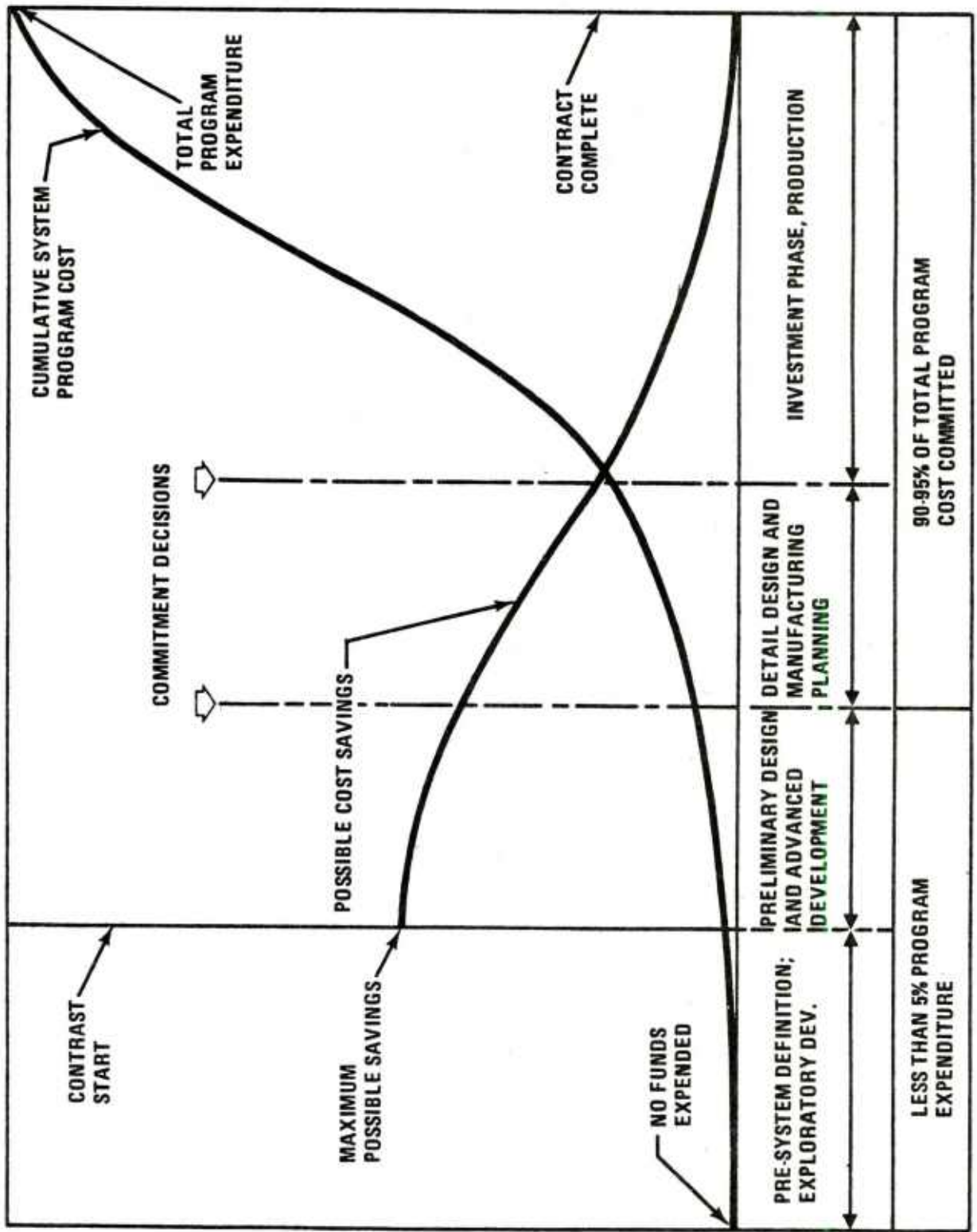
	<u>PROGRAM MANAGER</u>	<u>PROJECT ENGINEERS</u>
ROCKWELL INTERNATIONAL CORPORATION AVIONICS & MISSILES GROUP COLLINS AVIONICS DIVISION	J. G. VECELLIO	J. A. MARTIN J. W. DONALDSON
HONEYWELL, INCORPORATED AVIONICS DIVISION	R. REMSKI	D. E. LUTZ G. L. GRAVES

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MATERIALS LABORATORY, AFWAL/MLTC

AIR FORCE WRIGHT AERONAUTICAL LABORATORIES  
WRIGHT PATTERSON AIR FORCE BASE, OHIO 45433

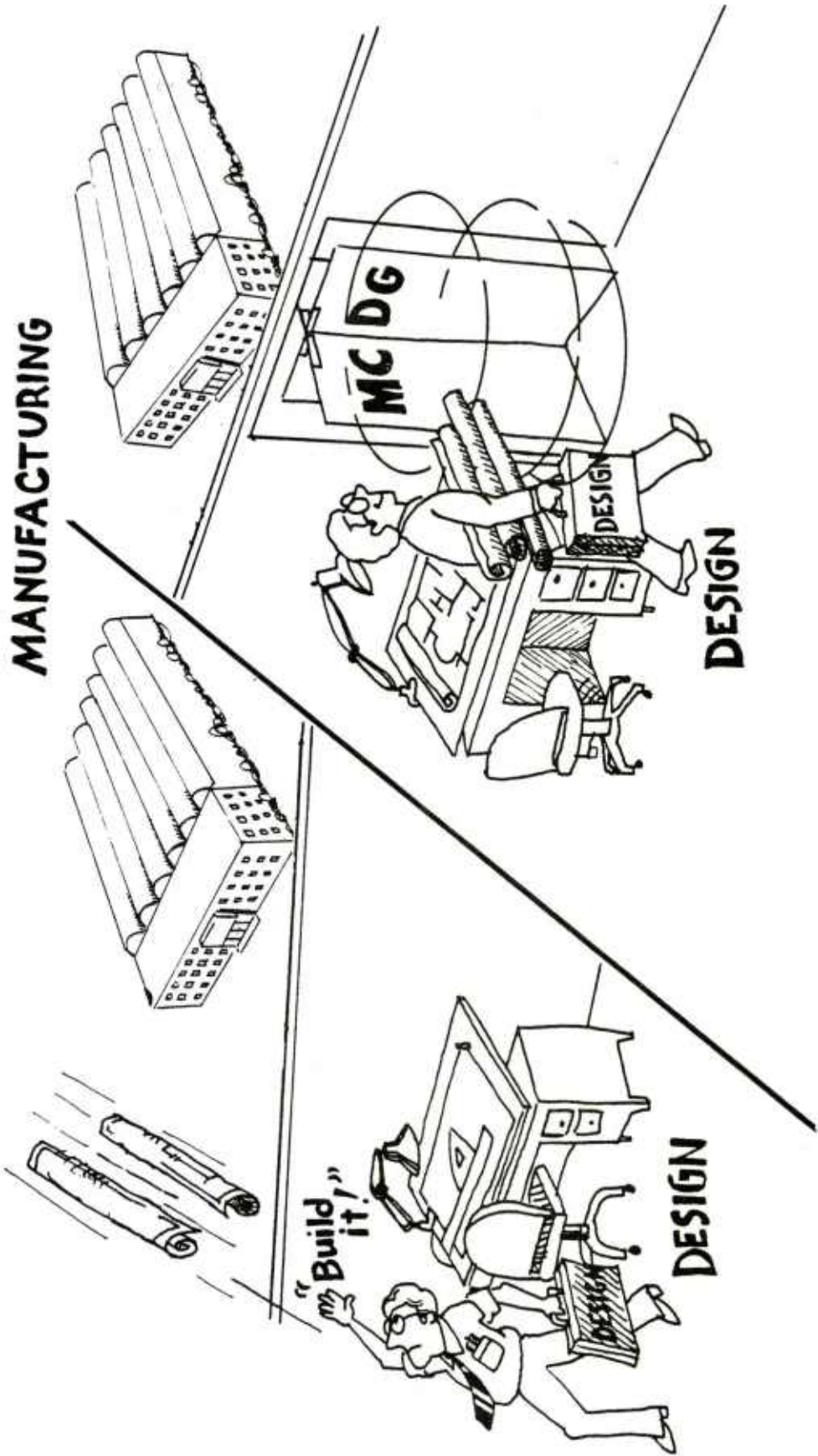
CONTRACT NO. F33615-79-C-5102

# DECREASING COST-SAVINGS LEVERAGE AS PROGRAM PROGRESSES



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COST \$

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⏏  
TIME



## **MC/DG FOR ELECTRONICS**

### **PROBLEMS**

- **NECESSARY TO ARREST AND REDUCE COSTS AT ALL LEVELS OF ELECTRONIC SYSTEMS**
- **IN TODAY'S ENVIRONMENT, THE MAJOR THRUST OF DESIGNERS IS TO DESIGN SYSTEMS WITH LITTLE OR NO EMPHASIS ON PRODUCTION COSTS**
- **DESIGNERS DO NOT HAVE A WORKING KNOWLEDGE OR AVAILABLE USEFUL REFERENCES RELATIVE TO PRODUCTION COSTS**
- **DESIGNERS CANNOT PERFORM THEIR OWN TRADE-STUDIES BY DEVELOPING THEIR OWN COST DATA TO REVISE COST EFFECTIVE DESIGNS**
- **SCHEDULED CONSTRAINTS DO NOT ALLOW REITERATIONS OF DESIGN CONFIGURATIONS TO IMPLEMENT COST REDUCTIONS**

## **MC/DG FOR ELECTRONICS**

### **MC/DG HELPS SOLVE THESE PROBLEMS**

- **PROVIDES DESIGNERS WITH AVAILABLE AND USABLE INFORMATION RELATING TO PRODUCTION COSTS**
- **INSTALLS A COST AWARENESS TO BOTH EXPERIENCED AND INEXPERIENCED DESIGNERS**
- **ASSURES THAT DESIGNERS WILL GET ON THE LOWEST PRODUCTION COST TRACT EARLY IN THE DESIGN SCHEDULE**
- **ENABLES DESIGNERS TO PERFORM TRADE-STUDIES INVOLVING ALTERNATIVE CONFIGURATIONS AND IDENTIFYING THE MOST COST EFFECTIVE DESIGN APPROACH**

MC/DG FOR ELECTRONICS

PRIMARY TASKS IN DEVELOPMENT OF MC/DG

- DEVELOP GLOSSARY TO IMPROVE COMMUNICATION
- DEVELOP OUTLINE OF CONTENTS FOR MC/DG
- DEVELOP GENERAL AND DETAILED GROUND RULES
- PREPARE SKETCHES FOR PARTS AND ASSEMBLIES
- PREPARE OPERATIONAL SEQUENCES FOR FABRICATION AND ASSEMBLY PROCESSES
- SPECIFY DETAILED DATA DEVELOPMENT PROCEDURES AND PREPARE DATA COLLECTION FORMS
- CONDUCT PILOT RUN FOR MANUFACTURING MAN-HOUR DEVELOPMENT FOR A SELECTION OF LOT SIZES

## **MC/DG FOR ELECTRONICS**

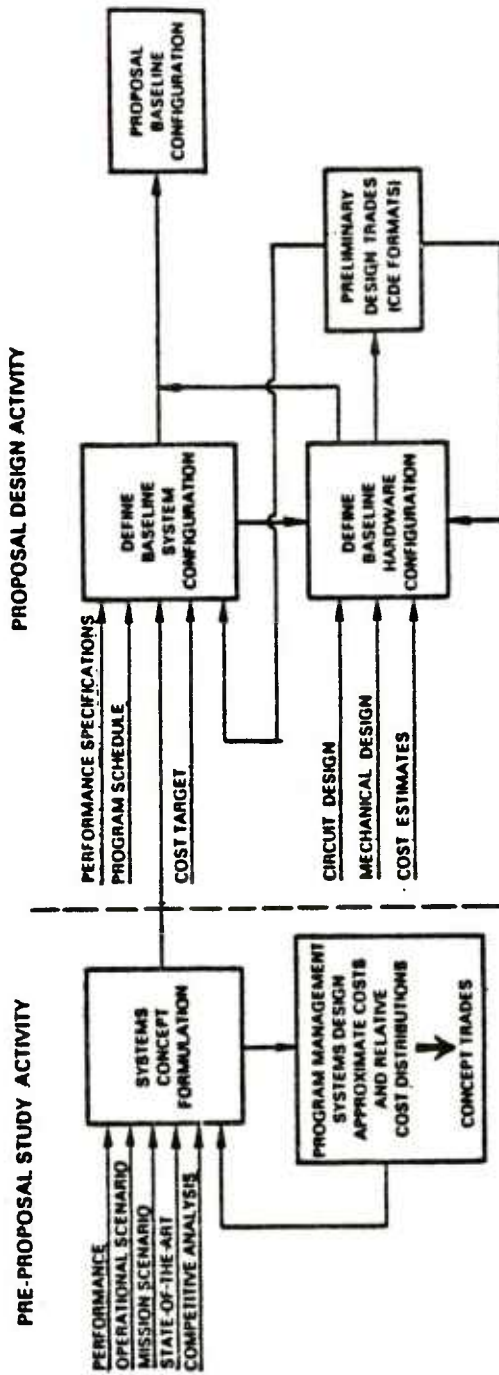
### **OBJECTIVES OF THE MC/DG**

- **PROVIDE SIMPLE COST COMPARISONS**
- **EMPHASIZE DESIGN ORIENTATION OF MC/DG FORMATS**
- **EMPHASIZE POTENTIAL COST ADVANTAGES OF EMERGING MATERIALS AND MANUFACTURING METHODS**
- **PUT ELECTRONIC DESIGNERS ON LOWEST COST TRACK**
- **IDENTIFY MANUFACTURING COST DRIVERS**

**MC/DG VOLUME CONTENTS: "MANUFACTURING TECHNOLOGIES FOR  
AEROSPACE ELECTRONIC FABRICATION, ASSEMBLY, AND TEST"**

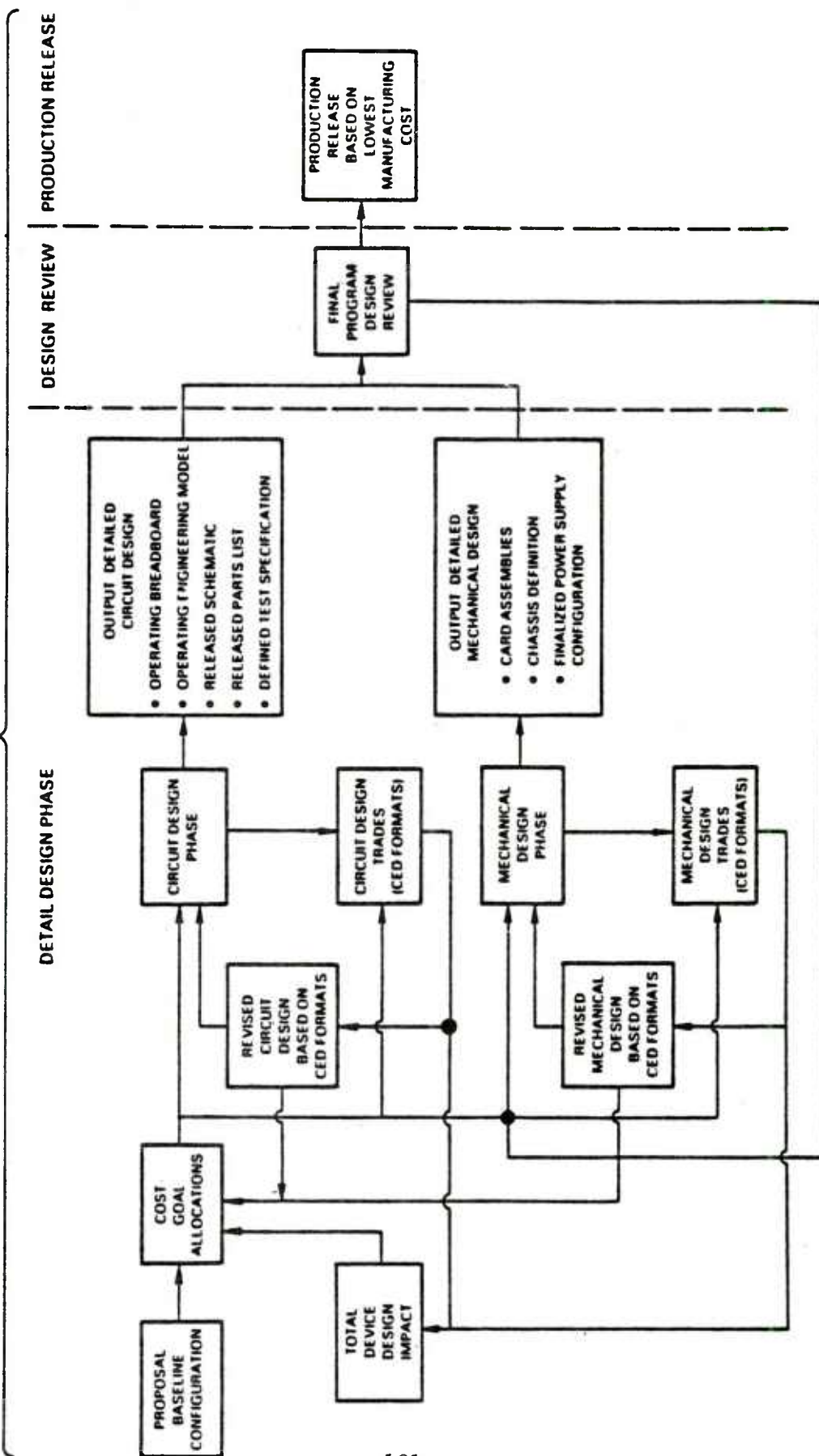
I	II	III	IV	
PROCURED ITEMS	DETAIL FABRICATION	ASSEMBLY		
<u>Schematic Parts</u> <ul style="list-style-type: none"> <li>• Electronic</li> <li>• Electromechanical</li> </ul> <u>Interconnect Parts</u> <ul style="list-style-type: none"> <li>• PWB</li> <li>• Connectors</li> <li>• Signal Interconnect               <ul style="list-style-type: none"> <li>- Wire</li> <li>- Coaxial</li> <li>- Flex Cable</li> <li>- Ribbon Cable</li> <li>- Wave Guides</li> </ul> </li> </ul> <u>Hardware</u> <ul style="list-style-type: none"> <li>• Mechanical</li> <li>• Electrical</li> </ul> <u>Fabricated Parts</u> <ul style="list-style-type: none"> <li>• Castings</li> <li>• Sheet Metal</li> <li>• Plastic Parts</li> <li>• Powdered Metal</li> <li>• Machined Parts</li> <li>• Extrusions</li> </ul> <u>Emerging Technologies</u> <ul style="list-style-type: none"> <li>• VLSI</li> <li>• Displays (i.e., liquid crystal, electroluminescent, etc.)</li> <li>• Chip Carrier</li> <li>• Fiber-optics</li> <li>• Multilayer Flex Circuit</li> </ul>	<u>Metallic</u> <ul style="list-style-type: none"> <li>• Machining</li> <li>• Forming</li> <li>• Chem-milling</li> </ul> <u>Nonmetallic</u> <ul style="list-style-type: none"> <li>• Molding</li> <li>• Laminating</li> <li>• Machining</li> <li>• Forming</li> </ul> <u>Treatment/Coating/Marking</u> <ul style="list-style-type: none"> <li>• Anodize</li> <li>• Paint</li> <li>• Silk Screen</li> <li>• Plating</li> </ul> <u>Emerging Technologies</u> <ul style="list-style-type: none"> <li>• Laser Welding</li> <li>• Net Shape</li> <li>• Robotics</li> </ul>	<u>Mechanical Assembly</u> <ul style="list-style-type: none"> <li>• Connectors</li> <li>• Hardware</li> </ul> <u>Component Assembly (Pre-Wave and Post-Wave)</u> <ul style="list-style-type: none"> <li>• Automatic</li> <li>• Manual</li> <li>• Semiautomatic</li> </ul> <u>Cleaning</u> <ul style="list-style-type: none"> <li>• Hand</li> <li>• Flow</li> <li>• Vapor Phase</li> <li>• Oven</li> <li>• Induction</li> <li>• Infrared</li> </ul> <u>Solder</u> <ul style="list-style-type: none"> <li>• Sheet Metal/Standoff Assembly (Hard Wiring)</li> <li>• Standoff Insertion</li> <li>• Part Assembly</li> <li>• Interconnect</li> </ul> <u>Cable/Wire Harness Assembly</u> <ul style="list-style-type: none"> <li>• Coaxial</li> <li>• Wire Bundles</li> <li>• Ribbon Cable</li> </ul>	<u>Hybrids</u> <p><u>Other Assembly Techniques</u></p> <ul style="list-style-type: none"> <li>• Multi-Wire</li> <li>• Stitch Wire</li> <li>• Wire Wrap</li> </ul> <u>Chassis Assembly</u> <p><u>Final Equipment Assembly</u></p> <ul style="list-style-type: none"> <li>• Mechanical</li> <li>• Electrical</li> </ul> <u>Post-Assembly Processes</u> <ul style="list-style-type: none"> <li>• Conformal Coating               <ul style="list-style-type: none"> <li>- Masking</li> <li>- Spray/Dip/Brush</li> </ul> </li> <li>• Sealing</li> </ul> <p><u>Potting</u></p> <p><u>Adhesives</u></p> <p><u>Emerging Technologies</u></p> <ul style="list-style-type: none"> <li>• Chip Carrier</li> <li>• Chip/Epoxy</li> <li>• Robotics</li> <li>• Laser Soldering</li> </ul>	<u>Card/Module Level Test</u> <ul style="list-style-type: none"> <li>• Automatic</li> <li>• Manual</li> <li>• Calibrate</li> </ul> <u>Testability</u> <p><u>Burn-In/Screening Test</u></p> <ul style="list-style-type: none"> <li>• Automatic</li> <li>• Manual</li> </ul> <p><u>Device/Equipment Test</u></p> <ul style="list-style-type: none"> <li>• Automatic</li> <li>• Manual</li> <li>• Calibrate</li> </ul> <p><u>Emerging Technologies</u></p> <ul style="list-style-type: none"> <li>• Automated Assembly Handling</li> <li>• Improved CAD/CAM</li> <li>• CAT</li> <li>• Automatic Optical Comparison</li> <li>• Voice Control</li> <li>• Laser Inspection</li> <li>• Video Control Inspection</li> </ul>

# TYPICAL DESIGN FLOW FOR AEROSPACE AVIONICS INDUSTRY



# TYPICAL DESIGN FLOW FOR AEROSPACE AVIONICS INDUSTRY (Continued)

## FULL-SCALE ENGINEERING DEVELOPMENT CONTRACT PHASE



# MC/DG FOR ELECTRONICS

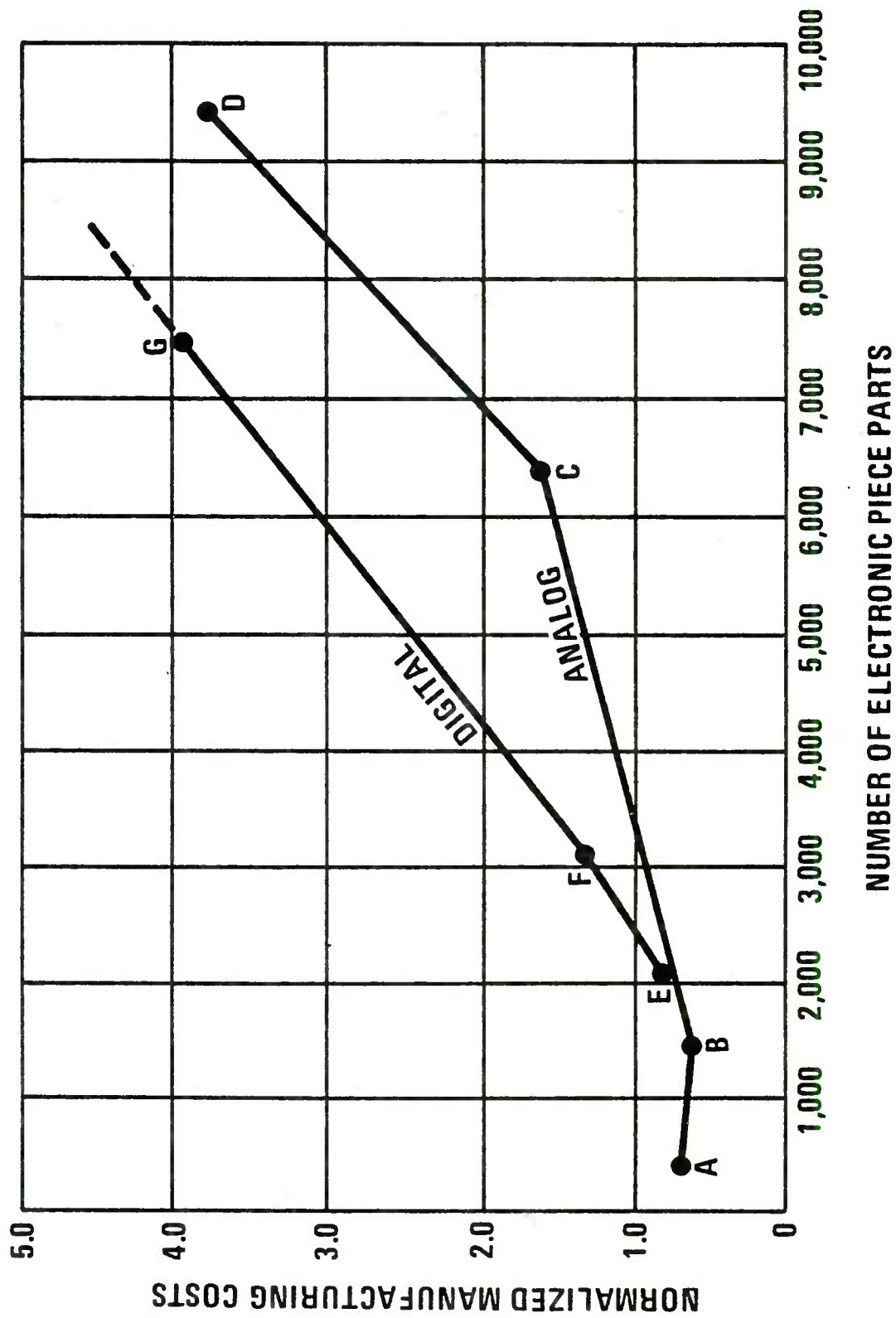
## CONCEPTUAL DESIGN TRADE STUDIES

- NEW TECHNOLOGY
- NUMBER OF ASSEMBLIES
- COMMON FUNCTIONS
- DIGITAL DESIGN
- BUILT-IN TEST
- PART COUNT

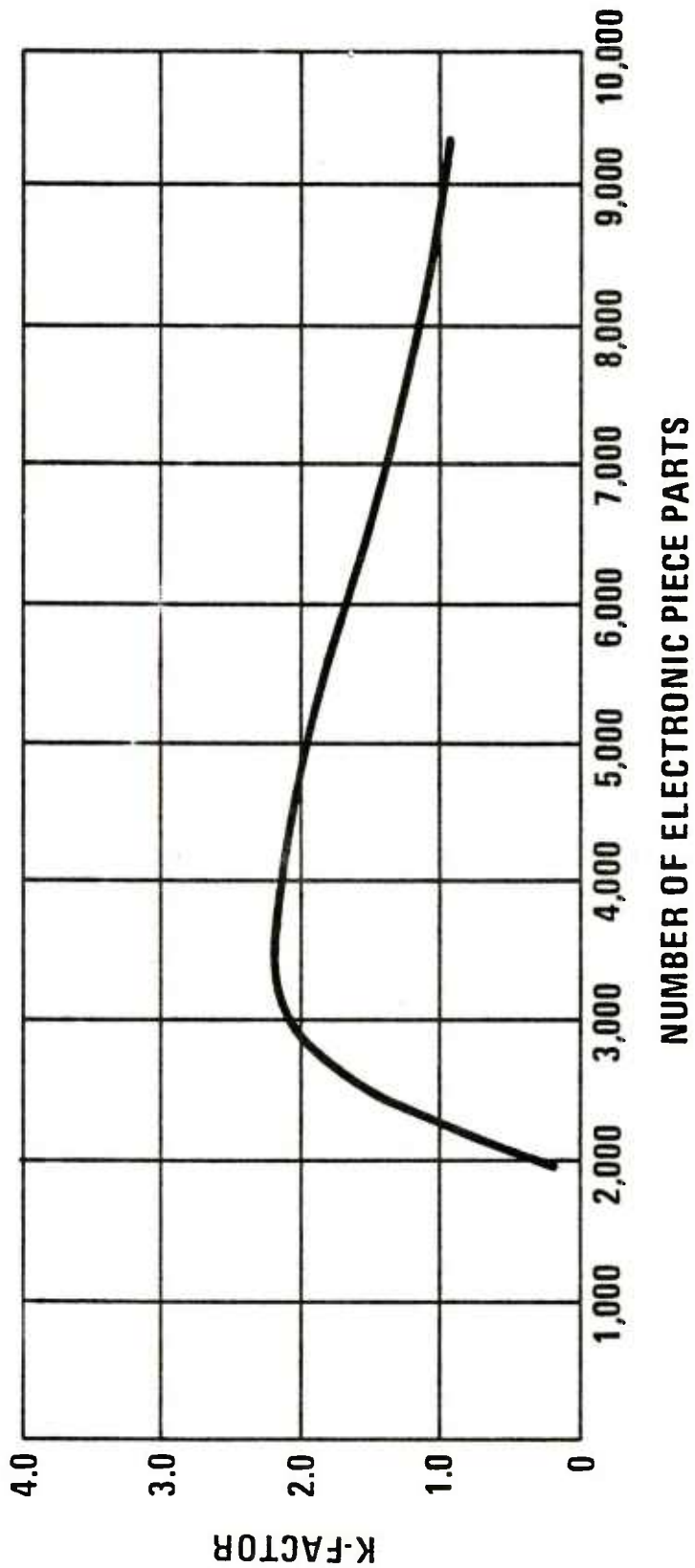
## MAJOR SECTIONS OF ELECTRONICS MC/DG

- MECHANIZATION
- PROCESSES
- INSERTION-RECURRING COSTS
- SOLDERING-RECURRING COSTS
- PART RELATIVE COST
  - PACKAGE
  - RELIABILITY

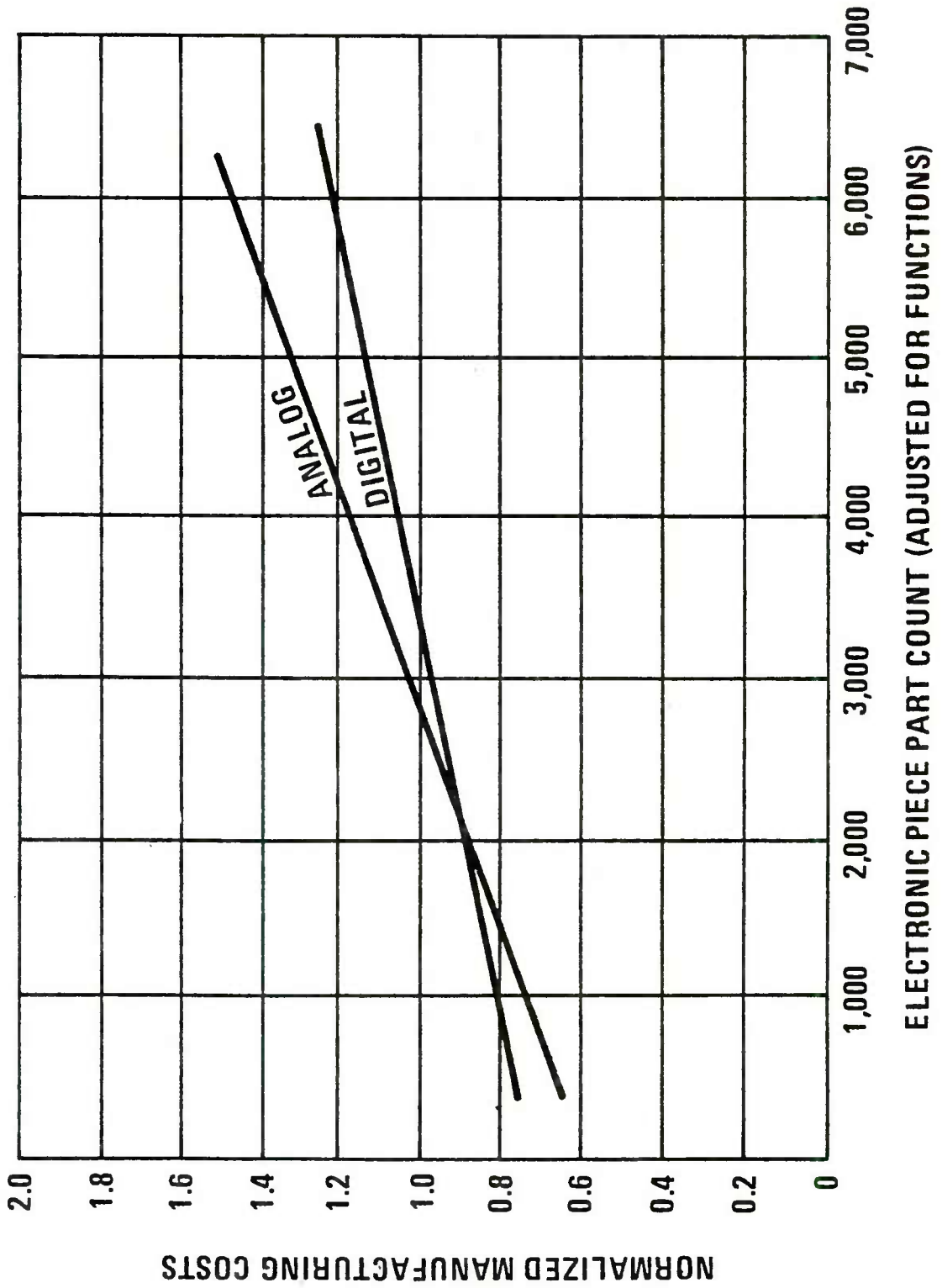
# ANALOG VS DIGITAL SYSTEMS UNADJUSTED COST DATA

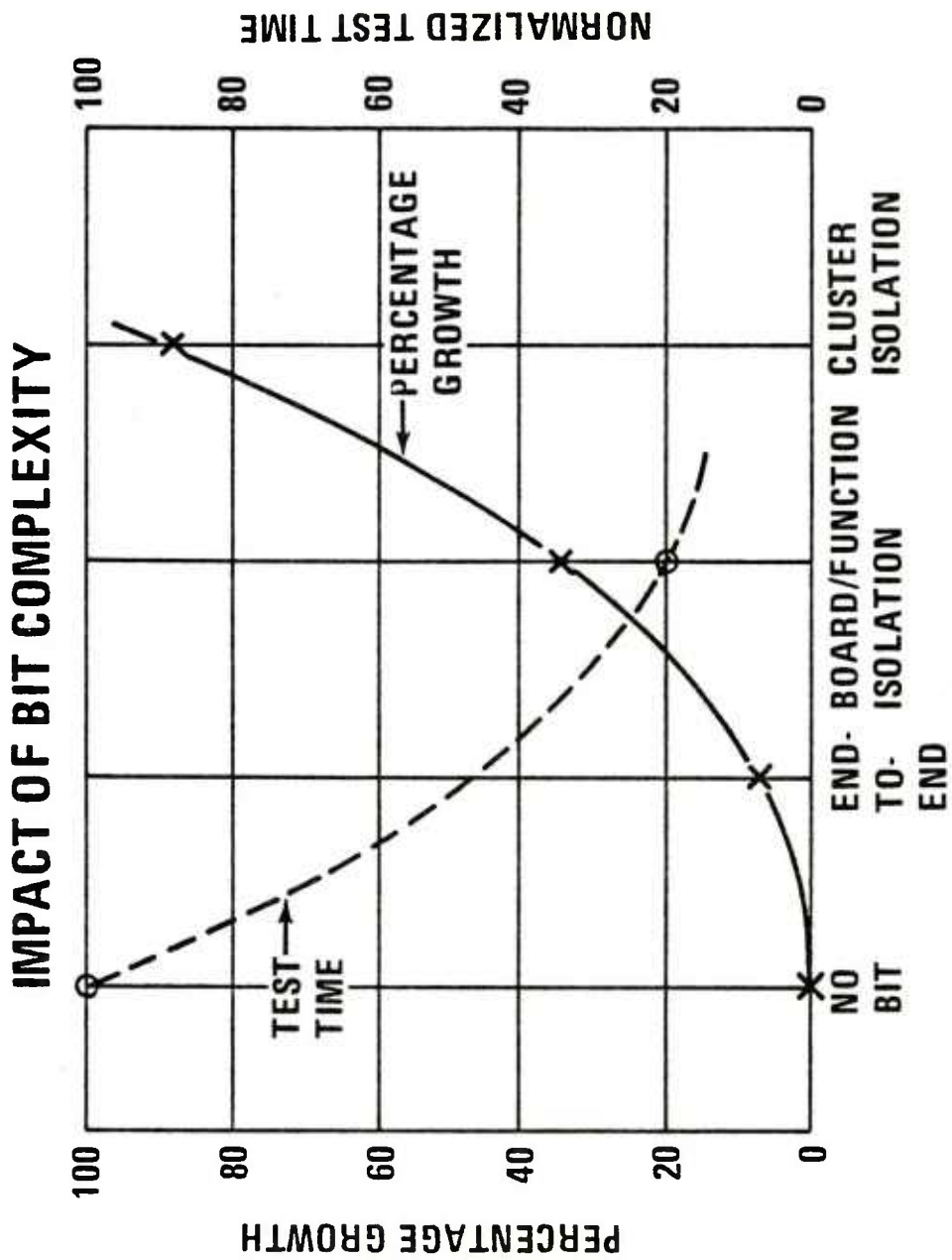


# FUNCTION ADJUSTMENT K FACTOR

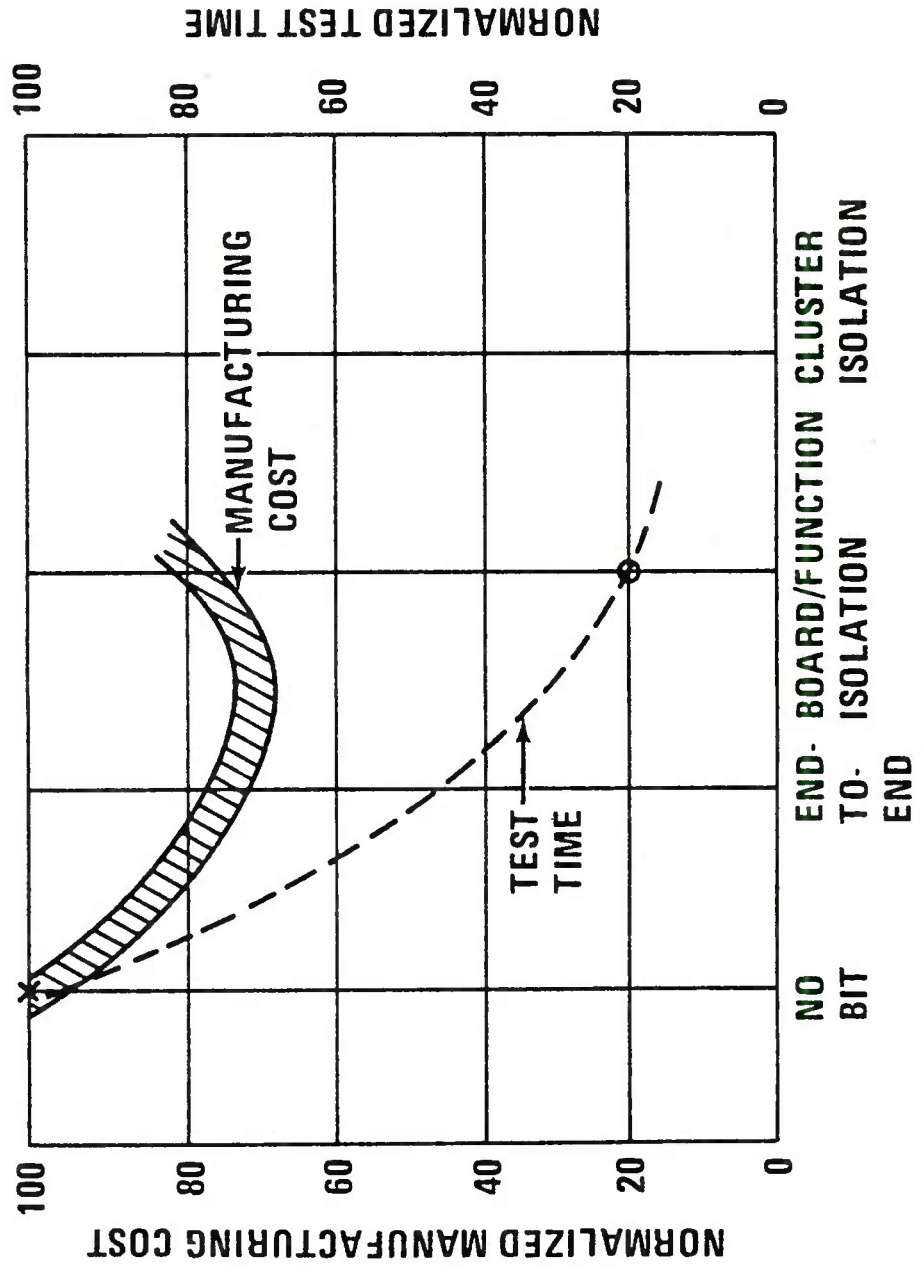


# ANALOG VS DIGITAL SYSTEMS FUNCTIONALLY ADJUSTED COST DATA





# BITE IMPACT ON MANUFACTURING COST



## INSERTION PROCESS FOR AVIONIC PARTS (PWA RELATED)

RELATIVE COST	LOW	MEDIUM	HIGH
INSERTION PROCESS	Auto	Semi-Auto	Hand
<b>PART TYPE</b>			
<b>RESISTORS</b>			
<b>Axlal Leded</b>	●	●	●
<b>DIP</b>	●	●	●
<b>SIP</b>	●	●	●
<b>Chlp</b>	●	●	●
<b>VARIABLE RESISTORS</b>			
<b>Sealed</b>	●	●	●
<b>Open</b>	●	●	●
<b>CAPACITORS</b>			
<b>Axlal Leded</b>	●	●	●
<b>Radlal Leded</b>	●	●	●
<b>DIP</b>	●	●	●
<b>SIP</b>	●	●	●
<b>Chlp</b>	●	●	●
<b>VARIABLE CAPACITORS</b>			
<b>Opened</b>	●	●	●
<b>Sealed</b>	●	●	●
<b>COILS</b>			
<b>Axlal Leded</b>	●	●	●
<b>Variable</b>	●	●	●
<b>DIODES</b>	●	●	●
<b>TRANSISTORS</b>			
<b>Standard Leded</b>	●	●	●
<b>Ribbon Leded</b>	●	●	●

● Applicable

● Applicable (May Require Special Processing/Equipment)

● Not Applicable

**SOLDERING PROCESS FOR  
AVIONIC PARTS (PWA RELATED)**

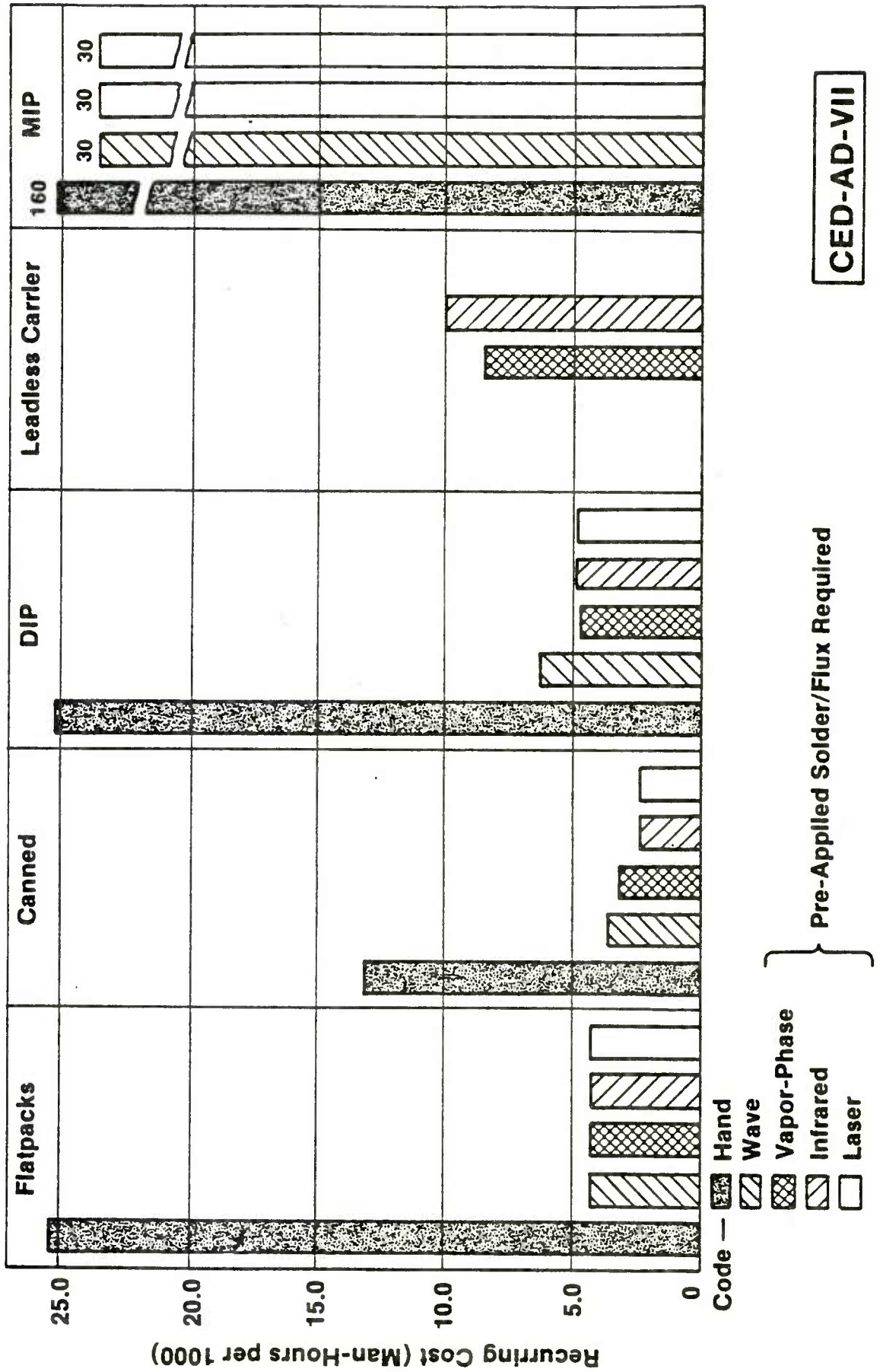
RELATIVE COST	HIGH	MEDIUM	MEDIUM	LOW	LOW
SOLDERING PROCESS	Hand	Wave	Vapor Phase*	Infrared*	Laser*
PART TYPE					
RESISTORS					
Axial Leaded	●	●	●	●	●
DIP	●	●	●	●	●
SIP	●	●	●	●	●
Chip	●	●	●	●	●
VARIABLE RESISTORS					
Sealed	●	●	●	●	●
Open	●	●	●	●	●
CAPACITORS					
Axial Leaded	●	●	●	●	●
Radial Leaded	●	●	●	●	●
DIP	●	●	●	●	●
SIP	●	●	●	●	●
Chip	●	●	●	●	●
VARIABLE CAPACITORS					
Sealed	●	●	●	●	●
Open	●	●	●	●	●
COILS					
Axial Leaded	●	●	●	●	●
Variable	●	●	●	●	●
DIODES	●	●	●	●	●
TRANSISTORS					
Standard Leaded	●	●	●	●	●
Ribbon Leaded	●	●	●	●	●

\*Pre-Applied Solder/Flux Required

- Applicable
- Applicable (May Require Special Processing/Equipment)
- Not Applicable

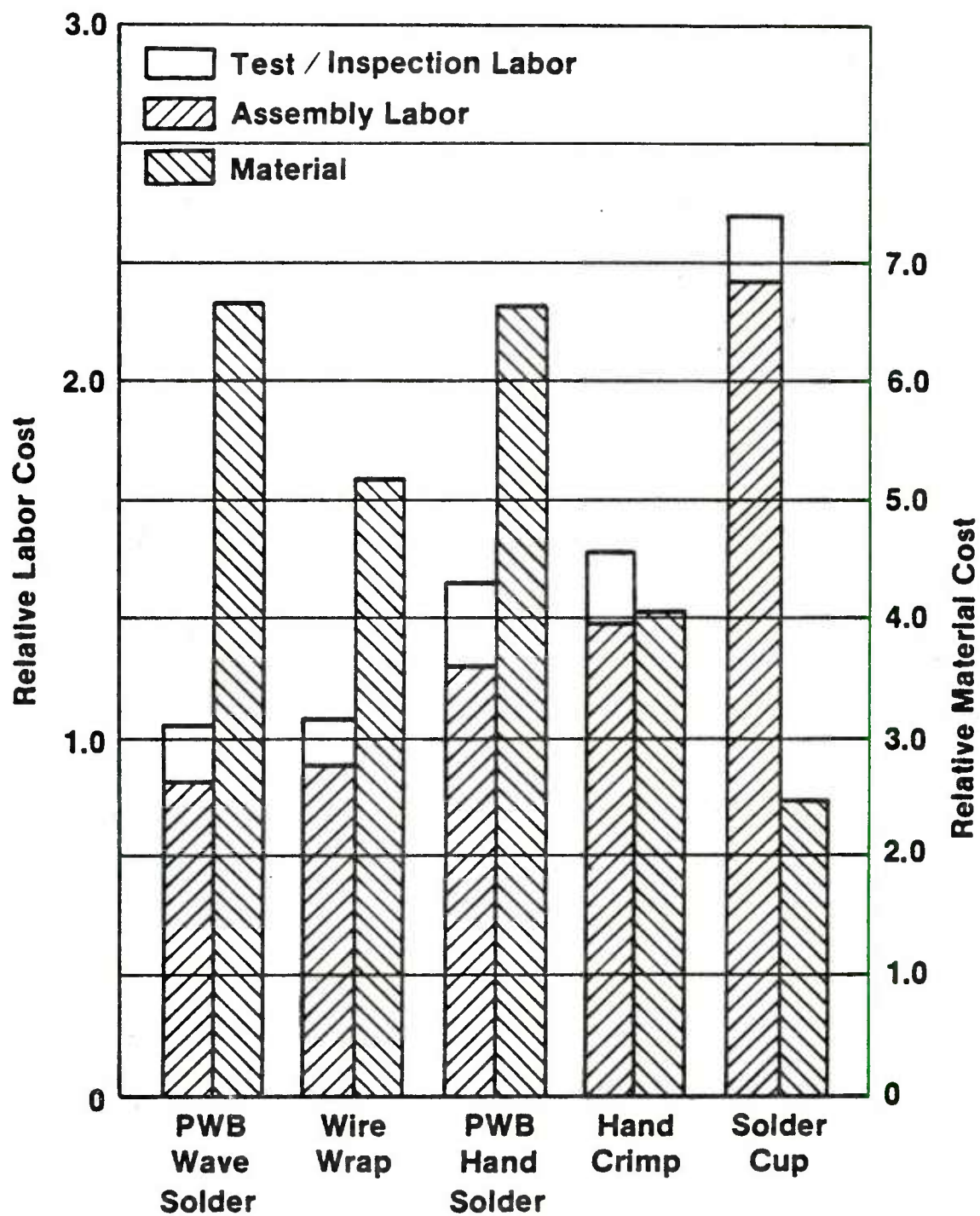
# SOLDERING PROCESS FOR AVIONIC PARTS (PWA RELATED)

## INTEGRATED CIRCUITS

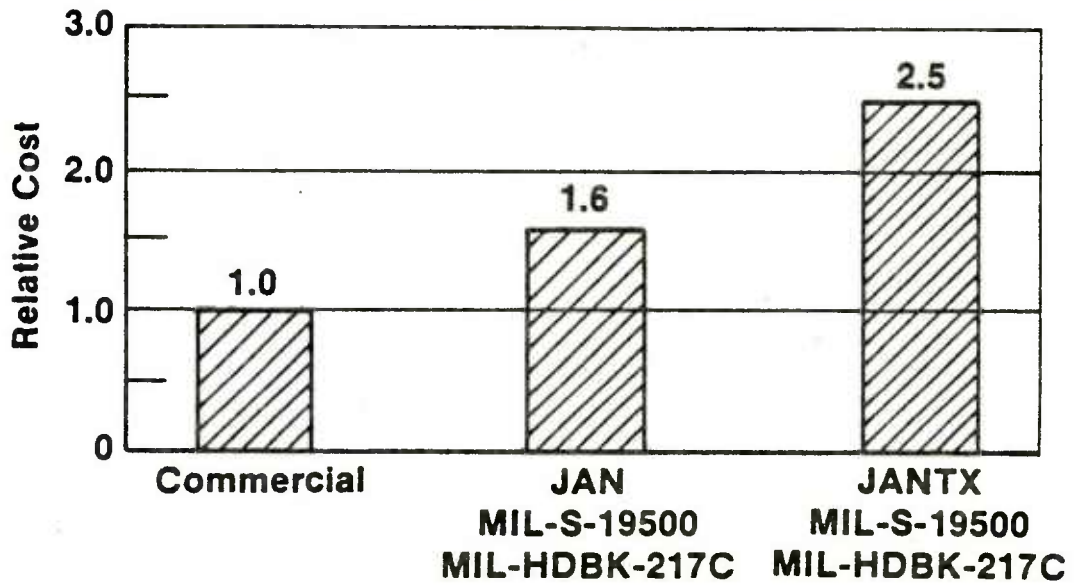


CED-AD-VII

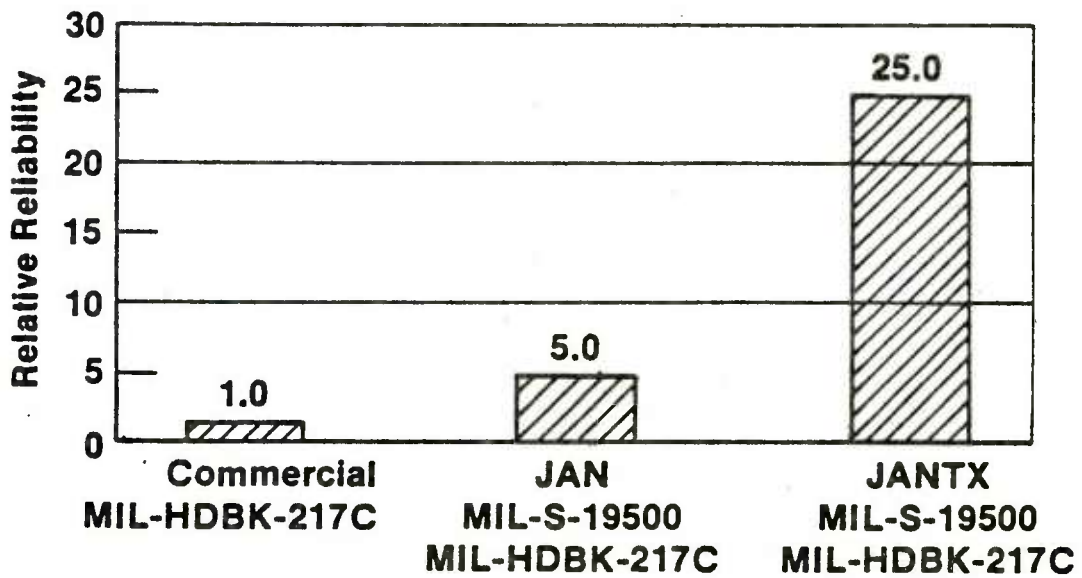
# LRU INTERCONNECTION MAN-HOURS-MATERIAL COST VS. TERMINATION TYPE



### TRANSISTOR — BIPOLAR SIGNAL



### TRANSISTOR — BIPOLAR SIGNAL



## MC/DG FOR ELECTRONICS

### MC/DG BENEFITS

- INFLUENCES DESIGN DECISIONS
- EMPHASIZES LOW COST PROCESSES
- PROVIDES QUALITATIVE/QUANTITATIVE MANUFACTURING COST DATA
- IMPARTS SENIOR DESIGNER EXPERIENCE ON NEW ENGINEERING
- DIRECT FEEDBACK OF MANUFACTURING COST IMPACT

SESSION IV - 1

# **AUTOMATED LAYOUT OF INTEGRATED CIRCUITS**

**A Project of the  
Manufacturing Technology Program**

**Naval Sea Systems Command**

**30 September 1981**



**Prepared by  
G.L. Haviland  
P.J. O'Connell  
M.L. Jones  
CDR N.C. Meck, USN**

**NAVAL OCEAN SYSTEMS CENTER  
SAN DIEGO, CALIFORNIA 92152**



NAVAL OCEAN SYSTEMS CENTER, SAN DIEGO, CA 92152

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A N A C T I V I T Y O F T H E N A V A L M A T E R I A L C O M M A N D

SL GUILLE, CAPT, USN  
Commander

HL BLOOD  
Technical Director

The work reported here was performed by members of the Micro-Electronics Technology and Applications Division under program element NSEA, project OPN-5, task area DN, and work unit 988728. The appendices were produced by CSC Corp under delivery order contract N0012379D0036.

Released by  
O. H. Lindberg, Head  
Micro-Electronics Technology  
and Applications Division

Under authority of  
P. C. Fletcher  
Electronics Engineering  
and Sciences Department

### OBJECTIVE

1. Decrease the design time and cost of custom Large-Scale Integrated (LSI) circuits applicable to military systems.
2. Improve the performance of LSI electronics and increase the reliability of LSI chips.

### RESULTS

The design tools developed can produce a 43% savings in time for custom LSI circuits. Based on a \$90M annual budget for DoD custom LSI, this corresponds to an annual saving of \$38.7M if fully implemented.

### RECOMMENDATIONS

It is recommended that the above results be disseminated to the manufacturers and users of Computer-Aided Design (CAD) systems. In addition to the publication and distribution of this report, this will be accomplished by

1. End-of-contract review presented to the NAVSEA sponsors and CAD manufacturers.
2. Generation and distribution of a videotape of the program's results.
3. Presentation of the results to CAD users' conferences.

## BACKGROUND

The rapid progress of electronics technology during the last half-century can be largely attributed to the driving force of military requirements. Large-Scale Integrated (LSI) circuits evolved out of the requirements for small size, low weight, low power, and increased reliability. Although the design cost of custom LSI is high and the time required lengthy, alternatives either cannot meet the requirements or would drive the total system cost even higher.

Recent years have given rise to a trend by the military to obtain increasingly smaller quantities of each type of system procured. The result is that systems which contain custom LSI end up costing considerably more per unit and may even become unavailable if the design costs cannot be amortized to an acceptable level. Therefore, "bargain" systems are often procured that compromise desirable reliability, size, and power requirements – all because the excessive time and/or cost involved in custom LSI circuit development.

The design and development of LSI circuits can be divided into the following categories:

1. Logic design and circuit analysis
2. Circuit layout and mask design
3. Prototype production and testing.

Circuit layout and mask design can account for up to 90% of the total design time required.

Computer-Aided Design (CAD) facilities have the capability of improving markedly on this figure. Equipment manufactured by Applicon, Calma, Computervision, and others greatly assist the designer in the circuit layout and mask design tasks. As designs get larger, such automated assistance is essential for organization support. The CAD technology is so new, however, that many of the useful facilities are left unimplemented.

The goal of this project is to develop such extensions for the purpose of decreasing circuit layout and mask design time to a point commensurate with the other phases of the design process.

## PROGRAM MANAGEMENT

The program was sponsored by the Naval Sea Systems Command (NAVSEA, Code 03542) under the direction of H. Byron. Technical support and contractual advice were provided by G. L. Haviland of NOSC Code 9252.

Throughout the project, Naval Ocean Systems Center (NOSC) has taken an active role in the specification, organization, development, and evaluation of the design effort. In addition to Mr Haviland, personnel instrumental in this task are CDR N. C. Meck, M. L. Jones, and P. J. O'Connell, all of NOSC Code 9252.

## FUNDING

The total program cost was \$590 000, with \$52 181 for Computer Sciences Corporation (CSC), \$30 035 for the University of Minnesota, \$278 504 for in-house management, and \$229 280 for equipment.

## CONTRACTOR

Computer Sciences Corporation (CSC), Applied Technology Division, San Diego, CA, was the prime contractor for this program. The period of performance was from March 1980 to September 1981.

A secondary contractor was the University of Minnesota. The period of performance is from 24 April 1981 to 15 September 1982.

## PROBLEMS WITH PRESENT METHODS

There are currently two approaches to circuit layout and mask design: (1) hand-crafted or (2) fully automated. Both are expensive and unsuitable for DoD-type LSI. With hand-crafting, an experienced, capable designer can produce a design close to optimal in terms of size, speed, and power. However, high front-end costs and long lead times make this approach prohibitive for many potential applications.

Fully automated designs suffer from another problem. Although the automated system will generate a workable design quickly (thus satisfying the front-end time and cost requirements), such systems are unimaginative and inflexible, yielding designs that are large, slow, and power-hungry. Much of the time, a circuit so designed will not satisfy the military application it was intended to fulfill.

Thus the problem is that neither of these resources is likely to be used efficiently. Either the designer is forced to perform manually many of the routine tasks, or the computer is forced to make many of the higher-level strategic decisions. Neither option results in a good design.

The design cycle, as viewed by NOSC, is shown in figure 1. In this view of the process, the design proceeds through several layers, from System through Board, Hybrid, Chip, and Architectural Macro to Cell, and then up again to System.

At each level, the design is subdivided into workable functional subsections, as many as required to perform that level's function. This can be viewed as an exercise in sequential, top-down design.

There is, however, another important criticism of the present design method. The design cycle is portrayed as a relatively static, sterile entity proceeding lock-step, from one level to the next. In reality, it is a very dynamic operation. Tradeoffs and compromises are constantly being made to better serve the overall design. The distinctions between levels become less well defined and boundaries move back and forth as interactions are better understood. (There is the recognition that no design is truly "top-down." In actuality, the only way a design could be fully top-down would be if all the answers were known ahead of time. That is, if it had been designed before; in the context of custom LSI for the DoD, this luxury obviously is not available.)

In actuality, most designs are the result of numerous passes around the design loop. For example, let us say the design has proceeded down through the partitioning, the cells have been constructed, the architectural macros have been built, and now these are being interconnected to form the chip. Let us say it is discovered at this point that the paths could not be run (for whatever reason). Depending on the severity of the problem, we might need to return to building the macro, to building the cells, to partitioning the macros, or to any previous level to resolve the difficulty. Then the design would continue until the next

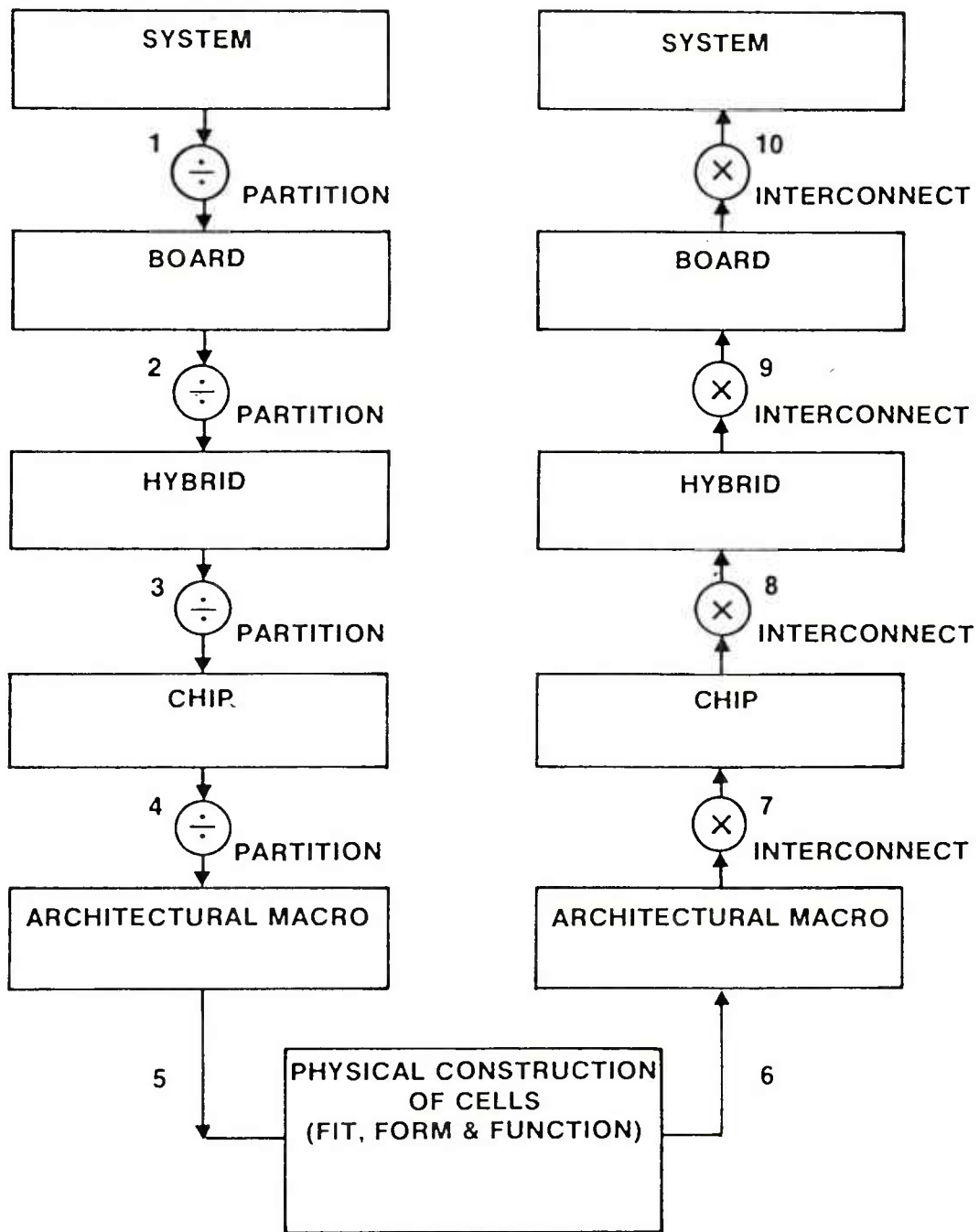


Figure 1. The NOSC design cycle.

problem surfaced (or perhaps to completion). Our design tools must be able to function and assist in such an environment. At present, this is not the case.

### SOLUTIONS AFFORDED BY METHOD DEVELOPED

It is within the design construct that one needs to identify areas in which automation can be incorporated to assist the design engineer. A number of factors should be examined. These are as follows:

1. Complex, but well defined, functions
2. Repetitious tasks at a single level
3. Similar tasks at multiple levels.

As will be seen in the next section, we have selected five operations that satisfy one or more of these conditions. They are

1. Topological Layout
2. Symbolic Layout
3. Path Router
4. Spacer
5. Transform.

The Path Router, Spacer, and Transform triad assist with the interconnection function to such an extent that a modified design cycle could be drawn as in figure 2. In this drawing, every level is fully interconnected and tested before one proceeds to the next lower level.

In this fashion, it is hoped that the design would only proceed once through those time-consuming steps of architectural macro partitioning and cell construction. Thus, time would be saved in two ways – first by the speed of automatic interconnection with the Path Router triad and then because the macros and cells would not have to be redone. This will be discussed in the Cost Savings section.

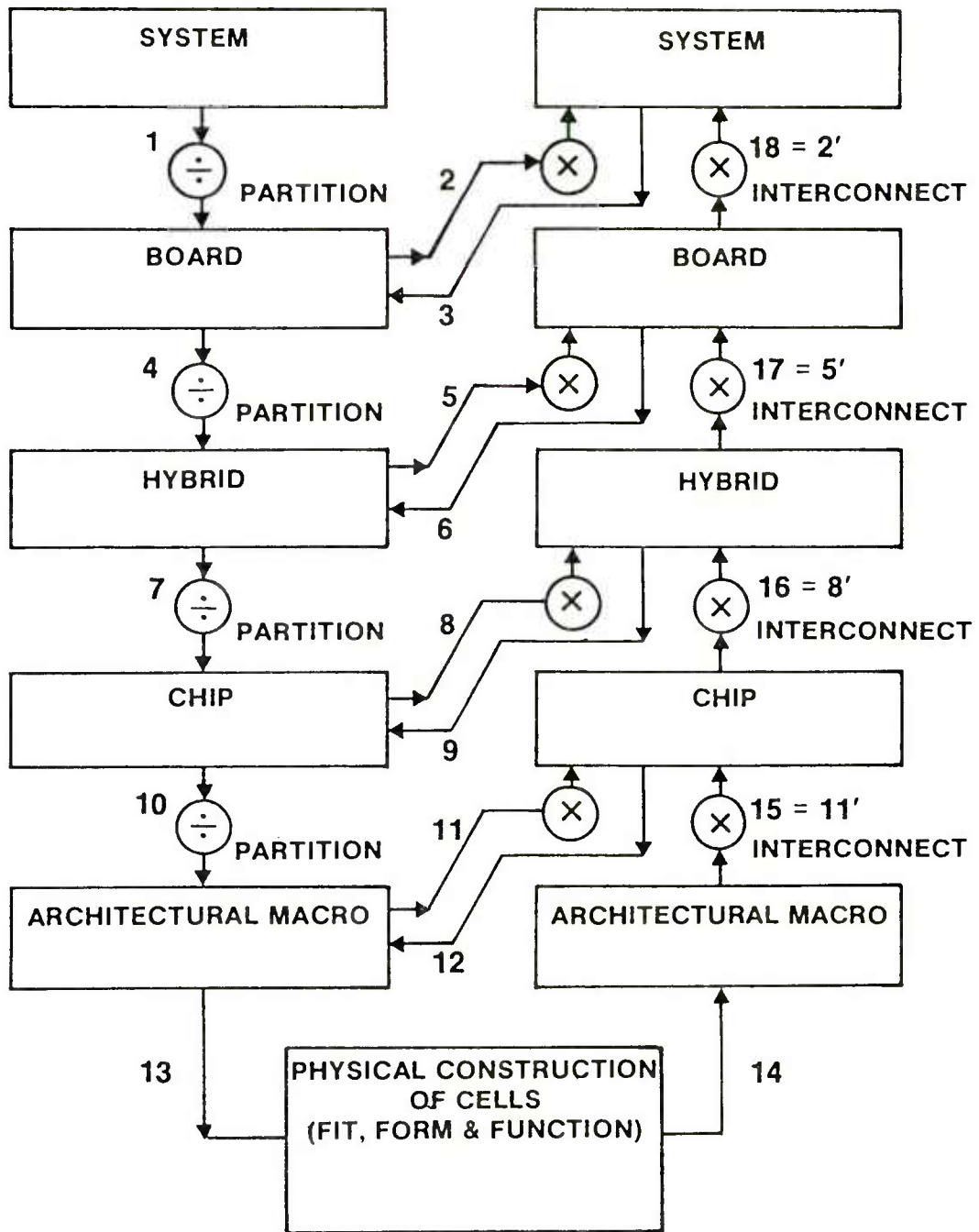


Figure 2. The NOSC design cycle (modified).

## ROUTINES

An explanation of the five routines follows. Special emphasis is placed on describing the purpose of each routine and its position within the design cycle.

### TOPOLOGICAL LAYOUT

The first area, that of Layout Topology, concerns the function of architectural macro placement and interconnection within the integrated circuit chip. Work on this topic is being handled by a subcontract awarded to Dr. A. Tuszynski at the University of Minnesota and entitled "IC Layout Topology – The Shortest Path From Theory to Applications." As mentioned in the Administrative Background section of this report, the contract was awarded in March 1981 and will be completed in September 1982. It is included below as a supplement. The work will consist in applying an area of mathematics graph theory involving numerator and denominator two-trees to the following topics: 1. placement techniques; 2. the order of nonplanarity criterion; 3. routing for glitch-free operation; and 4. guidelines for channel routing. The result will be a clear, concise, and intuitively convincing presentation of topology as it applies to chip layout.

### SYMBOLIC LAYOUT

The next area, that of Symbolic Layout, concerns the physical construction of cells. At this stage, the designer is laying out the many layers of mask patterns which will then be used to fabricate the transistors on the IC. As many as 15 masks are sometimes needed, with very exact rules about borders, overlaps, crossovers, and the other constraints necessary to result in a working device. Unless every transistor is exactly the same, the designer often must start from scratch, redesigning each of the layers again.

With the Symbolic Logic routine, however, the designer does not need to redesign every new transistor. What happens instead is that the designer sets up a Production Program listing input symbols and output component layers. He then designs, using the input symbols (either polygons or rectangles), until he reaches a design he is comfortable with. Then, by invoking the off-line Translation Program, the valid component layers are substituted for the input symbols, the result being operational devices.

Two features of the Symbolic Layout Program are uniquely valuable. The first is the program's ability to pass parameters from the input symbol through the interpreter to the output component. This is accomplished by defining the Production Program through the use of variables passed by the input symbol – such as the x-dimension breadth and y-dimension height. Thus, when the component layers are built, they will be a function not only of the type of component called but also of the size specified by the symbol's size.

The other feature is the capability of making multiple passes through the Translation Program. If the program is correctly defined (that is, the input symbols and output component layers are defined on different layers), multiple passes can be made through the Translation Program. Each time through, only the recently input symbols will be built into the components. As pointed out in the Design Cycle section, this can be especially valuable in that it supports the dynamic aspect of the design process.

## PATH ROUTER

The Path Router is useful for running bus structures in the integrated circuit, hybrid, printed circuit board, or back plane. It is run in on-line, interactive fashion and has three commands:

1. ROUTE PATH
2. ROUTE LEFT or ROUTE RIGHT
3. ROUTE CHANGE.

Its normal application proceeds as follows. The designer chooses those points which need to be connected by a signal path bus (a quantity of lines running parallel to each other) and verifies that the bus can be run without crossovers. He then connects the desired two-point pairs with two-point polygons (straight lines). The first path is then run by selecting the starting endpoint, invoking the ROUTE PATH command, specifying the width, and designating the route of the path. The routine then builds the path as specified, in either 45-degree or 90-degree lock. The designer may then modify the path if he so desires (the SPACER command also is often useful at this point to close the spacings to the minimum dimension).

To run the rest of the lines in the bus, the designer selects a single endpoint on the master path and the adjacent endpoints on the other two-point polygons. Then, by invoking a PATH LEFT or PATH RIGHT command (depending on whether the next path to be built is to the left or right of the first path's initial directed line segment) and giving a spacing, the rest of the bus structure can be built.

The final command, ROUTE CHANGE, allows the designer to revert from paths to two-point polygons. Thus modifications or reorientations can be made to the connected macros and the paths can be run again. This is just the type of support whose need was set forth in the PROPOSED METHOD-SOLUTION section, which allows one to move back and forth easily between the partition and the interconnection side of the design cycle for maximum flexibility.

The power of this facility should be emphasized at this point. In the past, to run any lines across the device, it was necessary to follow a number of pans and zooms on the CAD machine's video screen for each line. Grid spaces needed to be counted to assure correct spacing. In total, routing paths on a device often consumed over 65% of the mask design time. As a result, the sequential top-down design cycle of figure 1 was necessary. To attempt to proceed back and forth as suggested in figure 2 would have been unworkable. With the PATH ROUTING facility, the time is cut to a fraction, which allows a more flexible design scheme.

## SPACER

The SPACER routine is useful for moving selected components or elements a dimension relative to other specified components. This allows for quick manipulation to required distances without having to zoom down to count the grid spacings. This can significantly speed up the design.

The SPACER routine is invoked by first selecting the entities one wants moved; these may be vertices, line segments, or entire components. Then the command is SPACE, a direction (UP, DOWN, LEFT, RIGHT, or DISTANCE), and a distance. With the stylus, one then chooses the selected vertex to be moved relative to the target vertex; ie, the last point input with the stylus. The procedure then moves the selected elements, which maintain the same spacings relative to each other.

## TRANSFORM

The TRANSFORM routine is an extension of the Applicon ROTATE and FLIP commands. With the Applicon commands, these operations can be performed only on fully selected components. The TRANSFORM extension also allows the designer to operate on components with connected, two-point polygons for later use in the PATH ROUTING algorithm, and at the same time maintain their positions relative to the component. Once again, this facilitates the convenient manipulation of architectural macros while the interconnection information for later path building is maintained.

## COST SAVINGS

To quantify savings, a demonstration hybrid package and IC chip were designed. Both techniques were utilized, first the standard system and then the assisted routines, in an alternating fashion to negate any possible advantage (because of greater personnel familiarity) for either technique.

Cumulative times were kept for both methods. These figures, normalized for a 3000-man-hour total design, are given in table 1. As can be seen, the total savings for this design is 1300 man-hours, or 43%.

	Time Before	Time Now	Time Saved	Percent Savings
Symbolic Layout	750	500	250	33
Router/Spacer/Transform	1000	250	750	75
Spacer	500	200	300	60
TOTAL (for selected tasks)	2250	950	1300	58
TOTAL (for entire design)	3000	1700	1300	43

All time in man-hours.

Table 1. Design Enhancement Savings.

The return on investment for a \$90M annual IC design budget\* is as follows:

Return on Investment					
Years from start	1	2	3	4	5
Project costs (\$)	590k	-			
Savings (\$)	-	-	4 837.5k	9 675k	19 350k

\*IDA memorandum, Large Scale Integrated Circuits for Military Applications, February 1977, p 3.

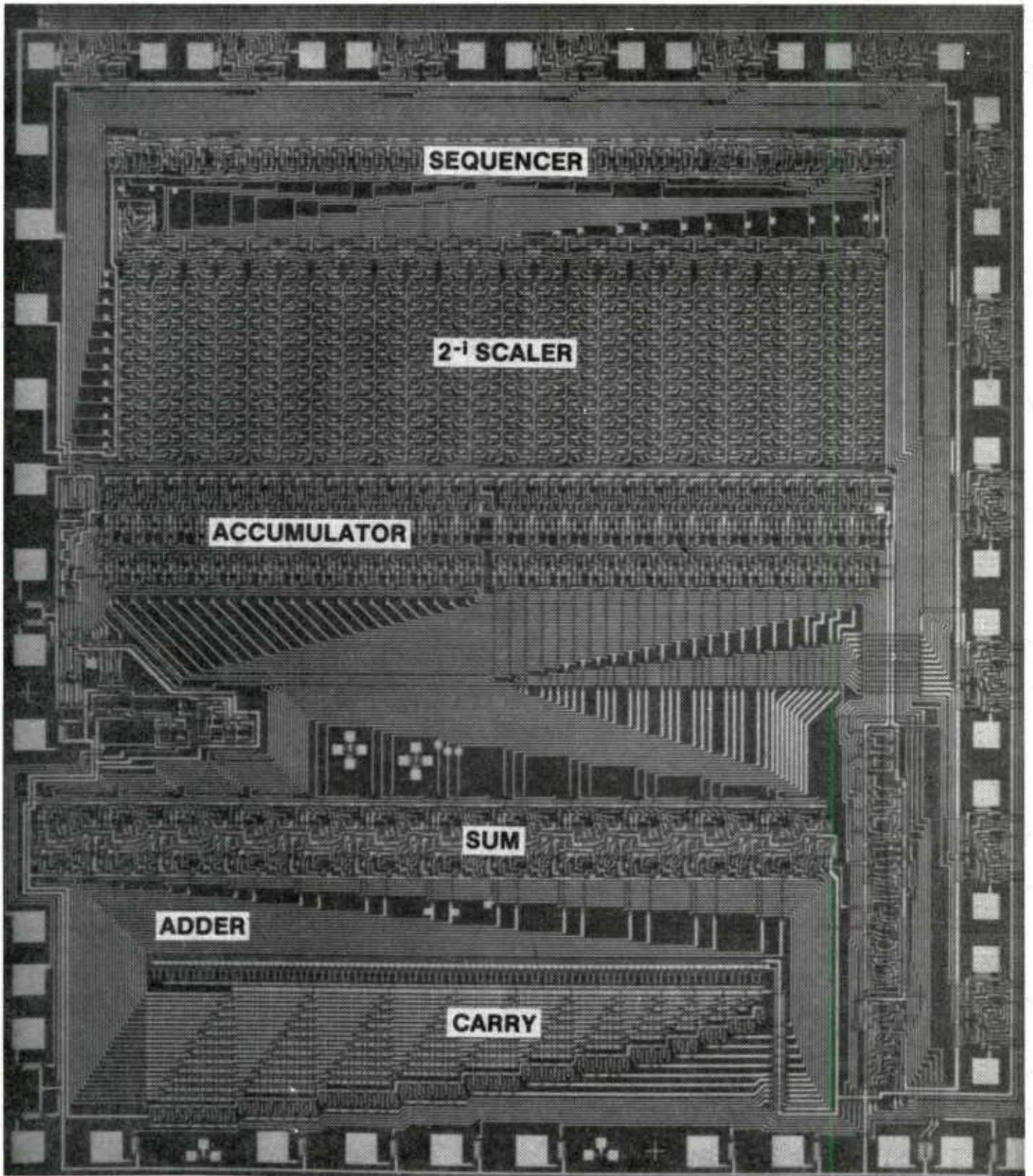
The table is computed by assuming utilizations of 1/8, 1/4, and 1/2 for years 3, 4, and 5. Thus the payback ratio (PR) is

$$PR = \frac{33\,862.5\text{k}}{590\text{k}} = 57.$$

This figure will be improved when the Topological Layout results are included. In addition, a restructuring of the design process, permitted by the interconnection tool triad, would improve upon this figure (see SOLUTIONS AFFORDED BY METHOD DEVELOPED, above).

## CONCLUSIONS

These enhanced tools for use in Computer-Aided Design systems can increase the designer's efficiency by automating many of the mundane, repetitious tasks while still maintaining control in the designer's hands. The tools, as implemented, not only support him in the immediate tasks of circuit layout and mask design, but also allow him more flexibility in the design cycle. Thus, they support the designer in the implementation of a well managed, layered, top-down design style, which is oriented at requiring only a single pass through the time-consuming cell generation phase.



**Figure 1. THE NOSC CORDIC ARITHMETIC PROCESSOR CHIP**

Sample Run of the PATH ROUTER and TRANSFORM ROUTINES  
Computer Graphics

- FIG 1 - The layout consists of three architectural macros, two of which are connected with sets of source/destination vectors which typically result in a "rat's nest". The third macro is an impediment to the routing.
- FIG 2 - A path route is selected and a pattern boundary is generated around the impediment block.
- FIG 3 - The first path is routed and plotted.
- FIG 4 - The remaining lines are plotted automatically by the routine in approximately 20 seconds.
- FIG 5 - In this figure a new obstacle is introduced, making the present routing unacceptable.
- FIG 6,7 - The macro configuration is altered by invoking the TRANSFORM operation in an attempt to overcome the new obstacle. These transforms include object translation, rotation, and mirror imaging (object is rotated about its own axis).
- FIG 8 - This layout represents the successful final result of the above three transforms.

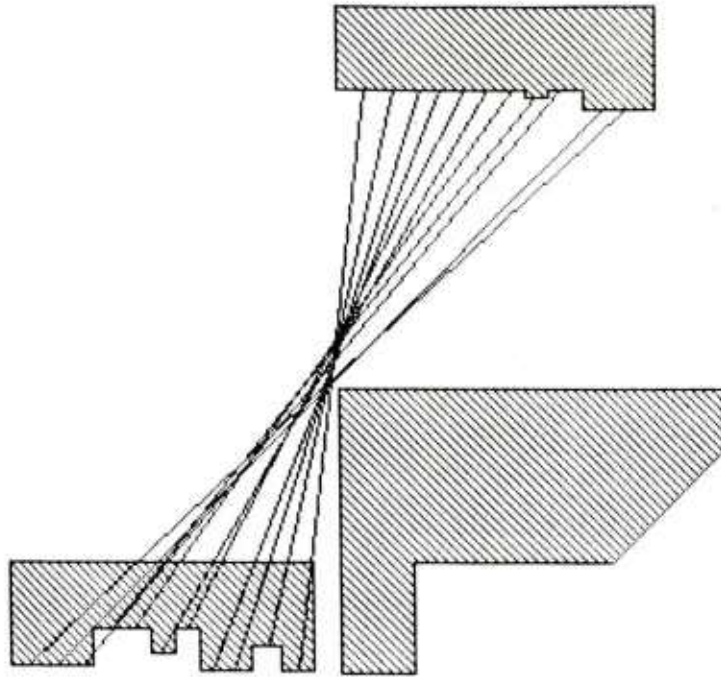


FIGURE 1

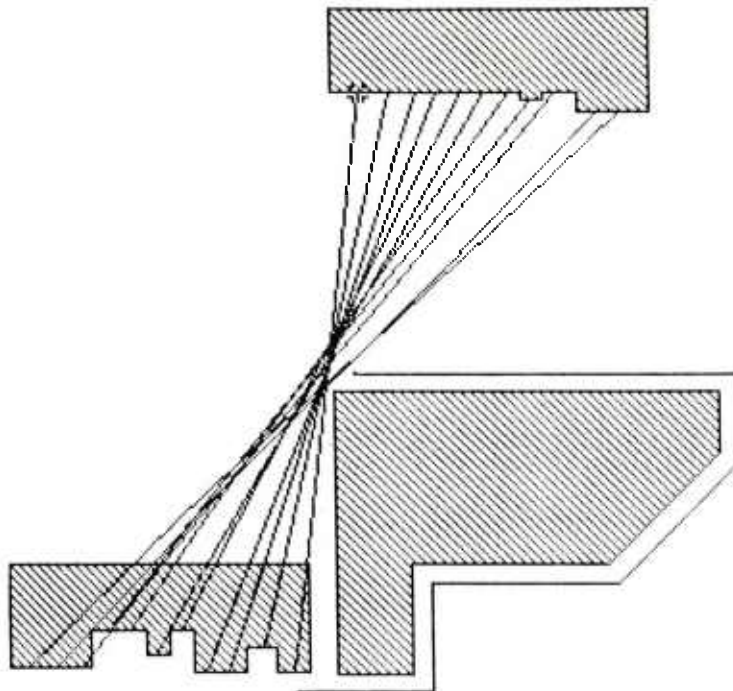


FIGURE 2

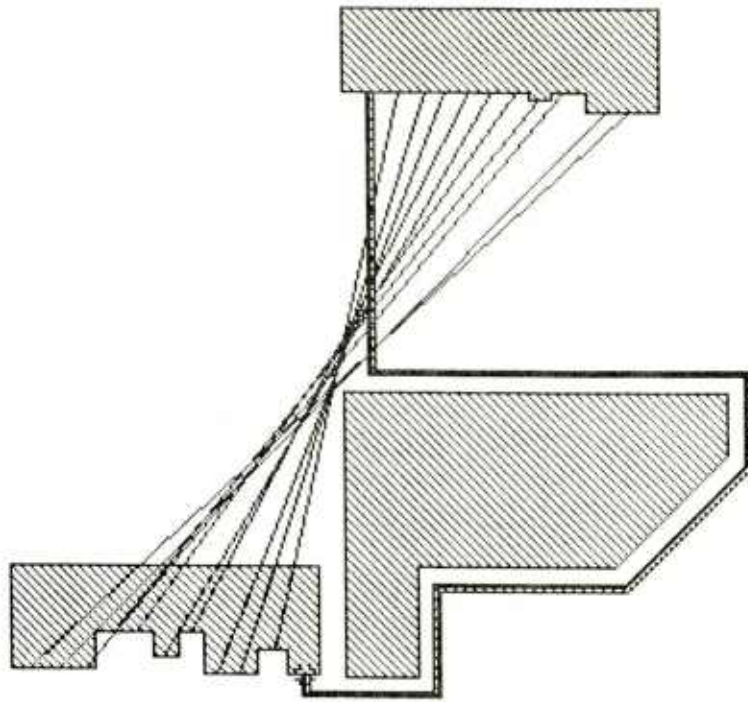


FIGURE 3

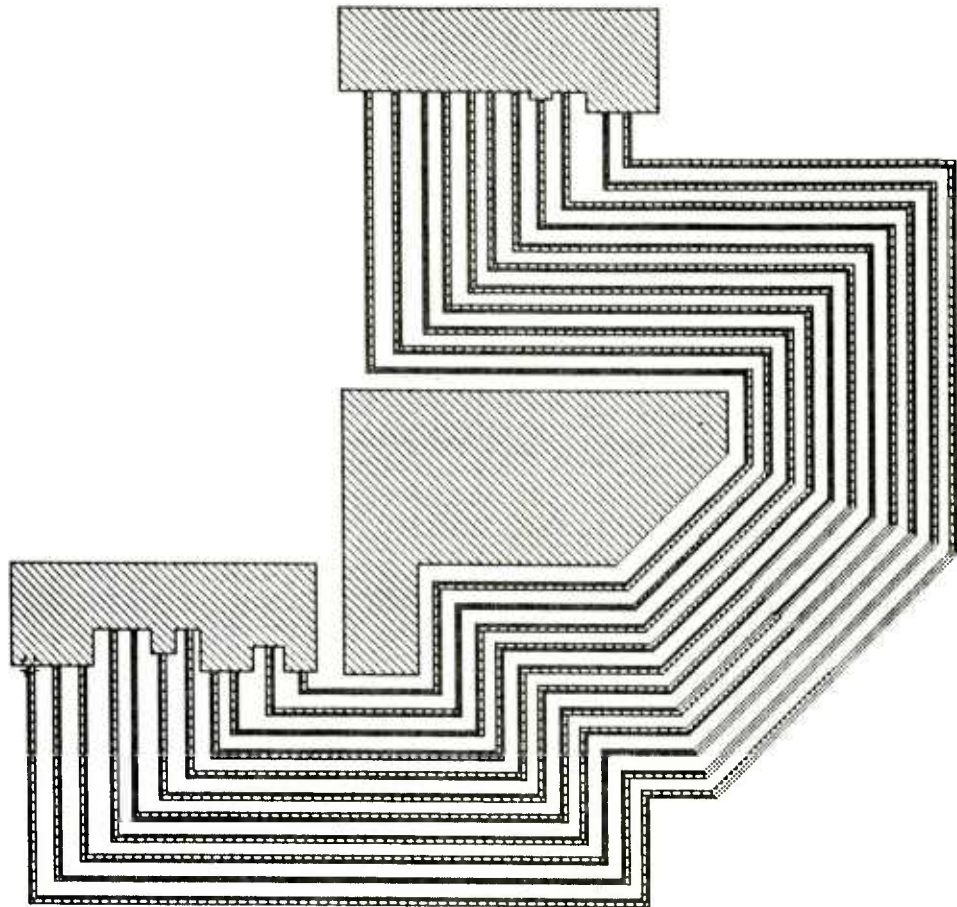


FIGURE 4

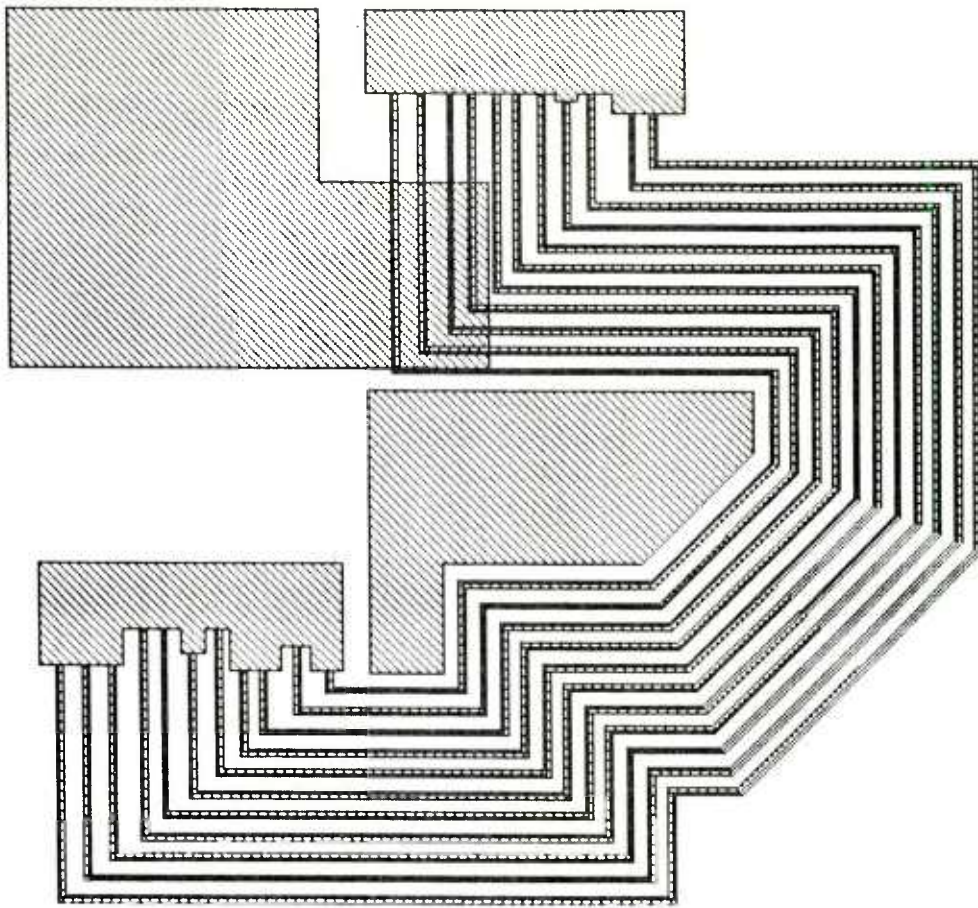


FIGURE 5

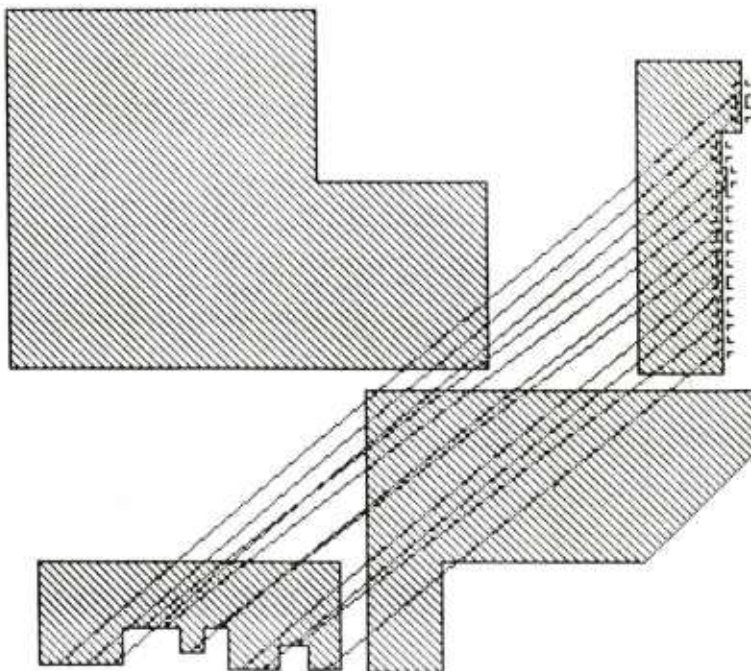


FIGURE 6

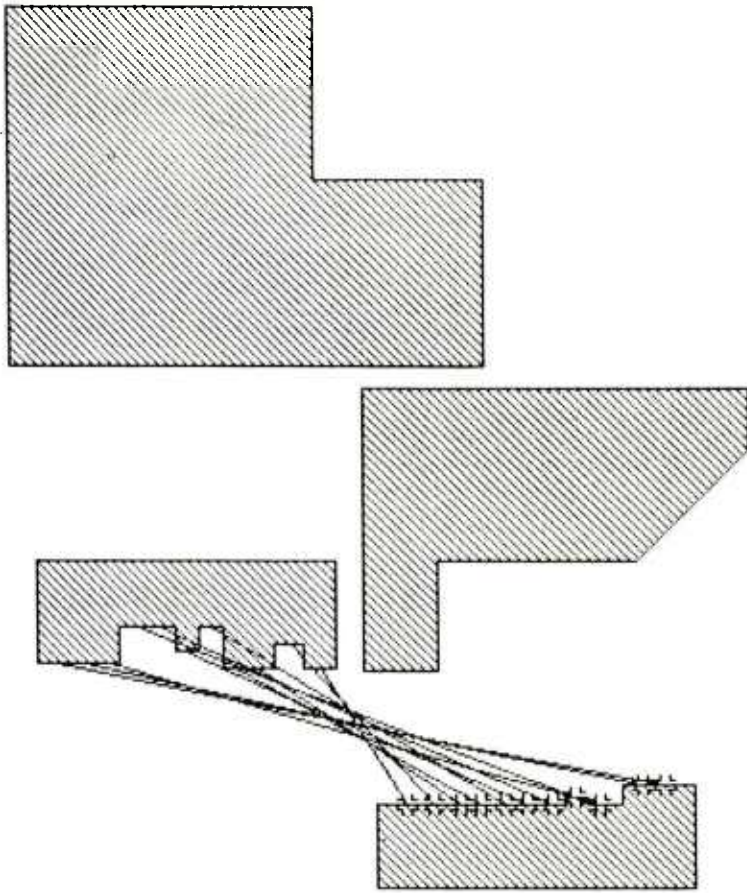


FIGURE 7

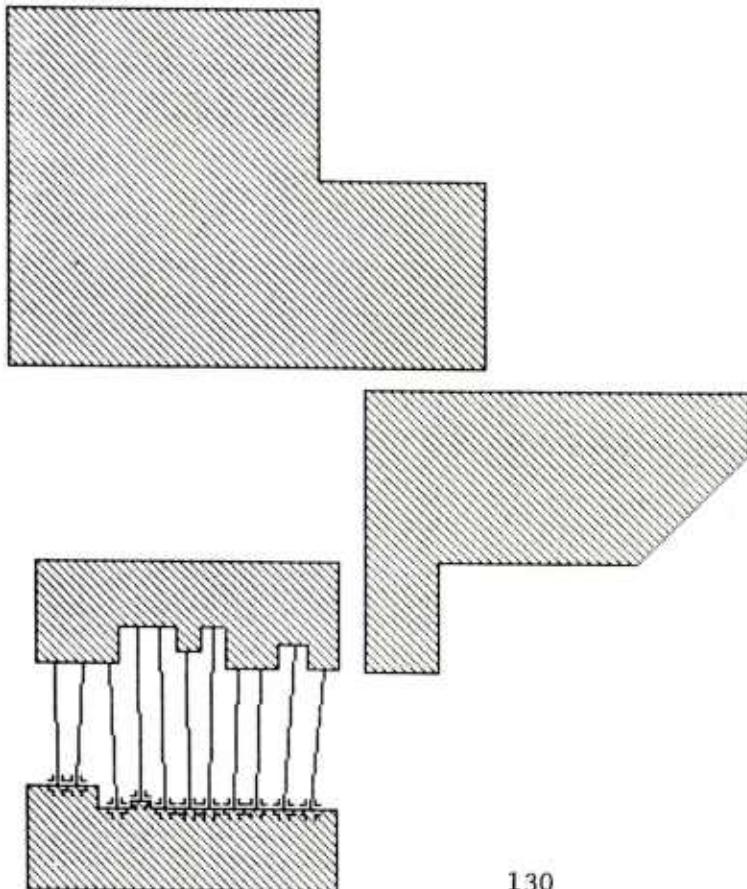


FIGURE 8

## SESSION IV - 2

### A RADIATION HARD CMOS/SOS MICROPROCESSOR CHIP SET

Mr. Richard Lydick  
Dr. Richard Glicksman

RCA Corporation  
Solid State Division  
Somerville, NJ 08876

This paper described a Large Scale Integrated (LSI) CMOS/SOS microprocessor chip set used to emulate standard military micro and minicomputers. As a result of AFWAL Materials Laboratory Manufacturing Technology Contracts, both the CMOS/SOS technology and the microprocessor chip set circuits are available from a manufacturing facility, and give promise of offering cost effective alternatives to other technologies and circuits, in the design of high performance military computers.

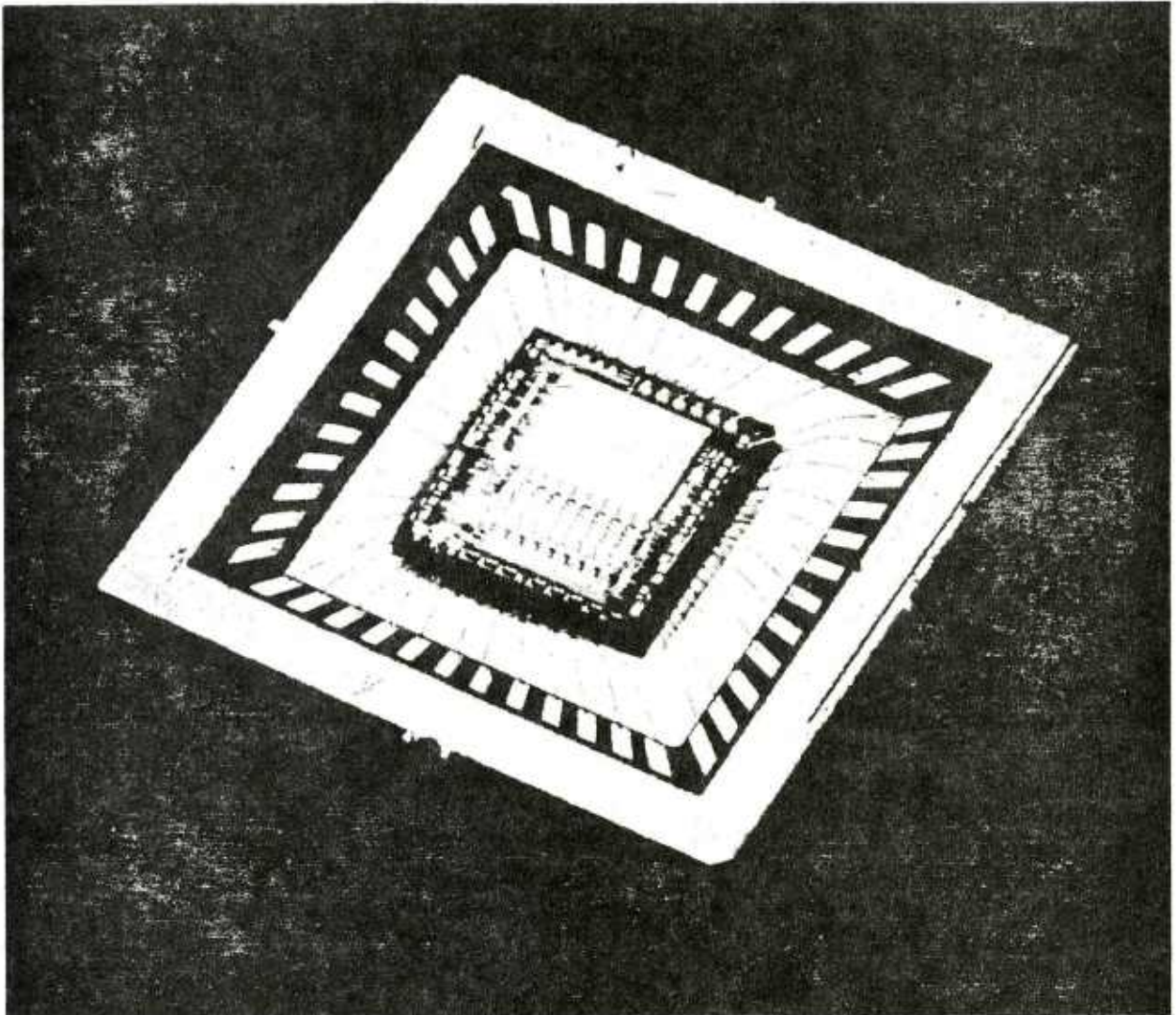
The advantages of CMOS/SOS technology will be presented along with a description of the salient design and performance features of the microprocessor chip set circuits. The heart of the chip set is an eight bit slice General Processor Unit (GPU). The rest of the set contains all the functional building blocks required for high performance, microcomputer systems. These include controllers to facilitate emulation, a multiplier to perform rapid numerical processing, a 4K mask programmable ROM, 4K RAMs, and a series of Gate Universal Arrays which are mask programmable, and provide the designer with unique logic functions needed to combine the other LSI circuits into a working system.

Tracor, Inc. is employing these circuits to fabricate a GPU emulator which is currently undergoing full scale development for the Magnavox User Equipment Sets for the Tri-Service NAVSTAR/GPS Program. The AFWAL Avionics Laboratory has also awarded Tracor a contract to build a 16-Bit Radiation Hard Emulating Computer (RHEC) using the microprocessor chip. Military standard architectures which the RHEC will be capable of emulating via microprogramming are Mil-Std-1750A, AN/UYK-20, AN/AYK-14 and AN/UYK-44.

Other applications of the chip set to be presented, include the Martin Marietta AMACS-1680 computer developed for spacecraft applications, and RCA work in emulating the PDP-11 as well as its new spacebourne computer, designated SCP050.

# EPIC

## Emulation and Programmable IC Family



**RCA** Solid State  
Division

# **Manufacturing Technology for Radiation Hardened Microprocessor**

**Contact # F33615-78-C-5135  
AFWAL Materials Laboratory  
Wright-Patterson AFB, Ohio**

**Project Engineer: Eugene H. Miller, AFWAL/MLTE**

## SLIDE #1 - EPIC CHIP SET

Today my presentation will be about a high performance microprocessor chip set that RCA developed on an Air Force contract.

A brief description of the technology and the circuits comprising this chip set will be presented, along with general family performance characteristics.

The application of this chip set in emulating various military computers will also be discussed.

## SLIDE #2 - AF CONTRACT SUPPORT

This work was supported by Contract #F33615-78-C-5135 with the Air Force Materials Laboratory in Dayton, Ohio. The program is being administered by the Electronics Branch under Major John Erbacher, and the contract project engineer is Gene Miller.

# **Genesis of EPIC Chip Set**

## **Problem**

- **Proliferation of Microprocessors in Air Force Applications**
- **Many Parts not Radiation Hardenable**
- **Limited Temperature Range**
- **Need for Computer Standardization**

## **Solution**

- **Provide Radiation Hardened Circuits Which Could Emulate Microcomputers of Interest**
- **Devices Also Must be Low Power, High Speed, Cost Effective**
- **Above Criteria Have Been Met With RCA EPIC Chip Set**

SLIDE #3 - CHIP SET GENESIS

Before I give a description of the microprocessor chip set, it would be informative to describe the genesis of this program.

In 1975, many Government R&D houses became alarmed by the proliferation of microprocessors in military applications. In particular, several of the approximately 65 types of microprocessors were being designed into strategic equipment, which required radiation hardness ranging from Aircraft levels (man-rated) to Satellite levels.

All microprocessors available at that time, with few exceptions, were N-MOS dynamic logic, which are not sufficiently hard for aircraft and satellite applications. Further, it is generally believed that N-MOS technology never can be made radiation-hardened.

Other concerns, were the ability of these microprocessors to operate over the full military temperature range, and the lack of computer standardization.

The Air Force's solution to this problem was to develop radiation hardened circuits which could emulate the microcomputers of interest. In addition to radiation hardness, these circuits were to have high speed, low power dissipation, and be cost effective.

The above criteria have been met with the microprocessor chip set, developed on this contract.

SLIDE #4 - TECHNOLOGY CHOICE

Although bulk CMOS technology could have been used in the microprocessor chip set, SOS was chosen for additional speed and transient radiation performance.

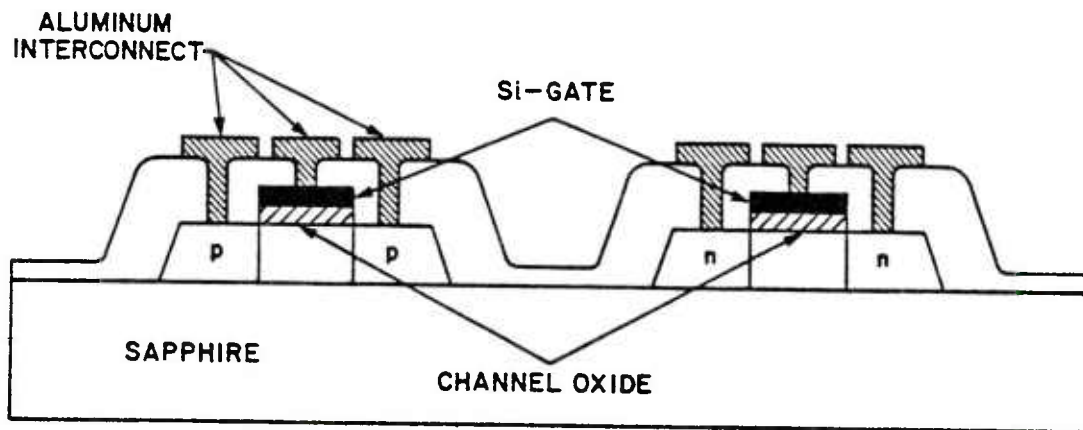
CMOS/SOS was the preferred technology with respect to the requirements of transient radiation hardness, speed, power dissipation, noise immunity, operation over the full military temperature range, and operating voltage range.

<b>Requirement</b>	<b>Bi-Polar</b>	<b>CMOS Bulk</b>	<b>CMOS/SOS</b>
• <b>Transient Radiation Tolerance</b>			<b>X</b>
• <b>High Speed</b>	<b>X</b>		<b>X</b>
• <b>Low Power</b>		<b>X</b>	<b>X</b>
• <b>Noise Immunity</b>		<b>X</b>	<b>X</b>
• <b>Temperature Range</b>	<b>X</b>	<b>X</b>	<b>X</b>
• <b>Power Supply Range</b>		<b>X</b>	<b>X</b>

SLIDE #5 - CMOS/SOS STRUCTURE

Shown in this viewgraph, is a cross-section of a CMOS/SOS structure. The substrate is sapphire, upon which thin islands of silicon are defined. These islands then become the starting point for the fabrication of the P-MOS and N-MOS transistors.

Because of the greatly reduced junction capacitance of this structure, and the elimination of channel stops, the SOS structure is characterized by high internal circuit speeds, low power dissipation ( $P=CV^2F$ ), high packing density, and resistance to transient radiation effects. (The device cannot latchup.)



92CS-32239

## SLIDE #6 - EPIC MICROPROCESSOR CHIP SET FAMILY

The various circuit types in the microprocessor chip set family are listed in this viewgraph.

The General Processor Unit is the heart of the chip set. It is an 8-bit slice which performs the arithmetic and logic operations required in most general purpose computers.

The emulating controller is a custom circuit which contains all functions necessary to implement the control function of a computer. There also is a controller, the microprogram sequencer, which is a pin-for-pin replacement for the AMD2910 bipolar circuit.

Two 4K RAMs are available, one organized as 1K x 4 bits, and the other 4K x 1 bits. These RAMs are relatively fast, having access times of 100 nanoseconds at 10V.

The 4K ROM is also available in two organization variants, 512 x 8 bits and 256 x 16 bits. The ROM access time is typically 50 nanosec at 10V.

A two's complement 8 x 8 multiplier and a family of Gate Universal Arrays complete the chip set. The GUA's available in sizes of 300, 452, and 632 gates, provide the logic not available on the other chips.

## **EPIC Microprocessor Chip Set Family**

- **General Processor Unit (8-Bit Slice)**
- **Emulating Controller**
- **Microprogram Sequencer (CMOS/SOS 2910)**
- **4K Random Access Memory (1Kx4, 4Kx1)**
- **4K Mask Programmable ROM (256x16, 512x8)**
- **8x8 Multiplier**
- **Gate Universal Arrays (300, 452, 632, Gates)**

# Microprocessor Chip Set Characteristics

- **Stand Alone Set -- Requires No Additional MSI Circuits**
- **Expandable -- In 8-Bit Increments**
- **High Performance -- GPU Cycle Time is 10 MHz @ 10 V**
- **Low Power Dissipation -- CMOS Technology**
- **Full Military Temperature Range -- -55° C to 125° C**
- **MIL-STD-883 Class B Screening**
- **Radiation Hardened**
- **Leadless Hermetic Chip Carrier Packaging**

## SLIDE # 7 - MICROPROCESSOR CHIP SET CHARACTERISTICS

Presented in this viewgraph are general performance characteristics of the microprocessor chip set.

They are a stand-alone set. That is, no additional SSI or MSI circuits are needed with this set. The General Processor Unit is expandable in 8-bit increments. Thus, two GPU's can be concatenated to build a 16-bit machine.

The GPU cycle time is 10MHz at 10V.

Because of its CMOS technology, power dissipation is low. Approximately an order of magnitude lower than bipolar technology used in existing computers.

The chips operate over the full military temperature range of -55°C to 125°C.

They can be screened to Mil-Std-883 Class B.

Are radiation hard.

And are packaged in leadless, hermetic chip carrier packages.

# Leadless Hermetic Chip Carrier Packaging

- Decreased Size
- Decreased Weight
- Reduced Cost
- Improved Electrical Performance
- Improved Thermal Characteristics
- Repairability

## SLIDE #12 - ADVANTAGES OF HERMETIC CHIP CARRIER PACKAGES

Some of the advantages of hermetic chip carrier packaging are listed in this viewgraph....

- decreased size - 1/6 size of DIP package (average)
- decreased weight - 7-20 x less depending upon pin-count
- cost - higher cost today which reflects startup costs  
- projected cost in high volume less than DIP
- improved performance - this is a result of shorter electrical paths which result in lower resistance, inductance, and capacitance. This permits faster switching times.
- repairability - when comparing overall assembly/system cost, the ease of repairability is a significant factor. (As lead count increases, the ability to remove DIP devices from PC boards without damage is difficult.)

Finally the use of chip carriers allows for cost effective screening in hybrid assemblies, and provides enhanced product reliability.

# **System Development With EPIC Chip Set**

## **Performance Improvements**

- **Maintains or Exceeds Computer Throughput**
- **Lower Power Dissipation**
- **Reduced Size and Weight**
- **Radiation Hard**

## **Low System Development Cost**

- **Improvements Realized While Maintaining Compatibility at User Instruction Set Level**
- **Large Savings of Existing Software**

## **Application**

- **High Technology Improvements to Existing Older Computers**
- **New Computers Operating In Environments Ranging from Man Pack to Space**

# System Applications of EPIC Chip Set

- **AN/UYK-20 Emulation**  
— Standard Navy 16 Bit Computer
- **Navstar GPS User Equipment**  
— Now in FSED
- **Radiation Hardened Emulating Computer**  
— Air Force Mil-Std-1750 ISA
- **PDP-11 Emulation**

## SLIDE #13 - SYSTEM DEVELOPMENT WITH EPIC CHIP SET

For the remainder of my presentation, I will deal with the systems application of the microprocessor chip set.

The combination of LSI CMOS/SOS technology and high density ceramic chip carrier packaging should result in the following system improvements.

The computer throughput should be maintained or exceeded using the chip set. In addition significant reductions in size, weight, and power dissipation should also be realized. Radiation hardness should also be enhanced.

These improvements should be realized while maintaining compatibility at the user instruction set level -- and thereby result in a large saving of existing software.

Thus the application of the chip set in emulating computers could result in:

- High technology improvements to existing older computers
- Or new computers operating in stringent military environments.

SLIDE #14 - SYSTEM APPLICATIONS OF EPIC CHIP SET

Tracor Corp. in Austin, Texas has used the chip set to emulate the AN/UYK-20, which is a standard Navy 16 Bit Computer. The Central Processor Unit built by Tracor, has a throughput equivalent to, or greater than the AN/UYK-20, while consuming less than 2 watts of power from a 10V DC source.

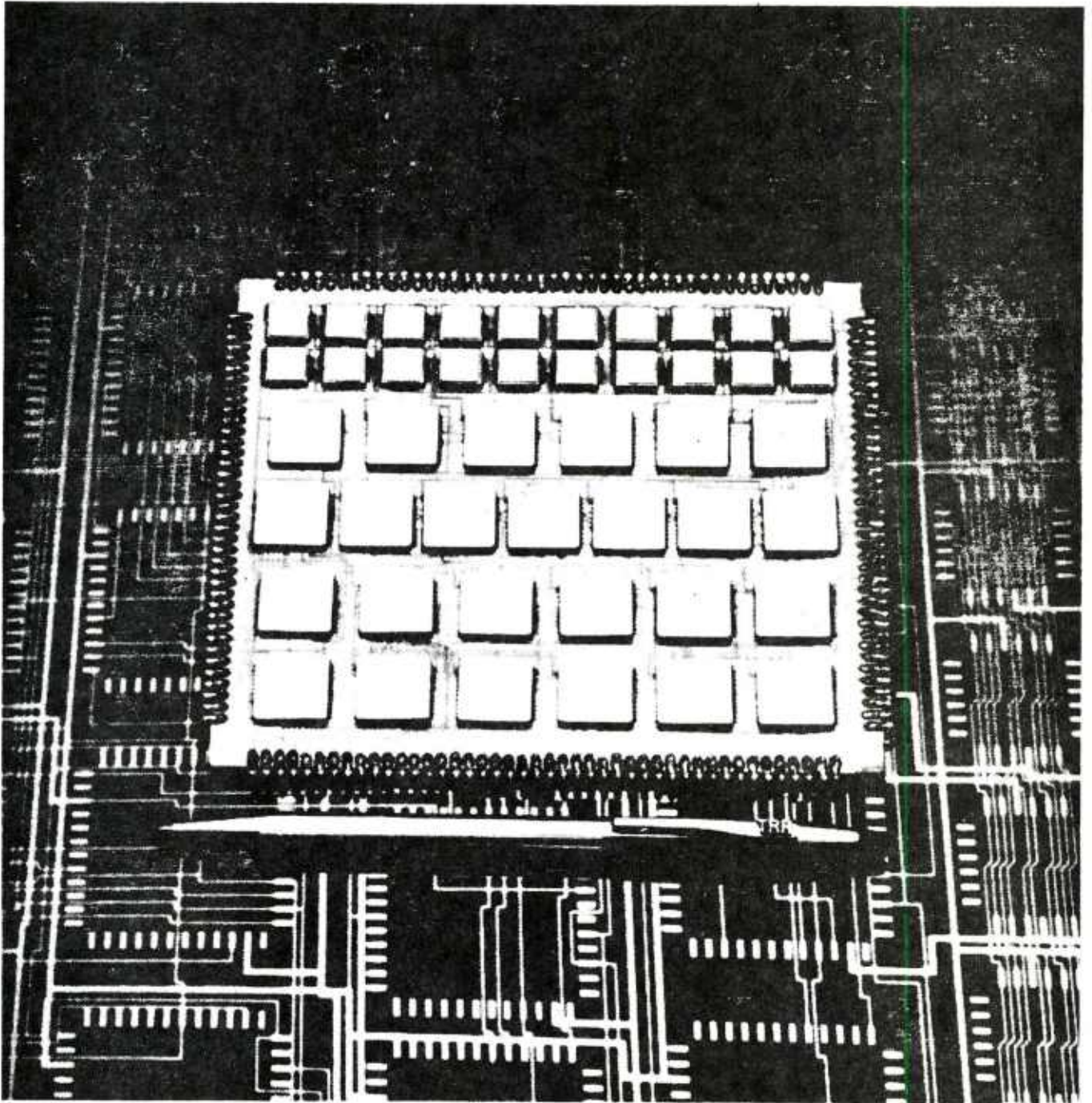
This emulator is currently undergoing Full Scale Engineering Development for use in the NAVSTAR Global Positioning System User Equipment.

The Air Force has also awarded Tracor a contract to develop a Radiation Hardened Emulating computer using the microprocessor chip set. This computer will be capable of emulating the Air Force Mil-Std-1750A instruction set architecture as well as other instruction set architectures.

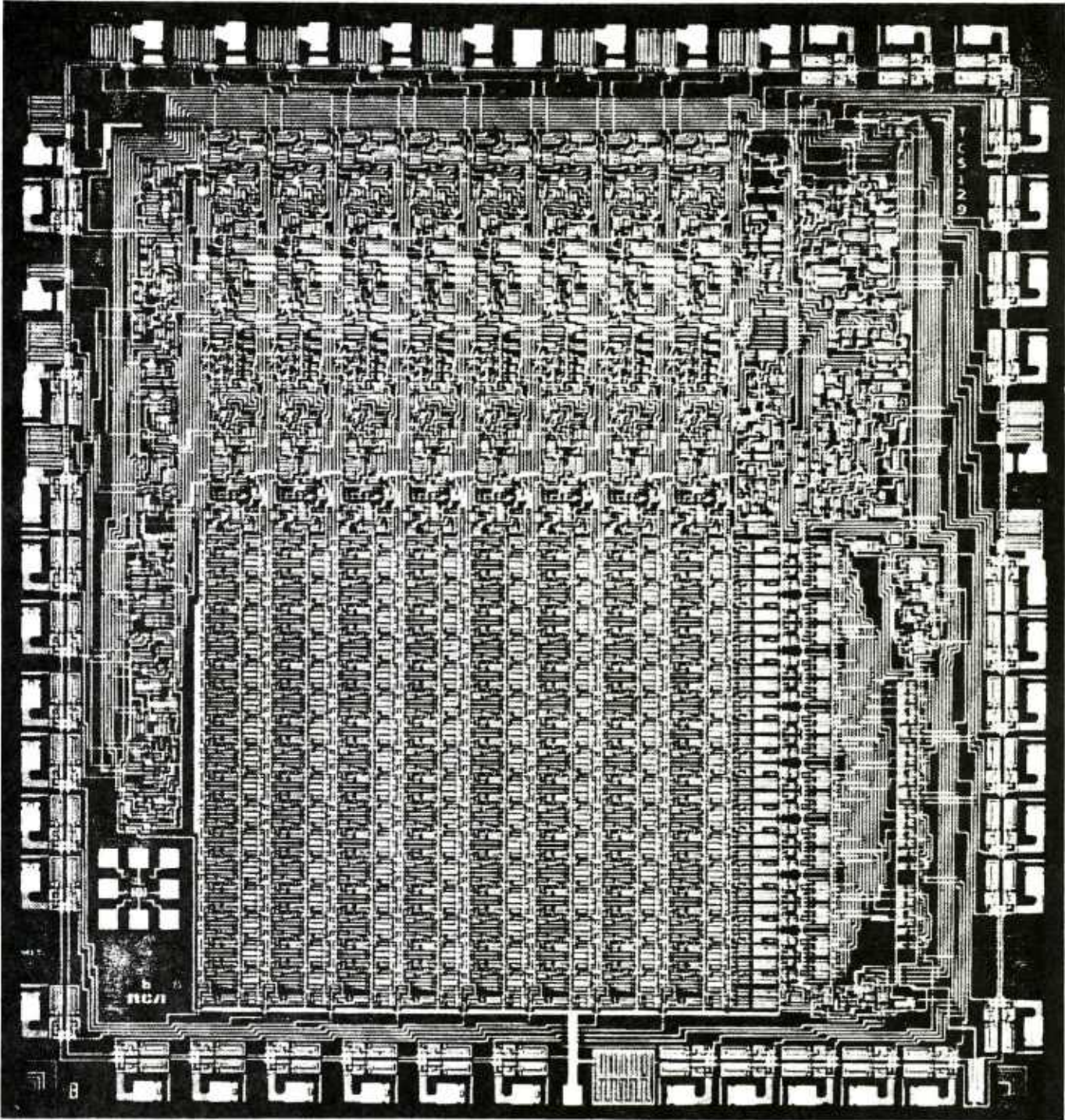
The RCA Government Systems Division has emulated a PDP-11 computer, and demonstrated equivalent throughput and a significantly lower power dissipation than the original machine.

SLIDE #15 - PHOTO OF CPU EMULATOR BOARD

On this viewgraph is a photograph of the CPU Emulator developed by Tracor. It is packaged on one side of a 4.5" x 5.0" ceramic substrate. The larger packages are 48 pin chip carriers containing the General Processor Unit, Emulating Controller, and Gate Universal Array logic circuits. The smaller packages are 24-pin chip carriers containing ROM and RAM memory devices.



CPU EMULATOR BOARD



SLIDE #16 - SPACEBORNE COMPUTER APPLICATIONS

Presented in this viewgraph are some applications of the microprocessor chip set in spaceborne computers.

Martin-Marietta (Denver) has developed an Auxiliary Processor Unit which will be used on the NASA Standard Spacecraft Computer.

Martin has also developed a full blown computer, the AMACS-1680, using the chip set. They plan to use two of these computers in the NASA End-to-End Data System, being developed for NASA Langley.

Finally the RCA Space Division is upgrading their TIROS and DMSP satellites from a bulk CMOS implementation to the CMOS/SOS chip set.

In all of these applications -- gains in size, weight, power dissipation, and radiation hardness are realized with no degradation in computer throughput.

SUMMARY

A microprocessor chip set has been developed, which is ideally suited for emulating military computers. The circuits in this chip set, combine the high speed, low power, and radiation resistant qualities of CMOS/SOS technology, with the high density packaging benefits of leadless hermetic chip carriers.

A number of system applications have been described, which illustrate the use, and advantages, of these circuits in emulating existing computers such as the AN/UYK-20 and PDP-11, and in new spaceborne computers such as the AMACS-1680.

The microprocessor chip set circuits are now commercially available from RCA. In addition work is planned to extend the capability of the chip set by providing circuits with higher speeds, greater chip densities, and increased radiation hardness.

I would like to acknowledge the support of the Air Force Materials Laboratory, for both the microprocessor chip set contract and the hermetic chip carrier package work.

## **Spaceborne Computer Applications**

- **Auxiliary Processor Unit (APU)**
  - **NASA Standard Spacecraft Computer**
- **AMACS - 1680**
  - **NASA End-To-End Data System (Needs)**
- **SCP234**
  - **Tiros and DMSP Satellites**

## SESSION IV-3

### AN OPTICAL DIRECT STEP ON THE WAFER SYSTEM FOR SUB-MICRON LITHOGRAPHY

BY

MR. JAMES DEY

OPTIMETRIX

AND

MR. ROBERT REAMS

HARRY DIAMOND LABORATORIES

The paper described the MM&T work done by Optometrix, Sunnyvale, CA. for Harry Diamond Laboratories under a late start FY77 contract. Optometrix provided the Laboratories a prototype station for direct-step-on-the-wafer photolithographic exposure to aid in the development of the technology needed to pattern semiconductor integrated circuits having feature sizes below 1.25 micrometers. The paper illustrated the equipment, its operational capability, and some of its advanced results.

# SESSION V - 1

13th Annual DOD Manufacturing Technology Conference

## Traveling Wave Tube Manufacturing Technology Program Results, One Example

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### Acknowledgements

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## Abstract

Teledyne MEC and Raytheon, acting in concert over the past two years, carried out a multi-tasked manufacturing technology program for the Naval Research Lab in Washington, D.C. This program was directed toward cost reduction in the manufacture of high power, helix-type traveling-wave tubes.

Improved manufacturing techniques and cost reductions were achieved over the complete spectrum of TWT production from parts fabrication to automatic inspection and testing. In general, the program results are applicable to all helix-type TWTs.

One example of the cost reduction techniques achieved is in the area of helix manufacturing. Through the application of commercially available automatic inspection equipment, not only was the cost of a finished unit cut by half but accuracy of inspection was greatly increased.

## Introduction

During 1979 and 1980, Teledyne MEC, in concert with Raytheon's Power Tube Division, carried out an extensive, multi-tasked manufacturing technology program for the Naval Research Lab in Washington, D.C. This program was directed toward cost reduction in the manufacture of high power, helix-type, traveling-wave tubes.

A cardinal guideline established at the onset of the program was to conduct the effort in such a way that the results would be applicable to all helix TWTs in general. This was accomplished. Improved manufacturing techniques and cost reductions were achieved over the complete spectrum, from prime parts fabrication to automatic inspection and testing.

One of the cost saving techniques developed on this program was the automatic inspection of helices.

### Helix Fabrication and Inspection

Up to and during the early stages of this program, TMEC's helix inspection was performed with the aid of a microscope and digital readout, traveling table. Although inspection was performed on a sampling basis, the time required for this operation was still high; 52 percent of the total labor involved in the manufacture of the helix was spent on inspection. Accuracy was also a problem, being both variable and limited, due to human variations and fatigue.

With the objective of reducing time and increasing the accuracy of helix measurement in mind, an investigation was launched into the suitability of commercially available equipment for this job. Five

companies were consulted and four were visited for an in-depth review of our specific needs.

The Automatic Optical Micrometer, manufactured by View Engineering, Inc., of Chatsworth, California was selected. This equipment utilizes a video imaging camera with either direct or backlighting of the object being measured. Digitalizing of the image for processing is accomplished by a microprocessor, which also controls the movement of the camera and the part being measured. Figure 1 shows the equipment control console and video screen.

Because the automatic measuring equipment is designed for general inspection, a specific holding device had to be designed to support helices during measurement. This fixture, shown in Figure 2, supports the helix on a mandrel, either the winding mandrel or a loose fitting steel mandrel (drill rod) as is the case with a finished free helix. The fixture accepts a large variation in mandrel lengths as well as mandrel diameters, while maintaining a constant centerline. The latter is important for the automatic programming of the equipment.

## Results

Operating and programming the unit is quite easy and, by using stored programs (the unit contains a floppy disc memory), complete inspection of a helix can be accomplished in less than two minutes. This, compared to the previous 20 minutes per inspection, is quite a dramatic improvement and has resulted in cost savings alone of 48 percent on this tube part.

This equipment is now being used in TMEC's helix production department full time, on two eight-hour shifts per day. This, and other results of the manufacturing technology program, have been put into practice at TMEC, resulting in reduced costs for producing TWTs for U.S. Military applications.

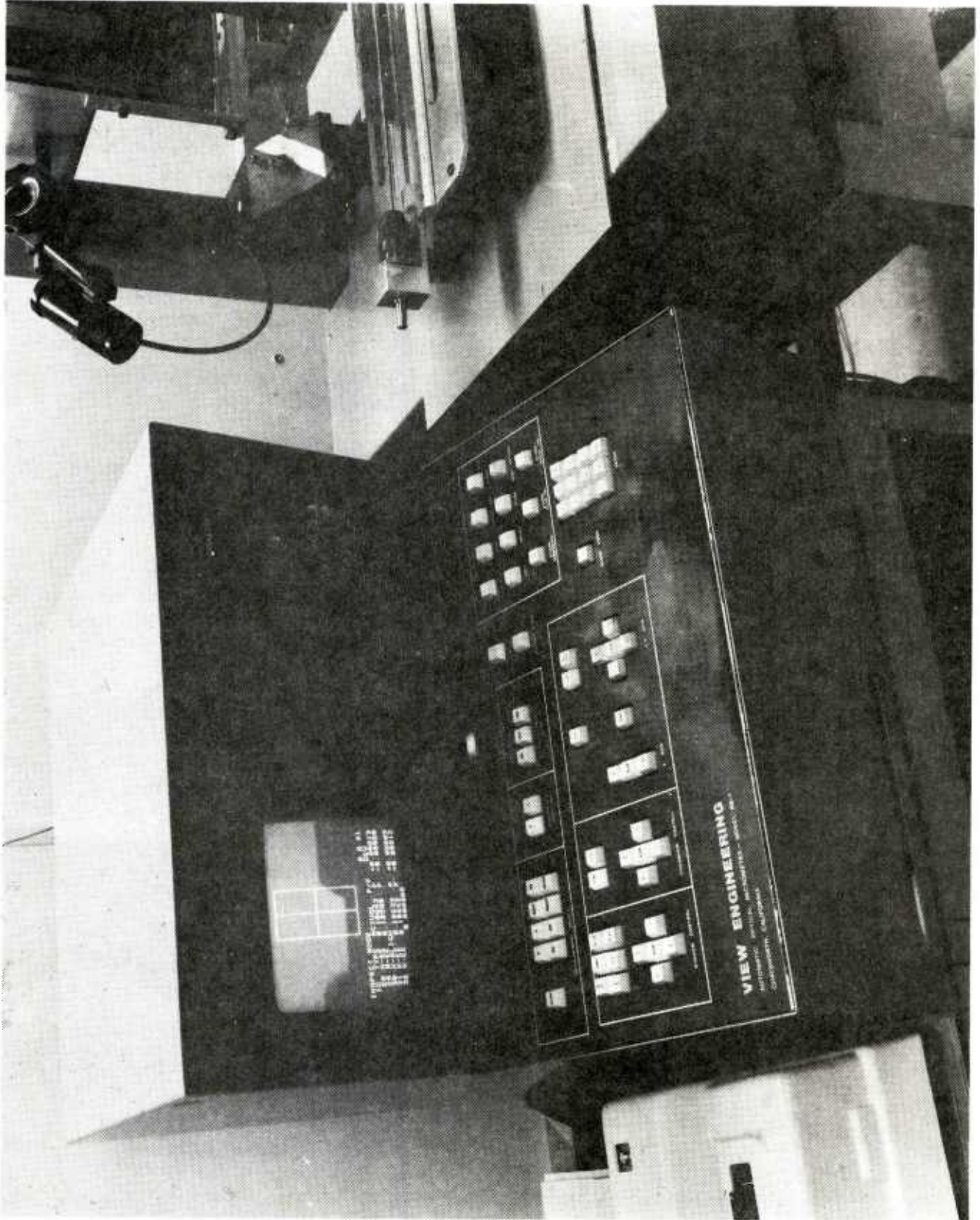


FIGURE 1 AUTOMATIC OPTICAL MICROMETER CONSOLE

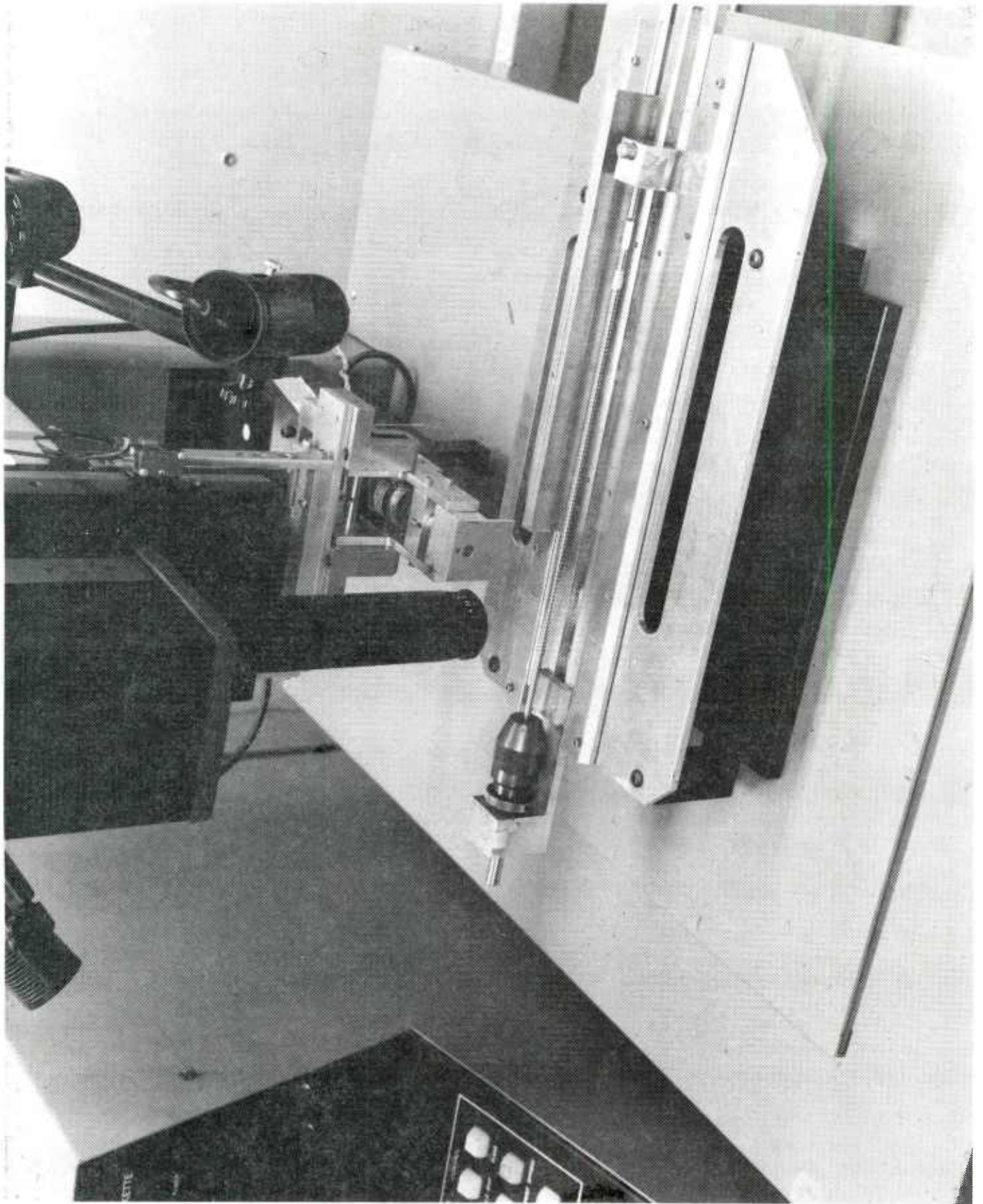


FIGURE 2 MEASURING TABLE AND HELIX SUPPORT

The final category of tasks was the hardware demonstration task under which a group of 20 tubes was built and tested. During the prime parts fabrication task, the baseline parts cost was established first for a quantity of 6000 tubes then the cost drivers were identified and selected for cost reduction. Parts selected were grids, pole pieces and spacers, support rods and magnets. For instance methods were developed to photo etch the grids and punch the hubless pole pieces out of iron sheet rolled to the required thickness and cut the spacers off custom drawn tubing. In summary, the prime parts cost reduction task resulted in a cost reduction of 15%.

The task that addressed the cost effective fabrication methods was the most ambitious task. A system was developed to sputter the attenuators on the support rods instead of coating them one by one in a hot coil by carbon deposition out of a hydrocarbon atmosphere. The new sputter equipment was built and tested and can produce hundreds of rods at a time with excellent reproducibility. A cost reduction of 80% was achieved.

In order to reduce the cost of the helix winding and improve the accuracy, a helix winding and inspection machine was designed and built. Excellent results were achieved with a maximum pitch deviation of only plus or minus three ten thousands of an inch. Helix fabrication cost was reduced by 35%.

In the category of automatic equipment, a computer controlled aging and testing station was designed and purchased. All functions required for tube operation and parameter sensitivity measurements are computer controlled. Operating parameters such as beam and grid voltages are automatically measured and recorded by computer. The cost saving was 20% by using this automatic equipment.

During the hardware demonstration phase, tubes were built and tested and the results were compared with a group of 12 tubes that were built during the development phase. The tubes built and tested showed less of a performance data spread than the development tubes. Beam transmission was about 4% lower which can be attributed to the introduction of a contiguous grid. The rf-output power was about 5% higher and cathode current and power input remained unchanged.

In summary it can be said that a substantial cost reduction was achieved and that the established tube cost goal was met. The cost goal was \$2836 in 1978

dollars. The costing as based on a single buy of 6000 tubes over a five year period and an unpackaged tube with magnets, high voltage pottings and leads. Assuming an 85% yield through test, the cost exercise carried out at the end of this program resulted in a tube cost of \$2809 again adjusted to the 1978 dollars for comparison.

## SESSION V - 2

### A DESCRIPTION OF NEW MANUFACTURING TECHNOLOGY FOR A HIGH POWER TWT

by

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This paper describes the results of a manufacturing methods and technology program that was sponsored by the United States Navy. The objective of this program was to achieve cost reduction of an existing high power pulse TWT by introduction of cost effective manufacturing methods and new technologies in order to meet a given cost goal. This program was carried out as a joint effort of two companies, Raytheon's Microwave and Power Tube Division and Teledyne MEC. Each company was addressing some special tasks which were in their area of expertise and in addition there were joint tasks. The cooperation between the two companies was excellent and there was a free exchange of information.

The TWT selected for this program was developed for the Navy's Active Expendable Decoy program. This TWT represents the absolute state of the art in the pulsed high peak power wideband helix TWT class. This TWT has a shadow grid controlled electron beam, is focused with a periodic permanent magnet structure, uses collector depression for improved efficiency and can be packaged in a conduction cooled package.

The tasks carried out during this program can be divided into four major categories. The first category consisted of tasks that concentrated on the cost reduction of the tube itself by looking at prime parts fabrication, the assembly tooling and inspection methods. The second category of tasks concentrated on cost effective fabrication methods such as attenuator deposition, helix winding getter processing and high voltage potting methods. The third category of tasks addressed the usage of automatic equipment during the fabrication process. Automatic helix winding was investigated and a helix winding and inspection machine was built. Automatic aging and test methods were developed and the equipment was designed and purchased. Automatic bakeout methods were studied and equipment was purchased.

## SESSION VI - 1

### "MM&T PROGRAM TO DEVELOP ADVANCED METHODS FOR FABRICATING ARSENIC SELENIDE GLASS"

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#### ABSTRACT

Amorphous Materials, Inc. was founded in 1977 to provide a source of infrared transmitting glass used in U. S. Army FLIR Common Modules. A Manufacturing Methods & Technology (MM&T) program was funded by the Army through the Night Vision Laboratory (NVL) to improve the ability of Amorphous Materials, Inc. to provide AMTIR-1 glass lens blank at a greater production rate and at lower cost to U. S. Army Common Module FLIR production programs. The twenty month program was very successful. Production & fabrication processes developed are discussed. Increases in through put and yield are discussed along with cost reductions.

## INTRODUCTION

### Background

The advent of mercury cadmium telluride detector arrays led to the use of a second infrared optical material coupled with germanium to provide color corrected lenses for FLIR systems. The most extensively used second optical material was an infrared transmitting glass, TI 1173, proprietary to Texas Instruments. Clearly, a second source of infrared transmitting glass was needed before the U. S. Army Common Module FLIR programs reached full production.

Amorphous Materials was founded in 1977 to provide the needed second source of infrared glass. The composition chosen for production was a germanium-arsenic-selenium glass which had been fully developed in a U. S. Air Force funded program. The trade name chosen was AMTIR from the acronym Amorphous Materials Transmitting IR.

### Qualification of AMTIR-1

A comparison of the physical properties of AMTIR-1 with those of TI 1173 reveals that the Ge-As-Se glass is actually a better material, harder, stronger and less susceptible to heat shock. Optically, the two glasses are about the same. Design studies indicated AMTIR could be substituted for TI 1173 in the TOW Night Sight with no measureable difference in performance provided the radius of curvature for glass elements was slightly changed. Substitu-

tion could then be made with no change in element spacing, no change in lens mount and no change in appearance of the elements.

An unsolicited proposal was submitted to the Night Vision Laboratory in April, 1978 suggesting that AMTIR-1 glass and lenses be prepared for evaluation as a direct substitute for TI 1173. The proposal resulted in a direct purchase by NVL of ANTAS lens elements through the Common Module program at Magnavox, Government Industrial Electronics Corp. at Mahwah, New Jersey. The lens elements were fabricated and coated at Optics Electronics Corp. of Dallas, Texas. Evaluation demonstrated AMTIR-1 lens elements met all system specifications. As a result, the U. S. Army ammended the data package allowing the use of AMTIR-1 as a direct substitute for TI 1173 in the ANTAS second source program which was awarded to Kollsman Instrument Company in the fall of 1978. Amorphous Materials, Inc. was designated for the first time as a second source of infrared transmitting glass.

#### Facility Development Program

The ability of Amorphous Materials to produce ANTAS blanks at that time was very limited. Even though the first year need for glass by Kollsman was not great, some support towards the development of the AMTIR-1 production facility was needed. In the fall of 1978, an unsolicited proposal was submitted to NVL by Amorphous Materials again through Magnavox. The program began in January and ended in the fall of 1979. The aid provided was mostly in the form of equipment needed to improve the quali-

ty and quantity of glass. Equipment was provided direct from DIPEC, purchased by Magnavox and shipped to Amorphous Materials, or designed and built by and at Amorphous Materials. A semi-automatic unit for compounding and casting glass was constructed. An IR refractometer was built and used to measure the refractive index of AMTIR-1 glass to demonstrate batch to batch variation meet print specifications. Methods to fabricate and evaluate ANTAS lens blanks were developed. The capacity to produce in excess of 70 ANTAS lens blanks was demonstrated. Based on the existing 6" diameter production process, approximately 125 acceptable ANTAS lens blanks could be produced per month. However, the Kollman ANTAS program alone required over 200 blanks per month. Clearly an increase in capacity was needed.

## MM&T PROGRAM

### General Approach

The purpose of the Manufacturing Methods & Technology program was to improve the ability of Amorphous Materials to provide high quality AMTIR-1 lens blanks at a greater production rate and lower cost to U. S. Army Common Module FLIR production programs. Capacity would be increased by casting larger diameter plates. Verification of glass quality and improved process reliability would lead to increased yield. Further cost reduction would occur through the development of processes to recast glass scrap and preshape lens blanks.

### Specific Goals

1. Develop a production process for 8" diameter cast plates. Demonstrate the performance of the process through the evaluation of 2 Engineering plates and 4 Production Run plates. Demonstrate a 70% yield for lens blanks cored from the plates.
2. Develop a production process for 10" diameter plates and demonstrate again as for the 8" plates, a 70% yield.
3. Develop a process for recasting scrap.
4. Develop a process for preshaping blanks through slumping.
5. Develop a quality assurance plan to monitor production processes.
6. Provide full documentation for all processes and demonstrate the processes publicly to representatives from the infrared community.

## RESULTS FOR THE PROGRAM

1. The production processes for 8" and 10" diameter plates were developed and documented. Capacity was increased to about 10,000lbs. per year. Potential blank yield per month stands at 1,820 in contrast to 125 per month at the beginning of the program. Casting yields have been 28% (1978), 55% (1979) and 80% (1980) showing the impact of the program. Glass actually cast was 240lbs. (1978) 1100 lbs. (1979) and 3,800lbs. (1980) illustrating the impact of the program on throughput. The overall yield value for 1980 was about 50%.

2. Engineering plates, Production plates and lens blanks cut from these plates met all quality and yield requirements for the program. The physical properties related to optical applications were remeasured and found to agree with previously reported values for the same composition.

3. A process for recasting glass scrap was developed and is currently in use. A slumping process was developed and demonstrated.

4. The public demonstration was held as scheduled with representatives from government and industry present.

5. The price of ANTAS blanks sold by Amorphous Materials has remained essentially the same since 1979 even though the cost of germanium, the major material cost item, has tripled during the same time frame. The continued low cost is due to improved yield and blank fabrication methods.

SESSION VI - 2

**CO<sub>2</sub> WAVEGUIDE LASER MANUFACTURING TECHNOLOGY**

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## ABSTRACT

CO<sub>2</sub> waveguide lasers have been identified as critical sources for a number of Navy and Marine Corps applications. Some key cost drivers for these devices were identified in FY 78, and Phase I of a two-phase effort was initiated to address them. Honeywell's Systems and Research Center won the competitive procurement for Phase I and demonstrated techniques for low-cost waveguide bore production, inexpensive optical and mechanical seals, and a number of other processes resulting in a tenfold cost reduction on these devices.

The paper will describe these processes and relate them to cost reduction and redistribution of effort. Finally, the Phase II effort (recently awarded to Honeywell) will be described. The Phase II effort is basically a pilot run of 25 units, utilizing the techniques and methodology demonstrated in Phase I.

## BACKGROUND

CO<sub>2</sub> waveguide lasers provide a small but powerful source of coherent radiation in the 9- to 11-micrometer region of the spectrum. The device described in this paper operates in a continuous wave (CW) mode, while similar devices have been operated in pulsed modes. CO<sub>2</sub> lasers are receiving considerable attention due to their forward-looking infrared (FLIR) compatibility (based on performance in low-visibility situations), eye safety, and frequency stability (which allows them to be used in coherent detection systems). The CO<sub>2</sub> laser is one of the most efficient lasers available (electrical energy input to optical energy output). The particular device described here has the added advantage of a rugged design based on a monolithic ceramic structure (Figure 1). These points are summarized in Table 1.

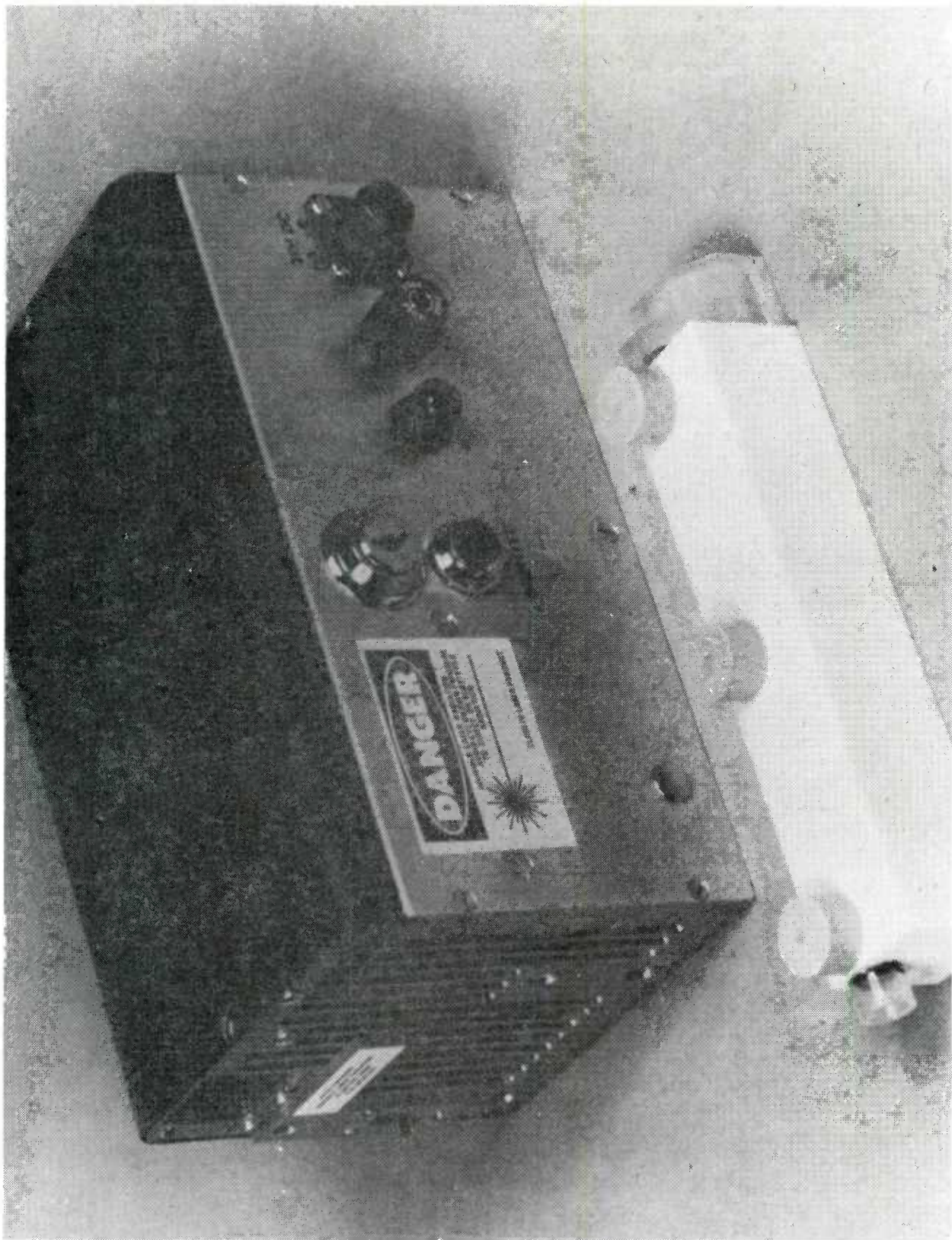


FIGURE 1 CO<sub>2</sub> Waveguide Laser.

TABLE 1. Waveguide CO<sub>2</sub> Laser.

Device .....	<p>Laser provides a highly collimated output beam for efficient use of energy.</p> <p>Continuous output.</p> <p>Carbon dioxide laser for far infrared (10.6 μm wavelength).</p> <p>Waveguide for compactness.</p>
Advantages .....	<p>10.6 μm for smoke and haze penetration, eye safety, and FLIR compatibility.</p> <p>High efficiency.</p> <p>Very stable, rugged mechanical design.</p>

**APPLICATIONS**

At the start of the manufacturing technology (MT) effort, only a few applications of this device had been specifically identified. These were for use in FLIR compatible beacons and in missile fuzing. Since that time a number of related efforts in all of the services have emerged that will benefit from the cost reduction efforts of this MT program. Some of these programs are listed in Table 2. They include beam riders, laser radars, and a number of specialized requirements. Although the MT program specifically addresses CW sources, many of the methods and techniques that have evolved can be applied to pulsed versions of these CO<sub>2</sub> lasers.

**OBJECTIVE**

The objective of the CO<sub>2</sub> waveguide laser MT program was to achieve a significant (one-tenth) cost reduction in a CO<sub>2</sub> waveguide laser. A small 2-watt device was chosen as the vehicle for demonstrating the cost reduction, but all of the techniques have been evaluated for applicability to higher power (i.e., longer) devices. This program then represents a generic solution to reducing the cost drivers in a whole family

TABLE 2. CO<sub>2</sub> Waveguide Laser Applications.

Forward edge battle area identification .....	FEBA	NWC
Optical communications .....	...	NOSC
Fuzing .....	...	NWC
Beam rider missiles .....	...	McDonnell Douglas (MIRADCOM) Martin Marietta Northrop/Sanders
CW laser radar .....	Multifunctional NOE IR-STARTLE MICOS	AVRADA NVEOL WPAFB
Laser assisted air rescue system ....	LAARS	NWC, WPAFB
Remote toxic gas sensing .....	...	Edgewood
Countermeasure laser .....	...	WSMR
Threat warning system .....	...	WPAFB

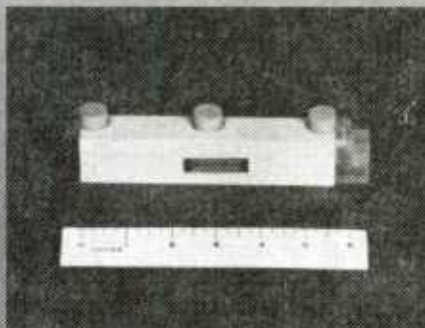
of CO<sub>2</sub> waveguide lasers. Figure 2 shows the basic 2-watt device and also 5- and 10-watt sources that have evolved from this design.

#### APPROACH

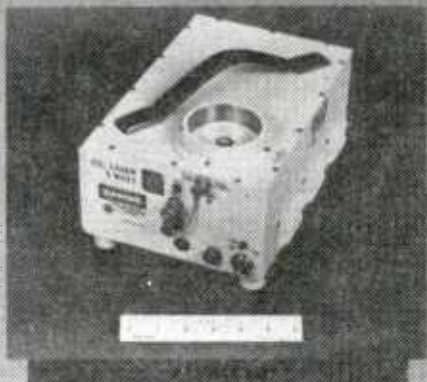
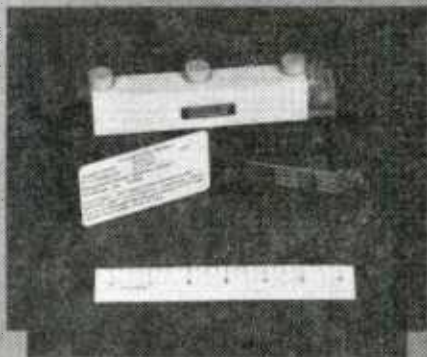
The MT program was divided into two phases, listed in Table 3. The first phase identified the major cost drivers and set up specific subtasks to be accomplished in order to achieve the required cost reduction. In particular, laser bore fabrication, block finishing, vacuum seals of components (electrical and optical), and electrode fabrication were highlighted as critical labor intensive tasks. Quality assurance and reliability plans were generated for use in batch runs. A more complete breakdown

# CO<sub>2</sub> WAVEGUIDE LASER EVOLUTION

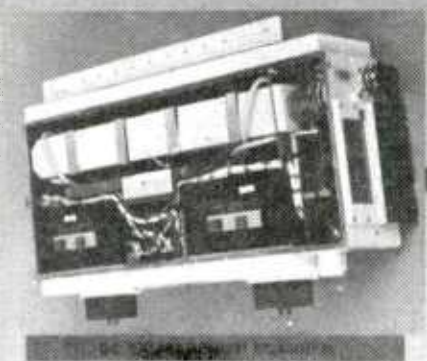
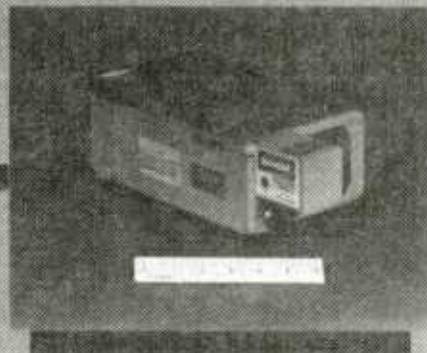
## MANUFACTURING TECHNOLOGY



2 WATT CO<sub>2</sub> LASER



6 WATT CO<sub>2</sub> LASER



10 WATT CO<sub>2</sub> LASER



FIGURE 2 CO<sub>2</sub> Waveguide Laser Evolution.

TABLE 3. Program Goals.

Phase I . . . . .	<p>Reduce cost of laser assembly from present single unit cost of \$9000 to thousandth unit cost of \$900 (79% learning curve) through improved techniques for:</p> <p>Laser waveguide bore fabrication          Surface finishing of block          Vacuum sealing of electrodes          Fabrication of electrodes          Optical seals and alignment</p>
Phase II . . . . .	<p>Implement Phase I processes in the build and test of 25 lasers.</p>

of the Phase I tasks is given in the block diagram (Figure 3). A unit cost reduction to below \$900 a copy was the target for a 1000-laser-unit build.

The second phase involved applying the processes established in Phase I to a small (25-unit) pilot run. The run would allow the generation of a suitable data base to allow verification of the suitability of the overall manufacturing process.

**DESCRIPTION OF SUBTASKS**

Each subtask under the Phase I program will be reviewed in the following sections. In many cases, a number of iterations were required to arrive at the final process. For the purposes of this paper, only the approach ultimately selected for each process will be described.

**WAVEGUIDE BORE FABRICATION**

Since the device selected for the demonstration involved a rugged monolithic ceramic structure, some means was needed of introducing the long ( $\approx 6$ -inch) and narrow ( $\approx 1.5$ - to 2.5-millimeter) waveguide bore into the ceramic structure. The pre-MT approach involved drilling these small bores in the extremely hard (second only

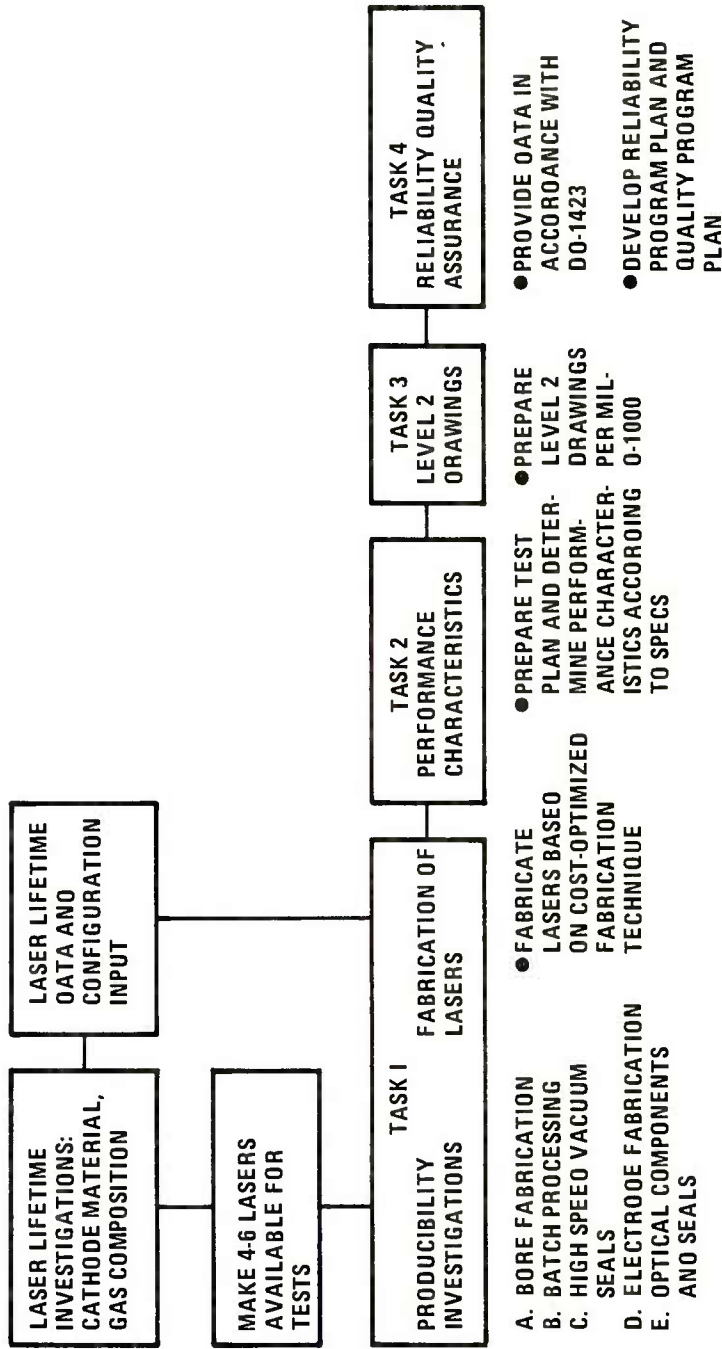


FIGURE 3 Major Elements of MM&T Program: Development of Manufacturing Methods and Production of Axial Discharge CO<sub>2</sub> Waveguide Lasers.

to diamond in hardness) alumina blocks. Costly and time-consuming drilling operations were required to achieve the straightness and smoothness required for low-loss waveguide bores. The approach selected to reduce costs involved the drilling of the bores in the soft (green or unfired) state of the alumina. Figure 4 shows the alumina powder, which is isostatically (actually hydrostatically) pressed in blocks having the consistency of chalk. These pieces can then be easily cut, shaped, and drilled with conventional tools to produce the desired shape. The key issue was whether these bores would remain smooth and straight after the high-temperature firing required to bring the alumina to its optimum properties. Sixteen units were fabricated by this method, but a means to evaluate their characteristics had to be developed. A method was used that involved filling the laser bore with mercury and then X raying the part (from at least two sides) with inspection master blanks alongside. Then an optical comparator could be used to evaluate the straightness (deviation) of the bores. Figure 5 shows sample X rays of these parts. A typical graph of deviation obtained by this method is shown in Figures 6 and 7 (side and top profiles). Figure 8 shows the two-axis deviation of the 16 sample blocks, which ultimately resulted in an 80% yield. Subsequent testing of this method indicates that the waveguide bores (1.5-mm diameter) can be made up to 9 inches long using this method.

#### **SURFACE FINISHING OF BLOCK**

The monolithic waveguide CO<sub>2</sub> laser structure utilized an internal mirror system that involved the mounting of the optical elements directly to the ends of the ceramic block. The surface flatness and parallelism of the ends of the block were considered extremely critical, and this was a time-intensive operation also. Fixtures were needed to support batch processing, but more critical was the evaluation of whether a single-step process could produce the surface characteristics required. The time-intensive

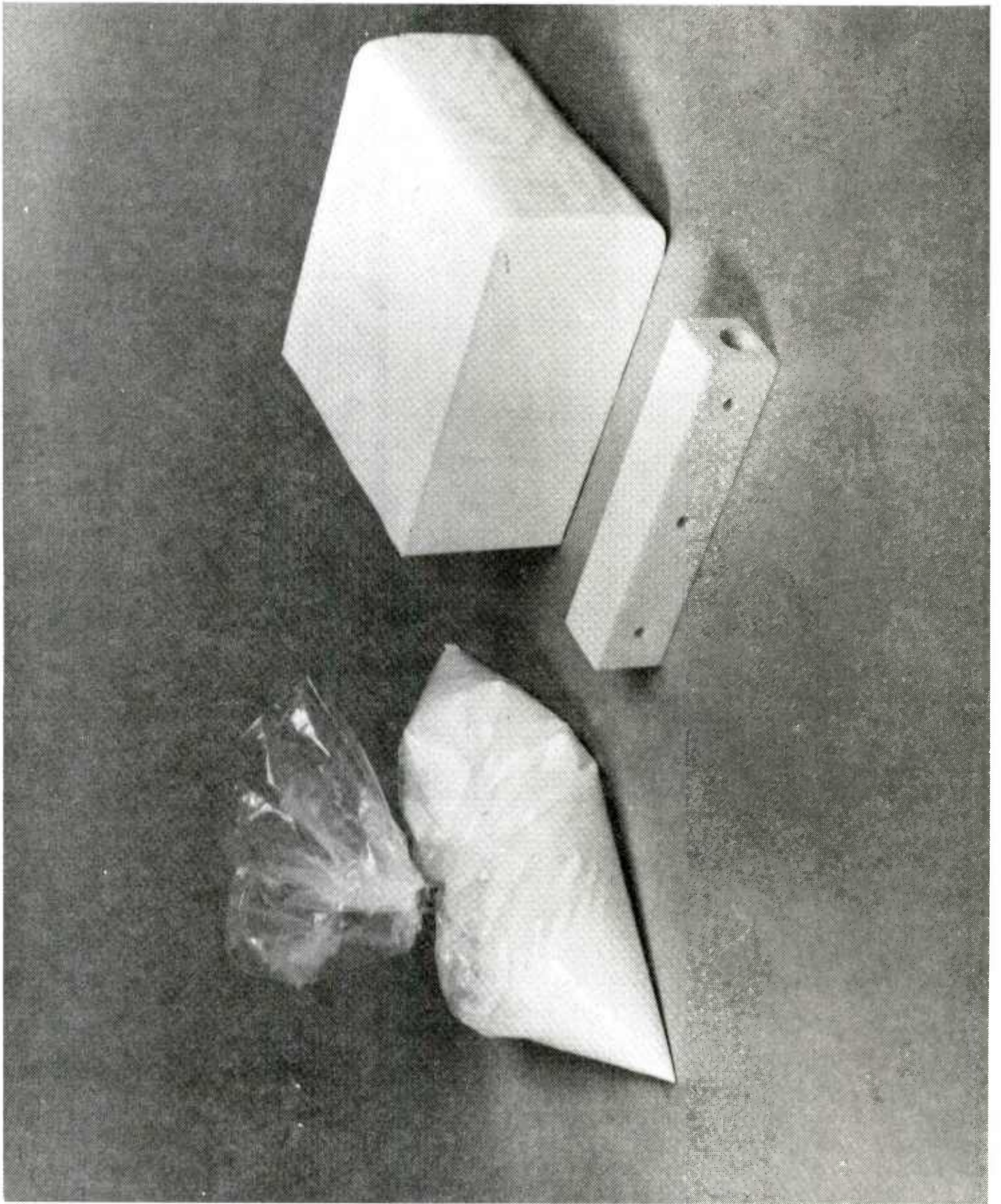


FIGURE 4 Alumina Powder, Pressed Block, Unfired Part.

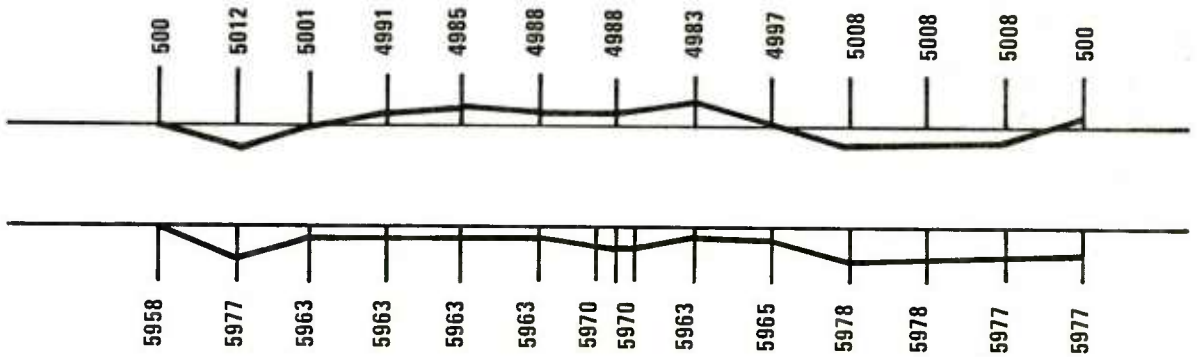


FIGURE 5 X-ray Photo of Block for Measurement of Bore Straightness.

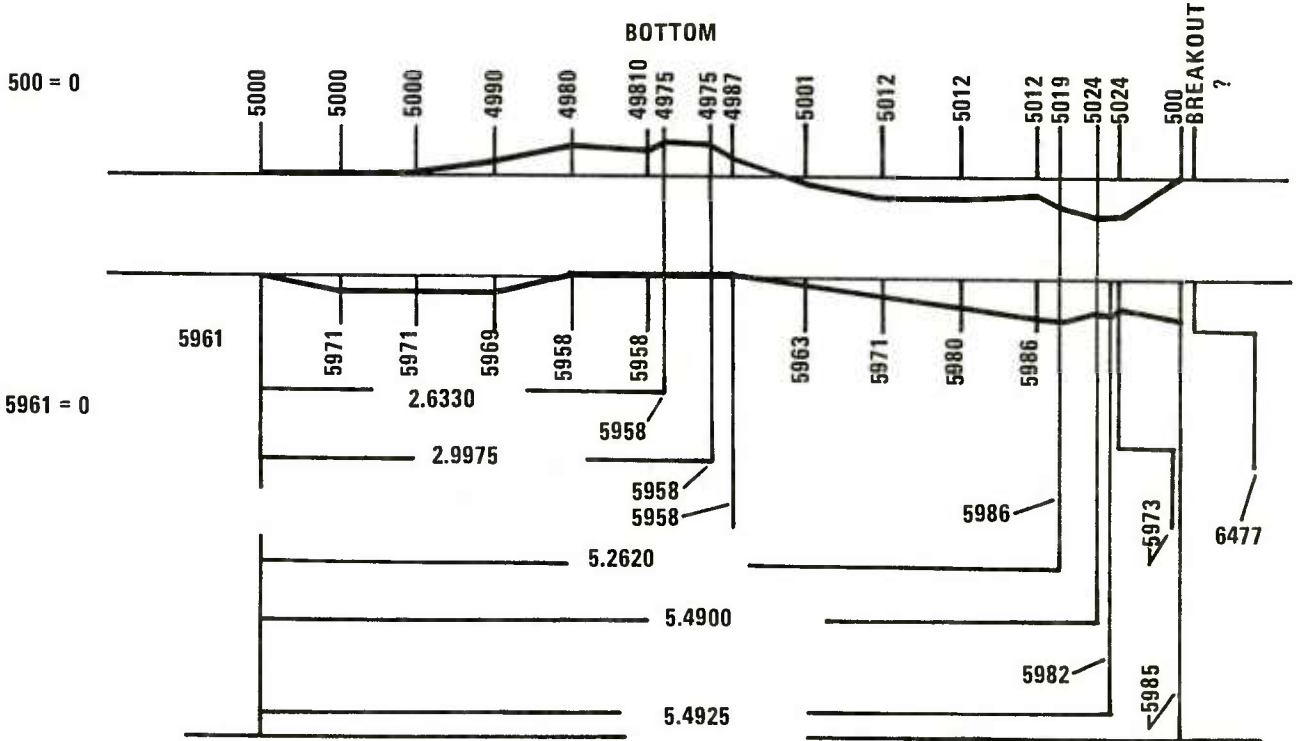
500 = 0

S/N 235  
TOP

.01 = .0001



5958 = 0



Figures 6 and 7. Typical Graph of Deviations along Bore

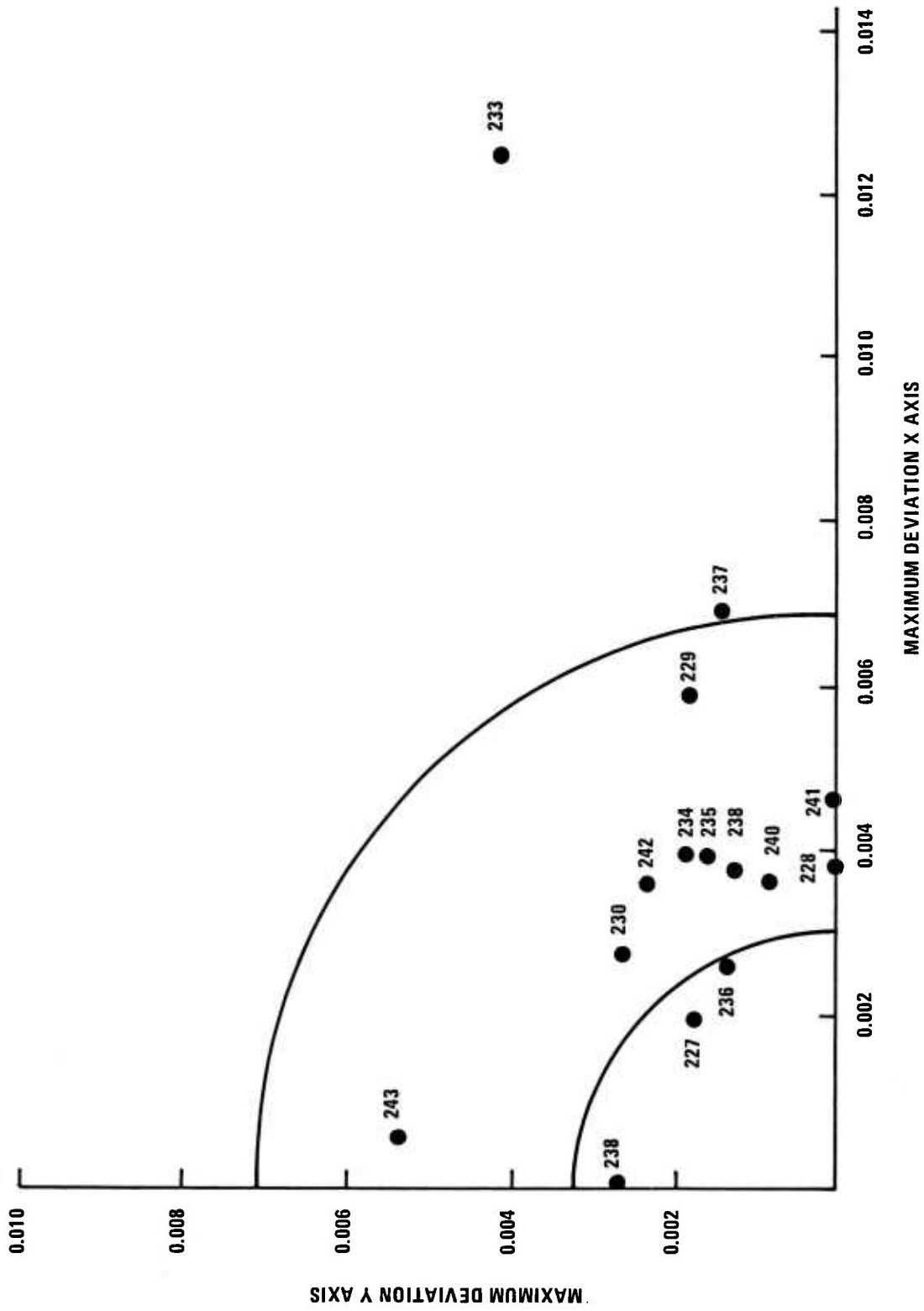


Figure 8 Straightness of Blocks Drilled in Green State

lapping and polishing operations were replaced with a single-step grinding process. This result is summarized in Table 4. Figure 9 shows one of the batch-processing assemblies considered for the larger volume requirements anticipated.

## VACUUM SEALS

The CO<sub>2</sub> waveguide laser is a low-pressure device ( $\approx 100$  torr or  $1/7$  atmosphere) and requires excellent seals to guarantee long lifetime and freedom from contamination. The original devices used a gold-indium seal developed by Dr. U. Hochuli of the University of Maryland. Although this seal yielded excellent results, it was extremely time intensive in its preparation and did not lend itself to multiple simultaneous sealing operation. Instead, a pressed indium metal seal was developed that could be used to make all the laser system seals. The application of the pressed indium seal to electrode connections and fill ports was demonstrated early in the program and is summarized in Table 5. The adaption of this sealing method to the optical components was the source of numerous delays and frustrations. The optical components are relatively soft compared to the other parts of the waveguide laser. Small non-uniformities in the pressing rapidly resulted in damaged optics or misaligned systems. The final pressing configuration (Figure 10) involved a relief area to allow the indium to flow and seal uniformly. The press system used for all the pressing operations is shown in Figure 11. Once the optics are pressed into place a helium-neon alignment testing setup (Figure 12) is used to evaluate whether repressing is required.

## ELECTRODE FABRICATION

At the start of the program, a number of metallic electrode structures were being considered. Typical materials included nickel, aluminum, copper, and copper-silver alloys. During Phase I, Dr. U. Hochuli of the University of Maryland, under

TABLE 4. Surface Finishing of Block.

Goal . . . . .	Reduce the cost of fabricating seal and alignment surfaces through batch processing of parts in lapping and polishing operations.
Status . . . . .	Lapping and polishing operations eliminated through process improvement in sealing operation.  Grinding operations improved through definition of multiple fixturing of parts in vertical spindle machine.

TABLE 5. Baseline Indium Seal Parameters for Metal Parts.

---

Finish of 45-50  $\mu$ in. (ground with 220 wheel)

Indium wire 0.015-in. diam.

Pressures on ram of 1-in. diam.

Anodes	1200 psi	5 min
Cathode cap	1200	5 min.
Fill port	2000	5 min.

Sliding yield

50 to 60 lb for 0.6-in. diam. seal (cathode cap)
25 to 38 lb for 0.38-in. diam. seal (anode)

Pulling yield

95 to 110 lb for 0.6-in. diam. seal (cathode cap)
65 to 80 lb for 0.38-in. diam. seal (anode)

Leak rate less than  $2 \times 10^{-11}$  standard  $\text{cm}^3/\text{s}$

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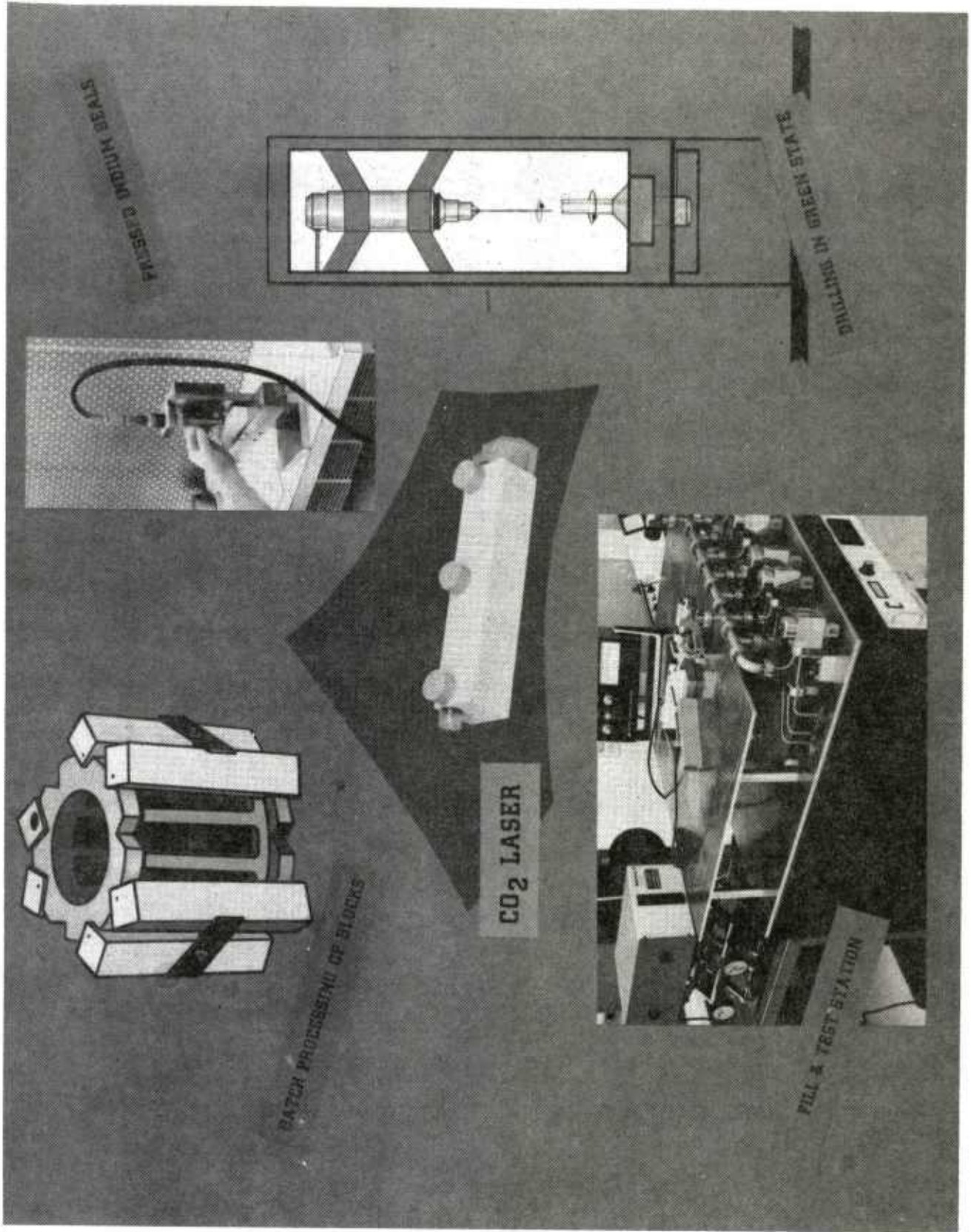


FIGURE 9 Batch Processing (Top Left).

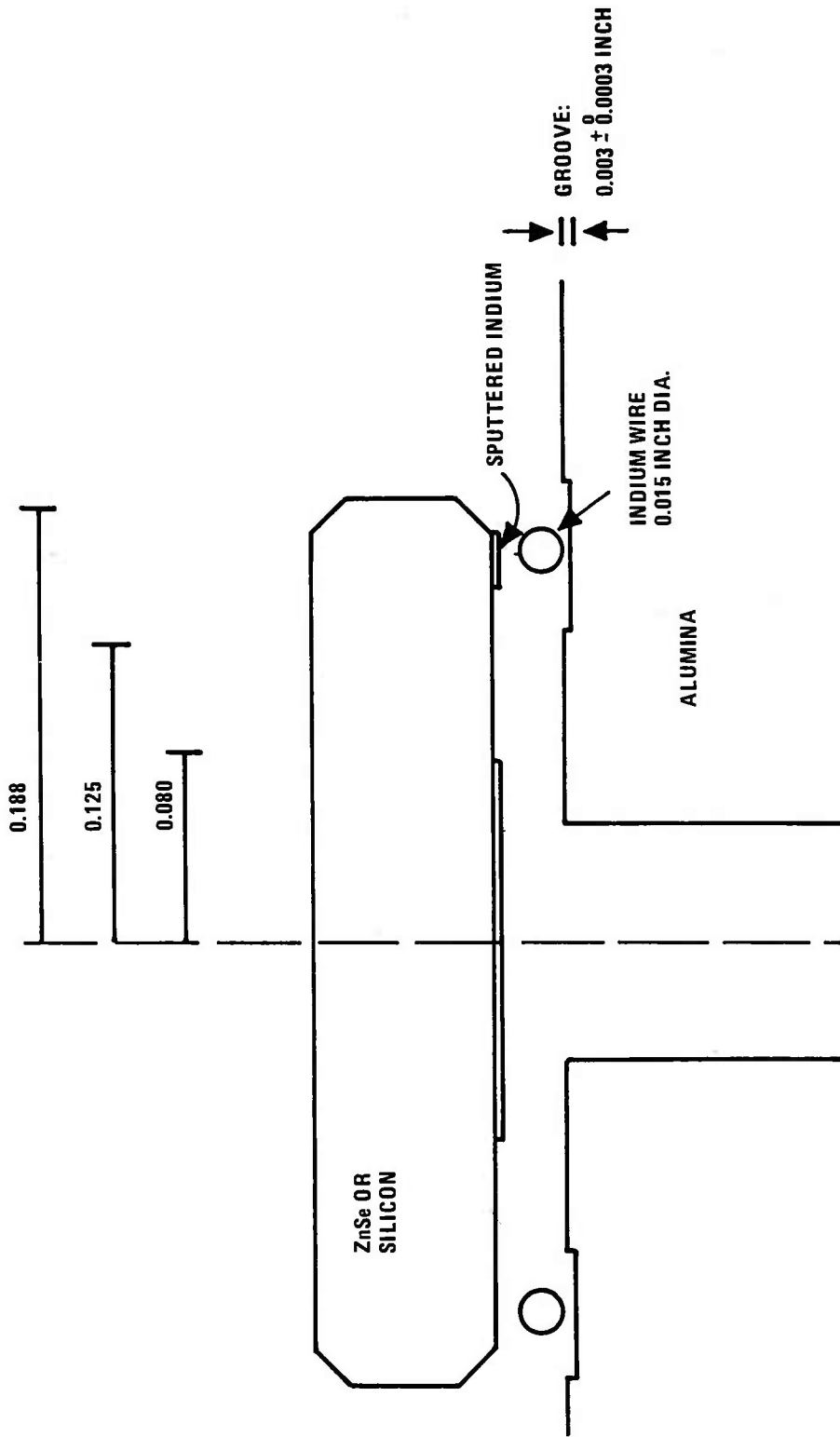
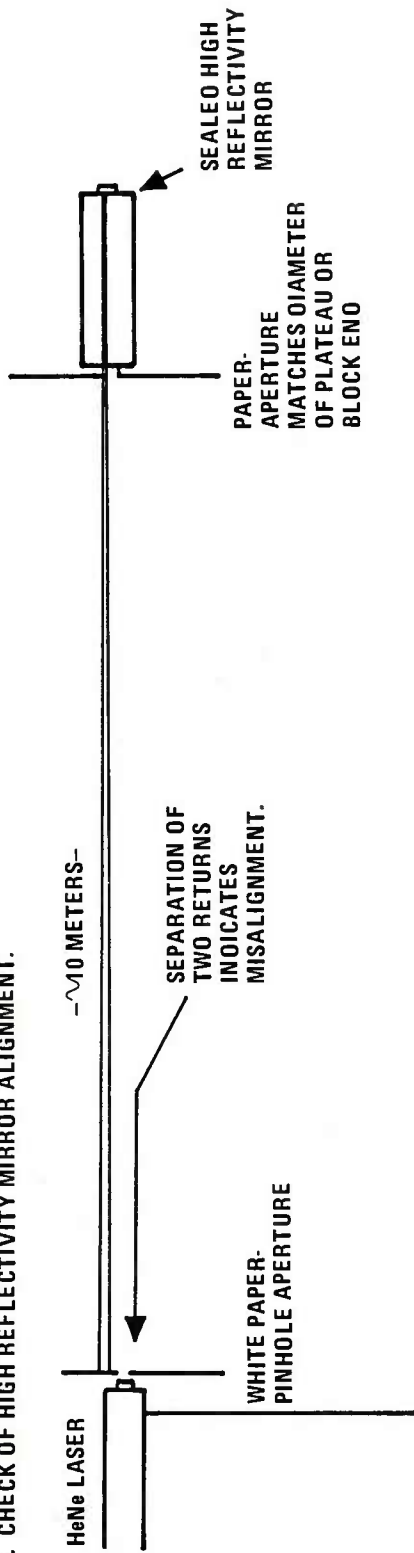


Figure 10. Geometry for Pressed Indium Mirror Seal



FIGURE 11 Pressing System For Seals.

a. CHECK OF HIGH REFLECTIVITY MIRROR ALIGNMENT.



b. CHECK OF OUTPUT COUPLER ALIGNMENT

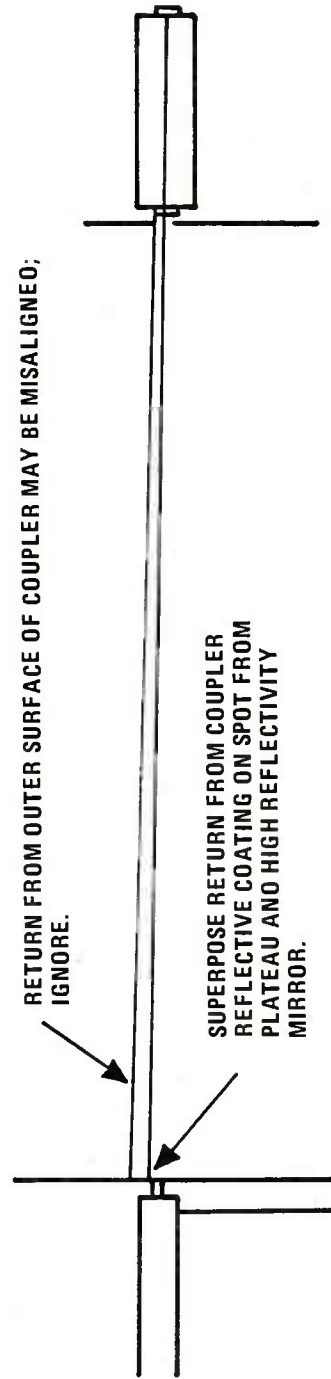


Figure 12. Mirror Alignment Checks Using He Ne Lasers

ONR support, developed a semiconductor material (lithium-nickel oxide) which exhibited far superior properties for use in cathodes. A gold-plated aluminum pin was selected for the twin anodes. Electrode fabrication and assembly were then optimized for these two types of electrodes (Figure 13).

## **FINAL ASSEMBLY AND TEST**

Table 6 lists the remaining operations required to complete the laser assembly and ready the unit for testing. A fill station (Figure 14) provides access to the vacuum system, gas supplies, and final pinch-off for sealing. The waveguide laser is then evaluated with respect to critical operating parameters such as output power, beam divergence, output wavelength, amplitude and frequency stability, and for selected units operating lifetime. Under Phase I, device operating lifetimes were set at 500 hours to the half-power points. Under a separate contracted effort, four units are being set aside for shelf life testing. These units will be tested every 3 months until they decline to unacceptable operating characteristics.

## **SUMMARY OF PHASE I**

The Phase I effort concluded in June 1981 with the receipt of all deliverables (laser units, final report, drawing packages, etc.). The units were evaluated and judged to be in compliance with the goals of the Phase I project. In terms of the cost impact of the Phase I effort, Table 7 summarizes this evaluation. The cost per unit is reduced from \$7800 per unit to \$845 per unit (almost a tenfold reduction). The redistribution of effort is also shown in Table 7, as are the specific subtasks accomplished to achieve these goals. Although 10 lasers were built under this program, only four operating units (the others had undergone life-testing or some other use) were delivered to NWC. Table 8 summarizes the properties of these units.

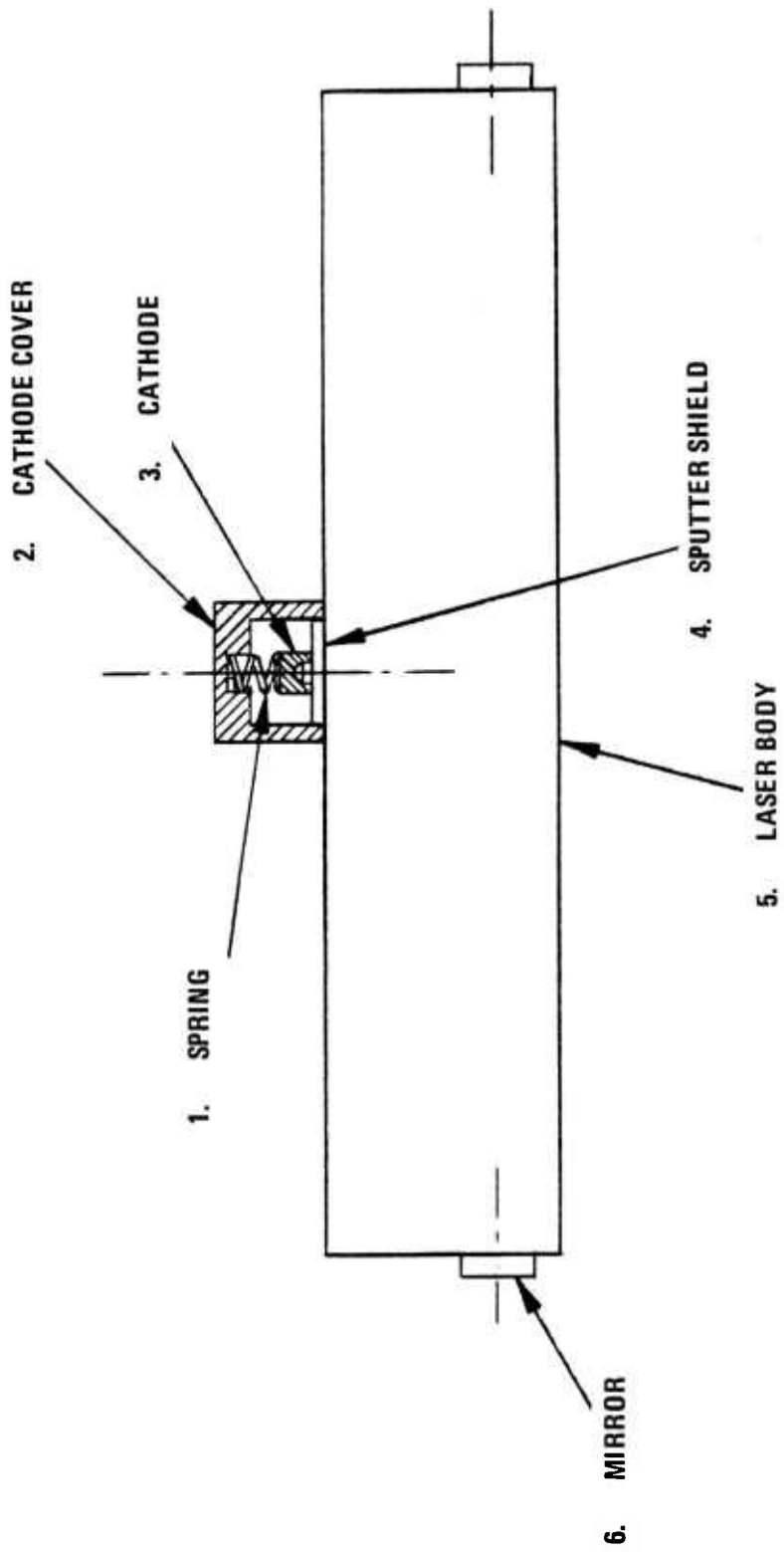


Figure 13. Cathode Assembly

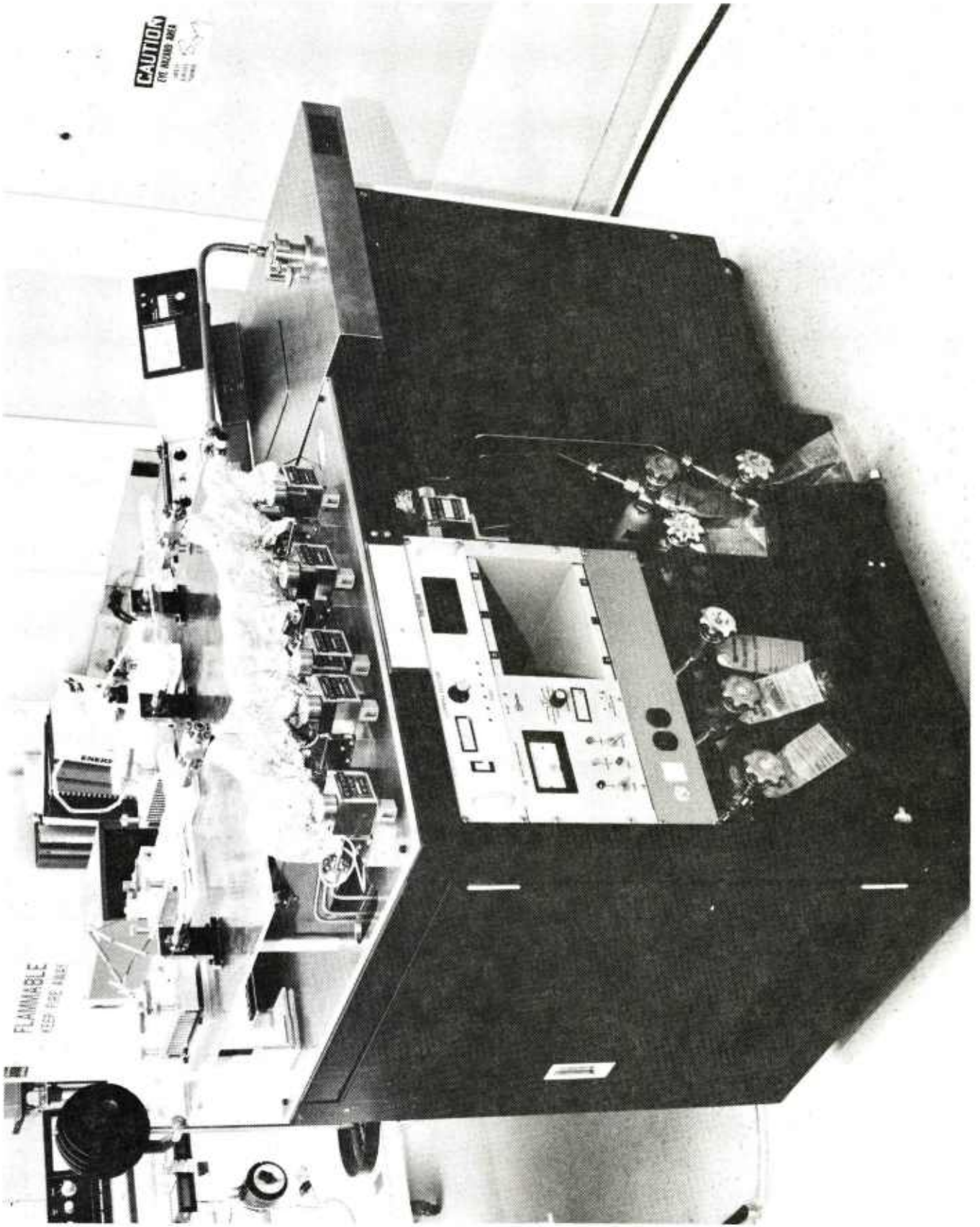


FIGURE 14 Fill and Test Station.

TABLE 6. Final Process Steps.

---

The laser fabrication process is completed by:

Evacuating

Filling with CO<sub>2</sub>, CO, He and Xe gases

Fill station tests

Sealing

Final acceptance testing.

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## FUTURE PLANS

The kickoff meeting for the Phase II effort is scheduled for 27 October 1981. The actual building of the 25 units under the pilot run should be completed by summer 1982. Currently a number of government laboratories and six NATO nations have requested sample units for evaluation. CO<sub>2</sub> waveguide laser devices will be distributed as they become available, and test data will be collected and reduced to obtain trends for the pilot run devices.

TABLE 7. CO<sub>2</sub> Waveguide Laser Cost Comparison.

Present technique (1-2 each cost) \$7,800	Method	Task	Predicted technique (1000 each cost) \$845
11% fill station and testing	Production methods	Task 1E WBS AF	19% fill station and test
12% optical seals and electrode seals	Vacuum seals and optical part sealing	Task 1C, 1E WBS AC	11% seals
7% assembly	Lifetime development	Task 1G WBS AF	14% cleaning and installing misc. parts
14% misc. parts and material	Standard machine shop procedures		2% misc. parts
10% electrodes and fill tube	Electrode fabrication	Task 1D WBS AD	10% electrodes
14% mirrors	Standard vendor volume processes		14% optics
9% lapping and polishing	Block lapping method	Task 1B WBS AE	4% lapping
23% block material and machining	Block boring method	Task 1A WBS AA	26% block material and machining

TABLE 8. Laser Performance and Waveguide Quality.

Lasers delivered, operating	Peak power at 4 mA, W	Modes	Final bore, in.	Bore deviation, in.
228	2.5	EH <sub>11</sub>	0.094	0.0038
236 4-30-81	2.1	EH <sub>11</sub>	0.094	0.0030
233	1.7	Many	0.094	0.013
240	2.3	EH <sub>11</sub>	0.065	0.0038
241 4-15-81	2.4	EH <sub>11</sub>	0.065	0.0046

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Titles of the papers, and authors are:

<u>TITLE</u>	<u>AUTHOR</u>
Major Thrusts of the Hybrids Program	Dr. Victor Ruwe Dr. Dean McKee,
Hybrid Integrated CAM and Manufacturing of Microelectronics. HICADAM	Mr. Dean Keller Mr. John Hawk,
Ceramic Chip Carrier Technology	Dr. John Prokop
Precious Metal Elimination	Dr. John Crist
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Coating Process for Power Vacuum Tube Grid Wires	Mr. J. Dutkowski
Major Thrusts in the Electronics CAD/CAM Program	Mr. Gil Wagner
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CO <sub>2</sub> Waveguide Laser MT	Mr. Robert Hintz