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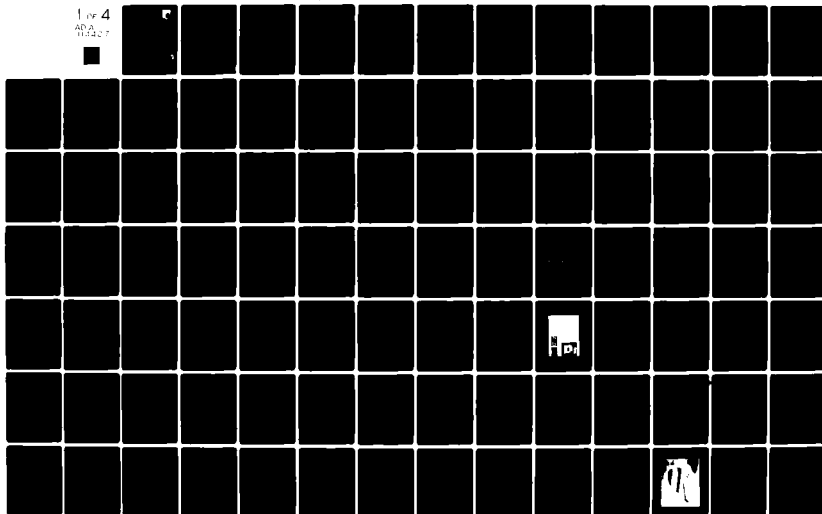
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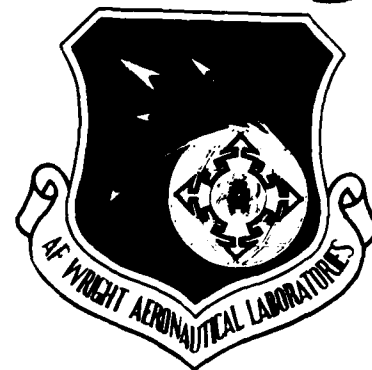
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MULTIFUNCTION MULTIBAND AIRBORNE RADIO
ARCHITECTURE STUDY

TRW DEFENSE AND SPACE SYSTEMS GROUP
ONE SPACE PARK
REDONDO BEACH, CALIFORNIA 90278

JANUARY 1982

FINAL REPORT FOR PERIOD APRIL 1978 - JANUARY 1980

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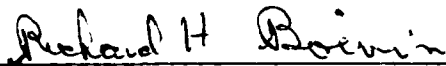


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→ and equipment with desired performance capabilities. The problem is further compounded by the lack of available space in the tactical aircraft, the transition of new equipment into the inventory, and the retention of many current systems. The multifunction multiband airborne radio system (MFBARS) program is formulated to explore the feasibility of producing a modern CNI system at an affordable life cycle cost (LCC) and within real estate requirements.

— A cost effective system approach was developed that revolved around high technology RF-LSI analog components that are in the development stage, high speed digital pre-processor elements and a programmable signal processor all under control of a host processor configuration. This design trades the ultimate gain in volume, weight and life cycle cost against a reasonable risk for the mid 1980's development.

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LIST OF ABBREVIATIONS

ADM	ADVANCED DEVELOPMENT MODEL
AFSAT	AIR FORCE SATELLITE
AFSATCOM	AIR FORCE SATELLITE COMMUNICATIONS
AGC	AUTOMATIC GAIN CONTROL
AJ	ANTI-JAM
AS	AMPLITUDE SHIFT
ASK	AMPLITUDE SHIFT KEYING
ATR	AIR TRANSPORT RACK
BIT	BUILT-IN TEST
BITE	BUILT-IN TEST EQUIPMENT
BPF	BAND PASS FILTER
BW	BANDWIDTH
C	CONNECTOR (BUS)
CCSK	CYCLIC CODE SHIFT KEYING
CMD	COMMAND
CMDS	COMMANDS
CNI	COMMUNICATION NAVIGATION IDENTIFICATION
DAIS	DIGITAL AVIONICS INFORMATION SYSTEM
DIP	DIPLEXER
DIP	DUAL-IN-LINE PACKAGE
DSPN	DOUBLE SIDE-BAND PSEUDO NOISE
DTDMA	DISTRIBUTED TIME DIVISION MULTIPLE ACCESS
EBS	ELECTRON BOMBARDMENT SEMICONDUCTOR
EMI/EMC	ELECTROMAGNETIC INTERFERENCE/ELECTROMAGNETIC COMPATABILITY
FH	FREQUENCY HOPPED
GPS	GLOBAL POSITION SYSTEM

LIST OF ABBREVIATIONS (CONT.)

HPF	HIGH PASS FILTER
IFA	INTERMEDIATE FREQUENCY AMPLIFIER
IFF	IDENTIFICATION, FRIEND OR FOE
IJMS	ITERIM JTIDS MESSAGE STANDARD
INS	INERTIAL NAVIGATION SYSTEM
JTIDS	JOINT TACTICAL INFORMATION DISTRIBUTION SYSTEM
LCC	LIFE CYCLE COST
LMS	LEAST MEAN SQUARE
LNA	LOW NOISE AMPLIFIER
LO	LOCAL OSCILLATOR
LPI	LOW PROBABILITY OF INTERCEPT
LRU	LINE-REPLACABLE UNIT
LSI	LARGE SCALE INTEGRATION
MFBARS	MULTIFUNCTION MULTIBAND AIRBORNE RADIO SYSTEM
MPSK	MULTI PHASE SHIFT KEYING
MSK	MINIMUM SHIFT KEYING
MSP	MATRIX SIGNAL PROCESSOR
MSP	MICRO SIGNAL PROCESSOR
NBF	NARROW BAND FILTER
NBFM	NARROW BAND FM
NOSC	NAVAL OCEAN SYSTEMS COMMAND
OAT	OXIDE ALIGNED TRANSISTOR
PELS	POSITION EMITTER LOCATION AND STRIKE SYSTEM
PEP	PEAK ENVELOPE POWER
PLL	PHASE LOCKED LOOP
PLRS	POSITION LOCATING REPORTING SYSTEM
PLSS	POSITION LOCATION AND STRIKE SYSTEM

LIST OF ABBREVIATIONS (CONT.)

PN	PSEUDO NOISE
PNFH	PSEUDO NOISE FREQUENCY HOPPED
PRICE	PROGRAMMED REVIEW OF INFORMATION FOR COSTING AND EVALUATION (RCA TERMINOLOGY)
PSF	POSITIVE SIGNAL FEEDBACK
PSK	PHASE SHIFT KEYING
PWB	PRINTED WIRING BOARD
RFLSI	RADIO FREQUENCY LARGE SCALE INTEGRATION
RF/IF	RADIO FREQUENCY/INTERMEDIATE FREQUENCY
S	SELECT (SWITCH)
SAM	STANDARD AVIONICS MODULE
SAW	SURFACE ACOUSTIC WAVE
SINGARS	SINGLE CHANNEL GROUND AND AIRBORNE RADIO SYSTEM
SSE	SINGLE SIDE BAND
SSP	SPECIAL SIGNAL PROCESSOR
SP4T	SINGLE POLE, FOUR THROW (SWITCH)
TACAN	TACTICAL AIR NAVIGATION
TBD	TO BE DETERMINED
TDMA	TIME DIVISION MULTIPLE ACCESS
T/R	TRANSMIT/RECEIVE
VCO	VOLTAGE CONTROLLED OSCILLATOR
VHSIC	VERY HIGH SPEED INTEGRATED CIRCUIT
VLSI	VERY LARGE SCALE INTEGRATION
4PST	FOUR POLE, SINGLE THROW (SWITCH)

1. INTRODUCTION AND SUMMARY

1.1 INTRODUCTION

The demands of modern military avionic communication, radio navigation, and cooperative identification (CNI) equipment has been greatly expanded as the result of the need for antijam (AJ), low probability of intercept (LPI), higher navigation accuracy, and increased volume of information transfer. These demands are verified in programs such as GPS, JTIDS, SEEK TALK, SINCGARS and AFSAT I and II. The cost of this additional capability has severely hampered the ability of the Government to procure new CNI systems and equipment with desired performance capabilities. The problem is further compounded by the lack of available space in the tactical aircraft, the transition of new equipment into the inventory, and the retention of many current systems. The multifunction multiband airborne radio system (MFBARS) program is formulated to explore the feasibility of producing a modern CNI system at an affordable life cycle cost (LCC) and within real estate requirements.

Another objective of the MFBARS program is the capability to accommodate the CNI systems in the 2 to 2000 MHz frequency band as tabulated in Table 1-1. Most of these CNI systems are currently under development; however, some currently operating systems were also included. Thus, in order to achieve the highest usefulness the MFBARS is required to be operational by the late 1980's.

The MFBARS program is divided into three phases: (1) System definition, (2) System design, and (3) Validation of the new technology required to implement the MFBARS baseline system developed in Phases I and II.

Phase I and II studies have been completed. The results are presented in this report, which is submitted in fulfillment of the CDRL requirement of contract F33615-77-C-1172.

Phase I concentrated on defining alternative architectures and developing an approach for economic comparison of the different architectures. Phase II efforts were devoted to system design, system analysis, and refinement of economic analysis of a selected MFBARS architecture. The design and evaluation of the adaptive antenna system and integrated

Table 1-1. MFBARS Baseline Capability

Function	Band (MHz)	Modulation	Tx Power (Watts)	Receiver Sensitivity	Equipment	Addressed?
HF Voice	2-30	SSB	400 WPEP	1 μ V 10dB SNR	ARC-112	Yes
VHF Voice	30-88	FM	1 or 10	0.5 μ V 10dB SNR	ARC-131	Yes
VHF Voice	108-156	AM	10	3 μ V 10dB SNR	ARC-115	Yes
UHF Voice	225-400	AM	10	4 μ V 10dB SNR	ARC-164	Yes
ILS/VOR	—	Pulse	—	—	ARN-108	No
Localizer	108-112	—	—	—	—	—
Glide Slope	329-335	—	—	—	—	—
Marker Beacon	75	—	—	750 μ V	—	—
TACAN	962-1213	Pulse	0.5 to 2K	-89 to -92 dBm	ARN-118	Yes
IFF Transponder	1090 Tx 1030 Rx	Pulse	500	-65 to -77 dBm	APX-101	Yes
IFF Interrogator	1030 Tx 1090 Rx	Pulse	1 to 2.5K	-80 dBm	APX-76	No
Future IFF	TBD	—	—	—	—	No
GPS Navigation	1228, 1575	DSPN	—	-36 dBm	—	Yes
JTIDS	960-1215	PNFH	200 to 800	—	—	Yes
SEEK TALK	225-400	DSPN	1	—	—	Yes
UHF SATCOM	225-400	FH	100	—	—	Yes
SINGAR	30-88	FH	—	—	—	No

inertial navigation system (INS) for MFBARS application were also utilized. In addition, the key technologies required to implement the selected baseline MFBARS system were identified in Phase II. A recommendation was made for the development of some high priority items on the basis of their cost and performance, as well as long-lead development time.

The work performed consisted of eight tasks each in Phases I and II as follows:

1) Phase I

- Task 1 - Identify areas of functional commonality across CNI systems and propose functional mechanizations in light of probable applications for each radio function. The primary input to this effort was a requirements analysis furnished by the Government.
- Task 2 - Identify and list significant tradeoffs and recommend approaches and criteria for the evaluation of alternative MFBARS designs. Make recommendations to advise the Government in selecting a suitable cost model approach, exercising the selected cost models, and in evaluating the results.
- Task 3 - Identify and evaluate technology for implementation of the functional mechanizations previously identified in task 1. The time frame of implementation, i.e., 1985, was evaluated against emerging technologies and a best fit recommended. Alternative technologies were also listed and identified.
- Task 4 - Generate and describe several different MFBARS architectures. Consideration was given to:
 - DAIS compatibility
 - Comparative economic analysis
 - Predictions of applicable technologies
 - Growth to accommodate new CNI systems
- Task 5 - Several cost models established in task 2 were exercised to provide quantitative assessment of the comparative economics of alternative architectures developed in task 4. Consideration was given to the entire life cycle cost, i.e., development, acquisition, installation and logistic support.
- Task 6 - High leverage cost drivers were identified and economic criteria developed for use in task 7.

- Task 7 - On the basis of results of tasks 1 through 6, as well as engineering judgement, a number of potential architectures were selected for further consideration. The output of this task was used to support the Government in establishing a rationale for evaluating these relatively unconstrained approaches, and to provide criteria for selecting those most promising for further investigation and detailed design efforts.
- Task 8 - The Phase I interim report documents all Phase I activity, presents the results of tradeoffs and analyses, and recommends architectures for the Phase II effort.

2) Phase II

- Task 1 - Generate preliminary designs on the selected approach to define the system architecture and obtain better assessment of technology requirements and system performance.
- Task 2 - Perform detail partitioning and detail design to achieve modularity and commonality of modules in the MFBARS system. The partition was based on technologies which can be achieved by 1985 or earlier.
- Task 3 - Perform conceptual design for a high performance, cost effective, integrated adaptive antenna array system for the MFBARS service.
- Task 4 - Generate an alternative system design on an integrated inertial navigation system for the MFBARS and determine the software requirements for each of the system designs.
- Task 5 - Update economic analysis and cost data from the results generated in the Phase II system design effort.
- Task 6 - Identify critical technology areas associated with the MFBARS realization and define and recommend technology validation tasks for Phase III.
- Task 7 - Phase II extension effort TBD.
- Task 8 - Preparation of a final report. Includes the results of Phase II extensions, as well as Phase I and II tasks.

The results of performing the tasks in Phases I and II are summarized in the following section and are presented, in detail, in the remainder of

this report. However, all Phase I materials not superseded by Phase II studies have been included in this report. The remainder of the report is organized into eight sections. The results of system design are presented in Section 2, which begins with a definition of system requirements and includes the description of the baseline system design. Section 2 finally describes the alternate system design developed in Phase I. Section 3 provides a short description of the results of partitioning the baseline system into modules/slices and line replaceable units (LRU). The adaptive antenna array study results comprise Section 4. Section 5 includes a detailed discussion of topics related to the design of RF/IF subsystems, including low noise and power amplifiers, RF LSI circuits, frequency synthesizers, and SAW devices. The microsignal processor design is described in Section 6. Sections 7 and 8 present the results of the integrated inertial navigation system study and the economic data analysis, respectively. The report concludes with the presentation of the definition and recommendations for technology validation tasks to be carried out in Phase III.

1.2 BASELINE SYSTEM

To fulfill the program objectives, Phase I was initially concentrated on conceptual definition, preliminary system design, and trade-off. Five major areas on each of the CNI functions were:

- 1) Frequency
- 2) Range
- 3) Modulation format
- 4) Spread spectrum processing
- 5) Transmit power requirement.

These were studied in order to set up requirements and develop MFBARS architecture. In developing alternative architectures, it was quickly determined that there were only two basic architectures and numerous variations within each architecture. The basic architectures are a centralized time-shared terminal and a distributed channelized terminal. A fully centralized terminal would involve digitizing at the antenna

and processing everything in an ultra high-speed digital signal processor running at near GHz clock rates. This approach was clearly beyond the MFBARS technology time frame.

Thus, the RF architecture reverted to the conventional chain of preselector, downconverter, IF amplifier, and signal processing with one such channel used for each frequency/band/service. For the nonspread spectrum, service is sufficiently narrow in bandwidth and limited dynamic range to be further processed by state-of-the art digital techniques. Thus, the architectures which were evaluated in the study were basically limited to centralized and distributed signal processing.

The TRW recommended baseline is a hybrid architecture where the RF front end is essentially a distributed channelized system, which is reassembled and processed at a central microsignal processor.

The proposed MFBARS architecture places great emphasis on employing standard modules. TRW's approach to achieve standardized modules is based on the realization that all CNI systems can be broken down into five basic processing/operating subsystems (Figure 1-1):

- Antenna System (with or without adaptive processor)
- Frequency dehoppping converter
- PN correlator/IF processor (programmable to achieve functional requirements)
- Microsignal processor (MSP)
- Transmitter.

The antenna system is envisioned to consist of either conventional nonadaptive antennas or adaptive array. When antijam requirements exceed the capabilities of the original system, adaptive antenna arrays are to be used. Otherwise, conventional antennas are sufficient. Preselectors, when needed, are also included as part of the antenna system. The main functions of the frequency dehoppping converter channel are to: (1) convert the incoming signal covering the frequency spectrum of 2 MHz to 2 GHz into a common IF, (2) perform dehoppping, if necessary, and (3) reduce the output dynamic range by means of AGC. The PN correlator/IF processor performs PN despread and/or processes the IF signal into a suitable form.

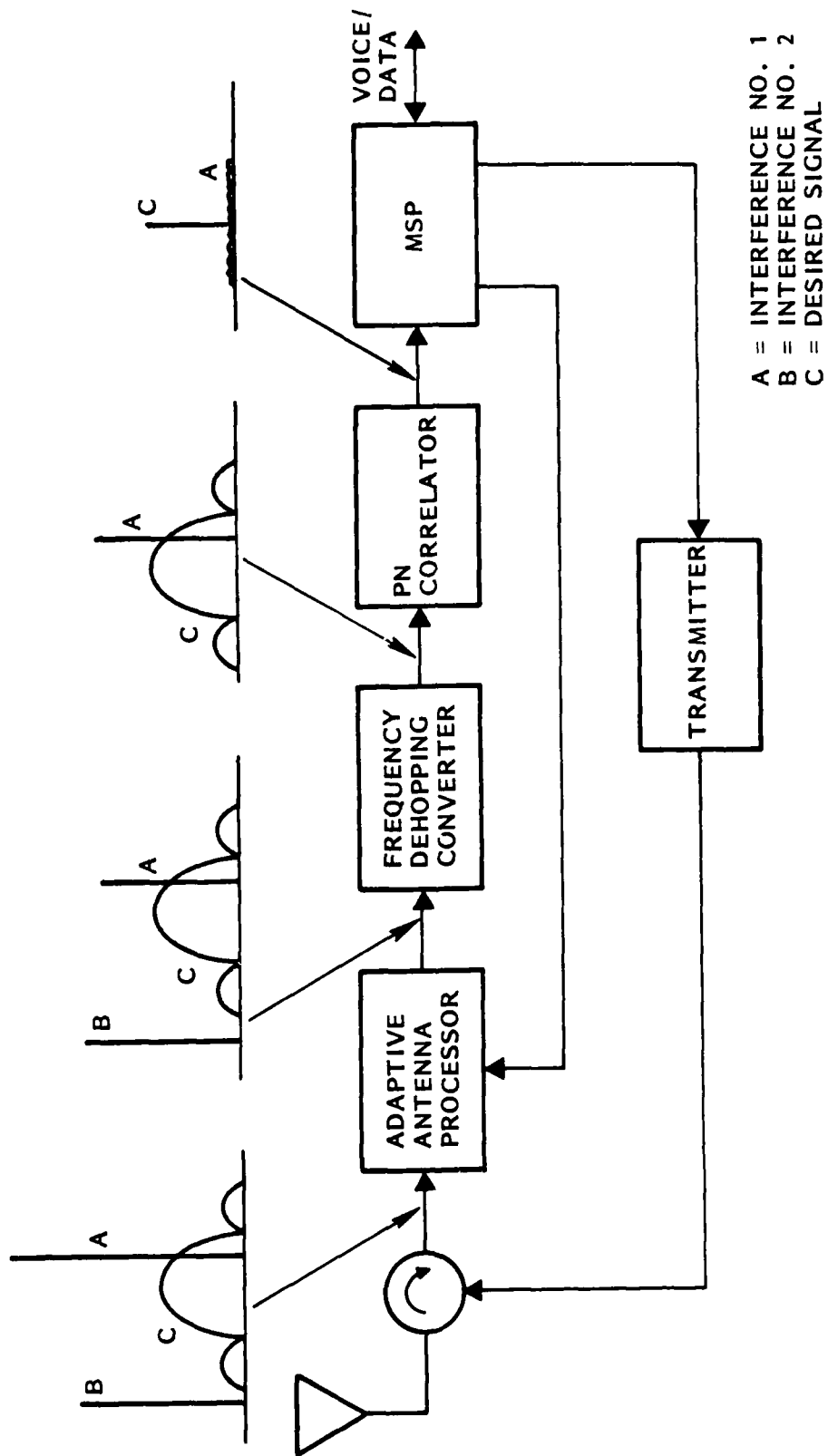


Figure 1-1. Generalized Multifunction Multiband Radio System (MFBARs)

and at a sufficiently low rate for processing at the microsignal processor. The final signal processing step takes place in the microprocessor, which maintains basic control of the MFBARS terminal as well as of the demodulation, synchronization, detection of the received signal, and interfacing with terminal users via the DAIS bus. For transmission, the microsignal processor codes the user input into a suitable signal waveform. Coding may involve spread-spectrum coding, error correction/detection coding, and simple formatting. The transmitter/exciter performs the modulation, frequency hopping, and amplification to the proper power level for transmission.

Ideally, the proposed system concept could be implemented with one design for each of the five operating subsystems covering the entire three decades of frequency range (2 to 2000 MHz). (Refer to Figure 1-1). The MFBARS terminal can then be configured with as many subsystems as required to accommodate the CNI user requirements. For added flexibility and reliability matrix switches can be used to cross strap the five operating subsystems.

However, technology limitations will not allow such an implementation. Fortunately, the CNI function in MFBARS does not require continuous coverage of the entire frequency range and can be easily broken down into two separate bands; the higher frequency band covers the L-Band of 960 to 1575.42 MHz and includes the GPS, JTIDS, TACAN and IFF functions, and the lower frequency bands cover from HF to UHF (2 to 400 MHz). The TRW baseline system is configured on the basis of this frequency separation. The designs for these five subsystems are described in detail in the following paragraphs.

1.2.1 Antenna

When conventional antennas are used, seven antennas are required to cover the frequency range and to overcome the aircraft blockage. As shown in Figure 1-2, the seven antennas are:

<u>Antenna</u>	<u>MHz</u>
● GPS	1228 to 1575
● L-Band top	960 to 1215

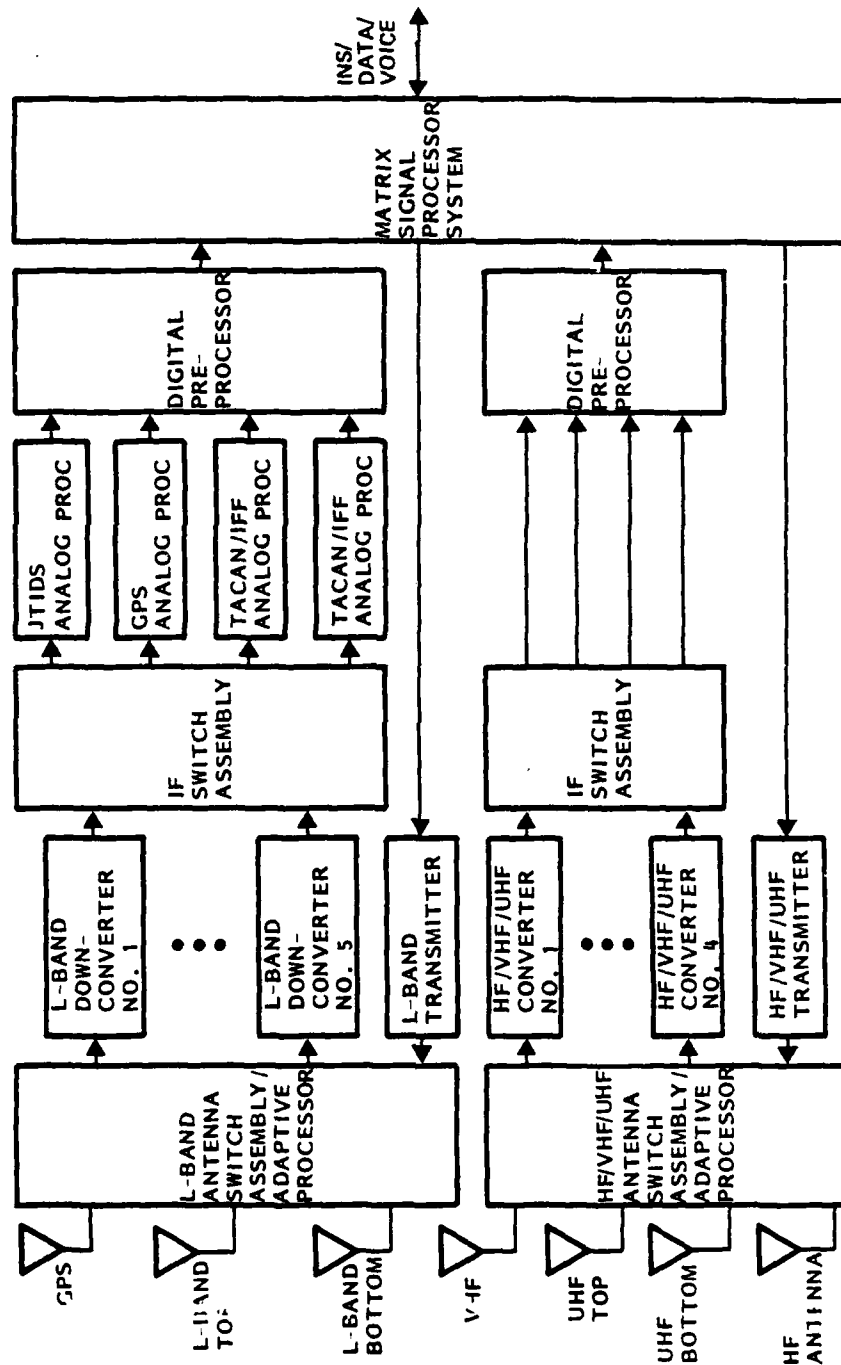


Figure 1-2. MFBARS Block Diagram, TRW Design

- L-Band bottom 960 to 1215
- UHF top 100 to 400
- UHF bottom 100 to 400
- VHF 30 to 100
- HF 2 to 30

When the adaptive antenna is contemplated, preliminary studies indicate that two adaptive antenna arrays are needed. One antenna array covers the L-Band and will replace the GPS, L-Band top and L-Band bottom, serving GPS and JTIDS simultaneously. The other covers the UHF band and replaces the UHF top and UHF bottom antennas. The resulting array serves the SEEK TALK and SINCGARS. The recommended adaptive antenna array processor design is based on the hybrid digital analog approach where beam-shaping is performed with analog circuits and the adaptive algorithm is processed by means of a digital processor. Even though the configuration recommended shares some of the receiver RF/IF circuits, the adaptive antenna system is basically separate and allows the MFBARS receiver to be used without the adaptive antenna system for those applications which do not require additional AJ protection of null steering.

1.2.2 RF Frequency Dehopping Converter

Two RF frequency dehopping converter designs are proposed for the MFBARS. One covers the L-Band and the other HF/VHF/UHF. The main functions of the converters are to translate the incoming signal into a common IF, 70 MHz for the HF/VHF/UHF and 186 MHz for L-Band. A fast hop frequency synthesizer is also included as part of the RF converter to accommodate spread-spectrum systems using frequency hopping, i.e., JTIDS, AFSATCOM, etc. Two indirect frequency synthesizer designs are used to cover the two separate bands. The L-Band frequency synthesizer covers the JTIDS requirements and the other synthesizer is used to process the HF/VHF/UHF signals which include AFSATCOM and SINGARS. The converter also includes variable gain RF and IF amplifiers which can be used as AGC amplifiers to reduce the dynamic range at the output.

1.2.3 PN Correlator/IF Preprocessor

The desired approach of having a single design programmable PN/correlator preprocessor also has to be compromised because of the diversity of waveforms and processing speed requirements. At one extreme, the GPS and JTIDS signals are spread with 10 MHz PN code, whereas the HF voice as a conventional single sideband AM requires only 3 kHz IF bandwidth. However, partial design standardization can be achieved and the MFBARS requires only five preprocessor designs; narrowband, nonspread signal (such as conventional voice and data communications) can be demodulated, detected and processed directly by the microsignal processor. In these cases, the preprocessor, basically consists of quadrature sampling and quantizing the IF signals. This processor is applicable to all MFBARS functions in the HF/VHF/UHF band except for SEEK TALK, which requires its own special preprocessor, yet undefined, to strip the PN code from the spread-spectrum signal. The third preprocessor, which is designed to detect pulse signals, can be used for both TACAN and IFF applications. The other remaining two preprocessors are required for GPS and JTIDS.

1.2.4 Microsignal Processor

The baseline microsignal processor is to be a high-speed, centralized microsignal processor (MSP) which consists of a pair of signal processors tightly coupled through a matrix switch network. Each processor has four modules (RAM, MPY, CPU, and I/O). This configuration is considered to be a 2 x 2 matrix signal processor. It has an operating speed of 64 MIPS, which is in excess of the MFBARS requirements of 41 MIPS. The breakdown of MFBARS processing requirements is as follows:

JTIDS	20.7 MIPS
GPS	7.7 MIPS
TACAN	1.2 MIPS
IFF	0.5 MIPS
Narrowband Modem	3.0 MIPS
Overhead	<u>7.8 MIPS</u>
	40.9 MIPS

The MSP has modular design and is highly flexible. It can expand from the 2 x 2 structure up to a 4 x 4 matrix, with processing speed of 128 MIPS. At its fully expanded configuration, it can be used to perform additional signal processing functions such as adaptive antenna control or integrated navigational system calculations. The MSP can also be reduced to the basic 1 x 1 processor for application where reduced MFBARS capability is desirable, such as the elimination of JTIDS. The important features of the MSP are summarized as follows:

- High Availability
 - Redundancy and Reconfiguration
- Higher Order Language (HOL) Compatible
 - Interpreter/Compiler
 - Assembler/Emulator
- High Data Throughput
 - Multiple Computational and Storage Elements
- Low Life Cycle Cost
 - Maintenance vs Production Cost
- Minimum Physical Characteristics
 - Parts Count 160 IC's
 - Volume 150 Cubic Inches
 - Power Dissipation 60 Watts
- Flexibility for Growth/Other Applications
 - Modular by Function
 - Programmable
 - Technology Transparent

1.3 SUMMARY AND CONCLUSIONS

As will be shown by the materials presented in this report, the MFBARS Phase I and Phase II program objectives have been essentially achieved. The more important tasks completed are:

- System Architecture Tradeoff
- Preliminary System and Hardware Design on the Selected Configuration
- Evaluation of Key Component Requirements and Status
- Evaluations of Life-Cycle Cost on Selected Configurations
- Design and Evaluations of Adaptive Antenna
- Sizing Integrated Inertial Navigation Data Processing Requirements

The study program has produced a viable MFBARS baseline system which can accommodate all of the required CNI systems. The baseline employs standard modules/slices to achieve one of objectives of reduced cost for design and maintenance. The target for module standardization was centered on fulfilling each functional requirement with a minimum number of designs covering the entire frequency bandwidth. Recently developed RF LSI and digital LSI circuits provide the key to the development of useful standardized modules. The results of such efforts are summarized in Table 1-2, which shows a varying degree of success ranging from a single design for the microsignal processor to the antenna and PN correlator/IF Processor, which require five different designs. The use of standardized modular concepts also gives a high degree of flexibility to configure the MFBARS terminal in accordance with the requirements of the user. Such flexibility is illustrated in Table 1-3, which shows the complement of standard modules required for different applications, ranging from a complete MFBARS system to a single function. Additionally, the baseline system takes advantage of programmable standard modules to

Table 1-2. MFBARS Standard Module Designs

Functions	Number of Designs	Notes
Antenna	5	
Adaptive Array	2	one for L-Band and the other for UHF
Frequency Dehopping	2	one for L-Band and the other covers 2 to 400 MHz
PN Correlator/IF Processor	5	one for narrow band signal and the four others are for GPS, JTIDS, IFF/TACAN and SEEK TALK
Microsignal Processor	1	one fast processor to cover all functions
Transmitter	2	one for L-Band and the other for 2 to 400 MHz
Total	17	other supporting functions, such as power supplies and matrix switches are not included

employ the following time sharing of functions to reduce equipment complements:

- A single HF/VHF/UHF transmitter for all the functions in the frequency band, i.e., SEEK TALK, SINGARS, HF Voice, VHF/FM, UHF SATCOM etc.
- A single L-Band transmitter for JTIDS, TACAN and IFF
- Five L-Band frequency dehopping converters are time-shared among JTIDS, GPS, TACAN and IFF (instead of the eight channels required when no time sharing is used).
- Four HF/VHF/UHF receiver module (frequency dehopping converter) is time-shared among all the HF/VHF/UHF functions (instead of seven or more which would be required, depending upon the total complement systems to be accommodated).

Time sharing reduces the complement possibly by half that required when not using time sharing.

Table 1-3. MFBARS/INCIA Slices/Components

STANDARD SLICE/APPLICATIONS	MFBARS	JTIDS	GPS	JTIDS/ GPS	JTIDS/IFF /TACAN	GPS/IFF /TACAN	GUARD	VHF RADIO	UHF SATCOM	SEEK TALK	UHF/ SEEK TALK	VHF/ UHF
INCIA TERMINAL												
1. L-BAND RECEIVER RF SWITCH	1	1	1	1	1	1	---	---	---	---	---	---
2. L-BAND FREQUENCY DEHOPPING CONVERTER	5	4	2	4	5	4	---	---	---	---	---	---
3. L-BAND IF SWITCH	1	---	---	1	1	1	---	---	---	---	---	---
4. JTIDS DEMODULATOR	1	1	---	1	1	---	---	---	---	---	---	---
5. GPS DEMODULATOR	1	---	1	1	---	1	---	---	---	---	---	---
6. IFF/TACAN DEMODULATOR	2	---	---	---	2	2	---	---	---	---	---	---
7. REFERENCE FREQUENCY SOURCES	1	1	1	1	1	1	---	---	---	---	---	---
8. VHF/UHF RECEIVER RF SWITCH	1	---	---	---	---	---	1	1	1	1	1	1
9. HF/VHF/UHF RECEIVER MODULE	4	---	---	---	---	---	1	1	2	1	2	2
10. HF/VHF/UHF IF SWITCH	1	---	---	---	---	---	---	---	1	---	1	1
11. SEEK TALK DEMODULATOR	1	---	---	---	---	---	---	---	---	---	1	---
12. IF FREQUENCY SOURCES	1	---	---	---	---	---	1	1	1	1	1	1
13. PREPROCESSOR	1	1	1	1	1	1	1	1	1	1	1	1
14. MATRIX SIGNAL PROCESSOR	4X4	2X2	1X1	4X4	2X2	1X1	1X1	1X1	1X1	1X1	1X1	1X1
L-BAND TRANSMITTER												
15. MODULATOR FOR L-BAND	1	1	---	1	1	1	---	---	---	---	---	---
16. L-BAND XMITTER DRIVER	1	1	---	1	1	1	---	---	---	---	---	---
17. L-BAND POWER AMPLIFIER	1	1	---	1	1	1	---	---	---	---	---	---
18. L-BAND XMITTER ANTENNA INTERFACE	1	1	---	1	1	1	---	---	---	---	---	---
HF/VHF/UHF TRANSMITTER												
19. HF/VHF/UHF MODULATOR/EXCITER	1	---	---	---	---	---	1	1	1	1	1	1
20. HF/VHF/UHF POWER AMPLIFIER	1	---	---	---	---	---	1	1	1	1	1	1
21. HF/VHF/UHF ANTENNA INTERFACE	1	---	---	---	---	---	1	1	1	1	1	1

The results of this study have clearly shown that MFBARS is a viable concept. The technology required to implement the baseline system is currently available, even though some maturing processing is required. Key components can be developed in time to achieve production in the late 1980's. However, the key to viability is the extensive utilization of the recent TRW-developed RF LSI circuits in the baseline design.

Usage of RF LSI and the employment of standardized modules results in life cycle cost and real estate savings which make the MFBARS highly attractive. The comparison of these savings as highlighted in Table 1-4, which include only the radio but not the antenna system. The volume saving is more than 4 to 1, and could be significantly more except for the power amplifiers where the required volume is basically limited by thermal dissipation requirements. The cost saving is in the order of \$200 M, based on a production volume of 1000 units. Although the economic analysis is based on preliminary cost data, the basic 3 to 1 in cost savings is a realistic figure.

The baseline MFBARS system employs advanced technologies to achieve an attractive system design. The risk in realizing this system can be minimized when these advanced technologies can be validated prior to advanced model development. As part of Phase II studies, the critical advanced technology areas have been identified and the priority for their undertaking has been developed for the TRW MFBARS design. The criteria for the priority recommendation is based on the following factors:

- High leverage for cost and size reduction
- Development lead time
- Uniqueness to MFBARS
- Risk minimization prior to advance development model.

Table 1-4. MFBARS vs. Single Function CNI Avionics

	MFBARS	Single Function Avionics
Configuration	3 ATR Cases (One Full, Two Half)	13 ATR Cases, Various Sizes
Volume	1.7 Cu. Ft.	7.0 Cu. Ft.
Weight	100 Lbs.	300 Lbs.
LCC (Phase I)	\$100 Million	\$300 Million

The primary tasks recommended for Phase III are presented in this report and summarized in their order of their priority as follows:

- 1) Design development of an RF LSI HF/VHF/UHF receiver module.
- 2) Validation and demonstration of the matrix signal processor architecture.
- 3) Design and development of a wideband antenna system.
- 4) Design and development of an RF LSI quadrature linear amplitude modulator.

2. SYSTEM DESIGN

The basic requirement for the MFBARS system is to provide the capability to accommodate the avionic functions of communications, navigation, and identification (CNI) in the frequency range of 2 to 2000 MHz. For the most part, these functions include systems such as JTIDS, GPS, SEEK TALK, and SINGARS, which are still in the development stage. However, some currently operating systems (TACAN, IFF, HF and VHF radios) are also included.

It would be impractical to involve all of these functions in an aircraft using today's equipment technology for two reasons: (1) real estate constraints, particularly on tactical fighter aircraft, and (2) life cycle costs. The cost of maintenance of the avionic equipment would be extremely high. The prime objective of the MFBARS system design is to achieve significant savings in both of these areas.

TRW believes the key to achieving these fundamental objectives is to use RF as well as digital LSI circuits extensively. The size and product cost reduction is a well-known advantage of using the LSI circuit. It also has another equally important impact of allowing more extensive use of standardized modules. In fact, because of its size and cost reduction, the standard module can be more encompassing and flexible without being prohibitively large. Thus, the number of required standard modules can be reduced. The maintenance cost, as well as the total acquisition cost and, thus, the total life cycle cost, can be further reduced. In fact, the extensive use of RF and digital LSI circuits is the key to the viability of the MFBARS.

The other important features in designing a system to achieve the MFBARS objective include time sharing throughout to reduce equipment and modular construction to give flexibility for terminal configuration.

Functional commonality across the CNI systems in MFBARS is illustrated in the block diagram shown in Figure 2-1. The common thread through all

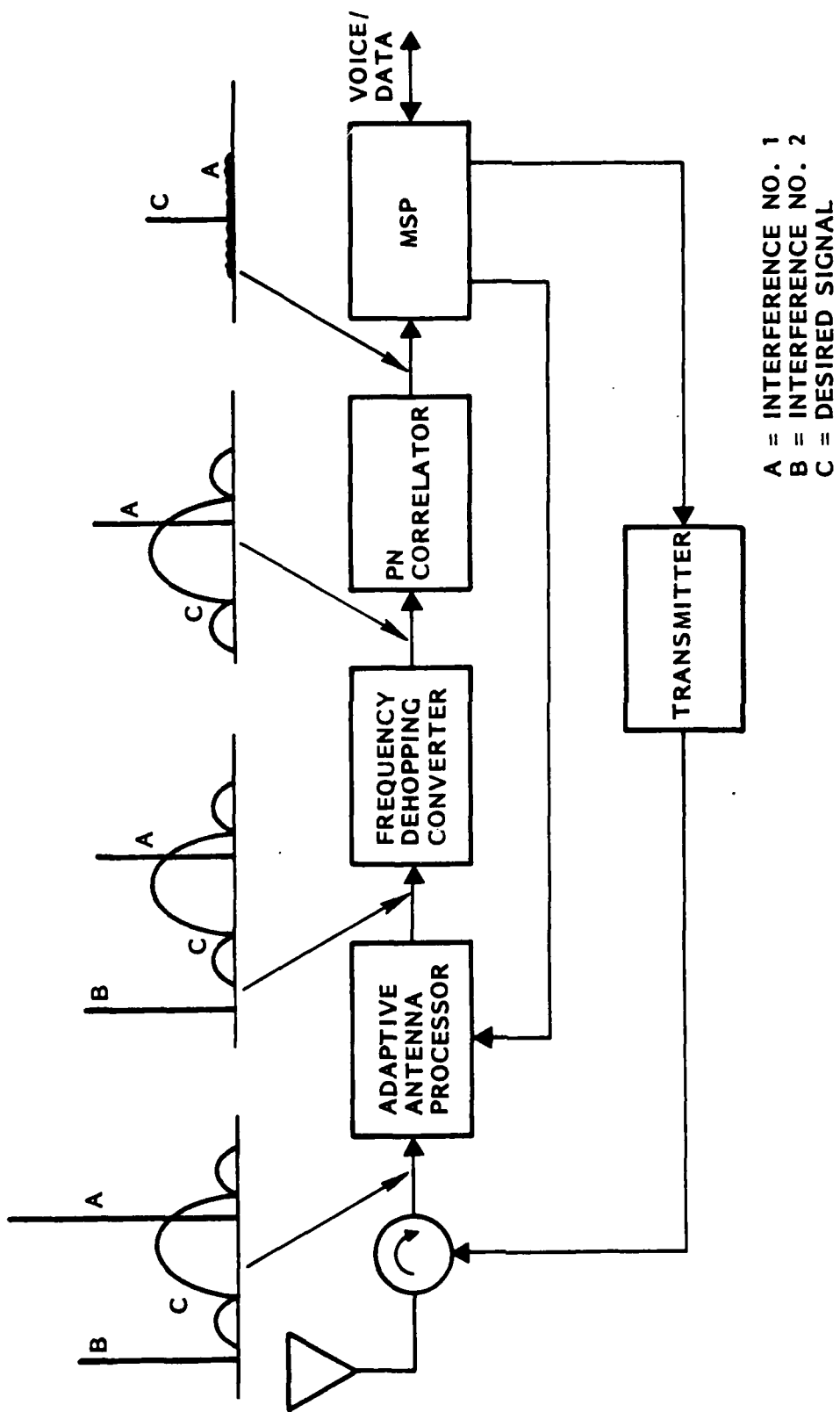


Figure 2-1. Generalized Multifunction Multiband Radio System (MFBARS)

of these systems is apparent in this block diagram, which shows the totality of CNI functions and can be broken down into six basic processing subsystems.

Ideally, any MFBARS function can be accommodated within these six subsystems, provided that each of these subsystems has the capability and flexibility to cover frequency range and waveform requirements.

- 1) Antenna Subsystem. For receiving and transmitting signals.
- 2) Adaptive Antenna Processor. Which provides antijam protection through spatial discrimination.
- 3) Frequency Hopping Converter. Which performs the function of frequency dehopping to compress the desire signal into a narrower bandwidth and thus reduce the jamming signal power.
- 4) PN Correlator. Which performs the PN despreading to further narrow the bandwidth and reduce the jamming signal power.
- 5) Microsignal Processor (MSP). A highly flexible processor and which performs all signal processing functions, such as demodulation, synchronization, decoding, waveform generation, as well as control the configurations on the radio system.
- 6) Transmitter. Which accepts the data from the MSP, performs modulations, frequency conversion, and amplifications to appropriate power levels.

An ideal MFBARS system will consist of as many similar systems as required to serve the maximum number of functions to be operated simultaneously. Such an ideal system is, of course, not achievable if the schedule of having an advanced development model (ADM) by 1985 is to be met.

The baseline system detailed in Section 2.2 features a varying degree of success, as expected, in achieving the six standard modules. The most notable area of success is the microsignal processor, which can be configured into one standard module. The MSP is capable of being programmed to handle the necessary processing for all required CNI functions. The standardization of the frequency dehopping module is

slightly less successful. However, it does represent a significant advancement in the state-of-the-art. Phase II results indicate that it is possible to have only two standard frequency dehopping modules to cover the entire MFBARS frequency spectrum, one for the L-Band functions and the other for functions below UHF. The transmitters also require two designs which cover the same frequency band as the frequency dehopping modules. The results also indicate that the antenna and adaptive antenna processor can be similarly standardized, but are less conclusive. The most notable failure is in obtaining a standard design for the PN correlator. The baseline design requires individually tailored PN correlators for each of the functions. However, this negative result is not due to any theoretical or obvious practical limitation. It is rather a problem of the combination of diversity and uncertainty in requirements of these systems; i.e., JTIDS, GPS, and SEEK TALK, and the limited resources devoted to this module.

The alternate system was developed during the Phase I studies and was also based on the use of digital and RF LSI, as well as standard modular concepts. The two systems differ essentially in the degree of refinement. The alternate approach described in Section 2.3 calls for a separate MSP and receiver for each of the functional channels. The alternate approach also has less equipment time sharing.

2.1 SYSTEM DESIGN REQUIREMENTS

The requirements and baseline configuration contained herein are derived from the following government-furnished information.

- 1) Requirements analysis for a multifunction, multiband airborne radio system (MFBARS), March 1978 by ARINC Research Corp.
- 2) Clarification of MFBARS SOW with respect to technical and economic consideration of the definition phase, 15 May 1978 from AFAL/AAA.
- 3) Final Report, GPS/JTIDS/INS Integration Study, Volume 1, April 1978, by Draper Laboratories.
- 4) Correspondence of 26 July 1978 from AFAL/AAA.
- 5) Verbal guidance received at program review meetings with AFAL/AAA on 10 July and 25, 26 July 1978.

The tactical aircraft in the current inventory, as well as those likely to be produced in the foreseeable future are all designed to be mission oriented and, as such, carry a variety of CNI equipment suits. For example, those air support platforms such as the A-10 and F-16A/B carry VHF radios to communicate with ground forces. Long-range aircraft such as the EF-111A carry HF radios for long-haul communications. A chart from the ARINC report shown in Table 2-1 indicates the large variety of possible CNI configurations which could be considered.

For the purpose of the current study, where the intent is to develop and analyze MFBARS architectures, a single composite baseline has been developed. Although the composite baseline dictates the requirements for the MFBARS effort, the personalities of the various host platforms are considerations of functional modularity and growth to accommodate future functions. The following government-furnished guidance is used in developing the MFBARS baseline:

- a) The application of MFBARS is considered to be a core CNI design for new aircraft.
- b) The interface with the core information system onboard will be through a DAIS-compatible remote terminal or bus control interface unit.
- c) Applicable technology will be that which is presently forecast to be available for design into 1985 advanced development model equipment.
- d) Capable of interfacing and utilizing an Inertial Navigation System (INS) to improve MFBARS system performance, which includes antijam performance.

The MFBARS baseline capability encompasses the functions provided by the equipment shown in Table 2-2. The following functional capability derived from the equipment listed is the MFBARS baseline.

- 1) Position (3D) and velocity determination from whatever beacon environment is available (Precision: GPS X set)
 - a) Absolute
 - b) Relative
 - c) Downgraded to reflect availability of external system (e.g., R Nav).

Table 2-1. CNI Functions and Types of Equipment

	Functions	F-15A	F-16A/B	EF-111A	A-10A/B	F-4G	FAC-X (A-10)	ATF	FOI (F-15)	RF-X
Communication	UIF	ARC-164 (2)	ARC-164	ARC-164	ARC-164	ARC-164	X	X	ARC-164	X
	VIIF-AM	-	ARC-115	-	807A	-	X	-	-	-
	VIIF-FM	-	-	-	ARC-131	-	X	-	-	-
	HF	-	-*	ARC-112	ARC-154*	-	X	X	-	X
	Crypto	KY-28	KY-28	KY-28	KY-28/58	KY-28	X	X	KY-28	X
	JTIDS	X	X	X	X	X	X	X	X	X
	SEEK T/LK	X	X	X	X	X	X	X	X	X
	TIDS	ASN-109	SKN-2400	AJQ-20	X	ASN-63	X	X	ASN-109	X
Navigation	TACAN	ARN-118	ARN-118	ARN-118	ARN-118	ARN-118	ARN-118	X	ARN-118	X
	ILS	ARN-112	ARN-108	ARN-58	ARN-108	-	ARN-108	X	ARN-112	-
	UHF/ADF	OA-8639/ARD	-	ARN-50	OA8697/ARD	-	OA-8697/ARD	X	OA-8639/ARD	X
	IID	AVQ-20	X	-	X	-	X	X	AVQ-20	X
	Navigation Radar	-	X	-	-	-	-	-	-	-
	Radar Altimeter	-	-	APN-167	-	APN-155	-	-	-	X
	TFR	-	-	APQ-110	-	-	-	X	-	X
	Radar Beacon	-	-	-	UPN-25	UPN-25	UPN-25	X	-	-
	OMEGA	-	-	-	-	-	-	X	-	-
	GPS	X	X	X	X	X	X	X	X	X
	MLS	X	X	X	X	X	X	X	X	X
	IFF Transponder	APX-101	APX-101	APX-64	APX-101	ASQ-19	APX-101	X	APX-101	X
	IFF Interrogator	APX-76	-	-	-	APX-76	-	X	APX-76	X
Identification	IFF Crypto	KIT-1A	KIT-1A	KIT-1A	KIT-1A	KIT-1A	KIT-1A	X	KIT-1A	X
	Automatic Altitude Reporting	-	-	-	AAV-19	-	AAV-19	X	-	X

*Weight, space, volume allocations X: Equipment set planned but designation unknown
 -: No equipment planned

Table 2-2. MFBARS Baseline Capability

FUNCTION	BAND (MHz)	MODULATION	Tx POWER (WATTS)	RECEIVER SENSITIVITY	EQUIPMENT	ADDRESSED?
HF VOICE	2-30	SSB	400 WPEP	1 μ V 10dB SNR	ARC-112	YES
VHF VOICE	30-88	FM	1 OR 10	0.5 μ V 10dB SNR	ARC-131	YES
VHF VOICE	108-156	AM	10	3 μ V 10dB SNR	ARC-115	YES
UHF VOICE	225-400	AM	10	4 μ V 10dB SNR	ARC-164	YES
ILS/VOR	-	PULSE	-	-	ARN-108	NO
LOCALIZER	108-112	-	-	-	-	-
GLIDE SLOPE	329-335	-	-	-	-	-
MARKER BEACON	75	-	-	750 μ V	-	-
TACAN	962-1213	PULSE	0.5 TO 2K	-89 TO -92 dBm	ARN-118	YES
IFF TRANSPONDER	1090 Tx 1030 Rx	PULSE	500	-65 TO -77 dBm	APX-101	YES
IFF INTERROGATOR	1030 Tx 1090 Rx	PULSE	1 TO 2.5K	-80 dBm	APX-76	NO
FUTURE IFF	TBD	-	-	-	-	NO
GPS NAVIGATION	1228, 1575	DSPN	-	-36 dBm	-	YES
JTIDS	960-1215	PNFH	200 TO 800	-	-	YES
SEEK TALK	225-400	DSPN	1	-	-	YES
UHF SATCOM	225-400	FH	100	-	-	YES
SINGGARS	30-88	-	-	-	-	NO

- 2) Automatic responses to external interrogations (962-1215 MHz)
 - a) Identification in MK XII modes 1 through 4 (1090 MHz T, 1030 MHz R)
 - b) A/A TACAN interrogation
 - c) RTT requests
 - d) Technical acknowledgment to all messages requiring pilot response.
- 3) Receive selected signals in accordance with appropriate format, modulation and protocol as follows:
 - a) JTIDS (IJMS) in TDMA format
 - b) JTIDS signals in DTDMA format up to maximum constraint of our channels for (i)
 - c) TACAN ground beacon responses to a/c interrogation
 - d) All MK XII interrogations
 - e) AJ voice and command transmissions
- 4) Performance requirements shall meet the equivalent rates, thresholds, error rates, etc., values of the parent single function equipment.
 - a) The performance shall be required to be functionally the same as that achieved by having independent JTIDS, TACAN, MK XII and SEEK TALK hardware simultaneously in the switch-on/active mode.
- 5) Receive selected signals in conventional modes (signal bandwidth constraint to 25 kHz) in the 2 to 400 MHz portion of the spectrum, as follows:
 - a) (i) On guard channels, one in each of 2 to 30, 30 to 88, 108 to 156, and 255 to 400 MHz band allocations.
 - (ii) On designated operating channels: two in the 225 to 400 MHz bandwidth, one in each of the other bandwidths.

- b) Performance requirements for each channel, individually, are those of the individual terminals constituting the baseline. Any degradations arising from integration should not significantly degrade the aircraft mission performance.
 - c) Simultaneous voice outputs from at least three selectable channels is required, with at least one guard channel included. Selection may be manual or may be automatically selected from parameter (i.e., signal presence detection) indicating channel activity.
- 6) Transmission of required signals in the JTIDS, TACAN, IFF, and AJ voice formats as required, and only one at a time.
 - 7) Transmission on one channel corresponding to the receive capability in item 4 above.
 - 8) The ability to select, and/or preprogram channel and information transfer function as required in the systems identified in items 1 through 4 above.
 - 9) The ability to automatically reprogram and/or provide actions for pilot reprogramming of module configurations to meet the condition of the mission segment.
 - 10) Flexibility to add preprograms and to select algorithms to provide functions of DABS and derivatives, improved MK XII, SINGARS, PLRS, PLSS one link, radar altimeter, direction finding, and relay.

2.2 BASELINE SYSTEM APPROACH

This subsection describes the TRW-proposed baseline design for the MFBARS system. This design is based on utilization of standard modules to reduce life-cycle cost and provide maximum flexibility. It also depends heavily on the utilization of recent TRW-developed RF LSI as well as the more well-developed digital LSI to reduce volume and ownership cost. The block diagram of the basic design is shown in Figure 2-2. The baseline system is basically implemented with an antenna system, an L-Band subsystem, HF/VHF/UHF subsystem, and a digital signal processing system. The baseline MFBARS consists of a set of antennas covering the entire frequency range of 2.0 to 1575 MHz. The antenna system can be either adaptive or nonadaptive.

The baseline system is targeted to have as few standard modules as possible, to utilize technologies which can be reasonably mature, and to achieve the MFBARS objective of having an operational system in the

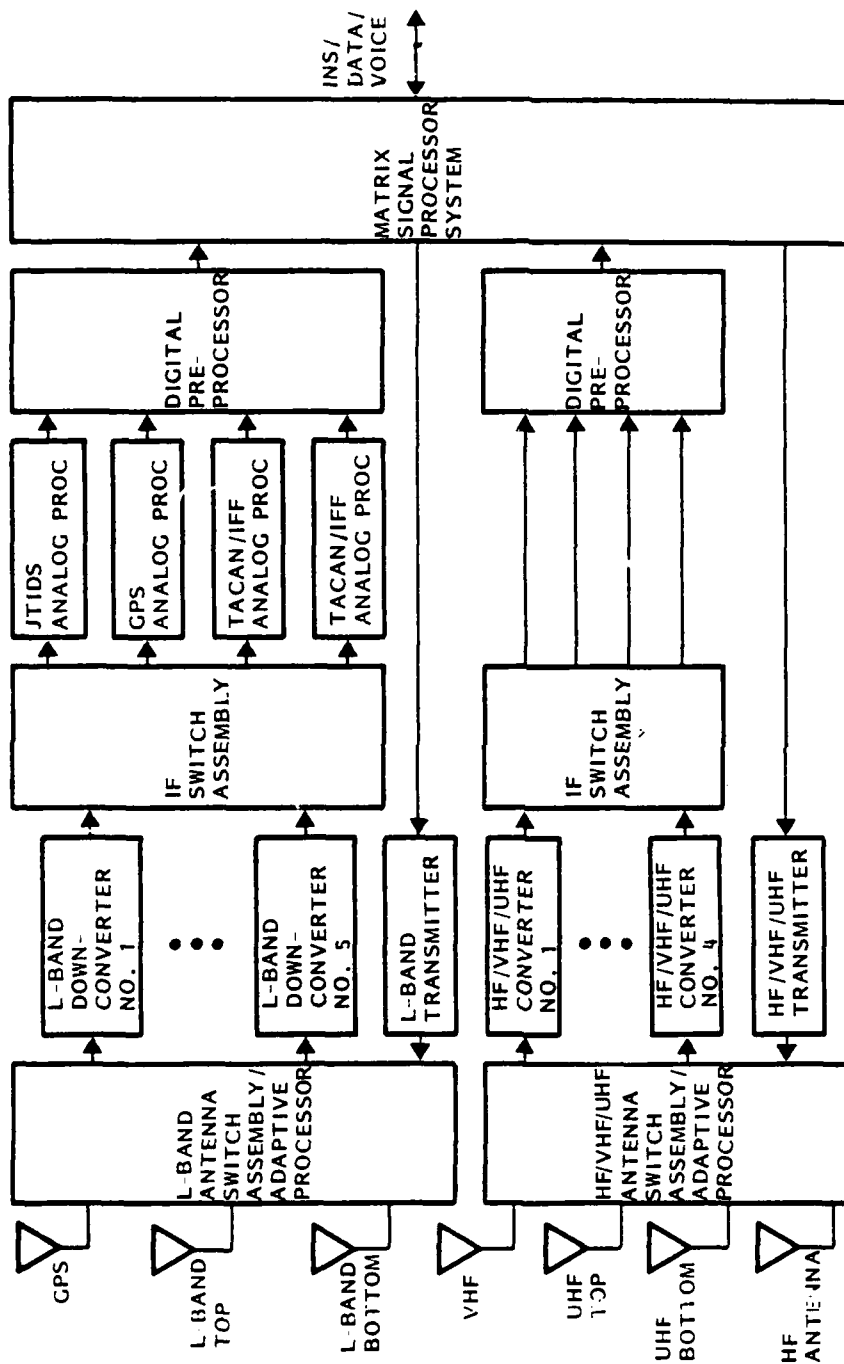


Figure 2-2. MFBARS Block Diagram, TRW Design

late 1980's. The TRW baseline design separated the RF/IF subsystem into two standard designs, one for L-Band (960 to 1575.42 MHz) functions (JTIDS, GPS, TACAN, IFF), and another for the HF/VHF/UHF band (2 to 400 MHz) functions (SEEK TALK, SINCGARS, UHF SATCOM and HF radio).

When the adaptive antenna system is used, additional AJ protection can be obtained. A detail discussion on the results for the preliminary design study for the adaptive antenna is given in Section 4. Using the nonadaptive antenna system, in general, will be the same as individual antennas covering separate frequency bands.

Antennas are connected to the transmitters and receivers. For transmissions, the power amplifiers are connected through circulators, and for receiving the antennas are connected through an L-Band antenna switch bank to one of the five identical L-Band downconverters or the HF/VHF/UHF antenna switch banks to one of the four identical HF/VHF/UHF converters. Each of these converters has fast-settling time frequency synthesizers to perform frequency dehoppping and to convert the output to a fixed IF frequency of 184 MHz for the L-Band functions and 70 MHz for the other functions. The converter outputs are then connected into two separate IF switch assemblies, one for L-Band functions and the other for the HF/VHF/UHF functions. These IF switch assemblies connect any of the converter outputs into any of the dedicated analog and digital processors. Analog preprocessors are required in cases of wideband functions such as those in the L-Band. The analog processors perform the function of PN despread, filtering as well as analog to digital conversion. In some cases, dedicated digital processors are used to further reduce the data rate before inputting the received signal into the matrix signal processor which performs a multitude of signal processing, such as error correction decoding, filtering, demodulation, bit synchronization, as well as accepting external command inputs via DAIS to reconfigure and control the operation of the MFBARS. The results of the detail design of this MSP are presented in Section 6. The MSP also formulates and structures the signal waveform as inputs to both transmitters for transmissions. The detail design of some of the more important subsystems is detailed in this section, except for the adaptive antenna design and the matrix

signal processor which are discussed in much greater detail in Sections 4 and 6, respectively.

2.2.1 L-Band Front-End

The L-Band antenna is used to serve GPS, JTIDS, TACAN, and IFF. Using nonadaptive antenna systems, an L-Band front-end design is shown in Figure 2-3. The L-Band front-end is basically separated into two subsystems. One subsystem is for GPS, which uses the same antenna in two separate filters to cover the L_1 and L_2 frequencies of 1575.42 MHz and 1227.6 MHz. The filters narrow the total input bandwidth into the region centered around the carrier frequencies and recombines L_1 and L_2 before applying them to the L-Band low noise amplifier. A burnout protection device is used to protect the LNA. JTIDS, TACAN, and IFF systems require different polarization and coverage and use separate antenna systems. These systems require two antennas, one on top of the aircraft and the other on the bottom. The antenna selection is controlled by the matrix signal processor based upon the command received through the DAIS. As in the case of GPS, the LNA also proceeds by a burnout protector. However, unlike the GPS front-end, a bandpass filter centered at 1030 MHz is also included for IFF reception. This filter is used to assure the continuous reception of IFF, and assures that the internal transmission of JTIDS and TACAN will not interfere. For transmission, three sets of filters are used to shape the transmitted signal spectrum of the various functions: (1) a band reject filter at 1030 and 1090 MHz is used for TACAN and JTIDS, (2) a bandpass filter at 1090 MHz is employed for IFF transmissions, and, finally, (3) a bandpass filter at 969 MHz for narrowband JTIDS.

2.2.2 L-Band Downconverters

The baseline design utilizes five identical L-Band downconverters to perform frequency dehop and/or simply frequency downconversion with a fixed frequency source to an IF. These downconverters are designed to be usable for all L-Band functions by simply selecting the proper local oscillator (LO) inputs. These complex L-Band converters are made possible through the extensive use of RF LSI. As shown in Figure 2-4, the L-Band downconverters basically consist of a single RF LSI chip (RF AMP/DC chip, subsection 5.2),

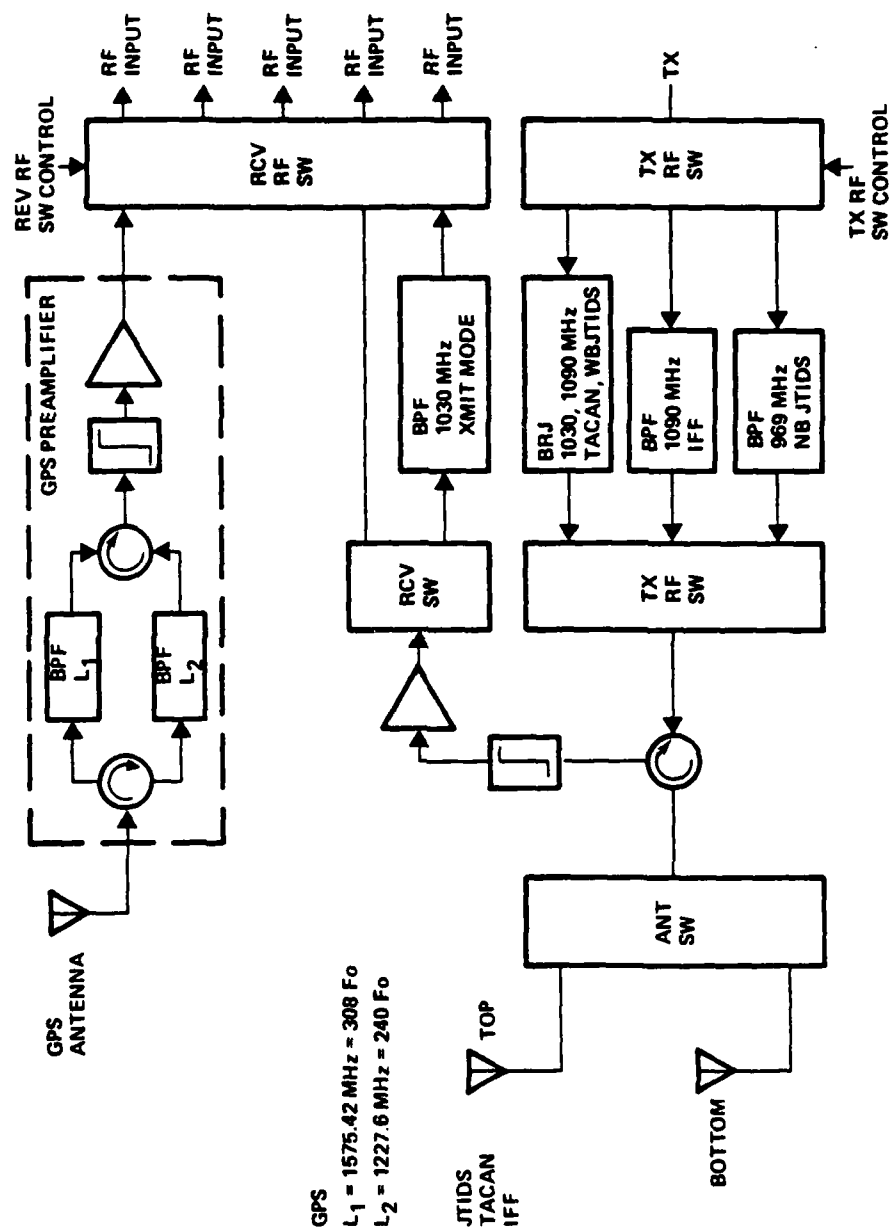


Figure 2-3. L-Band Front End

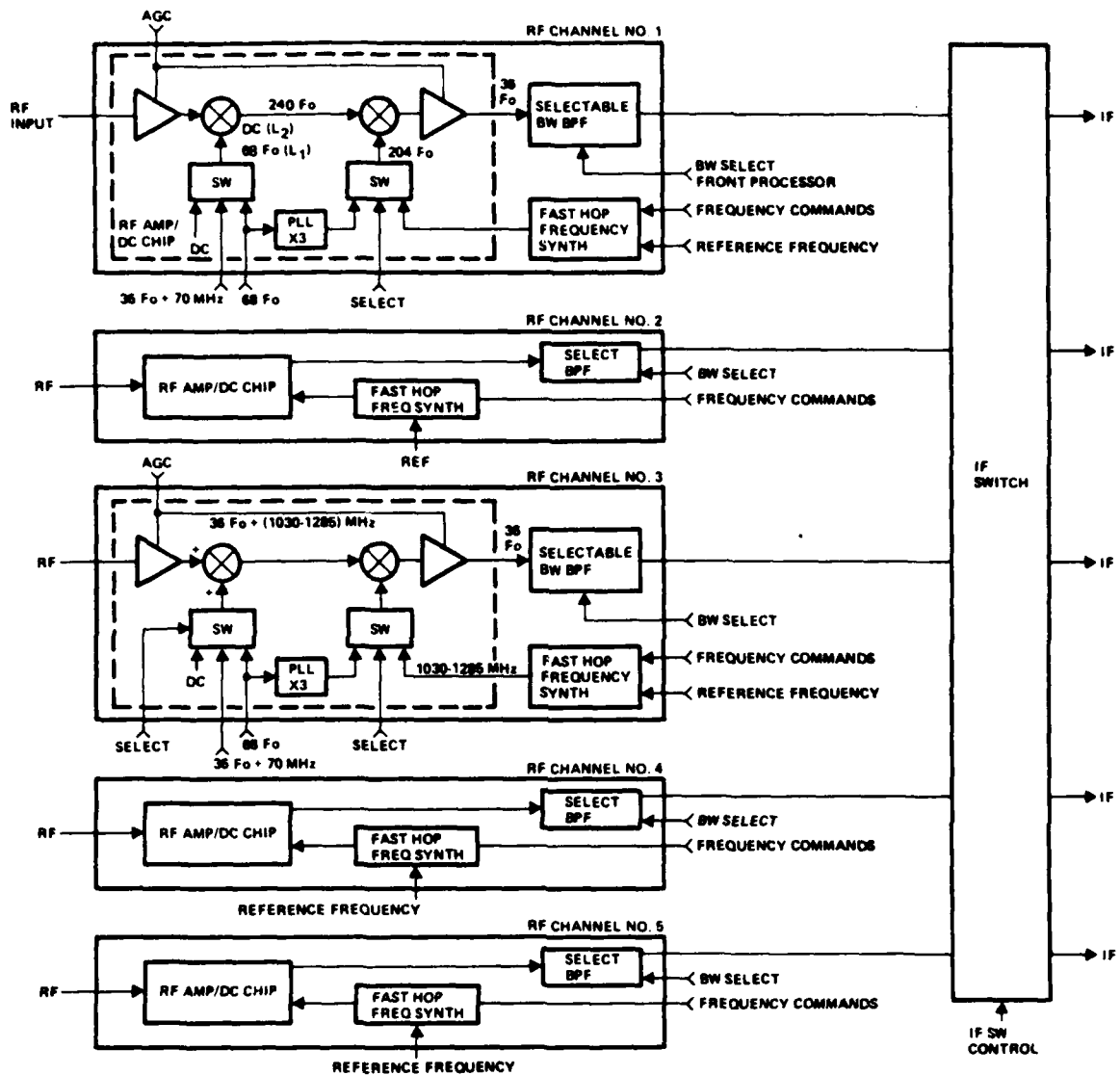


Figure 2-4. L-Band Downconverters

which performs the frequency mixing; a fast hop frequency synthesizer (subsection 5.3), which is also envisioned to be two RF LSI chips; and a selectable bandwidth bandpass filter (subsection 5.4). The total component counts and the physical volume for a converter is very small and it makes a very attractive standard unit for all L-Band functions.

For GPS operations, the downconverter does not need the frequency synthesizer, and the RF channel number 1 in Figure 2-4 shows the resulting frequency conversion. For receiving GPS L_2 frequency, the local oscillator of the first mixer is dc and enables the first mixer to operate as a low-gain linear amplifier. The output frequency of the first mixer remains $240 f_0$ (1227.6 MHz). The LO for the second mixer is selected to be $204 f_0$ and to produce an IF frequency of $36 f_0$ (184 MHz). For receiving the GPS L_1 frequency, the first LO has to be $68 f_0$ instead of dc in order to produce the same IF frequency.

For the JTIDS operation (RF Channel Number 3, Figure 2-4), the frequency synthesizer is used to account for the frequency hopping nature of the JTIDS signal. The first LO frequency is selected to be $36 f_0$ plus 70 MHz, and the second LO is derived from the frequency synthesizer whose possible output frequencies are 70 MHz higher than the JTIDS transmitted frequencies. When the frequency synthesizer is hopping to the correct frequencies and in synchronism with the received signal, the IF frequency will be constant at $36 f_0$. For TACAN and IFF, the L-Band downconverter LO frequencies are similarly connected as in the case of the JTIDS, except that the frequency synthesizer will be stationary at the select frequencies.

The number of L-Band downconverters needed in the MFBARS depends on the number of simultaneous functions required and the acquisition requirements for the JTIDS. Five L-Band converters are selected in the baseline system to allow for a dedicated IFF channel; the remaining four channels are to be used for either: (1) JTIDS acquisition or (2) JTIDS tracking, (3) GPS receiving, and (4) TACAN receiving.

2.2.3 Analog Processors

To be consistent with the standard module concept, it would be desirable to have a standard analog processor to perform PN despreading and other signal processing as in the case of the L-Band downconverter performing the frequency de hopping and frequency conversion. Study efforts up to now have produced minimal success because of the diversity of requirements. The baseline design utilizes dedicated analog processors for GPS and JTIDS, and a common analog processor for IFF and TACAN. Figure 2-5 shows the GPS analog processor which performs the PN despreading. The design is conventional and all of the active components are intended to be implemented as a single RF/LSI chips (IF correlator/Demod Chip, Subsection 5.2). This design has four correlation channels. For code acquisitions, the four channels are used to perform four code-phase tests at a time. For code tracking, these channels are used to generate the punctual, early, and late correlations. For JTIDS, the PN despreading processor utilizes parallel (passive) correlations. For acquisitions, four sets of 32-bit parallel correlations are used. Each is associated with one of four L-Band downconverters which are tuned to cover four of the eight possible frequencies in the JTIDS preamble. Each of the four correlator outputs is then properly delayed in accordance with the expected frequency patterns. After code acquisition, three of the four sets of the correlators are used for tracking and CCSK code detection as shown in Figure 2-6. In the case of demodulation, the parallel correlators are operated on the same IF input, but the PN codes are time phase different by one chip to formulate the early, punctual, and late channels. After PN wipe-off, each of the three resulting signals is then quantized with A/D converters and loaded into the memory correlator for the entire 32 chips of CCSK coded signal. Maximum likelihood technique is used to perform the decoding of the CCSK signal. The reference signal set is obtained by also A/D converting a CCSK coded and MSK modulated signal. Consequently, 32 possible correlation values are obtained through 32 cyclic shifts. For a single correlator to perform this function, it would be required to operate at a speed 32 times that of the chip rate, which is impractical at the present time. The baseline system uses two set correlators for each channel. When one is loading the input signal, the other correlator will perform the 32 correlations on the previous pulse, thus requiring the correlator to operate only at the chip rate.

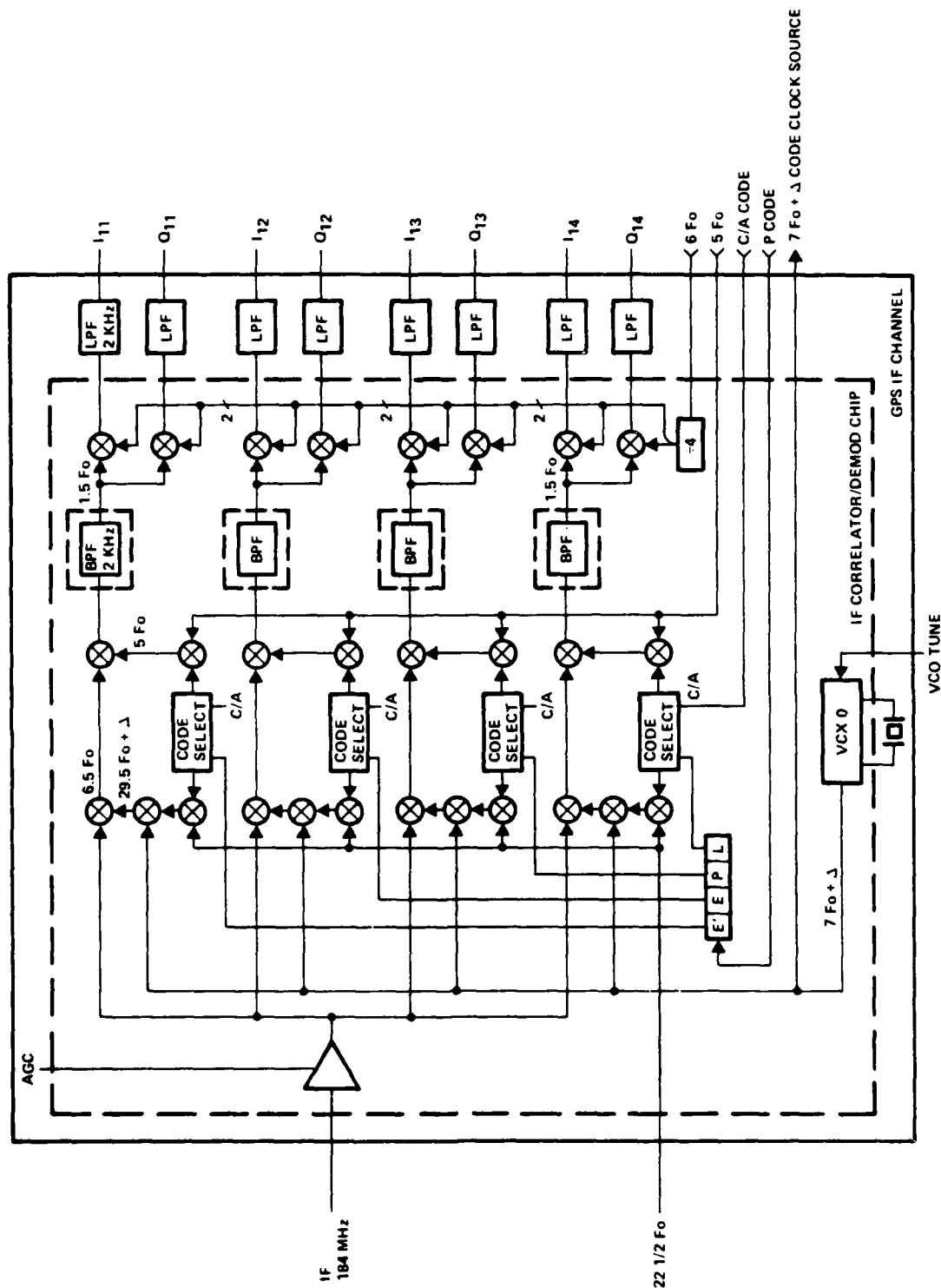


Figure 2-5. GPS IF Channel

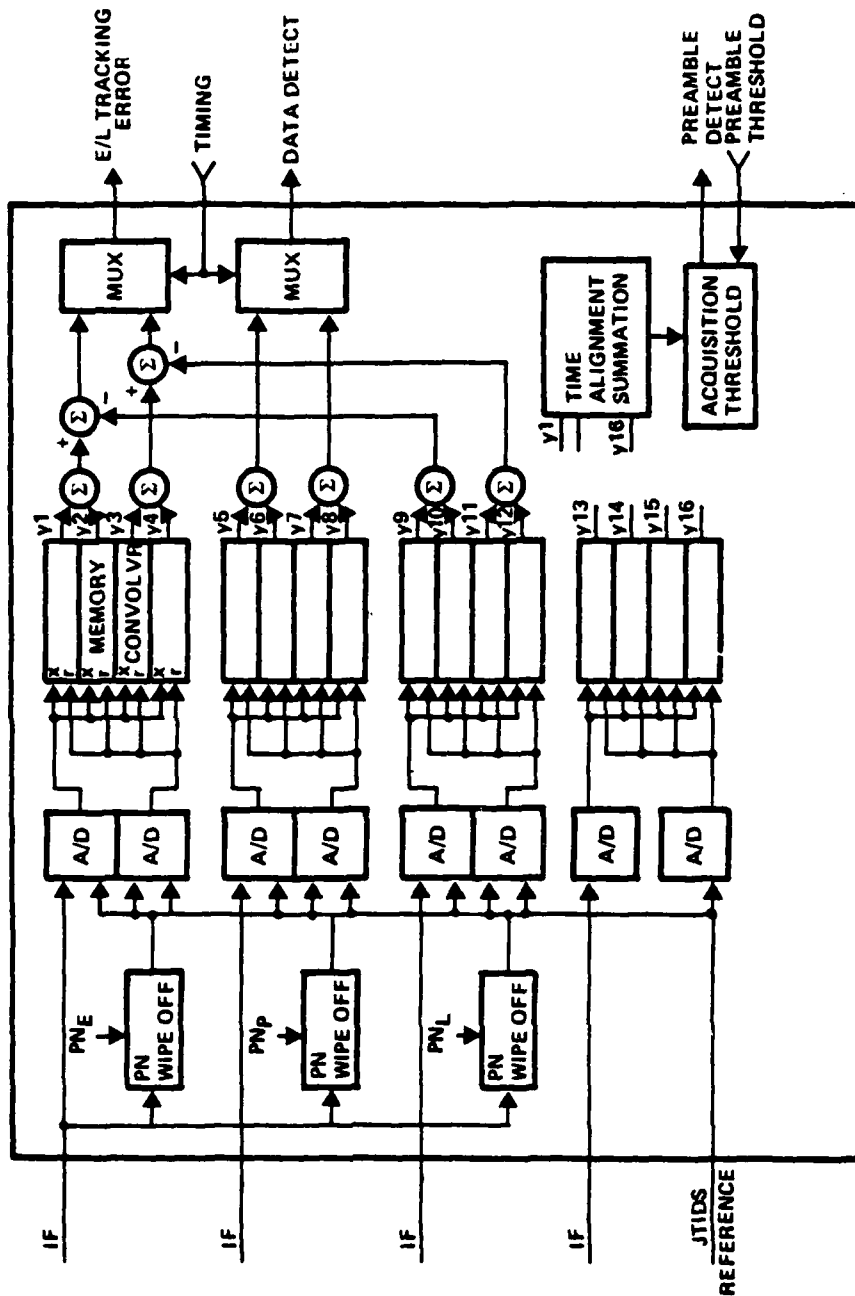


Figure 2-6. JTIDS Demodulator

2.2.4 TACAN and IFF Detector

The analog signal processing for TACAN and IFF is much simpler because both are not spread-spectrum signals. One design can be used for both functions since they are both related to the detection of three pulse parameters; i.e., time of arrival, pulse width, and pulse amplitude. The block diagram of the baseline design is shown in Figure 2-7, which is conventional in design and is self-explanatory.

2.2.5 L-Band Transmitter

In maintaining the standard module design concept, the baseline system employs a single transmitter to cover all of the L-Band functions of JTIDS, TACAN and IFF. It further uses a TRW concept developed under the Standard Avionic Module (SAM) development contract for generating transmitting waveforms. In this TRW concept, the signal waveform is decomposed into its two quadrature components. The amplitudes of the components are linearly modulated by an appropriate waveform to achieve any desired modulated signal such as AM, PM, FM, PSK and MSK. The waveform generation for the L-Band functions, JTIDS, TACAN, and IFF is controlled and formulated by the MSP. The output of the MSP is then further processed and converted to analog signal as modulation input to the Quadrature Linear Amplitude Modulator, which is expected to be a single RF LSI chip (Subsection 5.2).

The carrier of the modulator is 70 MHz, which is selected as the standard carrier frequency for both the L-Band modulator and the HF/VHF/UHF modulator. In order to use the same frequency synthesizer design as that for the receiver, the output of the modulator is further upconverted to $36 f_0 + 70 \text{ MHz}$ as shown in Figure 2-8. The final power amplifier is expected to be an electron bombardment semiconductor (EBS). A detailed discussion of the power amplifier is given in subsection 5.1.

In the case of JTIDS, the L-Band modulator is also used to generate the reference signal for the correlator to perform the maximum likelihood decoding of the CCSK signal. The reference signal is generated in a manner similar to the transmitting waveforms except that in each pulse time all 32 cyclic code states have to be generated and the carrier frequency has to be $36 f_0$ as shown in Figure 2-8. The carrier frequency conversion is achieved by means of a single mixer which has an LO at 70 MHz.

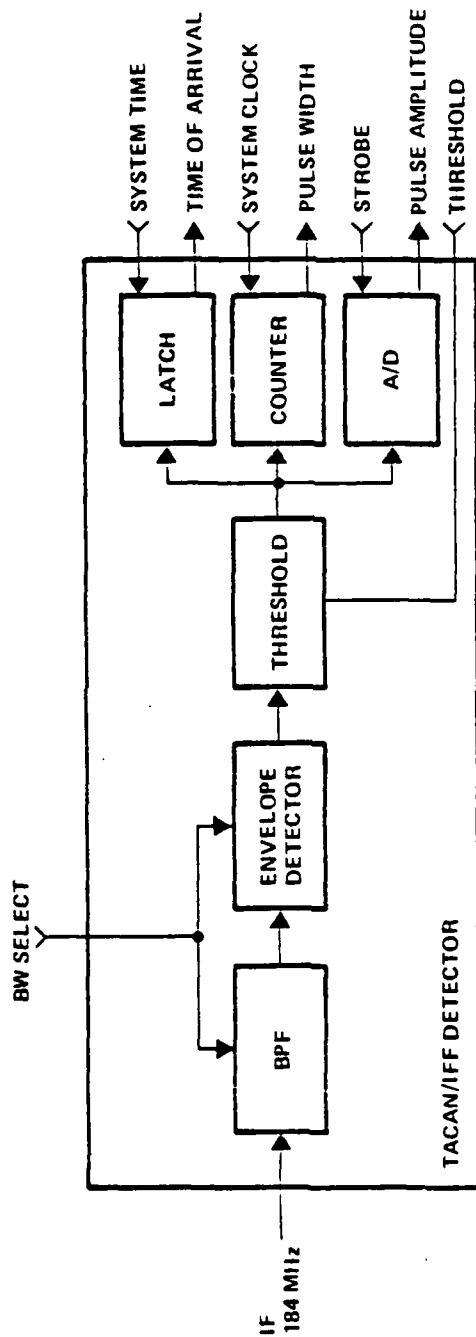


Figure 2-7. TACAN and IFF Detectors

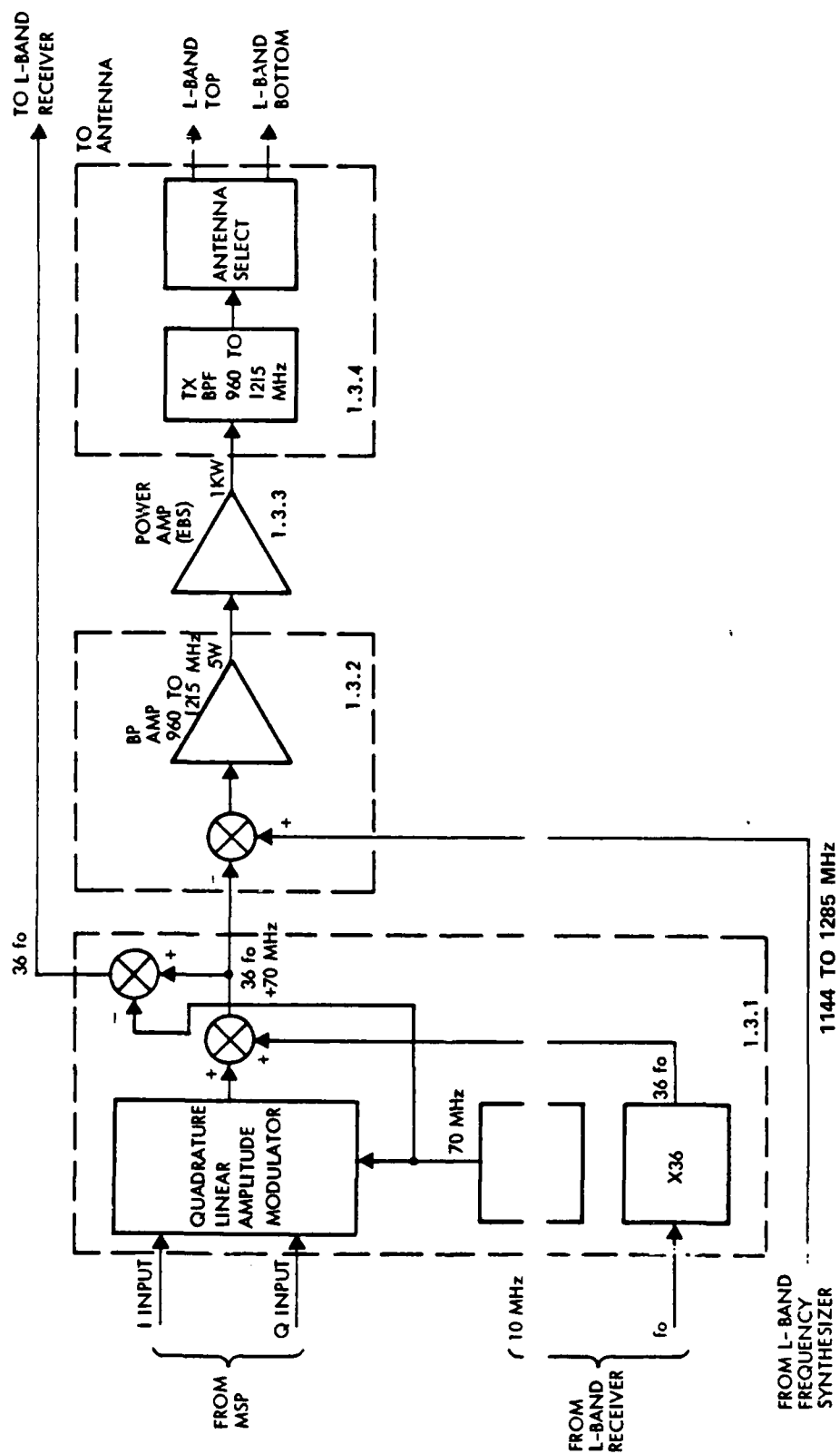


Figure 2-8. L-Band Transmitter

2.2.6 HF/VHF/UHF RF Front-End

The conventional antenna complement needed to cover the HF/VHF/UHF band is shown in Figure 2-9. Basically, one antenna each to cover the HF (2 to 30 MHz) and VHF (30 to 156 MHz) bands and two antennas (one on top and the other on the bottom) to cover the UHF band (225 to 400 MHz). The basic design is conventional; transmit/receiver switches, preselector, and burnout protection devices are used. For receiving, all four antennas are connected to the antenna switch assembly, which allows each antenna output to be connected to one or more (up to all four) of the standard RF LSI HF/VHF/UHF receiver modules to receive the programmed functions.

2.2.7 RF LSI HF/VHF/UHF Receiver Modules

This receiver module is designed to accommodate the entire HF/VHF/UHF band (2 to 400 MHz). It converts, through one or two stages, the received signal to an IF of 70 MHz. Frequency dehoppping is also performed in this module. It is essentially the heart of the HF/VHF/UHF portion of the MFBARS receiver terminal.

As shown in Figure 2-10, the receiver modules are designed around the RF LSI converter/amplifier chip (detailed discussion given in subsections 5.2 and 9.1). The LSI chip has three stages of mixers and two stages of AGC amplifiers to provide frequency conversions and signal amplification. The unit also determines the noise figure of the receiver. The other important components in the receiver modules are: (1) the standard UHF frequency synthesizer which is also expected to be implemented in two RF LSI chips (subsection 5.3), (2) a divide-by-5 circuit, (3) 225 MHz high-pass frequency filter, and (4) a 70 MHz IF bandpass filter. This module is indeed simpler. However, its usefulness is extremely broad and is illustrated in the remainder of this section by detailing how the receiver will operate in each of the three frequency bands, HF, VHF, and UHF.

For the HF frequency band, 2 to 30 MHz, the first mixer stage is used as an amplifier only. The first LO is selected at a dc level, and no IF filtering is used. The second mixer stage will upconvert the HF input into 70 MHz by means of applying a second LO signal whose frequency ranged from 72 to 100 MHz. This LO signal is derived by frequency divide-by-5, the output of the standard UHF frequency synthesizer which covers more than

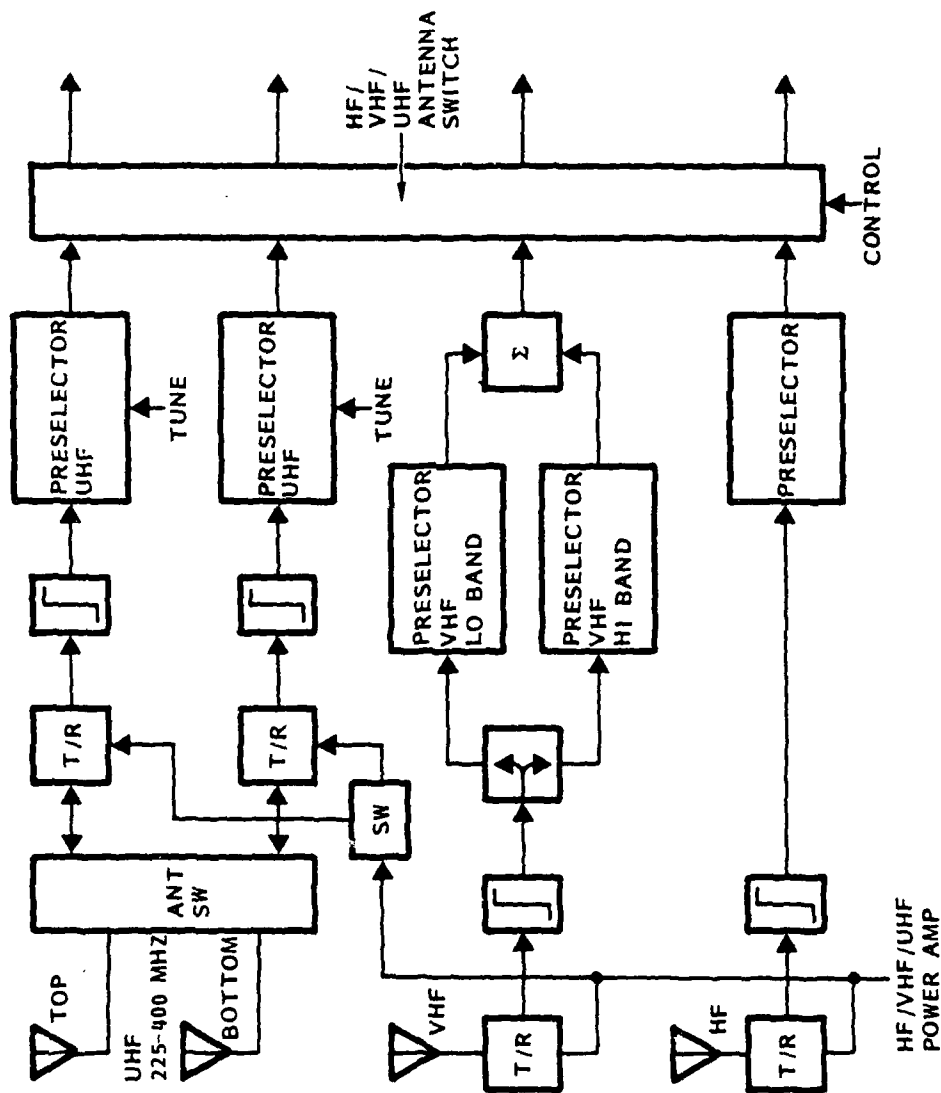


Figure 2-9. HF/VHF/UHF RF Front End

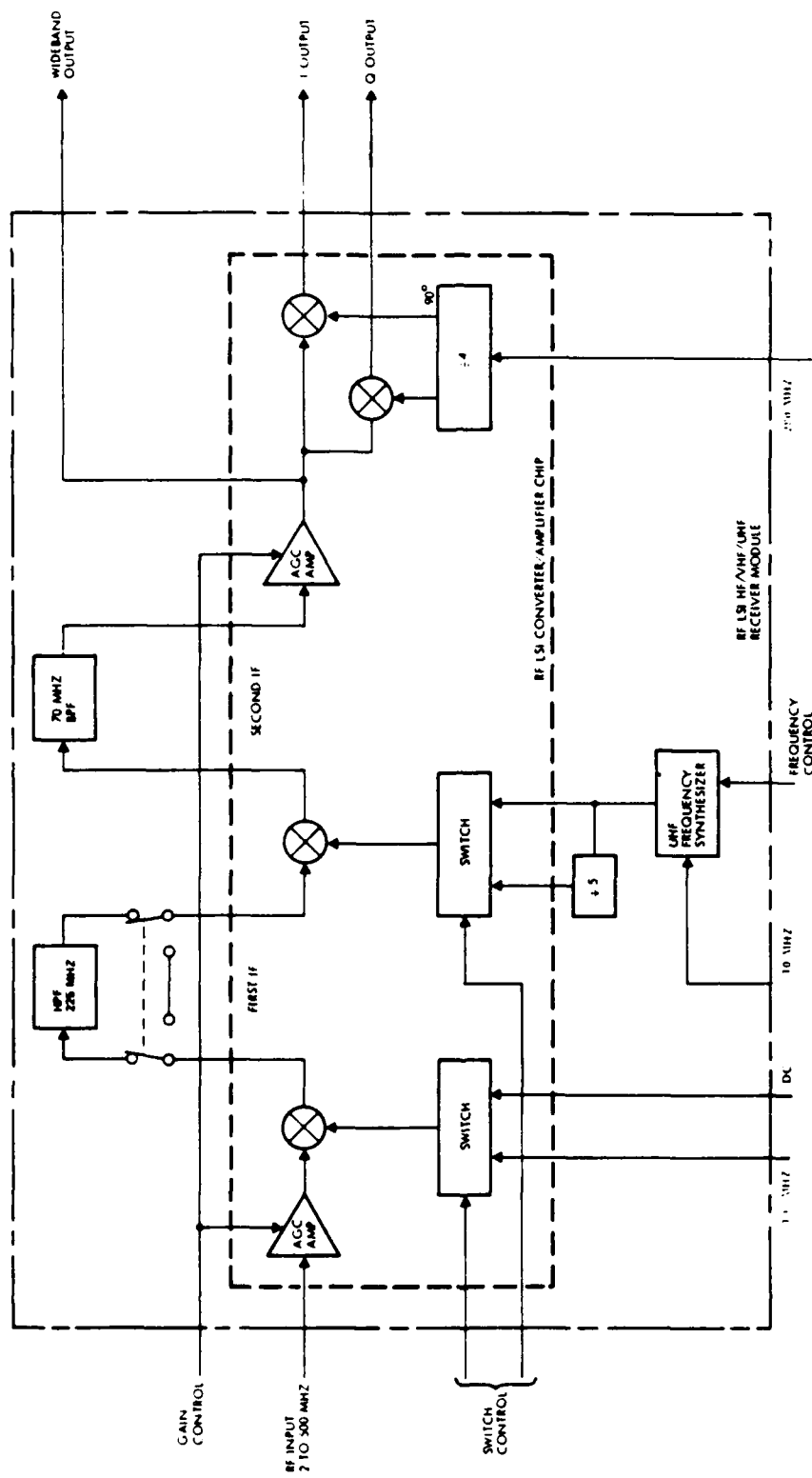


Figure 2-10. RF LSI HF/VHF/UHF Receiver Module

the required frequency range of 360 to 500 MHz. Consequently, it can also perform frequency de hopping. After bandpass filtering and amplification, the 70 MHz is then resolved into two quadrature components by mixing the third mixer stage with two 70 MHz references which are in phase quadrature. Since the communications functions in the HF region are basically narrow band, these quadrature outputs are then digitized and sent to the micro-signal processor for demodulation and processing.

In the case of the VHF band (30 to 150 MHz), the operation is similar to the HF band except that the first mixer stage is used to upconvert the signal into UHF band. The upconversion is achieved by selecting the first LO frequency at 195 MHz. Thus, the output signal of first stage mixer will be from 225 to 375 MHz. The second stage mixer then uses the standard UHF frequency synthesizer to frequency dehop or tune the receiver to a 70 MHz second IF, as in the case of the HF band.

The last case is the UHF band (225 to 400 MHz). As in the case for receiving, the HF band signal, the first mixer stage is again bypassed.

In the second mixer stage, the standard UHF frequency synthesizer is used directly as the LO and performs frequency tuning and de hopping, as in the case of UHF SATCOM.

For narrow band IF signals such as the frequency de hopped UHF SATCOM, the signal can be demodulated and detected by the microsignal processor as in previous cases. However, in the UHF band, wideband PN spread-spectrum signals, such as SEEK TALK, cannot be processed directly by the micro-signal processor. The receiver module provides a wideband 70 MHz IF output so that a wideband analog processor can be added to perform PN despreading.

In the baseline system, four HF/VHF/UHF receiver modules are provided to give the capability of receiving four signals simultaneously. These capabilities can be expanded and reduced with the MFBARS requirements.

2.2.8 HF/VHF/UHF Transmitter

The baseline design of the HF/VHF/UHF transmitter follows the same system design approach as the L-Band transmitter. As shown in Figure 2-11, the identical technique of using the microsignal processor to formulate the in-phase and quadrature channel inputs to the quadrature linear amplitude

modulator is employed to generate the modulation waveform for transmissions. Furthermore, a single power amplifier (Subsection 5.1) is to be used to cover the entire frequency band. The basic UHF frequency synthesizer is used as the source for the LO to convert the 70 MHz modulator output into the proper frequency for transmission as shown in Figure 2-11.

2.3 ALTERNATE SYSTEM

This subsection describes the alternate system design formulated in Phase I of this study. The general organization of the alternate system is shown in Figure 2-12. Key features of this organization are listed below.

- Separate receiver front-ends are dedicated to each of the required baseline functions.

Guard channels (one in each band):

2 to 30 MHz

30 to 88 MHz

108 to 156 MHz

225 to 400 MHz

Designated operating channels:

2 to 30	}	one per channel
30 to 88		
108 to 156		
225 to 400		two in band

- Receiver front-ends are dedicated to each of the baseline channels; they are not time-shared.
- Three separate transmitter power amplifiers are provided.

HF (2 to 30 MHz)

VHF/UHF (30 to 400 MHz)

L-Band (960 to 1215 MHz)

- The L-Band transmitter is time shared for:

JTIDS

TACAN

IFF

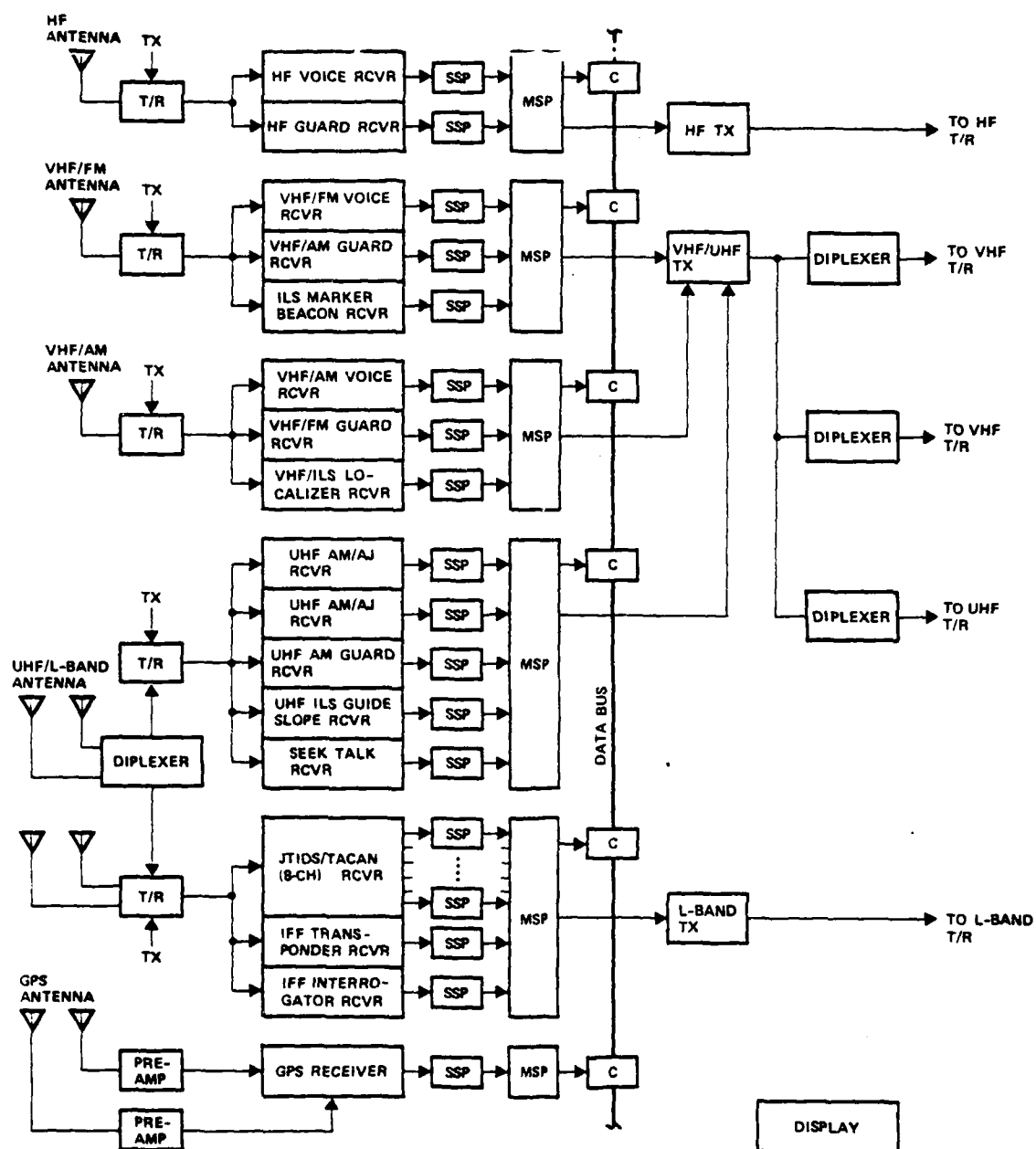


Figure 2-12. General Organization of Receivers and Transmitters

- The requirement is fulfilled for transmission on at least one channel corresponding to receiver band capability of:

2 to 30 MHz
 30 to 88 MHz
 100 to 156 MHz
 225 to 400 MHz

- Transmitter exciters (signal sources, modulators, upconverters, and frequency synthesizers) are, like the receivers, realized with RF LSI technology.
- Antenna subsystems are partitioned according to existing practice as follows:

HF
 VHF
 UHF
 L-Band
 GPS

- Interconnection and cross-connection between transmitters, receivers, and antennas is by antenna interface units containing diplexers, switches, filters, and T/R devices.

The premise leading to the architectures described above is that with RF LSI technology, the parallel system with dedicated functions can be realized at a reasonable cost. The effect of comparatively high development cost of RF LSI functional chips can be minimized by the multiple use of a single chip design. A key to this approach is to design these circuit chips with very wide bandwidths, and then connect band-determining functions (such as crystal IF filters, etc.) outside the package.

2.3.1 Receivers

The baseline architecture employs the following types of receiver modules:

HF Band (2 to 30 MHz)	HF voice
	HF guard
VHF/FM (30 to 88 MHz)	VHF/FM voice
	VHF/AM guard
	VHF/ILS marker beacon receiver

VHF/AM (119 to 124 MHz)	VHF/AM voice VHF/AM guard VHF/ILS localizer receiver
UHF (200 to 400 MHz)	UHF/AM/AJ (SEEK TALK - 2 channels) UHF/AM guard UHF/ILS glide slope receiver
L-Band (960 to 1575 MHz)	JTIDS/TACAN (8 channels) IFF transponder receiver IFF interrogator receiver GPS (5 channels)

Table 2-2 summarizes the electrical characteristics of the receivers, including references to existing avionics nomenclature.

The general format for all receivers is shown in Figure 2-13. The incoming RF signal passes through the antenna control unit to the receiver LRU. The signals are routed to an RF module containing three sections, an RF chip, a frequency synthesizer, and a decoder.

The RF chip contains a low noise amplifier, which sets the noise figure, and a mixer downconverter to the first IF frequency. Because bandpass filters are not easily constructed on the RF LSI chip, the signal is routed to the first IF bandpass filter located outside (adjacent to) the RF LSI package. The signal is routed back into the RF LSI chip where it is downconverted to the second IF frequency in the mixer downconverter.

As before, the second IF frequency is filtered in an outboard bandpass filter; in some instances, it is necessary to provide two bandpass filters with diode switches to allow selection by command. After filtering, the IF signal is routed back to the RF LSI chip for further amplification and demodulation.

Demodulation can be accomplished using a Costas loop demodulator located in the RF LSI chip; Figure 2-14 shows Costas loop demodulator chips built at TRW. Note that because of the size of the discrete components, the loop filter is located outboard of the RF LSI chip.

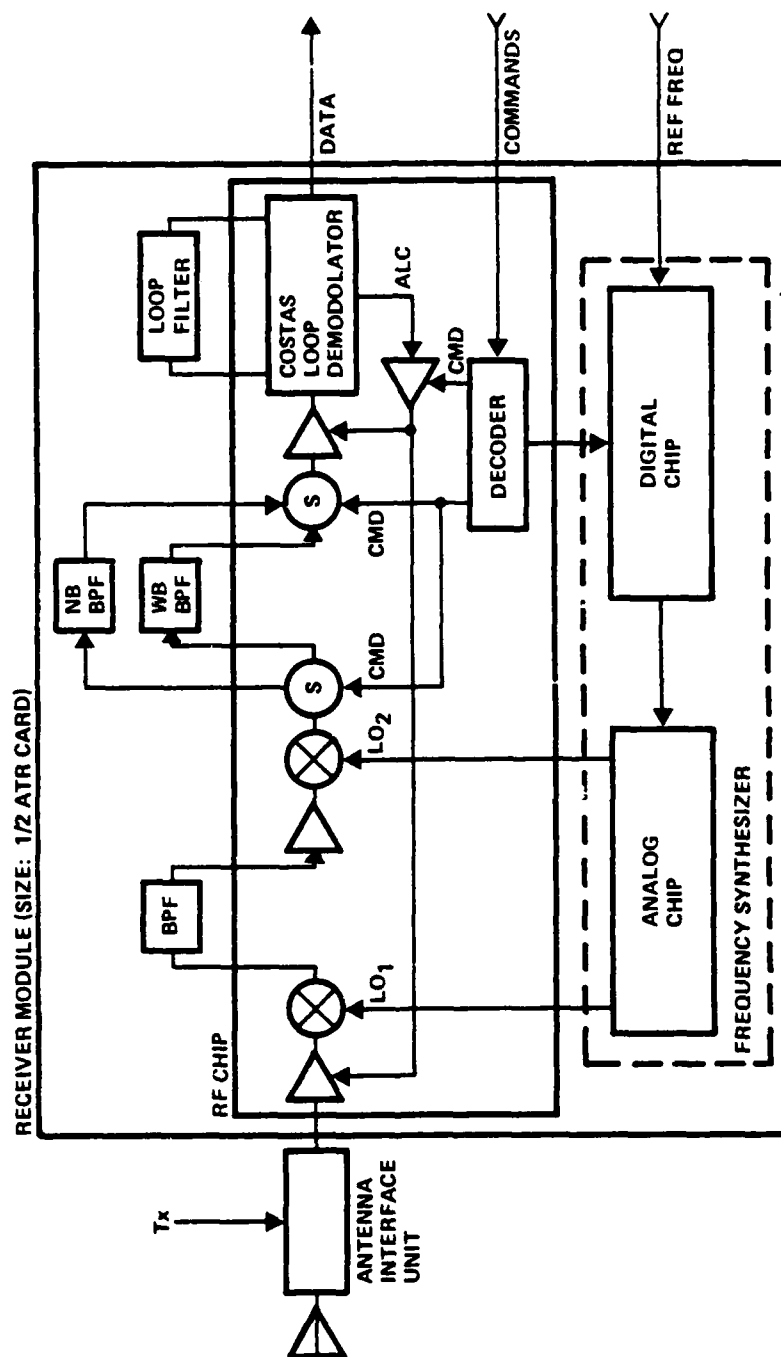


Figure 2-13. Generalized Block Diagram for RF LSI Receiver

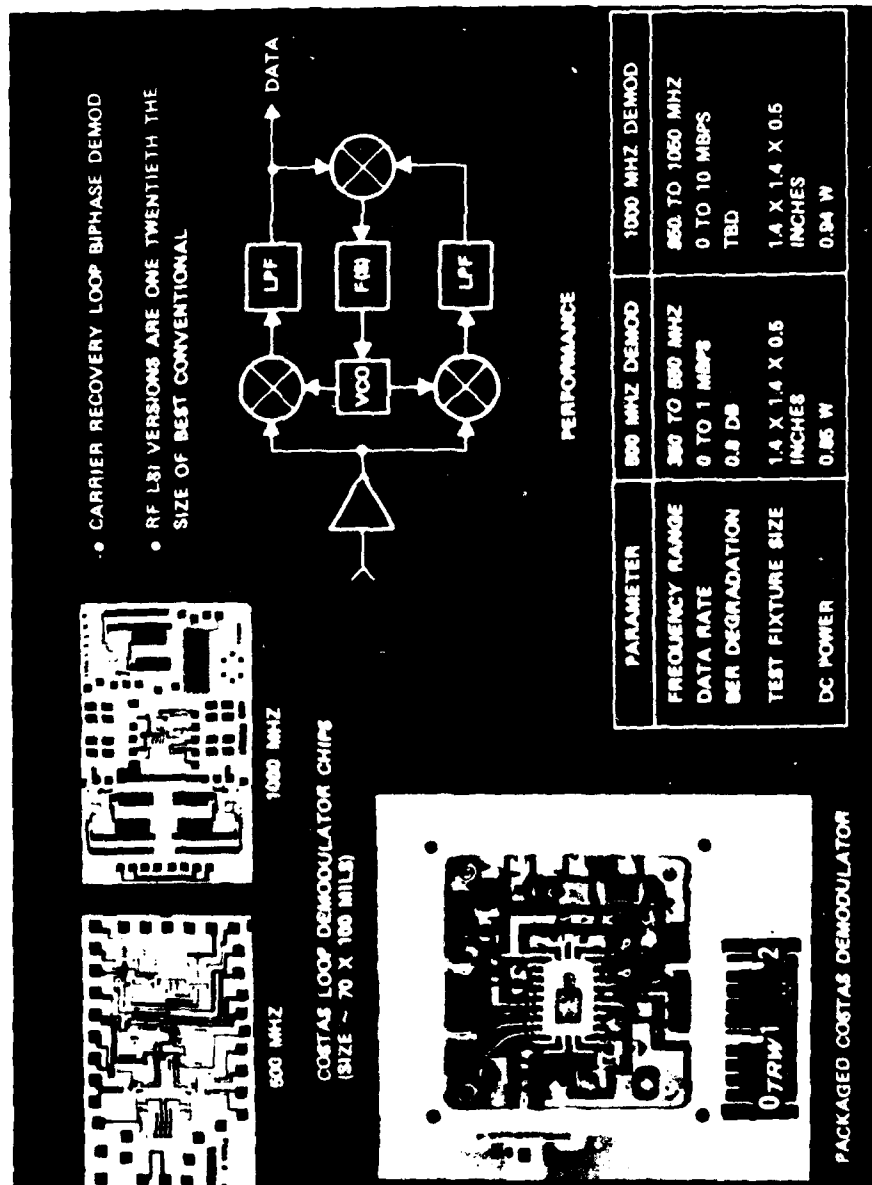


Figure 2-14. Costas Loop Demodulators

As shown in Figure 2-13, the strength of the RF signal can be controlled by the use of automatic gain control (AGC) loops which adjust the amplifier gain.

Bias current is supplied by dc amplifiers located on the RF LSI chip; the signal strength detector is located in the demodulator portion of the circuit.

Bandpass filters in the 100 to 1000 MHz range can be realized using surface acoustic wave (SAW) substrates.

Figure 2-15 shows the RF LSI version of the HF voice communications receiver module, based on the functional diagram for the existing AN/ARC-112; an identical RF module is used for the HF voice guard channel.

A block diagram for the VHF/FM voice channel is shown in Figure 2-16; the existing AN/ARC-131 is the basis for this configuration. The VHF/AM and UHF receivers are similar in layout and will also be realized in the 1/2 ATR card-size module (one module for each channel).

The L-Band JTIDS/TACAN/IFF receivers are shown in Figure 2-17. The received signal passes from the receiver antenna and antenna interface unit (Figure 2-18) to the L-Band receiver. Here, the signal is filtered and power-split to feed each of the eight JTIDS channels, the IFF interrogator receiver, and the IFF transponder receiver. Each of these receiver channels, including the associated frequency synthesizer, is packaged in separate RF modules the size of a standard 1/2 ATR card. It should be noted that the JTIDS channels require a sophisticated, fast-hopping LO source; nevertheless, the use of RF LSI and SAW filter technology allows the required miniaturization.

A block diagram of the GPS receiver is shown in Figure 2-19. An RF LSI version of this receiver is presently under development under a contract for NOSC. Work is now focused on the RF chip containing the RF amplifier, downconverter, and Costas demodulator. Objectives of this development include reduced size, weight, volume, power, and production costs. Each of the five receiver channels (including LO source) will be packaged in a module the size of a standard 1/2 ATR card. In the normal mode the four receiver channels track four satellites simultaneously on frequency L_1 ; the fifth channel is provided for simultaneous L_2 measurement or fifth satellite backup.

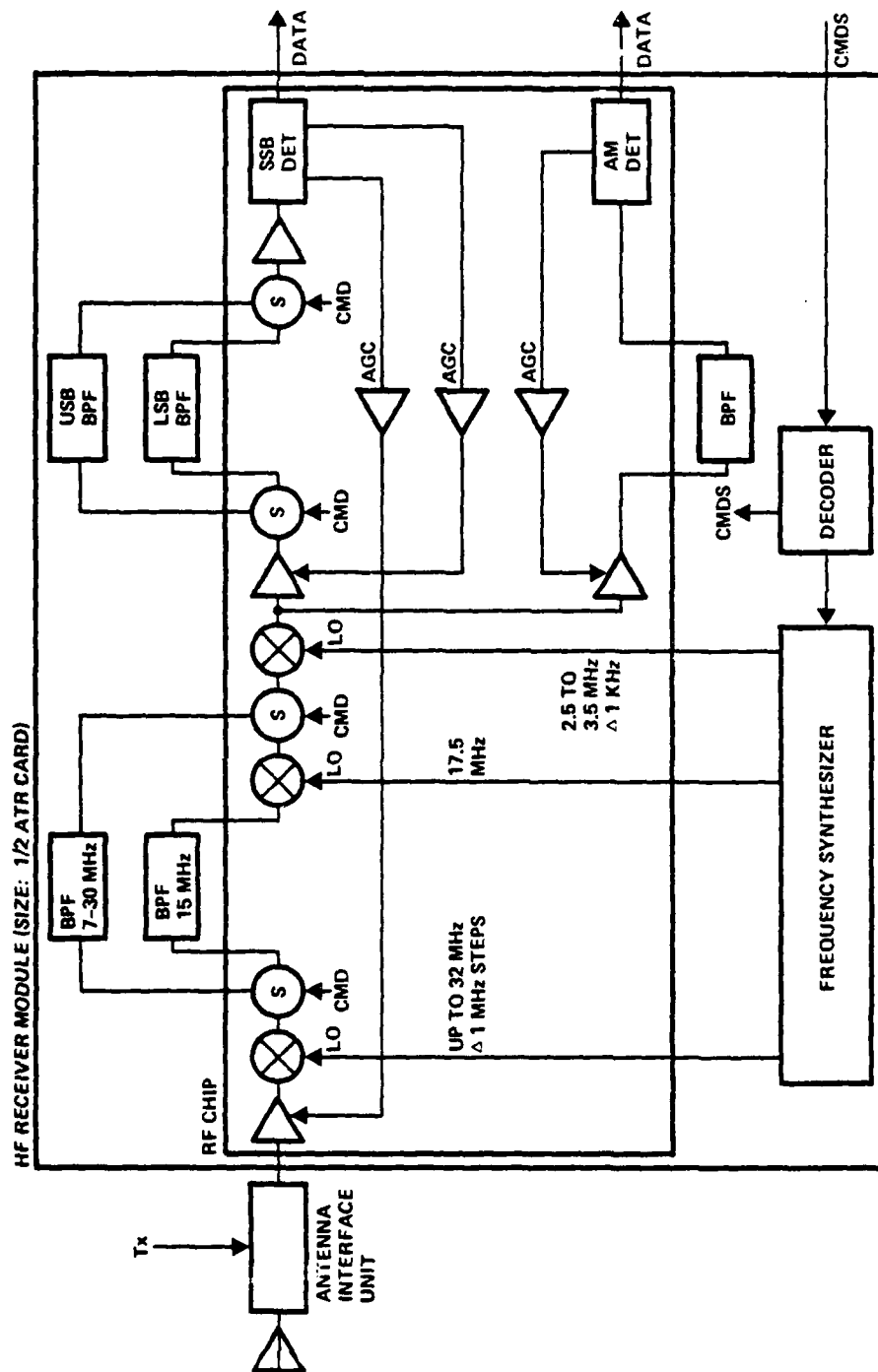
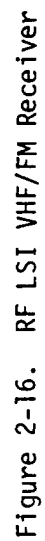


Figure 2-15. RF LSI HF Receiver



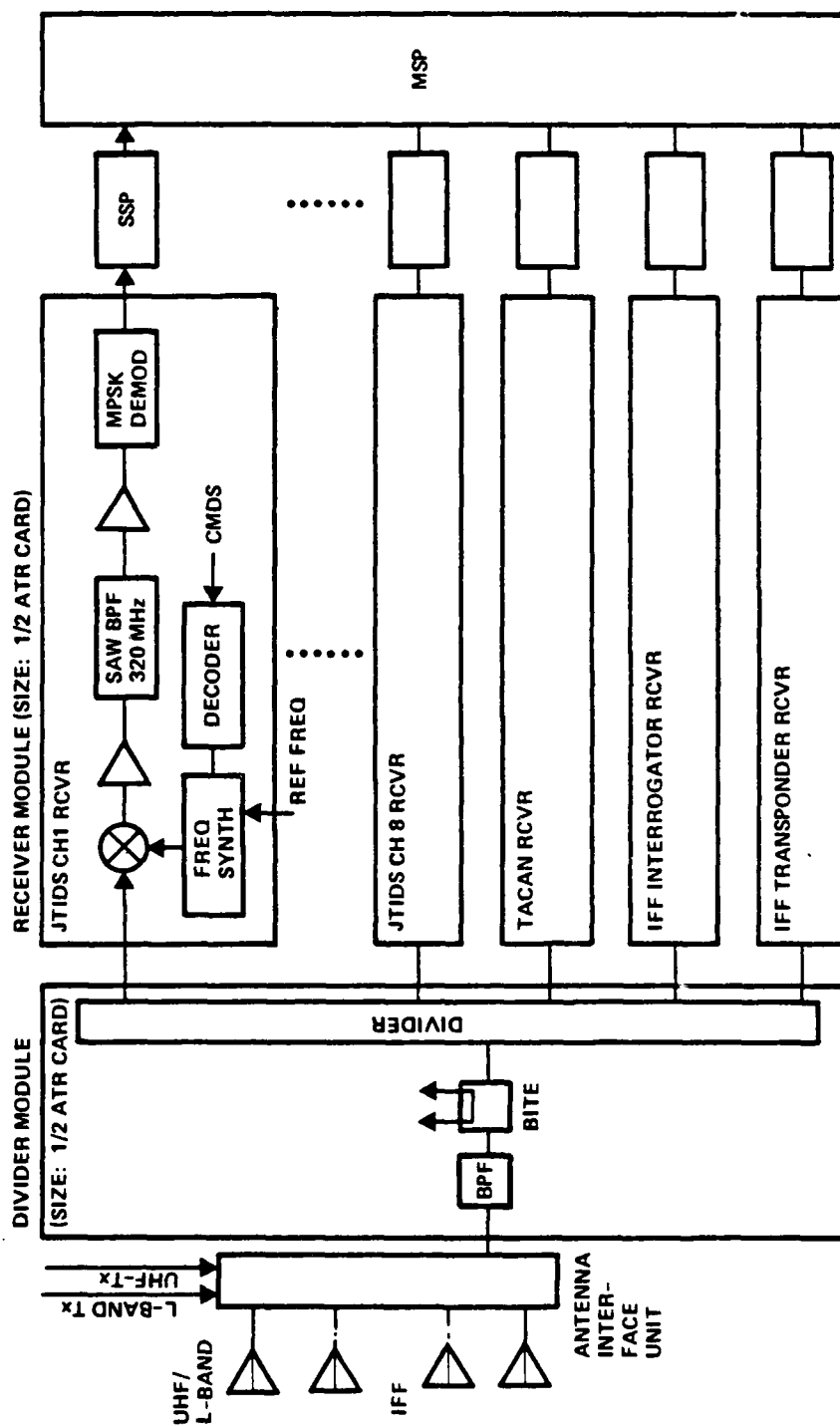


Figure 2-17. RF LSI L-Band Receiver

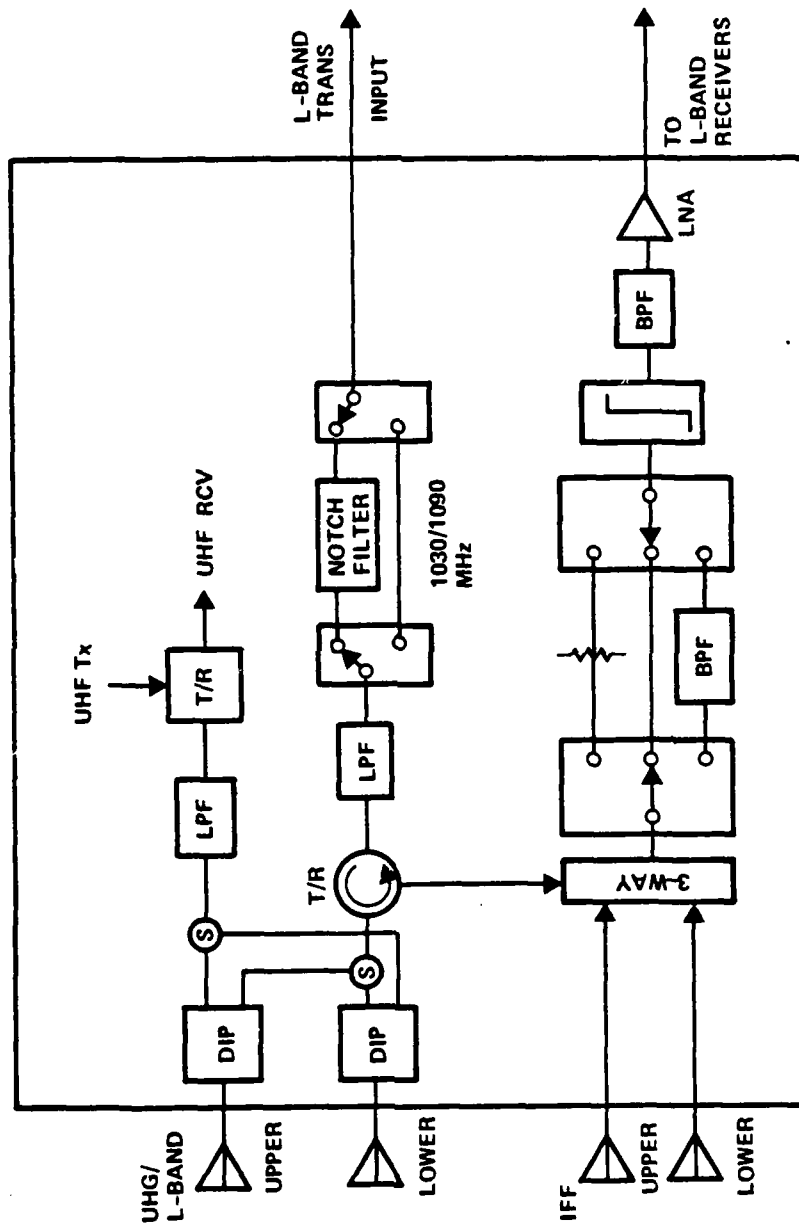


Figure 2-18. UHF/L-Band Antenna Interface Unit

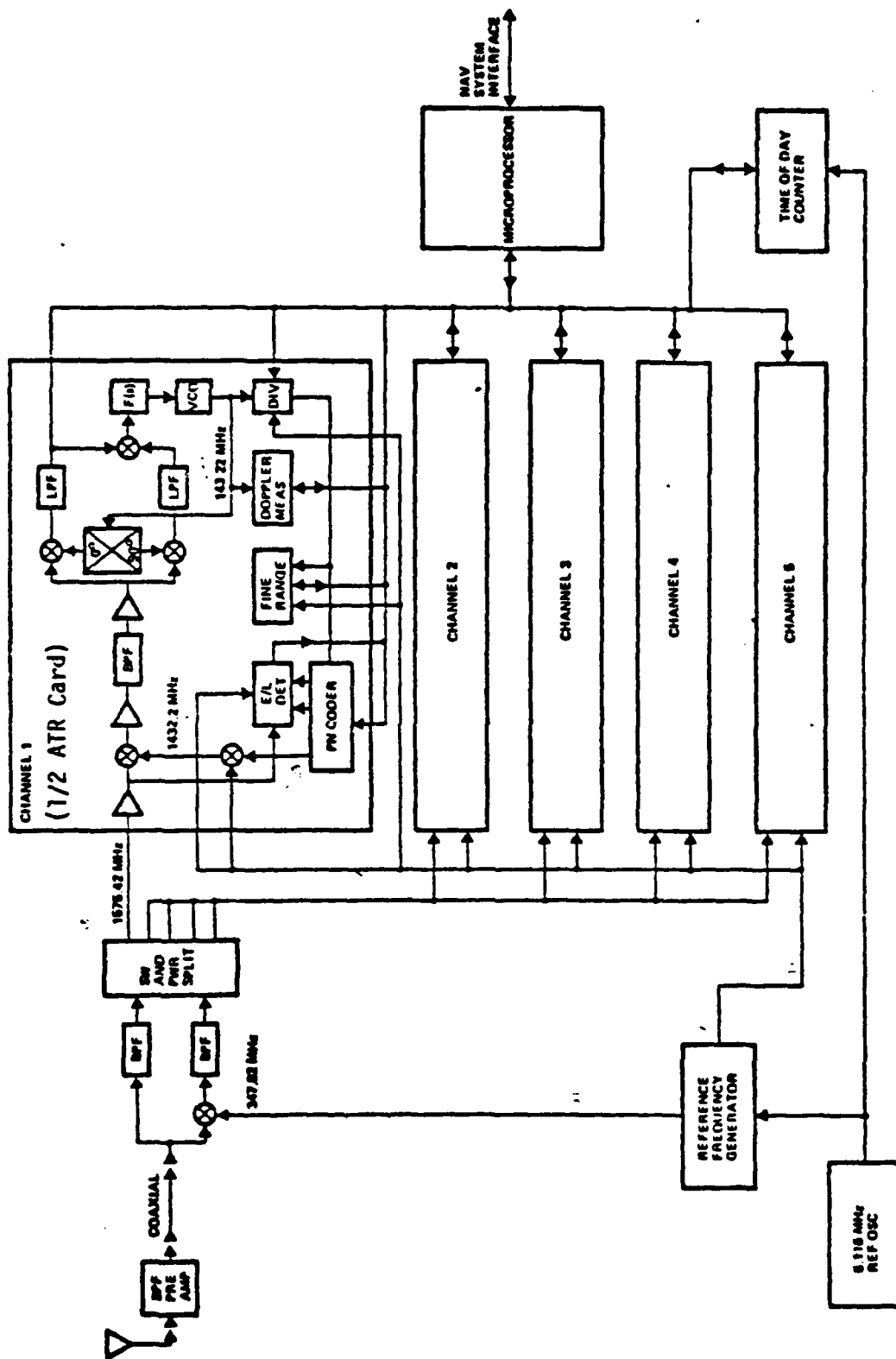


Figure 2-19. GPS Receiver System Block Diagram

2.3.2 Transmitters

As described above, the baseline architecture shows the HF, VHF, UHF and L-Band transmitters combined into three units:

HF (2 to 30 MHz)

UHF (30 to 400 MHz)

L-Band (960 to 1215 MHz)

Table 2-3 describes the functions of the transmitter, relating them to the service functions. The consolidation of the VHF/AM, VHF/FM and UHF transmitters into a single 30 to 400 MHz unit is the result of forecasted improvements in broadband power transistor technology. The use of emerging electron bombarded semiconductor (EBS) amplifier technology is applied to the L-Band transmitter for the JTIDS/TACAN/IFF functions.

Figure 2-20 gives a generalized block diagram for one of the baseline transmitters and shows the exciter/L0 source, power amplifier, power supply, antenna interface unit, and antenna. The same RF LSI technology referred to in the receivers is applicable to the exciter/L0 source/modulation function.

The antenna interface unit contains bandpass filters, diplexers, T/R switches, and impedance matching networks.

Figure 2-21 shows the HF transmitter functional block diagram based on the present AN/ARC-112. The exciter, frequency synthesizer, decoder, modulator, and upconverter are realized in RF LSI technology. The various bandpass filters are quartz and discrete component types. All of these functions are contained in a single 1/2 ATR card-size module.

The VHF/UHF transmitter covers the 30 to 400 MHz frequency range and is similar in configuration to the HF transmitter described above.

The block diagram for the L-Band transmitter is given in Figure 2-22. The modulator, frequency synthesizer, upconverter, and modulator functions are realized in two modules, each the size of a standard 1/2 ATR card. As in the baseline system, an EBS power amplifier is also used.

Table 2-3. MFBARS Transmitter Types

SERVICE			MFBARS TRANSMITTER		
DESCRIPTION	FREQUENCY (MHZ)	RF POWER	DESCRIPTION FREQUENCY (MHZ)	RF POWER	DEVICE TYPE
HF (VOICE GUARD)	2-20	400 W PEP 123 W CARRIER	HF 2-20 HF 2-20	400 W PEP 123 W CW	100 W FET 100 W FET
VHF FM (VOICE GUARD) VHF AM (VOICE GUARD) UHF RADIO (VOICE GUARD) SEEK TALK (VOICE COM)	30-88 108-156 225-400 225-400	1 W/10 W SELECTABLE 40 W 10 W 30 W AS 10 W AM	UHF 30-400 UHF 30-400	1 W/10 W (CLASS C) 40 W (AB) 1 W/10 W (CLASS C) 40 W (AB)	50 W BIPOLAR TRANSISTOR 50 W BIPOLAR TRANSISTOR
JTIDS TACAN IFF TRANSPONDER IFF INTERROGATOR	960-1215 962-1213 1090 1030	0.5/2 KW (20% DUTY) 0.5/2 KW PK 0.5 KW PK (1% DUTY) 1.0 TO 2.5 KW PK (1% DUTY)	D-BAND 960-1215 D-BAND 960-1215	0.5/2.5 KW PK 2.0 KW (20% DUTY) 2.5 KW (1% DUTY)	0.5 KW EBS 0.5 KW EBS

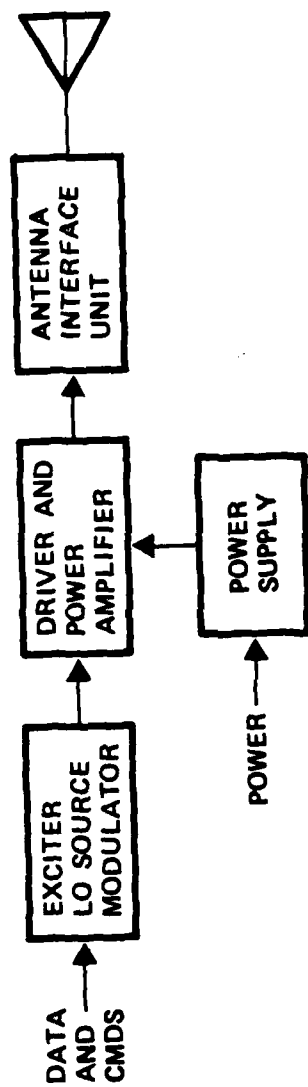


Figure 2-20. Generalized Block Diagram of Baseline Transmitter

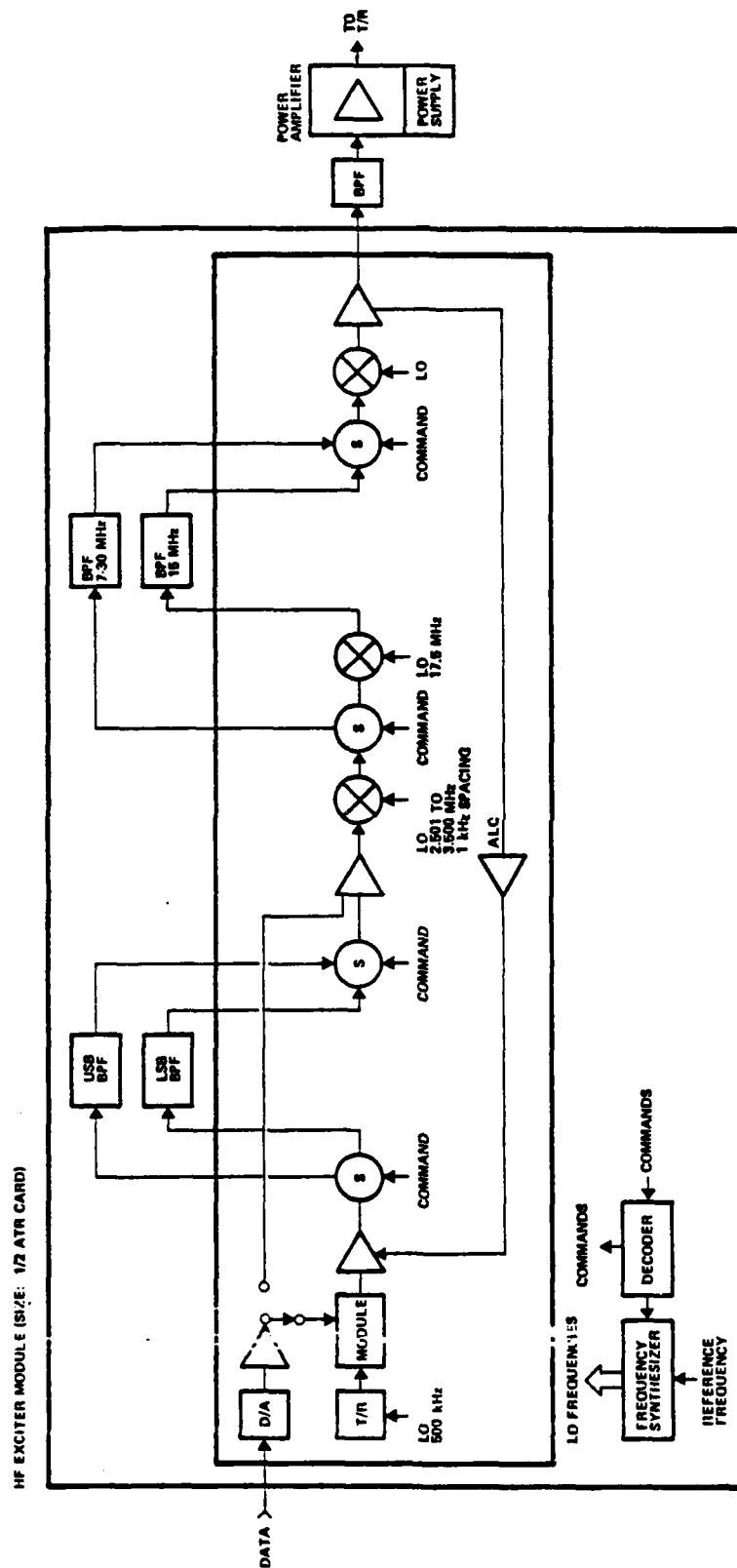


Figure 2-21. RF LSI Exciter for HF Transmitter

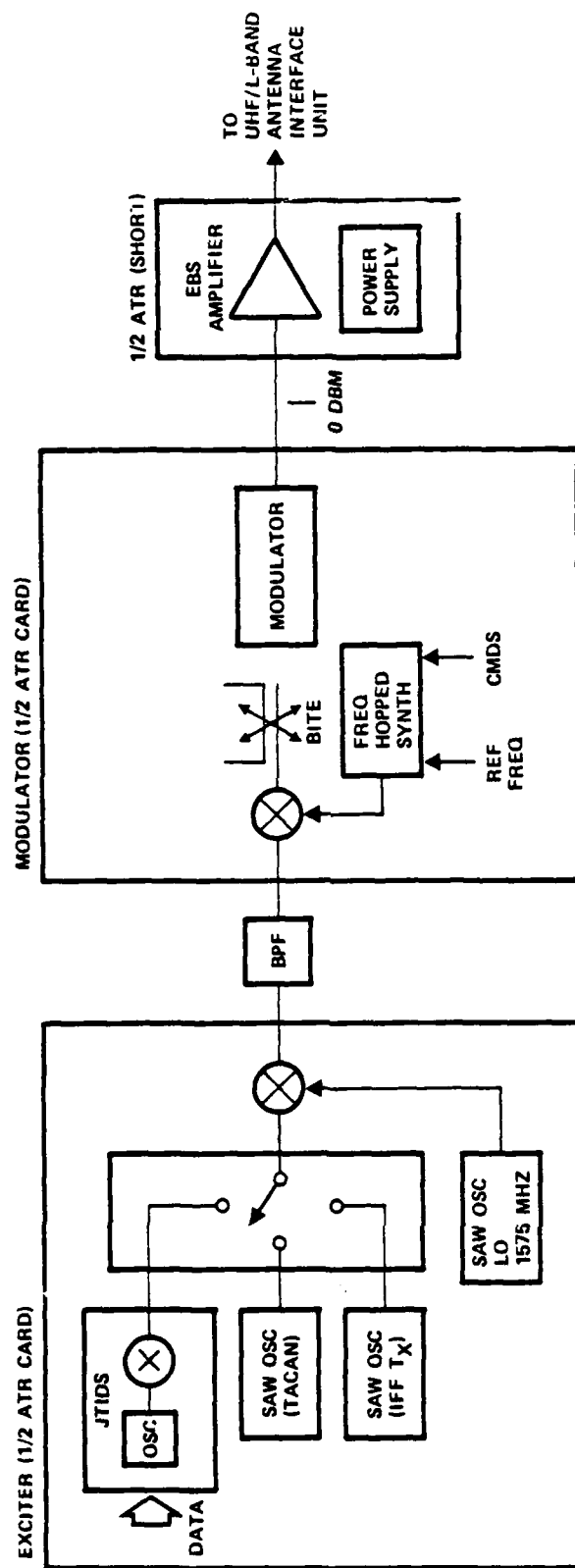


Figure 2-22. L-Band Transmitter

3. EQUIPMENT PARTITIONING

To fully utilize the standard module concepts and to assess the approximate size of the MFBARS terminal, the baseline system was partitioned into LRU and slices. The results are presented in this section and indicate that the electronics, exclusive of the antenna, can be packaged into one full ATR and two half ATR housings (Figure 3-1). The two one-half ATR house the L-Band transmitter and HF/VHF/UHF transmitter. The remainder of the ICNIA terminal is housed in the full ATR and includes all RF/IF circuits for the receivers as well as the microsignal processors. The partition studies show that the total MFBARS can be separated into 21 modules/slices as tabulated in Table 3-1, which indicates that 14 modules are required for the ICNIA terminal, 4 modules for the L-Band transmitter, and 3 modules for the HF/VHF/UHF transmitter. The circuits and components included in each module are summarized in this section.

Except for the specialized modules, modules are housed in either RF slices of 4 x 6 x 1 inches or in 4 x 6 x 1/2 inch digital circuit cards. A brief description of each module is given in the following paragraphs.

3.1 ICNIA TERMINAL

- 1) L-Band Receiver RF Switch. This module will have a unique design and will contain all of the preselectors, L-Band preamplifiers related to the L-Band receiving functions, and an RF switch which will enable the terminal to connect any one antenna to one or more L-Band frequency de hopping modules. These modules basically relate the functions shown in the block diagram in Figure 2-3, L-Band front end.
- 2) L-Band Frequency De hopping Converter. Five modules are used in the ICNIA terminal. They contain all of the components in the L-Band frequency de hopping converter as shown in Figure 2-4.
- 3) L-Band IF Switch. This module, packaged in standard slices, houses a switching matrix interconnecting the five L-Band frequency de hopping downconverters with various IF processors.
- 4) GPS Demodulator. This module houses the complete GPS demodulator, including PN code generation. The RF functional block diagram is shown in Figure 2-5.
- 5) JTIDS Demodulator. This module houses the JTIDS demodulator. Its functional block diagram is shown in Figure 2-6.

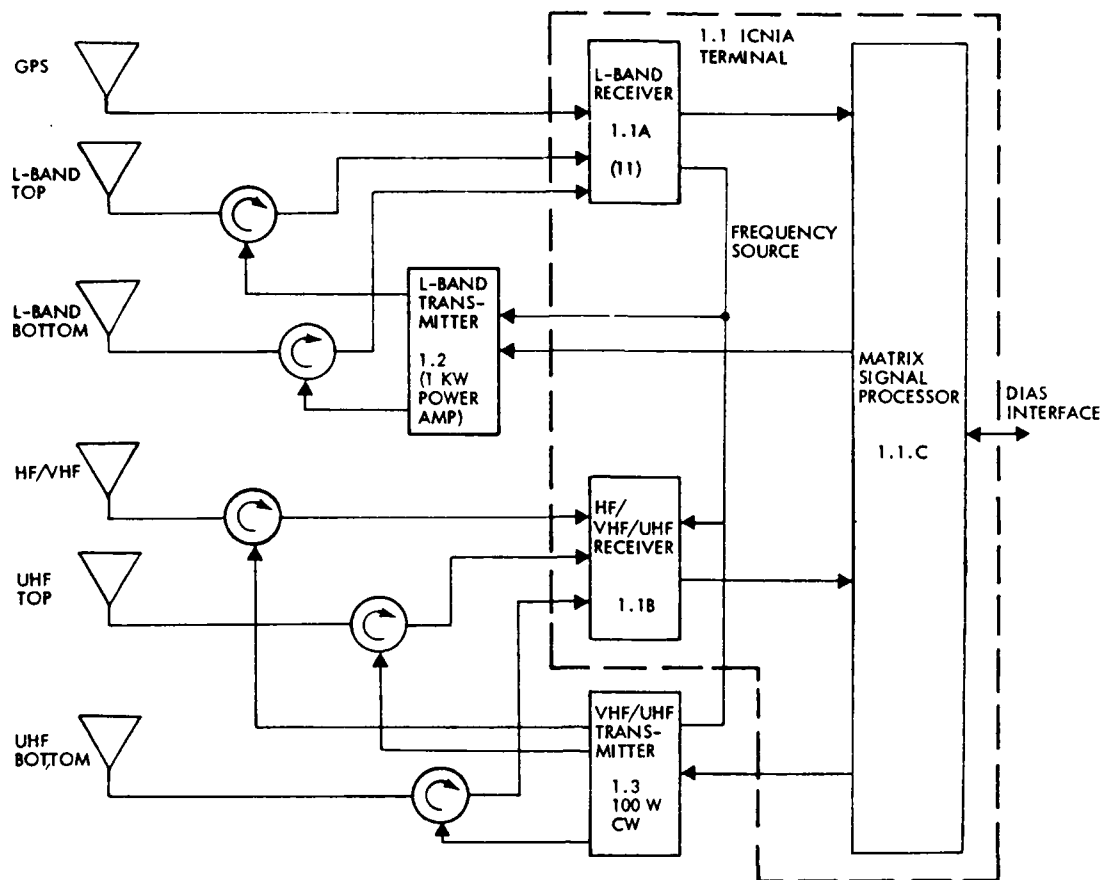


Figure 3-1. MFBARS Block Diagram

- 6) IFF/TACAN Demodulator. This module houses two IFF/TACAN demodulators whose functional block diagram is shown in Figure 2-7.
- 7) Reference Frequency Source. This module contains the crystal oscillator for use as the frequency standard for the terminal. It also contains the frequency multiplier to generate some of the required local oscillator signals.
- 8) HF/VHF/UHF Receiver RF Switch. Similar to the L-Band counterpart, this is a unique module and contains the preselector and bandpass filter for the HF/VHF/UHF front end as shown in Figure 2-9 as well as a matrix switch to connect any antenna to one or more of the HF/VHF/UHF receiver modules.
- 9) HF/VHF/UHF Receiver Module. This module houses all of the components necessary to implement the functional diagram shown in Figure 2-10. Four of these modules are used in the ICNIA terminal.

Table 3-1. MFBARS/INCIA Slices/Components

STANDARD SLICE/APPLICATIONS	MFBARS	JTIDS	GPS	JTIDS/ GPS	JTIDS/IFF /TACAN	GPS/IFF /TACAN	GUARD	VHF RADIO	UHF SATCOM	SEEK TALK	UHF/ SEEK TALK	VHF/ UHF
INCIA TERMINAL												
1. L-BAND RECEIVER RF SWITCH	1	1	1	1	1	1	---	---	---	---	---	---
2. L-BAND FREQUENCY DEHOPPING CONVERTER	5	4	2	4	5	4	---	---	---	---	---	---
3. L-BAND IF SWITCH	1	---	---	1	1	1	---	---	---	---	---	---
4. JTIDS ^c DEMODULATOR	1	1	---	1	1	---	---	---	---	---	---	---
5. GPS DEMODULATOR	1	---	1	1	---	1	---	---	---	---	---	---
6. IFF/TACAN DEMODULATOR	2	---	---	---	2	2	---	---	---	---	---	---
7. REFERENCE FREQUENCY SOURCES	1	1	1	1	1	1	---	---	---	---	---	---
8. VHF/UHF RECEIVER RF SWITCH	1	---	---	---	---	---	1	1	1	1	1	1
9. HF/VHF/UHF RECEIVER MODULE	4	---	---	---	---	---	1	1	2	1	2	2
10. HF/VHF/UHF IF SWITCH	1	---	---	---	---	---	---	---	1	---	1	1
11. SEEK TALK DEMODULATOR	1	---	---	---	---	---	---	---	---	---	1	---
12. IF FREQUENCY SOURCES	1	---	---	---	---	---	1	1	1	1	1	1
13. PREPROCESSOR	1	1	1	1	1	1	1	1	1	1	1	1
14. MATRIX SIGNAL PROCESSOR	4X4	2X2	1X1	4X4	2X2	1X1	1X1	1X1	1X1	1X1	1X1	1X1
L-BAND TRANSMITTER												
15. MODULATOR FOR L-BAND	1	1	---	1	1	1	---	---	---	---	---	---
16. L-BAND XMITTER DRIVER	1	1	---	1	1	1	---	---	---	---	---	---
17. L-BAND POWER AMPLIFIER	1	1	---	1	1	1	---	---	---	---	---	---
18. L-BAND XMITTER ANTENNA INTERFACE	1	1	---	1	1	1	---	---	---	---	---	---
HF/VHF/UHF TRANSMITTER												
19. HF/VHF/UHF MODULATOR/EXCITER	1	---	---	---	---	---	1	1	1	1	1	1
20. HF/VHF/UHF POWER AMPLIFIER	1	---	---	---	---	---	1	1	1	1	1	1
21. HF/VHF/UHF ANTENNA INTERFACE	1	---	---	---	---	---	1	1	1	1	1	1

- 10) HF/VHF/UHF IF Switch. This module contains a switch matrix which interconnects the four HF/VHF/UHF receiver modules to the digital preprocessors or to the SEEK TALK demodulator.
- 11) SEEK TALK Demodulator. The SEEK TALK demodulator has not yet been defined. It is assumed that it is similar to the JTIDS demodulator in complexity and, thus, can be housed in one standard module.
- 12) IF Frequency Source. This module houses all of the required local oscillator frequency sources not contained in the reference frequency source module.
- 13) Preprocessor. This is a digital module composed of four standard digital circuit cards. It contains the A/D converters and delicate digital circuits which perform high-speed processing. This module acts as an interface between the IF subsystems and the microsignal processor.
- 14) Microsignal Processor. This module contains 12 digital circuit cards for a 2 x 2 matrix signal processor. They are described in Section 6 of this report.

3.2 L-BAND TRANSMITTER (FIGURE 2-8)

- 1) Modulator for L-Band. This module contains the components which perform the modulation and frequency conversion shown in Figure 2-8.
- 2) L-Band Transmitter Driver. The L-Band transmitter driver contains a frequency synthesizer to perform frequency hopping and turning for transmission as well as an amplifier to boost the signal to a level high enough to drive the power amplifier.
- 3) L-Band Power Amplifier. This is a specially designed module which houses the 1KW EBS amplifier and its associated power supplies.
- 4) L-Band Transmit Antenna Interface Unit. This is also housed in a specialized slice and contains the bandpass filter and antenna select switches.

3.3 HF/VHF/UHF TRANSMITTER (FIGURE 2-11)

- 1) HF/VHF/UHF Modulator/Exciter. This module contains the RF components which perform the functions of modulation, frequency hopping and conversion, and amplification for the HF/VHF/UHF transmitter.
- 2) HF/VHF/UHF Power Amplifier. This module has to depart from the standard slice housing in order to accommodate the heat dissipation requirements of the HF/VHF/UHF power amplifier. The power supply for the power amplifier is also contained in this module.

- 3) HF/VHF/UHF Antenna Interface Unit. This module contains all band-pass filters and switches which connect the transmitter to any of the HF/VHF/UHF antennas.

Table 3-1 also shows the flexibility of the partitioning. The modules and the number of modules required can be tailored to individual user requirements. Module requirements can range from a full complement of modules for a completed MFBAR terminal to 8-module complements for the VHF radio.

Mechanically, the MFBARS terminal design is conceptualized as shown in Figures 3-2, 3-3, and 3-4. The mechanical design has three options, depending on the availability of cooling. Options A and B assume that the aircraft supplies forced air for cooling; these options include conduction and forced convection heat transfer. Heat from the components will be dissipated through metallic paths to the inner walls of the parallel heat exchangers. Each slice and PWB has two wedge lock devices which lock into channels on the inner side walls. This ensures a maximum contact between the unit thermal paths and the heat sink surfaces. Forced air cooling through the heat exchangers removes the heat load from the ATR box.

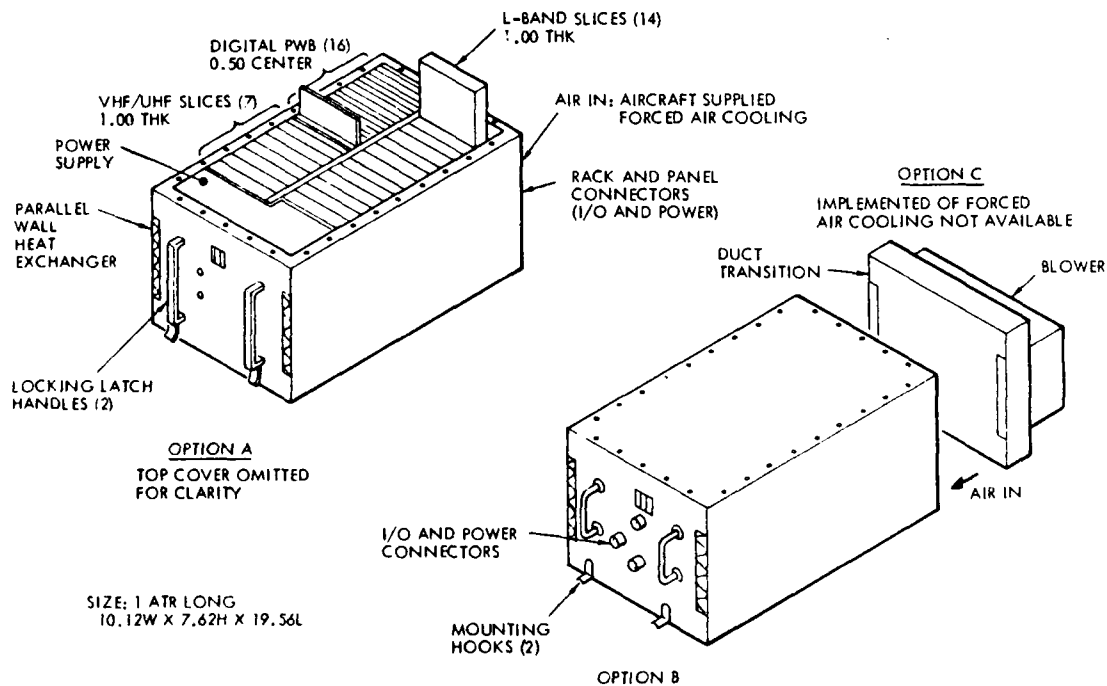


Figure 3-2. ICNIA Terminal

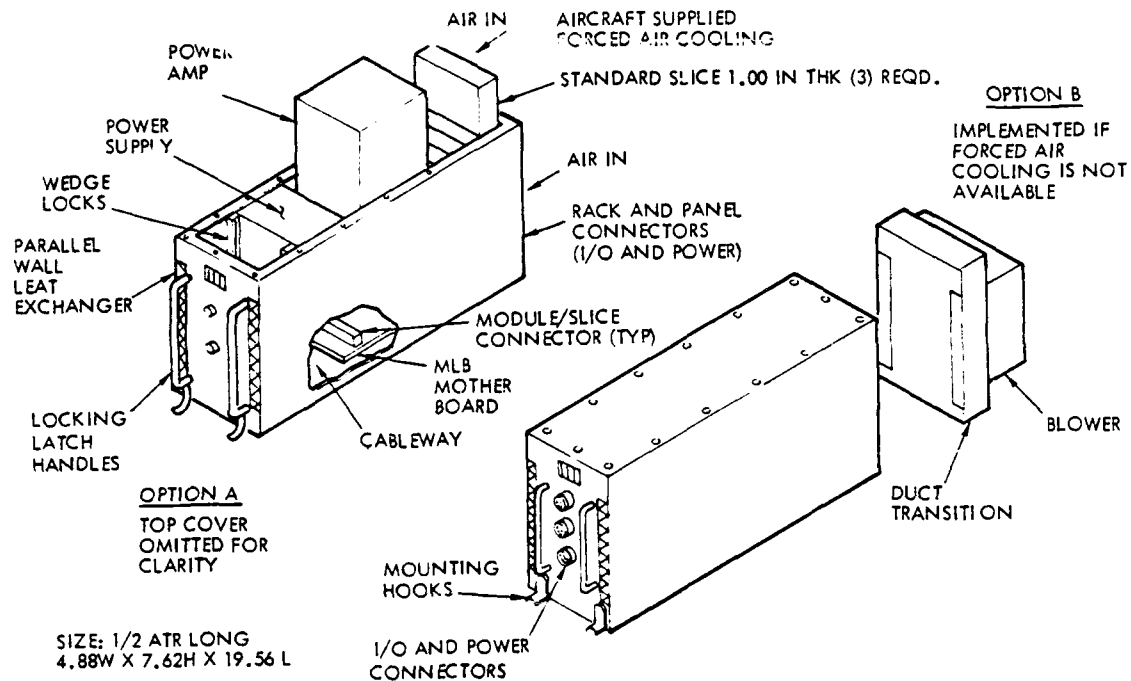


Figure 3-3. L-Band Transmitter

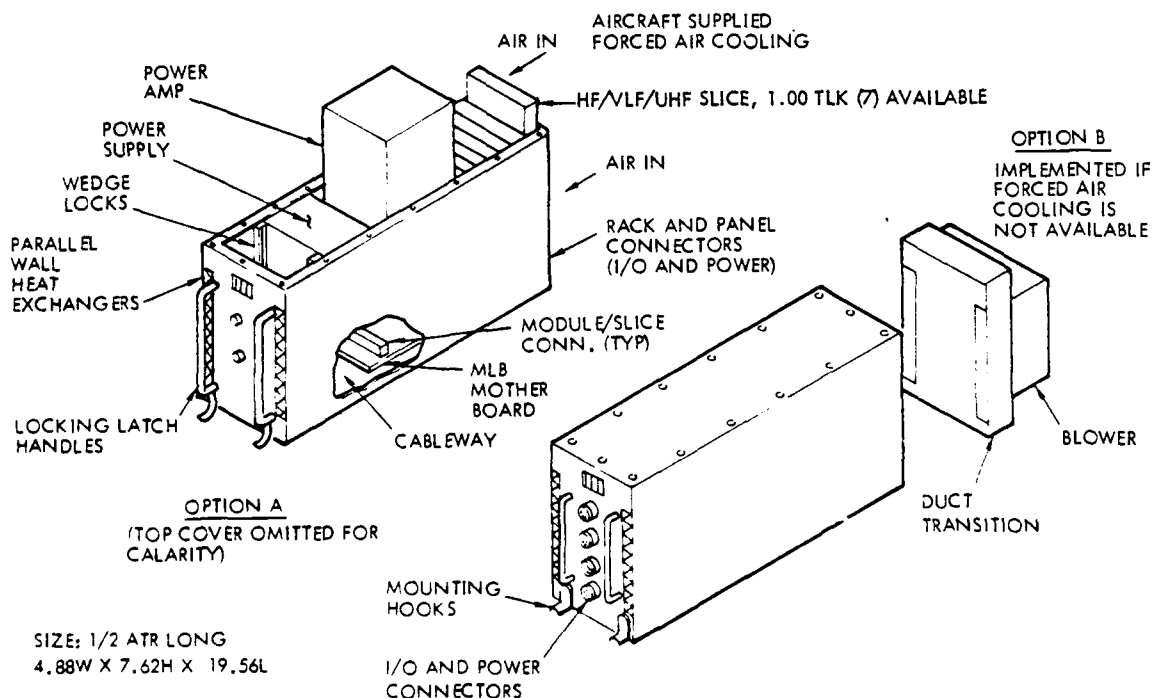


Figure 3-4. HF/VHF/UHF Transmitter

The thermal design objective is to ensure that the temperatures of the electronic components are maintained at satisfactory levels for electrical performance and long-term reliability when exposed to combined extremes of ambient temperatures and power. To meet this objective, the proposed design will include the following:

- High power dissipating components are mounted with efficient thermal conduction paths, of minimum length, to their respective mounting surfaces.
- The number of structural interfaces between parts and the ultimate heat sink are minimized in order to reduce overall thermal resistance.
- Interfacial conductances shall be enhanced by using interfacial filter materials as required.
- Temperature sensitive components are located away from higher power dissipating components to minimize thermal conduction and radiation from high powered parts.

The wedge lock devices also provide maximum resistance to shock and vibration.

Option C is intended for use when no aircraft forced air cooling is available. Option D (not shown) transfers heat from dissipating components by conduction to the chassis side walls, and then by natural convection at the side wall fins. In this case, a blower is provided as shown. The ICNIA terminal is housed in a full ATR box and consists of 21 RF standard slices and 16 digital printed wiring boards. The design of the 2 transmitters is expected to be similar, and consists of 3 standard RF slices and their power amplifier and associated power supplies.

EMI/EMC

Electromagnetic shielding is provided at each ATR box removable interface in the form of EMI/environmental gasketing. To accommodate the required attenuation at the specified frequencies, careful attention will be paid to the selection of shielding gaskets, grooves, and the spacing of attachment screws. The aim of shielding is to ensure ATR compliance to the requirements of MIL-STD-461 and MIL-STD-462. It is intended to provide reasonable assurance of subsequent compatible integration and operation aboard the flying system.

Structural Design

To ensure major resonant responses above the frequency range of the maximum input, the ATR chassis design has been configured to present a reasonably rigid housing for the slices and PWBs. Stresses will be maintained below endurance vibration test limits to provide assurance that no problems will occur.

4. ADAPTIVE ANTENNA DESIGN

This section describes an adaptive processor design suitable for incorporation into the MFBARS system. The principal task was to provide a design for a high-performance, cost effective, integrated adaptive array processor. Important constraints observed were that the processor accommodate multifunctional, multiband radio services, and that it be compatible with the basic radio design philosophy. Required performance was established on the basis of independent studies performed at Harris on the GPS and JTIDS systems, plus other studies directly relevant to the SEEK TALK problem and SINGARS application. Major efforts were directed toward reducing the overall costs while retaining required performance. Significantly, cost reduction implies size, weight, power, and complexity reduction as well. It is believed that the hybrid analog-digital approach described herein represents the best overall choice consistent with these constraints.

Antenna array design topics first receive consideration in subsection 4.1. This subsection is comprised of: design factors, grating conditions, and design solutions. Topics include signal coverage requirements, threat reduction requirements, platform properties, multiple service elements, grating lobe and grating null considerations, and a presentation of an effective compromise array design for the MFBARS problem.

Subsection 4.2 is devoted to algorithm considerations. Potential realizations, an important topic, is treated in paragraph 4.2.5 where analog, digital and analog/digital hybrid configurations are compared. Leading algorithm candidates are presented in paragraph 4.2.6; paragraph 4.2.7 summarizes major digital processor performance requirements.

Configuration of the adaptive processor and radio components are discussed in paragraph 4.3. The selected arrangement and reasons for this arrangement are first given in paragraph 4.3.1. Paragraph 4.3.2 is a brief discussion of the required interfaces between the adaptive processor and other components, such as the antenna array and the MFBARS radio.

Conclusions and recommendations for the antenna array are given in subsection 4.4. Paragraph 4.4.1 is a review of the need for multiple use arrays, the hybrid digital-analog type adaptive processor, and separate adaptive processor radio designs. Paragraph 4.4.2 is devoted to a summary of additional development required if the approach described herein is to become an effective one. Specifically, identified needs are a wideband JTIDS/GPS element, a low-loss RF weight design, technology for developing antenna array placement, and a detailed determination of required interfaces.

4.1 ANTENNA ARRAY DESIGN

Topics discussed in this subsection include array design factors, grating null limitations, and design solutions for the MFBARS problem. Figures showing suggested antenna locations are provided, as well as discussion of a possible broadband element design.

4.1.1 Design Factors

Those design factors given consideration herein are signal coverage requirements, threat reduction requirements, platform properties, and multiple service elements.

4.1.1.1 Signal Coverage Requirements

It is desirable that each antenna element in the array for a specific MFBARS function be capable of providing a useful degree of desired signal gain. Furthermore, it is necessary that, under the condition of interference being present, the weighted combination of antenna element inputs provide a minimum acceptable desired signal gain. In the case of GPS, due to the fact that very weak signals are being received, absolute gain is very important. Alternatively, in the case of SEEK TALK or, to a lesser extent JTIDS, signal path margins are better and some gain compromise may be acceptable.

Polarization requirements must also be satisfied, but, because of the diversity of requirements in a given band, a common element may not provide satisfactory performance (GPS requires circular polarization while JTIDS requires linear-vertical).

Both the antenna element and the array as a whole must be capable of meeting minimum bandwidth requirements for the wideband signals expected in the L-Band. The JTIDS requires a wider bandwidth than GPS since any of a multitude of narrowband slots may be used for transmission and reception. Although GPS has a wider instantaneous bandwidth than any given JTIDS transmission, total bandwidth requirements are substantially less than for JTIDS. However, the fact that GPS must operate on widely separated frequencies L_1 and L_2 means that either a GPS element must be substantially broadband or be tuned at the two frequencies.

4.1.1.2 Threat Reduction Requirements

In addition to providing desired signal gain, a suitable antenna array must also be capable of the desired degree of threat reduction. From a fundamental point of view, enough antenna elements must be provided to ensure ones ability to cancel the several interfering sources. However, from a practical point of view, it is desirable to have many additional elements so as to allow some degrees of freedom for treatment of the desired signal and for accommodation of array and circuit dispersion effects.

In the case of VHF and UHF desired signals such as SINCGARS and SEEK TALK, the number of antenna elements will be less determined by the potential threat than by the number of antenna elements than can be physically placed upon the platform.

Relative location of the antenna elements is also very important in threat reduction in that array resolution as well as grating conditions are determined by the relative spacing of the antenna elements. Furthermore, some elements will have a field of view that is different from others. Elements located in such a position that view of a jammer is blocked by a wing or fuselage will be relatively ineffective in contributing to a jammer null; thus, degrees of freedom can be reduced. Furthermore, jammer signals arriving at those elements can be highly dispersed due to vehicle multipath.

Vehicle multipath, a form of mutual coupling, is a very important contributor to null depth limitation. Significantly, in order to get a 35 dB null against a particular interferer over a given bandwidth it is

necessary that signals in two different pathways agree to within 0.05 dB and 0.95 degree rms phase. This is a severe requirement. Consider for a moment two antenna elements, one located on top of a fuselage and one below. Consider a jammer on the ground located so that the lower element views the jammer relatively well while the top element views the jammer from behind the wing. Signals reach the top element primarily through diffraction paths; for example, from the vertical stabilizer or from waves creeping around the wings. Even then, signals received by the lower element are not completely free of dispersion in that the direct path may well be augmented by a reflected path including the wing. It is not difficult to see that vehicle multipath can severely limit achievable null depth.

4.1.1.3 Platform Properties

Possibly the most important platform induced constraint is that of available space. From a gain standpoint, it is clear that the platform area defines maximum achievable gain. In the case of VHF frequencies, effective area of the platform may be quite small.

Given enough area in which to place the antenna elements, then the problem becomes one of finding particular places at which an element can be located. In an aircraft application, many appealing element location positions are placed off limit by the air frame designers.

Vehicle dynamics must also be taken into account in that widely spaced elements on a rapidly rotating vehicle results in signals at the elements displaying a rapid differential phase change. Such inputs are more burdensome for the adaptive processor than those from elements located more closely together.

4.1.1.4 Multiple Service Elements

In order to reduce the profusion of antenna elements on a given platform it is tempting to use a given element for multiple services. For example, JTIDS and GPS and possibly SEEK TALK might be received by a single broadband element. Such usage entails considerable performance tradeoffs and performance penalties. From a fundamental standpoint, multiple service elements in a multiple service array must satisfy coverage, required bandwidth, and grating conditions.

At the onset, coverage requirements may be difficult to achieve with multifunction elements. For example, GPS requires circular polarization largely from overhead directions while JTIDS requires vertical polarization largely for azimuthally located emitters. The fact that GPS and JTIDS are in different frequency bands means that design of the multiple service element is increased in difficulty, largely because of the increased bandwidth. Finally, even though an antenna element can be made to satisfactorily perform two different functions, for example SEEK TALK and GPS, there is considerable doubt as to whether an array of such elements will be useful at both frequencies. This is due to the fact that an array sized so as to provide reasonable performance at the lowest frequency will be characterized by an abundance of grating conditions at the higher frequency.

4.1.2 Grating Null Conditions

Basically a grating condition occurs when the relative phase of waveforms induced in a number of antenna elements is the same for different emitters even though those emitters are located at different spatial angles of arrival. Such a situation usually occurs when antenna elements are located many wavelengths apart; for example, this effect is well known in interferometry when elements are deliberately located many wavelengths apart, giving rise to a multilobed antenna pattern.

Specifically, the phasing or steering vector for an antenna array can be calculated from the relative path lengths from each of the antenna elements from the emitter. Each of these relative phases becomes an entry into the vector defined by the number of antenna elements N . Therefore, the steering vector of a desired signal s can be written

$$V_s = \sum_{i=1}^N \frac{a_i e^{j2\pi}}{N\lambda} \left[(\sin \theta_s \cos \phi_s) x_i + (\sin \theta_s \sin \phi_s) y_i + (\cos \theta_s) z_i \right]$$

In the above i is used to designate antenna elements up to N , and the quantity a_i is a unit vector designating a dimension associated with that antenna element. The terms x_i , y_i , and z_i are respectively xyz coordinates of the i th antenna element. The angles ϕ_s and θ_s are the elevation and azimuth angles of arrival for the desired signal.

From a study of antenna arrays and adaptive antenna theory it can be shown that an important determinant in establishing the grating condition is the inner product of the steering vector of one emitter with that of another. For example, the inner product of the signal steering vector with the steering vector of a jammer. This scalar quantity is denoted as γ_{SJ} .

$$\gamma_{SJ} = \mathbf{V}_S^T \mathbf{V}_J$$

It can be shown that the maximum value of γ is +1 if the steering vectors are completely aligned and -1 if they are completely misaligned. Orthogonal or uncorrelated steering vectors are characterized by $\gamma = 0$.

In the simple inteferometer example the inner product of the steering vector of an emitter arriving on an interference pattern lobe taken with that of another emitter arriving on a similar pattern lobe would be nearly one. Similarly, one signal arriving on a lobe and another signal in the minima would have an inner product of -1. In either case a high degree of correlation in the steering vectors exists: if one signal were desired and the other undesired, it would be impossible to simultaneously null one while maximizing the other; if both were desired signals, a good situation would exist in that both would be received optimally. In the second case, the situation is ideal for the reception of a desired signal and the nulling of an interferor in that the same phasing condition ensures both. However, if both signals were desired, simultaneous maximization would not be possible. Independent beam and null forming ability is obtained when $\gamma = 0$.

Figure 4-1 illustrates the grating null response for a VHF array used at L-Band. In this case a four element array spaced for good performance at VHF was assumed to be used at L-Band frequencies. Element spacings of a fraction of a wavelength at VHF become many wavelengths at L-Band. Consequently, a multitude of grating conditions exist.

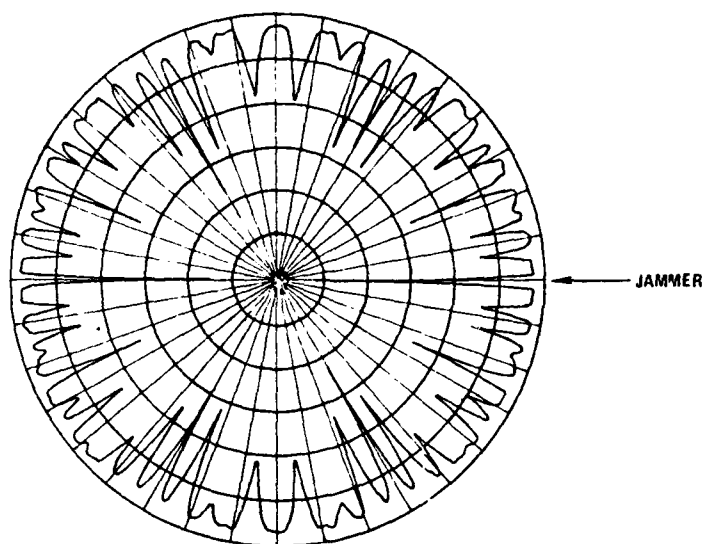


Figure 4-1. Illustration of Grating Null Response for a VHF Array Used at L-Band

The figure shows a null in the direction of an interfering jammer. While many of the additional pattern minima and pattern maxima can be independently controlled, a large number of these cannot; consequently, there are large numbers of desired signal angles of arrival for which simultaneous desired signal gain and a jammer null cannot be provided. Ordinarily, such an antenna pattern would not be particularly desirable; however, there is an exception in the case of JTIDS.

4.1.3 Array Design Solutions

In the following paragraphs, high performance, and possibly unachievable antenna array solutions are discussed.

4.1.3.1 Approaches

The obvious and relatively high performance solution to the MFBARS antenna problem is a different antenna element for each of the several functions. That is, a different element for GPS, for JTIDS, for SEEK TALK, for SINCGARS, etc. Furthermore, because phased arrays are relatively narrowband, a different array will be required for each function. Otherwise a grating lobe problem will appear.

Such a high performance solution would be characterized by very high cost; specifically, a large number of antenna elements and a large number

of element types would be required. A major portion of antenna array cost on a vehicle such as an aircraft is the cost of installation of the antenna elements and routing of the necessary cables. Practical experience has shown these costs to greatly exceed the cost of the antenna elements themselves. There is the additional effect of aerodynamic drag induced by those antenna elements which cannot be conformally mounted.

The functions for which adaptive null steering is to be realized are JTIDS, GPS, SEEK TALK, and SINGARS. A reasonably effective array design can be achieved by combining JTIDS and GPS functions (a frequency ratio range of 1.6 to 1) and by combining SEEK TALK and SINGARS (13 to 1). Significantly, the GPS-JTIDS array can be achieved as a single package; thus, its installation costs are essentially that of a single element.

While a 1.6 to 1 frequency range may be regarded as workable, considerable doubt is expressed in the case of the SEEK TALK-SINGARS array with a 13 to 1 ratio. However, because SINGARS is VHF, a fighter aircraft is not sufficiently large to permit realization of desired array dimensions. Consequently, no significant compromise beyond that which would have been necessary is anticipated.

In order not to encounter significant grating nulls for GPS, it is necessary to adjust the combined JTIDS GPS array so that somewhat closer wavelength spacing is seen for JTIDS frequencies. Additionally, somewhat wider spacing will be obtained for the GPS frequencies with an attempt made to reduce grating conditions by randomizing element locations.

Because of the lower frequency of JTIDS operations, the size of an efficient JTIDS element is somewhat larger than the size of a GPS element. A compromise is recommended in that somewhat reduced efficiency can be tolerated for the JTIDS service.

Radio transmission in each band will be accomplished from a single element. This is suggested because use of the array is made difficult by lack of precise knowledge as to the desired direction of transmission.

4.1.3.2 Element Location

Suggested antenna element locations for the JTIDS-GPS array and the SEEK TALK-SINGARS array are given in this paragraph. The GPS element

placement is largely based upon independent work done at Harris for GPS and JTIDS studies. Element locations for SEEK TALK are less rigorously determined and would benefit from a GTD (Geometric Theory of Diffraction) type analysis.

Antenna element locations for JTIDS-GPS for the F-16 aircraft are diagrammed in Figure 4-2. Two views are shown, one from above and one from the side. The basic GPS array consists of seven antenna elements and is located immediately behind the cockpit. Conformal elements are used.

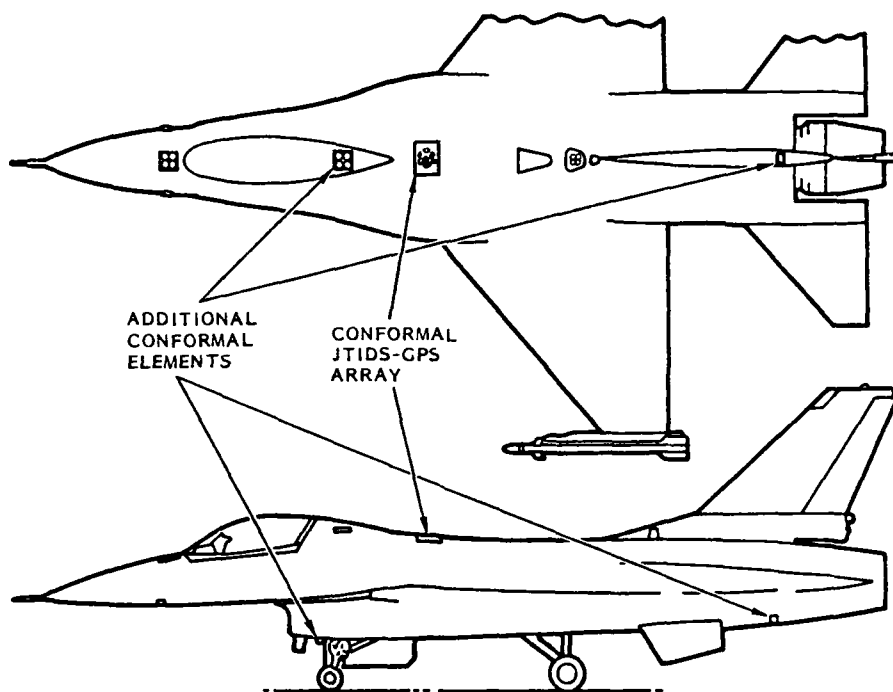


Figure 4-2. Possible Antenna Locations - JTIDS/GPS

Significantly, the multimode microstrip antenna developed by Harris for GPS has the necessary CP response above for GPS and a vertical linear response on the horizon which is required for JTIDS. To provide additional azimuthal resolution of JTIDS band emitters which may be arriving from underneath the aircraft, additional conformal elements are located on the underside of the aircraft as indicated in the lower view of Figure 4-2. All these elements will optimally be combined by the adaptive processor.

Unfortunately, the GPS conformal antenna element suggested here is not particularly efficient at JTIDS frequencies. Furthermore, the design of such an element covering the full 1.6 to 1 frequency range with high efficiency, coverage and polarization will be a difficult design problem.

A scale model showing how the conformal GPS-JTIDS array would be mounted is given in Figure 4-3. The elements are conformal and are located in an environmentally protected area. Temperatures near the cockpit are somewhat milder than those elsewhere on the airframe. Furthermore, installation volume is available at this point because a fuel tank does not completely fill the space available. A picture of the antenna elements is given in the lower right-hand portion of the photograph.

Configuration of a possible SEEK TALK-SINGARS array is shown in Figure 4-4. Five elements are used, two of which are already existing as indicated in the diagram. One additional element is placed in close proximity to the GPS-JTIDS array so as to minimize installation effort. The two remaining blades situated on the wings are shown. A wing location has the disadvantage that signals arriving from underneath the aircraft will not be well received. However, in most cases the aircraft will be communicating with other aircraft or ground stations near the horizon.

This is a relatively small array for the SINGARS function, but little improvement can be obtained unless elements are placed at the periphery of the airframe, such as at wing tips. This is electrically acceptable provided other UHF elements are located so as to destroy the grating effect at SEEK TALK frequencies.

Because the spacing of the elements used for SINGARS will be relatively small measured in wavelengths, desired signal performance will suffer when jammer nulling is required. However, the ability to form nulls is not significantly impaired. Desired signal performance is compromised because of the natural spatial period of the array; that is, the maximum angular rate at which the pattern can change from a null to a lobe is set by array physical dimensions.



Figure 4-3. Conformal Array for GPS-JTIDS

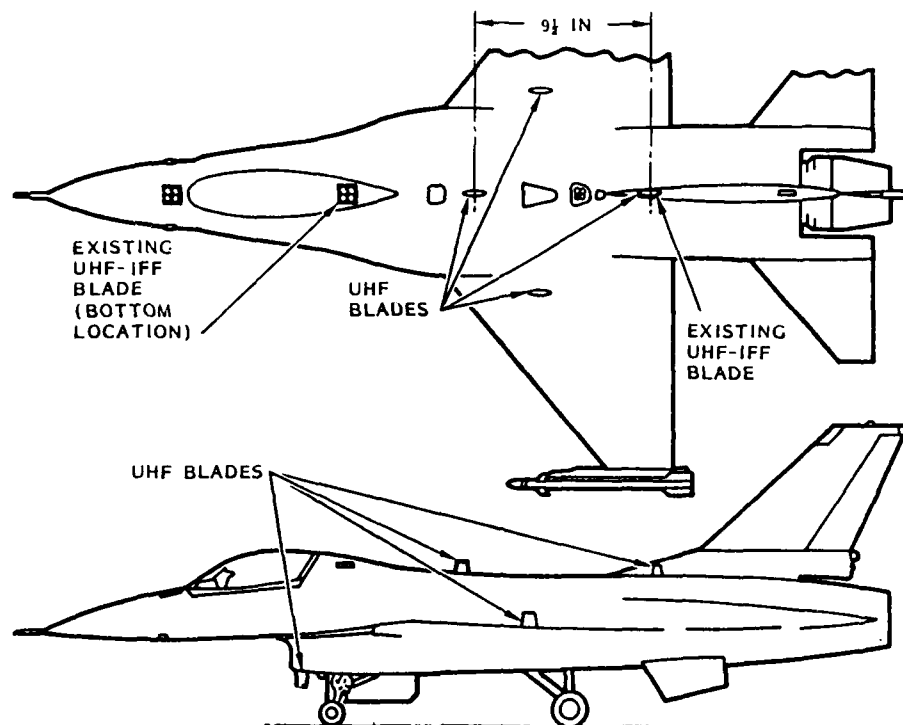


Figure 4-4. Possible SEEK TALK-SINCGARS Array

4.1.3.3 Broadband Element Design

Several approaches which may be of benefit in achieving the broadband element design required for the combined GPS-JTIDS array are discussed in this subsection.

The multiple tuning approach would, in effect, utilize a relatively complex filter circuit along with a multimode antenna having multiple taps to realize a broadband element. The physical size of this element would be roughly that of a JTIDS element or somewhat smaller if reduced gain is permitted. The size of this element is largely determined by the gain necessary at the lowest operating frequency. GPS performance for such an element would be largely unaffected while JTIDS response would be on the order of -6 dBi.

Possibly, multimode operation of an element similar to the Harris GPS design could be used in this application by driving the radiating element in an orthogonal mode. For example, elements could be fed to give CCW phase rotation for GPS and uniform phase for JTIDS. This approach also

would provide additional independent antenna ports for adaptive array use. In effect, different portions of the physical structure would be used to realize different radiating patterns.

In a third approach, the radiating element could be provided with separate feeds for different portions of the same element, in effect, diplexing the element. This approach would require frequency selective impedance matching to isolate the separate feeds. Furthermore, special designs would be required to provide the required antenna pattern at each port.

In an essentially conventional approach, elements for GPS and JTIDS could be interposed. Separate designs would be used for GPS and JTIDS but these two design would be merged into a single array, thus reducing installation costs. If such an approach is to succeed, special designs will be required in order that the larger elements do not adversely perturb the pattern of the smaller elements. Furthermore, it is not clear that a desired positioning of the elements can be achieved in that avoidance of a grating condition might require the colocation of certain elements. Hopefully, an array of smaller elements could be placed around a larger element.

It is possible to simply use the GPS element at JTIDS frequencies and accept the loss due to the smaller aperture at the lower frequency. One would expect such an approach to yield a gain of about 9 dB below isotropic for the JTIDS band.

In what is probably the most appealing approach, but yet the one that is the most technically demanding, a reduced size element such as a GPS element could be effectively operated at JTIDS frequency by instantaneous electronic tuning. Recall that JTIDS is a frequency hopping system and that although the entire bandwidth is very large, instantaneous bandwidth is relatively narrow. Using a method of electronic tuning, perhaps through the use of varactors, the standard GPS element could be tuned as a function of time to the desired JTIDS frequency. Information necessary for such tuning is already provided to the adaptive processor which requires knowledge of the JTIDS band. It is thought that such electronic tuning of the GPS element might result in a JTIDS response about 4 dB below isotropic. Considering system link margins provided to assure

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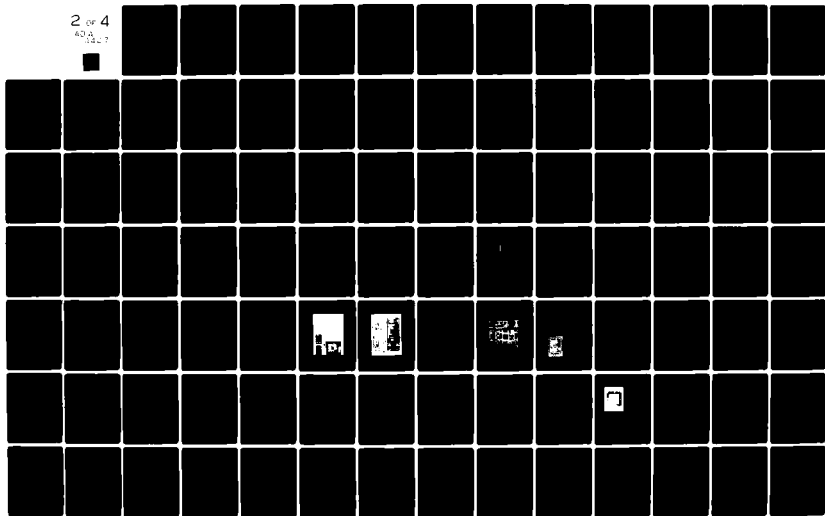
TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CA F/G 17/2.1
MULTIFUNCTION MULTIBAND AIRBORNE RADIO ARCHITECTURE STUDY.(U)
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performance against jamming, this antenna response in combination with null steering may provide satisfactory overall system performance.

4.2 ALGORITHM CONSIDERATIONS

This subsection is devoted to the adaptive algorithms considered for use in conjunction with the arrays described in subsection 4.1. We begin with a discussion of the theoretical basis of the several algorithms and follow this with consideration of the environment in which the algorithms must operate. Desired signal enhancement is treated, followed by expected and potential performance. These topics are of secondary importance relative to that of potential realization which is considered in detail in paragraph 4.2.5. Here the relative merits of analog, digital, and hybrid analog-digital realizations are discussed.

4.2.1 Theoretical Basis

A wide variety of adaptive algorithm approaches are available for our use. Those considered here are the gradient (LMS), digital search, recursive estimation, open loop, and higher order. These bases encompass very large areas of consideration.

4.2.1.1 Gradient

Gradient following techniques construct an error function, usually the difference between that which is desired and the array output, and seek to minimize this error. The gradient of the error surface with respect to the weights is measured and performance is improved by moving the weights in the direction opposite the gradient, thus reducing the error.

A variety of error performance criteria can be used, but the most common is least-mean-square. This naturally results in a minimization of the error signal's power.

Gradient algorithms are extremely versatile, have good performance, and are very well understood theoretically. Furthermore, the gradient technique can be realized in analog, digital, and analog-digital hybrid type formats.

4.2.1.2 Digital Search

The digital search approaches are best classified as analog-digital hybrids. In such an approach a processor would try arbitrary weight values

and remember those which resulted in the best performance. By successively selecting those weights which reduce the array error, one can eventually proceed to a good solution. The best known digital search technique is random search, for which a large amount of work has been done. It has been shown by G. Patrick Martin of Harris Corporation that random search as it is customarily practiced is, in fact, a normalized gradient algorithm (refer to the report for RADC contract F30602-77-C-0073).

In principal, digital search techniques could be realized in analog formats as well. However, as the name implies, these approaches are best in a digital hybrid format.

4.2.1.3 Recursive Estimation

The technique of recursive estimation can be classified as a self-orthogonalizing algorithm. It proceeds by iteratively developing the inverse of the covariance matrix. This approach requires direct samples of the several inputs as well as the matrix type operations (although a matrix inverse is not required). The task of sampling the input alone is formidable; thus, the entire algorithm would be prohibitively expensive in a MFBARS application.

Presently this approach is confined to applications wherein a relatively large and fast digital computer is available. Even then rate of adaptation is slow due to the multitude of computations required.

4.2.1.4 Open Loop

Open loop approaches have been receiving some attention lately in the literature. However, in contrast to the gradient approach, which is closed loop, extremely high precision measurements of the inputs will be required in order that effective null depths be obtained. Furthermore, extremely high quality RF/IF front ends are required unless measured compensation is made for differential response in the several channels.

4.2.1.5 Higher Order

Higher order techniques recognize that a given error function may be reduced more effectively by using knowledge of the error surface

characteristics. For example, it is known that the least-mean-square error criteria results in a parabolic error surface. Progression to the minimum error point can theoretically be made in a single step provided that the error surface is accurately estimated. This is in contrast to gradient following techniques which do not need to know the shape of the error function, only its gradient. Therefore, the gradient following techniques creep along toward the best solution in contrast to the higher order methods which, after a period of measurement and computation, go there directly.

Higher order techniques of various types can be realized in digital and analog digital hybrid formats. In some cases largely analog type circuits could benefit from this approach. Presently, it is thought that the additional complexity of these approaches more than offsets the marginal performance benefits they can provide.

Significantly, most of these five approaches could probably satisfy the MFBARS requirements. Furthermore, this list is far from complete in that other techniques could also meet the requirements. Specific selection of an algorithm will be made later in this section, but we can conclude now that the theoretical basis of the algorithm does not have a major constraining effect on the MFBARS adaptive subsystem design.

4.2.2 Environment

Design of the MFBARS adaptive processor must take into account the expected jamming threat, desired signal waveforms, and platform effects.

4.2.2.1 Threat

The jamming threats assumed here were those described independently for GPS, JTIDS, SEEK TALK and SINGARS. Important factors are the number of jammers, the relative power of these jammers and the type of jammer, such as noise, CW, pulse or deception.

4.2.2.2 Desired Signal Waveform

Significantly different performance is required for the adaptive algorithm in the case of GPS, JTIDS, SEEK TALK, and SINGARS. For example,

GPS is a direct spread system which operates in two different frequency bands: L_1 and L_2 . Additionally, signals from a number of different satellites are to be received simultaneously; in contrast, JTIDS is a TDMA type system which achieves some degree of bandwidth spreading by the method of frequency hopping. Signals are not received simultaneously and synchronization to the frequency hopping sequence is clearly required. SINGARS is also a frequency hopping system but with considerably less complexity than the JTIDS system. SEEK TALK requires reception of direct spread signals which may be simultaneously present from several desired signals (conferencing modes). The adaptive algorithm must perform in different modes for each of these functions.

4.2.2.3 Platform

Algorithm design is influenced by the platform upon which the antenna array is mounted through the mechanisms of vehicle multipath, dispersion and vehicle dynamics. Also, the existence of a grating condition can significantly slow response of the algorithm if the parameter γ is large and positive for a desired signal jammer combination.

Dispersion induced by vehicle mutual coupling limits achievable null depths unless a multiply tapped delay line type processor is used. Due to the cost and complexity of such an approach, this alternative will be avoided if possible.

Aircraft roll rates in excess of 360 deg/sec can induce a significant differential rate of change of phase in the waveforms arriving at the several antenna array elements. This rate of change phase forces the algorithm to be in a continual state of adaptation; if the algorithm does not adapt sufficiently rapidly, jammer null depth will be significantly reduced. Also, a particular problem with pulse jammers is evident when the array is rotating. Although good nulls may be formed on a pulse jammer during the period of time that pulse jammer is on, the adapted antenna pattern will rotate with the airframe; thus, the null direction is pointed away from the pulse jammer when the pulse reappears. In this case readaptation to the pulse jammer is required.

Desired signal adaptation during periods of high vehicle dynamics will not be particularly good if the desired signal is very weak compared with

the jammer since the rate of adaptation of the array toward the signal will be low. Fortunately this effect is compensated to some extent by the fact that antenna lobe responses are relatively broad as opposed to the nulls which are relatively narrow. Thus, even though a lobe may not be pointed accurately, the fact that it is slowly changing with angle means that a useful degree of gain may exist in the direction of the desired signal.

4.2.3 Desired Signal Enhancement

While enhancement of the desired signal is not always necessary, it is usually desirable. Three alternatives are considered: an a priori spatial discriminant, a priori temporal discriminant, and combined spatial/temporal discriminants.

4.2.3.1 A Priori Spatial Discriminant

By a priori spatial discriminant it is meant that the direction of arrival of a desired signal is known on an a priori basis. Such information is available from JTIDS relative navigation data or from the inertial navigation system. Provided system synchronization has been obtained, GPS provides very precise knowledge of the user's position; therefore, the desired satellite positions will be known.

Unfortunately, simple knowledge of relative directions to the desired emitters must be converted into desired signal steering vectors. That is, the relative phase of the arriving signal must be known in each of the several antenna array elements, this requires considerable computation even in the case of ideal elements, particularly if a three-dimensional array is utilized (the conformal arrays envisioned for use here will be three-dimensional). Actually, phasing based on time of flight is inadequate to obtain the necessary steering vectors in that the element-to-element electromagnetic coupling as well as the element-to-airframe coupling perturbs the phasing terms. Thus, the mutual coupling matrix must also be known and accounted for.

If the desired signals are very weak, the result of error in a desired signal steering vector is such that no significant degradation of the desired signal term will result unless a jammer closely approaches the desired signal in angle. In this case nulling failure can occur due to

the fact that the errors caused the algorithm to believe that the jammer was approaching coalignment with the desired signal when, in fact, it was not. If the desired signal strength is relatively large and errors exist in the computed steering vector, then the array will null the desired signal. This is a very powerful effect and errors as small as 0.04 degree in direction of arrival can result in 20 and 30 dB nulls for a four element array with one half wavelength uniform spacing.

Because of the necessity of large amounts of computation as well as the effect of inaccuracies induced by mutual, desired signal, a priori spatial discriminants are not easily applied. There is an important type of spatial discriminant which can be applied very simply if the desired signal is relatively weak compared with jamming and thermal noise. This is a zero steering vector or suppression type algorithm in which every emitter significantly present in the environment is nulled. Strong jammers are therefore nulled while the relatively weak desired signals are untouched. Performance of this approach is satisfactory given that the desired signal direction does not fall near that of a grating null.

4.2.3.2 A Priori Temporal Discriminant

By a priori temporal discriminant, it is meant that a feature of the system waveform is available. For example, the spreading sequence of the GPS, SEEK TALK, or JTIDS system. This can be a powerful and easily applied discriminant. It is particularly significant that this discriminant will be exactly known and available from the system modem once the modem has synchronized. Acquisition of the desired signal in the case of a very weak signal and very strong jamming may be somewhat more difficult than with the a priori spatial approaches due to the fact that modem synchronization is difficult to obtain.

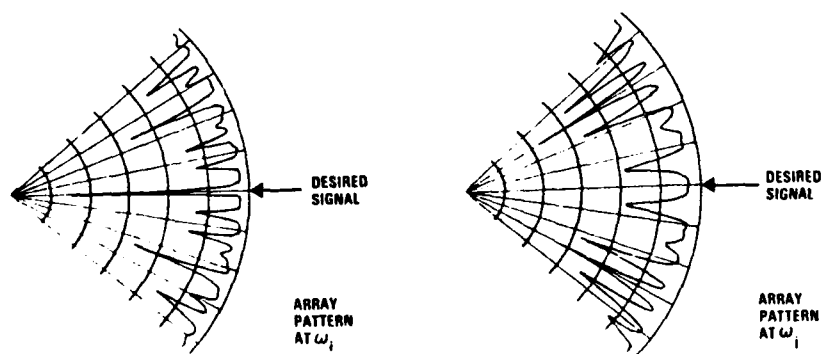
4.2.3.3 Combined Spatial/Temporal

Combined spatial/temporal approaches promise to be very powerful in that each helps to avoid weaknesses of the other. In the case of very weak desired signals and lack of modem synchronization, a priori spatial techniques can be used to point the array while jammer nulling proceeds on the basis of a suppression approach. Given strong desired signals where error in direction of arrival could lead to severe desired signal

nulling, rapid adaptation of the system to the desired signal can be achieved using temporal approaches. Such a combined spatial/temporal approach is recommended for the MFBARS system when desired signal maximization is required.

4.2.3.4 Special Effects

Grating conditions may be desirable in some applications, such may be the case for JTIDS in this application. Consider that a relatively widely spaced array is used, resulting in a very rapidly varying antenna pattern. Such a pattern is illustrated in Figure 4-5. At the upper left of this figure, the array pattern at a particular frequency, ω_i , is shown. In this case, due possibly to jammer nulls in other directions, a grating null also exists in the direction of a desired signal. Thus, for this particular frequency the desired signal is not received. When the system hops to a new frequency, grating conditions again exist but, as shown in the right-hand pattern for frequency ω_j , a grating lobe now appears roughly in the direction of the desired signal. One might expect on a probability basis that response at half of the frequencies might be poor while response for the remainder of the frequencies might be good. On an average basis, this might lead to very good system performance. Additional statistical type analysis is required to resolve this point.



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Figure 4-5. Illustrations of Possible Grating Effects on JTIDS Desired Signals

4.2.4 Potential Performance

Algorithm selection must take into account achievable signal-to-noise ratio improvement under static and dynamic conditions. Thus, basic null depth as well as adaptation speed are important factors.

4.2.4.1 Achievable S/N Improvement

Signal-to-noise ratio improvement is governed by null depth obtainable on the jammers as well as desired signal gain. Algorithm and circuit imperfections largely establish null depth. For example, 0.05 dB amplitude and 0.95 degree rms phase will limit null performance to about 35 dB. Furthermore, very fast adapting algorithms with a high degree of weight jitter will have reduced null depth compared with slower adapting algorithms due to the fact that weight jitter is always perturbing the weights away from their optimum solution. Similarly, perturbational type digital algorithms or hybrid analog/digital algorithms also continually displace weights away from their optimum solutions, thus reducing achievable null depth. Nevertheless, perturbational type algorithms, in spite of their reduced null depth capabilities, are attractive candidates due to their usually adequate performance and low overall system cost.

4.2.4.2 Adaptation Speed

Rate of adaptation of the algorithm to the interfering signals and desired signals is very important in two cases: first, when the platform upon which the array is mounted is subjected to relatively high rates of angular motion such as the roll of an aircraft and, second, when used in a TDMA or frequency hopping system with small or no weight memory. In such applications it is necessary that the algorithm be capable of adapting rapidly to any externally induced changes. Otherwise, signal-to-noise ratios predicted by optimum calculations will not be realized and the array will be in a continual state of adaptation.

4.2.5 Potential Realizations

Probably the single most important consideration for the MFBARS application is the manner in which the adaptive algorithm is realized. Practically every important parameter is affected by the realization,

including null depths, adaptation speed, size, weight, power, and especially cost. The following paragraphs briefly review analog, digital, and hybrid analog/digital approaches from a relative cost/performance standpoint. Following this review a selection of realization for MFBARS is made.

4.2.5.1 Analog

A basic block diagram of analog, digital and hybrid analog/digital approaches is shown in Figure 4-6. The analog approach is shown to the left. A customary LMS type approach is illustrated. At the top of the figure an antenna element with voltage output $x_i(t)$ provides signals to a weighting device, then to a correlator. All the weighted signals are summed, providing the array output as indicated. If a temporal reference type algorithm is used, a desired reference function is subtracted from the array output, thereby forming the array error. This error is then correlated with the individual inputs, forming the gradient of the error surface. This gradient is integrated, thus, producing the algorithm weight.

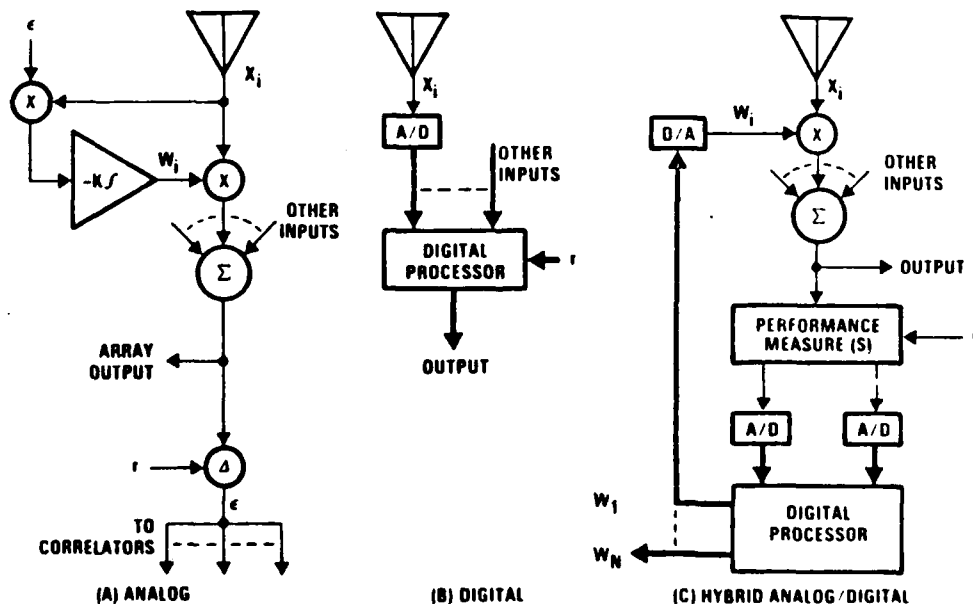


Figure 4-6. Adaptive Array Circuit Diagrams

The digital approach is shown in Figure 4-6, Part B. The voltage output of the antenna array elements are converted from analog to a digital format and are processed by a digital computer. This digital processor may also use a reference input in achieving its output function. The digital processor can generally accomplish any of the various algorithms. It would do this numerically, however, in contrast to the analog approach which would use analog weights, correlators, integrators, etc.

Figure 4-6, Part C shows a hybrid analog digital technique. The antenna input, the weighting device, and array combiner are the same as those used in the analog approach. These form the analog portion of the hybrid technique. Array output may or may not go directly to performance measure devices where the reference function R can be input. Either before or after the performance measure, an analog-to-digital conversion is performed and the digital results are provided to a digital processor. This processor then executes several of a number of acceptable algorithms, resulting in calculation of the several weight values. These digital quantities are delivered to a digital-to-analog converter, the output of which controls the analog weight.

At first glance the hybrid analog/digital approach seems the most complex of the three shown. In fact, however, the simple analog approach is quite unworkable as it is shown due largely to the fact that very weak signals arrive at the antenna input. Thus, amplification and, importantly, bandlimiting to the desired signal bandwidth must be accomplished before the correlation function is realized. Otherwise, the algorithm would concern itself with out-of-band interferers and the number of degrees of freedom would be quickly exhausted. What is required is, in effect, a receiver in each of the antenna inputs complete with amplifiers, LOs, and bandpass filters. A detailed block diagram of a typical analog adaptive null steering array is shown in Figure 4-7. Signals from each antenna input are sent from a preselection filter to a local oscillator which frequency converts those signals to an intermediate frequency. If amplification, bandpass filtering and amplification all follow before the signal is divided for correlation and weighting. This is a very complex and expensive portion of the analog approach.

The analog processor advantages and disadvantages may be summarized as follows. First, very fast adaptation is possible. Correlation and integration processes occur in parallel because a correlator and integrator is present for each weight. Such an approach is characterized by very low cross-correlation noise and, consequently, very low weight jitter. Thus, the solutions obtained are very good in their null depth and null stability. Finally, the approach is theoretically understood.

The fact that individual receivers are required for each antenna input means that this approach will be characterized by relatively high cost. Additionally, because of the inflexibility of analog designs once they are achieved, this approach is not particularly versatile. For example, it is difficult to provide weight memory (useful for frequency hop) or to change modes (i.e., suppression to S/N maximization).

4.2.5.2 Digital

A more detailed block diagram of the all digital adaptive processor is shown in Figure 4-8. Because analog waveforms are being transmitted, a portion of the processor must, in fact, be analog. As shown in the figure, voltages from the antenna array elements are preselect filtered, applied to a low noise amplifier, frequency converted, post select filtered, IF amplified, and then delivered to an analog-to-digital converter. Although this is the customary approach, it is noted that as technology improves, some filtering can be done in the digital processor at the expense of increased processor work load. At present, preselect and post select filtering is much more easily accomplished in analog format than within the digital processor. In principle, the digital processor can achieve all weighting, summing, filtering, and despreading operations, if desired.

Relative advantages and disadvantages of the digital processor can be summarized as follows. First, the digital approach is characterized by having the utmost flexibility. Almost any algorithm with practically any special constraints can be realized. Furthermore, this approach is suitable for VLSI. Potentially fast adaptation can be achieved in the future, given that higher order algorithms or recursive estimation type algorithms are used in lieu of the gradient following techniques.

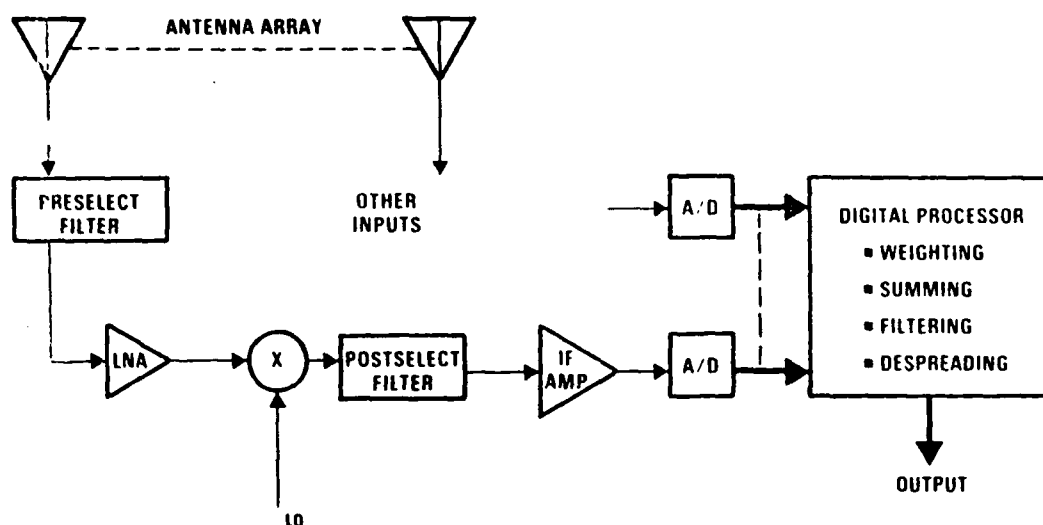


Figure 4-8. All Digital Adaptive Processor

Disadvantages, at present, are that insufficient digital processing capabilities exist for more complicated algorithms at the speeds required for practical system problems. Such technology appears to be at least a decade away. Furthermore, the present need for a complete receiver or a large portion of a receiver in each antenna input means that the high cost of the analog approach will also be present in the digital approach, at least for the foreseeable future. Due to computation rate limitations of practical digital computers in the near and medium term future, significant performance limitations will be encountered in that only the simpler algorithms can be realized at the speeds required for MFBARS application.

While we must reluctantly conclude that the all digital approach is not practical at present, it is likely to be the method of choice by the year 2000.

4.2.5.3 Hybrid Analog/Digital

A more detailed block diagram of the hybrid analog/digital approach is given in Figure 4-9. Signals from the several antenna array elements are delivered to low loss RF weights. Then, the weighted signals are combined, thus producing the array output. In a practical system, a receiver of customary design is used at the array outputs to amplify and band limit

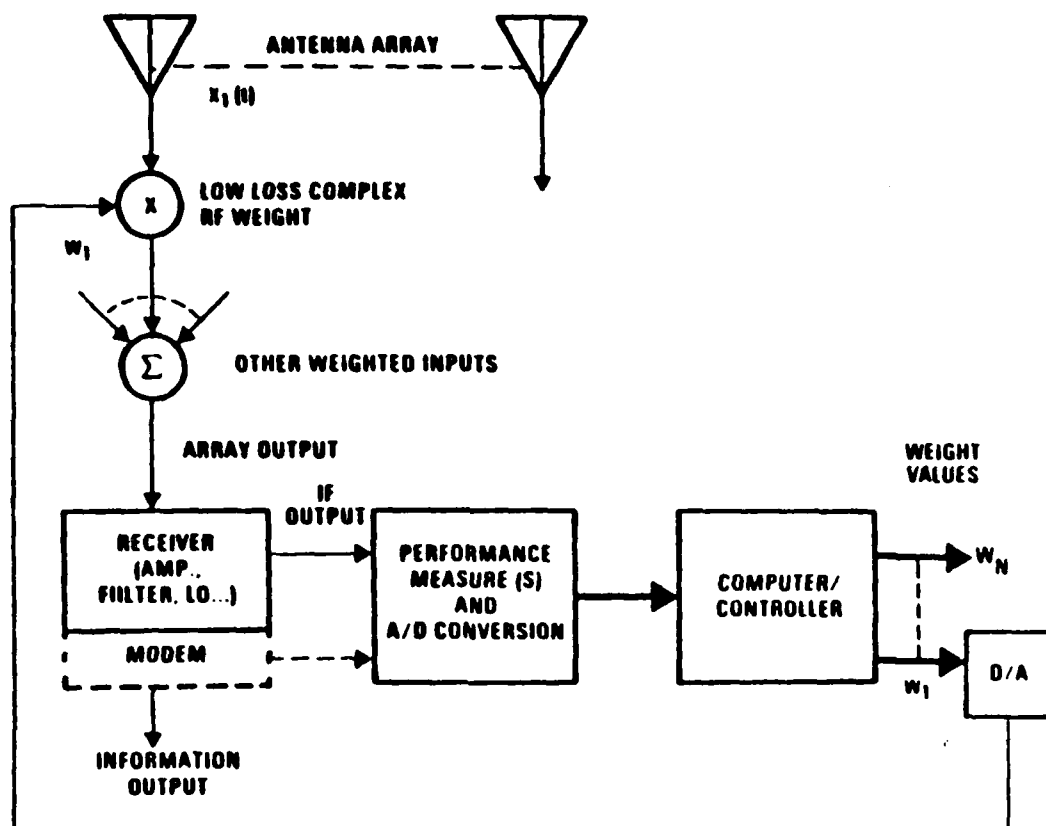


Figure 4-9. Hybrid Analog/Digital Adaptive Array Circuit

the desired signals. In fact, if the receiver design is an existing one, the receiver RF input, which would have been connected to a single antenna in the customary approach, is simply connected to the array output. After amplification and band limiting, signals from an intermediate frequency output of the receiver are delivered to performance measure and/or analog-to-digital conversion devices. The digital signals then go to a computer/controller which executes the algorithm and obtains the weight values. Application of these weight values then completes the algorithm loop.

The remarkable synergism of this approach is evident through study of Figure 4-9. The customary receiver design lacks provision for adaptive null steering. Simultaneously, the adaptive processor requires gain and band limiting of desired signals — functions provided very well by the receiver. It is also significant that the actual hardware required in the

hybrid analog/digital approach is not much more complex than that shown in the figure. This is in contrast to the analog and the digital approaches discussed earlier.

A hardware diagram of the hybrid analog/digital approach is shown in Figure 4-10. Signals obtained from an antenna array are routed to a weighting and combining box, the output of which is delivered to the usual antenna input of a radio set. If adaptive null steering were not required, this antenna input would be directly connected to an antenna element. Signals from the IF output of the radio set, having been amplified and band limited, are delivered to a digital processor which executes the algorithm and obtains weight values. These values are sent to the weighting and combining box. IF signals may optionally be delivered to an auxiliary modem. This modem may also provide a discriminant function for desired signal-to-noise ratio maximization.

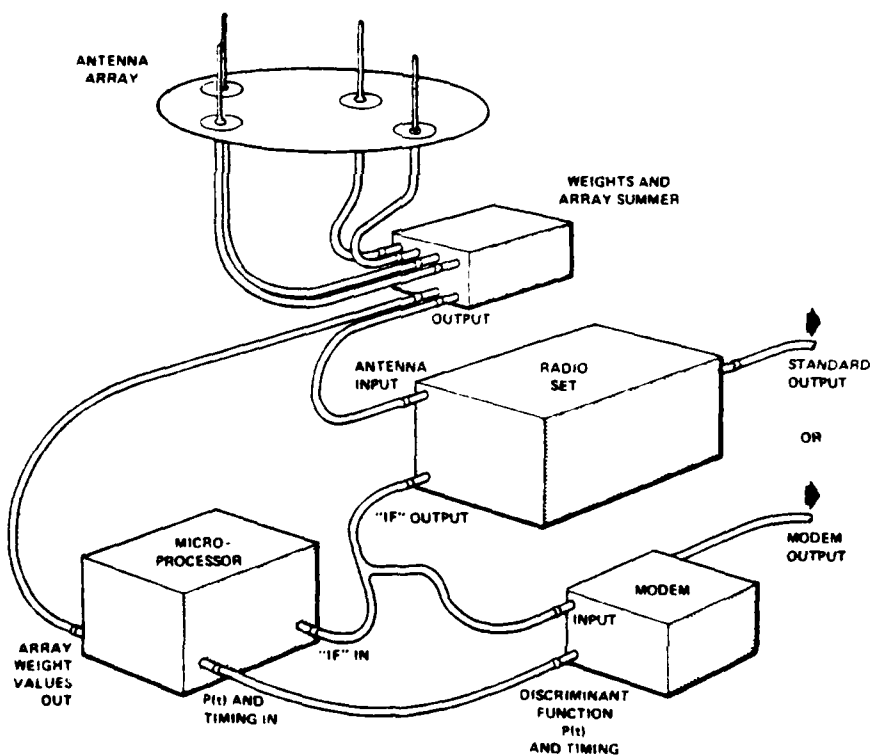


Figure 4-10. Hybrid Analog/Digital Adaptive Array Hardware Diagram

Thus, an existing radio set may be given an adaptive null steering capability simply by the addition of additional antenna elements, a weighting/combining circuit, and a digital microprocessor controller.

A somewhat more detailed block diagram of the analog portion of this approach is shown in Figure 4-11. Again, the antenna element weighting device and array summer are shown at the top of the diagram. Receiver LNAs, LOs, and filtering devices are shown within the dotted enclosure, including the possibility of spread spectrum despread operations. In some cases, such as the GPS application, it is not desirable to extract performance measures from the ultimate system narrowband. This is because the bandwidth of the receiver determines the rate at which the adaptive processor can adjust. To meet adaptation requirements imposed by platform dynamics, nulling must proceed as a rate compatible with a 25 to 50 kHz wide intermediate frequency bandwidth. Consequently, total power detection may take place at a portion of the IF circuitry prior to the final bandwidth reduction. Desired signal terms can be taken from more heavily filtered portions of the receiver.

The primary advantage of this approach is that it is highly synergistic. The adaptive processor provides a null steering antijam capability for the radio receiver while the radio receiver provides amplification and band limiting required by the adaptive processor. Consequently, this is a relatively low cost approach. Separate receivers are not required in each of the antenna inputs, thus reducing size, weight, power, and cost. The approach is relatively versatile in that a number of different algorithms can be run by the digital processor – significantly more than the all analog processor, but somewhat less than the all digital processor.

Significant disadvantages of this approach are imposed by the need for continual weight perturbations and by the bandwidth of the radio receiver. To sense the necessary direction in which to adapt (the gradient) a systematic method of weight perturbation is required. Such weight perturbation ensures that the weights will always be disturbed evenly at an optimum solution. Thus, null depths are not as good as with the analog approach. Furthermore, adaptation of the individual weights must be

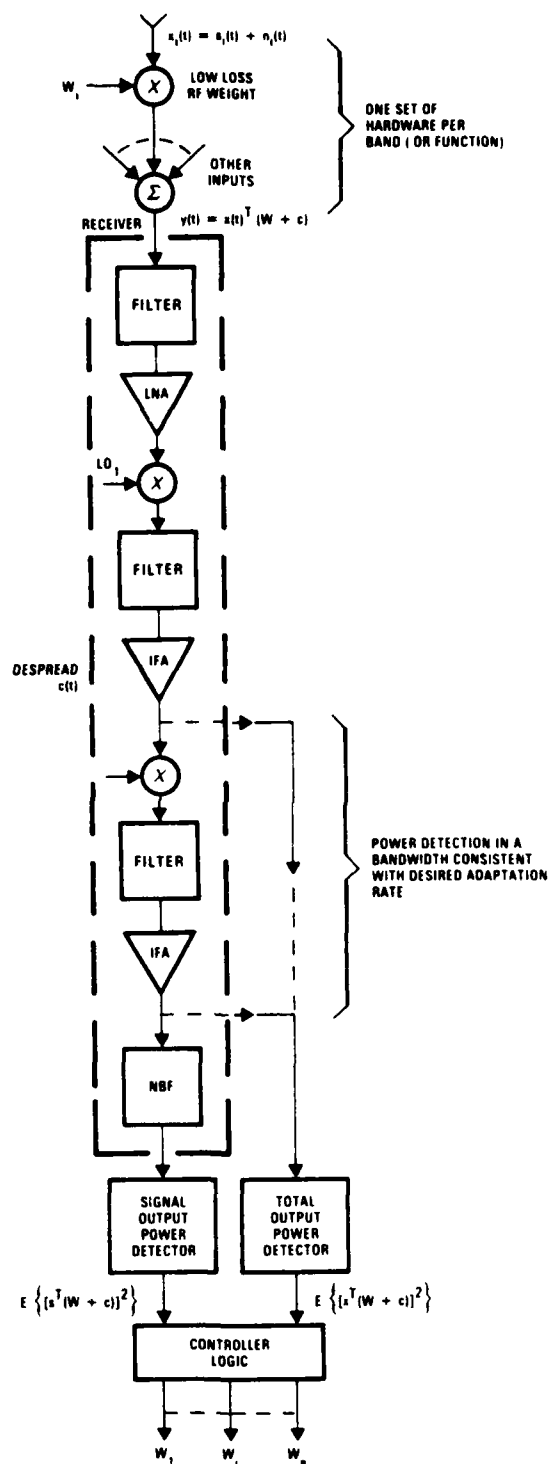


Figure 4-11. Alternative Methods of Performance Measure Generation

achieved in a serial rather than in a parallel fashion because the necessary gradient information must pass through the radio set. Non-interference of this information requires, in effect, serial transmission of such data (Harris Corporation prefers a code division multiplex technique having the same data rate). Summarizing, the algorithm is not as fast as in the analog approach, nor is the quality of null depth as good. In spite of this, the approach can be surprisingly fast and null depths limited by dispersion are often the case rather than null depths limited by weight perturbation.

4.2.5.4 Selections Made

On the basis of the discussion presented, the hybrid analog/digital processor is chosen. The principal reasons for this choice are the hardware savings, the acceptable algorithm performance achievable, and the fact that most algorithm type options are retained.

4.2.5.5 Implied Needs

While realization of an effective hybrid analog/digital controller can be achieved with present technology, there is a critical component which is a major contributor to overall system cost and lackluster performance. This is the RF weight. It is strongly recommended that an advanced low loss RF weight be designed and developed for the MFBARS application. Present day weights, although having very high quality from a dispersion viewpoint, have significant losses. For example, a minimum insertion loss of 10 to 12 dB is typical. Such a loss implies relatively large amounts of high quality, low noise amplification in order that the system noise figure be preserved. Due to the tendency of low noise amplifiers to saturate and produce intermodulation, such amplification is difficult to achieve, particularly in the presence of large amounts of jamming. Additionally, weighting devices broadband enough to be used at any of the several system frequencies would be desirable.

A further implied need is close cooperation in designing the radio and adaptive circuits. The fact that circuits are extensively shared by these processors means that, unless a high degree of cooperation exists among designers, problems will develop.

4.2.6 Example Algorithm Candidates

Algorithm candidates which are particularly useful in the MFBARS application and in the hybrid analog/digital format are given brief consideration in this subsection. Specific attention is given to the generalized positive signal feedback (PSF) algorithm, pattern search and random search.

4.2.6.1 Generalized PSF

The positive signal feedback algorithm is an explicit gradient type algorithm capable of achieving true signal-to-noise ratio maximization. Furthermore, if the desired signal steering term is absent, this algorithm achieves a suppression or sidelobe cancellor type function. Alternatively, a direction of arrival steering vector can be inserted for either single or multiple simultaneously desired signals. The PSF algorithm has been realized at Harris Corporation in both analog and digital formats. A thorough description of the technique is given in the report for Contract F30602-77-C-0073. This algorithm is very similar in part to Widrow's LMS algorithm; significant differences occur in formation and application of the desired signal reference function.

4.2.6.2 Pattern Search

The pattern search approach is a digital search technique which exploits the error function surface in weight space. It can be classified as an implicit gradient approach since explicit gradient calculations such as those found in the LMS and PSF algorithms never appear. Nevertheless, implicit use of gradient terms is an important part of the algorithm's operation. This technique is capable of providing effective suppression and sidelobe cancelling type performance. It can also work with direction of arrival constraints, provided they are applied at the weight level. Unfortunately, the algorithm is characterized by relatively slow signal-to-noise ratio maximization. This limitation is caused primarily by the fact that movement from one weight solution to the next can occur no faster than estimates of the performance measure. Typically, array output signal-to-noise ratio's can be made with the necessary precision.

4.2.6.3 Random Search

Random search is another implicit gradient algorithm, a fact which was unknown until recently. It is capable of very effective suppression type algorithms and can also work well with direction of arrival constraints, as in pattern search, provided that they are applied at the weight level. Similarly, random search is slow to achieve signal-to-noise ratio maximization because of the need for the performance measure to be accurately established. Given that the signal-to-noise ratio is poor, large amounts of filtering are required with subsequent time delay. Thus, the rate at which the algorithm can progress from one step to the next is limited by the high amount of filtering required.

4.2.6.4 Selections

Because adaptation requirements differ for GPS, JTIDS, SEEK TALK, and SINGARS, the algorithm of choice may be different as well. Since all of the algorithms mentioned work very well with the hybrid analog/digital processor, selection can be made on the basis of achievable performance.

GPS. Desirable adaptive modes for GPS include signal-to-noise ratio maximization, particularly for several desired signals, suppression, and protected angular space.

JTIDS. JTIDS can be adequately protected by a suppression algorithm incorporating a weight memory and recall technique. Consider for a moment how a basic gradient following algorithm can be modified for a frequency hopping application. The bandwidth of the frequency hopping system is often much greater than that effectively treatable by a narrowband adaptive processor. Furthermore, because of the TDMA nature of the hopping transmissions, a conventional array design would be in a continual state of adjustment as it hopped to the various bands. For example, some bands might have jamming and others not.

Figure 4-12 shows an effective method of modification of a basic gradient type algorithm suitable for frequency hopping. The usual antenna element, weighting device, and array summer are shown to the right of the diagram while the usual correlator and integrator are to the left. The

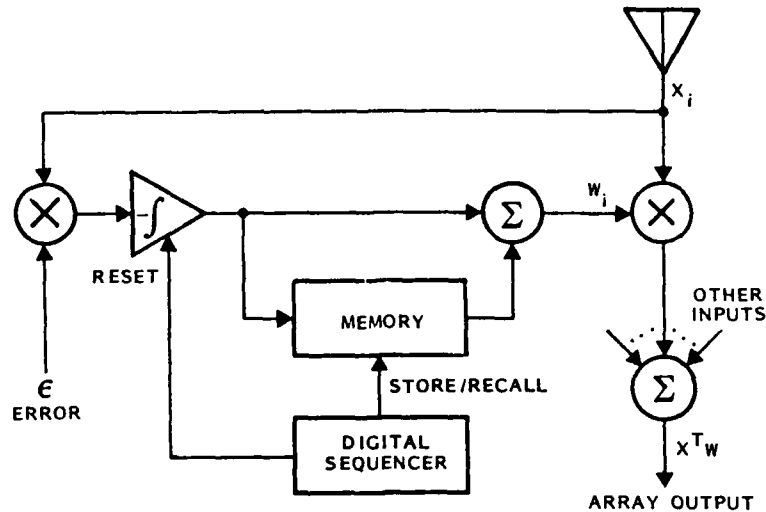


Figure 4-12. Weight Storage/Recall for TDMA, F-HOP

integrator output, which is the weight value in the usual algorithm, is sampled and stored in a memory making this information available for recall at a later time. A recalled weight value is sent to a summing device where it is combined with the instantaneous output. A digital sequencer controls flow of weight values into and out of the memory. This sequencer is controlled by a more fundamental digital processor in synchronism with the frequency hopping system; the integrator is reset following each weight recall cycle.

Suppose the system is followed from instant of turn-on through a few cycles. Initially, the system is unadapted in any of the several frequency bands. After hopping to the first frequency band, the circuit begins to adapt and has achieved some degree of nulling performance at the end of that particular interval. The weight associated with this adaptation is then transferred to memory, and hopping proceeds to the next frequency band. Again adaptation occurs and the best weight value, the one obtained at the end of that interval, is sent to the memory. When a particular frequency band is subsequently revisited, the weight value from the previous adaptation is recalled and summed with the integrator output. Because the integrator is reset at the beginning of each frequency hop, the system begins adapting where it previously left off. At the end of the interval,

the old weight value is summed with the new integrator output and this quantity is stored. In such a manner, the integrator adapts only to satisfy changes in a given frequency band from one visit to the next.

Although it is not shown in Figure 4-12, desired signal steering vectors can be remembered in a similar fashion, providing for complete pattern control both as a function of frequency and desired emitting. However, it is suggested that one use the grating null effect if simulation indicates that it is an effective approach. Signal-to-noise ratio maximization is not required for JTIDS and, furthermore, it is probably not desirable. This is because most desired signals which are received infrequently may require totally different weight solutions, thus, weight memory may be ineffective in these cases. The very large number of possible desired signals call for very large amounts of weight memory. Additional consideration is required for the JTIDS system, especially during acquisition.

SEEK TALK. Due to the fact that relatively strong desired signals can be present, SEEK TALK definitely requires signal-to-noise ratio maximization to prevent desired signal nulling. Furthermore, relatively fast adaptation is required as well. An algorithm capable of treating multiple simultaneous desired signals such as the PSF is recommended.

SINGARS. A suppression algorithm is adequate for SINGARS. As with JTIDS, an algorithm incorporating weight memory is recommended to accommodate frequency hopping over very broad bands. Because array element separation is very small when measured in wavelengths, grating conditions in the SINGARS application are not expected to be helpful as with JTIDS. Consequently, desired signal gain will largely be determined by separation in angular space of the desired signal from the jammers. In other words, the desired signal will practically always be on the slopes of the null formed on the jammer. For this reason, signal-to-noise ratio maximization would be only marginally useful.

4.2.7 Conclusions

It is noted that the generalized PSF algorithm is capable of solving all of the algorithm requirements. However, a detailed analysis is required to determine if a particular algorithm might be more cost effective for a particular application. Given the flexible array configuration,

it will be possible to use a given antenna array for different MFBARS functions. In such case, the adaptive processor should be capable of achieving any of the several functions — for example, GPS, JTIDS, SEEK TALK, or SINCGARS. As a result, the generalized PSF algorithm would be chosen since it is the only approach capable of meeting all requirements.

4.2.8 Major Digital Processor Needs

A summary of major digital processor performance requirements is given in Table 4-1. This digital processor executes the adaptive algorithm. The worst case processing rate is determined by JTIDS frequency hopping. Operations required here are calculation of the gradient as well as storage and recall of weight values. It is estimated that roughly 25 million operations per second will be required. Importantly, this computation assumes that no GPS direction of arrival information is required. Although computation requirements for determining desired signal steering vectors have not been accurately estimated, the need to account for three-dimensional element locations as well as for element mutual coupling will likely result in a digital processor rate exceeding that for the worst case JTIDS.

Approximately 8K bits of RAM memory are required for storage of weights associated with a particular JTIDS band of frequencies. ROM memory requirements of approximately 4K Bytes support algorithm instructions. Eight analog-to-digital converters are required, each having 8-bit capability with one million samples per second. Conversion of the digital weight values to the analog quantity necessary to control the weights will necessitate 42 8-bit D/A converters.

It is recommended that at least four processors be provided along with four arrays. The configuration and allocation of this array resource is discussed in subsection 4.3.

Alternatively, one may realize the adaptive processor with dedicated digital logic. Such a circuit would require numerous 8-bit high-speed add-and-multiply integrated circuits. The block diagram of this approach is shown in Figure 4-13. At the right-hand portion of the figure, the usual antenna, RF amplifier, weighter, and array summer path are shown. Output of the array is delivered to the radio as is usually the case in

Table 4-1. Major Digital Processor Needs

Processing Rate for Worst Case JTIDS (No GPS DOA)
25 x 10 ⁶ Operations/Sec
Memory
RAM 8 K Bits (JTIDS)
ROM 4 K Bytes
Total Processor Major Components
4 - TRW Processor Circuits
16 K Bits - RAM
16 K Bytes - ROM
8 Eight-Bit, 10 ⁶ Samples/Sec A/D
42 - 8 Bit D/A
Alternative Requirements
Slower Processor
Many Dedicated 8-Bit High-Speed Add and Multiply

the hybrid approach. IF output of this radio goes to power detectors, modems, and signal recognizers from which performance measurements are extracted in an analog fashion. These analog outputs are converted via 8-bit A/D converters to a digital format, and are multiplied by an algorithm gain factor obtained from a somewhat slower master computer located elsewhere. These digital quantities are delivered to digital correlators, PX and PS, which are shown at the upper left-hand portion of the figure. Correlation consists of an exclusive/or operation of the performance measure with a weight perturbation sequence suitably delayed to accommodate the delay in the receiver, power detectors, etc. The input perturbation is applied in the path shown at the upper center portion of the diagram. After correlation, desired signal steering terms are added to the total gradient terms via a high-speed adder, and are then delivered to a second high-speed adder that functions as an integrator (by connection of an adder output to one of the adder inputs). This approximation to inte-

gration provides the algorithm weight value which is converted from digital-to-analog format and applied to the weight. Note that the weight perturbations are added to the weight immediately prior to application.

Observe that most of the devices in this circuit are shown as being under the control of a master computer which could be the computer associated with the MFBARS radio. This computer adjusts algorithm gains, configuration of the algorithm, initialization, etc.

4.3 CONFIGURATION

This subsection discussed the arrangement of the antenna array, weighting devices, array combiners, adaptive processors, and the radio. It is apparent that a number of arrangements of these components is possible. For example, the adaptive processor, antenna combiner, and weighting devices could be colocated with the radio receiver. This arrangement would have the advantage of minimizing the need of data transmission between the radio and the adaptive processor. Other arrangements also have important attributes or disadvantages. Such considerations are the subject of this subsection.

The selected arrangement of the various hardware components is described, giving only brief consideration to those approaches which were not selected. Paragraph 4.3.2 includes a discussion of the various interfaces required among the several component blocks.

4.3.1 Selected Arrangement

A block diagram of the selected segregation of MFBARS components is presented in Figure 4-14. Observe that there are three basic functional blocks: (1) the antenna array elements, (2) the adaptive processors, and (3) the radio. For reasons given in the following three subsections, these elements will be physically distinct.

4.3.1.1 Separate Adaptive Processor/Radio

Colocation of the adaptive processor with the radio minimizes the need to transmit performance data from the radio to the adaptive processor and optimally combined RF signals from the adaptive processor to the radio. Furthermore, colocation might permit the digital computer

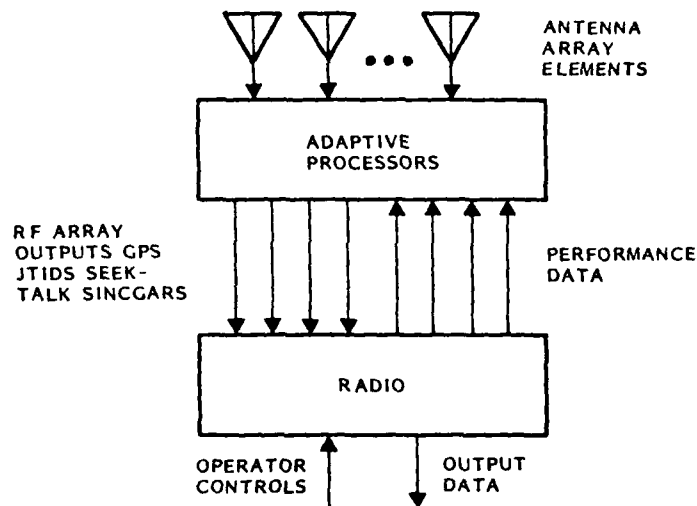


Figure 4-14. Segregation of MFBARs Components

necessary for the radio function to assist with the adaptive processing task. However, these advantages are offset by those gained by separation of the adaptive processor and radio.

First, modular building blocks such as a radio and an adaptive processor permit the use of the radio alone in those applications requiring no adaptive null steering. Because RF signals for the radio are obtained directly from an antenna element instead of the adaptive processor RF combiner, a very clean break is provided. No significant cost penalty is paid by radio users which do not need the adaptive options.

Additionally, the modular arrangement facilitates maintenance. A malfunctioning radio or adaptive processor can be individually serviced, possibly by replacement of the entire module.

Total cable requirements are reduced by this approach. If the adaptive processor and radio were colocated, cables from each of the numerous antennas would have to be run to the radio location. With the modular approach, the adaptive processor can be centrally located with respect to antenna elements. Reduction of total cable requirements reduces possible RFI and, of course, installation cost and weight.

Mechanical conformance with the airframe is also facilitated. It is often difficult to find sufficient space to locate a single bulky item.

However, there are usually somewhat smaller places within an airframe where packages can be located. In the case of the F16, the adaptive processor can be conveniently located behind the cockpit over a fuel storage area as shown in Figure 4-15. In this location the adaptive processor is close to the GPS-JTIDS elements, those most sensitive to RF losses. Optimally, combined RF signals are delivered through a single cable run to the radio located somewhat nearer the aircraft cockpit.

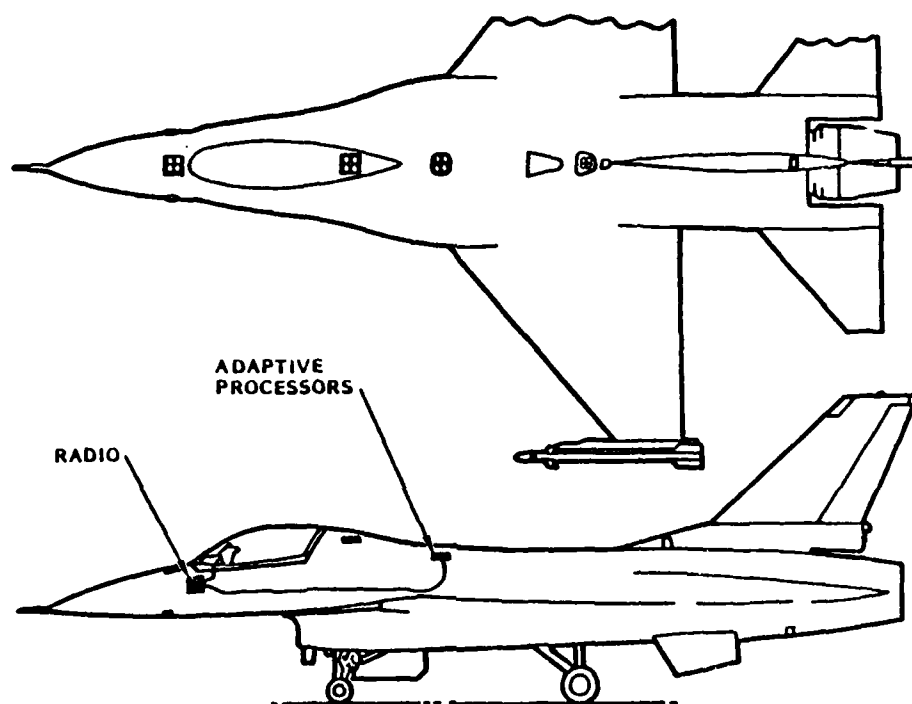


Figure 4-15. Selected Locations of Major Adaptive Processor Components

A disadvantage of this separate adaptive processor and radio approach is that adaptive processor performance data, which is necessarily obtained from the radio intermediate frequency output, needs to be sent from the radio to the adaptive processor. These data rates are relatively high, in the order of 10 Mbps.

4.3.1.2 Combined Weights-Summer-Digital Controller

Earlier, in paragraph 4.2.5, a block diagram of the hybrid analog/digital adaptive approach was given in Figure 4-10. The RF weighter-combiner was shown separately from the adaptive processor digital controller. While this approach permits the RF weighter-combiner to be located much closer to the antenna elements, a significant disadvantage of this approach is that weight update and weight perturbation values must be transmitted from the adaptive processor to the weighter-combiner. In the case of JTIDS frequency hop, for the number of antenna elements recommended, a total data rate of approximately 100 Mbps would be required. While not impossible, this is a moderately difficult problem. Consequently, it was decided that the RF weighter-combiner will be colocated with the digital controller.

4.3.1.3 Separate Antenna/Processor

In order to minimize RF losses between the antenna elements and the weighter-combiner, it is desirable to have the weighter-combiner located as close as possible to the antenna elements. There are two problems associated with closely locating the antenna array and weighter. First, the antenna elements are widely dispersed physically, particularly those elements for the lower frequencies. Secondly, heat and vibration can be a significant problem in certain locations on the aircraft. Skin temperatures, for example, can exceed hundreds of degrees. Such an environment is hostile to the active circuits required for the adaptive processor. For this reason, an environmentally moderate location such as the one chosen is required.

A simple approach using four separate adaptive processors for increased reliability is shown in Figure 4-16. At the top of the figure, two antenna arrays are shown, one a VHF/UHF array and the second an L-band array. After signals from the antenna elements are low noise amplified, they are diplexed into bands. Examples of JTIDS and GPS are shown in the right-hand portion of the figure. After diplexing, signals are adaptively weighted and combined, providing optimized RF outputs. A disadvantage of this approach is that, while it uses multifunction antenna elements, the adaptive processors are necessarily single function due to the presence of the diplexer ahead of the adaptive weighting function.

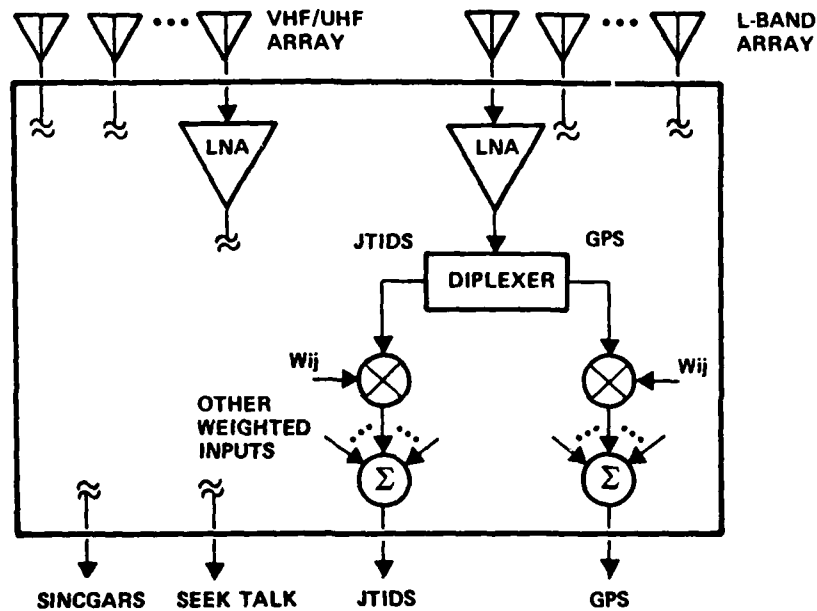


Figure 4-16. Adaptive Processor RF Circuitry

A much more versatile approach is shown in Figure 4-17. In addition to increased versatility, reliability of this second approach is enhanced because, if one of the adaptive processors should fail, the remaining three processors can continue operating on the three highest priority signals. Observe that after low noise amplification, signals are simply power divided and directed to the weighting and combining networks. Output of these combining networks is then diplexed (the best location for the diplexers is probably in the receiver) into the several frequency bands, e.g., JTIDS and GPS. If useful response of the VHF element is obtained in the L-band frequency range, additional diplexers could be provided for the remaining adaptive processors.

A significant advantage of this increased versatility approach is that, during GPS acquisition and from time to time, it might be desirable for both L_1 and L_2 signals to be independently adaptively processed. Additionally, acquisition of the JTIDS system is facilitated by simultaneous searches in different frequency bands, a process made more effective by having several independent adaptive processors. Note, however, that four separate arrays are not necessarily required for useful JTIDS acquisition — in spite of the fact that four separate frequency or time slots will be examined by the

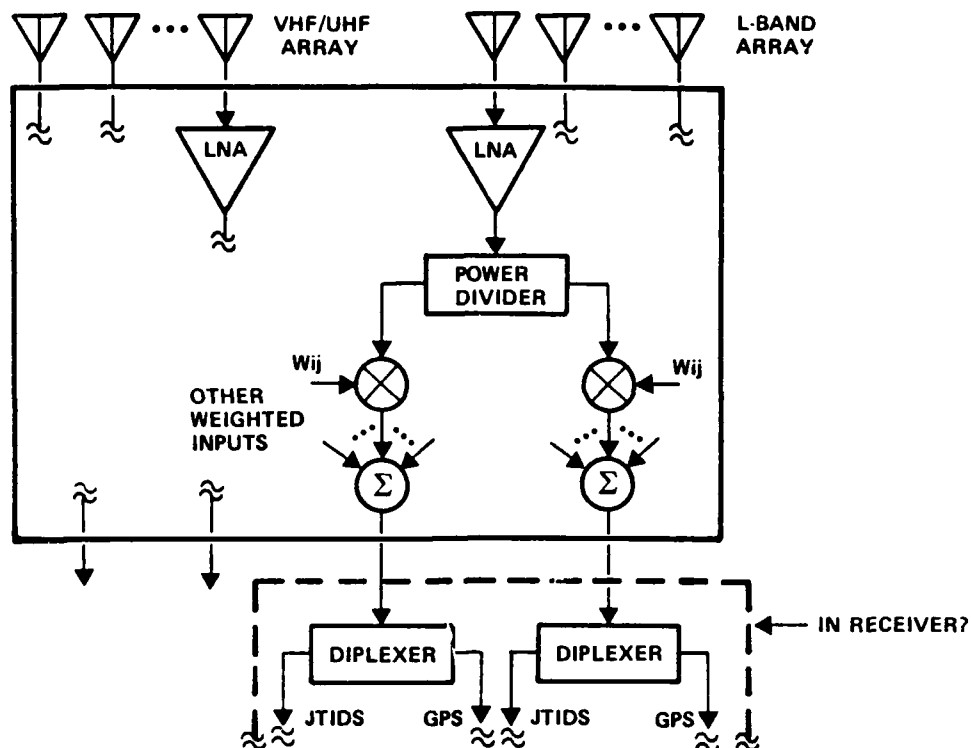


Figure 4-17. Increased Versatility RF Processor Circuitry

radio. Such acquisition could be accommodated with some performance degradation by permitting the adaptive processor to adapt simultaneously to the entire JTIDS band of frequencies rather than to specific bands in synchronization with a hopping procedure.

Although not shown in Figure 4-17, the increased versatility approach can be extended to allow all four adaptive processors to work independently on any given desired signal, even though the antenna elements themselves may not respond to that particular frequency band. This approach would require the incorporation of both power division and frequency diplexing prior to the adaptive weighting and summing operations. A future detailed analysis is necessary to determine the relative cost-performance benefits.

4.3.1.4 Separate Processor for Each Function

It appears possible to have a single digital processor handle all of the computational needs for the four adaptive arrays. Realization of such a processor, however, would likely require parallel processing by somewhat

smaller units. Furthermore, having a single processor for all the functions sacrifices the possibility of graceful degradation in the event one adaptive processor fails. Consequently, a design having four essentially identical digital processors is recommended, each having the capability of serving any of the MFBARS functions. In the event one of the adaptive processors fails, the remaining three highest priority functions could continue operating.

4.3.2 Interfaces

Separation of the adaptive processor from the antenna array and radio receiver means that careful attention must be given to the interface among these several devices. The intent of this section is to list the principal required interfaces. Additional work is required to specifically detail the interfaces, including such information as voltage levels, number of wires etc.

4.3.2.1 Radio/Adaptive Controller Shared Circuits

Although not strictly an interface, the fact that the radio and adaptive processor share circuits extensively results in the necessity for interrelated design and function considerations. Receiver AGC, for example has considerable influence upon adaptive processor performance. It will be necessary to provide information to the adaptive processor as to the amount of receiver AGC. Thus, receiver designs incorporating a number of independent AGC functions which may not be well-characterized over a temperature range would not be consistent with good adaptive processor performance. Furthermore, the adaptation rate of the algorithm is significantly affected by the bandwidth of the radio intermediate frequency. Thus, intermediate frequency sample points for the adaptive processor may need to be specified differently for each of the MFBARS functions. Design of the radio bandpass filters for minimum degradation of the adaptive processor perturbation functions is also highly desirable although it might result in somewhat less selective filters, at least at this point in the IF circuitry.

4.3.2.2 Adaptive Processor to Radio

The adaptive processor provides optimized RF signals to the radio. A signal RF output is provided from each of the adaptive processors. The adaptive processor also provides status information such as quality of the adaptation, health information, etc. to the radio master digital processor.

4.3.2.3 Radio to Adaptive Processor

The radio must provide noise and desired signal performance measurements to the adaptive processor. These performance measurements are obtained from the appropriate point in the radio's intermediate frequency circuits.

Frequency hop synchronization signals, in the case of JTIDS or SINCGARS, must be provided to the adaptive processor. It is expected that the adaptive processor will contain a read only memory, the contents of which can be used to calculate the required hopping sequences. However, the radio's digital processor, which has the responsibility of synchronization to the several desired signals, must convey sync information to the adaptive processor.

In the case of a priori direction of arrival information such as might be effectively utilized for GPS, it is assumed that computation of the desired signal steering vectors, including incorporation of the mutual coupling matrices, if necessary, will be provided by the master radio digital processor.

Finally, test and calibration signals should be sent from the radio processor to the adaptive processor, thus enabling and facilitating system checkout.

4.3.2.4 Other

Other interfaces such as power busses, heat transfer, cooling air, etc., may be required but are not considered here.

4.4 CONCLUSIONS AND RECOMMENDATIONS

The following paragraphs summarize the major findings of this investigation and recommend required additional development.

4.4.1 Summary

Because of the great expense associated with the installation of individual isolated antenna elements, the concept of multiple use arrays is recommended, specifically, an array serving GPS and JTIDS simultaneously and a second array serving SEEK TALK and SINCGARS. The number of elements in these arrays has been determined on the basis of other studies and formulated with specific threat information for the specific service. In some cases, particularly for SEEK TALK and SINCGARS, specific placement of antenna elements is nebulous and needs further refining.

In the area of adaptive processor design, a hybrid digital analog approach is strongly recommended. Such an approach utilizes the best features of a particular radio design while simultaneously removing the need for individual radio receivers in each of the antenna inputs. Thus, this approach is very cost effective and reduces size, weight and power. Performance of the hybrid approach can be nearly as satisfactory as the best analog circuits. Because the algorithm is realized in a digital processor which interfaces to the receiver intermediate frequency, algorithm improvement or change is easily accomplished by changing read-only memory devices.

The configuration selected for the receiver/adaptive processor/antenna array is one of separate rather than combined units. This approach has the advantage of allowing the radio to be used without the adaptive processor for those applications not requiring null steering AJ. Furthermore, the design facilitates a highly redundant weighting and combining structure, permitting continued system operation on the higher priority services even though one or more adaptive processors may fail. Additionally, this approach allows allocation of adaptive resources where needed; e.g., two separate adaptive processors can be used to optimally process L_1 and L_2 frequencies for GPS. Alternatively, all of the adaptive processors could be used independently to facilitate JTIDS acquisition.

Because of extensively shared circuits in the hybrid analog-digital processor approach, it is observed that close cooperation between the adaptive processor and the receiver designers is essential. Importantly, from a reliability standpoint, use of shared circuits does not reduce reliability.

If failure of the shared circuits occurs, this failure would result in function failure regardless of whether the circuits were shared or not.

4.4.2 Required Additional Development

In order to maximally benefit from the selected hybrid analog-digital processor and shared multiuse arrays, it is necessary that additional hardware be developed and additional analysis efforts be instituted. These items are follows:

- Low loss RF weight (broadband)
- Wideband JTIDS/GPS element
- Antenna array element placement technology
- Algorithms — detailed design and interfaces.

In summary, the wideband JTIDS/GPS element is required in order to reduce the installation cost of the antennas on a given vehicle. Development of a high quality broadband RF weight reduces or eliminates the need for low noise RF amplifiers in each of the antenna inputs. This development would not only reduce cost but would also improve algorithm performance. The antenna array element placement technology would use adaptive algorithm performance estimation programs, in conjunction with an electromagnetic analysis technique such as the geometric theory of diffraction, to determine best sites or locations for the antenna elements. This is most important for the SEEK TALK and SINGARS elements and, to a lesser extent, for the JTIDS elements which are not common to the GPS/JTIDS array (auxiliary elements). Finally, detailed algorithm design and specification of interfaces at the hardware level among the adaptive processors and the radio circuits is required. This effort will require that radio bandwidths consistent with the adaptive processor needs be selected and that such functions as automatic gain control can be properly communicated to the adaptive processor facilitating algorithm stability.

5. RF/IF SUBSYSTEMS AND COMPONENTS

The MFBARS baseline system utilizes extensively advanced technologies; The status of these technologies will greatly influence the viability of of the MFBARS. Historically, RF/IF subsystems and components generally dominate the cost and performance of most avionic systems. Extensive studies were made during Phase II to assess the availability of the RF/IF subsystem's and components required for an operational MFBARS in the late 1980's. These studies further accentuated the key RF/LSI subsystem/components for baseline design as follows:

- Amplifiers - L-Band low-Noise Amplifier
 - L-Band Power Amplifiers
 - HF, VHF and UHF Power Amplifiers
- RF LSI circuits
- Frequency synthesizers and frequency sources
- SAW devices

The results of these studies are presented in subsections 5.1 through 5.4.

The low-noise preamplifier (LNA) is one of the more critical components in a receiver and generally sets the noise figure and input dynamic range of the receiver. The requirements for the preamplifiers operating in the HF/VHF/UHF frequency range is relatively mild. A cursory study of these amplifiers indicates no difficulty in meeting the requirements shown in Table 5-1 with current technology. The requirements for the L-Band low-noise amplifier (LNA) are more difficult to meet. A low-noise amplifier study was concentrated on the L-band LNA. The results of this study presented in Paragraph 5.1.1., indicates that, with nominal amount of additional effort, the required L-Band LNA can be developed.

Power amplifiers for the MFBARS application also require two separate units in order to cover the two separate bands, an L-Band power amplifier and a HF/VHF/UHF power amplifier. The technology forecast and evaluation of L-Band and HF/VHF/UHF power amplifiers for the MFBARS application are described in Paragraphs 5.1.2 and 5.1.3, respectively. As shown in Figure 5-1,

Table 5-1. HF, VHF, and UHF Receiver Performance Requirements

Frequency Band Parameter	HF	VHF	UHF
Tuning range (MHz)	2.0-30.0	30.0-172.0	225.0-400.0
Tuning increment (kHz) min	0.100	25	25
Noise figure (dB) max	15	15	15
Modulation/demod	AM, SSB, FSK	AM, NBFM, FSK	AM, FM, FSK, PSK, AM-diphase
Receiving bandwidths at 3 dB (kHz)	3 to 6	24 to 40	40 to 80
Shape factor (3 dB/60 dB) max	2:1	2:1	2:1
Image and IF rejection in dB (min)	80	80	80
IM distortion	>60 dB down from two tones at -5 dBm at the input		
Cross modulation	Undesired signal 10% removed in frequency, and at +10 dBm must produce <30% cross modulation		
Receiver input protection	Input signal levels >2 V must not cause permanent damage		

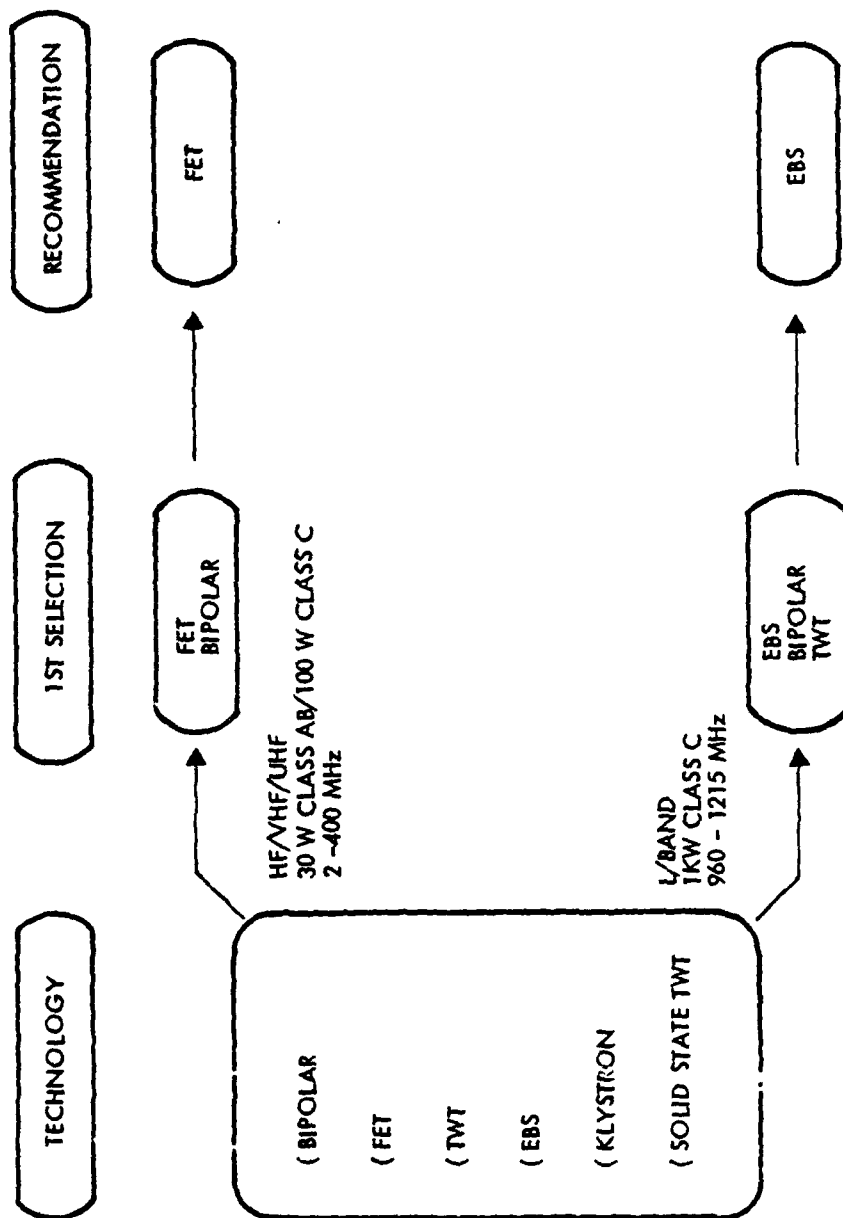


Figure 5-1. Power Amplifier Technologies Overview

the study looked into a large number of candidate power amplifiers and initially identified that FET and bipolar transistor amplifiers are the most suitable candidates for HF/VHF/UHF applications, and that electron bombardment semiconductors (EBS), bipolar transistors, and TWT amplifiers are best for the L-Band. The final recommendation was FET and EBS amplifiers.

The most important components in the TRW system's MFBAR architecture is the RF LSI circuit. The RF LSI is a TRW term for silicon bipolar transistor monolithic analog integrated circuits. It is, in effect, a high-speed bipolar IC process of using oxide aligned transistor (OAT) RF/IF circuits. The key RF LSI circuits for the MFBARS have been identified and are described in subsection 5.2. Another crucial RF/IF subsystem is the frequency synthesizer; TRW baseline systems require only two designs to cover the entire frequency bands of interest. Other important RF/IF subsystems include frequency sources and saw filters. Studies and results for the frequency synthesizer/sources and saw filters are presented in subsections 5.3 and 5.4, respectively.

5.1 AMPLIFIERS

5.1.1 L-BAND LOW NOISE AMPLIFIER

The MFBARS baseline architecture calls for a single L-Band low noise amplifier (LNA) to cover the entire L-Band (960 to 1575 MHz) functions of interest (JTIDS, TACAN, IFF and GPS). Because of technology limitations, past system designs were based on using two separate LNAs, one to cover the 960 to 1215 MHz bandwidth for JTIDS and TACAN operations, the other covering GPS operations at the specific frequencies of 1227.6 and 1575 MHz. This approach was originally proposed by TRW and carried on through Phase I studies. Recent advancements in L-Band low noise amplifier devices and designs at TRW indicate that a single LNA design will cover the entire desired L-Band frequency range with lower noise figure and remain capable of serving all functional requirements. Table 5-2 compares the performance of the new TRW LNA and the old design approaches.

The new TRW LNA design is clearly superior in that it has a lower noise figure (1.8 dB vs. 3.0 dB) and requires only one design to cover the entire

Table 5-2. L-Band Preamp Capabilities vs Requirements

	REQUIREMENTS	EXISTING	TRW (1982)
1) NOISE FIGURE (DB)	3.0	3.0	1.5
2) BANDWIDTH (MHZ)	960-1585	960-1215 1225-1575	960-1585
3) GAIN (DB)	30	30	30
4) IP ₃ (DBM)	+30	+30	+30
5) 1 DB COMPRESSION (DBM)	+20	+20	+20
6) FLATNESS (DB)	±0.5	±0.8	±0.5

frequency band. Additionally, experimental work at TRW indicates that a high reliability, single LNA design is achievable by 1982. Although the design is still in developmental stages, it will be ready for production well within the time frame of the MFBARS schedule requirements.

The TRW LNA is a discrete amplifier design using HP1101 FETs as the basic stage. Devices from several other manufacturers have also been evaluated. The basic configuration is shown in Figure 5-2. Preliminary laboratory measured results presented in Figure 5-3 indicate performance exceeding MFBARS requirements. The measured results indicate that the TRW amplifier design will have:

- Noise figure less than 1.5 dB
- VSWR less than 1.5:1
- Frequency bandwidth up to one octave
- IP_3 exceeds +25 dBm

5.1.2 L-Band Power Amplifier

The L-Band Power Amplifier is required for JTIDS, TACAN and IFF applications. The requirements for this power amplifier are summarized in Table 5-3, and are based on matching the greatest number of service performance requirements of the current equipment. The power amplifier is a key element in the Joint Tactical Information Distribution System (JTIDS) because it has a significant impact on system size, cost, power consumption, and overall performance capabilities. At present, power amplifiers are being developed using bipolar transistors. Due to inherent thermal limitations, transistors in this frequency range are capable of only low power or low power gain at high duty cycles. Therefore, transistor amplifiers are large, inefficient, complex, and expensive since the power outputs of many devices must be combined in order to meet the high power, high duty cycle requirements of JTIDS. A transistor amplifier having less capability was proposed in Phase I and is described in subsection 5.1.2.1. However, recent advancements in Electron Bombardment Semiconductor (EBS) devices indicate that they have the potential to achieve system design goals, and study results are presented in subsection 5.1.2.2.

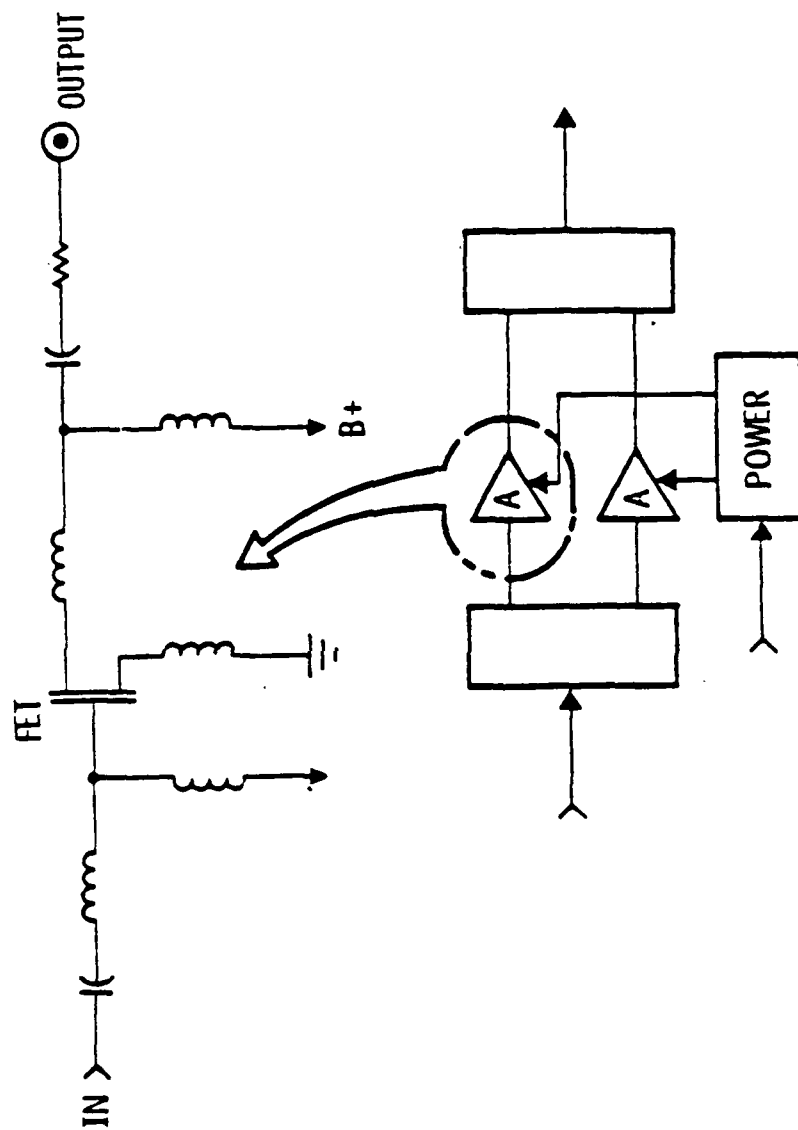


Figure 5-2. L-Band Preamplifier Design Uses Basic FET Stage

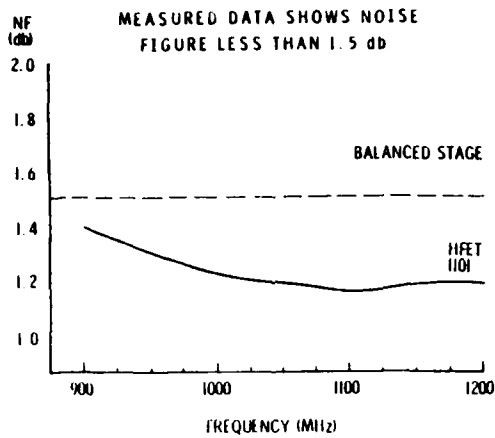


Figure 5-3a.

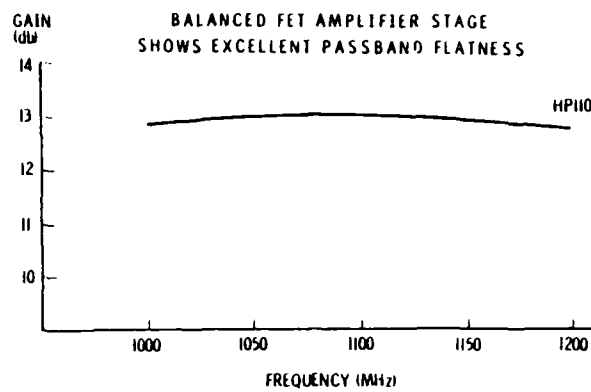


Figure 5-3b.

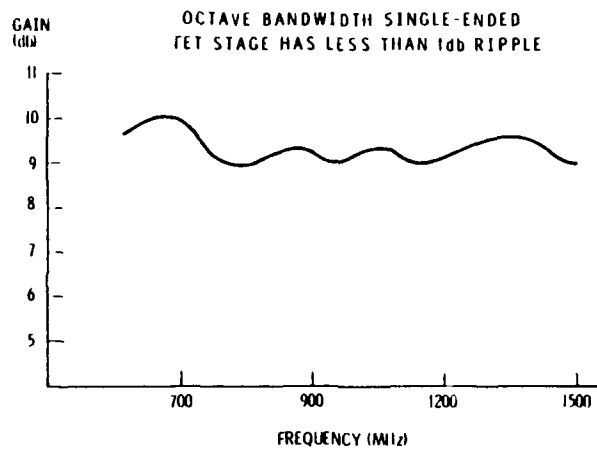


Figure 5-3c.

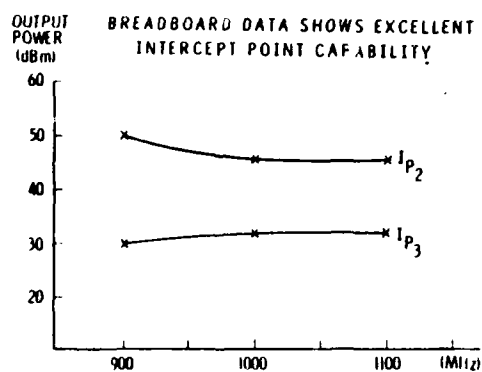


Figure 5-3d.

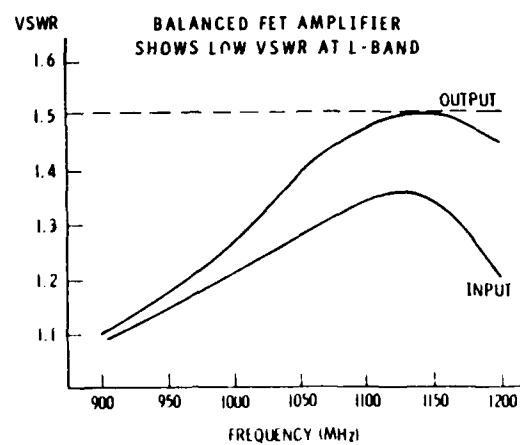


Figure 5-3e.

Figure 5-3. Low Noise Amplifier (LNA) Measured Performance

Table 5-3. L-Band Transmitter Requirements for MFBARS

Pin	0 dBm
Info Bandwidth	960 - 1215 MHz
Power (Pk) Low	500W
High	1000W
Flatness	$< \pm 1$ dB
IM at 1 dB compression point	< 35 dBd
Duty Cycle Long Term	1% to 20%
Short Term (5.7 mSEC)	$> 55\%$
Efficiency (incl. Converter)	$> 35\%$
Prime Power	115 vac < 1785 W (pk. low power)
Output Mode (Class II JTIDS)	
Low Power, $1/2 P_0$ to each antenna output	
High Power, $1/2 P_0$ to each antenna output	
TACAN/IFF, full P_0 to either antenna	
RF impedance (in/out)	50Ω , $\leq 1.5:1$
Modulation input impedance	50Ω , $\leq 1.5:1$
Volume	< 500 IN ³

5.1.2.1 100-Watt Power Amplifier

One possible design for the L-Band power amplifier is a 100-watt transistor amplifier. This design was considered in Phase I of the MFBARS studies. It is designed to produce at least 100 watts of CW power at L-Band with a solid state design. It is suited for JTIDS application in fighter class terminals, but can also be used for TACAN applications. Performance would be degraded relative to current equipment because of the peak power level (200 watts).

A block diagram of the power amplifier circuit is shown in Figure 5-4. The circuit consists of a 4-stage preamplifier and 4 final power amplifier stages. In the final power amplifier stage, two 40-watt transistor amplifiers are first combined to produce a 75-watt amplifier. Two 75-watt amplifiers are combined to produce a 100-watt power output. The 40-watt amplifiers are driven and combined using six L-Band hybrid couplers. When operated at a low duty factor (less than 5 percent), these amplifiers are capable of producing a peak power output of 200 watts. The overall dc to RF efficiency of the 100-watt amplifier is approximately 24 percent.

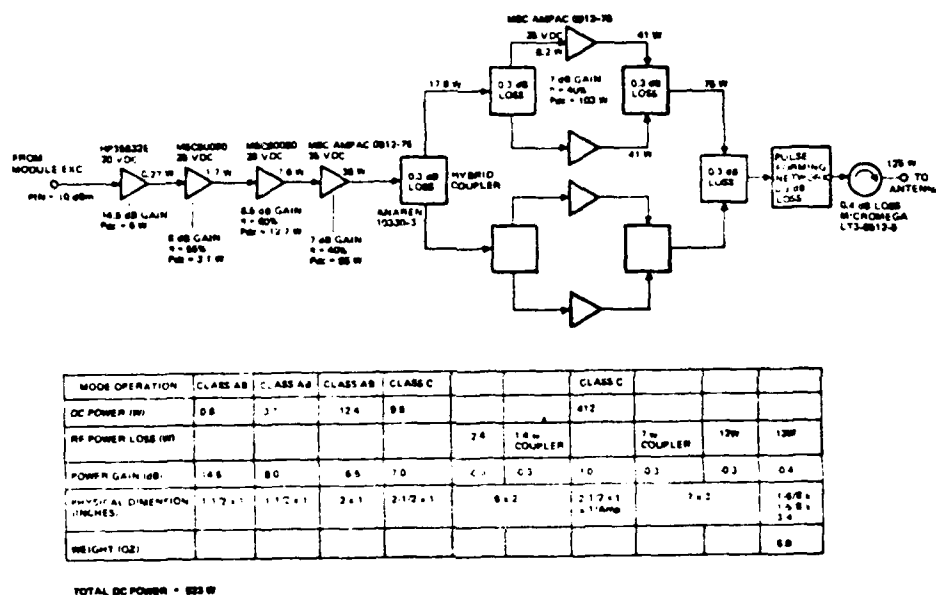


Figure 5-4. Power Amplifier

The transistor amplifier technology can be further extended to improve the output power capability. A preliminary design is shown in Figure 5-5. However, this design is deemed to be less efficient than that using the electron bombardment semiconductor amplifier which is described in the following section.

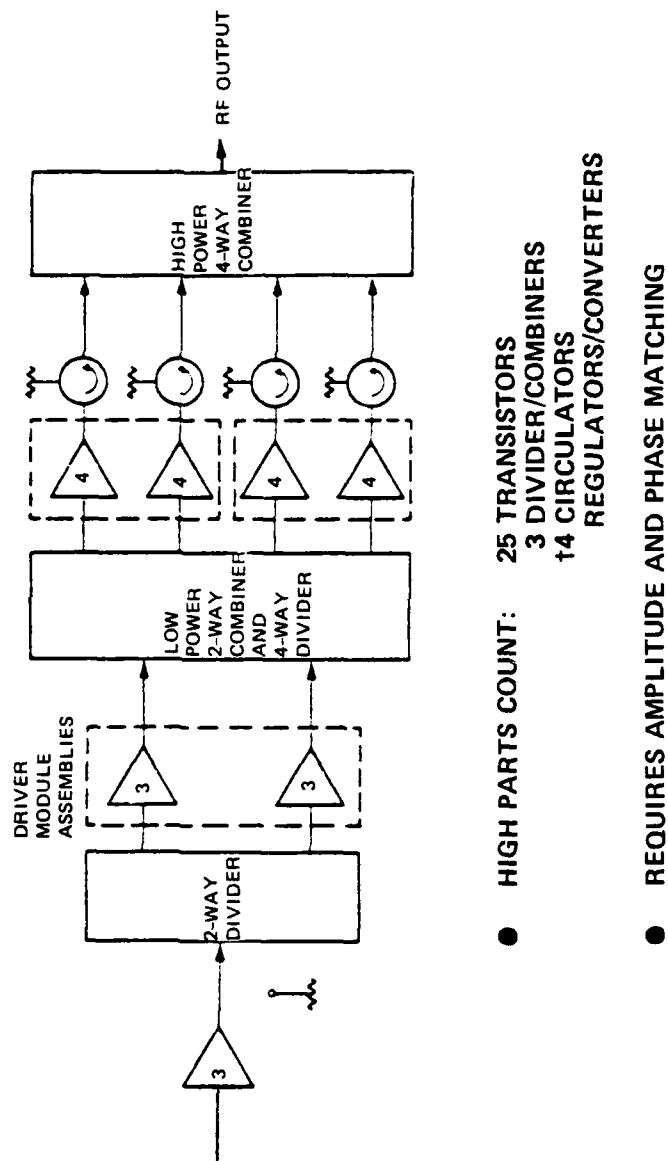


Figure 5-5. Full-Power Solid-State L-Band Power AMP

A microwave integrated circuit design for the transistor amplifier, minimizes size, weight, and manufacturing cost. The amplifier circuits will be fabricated on alumina substrates. All circuit elements, such as chip capacitors and resistors, will be reflow soldered to the substrates. A stripline approach is proposed in the 3 dB coupler design and achieves substantial size reductions compared with the standard microstrip Wilkinson coupler. A combination of stripline and microstrip circuitry will be utilized to best satisfy system and packaging requirements.

Because of high duty cycles, the basic design of the pulse amplifier is similar to the conventional CW power amplifier design. In the final design, it should be noted that the power transistors must be matched for power gain to obtain good load sharing. The main advantage of the power combining technique shown in Figure 5-5 is good reliability. This method takes advantage of the isolating properties of hybrid couplers. The 10 mW input signal is amplified to 38 W and fed into a hybrid power divider. The output power from the hybrid is split equally and fed into two separate amplifiers, each containing two amplifiers in parallel. The 75 watt output signals from the separate amplifiers are recombined to produce 138 watts to the isolator. Because of the isolating properties of the hybrid coupler, a failure of one amplifier reduces the total power output but does not cause failure of the overall amplifier stage.

For TACAN application, the output pulse of the amplifier is required to have a Gaussian response shape. To achieve this, it is necessary to connect a pulse-forming network section in cascade with the power amplifier. This corrects the phase or time delay characteristics of the amplifier chain over the specified bandwidth with the lowest possible error. An all-pass filter is usually used in the design of the pulse-forming network, adjusting the overall time delay of the amplifier. The all-pass filter consists of a multisection LC lattice network with zero attenuation and a controllable phase characteristic. The original amplifier circuit has a phase characteristic in the frequency region of interest that gives rise to phase or delay distortion. By adding the phase response of the all-pass filter to the amplifier circuit, a new phase characteristic is

achieved which produces minimum phase distortion in the region of interest. The addition of the all-pass filter does, of course, increase the total signal delay. In the proposed application, however, this is not important.

5.1.2.2. Electron Bombardment Semiconductor

An alternate to transistors is a relatively new component, the electron bombardment semiconductor (EBS) which has been under development for the past ten years, principally by Watkins Johnson (WJ). The material presented in this section is based on the work of WJ. The EBS has already demonstrated CW output power capabilities four to five times greater than state-of-the-art transistors and power gains (in dB) that are also four to five times as great. In most applications, one EBS can replace between 10 and 15 transistors, including the individual matching, bias circuitry, power combiners, and circulators required by the transistors. The resulting EBS amplifier is potentially less expensive, smaller, more efficient, and can provide superior electrical performance. Unlike the bipolar transistor, the operation of the EBS is dependent on the fact that an energetic electron striking a reverse biased silicon diode produces thousands of additional mobile electrons through impact ionization of the silicon. As shown in the Figure 5-6, the silicon diode is fabricated with a thin junction and contact layer so that the incident electrons can penetrate to the high-field regions in the depleted junction with minimum loss of energy. The resulting current gain is linear, since the output current is proportional to the incident electron current. A large power gain results when an external resistive load is connected to the diode.

A simple grid-modulated EBS RF amplifier consisting of a cathode, grid, semiconductor diode and input/output circuitry can be designed (Figure 5-7). An input signal applied between the grid and cathode modulates the electron beam which then strikes the semiconductor diode. The electron beam can be controlled with a low level RF signal by using a fine mesh grid located close to the cathode. The cathode bias supply is chosen so that if no input signal is applied, no electron beam current flows. Thus, the output power can be modulated solely by the input RF signal. Output matching, typically a section of microstrip transmission line, is included to electrically match the semiconductor diode at the desired operating frequencies.

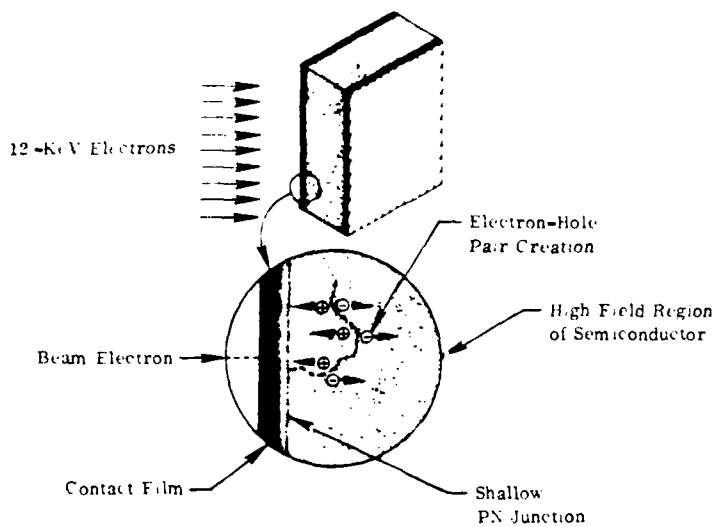


Figure 5-6. Electron Bombardment Semiconductor (EBS)

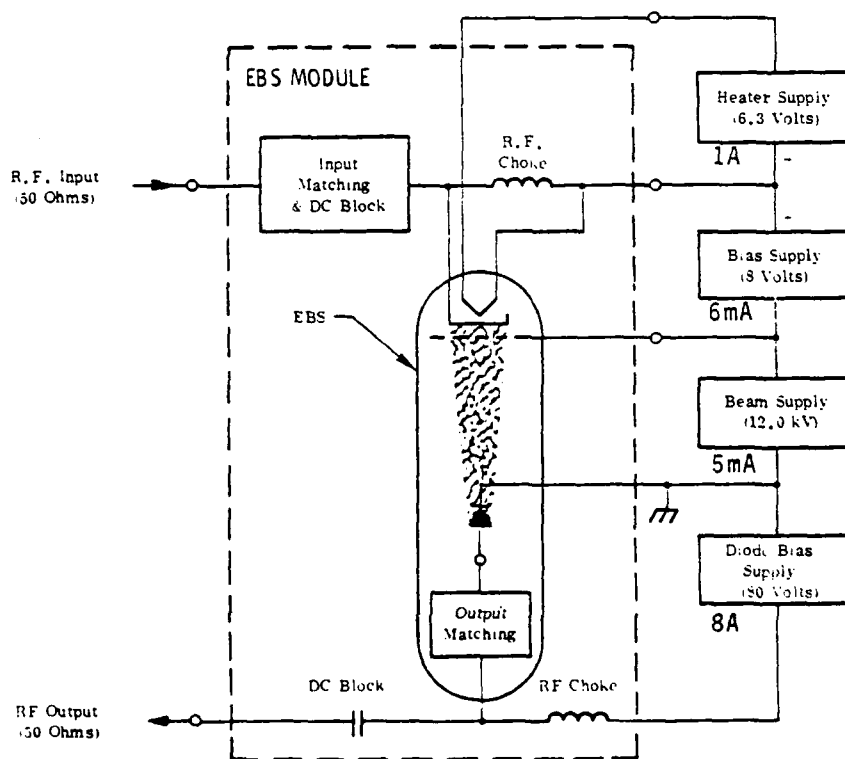


Figure 5-7. Grid (Density) Modulated EBS Amplifier

This EBS configuration results in a small and rugged design capable of high power and high gain. For example, over a 1500-watt peak output (1 percent duty) has been achieved at 1 GHz with a gain of over 25 dB. In addition, this type of EBS is very simple to use as a power amplifier since only four dc power supplies are required and output modulation can be achieved by modulating the low level input RF pulse. Approximately 90 percent of the total power consumption for the 500-watt peak, 50 percent duty EBS will be from the 80 volt, 6 amps diode bias supply. The electron beam operates at a relatively low power level, since the electron beam is used only for control of the much greater diode current. For example, in the proposed amplifier, the beam supply will be required to deliver 4-5 mA. Similarly, the 8 volt grid bias supply will operate at only 5-6 mA. The heater supply can operate either ac or dc at approximately 1.0 A. The required power supplies can be both compact and efficient. Since the overall efficiency of the EBS will be higher than present transistor amplifiers, the power supplies for the EBS are required to provide less power and, thus, are significantly smaller despite the need for the low current 12 kV supply. The EBS, when integrated with these supplies, and other support circuitry results in a compact, efficient, reliable amplifier.

Current EBS development particularly coincides with that of the MFBARS Program. Extensive efforts have been concentrated in developing EBS amplifiers for JTIDS and TACA applications. Development of an EBS amplifier module for the JTIDS Class II terminal is currently underway with three government-funded programs and an IR&D program. The basic program goals for the three Government programs are shown in the Table 5-4. The RADC program has a goal of 500 watt peak at 20 percent duty, with a gain of 23 dB and an overall efficiency of 40 percent.

The NOSC No. 1 program continues the development of the JTIDS EBS amplifier by increasing the duty cycle capability from 20 percent to 50 percent required for the JTIDS system. The NOSC No. 2 program will develop a complete amplifier module around the EBS device developed during the NOSC No. 1 program. The IR&D program is developing new diode and device technologies which will significantly improve EBS amplifier capability for JTIDS.

Table 5-4. Basic Program Goals

RADC Program Goals (Contract F30502-78-C-0247)	
Frequency Peak Power Duty Cycle Gain Pulse Width Efficiency	960 to 1215 MHz 500 W, +1, -0 dB 20 percent 23 dB 6.4 μsec 40 percent
NOSC No. 1 Program Goals (Contract N66001-78-C-0295 WJC)	
Frequency Peak Power Duty Cycle Gain Pulse Width Efficiency	960 to 1215 MHz 500 W, +1, -0dB 50 percent 23 dB 6.4 μsec 40 percent
NOSC No. 2 Program Goals To develop an EBS amplifier module with the RF performance characteristics of the NOSC No. 1 program, including input RF isolation transformer, input RF circuitry, EBS device, output RF and bias circuitry, and forced-air cooled heatsink.	

As indicated above, the programs are proceeding on or ahead of schedule. The end result will be an EBS amplifier module with characteristics ideally suited for the JTIDS Class II terminal. These characteristics will include 500 watt peak output at 50 percent duty cycle, 23 dB gain, and 40 percent overall efficiency.

Following is a summary of key milestones demonstrated with developmental EBS amplifiers:

- Demonstration of Bandwidth. The devices tested have consistently demonstrated greater bandwidth than required, with <1 dB of ripple across the band.
- 500 watt peak out at 20 percent duty. A single diode pair driving a single output has demonstrated 500 watt peak output at 20 percent duty. This forms the basic building block; higher powers and duty cycles are achieved by combining diode pairs.
- JTIDS/TACAN Pulse Shaping. Two techniques have been demonstrated for achieving the JTIDS or TACAN pulse shape. The first technique utilizes shaping of the input RF with a pin diode. The second technique applies a shaped video pulse to the cathode of the EBS which shapes the output pulse.
- Demonstration of Gain. The devices tested have consistently demonstrated gains in excess of 20 dB.
- Demonstration of Low/High Power TDMA and TACAN. The requirements of the Class II terminal are to be able to operate in two modes: (1) low or high power TDMA, with half power transmitted to each antenna; and (2) TACAN, with full power delivered to either antenna. The EBS device has demonstrated a unique solution to the problem with a two-output device, with each output designed to drive one antenna. Each diode pair has demonstrated the capability of outputting 125 or 250 watt for the TDMA mode (in phase) or independently outputting 500 watt from one output.
- Demonstration of Efficiency. The devices tested have consistently demonstrated target efficiencies of 45 to 50 percent with overall efficiencies in the 30 percent range. (Work on the NOSC No. 1 contract will increase overall efficiency to 40 percent).
- Demonstration of Long Pulse Capability. To simulate the long pulse burst required for TDMA, 5 msec RF pulses were run through the EBS device. There was no drop over the pulse length (except drop associated with bias voltage).

The advantages of the EBS amplifier as compared to alternative amplifiers were studied and presented in Table 5-5. A possible design for the MFBAR application is shown in Figure 5-8.

Table 5-5. Comparison of EBS, Transistor and TWT Amplifier for L-Band Application

	EBS vs. Solid State	EBS vs. TWT
Advantages of EBS	• Large Target Device • Higher Dynamic Range • Easy Pulse Shaping • Reliability • High Gain- Fewer Devices • Less Complex Power Supply	• Simpler Beam Tube Structure Short Beam, Easy Stability • Low Beam Current (10 mA/CM² vs. 2A/CM²) • Cooler Cathode • Easy Pulse Shaping • Reliability • Producibility • Less Complex Power Supply
Disadvantages	• Contact Punch-Thru • Thin Junction Defects, Surface Charge • On/Off Power Ratios	• Non-Linearity • On/Off Power Ratios

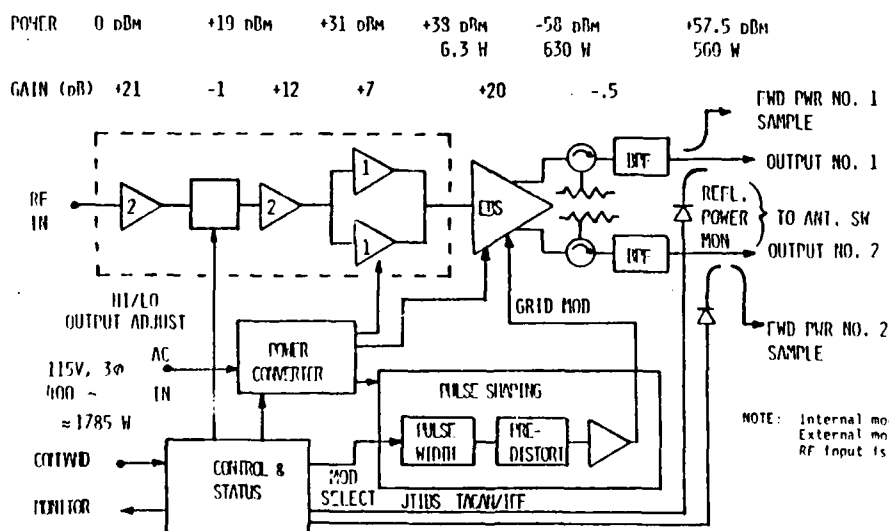


Figure 5-8. L-Band EBS Power AMP Module

In summary, the EBS amplifier appears to be the best choice for the MFBARS program and should be fully developed in time to achieve an advanced MFBARS development model by 1985. Additionally, the EBS technology can make significant contributions to the MFBARS performance objectives as follows:

- Reduce size/volume and weight
 - Prime RF circuits
 - Power supply
- Universal application for all L-Band CNI operations JTIDS/TACAN/IFF
- Lower LCC through producibility and reliability

EBS demonstrated performance is summarized as follows:

- Bandwidth (1 dB) Greater than
 960 to 1215 MHz
- Power (PK)/Duty Cycle 500 W @ 20%
- Gain >20 dB
- Dynamic Range Low/High Power
 - TDMA
 - TACAN/IFF
- Efficiency
 - Target 45 - 50%
 - Overall 30 - 40%
- Pulse Shaping/Linearity TACAN and JTIDS
 - Pin Diode Shares RF
 Input
 - Shaped Video Cathode
 Pulse
- Long Pulse Capability 5 mSEC
- Reliability CW 200K Hrs Test, No Failures
 (MTTF 87K Hrs @ 90% Conf.)
 - Pulse 86K Hrs Test, No Failures
 (MTTF 38K Hrs @ 90% Conf.)

5.1.3 HF/VHF/UHF Power Amplifier

The baseline architecture shows that a single power amplifier covers the entire HF/VHF/UHF (2 to 500 MHz) range. The power requirements for the various services are tabulated as follows:

<u>DESCRIPTION</u>	<u>FREQUENCY (MHz)</u>	<u>RF POWER</u>
HF (VOICEGUARD)	2-20	400W
VHF FM (VOICEGUARD)	30-88	123W SELECTABLE
VHF AM (VOICEGUARD)	108-156	40W
UHF RADIO (VOICEGUARD)	225-400	10W
SEE TALK (VOICE COM)	225-400	30W AS 10W AM

Implementation of such a power amplifier presently does not exist. However, it is believed to be within the state-of-the-art. To perform such a development was considered to be too much of a detail at this stage of the MFBARS Program. However, a cursory study of power amplifier designs indicates that the requirements can be readily met by using two power amplifiers, one to cover the HF (2 to 30 MHz) range and the other VHF/UHF (30 to 400 MHz). Current balanced bipolar transistor devices have the capability to fulfill the demand for such power amplifiers. In the future, field effect Transistors (FET) will improve the efficiency and durability of the power amplifier.

Typical power amplifier designs for VHF/UHF and HF applications are shown in the block diagrams in Figures 5-9 and 5-10. As indicated by distribution and power levels, they are realizable with existing bipolar transistors. It is well known that field-effect transistors have the following inherent advantages over the bipolar transistor:

- Ease of processing
- Better DC stability
- More Ruggedness
- Lower noise
- Better linearity
- High efficiency

POWER	0 dBm	+12.5 dBm	+25.5 dBm	+35.5 dBm	+45.5 dBm
				3.6 W	35.5 W
GAIN (dB)	+12.5	+12	+10	+10	

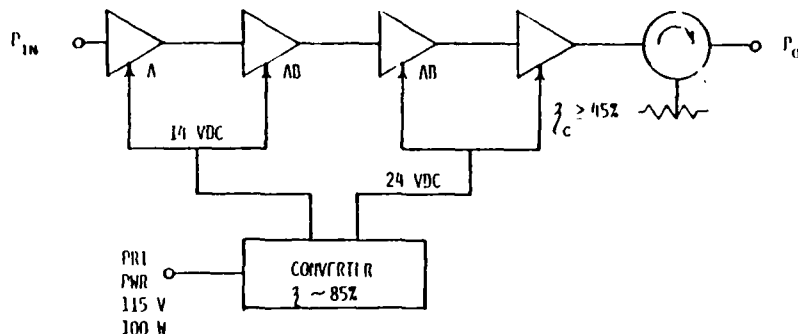


Figure 5-9. 30-400 MHz VHF/UHF Transmitter for MFBARS

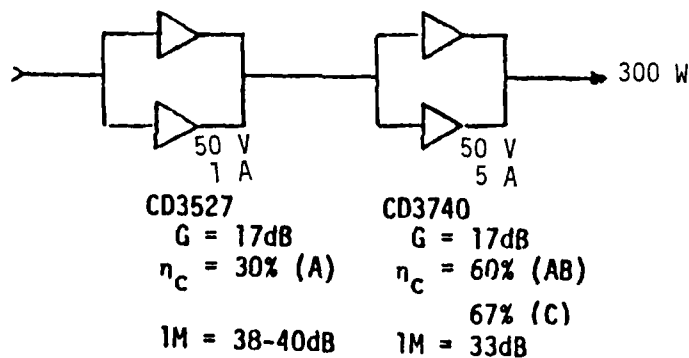
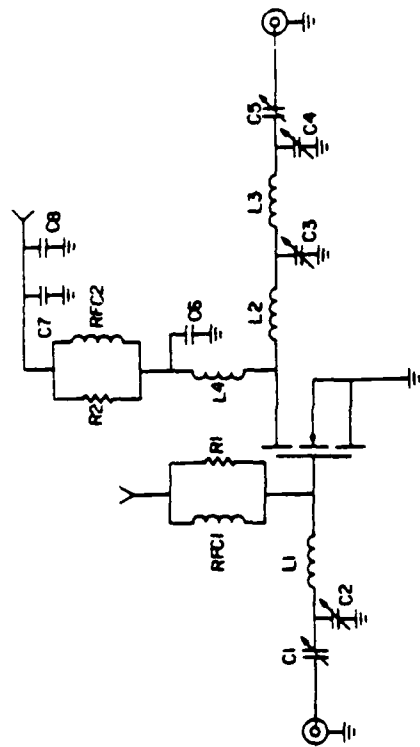


Figure 5-10. Transistors for HF Power Amplifier (2 to 30 MHz)

However, present FETs lack sufficient bandwidth and power requiring further development. The currently available FET transistor performance is shown in Figure 5-11. Necessary improvements to meet the MFBARS objectives could be achieved in the next 5 years as a natural evolution of the semiconductor industry if the demand is identified.

TEST CIRCUIT 175 MHZ, 100 WATT



N CHAN = Si FET

$\eta \geq 50\%$ AT $f = 175$ MHz, $V_{DS} = 35$ V, $I_Q = 40$ mA

$g_m = 2.2$ MHO TYP

$C_{DS} = 170$ pF TYP

$BV_{DS} \geq 65$ V

$\theta_{jc} = 0.7^\circ$ C/W TYP

TYPICAL POWER OUT VS. POWER IN AT 175 MHZ
CLASS AB $I_Q = 40$ mA

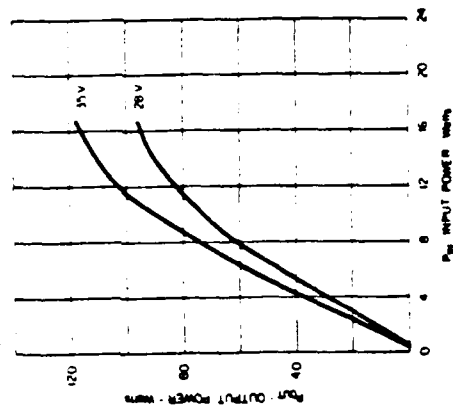


Figure 5-11. Available Performance for VHF FETs (CTC BF100-35)

5.2 RF LSI TECHNOLOGY FOR MFBARS

5.2.1 Introduction

While the MFBARS concept offers significant system simplification in all applications (GPS, IFF, JTIDS, etc.) because of shared rather than dedicated hardware, it is nevertheless a very complex system. If MFBARS is to be implemented within the size constraints of any but the largest aircraft, it is obvious that conventional hardware techniques must be modified. TRW's RF LSI technology, in combination with hybrid thin film technology (MIC), offers size reductions over conventional circuit technology by factors of 10 to 100. These size reductions are usually accompanied by DC power reduction and performance improvements. This section, after a brief introduction to the RF LSI technology, describes potential RF LSI implementations of the major MFBARS subsystems and indicates the current circuit development status.

5.2.2 RF LSI Background

RF LSI is TRW's acronym for silicon bipolar transistor monolithic analog integrated circuits. It is, in effect, a high-speed bipolar IC processing technology applied to analog circuits. In 1971 TRW began to develop an oxide aligned transistor (OAT) process with the initial aim of providing a monolithic implementation technique for high-speed digital circuits. This development effort has been very successful, leading to a family of digital ICs which clearly represent the state-of-the-art. Recent developments include a 400 megasample, 5-bit analog-to-digital converter, a frequency synthesizer programmer (in essence, a variable modulus divider) which operates to 1500 MHz, and a large assortment of high-speed digital multipliers.

Late in 1974, it was recognized that the OAT process had significant potential for analog circuit applications. The process offers transistors with a 5 GHz cut-off frequency, thin film resistors, metal-oxide-metal capacitors, and monolithic flat spiral inductors. An internally funded development effort was initiated, culminating late in 1975 in a Costas loop BPSK demodulator which operates at a 500 MHz carrier frequency and a one megabit data rate. With the exception of the loop filter's operational

amplifier, the Costas demodulator is entirely contained on a 70 x 115-mil silicon chip. The Costas loop contains about 175 active devices, requires 0.85 watts power, and has a measured bit error performance rate of 0.8 dB from theoretical.

Since the initial development effort, several additional RF LSI chips have been developed and are described briefly below:

- 1000 MHz BPSK Costas Loop Demodulator. Similar to the 500 MHz version, with the VCO frequency raised to 1000 MHz and the data rate increased to 10 Mbps. Both Costas loop chips are shown in Figure 5-12.
- 500 MHz Phase Logic Demodulator. A new type of BPSK demodulator utilizing an injection locked rather than phase locked oscillator. This design, a TRW innovation, has the advantage of fast acquisition
- Building Block Circuits. A chip development containing a variety of building block circuits intended to be generic test cases suitable for a wide variety of applications. The building blocks include RF and IF amplifiers, VCOs, analog multipliers, operational amplifiers, several versions of each circuit were fabricated to cover the 10-1800 MHz frequency range.
- L-Band Receiver. A chip development incorporating several circuits to form a superheterodyne receiver. The receiver consists of a preamplifier (1200 to 1400 MHz), a mixer, a local oscillator, IF amplifier (gain controlled), and a BPSK demodulator. A block diagram of this chip is shown in Figure 5-13.
- GPS Receiver Front End. This chip consists of a preamplifier (1575 MHz), a mixer which simultaneously downconverts the received signal to 143 MHz and despreads it with a punctual code, and an IF amplifier. A parallel path after the preamplifier downconverts to 143 MHz and multiplies the signal by an early/late version of the PN code is also included. The chip is in early check-out stages and has, thus far, functioned in a generally correct fashion (although signal processing gain has been lower than anticipated on the first two chips tested). Figure 5-14 shows a schematic of this chip, and Figure 5-15 is a photograph of the chip.
- Signal Detection Chip. This chip, intended for use in a channelized receiver, will provide (through a preamplifier, detector, and a bank of integrators and comparators) a preliminary measurement of radar pulse frequency, amplitude and pulsewidth. Key chip features include a 70 dB dynamic range, an AGC loop with less than 5 nsec response time, and a 500 MHz input bandwidth. This chip, in an early test phase, seems to be functioning correctly. The schematic and photo of this chip are shown in Figure 5-16.

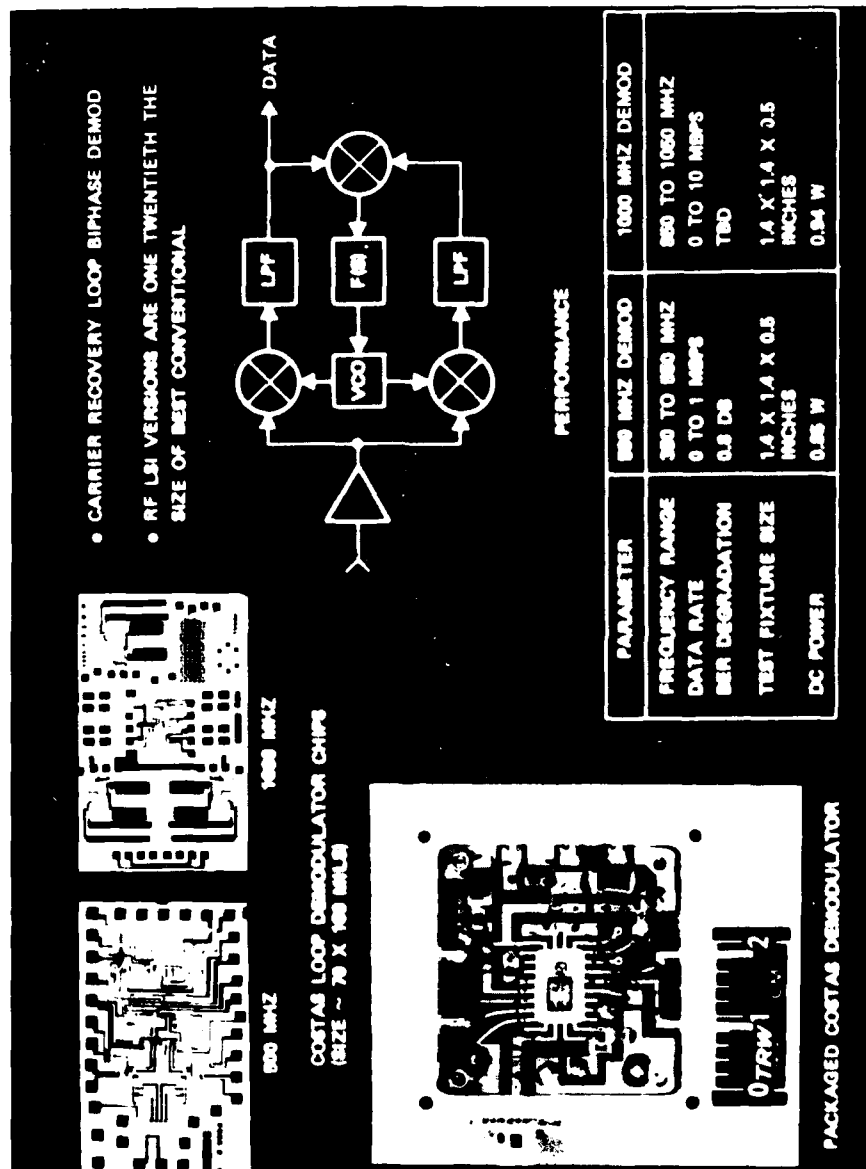


Figure 5-12. 500 MHz and 1000 MHz Costas Loop Demodulators

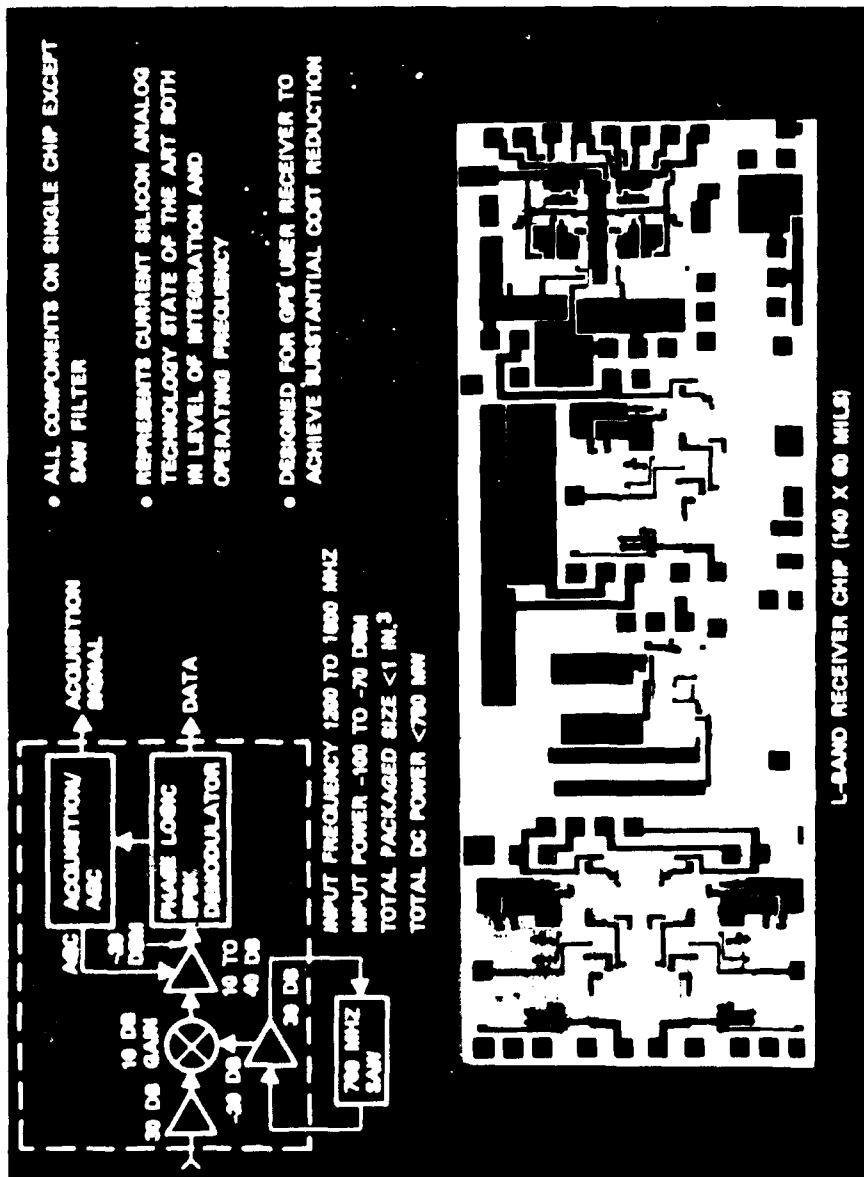


Figure 5-13. RF LSI L-Band Receiver

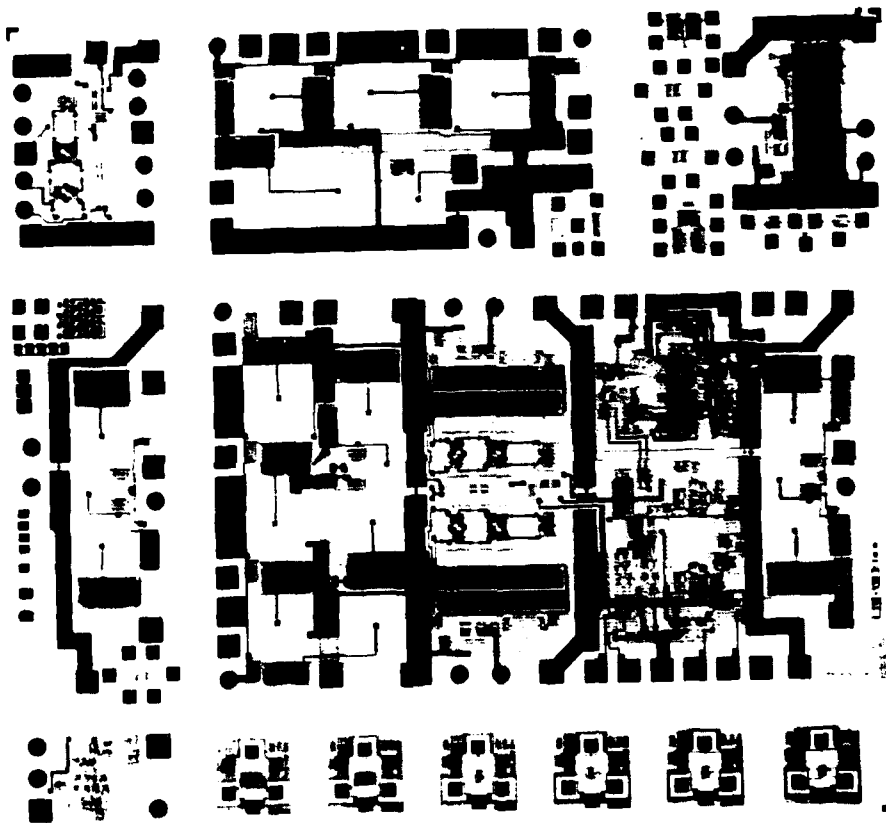
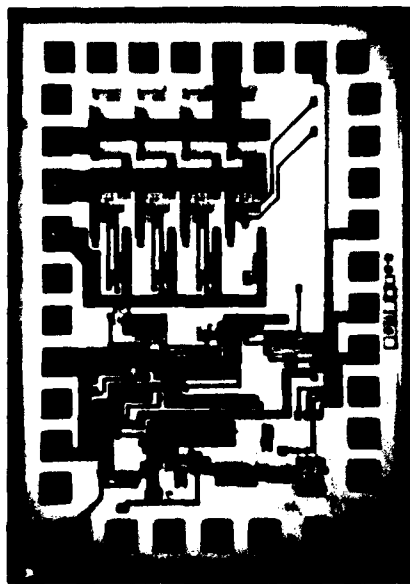


Figure 5-15. GPS Receiver Front End Chip



CHIP SIZE
100 X 70 MILS

- DETECTS SIGNAL PRESENCE WITHIN CHANNEL BANDWIDTH AGAINST A PRESET THRESHOLD
- MAKES INITIAL ESTIMATE OF PULSE WIDTH AND PULSE AMPLITUDE
- PROVIDES REDUCED DYNAMIC RANGE PRE AND POST DETECTION OUTPUTS
- PERFORMANCE:
 - RF BANDWIDTH 500 MHZ
 - VIDEO BANDWIDTH 20 MHZ
 - DYNAMIC RANGE 60 DB
 - AGC DELAY TIME 10 NSEC
 - DC POWER 616 MW

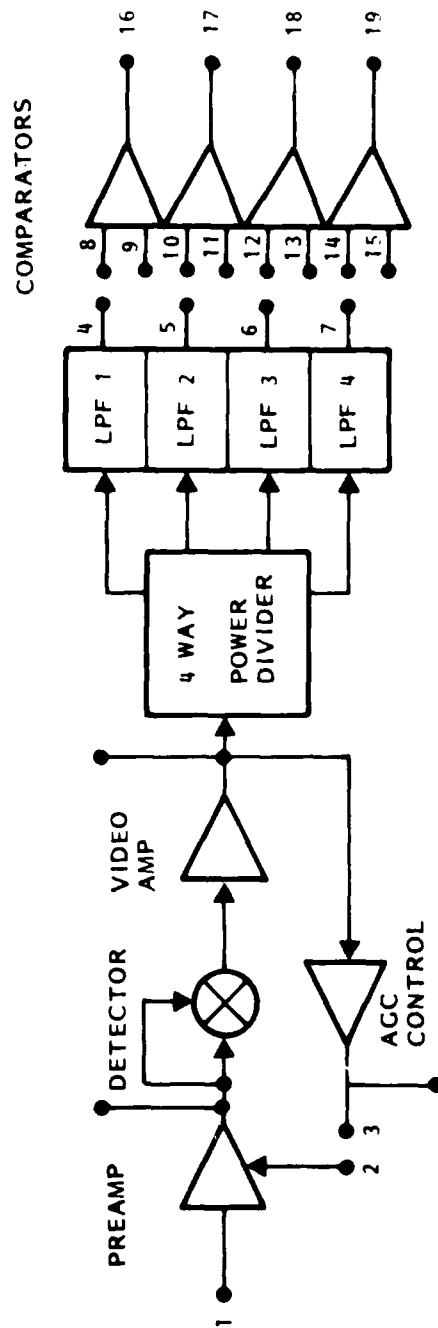


Figure 5-16. Signal Detection Chip Schematic and Photo

In addition to the above chips, seven new chips are under development, including a high-speed log amp, an instantaneous frequency measurer (IFM), three frequency synthesizers, and a frequency converter chip.

5.2.3 RF LSI Implementations for MFBARS

Preliminary designs have been developed for most of the MFBARS hardware. Virtually all of the RF circuitry in MFBARS, except for low noise and power amplifiers, can be implemented in RF LSI. A total of eight different chip types can be utilized in the system. Table 5-6 summarizes the types of chips, the number of chips required, and the chip system applications.

Table 5-6. MFBARS RF LSI Utilization

Chip	No. Per System	Application
SP4T Switch	20	IF Switch Assembly
4PST Switch	20	
IF Correlator/ Demodulator	5	GPS
GPS Frequency Synthesizer	1	GPS
RF Amplifier/ Downconverter	5	GPS, JTIDS, TACAN/IFF
HF/VHF/UHF Frequency Converter/Amp	4	UHF/VHF/SINCARS, SATCOM SEEK TALK/HF Radio
Quadrature Modulator	2	All but GPS
General Purpose Frequency Synthesizer	11	All but GPS and JTIDS
Total Chips	68	

5.2.4 Switches

5.2.4.1 SP4T and 4PST Switches

The switch matrix is composed of a collection or tree of single pole four throw (SP4T) and four pole single throw (4PST) switches. The SP4T switch consists of four emitter followers (connected at their bases) with each emitter functioning as a separate output. The 4PST switch also consists of four emitter followers, but with separate base inputs and connected emitters. Switching is accomplished by gating the collector currents on and off. The remaining circuitry is bias and decoding circuitry to interpret the digital control commands.

5.2.4.2 IF Correlator/Demodulator

This chip is specifically designed for GPS to despread the received signal (and spread any jamming signal), removing any doppler shift, down-converting to baseband, and providing quadrature versions of the baseband data signals. The TRW baseline design as shown in Section 2 employs four IF correlator/demodulator channels for fast acquisition. It is feasible to incorporate from two to all four channels into a single LSI chip. A preliminary schematic of these functions for a single channel is shown in Figure 5-17. A tandem correlator approach is employed. The received signal is first multiplied by the modulo 2 sum of the P and C/A codes, and then by either the P code or the C/A code. The second multiplication is by the P code if the C/A code is being received, and by the C/A code if the P code is being received. If this correlation is executed in a single step, the mixer must perform the multiplication process with 60 dB of carrier suppression. The tandem approach involves less risk, and thus is higher yield, in that each mixer need only achieve approximately 35 dB carrier suppression.

The IF input signal $36 f_0 + \Delta$ ($f_0 = 5.115$ MHz, Δ = the doppler shift) is first mixed with a local oscillator signal at $29\frac{1}{2} f_0 + \Delta$. This oscillator signal is modulated by the mod 2 sum of the P and C/A codes (Figure 5-17). The mod 2 sum is developed in a simple on-chip exclusive/or circuit. The doppler shift term is derived from a Costas loop, with the IQ multipliers and part of the VCXO on-chip and the remaining circuitry external. After the first mixer, the signal is at $6\frac{1}{2} f_0$ and is modu-

lated by the P code (if the signal was originally modulated by the C/A code) or the C/A (if the signal was originally modulated by the P code). This code is removed and the signal downconverted to $1.5 f_0$ in the second mixer. At the mixer output, despreading is completed and the SNR gain is realized by bandlimiting in an off-chip 2 kHz bandwidth bandpass filter. The final conversion to quadrature versions of the baseband signals is accomplished in the last pair of mixers. The quadrature $1\text{-}1/2 f_0$ local oscillator signals are derived from the divide-by-4 output of the $6 f_0$ synthesizer input.

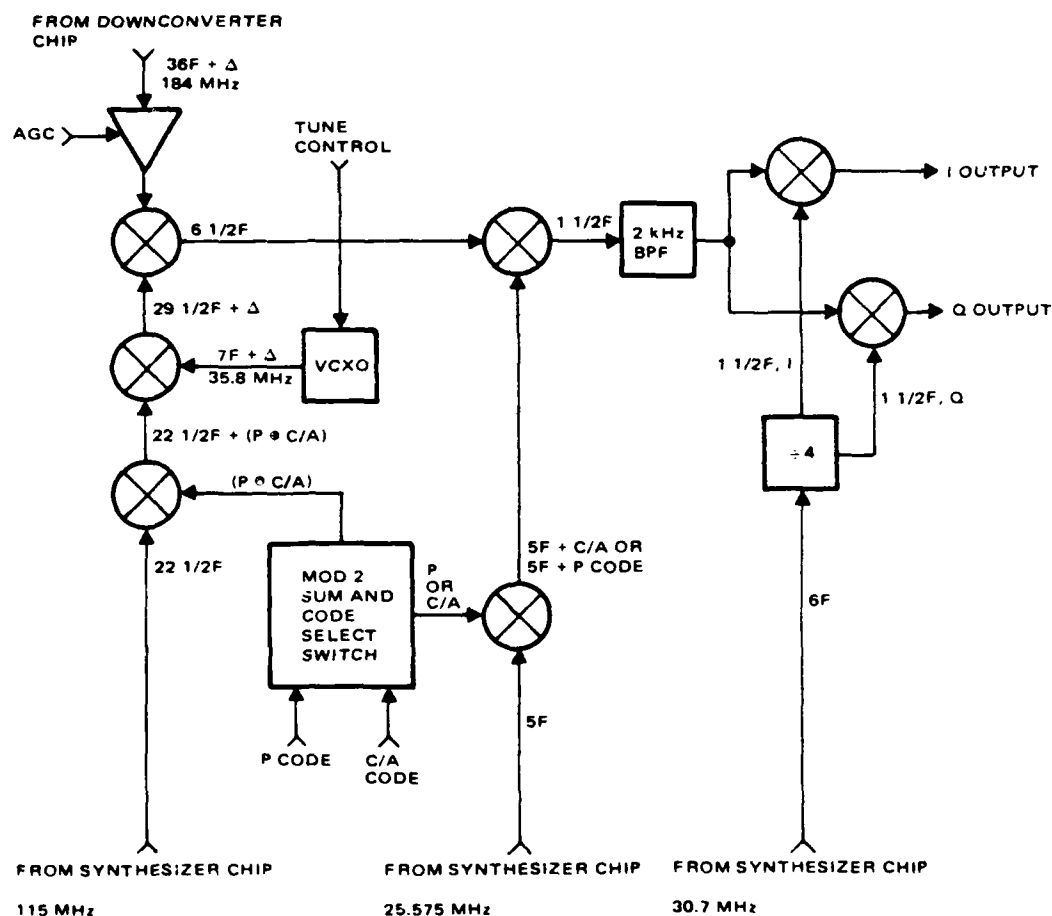


Figure 5-17. IF Correlator/Demodulator Chip

5.2.4.3 GPS Frequency Synthesizer

The frequency synthesizer chip provides reference signals to two GPS chips and portions of the GPS receiver. The reference signals are phase coherent to the 5.115 MHz (f_0) receiver reference source, and are derived from two phase locked loops (Figure 5-18). Four (of the five) required outputs are integer submultiples of $90 f_0$, and are derived from a single phase locked VCO. The remaining $68 f_0$ output drives the D/C chip and has a separate phase locked loop.

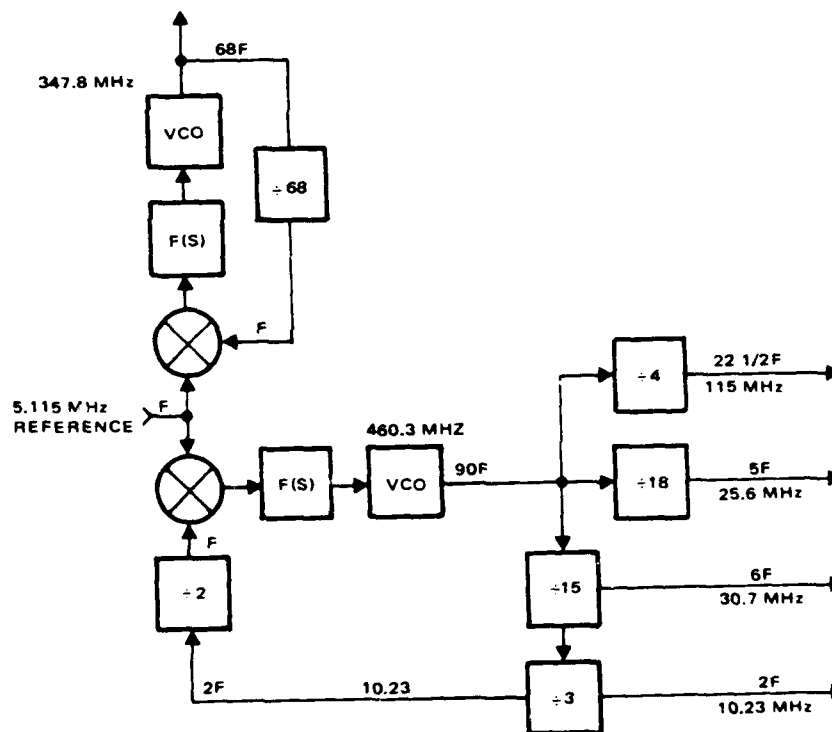


Figure 5-18. Frequency Synthesizer Chip

The technical risks associated with this chip do not involve operating frequency (TRW's first RF LSI chip was a 500 MHz Costas loop), but rather uncertainty regarding VCO phase noise performance. Preliminary calculations based on minor modifications of a current VCO design show that the 2^0 rms specification can be easily satisfied if an off-chip tuning varactor

is used. However, for a production quantity of synthesizer chips, such an off-chip element would be a significant cost factor. Therefore, TRW proposes a fully monolithic approach to these VCOs, provided that detailed design analysis indicates sufficient phase noise specification margins.

5.2.4.4 GPS Downconverter Chip

This chip amplifies the received signal at either 1227 or 1575 MHz, selects one of these signals and downconverts it to 184 MHz, and reduces the input 90 dB dynamic range to a 15 dB output range. Figure 5-19 shows TRW's preliminary schematic for this chip. The input amplifier has 30 dB maximum gain, 45 dB AGC range, and a 3 dB bandwidth around both 1227 and 1575 MHz of at least 30 MHz. The first mixer either downconverts the 1575 MHz signal to 1227 MHz or passes through the 1227 MHz signal, depending

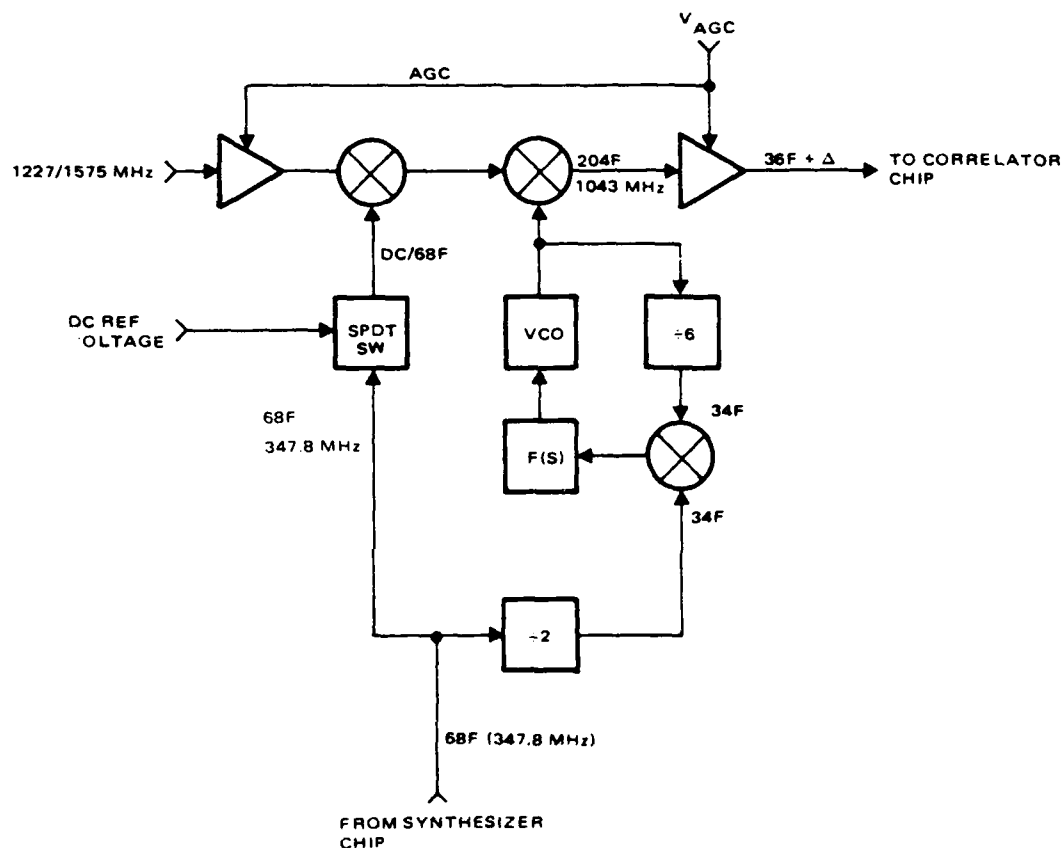


Figure 5-19. GPS Downconverter Chip

upon the command given to the SPDT switch. The dc reference voltage supplied to the first mixer, in the event that the 1227 MHz signal is selected, will be adjusted to compensate for any difference between the composite gain of the amplifier/first mixer to the 1575 and 1227 MHz signals.

The second mixer is employed to downconvert the 1227 MHz first mixer output to 184 MHz. The composite gain of the two mixers is set at 0 dB by adjustment of the amplitude of the 1043 MHz local oscillator. The local oscillator is phase locked to the 347.8 MHz signal from the frequency synthesizer chip by means of a simple frequency divider phase locked loop (PLL). It seems easier to use a divide-by-3 in the PLL rather than the divide-by-6 and the divide-by-2 at the 347.8 MHz input. However, attempting an odd integer divider at >800 MHz proves riskier than using an even integer divider which can begin with a divide-by-2. This even integer divider has been successfully demonstrated to at least 1500 MHz. Thus, although somewhat more complex, the even integer approach to the PLL results in lower risks and higher yields. Finally, the IF amplifier has a 35 dB maximum gain with 30 dB AGC range.

5.2.4.5 HF/VHF/UHF Frequency Converter/Amplifier

This chip (Figure 5-20) converts any input signal in the range of 2 to 500 MHz to a 70 MHz output frequency. It consists of three stages, and can be configured to perform single, double, or triple conversion and/or used as an RF/IF amplifier.

The first stage has a low noise wideband AGC amplifier at the front end followed by a mixer. The second stage reverses this order, with the mixer followed by an AGC amplifier. Switches are used to select one of two possible LO inputs for these two stages. Both mixer outputs are externalized to allow for off-chip filtering. The LO inputs can also be dc and can cause one or both stages to operate as wideband AGC amplifiers. The final stage of the chip is used to form two quadrature signals (I and Q) for demodulation. The quadrature signals are generated by mixing with the LO signals which are 90° out of phase. The 90° LO phase shift is obtained internally to the chip through a divide-by-4 circuit. Thus, the last LO input signal frequency must be four times greater than the desired frequency.

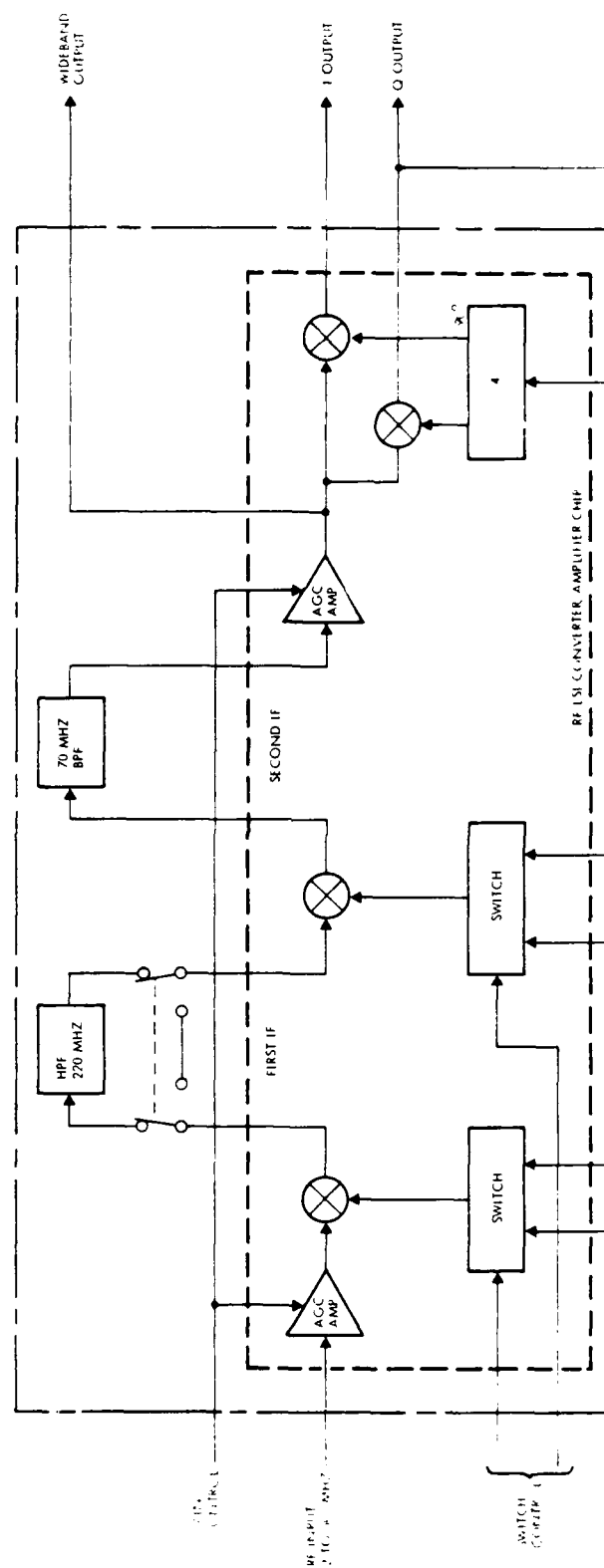


Figure 5-20. RF LSI Frequency Converter/Amplifier Chip

5.2.4.6 Quadrature Modulator

The quadrature modulator chip permits data to be modulated onto a 70 MHz carrier. The circuit schematic for this chip is shown in Figure 5-21. Beginning at the left, an input frequency of 280 MHz is divided-by-4 to provide quadrature versions of the 70 MHz signal to be modulated. I and Q data modulation is applied to analog multipliers whose outputs are summed. The resulting signal is either amplified for direct transmission at 70 MHz or is frequency translated by a third analog multiplier to the desired transmit frequency.

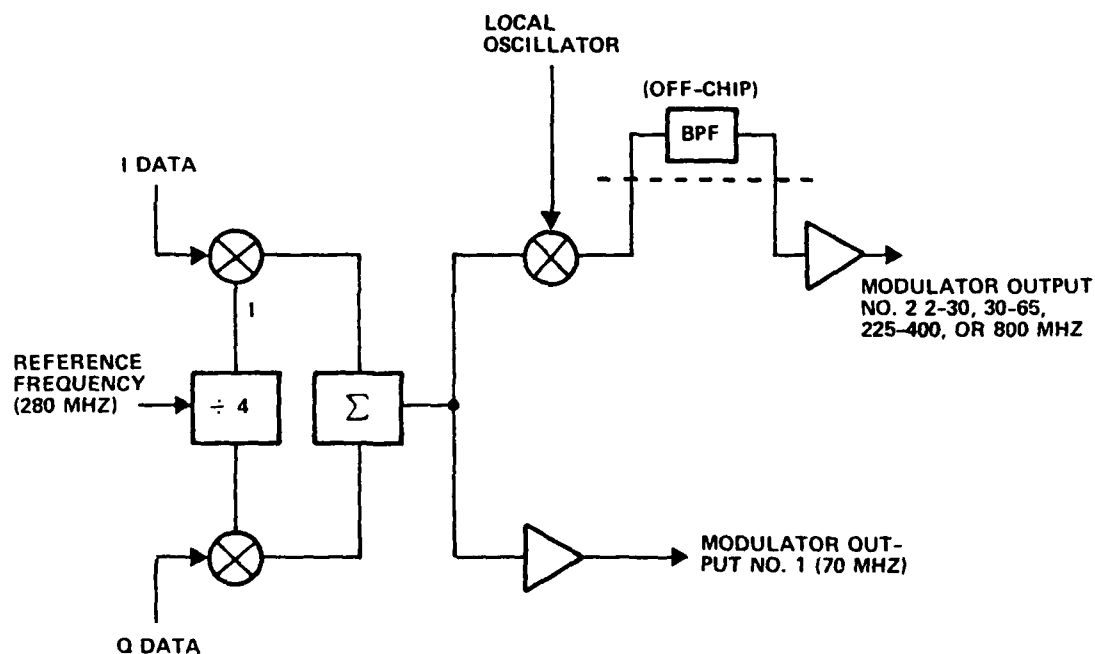


Figure 5-21. Quadrature Linear Amplitude Modulator

5.2.4.7 General Purpose Frequency Synthesizer

The MFBARS system includes 11 subsystems in which a fixed frequency source is required. Each of these subsystems requires a different frequency, but all are coherent with the system reference. Therefore, each can be implemented as a divider-type phase locked oscillator, with the divide ratio hard-wired as appropriate for each application.

5.3 FREQUENCY SOURCES

The frequency source contains three major elements: a stable, low noise crystal reference oscillator; a fixed frequency generator with eleven coherently derived outputs from the crystal reference; and eleven programmable frequency synthesizers. A block diagram of this frequency generation hardware is shown in Figure 5-22.

The frequency standard for the MFBARS system is the reference oscillator operating at 5.115 MHz. All frequency source outputs are coherent with this reference. The requirements for this oscillator are contained in Table 5-7. Commercially available oscillators developed for GPS programs (such as the FE-2099A) are planned for MFBARS use. Current work in the frequency control community on reduction of g-force effects for GPS weapons delivery/avionics should be applicable to MFBARS by the time it reaches the qualification test phase.

The fixed frequency generator provides eleven output frequencies phase-locked to the 5.115 MHz reference oscillator. Table 5-8 shows the required frequencies and other performance requirements; spurious requirements vary depending on usage. Power level requirements are consistent with deriving RF LSI frequency conversion chips and account for n-way divisions.

The programmable frequency synthesizers provide agile tuning local oscillators for the multimode front end/exciter circuits. The synthesizer requirements are shown in Table 5-9. To be compatible with TACAN, the six L-Band synthesizers cover the JTIDS/TACAN/IF range in 1 MHz steps (with a 70 MHz IF offset). Five microsecond settling permits all of the synthesizers to operate in the JTIDS fast hop mode or for shared JTIDS-acquisition/TACAN-operation. The UHF/VHF synthesizers cover the 225 to 400 MHz UHF range in 5 KHz steps with a 70 MHz IF offset. Using fixed sources to up-convert to UHF, HF and VHF are handled with the same LO. Settling, at 200 μ sec, is compatible with UHF and VHF hopping signal sets.

The application RF LSI to put a phase-locked loop into monolithic chips is the design approach selected for implementing both the fixed sources and the programmable frequency synthesizers. The bulk of the loops will be implemented using a general purpose two-chip set (Figure 5-23). For the

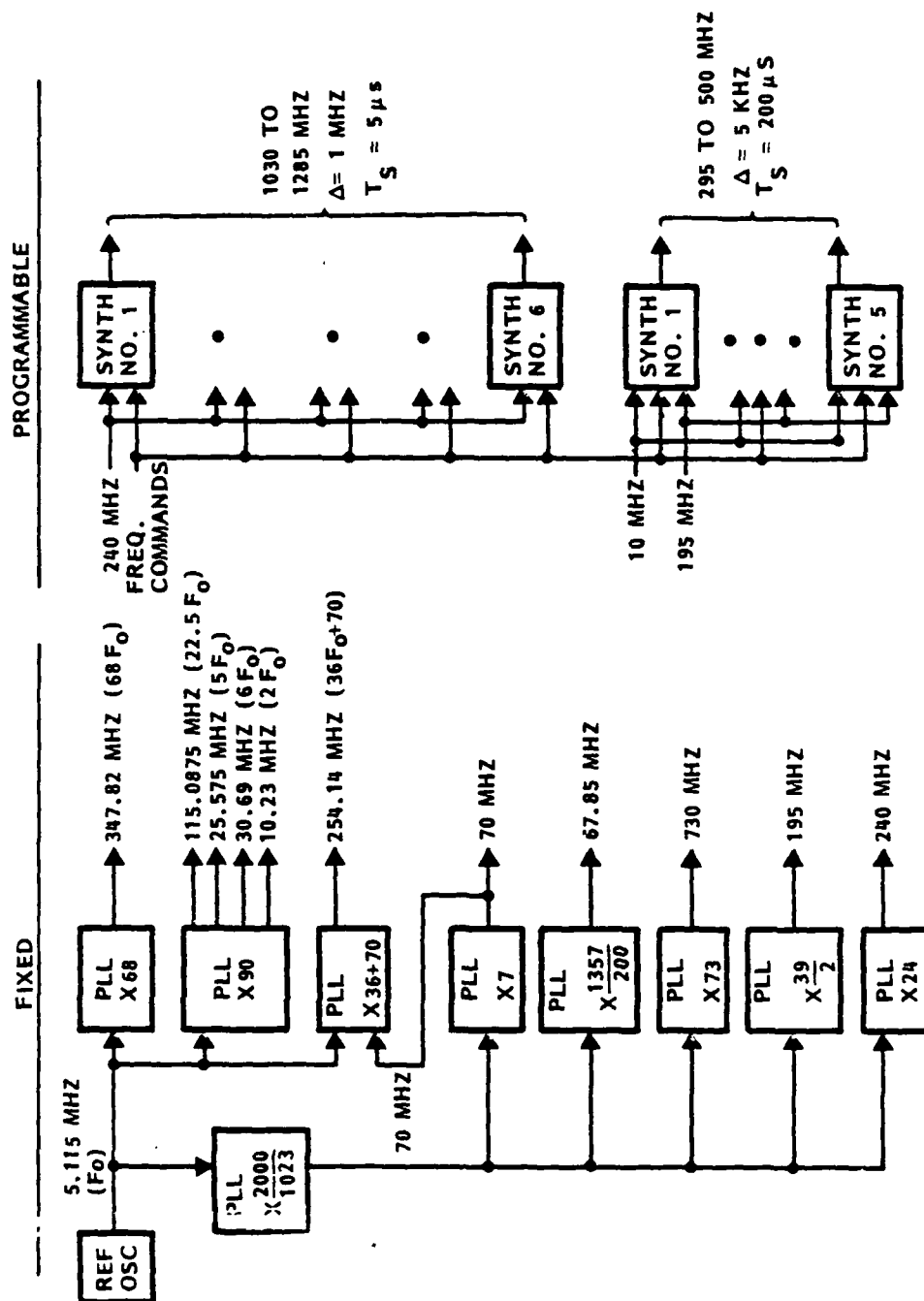


Figure 5-22. MFBARS Frequency Sources

Table 5-7. Reference Oscillator Requirements

FREQUENCY	REQUIRED (5.115 MHZ)	FE-2099A (5.115 MHZ)
STABILITY (SQUARE ROOT OF ALLEN VARIANCE)		
MEASUREMENT INTERVAL		
>1000S	10^{-7}	
100	10^{-10}	
10	10^{-9}	1.4×10^{-12}
5	6.7×10^{-10}	1.4×10^{-12}
1	2.5×10^{-11}	1.6×10^{-12}
0.5	6.7×10^{-9}	2.0×10^{-12}
0.1	6.7×10^{-10}	4.9×10^{-12}
0.063	4.0×10^{-10}	6.5×10^{-12}
0.010	2.5×10^{-9}	3.3×10^{-12}
WARM-UP	TBD	2×10^{-8} 5 MIN
AGING	TBD	2×10^{-11} /DAY
OUTPUT POWER	TBD	+3 DBM
WEIGHT	TBD	8 OZ
SIZE	TBD	3.2 X 1.6 X 1.6 IN.

Table 5-8. Fixed Source Requirements

LOOP	X73	X68	X36 + 70	X24	X19.5	X7	X $\frac{1357}{2000}$	X $\frac{2000}{1023}$
FREQUENCY (MHZ)	730	347.82	254.14	240	195	70	67.85	10
SPURIOUS (DBC)	-60	-60	-60	-80	-80	-80	-80	-90
POWER (DBM)	+3	+3	+3	+17	+14	+17	+3	+14

Table 5-9. Programmable Frequency Synthesizer Requirements

PARAMETER	L-BAND	UHF/VHF
FREQUENCY	1030 TO 1285 MHZ	295 TO 470 MHZ
STEP SIZE	1 MHZ	5 KHZ
SETTLING TIME	5 μ SEC	200 μ SEC
SETTLING ERROR	12 KHZ	5 DEG
SPURIOUS	-60 DBC	-60 DBC

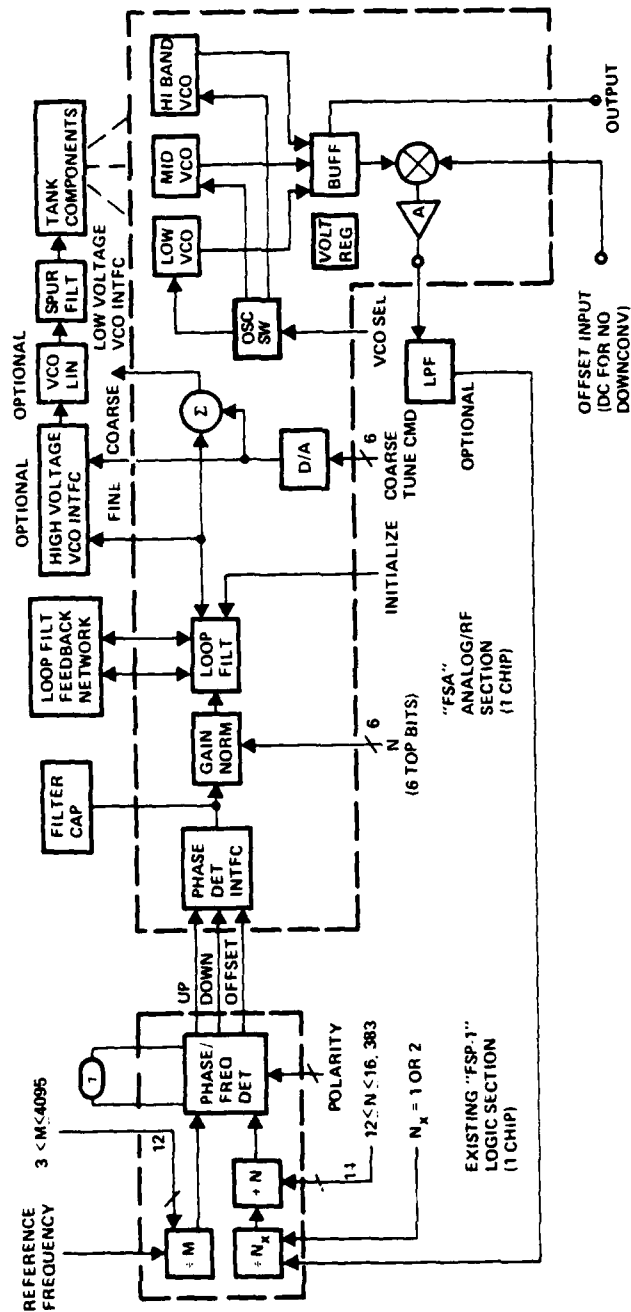


Figure 5-23. General Purpose Synthesizer Chip Set

X90 and X68 loops supplying GPS frequencies, a unique two-chip set is envisioned (Figure 5-24).

The general purpose two-chip set consists of a digital chip and an analog/RF chip. The digital chip is an existing high-speed bipolar LSI device designed and built with company funding and currently used on several high reliability programs. The device, designated FSP-1, is illustrated in Figure 5-25, along with some key performance features. Figure 5-26 shows a typical operating curve for the 750 MHz feedback divided-by-N counter. The FSP-1 phase detector/frequency discriminator is a dual R-S flip-flop type with a sawtooth phase error function as shown in Figure 5-27. The external delay line seen in Figure 5-23 is used to generate a pulse (OS) to slightly offset the phase detector and avoid nonlinearities. The OS pulse permits pulse cancellation to achieve low sample rate spur leakage, allowing wider loop bandwidths and faster settling without sacrificing spur performance.

The analog/RF chip (Figure 5-28), presently designated the FSA-1, is currently under development for the Naval Air Development Center (NADC). It contains analog and RF circuits for multipurpose use in C³NI systems such as TIES and MFBARS. The digital phase detector signals from the FSP-1 are converted to analog phase error signals in the phase detector interface circuit. An external filter capacitor is used to reduce phase detector spur leakage. The filtered phase error signal is processed by a gain normalizer which compensates the loop gain changes for the six most significant bits of the feedback divider. This normalized phase error signal is processed by an active integral plus proportional type loop filter. The filter's passive components are external for maximum flexibility. An initializing capability is provided for centering the fine tune signal during fast acquisition (when coarse tuning the VCO with the on-chip digital-to-analog converter). Since varactor tuned VCOs often require a high tuning voltage, the VCO interface circuit is off-chip (two transistors). For low-voltage applications (narrow tuning), an on-chip VCO interface is also provided to combine coarse and fine tuning signals.

The RF section of the FSA-1 chip contains three voltage controlled oscillator circuits which cover the 10 to 2000 MHz range. For flexibility and low noise (high Q) performance, the oscillators are designed for off-

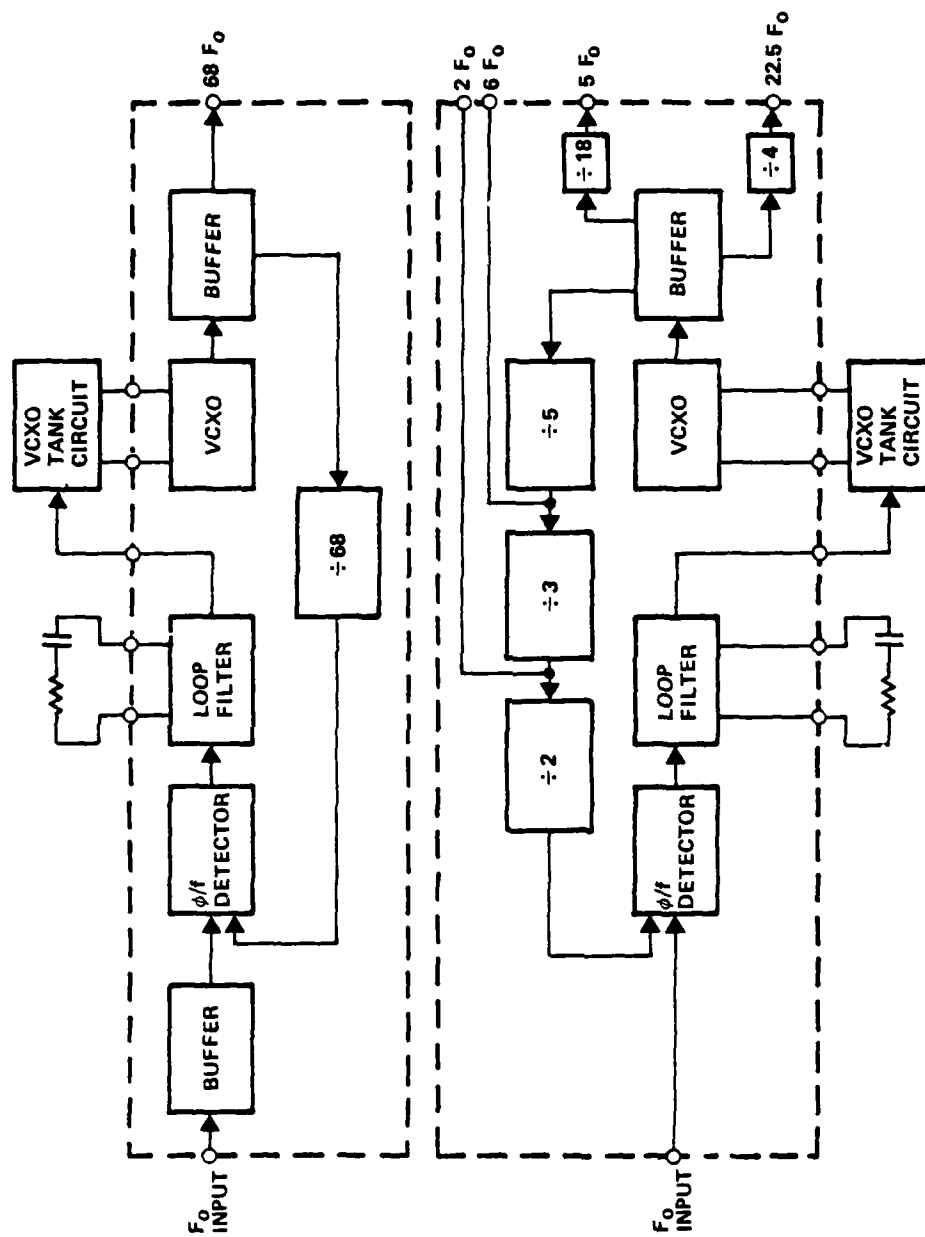


Figure 5-24. GPS Frequency Source Chip Set



PRESCALER FREQUENCY: 1500 MHZ
RATIO N_x : 2 OR BYPASS

PROGRAMMABLE DIVIDER FREQUENCY: 750 MHZ
RATIO N: 12 TO 16383

REFERENCE DIVIDER FREQUENCY: 200 MHZ
RATIO M: 3 TO 4095

DIVIDER INPUTS: 0 DBM, 50 Ω , VSWR < 1.5
PROGRAMMING INPUTS: TTL
OUTPUTS: ECL
PHASE DETECTOR RANGE: $\pm 2\pi$
FREQUENCY ACQUISITION: AUTOMATIC
POLARITY: REVERSIBLE
POWER: +5 V DC; 1.5 WATTS
SIZE: 64 LEAD FLAT PACK, 7/8 INCH SQUARE

FEATURES

- UNIQUE PERFORMANCE (TYPICAL $\pm N$ TO 1000 MHZ)
- EASY TO DESIGN WITH
- EASY TO INTERFACE: 50 Ω RF, TTL, ECL, +5 V
- PROGRAMMABLE DIVIDERS USABLE INDEPENDENTLY
- LOW POWER VERSIONS:
 - X—OMITS PRESCALER; 1.0 WATTS
 - Y— $\pm N < 4096$, < 200 MHZ; < 0.7 WATT

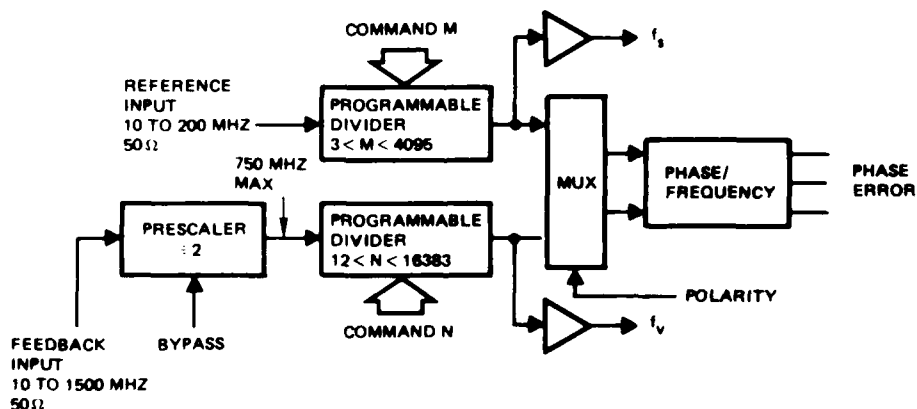


Figure 5-25. Monolithic Frequency Synthesizer Logic (FSP-1)

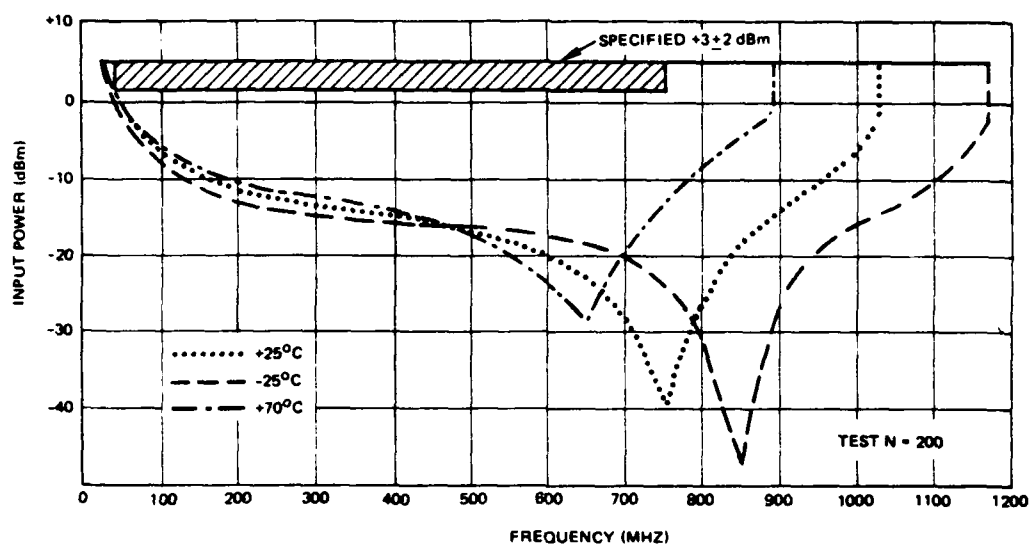
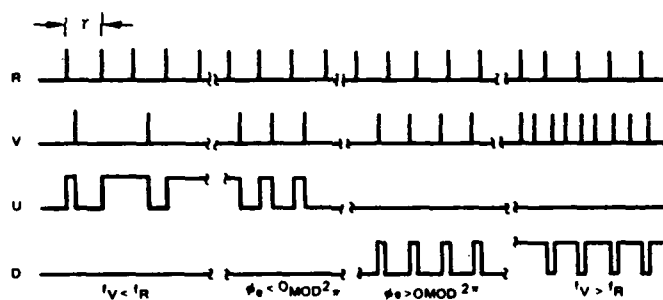
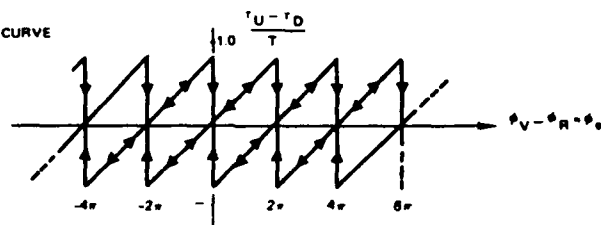


Figure 5-26. FSP-1 Counter Input Sensitivity vs Frequency (Typical)

b) TIMING



c) PHASE ERROR CURVE



d) DISCRIMINATOR CURVE

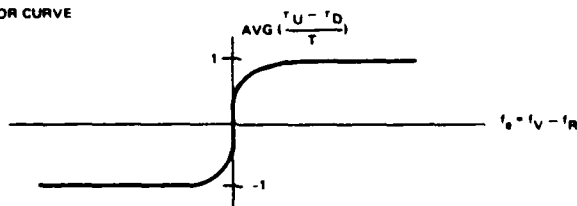


Figure 5-27. Phase/Frequency Detector

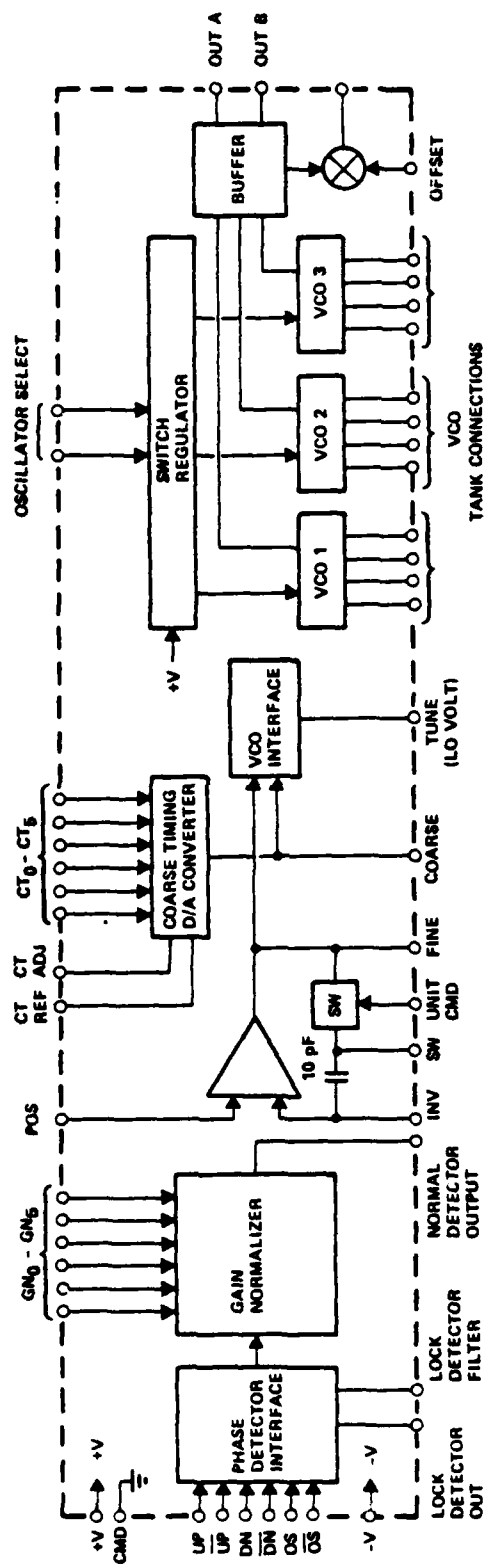


Figure 5-28. Interconnect Diagram for FSA-1 Synthesizer RF/Analog LSI

chip tuning. The low band oscillator is a feedback type suitable for use with L-C, bulk crystal, or SAW resonators. The SAW application would require an added amplifier stage (possible on-chip if space permits). The high band oscillators are negative impedance types optimized for the bands of operation. The oscillators are switched and buffered to provide adequate output power and load/spur isolation. A portion of the VCO signal drives a downconverter mixer (active balanced modulator) which is dc biased for applications not requiring conversion. The mixer output is fed out for filtering, and processed by an amplifier/limiter to drive the feedback divider. Power supply voltage regulation for the VCOs will also be provided.

The chip specification goals are given in Table 5-10. The FSP/FSA combination will be capable of a vast variety of frequency synthesis applications. The chip set capability goals are shown in Table 5-11. All MFBARS sources except the GPS reference loops fall within the realm of this chip set. Due to the large set of GPS applications (other than MFBARS), the GPS loops are excluded and a specially tailored, separate chip set development is anticipated.

The FSP/FSA chip set can be used and packaged in various ways to form single and multiloop synthesizers. One approach suited to single-loop applications such as frequency operation can be seen in the module described below. It is one of two approaches to be developed under the NADC contract to demonstrate the FSP/FSA chip set. The second approach, a JTIDS synthesizer, is also described below.

The single loop application is to be demonstrated for the TIES system which uses a frequency division multiplex (FDM) bus synthesizer to connect the mission RF front-end hardware to the digital signal processing frequency conversion subsystem. There are typically ten such synthesizers whose performance requirements for the synthesizer are given in Table 4-12. The single loop configuration is illustrated in Figure 5-29.

Design details determined the predicted size and power dissipation for this configuration. The first of the two LSI chips forming the synthesizer core, the FSP-1, contains the logic functions (divided-by-M, divided-by-N, and phase detector) of the loop. This chip has been successfully applied

Table 5-10. Minispecification for FSA Chip (Preliminary)

Phase detector interface	
Gain	$3/2\pi$ volts/radian ($\pm 1\%$)
Gain normalizer	
Word size	6 bits
Coding	Binary
Maintains	Constant = $K_o/N \pm 0.2$ dB (not included truncation error)
Loop filter of amp	
Input offset voltage	10 mV maximum
Input resistance	0.5 megohms minimum
Large signal voltage gain	25 V/mV minimum
Output swing	6 V _{p-p} minimum
Output resistance	50 ohms maximum
Unity gain (open loop)	12 MHz minimum
Loop filter initialize	
Loop filter output error	0.1 V maximum
Delay time	100 nsec maximum
Coarse tune D/A	
Current range	20 mA maximum
Coding	Binary
Word size	6 bits
Accuracy	$\pm 1/2$ LSB
VCO	
Frequency	10 MHz to 2000 MHz
Bandwidth	Up to octave
Power	+10 dBm minimum
Downconverter	
Offset frequency	10 MHz to 2000 MHz
Power	+3 ± 2 dBm
IF output	10 MHz to 1500 MHz
Power	+3 ± 2 dBm

Table 5-11. Synthesizer Performance Goals

Parameter	Goal
Output frequency	10 to 2000 MHz
Bandwidth	Up to octave
Step size*	1000 Hz at 20 MHz
Settling time**	5 μ sec to 100 msec
Settling error	12 kHz
Spurs	-80 dBc
Noise**	5 degrees
Power	+11 $\pm$ 2 dBm
Offset frequency	10 to 2000 MHz
Power	-10 $\pm$ 3 dBm
Reference frequency	5 to 250 MHz
Power	+2 $\pm$ 3 dBm
DC power	2.5 W
Parts	25 discretes
* Multiple loop configurations can provide steps as small as 0.1 Hz or lower. ** Depends on step size of individual loop.	

Table 5-12. TIES FDM Bus Synthesizer Requirements

Parameter	Requirement
Frequency	300 to 500 MHz
Bandwidth	200 MHz
Step Size	1 MHz
Settling Time	200 μ s max to within $\pm$ 5 degrees
Spurious	-80 dB — carrier max over tuning band
Short-Term Stability	1 degree rms max over 22 msec interval
Long-Term Stability	Phase-locked to external 10 MHz signal
External Programming	Internal latch, TTL commands

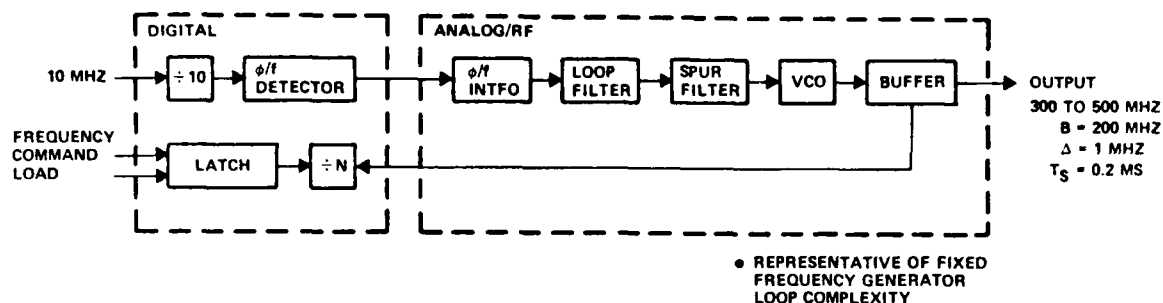


Figure 5-29. TIES FDM Bus Synthesizer

to over seven synthesizer designs and has been tested extensively. It is currently in limited production for several on-going programs. One of the chip's key features is its versatility. Another is the large range of divider moduli at high input frequencies. For applications which require minimum power, metal mask and resistor value changes can eliminate unneeded functions and tailor speed vs power performance. The resulting power level for a tailored mask option is 566 mW. Without mask changes, but with increased resistance values, the power would be 700 mW.

The analog/RF functions are performed by the FSA-1 chip. The chip block diagram is shown in Figure 5-28. Again, chip power dissipation depends on resistance values and metal mask circuit deletions or supply wiring (if extra V_{CC} pins are used). For the FDM bus synthesizer, only the phase detector interface, loop filter, and VCO/buffer circuits are required. This combination consumes about 350 mW.

The latch functions are performed using 54LS377 and 54LS74 chips. These provide 10 latch bits/108 mW. Thus, the total power required for this application is:

FSP-1 ()	566 mW
FSA-1 ()	350 mW
Latches	108 mW
1024 mW $\approx$ 1.0 watt	

Considering the wide tuning bandwidth and high frequencies generated, this is a very low power level.

Miniaturization is another key goal in applying the FSP/FSA chip set. The ultimate production configuration can be developed by examining the required circuits. The digital circuits are shown in Figure 5-30. The FSP-1 requires bypass capacitors for V_{CC} , internal references (CVR1), and the internal 50-ohm input terminations (CREF and CSYN). Use of a hybrid packaging technique to combine the latch MSI/SSI and the capacitors with the FSP-1 is cost effective and reduces external discretes to a minimum. This package will be 1.1 x 0.9 x 0.2 inches and will dissipate 674 mW.

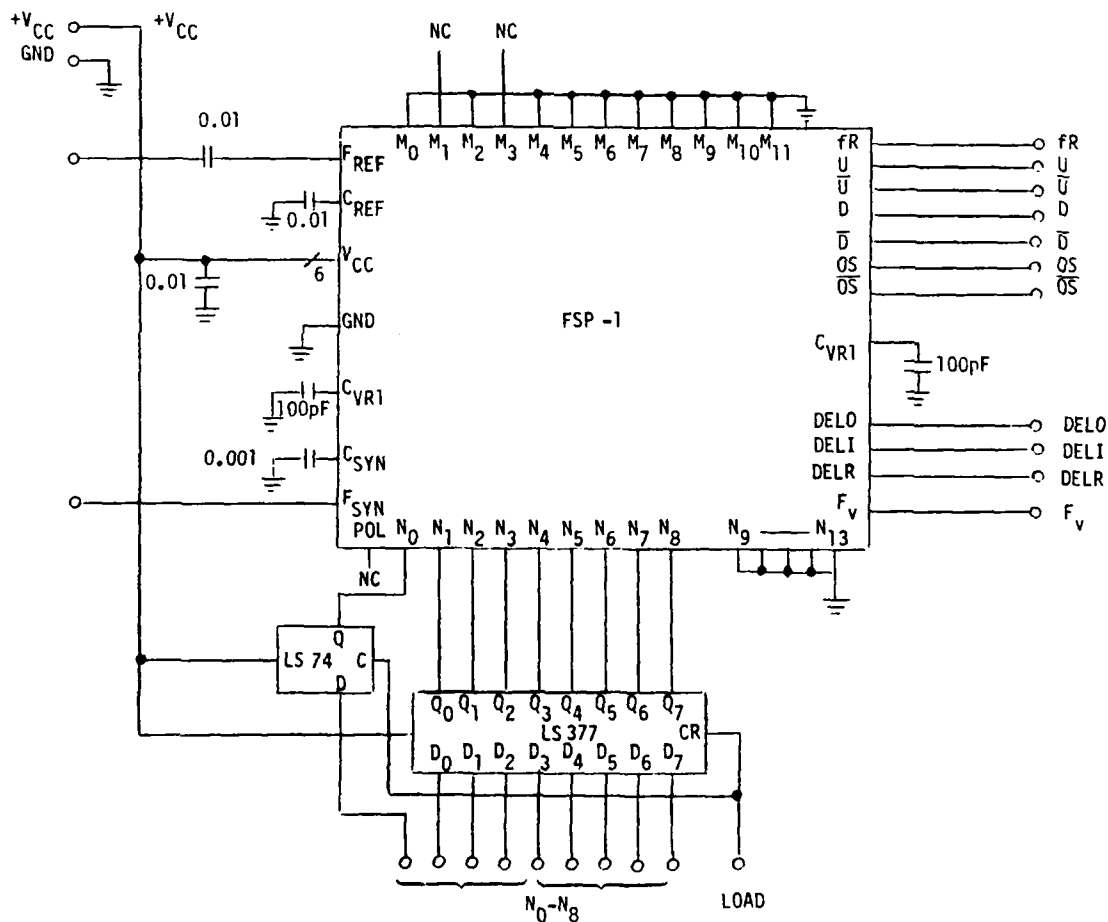


Figure 5-30. Digital Hybrid Schematic Diagram

The analog/RF circuits are shown in Figure 5-31. The FSA-1 chip requires power supply bypass capacitors, series coupling capacitors for the signal output, a voltage reference source bypass (REF), an oscillator regulator bypass (D), and a lock detector filter (LOCK FILT). In addition, the loop filter components, spur filter, and VCO tank components are off-chip. These components, which vary according to application, are shown in a separate hybrid package. This separation keeps the parts count per hybrid low and improves application flexibility. The FSA chips package is 0.8 x 0.95 x 0.2 inch and dissipates 350 mW. The external hybrid (Figure 5-32) is 0.5 x 0.8 x 0.2 inch and dissipates negligible power. This small, single loop synthesizer module (Figure 5-33) is representative of the simple loops used in the frequency generator.

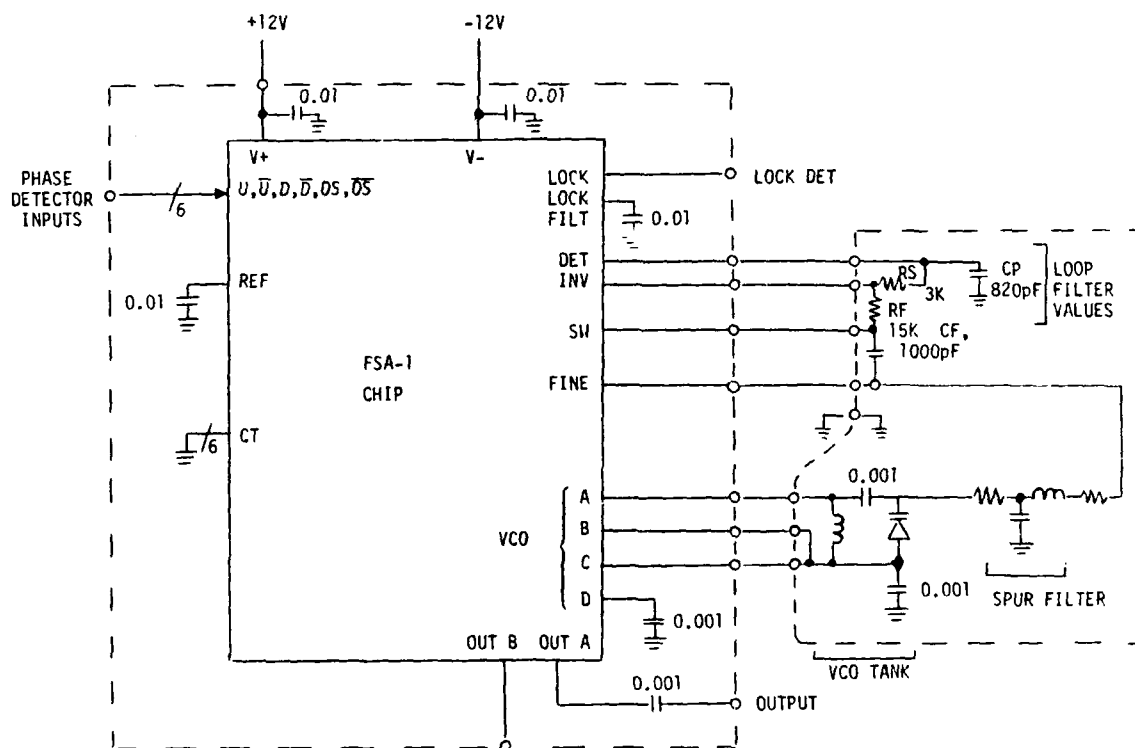


Figure 5-31. Analog Hybrid and Filter/Tank Hybrid

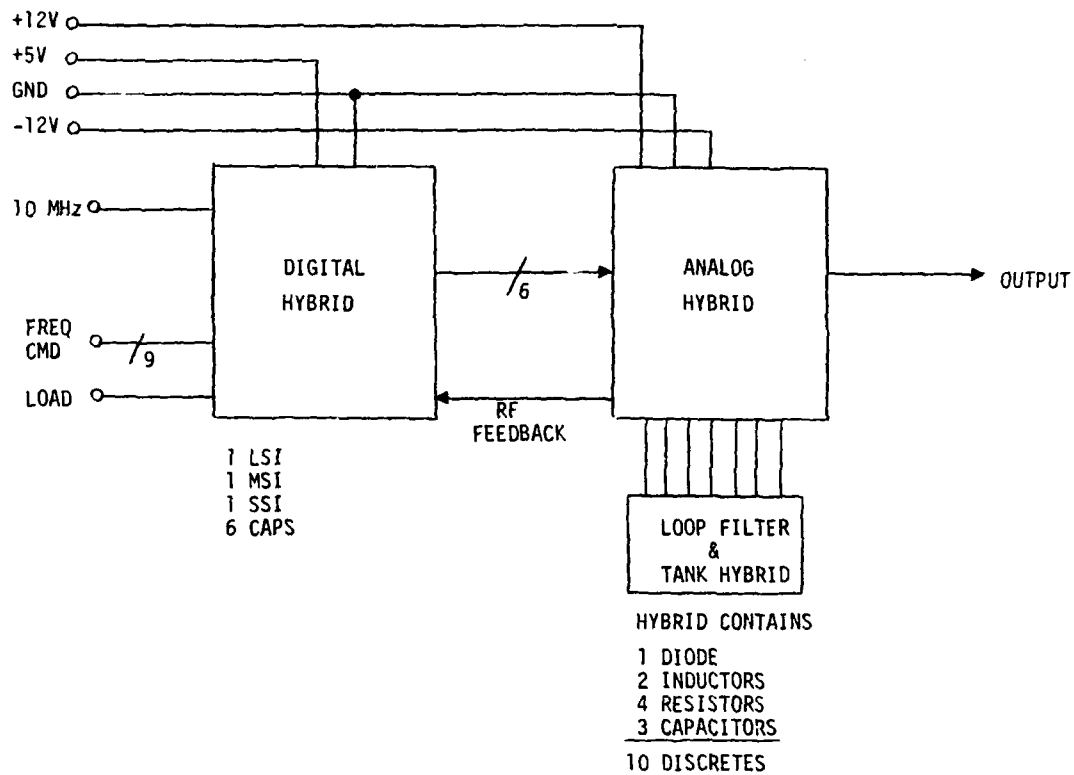


Figure 5-32. TIES UHF Bus Synthesizer Card Schematic

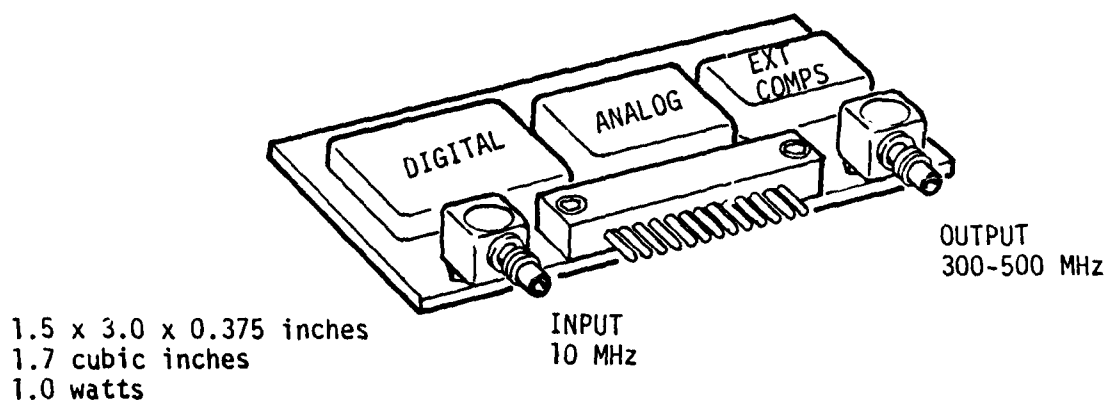


Figure 5-33. TIES FDM Bus Synthesizer

The JTIDS MFBARS synthesizers will be nearly identical to the synthesizer to be developed for NADC (due August 1981). The requirements for this application are given on Table 5-13.

Table 5-13. JTIDS Fast Hop Synthesizer Requirements

Parameter	Requirement
Frequency	1030 to 1285 MHz (70 MHz IF assumed)
Bandwidth	255 MHz
Step Size	1 MHz (TACAN/DME Compatible)
Settling Time	5 μ s to within 12 KHz
Spurious	-60 dB: carrier
Short Term Stability	—
Long Term Stability	Phase locked to external 10 MHz signal
External Programming	Internal latch, TTL commands

These requirements can be met using the configuration shown in Figure 5-34. A vernier architecture is employed to provide fast settling with narrow step sizes; fine steps are achieved by stepping two loops together. The net step size is the difference between the two individual loop sizes. A third loop is used to generate an offset signal to the lower loop, and for division to obtain the vernier step size frequencies. A command decoder provides the vernier tuning, giving external 8-bit binary tuning command.

In this application, the FSP/FSA chip set is used for each loop as in the UHF bus synthesizer. For the fast settling loops, however, the required analog VCO control circuits are more complex due to the faster settling requirement. In addition, the L-Band VCO frequency requires the tank circuit be adjacent to the FSA chip to minimize parasitic effects.

The analog/RF functions are performed with a single, larger hybrid. The schematic for this L-Band RF/analog section is shown in Figure 5-35. This hybrid package requires 1.1 x 1.2 x 0.2 inches and dissipates 1.0

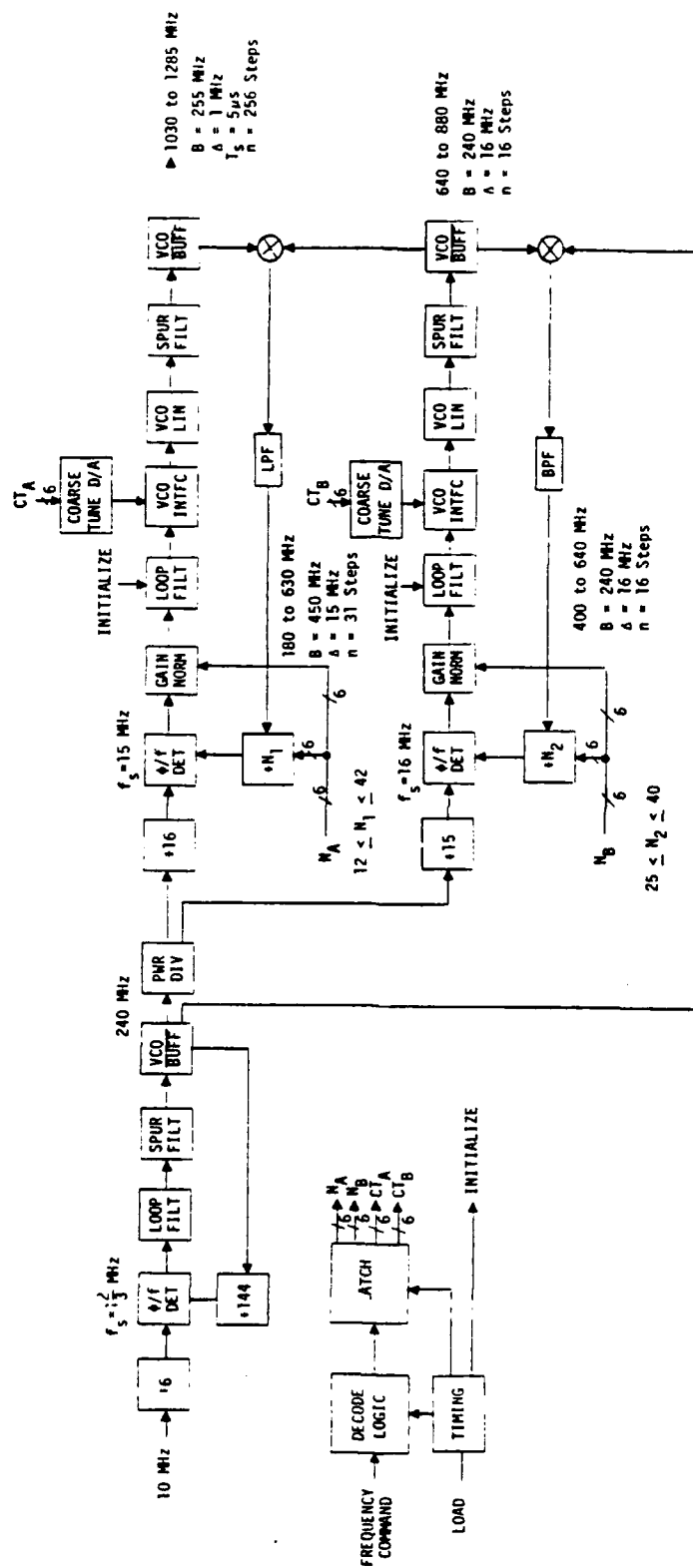


Figure 5-34. JTIDS Hopping Synthesizer



watt. In this application the fast settling loops require a higher feedback divider frequency (650 MHz). Thus, the dc power requirement is slightly higher (650 mW).

The command logic hybrid contains the vernier decode logic, the initialize timing logic, and a command latch. The decode logic is power-gated to reduce consumption. The timing logic controls this gating and latch loading and generates the initialized pulses. This circuit uses off-the-shelf components and requires 500 mW. It is included in a 0.9 x 1.1 x 0.150-inch hybrid.

The reference loop is similar to the bus synthesizer, except that the VCO frequency is fixed and slightly lower. In addition, the external tank and filter components are packaged with the FSA chip in a 1.1 x 1.2 x 0.2-inch hybrid which dissipates 350 mW.

Thus, the power budget for the JTIDS hopper is as follows:

Reference Generator

Digital	566 mW	
Analog	350 mW	916 mW

Vernier Loop 1

Digital	650 mW	
Analog	1000 mW	1650 mW

Vernier Loop 2

Digital	650 mW	
Analog	1000 mW	1650 mW

Command Logic

500 mW	<u>500 mW</u>
	4716 mW

The overall schematic diagram is shown in Figure 5-36.

The seven hybrids and two filters are packaged on a single 4 x 5-inch multilayer printed circuit board as shown in Figure 5-37. Occupying just 12 cubic inches and dissipating under 5 watts, this synthesizer is a dramatic advance compared to currently available units.

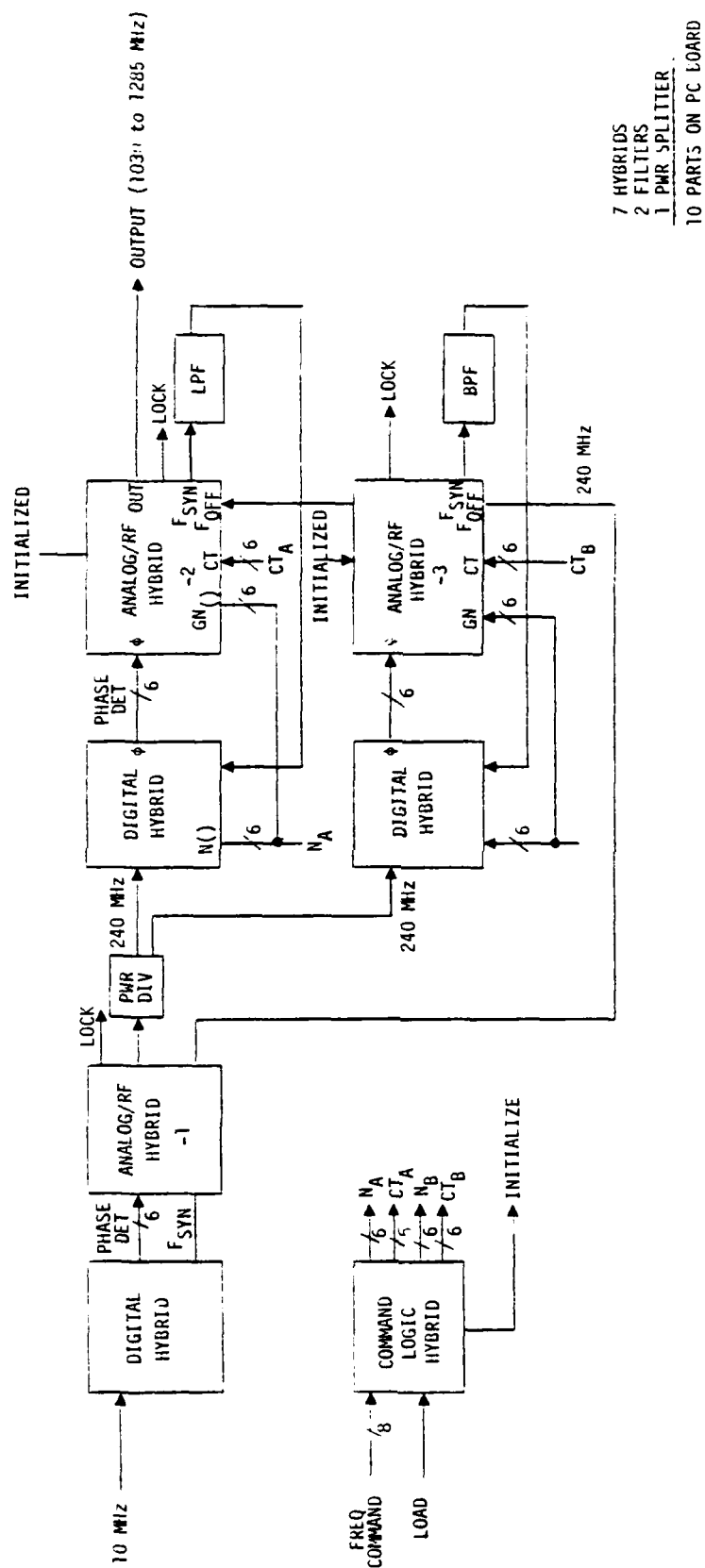


Figure 5-36. JTIDS Fast Hop Synthesizer Interconnect

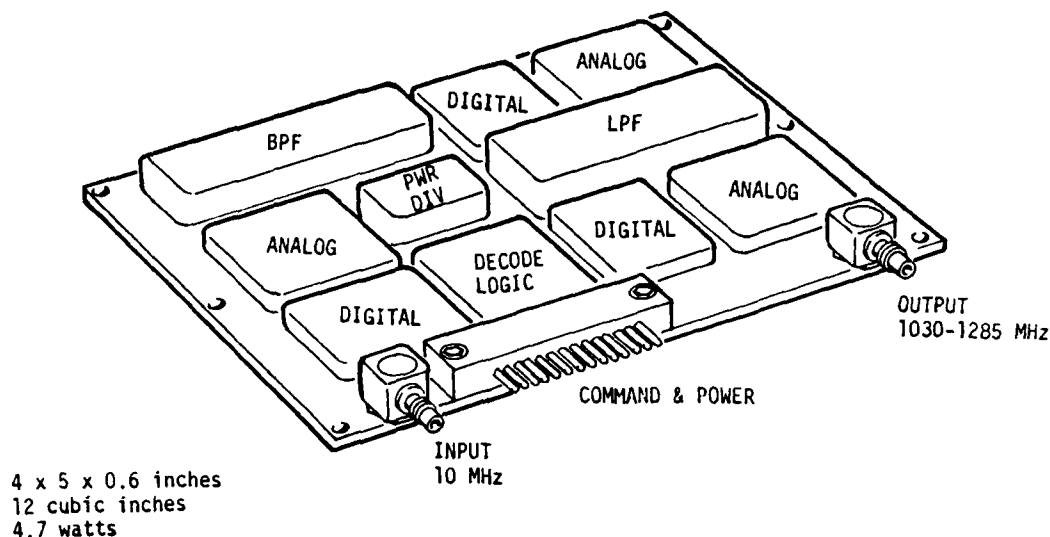


Figure 5-37. JTIDS Frequency Hop Synthesizer

For MFBARS, a 240-MHz reference signal will be used, permitting the 240-MHz loop components to be deleted from the module. The resulting dc power is thus under 4 watts per loop.

The UHF MFBARS synthesizers will employ the FSP/FSA chip set and share versions of the hybrids discussed above. The UHF synthesizer requirements are shown in Table 5-14.

The configuration block diagram is shown in Figure 5-38. The 5-kHz step size and 200 μ sec settling combination cannot be met in a single loop design. Therefore, a divide and mix approach is used with one loop selecting 350 500-kHz steps and another selecting 100 500-kHz coarse steps (divided by 100 to obtain fine 5-kHz steps). The divided fine step signal is added to the coarse steps in a summing loop. The sum loop VCO is slaved to the coarse step loop to prevent the sum loop feedback from exceeding desired limits. The size of this synthesizer will be similar to the JTIDS synthesizer, approximately 4.5 watts and 10 cubic inches.

Table 5-14. UHF Synthesizer Requirements

<u>Output</u>	
Frequency	295.000 to 470.000 MHz
Step Sizer	5 kHz
Number of Steps	35,000 (16 bits)
Power	-10 dBm
Settling Time	200 μ sec to ± 2 degrees
Spurious	-60 dBc maximum
Short-Term Stability	0.5 Hz or 2.38^0 in 22 μ sec period over 960 to 2.5 kHz; 5^0 max integrated 10 Hz to 10 MHz
<u>Reference Input No. 1</u>	
Frequency	10 MHz
Power	+0 dBm
<u>Reference Input No. 2</u>	
Frequency	240 MHz
Power	-10 dBm
<u>Command Input</u>	
Word Sizer	17 bits (16 freq., 1 initiate) .
Format	Parallel, Binary
Level	TTL

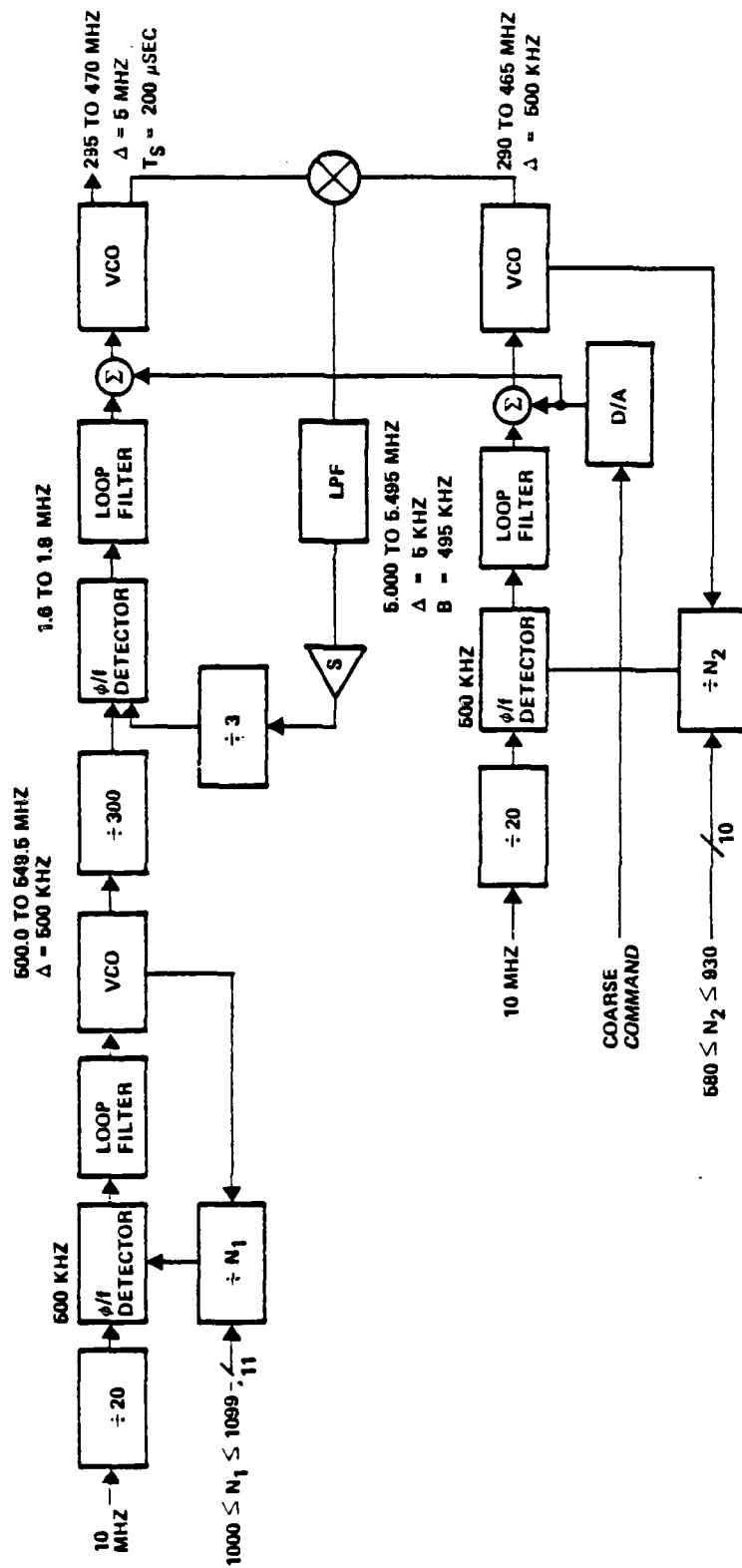


Figure 5-38. UHF Synthesizer

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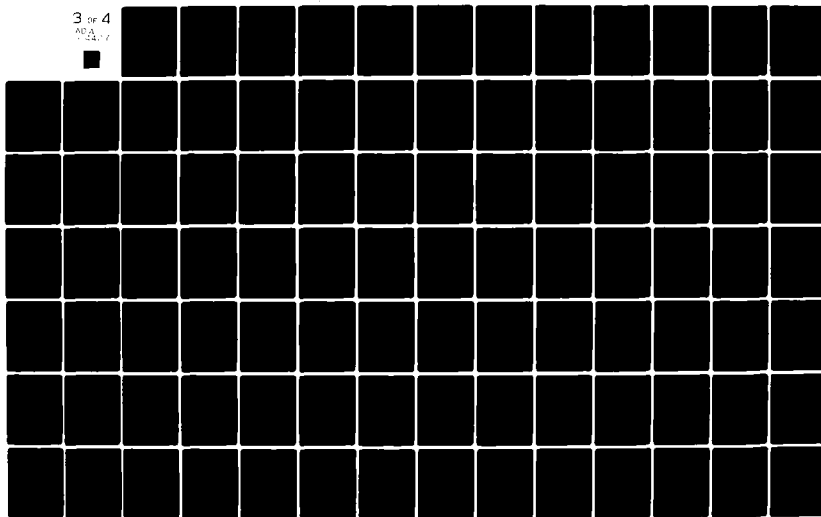
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6. MATRIX SIGNAL PROCESSOR

6.1 INTRODUCTION

The MFBARS digital signal processing is basically a high-performance programmable modulator-demodulator (modem). The modem processing includes all baseband data/message processing. The flexible processor organization is partitioned into preprocessor modules and a signal processor. The preprocessor modules perform specialized high-rate data processing unique to each waveform to be accommodated by the MFBARS terminal. This allows customization to particular, nonstandardized data processing. The signal processor is capable of handling the modem and message processing, including mode control and avionics compatible input/output (DAIS). A single, centralized but highly redundant micro-signal-processor (MSP) can process all algorithms simultaneously, thereby time-sharing the same hardware across all MFBARS waveforms. The MSP is a combination of signal processor and microprocessor denoting micro-programmable signal processors.

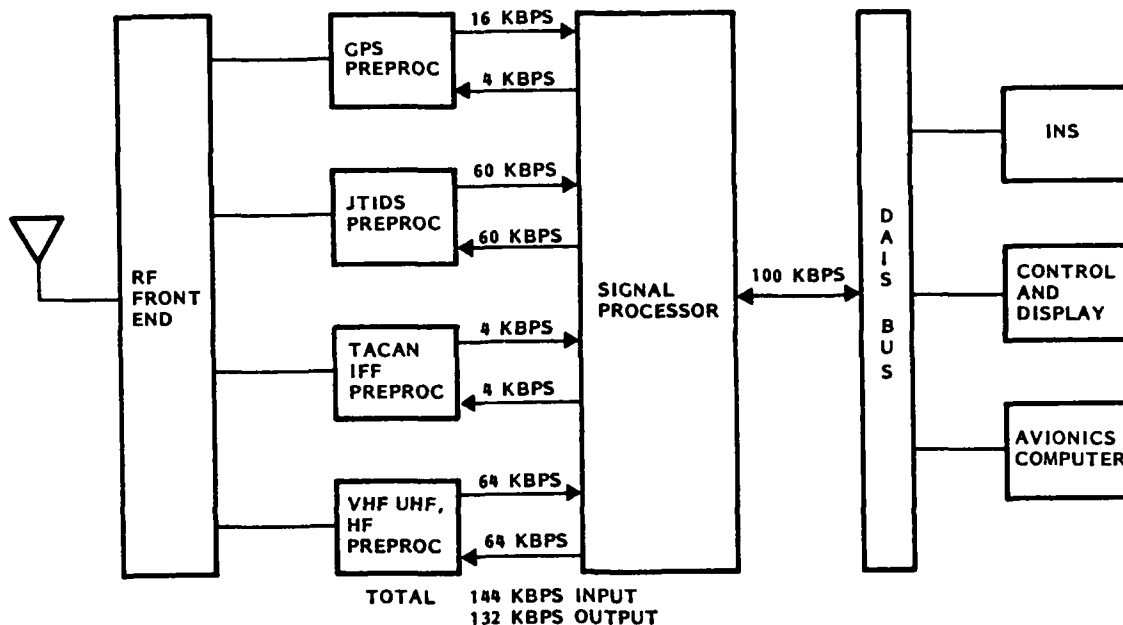
The digital signal processing system interfaces are summarized in Figure 6-1, with the two major elements shown - the preprocessors and the signal processor. The preliminary data rates tabulated are basic data rates without message overhead or analog-to-digital over-sampling factors. The DAIS data bus interface is based on voice communications, status data, and navigational data.

6.2 SYSTEM REQUIREMENTS

The MFBARS digital signal processing requirements are divided into the preprocessor and signal processor. The MFBARS waveforms considered include GPS, JTIDS, TACAN, IFF, and VHF/UHF/HF.

6.3 PREPROCESSORS

The preprocessors are, as formentioned, dedicated to each waveform and provides high-rate repetitive signal processing. These include analog-to-digital conversion, voltage comparison for data determination, and PN/CLOCK generation and control. The preprocessors standardize interfaces between the RF front-end/despreader and the common signal processor. The centralized signal processor requires computer-oriented



- PREPROCESSORS PERFORM HIGH RATE SPECIALIZED DIGITAL PROCESSING
- SIGNAL PROCESSOR ACCOMMODATES ALL WAVEFORM ALGORITHMS SIMULTANEOUSLY
- DAIS BUS INTERCONNECTS MFBARS TERMINAL WITH OTHER ON-BOARD SYSTEMS

Figure 6-1. MFBARS Digital Signal Processing System Interfaces

inputs, including block transfers at 5 to 10 mega-words/second rate. The block transfers at high rates reduce the input/output handling overhead. Another function of the preprocessors is to reduce the total data rate into the signal processor. There are simple operations such as accumulating 8 to 32 data samples prior to data synchronization and decoding. These operations, if done in the signal processor, would use a significant percentage of the available programming versus a small hardware addition. This would tend to be a hardware selection in the hardware-software trade-study.

Digital large-scale integration (LSI) technology can be applied to the preprocessors, especially in the timing/control sequencing and decoding, the analog-to-digital conversion, and the PN generators. The major advantages being the reduction in complexity with impact on acquisition and life-cycle costs, improvement in reliability, and trend towards functional standardization.

The functional details of each preprocessor are given in Figures 6-2 through 6-6. The GPS preprocessor (Figure 6-2) provides data digitizing and rate buffering through sample accumulation and the P/CA codes. The control sequencer is driven by a read-only memory (actually PROM) and permits some flexibility in including late changes. The JTIDS preprocessor (Figure 6-3) does CCSK data demodulation, data buffering, and PN codes and correlation clocks. The data demodulation is processed at a 5 megasymbol rate. The TACAN and IFF preprocessor (Figures 6-4 and 6-5) provide pulse-pair discrimination and time information. This processing occurs at a 10 to 20 megabit/second A to D sampling rate. The VHF/UHF preprocessor (Figure 6-6) does I-Q magnitude conversion ($\sqrt{I^2 + Q^2}$), some digital filtering, and PN code generation. Additionally, as with all preprocessors, it has a microprogrammable sequencer and the standard signal processor interface.

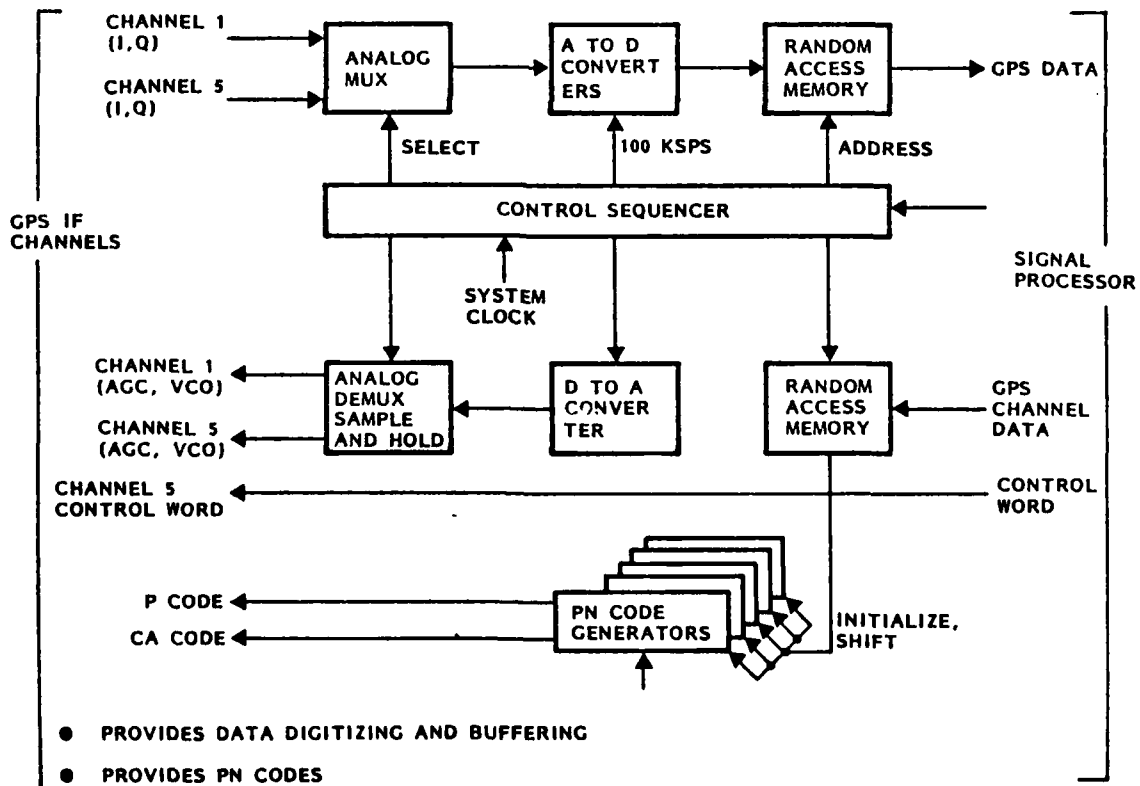


Figure 6-2. GPS Preprocessor

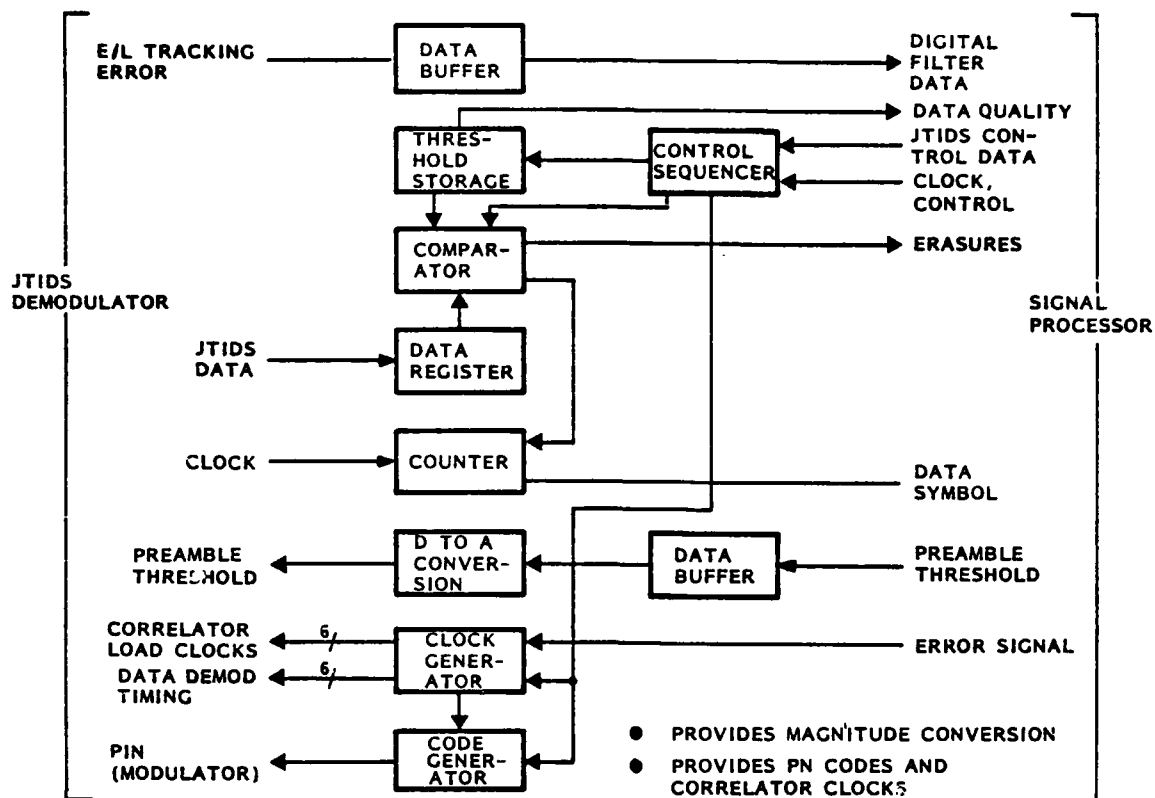


Figure 6-3. JTIDS Preprocessor

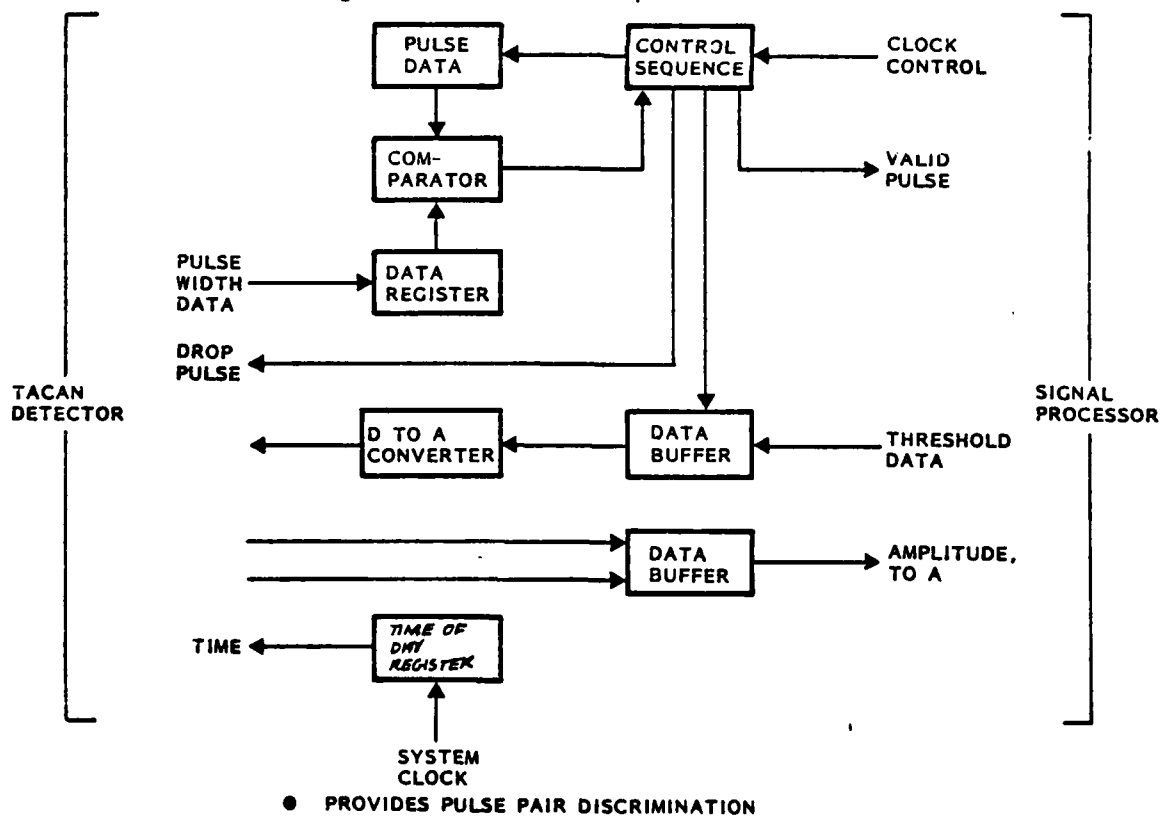


Figure 6-4. TACAN Preprocessor

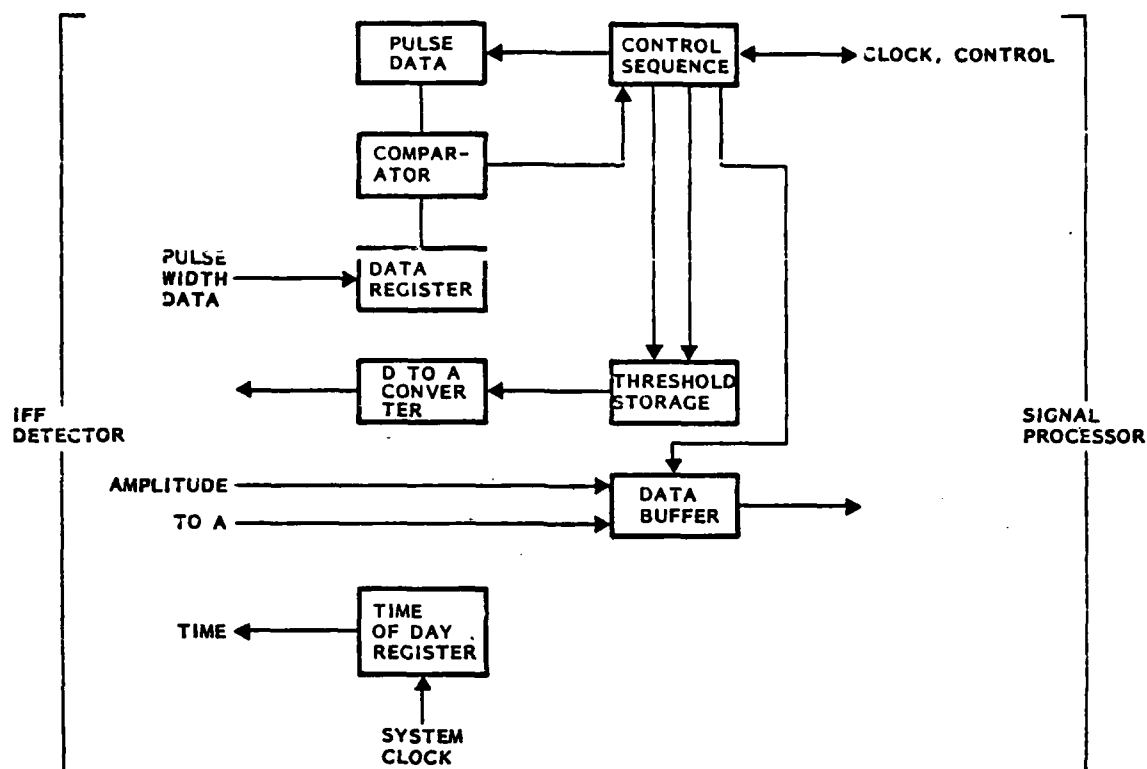


Figure 6-5. IFF Preprocessor

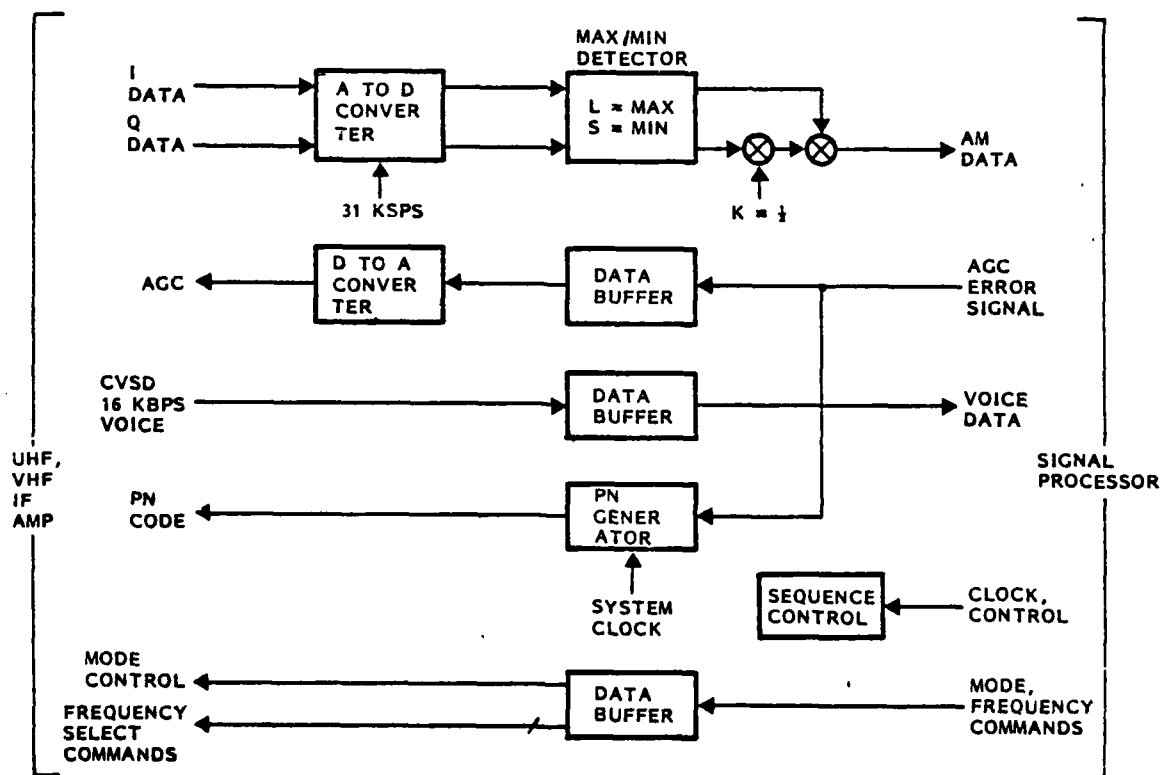


Figure 6-6. VHF/UHF Preprocessor

6.4 DIGITAL SIGNAL PROCESSOR

The signal processor or MSP as given earlier, provides high-speed digital processing at a low unit cost, especially when considering LSI technologies. Other advantages include flexibility through programmability and functional commonality across many systems through time-sharing the same hardware. The MSP programmability can provide more performance capability to counter improving communication threats. The use of digital processing implementations allow a technology substitution capability, both for future standard modules, emerging technologies, and the use of custom LSI. The custom LSI has a trend of improving densities (up to two orders of magnitude) while maintaining the same chip costs. The impact will be to lower acquisition and life-cycle costs.

Each waveform was analyzed for baseband processing in terms of what is necessary to program a standard processor such as a microprocessor/microcomputer. These are summarized in Figure 6-7 through 6-10 for GPS, JTIDS and TACAN/IFF. The algorithms considered for processing in the signal processor (MSP) are given as well as the number of operations. The number of operations per second are given for instructions such as multiply, addition, comparison, memory read or write, memory address generation, and input/output. The number of operations are given as millions of instructions per second (MIPS) as a basis for normalizing performance. Each algorithm was defined in terms of number of operations to be executed and the amount of time available. The latter is usually between A-to-D conversion samples or message transmissions.

The total signal processor programming algorithm summary is tabulated in Figure 6-11. Both GPS and JTIDS dominate the processor loading analysis - GPS in modem functions and JTIDS for the Reed-Solomon encoder/decoder. Much of the operations are in memory manipulations - data formatting/demultiplexing/buffering. A hardware multiplier is required due to the large number of execution's required. The miscellaneous column includes the executive routine. This is the master controller for all subroutine executions, coordination, and priorities. The executive is equivalent to a real-time operating system. The total processing required is estimated to be 40 mega instructions per second (MIPS).

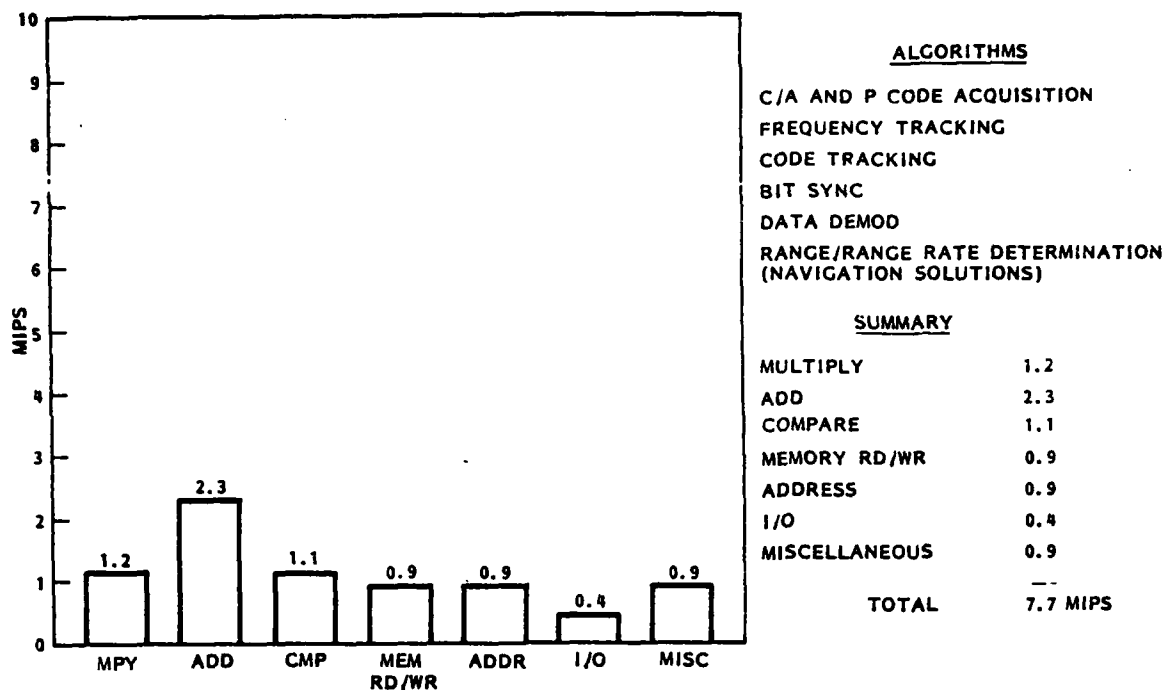


Figure 6-7. GPS-Signal Processor Algorithm Requirements

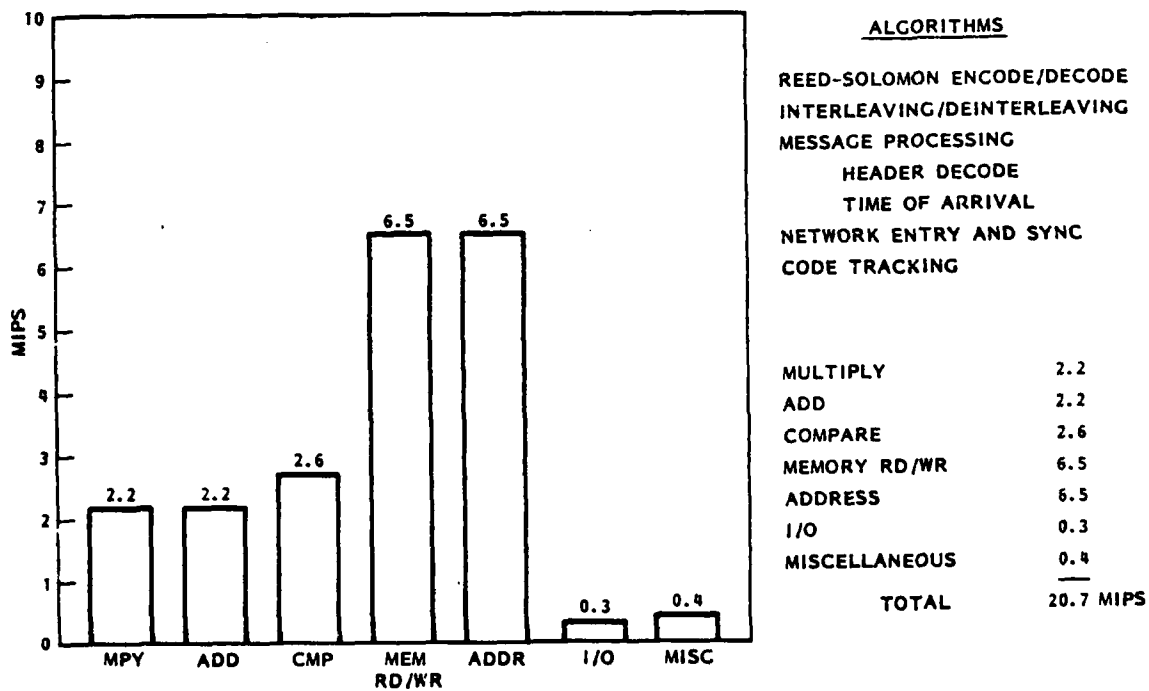
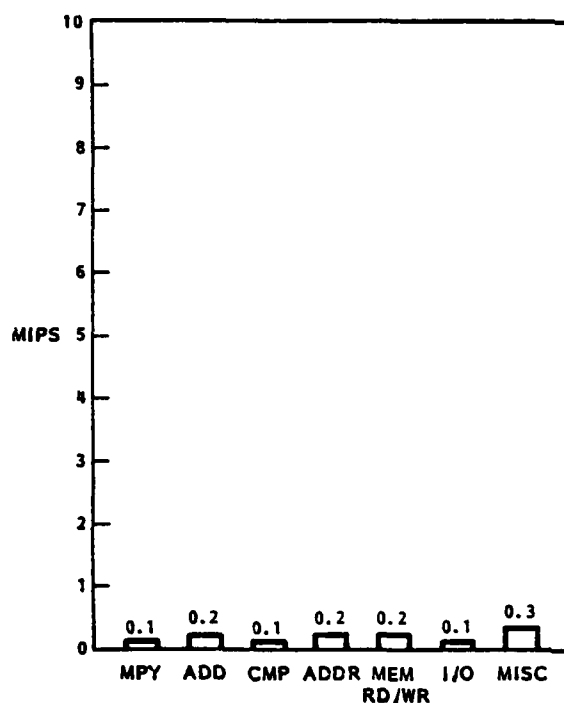


Figure 6-8. JTIDS-Signal Processor Algorithm Requirements

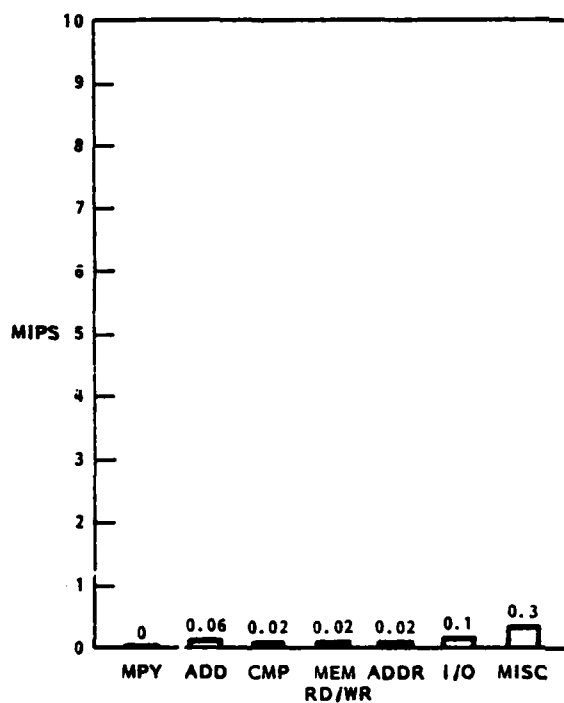


ALGORITHMS

PULSE ID
BEARING EXTRACTION
ACQUISITION AND TRACKING
PULSE PAIR DETERMINATION
PULSE AMPLITUDE DEMODULATION
RANGE ESTIMATION
THRESHOLD SETTING

MULTIPLY	0.1
ADD	0.2
COMPARE	0.1
MEMORY RD/WR	0.2
ADDRESS	0.2
I/O	0.1
MISCELLANEOUS	0.3
TOTAL	1.2 MIPS

Figure 6-9. TACAN-Signal Processor Algorithm Requirements



ALGORITHMS

PULSE ID
PULSE DETERMINATION
PULSE AMPLITUDE DEMODULATOR
MESSAGE CODING
THRESHOLD SETTING

SUMMARY

MULTIPLY	0
ADD	0.06
COMPARE	0.02
MEMORY RD/WR	0.02
ADDRESS	0.02
I/O	0.1
MISCELLANEOUS	0.3
TOTAL	0.52 MIPS

Figure 6-10. IF-Signal Processor Algorithm Requirements

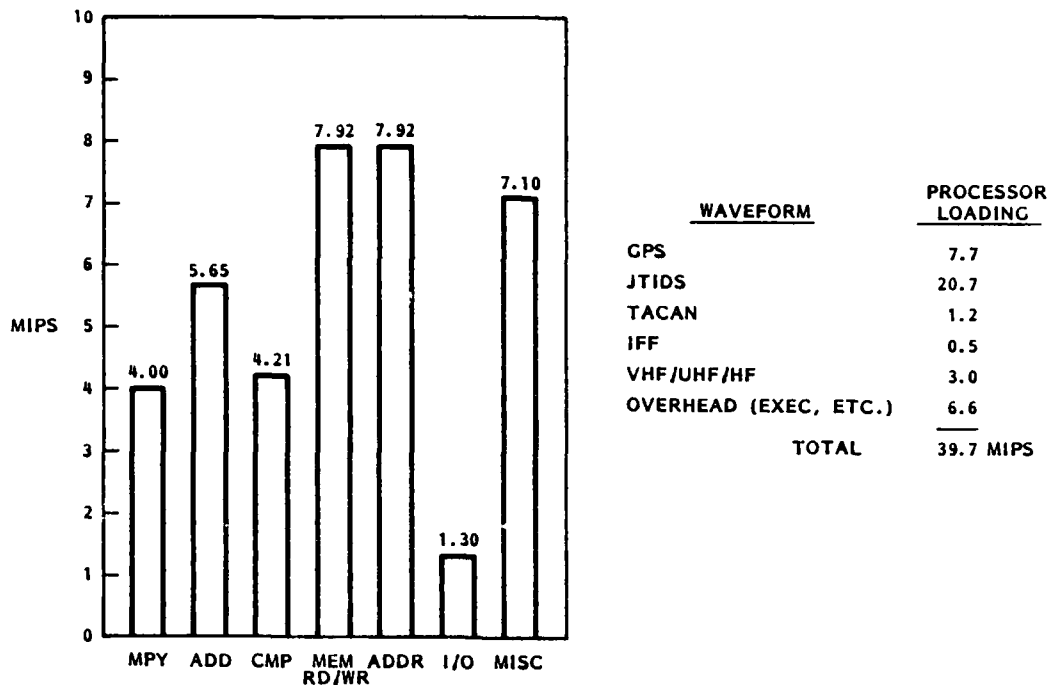


Figure 6-11. Summary: Signal Processor Algorithm Requirements

6.5 MATRIX SIGNAL PROCESSOR

The MFBARS signal processor is required to process many algorithms simultaneously and in real-time up to 40 MIPS. These algorithms include:

- 1) GPS — Acquisition (Time/Frequency)
 - Bit Sync (C/A Code)
 - Code Tracking
 - Phase/Frequency Tracking
 - Data Demodulation
- 2) JTIDS — Acquisition
 - Code Tracking
 - Data Demodulation
 - Error Correction Encoding/Decoding

3) TACAN — Pulse Detection

- Range Acquisition/Tracking
- Range/Bearing Computation

4) IFF — Pulse Detection

- Mode Decoding
- Reply Generation

Many of these algorithms require a sum-of-products computational capability or a hardware multiply-accumulate function. Additionally, fast test-and-branch decision making instructions are necessary for the modem algorithms.

The phase I study generated signal processor design feature goals for Phase II. These features include high reliability through redundancy and automatic reconfiguration, compatibility with a higher-order language (HOL) using an interpreter or a compiler, and flexibility for growth and use with other applications by functional modularity, firmware/software programmability, and technology transparency. The latter relates to the ease with which new technologies and very large-scale integration (VLSI) can be integrated without major modifications.

Minimum physical characteristics achievable include power dissipation of less than 50 watts and volume of less than 150 cubic inches. Implicit is minimum complexity and high density integration generating lower life-cycle and acquisition costs.

A major signal processor architecture trade study investigated two major alternatives: a centralized processor approach and distributed approach. The centralized implementation uses a basic single processor which directly connects all RF front ends/despreaders/modulators. For further data distribution, the output would be the DAIS Bus. The distributed processors dedicate a processor per waveform such as two processors - one each for GPS and JTIDS. Essentially, each waveform is a self-contained radio. Interprocessor communications are through the DAIS Bus.

The centralized processor requires a higher rate signal processor (25 to 50 MIPS) as opposed to the distributed lower rate processor (2 to 5

MIPS). The centralized processor can use a multiple-microprocessor network, while the distributed processor can be a single chip. In reality, the single chip expands to 10 to 15, depending on input/output and memory capacity requirements. The central processor can use a fast-data interchange that is efficient for array and multi-CPU algorithms, or simultaneous multiple-task processing. This is a tightly-coupled multiple processor network. Higher through put performance is possible as load-sharing — shifting CPUs, as necessary, can be done for optimum configurations. The distributed processors are loosely-coupled with low-data rate interchanges. Inefficiencies occur as the processors have a higher percentage of idle time.

The last major item is redundancy management. The centralized multiple processors allow m for n redundancy substitution — spare modules such as CPUs or RAMs can be switched in when failure is detected. This requires a switch matrix, or equivalent, and more complex hardware control. The distributed processors require simple block redundancy or a complex cross-strapping (multiple Buses) for interconnections and control. A preliminary reliability analysis indicates that the centralized approach has almost twice the reliability of the distributed network with equivalent hardware.

The phase II study refined the centralized approach by reviewing interconnection schemes for tightly-coupled networks. Figure 6-12 indicates the performance progression from existing single chip microprocessors to the MFBARS Matrix Signal Processor (MSP). A single chip type is capable of approximately 2 MIPS, while the pipeline microprocessor developed under the Standard Avionics Module (SAM) project is up to 30 MIPS. An LSI module interconnection chip allows at least two pipeline processors to be tightly-coupled, generating 60 MIPS capability in excess of the preliminary MFBARS signal processor requirements.

The SAM pipeline processor used multiple data buses and a dual-port RAM. The goal was to minimize data access conflicts, which would slow real-time processing (Figure 6-13). A hardware multiply-accumulate was used in conjunction with the CPU through cross-strapped buses. This allowed the CPU and MPU to be cascable for pipeline operations such as sum-of-products. A separate address generator for each memory was

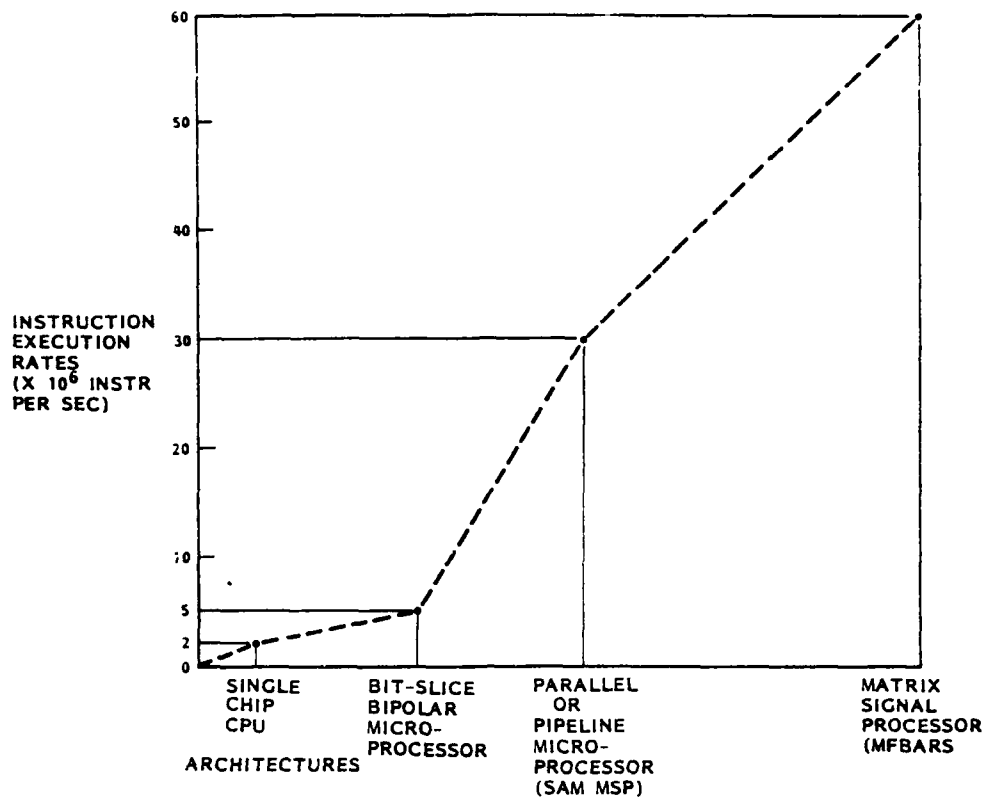


Figure 6-12. Microprocessor Technology and Architecture Leverage

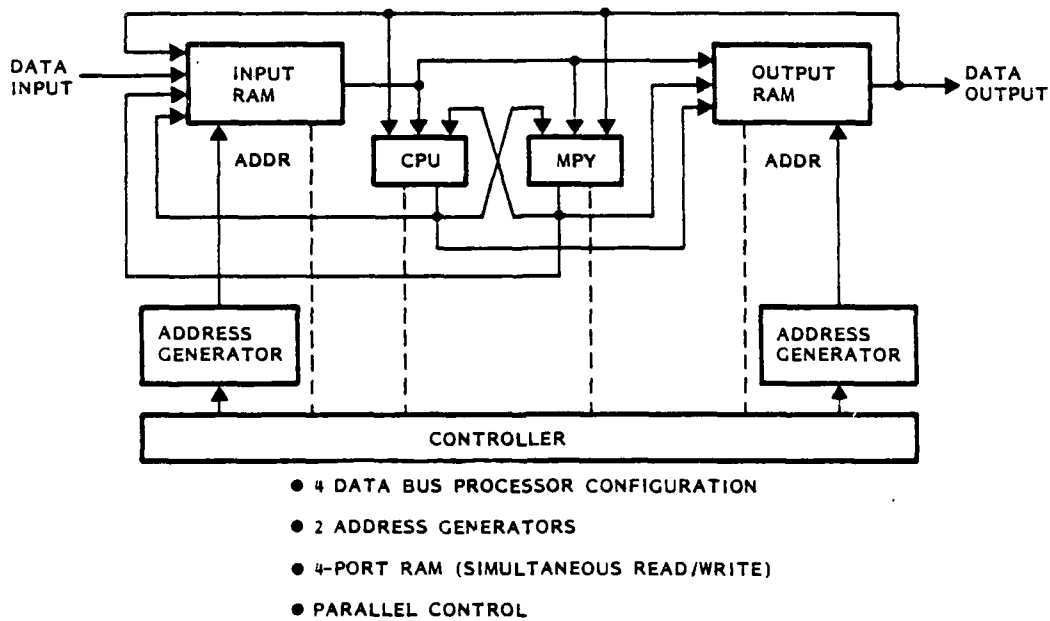
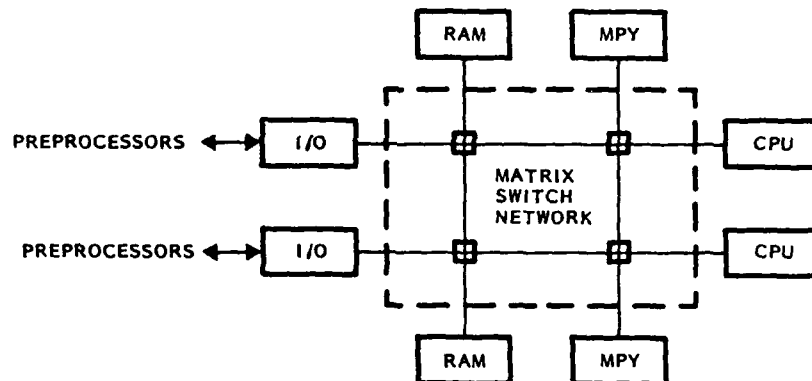


Figure 6-13. Basic Processor Topology (32 MIPS)

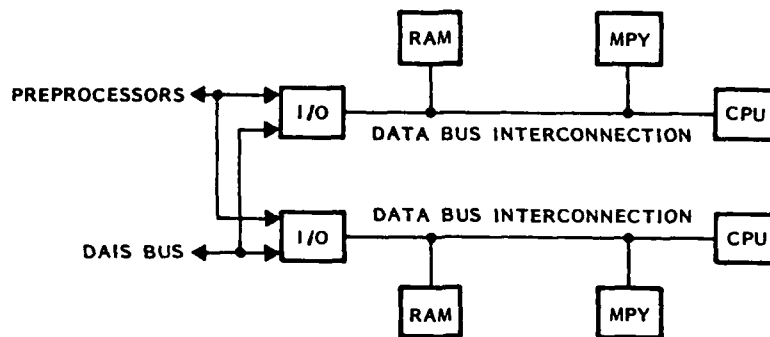
used to unload the CPU for processing algorithms only - again improving performance. The horizontal microprogrammed instructions can execute up to eight-to-ten instructions simultaneously, in parallel, for certain algorithms, thereby improving the basic instruction execution rate (5 MIPS) by that factor. Note that inefficiencies caused by program conflicts and idle time could lower the maximum rates by up to 20 percent.

Using the SAM pipeline processors, two units could meet the MFBARS requirements without redundancy considerations (Figure 6-14). Overlaying the centralized tightly-coupled concepts, the matrix signal processor (MSP) results. The matrix switch, as shown in Figure 6-15, is an array of switches not unlike cross-bar or cross-point switches that allow direct, noninterfering data interconnections between the modules - CPU, RAM, MPU and I/O. All resources can be reconfigured on an instruction-by-instruction basis, allowing load-sharing and redundancy reconfiguration.



- MATRIX SWITCH NETWORK PROVIDES DIRECT DATA INTERCONNECTION FOR ALL MODULES
- MATRIX SWITCH NETWORK
 - INCREASES AVAILABILITY BY TIMESHARING PROCESSING
 - MAXIMIZES FLEXIBILITY BY MODULE TYPE AND RESOURCE ASSIGNMENT

Figure 6-14. Basic MFBARS Dual Signal Processor Architecture



- DUAL INDEPENDENT SIGNAL PROCESSORS
- EACH SIGNAL PROCESSOR CAPABLE OF 32 MIPS
- ACCOMMODATES MFBARS 40 MIPS REQUIREMENT

Figure 6-15. Matrix Signal Processor Architecture

The TRW MSP has the following features:

- 1) Improved Availability
 - Limited Fault Tolerance Capability
- 2) 64 MIPS Capability meets MFBARS Performance (40 MIPS) Simultaneously
- 3) Expandable to 4 x 4 Matrix
 - 128 MIPS Capability
 - 32 Bits Per Word Expansion
 - Technology Transparent Modules
- 4) High Performance for Given Volume
 - Capable of 1024 Point Complex FFT in 1.5 MS Within 280 Cubic Inches (5 x 7 x 8 inches)

The dual MSP configuration is labeled a 2 x 2 matrix signal processor and can be expanded to a 4 x 4, which is essentially four complete micro-processors. Using a 4 x 4 generates the signal processing bench mark (FFT algorithms) within 1.5 ms. This configuration, with spare modules, is illustrated in Figure 6-16.

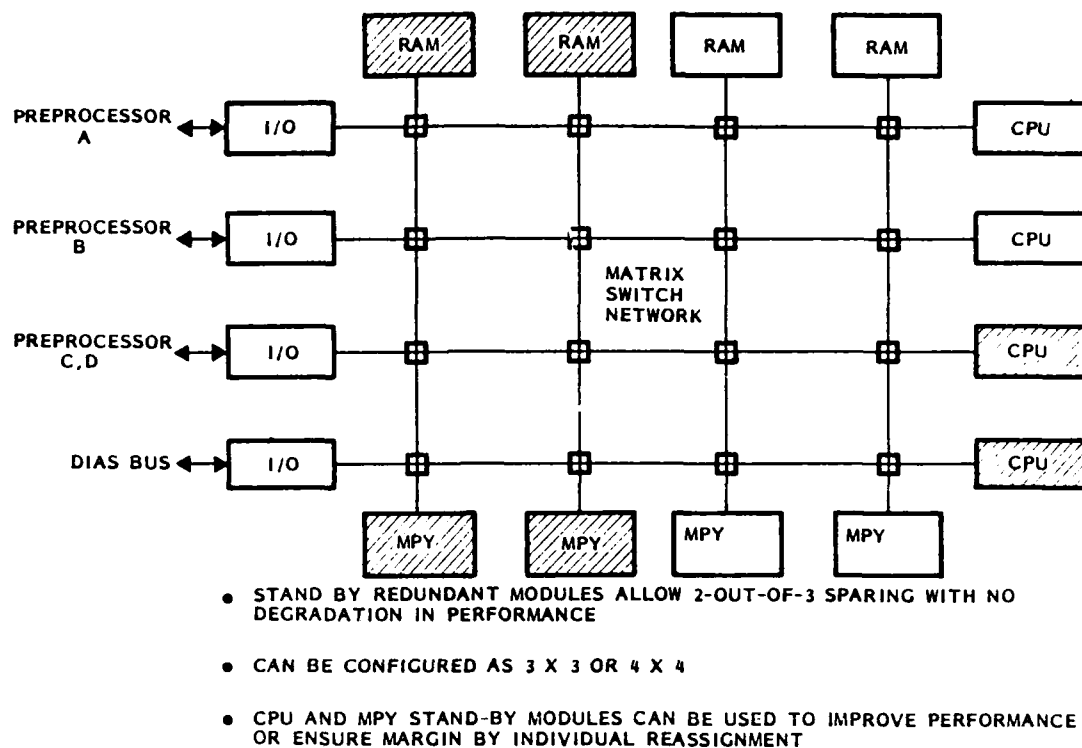


Figure 6-16. Matrix Signal Processor Expandability 4 X 4 Matrix

The matrix switch can easily be in LSI form as it is a bank of simple multiplexers. The 2 x 2 MSP requires eight multiplexers that select one-of-eight inputs per module. This is shown in Figure 6-17. Sixteen LSI chips for the 2 x 2 matrix switch are required, as each LSI is in a bit plane organization - as RAM's are configured. All the interconnections shown are on-chip to minimize wiring complexity.

This matrix switch is one of the key new technology developments required for the MSP. Another chip with major impact on complexity is a high-speed 48-bit instruction register. All other elements are off-the-shelf or in development. This is summarized in Figure 6-18.

6.6 MATRIX SIGNAL PROCESSOR CONTROL

The matrix signal processor control concept is based on a time-division multiple access control bus. Each computational element (memory, CPU, multiplier, etc) in the matrix has an assigned time slot on the bus. The controller sends a 48-bit control slice to each computational element

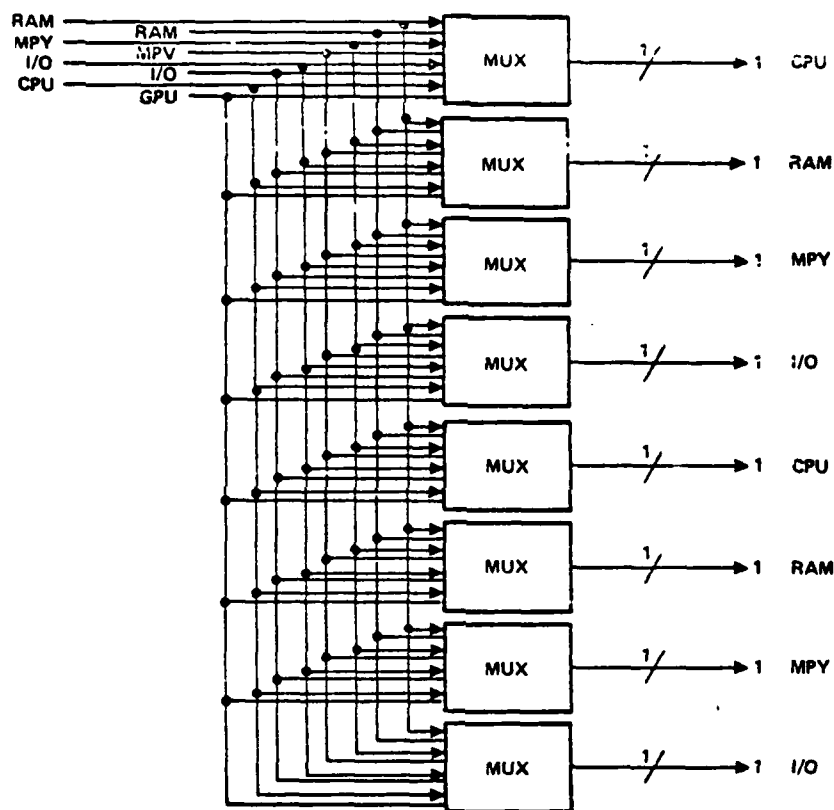


Figure 6-17. 2 x 2 Matrix Switch

MODULE	KEY ELEMENT	DEVELOPMENT* STATUS	LSI LEVERAGE
RANDOM ACCESS MEMORY	● 4-PORT REGISTER FILE ● ADDRESS GENERATOR	IN-DEVELOPMENT NEW DEVELOPMENT INITIATED	10 TO 1 12 TO 1
MULTIPLIER	● TRW 16 X 16 MAC	COMMERCIALY AVAILABLE	—
CPU	● AMD 2903	COMMERCIALY AVAILABLE	—
MATRIX SWITCH	● MATRIX SWITCH LSI	NEW	200 TO 16
CONTROLLER	● 50 MBPS DUAL RANK 48-BIT INSTR REGISTER	NEW	120 TO 8
I/O	● DMA CONTROLLER (AMD 2940)	COMMERCIALY AVAILABLE	—

* 31POLAR LSI TECHNOLOGY

Figure 6-18. Key Elements — Matrix Signal Processor

and the specific element decides whether the control information is intended for that element. Each element loads its control slice into a dedicated 48-bit register and holds it until the next TDMA assigned time slot. This scheme is conceptually illustrated in Figure 6-19 and can be regarded as a fully synchronous centralized control concept.

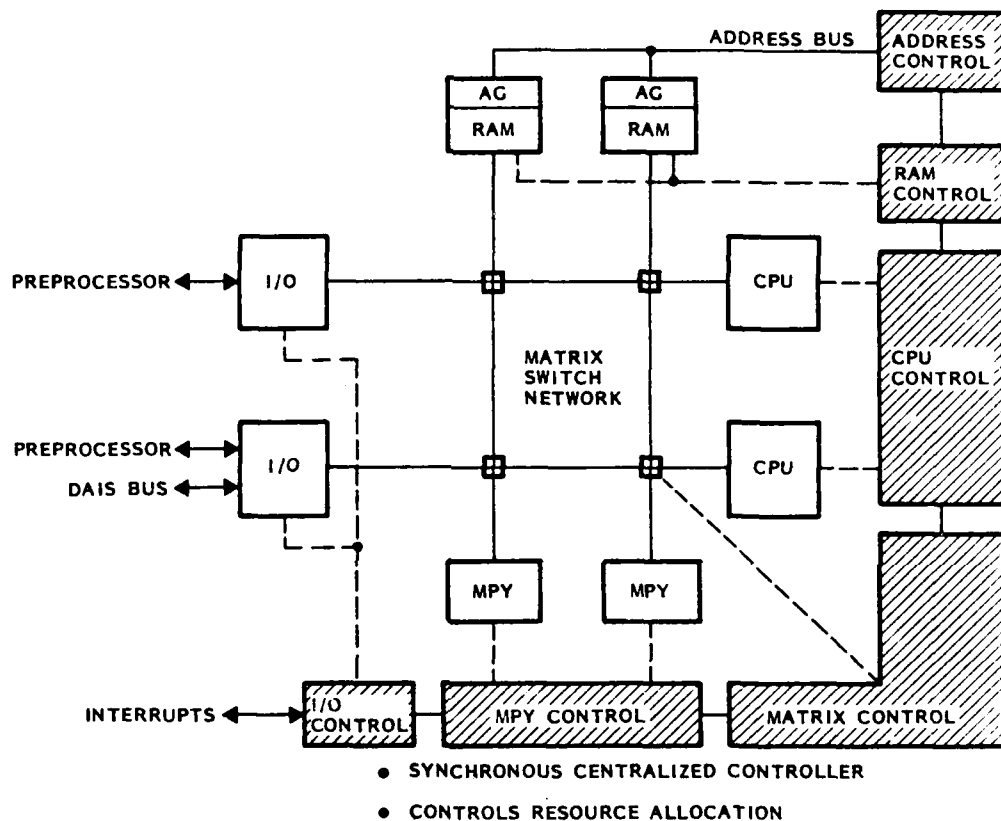


Figure 6-19. Matrix Signal Processor Controller

This control concept has several advantages. The first is that the TDMA control, in conjunction with the fully parallel data path interconnect, allows reconfiguration of computational modules and hardware resource management in the event of hardware module failures. The signal processor can accommodate high availability/graceful degradation requirements due to its inherent ability to switch computational modules on and off line by simply reassigning time slots on the control bus. Figure 6-20 illustrates the interface between the controller and computational modules via the time divided control bus.

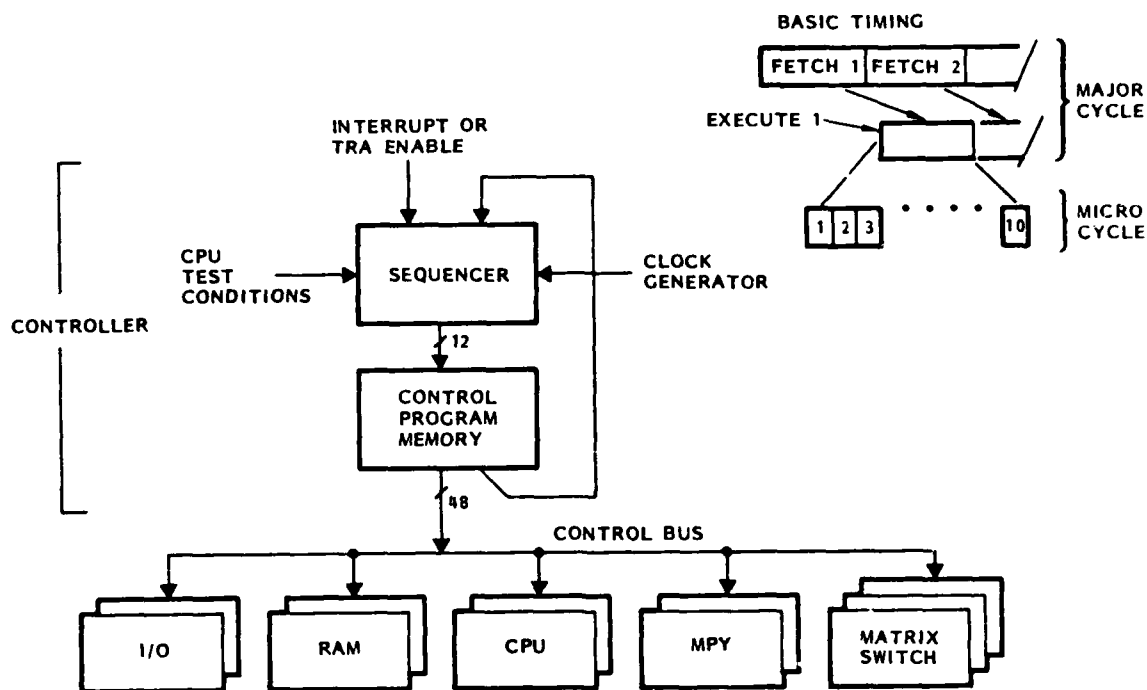


Figure 6-20. Controller Architecture

The second advantage of this control concept is that by adding a multiplexer on the control path and reassigning time slots, multiple controllers can be implemented. That is, a single matrix computational section can functionally emulate two independent machines. Figure 6-21 illustrates this configuration with a 2 x 2 matrix and two controllers. This feature adds a significant flexibility factor in processing options. For example, a single computational section can be reorganized to accommodate two vastly different problems. A memory intensive data acquisition/control function and a computationally intensive signal processing problem are two examples of this organizational flexibility.

6.7 SUPPORT SOFTWARE DESIGN CONCEPT

The support software design concept consists of three interdependent software packages, the first being a higher-order language compiler. This compiler is the primary application program interface with the signal processor hardware. Because the matrix signal processor is a highly parallel architecture, assembly language programming techniques are

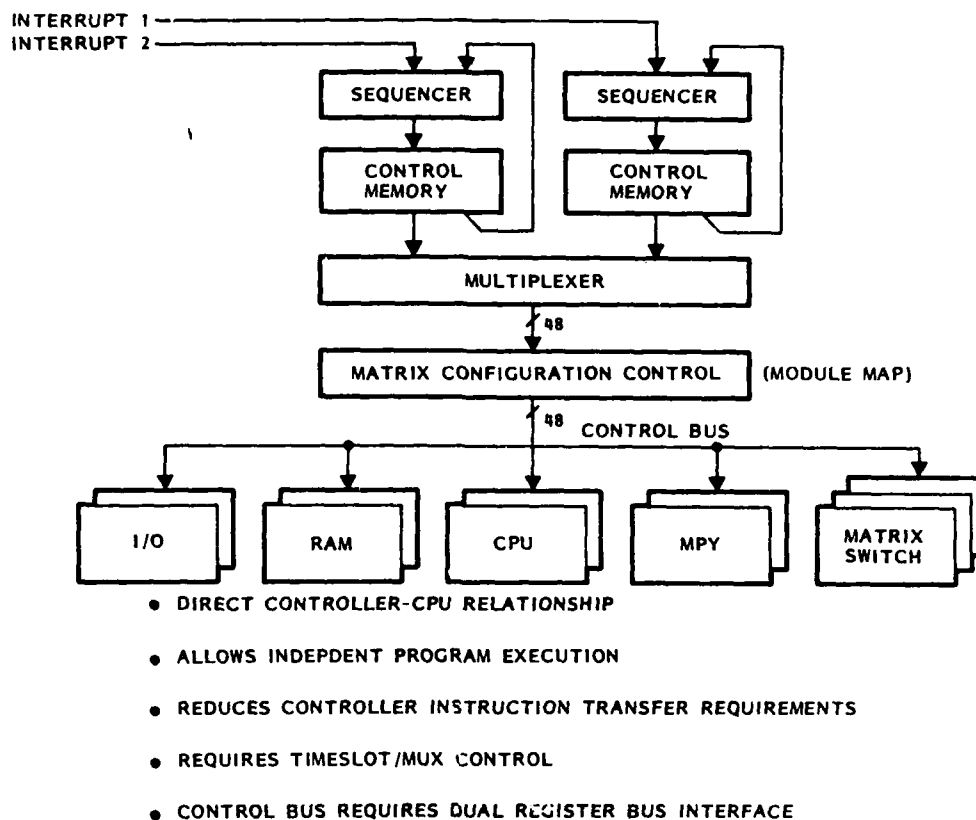


Figure 6-21. Controller Architecture – 2 x 2 Matrix

regarded as ineffective from a programming cost standpoint. Parallel architectures also generally require a higher level of programming expertise if the parallelism is not hidden from the programmer via some software automation.

The second software package, known as the resource allocator, is the software automation designed to map programs written in a sequential higher-order language to the parallel matrix signal processor architecture. This software package accepts an intermediate sequential language output from the higher-order language compiler and analyzes it for varying degrees of parallelism. Using a hardware architectural description, the resource allocator determines a matrix of free computational elements and assigns all possible parallel program operations to free resources at a given sequential program step. There is some automation overhead using this approach, but it is more than offset by savings in programming costs, transportability of application programs, and programmer acceptance of the overall hardware/software interface.

The third software package, the assembler, is a straightforward modification of existing table-driven assemblers which produce machine code from mnemonic parallel programs generated by the resource allocator.

The interdependence of the overall software design concept is illustrated in Figure 6-22. Each software package uses inputs from another package to perform a portion of the complete task of generating machine code for a highly parallel processor architecture (from a standard higher language such as ADA). Each portion of the software design concept either currently exists or is under development.

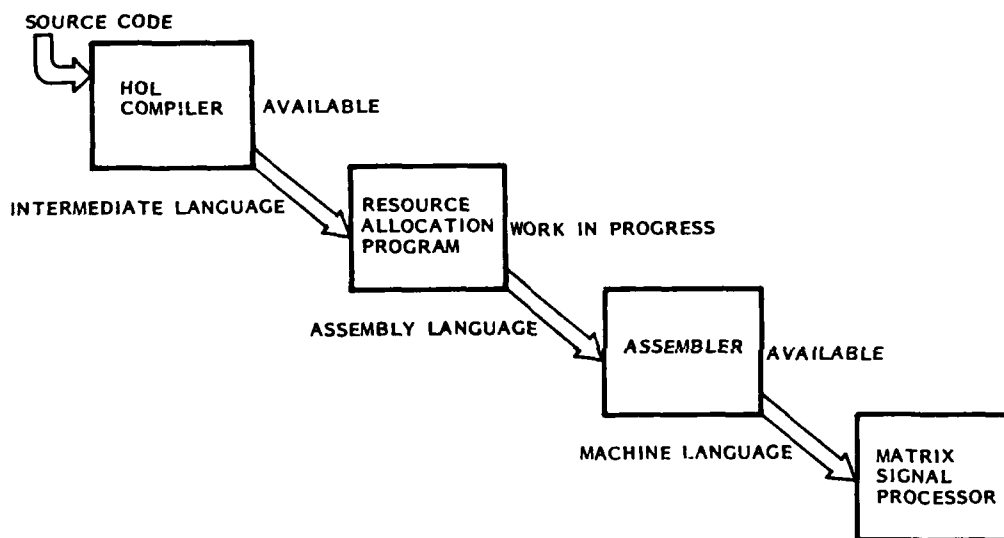


Figure 6-22. Software System Overview

6.8 PROGRAMMING EXAMPLE

The programming example of Figure 6-23 is intended to further clarify the matrix signal processor hardware/software interface. This example implements a complex multiply on a 4 x 4 matrix machine. It is assumed that the machine has four adders, four multipliers, and four random access memories for data storage. It is unrealistic to assume data partitioning in four distinct memories, so it is assumed that the real data resides in one distinct memory and imaginary data resides in another. Using these

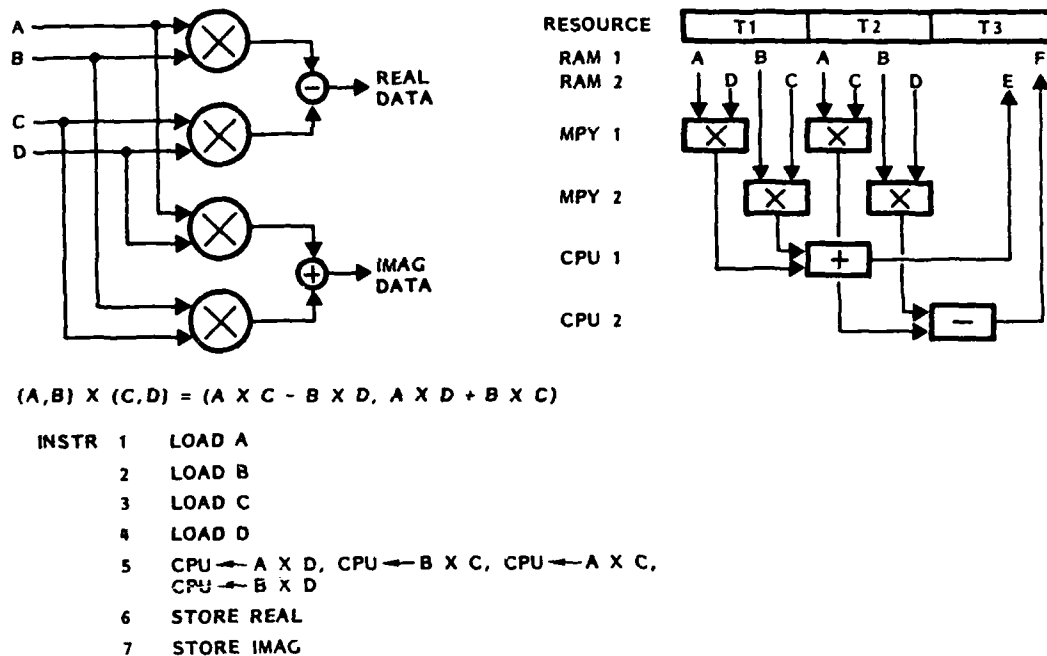


Figure 6-23. Programming Example

assumptions, a complex multiply can be accomplished in four machine instructions as follows:

$$(A, B) * (C, D) = (A * C - B * D, A * D + B * C)$$

- 1) Load A, Load D
- 2) Load C, Load B
- 3) CPU 0 ← A*D, CPU 1 ← B*C
CPU 2 ← A*C, CPU 3 ← B*D
- 4) Store A*D + B*C, Store A*C - B*D

This example illustrates the parallel computational structure of the matrix signal processor. In instruction (1), one real and one imaginary data word are loaded to two multipliers. Instruction (2) loads two data words to two multipliers. Eight data moves are accomplished in two instructions and unused resources may be devoted to other tasks. Instruction (3) moves four multiplier outputs to four input registers on two CPUs in preparation for the add and subtract. Instruction four moves two CPU results

to the real and imaginary memories, respectively. Note also that memory addressing is accomplished independently of arithmetic computations in separate memory address generators.

The overall matrix signal processor control and software design concept maximizes throughput, availability, and flexibility by utilizing a unique, modular, parallel processor architecture. The software cost effectiveness problems created by this approach are solved by automating the program development process to a standard higher-order language such as ADA.

6.9 SUMMARIES - FIRMWARE AND HARDWARE

Firmware and hardware summaries are given in Figures 6-24 and 6-25 respectively. For the estimated signal processing algorithms, approximately 4096 assembly language instructions are required as most of these MSP programs are small. Although note that these are parallel instructions, and that they can be equivalent to about 32,000 simple instructions. The hardware summary shows physical parameters for the 2 x 2 and 4 x 4 configurations. Consideration for VLSI (the matrix switch LSI and register) can improve the parts count by 70 percent, halve the power dissipation, and improve performance (simple instruction execution rates) by 30 percent.

	ASSEMBLY LANGUAGE INSTRUCTION TOTAL
GPS	512
JTIDS	1024
TACAN	256
IFF	256
VHF/UHF/HF	1024
OVERHEAD	512
SPARES	512
TOTAL	4096
NOTE: PARALLEL INSTRUCTION EQUIVALENT TO EIGHT STANDARD INSTRUCTIONS	

Figure 6-24. Matrix-Signal Processor Firmware

	2 X 2 MATRIX		4 X 4 MATRIX
	MSI/LSI	VLSI	VLSI
PARTS COUNT	480 IC'S	152 IC'S	246 IC'S
POWER DISSIPATION	97 W	55 W	93 W
BASIC CLOCK CYCLE	300 NS	200 NS	200 NS

● SUMMARY: VLSI VERSUS MSI/LSI IMPROVEMENTS

PARTS COUNT	68 PERCENT
POWER DISSIPATION	43 PERCENT
BASIC CLOCK CYCLE	33 PERCENT

● VLSI CONFIGURATION INCLUDES KEY ELEMENTS SUCH AS MATRIX SWITCH, 4-PORT RAM, ETC.

Figure 6-25. Matrix Signal Processor Hardware Summary

In summary, the MFBARS Matrix Signal Processor can achieve all the design features given earlier — high reliability by module configuration, higher-order language compatibility with emphasis on a sophisticated resource allocator/interpreter, maximized flexibility through module interconnections, and minimum physical characteristics. The latter requires the use of VLSI, as in the matrix switch, but this provides very high data throughput capability on the order of 128 MIPS within a very small package. In addition to the MFBARS communication requirements, the MSP can now be applied to many other systems such as radar signal processors that require high performance signal processing.

7. INTEGRATED INERTIAL NAVIGATION WITH MFBARS

7.1 INTRODUCTION

This section details the software requirements for a number of MFBARS integrated navigation system design options for the case with GPS, JTIDS, gimballed inertial measurement unit (IMU) and barometer altimeter as navigation sensors. Computational requirements are in part dictated by the extent of aiding, especially GPS aiding. During the Phase II add-on task the emphasis has been first of all on establishing the basic criteria for MFBARS navigation system operation in a jamming environment and secondly on defining the software functions and its interfaces, and estimating its computational requirements, e.g., throughput, memory, word length, etc. These data are used in the computer architecture design trades of Section 6 and in the economic analysis of Section 8.

The remainder of the introduction provides an Integrated Inertial Navigation system overview. Subsection 7.2 discusses system operation. Subsection 7.3 covers filter design. Subsection 7.4 covers data processor functional design. Section 7.5 gives data processor sizing and timing estimates. Recommendations for additional studies are given in Section 7.6. The recommendations are directed toward resolving critical issues associated with operation and integration of inertial and radio navigation systems.

The MFBARS radio navigation subsystems GPS and JTIDS and the inertial navigation system (INS) have complimentary features, which when used in an integrated system, can improve navigation performance for tactical aircraft and/or in jammer environment applications. The INS is an inherently short-term accurate navigation system, ≈ 0.8 n mi/hr for current tactical applications. Thus data from sources external to the INS could be used to improve long-term navigation performance. GPS and/or JTIDS measurements, after processing by (Kalman) filter algorithms are of sufficient accuracy to be an external source for improvement. There are direct improvements on the INS estimates of position and velocity. In addition, accurate estimates for altitude reference bias and inertial measurement unit (IMU) platform alignment and drift biases can be obtained as outputs from the above noted filter.

GPS provides a long-term accurate, absolute navigation capability, which estimates position with less than 50 ft error. However, satellite signal tracking is sensitive to jammer interference. This sensitivity to jammer interference can be reduced by using INS information to reduce vehicle dynamics effects and decrease the receiver tracking loop bandwidths, so that the tracking loops can operate at increased jammer to signal ratios (J/S). In addition, with INS provided position and velocity data the receiver search region in the phase-frequency domain can be limited, therefore reducing time for acquisition and reacquisition. While accurate knowledge of the system time, through JTIDS, allows for faster, direct P-Code acquisition. In general, the aiding INS and JTIDS sensors provide augmented navigation capability which gives optimal navigation performance with GPS and continuity during GPS outages.

JTIDS provides a jammer resistant, relative navigation capability with a long-term position accuracy of ≈ 200 ft. Aiding of the JTIDS net is primarily provided through synchronization of GPS and JTIDS system times, in which case the availability of GPS time provides fast entry into the JTIDS net, while the GPS and INS subsystems can provide absolute navigation to the JTIDS net. In general, the aiding GPS and INS sensors provide augmented navigation capability, which gives optimal navigation performance with JTIDS and continuity during JTIDS outages.

If a multiple beam phased array antenna design is selected for the MFBARS system, then the navigation system must aid the antenna system by providing beam-pointing information for phase command generation.

The software functions, which perform the integrated navigation are designated as data processor in the following. The basic difference between the data processor and signal processor functions is that the first requires a relatively low data throughput rate and a large memory, while the latter requires high data rates and little memory. These differences should influence the MFBARS computer architecture design and its interfaces with the DAIS data bus.

7.2 MFBARS NAVIGATION SYSTEM OPERATION

The impetus for integration of the INS, GPS and JTIDS navigation subsystems is the improvement in navigation performance that can be achieved

through mutual aiding for high dynamics vehicles operating in a jamming environment. In order to design an integrated MFBARS navigation system, it is necessary to define the extent of aiding. When operating in a benign environment, GPS satellite signal acquisition and JTIDS net entry is facilitated with aiding data. The GPS aiding consists of position and velocity data, which can be provided by the INS and possibly system time, which can be provided by JTIDS, if GPS and JTIDS times are synchronized for faster acquisition. JTIDS aiding consists of system time for faster net entry, provided by GPS, if GPS and JTIDS times are synchronized. GPS and/or JTIDS aiding of the INS is required continually to improve the long-term inertial navigation accuracy. GPS aiding is preferred over JTIDS aiding because of its greater accuracy. However, GPS is relatively sensitive to jammer interference. JTIDS, to the contrary, is more resistant to jammer interference through the use of longer codes and frequency hopping techniques. By providing additional aiding to the GPS subsystem, it is possible to increase the resistance of GPS to jammer activity. The extent of the additional GPS aid functions and rationale for the selected aiding options for the MFBARS design are given in the remainder of this section.

The GPS aiding functions, which impact the data processor design, are related to the following: (1) more accurate estimation of tracking loop parameters, (2) control of antenna pointing parameters, (3) satellite selection/switching. The GPS receiver design implements tracking loops with noise thresholds which are determined by the finite tracking loop bandwidth required to track the anticipated loop dynamics. While loop noise demands a narrow bandwidth to maintain track, a wider bandwidth is required to track the vehicle dynamics. Thus, by providing an independent estimate of the vehicle dynamics, it is, in principle, possible to narrow the loop bandwidth which results in a greater antijam margin. The quality of the aiding data determines the amount of bandwidth reduction, and the errors in the aiding become the new dynamic disturbances which the tracking loops must follow. These errors establish the aided receiver threshold. Three receiver tracking thresholds must be considered:

- Data demodulation
- Carrier tracking
- Code tracking.

The tracking threshold for the data demodulation Costas tracking loop is not increased by any form of navigational data aiding. The data processor uses the satellite ephemeris and clock bias data obtained at initial acquisition, hence acquisition must occur in a benign or near benign environment.

The carrier loop provides the delta range or doppler measurements. In order to avoid loss of lock the tracking error should be kept within 0.1 ft (phase-locked) and 0.05 ft (Costas) (Reference 1). In order to provide this accuracy with narrow tracking-loop bandwidths during high-dynamics maneuvers, the aiding velocity signals must be updated frequently, on the order of every 10 ms. Because data are generally not available from the INS mechanization algorithms this frequently, the aiding data must be provided by a dedicated IMU, in which case an increase of up to 10 db in antijam margin can be obtained (Reference 2). Loss of carrier loop lock results in loss of the doppler measurements, which is not a severe drawback since doppler information is usually more accurately obtained by differencing range measurements.

The code tracking loop provides the pseudorange measurements. The code loop inherently places lower restrictions on both the allowable delay and the accuracy of the velocity aiding data, due to the fact that the code loop dynamics are scaled down by a factor of about 160, the L-band to the P-code frequency ratio. Hence the code loop tracking errors can be on the order of tens of feet, and INS computational delays of up to about 150 ms are acceptable. Code loop bandwidth reductions of 0.1 Hz have been achieved with a second order loop implementation, which corresponds to a 8 db increase in the antijam margin over the unaided code loop (Reference 2). For small bandwidths, the aided code loop implementation might become unstable and a compensation might have to be incorporated. For higher order loops, the time delays are such that measurement errors are no longer independent and residual editing should not be used to decide if a measurement is acceptable or not (Reference 3). Instead, the range measurement data quality must be based on the measured jammer-to-signal ratio (J/S).

In addition, adaptive tracking techniques have been developed to calculate optimum tracking loop parameters. In these techniques INS data is used to determine the time variable parameters in a model of the effective pseudorange dynamics and INS and receiver data is used to determine the signal-to-noise ratio. From this information, together with initial values for covariances of the tracking error states, successive tracking error covariances and optimum tracking loop parameters can be calculated.

In the MFBARS navigation system design, aiding is only provided for code loop tracking. Carrier loop tracking aiding is not implemented for the following reasons:

- 1) Accuracy and rate of aiding requires a dedicated IMU.
- 2) For high-dynamic maneuvers of tactical aircraft, the effects of acceleration on the frequency of the GPS crystal oscillator can be a significant cause of residual tracking errors in the inertially aided tracking loops, thus negating part or all of the benefits of the aiding.
- 3) Range rate can be obtained by differencing the range measurements, thus the range rate measurements are not critical.
- 4) JTIDS provides a backup for aiding the INS in case one or more GPS measurements are lost for an extended period.

Adaptive tracking has not been included in the MFBARS navigation system design for the same reasons.

The second way of enhancing GPS performance in jamming environments is by means of advanced antenna techniques in which either jammer signals are detected and suppressed or narrow beams are directed at the satellites. The first technique which uses an adaptive null steering array antenna does not require any outputs from the navigation data processor. The second technique, which uses a multiple beam array antenna, requires the calculation of beam pointing angles (phase shifter commands if the conversion is not performed in a special purpose processor) as part of the navigation data processor GPS aiding functions. For the MFBARS navigation data processor design, it is assumed that an adaptive null steering array antenna is used. Hence no data processing resources are required for antenna beam pointing.

The third method of protecting the operation of GPS in a jamming environment is by selecting satellites with signals which are least affected by jammer interference. In most cases ground based jammers are more effective against tactical aircraft than are space based jammers. Consequently, the signals from low elevation satellites are affected more by the jammers than are the signals from high elevation satellites. The currently used satellite selection criterion is generally based on minimizing Geometric Dilution of Precision (GDOP), which results in the selection of satellites which have the greatest relative spread, usually with one or more close to the minimum elevation limit. By also taking into account environmental conditions such as expressed by J/S, it might be possible to select the set of 4 visible satellites which are least affected by jamming. However, time constraints and/or jammer interference (no data) might prevent the acquisition of a new satellite signal towards the end of a mission. Also, as the time remaining in the mission approaches zero, the INS error divergence approaches zero.

The navigation system aiding functions which constitute the basis for MFBARS navigation system design requirements are summarized in Table 7-1. The data processing design and computer sizing estimates for the MFBARS data processor are derived from these requirements.

7.3 MFBARS INTEGRATED NAVIGATION FILTER DESIGN

The most effective GPS/JTIDS/INS aiding is obtained by processing the GPS and JTIDS measurements and data from the INS mechanization algorithms in an integrated navigation filter as depicted in Figure 7-1. Included with the measurements are those from auxiliary sensors such as barometric altimeter.

A typical set of subsystem measurements is given in Table 7-2, which also lists the commonly used set of GPS, JTIDS and INS error parameters estimated by the navigation filter. These error estimates are used as infrequent corrections to the navigation states, obtained by frequently updating the navigation mechanization equations with the IMU outputs. Because the INS system errors grow slowly compared with the rate of growth of uncertainties in vehicle dynamics, the update rate of the integrated GPS-JTIDS-INS navigation filter can be much slower than for an

Table 7-1. MFBARS Integrated Navigation System Aiding

System	Function	Aided Operation	Aiding Data	Source
INS	Navigation	Use Kalman filter(s) to integrate the navigation functions based on GPS, JTIDS, INS (IMU), CADC.	Range, range rate Time of arrival (relative range) Altitude	GPS JTIDS CADC
GPS	Satellite Selection Acquisition and Reacquisition	Revised GDOP, J/S and or mission time criterion System time accuracy determines C/A or P code acquisition mode. Receiver search region is determined by position/ velocity uncertainty.	Vehicle position System time Position, velocity	INS JTIDS
	Tracking Antenna	Code tracking only Adaptive null steering array	Position, velocity None	INS -
JTIDS	Net entry Navigation	GPS and JTIDS time are synchronized for fast net entry Provide absolute navigation data to JTIDS NET	System time Position, velocity	GPS GPS/INS

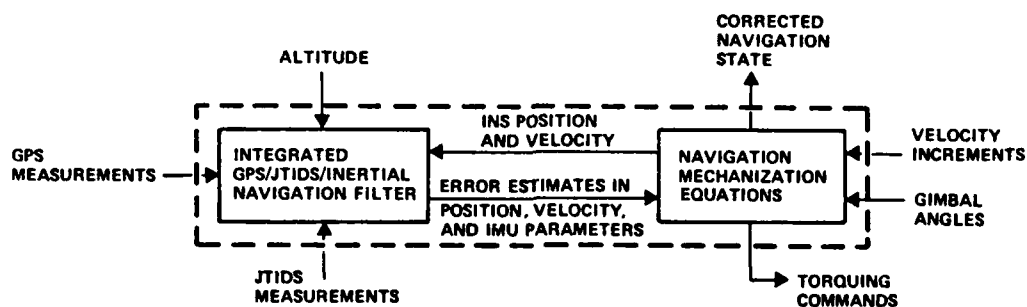


Figure 7-1. Integrated Navigation Filter

Table 7-2. Integrated Navigation Filter Measurements and Error Parameters

System	Measurements	Error Estimates
GPS	Pseudo range Pseudo range rate	User clock phase bias User clock frequency bias
JTIDS	Time of arrival (Relative range)	User clock phase bias User clock frequency bias Grid origin position Grid origin velocity Grid azimuth orientation
Inertial	Velocity increments Gimbal angles	Position Velocity Platform alignment Platform drift
CADC	Barometric altitude	Altitude reference

unaided GPS-JTIDS filter which does not use the IMU measurements. This greatly benefits the implementation of the Kalman filter algorithms, which require a substantial amount of execution time.

During periods when a reduced number or no GPS measurements are available because of jamming, JTIDS measurements should provide the navigation filter with inputs to generate the required error updates to the INS

navigation states. If both GPS and JTIDS are not available, then the in-flight estimation of IMU alignment made possible by the earlier availability of GPS and JTIDS should improve the INS navigation accuracy.

The use of a completely integrated GPS/JTIDS/INS filter has the following advantages:

- 1) Common, redundant filter states do not have to be carried along.
- 2) GPS derived geodetic position and velocity updates are immediately available for use in JTIDS navigation processing, without special interfaces and vice versa.
- 3) The IMU interfaces directly with a single filter.

In the case that the MFBARS navigation data processor has to interface with an existing avionics processor with INS navigation mechanization, then the INS position and velocity data can be directly processed by the integrated navigation filter. The use of two processors also adds a certain degree of redundancy to the system. For that reason it might also be desired to process the GPS and JTIDS measurements independently in GPS/INS and JTIDS/INS filters. Therefore, sizing and timing estimates have been developed for four different MFBARS navigation data processor design configurations as depicted in Figures 7-2 and 7-3. The first two designs use an integrated GPS/JTIDS filter, which interfaces with either a dedicated IMU or with a stand-alone INS. The remaining two designs use decoupled GPS and JTIDS navigation filters, which interface either with an IMU or an INS subsystem. The last system features only minimal data transfer between the GPS/INS and JTIDS/INS mechanizations. Table 7-3 describes each of the designs, its advantages and disadvantages.

7.4 MFBARS DATA PROCESSOR FUNCTIONAL DESIGN

This section describes the MFBARS data processing functional design for the four integrated navigation data processing configurations. Only the navigation filter and navigation integration function designs differ among the four configurations. Executive, initialization and control, and display functions form an integral part of the navigation system software and must be added to the functions given in Figures 7-2 and 7-3. The

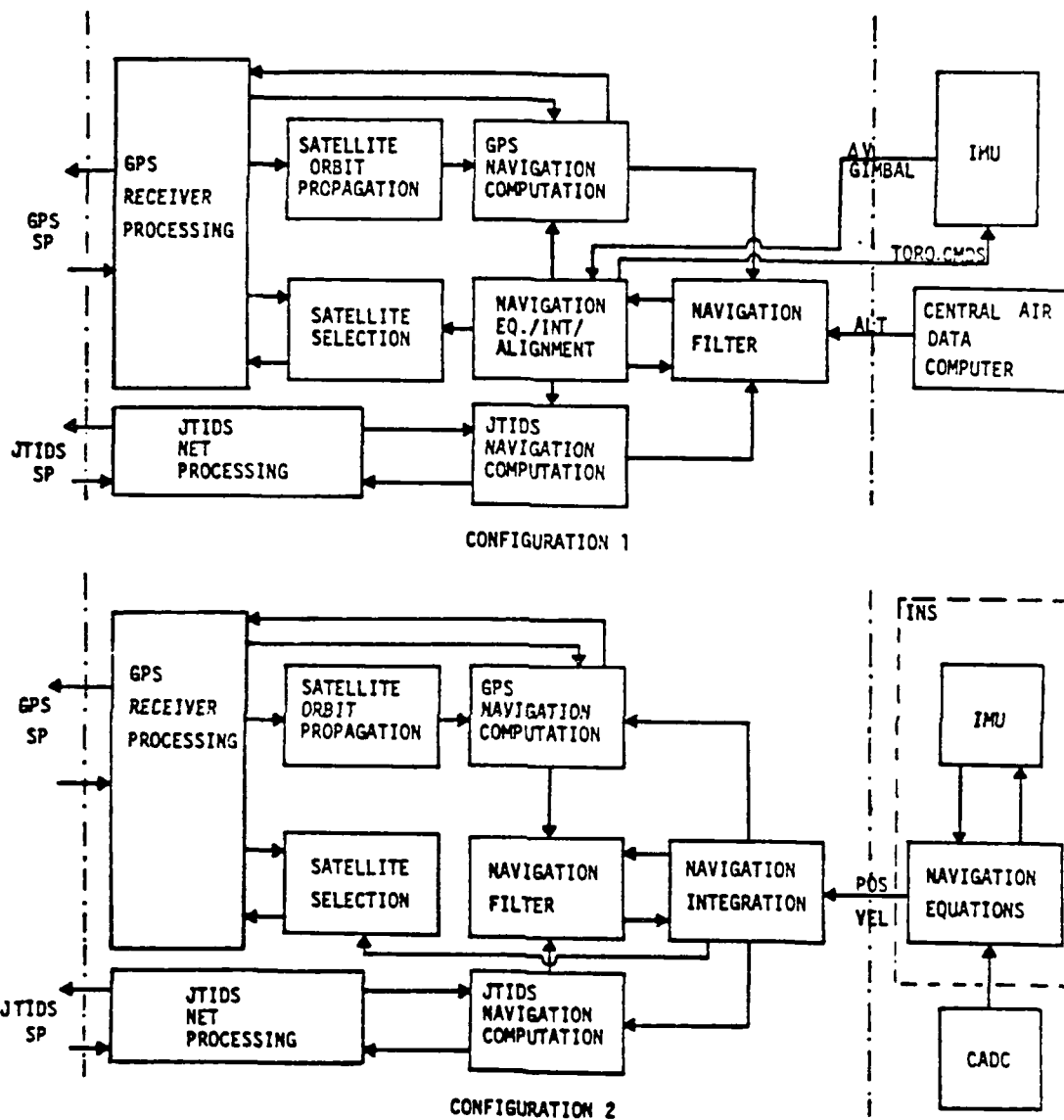
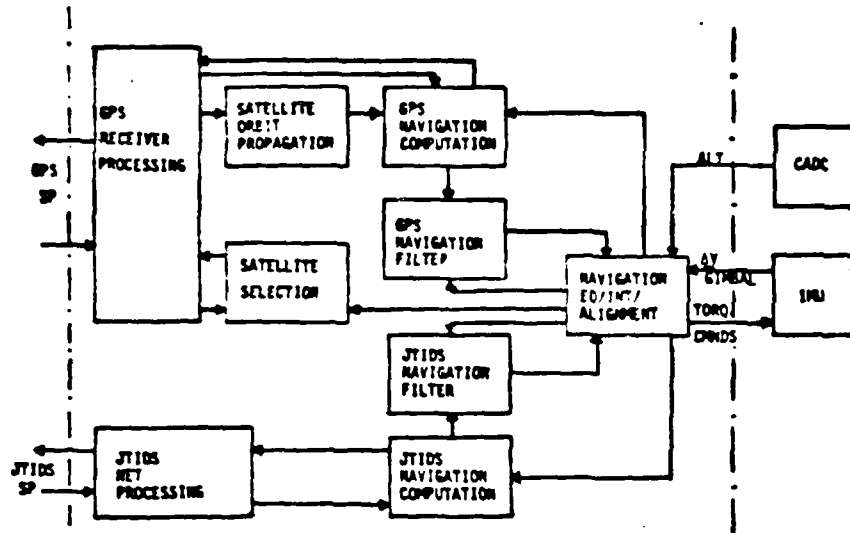
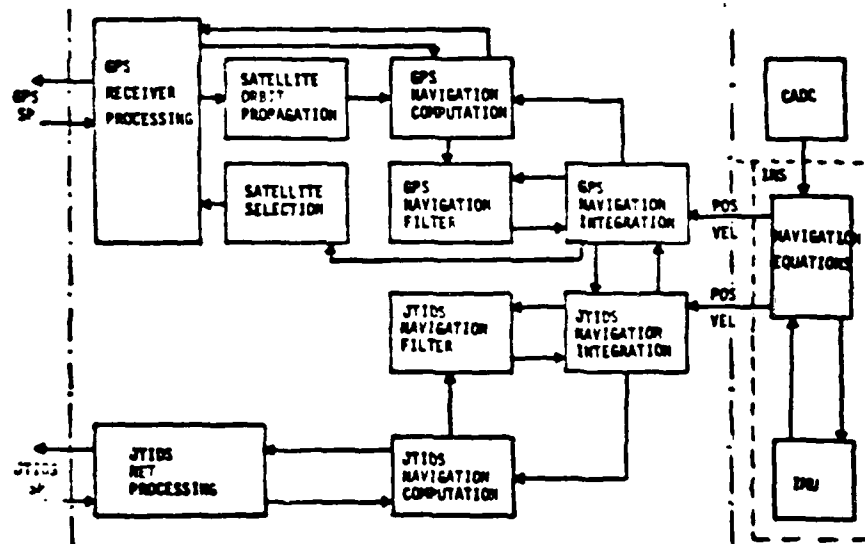


Figure 7-2. Integrated Inertial Navigation Data Processing Configurations with an Integrated Navigation Filter



CONFIGURATION 3



CONFIGURATION 4

Figure 7-3. Integrated Inertial Navigation Data Processing Configurations with Decoupled Navigation Filters

Table 7-3. Integrated Inertial Navigation Data Processing Characteristics

Configuration	Description	Advantages	Disadvantages
1	• Single navigation filter (22 states) • Inertial navigation and navigation filter in same processor	• No redundant filter states • Single interface with IMU • GPS data easily available to JTIDS and vice versa	• Navigation equation mechanization for dedicated IMU • Delay in JTIDS measurements complicates measurement processing
2	• Single navigation filter (22 states) • Inertial navigation in separate processor (INS)	• No redundant filter states • Single interface with INS • Can be integrated with existing avionics system • GPS data easily available to JTIDS and vice versa	• Position/velocity resolution determined by avionics computer/interface word length • Delay in JTIDS measurements complicates measurement processing
3	• GPS navigation filter (15 states) • JTIDS navigation filter (18 states) • Inertial navigation and filters in same processor	• Single interface with IMU • GPS data available to JTIDS and vice versa	• Redundant filter states • Navigation equation mechanization for dedicated IMU • Delay in JTIDS measurements complicates updating error states
4	• GPS navigation filter (15 states) • JTIDS navigation filter (18 states) • Independent integrated navigation • Inertial navigation separate (INS)	• GPS and JTIDS separately integrated with inertial navigation • Can be integrated with existing avionics system	• Redundant filter states • Position/velocity resolution limitation • Interface required for transfer of GPS data to JTIDS and vice versa

designs for these three functions are configuration-dependent and greatly influenced by the computer system architecture and the navigation, control, and display subsystem designs. The processing rates are consistent with the design requirements for aiding established in Section 7.2. These rates form the basis for the timing estimates given in Section 7.5.

7.4.1 GPS Satellite Selection Function

The GPS Satellite Selection function determines which four of the 24 satellites are to be initially acquired and, during navigation, which replacement satellites should be acquired to prevent deterioration of GDOP or loss of signal due to jammer interference or to a satellite dropping below the minimum elevation limit. Using almanac data and the vehicle geocentric state vector, the function calculates the vectors to all potentially visible satellites. Four satellites are selected dependent on atmospheric effects, mission requirements, satellite health and expected duration of satellite visibility, and minimum GDOP considerations. Following initial acquisition, the function is enabled every 300-500 seconds to compare the performance criterion for the currently used set of satellites to those for candidate replacement sets or to switch satellites because of large J/S or bad visibility.

7.4.2 GPS Satellite Orbit Propagation Function

The GPS Satellite Orbit Propagation function supplies precise satellite position and velocity states to the GPS Navigation Computation function for the estimation of range and range rate. These data are generated using sixth order polynomials. The polynomial coefficients are part of the satellite signal data contents, which are provided by the GPS Receiver Processing function and are updated once per hour. The geocentric satellite position output requires a word length of at least 29 bits and the corresponding velocity a minimum of 22 bits.

7.4.3 GPS Receiver Processing Function

The GPS Receiver Processing function forms the interface of the MFBARS data processor with the GPS receiver signal processor. This function processes control inputs to the receiver and calculates and formats the appropriate receiver aiding quantities for performing acquisition, reacquisition and code tracking. The aiding data are computed from the

range and its derivative data, received from the GPS navigation computation function by extrapolating to the appropriate time and, where necessary, applying lever arm corrections. From the receiver signal processor the function receives the data, code phase, and doppler reading for each of five receiver channels. Gross reasonableness checks are made on the measurement data which, if passed, are converted to pseudoranges and pseudorange rates. The four L_1 pseudoranges are corrected to compensate for the effects of tropospheric and ionospheric delays. The L_2 pseudorange measurement, which is sequentially obtained for the four satellites by the fifth receiver channel, is used as input to the ionospheric corrections for the satellite signals. These corrections are, among others, a function of the respective L_1 , L_2 pseudorange differences.

The measurements may also be corrected for lever arm effects and calibration constants. Pseudorange and pseudorange rate measurements to each of the four satellites are provided to the GPS navigation computation function at a maximum rate of 1/6 Hz. Satellite ephemeris updates are processed once per hour and output to the satellite orbit propagation function. The data used to calculate the aiding quantities is updated at a 10 Hz rate by the GPS navigation computation function.

7.4.4 GPS Navigation Computation Function

The GPS navigation computation function calculates estimated range and range rate relative to the four satellites being tracked from the geocentric vehicle and satellite position and velocity vectors obtained from the navigation integration and the satellite orbit propagation functions, respectively. The output data to the GPS Receiver Processing function may include higher order derivatives required to calculate the aiding quantities properly. The measurement residuals, which are output to the navigation filter function, are obtained by differencing the measured and estimated range and range rate values and applying the phase and frequency bias error corrections.

7.4.5 JTIDS Navigation Computation Function

The JTIDS navigation computation function calculates vehicle relative position and velocity for output to the JTIDS net processing function based on the inertial position, velocity estimates, and grid position, and

velocity and orientation estimates received from the navigation integration function. While this last function updates the input data at a 10 Hz rate, the JTIDS Net Processing function requires in principle only one position message every 12 seconds.

Three time-of-arrival (TOA) measurements are received from the JTIDS Net Processing function every 12 seconds. The measurement data includes the relative position state of the corresponding users. This data, combined with the user's own relative position and clock bias error estimates, are used to calculate the measurement residuals for output to the navigation filter function.

7.4.6 JTIDS Net Processing Function

The JTIDS net processing function provides the interface between the navigation data processor and the JTIDS receiver signal processor. The basic responsibility of this function is to establish and maintain synchronization and communication with the JTIDS nets. The processing that must be performed as part of this function consists of:

- 1) Slot-usage control for transmission and reception
- 2) Coarse and fine synchronization with JTIDS time
- 3) Time drift model maintenance
- 4) Gross error checking of incoming messages
- 5) Process time updating and time-slot message assignment
- 6) Position extrapolation to reflect expected user position at time of position message transmission.

The JTIDS Net Processing function as currently envisioned is extremely complex. A dedicated effort is required to define for tactical vehicles a user hierarchy and to establish a minimal net processing functional design. The software timing and sizing is based on such a design.

7.4.7 Navigation Filter Function

The navigation filter function implements a Kalman filter for processing the GPS, JTIDS, and altimeter measurements, which estimate the errors in the following 22 state variables.

- 1) Geographic vehicle position - 3 states
- 2) Geographic vehicle velocity - 3 states
- 3) Grid relative position - 2 states
- 4) Grid azimuth orientation - 1 state
- 5) Grid origin velocity - 2 states
- 6) Altitude reference error - 1 state
- 7) Platform alignment errors - 3 states
- 8) Platform drift errors - 3 states
- 9) User-clock phase bias - 2 states
- 10) User-clock frequency bias - 2 states

TRW experience with Kalman filter designs has established the virtues of: (1) writing the covariance propagation equations in conventional form as opposed to the square root mechanization, and (2) using a symmetrization procedure to prevent numerical stability problems. Performance is equivalent and the mechanization is substantially simpler than the square root mechanization. The measurement processing scheme to be incorporated in the integrated filter configuration design remains to be defined, since it depends on the finalization of the JTIDS net processing characteristics and the results of further performance analyses. A number of options are available to process the delayed JTIDS measurements: (1) maintain "synchronization" of the filter and navigation state times and propagate the measurements to that time, and (2) let filter time lag navigation state time, process all measurements chronologically and update the navigation state with error state estimates that have been propagated to the current navigation state time. The second approach is preferred over the first, since:

- (1) Kalman filter algorithms require a substantial execution time;
- (2) corrections to the navigation state can be made infrequently.

Additional savings in execution time are realized by sequentially processing the set of 4 GPS range and 4 GPS range rate measurements made at the same instant as 3 single measurements. This avoids having to compute the inverse of an 8 x 8 matrix, while time consuming state

propagations and covariance matrix extrapolations do not have to be performed between the processing of the 8 measurements.

The filter design incorporates a 12 second cycle. Computer sizing and timing estimates are based on processing a maximum of 2 sets of 8 GPS measurements each, 3 JTIDS range measurements, and 6 altimeter measurements during this cycle. A reduction of the state vector from 22 to 19 state variables appears feasible without affecting performance much by deleting the platform drift bias states. And if all JTIDS net members possess a GPS capability, then only one set of user-clock states is required, thereby further reducing the number of state variables to 17.

Separate Kalman filters must be implemented for the configurations with decoupled filters. The GPS/INS navigation filter contains as state vector elements:

1) Vehicle position	- 3 states
2) Vehicle velocity	- 3 states
3) Altitude reference error	- 1 state
4) Platform alignment errors	- 3 states
5) Platform drift errors	- 3 states
6) User-clock phase bias	- 1 state
7) User-clock frequency bias	- 1 state

The JTIDS/INS navigation filter uses a state vector consisting of the following elements:

1) Vehicle position	- 2 states
2) Vehicle velocity	- 2 states
3) Grid-relative position	- 2 states
4) Grid-azimuth orientation	- 1 state
5) Grid origin velocity	- 2 states
6) Altitude reference error	- 1 state
7) Platform alignment errors	- 3 states
8) Platform drift errors	- 3 states

- 9), User-clock phase bias - 1 state
- 10) User-clock frequency bias - 1 state

The basic design considerations discussed above for the integrated navigation filter apply to the individual filters as well.

7.4.8 Navigation Integration Function

The navigation integration function maintains and propagates the integrated system navigation state. The complexity of this function depends heavily on the selected configuration. If the navigation integration function interfaces directly with the IMU, then the IMU mechanization algorithms become an integral part of this function. It must not only propagate the navigation state using the incremental velocity output of the IMU at a minimum 10 Hz rate to accurately follow vehicle dynamics, it must also accomplish gyrocompassing for preflight alignment of the inertially stabilized frame in the case of a stable platform implementation. For that implementation the function also computes the gyrotorquing commands required to maintain the IMU in a local level orientation. Periodically the navigation state is corrected with the error estimates supplied by the navigation filter(s).

In the case with a separate INS, the navigation integration function is no longer responsible for IMU platform management. Instead, the navigation state is received from the INS at a 10 Hz rate. The function propagates the navigation state for use by the navigation filter and aiding functions, and incorporates the filter error estimates as required.

7.5 MFBARS DATA PROCESSOR SIZING AND TIMING ESTIMATES

The MFBARS navigation data processor sizing and timing estimates for the four integrated navigation data processor configurations are summarized in Table 7-4. These estimates reflect the functional design described in Section 7-4 and are based in part on the sizing data given in References 4 and 5. Table 7-4 shows that the maximum required word-length is 32 bits, hence, if a 16-bit computer is used, a double precision capability must be provided. Either fixed-point or floating-point arithmetic may be implemented. The storage estimates combine the instruction and data memory requirement for which a 3:1 ratio is assumed. Furthermore, the instructions

Table 7-4. Data Processing Sizing and Timing Estimates

Function	Precision (bits)	Configuration 1		Configuration 2		Configuration 3		Configuration 4	
		Storage* (16-bit Words)	Timing** (ms/sec)	Storage* (16-bit Words)	Timing** (ms/sec)	Storage* (16-bit Words)	Timing** (ms/sec)	Storage* (16-bit Words)	Timing** (ms/sec)
Executive	16	6,500	40	6,000	30	6,250	35	6,500	40
Initialization	16	3,000		3,000		3,500		3,500	
Satellite selection	32	3,000	15	3,000	15	3,000	15	3,000	15
Satellite orbit propagation	32	1,200	30	1,200	30	1,200	30	1,200	30
GPS receiver processing	32	5,000	90	5,000	90	5,000	90	5,000	90
GPS navigation computation	32	1,500	20	1,500	20	1,500	20	1,500	20
JTIOS navigation computation	16	2,000	30	2,000	30	2,000	30	2,000	30
JTIOS net processing	16	9,000	90	9,000	90	9,000	90	9,000	90
Navigation filter	32	15,000	90	15,000	90				
GPS navigation filter	32					8,000	20	8,000	20
JTIOS navigation filter	32					11,000	40	11,000	40
Navigation integration	16	6,500	70	3,000	30	6,500	75		
GPS navigation integration	16							2,000	30
JTIOS navigation integration	16							2,500	30
Control and display	16	5,000	50	4,500	50	5,000	50	5,000	50
Self-test	16	1,500		1,500		1,500		1,500	
Math subroutines	32	1,200		1,200		1,200		1,200	
Total		60,400	525	55,900	475	64,650	495	62,900	485

*Instructions and data

**Based on 1 MIPS CPU

represent an assembly language software implementation. A 30 percent inefficiency factor is assumed if an Higher Order Language (HOL) such as FORTRAN is used. Hence, the software development cost estimate derived in Section 8 is based on the Configuration 1 estimate of $0.75 \times 1.3 \times 60,400 = 58,890$ 16-bit machine language instructions programmed in HOL.

The timing estimates of Table 7-4 are developed for a computer with a one MIPS CPU. The data shows the maximum execution time in milliseconds of a function during a one second period. The data in Table 7-4 reflects a CPU utilization of 52.5, 47.5, 49.5, and 48.5 percent for the respective configurations. The use of an HOL might increase these values somewhat. Considering the design uncertainties and allowing for future growth a one MIPS processor with the equivalent of a 128,000 16-bit memory capacity is recommended for the MFBARS data processing implementation.

7.6 MFBARS INTEGRATED INERTIAL NAVIGATION STUDY RECOMMENDATIONS

The MFBARS integrated inertial navigation study conducted as part of the MFBARS Phase II add-on task has been limited in scope. Navigation system software requirements have been generated for four-candidate integrated inertial navigation system configurations for tactical aircraft operating in a jammer environment. The requirements are derived for navigation systems consisting of GPS, JTIDS, gimballed inertial measurement unit, and barometric altimeter operating throughout the entire mission. Configuration 1 has, from an integration point of view, a number of advantages; however, its performance must be demonstrated under simulated tactical mission conditions. The final design must, besides performance, reflect considerations as reliability, maintainability and testability. However, the task recommendations for a follow-on study emphasize the operability and performance aspects of a MFBARS integrated navigation system design.

Task 1: Establish subsystem operability as a function of mission phase.

The integrated navigation system design is based on the assumption that the JTIDS system provides an effective backup for INS aiding in the absence of GPS, i.e., when operating under heavy jamming conditions. For this assumption to be valid, it must be demonstrated first of all that an effective JTIDS net can be established and maintained during those mission

phases. As part of this task, tactical mission phases will be defined and subsystem operability requirements will be established for each phase. It will next be determined if these requirements can be satisfied.

Task 2: Investigate alternate satellite selection/switching schemes.

The GDOP criterion, generally used for satellite selection, only considers the geometrical aspects in determining the optimum set of satellites. This may result in the selection of one or more satellites with a low elevation angle. The signals from these satellites are extremely sensitive to interference from ground-based jammers and, consequently, may lose lock easily. This task will analyze the effect of land and space-based jammers on satellite signals as a function of satellite vehicle geometry. Based on the results, alternate selection schemes, which may include the use of J/S and mission time in addition to GDOP, will be defined and evaluated.

Task 3: Determine minimum set of JTIDS net processing requirements.

Present JTIDS net processing designs are extremely complicated and require a large amount of computer resources. Based on the results of the operations analysis of Task 1, the net processing requirements for tactical vehicle applications will be evaluated under this task to determine the minimum set which must be supported by the MFBARS terminal. Special emphasis will be placed on the measurement selection scheme in support of the measurement processing analysis addressed in the next task.

Task 4: Perform integrated navigation system performance analysis.

Although navigation system performance of the integrated designs must be demonstrated in general, the impact of the concurrent processing of JTIDS and GPS measurements on system performance requires special attention. Typically, the JTIDS net processing function determines, based on data quality measures, which set of 3 measurements within a 12 second time slot should be processed by the navigation filter. As a result the measurements may become available to the filter with delays of more than 12 seconds, thereby requiring either propagation to the current filter time or delaying GPS measurement processing. This task will investigate the impact on navigation performance of these measurement processing approaches. The results of Task 3, concerning the designation of user measurements, will be

incorporated in this task. Use of a system or scientific simulation is mandatory for this analysis.

Task 5: Investigate application of alternate navigation subsystems.

The present design study was based on a gimballed IMU and made assumptions concerning the operational availability of JTIDS. If Task 1 shows that these assumptions are not valid and/or if Task 4 shows that performance in general is unacceptable, then additional GPS aiding might be required. The application of a strapdown inertial measurement unit, although requiring increased computer resources, has several distinct advantages. Elimination of gimbals leads to lower system costs, smaller mechanical and electrical form factor, and increased reliability. However, the proper resolution of acceleration information requires rapid updating of the transformation matrices relating body and navigation coordinate frames. The availability of attitude and angular rate in a high-speed digital format could provide the antenna motion velocity compensation necessary for code loop aiding and maybe antenna array pointing. The smaller physical size of a strapdown IMU may enable mounting close to the antenna, thereby making lever arm motion effects negligible. This task will investigate the impact on integrated inertial navigation system design and performance for alternate navigation system complements, especially the use of a strapdown IMU in place of a gimballed IMU.

The tasks identified above are interrelated. The data flow between the tasks is indicated in Figure 7-4.

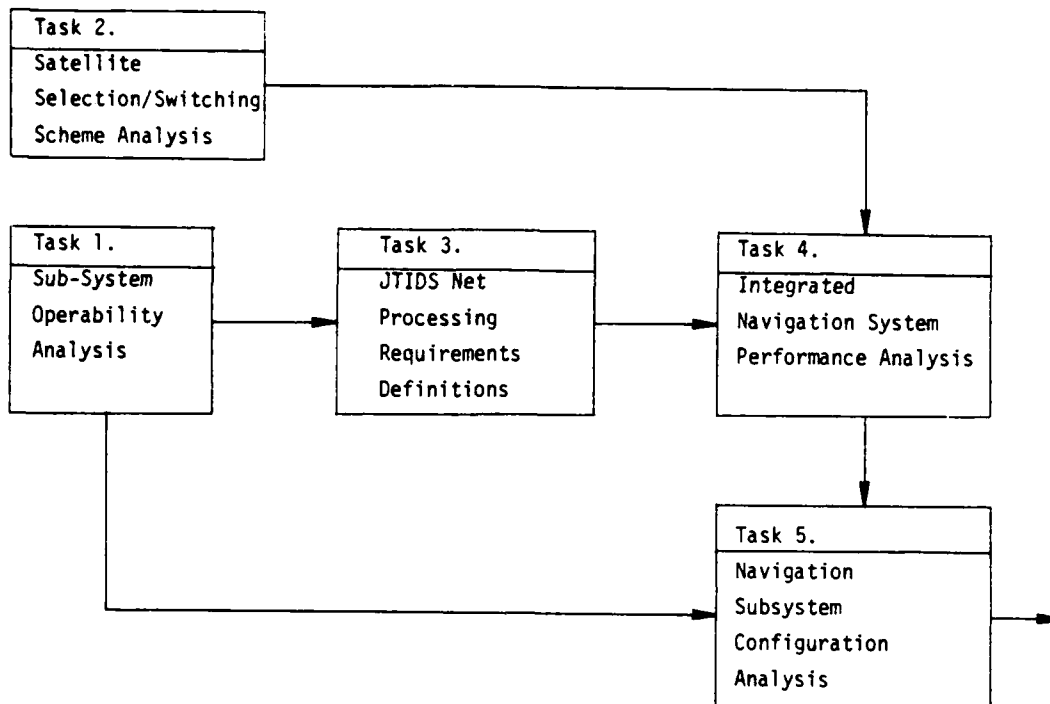


Figure 7-4. Task Data Flow

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8. PHASE I ECONOMIC ANALYSIS

The MFBARS program employed six cost models to study the acquisition, production, logistic support and software costs. These models were (1) AF Logistic Support Cost Model-Mini, (2) Marine Corps TRI TAC Cost model, (3) RCA's PRICE-H model, (4) RCA's PRICE-S model, (5) RCA's PRICE-L model, and (6) TRW's Software Cost Estimation Program (SCEP) software model. The PRICE models were run by the customer from input sheets provided by TRW.

8.1 MODEL DESCRIPTION

8.1.1 TRW Software Cost Estimation Program (SCEP)

SCEP is a computer model which accepts a hierarchial description of a software project in terms of 14 distinct parameters, and provides labor estimates for completion of the project. The model covers the costs associated with preliminary design, detailed design, coded unit test, and integration test.

8.1.2 PRICE Software Model

The PRICE software model takes into consideration 10 distinct parameters and provides an output in terms of dollar-cost or man-months (months required to perform the various phases of the job and schedule information and sensitivity data). The model computes the costs associated with design, implementation and test, and integration.

8.1.3 PRICE H Model

PRICE (Programmed Review of Information for Costing and Evaluation) provides estimates for engineering development prototype and production costs. These costs are developed from physical characteristics of the design concepts such as weight, volume, quantity of units, types of components, type of construction, and complexity.

8.1.4 AF Logistics Support Cost Model-Mini

The mini LSC model estimates the support cost expected by adapting a particular design concept and support philosophy. Inputs to the model fall into the following categories:

- a) System variables. Force operating hours, service life, fraction employed overseas.
- b) Software constants. Programmer cost and turnover rate, number of instructions and complexity, percent of expected changes.
- c) Subsystem variables. Depot and base labor rate, number of man-hours per month available.
- d) LRU variables. MTBF, unit cost, average fault isolation/repair times at both base and depot, unit weight, etc.
- e) AGE variables. Cost of AGE, base and depot utilization rate, percent downtime.

The model calculates four equations:

- a) Initial and replacement LRU spare costs
- b) Off-equipment maintenance costs
- c) Support equipment costs
- d) Software acquisition and maintenance costs.

The model calculates the costs associated with the number of operating-bases input by the analyst, but assumes one depot activity.

8.1.5 TRI TAC Computer Model for Life Cycle Costing

The model employs a set of 69 input cost elements to compute the annual operating and support costs, as well as the life cycle cost.

Annual operating and support costs are listed as:

- a) Electric power
- b) Special materials
- c) Maintenance personnel
- d) Support equipment maintenance
- e) Software maintenance
- f) Supply personnel

- g) Spare parts and repair materials
- h) Inventory
- i) Transportation.

These computed costs are combined with three-point estimates determined by the analyst (R&D estimate, software procurement, and software maintenance cost) to provide the life cycle costs. The total life cycle cost is divided into three main groups: (1) R&D, (2) investment, and (3) operations and logistics support.

8.2 PHASE I BASELINE CONFIGURATION ECONOMIC RESULTS

The baseline architecture (Figure 8-1) is a distributed configuration consisting of one processor and three transmitters.

The "(1 RF/ 1 syn)" of Figure 8-1 refers to the use of one RF and one synthesizer module for the function.

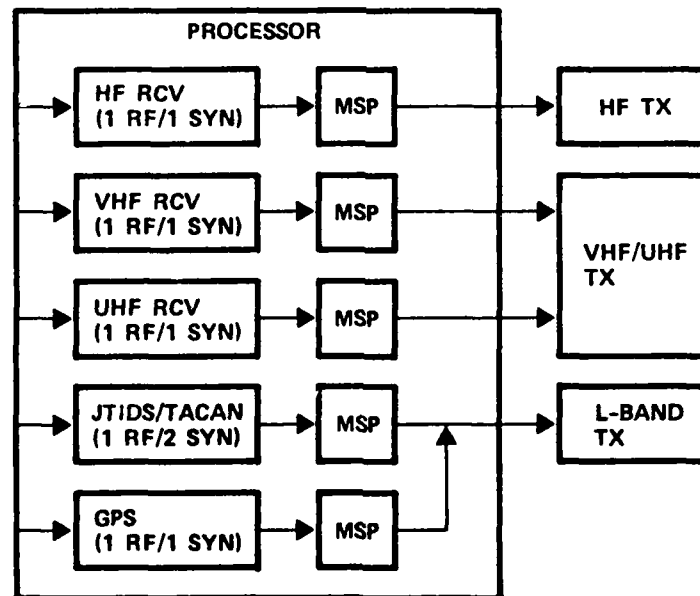


Figure 8-1. Phase I Baseline Architecture

The following maintenance concept was used in order to complete the input data for the LSC and LCC models:

- Remove/replace an LRU at the organizational level
- Repair and retest an LRU at the intermediate level by removal/replacement of SRUs (modules)
- SRU repair at the depot with back-up LRU test capability for a small percentage of very difficult LRU repairs.

8.2.1 Software Acquisition Costs

Three models were used to predict the software acquisition costs. The models and their results are as follows:

<u>Model</u>	<u>Cost</u>	<u>Result</u>
TRW's SCEP	\$524,210	87.4 MM
LSC-Mini	\$655,500	109.8 MM
Price-S	\$983,000	163.8 MM

All costs were computed in 1978 dollars with one man-month equal to \$6,000.

The SCEP computer output data sheets are found in Table 8-1, Price Software model data sheets are Table 8-2, and the LSC-Mini in Table 8-3.

8.2.2 Software Support Costs

The logistics support cost model mini version is the only model that predicts software support costs. Support costs for the baseline system over the 10-year life of the program equals \$248,775. This value is also in 1978 dollars.

8.2.3 Logistics Support Costs

The logistics support model used in this analysis is the Mini-LSC, version 1.3 AFALD/AQS, Space and Missile Systems Organization, Los Angeles, California.

Table 8-1. TRW Software Cost Estimating Program

VERSION SCEP1.0

DATE 10/12/78.

SYSTEM MFBARS

ESTIMATED EFFORT BY PHASE IN MANMONTHS

TOTAL SYSTEM

PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	*DEMI	DEMI/MM
9.0	25.5	22.0	30.8	87.4	13400	153.4

BY SUBSYSTEM

S/S	IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
1	JTI	.2	.8	1.2	1.1	3.3	500	151.2
2	GPSM	.1	.5	.7	.7	2.0	300	151.2
3	GPSH	8.3	23.4	16.7	27.7	78.1	12000	153.6
4	HF	.3	.9	1.4	1.3	4.0	600	151.2

*DEMI-Deliverable
Executable
Machine
Instruction

Table 8-1. TRW Software Cost Estimating Program (Continued)

BY UNIT

SUBSYSTEM 1 JTI

UNIT IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
1 JTIDS	.0	.2	.2	.2	.7	100	151.2
2 TACAN	.0	.2	.2	.2	.7	100	151.2
3 IFF	.0	.2	.2	.2	.7	100	151.2
4 I/O	.0	.2	.2	.2	.7	100	151.2
5 EXEC	.0	.2	.2	.2	.7	100	151.2

SUBSYSTEM 2 GPSM

UNIT IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
1 GPS	.0	.2	.2	.2	.7	100	151.2
2 EXEC	.0	.2	.2	.2	.7	100	151.2
3 I/O	.0	.2	.2	.2	.7	100	151.2

SUBSYSTEM 3 GPSH

UNIT IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
1 MICRO	8.3	23.4	18.7	27.7	78.1	12000	153.0

SUBSYSTEM 4 HF

UNIT IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
1 HF	.0	.2	.2	.2	.7	100	151.2
2 VHF	.0	.2	.2	.2	.7	100	151.2
3 UHF	.0	.2	.2	.2	.7	100	151.2
4 SEEKTAIK	.0	.2	.2	.2	.7	100	151.2
5 EXEC	.0	.2	.2	.2	.7	100	151.2
6 I/O	.0	.2	.2	.2	.7	100	151.2

Table 8-1. TRW Software Cost Estimating Program (Continued)

VERSION SCEP1.0

DATE 10/12/78.

SYSTEM MFBARS

ESTIMATED EFFORT BY PHASE IN DOLLARS

TOTAL SYSTEM

PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
54033	153146	131938	185093	524210	13400	39.12

BY SUBSYSTEM

S/S	IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
1	JTI	1495	4626	7066	5658	19845	500	39.69
2	GPSM	897	2776	4239	3995	11907	300	39.69
3	GPSH	49845	140192	112154	166450	468642	12000	39.05
4	HF	1794	5552	8479	7990	23815	600	39.69

Table 8-1. TRW Software Cost Estimating Program (Continued)

BY UNIT

SUBSYSTEM 1 JTI

UNIT IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
1 JTIDS	299	925	1413	1332	3969	100	39.69
2 TACAN	299	925	1413	1332	3969	100	39.69
3 IFF	299	925	1413	1332	3969	100	39.69
4 I/O	299	925	1413	1332	3969	100	39.69
5 EXEC	299	925	1413	1332	3969	100	39.69

SUBSYSTEM 2 GPSM

UNIT IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
1 GPS	299	925	1413	1332	3969	100	39.69
2 EXEC	299	925	1413	1332	3969	100	39.69
3 I/O	299	925	1413	1332	3969	100	39.69

SUBSYSTEM 3 GPSH

UNIT IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
1 MICRO	49946	140192	112154	166450	468642	12000	39.05

SUBSYSTEM 4 HF

UNIT IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
1 HF	299	925	1413	1332	3969	100	39.69
2 VHF	299	925	1413	1332	3969	100	39.69
3 UHF	299	925	1413	1332	3969	100	39.69
4 SEEKTAIK	299	925	1413	1332	3969	100	39.69
5 EXEC	299	925	1413	1332	3969	100	39.69
6 I/O	299	925	1413	1332	3969	100	39.69

Table 8-2. Price Software Model

DATE 10/12/78 TIME 14:07:48

ASSEM

MFBARS

FILENAME: MFBARS

INPUT DATA

DATED: 9/23/78

DESCRIPTORS					
INSTRUCTIONS	1400	APPLICATION	0.0	RESOURCE	0.000
FUNCTIONS	0	STRUCTURE	0.0	LEVEL	0.0
				INTEGRATION	0.500

APPLICATION CATEGORIES		NEW DEVELOPMENT		SYSTEM CONFIGURATION	
	MIX	DESIGN	CODE	TYPES	QUANTITY
DATA S/R	0.0	1.00	1.00	0	0
ONLINE COMM	0.0	1.00	1.00	0	0
REALTIME C&C	1.00	1.00	1.00	0	0
INTERACTIVE	0.0	1.00	1.00	0	0
MATHEMATICAL	0.0	1.00	1.00	***	***
STRING MANIP	0.0	1.00	1.00	***	***
OPR SYSTEMS	0.0	1.00	1.00	***	***

SCHEDULE					
COMPLEXITY	1.100	IMPL START	0	T&I START	0
DESIGN START	AUG 84	IMPL END	0	T&I END	0
DESIGN END	0				

SUPPLEMENTAL INFORMATION					
YEAR	1984	ESCALATION	0.0	TECH IMP	1.00
MULTIPLIER	1.000	PLATFORM	1.8	UTILIZATION	0.50

PROGRAM COSTS

COST ELEMENTS	DESIGN	IMPL	T & I	TOTAL
SYSTEMS ENGINEERING	25.	1.	21.	47.
PROGRAMMING	4.	7.	8.	19.
CONFIGURATION CONTROL	4.	1.	10.	15.
DOCUMENTATION	3.	0.	4.	7.
PROGRAM MANAGEMENT	2.	0.	2.	4.
TOTAL	38.	10.	45.	93.

ADDITIONAL DATA

DESCRIPTORS				
INSTRUCTIONS	1400	APPLICATION	8.460	RESOURCE
FUNCTIONS	16	STRUCTURE	0.0	LEVEL
				0.0

SCHEDULE				
COMPLEXITY	1.100	IMPL START	SEP 84	T&I START
DESIGN START	AUG 84	IMPL END	JAN 85	T&I END
DESIGN END	NOV 84			NOV 84
				APR 85

SCHEDULE GRAPH

AUG 84

***** DESIGN *****

***** IMPLEMENT *****

***** TEST & INTEGRATE *****

Table 8-2. Price Software Model (Continued)

DATE 10/12/78 TIME 14:09:14

ASSEM

MFBNAL

SENSITIVITY DATA

R E S O U R C E	COMPLEXITY					
	1.000		1.100		1.200	
2.900	COST	83.	COST	89.	COST	95.
	MONTHS	7.0	MONTHS	7.8	MONTHS	8.6
3.000	COST	87.	COST	93.	COST	100.
	MONTHS	7.1	MONTHS	7.8	MONTHS	8.6
3.100	COST	90.	COST	97.	COST	104.
	MONTHS	7.1	MONTHS	7.9	MONTHS	8.7

SCHEDULE EFFECT SUMMARY

ACTIVITY LENGTH IN MONTHS				
COMPLEXITY = 1.100	DESIGN	IMPL	T & I	TOTAL
SPECIFIED SCHEDULE (OVERLAP)	3.4 (2.2)	3.7 (2.4)	5.3	7.6
TYPICAL SCHEDULE (OVERLAP)	3.4 (2.2)	3.7 (2.4)	5.3	7.6

DEVELOPMENT COSTS				
COMPLEXITY = 1.100	DESIGN	IMPL	T & I	TOTAL
SPECIFIED SCHEDULE	38.	10.	45.	93.
TYPICAL SCHEDULE	38.	10.	45.	93.
ESTIMATED PENALTY	0.	0.	0.	0.

Table 8-2. Price Software Model (Continued)

DATE 10/12/78 TIME 14:11:04

ASSEM		% COMPLETED				\$ EXPENDED		% EXPENDED		MFBARS	
:	:	MONTH	DESIGN	IMPL	T & I	THIS MONTH	TOTAL	THIS MONTH	TOTAL	:	
:	:	AUG 84	13.7	0.0	0.0	5.2	5.2	5.6	5.6	:	
:	:	SEP 84	67.6	0.5	0.0	20.6	25.9	22.2	27.8	:	
:	:	OCT 84	96.6	23.2	0.0	13.4	39.2	14.4	42.2	:	
:	:	NOV 84	100.0	70.9	1.2	6.7	46.0	7.3	49.5	:	
:	:	DEC 84	100.0	98.7	10.2	6.9	52.9	7.4	56.8	:	
:	:	JAN 85	100.0	100.0	33.0	10.3	63.2	11.1	67.9	:	
:	:	FEB 85	100.0	100.0	67.4	15.3	78.5	16.5	84.4	:	
:	:	MAR 85	100.0	100.0	96.9	13.2	91.6	14.1	93.5	:	
:	:	APR 85	100.0	100.0	100.0	1.4	93.0	1.5	100.0	:	
#	#	ALPHA	=	0.82	0.0	FOR PROFILE GRAPHS					#
#	#	BETA	=	0.18	1.00	RESPOND OK = 7					#
#	#	PEAK/AV	=	1.93	1.88						#

Table 8-2. Price Software Model (Continued)

DATE 10/12/78 TIME 14:12:03

HOL

FILENAME: MFBARS INPUT DATA MFBARS

DATED: 9/28/77

DESCRIPTORS					
INSTRUCTIONS	12000	APPLICATION	0.0	RESOURCE	3.000
FUNCTIONS	0	STRUCTURE	0.0	LEVEL	0.0
				INTEGRATION	0.500

APPLICATION CATEGORIES		NEW DEVELOPMENT		SYSTEM CONFIGURATION	
MIX		DESIGN	CODE	TYPES	QUANTITY
DATA S/R	0.0	1.00	1.00	0	0
ONLINE COMM	0.0	1.00	1.00	0	0
REALTIME C&C	1.00	1.00	1.00	0	0
INTERACTIVE	0.0	1.00	1.00	0	0
MATHEMATICAL	0.0	1.00	1.00	***	***
STRING MANIP	0.0	1.00	1.00	***	***
OPR SYSTEMS	0.0	1.00	1.00	***	***

SCHEDULE					
COMPLEXITY	1.100	IMPL START	0	T&I START	0
DESIGN START	AUG 84	IMPL END	0	T&I END	0
DESIGN END	0				

SUPPLEMENTAL INFORMATION					
YEAR	1984	ESCALATION	0.0	TECH IMP	1.00
MULTIPLIER	1.000	PLATFORM	1.8	UTILIZATION	0.50

PROGRAM COSTS				
COST ELEMENTS	DESIGN	IMPL	T & I	TOTAL
SYSTEMS ENGINEERING	193.	10.	162.	370.
PROGRAMMING	35.	52.	66.	153.
CONFIGURATION CONTROL	37.	15.	101.	152.
DOCUMENTATION	33.	5.	45.	84.
PROGRAM MANAGEMENT	22.	5.	20.	47.
TOTAL	324.	87.	395.	806.

ADDITIONAL DATA				
DESCRIPTORS				
INSTRUCTIONS	12000	APPLICATION	8.460	RESOURCE
FUNCTIONS	133	STRUCTURE	0.0	LEVEL
				3.000
				0.0

SCHEDULE				
COMPLEXITY	1.100	IMPL START	NOV 84	T&I START
DESIGN START	AUG 84	IMPL END	JUL 85	FEB 85
DESIGN END	MAR 85			JAN 85

SCHEDULE GRAPH

AUG 84

***** DESIGN *****

***** IMPLEMENT *****

***** TEST & INTEGRATE *****

JAN 85

Table 8-2. Price Software Model (Continued)

DATE 10/12/78 TIME 14:13:37

HOL

MFBARS

SENSITIVITY DATA

R E S O U R C E	COMPLEXITY					
	1.000		1.100		1.200	
	2.900		3.000		3.100	
	COST	706.	COST	767.	COST	831.
	MONTHS	15.5	MONTHS	17.3	MONTHS	19.1
	COST	743.	COST	806.	COST	874.
	MONTHS	15.6	MONTHS	17.4	MONTHS	19.1
	COST	779.	COST	847.	COST	918.
	MONTHS	15.7	MONTHS	17.5	MONTHS	19.2

SCHEDULE EFFECT SUMMARY

ACTIVITY LENGTH IN MONTHS				
COMPLEXITY = 1.100	DESIGN	IMPL	T & I	TOTAL
SPECIFIED SCHEDULE (OVERLAP)	7.5 (4.8)	8.3 (5.3)	11.8	17.4
TYPICAL SCHEDULE (OVERLAP)	7.5 (4.8)	8.3 (5.3)	11.8	17.4

DEVELOPMENT COSTS				
COMPLEXITY = 1.100	DESIGN	IMPL	T & I	TOTAL
SPECIFIED SCHEDULE	324.	87.	395.	806.
TYPICAL SCHEDULE	324.	87.	395.	806.
ESTIMATED PENALTY	0.	0.	0.	0.

Table 8-2. Price Software Model (Continued)

DATE 10/12/78 TIME 14:15:37

HOL

MFBARS

MONTH	% COMPLETED			\$ EXPENDED			% EXPENDED		
	DESIGN	IMPL	T & I	THIS MONTH	TOTAL	THIS MONTH	TOTAL	THIS MONTH	TOTAL
AUG 84	3.3	0.0	0.0	10.6	10.6	1.3	1.3	1.3	1.3
SEP 84	22.8	0.0	0.0	63.3	73.9	7.9	7.9	9.2	9.2
OCT 84	48.3	0.0	0.0	82.9	156.8	10.3	10.3	19.4	19.4
NOV 84	71.3	0.9	0.0	75.1	231.9	9.3	9.3	28.6	28.6
DEC 84	87.5	7.7	0.0	58.5	290.3	7.3	7.3	36.0	36.0
JAN 85	96.4	22.5	0.0	41.7	332.1	5.2	5.2	41.2	41.2
FEB 85	99.6	43.3	0.1	28.9	361.0	3.6	3.6	44.8	44.8
MAR 85	100.0	65.7	0.8	23.7	384.7	2.9	2.9	47.7	47.7
APR 85	100.0	84.5	3.0	24.9	409.6	3.1	3.1	50.8	50.8
MAY 85	100.0	96.1	7.3	27.2	436.8	3.4	3.4	54.2	54.2
JUN 85	100.0	99.9	14.4	31.2	468.1	3.9	3.9	58.0	58.0
JUL 85	100.0	100.0	24.5	40.0	508.1	5.0	5.0	63.0	63.0
AUG 85	100.0	100.0	37.5	51.4	559.5	6.4	6.4	69.4	69.4
SEP 85	100.0	100.0	52.8	60.5	619.9	7.5	7.5	76.9	76.9
OCT 85	100.0	100.0	69.1	64.6	684.5	8.0	8.0	84.9	84.9
NOV 85	100.0	100.0	84.5	60.8	745.3	7.5	7.5	92.4	92.4
DEC 85	100.0	100.0	96.1	45.6	790.8	5.7	5.7	98.1	98.1
JAN 86	100.0	100.0	100.0	15.6	806.4	1.9	1.9	100.0	100.0
FOR PROFILE GRAPHS									
# ALPHA	=	0.82	0.0	0.0					
# BETA	=	0.18	1.00	0.18					
# PEAK/AV	=	1.93	1.88	1.93					
RESPOND OK = 7									

Table 8-2. Price Software Model (Continued)

SYSTEM INTEGRATION
DATE 10/12/73 TIME 14:15:55

SYSTEM INTEGRATION MFBARS

FILENAME: MFBARS INPUT DATA DATED: 9/26/77

SCHEDULE					
COMPLEXITY	1.100				
DESIGN START	JAN 85	IMPL START	0	T&I START	0
DESIGN END	0	IMPL END	0	T&I END	0

SUPPLEMENTAL INFORMATION					
YEAR	1984	ESCALATION	0.0	TECH IMP	1.00
MULTIPLIER	1.000	PLATFORM	1.8	UTILIZATION	0.50

PROGRAM COSTS				
COST ELEMENTS	DESIGN	IMPL	T & I	TOTAL
SYSTEMS ENGINEERING	23.	1.	19.	43.
PROGRAMMING	4.	6.	8.	18.
CONFIGURATION CONTROL	3.	1.	9.	13.
DOCUMENTATION	3.	0.	4.	7.
PROGRAM MANAGEMENT	2.	0.	2.	4.
TOTAL	35.	9.	40.	84.

ADDITIONAL DATA

SCHEDULE					
COMPLEXITY	1.100				
DESIGN START	JAN 85	IMPL START	FEB 85	T&I START	MAR 85
DESIGN END	APR 85	IMPL END	JUN 85	T&I END	SEP 85

SCHEDULE GRAPH

JAN 85 SEP 85

***** DESIGN *****

***** IMPLEMENT *****

***** TEST & INTEGRATE *****

Table 8-2. Price Software Model (Continued)

SUMMARY OF SOFTWARE DEVELOPMENT TOTALS

COST ELEMENTS	PROGRAM COSTS				TOTAL
	DESIGN	IMPL	T & I		
SYSTEMS ENGINEERING	246.	13.	201.		459.
PROGRAMMING	43.	65.	82.		190.
CONFIGURATION CONTROL	43.	18.	119.		180.
DOCUMENTATION	39.	6.	53.		99.
PROGRAM MANAGEMENT	26.	5.	24.		55.
TOTAL	397.	107.	430.		933.

SYSTEM INTEGRATION

DATE 10/12/78 TIME 14:18:22

SYSTEM INTEGRATION

MFBARS

SENSITIVITY DATA

		COMPLEXITY					
		1.000		1.100		1.200	
R E S O U R C E	2.900	COST	75.	COST	80.	COST	85.
		MONTHS	6.7	MONTHS	7.5	MONTHS	8.3
	3.000	COST	78.	COST	84.	COST	90.
		MONTHS	6.8	MONTHS	7.5	MONTHS	8.3
	3.100	COST	82.	COST	88.	COST	94.
		MONTHS	6.8	MONTHS	7.6	MONTHS	8.4

Table 8-2. Price Software Model (Continued)

SCHEDULE EFFECT SUMMARY

ACTIVITY LENGTH IN MONTHS				
COMPLEXITY = 1.100	DESIGN	IMPL	T & I	TOTAL
SPECIFIED SCHEDULE (OVERLAP)	3.2 (2.1)	3.6 (2.3)	5.1	7.5
TYPICAL SCHEDULE (OVERLAP)	3.2 (2.1)	3.6 (2.3)	5.1	7.5

DEVELOPMENT COSTS				
COMPLEXITY = 1.100	DESIGN	IMPL	T & I	TOTAL
SPECIFIED SCHEDULE	35.	9.	40.	84.
TYPICAL SCHEDULE	35.	9.	40.	84.
ESTIMATED PENALTY	0.	0.	0.	0.

SYSTEM INTEGRATION

DATE 10/12/78 TIME 14:20:27

SYSTEM INTEGRATION

MFDAFC

% COMPLETED				% EXPENDED		% EXPENDED	
MONTH	DESIGN	IMPL	T & I	THIS MONTH	TOTAL	THIS MONTH	TOTAL
JAN 85	14.7	0.0	0.0	5.1	5.1	6.0	6.0
FEB 85	70.3	0.8	0.0	19.3	24.3	22.9	29.0
MAR 85	97.6	27.4	0.0	11.9	36.2	14.2	43.2
APR 85	100.0	76.9	1.8	6.1	42.4	7.3	50.5
MAY 85	100.0	99.7	13.2	6.7	49.1	8.0	58.4
JUN 85	100.0	100.0	39.9	10.7	59.8	12.8	71.2
JUL 85	100.0	100.0	76.6	14.8	74.6	17.6	88.8
AUG 85	100.0	100.0	99.9	9.4	84.0	11.2	100.0
SEP 85	100.0	100.0	100.0	0.0	84.0	0.0	100.0
# ALPHA =	0.82	0.0	0.0	FOR PROFILE GRAPHS			
* BETA =	0.18	1.00	0.18	RESPOND OK = 7			
# PFAK/AV =	1.93	1.88	1.93				

Table 8-2. Price Software Model (Continued)

```

C>EDIT MFBARS DATA
E>T*
TOF:
ASSEM
MFBARS
9/23/78
1400 0 3.0 0 0 0 .5
0 0 1 0 0 0 0
0 0 1 0 0 0 0
0 0 1 0 0 0 0
0 0 0 0
0 0 0 0
1.1 884 0 0 0 0 0
1934 0 1 1 1.8 .5
HOL
MFBARS
9/23/78
12000 0 3.0 0 0 0 .5
0 0 1 0 0 0 0
0 0 1 0 0 0 0
0 0 1 0 0 0 0
0 0 0 0
0 0 0 0
1.1 884 0 0 0 0 0
1984 0 1 1 1.8 .5
SYSTEM INTEGRATION
MFBARS
9/23/78
$
1.1 185 0 0 0 0 0
1934 0 1 1 1.8 .5
EOF:
E>

```

Table 8-3. Logistics Support Cost Model Program (Mini)
Phase I - Baseline

MF SUBSYSTEM
4 LRU'S
9 AGE ITEMS

	SUBSYSTEMS	LRUS	AGE ITEMS	SOFTWARE
TOTAL	1	4	9	4
MAX	30	300	200	100

TOTAL SYSTEM COST (IN MILLIONS) IS \$ 2.21

SUBSYSTEM	COST	FRACTION OF TOTAL COST

MF	1.3060E+06	.5909

SUBSYSTEM MF

LRU NAME	COST	FRACTION OF SUBSYSTEM COST

PRD	6.9621E+05	.5331
HF	2.4375E+05	.1866
L-B	2.4375E+05	.1866
UHF	1.2227E+05	.0936

1 SYSTEM COST BY EQUATION

C1 = 1.089809E+06 C3 = 7.115497E+04 C5 = 1.450000E+05

1 SUBSYSTEM COST BY EQUATION

Table 8-3. Logistics Support Cost Model Program (Mini) (Continued)
Phase I - Baseline

SUBSYSTEM MF

C1 = 1.089809E+06 C3 = 7.115497E+04 C5 = 1.450000E+05

LRU PRO

C1 = 4.845614E+05 C3 = 6.664446E+04 C5 = 1.450000E+05

LRU HF

C1 = 2.420992E+05 C3 = 1.647504E+03 C5 = 0.

LRU UHF

C1 = 1.210496E+05 C3 = 1.215504E+03 C5 = 0.

LRU L-B

C1 = 2.420992E+05 C3 = 1.647504E+03 C5 = 0.

TOTAL SOFTWARE COST IS \$ 904275.00
SOFTWARE ACQUISITION COST = \$ 655500.00
SOFTWARE SUPPORT COST = \$ 248775.00

PACKAGE	MAN MONTHS TO PROGRAM	NUMBER OF MEN TO SUPPORT IT	COST OF SUPPORT PROGRAMMERS
GPSF	24	♦	1440.00
HF	6	♦	180.00
JIT	5	♦	150.00
GPSA	3	♦	90.00

1 AGE BREAKOUT

AGE NAME	TOTAL BASE AGE REQUIREMENT	TOTAL DEPOT AGE REQUIREMENT
PRO-AGE	.04 (20)	.03 (1)
CARD 1	.00 (0)	.03 (1)
CARD 2	.00 (0)	.03 (1)
XMTR AGE	.00 (0)	.00 (0)
CARD 3	.00 (0)	.00 (0)

Table 8-3. Logistics Support Cost Model Program (Mini) (Continued)
Phase I - Baseline

LIST,M1

```

1.3600000    .,35000.,145.11,145.11,1.62,0.76,104.20,104.20,250.,10.
  20.,17.63,.16,.31,.90,.001,1728.,1728.,.24,.08,.25, .25,.33,.15
SOFTWARE, .15,6000.,15000., .5,4
JIT ,5.,100.,100.,0.005
GPSA,3.,100.,100.,0.005
GPCF,10.,1200.,500.,0.01
HF , 6.,100.,100.,0.005
MF,0., 0.,0 .,0.,0.
16.42,32.62,0.,0.,168.,168.,1.25,0.,4
PRD,16700.,19200.,2.5,2.5,0.,0., 0.134,1.73,20.,1.
.01,.01, 0.15,0.85,0.01,0.,0.,0.,1,0.,3
PRD-AGE ,5000.,5000.,0.,0., 0.125, .9 ,.02
CARD 1 ,0.,20000.,0.,0.,1.,.98,.02
CARD 2 ,0.,20000.,0.,0.,1.,.98,.02
HF , 500000.,12000.,2.5,2.5,0.,0., 0.134,1.73,16.,1.
.01,.01, 0.15,0.85,0.01,0.,0.,0.,1,0.,2
XMTR AGE,5000.,5000.,0.,0.,0.16,.82,0.02
CARD 3 ,0.,20000.,0.,0.,1.,.9 ,.02
UHF,500000.,6000.,2.5,2.5,0.,0., 0.134,1.73,16.,1.
.01,.01, 0.15,0.85, 0.01,0, 0.,0.,1,0.,2
XMTR AGE,5000.,5000.,0.,0.,.16 ,.82,0.02
CARD 3 ,0.,20000.,0.,0.,1.,.9 ,.02
L-B,500000.,12000.,2.5,2.5,0.,0., 0.134,1.73,16.,1.
.01,.01,0.15,.85,0.01,0.,0.,0.,1,0.,2
XMTR AGE,5000.,5000.,0.,0.,0.16,.82,0.02
CARD 3 ,0.,20000.,0.,0.,1.,.9 ,.02

```

Table 8-3 contains the computer output data and the input data base for the baseline configuration. The original input data sheets are contained in Table 8-4, and include the input values and definition of terms. Government-furnished and government standard values were obtained from several sources. Total force operation hours over the program life (TFOH) was adapted from the customer PRICE model usage. PSO and PSC, average packing and shipping cost for overseas and CONUS, Base Labor Rate (BLR) and Depot Labor Rate (DLR) were derived from a July 21, 1978 letter containing MFBARS price guidelines. Some of the values contained in the data sheets, but not actually used in the Mini program, were taken from the Version 2.0 model.

The results were as follows:

- C1 - Initial and replacement LRU spares cost for the system: \$1.09 M
- C3 - Off equipment maintenance cost: \$71.15K
- C5 - AGE cost: \$145K
- Software acquisition: \$655,500
- Software maintenance: \$248,775.

The model's output suggests a maintainability concept: that each base be provided with an LRU test set for the processor, but that because of the transmitter's high MTBF, none be provided for the transmitters. Likewise, at the depot, the model suggests an LRU test set for the processor and the analog and digital cards that are a part of the processor, but no test set for the transmitter LRUs or their module test.

8.2.4 TRI TAC Life Cycle Costs

The TRI TAC model output (Table 8-5) is composed of the annual operating and support costs (dollars), the Life Cycle costs (thousands of dollars), and a listing of the input cost element values (sheet 2). Table 8-6 is a list of the input cost elements and their definitions.

Table 8-4. Input Cost Elements Mini-LSC Baseline System

System Variables

First of two system data lines

	NO.	DATA ELEMENT NAME	VALUE
M	1	NSUB NO. OF SUB SYS IN SYS	1
M	2	TFFH TOTAL FORLE OPERATION HRS OVER PROG. LIFE (G)	3600 000
M	3	PFFH PEAK FORLE OP. HRS PER MONTH (G)	35 000
	4	LAC (S)	145.11
	5	IPC (S)	145.11
M	6	PSO (S)	1.62
M	7	PSC (S)	.76
	8	RAC (S)	104.20
	9	RPC (S)	104.20
	10	TD (S)	220.
M	11	PIUP SERVICE LIFE IN YRS (G)	10.
		G = GOV'T FURNISHED	
		S = GOV'T STD VALUE	

M = USED IN MINI PROG.

Table 8-4. Input Cost Elements Mini-LSC Baseline System (Continued)

System Variables

Second of two system data lines

NO.	DATA ELEMENT NAME	VALUE
M 1	M NO. OF OPERATING BASE LOCATIONS (G)	20.
2	SA (S)	17.63
3	TR (S)	.16
4	OSTCON (S)	.31
5	OSTOS (S)	.90
6	EBO STANDARD ESTAB. FOR EXPECTED BACKORDERS (G)	.001
7	PMB (S)	1728
8	PMD (S)	1728
9	MRF (S)	.24
10	MRO (S)	.08
M 11	OS FRACTION EMPLOYED OVERSEAS (G)	.25
12	SR (S)	.25
13	TRB (S)	.33
14	TRD (S)	.15

Software Header Data Line

-253-

One Line per Package

-254-

Table 8-4. Input Cost Elements Mini-LSC Baseline System (Continued)

Subsystem Variables

First Of Two Subsystem Data Lines

[illegible]

Subsystem Variables

[illegible]

Table 8-4. Input Cost Elements Mini-LSC Baseline System (Continued)

LRU Variables

First Of Two LRU Data Lines

	NO.	DATA ELEMENT NAME				VALUE
M	1	LRU Name (three characters - must be in col's 1-3)				
M	2	MFTBMA (May not appear left of column 5)				
M	3	UC	UNIT COST - INITIAL PROVISIONING			
M	4	BMH	AV. MH @ BASE TO FAULT ISOLATE/REPAIR LRU			
M	5	DMH	SAME AS BMH FOR DEPT			
	6	IMH	AV. MH - CORRECTIVE MAINT. IN PLACE			
	7	RMH	AV. MH TO REMOVE/ REPLACE AN LRU			
	8	BRCT	AV. BASE REPAIR CYCLE TIME (MONTHS)			
M	9	DRCT	AV. DEPT REPAIR CYCLE TIME (MONTHS)			
M	10	W	UNIT WEIGHT, LBS.			
M	11	UP	LRU UTILIZATION FACTOR CONSTANT USAGE = 1.0 10% UTILIZATION = 0.10			
	1	PRO	HF	UHF	L-B	
	2	16700	500000	500000	500000	
	3	19200	12000	6000	12000	
	4	2.5	2.5	2.5	2.5	
	5	2.5	2.5	2.5	2.5	
	6	0	0	0	0	
	7	0	0	0	0	
	8	0.134	0.134	0.134	0.134	
	9	1.73	1.73	1.73	1.73	
	10	20	16	16	16	
	11	1	1	1	1	

Table 8-4. Input Cost Elements Mini-LSC Baseline System (Continued)

ACIF: Variables

One Data Line Per AGE Item

NO.	DATA ELEMENT NAME				VALUE
M	1	AGE Item Name (8 characters max - must be in col's 1-8)			
M	2	CAB	COST / UNIT OF PECULIAR AGE@BASE (may not appear left of column 10)		
M	3	CAD	SAME AS CAB - DEPOT		
M	4	COB	ANNUAL COST TO OPERATE A UNIT OF AGE@BASE		
M	5	COD	SAME AS COB - DEPOT		
M	6	BEUR	BASE LEVEL UTILIZATION RATE (MUST HAVE NON-ZERO ENTRY)		
M	7	DUR	DEPOT LEVEL UTILIZATION RATE (MUST BE NON-ZERO)		
M	8	DOWN	% DOWN TIME FOR A UNIT OF AGE FOR CMIB. REQ.		
	1	PRD-AGE	XMTR AGE	CARD 1	CARD 2
	2	5000	5000	0	0
	3	5000	5000	20000	20000
	4	0	0	0	0
	5	0	0	0	0
	6	.125	.16	1.	1.
	7	.9	.9	.98	.98
	8	.02	.02	.02	.02

LRU Variables

[illegible]

Table 8-5. Phase I Baseline TRI TAC Life Cycle Costs

10/18/78.

BASELINE LIFE CYCLE COSTS		
0		
0	ANNUAL O & S COSTS IN \$	
-	ELECTRIC POWER	24572.16
0	SPECIAL MATERIAL	0.00
0	OPERATOR PERSONNEL	0.00
0	ORG. MAINT. PERSONNEL	24.38
0	INT. MAINT. PERSONNEL	185.32
0	DEPOT MAINT. PERSONNEL	558316.32
0	TOTAL MAINT. PERSONNEL	558526.02
0	SUPPORT EQUIP. MAINT.	7000.00
0	SOFTWARE MAINTENANCE	248775.00
0	SUPPLY PERSONNEL	6.29
0	SPARE PARTS & REPAIR MATERIAL	7123.55
0	INVENTORY MANAGEMENT	1540.00
0	INVENTORY HOLDING	1696580.79
0	INVENTORY ADMINISTRATION	1698120.79
0	TRANSPORTATION	355.63
0		
0	LIFE CYCLE COSTS IN \$K	
-	R & D ESTIMATE	4405.50
0	INVESTMENT-NON-RECURRING	20740.00
0	INVESTMENT-RECURRING	49200.00
0	TOTAL INVESTMENT	69940.00
0	OPERATIONS	245.72
0	LOGISTICS SUPPORT	26223.07
0	OPERATIONS & LOGISTICS SUPP. TOTAL	26468.79
0	TOTAL LIFE CYCLE COST	100814.29

Table 8-5. Phase I Baseline TRI TAC Life Cycle Costs (Continued)

INPUT COST ELEMENT VALUES

P1	=	360.00	R21	=	.14	R65	=	.0476
R2	=	5.00	R22	=	0.00	R66	=	.0004
R3	=	1.19	R24	=	0.00	R67	=	40.00
R4	=	10.00	R25	=	0.00	R71	=	5.00
R5	=	5.00	R26	=	16.42	R72	=	95.00
R6	=	10.00	R27	=	5.00	R75	=	0.00
R7	=	23.00	R28	=	16.42	R76	=	0.00
R8	=	.48	R29	=	70000.00	TF	=	E
R9	=	1000.00	R50	=	0.00	R78	=	0.00
R10	=	0.00	R51	=	0.00	R79	=	0.00
R11	=	0.00	R52	=	0.00	X(1)	=	1070.00
R12(1)	=	0.00	R53	=	0.00	X(2)	=	770.00
R12(2)	=	3.00	R54	=	0.00	X(3)	=	580.00
R12(3)	=	1.00	R55	=	0.00	X(4)	=	460.00
R12(4)	=	0.00	R56	=	102400.00	Y(1)	=	720.00
R13	=	68.00	R57	=	3750000.00	Y(2)	=	420.00
R14	=	12300.00	R58	=	1060000.00	Y(3)	=	130.00
R15	=	.250	R59	=	0.00	Y(4)	=	110.00
R16	=	60606.00	R60	=	5.00	UP	=	T
R17	=	2.00	R61	=	17.00	R80	=	655500.00
R18	=	49200.00	R62	=	.18	R81	=	248775.00
R19	=	1000.00	R63	=	25.00	INVR	=	T
R20	=	85.00	R64	=	1500.00	INVN	=	T

Table 8-6. Phase I Baseline TRI TAC Input Cost Elements

<u>Cost Element</u>		<u>Definition (Units)</u>
R1	360.	Operating hours (hrs/year) <i>PER SYSTEM</i>
R2	5.	Depot Overhaul Rate (%)
R3	1.14	Transportation Cost Factor (\$/lb.)
R4	10.	Support Equip. Maintenance Factor (%) <i>OF R29</i>
R5	5.	Repair Material Cost Factor (%)
R6	10.	Years of Operation
R7	23	Holding Inventory Factor (%)
R8	.48	Power Cost (\$/kwh)
R9	1000.	Equipment Quantity (#)
R10	0.	No. Operators/equipment (#)
R11	0.	Annual Operator Cost (\$/yr.)
R12(1)	0.	No. of new FSN, value greater than \$25,000 (#)
R12(2)	3.	No. of new FSN, value - \$10,000 to \$24,999 (#)
R12(3)	1.	No. of new FSN, value - \$2,500 to \$9,999 (#)
R12(4)	0.	No. of new FSN, value less than \$2,500 (#)
R13	68.	Equipment Weight (lbs.) <i>PER SYSTEM</i>
R14	12300.	Avg. Replacement Assembly (LRU) cost (\$)
R15	.25	MTTR (Org. level) (hrs.)
R16	60606.00	MTBF (hrs.) <i>AVERAGE OF LRU'S</i>
R17	2.0	LRU MTTR (Int. or Depot Level) (hrs.)
R18	49200.	Unit Production Cost Est. (\$) <i>PER SYSTEM</i>
R19	1000.	Quantity Used for UPC Est. (\$) <i>(UNIT PRICE COST)</i>
R20	85.	Learning Curve Slope (%)
R21	.14	Power Rating (kw)
R22	0.	Preventative Maintenance (hr./yr.)
R24	0.	Material No. 1 Consumption Rate (units/yr./equip.)
R25	0.	Material No. 1 Cost (\$/unit)
R26	16.42	Org. Level Maintenance Personnel Cost (\$/hr.)
R27	5.	Discard Rate (%)
R28	16.42	Int. Level Maintenance Personnel Cost (\$/hr.)
R29	70000.	Common and Peculiar Support Equip. Cost (\$)
R30	0.	Operational Facilities (\$)
R31	0.	Equipment Leaseholds (\$)
R32	0.	Other Operating Costs (\$)
R33	0.	Maintenance Facilities (\$)
R34	0.	Contractor Services (\$)
R35	0.	Supply Facilities (\$)
R36	102400.00	Other Logistics Support Costs (\$)
R37	3750000.	R & D Estimate (\$)
R38	1060000.	Other Non-Recurring Investment Costs (\$)
R39	0.	Other Recurring Investment Costs (\$)
R60	5.	Transportation Cost Factor (%)
R61	17.	Wt. of Avg. LRU (lbs.)
R62	.18	Wt. of Repair Parts (lbs.)

Table 8-6. Phase I Baseline TRI TAC Input Cost Elements (Continued)

<u>Cost Element</u>	<u>Definition (Units)</u>
R63 25.	Dist A (Org. to Int. Level) (mi.)
R64 1500	Dist B (Int. to Depot Level) (mi.)
R65 .0476	Transportation Factor A (\$/lb./mi.) ORG. TO INT. [R3/R63]
R66 .0004	Transportation Factor B (\$/lb./mi.) INT. TO DEPOT [R3/R64]
R67 40.	Non-Recurring Investment Cost Factor (%)
R71 5.	P2 (% of failures assigned to Int. level for repair/discard) (%)
R72 95.	P3 (% of failures assigned Depot level for repair/discard) (%)
R75 0	Material No. 2 Consumption Rate (units/yr./equip.)
R76 0	Material No. 2 Cost (\$/unit)
R78 0	Special Materials Cost (\$) GFE & ETC. NOT INCL. IN R49
R79 0	Transportation to and from Exercises (\$)
X(1) 1070.	First year cost of new FSN, value greater than \$25,000 (\$)
X(2) 776.	First year cost of new FSN, value \$10,000 to \$24,999 (\$)
X(3) 580.	First year cost of new FSN, value \$2,500 to \$9,999 (\$)
X(4) 460.	First year cost of new FSN, value less than \$2,500 (\$)
Y(1) 720.	Annual recurring cost of new FSN, value greater than \$25,000 (\$)
Y(2) 420.	Annual recurring cost of new FSN, value \$10,000 to \$24,999 (\$)
Y(3) 130.	Annual recurring cost of new FSN, value \$2,500 to \$9,999 (\$)
Y(4) 110.	Annual recurring cost of new FSN, value less than \$2,500 (\$)
R80 655500.	Software Procurement Cost (\$)
R81 248775	Software Maintenance Cost (\$/yr.)

Additionally, four pseudo-cost-elements have been added to the list of variables:

TF - Informs program how annual transportation costs (R44) are to be calculated.

UP - Informs program whether unit production cost (R49) is to be computed according to the model or overridden by the user.

INVN - Indicates whether or not the cost estimating relationship for computing investment-non-recurring costs (R45) has been overridden.

INVR - Indicates whether or not the cost estimating relationship for computing investment-recurring costs (R46) has been overridden.

The total life cycle cost of \$100,814,290 over the 10-year life of the program appears to be a credible value since total operations and logistics support costs are 26% of the LCC cost, a good ballpark number, and the fact that some values, such as R&D estimate, software costs and recurring investment, are taken directly from input data and are not modified by the model.

8.2.5 PRICE Life Cycle Cost

The PRICE input worksheets (Table 8-7) given to the customer are the basis for the PRICE LCC model printout included as Table 8-8.

The two LCC models, PRICE and TRI TAC, are compared in Table 8-9. It is interesting to note that, although the two models predict an LCC that is very close in value, the emphasis is shifted between acquisition and support costs. The PRICE support cost of \$12.25M, only 10.5% of the total LCC of \$116.6M, appears low; whereas, the 25.8% figure predicted by TRI TAC seems more reasonable.

The input data base used for the two models is compared in Table 8-10. Probably the largest significant data difference is that of MTBF. TRW feels that the MTBFs used by PRICE are low, not only in today's world, but especially so for 1983 technology.

8.3 PHASE I ALTERNATIVE ARCHITECTURES

Two alternative architectures were evaluated for logistic support and life cycle costs.

Alternate "A", a hybrid configuration, is depicted in Figure 8-2. The LSC model output is shown in Table 8-11 and the TRI TAC output in Table 8-12.

Table 8-7. Phase I

PRICE System

Input Worksheet — ECIRP

Item	Date				
<i>HF XMTR, MFBARS</i>					
	QTY*	PROTOS	WT*	VOL*	MODE
General	<i>1000</i>	<i>10</i>	<i>20</i>	<i>0.42</i>	<i>1</i>
	WS*	MCPLXS	PRODS	NEWST	DESRPS
Mechanical/ Structural	<i>3.2</i>	<i>0</i>	<i>0</i>	<i>—</i>	<i>—</i>
	USEVOL**	MCPLXE	PRODE	NEWEL	DESRPE
Electronics	<i>.70</i>	<i>0</i>	<i>0</i>	<i>—</i>	<i>—</i>
	ENMTMS	ENMTHP	ENMTHT	ECMLPX	PRNF
Engineering	<i>—</i>	<i>—</i>	<i>—</i>	<i>—</i>	<i>—</i>
	PRMTH2	PRMTHF	LCURVE***	ECNE	ECNS
Production	<i>—</i>	<i>—</i>	<i>.90</i>	<i>—</i>	<i>—</i>
	AVCOST*	TECOST	TMCOST	LCN***	
Additional Data	<i>10.0</i>	<i>—</i>	<i>—</i>	<i>0</i>	
	YEAR*				
Global	<i>1983</i>				
	PLTFM*	SYSTEM	PPROJ	POATA	PTLGTS
	<i>1.8</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>1</i>

Notes:

- *Mandatory input.
 **Mandatory input for E/M item.
 ***Input for either LCURVE or LCN is mandatory.

Modes (For User Reference Only — Input Optional)

1. E/M ITEM
2. MECH. ITEM

Table 8-7. Phase I (Continued)

PRICE System Input Worksheet

[illegible]

Table 8-7. Phase I (Continued)

PRICE System

Input Worksheet — ECIRP

Item	Date				
<u>UHF XMTR, MFBAR S</u>					
	QTY*	PROTOS	WT*	VOL*	MODE
General	<u>1000</u>	<u>10</u>	<u>16</u>	<u>0.42</u>	<u>1</u>
	WS*	MCPLXS	PRODS	NEWST	DESAPS
Mechanical/ Structural	<u>3.2</u>	<u>0</u>	<u>0</u>	<u>—</u>	<u>—</u>
	USEVOL**	MCPLXE	PRODE	NEWEL	DESAPF
Electronics	<u>.70</u>	<u>0</u>	<u>0</u>	<u>—</u>	<u>—</u>
	ENMTHS	ENMTHP	ENMTHT	ECMPLX	PRNF
Engineering	<u>—</u>	<u>—</u>	<u>—</u>	<u>—</u>	<u>—</u>
	PRMTHS	PRMTHP	LCURVE***	ECNE	ECNS
Production	<u>—</u>	<u>—</u>	<u>.90</u>	<u>—</u>	<u>—</u>
	AVCOST*	TECOST	TMCOST	LCN***	
Additional Data	<u>5.0</u>	<u>—</u>	<u>—</u>	<u>0</u>	
	YEAR*				
Global	<u>1983</u>				
	PLTFM*	SYSTEM	PPROJ	PDATA	PTLGTS
	<u>1.8</u>	<u>1</u>	<u>1</u>	<u>1</u>	<u>1</u>

Notes:

- *Mandatory input.
 **Mandatory input for E/M Item.
 ***Input for either LCURVE or LCN is mandatory.

Modes (For User Reference Only — Input Optional)

1. E/M ITEM
2. MECH. ITEM

SYSTEMS 5224

Table 8-7. Phase I (Continued)

PRICE System
Input Worksheet

Item		Date			
UHF XMTR, MFBARS					
General	QTY	PROTOS	WT	VOL	MODE
	1000	10	16	0.42	1
	QTYSYS	INTEGE	INTEGS	AMULTE(%)	AMULTM(%)
	1	0.5	0.3	150	150
Mechanical/ Structural	WS	MCPLXS	PRODS	NEWST	DESAPS
	3.2	0	0	.80	.40
Electronics	USEVOL	MCPLXE	PRODE	NEWEL	DESAPPE
	.70	0	0	.80	.40
	PWR	CMPNTS	CMPID	PWRFAC	CMPEFF
	40	0	602	0.2	-32
Engineering	ENMTHS	ENMTHP	ENMTHT	ECMPLX	PRNF
	9	12	24	1.0	-
Production	PRMTHS	PRMTHF	LCURVE	ECNE	ECNS
	33	81	.90	.025	.025
Purchased Item (Mode 3)	WS	BVCOST	LCURVE	MODES	
GFE (Mode 4)	WS	MCPLXE	MCPLXS	0 PRINT TOTALS 1 E-ITEM 2 MECH ITEM 3 PURCH ITEM 4 GFE ITEM 5 INTEG & TEST 6 MODIFIED PURCH ITEM 7 MODIFIED GFE ITEM 8 PARASYN 9 E-ITEM CALC WT & VOL 10 GEOSYN	
Additional Data (Modes 9 & 10)	MCONST	MEXP	WECF	TARCST (Mode 10 only)	
Global	YEAR	ESC	PROJCT	DATA	TLGTST
	1983	100	1	1	1
	PLTFM	SYSTEM	P PROJ	POATA	PLYGTS
	1.8	1	1	1	1

Notes:

SYSTEM 8223

Table 8-7. Phase I (Continued)

PRICE System
Input Worksheet — ECIRP

Item	Date				
L-BAND XMTR, MFBARS					
	QTY*	PROTOS	WT*	VOL*	MODE
General	<u>1000</u>	<u>10</u>	<u>16</u>	<u>0.42</u>	<u>1</u>
	WS*	MCPLXS	PRODS	NEWST	DESRPS
Mechanical/ Structural	<u>3.2</u>	<u>0</u>	<u>0</u>	<u>—</u>	<u>—</u>
	USEVOL**	MCPLXE	PRODE	NEWEL	DESRPE
Electronics	<u>.70</u>	<u>0</u>	<u>0</u>	<u>—</u>	<u>—</u>
	ENMTHS	ENMTHP	ENMTHT	ECMPLX	PRNF
Engineering	<u>—</u>	<u>—</u>	<u>—</u>	<u>—</u>	<u>—</u>
	PRMTHS	PRMTHF	LCURVE***	ECNE	ECNS
Production	<u>—</u>	<u>—</u>	<u>.90</u>	<u>—</u>	<u>—</u>
	AVCOST*	TECOST	TM COST	LCN***	
Additional Data	<u>10.0</u>	<u>—</u>	<u>—</u>	<u>0</u>	
	YEAR*				
Global	<u>1983</u>				
	PLTFM*	SYSTEM	PROJ	PDATA	PTLGTS
	<u>1.8</u>	<u>1</u>	<u>1</u>	<u>1</u>	<u>1</u>

Notes:

- *Mandatory input.
 **Mandatory input for E/M Item.
 ***Input for either LCURVE or LCN is mandatory.

Modes (For User Reference Only — Input Optional)

1. E/M ITEM
2. MECH. ITEM

SYSTEMS 5220

Table 8-7. Phase I (Continued)

PRICE System Input Worksheet

Item	L-BAND XMTR, MFBARS				Date
General	QTY	PROTOS	WT	VOL	MODE
	<u>1000</u>	<u>10</u>	<u>16</u>	<u>0.42</u>	<u>1</u>
	QTYSYS	INTEGE	INTEGS	AMULTE(%)	AMULTM(%)
	<u>1</u>	<u>0.5</u>	<u>0.3</u>	<u>150</u>	<u>150</u>
Mechanical/ Structural	WS	MCPLXS	PRODS	NEWST	DESAPS
	<u>3.2</u>	<u>0</u>	<u>0</u>	<u>.80</u>	<u>.40</u>
Electronics	USEVOL	MCPLXE	PRODE	NEWEL	DESAPPE
	<u>.70</u>	<u>0</u>	<u>0</u>	<u>.80</u>	<u>.40</u>
	PWR	CMPNTS	CMPID	PWRFAC	CMPEFF
	<u>236</u>	<u>0</u>	<u>602</u>	<u>1.18</u>	<u>-32</u>
Engineering	ENMTHS	ENMTHP	ENMTMT	ECMPLX	PRNF
	<u>9</u>	<u>12</u>	<u>24</u>	<u>1.0</u>	<u>—</u>
Production	PRMTHS	PRMTHF	LCURVE	ECNE	ECNS
	<u>33</u>	<u>81</u>	<u>.90</u>	<u>.025</u>	<u>.025</u>
Purchased Item (Mode 3)	WS	BVCOST	LCURVE	MODES 0 PRINT TOTALS 1 E M ITEM 2 MECH ITEM 3 PURCH ITEM 4 GFE ITEM 5 INTEG & TEST 6 MODIFIED PURCH ITEM 7 MODIFIED GFE ITEM 8 PARASYN 9 E ITEM CALC WT & VO. 10 GECSYN	
GFE (Mode 4)	WS	MCPLXE	MCPLXS		
Additional Data (Modes 9 & 10)	MCONST	MEXP	WECF	TARCSST (Mode 10 only)	
	<u> </u>	<u> </u>	<u> </u>	<u> </u>	
Global	YEAR	ESC	PROJECT	DATA	TLGTST
	<u>1983</u>	<u>100</u>	<u>1</u>	<u>1</u>	<u>1</u>
	PLTFM	SYSTEM	P PROJ	P DATA	PTLGTS
	<u>1.8</u>	<u>1</u>	<u>1</u>	<u>1</u>	<u>1</u>
Notes:					

Table 8-7. Phase I (Continued)

PRICE System
Input Worksheet — ECIRP

Item	PROCESSOR, MFBARS					Date
General	QTY*	PROLOS	WT*	VOL*	MODE	
	<u>1000</u>	<u>10</u>	<u>20</u>	<u>0.42</u>	<u>1</u>	
Mechanical/ Structural	WS*	MCPLXS	PRODS	NEWST	DESAPS	
	<u>4</u>	<u>0</u>	<u>0</u>	<u>—</u>	<u>—</u>	
Electronics	USEVOL**	MCPLXE	PRODE	NEWEL	DESAPPE	
	<u>.7</u>	<u>0</u>	<u>0</u>	<u>—</u>	<u>—</u>	
Engineering	ENMTHS	ENMTHP	ENMTHT	ECMPLX	PRNF	
	<u>—</u>	<u>—</u>	<u>—</u>	<u>—</u>	<u>—</u>	
Production	PRMTHS	PRMTHF	LCURVE***	ECNE	ECNS	
	<u>—</u>	<u>—</u>	<u>.90</u>	<u>—</u>	<u>—</u>	
Additional Data	AVCOST*	TECOST	TM COST	LCN***		
	<u>16.0</u>	<u>—</u>	<u>—</u>	<u>0</u>		
Global	YEAR*					
	<u>1983</u>					
	PLTFM*	SYSTEM	PPROJ	PDATA	PTLGTS	
	<u>1.8</u>	<u>1</u>	<u>1</u>	<u>1</u>	<u>1</u>	

Notes:

- * Mandatory input.
 ** Mandatory input for E/M item.
 *** Input for either LCURVE or LCN is mandatory.

Modes (For User Reference Only — Input Optional)

1. E/M ITEM
2. MECH. ITEM

SYSTEMS 8224

Table 8-7. Phase I (Continued)

PRICE System
Input Worksheet

Item	PROCESSOR, MFBARS					Date
General	QTY	PROTOS	WT	VOL	MODE	
	<u>1000</u>	<u>10</u>	<u>20</u>	<u>0.42</u>	<u>1</u>	
	QTSYS	INTEGE	INTEGS	AMULTE(%)	AMULTM(%)	
	<u>1</u>	<u>0.5</u>	<u>0.3</u>	<u>150</u>	<u>150</u>	
Mechanical/ Structural	WS	MCPLXS	PRODS	NEWST	DESAPS	
	<u>4</u>	<u>0</u>	<u>0</u>	<u>.80</u>	<u>.40</u>	
Electronics	USEVOL	MCPLXE	PRODE	NEWEL	DESAPF	
	<u>.7</u>	<u>0</u>	<u>0</u>	<u>.80</u>	<u>.40</u>	
	PWR	CMPTS	CMPIO	PWRFAC	CMPEFF	
	<u>150</u>	<u>0</u>	<u>204</u>	<u>.42</u>	<u>6.33</u>	
Engineering	ENMTHS	ENMTHP	ENMTHY	ECMLPX	PRNF	
	<u>9</u>	<u>12</u>	<u>24</u>	<u>1.0</u>	<u>-</u>	
Production	PRMTHS	PRMTHF	LCURVE	ECNE	ECNS	
	<u>33</u>	<u>81</u>	<u>.90</u>	<u>0.25</u>	<u>0.25</u>	
Purchased Item (Mode 3)	WS	BVCOST	LCURVE	MODES		
GFE (Mode 4)	WS	MCPLXE	MCPLXS	0 PRINT TOTALS 6 MODIFIED PURCH ITEM 1 E-M ITEM 7 MODIFIED GFE ITEM 2 MECH ITEM 8 PARASYN 3 PURCH ITEM 9 E-M ITEM-CALC WT & VOL 4 GFE ITEM 10 GEOSYN 5 INTEG & TEST		
Additional Data (Modes 9 & 10)	MCONST	MEXP	WECF	TARCST (Mode 10 only)		
Global	YEAR	ESC	PROJCT	DATA	TLGTST	
	<u>1983</u>	<u>100</u>	<u>1</u>	<u>1</u>	<u>1</u>	
	PLTFM	SYSTEM	PPROJ	PDATA	PTLGTS	
	<u>1.8</u>	<u>1</u>	<u>1</u>	<u>1</u>	<u>1</u>	
Notes:						

SYSTEM 8223

Table 8-8. PRICE LCC Printout

LC FILE INPUT DATA

TPM MFEAR: PROPOSAL BOX 1: HF LMTTP

DEPLOYMENT
EQUIP:ED: 1050. ORGANIZATION:DD: 20. INTERMEDIATE:DI: 20. DEPOT:DD: 2.

DURATION OF SUPPORT PERIOD:YEAR:YF: 10.00
ON-TIME FRACTION(OTF) .041

LRU MTBF:HOURL:MTBF: 683.
LRU REPAIR TIME:HOURL:TF: 1.41
MODULE REPAIR TIME:HOURL:TMD: 2.86
LRU PER SYSTEM:EE: 1.
LRU COST:\$(CUP) 14523.
MODULE COST:\$(CMP) 2573.50
PART COST:\$(CPP) 22.19
PART COST ON-EQUIPMENT REPAIR:\$(CPPE) 22.19
DEVELOPMENT COST:\$(CEND) 1572625.
NON-RECURRING PRODUCTION COST:\$(CPE) 1133603.
CONTRACTOR LRU REPAIR COST:\$(CUP) 729.16
CONTRACTOR MODULE REPAIR COST:\$(CMP) 900.73
MODULE TYPES:(P) 13.
PART TYPES:(PP) 363.
FRACTION NON-STD.PARTS:(FNIP) 0.50
LRU SUPPORT EQPT. COST:\$(CFIM) 89201.
LRU+MODULE SUPPORT EQPT.:(CFIP) 103722.
LRU S.E. FLOOR SPACE:SQ.FT.(FTSOF) 1.89
LRU+MODULE S.E. FLOOR SPACE:SQ.FT.(FTSOP) 2.20

COST-QUANTITY EXPONENTS (LEARNING FACTORS):
UNIT:EUP) 0.900 MODULE:EMP) 0.950 PART:EPF) 0.975
REFERENCE QUANTITIES:
UNIT:RNU) 1000. MODULE:RNM) 1000. PART:RNP) 1000.
CHIPPING WEIGHT: POUNDS:
UNIT:MU) 16.0 MODULE:MM) 0.75 PART:MP) 0.006
STORAGE CUBES: CUBIC FEET:
UNIT:CUBEU) 0.504 MODULE:CUBEM) 0.030 PART:CUBEF) 0.0003
DEVELOPMENT PHASE: YEARS (YD) 2.00
PRODUCTION PHASE: YEARS (YP) 4.00

OK =

ENTER %NL NAMELIST
%%NL EUP=.9,RNU=1050,RNM=1050,RNP=1050,MC=6.0%

ENTER %NL NAMELIST
%%NL EUP=.9,RNU=1050,RNM=1050,RNP=1050,MC=8.0%

Table 8-8. PRICE LCC Printout (Continued)

PRICE LIFE CYCLE COST

TRM MFRAP: PROPOSAL EOM: 1: MF: MMTF LC: L6

INPUT DATA

PCM DATA
MTBF 683. MTTR-LPU 1.4 MTTR-MOD 2.9

DEPLOYMENT
EQUIP 1050. ORGANIZATION 20. INTERMEDIATE 20. DEPOT 2.
LRU/EQUIP 1. MOD/LPU 13. PARTS/LRU 363.

EMPLOYMENT
SUPPORT PERIOD 10. HPI-MON 30.0 OTF 0.041

GLOBAL
EQUISUP 1050. ORGSUP 20. INTSUP 20. DEPSUP 2.
ECC 0.000 LPU FAIL ALLOW 0.

MAINTENANCE CONCEPT 6
LRU REPAIR AT ORGANIZATION. MODULE REPAIR AT DEPOT.

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	1573.	16448.	0.	18012.
SUPPORT EQUIP	0.	1991.	1991.	3982.
MANPOWER	0.	0.	302.	302.
SUPPLY	0.	1362.	40.	1402.
SUPPLY ADM.	0.	19.	195.	214.
CONTRACTOR SUPPORT	0.	0.	0.	0.
OTHER	0.	0.	3.	3.
TOTAL COST	1573.	19818.	2531.	23922.

AVAILABILITY
INHERENT 0.9982 OPERATIONAL 0.9982

	ORG	INT	DEPOT
SUPPORT EQUIPMENT NO.	20.	0.	2.
UTILIZATION	0.107	0.000	0.130

	UNITS	MODULES	PARTS
SUPPLY INITIAL PER TYPE	0.	40.	7.
BALANCE CONSUMED	0.000	0.000	8.213

Table 8-8. PRICE LCC Printout (Continued)

LC FILE INPUT DATA

BOX 2:UHF NMTP

DEPLOYMENT

EQUIPS(ED) 1050. ORGANIZATION(OD) 20. INTERMEDIATE(DI) 20. DEPOT(DD) 2.

DURATION OF SUPPORT PERIOD,YEARS(YR) 10.00
ON-TIME FRACTION(OTF) .041

LPU MTEF,HOURS(MTEF) 582.
LPU REPAIR TIME,HOURS(TF) 1.34
MODULE REPAIR TIME,HOURS(TMD) 2.71
LPU PER SYSTEM,TEE 1.
LPU COST,\$(CUP) 3215.
MODULE COST,\$(CMP) 1974.68
PART COST,\$(CPP) 329.11
PART COST ON-EQUIPMENT REPAIR,\$(CPPE) 329.11
DEVELOPMENT COST,\$(CEND) 1205576.
NON-RECURRING PRODUCTION COST,\$(CPE) 724883.
CONTRACTOR LPU REPAIR COST,\$(CUP) 460.76
CONTRACTOR MODULE REPAIR COST,\$(CMP) 691.14
MODULE TYPES,(P) 10.
PART TYPES,(PP) 37.
FRACTION NON-STD.PARTS,(FNCP) 0.50
LPU SUPPORT EORT, COST,\$(CFIM) 62883.
LPU+MODULE SUPPORT EORT,\$(CFIP) 73119.
LPU S.E. FLOOR SPACE,SQ.FT.(FTOP) 1.33
LPU+MODULE S.E. FLOOR SPACE,SQ.FT.(FTOP) 1.55

COST-QUANTITY EXPONENTS (LEARNING FACTORS):

UNIT(EMP) 0.900 MODULE(EMP) 0.950 PART(EPF) 0.975

REFERENCE QUANTITIES:

UNIT(PNU) 1000. MODULE(PNM) 1000. PART(PNP) 1000.

SHIPPING WEIGHT, POUNDS:

UNIT(WU) 16.0 MODULE(WM) 0.91 PART(WP) 0.152

STORAGE CUBES, CUBIC FEET:

UNIT(CUBEU) 0.504 MODULE(CUBEM) 0.036 PART(CUBEF) 0.0060

DEVELOPMENT PHASE, YEARS (YD) 2.00

PRODUCTION PHASE, YEARS (YP) 4.00

OK #1

Table 8-8. PRICE LCC Printout (Continued)

```

PRICE LIFE CYCLE COST

BOM: 2:UHF AMTTP                                     LC:  L8
INPUT DATA
PCM DATA
MTEF          582. MTP-LPU          1.3 MTP-MOD          2.7
DEPLOYMENT
EQUIPS        1050. ORGANIZATION    20. INTERMEDIATE    20. DEPOT    2.
LPU/EQUIP     1. MODS/LRU          10. PARTS/LPU        37.
EMPLOYMENT
SUPPORT PERIOD 10.                HPS/MON          30.0 OTF          0.041
GLOBAL
EQUIPUP       1050. OPSUP          20. INTUP          20. DEPSUP    2.
ESC          0.000 LRU FAIL ALLOW  0.
MAINTENANCE CONCEPT 6
LRU REPAIR AT ORGANIZATION. MODULE REPAIR AT DEPOT.
PROGRAM COST      DEVELOPMENT      PRODUCTION      SUPPORT      TOTAL
EQUIPMENT          1206.          10330.           0.          11536.
SUPPORT EQUIP       0.          1404.          1404.          2801.
MANPOWER           0.           0.           336.          336.
SUPPLY             0.          1361.          1027.          2388.
SUPPLY ADM.        0.           3.           29.           31.
CONTRACTOR SUPPORT 0.           0.           0.           0.
OTHEP             0.           0.           5.           5.
TOTAL COST          1206.          13093.          2800.          17104.

AVAILABILITY
INHERENT          0.9979 OPERATIONAL          0.9979
SUPPORT EQUIPMENT  OPS          INT          DEPOT
NO.              20.           0.           2.
UTILIZATION      0.119          0.000          0.200
SUPPLY           UNITS          MODULES          PARTS
INITIAL, PER TYPE 0.           60.           31.
BALANCE CONSUMED  0.000          0.000          144.165

COST/EFFECTIVENESS LIST (C)
BBD =100.0
NEXT BOX:OK=

ENTER %NL NAMELIST
%NL PNU=1050.PNM=1050.RNP=1050%

```

Table 8-8. PRICE LCC Printout (Continued)

LC FILE INPUT DATA

BOMB: L-BAND MITEF

DEPLOYMENT

EQUIP(ED) 1050. ORGANIZATION(OD) 20. INTERMEDIATE(DI) 20. DEPOT(DD) 2

DURATION OF SUPPORT PERIOD-YEAR(S)(YP) 10.00
ON-TIME FRACTION(OTF) .041

LPU MTEF-HOUR(S)(MTEF) 735.
LPU REPAIR TIME-HOUR(S)(TF) 1.45
MODULE REPAIR TIME-HOUR(S)(TMD) 2.95
LPU PER SYSTEM-FEE 1.
LPU COST-\$(CUP) 18225.
MODULE COST-\$(CMP) 2377.60
PART COST-\$(CPR) 8.11
PART COST ON-EQUIPMENT REPAIR-\$(CPPE) 8.11
DEVELOPMENT COST-\$(CEND) 1853323.
NON-RECURRING PRODUCTION COST-\$(CPE) 1410098.
CONTRACTOR LPU REPAIR COST-\$(CUP) 911.24
CONTRACTOR MODULE REPAIR COST-\$(CMP) 1007.16
MODULE TYPES-(P) 14.
PART TYPES-(PP) 876.
FRACTION NON-STD.PARTS-(FNP) 0.50
LPU SUPPORT EORT. COST-\$(CFIM) 105376.
LPU+MODULE SUPPORT EORT.-(CFIP) 122530.
LPU S.E. FLOOR SPACE-10.FT.(FTSOF) 2.23
LPU+MODULE S.E. FLOOR SPACE-10.FT.(FTSORP) 2.59

COST-QUANTITY EXPONENTS (LEARNING FACTORS):

UNIT-EUP 0.900 MODULE-EMP 0.950 PART-EPF 0.975

REFERENCE QUANTITIES:

UNIT-PNU 1000. MODULE-PNM 1000. PART-PNP 1000.

SHIPPING WEIGHT- POUNDS:

UNIT-MMU 16.0 MODULE-MMN 0.67 PART-MPF 0.002

STORAGE CUBED- CUBIC FEET:

UNIT-CUBEU 0.504 MODULE-CUBEM 0.027 PART-CUBEP 0.0001

DEVELOPMENT PHASE- YEARS (YD) 2.00

PRODUCTION PHASE- YEARS (YP) 4.00

OK =

ENTER ENL NAMELIST

%ENL SUP=,9.PNU=1050.PNM=1050.PNP=10508

Table 8-8. PRICE LCC Printout (Continued)

PRICE LIFE CYCLE COST

EQ: 3: L-BAND XMTTP LC: L2

INPUT DATA

R&M DATA
MTEF 735. MTTR-LRU 1.5 MTTR-MOD 2.9

DEPLOYMENT
EQUIP 1050. ORGANIZATION 20. INTERMEDIATE 20. DEPOT 2.
LRU/EQUIP 1. MODC/LRU 14. PARTS/LRU 876.

EMPLOYMENT
SUPPORT PERIOD 10. HRS/MON 30.0 DTF 0.041

GLOBAL
EQUIP 1050. OPSUP 20. INTSUP 20. DEPSUP 2.
ECC 0.000 LRU FAIL ALLOW 0.

MAINTENANCE CONCEPT 6
LRU REPAIR AT ORGANIZATION. MODULE REPAIR AT DEPOT.

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	1853.	20546.	0.	22400.
SUPPORT EQUIP	0.	2353.	2353.	4706.
MANPOWER	0.	0.	289.	289.
SUPPLY	0.	1620.	8.	1628.
SUPPLY ADM.	0.	45.	452.	497.
CONTRACTOR SUPPORT	0.	0.	0.	0.
OTHER	0.	0.	3.	3.
TOTAL COST	1853.	24564.	3104.	29521.

AVAILABILITY
INHERENT 0.9983 OPERATIONAL 0.9983

	OPS	INT	DEPOT
SUPPORT EQUIPMENT NO.	20.	0.	2.
UTILIZATION	0.102	0.000	0.173

	UNITS	MODULES	PARTS
SUPPLY INITIAL PER TYPE	0.	40.	4.
BALANCE CONSUMED	0.000	0.000	1.861

COST EFFECTIVENESS LIST NO
BDD =100.0
NEXT BOXOK=1

AD-A114 427

TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CA
MULTIFUNCTION MULTIBAND AIRBORNE RADIO ARCHITECTURE STUDY.(U)

F/G 17/2.1

JAN 82 L N MA, S K OSI, M Y HUANG, L L BODNAR F33615-77-C-1172

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Table 8-8. PRICE LCC Printout (Continued)

LC FILE INPUT DATA

EQ. 4: PROCECCOF

DEPLOYMENT
EQUIP=ED 1050. ORGANIZATION=OD 20. INTERMEDIATE=DI 20. DEPOT=DD 2.

DURATION OF SUPPORT PERIOD=YEARS=YP 10.00
ON-TIME FRACTION=OTF 0.041

LPU MTBF=HOURS=MTBF 710.
LPU REPAIR TIME=HOURS=TF 1.48
MODULE REPAIR TIME=HOURS=TMD 3.00
LPU REF SYSTEM=EE 1.
LPU COST=\$=CUR 29030.
MODULE COST=\$=CMP 3349.66
PART COST=\$=CPF 93.05
PART COST ON-EQUIPMENT REPAIR=\$=CPPE 93.05
DEVELOPMENT COST=\$=CEND 2892986.
NON-RECURRING PRODUCTION COST=\$=CPE 2248750.
CONTRACTOR LPU REPAIR COST=\$=CUR 1451.52
CONTRACTOR MODULE REPAIR COST=\$=CMP 1172.38
MODULE TYPES=PT 18.
PART TYPES=PP 221.
FRACTION NON-STD.PARTS=(FNSTP) 0.50
LPU SUPPORT EQPT. COST=\$=CFIM 141919.
LPU+MODULE SUPPORT EQPT.=\$=CFIP 165022.
LPU S.E. FLOOR SPACE=SQ.FT.=FTSQF 3.00
LPU+MODULE S.E. FLOOR SPACE=SQ.FT.=FTSQP 3.49

COST-QUANTITY EXPONENTS (LEARNING FACTORS):
UNIT=EUP 0.900 MODULE=EMP 0.950 PART=EPP 0.975
REFERENCE QUANTITIES:
UNIT=PNU 1000. MODULE=RNM 1000. PART=PNP 1000.
SHIPPING WEIGHT, POUNDS:
UNIT=MU 20.0 MODULE=MM 0.62 PART=MP 0.017
STORAGE CUBES, CUBIC FEET:
UNIT=CUBEU 0.504 MODULE=CUBEM 0.019 PART=CUBEP 0.0005
DEVELOPMENT PHASE, YEARS (YD) 2.00
PRODUCTION PHASE, YEARS (YP) 4.00

DI =

ENTER %NL NAMELIST

%NL EUP=.9.PNU=1050.RNM=1050.RNP=1050%

Table 8-8. PRICE LCC Printout (Continued)

PRICE LIFE CYCLE COST

BOX 4: PROCEED

LC: 02

INPUT DATA

PCM DATA

MTBF	710.	MTTP-LRU	1.5	MTTP-MOD	3.0

DEPLOYMENT

EQUIP	1050.	ORGANIZATION	20.	INTERMEDIATE	20.	DEPOT	2.
LRU/EQUIP	1.	MODS/LRU	18.	PARTS/LRU	221.		

EMPLOYMENT

SUPPORT PERIOD	10.	HRS/MON	30.0	OTF	0.041

GLOBAL

EQUIP	1050.	DEPOT	20.	INTSUP	20.	DEPOT	2.
ESC	0.000	LRU FAIL ALLOW	0.				

MAINTENANCE CONCEPT 6

LRU REPAIR AT ORGANIZATION. MODULE REPAIR AT DEPOT.

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	2893.	32730.	0.	35623.
SUPPORT EQUIP	0.	3168.	3168.	6337.
MANPOWER	0.	0.	305.	305.
SUPPLY	0.	2475.	212.	2687.
SUPPLY ADM.	0.	13.	129.	141.
CONTRACTOR SUPPORT	0.	0.	0.	0.
OTHER	0.	0.	3.	3.
TOTAL COST	2893.	38367.	3816.	45076.

AVAILABILITY

INHERENT	0.9983	OPERATIONAL	0.9983

SUPPORT EQUIPMENT

NO.	OPG	INT	DEPOT
UTILIZATION	20.	0.	2.
	0.108	0.000	0.182

SUPPLY

INITIAL PER TYPE	UNITS	MODULES	PARTS
BALANCE CONSUMED	0.	40.	7.
	0.000	0.000	17.049

COST/EFFECTIVENESS LIST 100

ABD =100.0

NEXT BOX ON=1

Table 8-9. Phase I Comparison of PRICE and TRI TAC

	PRICE (M)	TRI TAC (M)
Acquisition Cost	\$103.4	\$ 74.3
Support Cost	12.25	26.0
TOTAL LCC	116.6	100.8

Table 8-10. Phase I Data Base Comparison

LRU	Parameter	Price	TRI TAC
Processor	MTBF	710 Hrs	16,700 Hrs
	LRU Cost	\$29,030	\$19,200
	Dev. Cost	\$2.9M	\$4.16M
	LRU S.E.	\$142K	\$110K 22 LRU Testers at \$5K Ea.
L-Band Xmtr	MTBF	735 Hrs	500,000 Hrs
	LRU Cost	\$18,225	\$12,000
	Dev. Cost	\$1.85M	\$450K
	LRU S.E.	\$105,376	\$110,000 22 LRU Testers at \$5K Ea.
HF Xmtr	MTBF	683 Hrs	500,000 Hrs
	LRU Cost	\$14,583	\$12,000
	Dev. Cost	\$1.6M	\$450K
	LRU S.E.	\$89,201	\$110,000 22 LRU Testers at \$5K Ea.
UHF Xmtr	MTBF	582 Hrs	500,000 Hrs
	LRU Cost	\$9,215	\$6,000
	Dev. Cost	\$1.2M	\$450K
	LRU S.E.	\$62,883	\$110,000 22 LRU Testers at \$5K Ea.

Table 8-11. Phase I (Alternate A) Logistics Support Cost
Model Program (Mini)

MA SUBSYSTEM
3 LRU'S
7 AGE ITEMS

	SUBSYSTEMS	LRUS	AGE ITEMS	SOFTWARE
TOTAL	1	3	7	4
MAX	30	300	200	100

TOTAL SYSTEM COST (IN MILLIONS) IS \$ 2.10

SUBSYSTEM	COST	FRACTION OF TOTAL COST

MA	1.1974E+06	.5697

SUBSYSTEM MA

LRU NAME	COST	FRACTION OF SUBSYSTEM COST

PRO	6.5346E+05	.5499
HVU	2.9517E+05	.2465
L-B	2.4375E+05	.2036

1 SYSTEM COST BY EQUATION

C1 = 9.872773E+05 C3 = 6.510085E+04 C5 = 1.450000E+05

Table 8-11. Phase I (Alternate A) Logistics Support Cost
Model Program (Mini) (Continued)

1 SUBSYSTEM COST BY EQUATION

SUBSYSTEM MA

C1 = 9.872773E+05 C3 = 6.510085E+04 C5 = 1.450000E+05

LRU PRO

C1 = 4.531476E+05 C3 = 6.031038E+04 C5 = 1.450000E+05

LRU HVU

C1 = 2.920305E+05 C3 = 3.142967E+03 C5 = 0.

LRU L-B

C1 = 2.420992E+05 C3 = 1.647504E+03 C5 = 0.

TOTAL SOFTWARE COST IS \$ 904275.00
SOFTWARE ACQUISITION COST = \$ 655500.00
SOFTWARE SUPPORT COST = \$ 248775.00

PACKAGE	MAN MONTHS TO PROGRAM	NUMBER OF MEN TO SUPPORT IT	COST OF SUPPORT PROGRAMMERS
GPSF	24	♦	1440.00
HF	6	♦	180.00
JIT	5	♦	150.00
GPSA	3	♦	90.00

1 AGE BREAKOUT

AGE NAME	TOTAL BASE AGE REQUIREMENT	TOTAL DEPOT AGE REQUIREMENT
PRO-AGE	.04 (20)	.03 (1)
CARD 1	.00 (0)	.03 (1)
CARD 2	.00 (0)	.03 (1)
XMTR AGE	.00 (0)	.00 (0)
CARD 3	.00 (0)	.00 (0)

Table 8-11. Phase I (Alternate A) Logistics Support Cost
Model Program (Mini) (Continued)

LIST,MA

1.3600000 .,35000.,145.11,145.11,1.62,0.76,104.20,104.20,250.,10.
20.,17.63,.16,.31,.90,.001,1728.,1728.,.24,.08,.25, .25,.33,.15
SOFTWARE, .15,6000.,15000., .5,4
JIT ,5.,100.,100.,0.005
GPSA,3.,100.,100.,0.005
GPSF,10.,1200.,500.,0.01
HF , 6.,100.,100.,0.005
MA,0., 0.,0 .,0.,0.
16.42,32.62,0.,0.,168.,168.,1.25,0.,3
PRD,17857.,18200.,2.5,2.5,0.,0., 0.134,1.73,20.,1.
.01,.01, 0.15,0.85,0.01,0.,0.,0.,1,0.,3
PRD-AGE ,5000.,5000.,0.,0., 0.125, .9 ,.02
CARD 1 ,0.,20000.,0.,0.,1.,.98,.02
CARD 2 ,0.,20000.,0.,0.,1.,.98,.02
HVD, 312500.,14400.,2.5,2.5,0.,0., 0.134,1.73,25.6,1.
.01,.01, 0.15,0.85,0.01,0.,0.,0.,1,0.,2
XMTR AGE,5000.,5000.,0.,0.,0.16,.82,0.02
CARD 3 ,0.,20000.,0.,0.,1.,.9 ,.02
L-B,500000.,12000.,2.5,2.5,0.,0., 0.134,1.73,16.,1.
.01,.01,0.15,.85,0.01,0.,0.,0.,1,0.,2
XMTR AGE,5000.,5000.,0.,0.,0.16,.82,0.02
CARD 3 ,0.,20000.,0.,0.,1.,.9 ,.02

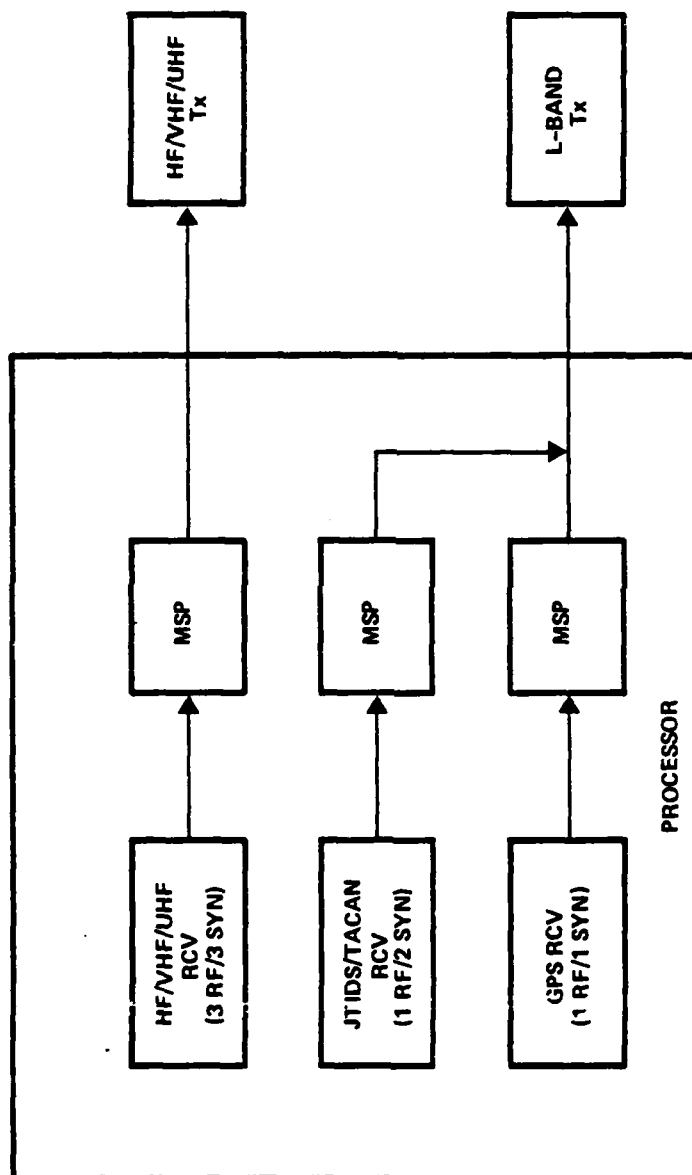


Figure 8-2. Phase I (Alternate A) Architecture

Table 8-12. Phase I (Alternate A) TRI TAC Output

10/16/78.

ALTERNATE "A" LIFE CYCLE COSTS

0			
0	ANNUAL O & S COSTS IN \$		
-	ELECTRIC POWER		24572.16
0	SPECIAL MATERIAL		0.00
0	OPERATOR PERSONNEL		0.00
0	ORG. MAINT. PERSONNEL	22.61	
0	INT. MAINT. PERSONNEL	171.84	
0	DEPOT MAINT. PERSONNEL	511971.40	
0	TOTAL MAINT. PERSONNEL		512165.85
0	SUPPORT EQUIP. MAINT.		7000.00
0	SOFTWARE MAINTENANCE		248775.00
0	SUPPLY PERSONNEL		5.83
0	SPARE PARTS & REPAIR MATERIAL		5987.84
0	INVENTORY MANAGEMENT	1365.00	
0	INVENTORY HOLDING	1538011.40	
0	INVENTORY ADMINISTRATION		1539376.40
0	TRANSPORTATION		397.65
0			
0	LIFE CYCLE COSTS IN \$K		
-	R & D ESTIMATE		4405.50
0	INVESTMENT-NON-RECURRING	18900.00	
0	INVESTMENT-RECURRING	44600.00	
0	TOTAL INVESTMENT		63500.00
0	OPERATIONS	245.72	
0	LOGISTICS SUPPORT	24161.09	
0	OPERATIONS & LOGISTICS SUPP. TOTAL		24406.81
0	TOTAL LIFE CYCLE COST		92312.31

Table 8-12. Phase I (Alternate A) TRI TAC Output
(Continued)

INPUT COST ELEMENT VALUES

R1	=	360.00	R21	=	.14	R65	=	.0476
R2	=	5.00	R22	=	0.00	R66	=	.0004
R3	=	1.19	R24	=	0.00	R67	=	40.00
R4	=	10.00	R25	=	0.00	R71	=	5.00
R5	=	5.00	R26	=	16.42	R72	=	95.00
R6	=	10.00	R27	=	5.00	R75	=	0.00
R7	=	23.00	R28	=	16.42	R76	=	0.00
R8	=	.48	R29	=	70000.00	TF	=	B
R9	=	1000.00	R50	=	0.00	R78	=	0.00
R10	=	0.00	R51	=	0.00	R79	=	0.00
R11	=	0.00	R52	=	0.00	X(1)	=	1070.00
R12(1)	=	0.00	R53	=	0.00	X(2)	=	770.00
R12(2)	=	3.00	R54	=	0.00	X(3)	=	580.00
R12(3)	=	0.00	R55	=	0.00	X(4)	=	460.00
R12(4)	=	0.00	R56	=	102400.00	Y(1)	=	720.00
R13	=	61.60	R57	=	3750000.00	Y(2)	=	420.00
R14	=	11150.00	R58	=	1060000.00	Y(3)	=	130.00
R15	=	.250	R59	=	0.00	Y(4)	=	110.00
R16	=	65360.00	R60	=	5.00	UP	=	T
R17	=	2.00	R61	=	20.50	R80	=	655500.00
R18	=	44600.00	R62	=	.18	R81	=	248775.00
R19	=	1000.00	R63	=	25.00	INVR	=	T
R20	=	85.00	R64	=	1500.00	INVN	=	T

Alternate "B" is a centralized configuration (Figure 8-3). The Mini-LSC output is shown in Table 8-13, while the TRI TAC output is shown in Table 8-14.

It is apparent from the small change in output values between the three configurations that the primary use determinant should be engineering judgement. The principle difference between the baseline and Alternate "A" is the reduction in transmitters (from 3 to 2).

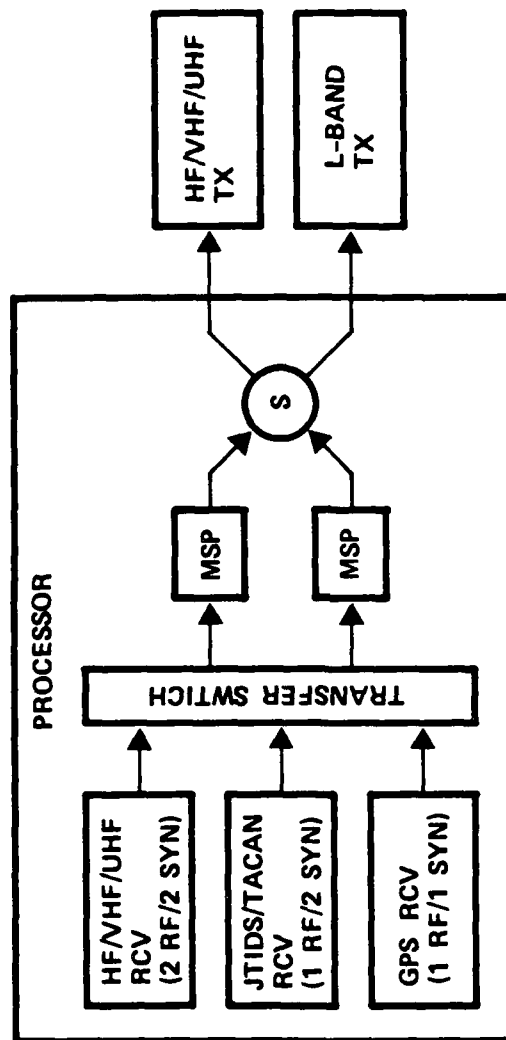


Figure 8-3. Phase I (Alternate B) Architecture

Table 8-13. Phase I (Alternate B) Mini-LSC Output

LOGISTICS SUPPORT COST MODEL PROGRAM (MINI)

XDTC 10/13/78.

MB SUBSYSTEM

3 LRUS

7 AGE ITEMS

	SUBSYSTEMS	LRUS	AGE ITEMS	SOFTWARE
TOTAL	1	3	7	5
MAX	30	300	200	100

TOTAL SYSTEM COST (IN MILLIONS) IS \$ 2.36

SUBSYSTEM	COST	FRACTION OF TOTAL COST
MB	1.3721E+06	.5810

SUBSYSTEM MB

LRU NAME	COST	FRACTION OF SUBSYSTEM COST
PRO	8.3317E+05	.6072
HVU	2.9517E+05	.2151
L-B	2.4375E+05	.1776

1 SYSTEM COST BY EQUATION

C1 = 1.144879E+06 C3 = 8.221338E+04 C5 = 1.450000E+05

Table 8-13. Phase I (Alternate B) Mini-LSC Output (Continued)

1 SUBSYSTEM COST BY EQUATION

SUBSYSTEM MB

C1 = 1.144879E+06 C3 = 8.221338E+04 C5 = 1.450000E+05

LRU PRO
C1 = 6.107493E+05 C3 = 7.742290E+04 C5 = 1.450000E+05

LRU HVU
C1 = 2.920305E+05 C3 = 3.142967E+03 C5 = 0.

LRU L-B
C1 = 2.420992E+05 C3 = 1.647504E+03 C5 = 0.

TOTAL SOFTWARE COST IS \$ 989325.00
SOFTWARE ACQUISITION COST = \$ 724500.00
SOFTWARE SUPPORT COST = \$ 264825.00

PACKAGE	MAN MONTHS TO PROGRAM	NUMBER OF MEN TO SUPPORT IT	COST OF SUPPORT PROGRAMMERS
GPSF	24	♦	1440.00
HF	6	♦	180.00
JIT	5	♦	150.00
I/O	4	♦	120.00
GPSA	3	♦	90.00

1 AGE BREAKOUT

AGE NAME	TOTAL BASE AGE REQUIREMENT	TOTAL DEPOT AGE REQUIREMENT
PRO-AGE	.04 (20)	.03 (1)
CARD 1	.00 (0)	.03 (1)
CARD 2	.00 (0)	.03 (1)
XMTR AGE	.00 (0)	.00 (0)
CARD 3	.00 (0)	.00 (0)

Table 8-13. Phase I (Alternate B) Mini-LSC Output (Continued)

```

1,3800000    .,35000.,145.11,145.11,1.62,0.76,104.20,104.20,250.,10.
20.,17.63.,16.,31.,90.,.001,1728.,1728.,.24.,.08.,.25, .25.,.33.,.15
COFTWARE, .15,6000.,15000., .5.5
JIT .5.,100.,100.,0.005
GPCR.3.,100.,100.,0.005
GPCF.10.,1200.,500.,0.01
HF , 6.,100.,100.,0.005
I/O 1., 1000., 250., .005
MB.0., 0.,0 .,0.,0.
16.42,32.62,0.,0.,168.,168.,1.25,0.,3
PRQ.16700.,24200.,2.5,2.5,0.,0., 0.134,1.73,20.,1.
.01.,.01, 0.15,0.85,0.01,0.,0.,0.,1,0.,3
PRQ-AGE ,5000.,5000.,0.,0., 0.125, .9 ,.02
CARD 1 ,0.,20000.,0.,0.,1.,.98,.02
CARD 2 ,0.,20000.,0.,0.,1.,.98,.02
HVV, 312500.,14400.,2.5,2.5,0.,0., 0.134,1.73,25.6,1.
.01.,.01, 0.15,0.85,0.01,0.,0.,0.,1,0.,2
XMTR AGE,5000.,5000.,0.,0.,0.16,.82,0.02
CARD 3 ,0.,20000.,0.,0.,1.,.9 ,.02
L-B.500000.,12000.,2.5,2.5,0.,0., 0.134,1.73,16.,1.
.01.,.01,0.15,.85,0.01,0.,0.,0.,1,0.,2
XMTR AGE,5000.,5000.,0.,0.,0.16,.82,0.02
CARD 3 ,0.,20000.,0.,0.,1.,.9 ,.02

```

Table 8-14. Phase I (Alternate B) TRI TAC Output

10/16/78.

ALTERNATE "B" LIFE CYCLE COSTS

0			
0	ANNUAL O & S COSTS IN \$		
-	ELECTRIC POWER		24572.16
0	SPECIAL MATERIAL		0.00
0	OPERATOR PERSONNEL		0.00
0	ORG. MAINT. PERSONNEL	22.61	
0	INT. MAINT. PERSONNEL	171.84	
0	DEPOT MAINT. PERSONNEL	571325.24	
0	TOTAL MAINT. PERSONNEL		571519.69
0	SUPPORT EQUIP. MAINT.		7000.00
0	SOFTWARE MAINTENANCE		264825.00
0	SUPPLY PERSONNEL		5.83
0	SPARE PARTS & REPAIR MATERIAL		6793.38
0	INVENTORY MANAGEMENT	1365.00	
0	INVENTORY HOLDING	1744918.76	
0	INVENTORY ADMINISTRATION		1746263.76
0	TRANSPORTATION		397.65
0			
0	LIFE CYCLE COSTS IN \$K		
-	R & D ESTIMATE		4474.50
0	INVESTMENT-NON-RECURRING	21300.00	
0	INVESTMENT-RECURRING	50600.00	
0	TOTAL INVESTMENT		71900.00
0	OPERATIONS	245.72	
0	LOGISTICS SUPPORT	26992.25	
0	OPERATIONS & LOGISTICS SUPP. TOTAL		27237.97
0	TOTAL LIFE CYCLE COST		103612.47

Table 8-14. Phase I (Alternate B) TRI TAC Output (Continued)

INPUT COST ELEMENT VALUES

R1	=	360.00	R21	=	.14	R65	=	.0476
R2	=	5.00	R22	=	0.00	R66	=	.0004
R3	=	1.19	R24	=	0.00	R67	=	40.00
R4	=	10.00	R25	=	0.00	R71	=	5.00
R5	=	5.00	R26	=	16.42	R72	=	35.00
R6	=	10.00	R27	=	5.00	R75	=	0.00
R7	=	23.00	R28	=	16.42	R76	=	0.00
R8	=	.48	R29	=	70000.00	TF	=	8
R9	=	1000.00	R50	=	0.00	R78	=	0.00
R10	=	0.00	R51	=	0.00	R79	=	0.00
R11	=	0.00	R52	=	0.00	X(1)	=	1070.00
R12(1)	=	0.00	R53	=	0.00	X(2)	=	770.00
R12(2)	=	3.00	R54	=	0.00	X(3)	=	580.00
R12(3)	=	0.00	R55	=	0.00	X(4)	=	460.00
R12(4)	=	0.00	R56	=	102400.00	Y(1)	=	720.00
R13	=	61.60	R57	=	3750000.00	Y(2)	=	420.00
R14	=	12650.00	R58	=	1060000.00	Y(3)	=	130.00
R15	=	.250	R59	=	0.00	Y(4)	=	110.00
R16	=	65360.00	R60	=	5.00	UP	=	T
R17	=	2.00	R61	=	20.50	R80	=	724500.00
R18	=	50600.00	R62	=	.18	R81	=	264825.00
R19	=	1000.00	R63	=	25.00	INVR	=	T
R20	=	85.00	R64	=	1500.00	INVN	=	T

8.4 PHASE II ECONOMIC ANALYSIS

The Phase II analysis made use of the same models employed in Phase I.

8.4.1 Background and Assumptions

The configuration for the Phase II TRW designed portion consists of three Line Replaceable Units (LRUs): an Integrated Command, Navigation, Identification Avionics (ICNIA) Terminal, and L-Band and VHF/UHF transmitters. This differs from the Phase I baseline configuration, but the number of LRUs is similar to the alternate architectures.

In general, the economic analysis contains the maintenance philosophy depicted in Figure 8-4. LRUs will be fault-isolated to the module (circuit board) level at the 20 intermediate level repair facilities. Circuit cards and troublesome LRUs will be sent to the depot for repair.

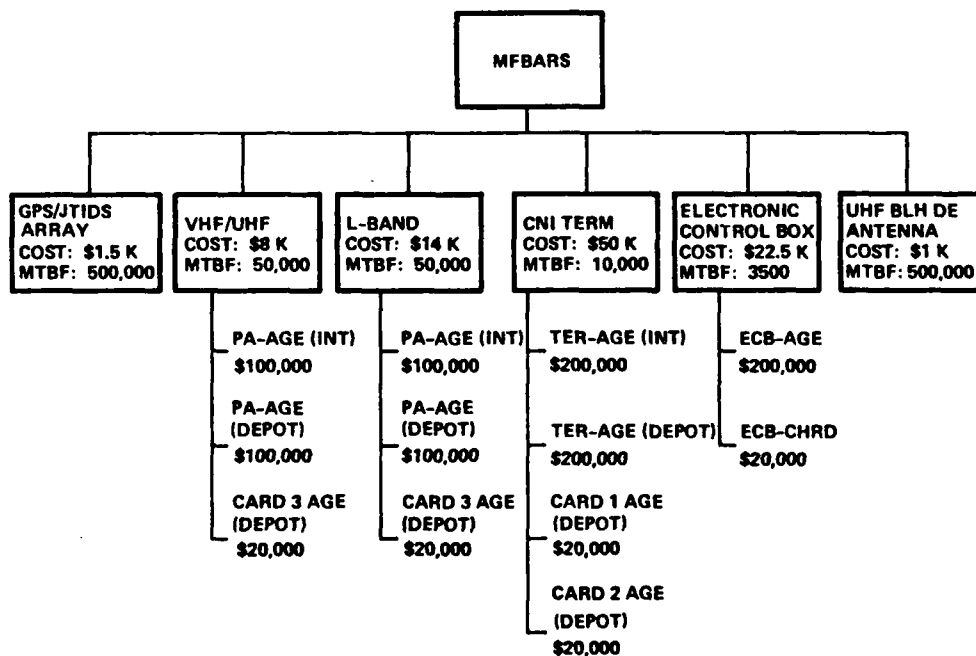


Figure 8-4. Maintenance Philosophy

Comparing the Phase I Alternate "A" data base with that of Phase II, the following important changes were made:

- a) The programmer cost estimate was increased from \$6000/MM to \$7500/MM.
- b) The number of software instructions increased from 13,400 to 62,790 primarily as a result of adding the INS interface.
- c) MTBF estimates were lowered:
 - Terminal was 17,857; is 10,000
 - L-band was 500,000; is 50,000
 - VHF/UHF was 312,500; is 50,000
- d) Cost per LRU estimates were changed:
 - Terminal was \$18,200; is \$50,000
 - L-band was \$12,000; is \$14,000
 - VHF/UHF was \$14,400; is \$8,000
- e) Weight estimates were changed:
 - Terminal was 20 pounds; is 45 pounds
 - L-band was 16 pounds; is 26 pounds
 - VHF-UHF was 25.6 pounds; is 26 pounds
- f) Cost of AGE equipment was changed:
 - Terminal AGE was \$5,000 each; is \$200,000 each
 - Transmitter AGE was \$5,000 rack; is \$100,000 each.

8.4.2 Phase II Model Outputs

The Phase II model outputs reflect the changes made to the TRW data base (8.4.1) and the addition of three Harris LRUs: 1) GPS/JTIDS Array, 2) UHF Blade Antenna, and 3) Electronic Control Box. There are no software costs associated with the Harris portion of the design.

8.4.2.1 Logistics Support Cost Model (LSC)

Two of the LSC printouts are shown in Table 8-15. In the first example, Table 8-15a depicts the MFBARS with the Harris supplied GPS/JTIDS Array, the UHF Blade Antenna, and the Electronic Control Box (ECB) and its associated AGE. In the second, Table 8-15b reflects the MFBARS design with a simpler TRW-supplied GPS/JTIDS Array and UHF blade antenna. It does not require an ECB as its complex AGE.

Due to the following reasons, the costs associated with TRW's three LRUs increased over those of Phase I.

- C1 - Initial and replacement LRU spare cost increased due to the lowering of the MTBF estimate.
- C3 - Off equipment maintenance cost also increased because of the lowered MTBFs.
- C5 - Cost of AGE is greater than Phase I because the equipment cost was increased to reflect the more sophisticated equipment required for fast turnaround.
- Software support costs increased because of the higher number of instructions and the higher programmer cost estimate.

The Harris antenna LRUs will not require their separate AGE. The test capability will be added to the AGE for testing the ICNIA Terminal, thereby permitting some cost savings. Table 8-16 defines the terms used in the LSC model.

8.4.2.2 TRI TAC Model

The output of the TRI TAC model is shown in Table 8-17. The input cost element values reflect the changes outlined in paragraph 8.4.1.

The addition of some cost elements, such as two advance development modules and product engineering for the LSIs and the increased software cost, increased R&D costs over those in Phase I.

Both operation and support (O&S) costs and the total LCC have increased over Phase I projections. The projected operating and support

Table 8-15a. Phase II LSC Printout Summary

MFARS LOGISTIC SUPPORT COST SUMMARY

INITIAL AND REPLACEMENT LRU SPARES	\$	6609983
OFF-EQUIPMENT MAINTENANCE		1084856
SUPPORT EQUIPMENT		21160000

TOTAL LOGISTIC SUPPORT COST	\$	28854839

SOFTWARE ACQUISITION COST	\$	3982086.40
SOFTWARE SUPPORT COST		907223.16

TOTAL SOFTWARE COST	\$	4889309.56

TOTAL SYSTEM COST	\$	33744149

Table 8-15a. Phase II LSC Printout Summary (Continued)

LOGISTICS SUPPORT COST MODEL PROGRAM (MINI) JLNH 10/15/79.

NF SUBSYSTEM
6 LRUS
9 AGE ITEMS

	SUBSYSTEMS	LRUS	AGE ITEMS	SOFTWARE
TOTAL	1	6	9	2
MAX	30	300	200	100

TOTAL SYSTEM COST (IN MILLIONS) IS \$ 33.74

OPTION? (TYPE 'HELP' FOR HELP)

SUBSYSTEM	COST	FRACTION OF TOTAL COST

NF	2.8855E+07	.8551

SUBSYSTEM NF

LRU NAME	COST	FRACTION OF SUBSYSTEM COST

TER	1.2071E+07	.4183
ECB	1.1944E+07	.4139
L-B	3.7719E+05	.0131
UHF	2.2091E+05	.0077
GPS	3.9045E+02	.0000
ANT	7.5703E+02	.0000

1 SYSTEM COST BY EQUATION

C1 = 6.609383E+06 C3 = 1.084856E+06 C5 = 2.116000E+07

Table 8-15a. Phase II LSC Printout Summary (Continued)

1 SUBSYSTEM COST BY EQUATION

SUBSYSTEM NF

C1 = 6.609383E+06 C3 = 1.084856E+06 C5 = 2.116000E+07

LRU TER
C1 = 3.187612E+06 C3 = 4.029517E+05 C5 = 3.480000E+06

LRU UHF
C1 = 1.980036E+05 C3 = 2.290720E+04 C5 = 0.000000

LRU L-B
C1 = 3.465063E+05 C3 = 3.062320E+04 C5 = 0.000000

LRU GPS
C1 = 5.581650E+02 C3 = 4.322857E+02 C5 = 0.000000

LRU ANT
C1 = 3.721100E+02 C3 = 3.849232E+02 C5 = 0.000000

LRU ECB
C1 = 2.876930E+06 C3 = 6.274970E+05 C5 = 3.440000E+06

TOTAL SOFTWARE COST IS \$ 4889309.56
SOFTWARE ACQUISITION COST = \$ 3982026.40
SOFTWARE SUPPORT COST = \$ 907223.16

PACKAGE	MAN MONTHS TO PROGRAM	NUMBER OF MEN TO SUPPORT IT	COST OF SUPPORT PROGRAMMERS
DATA	173.	1.	6495.22
SSNL	11.	0.	430.15

1 AGE BREAKOUT

AGE NAME	TOTAL BASE AGE REQUIREMENT	TOTAL DEPOT AGE REQUIREMENT
TER-AGE	.09 (20)	.07 (1)
CARD 1	.05 (20)	.10 (1)
CARD 2	.05 (20)	.10 (1)
PA-AGE	.04 (20)	.08 (1)
CARD 3	.02 (20)	.04 (1)
ECB-AGE	.56 (20)	.21 (1)
ECB-CARD	.56 (20)	.29 (1)

Table 8-15a. Phase II LSC Printout Summary (Continued)

```

1 ,3600000 ,35000.,145.11,145.11,1.62,0.74,104.20,104.20,250.,10.
 20.,17.63,.15,.31,.90,.001,1728.,1728.,.74,.08,.25, .25,.33,.15
SCFTWARE, .15, 7500., 15000., .5, 2
SGNL, 1., 3900., 340., 0.005
DATA, 1., 58890., 340., 0.005
MF, 0., 0., 0., 0., 0.
16.42,32.62,0.,0.,168.,168.,1.25,0.,6
TER, 10000.,50000.,2.5,2.5,0.,0., 0.134,1.73,45.,1.
.01,.01,.85,.95,.05,0.,0.,0.,1.,0., 3
TER-AGE ,200000.,200000.,20000.,20000., 0.5, .7 ,.02
CARD 1 ,0.,20000.,0000.,2000.,1.0,.50,.02
CARD 2 ,0.,20000.,0000.,2000.,1.,.50,.02
UHF, 50000.,8000.,2.5,2.5,0.,0., 0.134,1.73,26.,1.
.C1,.C1, .85, .95, .05, 0., 0., 0., 1., 0., 2
PA-AGE ,100000.,100000.,10000.,10000.,1., .70 ,0.02
CARD 3 ,0.,20000.,0000.,2000.,1.,.5 ,.02
L-B, 50000.,14000.,2.5,2.5,0.,0., 0.134,1.73,26.,1.
.01,.01,0.85,.95,.05,0.,0.,0.,1.,0.,2
PA-AGE , 100000., 100000.,10000.,10000.,1., .5, .7, 0., .02
CARD 3 ,0.,20000.,0000.,2000.,1.,.5 ,.02
GFS,500000.,1500.,2.5,2.5,0.,0.,0.134,1.73,9.,1.
.01,.01,.85,.1,.05,0.,0.,0.,1.,0.,0
ANT,500000.,1000.,2.5,2.5,0.,0.,0.134,1.73,3.,1.
.01,.01,.85,.1,.05,0.,0.,0.,1.,0.,0
ECB,3500.,22500.,2.5,2.5,0.,0.,0.134,1.73,17.,1.
.01,.C,1.85,.95,.05,0.,0.,0.,1.,0.,2
ECB-AGE ,200000.,200000.,20000.,20000.,0.5,.7,.02
ECB-CARD,0.,20000.,0.,2000.,0.5,0.5,.02

```

NOTE: Data input format is identical to Phase I
(see Table 8-4 for explanation)

Table 8-15b. Phase II LSC Printout Summary

MFARS LOGISTIC SUPPORT COST SUMMARY

INITIAL AND REPLACEMENT LRU SPARES	\$ 3732867
OFF-EQUIPMENT MAINTENANCE	457325
SUPPORT EQUIPMENT	12720000

TOTAL LOGISTIC SUPPORT COST	\$ 16910192

SOFTWARE ACQUISITION COST	\$ 3982086.40
SOFTWARE SUPPORT COST	907223.16

TOTAL SOFTWARE COST	\$ 4889309.56

TOTAL SYSTEM COST	\$ 21799502

Table 8-15b. Phase II LSC Printout Summary (Continued)

LOGISTICS SUPPORT COST MODEL PROGRAM (MINI) JLNH 10/15/79.

MF SUBSYSTEM
 5 LRUS
 7 AGE ITEMS

	SUBSYSTEMS	LRUS	AGE ITEMS	SOFTWARE
TOTAL	1	5	7	2
MAX	30	300	200	100

TOTAL SYSTEM COST (IN MILLIONS) IS \$ 21.80

OPTION? (TYPE 'HELP' FOR HELP)

SUBSYSTEM	COST	FRACTION OF TOTAL COST
MF	1.6910E+07	.7757

SUBSYSTEM MF

LRU NAME	COST	FRACTION OF SUBSYSTEM COST
TER	1.2071E+07	.7138
L-B	3.7719E+05	.0223
UHF	2.2091E+05	.0131
GPS	7.7020E+02	.0000
ANT	7.5703E+02	.0000

1 SYSTEM COST BY EQUATION

C1 = 3.732867E+06 C3 = 4.573251E+05 C5 = 1.272000E+07

Table 8-15b. Phase II LSC Printout Summary (Continued)

1 SUBSYSTEM COST BY EQUATION

SUBSYSTEM NF

C1 = 3.732867E+06 C3 = 4.573251E+05 C5 = 1.272000E+07

LRU TER
C1 = 3.187612E+06 C3 = 4.029517E+05 C5 = 2.420000E+06

LRU UHF
C1 = 1.920036E+05 C3 = 2.290720E+04 C5 = 0.000000

LRU L-B
C1 = 3.465063E+05 C3 = 3.062320E+04 C5 = 0.000000

LRU GPS
C1 = 3.721100E+02 C3 = 3.980857E+02 C5 = 0.000000

LRU ANT
C1 = 3.721100E+02 C3 = 3.849232E+02 C5 = 0.000000

TOTAL SOFTWARE COST IS \$ 4889309.56
SOFTWARE ACQUISITION COST = \$ 3982086.40
SOFTWARE SUPPORT COST = \$ 907223.16

PACKAGE	MAN MONTHS TO PROGRAM	NUMBER OF MEN TO SUPPORT IT	COST OF SUPPORT PROGRAMMERS
DATA	173.	1.	6495.22
SGNL	11.	0.	430.15

1 AGE BREAKOUT

AGE NAME	TOTAL BASE AGE REQUIREMENT	TOTAL DEPOT AGE REQUIREMENT
TEP-AGE	.09 (20)	.07 (1)
CARD 1	.05 (20)	.10 (1)
CARD 2	.05 (20)	.10 (1)
PA-AGE	.04 (20)	.08 (1)
CARD 3	.02 (20)	.04 (1)

Table 8-15b. Phase II LSC Printout Summary (Continued)

```

1 ,3600000    ,.35000.,145.11,145.11,1.62,0.78,104.20,104.20,250.,10.
  20.,17.63,.16,.31,.90,.001,1728.,1728.,.24,.02,.25, .25,.33,.15
SOFTWARE, .15, 7500., 15000., .5, 2
SGL, 1., 3900., 340., 0.005
DATA, 1., 58290., 340., 0.005
NF, 0., 0., 0., 0., 0., 0.
16.42,32.62,0.,0.,168.,168.,1.25,0.,5
TER, 10000.,50000.,2.5,2.5,0.,0., 0.134,1.73,45.,1.
.01, .01, .25, .95, .05, 0., 0., 0., 1., 0., 3
TER-AGE ,200000.,200000.,20000.,20000., 0.5, .7 ,.02
CARD 1 ,0.,20000.,0000.,2000.,1.0,.50,.02
CARD 2 ,0.,20000.,0000.,2000.,1.,.50,.02
UHF, 50000.,2000.,2.5,2.5,0.,0., 0.134,1.73,26.,1.
.01,.01, .25, .95, .05, 0., 0., 0., 1., 0., 2
PA-AGE ,100000.,100000.,10000.,10000.,1., .70 ,0.02
CARD 3 ,0.,20000.,0000.,2000.,1.,.5 ,.02
L-B, 50000.,14000.,2.5,2.5,0.,0., 0.134,1.73,26.,1.
.01,.01,0.25,.95,.05, 0.,0.,0.,1.,0.,2
PA-AGE , 100000., 100000.,10000.,10000.,1., .5, .7, 0., .02
CARD 3 ,0.,20000.,0000.,2000.,1.,.5 ,.02
GPS,500000.,1000.,2.5,2.5,0.,0.,0.134,1.73,9.,1.
.01,.01,.25,.1,.05,0.,0.,0.,1.,0.,0
ANT,500000.,1000.,2.5,2.5,0.,0.,0.134,1.73,3.,1.
.01,.01,.25,.1,.05,0.,0.,0.,1.,0.,0
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Table 8-16. LSC Definition of Terms

Term	Definition
SGNL	Software package for ICNIA terminal signal processor
DATA	Software package for ICNIA terminal INS interface
MF	Name assigned to MFBARS subsystem
TER	ICNIA terminal
TER-AGE	AGE to test the ICNIA terminal
CARD 1	AGE to test part of the cards complement of the ICNIA terminal
CARD 2	AGE to test part of the card complement of the ICNIA terminal
UHF	VHF/UHF power amplifier
PA-AGE	AGE to test both the VHF/UHF power amplifier and the L-Band power amplifier
CARD 3	AGE to test the cards of both power amplifiers
L-B	L-Band power amplifier
GPS	GPS/JTIDS array
ANT	UHF blade antenna
ECB	Electronic control box for the antennas

Table 8-17. Phase II TRI TAC ICNIA Terminal Input and Cost Printout

INPUT COST ELEMENT VALUES

R1	=	360.00	R21	=	.15	R65	=	.0476
R2	=	5.00	R22	=	0.00	R66	=	.0004
R3	=	1.19	R24	=	0.00	R67	=	40.00
R4	=	10.00	R25	=	0.00	R71	=	5.00
R5	=	5.00	R26	=	16.42	R72	=	95.00
R6	=	10.00	R27	=	5.00	R75	=	0.00
R7	=	23.00	R29	=	16.42	R76	=	0.00
R8	=	.48	R29	=	200000.00	TF	=	0
R9	=	1000.00	R50	=	0.00	R78	=	0.00
R10	=	0.00	R51	=	0.00	R79	=	0.00
R11	=	0.00	R52	=	0.00	X(1)	=	1070.00
R12(1)	=	1.00	R53	=	0.00	X(2)	=	770.00
R12(2)	=	0.00	R54	=	0.00	X(3)	=	580.00
R12(3)	=	0.00	R55	=	0.00	X(4)	=	460.00
R12(4)	=	0.00	R56	=	0.00	Y(1)	=	720.00
R13	=	45.00	R57	=	0.00	Y(2)	=	420.00
R14	=	50000.00	R58	=	0.00	Y(3)	=	130.00
R15	=	.250	R59	=	0.00	Y(4)	=	110.00
R16	=	1000.00	R60	=	5.00	UP	=	T
R17	=	2.00	R61	=	45.00	R80	=	3884100.00
R18	=	50000.00	R62	=	.18	R81	=	907223.00
R19	=	1000.00	R63	=	25.00	INVR	=	T
R20	=	85.00	R64	=	1500.00	INVN	=	T

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ICNIA TERMINAL

0	ANNUAL O & S COSTS IN \$	
-	ELECTRIC POWER	25920.00
0	SPECIAL MATERIAL	0.00
0	OPERATOR PERSONNEL	0.00
0	ORG. MAINT. PERSONNEL	1477.80
0	INT. MAINT. PERSONNEL	11231.28
0	DEPOT MAINT. PERSONNEL	543453.81
0	TOTAL MAINT. PERSONNEL	576162.89
0	SUPPORT EQUIP. MAINT.	20000.00
0	SOFTWARE MAINTENANCE	907223.00
0	SUPPLY PERSONNEL	381.27
0	SPARE PARTS & REPAIR MATERIAL	175500.00
0	INVENTORY MANAGEMENT	755.00
0	INVENTORY HOLDING	1523175.00
0	INVENTORY ADMINISTRATION	1523930.00
0	TRANSPORTATION	57050.15
0	LIFE CYCLE COSTS IN \$K	
-	R & D ESTIMATE	3884.10
0	INVESTMENT-NON-RECURRING	20000.00
0	INVESTMENT-RECURRING	40700.00
0	TOTAL INVESTMENT	70000.00
0	OPERATIONS	759.20
0	LOGISTICS SUPPORT	48397.47
0	OPERATIONS & LOGISTICS SUPP. TOTAL	48656.67
0	TOTAL LIFE CYCLE COST	122540.77

Table 8-17. Phase II TRI TAC ICNIA Terminal Input and Cost Printout
(Continued)

INPUT COST ELEMENT VALUES

R1	"	360.00	R21	"	.20	R65	"	.0476
R2	"	5.00	R22	"	0.00	R66	"	.0004
R3	"	1.19	R24	"	0.00	R67	"	40.00
R4	"	10.00	R25	"	0.00	R71	"	5.00
R5	"	5.00	R26	"	16.42	R72	"	95.00
R6	"	10.00	R27	"	5.00	R75	"	0.00
R7	"	23.00	R29	"	14.42	R76	"	0.00
R8	"	.48	R29	"	100000.00	TF	"	8
R9	"	1000.00	R50	"	0.00	R78	"	0.00
R10	"	0.00	R51	"	0.00	R79	"	0.00
R11	"	0.00	R52	"	0.00	X(1)	"	1070.00
R12(1)	"	0.00	R53	"	0.00	X(2)	"	770.00
R12(2)	"	0.00	R54	"	0.00	X(3)	"	580.00
R12(3)	"	1.00	R55	"	0.00	X(4)	"	460.00
R12(4)	"	0.00	R56	"	0.00	Y(1)	"	720.00
R13	"	26.00	R57	"	0.00	Y(2)	"	420.00
R14	"	14000.00	R58	"	0.00	Y(3)	"	130.00
R15	"	.250	R59	"	0.00	Y(4)	"	110.00
R16	"	50000.00	R60	"	5.00	UP	"	T
R17	"	2.00	R61	"	25.00	R80	"	0.00
R18	"	14000.00	R62	"	.18	R81	"	0.00
R19	"	1000.00	R63	"	25.00	INVR	"	T
R20	"	85.00	R64	"	1500.00	INVN	"	T

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L-BAND POWER AMPLIFIER

0	ANNUAL O & S COSTS IN \$	
0	ELECTRIC POWER	34560.00
0	SPECIAL MATERIAL	0.00
0	OPERATOR PERSONNEL	0.00
0	ORG. MAINT. PERSONNEL	29.56
0	INT. MAINT. PERSONNEL	224.63
0	DEPOT MAINT. PERSONNEL	124920.56
0	TOTAL MAINT. PERSONNEL	165174.74
0	SUPPORT EQUIP. MAINT.	10000.00
0	SOFTWARE MAINTENANCE	0.00
0	SUPPLY PERSONNEL	7.63
0	SPARE PARTS & REPAIR MATERIAL	9828.00
0	INVENTORY MANAGEMENT	175.00
0	INVENTORY HOLDING	421869.78
0	INVENTORY ADMINISTRATION	482044.76
0	TRANSPORTATION	659.26
0	LIFE CYCLE COSTS IN \$K	
0	R & D ESTIMATE	0.00
0	INVESTMENT-NON-RECURRING	5600.00
0	INVESTMENT-RECURRING	14000.00
0	TOTAL INVESTMENT	19600.00
0	OPERATIONS	345.60
0	LOGISTICS SUPPORT	6877.14
0	OPERATIONS & LOGISTICS SUPP. TOTAL	7222.74
0	TOTAL LIFE CYCLE COST	26822.74

Table 8-17. Phase II TRI TAC ICNIA Terminal Input and Cost Printout
(Continued)

INPUT COST ELEMENT VALUES

R1	=	360.00	R21	=	.15	R65	=	.0476
R2	=	5.00	R22	=	0.00	R66	=	.0004
R3	=	1.19	R24	=	0.00	R67	=	40.00
R4	=	10.00	R25	=	0.00	R71	=	5.00
R5	=	5.00	R26	=	15.42	R72	=	95.00
R6	=	10.00	R27	=	5.00	R75	=	0.00
R7	=	23.00	R28	=	16.42	R76	=	0.00
R8	=	.48	R29	=	100000.00	TF	=	8
R9	=	1000.00	R50	=	0.00	R78	=	0.00
R10	=	0.00	R51	=	0.00	R79	=	0.00
R11	=	0.00	R52	=	0.00	X(1)	=	1070.00
R12(1)	=	0.00	R53	=	0.00	X(2)	=	770.00
R12(2)	=	0.00	R54	=	0.00	X(3)	=	580.00
R12(3)	=	1.00	R55	=	0.00	X(4)	=	460.00
R12(4)	=	0.00	R56	=	0.00	Y(1)	=	720.00
R13	=	26.00	R57	=	0.00	Y(2)	=	420.00
R14	=	8000.00	R58	=	0.00	Y(3)	=	130.00
R15	=	.250	R59	=	0.00	Y(4)	=	110.00
R16	=	50000.00	R60	=	5.00	UP	=	T
R17	=	2.00	R61	=	26.00	R80	=	0.00
R18	=	8000.00	R62	=	.15	R81	=	0.00
R19	=	1000.00	R63	=	25.00	INVR	=	T
R20	=	85.00	R64	=	1500.00	INVA	=	T

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VHF/UHF POWER AMPLIFIER

0	ANNUAL O & S COSTS IN \$	
-	ELECTRIC POWER	25920.00
0	SPECIAL MATERIAL	0.00
0	OPERATOR PERSONNEL	0.00
0	ORG. MAINT. PERSONNEL	29.56
0	INT. MAINT. PERSONNEL	224.63
0	DEPOT MAINT. PERSONNEL	114149.59
0	TOTAL MAINT. PERSONNEL	114403.87
0	SUPPORT EQUIP. MAINT.	10000.00
0	SOFTWARE MAINTENANCE	0.00
0	SUPPLY PERSONNEL	7.63
0	SPARE PARTS & REPAIR MATERIAL	5616.00
0	INVENTORY MANAGEMENT	175.00
0	INVENTORY HOLDING	275354.16
0	INVENTORY ADMINISTRATION	275529.16
0	TRANSPORTATION	659.26
0	LIFE CYCLE COSTS IN \$K	
-	R & D ESTIMATE	0.00
0	INVESTMENT-NON-RECURRING	3200.00
0	INVESTMENT-RECURRING	8000.00
0	TOTAL INVESTMENT	11200.00
0	OPERATIONS	259.20
0	LOGISTICS SUPPORT	4062.15
0	OPERATIONS & LOGISTICS SUPP. TOTAL	4321.36
0	TOTAL LIFE CYCLE COST	15521.36

Table 8-17. Phase II TRI TAC ICNIA Terminal Input and Cost Printout
(Continued)

INPUT COST ELEMENT VALUES

R1	=	360.00	R21	=	0.00	R65	=	.0476
R2	=	5.00	R22	=	0.00	R66	=	.0004
R3	=	1.19	R24	=	0.00	R67	=	40.00
R4	=	10.00	R25	=	0.00	R71	=	5.00
R5	=	5.00	R26	=	14.42	R72	=	95.00
R6	=	10.00	R27	=	5.00	R75	=	0.00
R7	=	23.00	R28	=	16.42	R76	=	0.00
R8	=	.48	R29	=	0.00	TF	=	B
R9	=	1000.00	R50	=	0.00	R78	=	C.00
R10	=	0.00	R51	=	0.00	R79	=	0.00
R11	=	0.00	R52	=	0.00	X(1)	=	1070.00
R12(1)	=	0.00	R53	=	0.00	X(2)	=	770.00
R12(2)	=	0.00	R54	=	0.00	X(3)	=	580.00
R12(3)	=	1.00	R55	=	0.00	X(4)	=	460.00
R12(4)	=	0.00	R56	=	0.00	Y(1)	=	720.00
R13	=	12.40	R57	=	0.00	Y(2)	=	420.00
R14	=	3000.00	R58	=	0.00	Y(3)	=	130.00
R15	=	.250	R59	=	0.00	Y(4)	=	110.00
R16	=	50000.00	R60	=	5.00	LP	=	T
R17	=	2.00	R61	=	12.40	R80	=	C.00
R18	=	3000.00	R62	=	.18	R81	=	0.00
R19	=	1000.00	R63	=	25.00	INVR	=	T
R20	=	85.00	R64	=	1400.00	INVM	=	T

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GPS/JTIDS ARRAY

0			
0	ANNUAL O & S COSTS IN \$		
-	ELECTRIC POWER		0.00
0	SPECIAL MATERIAL		0.00
0	OPERATOR PERSONNEL		0.00
0	ORG. MAINT. PERSONNEL	29.56	
0	INT. MAINT. PERSONNEL	224.63	
0	DEPOT MAINT. PERSONNEL	4277.38	
0	TOTAL MAINT. PERSONNEL		48531.56
0	SUPPORT EQUIP. MAINT.		C.00
0	SOFTWARE MAINTENANCE		0.00
0	SUPPLY PERSONNEL		7.63
0	SPARE PARTS & REPAIR MATERIAL		2106.00
0	INVENTORY MANAGEMENT	175.00	
0	INVENTORY HOLDING	103257.81	
0	INVENTORY ADMINISTRATION		103432.81
0	TRANSPORTATION		314.44
0			
0	LIFE CYCLE COSTS IN \$K		
-	R & O ESTIMATE		C.00
0	INVESTMENT-NON-RECURRING	1200.00	
0	INVESTMENT-RECURRING	3000.00	
0	TOTAL INVESTMENT		4200.00
0	OPERATIONS	0.00	
0	LOGISTICS SUPPORT	1543.92	
0	OPERATIONS & LOGISTICS SUPP. TOTAL		1543.92
0	TOTAL LIFE CYCLE COST		5743.92

Table 8-17. Phase II TRI TAC ICNIA Terminal Input and Cost Printout
(Continued)

INPUT COST ELEMENT VALUES

R1	"	360.00	R21	"	0.00	R65	"	.0476
R2	"	5.00	R22	"	0.00	R66	"	.0004
R3	"	1.19	R24	"	0.00	R67	"	40.00
R4	"	10.00	R25	"	0.00	R71	"	5.00
R5	"	5.00	R26	"	16.42	R72	"	95.00
R6	"	10.00	R27	"	5.00	R75	"	0.00
R7	"	23.00	R28	"	16.42	R76	"	0.00
R8	"	.48	R29	"	0.00	TF	"	P
R9	"	1000.00	R50	"	0.00	R78	"	0.00
R10	"	0.00	R51	"	0.00	R79	"	0.00
R11	"	0.00	R52	"	0.00	X(1)	"	1070.00
R12(1)	"	0.00	R53	"	0.00	X(2)	"	770.00
R12(2)	"	0.00	R54	"	0.00	X(3)	"	580.00
R12(3)	"	0.00	R55	"	0.00	X(4)	"	460.00
R12(4)	"	1.00	R56	"	0.00	Y(1)	"	720.00
R13	"	4.00	R57	"	0.00	Y(2)	"	420.00
R14	"	1000.00	R58	"	0.00	Y(3)	"	130.00
R15	"	.250	R59	"	0.00	Y(4)	"	110.00
R16	"	50000.00	R60	"	5.00	UP	"	T
R17	"	2.00	R61	"	4.00	R80	"	0.00
R18	"	1000.00	R62	"	.18	R81	"	0.00
R19	"	1000.00	R63	"	25.00	INVR	"	T
R20	"	85.00	R64	"	1500.00	INVN	"	T

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UHF BLADE ANTENNA

0				
0		ANNUAL O & S COSTS IN \$		
-		ELECTRIC POWER		0.00
0		SPECIAL MATERIAL		0.00
0		OPERATOR PERSONNEL		0.00
0		CRG. MAINT. PERSONNEL	20.56	
0		INT. MAINT. PERSONNEL	274.63	
0		DEPOT MAINT. PERSONNEL	18255.46	
0		TOTAL MAINT. PERSONNEL		18509.64
0		SUPPORT EQUIP. MAINT.		0.00
0		SOFTWARE MAINTENANCE		0.00
0		SUPPLY PERSONNEL		7.63
0		SPARE PARTS & REPAIR MATERIAL		702.00
0		INVENTORY MANAGEMENT	145.00	
0		INVENTORY HOLDING	34419.27	
0		INVENTORY ADMINISTRATION		34564.27
0		TRANSPORTATION		101.46
0				
0		LIFE CYCLE COSTS IN \$K		
-		R & D ESTIMATE		0.00
0		INVESTMENT-NON-RECURRING	400.00	
0		INVESTMENT-RECURRING	1000.00	
0		TOTAL INVESTMENT		1400.00
0		OPERATIONS	0.00	
0		LOGISTICS SUPPORT	538.85	
0		OPERATIONS & LOGISTICS SUPP. TOTAL		538.85
0		TOTAL LIFE CYCLE COST		1938.85

Table 8-17. Phase II TRI TAC ICNIA Terminal Input and Cost Printout
(Continued)

INPUT COST ELEMENT VALUES

R1	•	360.00	R21	•	.07	R65	•	.0478
R2	•	5.00	R22	•	0.00	R66	•	.0004
R3	•	1.19	R24	•	0.00	R67	•	40.00
R4	•	10.00	R25	•	0.00	R71	•	5.00
R5	•	5.00	R26	•	16.42	R72	•	95.00
R6	•	10.00	R27	•	5.00	R75	•	0.00
R7	•	23.00	R28	•	16.42	R76	•	0.00
R8	•	.48	R29	•	200000.00	TF	•	B
R9	•	1000.00	R50	•	0.00	R78	•	0.00
R10	•	0.00	R51	•	0.00	R79	•	0.00
R11	•	0.00	R52	•	0.00	X(1)	•	1070.00
R12(1)	•	0.00	R53	•	0.00	X(2)	•	770.00
R12(2)	•	1.00	R54	•	0.00	X(3)	•	580.00
R12(3)	•	0.00	R55	•	0.00	X(4)	•	460.00
R12(4)	•	0.00	R56	•	0.00	Y(1)	•	720.00
R13	•	17.00	R57	•	0.00	Y(2)	•	420.00
R14	•	22500.00	R58	•	0.00	Y(3)	•	130.00
R15	•	.250	R59	•	0.00	Y(4)	•	110.00
R16	•	1000.00	R60	•	5.00	UP	•	T
R17	•	2.00	R61	•	17.00	R80	•	0.00
R18	•	22500.00	R62	•	.1	R81	•	0.00
R19	•	1000.00	R63	•	25.00	INVR	•	T
R20	•	25.00	R64	•	1500.00	INVR	•	T

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ELECTRONIC CONTROL BOX

0	ANNUAL O & S COSTS IN \$	
-	ELECTRIC POWER	12096.00
0	SPECIAL MATERIAL	0.00
0	OPERATOR PERSONNEL	0.00
0	CRG. MAINT. PERSONNEL	1477.00
0	INT. MAINT. PERSONNEL	11331.29
0	DEPOT MAINT. PERSONNEL	278202.43
0	TOTAL MAINT. PERSONNEL	290911.51
0	SUPPORT EQUIP. MAINT.	20000.00
0	SOFTWARE MAINTENANCE	0.00
0	SUPPLY PERSONNEL	361.27
0	SPARE PARTS & REPAIR MATERIAL	789750.00
0	INVENTORY MANAGEMENT	455.00
0	INVENTORY HOLDING	685429.75
0	INVENTORY ADMINISTRATION	685883.75
0	TRANSPORTATION	21553.43
0	LIFE CYCLE COSTS IN \$K	
-	R & D ESTIMATE	0.00
0	INVESTMENT-NON-RECURRING	9000.00
0	INVESTMENT-RECURRING	22500.00
0	TOTAL INVESTMENT	31500.00
0	OPERATIONS	170.94
0	LOGISTICS SUPPORT	18084.80
0	OPERATIONS & LOGISTICS SUPP. TOTAL	18205.76
0	TOTAL LIFE CYCLE COST	49705.76

Table 8-17. Phase II TRI TAC ICNIA Terminal Input and Cost Printout
(Continued)

INPUT COST ELEMENT VALUES

R1	=	360.00	P21	=	0.00	R65	=	.0476
R2	=	5.00	P22	=	0.00	R66	=	.0004
R3	=	1.19	P24	=	0.00	R67	=	40.00
R4	=	10.00	P25	=	0.00	R71	=	5.00
R5	=	5.00	P26	=	16.42	R72	=	95.00
R6	=	10.00	P27	=	5.00	R75	=	0.00
R7	=	23.00	P28	=	16.42	R76	=	0.00
R8	=	.48	P29	=	0.00	TF	=	B
R9	=	1000.00	P50	=	0.00	R78	=	0.00
R10	=	0.00	P51	=	0.00	R79	=	0.00
R11	=	0.00	P52	=	0.00	X(1)	=	1070.00
R12(1)	=	0.00	P53	=	0.00	X(2)	=	770.00
R12(2)	=	0.00	P54	=	0.00	X(3)	=	580.00
R12(3)	=	0.00	P55	=	0.00	X(4)	=	460.00
R12(4)	=	0.00	P56	=	172400.00	Y(1)	=	720.00
R13	=	0.00	P57	=	20000000.00	Y(2)	=	420.00
R14	=	0.00	P58	=	17000000.00	Y(3)	=	130.00
R15	=	.250	P59	=	0.00	Y(4)	=	110.00
R16	=	0.00	P60	=	5.00	LP	=	T
R17	=	2.00	P61	=	0.00	R80	=	0.00
R18	=	0.00	P62	=	.10	RE1	=	0.00
R19	=	1000.00	P63	=	25.00	INVR	=	T
R20	=	25.00	P64	=	1500.00	INVN	=	T

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#SYSTEMS# COSTS FOR FOLLOWING FAMILY:

ICNIA TERMINAL
L-BAND POWER AMPLIFIER
VHF/UHF POWER AMPLIFIER
GPS/JTIDS ARRAY
UHF BLADE ANTENNA
ELECTRONIC CONTROL BOX

0	ANNUAL O & S COSTS IN \$	
0	- ELECTRIC POWER	0.00
0	SPECIAL MATERIAL	0.00
0	OPERATOR PERSONNEL	0.00
0	ORG. MAINT. PERSONNEL	0.00
0	INT. MAINT. PERSONNEL	0.00
0	DEPOT MAINT. PERSONNEL	0.00
0	TOTAL MAINT. PERSONNEL	0.00
0	SUPPORT EQUIP. MAINT.	0.00
0	SOFTWARE MAINTENANCE	0.00
0	SUPPLY PERSONNEL	0.00
0	SPARE PARTS & REPAIR MATERIAL	0.00
0	INVENTORY MANAGEMENT	0.00
0	INVENTORY HOLDING	0.00
0	INVENTORY ADMINISTRATION	0.00
0	TRANSPORTATION	0.00
0	LIFE CYCLE COSTS IN \$K	
0	- R & D ESTIMATE	20000.00
0	INVESTMENT-NON-RECURRING	12000.00
0	INVESTMENT-RECURRING	0.00
0	TOTAL INVESTMENT	12000.00
0	OPERATIONS	0.00
0	LOGISTICS SUPPORT	1024.00
0	OPERATIONS & LOGISTICS SUPP. TOTAL	1024.00
0	TOTAL LIFE CYCLE COST	33024.00

Table 8-17. Phase II TRI TAC ICNIA Terminal Input and Cost Printout
(Continued)

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TOTAL COSTS OVER FAMILY:

	ICNIA TERMINAL	
	L-BAND POWER AMPLIFIER	
	VHF/UHF POWER AMPLIFIER	
	GPS/JTIDS ARRAY	
	UHF BLADE ANTENNA	
	ELECTRONIC CONTROL BOX	
0		
0	ANNUAL O & S COSTS IN \$	
-	ELECTRIC POWER	98496.00
0	SPECIAL MATERIAL	0.00
0	OPERATOR PERSONNEL	0.00
0	ORG. MAINT. PERSONNEL	3073.42
0	INT. MAINT. PERSONNEL	23361.06
0	DEPOT MAINT. PERSONNEL	1207259.33
0	TOTAL MAINT. PERSONNEL	
0	SUPPORT EQUIP. MAINT.	1233694.21
0	SOFTWARE MAINTENANCE	60000.00
0	SUPPLY PERSONNEL	907223.00
0	SPARE PARTS & REPAIR MATERIAL	793.05
0	INVENTORY MANAGEMENT	2563002.00
0	INVENTORY HOLDING	1880.00
0	INVENTORY ADMINISTRATION	3103504.77
0	TRANSPORTATION	3105384.77
0		80337.99
0		
0	LIFE CYCLE COSTS IN \$K	
-	R & D ESTIMATE	23884.10
0	INVESTMENT-NON-RECURRING	51400.00
0	INVESTMENT-RECURRING	98500.00
0	TOTAL INVESTMENT	
0	OPERATIONS	149900.00
0	LOGISTICS SUPPORT	984.96
0	OPERATIONS & LOGISTICS SUPP. TOTAL	90528.35
0	TOTAL LIFE CYCLE COST	81513.31
C		255297.41

costs are \$60.2M, 30.4 percent of the total LCC of \$197.8, which includes the system LCC.

The addition of the three Harris LRUs brought the total LCC to \$255.3M, O&S to \$81.5M, and the O&S proportion of the total LCC to 31.9%.

8.4.2.3 SCEP

The SCEP model was run twice; once to predict the number of man-months required for each of the two software packages and again to connect that prediction to a dollar value. As shown in Table 8-18, the model estimates a 42.7 man-month effort for the signal processor software and 428.7 man-months for the INS (Data) software. Using \$7500/MM, this translates to \$3.53M (Table 8-19).

8.4.2.4 PRICE

The PRICE model is run by the customer from data sheets supplied by TRW. Tables 8-20 and 8-21 present the software and hardware input sheets, respectively, which include TRW units only. The latter covers development costs only. Table 8-22 is composed of the PRICE software printouts and Table 8-23 provides the PRICE hardware development and integration results.

Table 8-24 shows the Harris provided PRICE hardware input data sheets for the MFBARS antenna system. The results of this rough parametric cost analysis of the antenna system were not provided to TRW and are, therefore, not included in this report. According to Harris, the analysis indicates that the system might be built in 1000 unit quantities for a unit cost of approximately \$25,000. These analyses were based on estimated costs of similar units used in other Harris systems.

Harris offers a caution that since the electronics are characterized at the box level and since the RF hybrid components within the box are quite complex fabrications, the PRICE model may underestimate the cost of this portion of the system.

8.5 CONCLUSIONS

The economic analyses of MFBARS (Phases I and II) provide insight as to the range of life cycle costs that may be encountered in various stages of the hardware architecture. The cost models used are economic

Table 8-18. TRW Software Cost Estimation Program

THIS IS EXPLORATORY AND DOES NOT REPRESENT AN ORGANIZATIONAL COMMITMENT

VERSION SCEP1.51

DATE 08/13/79

TIME 14:26

** ESTIMATE REPORT **

MFBARS-2

ESTIMATED EFFORT BY PHASE IN MANMONTHS AT 152 HOURS/MM

OPTIMUM CONTRACT LIFE = 26 MONTHS

TOTAL SYSTEM

PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
48.0	139.4	118.4	165.1	470.8	62790	133.4

BY SUBSYSTEM

S/S	IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
1	SIGNAL	3.0	9.5	14.5	15.8	42.7	3900	91.3
2	DATA	45.0	129.9	103.9	149.2	428.1	58890	137.6

BY UNIT

SUBSYSTEM 1 SIGNAL

UNIT	IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
1	SIGNAL	3.0	9.5	14.5	15.8	42.7	3900	91.3

SUBSYSTEM 2 DATA

UNIT	IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	DEMI/MM
1	DATA	45.0	129.9	103.9	149.2	428.1	58890	137.6

Table 8-19. TRW Software Cost Estimation Program

THIS IS EXPLURATORY AND DOES NOT REPRESENT AN ORGANIZATIONAL COMMITMENT

VERSION SCEP1.51

DATE 08/13/79

TIME 14:26

** ESTIMATE REPORT **

HFBARS-2

ESTIMATED EFFORT BY PHASE IN DOLLARS AT
7500, 7500, 7500, 7500, DOLLARS/MM

OPTIMUM CONTRACT LIFE = 26 MONTHS

TOTAL SYSTEM

PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
359652	1045447	887985	1237897	3530981	62790	56.23

BY SUBSYSTEM

S/S	IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
1	SIGNAL	22339	70987	108417	118601	320343	3900	82.14
2	DATA	337313	974460	779568	1119296	3210638	58890	54.52

BY UNIT

SUBSYSTEM 1 SIGNAL

UNIT	IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI
1	SIGNAL	22339	70987	108417	118601	320343	3900	82.14

SUBSYSTEM 2 DATA

UNIT	IDENT	PRE-DES	DET-DES	CODE-UT	INT-TST	TOTAL	DEMI	\$/DEMI

Table 8-20. CNI Software (Signal Processor)

LAWRENCE DEIGHT
(213) 535-0863

PRICE SOFTWARE PARAMETRIC INFORMATION		
I. SOFTWARE INPUT DATA		
1. PROGRAM NAME MFBARS	2. APPLICATION COMMAND, NAVIGATION, IDENTIFICATION	
II. DESCRIPTION		
3. PROGRAM/USE (Describe) SIGNAL PROCESSING		
4. PURPOSE/MISSION/ENVIRONMENT PROCESS CNI I/O - AIR CRAFT		
5. TYPE MACHINE UTILIZED/WORD LENGTH 16 BITS/WORD	6. NO. MACHINE LANGUAGE INSTRUCTIONS (If known) 3900	
7. TYPE EXECUTABLE INSTRUCTIONS BY WORD LENGTH		
8. TOTAL INSTRUCTIONS REQUIRING 16 BIT WORD 100%	9. TOTAL INSTRUCTIONS REQUIRING 24 BIT WORD	
10. TOTAL INSTRUCTIONS REQUIRING 32 BIT WORD	11. TOTAL INSTRUCTIONS REQUIRING 36 BIT WORD	
12. TOTAL INSTRUCTIONS REQUIRING 48 BIT WORD	13. TOTAL INSTRUCTIONS REQUIRING ___ BIT WORD	
TOTAL NO. WORDS REQUIRED FOR ENTIRE PROGRAM 8000		
III. MIX		
A. PERCENTAGE OF TOTAL MACHINE INSTRUCTIONS BY APPLICATION		
B. MATHEMATICAL APPLICATIONS 40%	B.(1) FRACTION REQUIRING NEW DESIGN 100%	B.(2) FRACTION REQUIRING NEW CODING 100%
C. STRING MANIPULATION 5%	C.(1) FRACTION REQUIRING NEW DESIGN 100%	C.(2) FRACTION REQUIRING NEW CODING 100%
D. SYSTEM OPERATIONS 20%	D.(1) FRACTION REQUIRING NEW DESIGN 100%	D.(2) FRACTION REQUIRING NEW CODING 100%
E. DATA STORAGE/RETRIEVAL 20%	E.(1) FRACTION REQUIRING NEW DESIGN 100%	E.(2) FRACTION REQUIRING NEW CODING 100%
F. ON-LINE COMMUNICATIONS 0	F.(1) FRACTION REQUIRING NEW DESIGN	F.(2) FRACTION REQUIRING NEW CODING
G. REAL TIME COMMAND/CONTROL 10%	G.(1) FRACTION REQUIRING NEW DESIGN 100%	G.(2) FRACTION REQUIRING NEW CODING 100%
H. INTERACTIVE OPERATIONS 5%	H.(1) FRACTION REQUIRING NEW DESIGN 100%	H.(2) FRACTION REQUIRING NEW CODING 100%

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Table 8-20. CNI Software (Signal Processor) (Continued)

A. DATA STORAGE DEVICES (Type/No.)		B. ON-LINE COMMUNICATION DEVICES (Type/No.)	
RAM		0	
A.(1) QTY (Total)		B.(1) QTY (Total)	
1		0	
C. REAL-TIME COMMAND AND CONTROL DEVICES (Type/No.)		D. INTERACTIVE DEVICES (Type/No.)	
CONTROL & DISPLAY		HEADS UP DISPLAY	
C.(1) QTY (Total)		D.(1) QTY (Total)	
1		1	
E. SCHEDULE (Base Year)			
F. START DATE OF DESIGN PHASE		G. END DATE OF DESIGN PHASE	
OCT 1982		OCT 1983	
H. START DATE OF IMPLEMENTATION		I. END DATE OF IMPLEMENTATION	
OCT 1983		MAR 1984	
J. START DATE OF TEST & INTEGRATION		K. END DATE OF TEST & INTEGRATION	
MAR 1984		OCT 1984	
L. GENERAL (Who is doing the work: contractor, Air Force, etc.) (Experience)			
TRW - IMPLEMENTATION SHOULD BE SOMEWHAT MORE DIFFICULT THAN AVERAGE BUT NOT EXCESSIVELY SO. LANGUAGE NOT EASIEST TO WORK WITH, BUT HAVE EXPERIENCED PEOPLE.			
M. ADD-ONS FOR INTEGRATING CONTRACTOR		N. GSA	O. FEE
0		13.05 %	
P. PERCENTAGE OF AVAILABLE HARDWARE SPEED UTILIZED		Q. PERCENTAGE OF AVAILABLE MEMORY CAPACITY UTILIZED	
85 %		83 %	
IV. IBM HIPO INFORMATION ¹			
R. NO. IBM HIPO FUNCTIONAL MODULES ¹		S. AVE HIPO LEVEL ¹	
T. NO. HIPO FUNCTIONAL MODULES/LEVEL ¹		U. HIGHER LEVELS (Level/s Funct Modules)	
LEVEL 0 = LEVEL 1 = LEVEL 2 = LEVEL 3 =		LEVEL 4 = LEVEL 5 = LEVEL 6 = HIGHER LEVELS (Level/s Funct Modules)	

¹ See IBM Publication GC30-1851-1

Table 8-20. CNI Software (Signal Processor) (Continued)

PRICE SOFTWARE PARAMETRIC INFORMATION		LAURENCE VERN (213) 585-0863
I. SOFTWARE INPUT DATA		
1. PROGRAM NAME MFBARS	2. APPLICATION COMMAND, NAVIGATION, IDENTIFICATION	
II. DESCRIPTION		
3. PROGRAM/USE (Describe) INTEGRATE MFBARS WITH INERTIAL NAVIGATION SYSTEM		
4. PURPOSE/MISSION/ENVIRONMENT AIDING OF GPS WITH INS DATA, IMPROVED NAVIGATION SYSTEM PERFORMANCE IN JAMMING ENVIRONMENT - AIRCRAFT		
5. TYPE MACHINE UTILIZED/WORD LENGTH 16 BIT/WORD - DOUBLE PRECISION, 32 BIT/WORD - SINGLE PRECISION	6. NO. MACHINE LANGUAGE INSTRUCTIONS (if known) 58,890	
7. TYPE EXECUTABLE INSTRUCTIONS BY WORD LENGTH		
8. TOTAL INSTRUCTIONS REQUIRING 16 BIT WORD 60 %	9. TOTAL INSTRUCTIONS REQUIRING 24 BIT WORD	
10. TOTAL INSTRUCTIONS REQUIRING 32 BIT WORD 40 %	11. TOTAL INSTRUCTIONS REQUIRING 36 BIT WORD	
12. TOTAL INSTRUCTIONS REQUIRING 64 BIT WORD	13. TOTAL INSTRUCTIONS REQUIRING ___ BIT WORD	
TOTAL NO. WORDS REQUIRED FOR ENTIRE PROGRAM 60,400		
III. MIX		
4. PERCENTAGE OF TOTAL MACHINE INSTRUCTIONS BY APPLICATION		
5. MATHEMATICAL APPLICATIONS 70 %	6.(1) FRACTION REQUIRING NEW DESIGN 100 %	6.(2) FRACTION REQUIRING NEW CODING 100 %
7. STRING MANIPULATION 0	8.(1) FRACTION REQUIRING NEW DESIGN	8.(2) FRACTION REQUIRING NEW CODING
9. SYSTEM OPERATIONS 15 %	9.(1) FRACTION REQUIRING NEW DESIGN 100 %	9.(2) FRACTION REQUIRING NEW CODING 100 %
10. DATA STORAGE/RETRIEVAL 10 %	10.(1) FRACTION REQUIRING NEW DESIGN 100 %	10.(2) FRACTION REQUIRING NEW CODING 100 %
11. ON-LINE COMMUNICATIONS 0	11.(1) FRACTION REQUIRING NEW DESIGN	11.(2) FRACTION REQUIRING NEW CODING
12. REAL TIME COMMAND/CONTROL 5 %	12.(1) FRACTION REQUIRING NEW DESIGN 100 %	12.(2) FRACTION REQUIRING NEW CODING 100 %
13. INTERACTIVE	13.(1) FRACTION REQUIRING NEW DESIGN	13.(2) FRACTION REQUIRING NEW CODING

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Table 8-20. CNI Software (Signal Processor) (Continued)

A. DATA STORAGE DEVICES (Type/No.)		B. ON-LINE COMMUNICATION DEVICES (Type/No.)	
RAM 64K X 16		0	
A.(1) QTY (Total)		B.(1) QTY (Total)	
2		0	
C. REAL-TIME COMMAND AND CONTROL DEVICES (Type/No.)		D. INTERACTIVE DEVICES (Type/No.)	
0		0	
C.(1) QTY (Total)		D.(1) QTY (Total)	
0		0	
E. SCHEDULE (Base Year)			
F. START DATE OF DESIGN PHASE		G. END DATE OF DESIGN PHASE	
OCT 1982		OCT 1983	
H. START DATE OF IMPLEMENTATION		I. END DATE OF IMPLEMENTATION	
OCT 1983		MAR 1984	
J. START DATE OF TEST & INTEGRATION		K. END DATE OF TEST & INTEGRATION	
MAR 1984		OCT 1984	
L. GENERAL (Who is doing the work: contractor, Air Force, etc.) (Experience)			
TRW - EXPERIENCED PERSONNEL			
M. ADD-ONS FOR INTEGRATING CONTRACTOR		N. GSA	O. FEE
P. PERCENTAGE OF AVAILABLE HARDWARE SPEED UTILIZED		Q. PERCENTAGE OF AVAILABLE MEMORY CAPACITY UTILIZED	
85%		83%	
IV. IBM HIPO INFORMATION ¹			
R. NO. IBM HIPO FUNCTIONAL MODULES ¹		S. AVE HIPO LEVEL ¹	
T. NO. HIPO FUNCTIONAL MODULES/LEVEL ¹		U. HIGHER LEVELS (Level/s Functional Modules)	
LEVEL 0 = LEVEL 1 = LEVEL 2 = LEVEL 3 =		LEVEL 4 = LEVEL 5 = LEVEL 6 = HIGHER LEVELS (Level/s Functional Modules)	
¹ See IBM Publication CC20-1851-1			

Table 8-21. PRICE Hardware Data Sheets

PARAMETRIC INFORMATION IMPORTANT: READ INSTRUCTIONS CAREFULLY		TITLE	
		PHONE	DATE
2. SYSTEM NAME & CONTRACTOR MFBARS-TRW	3a. UNIT NAME & SOURCE L-BAND PWR AMP	☒ MANUFACTURED ☐ PURCHASED ITEM: ☐ OFF THE SHELF ☐ CUSTOM MADE ☐ GFE	3b. IF PURCHASED: CURRENT UNIT COST \$ SUPPLIER NAME
4a. PHYSICAL DESCRIPTION 1/2 ATR LONG CONTAINING PC CARDS, PWR AMPLIFIER, PWR SUPPLY, COOLING FAN, MLB MOTHERBOARD			
OTHER APPLICATIONS OF THIS UNIT NONE			
4b. FUNCTIONAL DESCRIPTION TAKE ANALOG/DIGITAL SIGNALS, MODULATE & UP-CONVERT TO L-BAND, PROCESS, AMPLIFY AND TRANSMIT TO ANTENNA.			
5a. MILITARY SPECIFICATION REQUIRED ☒ YES ☐ NO	5b. NUCLEAR HARDENED ☐ YES ☒ NO	5c. WORK BREAKDOWN STRUCTURE	6. TOTAL NO. OF UNITS 1010 NO. OF UNIT/SYS 1
7a. OTHER UNITS INTERFACING WITH THIS UNIT DIAS, AK PWR, TERMINAL, ANTENNA	7b. ELECTRICAL INTERFACES ☐ POWER FURNISHED ☒ POWER & SIGNAL ☐ ADJUSTMENT OR TUNING	7c. MECHANICAL INTERFACES ☐ ONE SURFACE MATING ☒ MORE THAN ONE SURFACE ☐ SHIMMING, MACHINING	
8. TOTAL UNIT WEIGHT (LBS) 26	9. MECHANICAL & STRUCTURAL WEIGHT (LBS) 5	10. VOLUME AND DIMENSIONS VOLUME 727.35 (IN ³) DIMENSIONS 2.88 X 2.62 X 19.56	
11a. ELECTRONIC PACKING DENSITY ☒ TYPICAL ☐ LOW ☐ HIGH	12. NO. OF DISCRETE ELECTRONIC PARTS R/C _____ RAM/PROM _____ SS _____ HYBRID _____ IC _____ OTHER 2-VLS	13. AVERAGE DISSIPATED PWR FROM ELECTRONICS (WATTS) 200	
11b. PERCENT ELECTRONIC VOLUME 50	14a. NO. OF CARDS AND SIZE 3-1 TRK X 4.5 IN X 7.25 L	14b. NO. OF ICS/CATALOG OR CUSTOM MADE SMALL SCALE MEDIUM SCALE LARGE SCALE	
15. DIGITAL/ANALOG ANALOG	16. TYPE OF DISPLAY OR HEADOUT N/A	17. MATERIAL USED IN STRUCTURE ALUMINUM	18. METHOD OF COOLING FAN
19a. DISCRETE ELECTRONIC MODULES (TW, CRT, P.S., ETC.) AND WEIGHT & VOLUME OF EACH PWR AMP: 6.5 LBS, 290 IN³ PWR SUPPLY: 10 LBS, 242 IN³		19b. DISCRETE MECHANICAL MODULES (GYROS, MOTORS, FANS, BATTERIES, ANTENNAS, ETC.) AND WT & VOL OF EACH FAN	
19c. TOTAL WEIGHT, VOLUME, & COST PWR AMP		20. TOTAL UNIT WEIGHT, VOLUME, & COST WT 6.5 VOL 290 IN³ COST 3,500	

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Table 8-21. PRICE Hardware Data Sheets (Continued)

21a. COMPLEXITY OF ENGINEERING EFFORT			REMARKS
	MODIFICATION	NEW	ADVANCE IN ART
SIMPLE	☐	☐	☐
ROUTINE	☐	☐	☐
DIFFICULT	☐	☐	☒
COMPLEX	☐	☐	☐
21b. LEVEL OF NEW MECHANICAL DESIGN			21c. LEVEL OF NEW ELECTRONIC DESIGN
SEE INSTRUCTION: NEW DESIGN <u>80</u> SAME AS EXISTING DESIGN <u>20</u>			SEE INSTRUCTION: NEW DESIGN <u>180</u> SAME AS EXISTING DESIGN <u>0</u>
22a. NO. OF PROTOTYPES (Non-deliverable)	22b. NO. OF RDT&E UNITS (Deliverable)	22c. NO. OF PRODUCTION UNITS	
<u>4</u>	<u>10</u>	<u>1000</u>	
23. LEARNING CURVE SLOPE (Note unit or cum average)			
<u>85</u>			
24. LIST DCAA APPROVED RATES			
a. MATERIAL HANDLING	b. GENERAL AND ADMINISTRATIVE	c. PROFIT	
<u>7.6 %</u>	<u>13.05 %</u>	<u>8.2 %</u>	
SCHEDULE		DATE	
25. MONTH AND YEAR OF START OF ENGINEERING EFFORT		<u>OCT 1982</u>	
26. MONTH AND YEAR OF COMPLETION OF 1ST PROTOTYPE (Non-deliverable)		<u>OCT 1984</u>	
27. MONTH AND YEAR OF COMPLETION OF LAST PROTOTYPE (Non-deliverable)		<u>—</u>	
28. MONTH AND YEAR OF COMPLETION OF 1ST RDT&E UNIT (Deliverable)		<u>MAR 1985</u>	
29. MONTH AND YEAR OF COMPLETION OF LAST RDT&E UNIT (Deliverable)		<u>OCT 1985</u>	
30. MONTH AND YEAR OF START OF PRODUCTION		<u>OCT 1986</u>	
31. MONTH AND YEAR OF COMPLETION OF LAST PRODUCTION UNIT		<u>MAR 1988</u>	
32. REMARKS			
<u>ONE YEAR BETWEEN ITEM 29/30 FOR CUSTOMER EVALUATION.</u>			
<u>F 2089</u>			

Table 8-21. PRICE Hardware Data Sheets (Continued)

PARAMETRIC INFORMATION IMPORTANT: READ INSTRUCTIONS CAREFULLY		TITLE	
		PHONE	DATE
2. SYSTEM NAME & CONTRACTOR MFBARS - TRW	7a. UNIT NAME & SOURCE VHF/UHF POWER AMP	☒ MANUFACTURED ☐ OFF THE SHELF ☐ CUSTOM MADE ☐ CFE	3b. IF PURCHASED: CURRENT UNIT COST \$ SUPPLIER NAME
4a. PHYSICAL DESCRIPTION 1/2 ATR LONG CONTAINING PC CARDS, POWER AMPLIFIER, POWER SUPPLY, COOLING FAN, MLB MOTHER BOARD			
OTHER APPLICATIONS OF THIS UNIT NONE			
4b. FUNCTIONAL DESCRIPTION TAKE ANALOG/ DIGITAL SIGNALS, MODULATE & UP- CONVERT TO VHF/UHF BAND, PROCESS, AMPLIFY AND TRANSMIT TO ANTENNA			
5a. MILITARY SPECIFICATION REQUIRED ☒ YES ☐ NO	5b. NUCLEAR HARDENED ☐ YES ☒ NO	5c. WORK BREAKDOWN STRUCTURE	6. TOTAL NO. OF UNITS 1010 NO. OF UNIT/SYS 1
7a. OTHER UNITS INTERFACING WITH THIS UNIT DIAS, A/C PWR, ANTENNA, TERMINAL	7b. ELECTRICAL INTERFACES ☐ POWER FURNISHED ☒ POWER & SIGNAL ☐ ADJUSTMENT OR TUNING	7c. MECHANICAL INTERFACES ☐ ONE SURFACE MATING ☒ MORE THAN ONE SURFACE ☐ SHIMMING, MACHINING	
8. TOTAL UNIT WEIGHT (LBS) 26	9. MECHANICAL & STRUCTURAL WEIGHT (LBS) 5	10. VOLUME AND DIMENSIONS VOLUME 727.35 (IN ³) DIMENSIONS 4.88W X 7.62H X 9.56L	
11a. ELECTRONIC PACKING DENSITY ☒ TYPICAL ☐ LOW ☐ HIGH	12. NO. OF DISCRETE ELECTRONIC PARTS R/C _____ RAM/PROM _____ SS _____ HYBRID _____ IC _____ OTHER 2-VLSI	13. AVERAGE DISSIPATED PWR FROM ELECTRONICS (WATTS) 150	
11b. PERCENT ELECTRONIC VOLUME 50	14a. NO. OF CARDS AND SIZE 7-1.7" H X 4.5" W X 7.25" L	14b. NO. OF ICs: CATALOG OR CUSTOM MADE? SMALL SCALE _____ MEDIUM SCALE _____ LARGE SCALE _____	
15. DIGITAL/ANALOG ANALOG	16. TYPE OF DISPLAY OR HEADOUT N/A	17. MATERIAL USED IN STRUCTURE ALUMINUM	18. METHOD OF COOLING FAN
19a. DISCRETE ELECTRONIC MODULES (CRT, P.S., ETC.) AND WEIGHT & VOLUME OF EACH PWR AMP: 6 LBS, 242.4 IN³ PWR SUPPLY: 10 LBS, 242.4 IN³		19b. DISCRETE MECHANICAL MODULES (GYROS, MOTORS, FANS, BATTERIES, ANTENNAS, ETC.) AND WT & VOL OF EACH FAN	
GIVE WT, VOL, & COST N/A		GIVE WT, VOL, & COST WT _____ VOL _____ COST _____	

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Table 8-21. PRICE Hardware Data Sheets (Continued)

21a. COMPLEXITY OF ENGINEERING EFFORT				REMARKS
	MODIFICATION	NEW	ADVANCE IN ART	
SIMPLE	☐	☐	☐	
ROUTINE	☐	☐	☐	
DIFFICULT	☐	☐	☒	
COMPLEX	☐	☐	☐	
21b. LEVEL OF NEW MECHANICAL DESIGN				21c. LEVEL OF NEW ELECTRONIC DESIGN
80 SEE INSTRUCTION! 20 NEW DESIGN _____% SAME AS EXISTING DESIGN _____%				100 SEE INSTRUCTION! NEW DESIGN _____% SAME AS EXISTING DESIGN _____%
22a. NO. OF PROTOTYPES (Non-deliverable)		22b. NO. OF ROT&E UNITS (Deliverable)		22c. NO. OF PRODUCTION UNITS
4		10		1000
23. LEARNING CURVE SLOPE (Note unit or full average)				
.85				
24. LIST DCAA APPROVED RATES				
a. MATERIAL HANDLING		b. GENERAL AND ADMINISTRATIVE		c. PROFIT
7.6 %		13.05 %		8.2 %
SCHEDULE				DATE
25. MONTH AND YEAR OF START OF ENGINEERING EFFORT				OCT 1982
26. MONTH AND YEAR OF COMPLETION OF 1ST PROTOTYPE (Non-deliverable)				OCT 1984
27. MONTH AND YEAR OF COMPLETION OF LAST PROTOTYPE (Non-deliverable)				—
28. MONTH AND YEAR OF COMPLETION OF 1ST ROT&E UNIT (Deliverable)				MAR 1985
29. MONTH AND YEAR OF COMPLETION OF LAST ROT&E UNIT (Deliverable)				OCT 1985
30. MONTH AND YEAR OF START OF PRODUCTION				OCT 1986
31. MONTH AND YEAR OF COMPLETION OF LAST PRODUCTION UNIT				MAR 1987
32. REMARKS				
ONE YR BETWEEN 29/30 FOR CUSTOMER EVALUATION				

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Table 8-21. PRICE Hardware Data Sheets (Continued)

PARAMETRIC INFORMATION IMPORTANT: READ INSTRUCTIONS CAREFULLY		TITLE	
		PHONE	DATE
2. SYSTEM NAME & CONTRACTOR MFARS - TRW	3a. UNIT NAME & SOURCE CUI TERMINAL ☒ MANUFACTURED ☐ PURCHASED ITEM: ☐ OFF THE SHELF ☐ CUSTOM MADE ☐ CFE	3b. IF PURCHASED: CURRENT UNIT COST \$ SUPPLIER NAME	
4a. PHYSICAL DESCRIPTION 1- ATR LONG CONTAINING PC CARDS, POWER SUPPLY, COOLING FAN, MLB MOTHERBOARD			
OTHER APPLICATIONS OF THIS UNIT NONE			
4b. FUNCTIONAL DESCRIPTION RECEIVE SIGNALS FROM ANTENNA, DOWN-CONVERT, AMPLIFY, DEMOD, DETECT, DIGITIZE, PROCESS AND TRANSMIT TO DIAS.			
5a. MILITARY SPECIFICATION REQUIRED ☒ YES ☐ NO	5b. NUCLEAR HARDENED ☐ YES ☒ NO	5c. WORK BREAKDOWN STRUCTURE	6. TOTAL NO. OF UNITS 1010 NO. OF UNIT/SYS 1
7a. OTHER UNITS INTERFACING WITH THIS UNIT DIAS, AIC PWR, ANTENNA	7b. ELECTRICAL INTERFACES ☐ POWER FURNISHED ☒ POWER & SIGNAL ☐ ADJUSTMENT OR TUNING	7c. MECHANICAL INTERFACES ☐ ONE SURFACE MATING ☒ MORE THAN ONE SURFACE ☐ SHIMMING, MACHINING	
8. TOTAL UNIT WEIGHT (LBS) 45	9. MECHANICAL & STRUCTURAL WEIGHT (LBS) 10	10. VOLUME AND DIMENSIONS VOLUME 1508.36 (IN ³) DIMENSIONS 10.12 W X 7.62 H X 19.58 L	
11a. ELECTRONIC PACKING DENSITY ☒ TYPICAL ☐ LOW ☐ HIGH	12. NO. OF DISCRETE ELECTRONIC PARTS R/C _____ RAM/PROM _____ SS _____ HYBRID _____ IC _____ OTHER 2-VLSI	13. AVERAGE DISSIPATED PWR FROM ELECTRONICS (WATTS) 150	
11b. PERCENT ELECTRONIC VOLUME 50	14a. NO. OF CARDS AND SIZE 21- 1" THK X 4.5" W X 7.25" L 16- 1/2" THK X 4.5" W X 7.25" L	14b. NO. OF ICs/CATALOG OR CUSTOM MADE? SMALL SCALE MEDIUM SCALE LARGE SCALE	
15. DIGITAL/ANALOG ANALOG / DIGITAL	16. TYPE OF DISPLAY OR HEADOUT N/A	17. MATERIAL USED IN STRUCTURE ALUMINUM	18. METHOD OF COOLING FAN
19a. DISCRETE ELECTRONIC MODULES (WT, CRT, P.S., ETC.) AND WEIGHT & VOLUME OF EACH PWR SUPPLY: 12 LBS, 377 IN³		19b. DISCRETE MECHANICAL MODULES (GYROS, MOTORS, FANS, BATTERIES, ANTENNAS, ETC.) AND WT & VOL OF EACH FAN	
GIVE WT, VOL, & COST		WT _____ VOL _____ COST _____	

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Table 8-21. PRICE Hardware Data Sheets (Continued)

21a. COMPLEXITY OF ENGINEERING EFFORT			REMARKS
	MODIFICATION	NEW	ADVANCE IN ART
SIMPLE	☐	☐	☐
ROUTINE	☐	☐	☐
DIFFICULT	☐	☐	☐
COMPLEX	☐	☐	☒
21b. LEVEL OF NEW MECHANICAL DESIGN			21c. LEVEL OF NEW ELECTRONIC DESIGN
SEE INSTRUCTION! NEW DESIGN <u>80</u> % SAME AS EXISTING DESIGN <u>20</u> %			SEE INSTRUCTION! NEW DESIGN <u>100</u> % SAME AS EXISTING DESIGN <u>0</u> %
22a. NO. OF PROTOTYPES (Non-deliverable)	22b. NO. OF RDT&E UNITS (Deliverable)	22c. NO. OF PRODUCTION UNITS	
4	10	1000	
23. LEARNING CURVE SLOPE (Note unit or sum average)			
85			
24. LIST DCAA APPROVED RATES			
a. MATERIAL HANDLING	b. GENERAL AND ADMINISTRATIVE	c. PROFIT	
7.6 %	13.05 %	8.2 %	
SCHEDULE		DATE	
25. MONTH AND YEAR OF START OF ENGINEERING EFFORT		OCT 1982	
26. MONTH AND YEAR OF COMPLETION OF 1ST PROTOTYPE (Non-deliverable)		OCT 1984	
27. MONTH AND YEAR OF COMPLETION OF LAST PROTOTYPE (Non-deliverable)		—	
28. MONTH AND YEAR OF COMPLETION OF 1ST RDT&E UNIT (Deliverable)		MAR 1985	
29. MONTH AND YEAR OF COMPLETION OF LAST RDT&E UNIT (Deliverable)		OCT 1985	
30. MONTH AND YEAR OF START OF PRODUCTION		OCT 1986	
31. MONTH AND YEAR OF COMPLETION OF LAST PRODUCTION UNIT		MAR 1988	
32. REMARKS			
ONE YEAR BETWEEN ITEM 29/30 FOR CUSTOMER EVALUATION			
F 2089			

Table 8-22. PRICE Software Costs

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----- PRICE SOFTWARE MODEL -----
DATE 24-AUG-79    TIME 09:14

MEBARS1: COMPACT E                SIGNAL PROCESSING

                                INPUT DATA
FILENAME: EMBEE                DATED: 20 AUG 79

DESCRIPTORS
INSTRUCTIONS 3900      APPLICATION  0.000      RESOURCE  2.700
FUNCTIONS     0        STRUCTURE    0.000      LEVEL      0.000
                                           INTEGRATION  0.500

APPLICATION CATEGORIES
NEW DEVELOPMENT  SYSTEM CONFIGURATION
  DESIGN  CODE  TYPE  QUANTITY
DATA PRG  0.20  1.00  1.00  1
ONLINE COM  0.00  1.00  1.00  0
REALTIME COC  0.10  1.00  1.00  0
INTERACTIVE  0.05  1.00  1.00  0
MATHEMATICAL  0.40  1.00  1.00  ***
STRING MANIP  0.05  1.00  1.00  ***
OPR SYSTEMS  0.20  1.00  1.00  ***

SCHEDULE
COMPLEXITY  1.100
DESIGN START OCT 82    IMPL START  0 00    T&I START  0 00
DESIGN END   0        IMPL END    0 00    T&I END    0 00

SUPPLEMENTAL INFORMATION
YEAR 1982    EDUCATION  1.000    TECH INF  1.00
MULTIPLIER  1.290    PLATFORM  1.2    UTILIZATION  0.85

----- PROGRAM COSTS -----
COST ELEMENTS      DESIGN  IMPL  T & I  TOTAL
SYSTEMS ENGINEERING  37.  5.  68.  110.
PROGRAMMING  13.  16.  27.  56.
CONFIGURATION CONTROL  12.  4.  36.  52.
DOCUMENTATION  11.  1.  18.  30.
PROGRAM MANAGEMENT  7.  1.  7.  15.
TOTAL  121.  25.  150.  296.

----- ADDITIONAL DATA -----
DESCRIPTORS
INSTRUCTIONS 3900      APPLICATION  4.867      RESOURCE  2.700
FUNCTIONS 43          STRUCTURE    0.000      LEVEL      0.000

SCHEDULE
COMPLEXITY  1.100
DESIGN START OCT 82    IMPL START  DEC 82    T&I START  JAN 83
DESIGN END   FEB 83    IMPL END    APR 83    T&I END    MAY 83

----- SCHEDULE GRAPH -----
OCT 82
***** DESIGN *****
***** IMPLEMENT *****
***** TEST & INTEGRATE *****
  
```

Table 8-22. PRICE Software Costs (Continued)

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--- PRICE SOFTWARE MODEL ---

DATE 24-AUG-79    TIME 09:16

MEMBER: COMPANY B      COMMAND BAY IDENTIFICATION

INPUT DATA
FILENAME: EMPER      DATED: 20 AUG 79

DESCRIPTOR
INSTRUCTIONS 58880    APPLICATION 0.000    RESOURCE 2.700
FUNCTIONS 0          STRUCTURE 0.000    LEVEL 0.000
                                INTEGRATION 0.600

APPLICATION CATEGORIES
MIS          DESIGN  CODE  TYPE  QUANTITY
DATA B R     0.10    1.00  1.00  1          2
ONLINE COMM  0.00    1.00  1.00  0          0
REALTIME C&C 0.05    1.00  1.00  0          0
INTERACTIVE  0.00    1.00  1.00  0          0
MATHEMATICAL 0.70    1.00  1.00  ***        ***
STRING MANIP  0.00    1.00  1.00  ***        ***
OPR SYSTEMS  0.15    1.00  1.00  ***        ***

SCHEDULE
COMPLEXITY 1.100
DESIGN START OCT 82    IMPL START 0          T&I START 0
DESIGN END 0          IMPL END 0          T&I END 0

SUPPLEMENTAL INFORMATION
YEAR 1982    EDUCATION 1.000    TECH IMP 1.00
MULTIPLIER 1.290    PLATFORM 1.8    UTILIZATION 0.85

PROGRAM COSTS
COST ELEMENTS      DESIGN      IMPL      T & I      TOTAL
SYSTEM ENGINEERING  663.        26.        583.      1268.
PROGRAMMING        114.        137.       238.       490.
CONFIGURATION CONTROL 143.        46.        430.       618.
DOCUMENTATION      134.        16.        206.       355.
PROGRAM MANAGEMENT  89.         15.        94.       198.
TOTAL             1132.       241.      1550.     2923.

ADDITIONAL DATA
DESCRIPTOR
INSTRUCTIONS 58880    APPLICATION 3.022    RESOURCE 2.700
FUNCTIONS 654        STRUCTURE 0.000    LEVEL 0.000

SCHEDULE
COMPLEXITY 1.100
DESIGN START OCT 82    IMPL START FEB 83    T&I START JUN 83
DESIGN END AUG 83    IMPL END JAG 84    T&I END OCT 84

SCHEDULE GRAPH
OCT 82          OCT 84
***** DESIGN *****
***** IMPLEMENT *****
***** TEST & INTEGRATE *****

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Table 8-22. PRICE Software Costs (Continued)

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--- PRICE SOFTWARE MODEL ---
SYSTEM INTEGRATION
DATE 23-806-78    TIME 09:18

OPERATOR: COMMANDER                                INTEGRATION AND TEST
FILENAME: PRICE                                INPUT DATA                                DATED: 20 806 7

SCHEDULE
COMPLETION      1.000
DESIGN START    OCT 82
DESIGN END      0
IMPL START      0
IMPL END        0
T&I START      0
T&I END        OCT 82

SUPPLEMENTAL INFORMATION
YEAR      1982
MULTIPLIER 1.290
EDUCATION 1.000
PLATFORM  1.8
TECH IMP  1.0
UTILIZATION 0.8

PROGRAM COSTS
COST ELEMENTS      DESIGN      IMPL      T & I      TOTAL
SYSTEM ENGINEERING  108.        4.        81.        193.
PROGRAMMING         22.        23.        26.        71.
CONFIGURATION CONTROL 15.        6.        52.        73.
DOCUMENTATION       15.        21.        23.        60.
PROGRAM MANAGEMENT  12.        2.        10.        24.
TOTAL              168.        56.        212.        436.

ADDITIONAL DATA

SCHEDULE
COMPLETION      1.000
DESIGN START    OCT 82
DESIGN END      0
IMPL START      0
IMPL END        0
T&I START      0
T&I END        OCT 82

SUMMARY OF SOFTWARE DEVELOPMENT TOTALS

PROGRAM COSTS
COST ELEMENTS      DESIGN      IMPL      T & I      TOTAL
SYSTEM ENGINEERING  832.        34.        737.        1603.
PROGRAMMING         149.        178.        302.        629.
CONFIGURATION CONTROL 170.        56.        517.        743.
DOCUMENTATION       159.        20.        243.        422.
PROGRAM MANAGEMENT  108.        18.        111.        237.
TOTAL              1420.        303.        1911.        3634.

```

Table 8-23. PRICE Hardware Acquisition Costs

0341C-PH00 POWER AMP

INPUT DATA PRICE 83E 24-H006-09 10:05 1 7
 QTY 0. PROTOT 3.0 QTY 26.000 SOL 0.420 CODE 1
 QTY 1. INTEGE 0.500 INTEGE 0.500 AMOCTD 129.000 AMOCTF 129.000

MECH DIRECT
 ME 5.000 MEPCD 5.520 PRODC 0.000 MEKIT 0.500 DEIFF 2.000

ELECTRONIC
 MEPCD 0.420 MEPCD 8.125 PRODC 0.000 MEKIT 0.500 DEIFF 2.000
 ME 200.000 MEKIT 0.000 MEKIT 0.000 MEKIT 0.000 MEKIT 0.000

ENGINEERING
 EMKIT 10.0 EMKIT 0.0 EMKIT 0.0 EMKIT 1.200 PRMF 0.250

GENERAL
 YEAR 1982. EDC 100.000 PRODC 1.000 DATA 1.000 TOGTC 1.000
 CTEN 1.200 CTEN 1.000 PRMF 1.000 DATA 1.000 PRMF 1.000

PROGRAM COST	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	237.	0.	237.
DESIGN	360.	0.	360.
PLATE	148.	0.	148.
PROG. MNT	140.	0.	140.
DATA	52.	0.	52.
TOTAL ENGINEERING	1441.	0.	1441.

MANUFACTURING	DEVELOPMENT	PRODUCTION	TOTAL COST
PRODUCTION	0.	0.	0.
PROTOTYPE	309.	0.	309.
TOOL-TEST EO	36.	0.	36.
TOTAL MANUFACTURING	425.	0.	425.
TOTAL COST	1866.	0.	1866.

ACOST 0.000 0.000 TOTAL BY PROD COST 0.000
 ME 26.000 SOL 0.420 EDC 0.000 MEKIT 0.500 DEIFF 0.000
 ME 0.000 0.000 EDC 0.000 MEKIT 0.500 DEIFF 0.000

MECH DIRECT
 ME 5.000 MEPCD 11.900 MEKIT 0.000 PRODC 4.159 MEPCD 5.520
 ELECTRONIC
 ME 21.000 MEPCD 51.920 MEKIT 0.000 PRODC 4.333 MEPCD 8.125
 ME 200.000 MEKIT 2617.000 MEKIT 0.000 MEKIT 0.000 MEKIT 0.000

SCHEDULES
 EMKIT 10.000 EMKIT 15.145 EMKIT 21.755 EDC 1.200 PRMF 0.250
 COST RANGES DEVELOPMENT PRODUCTION TOTAL COST
 FROM 1652. 0. 1652.
 CENTER 1866. 0. 1866.
 TO 2178. 0. 2178.

Table 8-23. PRICE Hardware Acquisition Costs (Continued)

02: CMI TERMINAL

INPUT DATA		PRICE SEE 24-800-09 10404			
MT	0. PROTOT	4.0 MT	45,000.000	0.000 MECE	1.
ATTACH	1. INTEGE	0.500 INTEGE	0.500 AMPLID	100,000.000	ATTACH 100,000.
MECH DIRECT					
MT	10,000.000	0.000	0.000	0.000	0.000
ELECTRONIC					
MT	0.000.000	0.000	0.000	0.000	0.000
MT	100,000.000	0.000	0.000	1.000	0.000
ENGINEERING					
MT	10.000	0.000	0.000	1.000	0.000
GLOPAC					
MT	1000.000	100,000.000	1.000	1.000	1.000
MT	1000.000	1.000	1.000	1.000	1.000
PROGRAM COST		DEVELOPMENT	PRODUCTION	TOTAL COST	
ENGINEERING					
DRAWING		0.000	0.	0.000	
DESIGN		1000.	0.	1000.	
SYSTEM		0.000	0.	0.000	
PROD. DATA		0.000	0.	0.000	
DATA		0.000	0.	0.000	
TOTAL ENGINEERING		2000.	0.	2000.	
MANUFACTURING					
PRODUCTION		0.	0.	0.	
PROTOTYPE		0.000	0.	0.000	
TOOL-TEST EQ		0.000	0.	0.000	
TOTAL MANUFACTURING		0.000	0.	0.000	
TOTAL COST		2000.	0.	2000.	
ACQUIT		0.000	TOTAL AS PROD. COST		0.000
MT	45,000.000	0.000	0.000	0.000	0.000
LOOSE	0.000	0.000	0.000	0.000	0.000
MECH DIRECT					
MT	10,000.000	11,494.000	0.000	4,168.000	5,526.000
ELECTRONIC					
MT	0.000.000	41,051.000	0.000	4,400.000	8,100.000
MT	100,000.000	0.000	0.000	1.000	0.000
ENGINEERING					
MT	10,000.000	16,234.000	22,991.000	1,200.000	0.000
COST RANGE		DEVELOPMENT	PRODUCTION	TOTAL COST	
FROM		0.000	0.	0.000	
CENTER		2000.	0.	2000.	
TO		3492.	0.	3492.	

Table 8-23. PRICE Hardware Acquisition Costs (Continued)

NEARBY COMPANY ESTIMATE OF PRICE									
INPUT DATA									
QTY	0.1	PROTOD	4.0	WT	26.000	QOL	0.420	QDIE	1.0
QTY	1.0	INTER	0.500	INTER	0.500	BRCLD	129.000	BRCLF	129.000
MECH STRUCT									
MC	5.000	MCPLSD	5.520	PRODD	0.000	DEMET	0.500	DECRPD	2.000
ELECTRONICS									
QTY	0.200	MCPLSD	8.125	PRODD	0.000	DEMET	0.500	DECRPD	2.000
MC	150.000	CMRCLD	0.0	CMRCLD	0.000	CMRCLD	0.500	CMRCLD	0.000
ENGINEERING									
EMTAT	10.0	EMTAT	0.0	EMTAT	0.0	EMTAT	1.200	EMTAT	0.250
GLOBAL									
YEAR	1982	EDC	100.000	PRODD	1.000	DATA	1.000	FIGIT	1.000
PLTFM	1.000	PLTFM	1.000	PRODD	1.000	DATA	1.000	FIGIT	1.000
PROGRAM COST									
			DEVELOPMENT		PRODUCTION		TOTAL COST		
ENGINEERING									
DRAFTING			237.		0.		237.		
DESIGN			062.		0.		062.		
SYSTEMS			142.		0.		142.		
PROD MGMT			146.		0.		146.		
DATA			52.		0.		52.		
COSTOTAL ENG			1439.		0.		1439.		
MANUFACTURING									
PRODUCTION			0.		0.		0.		
PROTOTYPE			378.		0.		378.		
TOOL-TEST EQ			146.		0.		146.		
COSTOTAL MFG			424.		0.		424.		
TOTAL COST			1863.		0.		1863.		
PRICE									
PRODD			0.00		TOTAL BY PROD COST		0.00		
WT	26.000	QOL	0.420	ECNE	0.000	DEMET	0.500	DECRPD	0.014
ECORVE	0.000			ECNE	0.000	DEMET	0.500	DECRPD	0.452
MECH STRUCT									
MC	5.000	MCPLSD	11.305	MECID	0.000	PRODD	4.158	MCPLSD	5.520
ELECTRONICS									
MC	21.000	MCPLSD	51.020	CMRCLD	0.000	PRODD	4.320	MCPLSD	8.125
MC	150.000	CMRCLD	1559.			CMRCLD	0.500	CMRCLD	0.225
SCHEDULED									
EMTAT	10.000	EMTAT	15.135	EMTAT	21.284	ECMPLD	1.200	EMTAT	0.250
COST RANGES									
			DEVELOPMENT		PRODUCTION		TOTAL COST		
FROM			1649.		0.		1649.		
CENTER			1863.		0.		1863.		
TO			2174.		0.		2174.		

Table 8-23. PRICE Hardware Acquisition Costs (Continued)

```

DATA IN
INPUT DATA
CITY 0.000000 0.000000 0.000000 0.000000 0.000000 0.000000
CITY 1.000000 0.000000 0.000000 0.000000 0.000000 0.000000
DECH STREET
IMO 0.000000 0.000000 0.000000 0.000000 0.000000 0.000000
ELECTRONIC
I-ROAD 0.000000 0.000000 0.000000 0.000000 0.000000 0.000000
RFE 0.000000 0.000000 0.000000 0.000000 0.000000 0.000000
ENGINEERING
EMTH 0.000000 0.000000 0.000000 0.000000 0.000000 0.000000
GLOBAL
YEAR 1988.000000 100.000000 100.000000 100.000000 100.000000 100.000000
PCTEM 1.000000 1.000000 1.000000 1.000000 1.000000 1.000000

```

REF ID: A66740-0000

PROGRAM COST		DEVELOPMENT		PRODUCTION		TOTAL COST	
ENGINEERING							
DESIGN	127.			0.		127.	
CONTRACT	579.			0.		579.	
PROG. COST	179.			0.		179.	
DATA	135.			0.		135.	
TOTAL DEVELOPMENT	921.			0.		921.	
MANUFACTURING							
PRODUCTION							
PROTOTYPE	0.			0.		0.	
TOOL-TEST ETC	36.			0.		36.	
TOTAL MANUFACTURING	36.			0.		36.	
TOTAL COST	957.			0.		957.	
COST RANGES		DEVELOPMENT		PRODUCTION		TOTAL COST	
FROM							
CENTER	1126.			0.		1126.	
TO	1879.			0.		1879.	
	1394.			0.		1394.	

Table 8-23. PRICE Hardware Acquisition Costs (Continued)

TOTAL COST, LESS INTEGRATION COST		PRODUCTION	TOTAL COST
PROGRAM COST	DEVELOPMENT		
ENGINEERING			333.
DRAWING	3066.	0.	3066.
DESIGN	532.	0.	532.
SYSTEMS	551.	0.	551.
PROD MGMT	197.	0.	197.
DATA	197.	0.	197.
SUBTOTAL ENG	5206.	0.	5206.
MANUFACTURING			0.
PRODUCTION	0.	0.	0.
PROTOTYPE	1367.	0.	1367.
TOOL-TEST EQ	167.	0.	167.
PURCH ITEMS	0.	0.	0.
SUBTOTAL MFG	1534.	0.	1534.
TOTAL COST	6740.	0.	6740.
COST RANGES		PRODUCTION	TOTAL COST
FROM	5206.	0.	5206.
CENTER	6740.	0.	6740.
TO	6740.	0.	6740.
TOTAL COST, WITH INTEGRATION COST		PRODUCTION	TOTAL COST
PROGRAM COST	DEVELOPMENT		
ENGINEERING			966.
DRAWING	3661.	0.	3661.
DESIGN	511.	0.	511.
SYSTEMS	751.	0.	751.
PROD MGMT	273.	0.	273.
DATA	273.	0.	273.
SUBTOTAL ENG	6362.	0.	6362.
MANUFACTURING			0.
PRODUCTION	0.	0.	0.
PROTOTYPE	1463.	0.	1463.
TOOL-TEST EQ	183.	0.	183.
PURCH ITEMS	0.	0.	0.
SUBTOTAL MFG	1645.	0.	1645.
TOTAL COST	8013.	0.	8013.
COST RANGES		PRODUCTION	TOTAL COST
FROM	7101.	0.	7101.
CENTER	8013.	0.	8013.
TO	9339.	0.	9339.

Table 8-24. PRICE Hardware Data Sheet (Harris)

PARAMETRIC INFORMATION IMPORTANT: READ INSTRUCTIONS CAREFULLY		TITLE <i>F.L. Anderson</i> PHONE <i>(305) 727-6771</i> DATE <i>9/19/79</i>	
2. SYSTEM NAME & CONTRACTOR <i>MF3ARS - HARRIS GCSD</i>	3a. UNIT NAME & SOURCE <i>Antenna Control Assy</i>	☒ MANUFACTURED PURCHASED ITEM ☐ OFF THE SHELF CUSTOM MADE ☐ CPE	3b. IF PURCHASED: CURRENT UNIT COST \$ SUPPLIER NAME
4a. PHYSICAL DESCRIPTION <i>Adaptive Antenna Control Electronics Assembly</i>			
OTHER APPLICATIONS OF THIS UNIT • • •			
4b. FUNCTIONAL DESCRIPTION <i>Provides adaptive receive pattern control. Four different communication links serviced, interfaces with L-Band Array Antenna, five (5) UHF Blade Antennas, and a MF3ARS radio receiver. Mounts inside aircraft fuselage</i>			
5a. MILITARY SPECIFICATION REQUIRED ☒ YES <i>Antenna</i> ☐ NO	5b. NUCLEAR HARDENED ☒ YES ☐ NO	5c. WORK BREAKDOWN STRUCTURE <i>N/A</i>	6. <i>Qty</i> TOTAL NO. OF UNITS <i>1210</i> <i>Qty</i> 545 NO. OF UNIT/SYS <i>1</i>
7a. OTHER UNITS INTERFACING WITH THIS UNIT (Electrical) <i>UHF Blade Antenna (5) - Band Array Antenna (1)</i>	7b. ELECTRICAL INTERFACES / INTERFACES ☒ POWER FURNISHED <i>0.5</i> ☐ POWER & SIGNAL ☐ ADJUSTMENT OR TUNING	7c. MECHANICAL INTERFACES / INTERFACES ☒ ONE SURFACE MATING <i>0.3</i> ☐ MORE THAN ONE SURFACE ☐ SWIMMING MACHINING	
8. TOTAL UNIT WEIGHT (LBS) <i>WT</i> <i>17.0</i>	9. MECHANICAL & STRUCTURAL WEIGHT (LBS) <i>WS</i> <i>3.0</i>	10. VOLUME AND DIMENSIONS <i>10L</i> VOLUME <i>750</i> (IN ³) DIMENSIONS <i>6" x 5" x 5"</i>	
11a. ELECTRONIC PACKING DENSITY ☐ TYPICAL ☐ LOW ☒ HIGH	12. NO. OF DISCRETE ELECTRONIC PARTS R/C <i>/</i> RAM/PROM <i>/</i> SS <i>/</i> HYBRID <i>/</i> IC <i>/</i> OTHER <i>/</i>	13. AVERAGE DISSIPATED PWR FROM ELECTRONICS (WATTS) <i>70 watts</i>	
14a. NO. OF CARDS AND SIZE <i>8 PC Cards 6x6</i> <i>37 Pcs</i>	14b. NO. OF ICs: CATALOG OR CUSTOM MADE? SMALL SCALE MEDIUM SCALE <i>90</i> LARGE SCALE <i>56</i> <i>total all cards</i>		
15. DIGITAL/ANALOG <i>25% Analog 75% Digital</i>	16. TYPE OF DISPLAY OR HEADOUT <i>None</i>	17. MATERIAL USED IN STRUCTURE <i>ALCONST</i> <i>Aluminum Casting</i>	18. METHOD OF COOLING <i>Convection</i>
19a. DISCRETE ELECTRONIC MODULES (Wt, CRT, P.S., ETC.) AND WEIGHT & VOLUME OF EACH <i>→ RF Modules 0.1 lbs + RF Antenna 7.5 lbs 0.8 lbs + Power Supply Mch 2.0 lbs 0.25 lbs</i>		19b. DISCRETE MECHANICAL MODULES (GYROS, MCTORS, FANS, BATTERIES, ANTENNAS, ETC.) AND WT & VOL OF EACH <i>None</i>	
TOTAL WT. VOL. COST <i>None</i>		WT _____ VOL _____ COST _____	

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Table 8-24. PRICE Hardware Data Sheet (Harris) (Continued)

21a. COMPLEXITY OF ENGINEERING EFFORT			REMARKS
	MODIFICATION	NEW	ADVANCE IN ART
SIMPLE	☐	☐	☐
ROUTINE	☐	☐	☐
DIFFICULT	☐	☐	☐
COMPLEX	☐	☒	☐
			EM CPLX = 1.7
21b. LEVEL OF NEW MECHANICAL DESIGN		21c. LEVEL OF NEW ELECTRONIC DESIGN	
SEE INSTRUCTION!		SEE INSTRUCTION!	
NEW DESIGN <u>100</u> SAME AS EXISTING DESIGN <u>1</u>		NEW DESIGN <u>100</u> SAME AS EXISTING DESIGN <u>1</u>	
22a. NO. OF PHOTOTYPES (Non-deliverable)	22b. NO. OF RDT&E UNITS (Deliverable)	22c. NO. OF PRODUCTION UNITS	
<u>4</u>	<u>10</u>	<u>1000</u>	
23. LEARNING CURVE SLOPE (Note unit or sub average)			
<u>0.90</u> <u>LEAVE</u>			
24. LIST DCAA APPROVED RATES			
a. MATERIAL HANDLING	b. GENERAL AND ADMINISTRATIVE	c. PROFIT	
SCHEDULE		DATE	
25. MONTH AND YEAR OF START OF ENGINEERING EFFORT		<u>Oct 1982</u>	
26. MONTH AND YEAR OF COMPLETION OF 1ST PROTOTYPE (Non-deliverable)		<u>Oct 1984</u>	
27. MONTH AND YEAR OF COMPLETION OF LAST PROTOTYPE (Non-deliverable)		<u>—</u>	
28. MONTH AND YEAR OF COMPLETION OF 1ST RDT&E UNIT (Deliverable)		<u>Mar 1985</u>	
29. MONTH AND YEAR OF COMPLETION OF LAST RDT&E UNIT (Deliverable)		<u>Oct 1985</u>	
30. MONTH AND YEAR OF START OF PRODUCTION		<u>Oct 1986</u>	
31. MONTH AND YEAR OF COMPLETION OF LAST PRODUCTION UNIT		<u>Mar 1988</u>	
32. REMARKS			
1. MODE 1 INPUT — E/M Item 2. One year BET Item 29 ± 30 for customer evaluation			
F 2089			

Table 8-24. PRICE Hardware Data Sheet (Harris) (Continued)

PARAMETRIC INFORMATION IMPORTANT: READ INSTRUCTIONS CAREFULLY		TITLE <i>F. L. Anderson</i> PHONE <i>(305) 727-6778</i> DATE <i>9/19/79</i>	
2. SYSTEM NAME & CONTRACTOR <i>MFBARS - HARRIS</i> <i>GCSD</i>		3a. UNIT NAME & SOURCE <i>L Band</i> <i>Array</i> <i>Antenna</i> ☐ <i>GPE</i>	
		3b. IF PURCHASED: ☒ MANUFACTURED ☐ OFF THE SHELF ☐ CUSTOM MADE	
		CURRENT UNIT COST \$ SUPPLIER NAME	
4a. PHYSICAL DESCRIPTION <i>7 element, receive only, broad band antenna array</i>			
OTHER APPLICATIONS OF THIS UNIT • • •			
4b. FUNCTIONAL DESCRIPTION <i>Receives L Band Radio Signals. Interfaces with Antenna Control Assembly. Mounts separately to aircraft surface (flush, extending to interior).</i>			
5a. MILITARY SPECIFICATION REQUIRED ☒ YES <i>Antenna</i> ☐ NO		5b. NUCLEAR HARDENED ☒ YES ☐ NO	
		5c. WORK BREAKDOWN STRUCTURE <i>N/A</i>	
		5d. <i>Sup</i> TOTAL NO. OF UNITS <i>1010</i> Qty Sys NO. OF UNIT/SYS <i>1</i>	
7a. OTHER UNITS INTERFACING WITH THIS UNIT <i>Antenna Control Assy</i> <i>(3 electrical)</i>		7b. ELECTRICAL INTERFACES <i>NTES</i> ☒ POWER FURNISHED <i>0.5</i> ☐ POWER & SIGNAL ☐ ADJUSTMENT OR TUNING	
		7c. MECHANICAL INTERFACES <i>NTES</i> ☐ ONE SURFACE MATING ☐ MORE THAN ONE SURFACE ☒ SHIMMING, MACHINING <i>0.7</i>	
8. TOTAL UNIT WEIGHT (LBS) <i>WT</i> <i>2.4</i>		9. MECHANICAL & STRUCTURAL WEIGHT (LBS) <i>WT</i> <i>12.4</i>	
		10. VOLUME AND DIMENSIONS <i>VOL</i> VOLUME <i>400</i> (IN ³) DIMENSIONS <i>20" Dia x 13" high</i>	
11a. ELECTRONIC PACKING DENSITY ☐ TYPICAL ☐ LOW ☐ HIGH		12. NO. OF DISCRETE ELECTRONIC PARTS a. <i>/</i> RAM/PROM <i>/</i> b. <i>/</i> HYBRID <i>/</i> c. <i>/</i> OTHER <i>/</i>	
11b. PERCENT ELECTRONIC VOLUME <i>0</i> <i>USE VOL</i>		13. AVERAGE DISSIPATED PWR FROM ELECTRONICS (WATTS) <i>/</i>	
14a. NO. OF CARDS AND SIZE <i>/</i>		14b. NO. OF ICS/CATALOG OR CUSTOM MADE? SMALL SCALE MEDIUM SCALE LARGE SCALE	
15. DIGITAL/ANALOG <i>/</i>		16. TYPE OF DISPLAY OR HEADOUT <i>/</i>	
		17. MATERIAL USED IN STRUCTURE	
		18. METHOD OF COOLING	
19a. DISCRETE ELECTRONIC MODULES (CRT, P.S., ETC.) AND WEIGHT & VOLUME OF EACH <i>/</i>		19b. DISCRETE MECHANICAL MODULES (GYROS, MOTORS, FANS, BATTERIES, ANTENNAS, ETC.) AND WT & VOL OF EACH <i>/</i>	
(GIVE WT, VOL, & COST)		WT VOL COST	

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Table 8-24. PRICE Hardware Data Sheet (Harris) (Continued)

21a. COMPLEXITY OF ENGINEERING EFFORT			REMARKS
	MODIFICATION	NEW	ADVANCE IN ART
SIMPLE	☐	☐	☐
ROUTINE	☐	☐	☐
DIFFICULT	☐	☐	☐
COMPLEX	☐	☐	☐

21b. LEVEL OF NEW MECHANICAL DESIGN	21c. LEVEL OF NEW ELECTRONIC DESIGN
SEE INSTRUCTION!	SEE INSTRUCTION!
NEW DESIGN <u>100</u>	NEW DESIGN <u>5</u>
SAME AS EXISTING DESIGN <u>5</u>	SAME AS EXISTING DESIGN <u>5</u>

22a. NO. OF PROTOTYPES (Non-deliverable)	22b. NO. OF RDT&E UNITS (Deliverable)	22c. NO. OF PRODUCTION UNITS
<u>4</u> PROTOS	<u>10</u>	<u>1000</u>

23. LEARNING CURVE SLOPE (None unit or sum average)	<u>LCURVE</u>
<u>0.90</u>	

24. LIST DCAA APPROVED RATES		
2. MATERIAL HANDLING	3. GENERAL AND ADMINISTRATIVE	4. PROFIT

SCHEDULE	DATE
25. MONTH AND YEAR OF START OF ENGINEERING EFFORT	<u>Oct 1982</u>
26. MONTH AND YEAR OF COMPLETION OF 1ST PROTOTYPE (Non-deliverable)	<u>Oct 1984</u>
27. MONTH AND YEAR OF COMPLETION OF LAST PROTOTYPE (Non-deliverable)	<u>—</u>
28. MONTH AND YEAR OF COMPLETION OF 1ST RDT&E UNIT (Deliverable)	<u>Mar 1985</u>
29. MONTH AND YEAR OF COMPLETION OF LAST RDT&E UNIT (Deliverable)	<u>Oct 1985</u>
30. MONTH AND YEAR OF START OF PRODUCTION	<u>Oct 1986</u>
31. MONTH AND YEAR OF COMPLETION OF LAST PRODUCTION UNIT	<u>Mar 1988</u>

32. REMARKS
1. Mode 2 Input — suggest PRODS = 5.3 week item MCPLXS = 0 2. One year BET item 29 & 30 for customer evaluation

F 2089

Table 8-24. PRICE Hardware Data Sheet (Harris) (Continued)

PARAMETRIC INFORMATION		TITLE F. L. Anderson	
IMPORTANT: READ INSTRUCTIONS CAREFULLY		PHONE (305) 727-6778 DATE 9/19/79	
2. SYSTEM NAME & CONTRACTOR MFBARS - HARRIS GCSD		7a. UNIT NAME & SOURCE UHF Blade ☐ Antenna ☐ MANUFACTURED PURCHASED ITEM: ☒ OFF THE SHELF ☐ CUSTOM MADE ☐ CPE	
4a. PHYSICAL DESCRIPTION Low Drag Blade Antenna, 225 to 420 MC		5b. IF PURCHASED CURRENT UNIT COST \$ 200 SUPPLIER NAME Multiple Sources, one is Doral and Margolin	
OTHER APPLICATIONS OF THIS UNIT _____ _____ _____			
4b. FUNCTIONAL DESCRIPTION Receive UHF Radio Signals. Interfaces with Antenna control assembly. Mounts separately to aircraft surface.			
5a. MILITARY SPECIFICATION REQUIRED ☒ YES ☐ NO Airborne		5b. NUCLEAR HARDENED ☒ YES ☐ NO	
7a. OTHER UNITS INTERFACING WITH THIS UNIT Antenna Control Assy (Electrical)		7b. MECHANICAL INTERFACES INTERFACES ☒ POWER FURNISHED 0.5 ☐ POWER & SIGNAL ☐ ADJUSTMENT OR TUNING	
8. TOTAL UNIT WEIGHT (LBS) WT 0.8		9. MECHANICAL & STRUCTURAL WEIGHT (LBS) WS 0.8	
11a. ELECTRONIC PACKING DENSITY ☐ TYPICAL ☐ LOW ☐ HIGH		12. NO. OF DISCRETE ELECTRONIC PARTS R/C _____ RAM/ROM _____ SS _____ HYBRID _____ IC _____ OTHER _____	
11b. PERCENT ELECTRONIC VOLUME _____		13. AVERAGE DISSIPATED PWR FOR ELECTRONICS (WATTS)	
14a. NO. OF CARDS AND SIZE		14b. NO. OF ICs CATALOG OR CUSTOM MADE? SMALL SCALE MEDIUM SCALE LARGE SCALE	
15. DIGITAL/ANALOG		16. METHOD OF COOLING	
15. TYPE OF DISPLAY OR HEADOUT		17. MATERIAL USED IN STRUCTURE	
19a. DISCRETE ELECTRONIC MODULES (TWT, CRT, P.S., ETC.) AND WEIGHT & VOLUME OF EACH		19b. DISCRETE MECHANICAL MODULES (GYROS, MOTORS, FANS, BATTERIES, ANTENNAS, ETC.) AND WT & VOL OF EACH	
(GIVE WT, VOL, & COST) WT _____ VOL _____ COST _____			

Table 8-24. PRICE Hardware Data Sheet (Harris) (Continued)

21A. COMPLEXITY OF ENGINEERING EFFORT				REMARKS	
	MODIFICATION	NEW	ADVANCE IN ART		
SIMPLE	☐	☐	—		
ROUTINE	☐	☐	☐		
DIFFICULT	☐	☐	☐		
COMPLEX	☐	☐	☐		
21B. LEVEL OF NEW MECHANICAL DESIGN				21C. LEVEL OF NEW ELECTRONIC DESIGN	
SEE INSTRUCTION!				SEE INSTRUCTION!	
NEW DESIGN _____ SAME AS EXISTING DESIGN _____				NEW DESIGN _____ SAME AS EXISTING DESIGN _____	
22A. NO. OF PROTOTYPES (Non-deliverable)		22B. NO. OF ROT&E UNITS (Deliverable)		22C. NO. OF PRODUCTION UNITS	
20 PROTS		50		5000	
23. LEARNING CURVE SLOPE (Note unit or cum average) L CURVE					
0.95					
24. LIST DCAA APPROVED RATES					
A. MATERIAL HANDLING		1. GENERAL AND ADMINISTRATIVE		C. PROFIT	
SCHEDULE				DATE	
25. MONTH AND YEAR OF START OF ENGINEERING EFFORT				Oct 1982	
26. MONTH AND YEAR OF COMPLETION OF 1ST PROTOTYPE (Non-deliverable)				Oct 1984	
27. MONTH AND YEAR OF COMPLETION OF LAST PROTOTYPE (Non-deliverable)				—	
28. MONTH AND YEAR OF COMPLETION OF 1ST ROT&E UNIT (Deliverable)				Mar 1985	
29. MONTH AND YEAR OF COMPLETION OF LAST ROT&E UNIT (Deliverable)				Oct 1985	
30. MONTH AND YEAR OF START OF PRODUCTION				Oct 1986	
31. MONTH AND YEAR OF COMPLETION OF LAST PRODUCTION UNIT				Mar 1988	
32. REMARKS					
1. MODE 3 INPUT - Purchased Item 2. One year BET Item 29 & 30 for customer evaluation					
F 2082					

tools for providing guidance to MFBARS engineering and management personnel in assessing the LCC impact of proposed hardware configurations.

The Phase I LCC prediction varied from \$92M to \$116M, depending upon the model used and the hardware configuration (Table 8-25). The PRICE LCC prediction was heavily proportioned toward acquisition costs. The 10.5 percent of LCC remaining for logistics support is extremely low. On the other hand, the PRICE software procurement cost was considerably higher than that anticipated by TRW.

The Phase II LCC study saw some input values dramatically increased over Phase I levels (8.4.1), due to improved definition of the design and readjustment of cost inputs in today's economic climate. Of the models used in the Phase II analysis, only the TRI-TAC model shows total LCC costs. The LSC model, indicating costs of \$33.7 and \$21.8M (Table 8-25) for the two cases presented, does not include development, acquisition or operational costs, and the mini version excludes certain support cost categories. The Phase II PRICE results of \$8.013M indicates development cost and integration costs for TRW units only; it does not include production costs. (PRICE LCC runs were not provided by the Government during Phase II).

There is relatively close agreement in software procurement costs. Among the three models used, procurement costs were \$363M (PRICE-S), \$353M (SCEP), and \$4.0M (LSC), respectively; in addition, the LSC model designated \$.9M for software support costs.

The total life cycle cost, as projected by the TRI-TAC model, now stands at \$255M. This sum will be used as the baseline for the Phase III effort. TRW anticipates that, as the design matures in Phase III, improved definition of cost inputs will provide increased accuracy of MFBARS economic analyses.

Table 8-25. MFBARS Phases I and II LCC Summary Chart

	PHASE I			PHASE II
	BASELINE	ALTERNATE 'A'	ALTERNATE 'B'	
<u>ARCHITECTURE</u>	1 PROCESSOR 3 TRANSMITTERS 4 SOFTWARE PKG	1 PROCESSOR 2 TRANSMITTERS 4 SOFTWARE PKG	1 PROCESSOR 2 TRANSMITTERS 5 SOFTWARE PKG	1 ICNIA TERMINAL 2 TRANSMITTERS 2 SOFTWARE PKG 2 ANTENNA 1 ELECTRONIC BOX
<u>LOGISTIC SUPPORT COST</u>				(a) (b)*
SOFTWARE ACQUISITION	\$ 655,500	\$ 655,500	\$ 724,500	\$ 4.0M \$ 4.0M
SOFTWARE SUPPORT	248,775	248,775	264,825	.9M .9M
TOTAL LSC	2.21M	2.10M	2.36M	33.7M 21.8M
<u>TRI TAC</u>				
R&D ESTIMATE	\$ 4.4	\$ 4.4M	\$ 4.5M	\$ 23.9M
INVESTMENT	70.M	63.5M	72.M	149.9M
OP. & SUPPORT	26.5M	24.4M	27.2M	80.5M
TOTAL LIFE CYCLE COST	100.8M	92.3M	103.6M	255.3M
<u>PRICE</u>				
ACQUISITION	\$103.4M			\$8.013M
SUPPORT	12.25M			(Development, with Integ. cost, TRW units only.)
TOTAL LIFE CYCLE COST	116.6M			\$3.63M (TRW units only)
<u>PRICE S</u>				
PROCUREMENT COST	\$943,000			\$3.53M
<u>SCEP</u>				
PROCUREMENT COST	\$524,000			

*Less ECB & Associated AGE

9. RECOMMENDATIONS FOR PHASE III

TRW's baseline system for MFBARS employs advanced technology to achieve the basic objectives of real estate and life cycle cost savings. In order to solidify this system design, an examination of this technology was undertaken during the Phase II study to assure that the proposed system could be implemented for operation in the late 1980's. The results of this examination (Table 9-1) indicated that the required technologies are presently available except for additional improvements in a limited number of areas. No new breakthroughs in technology are required. Most of the required additional technology will occur as a natural outgrowth of scientific and engineering progress. However, some of this technology is unique to MFBARS. Therefore, it is prudent for the MFBARS program to conduct, in Phase III, a validation of the critical technology areas associated with the baseline design. A study was conducted to identify the priorities for such an undertaking. The criteria for the priority recommendation is based on:

- High leverage for cost and size reduction
- Development lead time
- Uniqueness to MFBARS
- Risk minimization prior to advance development model.

The results of this evaluation are tabulated in Table 9-2, and indicate that the four tasks should be considered for Phase III. These tasks are described in the next four sections of this report and are as follows:

- Design development of an RF LSI HF/VHF/UHF receiver module.
- Validation and demonstration of the matrix signal processor architecture.
- Design and development of a wideband antenna system.
- Design and development of an RF LSI quadrature linear amplitude modulator.

Table 9-1. MFBARS Technology Status

TECHNOLOGY	STATUS
1. <u>RECEIVER</u>	
LOW NOISE AMPLIFIER	UNDER DEVELOPMENT AT TRW
RF LSI	
SP4T SWITCH	UNDER DEVELOPMENT AT TRW
4PST SWITCH	NEW, TECHNOLOGY SIMILAR TO SP4T SWITCH
IF CORRELATOR/DEMODULATOR	NOSC CONTRACT, GPS PROPOSAL
GPS FREQUENCY SYNTHESIZER	GPS PROPOSAL
RF AMPLIFIER/DOWNCONVERTER	NOSC CONTRACT, GPS PROPOSAL
HF/VHF/UHF CONVERTER AMPLIFIER	NEW, TECHNOLOGY MATURE
GENERAL PURPOSE FREQUENCY SYNTHESIZER	NEW, SIMILAR TO EXISTING CHIP (FSP)
DIGITAL CORRELATOR/CONVOLVER	NEW, TECHNOLOGY MATURE
SAW FILTERS	NEW, TECHNOLOGY MATURE
2. <u>TRANSMITTERS</u>	
L-BAND POWER AMPLIFIER	EBS TECHNOLOGY UNDER DEVELOPMENT
VHF/UHF POWER AMPLIFIER	BIPOLAR TECHNOLOGY MATURE, ADDITIONAL DEVELOPMENT REQUIRED FOR FET
RF/LSI	
QUADRATURE MODULATOR	NEW, TECHNOLOGY MATURE
3. <u>MICROSIGNAL PROCESSOR</u>	
DIGITAL LSI (2)	
MATRIX SWITCH	NEW, TECHNOLOGY MATURE
SEQUENCER/CONTROLLER	NEW, TECHNOLOGY MATURE
PROCESSOR ARCHITECTURE	NEW, DESIGN
4. <u>ADAPTIVE ANTENNA</u>	
WIDEBAND ANTENNA ELEMENTS	NEW DEVELOPMENT
ANTENNA PLACEMENT TECHNIQUE	REQUIRED OF DEVELOPMENT OF COMPUTER SIMULATION PROGRAM
LOW LOSS WEIGHT	NEW DEVELOPMENT
ALGORITHM	TECHNOLOGY MATURE, NEW DESIGN

Table 9-2. Technology Development Priority Assessment

TECHNOLOGY	CRITERIA	LEVERAGE	RISK	UNIQUENESS	LEAD TIME (IN YEARS)
RECEIVER	• LOW NOISE AMPLIFIER	SMALL	MINIMAL	NO	2
	• RF LSI				
	SP4T	VERY HIGH	MINIMAL	NO	1
	4PST	VERY HIGH	AVERAGE	NO	1
	IF CORRELATOR / DEMODULATOR	MEDIUM	AVERAGE	NO	2
	GPS FREQUENCY SYNTHESIZER	SMALL	AVERAGE	NO	2
	RF AMPLIFIER / DOWNCONVERTER	VERY HIGH	AVERAGE	NO	2
	1. HF /VHF /UHF /CONVERTER	HIGH	AVERAGE	YES	2
	GENERAL PURPOSE FREQUENCY SYNTHESIZER	VERY HIGH	MINIMAL	NO	1
	3. DIGITAL CORRELATOR / CONVOLVER	VERY HIGH	AVERAGE	NO	2
	• SAW FILTER	MEDIUM	MINIMAL	YES	1

Table 9-2. Technology Development Priority Assessment (Continued)

TRW TECHNOLOGY	CRITERIA	LEVERAGE	RISK	UNIQUENESS	LEAD TIME (IN YEARS)
TRANSMITTERS					
•	L BAND POWER AMPLIFIER	HIGH	AVERAGE	NO	3
•	VHF/UHF POWER AMPLIFIER	MEDIUM	LOW	NO	2
5.	<u>RF/LSI QUADRATURE MODULATOR</u>	LOW	AVERAGE	YES	2
MICROSIGNAL PROCESSOR					
•	LSI MATRIX SWITCH	HIGH	LOW	YES	2
•	LSI SEQUENCER/CONTROLLER	HIGH	LOW	YES	2
2.	<u>PROCESSOR ARCHITECTURE</u>	HIGH	AVERAGE	YES	3
ANTENNA					
4.	<u>WIDEBAND ELEMENT</u>	HIGH	HIGH	YES	3
•	ANTENNA PLACEMENT TECHNIQUE	HIGH	LOW	YES	1
•	LOW LOSS WEIGHT	VERY	HIGH	NO	2
•	ALGORITHM	MEDIUM	AVERAGE	YES	2

9.1 RF LSI VHF/UHF RECEIVER MODULE

The proposed module is possibly the heart of receivers and covers the frequency region from HF to UHF, 2 to 500 MHz, which is utilized by many of the CNI systems such as SEEK TALK, UHF SATCOM, SINCGARS, and HF radio. Its development will allow an early evaluation of the standard module concept in the MFBAR program or other similar integrated radio and/or radar systems.

The proposed module as shown in Figure 9-1 consists of an RF LSI chip, two filters, and a frequency synthesizer. The RF LSI chip, wideband RF converter/amplifier is new and has to be developed in this program. It consists of three stages as shown in Figure 9-2, and can be configured to perform single, double, or triple conversion and/or be used as an RF/IF amplifier.

The first stage has a low-noise wideband AGC amplifier at the front end followed by a mixer. The second stage reverses this order with the mixer followed by an AGC amplifier. The LO inputs for these two stages are connected through switches which are used to select one of two possible LO inputs. Both mixer outputs are brought out from the chip to allow for external filtering. The LO inputs can also be dc and can cause one or both stages to operate as wideband AGC amplifiers. The final stage of the chip is used to form two quadrature signals (I and Q) for demodulation. The quadrature signals are generated by mixing with the LO signals which are 90 degrees out of phase. The 90 degree phase shift of the LO is obtained internally to the chip through a divided-by-4 circuit. Thus, the last LO input signal frequency must be four times that of the desired frequency. The recommended specifications for the RF LSI chip are summarized in Table 9-3.

The two filters in the module are used to attenuate the unwanted sidebands of the first two mixers. The first filter can be either a highpass filter with cutoff frequency at 225 MHz or a direct connection and thus can be used to select either the upper sideband of the first mixer or let the signal pass through without filtering. The second filter is a bandpass filter centered at the IF frequency of 70 MHz.

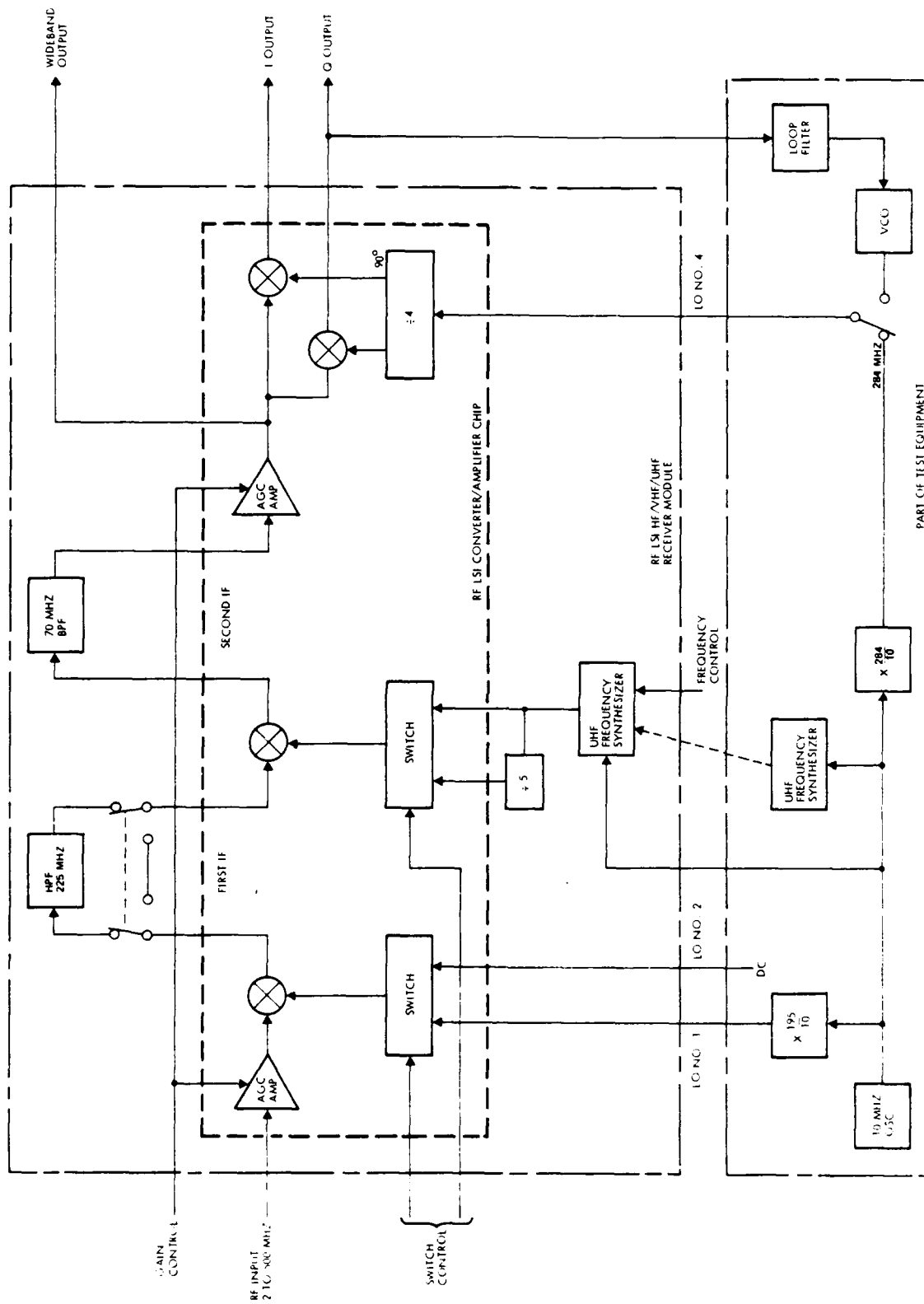


Figure 9-1. RF LSI HF/VHF/UHF Receiver Block Diagram

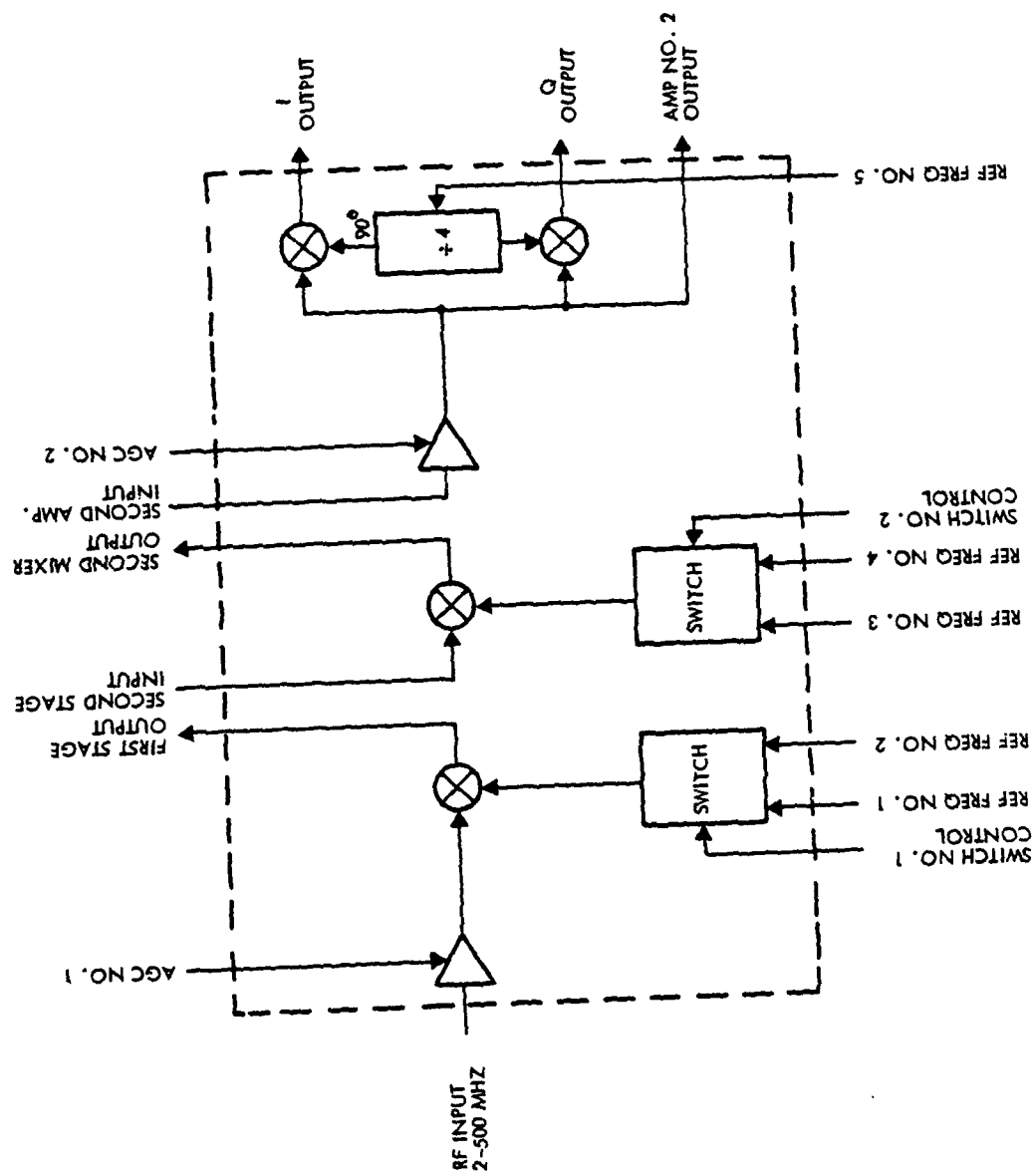


Figure 9-2. RF Converter/Amplifier Chip (RF LSI)

Table 9-3. Recommended Specifications for Frequency Converter/Amplifier RF LSI Chip

Item	Specification
Input Frequency Range	2 to 500 MHz
Wideband Output Frequency	70 MHz
Video Bandwidth	10 MHz
Video Output Imbalance	
Phase	<2 degrees
Amplitude	<0.5 dB
Gain	60 dB
AGC Range	70 dB
1 dB Output Compression Level	0 dBm
Noise Figure	5 dB
Local Oscillator Level	-10 dBm

The receiver module also contains a UHF frequency synthesizer (295 to 500 MHz), which can be either connected directly or through a divided-by-5 circuit into the LO port of the second mixer. By means of this frequency synthesizer, the output of the second mixer is centered at 70 MHz. The frequency synthesizer is expected to employ the TRW-developed RF LSI chip general purpose frequency synthesizer. This chip contains a complete single-loop indirect frequency synthesizer. The recommended specifications for the frequency synthesizer are tabulated in Table 9-4. It should also be noted that the receiver module provides a means to substitute an external frequency synthesizer as desired.

Table 9-4. Frequency Synthesizer Specifications

Item	Specification
Frequency Range	295 to 500 MHz
Step Size	5 kHz
Settling Time	≤ 200 μ S
Settling Error	5 degrees
Output Power	-10 dBm
Spurious	-60 dBc

The proposed program also includes the task of demonstrating the capability and performance of this module. The task can be accomplished with a test setup as shown in Figure 9-1. The test set is configured to operate over the MFBARS frequency band HF, 2 to 30 MHz; VHF, 30 to 88 MHz; and UHF, 225 to 400 MHz. For HF operation, the first mixer is operated with a dc input and causes the mixer to act as a buffer amplifier. No frequency conversion takes place. The LO for the second mixer must be selected from the divided-by-5 output which will have the desired frequency range of 72 to 100 MHz.

For the VHF operation, the LO of the first mixer will be at 195 MHz and thus upconvert the VHF input signals into the UHF range of 225 to 283 MHz. It will be necessary to employ the highpass filter. The output of the UHF frequency synthesizer can be used directly as the second LO to generate the 70 MHz IF.

Similarly, for the UHF input signal, the 70 MHz IF can be achieved with dc for the first LO and direct application of the UHF frequency synthesizer as the second LO. The operation and setting of the receiver module for the different frequency bands are summarized in Table 9-5.

Table 9-5. RF LSI HF/VHF/UHF Receiver Module Setting

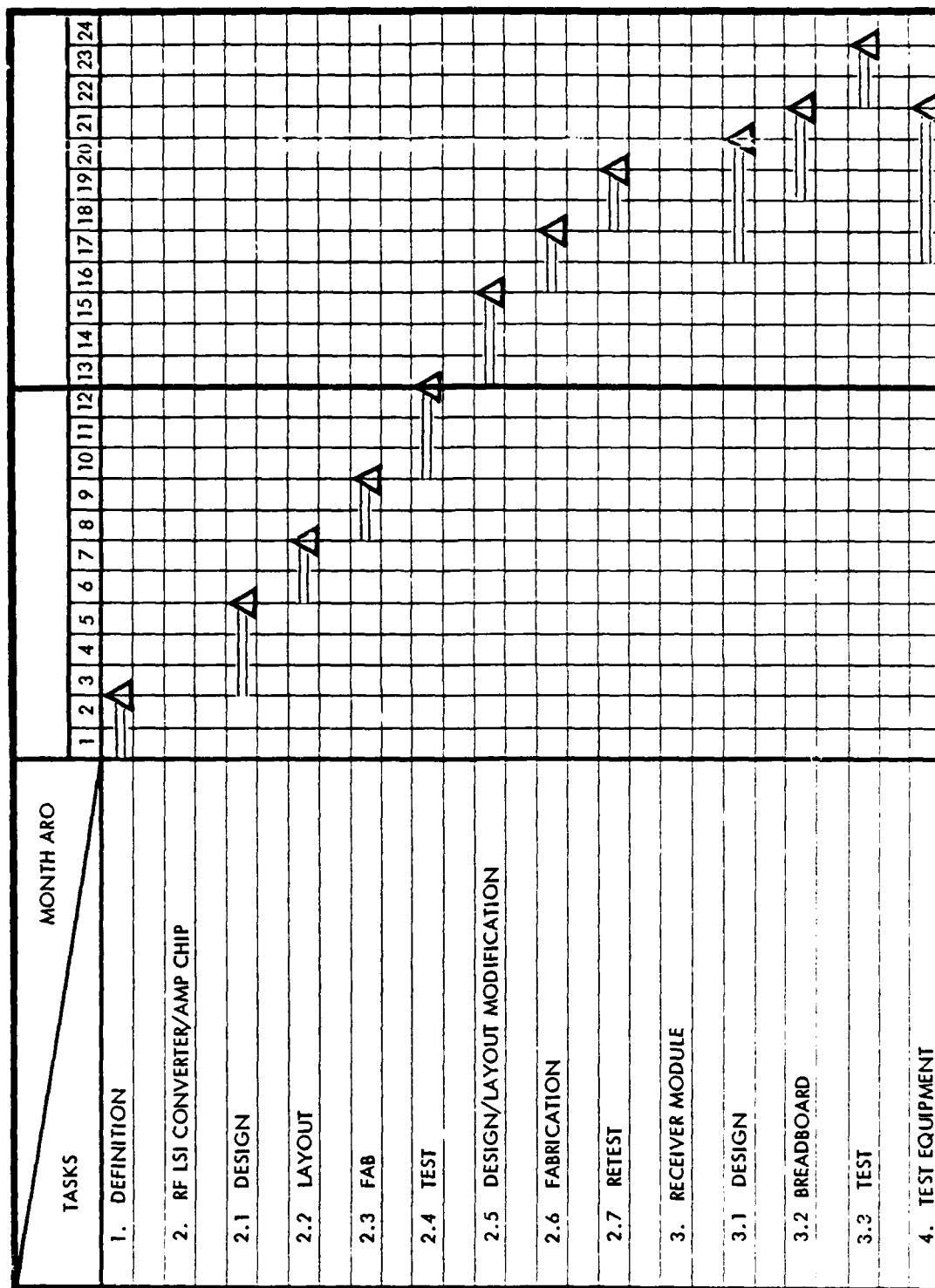
Parameters	Frequency		
	HF	VHF	UHF
First LO Frequency	DC	195 MHz	DC
First IF Filter	All pass	High pass	All pass
Second LO Frequency	72 to 100 MHz	295 to 353 MHz	295 to 470 MHz
Second LO Frequency Resolution	1 kHz	5 kHz	5 kHz

The test setup is also configured to demonstrate the usefulness of the receiver module to perform demodulation. Two video outputs are in quadrature and these can be conveniently connected externally to demodulate PM, AM, PSK, QPSK, FM, and other waveforms. For example, PM and FM signal demodulation and carrier tracking can be accomplished by utilizing the loop filter and VCO circuit connected as shown in the test equipment in Figure 9-1. In the case of digital processing, a fixed frequency LO is used and the I and Q outputs comprise the two quadrature components of the signal waveforms. They are available for IF sampling and A/D conversion into digital signals for processing by the computer or signal processor.

9.2 TASK AND SCHEDULE

The purpose of the proposed program is to design and develop a HF/VHF/UHF RF LSI receiver module prototype. The program consists of four tasks. The first task, definition, is for conceptual design and detail definition of the module and the RF LSI chips. The second task, RF LSI converter/amplifier, is for the development and building of the RF LSI chips. The third task, receiver module, includes the electrical design, construction, and testing of the receiver modules. The last task is for the assembly of the commercial and special test equipment for testing of the receiver module. The schedule for these tasks is shown in Table 9-6.

Table 9-6. RF LSI HF/VHF/UHF Receiver Module Development Schedule



9.3 VALIDATION AND DEMONSTRATION OF MATRIX SIGNAL ARCHITECTURE

The MFBARS Phase II design study defined the requirements and approach for a terminal encompassing seven different waveforms, including GPS, JTIDS, IFF, and SEEK TALK. A low cost TRW implementation for a fully integrated terminal incorporating small volume and low complexity consisted of an RF LSI front end and a high performance signal processor. The microprocessor-based signal processor or microsignal processor is a key flexibility and programmable element providing all baseband digital processing. This includes modulation, demodulation, digital filtering, link error correction/detection, and control/display.

High-speed real-time algorithm program executions are required for all simultaneous signal processing as well as meeting the combined 200 kbps input rates. The selected processor architecture, a closely-coupled distributed processor, can achieve very high processing capability in a small volume. The processor module interconnection network is based on a matrix or cross-bar switch not unlike that used in telephone exchanges. All processor module outputs (CPU, RAM, ROM, and I/O) can be connected to all of the module inputs upon command. Maximum multiprocessing utilization and limited fault tolerance are features of this matrix-signal-processor (MSP).

The largest multiprocessor configuration is four microprocessors interconnected by the matrix switch. A basic consideration of the interconnection is the degree of path conflicts or data concurrency. Higher processing efficiency would have fewer possible conflicts. Considerable analysis is required for different classes or applications.

Computer emulations are highly desirable as an effective method of modeling the MSP without committing to the expense of hardware. Benchmark programs can be programmed and executed by use of an accurate computer model of the basic MSP operation. Architecture refinements and iterations can be rendered inexpensive by modifying the model and performing a parametric sensitivity analysis.

The two selected MSP emulators are the SMITE and CDL programs. Refer to the task definitions, Table 9-7. SMITE is a multiprocessor analysis program emphasizing performance measurement and functional validation. CDL is a digital design language for multicomputer hardware simulation for hardware mapping and realizability. SMITE is used as a higher order language performance validator, complementing the more detailed CDL model which can validate actual processing throughput. Both programs are recommended for MSP architecture validation and demonstration.

Table 9-7. Validation and Demonstration of Matrix Signal Processor Architecture

<u>Tasks</u>
Benchmark algorithm selection and applications firmware signal processing algorithms
GPS Acq, R-S encoding, modem
Microcomputer Firmware
Executive, resource allocator
Assembler Modification
Existing MSP assembler table change
MSP Evaluation - I
Smite-analysis of multicomputer architectures oriented toward performance measurement and functional validation
MSP Emulation - II
CDL - digital design language for computer hardware simulation oriented toward hardware mapping and realizability

The basic tasks, in addition to the MSP emulation, include benchmark or demonstration programs such as Reed-Solomon decoding for effective performance display and the associated assembly language level instructions (which can be converted to machine level micro-instructions through the assembler). These tasks are necessary to provide the input stimuli for MSP signal processing emulation performance and operation. Normalized comparisons with standard benchmarks such as 1024-point complex FFT times are now feasible.

An 8-month schedule should be used for SMITE and CDL emulation development and evaluation. Emulation should be about 70 percent of the total effort. Figure 9-3 documents the final report with summary results, alternative architecture study, and emulation descriptions.

SCHEDULE

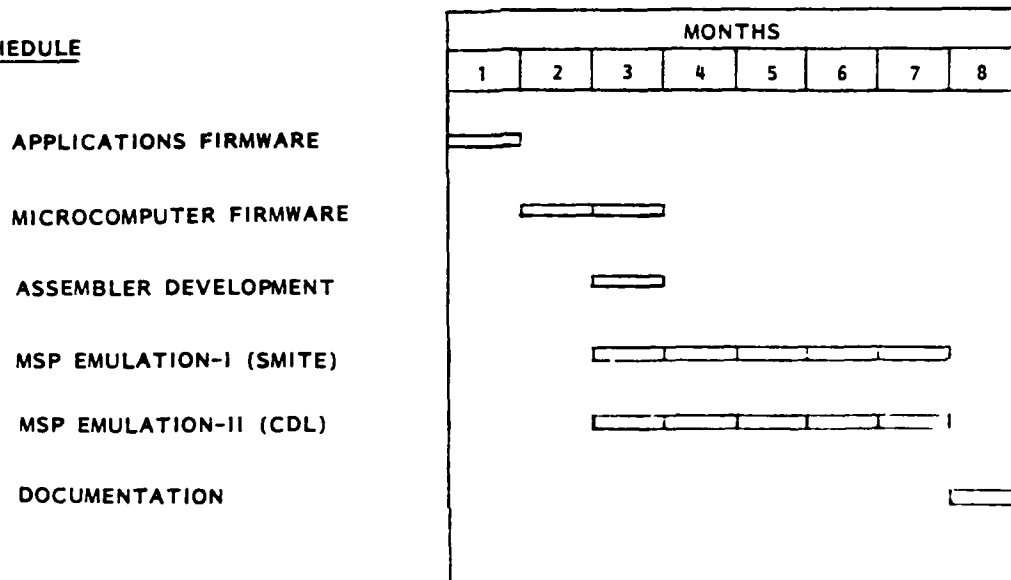


Figure 9-3. Validation and Demonstration of Matrix Signal Processor Architecture

9.4 WIDEBAND ADAPTIVE ANTENNA SYSTEM

9.4.1 Wideband Antenna Element Design

9.4.1.1 Problem

A high performance solution employing different antenna arrays for each MFBARS frequency band of function is extremely costly. An effective compromise single array solution for JTIDS/GPS can be realized provided that a wideband antenna element satisfying the following requirements can be developed (a similar design philosophy but different design constraints can be applied to SEEK TALK/SINGGARS):

- Desired signal coverage
 - Overhead for GPS
 - On horizon for JTIDS
- Desired signal polarization
 - RHCP for GPS
 - Vertical for JTIDS
- Bandwidth
 - L_1 and L_2 for GPS
 - Wideband frequency hop for JTIDS

9.4.1.2 Approach

Several approaches have been considered, but the two most attractive ones are based upon a conformal antenna element developed by Harris Corporation for GPS on an IR&D program. An important feature of this multimode microstrip design is that it can simultaneously satisfy the JTIDS/GPS coverage requirements. However, several important problems must be solved, including:

- An element optimized for GPS will have low gain in the JTIDS band unless the element can be rapidly tuned electronically
- An element optimized for JTIDS will be too large to array effectively at GPS frequencies.

An adaptive array processor which forms nulls independently in sub-bands of the full bandwidth is planned for JTIDS. Thus, information necessary for the tuning of antenna elements is available. Alternately, a nonconformal element design incorporating a monopole as well as microstrip components is under consideration (both fixed and electrically tuneable).

9.4.1.3 Tasks

The realization of a wideband design will require efforts ranging from system level specification of minimum acceptable performance to product design and testing. Several important tasks are:

- Definitization specification
- Preliminary design
- Performance estimation and design simulations
- Selection of best candidate
- Detail design
- Model fabrication
- Test
- Results analysis and comparison with theoretical predictions
- Design revision and repeat of fabrication test
- Report.

9.4.2 Low Loss Weight

9.4.2.1 Problem

A hybrid analog/digital adaptive array processor can very effectively reduce system costs. Critical components in this approach are the analog RF weights controlled by a digital processor. The customary RF weight is made from inphase and 90-degree phase-shifted power splitters which feed RF attenuating devices such as PIN diodes. This approach, however, has the disadvantage of relatively high minimum loss (approximately 10 dB).

In order to prevent significant system noise figure degradation, large amounts of low noise amplification (LNA) are required to overcome weight insertion loss. Additionally, in order to prevent signal-jammer cross-modulation, the LNA must have excellent intermodulation properties. One high quality amplifier is required for each antenna element; this is a relatively space expensive fix.

9.4.2.2 Approach

The need for high performance, low noise amplifiers is reduced or eliminated if a very low loss RF weight can be achieved. Three approaches are suggested:

- Dual phase shifter. Power is divided into two equal parts. Each is phase shifted independently and recombined. This results in an arbitrary amplitude and phase adjustment. Varactor phase shifters may be applicable to MFBARS.
- Phase shifter/attenuator. Use of varactors and PIN attenuators is suggested.
- Inphase-quadrature power division. Variable low noise gain elements replace the customary attenuators. Low noise FET devices are envisioned here.

9.4.3 MFBAR Antenna Placement Study

9.4.3.1 Problem

Antenna element placement suitable for an adaptive array on an airframe is considerably more difficult than element placement for simple coverage alone. The primary problem is that good reception of the jammers is required for effective null formation (nulling a jammer by 15 dB requires that the jammer inputs match to within 0.05 dB amplitude and 0.95 degrees RMS phase). Additionally, grating conditions must be avoided if desired signal enhancement is sought. This requirement is in conflict with good angular resolution of the jammers.

Regarding individual antenna element patterns, it is evident that if element/airframe coupling results in one element having a null in a particular direction and the other elements having good gain in that same direction, nulling degree of freedom will be lost if a jammer is located in that direction. For a fully constrained array (N elements, N-1 jammers), performance will suffer. Furthermore, due to limited available space for antenna location and the high cost of element placement on an airframe, it is desirable to share arrays among the several MFBARS functions. This substantially compounds the array design problem. Consider an array used simultaneously for JTIDS and GPS. If elements are placed to avoid grating conditions for GPS, low resolution of JTIDS jammers will occur.

9.4.3.2 Approach

For resolution, the problem must be divided into two major parts: basic array configurations and the effect of airframe/element interactions. Because what is acceptable (or good) for JTIDS may be poor for GPS, system level considerations are required to establish the basic shared array designs.

For example, grating nulls may actually be desirable for JTIDS. A widely spaced array design which has a grating null at one frequency may well have a lobe at another. Consequently, the fast wideband frequency hop of JTIDS might ensure that half of all signals are received on an antenna grating lobe. Conversely, GPS, being direct spread, would be harmed unless the widely spaced elements are turned off in that frequency band.

Secondly, the effect of airframe/element interactions can be accounted for through the use of GTD (Geometric Theory of Diffraction) analysis. An interactive process wherein basic array designs are generated and then specifically evaluated for airframe effects is expected to result in a satisfactory overall design. Principal items in this approach are:

- Basic Array Configuration
 - System requirements
 - Space availability
 - Function sharing constraints
- Airframe/Element Interactions
 - Modify adaptive and GTD performance prediction computer programs
 - Evaluate specific array designs for specific signals and jammers.

9.4.3.3 Tasks

Most tasks in this effort involve design or analytical evaluation. No hardware is to be constructed or experimentally evaluated. A summary of the effort follows:

- Establish system level constraints and performance requirements
- Produce several basic preliminary array designs
- Expand GTD/adaptive analysis computer programs
- Evaluate preliminary array designs in a representative system context
- Interactively refine basic array designs and evaluate
- Select the best design and detail its performance
- Report.

9.5 RF QUADRATURE LINEAR AMPLITUDE MODULATOR CHIP

The proposed RF LSI chip is the quadrature linear amplitude modulator. As shown in Figure 9-4, it consists of two basic stages. The first stage is a quadrature linear modulator which generates the modulations at the IF frequency; the second stage is a converter for obtaining the desired output carrier frequency at higher or lower levels than the IF. The heart of the first stage is the two four-quadrant multipliers which have the baseband data as one set of inputs and the IF carriers as the other. The IF carriers, generated by frequency dividing the LO No. 1 by 4, have the same frequency but offset by 90 degrees in phase. The outputs of the multipliers are then linearly summed. The summed output is split into two outputs. One output is buffered and brought out of the chip for use at the IF frequency, the other is connected to the mixer of the second stage. The mixer then converts (up or down) the modulated signal to the desired RF frequency for transmission. The recommended specifications for this RF LSI chip are shown in Table 9-8.

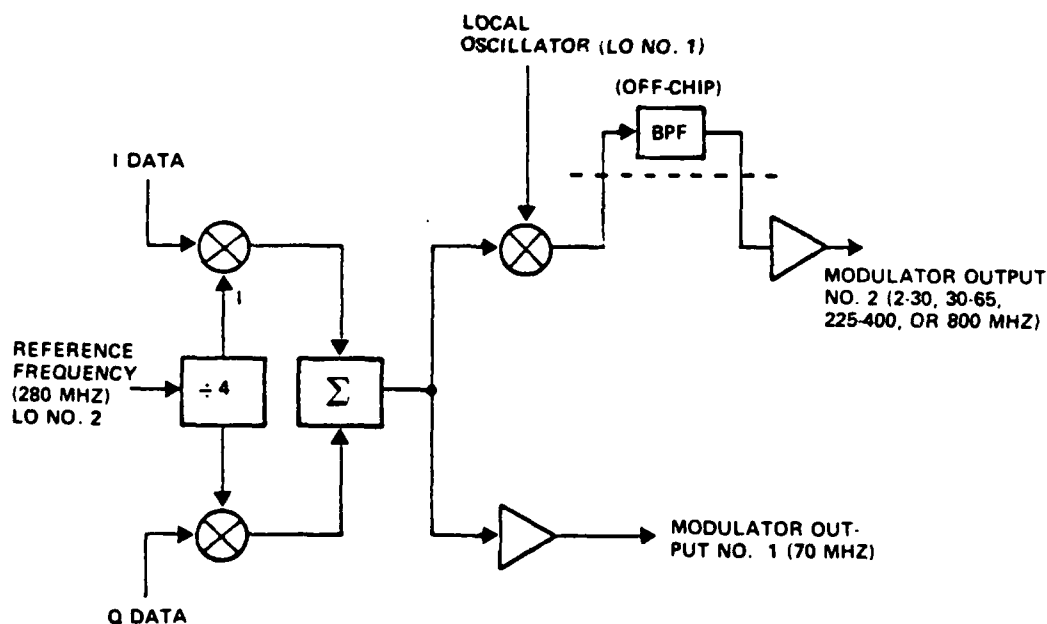


Figure 9-4. Quadrature Linear Amplitude Modulator Chip

Table 9-8. RF LSI Quadrature Linear Amplitude
Modulator Chip Specifications

Modulation	Specification
LO No. 1 Frequency Range	10 to 1600 MHz
Input level	-10 dBm
I or Q Data Rate	0 to 200 Mbps*
Output No. 1	Modulated IF
Level	0 dBm
Frequency	1/4 of LO No. 1 frequency
LO No. 2 Frequency Range	10 to 1600 MHz
Input level	-10 dBm
Output No. 2	RF output
Level	0 dBm
Frequency	$\frac{LO\ No.\ 1}{4} + LO\ No.\ 2$ But less than 1500 MHz
Maximum DC Power	1.5 W
Chip Size	200 mils square
Phase Imbalance	$\pm 2^\circ$ ($\pm 3^\circ$ for $f_o > 100$ MHz)
Amplitude Imbalance	± 0.3 dB
Amplitude Modulation Constant	100 percent per volt ± 5 percent

* Must be less than $1/8 \times LO\ No.\ 1$ frequency.

This RF LSI chip utilizes a proven configuration previously developed in the Standard Avionic Module (SAM) program. This configuration was proven capable of generating most modulation waveforms such as AM, PM, PSK, QPSK, FM, and FSK. For AM modulation, it is only necessary to put the same modulating signal to both baseband inputs. For PM modulation, the rms value of the two baseband inputs must be constant and the ratio of the inputs varies as a function of the information. Other modulation waveforms can be similarly formulated. This RF LSI chip is particularly useful when the baseband

inputs are derived from a signal processor which can be readily programmed to formulate the proper inputs and generate the desired modulation waveforms as required by many multifunctional radio systems such as MFBARS.

The proposed RF LSI chip can be developed in 18 months. It involves two cycles of design, layout, fabrication, and testing as shown in Table 9-9. The first cycle is the main effort and requires 12 months. The second cycle is for modification and correction, and requires approximately 6 months.

Table 9-9. RF LSI Quadrature Linear Amplitude Modulator Development Schedule

TASKS	MONTH ARO														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1. DEFINITION & DESIGN															
2. LAYOUT															
3. FAB															
4. TEST															
5. DESIGN & LAYOUT MOD															
6. FABRICATION															
7. RE-TEST															

DATE
FILME