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**Development of a Packet Speech Funnel Multiplexor:
A Final Report**

May 1982

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**Prepared for:
Defense Advanced Research Projects Agency**

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Bolt Beranek and Newman Inc.

DEVELOPMENT OF A PACKET SPEECH FUNNEL MULTIPLEXOR

A FINAL REPORT

15 July 1978 to 1 July 1981

May 1982

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Principal investigator: R. D. Rettberg



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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This Final Report summarizes Quarterly Technical Reports 1 through 12 which describe the development of a high-speed interface, called a Voice Funnel, between digitized speech streams and a packet-switching communications network.		

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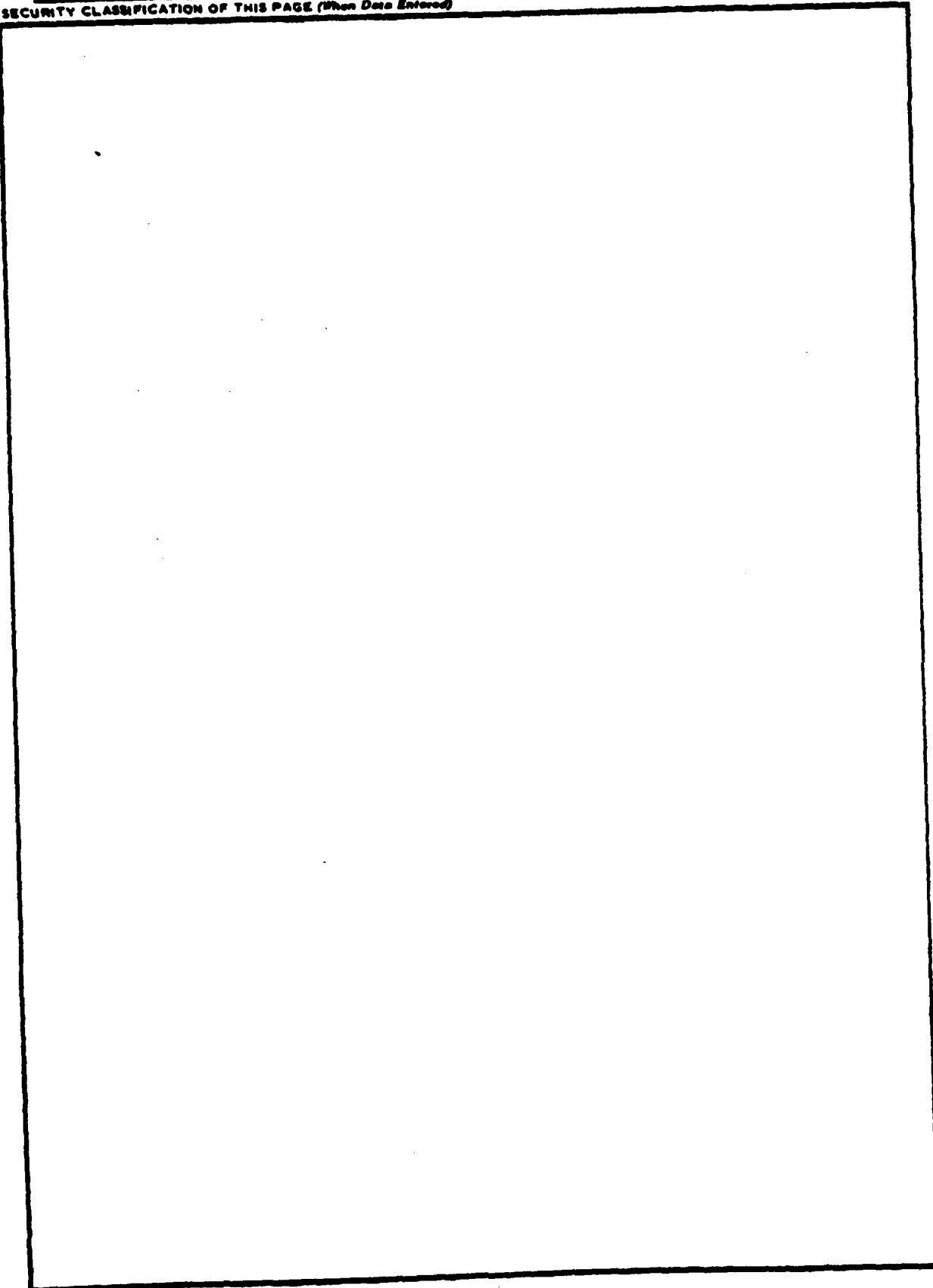
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Final Report

The combination of digital speech techniques with packet-switching technology can significantly increase the future voice transmission capability of the Department of Defense. To achieve this combination, however, requires a high speed interface between the digitized voice and the communications network. Under Contract No. MDA903-78-C-0356 during the period from 15 July 1978 to 31 July 1981, Bolt Beranek and Newman Inc. has designed and developed a system called the Voice Funnel which is a concentrator for digitized speech streams.

The Voice Funnel requires high data rate support; many connections; and the ability to perform processing in order to control the machine and the data streams. In order to meet these needs, a new multiprocessor called the Butterfly Multiprocessor has been developed.

The specifications and description of both the Butterfly Multiprocessor and the Voice Funnel have been provided in a series of Quarterly Technical Reports numbered 1 through 12. The contents and current applicability of these reports is summarized in the remainder of this report.

Abstracts of Quarterly Technical Reports

QTR1

QTR1, BBN Report No. 3972 [Obsolete], describes the criteria for the selection of a processor and several issues in the design of a Processor Node, and contains benchmarks for the Zilog Z8000 which was originally selected to be the processor in the Processor Node.

QTR2

QTR2, BBN Report No. 4143, describes the pre-implementation design of the Operating System and updates the design of the Butterfly Switch.

QTR3

QTR3, BBN Report No. 4149, examines the factors that limit the throughput of the Pluribus and provides strategies for flow control in the Wideband Network. It also provides a pre-implementation overview of the Voice Funnel design.

QTR4

QTR4, BBN Report No. 4182 [obsolete], describes the memory system of the Processor Node.

QTR5

QTR5, BBN Report No. 4396, introduces the notion of an Object system which unifies the structures of the operating system and the application software. It also describes the distributed power supply system of the Butterfly.

QTR6

QTR6, BBN Report No. 4563, describes in detail the design of the Processor Node hardware.

QTR7

QTR7, BBN Report No. 4564, describes the hardware of the current I/O interface board of the machine.

QTR8

QTR8, BBN Report No. 4660, documents the microcode development system we are using to develop the microprograms which control the Processor Node, the interface to the switch, and the I/O

board.

QTR9

QTR9, BBN Report No. 4666, explores the operation of the switch interface on the Processor Node and provides examples of the various switch transactions.

QTR10

QTR10, BBN Report No. 4816, provides the functional and programmer's specification for the I/O board.

QTR11

QTR11, BBN Report No. 4817, describes the development tools we are using for the Motorola MC68000.

QTR12

QTR12, BBN Report No. 4845, replaces QTR4 to give the current memory architecture and functions supported by the microcode of the Processor Node Controller.

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