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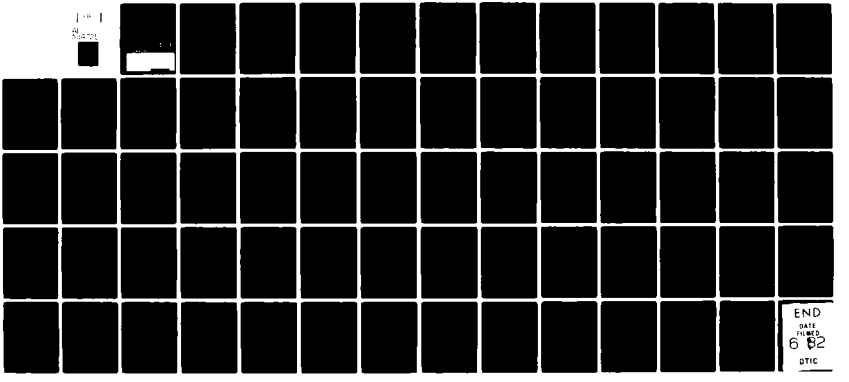

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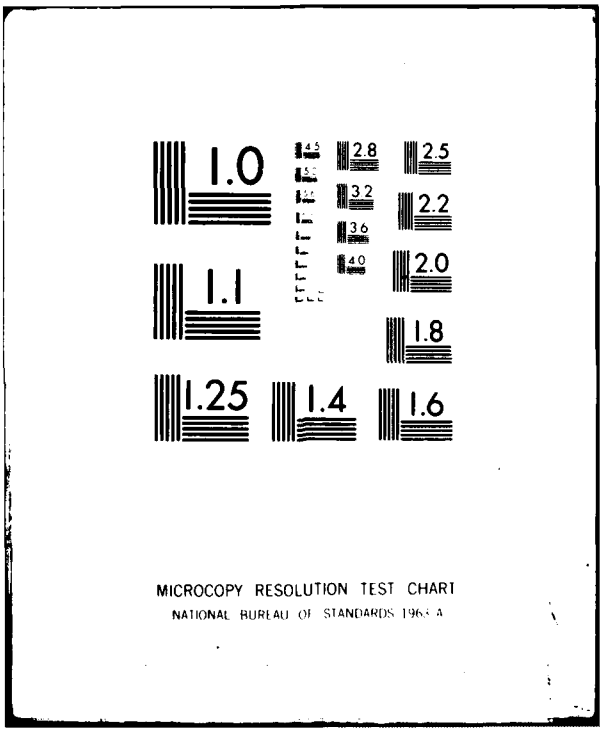
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DESIGN, TEST, AND COMPARATIVE ANALYSIS OF PROGRAMMABLE INTERFACE UNIT CIRCUIT CONFIGURATIONS

April 1982

Prepared for
NAVAL AIR REWORK FACILITY
NAVAL AIR STATION
ALAMEDA, CALIFORNIA
under Contract N00228-82-C-7132

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by

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ABSTRACT

This report summarizes the technical work performed by ARINC Research Corporation under Contract N00228-82-C-7132 from 2 November 1981 to 30 April 1982. This project was sponsored by the Naval Air Rework Facility (NARF), Naval Air Station, Alameda, California.

The report documents the results of analytic calculations and laboratory testing performed on three proposed configurations to solve power transistor overheating in the programmable interface unit (PIU) of the Hybrid Automatic Test Station (HATS). Recommendations are made regarding the most effective configuration in terms of cost and performance.

SUMMARY

This report contains the results of analytic calculations and laboratory testing performed on three proposed configurations to solve power transistor overheating in the programmable interface unit (PIU) of the Hybrid Automatic Test Station (HATS).

The HATS is a diagnostic device used by the Navy S-3A avionic support program to test and isolate faults on circuit cards and modules of Navy avionics systems. Frequent failures of the PIU cards in the HATS equipment prevent intermediate maintenance sites from providing necessary support for testing of aircraft avionics.

The objective of this project was to provide the Naval Air Rework Facility (NARF), Alameda, California, with (1) a PIU circuit configuration design that will limit the maximum output current of the stimulus buffer amplifier to 120 mA; (2) test results of this configuration and two other configurations proposed by NARF; and (3) a comparative analysis of the three configurations, with recommendations as to the most effective in terms of cost and performance.

The project was organized into three major tasks:

- Task 1 - Design Current-Limit Configuration and Analyze All Proposed Configurations. The current-limit configuration limited short-circuit output current to 120 mA. Two other configurations were also analyzed -- one substituting higher-rated transistors for the existing ones, and one combining the current-limit and transistor-substitution configurations.
- Task 2 - Conduct Testing and Comparative Analysis. All three proposed configurations were subjected to laboratory testing and a comparison of their performance and cost.
- Task 3 - Prepare Final Report. The report was prepared documenting the results of analytic calculations and laboratory testing and presenting conclusions and recommendations regarding the most feasible configuration.

The current-limit configuration consisted of changing the values for eight existing resistors that control the point at which current limiting of the amplifier output begins. The transistor-substitution configuration

substituted D40E7 and D41E7 transistors for the eight existing D40D11 and D41D11 transistors. The combined configuration implemented both the current-limit and the transistor-substitution configurations.

The pertinent electrical parameters considered were output amplitude, slew rate, rise time, fall time, and bandwidth. The primary thermal consideration was the power transistor junction temperature as a function of ambient temperature under low output, low load conditions.

Results obtained through laboratory testing confirmed the analytic predictions of electrical and thermal performance. These results were compared with the specified value for each parameter of interest or, where no value was specified, with the performance of the unmodified PIU.

The following primary conclusions were reached:

- The transistor-substitution configuration will not provide enough improvement in thermal performance to eliminate power transistor reliability problems.
- Both the current-limit and combined configurations will eliminate thermal problems in the power transistors, but will cause a slight degradation in output amplitude.
- The current-limit configuration is the least costly configuration to implement.

On the basis of these conclusions, the following actions are recommended:

- The criticality of the amplitude specification should be determined.
- On the basis of the criticality of the amplitude specification, either the current-limit configuration should be considered an acceptable solution to transistor overheating, or additional testing of that configuration should be conducted to determine if a trade-off can be made among output amplitude, current-limit level, and amplifier gain.

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CHAPTER ONE

INTRODUCTION

1.1 BACKGROUND

The Hybrid Automatic Test Station (HATS) is a diagnostic equipment used by the S-3A avionic support program to test and isolate faults on circuit cards and modules of Navy avionics systems. The HATS equipment is currently plagued with failures in the war wagon cabinet, which contains the programmable interface unit (PIU) card assemblies. Failure data obtained from the Navy maintenance material management (3-M) system have focused attention on the hybrid PIU (part number 400045-001). Frequent failures of the PIUs in the HATS equipment prevent intermediate maintenance sites from providing necessary support for aircraft avionic testing. As a result, the S-3A avionic support program is unable to meet mission requirements.

The Chief of Naval Operations has directed the Naval Air Systems Command (NAVAIR) to improve the exhibited poor reliability of the HATS. NAVAIR, in turn, has so directed the Naval Air Rework Facility (NARF), Alameda, California. Under Contract N00228-80-C-MV45, ARINC Research Corporation conducted a reliability improvement analysis of the PIU to determine the failure mechanisms of the PIU circuits. This analysis resulted in the isolation of problems in the PIU circuits, determination of the causes of failure, and identification of design deficiencies that promote or contribute to failure.

The conclusion of the analysis was that the largest single problem in the PIU is in the design of the stimulus amplifier power stage. Specifically, it was found that the junction temperatures in the D40D11/D41D11 power transistors exceed the maximum rated temperature of the devices under certain operating conditions.

The analysis recommended that the maximum allowable output current of the stimulus amplifier be limited to 120 mA. The effect of this would be twofold -- (1) the power transistor junction temperature would be held below its maximum rating under worst-case conditions; and (2) the resulting conservation of power would enhance the thermal environment of the PIU war wagon cabinet.

Another alternative, which was investigated by General Dynamics, San Diego, California, was to replace the D40D11/D41D11 power transistors with devices that have higher power ratings and thus could survive under worst-case conditions. This alternative was found to be less desirable than the first solution recommended, since it would involve potential problems with heat sinks and would not improve the war wagon thermal environment.

Engineers at NARF determined that further analysis and testing of all alternatives was required before initiating an engineering change proposal (ECP). Under Contract N00228-82-C-7132, ARINC Research Corporation was tasked to design a circuit configuration that will limit the maximum output current of the PIU to 120 mA and to analyze and test all alternative PIU configurations.

1.2 OBJECTIVES

The objectives of this project were as follows:

- Design a PIU circuit configuration that will limit maximum output current to 120 mA.
- Analyze and test three proposed PIU configurations -- the current-limit configuration, the transistor-substitution configuration, and a configuration that combines the current-limit and transistor-substitution configurations.
- Perform a comparative analysis of the three proposed configurations.
- Recommend the most effective configuration in terms of cost and performance.

1.3 SCOPE

The Statement of Work (SOW) constrained the current-limit configuration to replacement, substitution, or removal of components. No printed circuit board traces were allowed to be cut, and there could be no hardwire additions or changes in circuit card dimensions.

Each proposed configuration was analyzed to determine its thermal and operational performance. Specifically, the thermal analysis considered the impact of the proposed configurations on power transistor junction and case temperatures, heat sink temperatures, and surrounding components. The operational analysis considered the impact of the proposed configurations on output current amplitude, voltage amplitude, frequency response, slew rate, rise time, and fall time.

The proposed configurations were tested to verify the thermal and operational performance characteristics predicted by the analyses.

Finally, an analysis was conducted to compare the estimated cost and the performance of each of the proposed configurations.

1.4 TECHNICAL APPROACH

The project was organized into the three tasks described in the following subsections.

1.4.1 Task 1 - Design Current-Limit Configuration and Analyze All Proposed Configurations

Under Task 1, a circuit configuration was designed that limited the PIU output current to a maximum of 120 mA. This configuration did not require a change in circuit wiring or printed circuit board layout. A thermal performance analysis was conducted to consider power transistor junction temperature. An operational performance analysis considered PIU output voltages (amplitudes, frequency response, slew rate, and rise and fall times) and currents for each of three proposed PIU configurations. These configurations were (1) the present PIU modified to limit output current to 120 mA, (2) the present PIU with D40E7 and D41E7 transistors substituted for the D40D11 and D41D11 transistors, and (3) a PIU incorporating both the current-limit and the transistor-substitution configurations.

1.4.2 Task 2 - Conduct Testing and Comparative Analysis

The three proposed PIU configurations were physically implemented under Task 2. The modified PIUs were then subjected to operational and environmental tests to verify the thermal and operational performances predicted in Task 1. Test results were compiled in a format that allowed easy comparison of the three configurations.

1.4.3 Task 3 - Prepare Final Report

Task 3 was to incorporate the results of Tasks 1 and 2 into a final report, comparing the three proposed PIU configurations and an unmodified configuration from both a thermal and an operational performance perspective. This report presents a comparison of the relative complexity of the three proposed configurations, including time required and costs, and recommends the most effective configuration in terms of cost and performance. The report also includes pertinent schematics, parts lists, component layout drawings, and supporting engineering data.

1.5 REPORT ORGANIZATION

Chapter Two of this report presents a technical description of the proposed PIU configurations. Chapter Three addresses the plan of investigation, describing the details of the operational and thermal analyses, the laboratory test plan, and the test setup. Chapter Four presents the results of the investigation; it discusses the results of the theoretical analyses and presents the laboratory test data for each proposed configuration. Chapter Five is a comparative analysis of the results from Chapter Four. It also presents the conclusions and recommendations of the project.

Appendix A to this report presents the SYSCAP II model listings used in the operational analysis of the configurations. Appendix B discusses the PIU programmer used during laboratory testing. Appendixes C and D present thermal data recorded under various load conditions during laboratory testing.

CHAPTER TWO

TECHNICAL DESCRIPTION OF PROPOSED PIU CONFIGURATIONS

2.1 CURRENT-LIMIT CONFIGURATION

The current-limit configuration proposes to improve the reliability of the stimulus amplifier power transistors and thereby improve the reliability of the PIU. The configuration will do this by ensuring that the D40D11 and D41D11 transistors are held within their rated junction temperature extremes during worst-case conditions.

Figure 2-1 is a schematic diagram of the PIU stimulus buffer amplifier. The power transistors are shown as QX60, QX61, QX62, and QX63. The thermal performance of these transistors is illustrated in Figure 2-2,* which shows that an increase in ambient temperature operating range can be obtained if the maximum allowable current in each transistor is limited to 60 mA under worst-case load conditions ($V_O = 0$, $R_L = 0$).

The stimulus buffer amplifier is a push-pull type. Since the upper and lower halves of the amplifier operate identically, the following description of the current-limit configuration will be simplified if only the upper half of the amplifier is considered.

Figure 2-3 shows the subcircuit for the upper half of the amplifier from the base of driver transistor QX58 to the output port (V_O). In this design, the current-limiting transistor, QX56, shunts a portion of the base bias current of the driver transistor, QX58, whenever the base-emitter voltage of QX56 reaches 0.6 V. This turn-on voltage is controlled by voltage V_X through the voltage divider formed by RX70 and RX71. At the present values for RX70 and RX71, current limiting begins when V_X is 1.92 V:

$$V_B = \frac{(RX71)\left(V_X\right)}{RX70 + RX71}$$

---

*A detailed discussion of the transistor junction temperature performance can be found in *Reliability Improvement Analysis of the Programmable Interface Unit of the Hybrid Automatic Test Station*, ARINC Research Publication 1777-01-1-2318, November 1980.

Therefore

$$V_X = \frac{(100 + 220)\ (0.6)}{100} = 1.92\ V$$

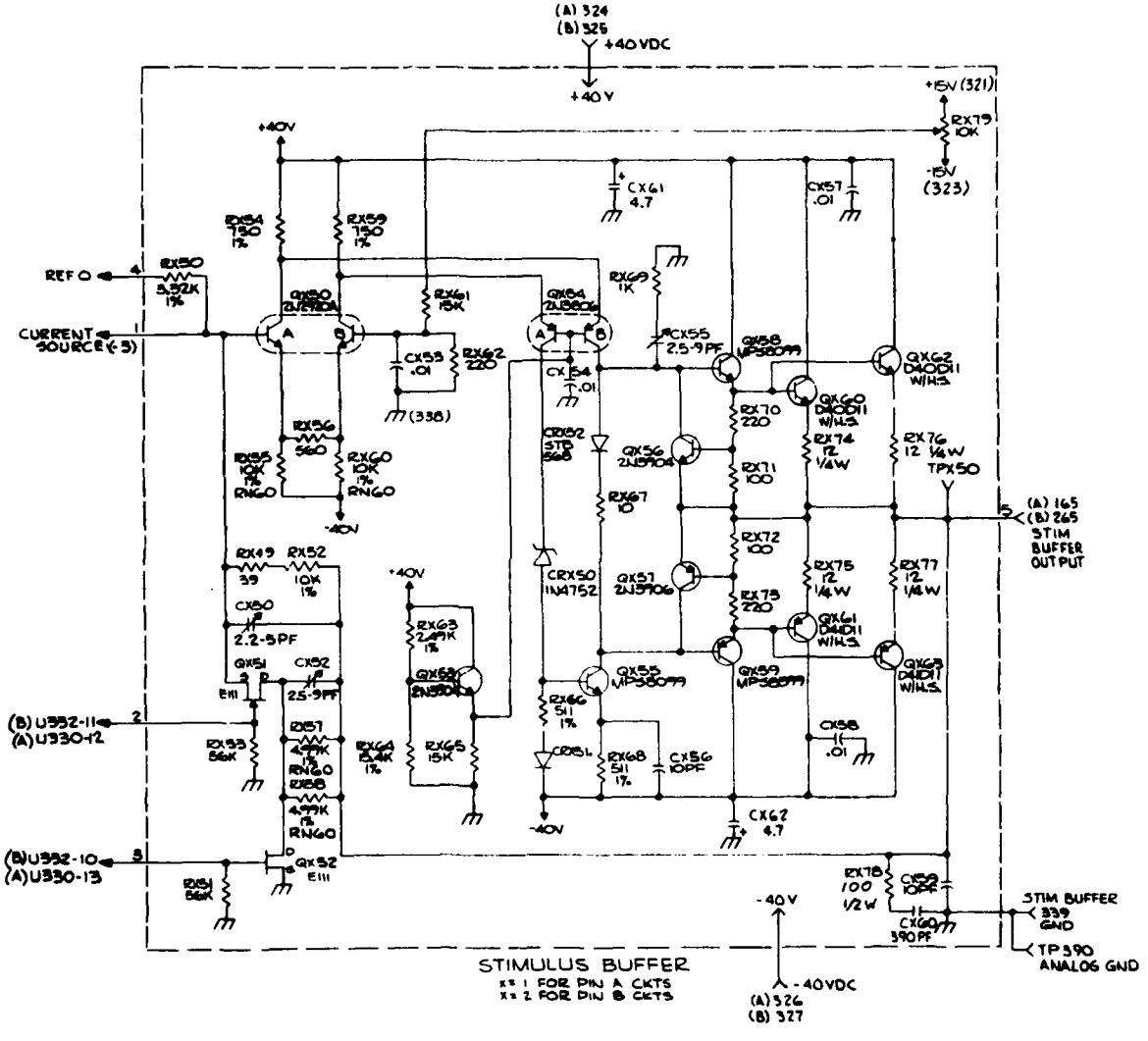


Figure 2-1. SCHEMATIC DIAGRAM OF THE PIU STIMULUS BUFFER AMPLIFIER

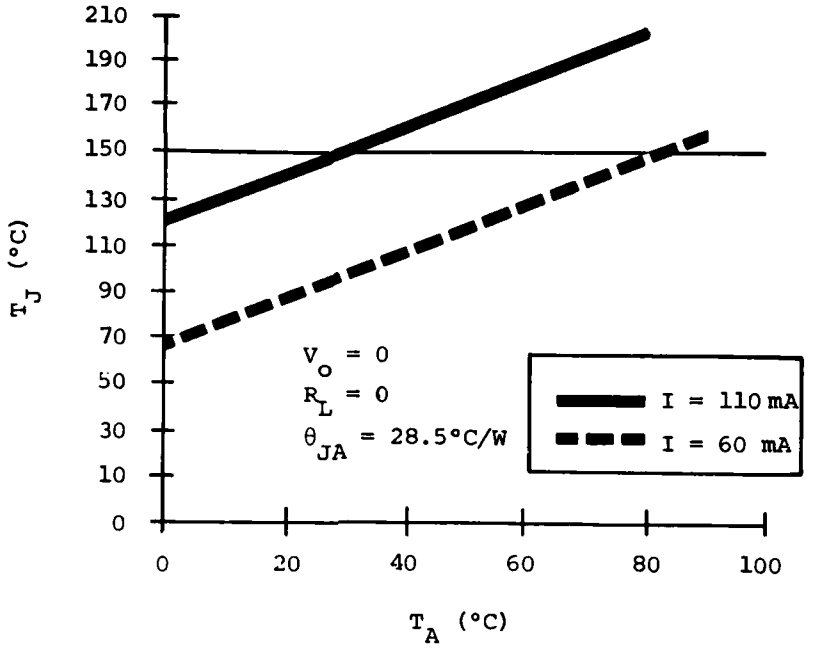


Figure 2-2. THERMAL PERFORMANCE OF D40D11/D41D11 TRANSISTORS

This corresponds to an emitter current in each power transistor (QX60 and QX62) of 110 mA:

$$I_E = \frac{V_X - V_{BE}}{RX74}$$

$$= \frac{1.92 - 0.6}{12} = 110 \text{ mA}$$

Since the power transistors are in parallel, the total current at the output port under short-circuit loading is approximately 220 mA.* The required modification to limit the current in each power transistor to 60 mA (i.e., approximately 120 mA output current) is shown in Table 2-1.

The modification limits the emitter current in each of the power transistors to 60 mA by changing the value of V_X, at which the current-limiting transistor QX56 begins to shunt the base current in driver transistor QX58.

*There will be some small additional current at the output port due to the voltage across RX71 and the shunt through QX56.

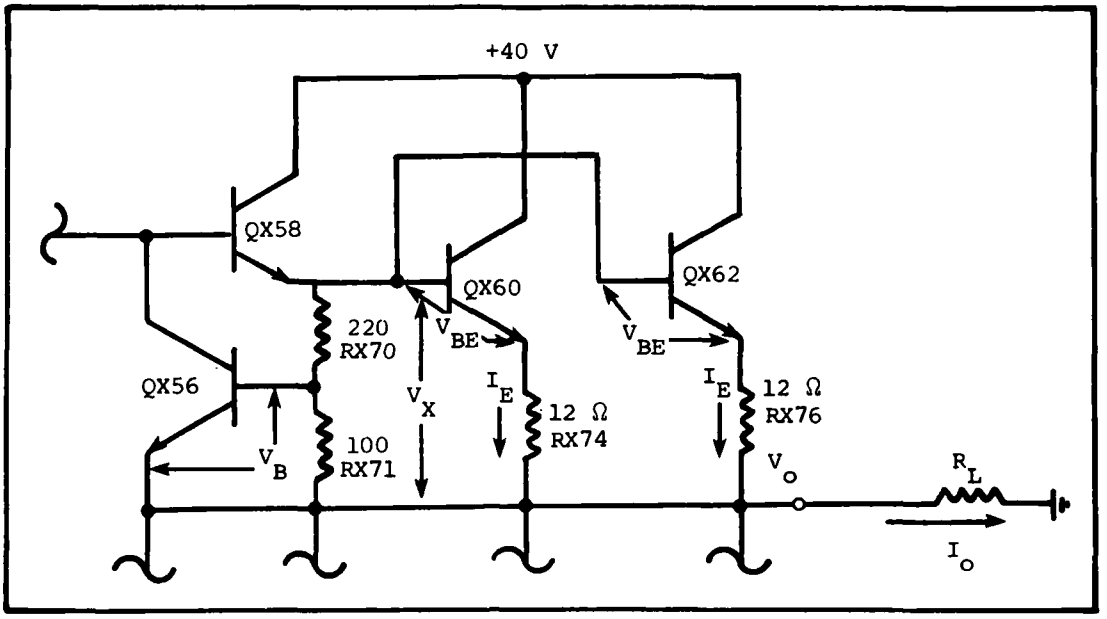


Figure 2-3. CIRCUIT FOR CURRENT-LIMIT CALCULATION

Table 2-1. CURRENT-LIMIT COMPONENT MODIFICATION

Transistor Circuit	Component	Original	Modified
Upper Half	RX70	220 Ω, 1/4 W	180 Ω, 1/4 W
	RX71	100 Ω, 1/4 W	150 Ω, 1/4 W
Lower Half	RX72	100 Ω, 1/4 W	150 Ω, 1/4 W
	RX73	220 Ω, 1/4 W	180 Ω, 1/4 W

Thus,

$$V_X = \frac{(RX70 + RX71)\left(V_B\right)}{RX71}$$

$$= \frac{(180 + 150)(0.6)}{150} = 1.32$$

This corresponds to an emitter current in each power transistor of 60 mA:

$$I_E = \frac{V_X - V_{BE}}{RX74}$$

$$= \frac{1.32 - 0.6}{12} = 60 \text{ mA}$$

Therefore, the maximum current that can flow through the output port under short-circuit loading is approximately 120 mA.

It should be noted that the total resistance seen by the active amplifier is RX70 + RX71. The current-limit configuration does not involve a significant change in this total resistance, but rather a change in the ratio of RX70 and RX71. This is important, because a significant change in the total resistance could lead to undesirable degradation in frequency response.

The configuration requires component substitution only; no printed circuit board traces need to be cut, and no hardwire additions or changes to the circuit card dimensions are required.

2.2 TRANSISTOR-SUBSTITUTION CONFIGURATION

The transistor-substitution configuration proposes to improve the reliability of the stimulus buffer amplifier power transistors by matching the thermal environment with higher-rated components. This configuration is a simple one-for-one replacement. Transistor type D40E7 replaces type D40D11 as QX60 and QX62; transistor type D41E7 replaces type D41D11 as QX61 and QX63. The pertinent characteristics of these transistors are shown in Table 2-2.

The most important difference in these two types of transistors is in their thermal resistance, θ_{JC}. Under worst-case PIU electrical conditions (i.e., $V_o = 0$, $R_L = 0$) with the present transistors, the power dissipation (P_D) in the device is 4.25 W.* Referring once again to Figure 2-3,

$$P_D = \left(V_{CE}\right)\left(I_E\right)$$

$$= [40 - (0.11)\ (12)]\ (0.11) = 4.25 \text{ W}$$

*A more detailed discussion of power calculations is given in ARINC Research Publication 1777-01-1-2318.

Table 2-2. COMPARISON OF OUTPUT TRANSISTOR RATINGS

Parameters	D40D11/ D41D11	D40E7/ D41E7	Degree of Improvement
Voltage			
V_{CEO}	75 V	80 V	5 V
V_{EBO}	5 V	5 V	None
V_{CES}	90 V	90 V	None
Current			
I_C (Continuous)	1.0 A	2.0 A	1.0 A
I_C (Peak)	1.5 A	3.0 A	1.5 A
Power Dissipation			
Tab at 25°C	6.25 W	8.00 W	1.75 W
Tab at 70°C	4.00 W	5.12 W	1.12 W
Thermal Resistance			
θ_{JC}	20.0°C/W	15.6°C/W	4.4°C/W
θ_{JA} (with PIU Heat Sink)	28.5°C/W	24.1°C/W	4.4°C/W

Since the transistor has a maximum allowable junction temperature of 150°C, the maximum safe ambient temperature (T_A) is 28.9°C:

$$T_A = T_J - \left(P_D\right)\left(\theta_{JA}\right)$$

$$= 150 - (4.25)\ (28.5) = 28.9°C$$

When the replacement transistors are used, the maximum allowable ambient temperature under worst-case PIU electrical conditions is 47.6°C:

$$T_A = T_J - \left(P_D\right)\left(\theta_{JA}\right)$$

$$= 150 - (4.25)\ (24.1) = 47.6°C$$

The increase of more than 18°C allowable ambient temperature is due to the increased capacity of the D40E7/D41E7 type of transistor to dissipate heat under maximum power operation. The predicted thermal performance improvement provided by the substitute transistors is illustrated in Figure 2-4.

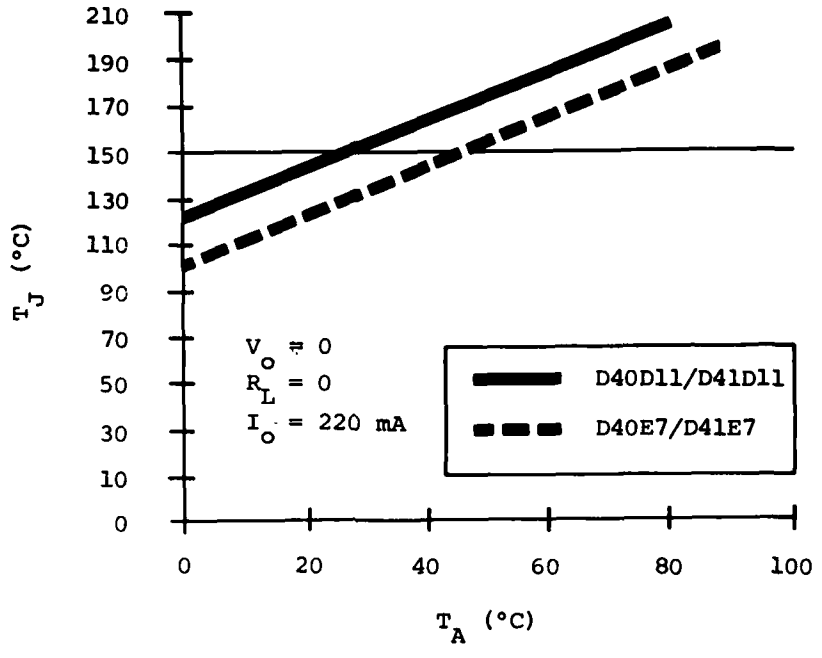


Figure 2-4. COMPARISON OF THERMAL PERFORMANCE OF D40E7/D41E7 TRANSISTORS AND D40D11/ D41D11 TRANSISTORS

2.3 COMBINED CONFIGURATION

To gain an extra margin of safety for operation of PIUs under high ambient temperature conditions, it was proposed that the current-limit configuration be combined with the transistor-substitution configuration. This configuration, hereafter referred to as the combined configuration, has the advantage over the other two configurations in that it should provide for optimal power transistor performance under even the most adverse PIU ambient temperature conditions.

In this configuration, the maximum power dissipation of the power transistors is 2.36 W:

$$P_D = \left(V_{CE}\right)\left(I_E\right)$$

$$= [40 - (0.06)\ (12)]\ (0.06) = 2.36\ W$$

The transistors have a maximum allowable junction temperature of 150°C with a thermal resistance (θ_{JA}) of 24.1°C/W. This corresponds to

a maximum safe ambient temperature of 93.1°C:

$$T_A = T_J - \left(P_D\right)\left(\theta_{JA}\right)$$

$$= 150 - (2.36)\ (24.1) = 93.1°C$$

Figure 2-5 compares the predicted power transistor performance for all three proposed configurations.

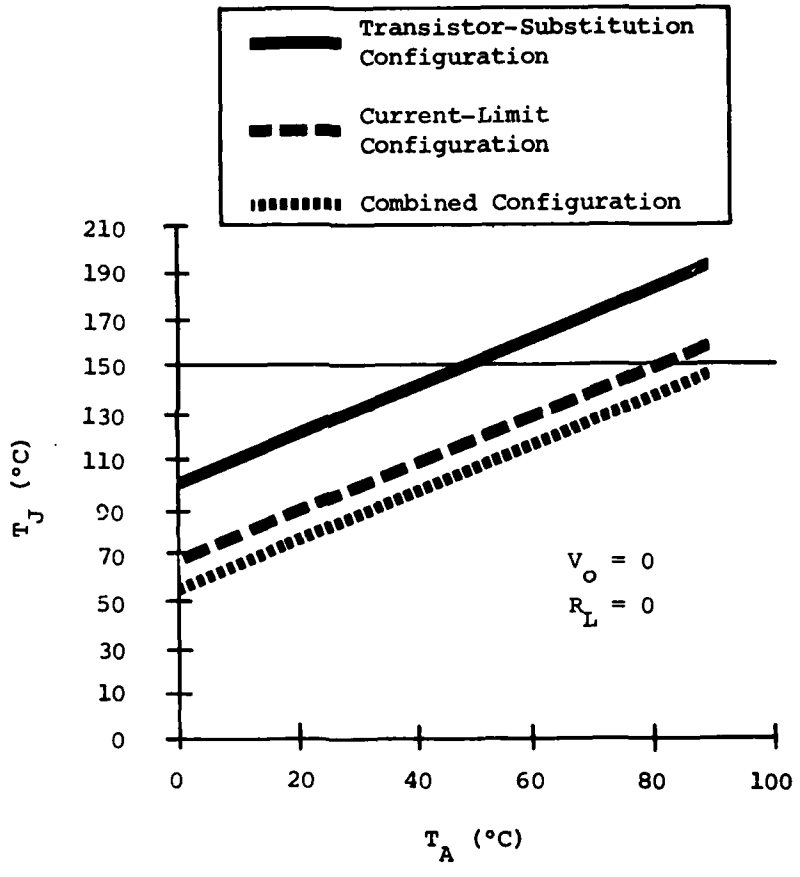


Figure 2-5. COMPARISON OF POWER TRANSISTOR THERMAL PERFORMANCE FOR ALL CONFIGURATIONS

CHAPTER THREE

PLAN OF INVESTIGATION

3.1 DESCRIPTION OF OPERATIONAL ANALYSIS

A systematic, theoretical analysis of the PIU amplifier circuit was performed for each configuration, in which the amplifier was modeled as a system of nodes and branches and representative admittance and current matrices were developed. These matrices were then used to solve for the desired node and branch voltages and currents. The complexity of the PIU amplifier is reflected in the unwieldy matrix that describes the circuit. The solutions were therefore developed by use of the CYBERNET System Circuit Analysis Program (SYSCAP II).

SYSCAP II converts the user input of circuit elements and interconnections into admittance and current matrices. Nonlinear elements such as transistors and diodes are modeled in such a way as to include the effects of temperature and dynamic impedance resulting from movements in the static operating point of the device. SYSCAP II initially assumes linearity and solves the matrices for node and branch parameters. These parameters are then checked against the nonlinear component models for consistency. If the error between the two exceeds a preset level, SYSCAP II revises the parameters of the nonlinear component model and repeats the calculations. This iterative process continues until all node and branch parameters are within the preset error bounds.

The transient analyses were performed on the PIU amplifier under a SYSCAP II routine called TRACAP (Transient Circuit Analysis Program). Appendix A contains the program listings describing each of the PIU amplifier configurations.

Four configurations of the PIU stimulus amplifier were modeled by use of the SYSCAP II circuit analysis software -- the unmodified amplifier configuration, the current-limit configuration, the transistor-substitution configuration, and the combined configuration. The operation of each was simulated for an output voltage of ±30 V, and both 10-ohm and 300-ohm loads. Input stimuli for these simulations were a 6 mA current pulse of 1 microsecond duration and rise and fall times of 10 nanoseconds.

3.2 DESCRIPTION OF THERMAL ANALYSIS

Table 3-1 presents specification data for the integrated circuits (ICs) used on the PIU board. These data show that most of the ICs have a maximum ambient operating temperature of 70°C. Therefore, to eliminate the power transistors as the limiting device on the PIU board, the ICs should not be allowed to exceed their rated junction temperature of 150°C under worst-case loading when the ambient temperature is under 70°C.

A thermal model for power transistor performance was developed to analyze each proposed configuration. The model was incorporated into a computer program that allowed rapid calculation of transistor thermal performance under a variety of ambient temperature and electrical loading conditions. The model treated thermal performance in a way that is analogous to an electrical circuit -- that is, temperatures were treated as voltages, power dissipation as currents, and thermal resistances as electrical resistances. The thermal model for the power transistors is described pictorially in Figure 3-1. The following equations were derived from the model.

$$T_J = T_A + P_D \, (\theta_{JC} + \theta_{CS} + \theta_{SA})$$

$$T_J = T_C + P_D \, (\theta_{JC})$$

where

T_J = junction temperature

T_A = ambient temperature

θ_{JC} = junction-to-case thermal resistance

θ_{CS} = case-to-sink thermal resistance

θ_{SA} = sink-to-ambient thermal resistance

T_C = case temperature

The first equation was used during the thermal analyses to predict the maximum ambient temperature allowable before the 150°C rated junction temperature is exceeded. The second equation was used during laboratory testing to relate recorded device case temperatures to junction temperatures.

3.3 OPERATIONAL AND THERMAL TEST PLAN

A test plan was established to organize the overall testing of the three PIU configurations. The test plan outlined the procedures, equipment setup, data acquisition, and the overall approach used in conducting the tests.

Table 3-1. PIU COMPONENT SPECIFICATION DATA -- INTEGRATED CIRCUITS

Component	Part Number	Device Function	Manufacturer	Type	Volts (+)	Volts (-)	Max Pkg Diss P_D (mW)	T_A (°C)	No. of Ckts.	Fan-In Logic No. of Inputs	Volts (High Logic)	Volts (Low Logic)	Fan-Out Load Factor	Propagation Delay (τ)
UX(01-15) Odd	93L34	Memory	AMD	TTL	5	0	--	0 - 70	1	8	2 - 5	0 - 0.8	--	--
UX(02-16) Even	93L12	Memory	AMD	TTL	5	0	220	0 - 70	1	8	2 - 5	0 - 0.8	--	34 ns
UX(30)	SN75107AN	Inverter NAND	TI	TTL	5	5	225	0 - 70	2	2 - 3	5	5	--	25 ns
UX(31)	SN74S175N	D Flip Flop	TI	TTL	5	0	--	0 - 70	4	--	2 - 5	0 - 0.8	--	--
UX(32)	N82S30B	1 of 8 Decoder	SIC	TTL	5	0	--	0 - 70	1	--	2 - 5	0 - 0.8	--	--
UX(33)	2527V	RS Flip Flop	--	TTL	5	0	--	0 - 70	--	--	2 - 5	0 - 0.8	--	--
UX(34-35)	SN74S153N	1 of 4 Decoder	NSC	TTL	5	0	350	0 - 70	2	4	2 - 5	0 - 0.8	--	18 ns
UX(90-91)	MN9067	DAC	MNC	--	15	15	--	0 - 70	1	--	2 - 5	0 - 0.8	--	--
U301	SN7437N	NAND	TI	TTL	5	0	397	--	4	2	2 - 5	0 - 0.8	--	22 ns
U302	SN7402N	NOR	TI	TTL	5	0	135	0 - 70	4	2	2 - 5	0 - 0.8	10	15 ns
U303	SN74LS08N	AND	TI	TTL	5	0	44	0 - 70	4	2	2 - 5	0 - 0.8	22	20 ns
U304	SN74S05N	Inverter	TI	TTL	5	0	270	0 - 70	6	1	2 - 5	0 - 0.8	--	7.5 ns
U305	MC4006P	1 of 8 Decoder	Motorola	TTL	5	0	100	0 - 70	1	3	2.5 - 5	0 - 0.4	--	14 ns
U306, U307	SN74S02N	NOR	TI	TTL	5	0	225	0 - 75	4	2	2 - 5	0 - 0.8	--	5.5 ns
U308, U309	944PC	NAND	TI	TTL	5	0	17	0 - 75	2	5	2 - 5	0 - 1.0	10	50 ns
U310	SN7404N	Inverter	TI	TTL	5	0	165	0 - 70	6	1	2 - 5	0 - 0.8	--	22 ns
U3(30, 32, 33)	7421	AND	SIC	TTL	5	0	--	0 - 70	2	4	2 - 5	0 - 0.8	--	--
U331	SN74LS02N	NOR	TI	TTL	5	0	27	0 - 70	4	2	2 - 5	0 - 0.8	22	15 ns
U3(34, 40)	SN74LS04N	Inverter	TI	TTL	5	0	33	0 - 70	6	1	2 - 5	0 - 0.8	--	20 ns
U335	SN74S04N	Inverter	TI	TTL	5	0	270	0 - 70	6	1	2 - 5	0 - 0.8	--	4.5 ns
U336	SN74S139N	1 of 4 Decoder	TI	TTL	5	0	300	0 - 70	2	3	2 - 5	0 - 0.8	--	7.5 ns
U337	SN74S86N	Excl-Or	TI	TTL	5	0	375	0 - 70	4	2	2 - 5	0 - 0.8	10	7 ns
U338	SN74S00N	NAND	SIC	TTL	5	0	180	0 - 70	4	2	2 - 5	0 - 0.8	20	3 ns
U339	SN74H52N	AND-OR	TI	TTL	5	0	120	0 - 70	1	10	2 - 5	0 - 0.8	10	15 ns
U390	741TC	OP AMP	F	Linear	15	15	P_q = 85 mW	0 - 80	1	2	--	--	--	500 mV/1 µs

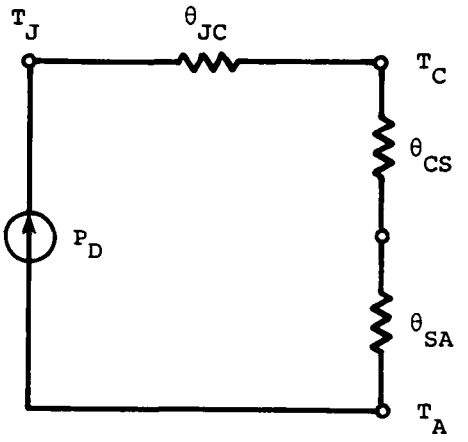


Figure 3-1. POWER TRANSISTOR THERMAL MODEL

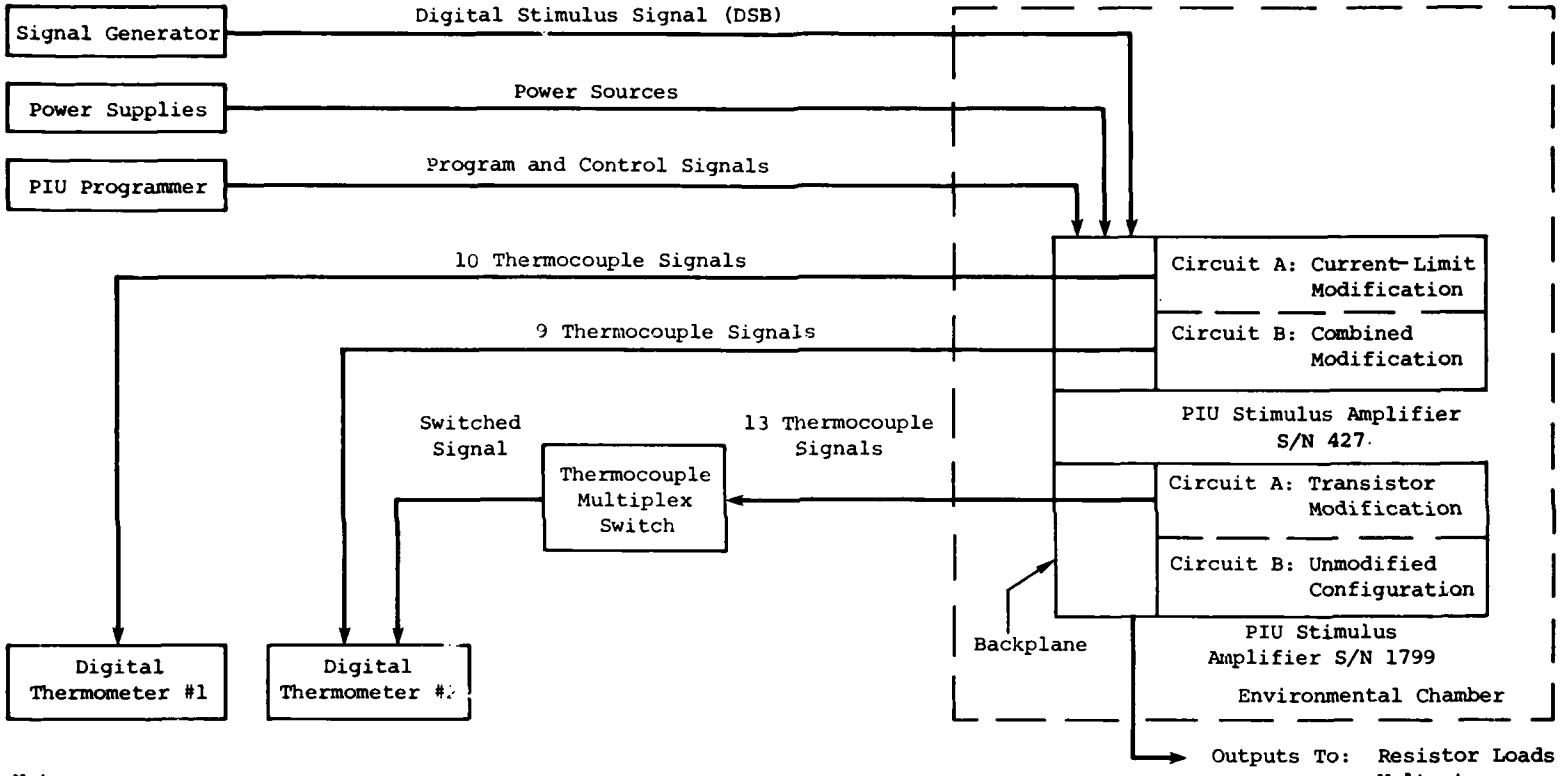
3.3.1 Pretest Requirements and Setup

To ensure that each PIU configuration was subjected to the same test conditions, all three configurations were placed in the environmental chamber and tested simultaneously. A test fixture was built to accommodate testing and monitoring of all three cards. The test fixture incorporated a backplane connector, provided by NARF, that was identical to the part used to interface the PIU cards with the HATS. During the test, access to the PIU card inputs, outputs, power source connections, data, address, and control lines was made through wiring connections at the backplane connector.

The PIU circuits require seven power supply potentials (+5 V, -12 V, +24 V, ±15 V, and ±40 V) for operation. These voltages were supplied to the PIUs through wiring connections in the backplane connector. A single-point ground connection was employed to avoid ground loop problems and reduce noise.

The input and output connections on each PIU card were also wired into the backplane connector to interface the card with the signal generator, external loads, and measuring instruments. The signal generator was used to provide the digital stimulus bus (DSB) signal required for the ac mode test. RG-223/U coaxial cables were used to couple the DSB signal to the PIU input, and the PIU output to the resistive loads, oscilloscope, voltmeters, ammeters, and spectrum analyzer.

Figure 3-2 depicts the overall laboratory test arrangement. The instrumentation setup for the temperature test measurements used thermocouple sensors, two digital thermometers, and a multiplex switch. The multiplexer allowed all three PIU configurations to be monitored with the limited number of digital thermometer input connections available.



Notes:

1. PIU inputs and outputs are accessed via connections to the backplane connector.
2. RG-223/U cable is used for DSB input and stimulus amplifier outputs.

Equipment Information:

- Spectrum Analyzer: HP 8553B (RF section), HP 8552B (IF section), HP 141T (display section)
- Power Supplies: HP 623GB, HP 6267B, Ambitrol TW-4005
- Signal Generator: Wavetek 166, 50 MHz pulse/function generator
- Digital Thermometer: Fluke 2100A, 10-channel unit
- Oscilloscope: Tektronix Type 561A
- Voltmeter: Simpson 260
- Ammeter: Daystrom, Inc., Weston Instruments Division
- Environmental Chamber: Tenny Engineering

Figure 3-2. TEST SETUP DIAGRAM

Finally, a means of programming the PIUs had to be devised so that the PIU modes of operation could be set up. The PIU is a subsystem of the HATS and is normally programmed and controlled by a computer in the HATS. In this test, however, the PIUs were to stand alone and could not be programmed in the usual manner. To circumvent this, a programmer was designed by ARINC Research to simulate functions performed by the HATS computer in setting up PIU operational modes. The programmer was interfaced with the PIU cards and provided typical functions, including:

- Storage of data containing PIU operational mode settings
- An addressing function to access the A and B circuits of each PIU card
- Loading of programming instructions into the PIU memories
- Hexadecimal display readout of data and code values
- Generation of timing and control signals

The programmer was used initially to check the operational status of the PIUs provided by NARF. This exercise checked the operation of the digital-analog converter (DAC) circuits, relays, memories, and the various digitally controlled functions of the PIU. More information on the design and operation of the programmer is provided in Appendix B.

3.3.2 Electrical Measurements

The electrical measurements consisted of PIU output voltages, currents, and operating frequency measurements corresponding to the various PIU operational modes used during the test. The electrical measurements were taken in conjunction with the thermal measurements as the PIUs were subjected to various temperature environments.

The PIU operational modes were classified into dc, ac, and current-limiting modes. In the dc mode, the PIUs were programmed for output voltages of +30 Vdc and +3.8 Vdc. In the ac mode, the PIU output was set for ±30 Vac and ±3.8 Vac modes of operation at a frequency of 100 kHz. The PIUs were tested at rated output conditions, which necessitated the use of a 300-ohm load for the +30 Vdc and ±30 Vac modes and a 39-ohm load for the +3.8 Vdc and ±3.8 Vac modes. In the current-limiting mode, the PIUs were programmed for +30 Vdc, -30 Vdc, +3.8 Vdc, and -3.8 Vdc modes. A 10-ohm load was used to force the PIU output into current limiting during the current limit tests.

The PIU operational modes used during the test are summarized as follows:

- DC mode
  - PIUs programmed for +30 V output with a 300-ohm load
  - PIUs programmed for +3.8 V output with a 39-ohm load

- AC mode (frequency = 100 kHz)
  - PIUs programmed for ±30 V output with a 300-ohm load
  - PIUs programmed for ±3.8 V output with a 39-ohm load
- Current-limiting mode
  - PIUs programmed for +30 V output with a 10-ohm load
  - PIUs programmed for +3.8 V output with a 10-ohm load
  - PIUs programmed for -30 V output with a 10-ohm load
  - PIUs programmed for -3.8 V output with a 10-ohm load

3.3.3 Thermal Measurements

The thermal measurements consisted of ambient temperature and case temperature measurements of instrumented PIU components. The following components were monitored in each PIU configuration:

- UX09, IC, 93L34PC
- UX11, IC, 93L34PC
- UX91, IC, MN9067
- UX90, IC, MN9067
- UX30, IC, SN75107A
- QX56, Transistor, 2N3904
- QX50, Transistor, 2N2920A
- QX60, Transistor, D40D11/D40E7
- QX61, Transistor, D41D11/D41E7
- QX58, Transistor, MPS8099

The components were instrumented with iron/constantan thermocouple sensors, which generated a voltage signal converted by the measuring instruments into a corresponding temperature value. The ambient temperature monitored was the air flow temperature in the vicinity of the instrumented components. The thermal measurements were taken at the ambient temperature range of 5°C to 65°C, and the measurement levels were divided into increments of 10°C. The PIUs were programmed in the operational modes previously described. The case temperatures were recorded for each operational mode after they stabilized at each ambient temperature measurement level.

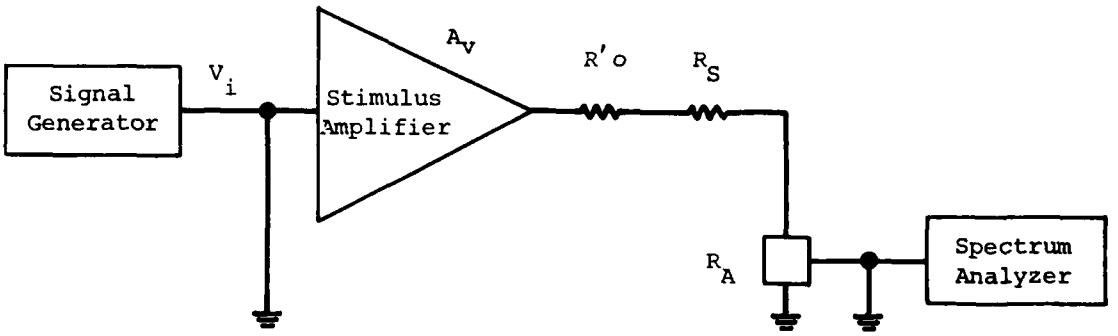
3.3.4 Circuit Response Measurements

The circuit responses measured were the frequency response and transient response on the stimulus buffer amplifier of each of the PIU configurations. These measurements were taken with the PIUs programmed in the ac operational

mode and at ambient temperature levels of 5°C, 25°C, and 65°C. These tests provided information about the following response characteristics:

- Bandwidth
- Slew rate
- Rise time
- Fall time
- Percent overshoot and undershoot
- Settling time

The bandwidth was measured by using the setup shown in Figure 3-3. The basic concept involved applying a signal with a known bandwidth spectrum at the input of the amplifier and observing the resulting spectrum at the amplifier's output. The bandwidth recorded was the 3 dB bandwidth of the amplifier.



Notes:

V_i - repetition rate = 22 kHz
pulse width = 50 nanoseconds

$R'o$ - programmed for 0 ohms

R_S - 220 ohms

R_A - 110 ohms (10 dB attenuation)

A_v - programmed for -3 (voltage gain)

Figure 3-3. BANDWIDTH MEASUREMENT SETUP

The transient response was measured by applying a 100 kHz DSB signal at the PIU input and monitoring the output signal with the oscilloscope adjusted to display the signal's time response characteristics.

CHAPTER FOUR

RESULTS OF INVESTIGATION

4.1 OPERATIONAL ANALYSIS

The following subsections present the results of the operational analysis described in Section 3.1. The output waveforms for each configuration exhibited a small dc offset from the zero baseline. This offset was the result of the values chosen for variable resistor RX79. This variable resistor is used to adjust the output dc offset in the physical implementation of the circuit. For purposes of this analysis, the waveforms were normalized to a zero dc offset.

4.1.1 Unmodified PIU Amplifier Configuration

Simulation of the unmodified stimulus amplifier operation provided a baseline for comparison with the proposed configurations. Figure 4-1 shows the output waveform of this configuration with a 300-ohm load as developed from the model.

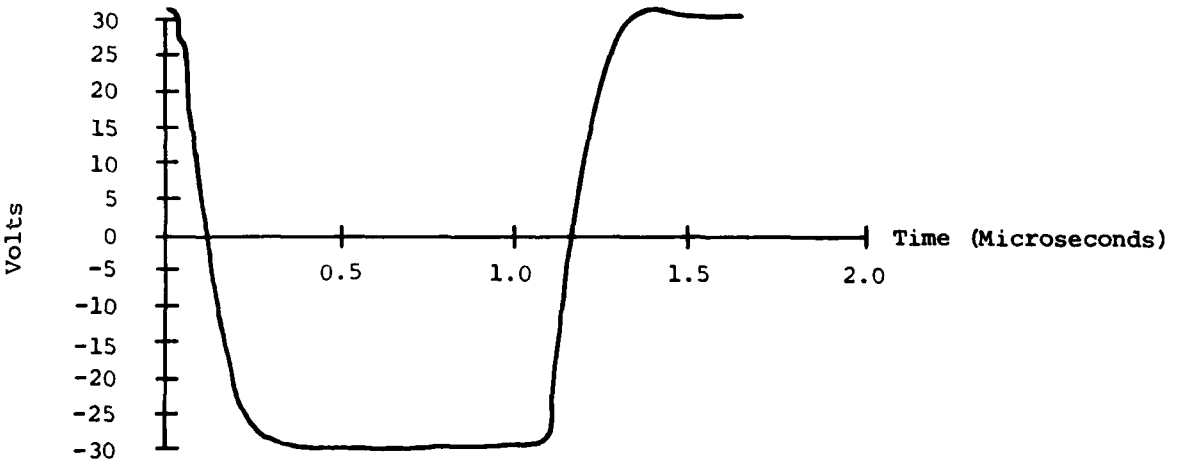


Figure 4-1. PIU UNMODIFIED CONFIGURATION RESPONSE WITH 300-OHM LOAD

The output voltage has an initial value of +30.203 V until time (t) = 12 nanoseconds (ns). At this point, the amplifier responds to the input by slewing from its initial value to -30.203 V. It remains at this voltage until t = 1.022 microseconds (μs), at which time it slews back to the initial value of +30.203 V. The 300-ohm load draws 100 mA from the output of the amplifier at the +30 V and -30 V limits shown in Figure 4-1. The simulation therefore predicts that the unmodified PIU stimulus amplifier meets the specified output of ±30 V at 100 mA.

Four parameters of interest are associated with the ac performance of the PIU stimulus amplifier -- slew rate, rise time, fall time, and bandwidth. These parameters are readily derived from the waveform in Figure 4-1.

Slew rate (S) is defined as the rate of change in output voltage when the amplifier is operating at its maximum rated current. For the unmodified PIU stimulus amplifier model, taken between plus and minus 10 volts,

$$S = \frac{\Delta V}{\Delta t}$$

$$= \frac{+10 - (-10)\ V}{(0.14 - 0.075)\,\mu s} = 308\ V/\mu s$$

Rise time (t_r) is the time required for the leading edge of a pulse to increase from 10 percent to 90 percent of its final value. Fall time (t_f) is the time during which a pulse is decreasing from 90 percent to 10 percent of its final amplitude. For the waveform shown in Figure 4-1, t_r = 159 ns and t_f = 150 ns.

The bandwidth (B) of the amplifier is inversely proportional to the rise time of the waveform in Figure 4-1, i.e., where K is a function of the amplifier damping constant and is approximately 0.35. For the unmodified PIU amplifier,

$$B = \frac{K}{t_r}$$

$$= \frac{0.35}{t_r} = 2.20\ MHz$$

Figure 4-2 shows the output of the unmodified PIU stimulus amplifier model when the simulation is performed with a 10-ohm load. From the waveform we can calculate the current delivered to a load during hard current-limiting operation. At equilibrium, the voltage across the 10-ohm load is 2.5 V, for an output current of 250 mA.

4.1.2 Current-Limit Configuration

Figure 4-3 shows the output waveform of the current-limit configuration model for simulated operation with a 300-ohm load. The initial voltage for this configuration is +29.67 V. It remains at this value until t = 12 ns,

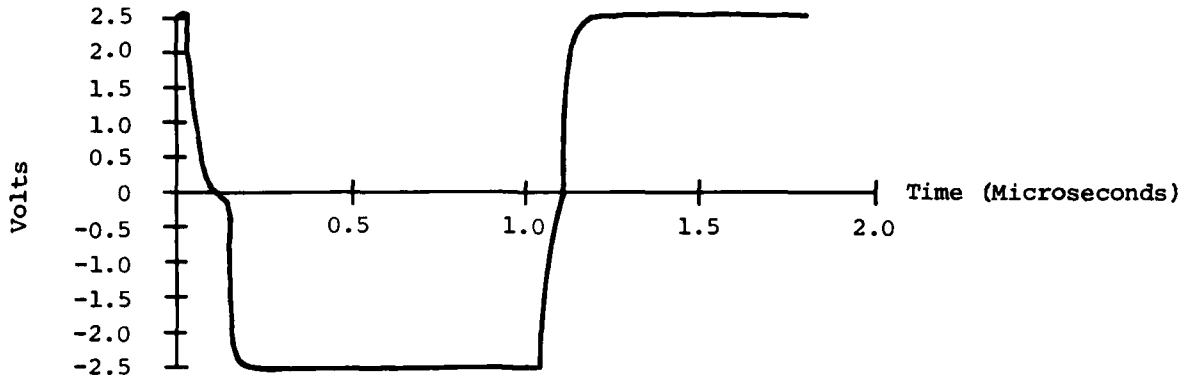


Figure 4-2. PIU UNMODIFIED CONFIGURATION RESPONSE WITH 10-OHM LOAD

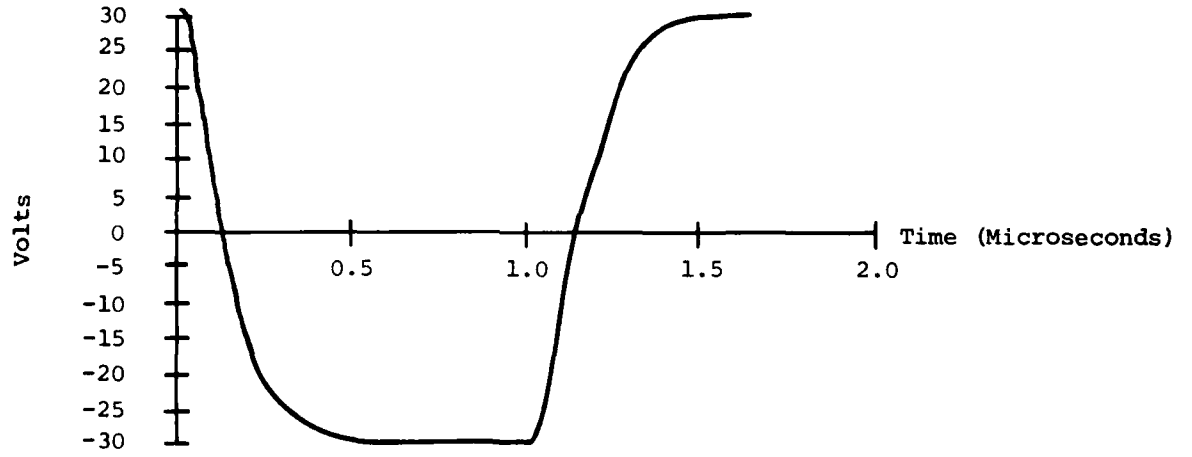


Figure 4-3. PIU CURRENT-LIMIT CONFIGURATION RESPONSE WITH 300-OHM LOAD

when the amplifier output begins to slew to -29.67 V in response to the input stimulus. It remains at this voltage until t = 1.022 μs, when it slews back to the initial value of +29.67 V. The simulation predicts that the current-limit configuration will not meet the requirement of ±30 V at 100 mA.

Slew rate, rise time, fall time, and bandwidth are derived in the same manner as for the unmodified amplifier model.

$S = 250\ V/\mu s$

$t_r = 259\ ns$

t_f = 220 ns

$B = \frac{0.35}{t_r}$ = 1.35 MHz

Figure 4-4 shows the simulation of current-limit operation into a 10-ohm load. Hard current-limiting occurs at 149.6 mA.

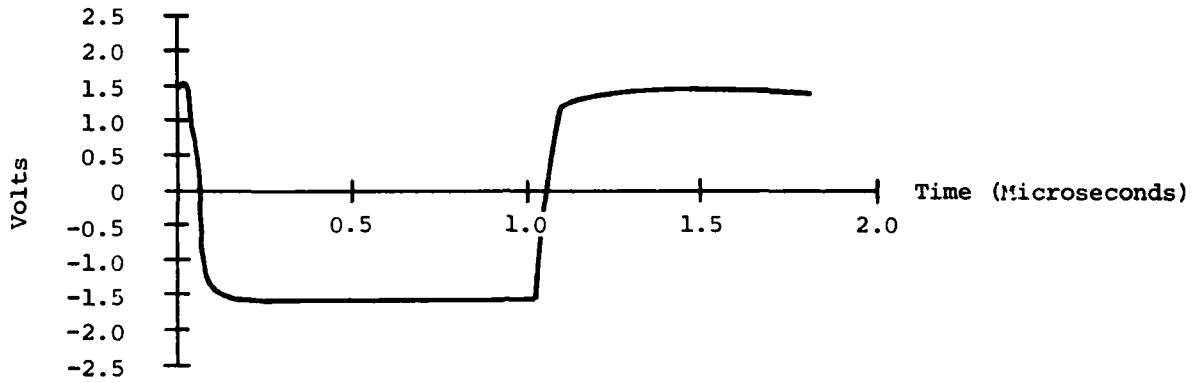


Figure 4-4. PIU CURRENT-LIMIT CONFIGURATION RESPONSE WITH 10-OHM LOAD

4.1.3 Transistor-Substitution Configuration

Figure 4-5 shows the output waveform of the transistor-substitution configuration model with a 300-ohm load. Initially, the output voltage is +30.21 V. At t = 12 ns, the output voltage slews to -30.21 V in response to the input stimulus. At t = 1.02 μs, the output slews back to its initial value of +30.21 V. At the 30-volt extremes of the waveform, the 300-ohm load draws 100 mA from the output of the amplifier. As with the unmodified configuration, the simulation predicts that this circuit will perform to the requirement of ±30 V output at 100 mA.

Slew rate, rise time, fall time, and bandwidth are derived in the same manner as for the unmodified amplifier model.

S = 285 V/μs

t_r = 190 ns

t_f = 160 ns

$B = \frac{0.35}{t_r}$ = 1.84 MHz

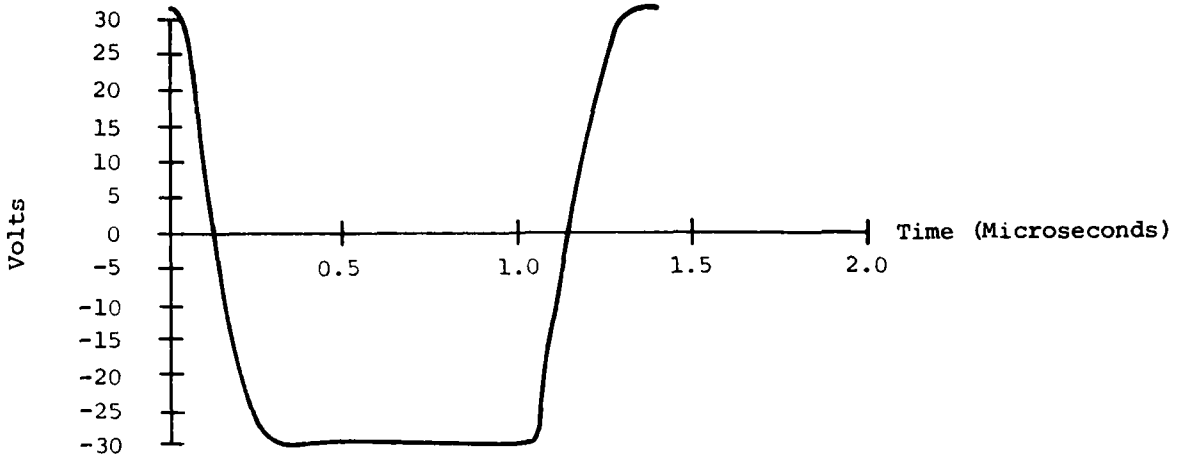


Figure 4-5. PIU TRANSISTOR-SUBSTITUTION CONFIGURATION RESPONSE WITH 300-OHM LOAD

Figure 4-6 shows the simulation results for the transistor-substitution configuration model connected to a 10-ohm load. Hard current limiting occurs at 265 mA.

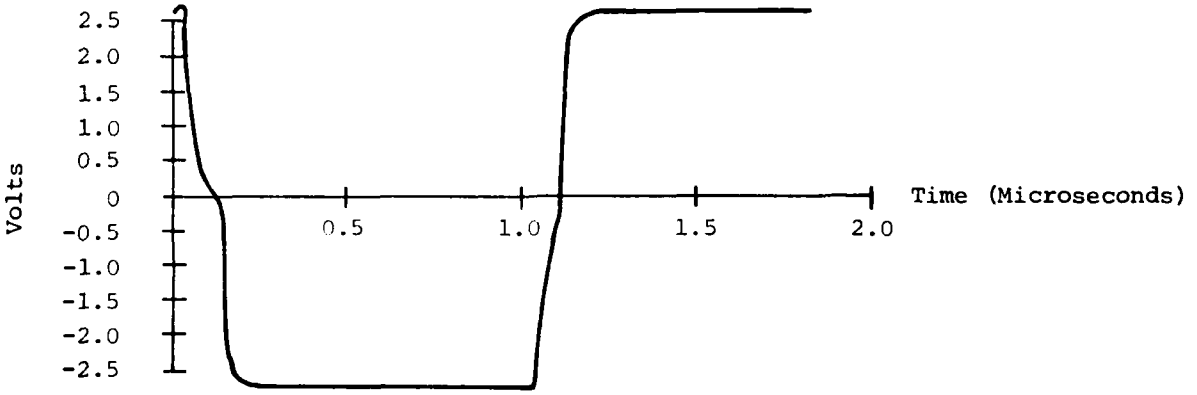


Figure 4-6. PIU TRANSISTOR-SUBSTITUTION CONFIGURATION RESPONSE WITH 10-OHM LOAD

4.1.4 Combined Configuration

Figure 4-7 shows the output waveform of the combined configuration model with a 300-ohm load. The initial value for the output voltage is +30.03 V. At t = 1 ns, the output slews to -30.03 V in response to the input stimulus. At t = 1.022 μs, the output voltage slews back to its

initial value of +30.03 V. This model predicts that the physical realization of this configuration will meet the requirement for ±30 V at 100 mA.

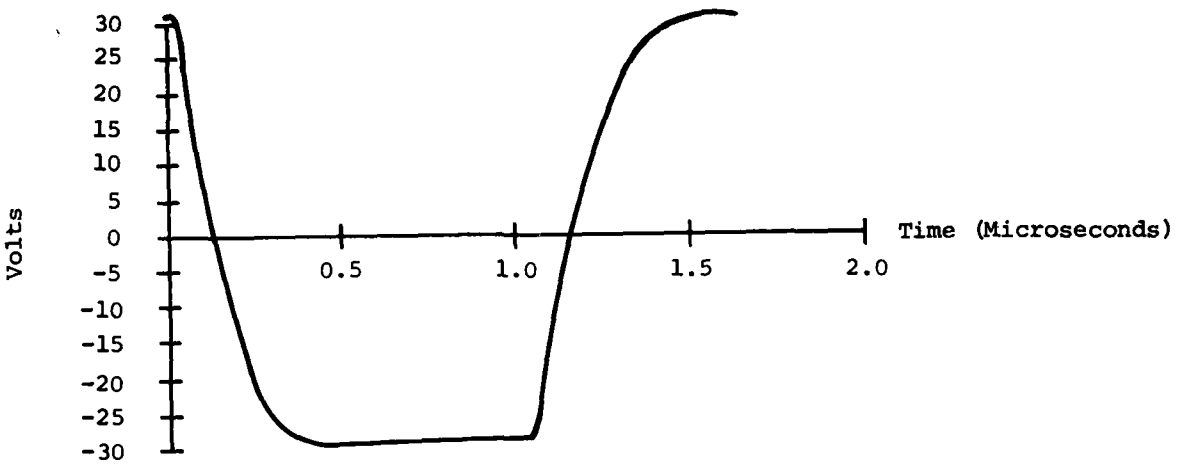


Figure 4-7. PIU COMBINED CONFIGURATION RESPONSE WITH 300-OHM LOAD

Slew rate, rise time, fall time, and bandwidth are derived from the data presented in Figure 4-7.

$S = 235\ V/\mu s$

$t_r = 280\ ns$

$t_f = 224\ ns$

$$B = \frac{0.35}{t_r} = 1.25\ MHz$$

Figure 4-8 shows the simulation results for the combined configuration model connected to a 10-ohm load. Hard current-limiting occurs at 160 mA.

4.2 THERMAL ANALYSIS

Application of the general thermal model described in Section 3.2 resulted in the specific models shown in Figure 4-9. These models were used to predict the ambient temperature at which device failure can be expected under low output, low load conditions. The results of the analysis are presented in Table 4-1.

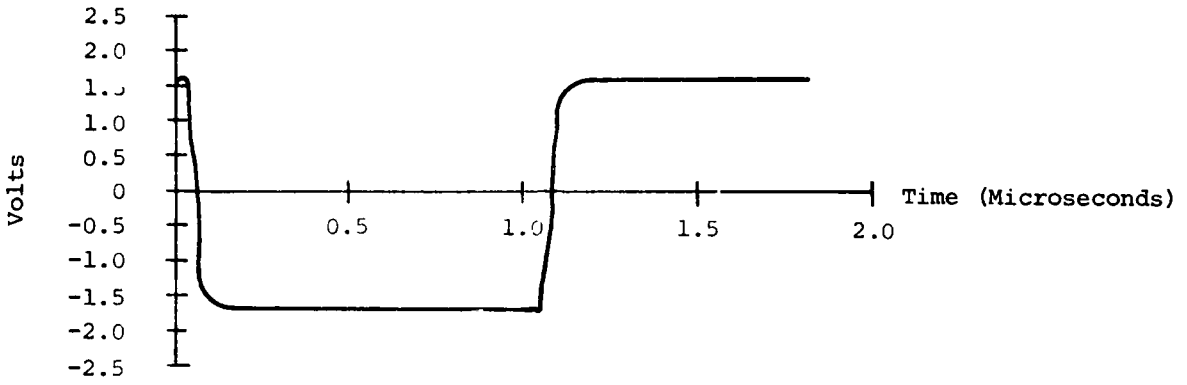


Figure 4-8. PIU COMBINED CONFIGURATION RESPONSE WITH 10-OHM LOAD

4.3 OPERATIONAL TEST RESULTS

4.3.1 DC Static Tests

DC static-test measurements revealed no major changes in the dc performance characteristics of the modified PIUs. There were no significant deviations in dc quiescent values nor any indication of severe offset problems. Correct amplitudes were generated in accordance with programmed dc modes.

4.3.2 Voltage Regulation Tests

The voltage regulation tests measured the ability of the modified PIUs to maintain constant amplitude from a no-load to full-load condition. The transistor-substitution configuration exhibited slightly better regulation than did the current-limit and combined configurations when driving a full load (300 ohms) in the 30 V mode. The results are tabulated in Table 4-2.

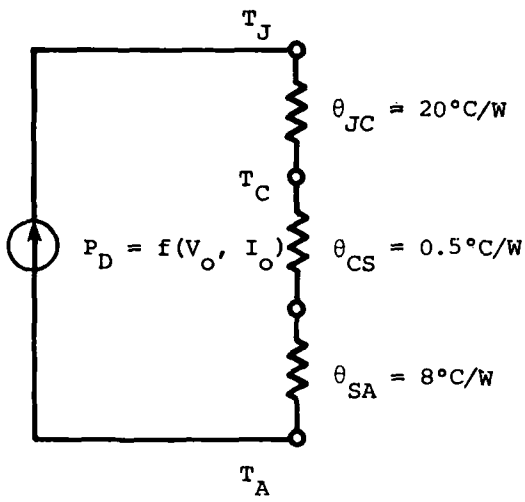
4.3.3 Transient Response Tests

Transient response test experiments consisting of time response and slew rate measurements indicated that all the PIU configurations meet or exceed specified values. Examination of recorded time response waveforms revealed slew rates better than 175 V/μs for the -0.6 gain and better than 100 V/μs for the -3 gain. The waveforms also indicated normal rise time, fall time, and settling time characteristics. These waveforms are presented in Figure 4-10.

4.3.4 Frequency and Bandwidth Tests

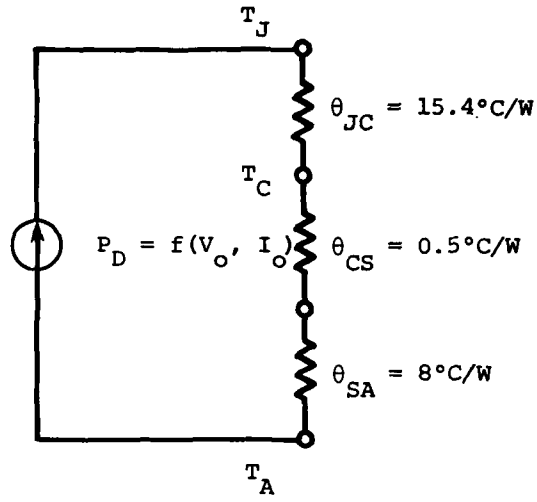
Frequency spectrum tests showed no major performance limitations in the frequency response and bandwidth characteristics of the modified circuits. The frequency response measurements indicated that 3 dB bandwidths are greater

D40/41D11 Transistor



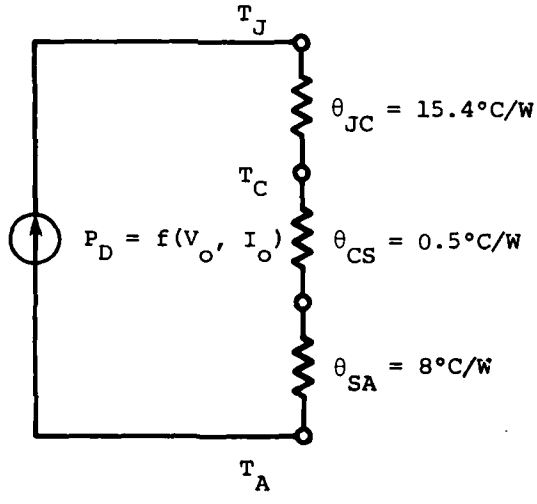
Current-Limit Configuration
(I_o max ≈ 120 mA)

D40/41E7 Transistor



Transistor-Substitution Configuration
(I_o max ≈ 220 mA)

D40/41E7 Transistor



Combined Configuration
(I_o max ≈ 120 mA)

Figure 4-9. APPLIED THERMAL MODELS

Table 4-1. MAXIMUM T_A BEFORE FAILURE FOR EACH CONFIGURATION (°C)*		
Current-Limit	Transistor-Substitution	Combined
83.5	47.6	93.1
*Conditions: T_J = 150°C, V_{prog} = 3.8 V, R_L = 0.		

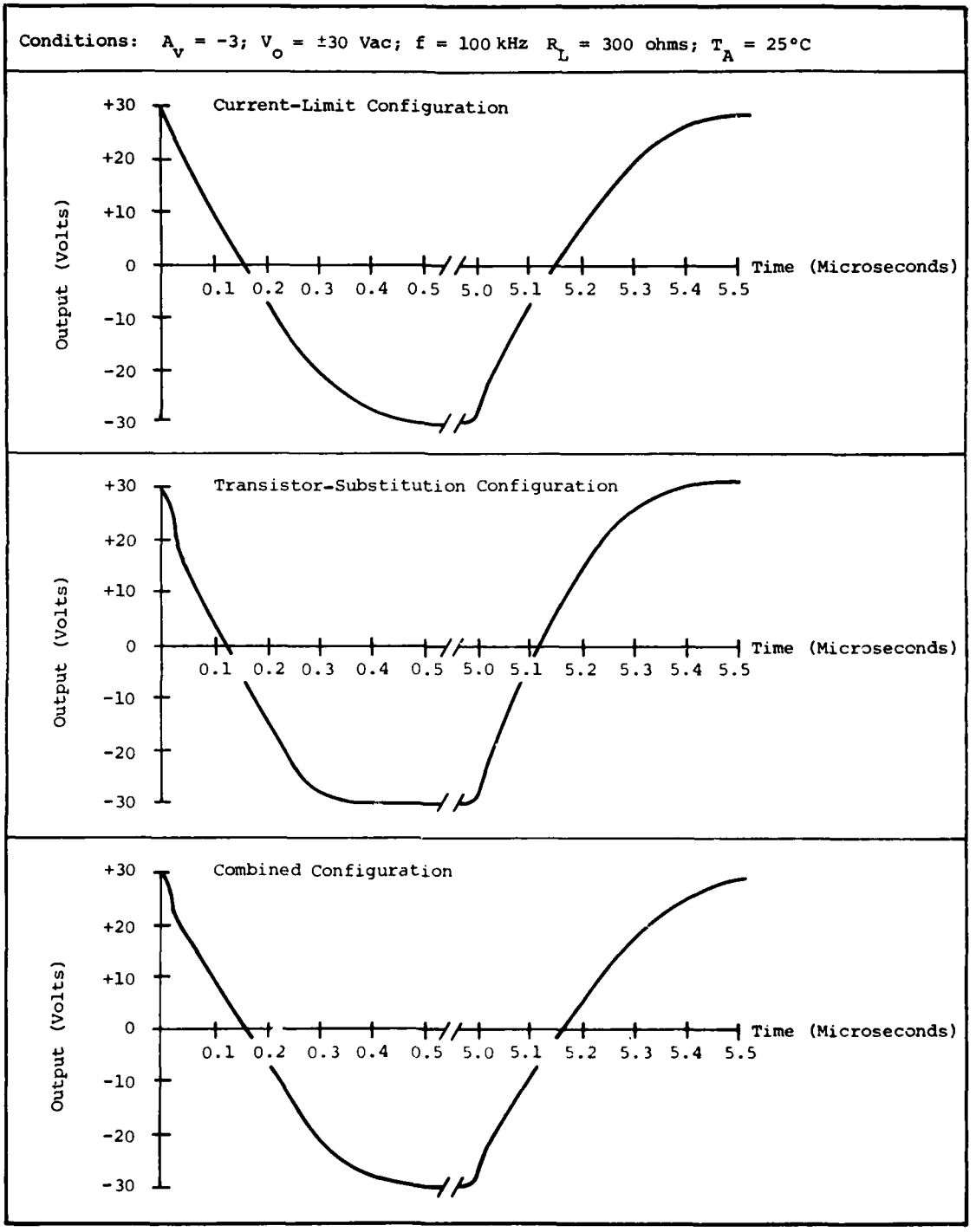
Table 4-2. RESULTS OF VOLTAGE REGULATION TESTS			
Configuration	V_O (R_L = 0 Ω) (Vdc)	V_O (R_L = 300 Ω) (Vdc)	Voltage Regulation (Percent)
Current-Limit	+30.7	+29.3	4.78
Transistor-Substitution	+30.7	+30.1	1.99
Combined	+30.7	+29.4	4.42

than 1 MHz for all three configurations. The spectrum test results are shown in Figure 4-11.

4.3.5 Current-Limit Tests

The design objective of reducing the maximum output current to 120 mA was essentially met by the circuit design change implemented in both the current-limit and combined PIU configurations. The transistor-substitution configuration remained at the 220 mA current-limit level. The current limiting characteristics of the three configurations are plotted in Figure 4-12, which compares the current-limit absolute values exhibited over the 5°C to 55°C ambient temperature range in voltage mode settings of +30 Vdc, -30 Vdc, +3.8 Vdc, and -3.8 Vdc. Examination of the figure reveals the following:

- The current-limit value is influenced by the temperature condition. Current limiting is maximum at low ambient temperatures and minimum at high ambient temperatures.
- Current limiting is maximum in the high-voltage-mode settings (+30 Vdc, -30 Vdc) and minimum in the low-voltage-mode settings (+3.8 Vdc, -3.8 Vdc). There was an average difference of 25 mA between the high- and low-voltage-mode settings.
- There were no significant differences in the current limit between the +30 Vdc and -30 Vdc high-voltage modes or between the +3.8 Vdc and -3.8 Vdc low-voltage modes.



(continued)

Figure 4-10. TRANSIENT RESPONSE MEASUREMENTS

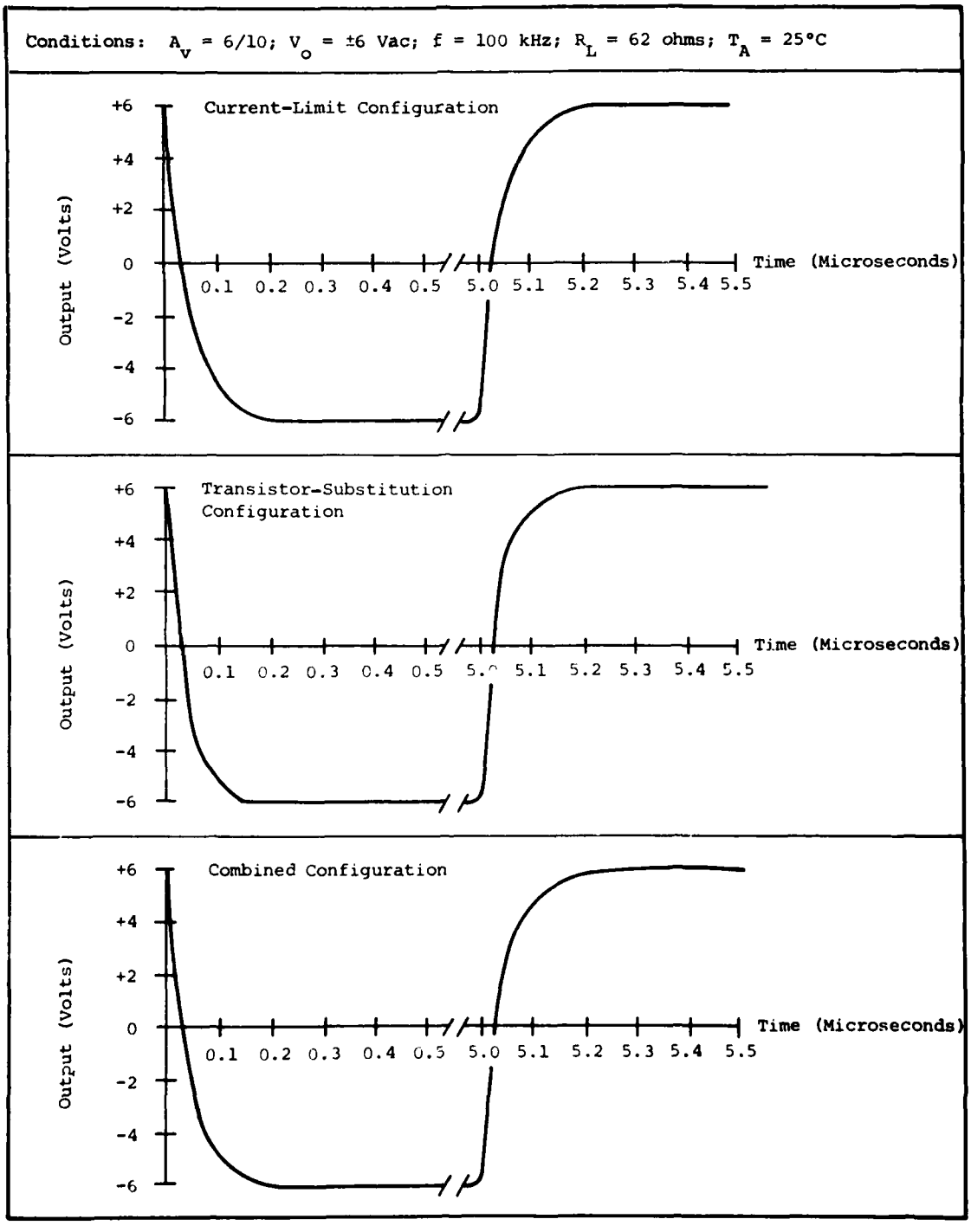


Figure 4-10. (continued)

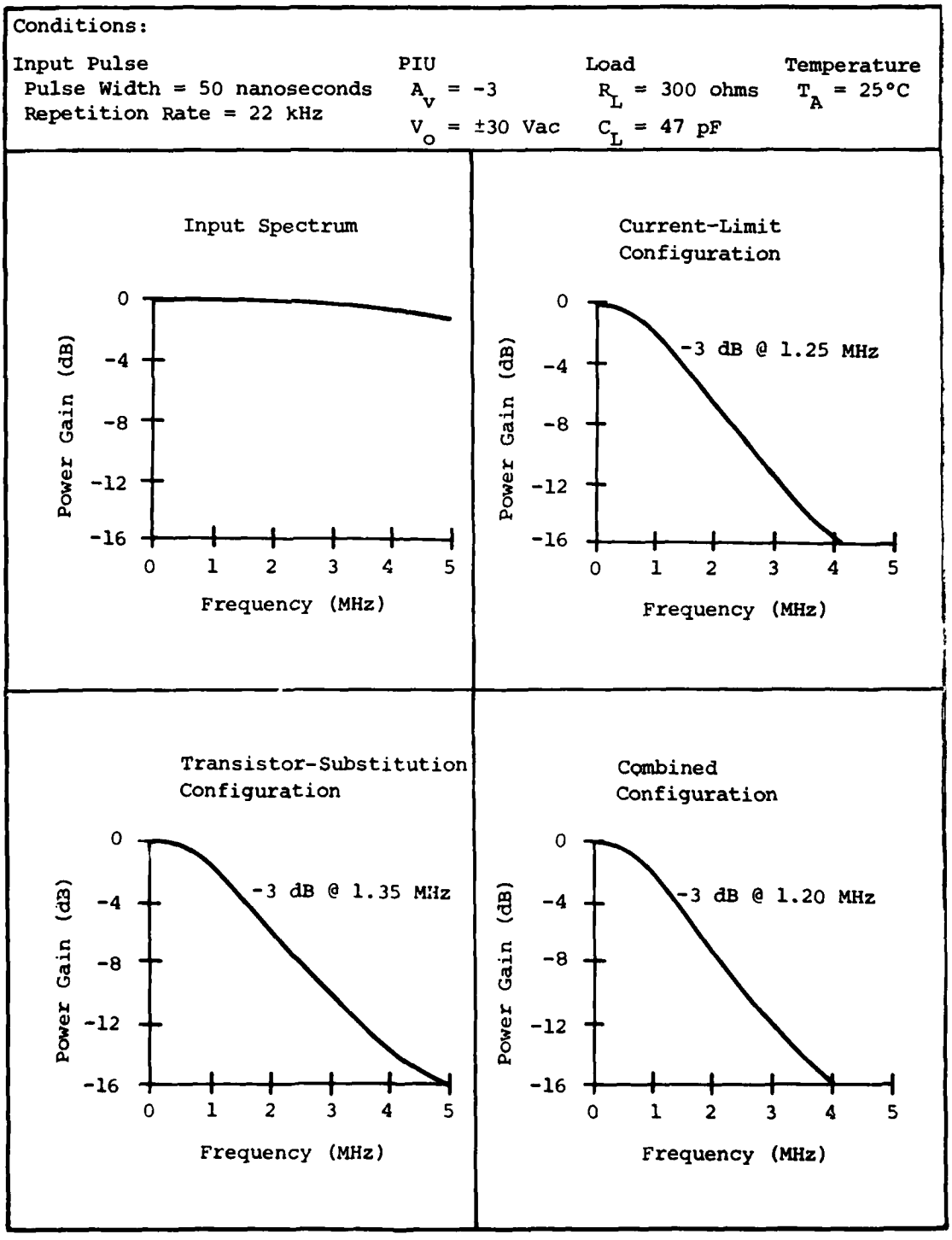


Figure 4-11. PIU FREQUENCY SPECTRUM TEST RESULTS

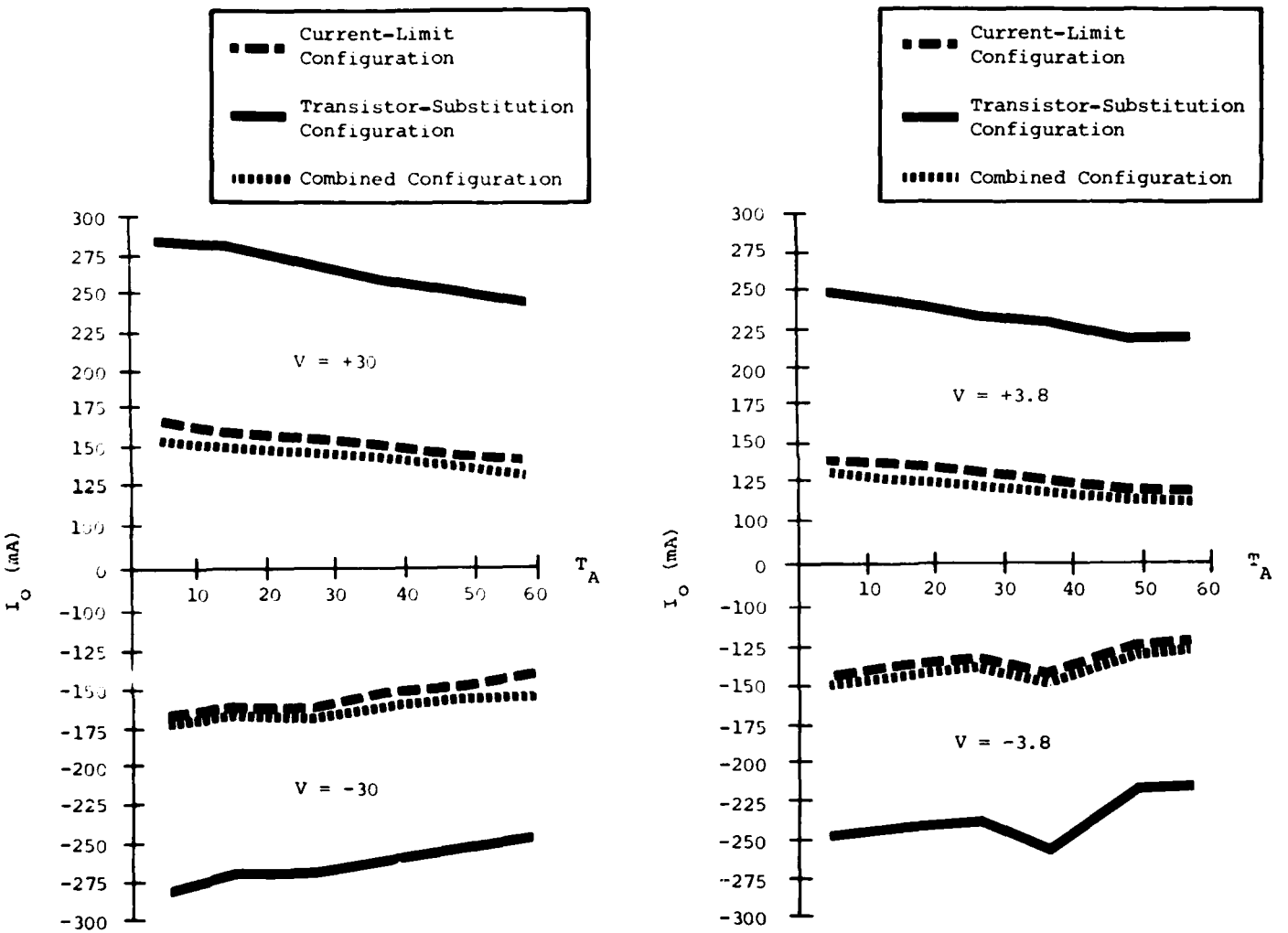


Figure 4-12. CURRENT-LIMIT TEST RESULTS

4.3.6 Test Summary

Table 4-3 is a comparative summary of experimental versus calculated circuit performance data. Examination of the data shows a close correlation between measured and expected results. Discrepancies are attributed to the fact that the SYSCAP II model used an ideal square wave input to the stimulus amplifier, whereas the actual input was somewhat less than ideal.

4.4 THERMAL TEST RESULTS

As described in Section 3.3.3, thermal data were recorded for PIU components under normal loading conditions. As expected, the three proposed configurations caused no significant thermal impact on the instrumented components under normal loading conditions. These data are tabulated for reference in Appendix C.

Each configuration was also tested under loading conditions that would drive the amplifier into the current-limiting mode of operation. The thermal performance of the power transistors was of primary interest. Figure 4-13 shows the transistor junction temperatures, which were derived from recorded case temperatures, plotted for each configuration on the same axis as the plot predicted by thermal calculations. These results confirm within experimental error the thermal performance predicted by the model described in Section 3.2.

Of the three proposed configurations, only the transistor-substitution configuration fails to provide safe power transistor operation through 70°C ambient temperature, which is the point at which other devices on the PIU begin to fail.

The data recorded under current-limit operating conditions are tabulated for reference in Appendix D.

Table 4-3. COMPARATIVE SUMMARY OF OPERATIONAL PERFORMANCE OF PIU CONFIGURATIONS

Performance Characteristics (T_A = 25°C)	Unmodified Configuration		Current-Limit Configuration		Transistor-Substitution Configuration		Combined Configuration	
	Calculated	Actual	Calculated	Actual	Calculated	Actual	Calculated	Actual
Maximum DC Output (R_L = 300 Ω)								
Voltage (V)	30.20	30.10	29.67	29.30	30.21	30.20	30.03	29.40
Current (mA)	100.67	100.33	98.90	97.67	100.70	100.67	100.10	98.00
Voltage Regulation								
No Load (V)	30.70	30.70	30.70	30.70	30.70	30.70	30.70	30.70
Full Load (V)	30.20	30.00	20.67	29.30	30.21	30.10	30.03	29.40
Regulation (%)	1.66	2.33	3.47	4.78	1.62	1.99	2.23	4.42
Current Limit (mA) (R_L = 10 Ω)	220	230	120	131	220	235	120	123
Frequency and Transient Response (A_v = -3)								
Slew Rate (V/μs)	308	200	250	143	285	187	235	136
Rise Time (ns)	159	250	259	320	190	270	280	340
Fall Time (ns)	150	240	220	300	160	245	224	310
Bandwidth (MHz)	2.20	1.40	1.35	1.25	1.84	1.35	1.25	1.20

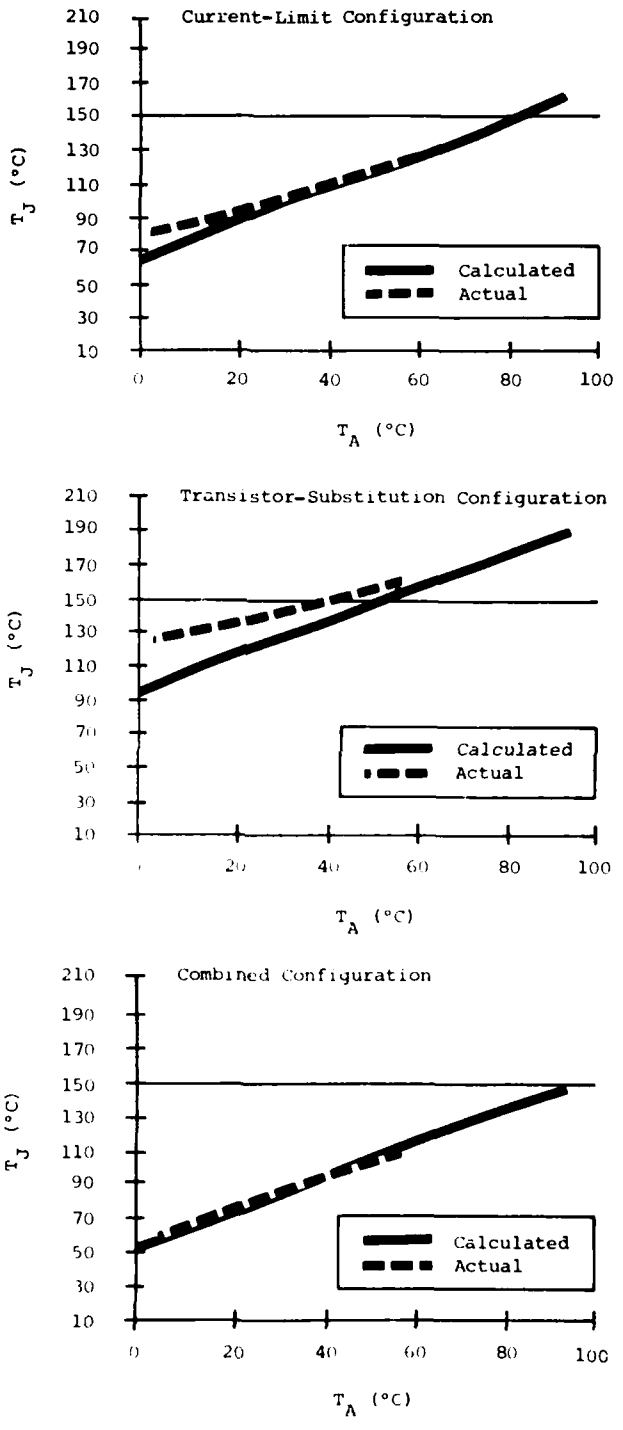


Figure 4-13. COMPARISON OF THERMAL RESULTS

CHAPTER FIVE

COMPARATIVE ANALYSIS

5.1 COST FACTORS

When any of the three proposed configurations are applied to a PIU card (which consists of two complete stimulus buffer amplifiers), it is assumed that costs for drawing changes, acceptance testing, and logistic support will be equal. Two factors were considered in our comparative analysis -- parts cost and labor cost. The following assumptions were made:

- The cost for each resistor required for the current-limit configuration is $0.10. Since eight resistors are required to modify a PIU, the total parts cost per modification is $0.80.
- The cost for each transistor required for the transistor-substitution configuration is $2.00. Since eight transistors are required to modify a PIU, the total parts cost per modification is $16.00.
- The cost per man-hour is $35.00.
- The estimated man-hours required to modify a complete PIU are as follows:
  - Current-limit configuration - 2 hours
  - Transistor-substitution configuration - 3 hours
  - Combined configuration - 5 hours

The cost for each configuration is thus determined by the following equation:

$$C = P + (H \times R)$$

where

C = modification cost per PIU card

P = parts cost per PIU card

H = man-hours required to remove and install parts per PIU card

R = cost per man-hour

Applying the equation to each proposed configuration yields the results shown in Table 5-1.

Table 5-1. COST FACTORS

Configuration	Cost per PIU Card (Dollars)		
	Parts	Labor	Total
Current-Limit	0.80	70.00	70.80
Transistor-Substitution	16.00	105.00	121.00
Combined	16.80	175.00	191.80

5.2 PERFORMANCE FACTORS

Table 5-2 presents the significant electrical and thermal performance parameters for each proposed configuration, along with the specified performance and the performance of the unmodified PIU.

Table 5-2. COMPARATIVE PERFORMANCE OF PIU CONFIGURATIONS WITH SPECIFICATION

Parameters	Specification	Unmodified	Current-Limit Configuration	Transistor-Substitution Configuration	Combined Configuration
Maximum DC Output (R_L = 300 Ω)					
Voltage (V)	30.00 minimum	30.10	29.30	30.20	29.40
Current (mA)	100.00 minimum	100.33	97.67	100.67	98.00
Slew Rate (V/μs)	100 minimum	200	143	187	136
Rise Time (ns)	350 maximum	250	320	270	340
Fall Time (ns)	350 maximum	240	300	245	310
Bandwidth (MHz)	1.00 minimum	1.40	1.25	1.35	1.20
Maximum Allowable T_A (°C)	--	28.70	83.20	47.60	93.10

With respect to thermal performance, these data indicate that, of the three proposed configurations, the transistor-substitution configuration is the only one that will not provide enough improvement to eliminate the power transistors as being a reliability problem on the PIU card. There is very little difference in thermal performance between the current-limit configuration and the combined configuration, and both provide adequate thermal protection for the power transistors.

With respect to electrical performance, both the current-limit and combined configurations meet or exceed requirements with the exception of voltage and current amplitudes. Voltage and current amplitude degradation is less than 5 percent in each configuration.

5.3 CONCLUSIONS

The analyses led to the following conclusions:

- It is possible to limit the output current of the stimulus buffer amplifier to 120 mA without changing circuit wiring or printed circuit board layout. The actual value of the current limit is temperature-dependent.
- Operational and thermal laboratory test results for each proposed configuration confirm the performance predicted by analytical techniques.
- The transistor-substitution configuration does not degrade electrical performance but does not increase the ambient temperature operating range enough to eliminate the power transistors as being a reliability problem when low output, low load conditions occur.
- Both the current-limit configuration and the combined configuration provide the required improvement in ambient temperature operating range. However, each of these configurations causes a slight degradation from specified output voltage and current levels.
- Of the thermally acceptable configurations, the current-limit configuration is the least costly. There is no other significant difference between the current-limit configuration and the combined configuration.

5.4 RECOMMENDATIONS

The specification for output voltage and current should be reviewed to determine its criticality. If these parameters are sufficiently flexible, either the current-limit configuration or the combined configuration can be considered as a solution to transistor thermal failure. However, the current-limit configuration should be given primary consideration because of its lower cost.

If the output amplitude specification is inflexible, additional testing of the current-limit configuration to transistor thermal failure should be conducted to determine whether the following trade-offs are feasible:

- Current limiting at a value greater than 120 mA but still low enough to offer substantial thermal protection for the power transistors
- Slight increase in the gain of the amplifier to meet output amplitude requirements in the current-limit configuration

APPENDIX A

SYSCAP II MODEL LISTINGS

This appendix presents ARINC Research model listings used with the SYSCAP II in the operational analysis of the PIU configuration.

Unmodified PIU Model

```
00100 TRACAP,SKIP
00110 PIU AMPLIFIER TRANSIENT ANALYSIS
00120 R50(6,7) 3.32K
00130 R53(2,G) 56K
00140 R51(1,G) 56K
00150 R58(3,4) 4.99K
00160 R57(3,4) 4.99K
00170 R52(5,4) 10K
00180 R49(6,5) 39
00190 R54(12,15) 750
00200 R55(8,10) 10K
00210 R56(8,9) 560
00220 R60(9,10) 10K
00230 R59(13,15) 750
00240 R61(14,16) 15K
00250 R62(14,G) 220
00260 R63(15,24) 2.49K
00270 R64(24,G) 15.4K
00280 R65(20,G) 15K
00290 R66(22,23) 511
00300 R67(26,28) 10
00310 R68(25,10) 511
00320 R69(19,G) 1K
00330 R70(30,31) 220
00340 R71(31,4) 100
00350 R72(4,32) 100
00360 R73(32,33) 220
00370 R85(3,6) 400K
00380 R86(3,G) 10
00390 R74(34,4) 12
00400 R75(27,4) 12
00410 R76(35,4) 12
00420 R77(36,4) 12
00430 R78(4,11) 100
00440 R79(16,17) 3.1K
00450 R80(18,16) 6.9K
00460 C50(6,4) 3.6P
00470 C52(3,4) 5.75P
00480 C53(14,G) .01U
00490 C61(15,G) 4.7U
00500 C57(15,G) .01U
00510 C62(10,G) 4.7U
00520 C58(10,G) .01U
00530 C55(29,19) 6.25P
00540 C56(25,10) 10P
00550 C59(4,G) 10P
00560 C60(11,G) 330P
00570 C54(20,G) .01U
00580 R83(2,1) 10MEG
00590 R84(1,10) 10MEG
00600 DZ50(A22,C21)1N973B
00610 DDUM(A37,C28)1N5712
00620 D51(A23,C10) 1N4454
00630 D52(A29,C37)1N5712
00640 Q50A,NPN(B6,C12,E8) 2N2920
00650 Q50B,NPN(B14,C13,E9)2N2920
00660 Q53,NPN(B24,C15,E20)2N3904
00670 Q56,NPN(B31,C29,E4)2N3904
00680 EM40(+G,-10)40,RS=1.0
00690 EP40(+15,-G)40,RS=1.0
00700 EM15(+G,-18)15,RS=1.0
00710 EP15(+17,-G)15,RS=1.0
00720 ED0(+G,-7)10,RS=1.0
00730 IS(R6,FG)I,PULSE,RI=1E6,0,6.024M,10N,10N,1.0U,10N,10U
```

```
00740 *THE 2N3806 IS NOT IN THE DATABANK.SUBBING THE 2N3810 IN Q54A & B.
00750 Q54A,PNP(B20,C21,E13) 2N3810
00760 Q54B,PNP(B20,C29,E12)2N3810
00770 *PARAMETERS FOR FOLLOWING QS SUPPLIED BY ROCKWELL.
00780 Q55,NPN(B22,C26,E25) NOM
00790 370,90M,0.3621,0.2M,0.4054,0.175,1,4.101,0.6006,6.006M,
00800 2.693E-11,1.366,5.406G,80,10M,40.54,7.05P,0.75,0.33,0.3623U,0,0,0,0,
00910 5.305E-12,1.205,0.5403G,7.059,10M,3.305,19.36P,0.75,0.5,530.8P,0,0,0,0
00920 Q58,NPN(B29,C15,E30) NOM
00830 370,90M,0.3621,0.2M,0.4054,0.175,1,4.101,0.6006,6.006M,
00840 2.693E-11,1.366,5.406G,80,10M,40.54,7.05P,0.75,0.33,0.3623U,0,0,0,0,
00850 5.305E-12,1.205,0.5403G,7.059,10M,3.305,19.36P,0.75,0.5,530.8P,0,0,0,0
00860 Q59,PNP(B26,C10,E33) NOM
00870 163,7M,0.8222,0.3M,0.4294,0.17,1,3.603,0.6435,6.435M,
00880 1.157E-13,1.1,7.2G,106.7,10M,42.36,9.401P,0.75,0.33,0.2189U,0,0,0,0,
00890 8.977E-15,1,0.45G,5.882,10M,2.121,23.24P,0.75,0.5,0.5308N,0,0,0,0
00900 Q60,NPN(B30,C15,E34)IE,P, NOM
00910 215.1,40M,0.7033,1M,0.279,0.8,1,1.357,0.3874,3.874M,
00920 2.573E-10,1.654,67.51MEG,100,10M,57.22,19.26P,.75,.33,.1445U,0,0,0,0,
00930 1.835E-10,1.503,4.501MEG,5.882,10M,3.302,10.33P,.75,.5,.7962N,0,0,0,0
00940 Q61,PNP(B33,C10,E27)IE,P, NOM
00950 200,20M,0.7565,1M,0.1499,0.9,1,1.501,0.9009,9.009M,
00960 4.475E-9,1.929,67.64MEG,100,10M,68.4,24.08P,.75,.33,54.23N,0,0,0,0,
00970 2.37E-9,1.754,4.511MEG,5.882,10M,3.856,12.91P,.75,.5,1.062N,0,0,0,0
00980 Q62,NPN(B30,C15,E35)IE,P, NOM
00990 215.1,40M,0.7033,1M,0.279,0.8,1,1.357,0.3874,3.874M,
01000 2.573E-10,1.654,67.51MEG,100,10M,57.22,19.26P,.75,.33,.1445U,0,0,0,0,
01010 1.835E-10,1.503,4.501MEG,5.882,10M,3.302,10.33P,.75,.5,.7962N,0,0,0,0
01020 Q63,PNP(B33,C10,E36)IE,P, NOM
01030 200,20M,0.7565,1M,0.1499,0.9,1,1.501,0.9009,9.009M,
01040 4.475E-9,1.929,67.64MEG,100,10M,68.4,24.08P,.75,.33,54.23N,0,0,0,0,
01050 2.37E-9,1.754,4.511MEG,5.882,10M,3.856,12.91P,.75,.5,1.062N,0,0,0,0
01060 Q57,PNP(B32,C26,E4) NOM
01070 200,10M,0.7691,0.1M,0.15,0.15,1,2.782,1.982,19.82M,
01080 3.73E-10,1.757,3.627G,53.33,10M,31.18,5.288P,0.75,0.33,0.1753U,0,0,0,0,
01090 8.494E-11,1.597,0.4513G,5.882,10M,3.165,7.746P,0.75,0.5,0.3185N,0,0,0,0
01100 *RL IS THE LOAD RESISTOR.
01110 RL(4,0)1,300
01120 FINIS
1130 TIME=10N,4.0U
01140 PLOT=ISII,NODE4
```

Current-Limit PIU Model

```
00100 TRACAP.SKIP
00110 PIU AMPLIFIER TRANSIENT ANALYSIS
00120 R50(6,7) 3.32K
00130 R53(2,6) 56K
00140 R51(1,6) 56K
00150 R58(3,4) 4.99K
00160 R57(3,4) 4.99K
00170 R52(5,4) 10K
00180 R49(6,5) 39
00190 R54(12,15) 750
00200 R55(8,10) 10K
00210 R56(8,9) 560
00220 R60(9,10) 10K
00230 R59(13,15) 750
00240 R61(14,16) 15K
00250 R62(14,6) 220
00260 R63(15,24) 2.49K
00270 R64(24,6) 15.4K
00280 R65(20,6) 15K
00290 R66(22,23) 511
00300 R67(26,28) 10
00310 R68(25,10) 511
00320 R69(19,6) 1K
00330 R70(30,31) 180
00340 R71(31,4) 150
00350 R72(4,32) 150
00360 R73(32,33) 180
00370 R85(3,6) 400K
00380 R86(3,6) 10
00390 R74(34,4) 12
00400 R75(27,4) 12
00410 R76(35,4) 12
00420 R77(36,4) 12
00430 R78(4,11) 100
00440 R79(16,17) 3.1K
00450 R80(18,16) 6.9K
00460 C50(6,4) 3.6P
00470 C52(3,4) 5.75P
00480 C51(14,6) .01U
00490 C61(15,6) 4.7U
00500 C57(15,6) .01U
00510 C62(10,6) 4.7U
00520 C58(10,6) .01U
00530 C55(29,19) 6.25P
00540 C56(25,10) 10P
00550 C59(4,6) 10P
00560 C60(11,6) 390P
00570 C54(20,6) .01U
00580 R83(2,1) 10MEG
00590 R84(1,10) 10MEG
00600 DC50(A22,C21)1N973B
00610 DIUM(A37,C28)1N5712
00620 D51(A23,C10) 1N4454
00630 D52(A29,C37)1N5712
00640 Q50A(NPN)(B6,C12,E8) 2N2920
00650 Q50B(NPN)(B14,C13,E9)2N2920
00660 Q53(NPN)(B24,C15,E20)2N3904
00670 Q5E(NPN)(B31,C29,E4)2N3904
00680 EM40(+6,-10)40,PI=1.0
00690 EP40(+15,-6)40,PI=1.0
00700 EM15(+6,-18)15,PI=1.0
00710 EP15(+17,-6)15,PI=1.0
00720 ED0(+6,-7)10,PI=1.0
00730 I(R6,FG)I,PULSE,PI=1E6,0,6.024M,10N,10N,1.0U,10N,10U
```

```
00740 *THE 2N3806 IS NOT IN THE DATABANK.SUBBING THE 2N3810 IN 054A & B.
00750 054A,PNP(B20,C21,E13) 2N3810
00760 054B,PNP(B20,C29,E12)2N3810
00770 *PARAMETERS FOR FOLLOWING QS SUPPLIED BY ROCKWELL.
00780 055,NPN(B22,C26,E25) NOM
00790 370,90M,0.3621,0.2M,0.4054,0.175,1,4.101,0.6006,6.006M,
00800 2.693E-11,1.366,5.406G,80,10M,40.54,7.05P,0.75,0.33,0.3623U,0,0,0,0,
00810 5.305E-12,1.205,0.5403G,7.059,10M,3.305,19.36P,0.75,0.5,530.8P,0,0,0,0
00820 058,NPN(B29,C15,E30) NOM
00830 370,90M,0.3621,0.2M,0.4054,0.175,1,4.101,0.6006,6.006M,
00840 2.693E-11,1.366,5.406G,80,10M,40.54,7.05P,0.75,0.33,0.3623U,0,0,0,0,
00850 5.305E-12,1.205,0.5403G,7.059,10M,3.305,19.36P,0.75,0.5,530.8P,0,0,0,0
00860 059,PNP(B26,C10,E33) NOM
00870 163,7M,0.8222,0.3M,0.4294,0.17,1,3.603,0.6435,6.435M,
00880 1.157E-13,1.1,7.2G,106.7,10M,42.36,9.401P,0.75,0.33,0.2189U,0,0,0,0,
00890 8.977E-15,1,0.456G,5.882,10M,2.121,23.24P,0.75,0.5,0.5308N,0,0,0,0
00900 060,NPN(B30,C15,E34)IE,P, NOM
00910 215.1,40M,0.7033,1M,0.279,0.8,1,1.357,0.3874,3.874M,
00920 2.573E-10,1.654,67.51MEG,100,10M,57.22,19.26P,.75,.33,.1445U,0,0,0,0,
00930 1.835E-10,1.503,4.501MEG,5.882,10M,3.302,10.33P,.75,.5,.7962N,0,0,0,0
00940 061,PNP(B33,C10,E27)IE,P, NOM
00950 200,20M,0.7565,1M,0.1499,0.9,1,1.501,0.9009,9.009M,
00960 4.475E-9,1.929,67.64MEG,100,10M,68.4,24.08P,.75,.33,54.23N,0,0,0,0,
00970 2.37E-9,1.754,4.511MEG,5.882,10M,3.856,12.91P,.75,.5,1.062N,0,0,0,0
00980 062,NPN(B30,C15,E35)IE,P, NOM
00990 215.1,40M,0.7033,1M,0.279,0.8,1,1.357,0.3874,3.874M,
01000 2.573E-10,1.654,67.51MEG,100,10M,57.22,19.26P,.75,.33,.1445U,0,0,0,0,
01010 1.835E-10,1.503,4.501MEG,5.882,10M,3.302,10.33P,.75,.5,.7962N,0,0,0,0
01020 063,PNP(B33,C10,E36)IE,P, NOM
01030 200,20M,0.7565,1M,0.1499,0.9,1,1.501,0.9009,9.009M,
01040 4.475E-9,1.929,67.64MEG,100,10M,68.4,24.08P,.75,.33,54.23N,0,0,0,0,
01050 2.37E-9,1.754,4.511MEG,5.882,10M,3.856,12.91P,.75,.5,1.062N,0,0,0,0
01060 057,PNP(B32,C26,E4) NOM
01070 200,10M,0.7691,0.1M,0.15,0.15,1,2.782,1.982,19.82M,
01080 3.73E-10,1.757,3.627G,53.33,10M,31.18,5.288P,0.75,0.33,0.1753U,0,0,0,0,
01090 8.494E-11,1.597,0.4513G,5.882,10M,3.165,7.746P,0.75,0.5,0.3185N,0,0,0,0
01100 *RL IS THE LOAD RESISTOR.
01110 RL(4,0)1,300
01120 FINIS
1130 TIME=10N,4.0U
01140 PLOT=I(1),NODE4
```

Transistor-Substitution PIU Model

```
00100 TRACAP
00110 PIU AMPLIFIER TRANSIENT ANALYSIS
00120 R50(6,7) 3.32K
00130 R53(2,G) 56K
00140 R51(1,G) 56K
00150 R58(3,4) 4.99K
00160 R57(3,4) 4.99K
00170 R52(5,4) 10K
00180 R49(6,5) 39
00190 R54(12,15) 750
00200 R55(8,10) 10K
00210 R56(8,9) 560
00220 R60(9,10) 10K
00230 R59(13,15) 750
00240 R61(14,16) 15K
00250 R62(14,G) 220
00260 R63(15,24) 2.49K
00270 R64(24,G) 15.4K
00280 R65(20,G) 15K
00290 R66(22,23) 511
00300 R67(26,29) 10
00310 R68(25,10) 511
00320 R69(19,G) 1K
00330 R70(30,31) 220
00340 R71(31,4) 100
00350 R72(4,32) 100
00360 R73(32,33) 220
00370 R85(3,6) 400K
00380 R86(3,G) 10
00390 R74(34,4) 12
00400 R75(27,4) 12
00410 R76(35,4) 12
00420 R77(36,4) 12
00430 R78(4,11) 100
00440 R79(16,17) 3.1K
00450 R80(18,16) 6.9K
00460 C50(6,4) 3.6P
00470 C52(3,4) 5.75P
00480 C53(14,G) .01U
00490 C61(15,G) 4.7U
00500 C57(15,G) .01U
00510 C62(10,G) 4.7U
00520 C58(10,G) .01U
00530 C55(29,19) 6.25P
00540 C56(25,10) 10P
00550 C59(4,G) 10P
00560 C60(11,G) 390P
00570 C54(20,G) .01U
00580 R83(2,1) 10MEG
00590 R84(1,10) 10MEG
00600 DZ50(A22,C21)1N973B
00610 DDUM(A37,C28)1N5712
00620 D51(A23,C10) 1N4454
00630 D52(A29,C37)1N5712
00640 Q50A,NPN(B6,C12,E8) 2N2920
00650 Q50B,NPN(B14,C13,E9)2N2920
00660 Q53,NPN(B24,C15,E20)2N3904
00670 Q56,NPN(B31,C29,E4)2N3904
00680 EM40(+6,-10)40,RS=1.0
00690 EP40(+15,-6)40,RS=1.0
00700 EM15(+6,-18)15,RS=1.0
00710 EP15(+17,-6)15,RS=1.0
```

```
00720 ED0(+6,-7)10,RS=1.0
00730 IS(R6,FG)I,PULSE,RI=1E6,0,6.024M,10N,10N,1.0U,10N,10U
00740 *THE 2N3806 IS NOT IN THE DATABANK.SUBBING THE 2N3810 IN Q54A & B.
00750 Q54A,PNP(B20,C21,E13) 2N3910
00760 Q54B,PNP(B20,C29,E12)2N3810
00770 *PARAMETERS FOR FOLLOWING QS SUPPLIED BY ROCKWELL.
00780 Q55,NPN(B22,C26,E25) NOM
00790 370,90M,0.3621,0.2M,0.4054,0.175,1,4.101,0.6006,6.006M,
00800 2.693E-11,1.366,5.406G,80,10M,40.54,7.05P,0.75,0.33,0.3623U,0,0,0,0,
00810 5.305E-12,1.205,0.5403G,7.059,10M,3.305,19.36P,0.75,0.5,530.8P,0,0,0,0
00820 Q59,NPN(B29,C15,E30) NOM
00830 370,90M,0.3621,0.2M,0.4054,0.175,1,4.101,0.6006,6.006M,
00840 2.693E-11,1.366,5.406G,80,10M,40.54,7.05P,0.75,0.33,0.3623U,0,0,0,0,
00850 5.305E-12,1.205,0.5403G,7.059,10M,3.305,19.36P,0.75,0.5,530.8P,0,0,0,0
00860 Q59,PNP(B26,C10,E33) NOM
00970 163,7M,0.8222,0.3M,0.4294,0.17,1,3.603,0.6435,6.435M,
00880 1.157E-13,1.1,7.2G,106.7,10M,42.36,9.401P,0.75,0.33,0.2189U,0,0,0,0,
00890 8.977E-15,1,0.45G,5.882,10M,2.121,23.24P,0.75,0.5,0.5308N,0,0,0,0
00900 Q60,NPN(B30,C15,E34)IE,P, NOM
00910  230,60M,0.9131,10M,0.1304,1,1,2.574,0.2369,2.369M,
00920  1.658E-9,1.654,9.735G,133.3,10M,85.4,21.67P,.75,.33,0.2906U,0,0,0,0,
00930  1.421E-9,1.503,0.5245G,5.882,10M,3.731,11.62P,.75,.5,0.6923N,0,0,0,0
00970 Q61,PNP(B33,C10,E27)IE,P, NOM
00980  220,40M,0.95,10M,0.1364,1.3,1,2.973,0.2721,2.721M,
00990  1.155E-12,1.1,9G,133.3,10M,58.27,31.3P,.75,.33,0.1806U,0,0,0,0,
01000  3.297E-13,1,0.45G,5.882,10M,2.437,16.78P,.75,.5,0.9099N,0,0,0,0
01040 Q62,NPN(B30,C15,E35)IE,P, NOM
01050  230,60M,0.9131,10M,0.1304,1,1,2.574,0.2369,2.369M,
01060  1.658E-9,1.654,9.735G,133.3,10M,85.4,21.67P,.75,.33,0.2906U,0,0,0,0,
01070  1.421E-9,1.503,0.5245G,5.882,10M,3.731,11.62P,.75,.5,0.6923N,0,0,0,0
01080 Q63,PNP(B33,C10,E36)IE,P, NOM
01090  220,40M,0.95,10M,0.1364,1.3,1,2.973,0.2721,2.721M,
01100  1.155E-12,1.1,9G,133.3,10M,58.27,31.3P,.75,.33,0.1806U,0,0,0,0,
01110  3.297E-13,1,0.45G,5.882,10M,2.437,16.78P,.75,.5,0.9099N,0,0,0,0
01120 Q57,PNP(B32,C26,E4) NOM
01130 200,10M,0.7691,0.1M,0.15,0.15,1,2.782,1.982,19.82M,
01140 3.73E-10,1.757,3.627G,53.33,10M,31.18,5.288P,0.75,0.33,0.1753U,0,0,0,0,
01150 8.494E-11,1.597,0.4513G,5.882,10M,3.165,7.746P,0.75,0.5,0.3185N,0,0,0,0
01160 *RL IS THE LOAD RESISTOR.
01170 RL(4,0)I,300
01180 FINIS
01190 TIME=10N,4.0U
01200 PLOT=ISII,NODE4
```

Combination PIU Model

```
00100 TRACAP,SKIP
00110 PIU AMPLIFIER TRANSIENT ANALYSIS
00120 R50(6,7) 3.32K
00130 R53(2,6) 56K
00140 R51(1,6) 56K
00150 R58(3,4) 4.99K
00160 R57(3,4) 4.99K
00170 R52(5,4) 10K
00180 R49(6,5) 39
00190 R54(12,15) 750
00200 R55(8,10) 10K
00210 R56(9,9) 560
00220 R60(9,10) 10K
00230 R59(13,15) 750
00240 R61(14,16) 15K
00250 R62(14,6) 220
00260 R63(15,24) 2.49K
00270 R64(24,6) 15.4K
00280 R65(20,6) 15K
00290 R66(22,23) 511
00300 R67(26,28) 10
00310 R68(25,10) 511
00320 R69(19,6) 1K
00330 R70(30,31) 180
00340 R71(31,4) 150
00350 R72(4,32) 150
00360 R73(32,33) 180
00370 R85(3,6) 400K
00380 R86(3,6) 10
00390 R74(34,4) 12
00400 R75(27,4) 12
00410 R76(35,4) 12
00420 R77(36,4) 12
00430 R78(4,11) 100
00440 R79(16,17) 3.1K
00450 R80(18,16) 6.9K
00460 C50(6,4) 3.6P
00470 C52(3,4) 5.75P
00480 C53(14,6) .01U
00490 C61(15,6) 4.7U
00500 C57(15,6) .01U
00510 C62(10,6) 4.7U
00520 C58(10,6) .01U
00530 C55(29,19) 6.25P
00540 C56(25,10) 10P
00550 C59(4,6) 10P
00560 C60(11,6) 390P
00570 C54(20,6) .01U
00580 R83(2,1) 10MEG
00590 R84(1,10) 10MEG
00600 D250(A22,C21)1N973B
00610 DDUM(A37,C28)1N5712
00620 D51(A23,C10) 1N4454
00630 D52(A29,C37)1N5712
00640 Q50A,NPN(B6,C12,E8) 2N2920
00650 Q50B,NPN(B14,C13,E9)2N2920
00660 Q53,NPN(B24,C15,E20)2N3904
00670 Q56,NPN(B31,C29,E4)2N3904
00680 EM40(+6,-10)40,PS=1.0
00690 EP40(+15,-6)40,PS=1.0
00700 EM15(+6,-18)15,PS=1.0
00710 EP15(+17,-6)15,PS=1.0
```

```
00720 ED0(+G,-7)10,RS=1.0
00730 IS(R6,F6)I,PULSE,RI=1E6,0,6.024M,10N,10N,1.0U,10N,10U
00740 *THE 2N3806 IS NOT IN THE DATABANK.SUBBING THE 2N3810 IN Q54A & B.
00750 Q54A,PNP(B20,C21,E13) 2N3810
00760 Q54B,PNP(B20,C29,E12)2N3810
00770 *PARAMETERS FOR FOLLOWING QS SUPPLIED BY ROCKWELL.
00780 Q55,NPN(B22,C26,E25) NOM
00790 370,90M,0.3621,0.2M,0.4054,0.175,1,4.101,0.6006,6.006M,
00800 2.693E-11,1.366,5.406G,80,10M,40.54,7.05P,0.75,0.33,0.3623U,0,0,0,0,
00810 5.305E-12,1.205,0.5403G,7.059,10M,3.305,19.36P,0.75,0.5,530.8P,0,0,0,0
00820 Q58,NPN(B29,C15,E30) NOM
00830 370,90M,0.3621,0.2M,0.4054,0.175,1,4.101,0.6006,6.006M,
00840 2.693E-11,1.366,5.406G,80,10M,40.54,7.05P,0.75,0.33,0.3623U,0,0,0,0,
00850 5.305E-12,1.205,0.5403G,7.059,10M,3.305,19.36P,0.75,0.5,530.8P,0,0,0,0
00860 Q59,PNP(B26,C10,E33) NOM
00870 163,7M,0.8222,0.3M,0.4294,0.17,1,3.603,0.6435,6.435M,
00880 1.157E-13,1.1,7.26,106.7,10M,42.36,9.401P,0.75,0.33,0.2189U,0,0,0,0,
00890 8.977E-15,1,0.456,5.882,10M,2.121,23.24P,0.75,0.5,0.5308N,0,0,0,0
00900 Q60,NPN(B30,C15,E34)IE,P, NOM
00910  230,60M,0.9131,10M,0.1304,1,1,2.574,0.2369,2.369M,
00920  1.658E-9,1.654,9.735G,133.3,10M,85.4,21.67P,.75,.33,0.2906U,0,0,0,0,
00930  1.421E-9,1.503,0.5245G,5.882,10M,3.731,11.62P,.75,.5,0.6923N,0,0,0,0
00940 Q61,PNP(B33,C10,E27)IE,P, NOM
00950  220,40M,0.95,10M,0.1364,1.3,1,2.973,0.2721,2.721M,
00960  1.155E-12,1.1,96,133.3,10M,58.27,31.3P,.75,.33,0.1806U,0,0,0,0,
00970  3.297E-13,1,0.45G,5.882,10M,2.437,16.78P,.75,.5,0.9099N,0,0,0,0
00980 Q62,NPN(B30,C15,E35)IE,P, NOM
00990  230,60M,0.9131,10M,0.1304,1,1,2.574,0.2369,2.369M,
01000  1.658E-9,1.654,9.735G,133.3,10M,85.4,21.67P,.75,.33,0.2906U,0,0,0,0,
01010  1.421E-9,1.503,0.5245G,5.882,10M,3.731,11.62P,.75,.5,0.6923N,0,0,0,0
01020 Q63,PNP(B33,C10,E36)IE,P, NOM
01030  220,40M,0.95,10M,0.1364,1.3,1,2.973,0.2721,2.721M,
01040  1.155E-12,1.1,96,133.3,10M,58.27,31.3P,.75,.33,0.1806U,0,0,0,0,
01050  3.297E-13,1,0.45G,5.882,10M,2.437,16.78P,.75,.5,0.9099N,0,0,0,0
01060 Q57,PNP(B32,C26,E4) NOM
01070 200,10M,0.7691,0.1M,0.15,0.15,1,2.782,1.982,19.82M,
01080 3.73E-10,1.757,3.627G,53.33,10M,31.19,5.288P,0.75,0.33,0.1753U,0,0,0,0,
01090 8.494E-11,1.597,0.4513G,5.882,10M,3.165,7.746P,0.75,0.5,0.3185N,0,0,0,0
01100 *RL IS THE LOAD RESISTOR.
01110 RL(4,0)I,300
01120 FINIS
01130 TIME=10N,4.0U
01140 PLOT=ISII,NODE4
```

APPENDIX B

PIU PROGRAMMER

The PIU programmer was designed to emulate the basic control and programming functions of the HATS computer to enable external programming and operation of the PIU card modules. The PIU programmer has a rear connector that hooks up via a cable to a special test fixture, where PIU cards can be plugged in. The test fixture uses the same backplane connector found inside the HATS machine.

Figure B-1 illustrates the functional design concept of the PIU programmer. This design is an enhancement of a manual programmer circuit developed earlier (see Appendix D of *Reliability Improvement Analysis of the Programmable Interface Unit of the Hybrid Automatic Test Station,* ARINC Research Publication 1777-01-1-2318, November 1980). The tedious and time-consuming operations involved in the use of the manual programmer have been eliminated by incorporating automatic features in the present design. Programming has been simplified by allowing storage and ready access of programmed instructions, hexadecimal readout of data and code information, and automatic PIU program loading.

The PIU programmer basically operates in three modes -- automatic, manual word, and manual bit. Control switches provide the reset, clear, SLEN, LSB, read/write, and auto/man selectable functions. In the primary (automatic) mode, the desired PIU operating mode instructions are first selected and stored in the machine (hexadecimal) code. Data/code instructions are selected via the SS_W (single-step word) switch, which advances the word counter every time this switch is depressed. The word counter generates a 4-bit word identical to the data and code word format used by the PIU. The selected code/data word is entered in the random access memory (RAM) via the SS_A (single-step address) switch. The code and data words are alternately stacked in sequential address locations in the RAM. Once the instructions are entered, the programming of the PIU is totally automatic. The programmer fetches the code and data instructions from the RAM, sends them to the proper buses, and transfers them to the PIU with data strobe signals. A steering control circuit (represented by the "valve" symbol in the diagram) is used to direct data/code instructions from the word counter to the RAM, code bus, or data bus, and data/code instructions from the RAM to the code bus or data bus.

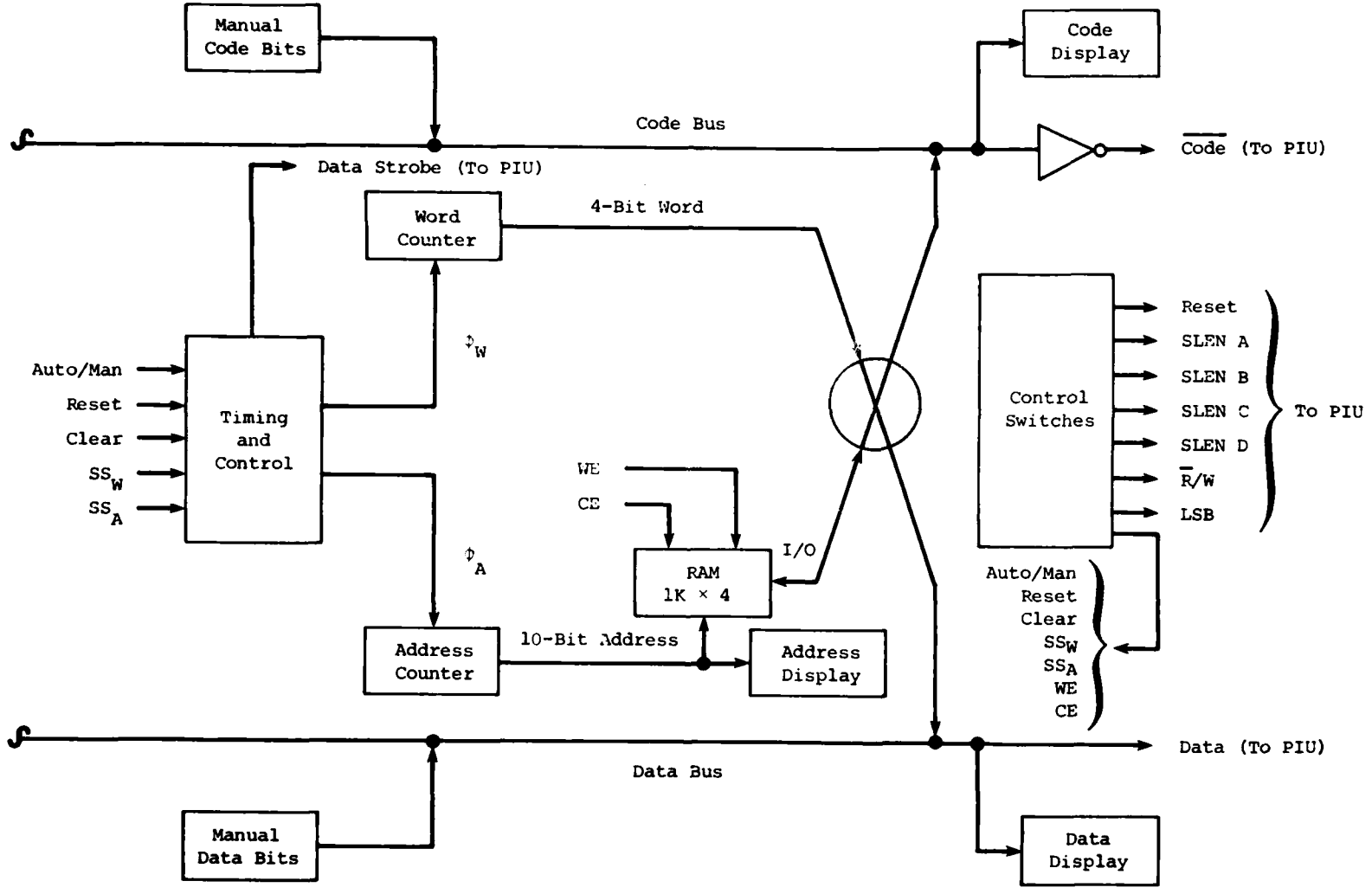


Figure B-1. SIMPLIFIED BLOCK DIAGRAM OF HATS PIU PROGRAMMER

The timing and control circuit generates clock and synchronization signals that instruct the programmer when to start, strobe, and stop transmitting data. Programming in the manual word mode involves sending the data and code instructions from the word counter directly to their respective buses and manually strobing each instruction to the PIU. The manual bit programming mode employs the method used in the earlier programmer circuit, where a set of switches provides the data and code bit instructions. The RAM is disabled in the manual modes.

APPENDIX C

PIU THERMAL PERFORMANCE DATA UNDER NORMAL LOADS

Table C-1 presents thermal data recorded under normal load conditions during laboratory testing of the PIU configuration.

Table C-1. PIU THERMAL PERFORMANCE UNDER NOR

Programmed Test Temperature (°C)	Programmed Mode	PIU Component Temperatures (°C) b														
		U109			U111			U191			U190			Q130		
		A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
5	+30 V R_L = 300	11.3	11.3	9.8	11.8	10.6	9.1	17.3	17.2	11.8	18.6	17.9	12.4	11.0	13.1	10.
	±30 V R_L = 300	13.0	11.1	8.9	13.2	10.4	8.4	16.9	16.5	11.7	18.7	17.7	11.7	10.9	12.2	9.
	±3.8 V R_L = 39	16.6	14.5	12.0	16.3	13.2	11.9	16.7	16.5	11.5	18.8	18.2	12.0	10.8	12.6	9.
	+3.8 V R_L = 39	15.4	14.3	11.6	15.7	13.3	11.5	16.5	17.1	11.4	18.4	17.6	12.0	10.8	13.2	10.
15	+30 V R_L = 300	19.0	19.5	18.0	19.7	19.3	17.8	25.7	24.9	21.7	26.6	25.8	21.3	19.9	21.1	19.
	±30 V R_L = 300	23.1	22.6	21.5	23.4	22.1	21.3	27.8	28.1	23.4	29.3	29.3	23.3	21.9	23.8	21.
	±3.8 V R_L = 39	30.0	27.7	26.1	29.8	26.5	26.1	30.2	29.5	25.5	32.0	31.0	25.5	24.7	26.0	23.
	+3.8 V R_L = 39	28.7	26.2	24.6	29.1	25.5	20.5	29.1	28.8	24.5	30.5	29.0	24.3	23.7	25.0	22.
25	+30 V R_L = 300	31.2	31.0	29.4	31.9	30.8	29.2	37.2	36.8	32.0	38.0	37.6	31.5	31.1	33.0	29.
	±30 V R_L = 300	34.1	33.3	31.3	34.6	32.5	31.1	38.2	38.2	33.4	39.4	39.6	33.2	32.3	34.0	30.
	±3.8 V R_L = 39	40.3	38.1	36.0	40.3	37.2	36.0	40.0	40.1	35.1	41.3	41.6	35.2	34.3	36.4	33.
	+3.8 V R_L = 39	38.5	36.4	34.5	39.0	35.8	34.9	39.0	38.5	34.2	40.1	39.7	33.9	33.4	35.0	32.
35	+30 V R_L = 300	39.8	39.4	37.4	40.4	39.3	37.0	45.5	45.2	41.0	46.0	45.9	40.5	39.6	41.4	38.
	±30 V R_L = 300	42.5	41.3	40.1	43.0	40.8	40.0	46.5	46.0	42.1	47.6	47.4	41.9	40.8	42.2	39.
	±3.8 V R_L = 39	47.3	44.9	43.0	47.5	43.9	43.3	46.8	46.6	42.3	48.1	48.0	42.3	41.2	43.0	40.
	+3.8 V R_L = 39	46.3	44.0	42.3	47.1	43.4	42.8	46.6	46.1	41.9	47.5	47.3	41.7	41.0	42.7	39.
45	+30 V R_L = 300	49.4	49.8	49.0	50.2	49.8	49.3	55.3	55.0	51.8	55.8	55.9	51.3	49.8	51.5	49.
	±30 V R_L = 300	52.2	52.0	51.1	52.8	51.7	51.4	56.7	56.7	53.3	57.6	58.1	53.0	51.4	52.8	50.
	±3.8 V R_L = 39	58.8	56.5	55.3	59.5	56.1	55.6	58.7	57.7	54.5	59.7	59.8	54.3	53.5	54.5	52.
	+3.8 V R_L = 39	58.1	55.8	54.4	59.1	55.3	55.0	58.0	57.5	54.1	58.7	58.8	53.8	52.8	54.3	52.
55	+30 V R_L = 300	63.3	61.8	61.0	64.0	61.5	61.0	67.8	67.1	63.5	67.5	67.9	62.7	62.4	63.8	61.
	±30 V R_L = 300	64.2	62.5	61.4	64.8	62.0	61.5	67.2	66.6	63.1	67.5	68.1	62.5	61.9	63.0	61.
	±3.8 V R_L = 39	66.9	65.1	63.2	67.7	64.4	63.8	65.9	65.8	62.4	66.6	67.7	61.8	61.2	62.6	61.
	+3.8 V R_L = 39	66.7	64.1	62.6	67.8	63.9	63.3	66.4	65.8	62.3	66.6	67.1	61.6	61.5	62.6	61.
65	+30 V R_L = 300	67.5	75.9	68.6	68.3	78.0	69.2	73.6	75.2	71.7	73.6	63.8**	70.9	68.6	72.1	
	±30 V R_L = 300	71.7	74.2	73.2	72.5	74.5	74.0	77.0	77.5	75.7	77.8	80.3	75.3	72.2	75.2	
	±3.8 V R_L = 39	75.4	72.7	72.1	76.2	72.5	72.8	74.9	73.5	71.6	76.5	77.5	71.5	70.1	71.6	
	+3.8 V R_L = 39	74.7	72.4	71.6	75.7	72.5	72.3	75.2	73.8	71.6	76.2	77.2	71.1	70.3	72.0	

*A = current-limit configuration; B = transistor-substitution configuration; C = combined configuration.
**Sensor failed.

RMAL PERFORMANCE UNDER . . LOAD CONDITIONS

ponent Temperatures (°C) by Configuration*

	Q130			Q156			Q150			Q160			Q158			Air Flow		
C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
12.4	11.0	13.1	10.2	6.5	10.9	5.9	12.2	17.2	9.8	10.4	12.9	9.7	8.3	11.5	8.8	4.1	3.8	5.3
11.7	10.9	12.2	9.2	7.0	10.6	5.7	13.2	14.9	12.2	11.5	13.2	6.5	8.8	10.6	7.4	4.4	2.2	2.3
12.0	10.8	12.6	9.6	6.8	12.0	7.0	12.0	15.0	12.5	17.4	22.4	15.0	9.8	13.3	9.9	3.0	4.1	4.3
12.0	10.8	13.2	10.0	7.7	12.5	6.7	12.4	16.0	9.4	20.5	26.1	18.4	12.4	15.8	13.1	4.0	4.8	4.2
21.3	19.9	21.1	19.2	17.2	20.5	16.9	23.4	26.1	23.4	20.0	22.1	16.4	18.7	20.8	18.0	15.7	15.5	15.7
23.3	21.9	23.8	21.9	18.4	23.3	18.7	25.0	27.8	25.1	22.7	25.2	21.7	24.0	23.3	25.0	16.0	16.0	16.3
25.5	24.7	26.2	23.4	20.6	25.5	21.0	26.3	28.3	26.6	31.0	35.7	29.3	23.6	26.5	24.0	17.8	17.7	18.0
24.3	23.7	25.0	22.3	20.5	25.4	20.8	26.0	27.6	26.0	34.3	38.4	31.0	25.7	28.1	25.7	16.8	16.9	17.2
31.5	31.1	33.3	29.8	27.0	31.1	26.8	33.5	36.7	33.1	30.8	33.0	29.7	29.3	31.6	28.7	25.0	25.0	24.6
33.2	32.3	34.0	30.9	28.3	33.4	28.2	35.2	37.8	34.7	33.0	35.6	31.5	30.4	33.4	30.0	25.8	25.8	25.5
35.2	34.3	36.4	33.1	30.5	35.5	30.5	36.6	38.4	36.4	41.9	46.0	39.3	34.3	36.6	33.6	27.3	27.5	27.2
33.9	33.4	35.7	32.3	30.1	35.1	30.3	35.9	37.9	35.6	43.8	48.0	41.0	35.9	38.0	35.2	26.6	26.4	26.3
40.5	39.6	41.4	38.7	35.9	39.9	35.5	42.9	44.9	42.3	39.7	41.8	35.2	38.3	40.3	36.6	33.9	33.8	33.7
41.9	40.8	42.2	39.7	36.9	41.5	36.8	44.0	46.1	43.3	41.7	43.8	40.3	39.4	41.6	39.0	34.2	34.2	34.0
42.3	41.2	43.1	40.2	37.6	42.3	37.5	43.9	45.0	43.3	48.7	52.6	46.3	41.6	43.5	40.6	34.2	34.2	34.1
41.7	41.0	42.7	39.4	37.0	43.0	38.0	43.7	35.3	43.4	51.6	55.8	48.7	43.6	45.8	43.0	34.0	34.2	34.0
51.3	49.8	51.5	49.4	47.4	51.0	47.8	54.1	56.5	54.0	50.7	52.5	50.3	49.7	51.5	49.5	45.5	45.9	46.6
53.0	51.4	52.8	50.4	48.8	52.6	48.8	55.8	57.9	55.2	52.6	54.8	51.8	51.1	53.1	50.7	46.9	46.2	46.6
54.3	53.2	54.5	52.3	50.1	54.4	49.8	56.7	57.7	55.4	60.9	64.3	58.2	54.1	55.4	52.9	46.6	46.4	46.3
53.8	52.8	54.3	52.1	50.2	55.0	50.7	56.3	57.8	55.9	64.1	67.6	60.6	56.2	57.9	55.5	46.2	46.7	47.2
62.7	62.4	63.8	61.1	58.4	61.8	57.9	65.4	67.1	63.9	63.1	63.8	61.0	61.4	62.2	60.1	55.6	55.4	55.0
62.5	61.9	63.0	60.7	58.3	62.4	57.8	65.6	67.6	63.8	63.4	64.6	61.1	61.2	62.6	59.9	55.1	54.9	54.4
61.8	61.2	62.6	60.2	58.1	61.4	57.7	64.5	65.3	63.1	68.9	69.5	66.0	62.2	61.5	60.8	54.5	54.0	53.8
61.6	61.5	62.6	60.2	58.6	62.9	58.1	64.6	66.0	63.2	72.4	75.4	68.1	65.0	65.6	63.2	54.3	54.1	53.7
70.9	68.6	72.1	68.8	67.4	76.0	67.6	73.6	77.3	72.9	70.5	73.3	70.3	69.3	72.5	70.0	65.4	69.4	65.9
75.3	72.2	77.2	72.9	72.5	75.7	72.4	77.3	79.2	78.7	74.6	73.6	75.0	73.5	71.2	74.7	70.4	71.5	69.5
71.5	70.1	71.6	69.4	69.1	71.8	66.6	72.3	72.9	72.3	79.6	80.5	74.3	71.3	71.3	70.6	63.3	63.2	64.8
71.1	70.3	72.0	69.4	69.9	74.7	67.6	72.7	73.7	72.6	83.1	84.0	76.6	73.9	72.9	73.6	63.2	63.8	64.8

APPENDIX D

PIU THERMAL PERFORMANCE DATA UNDER CURRENT-LIMITING CONDITIONS

Table D-1 presents thermal data recorded under current-limiting conditions during laboratory testing of the PIU configurations.

Table D-1. PIU THERMAL PERFORMANCE UNDER OVERLOAD (CUR

Test Conditions																				
Programmed Test Temperature (°C)	Programmed Mode ($R_L = 10 + R_A$)*	V_o Measured (Volts)			I_o Measured (mA)			U109			U111			U191			U190			
		A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	[illegible]	A
5	+3.8 V	+2.42	+2.70	+2.25	+138	+250	+131	18.6	24.0	13.3	18.7	26.1	13.9	15.7	15.6	11.3	16.2	19.[illegible]	11.	11.
	-3.8 V	-2.46	-2.70	-2.55	-147	-250	-150	25.2	28.6	18.4	24.0	30.0	18.5	18.[illegible]	18.4	14.[illegible]	18.7	20.8	13.[illegible]	13.
	+30 V	+2.80	+3.10	+2.60	+163	+285	+154	20.7	24.8	14.5	21.0	26.9	15.2	16.[illegible]	15.9	11.9	17.2	19.7	11.6	12.
	-30 V	-2.86	-3.00	-2.90	-166	-280	-172	23.5	29.6	18.5	22.5	31.5	19.[illegible]	16.[illegible]	16.1	12.7	17.1	20.1	12.[illegible]	12.
15	+3.8 V	+2.35	+2.60	+2.20	+136	+245	+127	29.4	33.3	24.2	29.8	35.3	24.6	25.[illegible]	25.4	21.9	21.1	23.3	2[illegible]	21.
	-3.8 V	-2.40	-2.60	-2.50	-139	-245	-146	33.3	37.9	27.7	32.0	39.4	28.[illegible]	26.5	26.[illegible]	22.9	22.2	23.8	2[illegible]4	22.
	+30 V	+2.78	+3.00	+2.55	+159	+280	+150	31.4	33.9	25.0	31.8	36.6	25.5	26.7	25.8	22.7	22.0	23.1	21.[illegible]	22.
	-30 V	-2.82	-2.90	-2.80	-162	-270	-167	35.2	39.5	29.0	34.0	41.2	29.1	27.3	26.6	23.3	22.6	23.7	21.[illegible]	22.
25	+3.8 V	+2.28	+2.50	+2.10	+131	+235	+123	39.7	33.2	35.0	40.1	45.6	35.5	36.0	35.9	32.9	36.3	39.0	3[illegible]	33.
	-3.8 V	-2.34	-2.50	-2.45	-135	-240	-142	44.4	48.2	39.4	43.7	50.1	39.9	37.8	37.4	34.2	38.0	40.3	33.[illegible]	33.
	+30 V	+2.[illegible]8	+2.90	+2.48	+155	+270	+145	43.8	46.0	37.8	44.3	49.0	38.4	38.8	38.0	35.0	38.8	41.0	33.8	34.
	-30 V	-2.72	-2.[illegible]	-2.80	-163	-268	-168	48.1	51.6	42.4	47.4	54.3	43.0	39.7	39.6	36.4	39.7	39.6	36.4	39.
35	+3.8 V	+2.18	+2.50	+2.00	+126	+230	+118	51.1	54.1	46.0	51.7	56.7	46.6	46.6	46.7	43.5	47.2	50.0	42.[illegible]	43.
	-3.8 V	-2.62	-2.80	-2.50	-152	-260	-146	57.0	59.5	50.0	57.0	62.2	50.9	48.0	47.6	44.7	48.2	50.6	43.3	43.
	+30 V	+2.61	+2.80	+2.4[illegible]	+151	+260	+142	54.2	55.4	47.9	54.9	58.3	48.6	48.5	47.5	44.9	48.7	50.6	43.[illegible]	44.
	-30 V	-2.62	-2.80	-2.75	-152	-260	-160	58.2	61.1	52.0	58.3	63.6	53.0	48.9	49.2	45.6	49.2	52.0	44.2	45.
45	+3.8 V	+2.10	+2.40	+1.95	+120	+220	+113	63.0	65.0	57.9	58.2	58.6	55.5	58.9	61.4	54.3	54.5	56.7	53.3	54.
	-3.8 V	-2.14	-2.40	-2.30	-125	-220	-132	66.6	69.5	61.9	59.2	60.0	56.4	59.6	62.6	55.0	55.2	57.4	54.[illegible]	55.
	+30 V	+2.52	+2.70	+2.30	+145	+250	+136	65.9	67.1	59.6	59.8	60.0	56.5	60.1	62.9	54.9	55.6	57.8	54.4	55.
	-30 V	-2.53	-2.70	-2.66	-147	-250	-156	69.3	71.8	63.8	60.0	60.9	57.1	60.4	63.5	55.4	55.9	58.2	54.9	55.
55	+3.8 V	+2.10	+2.30	+1.88	+118	+219	+112	70.2	73.4	66.0	71.0	75.9	67.0	66.2	66.7	63.8	67.0	69.5	62.5	6[illegible]
	-3.8 V	-2.10	-2.30	-2.23	-123	-218	-128	75.2	77.9	70.6	75.7	80.3	71.6	67.8	67.6	65.0	68.5	70.5	63.4	6[illegible]
	+30 V	+2.46	+2.60	+2.30	+142	+245	+132	74.2	75.2	68.2	75.1	78.0	69.2	68.2	68.3	64.9	68.9	71.2	63.4	6[illegible]
	-30 V	-2.48	-2.60	-2.60	-137	-245	-153	77.6	80.0	72.3	78.2	82.7	73.5	68.4	69.3	65.5	69.0	71.8	63.9	6[illegible]

*R_A is ammeter resistance in the load. R_A = 6.6 for configurations A and C; R_A = 0.8 for configuration B.

**A = current-limit configuration; B = transistor-substitution configuration; C = combined configuration.

†NA = temperature not recorded, because Q161 is off in the +1.8 V and +3[illegible] V modes.

RFORMANCE UNDER OVERLOAD (CURRENT-LIMITING) CONDITIONS

FIU Component Temperatures (°C) by Configuration**

	U190			Q130			Q156			Q150			Q160			Q161			Q158			Air Flow		
	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
	16.2	19.0	11.0	11.1	12.8	8.9	10.5	23.5	8.1	12.5	14.3	12.7	32.7	59.6	25.6	NA+	NA	NA	14.6	21.2	12.6	2.6	0.5	3.6
	18.7	20.8	13.3	13.3	14.1	11.5	9.3	12.6	8.4	16.0	15.9	12.0	22.2	40.8	21.8	34.3	54.9	NA	9.8	16.2	9.6	4.1	2.6	4.5
	17.2	19.7	11.6	12.0	13.3	9.8	11.7	23.7	8.8	12.7	14.8	12.7	30.5	60.0	28.5	NA	NA	NA	16.0	21.6	13.7	1.7	1.2	3.8
	17.1	20.1	12.2	12.0	13.6	10.4	8.7	14.2	8.4	12.1	15.2	12.7	24.0	43.9	23.8	37.9	59.0	NA	8.9	18.2	8.9	3.2	0.9	5.1
	21.1	23.3	20.0	21.1	23.3	20.0	18.3	31.4	17.9	24.1	25.7	21.0	37.6	63.6	35.4	NA	NA	NA	24.7	29.6	24.6	11.9	13.0	13.3
	22.2	23.8	20.4	22.2	23.8	20.4	17.4	23.1	17.7	24.6	26.4	21.8	30.5	49.3	31.6	43.4	63.0	34.5	18.5	26.6	19.3	13.0	13.6	14.2
	22.0	23.1	21.3	22.0	23.1	21.3	19.6	32.4	19.1	24.4	25.6	21.7	40.8	67.9	38.4	NA	NA	NA	26.0	30.3	25.8	13.0	13.2	14.5
	22.6	23.7	21.0	22.6	23.7	21.	18.2	23.9	18.3	24.5	26.1	21.5	32.8	52.9	33.4	47.2	67.4	35.8	19.3	28.0	19.8	13.1	14.6	14.6
	36.3	39.0	32.0	32.0	33.5	33.5	30.4	42.2	29.8	35.8	36.8	33.2	48.3	72.7	46.3	NA	NA	NA	36.6	40.0	36.4	24.0	24.1	25.2
	38.0	40.3	33.0	33.5	34.9	31.9	29.8	34.3	29.8	36.8	37.2	34.	42.5	59.5	43.1	55.2	72.9	45.4	31.0	37.4	31.2	24.7	24.8	26.2
	38.8	41.0	33.8	34.5	35.7	32.9	32.8	45.3	32.0	37.6	38.7	34.8	53.2	78.3	50.8	NA	NA	NA	40.0	42.8	38.8	25.5	25.9	27.0
	39.7	39.6	36.4	35.5	37.0	34.2	32.2	36.7	31.9	38.5	39.5	35.7	46.5	63.8	46.6	60.9	77.5	49.5	33.5	40.8	33.7	27.9	26.7	26.4
	47.2	50.0	42.5	43.0	44.6	41.6	41.2	53.2	40.9	49.1	48.3	45.2	59.7	82.5	57.2	NA	NA	NA	49.6	51.1	47.7	35.4	35.5	36.0
	48.2	50.6	43.3	43.7	45.2	42.3	42.1	44.9	40.3	49.2	47.7	45.6	55.8	70.9	54.5	66.1	85.2	56.5	43.8	48.1	42.3	35.4	35.3	36.1
	48.7	50.6	43.6	44.4	45.2	42.7	44.0	54.5	42.3	49.4	48.3	45.7	63.9	86.2	60.7	64.9	79.5	53.1	51.6	52.3	49.5	35.7	35.9	37.0
	49.2	52.0	44.2	45.0	46.6	43.6	43.0	46.4	41.8	50.4	48.7	46.3	56.4	72.2	56.4	71.6	86.1	59.5	54.9	49.9	43.7	36.0	36.2	37.4
	54.5	56.7	53.3	54.5	56.7	53.3	56.7	64.5	53.7	62.6	60.3	58.1	71.6	92.3	68.8	72.8	86.2	62.4	63.1	62.8	59.8	47.8	47.7	48.5
	55.2	57.4	54.0	55.2	57.4	54.0	54.8	57.0	53.2	62.9	60.1	58.9	65.5	79.6	65.8	78.6	91.7	68.8	56.5	59.9	55.0	48.0	47.9	49.0
	55.6	57.8	54.4	55.6	57.8	54.4	57.4	65.7	54.4	62.8	60.2	58.1	76.4	96.3	72.0	77.3	90.3	65.2	64.5	63.9	60.6	47.9	47.9	48.8
	55.9	58.2	54.9	55.9	58.2	54.9	56.1	57.8	53.9	63.1	60.2	58.2	68.1	83.1	68.2	83.1	96.3	71.7	57.6	61.3	55.6	47.8	47.6	49.0
	67.0	69.5	62.5	62.4	64.9	61.5	64.9	72.6	62.0	71.0	68.1	66.6	78.9	99.0	76.8	80.8	93.2	71.1	71.6	70.5	68.1	56.8	55.9	56.9
	68.5	70.5	63.4	63.8	65.5	62.7	64.2	65.5	62.0	71.8	69.3	67.2	74.0	87.7	74.2	86.6	100.0	77.3	65.2	68.4	63.7	56.7	56.9	57.3
	68.9	71.2	63.4	64.0	65.9	62.9	66.6	73.9	63.3	72.1	68.2	67.1	83.5	103.5	80.5	85.2	97.4	73.8	73.8	71.9	69.8	56.6	56.4	57.3
	69.0	71.8	63.9	64.3	66.6	63.3	65.0	66.6	63.0	72.0	68.8	67.5	76.8	90.3	76.6	90.5	103.5	80.3	66.9	70.0	64.8	56.5	57.2	58.0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