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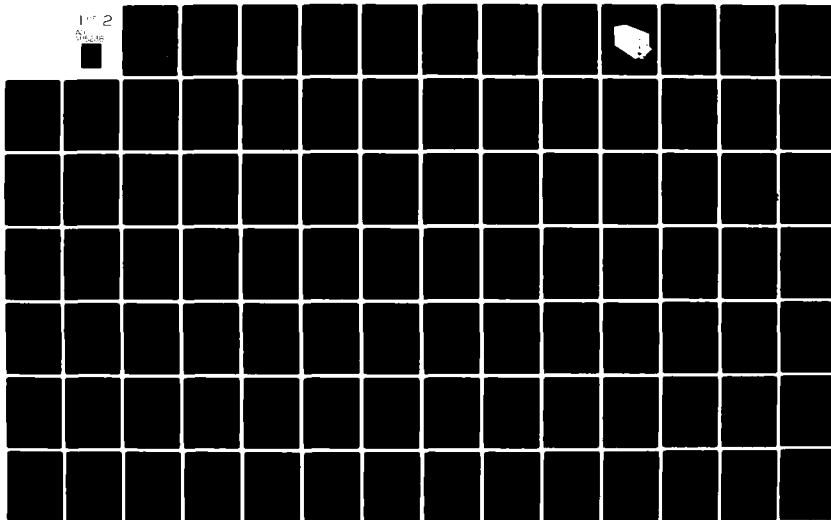
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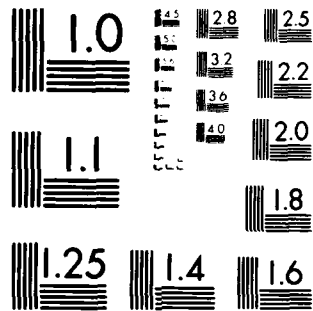
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PRELIMINARY
FINAL ENGINEERING REPORT
FOR
COMPUTER, WEAPON AIMING
CP-1444/A

CDRL SEQUENCE #A005

MANUFACTURER - Smiths Industries Aerospace and Defense Systems Inc.

Prepared By
Smiths Industries Aerospace and Defense Systems Inc.
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Prepared for
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ABSTRACT

This final report summarizes the development performed on the Weapon Aiming Computer (WAC), CP-1444/A, a weapon replaceable assembly (WRA), part of the AV-8C aircraft avionics. The WAC performs the following general functions:

- a. Signal conditioning of the aircraft attitude sensor data for use by the Head-Up Display (HUD) system;
- b. Air-to-air lead angle computation for the HUD air-to-air gunsight;
- c. Air-to-ground weapon depression and across-wind aimpoint computation for the HUD air-to-ground Continuously Computed Impact Point (CCIP) weapon release cue;
- d. Breakaway warning computation for terrain and weapon fragmentation avoidance for the HUD air-to-ground CCIP mode.

Nine preproduction WAC units have been manufactured and tested. Three of the units were tested by the Naval Air Test Center (NATC), Patuxent River, Maryland, (Technical Evaluation and Phase II BIS) and by VX5, China Lake, California, (Operational Evaluation). Another three units were subjected to a 4000 hour Reliability Development Test at the contractor's location. One of the remaining units was used for qualification testing and the remaining two units were held at the contractor's as spares.

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FINAL ENGINEERING REPORT

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1. BACKGROUND

1.1 General

The Interface and Weapon Aiming Computer (IWAC), part number 219 SUE/1, has been used as part of the weapon delivery system in the AV-8A Aircraft since 1976. The IWAC is of a hybrid design and has a weapon aiming capability of air-to-air guns only. An improvement to the IWAC, designated IWAC Phase II, was developed and flight tested in 1977 and 1978. This version of the IWAC incorporated air-to-ground weapon aiming, but was still of a hybrid design and, therefore, limited in speed, expansion capability, computation accuracy and reliability. These factors led to the initiation of the development of the WAC in 1978.

The WAC design guidelines were to develop a digital, special purpose computer which would incorporate all the functions of the IWAC Phase II, incorporate functional enhancements to improve weapon aiming performance, provide a minimum in-service Mean Time Between Failure (MTBF) of 1000 operating hours and have a minimum computation expansion of 20%.

Part of the WAC design and development effort was to incorporate the necessary modification to the Signal Data Converter, CV-3600/AVQ-30(V), which forms part of the AVQ-30 Digital Data Display Set (DDDS), to facilitate display of weapon aiming symbology to the pilot.

1.2 Purpose of Contracts

1.2.1 The purpose of Contract Number N00019-77-A-350-WW09 was to design and develop the WAC. Tasks involved in this effort were as follows:

- a. Design and fabricate nine WAC units, plus two sets of spare SRA's.
- b. Develop, fabricate, install and test five digital interface units to be installed in four SDC units. These interface units are to make the SDC compatible with the WAC.
- c. Develop, fabricate, install and test five Stability Augmentation Altitude and Hold System (SAAHS) digital interface units to be installed in four SDC units.
- d. Design and fabricate one SRA test set to test the WAC SRA's.
- e. Design and fabricate one WRA test set to test the WAC and perform fault isolation to the SRA level.
- f. Perform qualification testing of the WAC.
- g. Perform a 4000 hour Reliability Development Test.
- h. Support flight testing of the WAC.

- 1.2.1 Cont. i. Provide as a part of the non-recurring effort such production peculiar tooling and/or peculiar test equipment necessary for production purposes.
- j. Provide engineering data for review or approval.
- k. Provide a WAC/SDC Organizational level maintenance manual.
- l. Define, design and fabricate a SAAHS-WAC interface test set.
- 1.2.2 The purpose of Contract Number N00019-77-A-350-WW091H was to develop and implement design changes to the WAC/SDC as a result of the WAC flight test program. Tasks involved in this effort were as follows:
- a. Display stadiametric ranging symbol used in the air-to-air mode as a circle, with computed range to target shown in feet, using four digits located near the ranging symbol.
- b. Add, as a pilot selectable option, the use of radio height as the primary height input used in the air-to-ground weapon delivery mode.
- c. Display the WAC computed target height to enable the pilot to more accurately set the target heights via the target height setting control.
- d. Disable the display of the breakaway warning symbol when the target is not being tracked by the pilot.
- e. Removal of the invalid Continuously Computed Impact Point (CCIP) symbol parked at the boundary of the Head-Up Display (HUD) when the reflected CCIP symbol is displayed.
- f. Provide on the HUD an advanced breakaway warning cue.
- g. Provide a means to avoid the sudden appearance of the CCIP cue in the air-to-ground guns and rockets mode.
- h. Provide a flashing breakaway warning symbol.
- 1.2.3 The purpose of Contract Number N00019-81-G-0629-WW03 was to perform testing, repair, calibration and rework functions on all WAC units for a period of one year after delivery.

1.3 Equipment Description

- 1.3.1 The WAC, Figure one, is a microcontroller based computer housed in a 1/2 ATR short case. The unit receives analog, discrete and digital data from aircraft sensors. The received data is processed by the WAC to provide attitude, weapon aiming and breakaway information to the aircraft HUD system.
- 1.3.2 The WAC operates from the 400 hertz 3-phase aircraft power and also utilizes 28V DC for on/off control. Total power consumption is about 80 watts.
- 1.3.3 The WAC weighs 18 pounds, is 4.88" wide, 7.81" high and 15" long.
- 1.3.4 The hardware architecture of the WAC is comprised of a microcontroller utilizing bit-slice technology and a nano code program developed by the contractor. The microcontroller is used to control all functions of the WAC hardware, including analog-to-digital conversion, operational software execution and control, arithmetic processing and output interfacing.
- 1.3.5 The hardware involved in the analog-to-digital conversion consists of three functionally partitioned Shop Replaceable Assemblies (SRA); the Synchro Transformer Module, Synchro/Rate Module and A/D Converter Module. These three SRA's accept DC analog, AC analog, 3-wire synchro and DC discrete signals and convert them to 12-bit parallel digital data. A total of 40 channels of analog and discrete data is converted each WAC computing frame, with an 8 channel expansion capability designed into the system.
- 1.3.6 The hardware designed for the software execution and control consists of three SRA's; the microcontroller module, PROM and timing module and RAM and BIT module. These SRA's form the central processing function of the WAC and additionally control the Built-In-Test (BIT) fault indicators.
- 1.3.7 The arithmetic processing hardware consists of one SRA; the APU module. This SRA incorporates two Arithmetic Processor Units (APU) which perform 16-bit fixed point and 32-bit floating point arithmetic, including square roots and trigonometric functions. All WAC internal arithmetic operations are performed in floating point for maximum accuracy and precision.

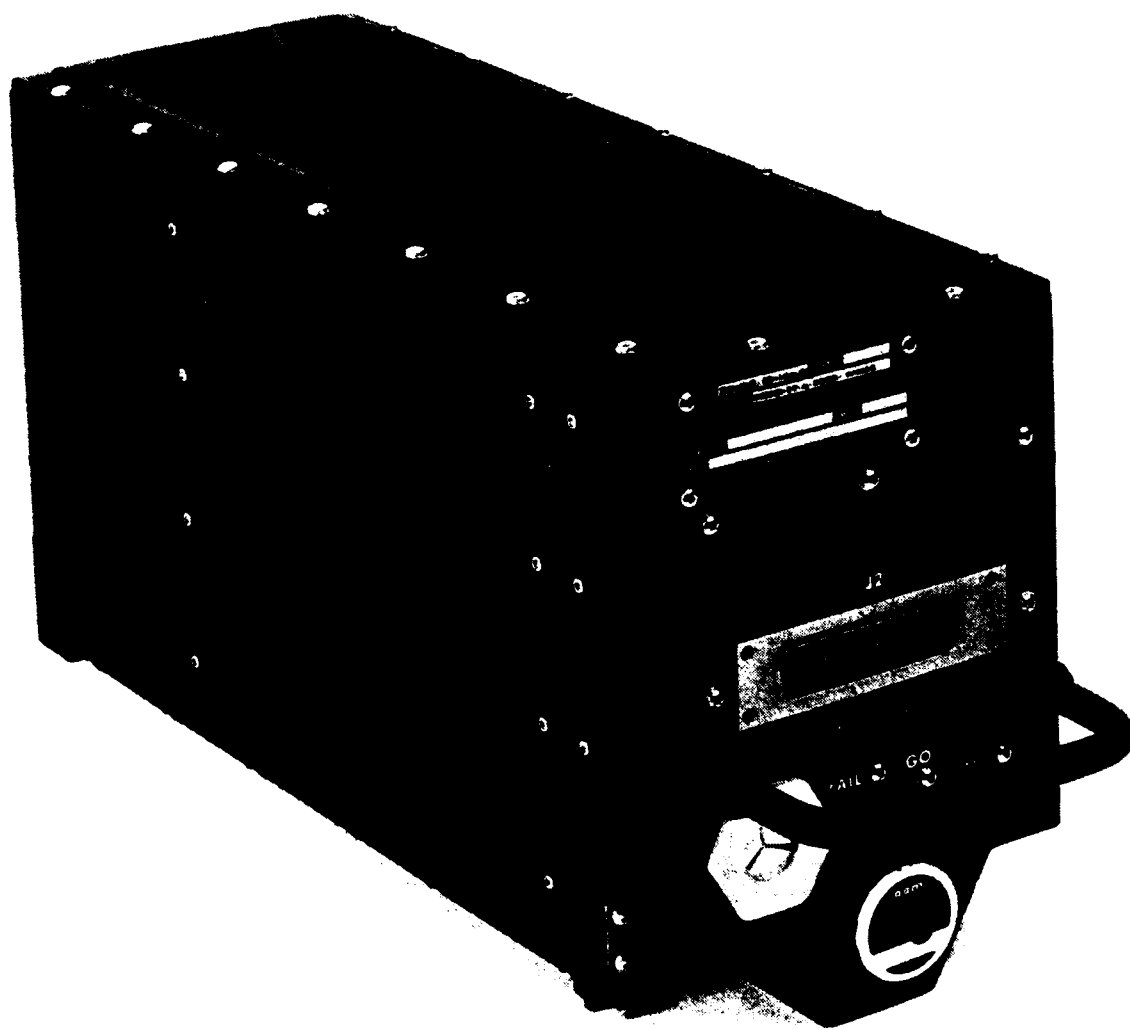


Figure 1. Weapon Aiming Computer
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- 1.3.8 The output interfacing hardware in the WAC consists of one SRA; the Output Interface module. This SRA converts 16-bit parallel digital data into two synchronous 8-bit serial digital data for transmission to the HUD system. This SRA additionally provides isolated reference voltages which are supplied to various aircraft sensors.
- 1.3.9 The operational software of the WAC is contained in Programmable Read Only Memory (PROM) physically located on the PROM and Timing module. The implementation of the WAC equations is done on a modular basis. These equations are structured on mode, and software modules are accessed depending on which weapon has been selected. Entry to each module is controlled by a software executive which allows for easier software test and debugging and software maintainability. A general system flowchart of the WAC operational software is illustrated in Figure two.
- 1.3.10 The equations implemented in the WAC software are contained in CWTR/S/2 and CWTR/WS/1.
- 1.3.11 The supporting software used/developed as part of the WAC development program is as follows:
- a. 2901 cross assembler
 - b. PROM download program
 - c. Dynamic test (DT) program
 - d. WAC mathematical model program
 - e. DT input data generation program
 - f. DT input data scaling program
 - g. DT output data scaling program
 - h. DT input data download program
 - i. DT output data upload program
 - j. DT data reduction program
 - k. File copy program
 - l. Paper tape program
 - m. Z terms program
 - n. WAC performance test programs
 - o. WAC troubleshooting programs
 - p. WAC SRA performance test programs
 - q. WAC SRA troubleshooting programs
 - r. WAC test set calibration programs
 - s. Bomb ballistic fitting program
 - t. Gun/rocket ballistic fitting program
 - u. WAC error analysis program.

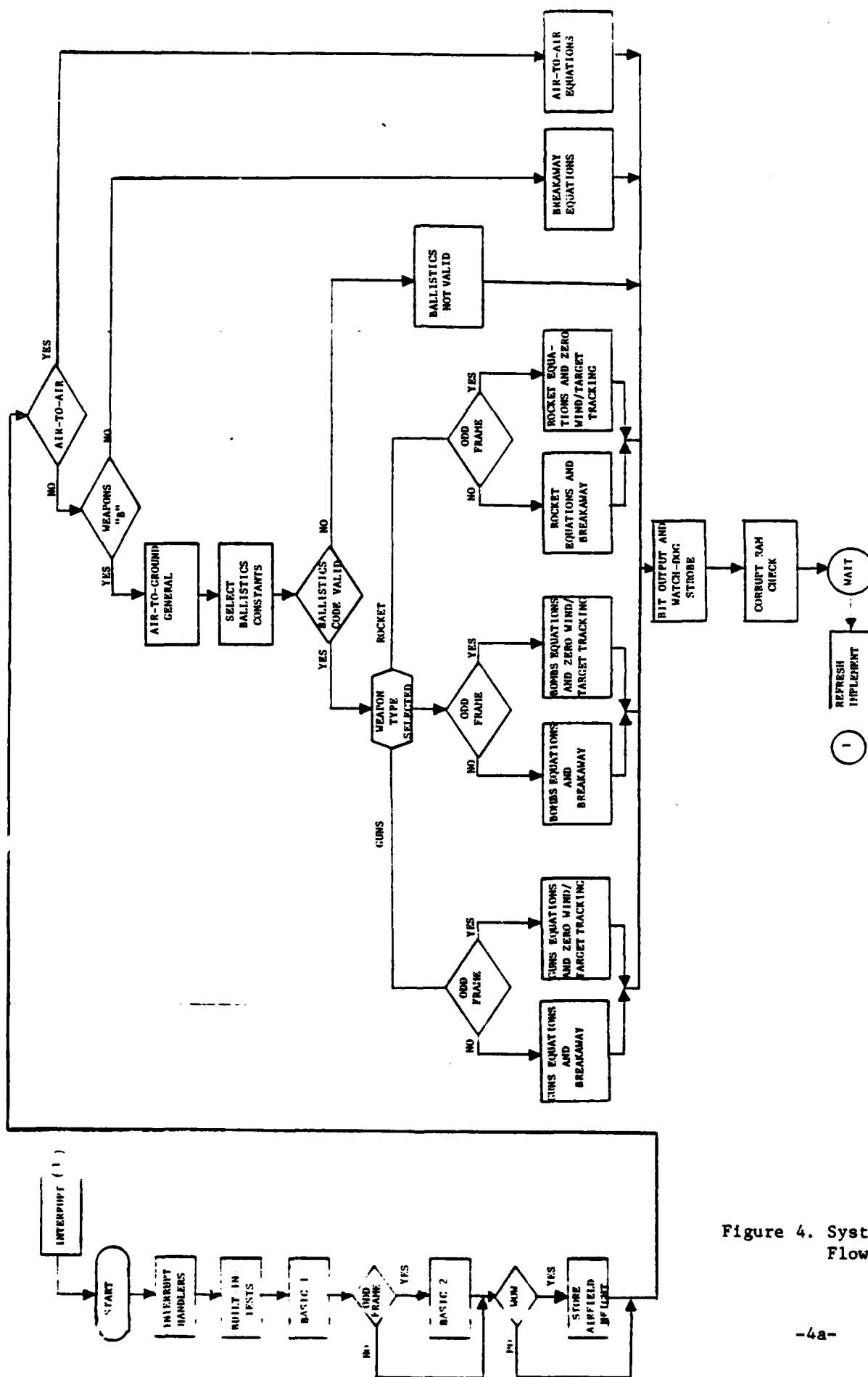


Figure 4. System Flowchart

1.4 General Factual Data

1.4.1 Weapon Aiming Functional Description

- 1.4.1.1 The weapon aiming algorithms developed for the WAC consist of two categories; air-to-air guns weapon aiming and air-to-ground guns, rockets and bombs weapon aiming.
- 1.4.1.2 In the air-to-air mode, the method used for providing the pilot with an aiming mark which, if kept on the target, will ensure that, when the guns are fired, the shells will strike the target is computation of the lead angle based upon aircraft rates of turn and range to the target aircraft. The target range is obtained using the technique of stadiametric ranging. In this technique a voltage is provided to the WAC which is derived from a wing span setting control on the aircraft's Display Set Control (DSC) and the output of the throttle twist grip.
- 1.4.1.3 The range data received by the WAC is proportional to the target wing span and the range to the target. The data is acquired as a result of the pilot estimation of the wing span and the adjustment of the diameter of the air-to-air ranging symbol on the HUD to caliper the target by adjustment of the throttle twist grip.
- 1.4.1.4 The rates of turn, i.e. pitch, roll and yaw rate, are derived from the aircraft's rate gyros in the form of amplitude modulated 400 Hz analog signals. These signals represent the turn rates of the target aircraft by virtue of the turn rates required to maintain the aiming mark on the target. The WAC demodulates, digitizes and applies various signal correction factors to the rate inputs prior to use in the lead angle computing algorithms.
- 1.4.1.5 The WAC additionally receives other aircraft sensor data representing true airspeed, pitch angle, bank angle, angle of attack and barometric height. Using all of the received sensor data the WAC computes the required lead angle based upon the stored ballistic constants for the ADEN 30 MM gun and transmits the azimuth and elevation position of the aiming mark to the HUD system for display. The range to the target is also transmitted to the HUD system for display while in the air-to-air mode.

- 1.4.1.6 In the air-to-ground mode, the method used for providing the pilot with a CCIP release cue which defines the weapon impact point on the ground is to execute a set of equations defining the trajectory which are based upon the ballistics and physical characteristics of the weapon and constructed to fit the ballistics tables. The constants used in the ballistic equations are computed for each weapon off-line and stored for use in the WAC program memory.
- 1.4.1.7 The algorithms implemented in the WAC for computing the CCIP position require aircraft sensor data to determine the weapon release height above the target, the aircraft dive angle, the aircraft pitch and bank angle and the total aircraft heading change during the target tracking phase of the air-to-ground attack. Since the AV-8C aircraft lacks any degree of sophistication with regards to aircraft sensors, explicit height above target and dive angle are not available. This necessitates considerable computing by the WAC to achieve the required aircraft positional data by use of sensor inputs for barometric height, target height, barometric datum, indicated airspeed, true airspeed, pitch and bank angle, angle-of-attack, mach number and airfield height in order to establish the in-range position of the CCIP.
- 1.4.1.8 The aircraft heading input is required for the target tracking phase of the attack in order to determine the across heading wind vector magnitude. This data is used to determine the azimuth position of the CCIP which will provide the pilot with both steering data and an offset aim-point to compensate for the cross trail effects of wind on the weapon. This degree of sophistication in mathematics is required due to the lack of aircraft sensor data concerning wind. The positional data transmitted to the HUD system for display is the CCIP azimuth and elevation position with respect to the aircraft's Flight Reference Line (FRL) and an azimuth steering line which is used to track the target.
- 1.4.1.9 Additional computations are performed by the WAC to provide a breakaway warning to the pilot in the event that the present aircraft's flight path will either intersect the ground or, in the case of a rocket or low drag bomb mode, the fragmentation pattern after weapon impact. An advance warning for breakaway is also computed to provide the pilot a minimum two second advanced warning of entering a breakaway condition. This information is also transmitted to the HUD system for display.

1.4.2 Display Format Development

- 1.4.2.1 The development of the display format and methods for the WAC took place in two phases. The first phase was the proposal by the contractor to implement the same display format as used in the Phase II IWAC with the exception of the bomb fall line, which would be displaced in azimuth to facilitate the target tracking mode and be redefined as an azimuth steering line, and to incorporate a reflective CCIP display method which offers the pilot an anticipation cue indicating the approach of the CCIP release cue into the HUD forward field of view. The second phase of display development was a result of both flight testing at the NATC, Patuxent River, and flight simulation at the contractor's facility. Flight testing brought about changes to the reflective display methods, air-to-ground guns presentation and air-to-ground rockets presentation. Flight simulation testing resulted in changes to the air-to-air display, all air-to-ground displays, the breakaway warning display and the addition of a CCIP display in an additional pilot selectable mode which would incorporate all air-to-ground mode displays except the target tracking information would be omitted. This change gives the pilot the option to perform a "zero wind" solution for the air-to-ground attack.

1.4.3 WRA/SRA Test Set Development

- 1.4.3.1 The WRA/SRA test set development for the WAC was designed to perform testing and fault isolation of the WAC to the module level and testing and fault isolation of the WAC modules to the piece part level.
- 1.4.3.2 The test set was designed to incorporate the use of a general purpose laboratory computer and specially designed interfacing to provide the WAC with input stimulus and evaluate the WAC output data for accuracy semiautomatically. The design additionally provided for computer aided troubleshooting at both the WRA and SRA level with a minimum amount of operator interaction. The test set is designated as depot level test equipment for use at the contractor's facility and, therefore, is not constructed as ruggedized equipment.

1.4.4 Dynamic Test Development

- 1.4.4.1 In order to ensure operational performance of the WAC under real time conditions prior to submission of the unit for flight testing, dynamic testing of the WAC was performed during WAC development. This testing required the design and fabrication of a WAC dynamic simulator and the development of test software and supporting software for data generation and reduction.
- 1.4.4.2 The dynamic simulator hardware was functionally similar to the hardware developed for the WRA/SRA test set, however, was fabricated as an engineering brassboard model. Many of the controls which are automated in the test set require manual operation by operator in the dynamic simulator. The simulator was designed and implemented in such a manner as to allow for maximum input/output (I/O) data transfer rates. This I/O speed allowed the simulator to subject the WAC to actual dynamic flight conditions and record the WAC outputs for off-line evaluation.
- 1.4.4.3 The software developed for the dynamic simulator consisted of a dynamic test program which performed all I/O functions between the WAC and the simulator and supporting software which resided off-line from the simulator and performed the following functions:
 - a. A data generation program which generated flight profile input data.
 - b. A download program to transfer input data files from the off-line computer to the dynamic simulator.
 - c. A data upload program to transfer output data files from the dynamic simulator to the off-line computer.
 - d. A data scaling program to convert I/O data to a useable format.
 - e. A WAC dynamic math model program to use for WAC output data comparison. This program was previously tested against the individual weapon ballistic tables to validate performance.
 - f. A data reduction program to compare WAC output data with the dynamic math model and flag errors on a per computing frame basis.
- 1.4.4.4 The dynamic simulator was additionally used during the WAC development to analyze problems encountered during the flight testing at the NATC, Patuxent River. The simulator proved to be an invaluable engineering tool in solving problems of a dynamic nature.

1.4.5 SDC Development

- 1.4.5.1 As part of the WAC development, the SDC required both hardware and software development and modification to interface with the WAC and SAAHS and incorporate the display functions for weapon aiming and SAAHS.
- 1.4.5.2 The hardware developed for the SDC consisted of a WAC/SAAHS interface module. This module was designed to transmit and receive dual 8-bit serial data for interfacing with the WAC and receive single 8-bit serial data for interfacing with the SAAHS.
- 1.4.5.3 The software developed for the SDC consisted of interfacing handler routines for WAC and SAAHS data and display software to display both the weapon aiming symbology and SAAHS status data. Several changes were incorporated to the SDC software as a result of display symbology changes requested by NAVAIR during the flight testing of the WAC.

1.4.6 Production Tooling/Test Equipment

- 1.4.6.1 During WAC development, production peculiar tooling and test equipment was developed to provide for production and fabrication of the WAC.
- 1.4.6.2 The peculiar tooling developed and fabricated for the WAC consisted of the following:
 - a. Three position WRA vibration test fixture
 - b. SRA vibration test fixture
 - c. Heat sink and wedgelock bonding fixtures
 - d. Cable harness fixture
- 1.4.6.3 The peculiar test equipment developed and fabricated for the WAC consisted of the following:
 - a. WAC/AVQ-30 burn-in controller
 - b. WAC BIT monitor
 - c. WAC data bus monitor
 - d. Power supply test set
 - e. Power supply A1 module test set
 - f. Power supply A2 module test set
 - g. Power supply A3 module test set
 - h. Power supply A4 module test set

1.5 Detail Factual Data

1.5.1 Design Milestones

1.5.1.1 In October 1978, a preliminary design review was held. This review was used to assess the effectiveness of development of the WAC in lieu of conversion of IWAC to the Phase II configuration. It had become evident to the contractor that, from both a cost and performance standpoint, the conversion of the IWAC was not practical. Advantages of the WAC in lieu of IWAC conversion to Phase II was as follows:

- a. Smaller weapons CEP due to:
 - o Longer word length (16 bits)
 - o Higher processing speed (8 MHz)
 - o Improved A/D conversion methods
 - o Improved input signal conditioning and filtering
 - o Elimination of D/A conversion
 - o Improved software structure
- b. Improved reliability and maintainability.
- c. Commonality to the SDC
- d. Improved logistics
- e. Reduced cost of ownership

As a result of this design review, the decision by NAVAIR was to pursue development of the WAC by modification of the IWAC to IWAC Phase II modification contract.

1.5.1.2 In November 1978, a draft Statement of Work (SOW) for WAC development was prepared. This SOW was revised numerous times as a result of design review meetings with NAVAIR. The final SOW enforced for the WAC development was dated 28 November 1979.

1.5.1.3 By April 1979, all of the design guidelines for the WAC were in a firm form. The hardware partitioning for the WAC was complete and the digital interface protocol between the WAC and SDC was selected. Full scale hardware and software design and hardware breadboarding was underway. The long lead time material required for WAC fabrication was placed on order. A Digital Equipment Corporation MINC11 minicomputer was selected as the controller for the WAC WRA test set and dynamic simulator. Aircraft wiring changes to facilitate WAC installation was defined and provided to the MacDonald Aircraft Company. The system requirement for the WAC Built-in-Test (BIT) fault indicators were defined and the required hardware design started.

- 1.5.1.4 In May 1979, the first SRA for the WAC utilizing multiwire technology was complete. Extensive testing by the contractor and an independent outside test lab was performed on the SRA to evaluate the mechanical and thermal characteristics of the multiwire design with extremely positive results. The multiwire system proved to be mechanically and thermally superior to the multilayer system for Printed Wiring Board (PWB) design. The multiwire PWB also offered a shorter lead time, less drafting time and a reduced material cost.

The I/O scaling factors for the WAC were also defined in May. This document allowed the I/O software module design to begin.

- 1.5.1.5 In August 1979, a customer design review was held. During the design review it was pointed out that the electrical design for the WAC was complete and the engineering brassboard was fabricated and tested. Software test and debug had been started using the engineering brassboard.
- 1.5.1.6 In November 1979, the WAC Critical Design Review was held. It was presented to NAVAIR that the WAC engineering model fabrication had been completed and was undergoing hardware test and debug. The WAC software development was 80% complete, however, new requirements for a reflected CCIP symbol and display boundary limitation introduced additional software effort.
- 1.5.1.7 In March 1980, the WAC WRA test set hardware design was completed and parts and materials placed on order. The WAC was fitted with a new PROM and Timing module which increased the available program storage from 8K words to 16K words. The WAC weapon delivery accuracy error analysis was completed and added to the equipment specification. The WAC and SDC were subjected to interface testing including display of the CCIP symbology.
- 1.5.1.8 In April 1980, the WAC operational software was completed and awaiting dynamic testing. WAC engineering prototypes one and two were in the final stages of assembly.
- 1.5.1.9 In June 1980, the WAC engineering model was shipped to the NATC, Patuxent River, for the purpose of test and checkout of the instrumentation package to be used during the Naval Technical Evaluation (NTE) of the WAC. Performance testing of engineering prototype number one was completed and the 48 hour burn-in started.
- 1.5.1.10 In July 1980, WAC engineering prototypes one and two were shipped to the NATC, Patuxent River, for NTE testing. Unit number one was installed in the test aircraft and passed operational ground tests.

- 1.5.1.11 In September 1980, WAC units numbers one and two were returned by the NATC, Patuxent River, and modified to correct CCIP mode guns and rockets display and to incorporate an APU reset signal. Both units were modified and returned to Patuxent River. WAC number three was completed and delivered to the R&M Group for Reliability Development testing.
- 1.5.1.12 In December 1980, WAC improvement modifications were started as a result of requirements by NAVAIR. These modifications were performed under contract number N00019-77-A-350-WW091H.
- 1.5.1.13 By April 1981, WAC improvement modifications were completed and WAC number two and seven were shipped to Patuxent River for testing of the modifications during the AV-8C Phase II BIS trials. Unit number four had been delivered to the R&M group for WAC Reliability Development testing which had begun in January 1981.
- 1.5.1.14 In May 1981, WAC number six was shipped to Patuxent River as part of the SDC Marine Remote Area Approach and Landing System (MRAALS) flight test program.
- 1.5.1.15 In June 1981, WAC numbers two and seven were sent to VX5, China Lake, for the AV-8C Operational Evaluation (OPEVAL) flight test program. WAC number one had been returned from Patuxent River for modification.
- 1.5.1.16 In July 1981, Wac units number five and eight were completed. Unit number five was sent to the R&M group for Reliability Development testing.
- 1.5.1.17 In August 1981, the dynamic testing of the WAC was completed with positive results. WAC number eight was shipped to China Lake to be used as a spare. WAC number nine started Qualification testing.
- 1.5.1.18 In October 1981, WAC number nine successfully completed Qualification testing. The WAC WRA test set was completed and all efforts placed on completion of the SRA test set. The OPEVAL flight test program was complete and the preliminary WAC results were reported as very good.
- 1.5.1.19 In March 1982, the WAC SRA test set was completed. Reliability Development testing of WAC units number three, four and five was completed.
- 1.5.1.20 In April 1982, the WAC Spare SRA's were completed and placed in bonded stock. the WAC Final Engineering report was written for submission to NAVAIR.

1.5.2 Built-in Test Circuits and Software

1.5.2.1 Once each computing frame time (24.516 ms), the WAC tests one of the following:

- a. Analog-to-digital interrupts
- b. Digital interface
- c. APU
- d. Analog-to-digital multiplexer
- e. Power supply
- f. PROM
- g. Random Access Memory (RAM)

For each test, a separate word in memory is designated to store the count of the failures which are detected. Additional memory locations are used to store data which, when interpreted, contains information concerning failure mode and other pertinent data for each BIT subroutine and is used to fault isolate to the SRA level. Each fault storage counter is incremented by one count if the corresponding test is good, and decremented by one count if not. If the counter is already at zero, it is kept at zero by proper operation. When a BIT failure is sensed, the corresponding counter is incremented by one count for each frame during which the failure occurs. If the count of any counter reaches the count of eight, a mechanical fault indicator is tripped and remains tripped until manually reset by maintenance personnel. This indicator is located on the front of the WAC housing. In addition to the tripping of the mechanical indicator, the WAC sends a +28VDC signal to the cockpit Central Warning Panel (CWP) to indicate to the pilot of a WAC BIT failure. This indication is reset only if a power-up clear or master clear occurs within the WAC. Since aircraft power transients may occasionally cause an indicator to trip, to minimize false removals, a green Light Emitting Diode (LED) is also provided in the front of the WAC housing. This LED when illuminated indicates that the WAC current BIT status is in a nonfailure mode, and can be used as a confidence indicator to override the mechanical and pilot warning indicators, and allow the WAC to be kept in service, assuming the Pilot's Confidence Check (PCC) displays on the HUD are normal. The pilot can view two separate test patterns using the WAC test switch and Display Set Control (DSC) mode selection switches. A 16-bit digital BIT status word is latched out to the WAC test connector each computing frame and is used by the WAC WRA test set to aid the test operator in fault isolation of the WAC to the faulty SRA.

1.5.3 Mechanical Design

- 1.5.3.1 The WAC case is a thin wall investment casting with reinforcing ribs to dissipate heat and minimize weight. The case was computer analyzed for static and dynamic deflection stress levels, resonant frequencies and mounting security. Results of the final stress analysis computer run showed no problem areas. During random vibration testing, however, a resonance of the top cover was noted, which induced unwanted vibration to the boards. This was corrected by applying silicon sponge rubber to the inside of the cover. This also served to secure the top edges of the boards which were otherwise unsupported. Additionally it was noted that the rear hold down points which mate to the aircraft rack dagger pins were being damaged due to extended random vibration. This was corrected by incorporation of stainless steel inserts at the hold down points.
- 1.5.3.2 The power supply was designed as an enclosed box replaceable as an SRA unit, to facilitate maintenance and to confine electrical noise and EMI. The power supplies identical to the power supply used in the SDC, thereby reducing cost and additional provisioning requirements.
- 1.5.3.3 All SRA's were designed to plug in, with two wedge lock devices on each board used to secure the SRA in place and ensure good heat transfer from the board heat sink to the case. The wedge locks were modified to prevent the bottom wedge from falling off in the event the screw should be unscrewed too far. A pair of extractors mounted on the top of each SRA was provided to facilitate removal of the board from the connector. The mating connectors on the motherboard assembly were designed to exhibit a degree of float for proper alignment during SRA insertion.
- 1.5.3.4 Heat sinks were bonded to all SRA boards. The main boards use aluminum heat sinks, insulated from the boards by anodizing and by using 0.005 inch glass beads as a filler in the epoxy bond. The power supply boards use tinned copper heat sinks which are insulated from the boards by a 0.010 inch sheet of glass-epoxy board cut to the same pattern as the heat sink.
- 1.5.3.5 A thermal survey of the WAC was performed. The hottest parts were, as expected, in the power supply. Accordingly, special attention was given to heat dissipation of the power transistors and transformers in the power supply. Additionally, it was found that the PROM devices on the PROM and Timing SRA were running quite hot and it was planned to incorporate a different component layout on the WAC production model, however this requirement has been superseded by the request by NAVAIR to use Erasable PROM (EPROM) for WAC production. These devices dissipate far less power than the PROM used in WAC development.

1.5.3.6 Considerable difficulty was experienced with the insulators used between the power supply power transistors and the heat sink. It is necessary to electrically insulate the case of the transistor from ground and hence from the heat sink. The insulator must be a good heat conductor and good electrical insulator, which requirements are somewhat antithetical. Tested were beryllium oxide, mica, anodized aluminum, mylar, kapton, and several formulations of insulators made by the Chomerics Company and the Bergguist Company. The Bergguist insulators were finally chosen although they are subject to slight cold flow, causing the transistor mounting screws to become loose, which, when tightened, strain the solder joints on the PWB. It is necessary to solder the transistors in place only after the mounting has been made, allowed to adjust, then retightened.

1.5.4 ELECTRICAL DESIGN

1.5.4.1 The electrical design of the WAC consists of the following SRA's:

- a. Synchro Transformer Module (A9)
- b. Synchro Rate Module (A1)
- c. Analog-to-Digital Converter Module (A2)
- d. Microcontroller Module (A3)
- e. PROM and Timing Module (A4)
- f. RAM and BIT Module (A5)
- g. APU Module (A6)
- h. Output Interface Module (A7)
- i. Power Supply Module (A10)
- j. Spare (A8)

Detailed factual data for each SRA is contained in Appendix A through H and Technical Development Report TDR 1006.

1.5.5 R&M CONSIDERATIONS

1.5.5.1 Reliability

- 1.5.5.1.1 The predicted MTBF calculated for the WAC is 1895 hours. This compares favorably with the IWAC which has an in-service MTBF of approximately 150 hours. Failures of the in-service WAC subsequent to the burn-in testing which screens out defective components and workmanship, have been limited to one failure in approximately 2500 hours of operation. 1200 of these hours have been in-service hours during the WAC flight test programs. Improvements to the production WAC units will be incorporated as a result of developmental testing which included a 4000 hour Reliability Development test program. These improvements along with improved assembly methods will serve to further reduce failures. A Reliability Development Test Report for the 4000 hour Reliability Development Test was submitted as Data Item A00B.

1.5.5.2 Maintainability

- 1.5.5.2.1 The maintainability of the WAC has been vastly improved over the IWAC by the mechanical, electrical and software design features and by a sophisticated WRA and SRA test system.
- 1.5.5.2.2 The WAC has a test connector which assists in fault isolation to the SRA level without opening up the unit. Each SRA has a test connector which provides test points used in fault isolation to the defective component piece part.
- 1.5.5.2.3 Each WAC SRA has components on one side only to facilitate replacement of parts.
- 1.5.5.2.4 The BIT circuit and indicators help prevent false removals as described under 1.5.2.

1.5.6 TESTS AND ANALYSES

1.5.6.1 Tests performed on the WAC are detailed in Data Items A00A, A00D and A00E. Briefly, the tests include Reliability Development, bench performance, burn-in, environmental, EMI and preflight and flight tests. All of the preproduction units passed the performance and burn-in tests. Three units were subjected to the 4000 hour Reliability Development test. One unit was subjected to the environmental tests, and after completion the unit was refurbished to put it into flight-worthy status. Four units underwent preflight and flight tests. The WAC EMI test was passed by similarity to the SDC and NAVAIR letter 54911B/81102/JGM which referenced TEMEST test report SUBINSURV Patuxent River MD271700Z Jun 1981(S) which states all tests were satisfactory. A test report was submitted under Data Item A002.

1.5.6.2 Test results and data are given in Data Items A00B and A00F.

1.5.6.3 Environmental Tests

1.5.6.3.1 The environmental tests run are described in contract Data Item A00D. The results and data are included in Data Item A00F. Briefly, the following tests were run:

- | | | |
|----|----------------------|--|
| a. | Temperature-Altitude | -54°C, 70,000 feet
+95°C for 16 hours
+30°C, 50,000 feet, 4 hours
+60°C, 50,000 feet
+10°C, 70,000 feet, 4 hours
+35°C, 70,000 feet |
| b. | Vibration | 3 hours each axis at 5.0 g rms, random |
| c. | Acceleration | 3 g's to 7 g's depending on axis direction. |
| d. | Shock | By similarity to SDC |
| | Crash Safety Shock | By similarity to SDC |
| e. | Humidity | By similarity to SDC |
| f. | Temperature Shock | By similarity to SDC |
| g. | Sand and Dusk | By similarity to SDC |
| h. | Salt Fog | By similarity to SDC |

1.5.6.4 Reliability Development Tests

The contract called for reliability development testing to establish a reliability growth potential of the WAC. The reliability testing performed is described in Data Item A00A, Reliability and Maintainability Test Plan Report. The test results of the Reliability Development tests are detailed in Data Item A00B. The environmental test profile used in the test is illustrated by figures three and four.

1.5.6.5 Flight Test

To be furnished by NAVAIR prior to submittal of Final Engineering Report.

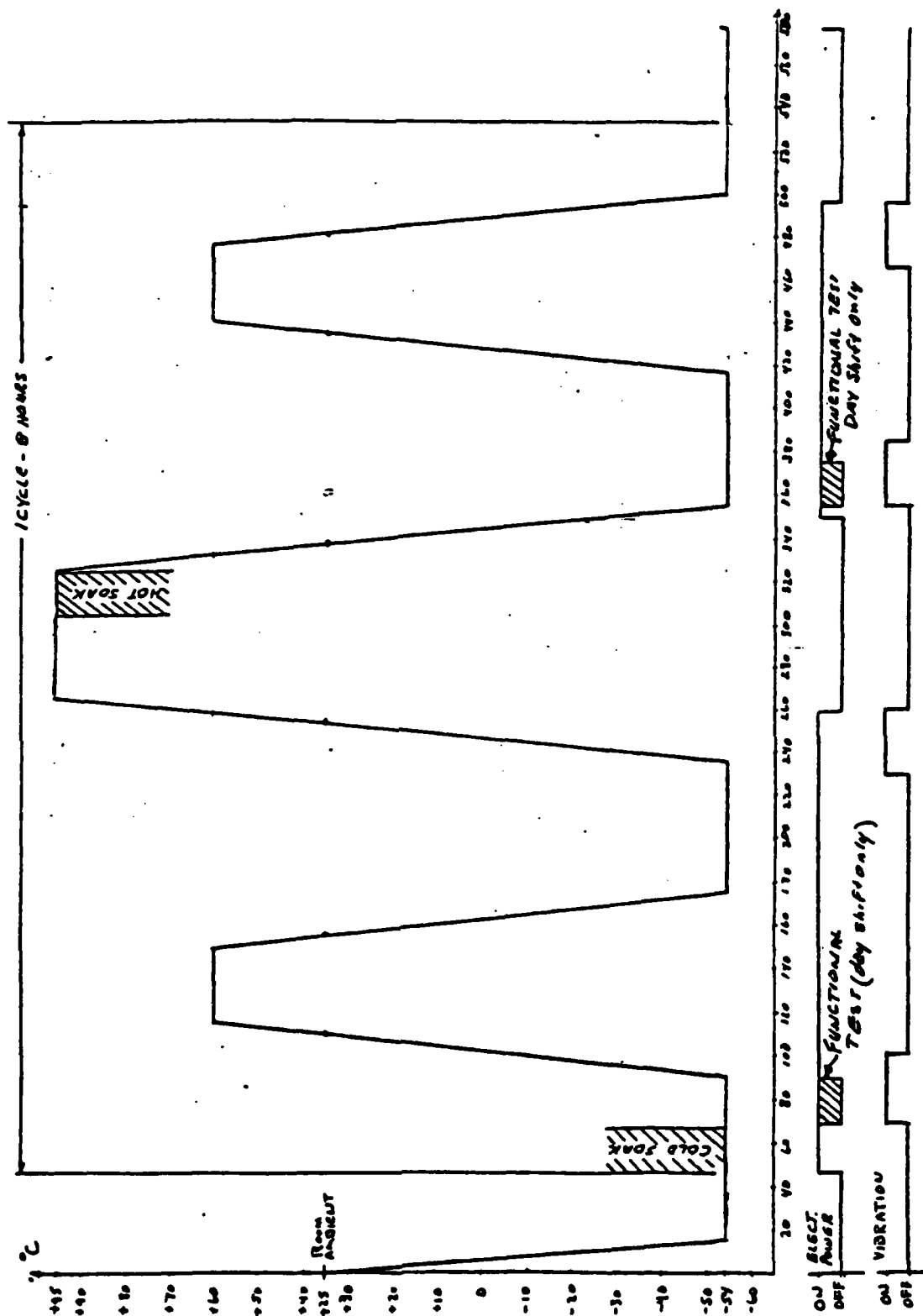
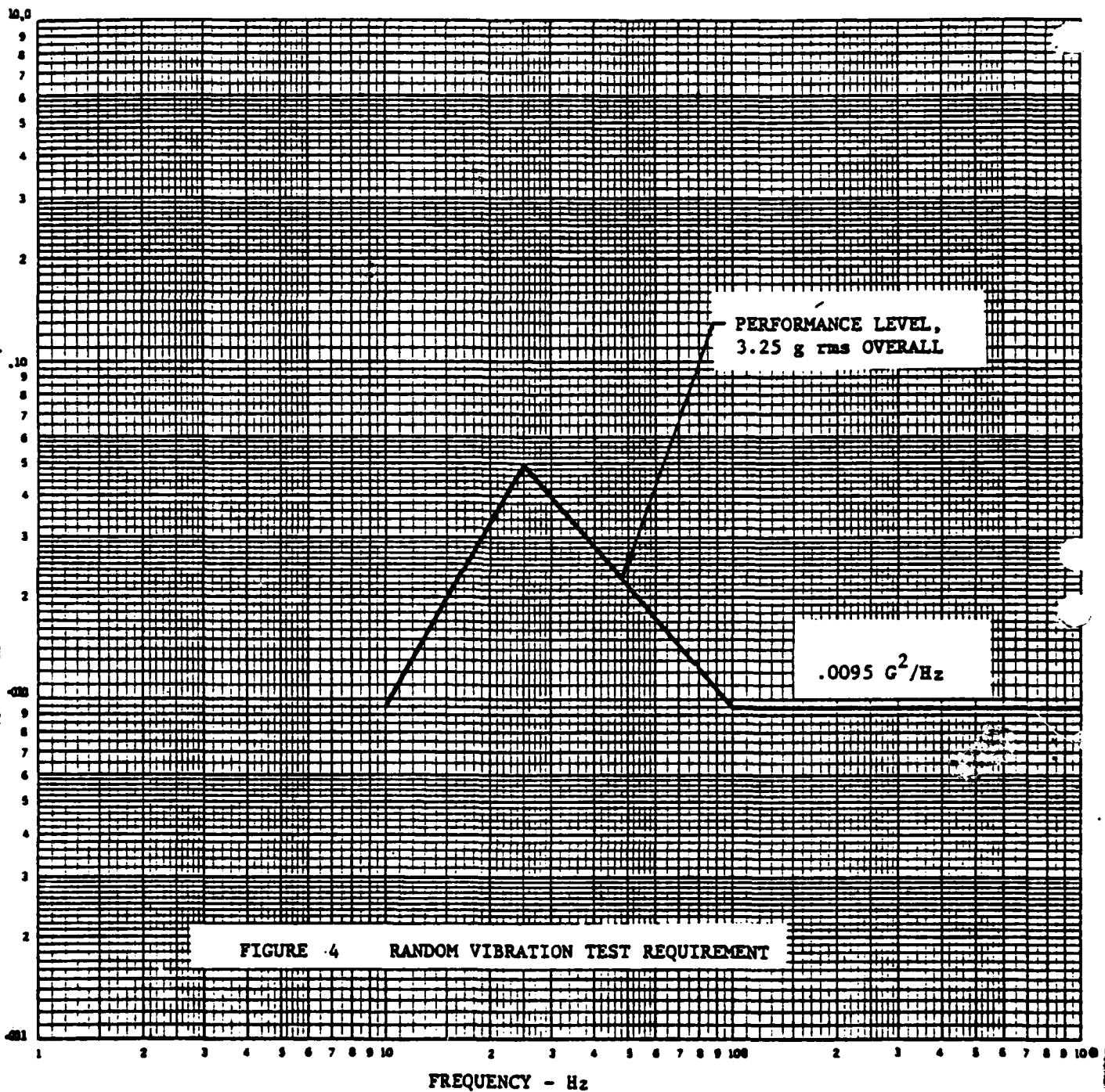


Figure 3. Environmental Test Profile



1.6 CONCLUSIONS

- 1.6.1 The WAC development has provided the AV-8C aircraft with the lowest cost weapon aiming capability available. The WAC has been designed and constructed to accomplish the weapon aiming function accurately with extremely limited passive aircraft sensor data while also providing great flexibility with regard to changes in weapon ballistics.
- 1.6.2 As evidenced by the numerous changes in the WAC SOW, the completion of WAC development has taken more time than anticipated. Although this delay has been an undesirable element of the development, the changes in scope have enabled the contractor to more completely satisfy the customer requirements and hence provide a product to the AV-8C fleet which is more useful, flexible and reliable.
- 1.6.3 The flight testing of the WAC has shown that the weapon aiming accuracy thresholds and goals set by NAVAIR for the AV-8C can be met with a low cost unit without relying on additional sophisticated and expensive aircraft sensors. The incorporation of the use of radio altimeter height as the primary height for weapon aiming, by pilot selection, during flight testing proved to be an excellent enhancement to the weapon delivery accuracy. Although this sensor is not passive, more accurate height data is provided to the WAC and, therefore, improved accuracy and flexibility.
- 1.6.4 The Reliability Development testing of the WAC pointed out several areas of the WAC design which could be changed to improve the WAC's reliability. Although the MTBF results of the testing were below what was anticipated, the contractor is convinced that the factors contributing to the low MTBF will be eliminated in the production WAC by improved workmanship, use of more highly screened components and incorporation of design changes, both at the vendor and contractor level, as documented during the testing.

2.0 RECOMMENDATIONS

2.1 As a result of the WAC development program, the following recommendations are made:

- a. WAC Reliability Development test units number three, four and five be scrapped. This action is recommended because of the extreme and prolonged exposure of these units to environmental testing. It is the opinion of the contractor that useful life and flightworthiness of the units has expired.
- b. All design changes required as a result of findings during developmental, Reliability Development and flight testing be incorporated in the production WAC.
- c. Update the ballistic fit on all weapons which have been modified. This will require weapon ballistic tables and ballistic check data from NWS, Dalgren.
- d. Utilize EPROM technology in the production WAC. This change will greatly reduce the cost of any future changes to the WAC software.

3.0 SUMMARY

3.1 DEVELOPMENT SUMMARY

- 3.1.1 The development of the WAC was begun as a result of a preliminary design review in October 1978. The preliminary SOW for the development was drafted in November 1978, and after several modifications resulted in the SOW dated 28 November 1979, which was used for all work performed. Contract numbers N00019-77-A-350-WW09, N00019-77-A-350-WW091H and N00019-81-G-06290-WW03 were the contracts enforced during all phases of the WAC development and support.
- 3.1.2 The first WAC working model was completed in November 1979. At this time a critical design review was held during which additional changes to the WAC operational software was agreed upon. These changes culminated in the completion of the software in April 1980. Extensive testing of the WAC hardware and software was performed until June 1980, when the WAC engineering model was sent to the NATC, Patuxent River, for test and debug of the instrumentation to be used during NTE flight testing.
- 3.1.3 In July 1980, the first two flight test WAC's were sent to the NATC for test and evaluation. These units were used until September 1980, when they were returned to the contractor to be modified to correct two design deficiencies which were discovered during flight testing. Both units were modified and returned to the NATC for completion of flight tests.
- 3.1.4 As a result of NTE flight tests and simulator testing, a WAC improvement modification program was begun in December 1980. This effort was completed in April 1981, and two WAC's were modified and sent to the NATC for testing during AV-8C Phase II BIS trials. Upon completion of BIS trials the WAC units were sent to VX5, China Lake for AV-8C OPEVAL flight testing in June 1981.
- 3.1.5 The Reliability Development test of the WAC was begun in January 1981, and completed in March of 1982. Various design changes were incorporated in the WAC during this test to improve the unit's reliability. Other design changes required as a result of the testing were delayed until WAC production, due to cost and physical constraints.
- 3.1.6 The test equipment developed for the WAC consisted of a Dynamic Simulator, WRA/SRA Semiautomated test set and numerous design aides and production special test equipment. All test equipment developed was completed by March 1982.
- 3.1.7 The Qualification of the WAC was conducted from August to October 1981. All tests conducted were successfully completed and a test report submitted to NAVAIR.

3.2

SUMMARY OF EQUIPMENT DEVELOPED (Part 1)

The Weapon Aiming Computer (WAC), CP-1444/A, is a microcontroller based digital computer housed in a 1/2 ATR short case which is designed and constructed for convection cooling.

The WAC performs lead angle computing for air-to-air guns and Continuously Computed Impact Point (CCIP) computing for air-to-ground guns, rockets and bombs. The WAC also performs interfacing of aircraft attitude and navigation sensor data for display on a Head-Up Display (HUD).

The WAC is functionally partitioned into nine Shop Replaceable Assemblies (SRA's) and a housing which contains a modular interconnect system. All SRA's are held in place with wedge lock devices and use zero insertion force connections. The unit has a spare SRA position which allows for future expansion capability.

The WAC has been successfully flight tested by the Navy under both controlled and operational conditions. As a result of this testing the WAC is slated for use in the U.S. Marines AV-8 Harrier.

The WAC provides a high degree of mathematical accuracy by performing all internal arithmetic operations in 32-bit floating point arithmetic. The software structure implemented uses a controlling executive for subroutine entry which facilitates maximum maintainability characteristics and program clarity.

3.3

SUMMARY OF EQUIPMENT DEVELOPED (Part 2)

The Weapon Aiming Computer (WAC) CP-1444/A, is a microcontroller based digital computer developed for the United States Marine Corps AV-8C Harrier Aircraft.

The WAC is housed in a 1/2 ATR short case which is designed and constructed for convection cooling. The unit is functionally partitioned into nine Shop Replaceable Assemblies (SRA's) and a modular interconnect system. All SRA's are secured in place with wedge lock devices and use zero insertion force type connectors. The unit is designed with provisions for a spare SRA position allowing for future expansion capabilities.

The functions performed by the WAC include:

- a. Interface of aircraft attitude and navigation sensors.
- b. Lead angle computation for air-to-air guns.
- c. Continuously Computed Impact Point (CCIP) computation for air-to-ground guns, rockets and bombs.
- d. Breakaway warning computation for air-to-ground terrain and weapon fragmentation avoidance.

All output data is digitally transmitted to Head-Up-Display (HUD) for display to the pilot.

All weapon aiming functions performed by the WAC utilize passive aircraft sensors of the AV-8 unless the pilot desires to use radio height in lieu of barometric height for the primary height above target data in the air-to-ground CCIP mode.

When operated in the CCIP mode, the WAC computes positional data for a release cue, in ground axis, based upon the aircraft sensor data and the weapon selected by the pilot for release. The target is tracked along an azimuth steering line which is displayed based upon the computed release elevation depression and the total change in heading required for the pilot to track. This method of display directs the pilot steering such that the aircraft is maintained on its velocity vector and continually computes an across heading aimpoint offset for effects due to the aircraft across heading wind vector or across heading target movement. The in range offset aimpoint required due to wind or target movement must be compensated for by the pilot. All outputs are displayed on the HUD and the pilot manually releases the weapon when the CCIP release cue coincides with the target or the in range offset aimpoint.

The WAC performs all mathematical operations in 32-bit floating point arithmetic which provides a high degree of computational accuracy. Square root and trigometric functions are performed in single operations by use of two Arithmetic Processor Units (APU's) which can be operated in parallel for concurrent arithmetic processing.

The software structure implemented in the WAC consists of an executive program which controls subroutine entry based upon mode selection by the pilot. This structure facilitates maximum maintainability characteristics and program clarity.

The WAC was flight tested by the Navy under both controlled and operational conditions. As a result of the testing performed, the WAC should be approved for fleet use and is slated for introduction on the AV-8C Harrier.

SYNCHRO RATE TECHNICAL DESCRIPTION

APPENDIX A

SYNCHRO RATE MODULE

1.0 INTRODUCTION

The Synchro Rate Board was developed to synchronously preprocess and demodulate analog data that has been resolved from synchro data for subsequent conversion to digital data. This is accomplished by scaling and sampling incoming data. Filtering is provided for analog outputs to remove ripple induced by airframe disturbances.

The Synchro Rate board contains three types of analog channel preprocessors and a Phase Lock Loop circuit for accommodating variations in the modulation reference frequency. One analog channel type provides for the scaling, sample and holding of data such as resolver heading and tacan. A second channel adds the capability of the analog channel previously described and provides the capability of injecting precise analog voltage at the analog channel input for use during Pilot's Confidence Checks (PCC). The third type of channel adds a low pass filter to the output of the analog sample to essentially convert a low frequency ac input to a dc output.

The DIWAC input analog signals and output voltage ranges after analog processing are given in Table 1.

TABLE 1. ANALOG INPUT/OUTPUT CHARACTERISTICS

Signal	Input	Output
Sine Pitch	0 to 11.8 rms at 400 Hz	0 to ± 9.5 Vdc
Cosine Pitch	0 to 11.8 rms at 400 Hz	0 to ± 9.5 Vdc
Sine Roll	0 to 11.8 rms at 400 Hz	0 to ± 9.5 Vdc
Cosine Roll	0 to 11.8 rms at 400 Hz	0 to ± 9.5 Vdc
Sine Heading	0 to 11.8 rms at 400 Hz	0 to ± 9.5 Vdc
Cosine Heading	0 to 11.8 rms at 400 Hz	0 to ± 9.5 Vdc
Sine Tacan	0 to 11.8 rms at 400 Hz	0 to ± 9.5 Vdc
Cosine Tacan	0 to 11.8 rms at 400 Hz	0 to ± 9.5 Vdc
Pitch Rate	0 to 4 Vrms (20°/sec) at 400 Hz	0 to ± 9.5 Vdc
Yaw Rate	0 to 4 Vrms (20°/sec) at 400 Hz	0 to ± 9.5 Vdc
Roll Rate	0 to 1.8 Vrms (40°/sec) at 400 Hz	0 to ± 9.5 Vdc
Reference	3 Vrms at 400 Hz	0 to ± 9.5 Vdc

2.0 SYNCHRO RATE BOARD KEY FEATURES

- a. Scaling, filtering and sampling of analog signals.
- b. Demodulation of resolved synchro data.
- c. Synchronization of analog signal sampling with reference to modulation reference frequency.
- d. Selection of fixed analog values instead of actual values for confidence checking of analog channels and subsequent equipment.
- e. The incorporation of a Phase Lock Loop (PLL) for compensation of modulation frequency variations
- f. The sampling hold time is much greater than the time between sampling intervals.
- g. The sampling control can be externally controlled.
- h. Adequate test points are available for monitoring circuit operation.
- i. High impedance sample and hold inputs are protected.
- j. Sample and hold circuits can be temperature compensated.
- k. Provisions are made for select-in-test (SIT) components for increasing channel scaling accuracy.

3.0 FUNCTIONAL DESCRIPTION

The use of aircraft sensor data for solving dynamic flight equations requires the digitization of this data. Certain aircraft data elements are available as synchro data and converted to resolver data. The resultant data is modulated, typically by a 400 Hz reference, and is not in a form suitable for direct digitization and non-ambiguous system accuracy. This analog data must therefore be preprocessed. The preprocessing of conditioning of this analog data must consider demodulation of the analog data, variations in the modulation frequency, constant time domain analog sampling, scaling, ripple introduced by airframe disturbances, and confidence checking.

The Synchro Rate Board is capable of performing the following analog signal conditioning processes:

- a. The translation of plus and minus peak voltage values to a scaled range of -9.5 volts for negative input voltage peaks and +9.5 volts for positive voltage peaks inputs.

- b. The demodulation of analog data by sampling and holding analog inputs at the same instant in time, preferable during the positive peak of one phase of the modulation frequency (400 Hz).
- c. The phase locking of one phase of the modulation frequency to minimize the effect of modulation frequency variations.
- d. Filtering of selected analog samples that essentially convert an ac frequency to a dc voltage.
- e. The injection of known analog voltage values into selected analog channels for use during confidence checking.

Figures 1, 2, and 3 depict simplified block diagrams of Synchro Rate board functions. Figure 1 is a block diagram of the on-board PLL used for generating an analog sample pulse. Figure 2 is a block diagram of converted synchro data that does not require output filtering. Figure 3 is a block diagram of the Analog Rate Conditioners.

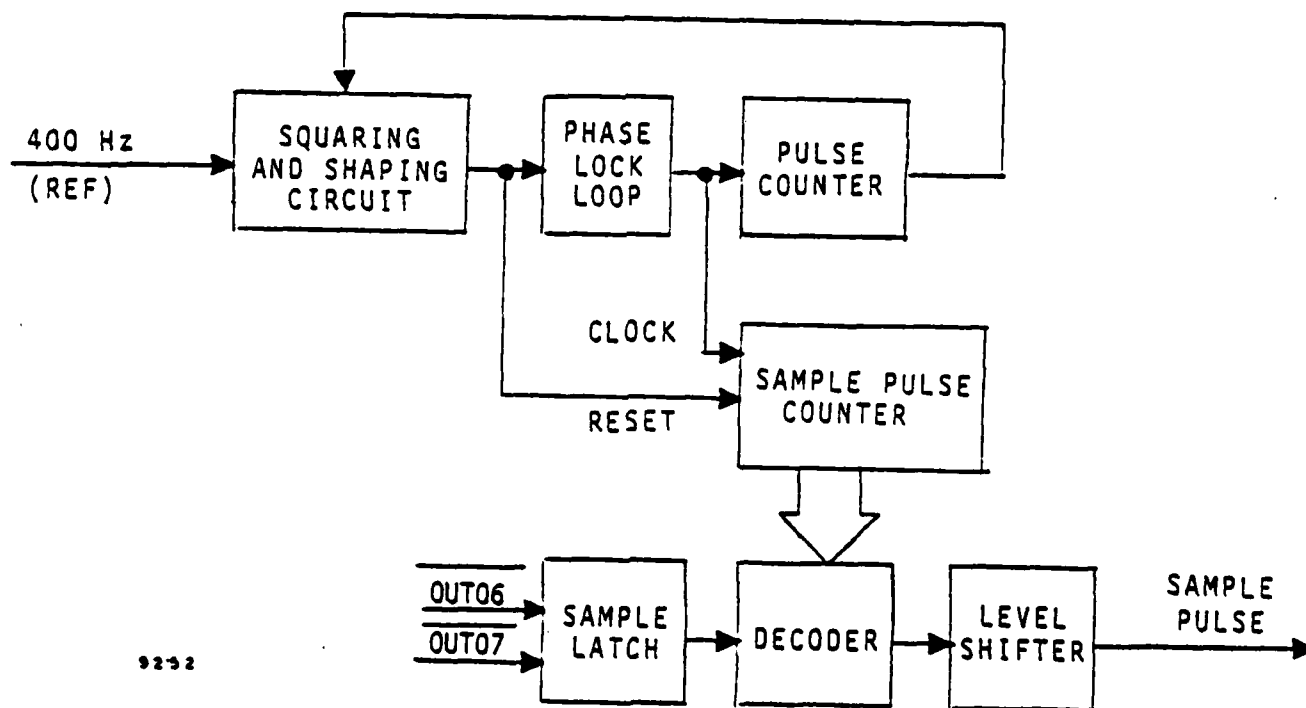


FIGURE 1. PHASE LOCK LOOP BLOCK DIAGRAM

3.1 Phase Lock Loop (Figure 1)

A phase of the modulation frequency (400 Hz) is passed through a squaring and shaping circuit which causes the ac sine wave to be converted to 0 volt to 5 volt square wave. This square wave is applied to the PLL and sample pulse counter. The output clock from the PLL is 256 x the input frequency or 102.4 KHz for a 400 Hz frequency input (400 Hz x 256). The PLL clocks are accumulated in the pulse counter. After 256 counts are accumulated, a pulse is returned to the PLL for comparison with the 400 Hz square wave. The frequency output clock of the PLL is changed when a phase error occurs, i.e., the frequency of the reference voltage is changed.

The sampling period counter is reset during the beginning of the negative cycle of the ac reference (negative zero crossing). PLL clock pulses are accumulated in the sample pulse counter. The decoder is enabled when a count of 64 ± 8 is reached in the sample pulse counter. (64 counts is equivalent to the time when the positive peak of the reference voltage occurs.) If the sample latch is enabled by an OUT06 I/O command, the decoded sample pulse of approximately 150 usecs duration is output from the decoder and level shifted to a 0 volt to -15 volt pulse for use by the on-board sample and hold demodulators.

3.2 Synchro Conditioners (Figure 2)

The non-filtered analog conditioners are provided for Heading (Hd), Tacan, Roll, and Pitch resolver analog (sine and cosine). Confidence checking of pitch and roll resolver inputs is provided by analog switches. Sensor analog voltage is transferred to the output of the analog switches unless confidence checking is required. The fixed analog values are transferred to the output of the analog switches. Confidence checking is enabled by input signal PCC.

All analog signals are simultaneously inputted to sample and hold circuits. Voltages are sampled when the sample pulse occurs with the respective voltages values held until the next sampling period.

3.3 Rate Analog Conditioners (Figure 3)

Rate Analog Conditioners are provided for Roll Rate, Pitch Rate, and Yaw Rate. Each channel is equipped with an analog switch for selecting sensor data or fixed analog data when confidence checking is required (PCC), a scaler for output analog voltage range compatibility, a sample and hold circuit for sensor demodulation and an output filter for removing ripple caused by airframe disturbances.

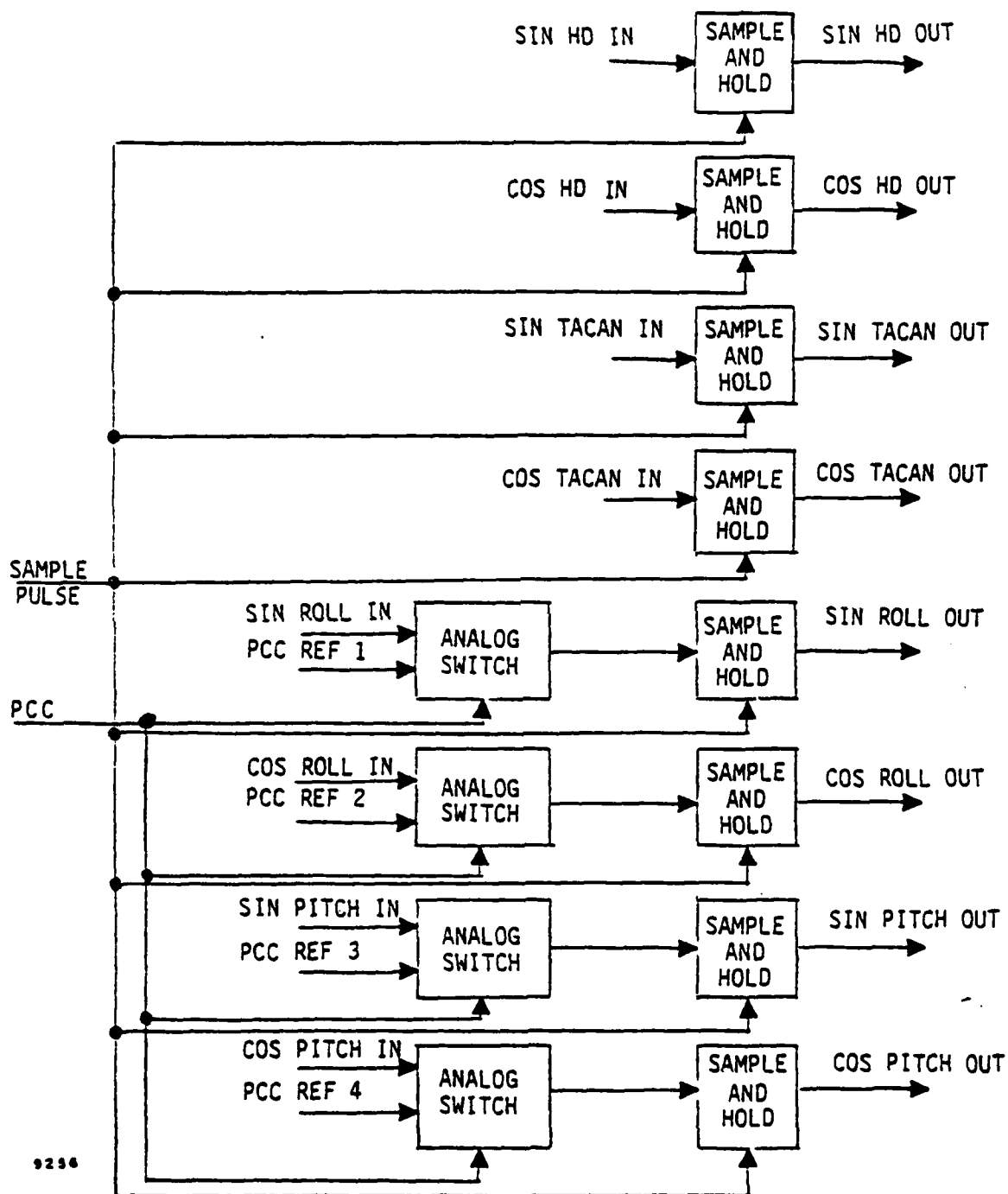


FIGURE 2. NON-FILTERING ANALOG CONDITIONERS

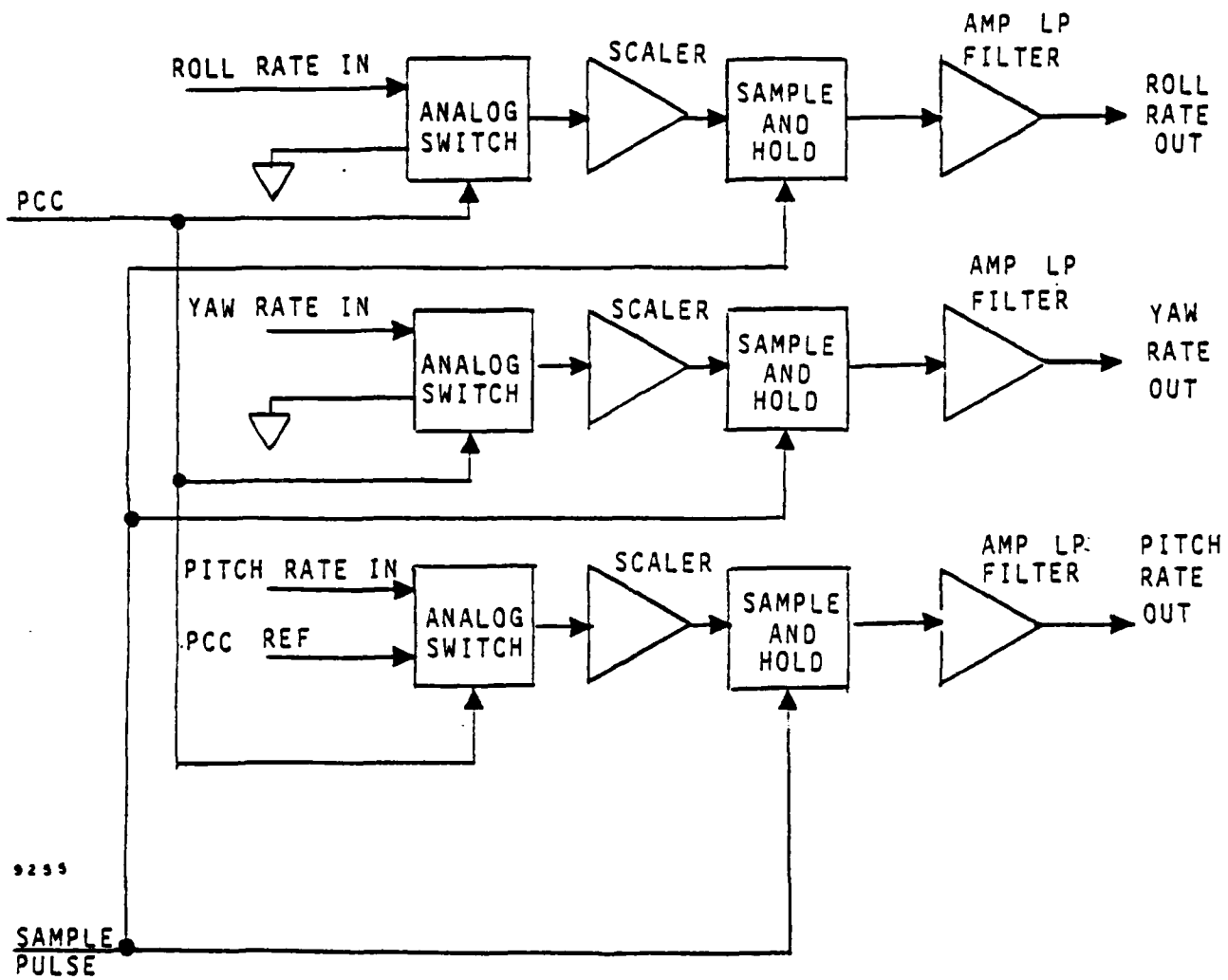


FIGURE 3. RATE CONDITIONERS BLOCK DIAGRAM

3.4 Detailed Theory of Operation

3.4.1 Phase Lock Loop

The PLL is used to track a 400 Hz $\pm 10\%$ reference signal. The 400 Hz reference signal is converted to a square wave by amplifier U22-6. The square wave output is clipped to +4.7 volts and -0.6 volts by resistor R88 and zener diode CR12 and converted to 0 and 5 volt logic levels by And Gate U23-12 and is input to the PLL (U24). (See Appendix A for PLL specifications.)

The PLL (U24) VCO is biased to provide 256 clocks per period of the reference frequency or 9.765 usec period clocks. The 256 clock periods are counted in U27 and U26. When 256 counts are obtained CP2 (U26-11) goes high and is applied to the phase comparator input of PLL (U24-3). This pulse is compared with the reference pulse and the error output is on PC2 (U24-13). Components, resistor R22 and capacitor C58 provide an error time constant for providing a PLL VCO bias change, i.e., as the input frequency reduces, the VCO frequency is reduced; whereas an increase in input reference cause the VCO frequency to increase. The PLL is biased for reference frequencies of 400 Hz $\pm 10\%$.

Figure 4 contains the timing relationships of the reference frequency. The free running clock frequency of the VCO is shown in Equation 1.

Equation 1:

$$\text{Reference Frequency} = 400 \text{ Hz}$$

$$\frac{\text{VCO}}{\text{Reference Frequency Period}} = 256$$

$$\text{VCO} = 256 \times 400 \text{ Hz} = 102.4 \text{ KHz}$$

The free-running VCO clock period is shown in Equation 2.

Equation 2:

$$T_{\text{VCO}} = \frac{1}{\text{VCO}}$$

where:

$$\text{VCO} = 102.4 \text{ KHz}$$

$$\frac{1}{\text{VCO}} = 9.765 \text{ usecs}$$

The sample pulse is set at ± 8 counts located at the center of the positive voltage peak of the reference frequency or at 64 ± 8 counts. The time duration of this pulse is shown in Equation 3.

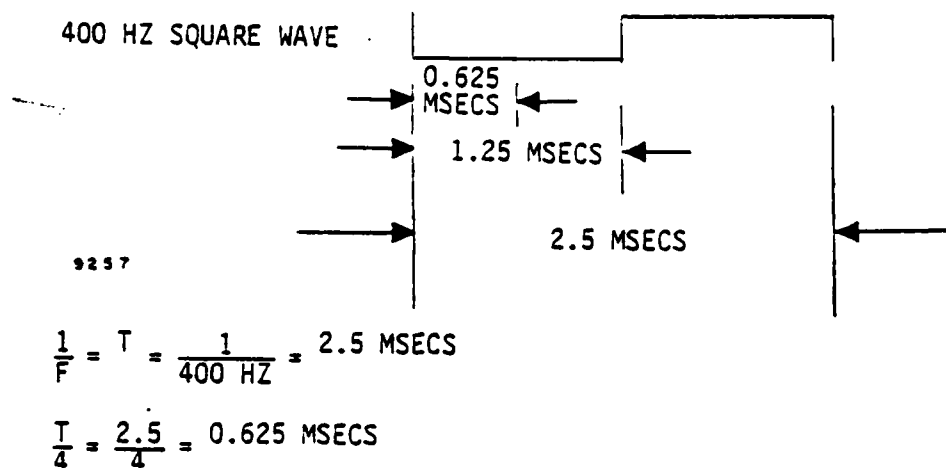


FIGURE 4. REFERENCE FREQUENCY TIMING RELATIONSHIPS

Equation 3:

$$\frac{T_{RF} + 8 \times T_{VCO}}{4} - \frac{T_{RF} - 8 \times T_{VCO}}{4} = \text{Sample pulse Equation 4}$$

where:

$$T_{RF} = 2.5 \text{ msecs}$$

$$T_{VCO} = 9.765$$

$$\frac{2.5 \text{ msec} + 8 \times 9.765 \text{ usec}}{4} - \frac{2.5 \text{ msec} - 8 \times 9.765 \text{ usec}}{4} = 156.25 \text{ usec}$$

The sample pulse period is obtained by counters U28 and U29 and the decoder comprised of inverter U25-5/6 and U25-8/9 and And Gate U23-6. Counters U28 and U29 are held in a preset condition whenever the reference frequency square wave is low, U28-9 and U29-9. Counter U28 is preset to an 8 and U28 is preset to a 0. When the leading edge of the reference frequency occurs, the preset goes high and enables U28 and U29 to count clock pulses. When counter U28 is counted to a 4, Q2 is high, 56 clocks have been counted ($2^6 - 8$ preset counts). Counter U29 remains at a 4 (Q2 high) until counter U29 counts 16 more VCO clocks and increments counter U28. Therefore, counter U28 remains at a 4 from counts 56 to 72.

When counter U28 is at a count of 4, And Gate input U23-3 goes high, counter outputs Q1 (U28-13) and Q0 (U28-14) are low and inverter to highs by inverters U25-5/6 and U25-8/9. And Gate output U23-6 goes high and enables And Gate U23-9/10. The second And Gate enable occurs when latch U30-5 goes high. The timing relationship for the sample pulse is shown in Figures 5 (a and b).

I/O command OUT06 goes low when active and returns high causing a clock at latch U30-3, setting latch U30-5. This latch is reset by the active low at I/O command OUT07.

When enabled, And Gate output U23-8 goes high for the duration of the sample period and initiates a level shifter by causing transistor Q27 to turn on. The ground at the collector of Q27 causes transistor Q28 to conduct. The collector of transistor Q28 goes from ground to -15 volts when turned off thereby completing the shift from 0 volts to -5 volts.

NOTE: The sample and hold timing constant is much greater than the sample pulse; however, the period of the sample pulse is constrained by the peak of the reference frequency. This condition is overcome by permitting numerous sample pulses to occur during any sample pulse enabling cycles (Latch U30-5 remains on for approximately 10 sampling periods).

3.4.2 Sample and Hold Circuits

Circuit configurations U7-U10 and U13, U19 and U23 are non-temperature compensated sample and hold circuits. Circuit configurations U2, U3, U5 and U6 are temperature compensated sample and hold circuits.

Using circuit configuration U9 as an example, the sample pulse turns on devices Q17 and Q18 and cause capacitor C26 to charge. The impedance of the feedback loop (resistor R41 and capacitor C26) is given in Equation 5 and the gain of U9 is given in Equation 6.

Equation 5:

$$Z_{\text{Feedback}} = \frac{R_{42} \cdot 1/C_{26}S}{R_{42} + 1/C_{26}S} = \frac{R_{42}}{R_{42} C_{26} S + 1}$$

Equation 6: Gain

$$\text{Gain} = \frac{Z_{\text{feedback}}}{R_{39}} = \frac{R_{42}}{R_{39}} \cdot \frac{1}{R_{42} C_{26} S + 1}$$

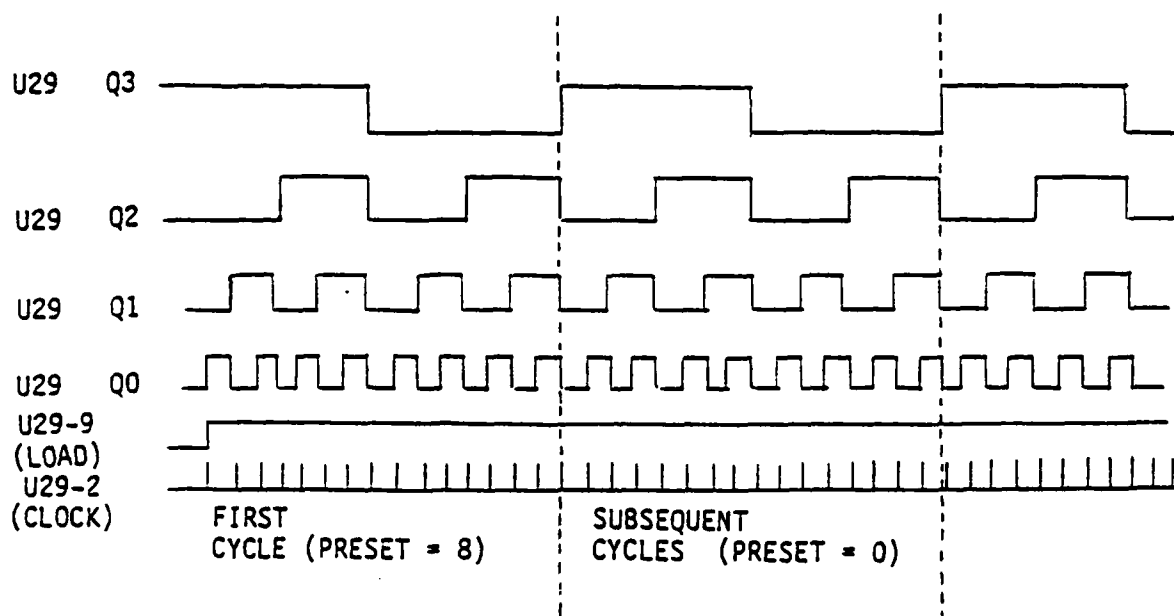


FIGURE 5(a) U29 COUNTER TIMING DIAGRAM

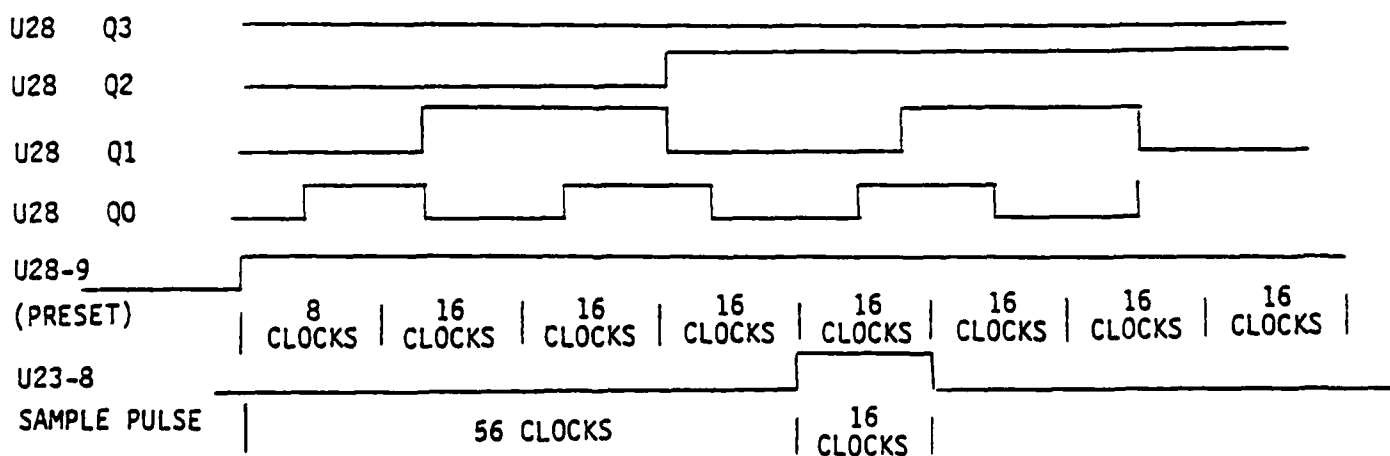


FIGURE 5(b) SAMPLE PULSE TIMING

$$\text{Gain} = \frac{e_o}{\Delta e_{IN}} = \frac{5.76 \text{ K}\Omega}{10 \text{ K}\Omega} \cdot \frac{1}{\frac{5.76 \text{ K}\Omega \cdot 0.047 \times 10^{-6}}{S} + 1} = \frac{2127.744}{S + 3694}$$

$$e_o = 0.576 \Delta e_{IN} (1 - e^{-3694t})$$

where:

$$\Delta e_{IN} = 0.0 \text{ to } 0.05 \text{ volts}$$

Figure 6 is a graph which depicts the voltage change of the holding capacitor versus time with a 25 millivolt step function for the gain of Equation 6.

The theoretical gain through the sample and hold circuits without trimming resistors is given in Table 2. Trimming resistors are provided to adjust the gain for a ± 9.5 volt peak to peak output.

Due to the timing constant, several successive samples are required before charging of the holding capacitor can be assured. Devices Q17 and Q18 offer a high impedance when not turned on to provide the holding capacitor with a long decay time constant. Circuits U2, U3, U5, and U6 have devices in series with the feedback resistor (such as Q1 in circuit U2) for temperature compensation.

3.4.3 Analog Switches

Analog switches U1, U4, U11 and U18 are SPST equivalent switches which require a high PCC input to switch from sensor data to confidence data. See Appendix B for additional information.

TABLE 2. THEORETICAL GAIN OF SAMPLE AND HOLD CIRCUITS

SAMPLE AND HOLD CIRCUIT	GAIN	INPUT SIGNAL (VOLTS)	OUTPUT SIGNAL (WITHOUT TRIM)
U7-U10	$\frac{5.76 \text{ K}\Omega}{10 \text{ K}\Omega} = .576$	11.8 rms (16.69 peak)	± 9.61 volts
U2, U3, U5, U6	$\frac{5.76 \text{ K}\Omega}{10 \text{ K}\Omega} = .576$	11.8 rms (16.69 peak)	± 9.61 volts
U13	$\frac{18 \text{ K}\Omega}{5.1 \text{ K}\Omega} = 1.529$	1.8 rms (2.545 peak)	± 8.9 volts
U16, U20	$\frac{15.8 \text{ K}\Omega}{10 \text{ K}\Omega} = 1.58$	4.0 rms (5.656 peak)	± 8.93 volts

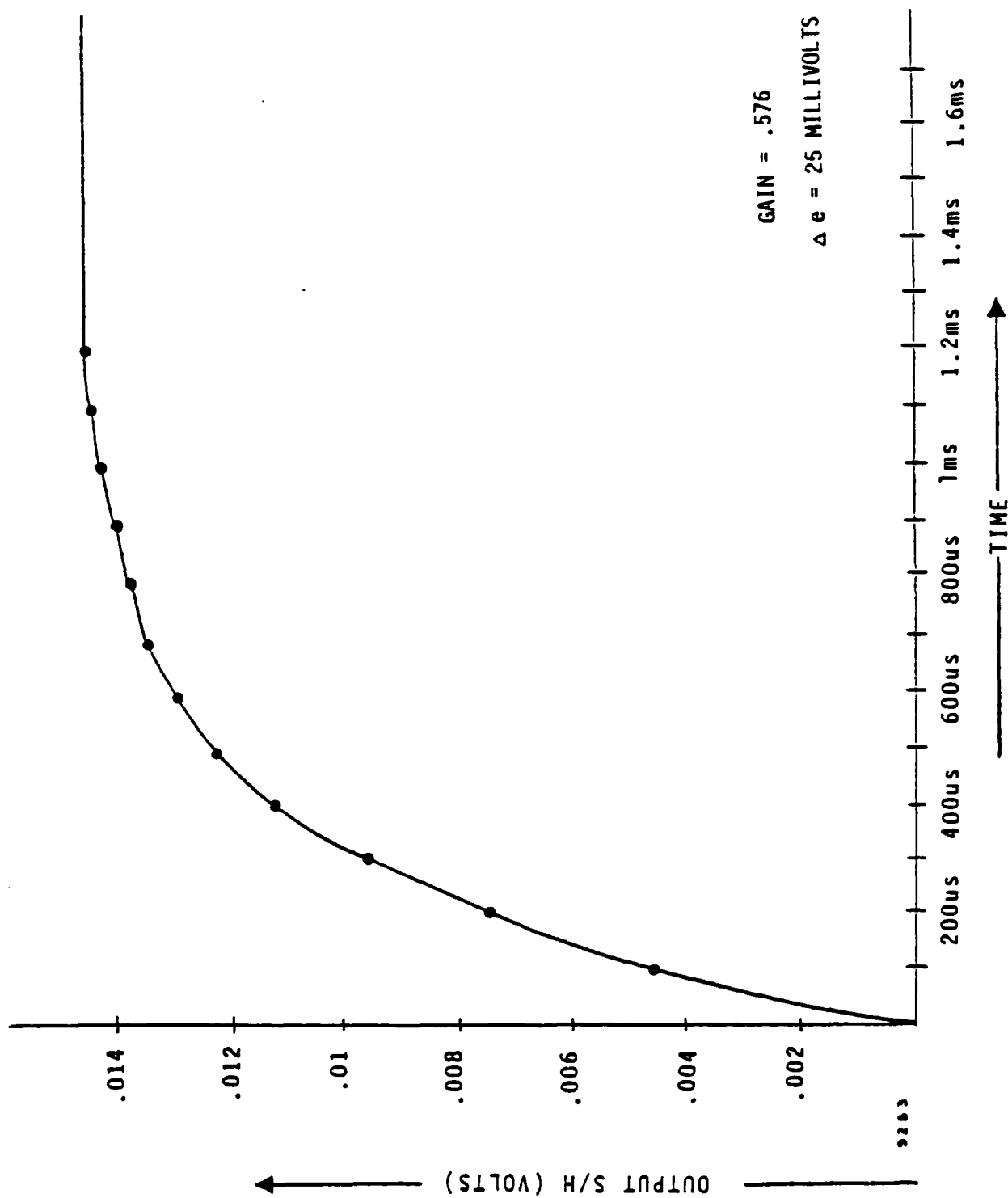


FIGURE 6. SAMPLE AND HOLD CHANGE RATE

3.4.4 Buffer Amplifiers

Amplifiers U12, U15 and U19 provide a high impedance unit gain circuit for buffering incoming analog signals.

Circuits U14, U17 and U21 provide a low pass filter for the 3 different rate input circuits.

4.0 INPUTS/OUTPUTS

The Synchro Rate board has three connectors; signal connector P1A, P1B and test connector J1. Pinouts and functions are shown in Tables 3 through 5 respectively.

5.0 POWER CHARACTERISTICS

Table 6(a) delineates the type of device and typical maximum power consumption for each device. Table 6(b) summarizes the active device power requirements for the synchro rate board.

TABLE 3. P1A PIN CONNECTIONS (SYNCHRO RATE)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	Digital Ground	28	
2	Digital Ground	29	
3		30	
4		31	Sin Pitch In
5		32	Cos Pitch In
6		33	Sin Hd In
7		34	Cos Hd In
8		35	Sin Roll In
9		36	Cos Roll In
10		37	Sin Tacan In
11		38	Cos Tacan In
12		39	Roll Rate In
13		40	Yaw Rate In
14		41	Pitch Rate In
15		42	Sin Roll Out
16		43	400 Hz Ref
17		44	
18		45	
19		46	
20		47	
21		48	
22		49	
23		50	
24		51	
25		52	
26		53	+5 Volts
27		54	+5 Volts

TABLE 4. P1B PIN CONNECTIONS (SYNCHRO RATE)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	+5 Volts	28	+15 Volts
2	+5 Volts	29	+15 Volts
3		30	
4		31	-15 Volts
5		32	-15 Volts
6		33	
7		34	+10 Volts
8		35	
9		36	-10 Volts
10		37	
11		38	Sin Pitch Out
12		39	Cos Pitch Out
13		40	Sin Hd Out
14		41	Cos Hd Out
15	<u>OUT 06</u>	42	Sin Roll Out
16	<u>OUT 07</u>	43	Cos Roll Out
17		44	Sin Tacan Out
18	Roll Rate Out	45	Cos Tacan Out
19	Yaw Rate Out	46	Sample Pulse
20	Pitch Rate Out	47	
21		48	
22		49	
23		50	
24	PCC	51	
25		52	
26		53	Signal Ground
27		54	Signal Ground

TABLE 5. J1 PIN CONNECTIONS (SYNCHRO RATE)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	Sample Pulse 2 ²	28	
2	Phase Lock Loop Output Clock	29	
3	Sample Pulse Enable	30	
4	Sample Pulse	31	
5		32	
6		33	
7		34	
8		35	
9		36	
10		37	
11	Roll Rate Scaled Analog	38	
12		39	
13		40	
14	Roll Rate Sampled Analog	41	
15	Yaw Rate Sampled Analog	42	
16	Pitch Rate Sampled Analog	43	
17		44	
18		45	
19		46	
20		47	
21		48	
22		49	
23		50	
24		51	
25		52	
26		53	
27		54	

TABLE 6(a). DEVICE TYPICAL POWER REQUIREMENTS

DEVICE NAME	DEVICE TYPE	CIRCUIT DESIGNATION	POWER (MILLIWATTS)			
			+5 VOLTS		±15 VOLTS	
			TYP	MAX	TYP	MAX
4 Bit Counter	54LS161	U26-U29	92.5	157.5		
Hex Inverter	54LS04	U25	12.0	22.5		
Dual D FF	54LS74	U30	20.0	40.0		
TR1-3 Input And Gate	54LS11	U23	13.0	25.5		
OP Amp	LM107	U2, U3, U5-U10 U12-U17 19-22			27.0	45.0
Analog Switch	HI-5051	U1, U4, U11, U18 U24			1.5	4.5

TABLE 6(b). SUMMARIZATION OF SYNCHRO RATE BOARD POWER REQUIREMENTS

DEVICE NAME	CIRCUIT DESIGNATOR	QTY	POWER (MILLIWATTS)			
			+5 VOLTS		±15 VOLTS	
			TYP	MAX	TYP	MAX
4 Bit Counter	U26-U29	4	370	630		
Hex Inverter	U25	1	12	22.5		
Dual D FF	U30	1	20	40		
TR1-3 Input And Gate	U23	1	13	25.5		
Op Amp	U2, U3, U5-U10 U12-U17, U19-U22,	18			486	810
Analog Switch	U1, U4, U11, U18 U24	5			7.5	22.5
TOTAL 5 Volts			415	718		
TOTAL +15 Volts					493.5	832.5
TOTAL +15 Volts					493.5	832.5

A/D TECHNICAL DESCRIPTION

APPENDIX B

ANALOG TO DIGITAL CONVERTER MODULE

1.0 INTRODUCTION

The Analog to Digital (A/D) Converter Board was developed to provide the conversion of instrument sensor data, represented as voltage levels, to digital words. These words are interpreted by a system processing function, the Microcontroller (μ C), which is integral to the DIWAC. The A/D converter was designed specifically for application to the DIWAC; however, the concept and basic hardware are applicable to many other interface requirements.

The design incorporates standard electronic parts for functional implementation using hybrid and Large Scale Integration (LSI) circuits where justified. Where possible, functions were integrated into the μ C to provide a reduction of interface hardware. The total interface is a combination of hardware and software.

2.0 A/D CONVERTER BOARD KEY FEATURES

Key features of the A/D converter are as follows:

- a. Input transient protection
- b. 40 amplifiers for analog scaling and impedance buffering
- c. 48 channel analog multiplexer
- d. 12 bit data conversion
- e. Full 48 channel conversion in 14 msec
- f. Selection of predetermined analog input data for confidence checking
- g. Inversion of MSB for simplified μ C data manipulation
- h. Conversion BIT
- i. Programmable operation via the μ C

3.0 FUNCTIONAL DESCRIPTION

The A/D Converter consists of a 48 channel analog buffer and multiplexer coupled to a 12-bit A/D converter. Channel selection and conversion start are software controlled which provides the user program complete command of interface functions.

3.1 Implementation

The A/D Converter function was implemented with an integration of hardware and software. A μ C data output is required to select the proper multiplexer channel and start the conversion cycle. Internal hardware logic completes the conversion process and generates an interrupt to the μ C. The μ C reacts, fetches the digital data, and resets the hardware in preparation for a new conversion. Data fetched by the μ C is processed by an interrupt handling routine. Table 1 summarizes the input voltages and scaling factors.

3.2 Converter Hardware

The following hardware implemented circuit functions are shown in Figure 1.

- a. Buffer Amplifiers
- b. Multiplexer
- c. Address Latch and Decode
- d. Sample and Hold
- e. A/D Converter
- f. Bus Transmitter
- g. Timing and Control

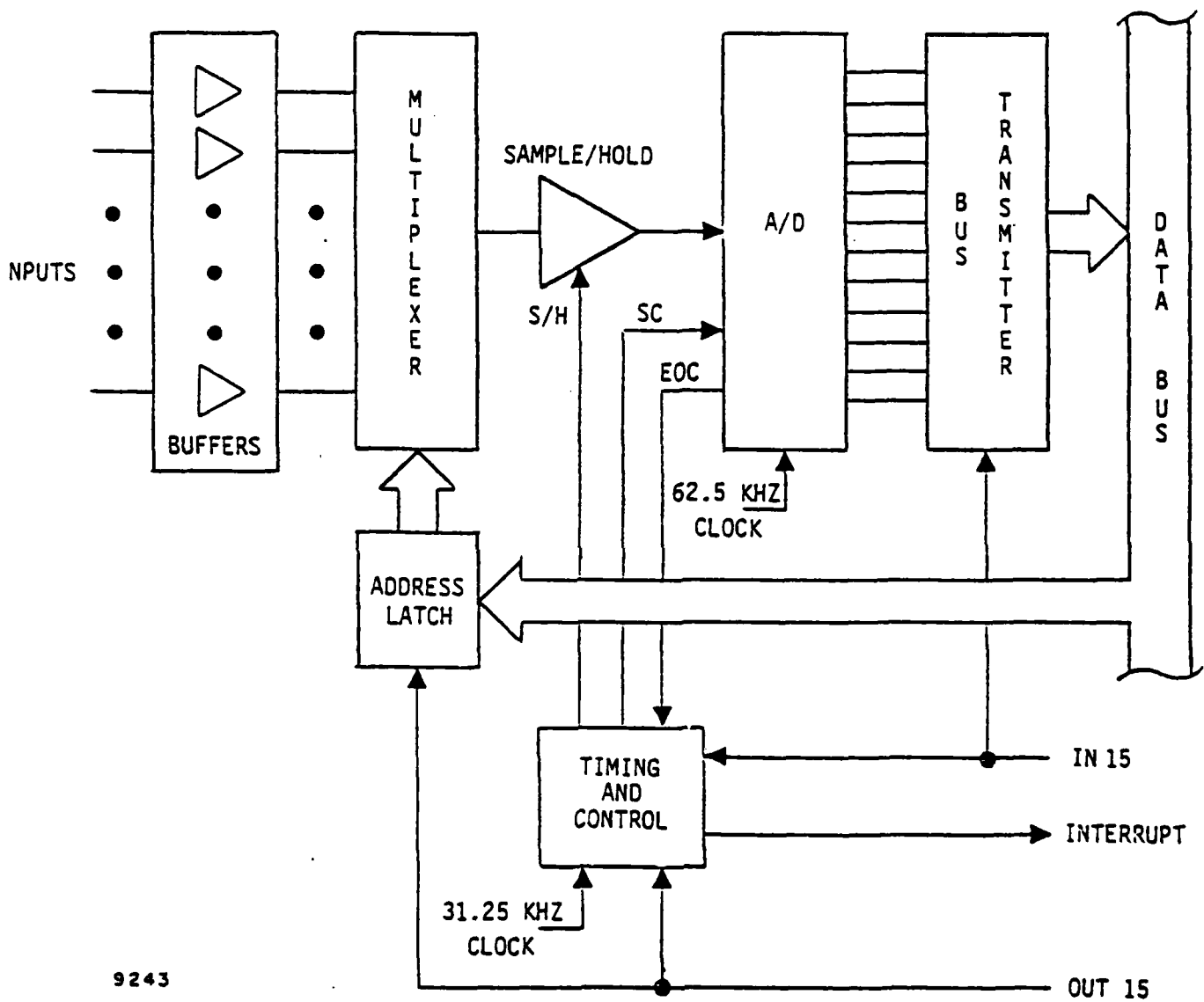
3.2.1 Buffer Amplifiers

Quad operational amplifiers, LM148D, are used to buffer and scale incoming signals to levels compatible with associated conversion hardware. Different amplifier configurations are provided for each of the following signal types.

- a. Continuous voltages with maximum amplitude equal to ± 10 Vdc
- b. Continuous voltages with maximum amplitude less than ± 10 Vdc
- c. Fixed reference voltages
- d. Two level discretes 28 Vdc and Open or Ground

TABLE 1. A/D SIGNAL INFORMATION

<u>Input Code</u>	<u>Analog Signal</u>	<u>Input Signal Range</u>
0	Target Height	0 to 10V
1	Stick Length (NTS)	0 to -10V
2	Rel Int (TS)	0 to 10V
3	1/Range	0 to 10V
4	True Air Speed (TAS)	0 to 10V
5	Baro Ht	0 to 10V
6	Baro Datum	0 to 10V
7	Multiplexer BIT	+5V
8	Pitch Rate	0 to $\pm 9.5V$
9	Yaw Rate	0 to $\pm 9.5V$
A	Roll Rate	0 to $\pm 9.5V$
B	Rate Channel Freq Ref	
C	Ind Air Speed (IAS)	0 to 10V
D	Mach No.	0 to 10V
E	Angle of Attack	0 to 10V
F	Multiplexer BIT	+5V
10	Cos Tacan	0 to $\pm 9.5V$
11	Sin Tacan	0 to $\pm 9.5V$
12	Cos Roll	0 to $\pm 9.5V$
13	Sin Roll	0 to $\pm 9.5V$
14	Cos Heading	0 to $\pm 9.5V$
15	Sin Heading	0 to $\pm 9.5V$
16	Rate Channel DC Ref	0 to 3 Vdc
17	Multiplexer BIT	+5V
18	Weight on Wheels	0 or +28V
19	Air to Air	0 or +28V
1A	IWAC Test	0 or +28V
1B	Store Heading	0 or +28V
1C	Weapons B	0 or 13.3V
1D	Cos Pitch	0 to $\pm 9.5V$
1E	Sin Pitch	0 to $\pm 9.5V$
1F	Multiplexer BIT	+5V
20	Power Supply BIT	-20V
21	Power Supply BIT	+20V
22	A/D Reference	-10V
23	Power Supply BIT	+5V
24	Power Supply BIT	-10V
25	Power Supply BIT	+10V
26	Power Supply BIT	-15V
27	Power Supply BIT	+15V
28	Spare	
29	Spare	
2A	Spare	
2B	Spare	
2C	Spare	
2D	Spare	
2E	Spare	
2F	Spare	



9243

FIGURE 1. A/D CONVERTER

- e. Two level discretes 10 Vdc and Ground
- f. Two level discretes 13.3 Vdc and Ground

3.2.1.1 Continuous Voltages with Maximum Amplitude Equal to ± 10 Vdc. Scaling is not necessary for signals with maximum amplitude equal to ± 10 Vdc; however, amplifiers are provided to buffer the impedance level of the incoming signals. The amplifiers are configured as voltages followers, see Figure 2. R1 is chosen to be equal to R2 to minimize the offset created by the flow of bias current into the amplifier inputs. Signals received in this manner as follows:

- | | |
|--------------------------|------------------------|
| a. Pitch Rate | l. Cos Heading |
| b. Yaw Rate | m. Sin Heading |
| c. Roll Rate | n. Rate Channel DC Ref |
| d. Rate Channel Freq Ref | o. Multiplexer BIT |
| e. IAS | p. Target Height |
| f. Mach No. | q. TS |
| g. Angle of Attack | r. I/R |
| h. Cos Tacan | s. TAS |
| i. Sin Tacan | t. Baro Datum |
| j. Cos Roll | u. Cos Pitch |
| k. Sin Roll | v. Sin Pitch |

3.2.1.2 Continuous Voltages with Maximum Amplitude Less than ± 10 Vdc. Signals with maximum amplitude of less than ± 10 Vdc are scaled up to ± 10 Vdc for full utilization of the 12-bit conversion resolution, see Figure 3.

The voltage gain is greater than one if R2 is not zero. R3 is chosen to match the parallel combination of R1 and R2 to minimize the offset created by the flow of bias current into the amplifier inputs. Baro height is scaled up to permit a finer resolution between 0 and 22,500,000 feet

3.3.1.3 Two Level Discretes Vdc and Ground. Five signals; Weight on Wheels, Air to Air, Store Heading, PGG, and Weapons B, are received by the circuit of Figure 4a and scaled as shown in Figures 4b and 4c, to the same levels as all other discretes.

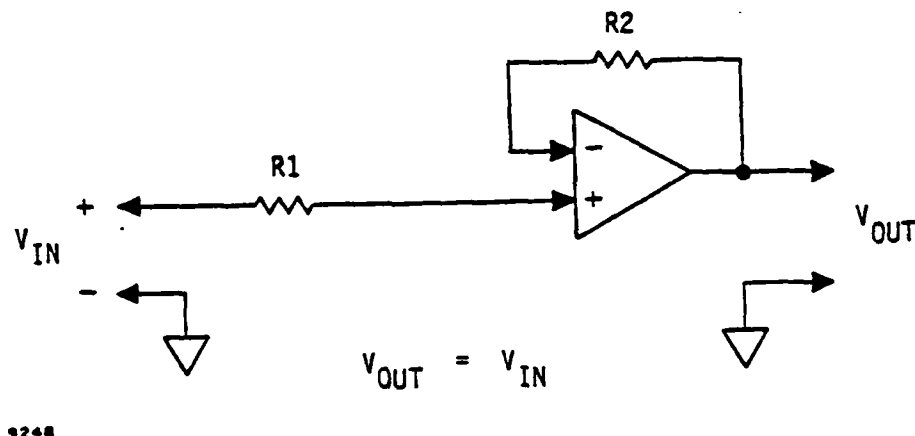
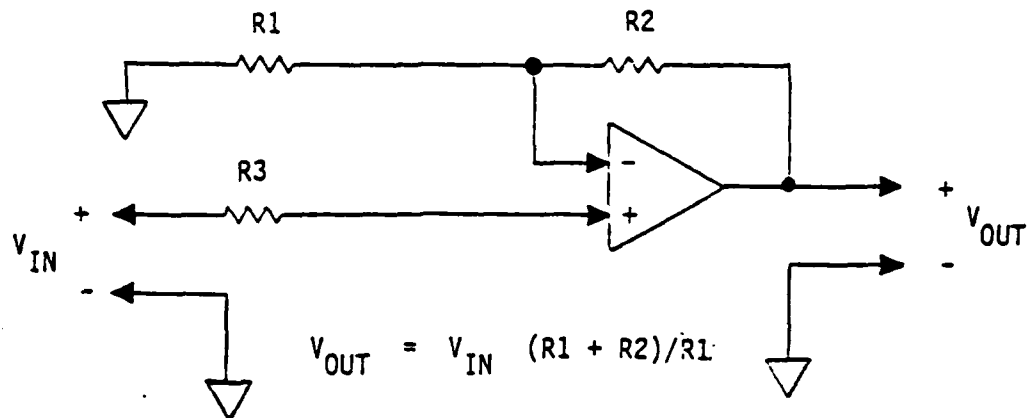


FIGURE 2. BUFFER AMPLIFIER (FOLLOWER)

- 3.2.1.4 Reference Voltage Scaling. Eight (8) reference voltages; ± 10 volts, ± 20 volts, ± 15 volts, $+5$ volts, and A/D ref, are scaled by a resistor divider network. See Figure 5.
- 3.2.1.5 Multiplexer. The multiplexer function of the A/D converter is provided by 8 to 1 analog multiplexer integrated circuits, HI-1818A (U15, U16, U26, U27, U30, and U31); see Appendix A for specification sheets. The integrated circuit outputs are connected together to implement a 48 to 1 channel multiplexer. Selection control is provided by the address latch and decoder discussed in paragraph 3.2.1.6.
- 3.2.1.6 Address Latch and Decode. A 6-bit latch, U11, is loaded by a strobe, OUT15, from the μC data bus system. The outputs of the latch are used to select each of the 48 multiplexer channels, see paragraph 3.2.1.5. The three least significant bits from the latch are directly tied to the eight multiplexer chips to select one of eight channels. The three most significant bits are decoded by U12 to provide circuit enables to each of the six multiplexers. Each enable line and select line has a 5.1K pull up resistor to $+5$ Vdc for compatibility of the logic gates and the analog chips.



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FIGURE 3. BUFFER AMPLIFIER (SCALE UP)

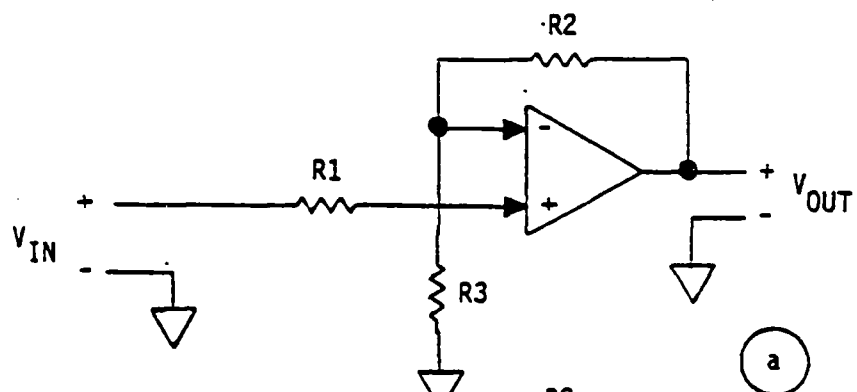
3.2.1.7 Sample and Hold. Steady input to the A/D converter during a conversion cycle is provided by the use of a sample and hold circuit, HA-2420 (U1); see Appendix B for specification sheets. When a logic zero is present at the control input, pin 14, the output, pin 7, tracks the input, pin 2. When the control line is at a logic one state, the output holds the voltage present at the time of the logic switch. Capacitor C5 stores the voltage during the hold time and must be a very low leakage component. A glass dielectric capacitor was chosen for this application.

Capacitor C3 provides a filter for high frequency rejection. The filter, formed by the capacitor and the on-state impedance of the multiplexer rejects noise that might be sensed as valid data.

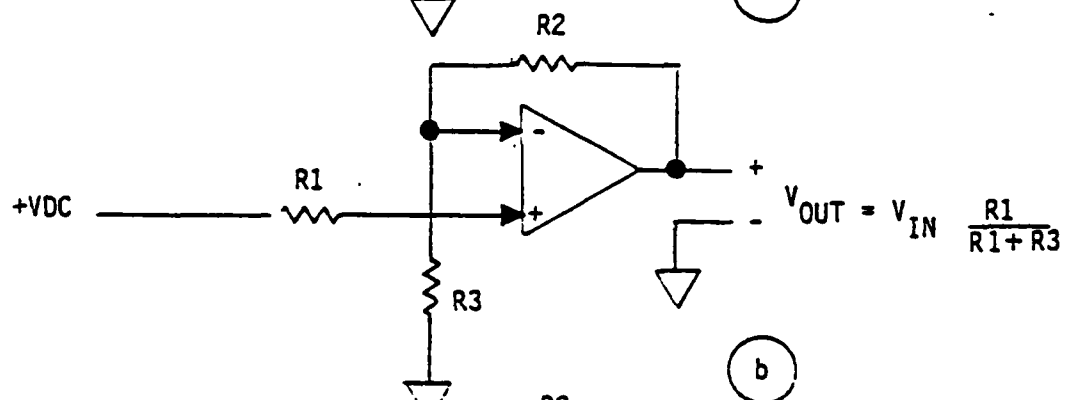
3.2.1.8 A/D Converter. A hybrid circuit, type MN5202H (U2), performs the analog-to-digital conversion. The circuit is a successive approximation converter generating an offset binary 12-bit output; see Appendix C for specification sheets. An analog input, a clock, and a start signal at pins 14, 24, and 1 respectively, are required to initiate and complete a conversion cycle. Completion of the cycle is signified by the End of Conversion (EOC) signal, pin 22. At the time EOC goes low, the twelve output bits are fixed in their final states and remain fixed until reset by the next start signal.

For maximum accuracy of conversion, an external voltage reference, type MN2002H, is used.

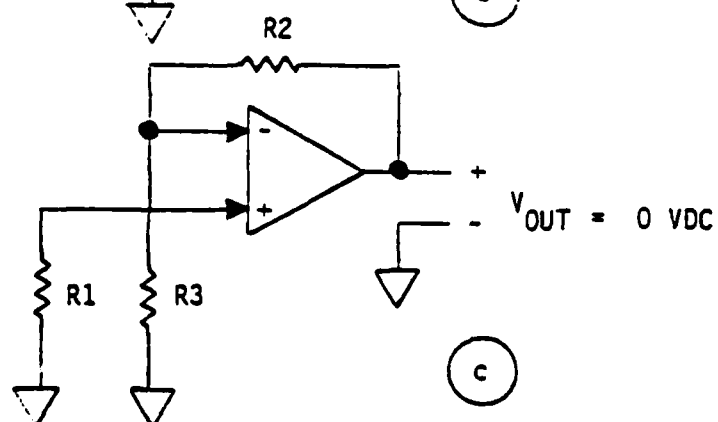
BASIC
CIRCUIT



VDC
INPUT

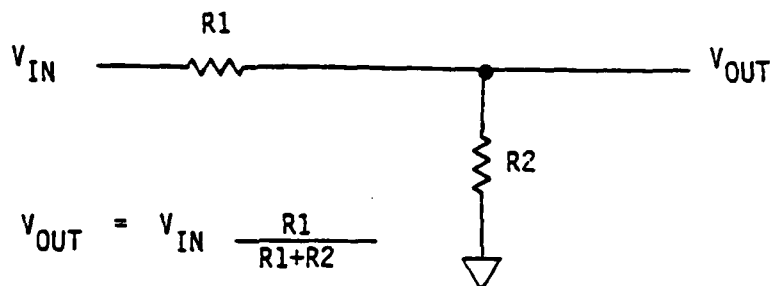


INPUT
GROUNDED



9249

FIGURE 4- DISCRETE RECEIVER (VDC-GROUND)



9246

FIGURE 5. REFERENCE VOLTAGE SCALING

- 3.2.1.9 Bus Transmitter. Quad tri-state drivers, U4, U5, and U6, are enabled whenever the μ C performs an Input to IN15 (ADLD), putting the A/D converter output bits onto the parallel data bus in the twelve most significant bit locations. The most significant bit from the A/D is inverted as a step toward converting the data from offset binary format to two's complement notation. Additional conversion steps are taken within the software.
- 3.2.1.10 Timing and Control. Control signal OUT15, see paragraph 3.2.1.6, initiates U9 and U10 to provide the control signals, Sample/Hold and Start Convert, as shown in Figure 6. Internal circuitry to the A/D converter performs the conversion and generates the EOC signal, see paragraph 3.2.1.8. EOC is inverted by U3 and used to clock U10-9 (ST07), to a logic one and U10-8, to a logic zero, causing a μ C interrupt. The μ C senses the source of the interrupt by polling the status line ST07, and performs an Input IN15. The input control strobe (IN15) resets the interrupt and status line to inactive states and enables the data bus drivers, see paragraph 3.2.1.9.
- 3.2.1.11 Analog Switches. Analog switches (U13, U18, U19, U22, and U23) are provided to select data from the sensors or a fixed known analog data when PCC is selected. The fixed analog data provides data for confidence testing. PCC is also an analog input for informing the computer that PCC is selected.

4.0 INPUTS/OUTPUTS

The A/D converter board has two signal connectors, P1A and P1B, and one test connector J1. Pin and signal information is given in Tables 2 through 4.

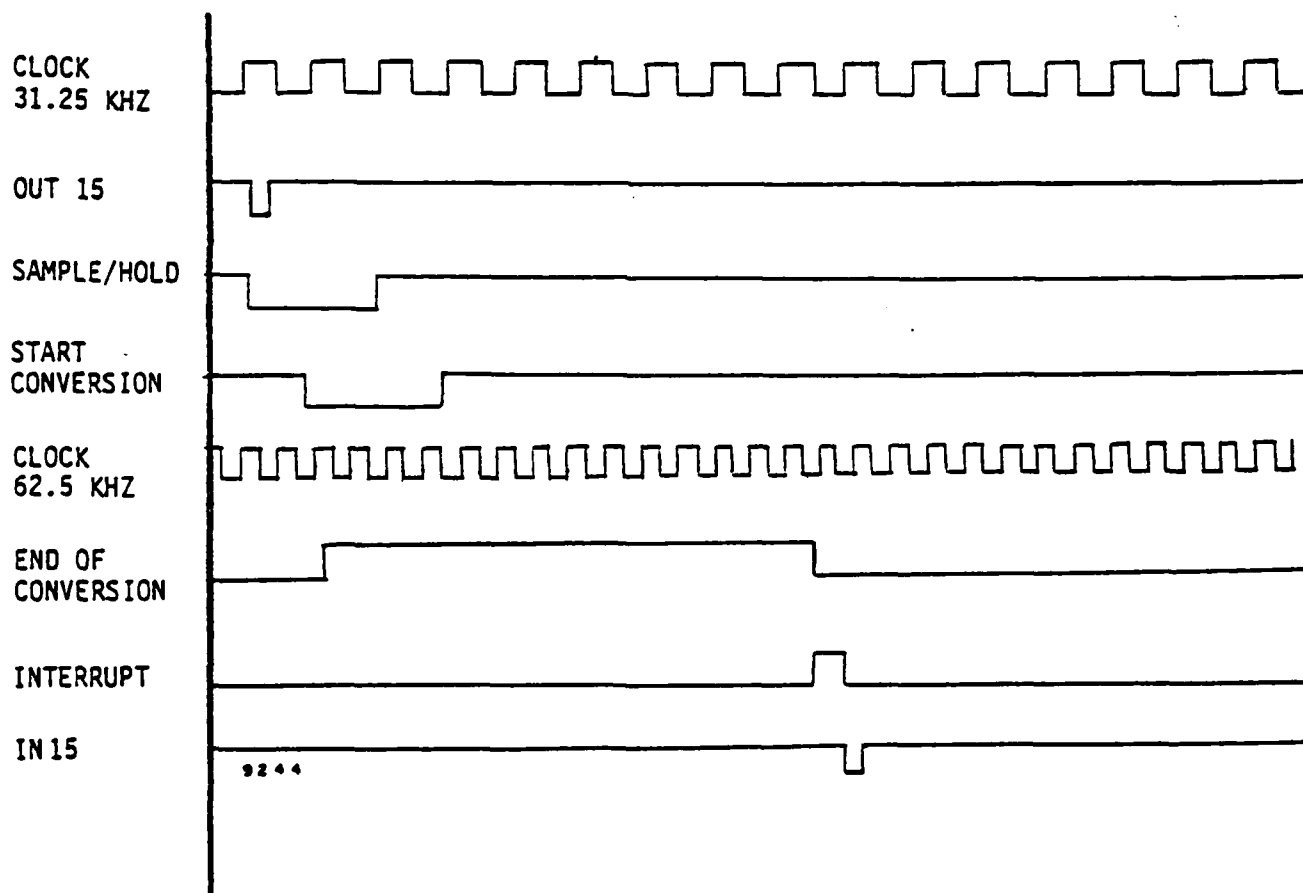


FIGURE 6. A/D CONVERTER CONTROL TIMING

TABLE 2. P1A PIN CONNECTIONS (A/D CONVERTER)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	Digital Ground	28	DB03 Data Bit 03
2	Digital Ground	29	
3	DB04 Data Bit 04	30	Target Height 0-10V
4	DB05 Data Bit 05	31	NTS 0-10V
5	DB06 Data Bit 06	32	TS 0-10V
6	DB07 Data Bit 07	33	I/R 0-10V
7	DB11 Data Bit 11	34	TAS 0-10V
8	DB10 Data Bit 10	35	Baro Height 0-10V
9	DB09 Data Bit 09	36	Baro Datum 0-10V
10	DB08 Data Bit 08	37	Pitch Rate
11		38	Yaw Rate
12		39	Roll Rate
13		40	Rate Chan. Freq. Ref.
14	A/D Ref	41	IAS 0-10V
15	DB15 Data Bit 15	42	Mach No. (0-10V)
16	ST07 Status 07	43	Angle of Attack (0-10V)
17	INT 1 Interrupt 1	44	
18	DB14 Data Bit 14	45	
19	CLK 2 62.5 KHz	46	
20	DB13 Data Bit 13	47	
21	CLK 1 31.25 KHz	48	
22	DB12 Data Bit 12	49	
23		50	
24		51	
25	DB00 Data Bit 00	52	+5V
26	DB01 Data Bit 01	53	+5V
27	DB02 Data Bit 02	54	

TABLE 3. P1B PIN CONNECTIONS (A/D CONVERTER)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	+5V	28	+15V
2	+5V	29	+15V
3		30	
4	Spare Analog Mux Input	31	-15V
5	Spare Analog Mux Input	32	-15V
6	Spare Analog Mux Input	33	
7	Spare Analog Mux Input	34	+10V
8	Spare Analog Mux Input	35	
9	Spare Analog Mux Input	36	-10V
10	Spare Analog Mux Input	37	
11	OUT15	38	+20V
12	IN15	39	
13	Weight on Wheel (+28V)	40	-20V
14	Air to Air (+28V)	41	
15	T Pilot's Cnfdnce Check Logic	42	
16	Store HDG (+28V)	43	
17	Weapons B (0V-ON 13.3 V-OFF)	44	Cos Tacan $\pm 9.5V$
18	Cos Pitch $\pm 9.5V$	45	Sin Tacan $\pm 9.5V$
19	Sin Pitch $\pm 9.5V$	46	Cos Roll $\pm 9.5V$
20		47	Sin Roll $\pm 9.5V$
21		48	Heading Cos HD $\pm 9.5V$
22	Pcc Pilot's Cnfdnce Check	49	Heading Sin HD $\pm 9.5V$
23		50	Rate Chan. DC Ref. 0-3V
24		51	
25		52	
26		53	Analog Ground
27		54	Analog Ground

TABLE 4. J1 PIN CONNECTIONS (A/D CONVERTER)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	TMUX1	MUX 1 Strobe	28
2	TMUX2	MUX 2 Strobe	29
3	TMUX3	MUX 3 Strobe	30
4	TMUX4	MUX 4 Strobe	31
5	TMUX5	MUX 5 Strobe	32
6	TMUX6	MUX 6 Strobe	33
7	TMUX7	MUX 7 Strobe	34
8	TMUX8	MUX 8 Strobe	35
9	TMUXC0	MUX Channel Address Bit 1	36
10	TMUXC1	MUX Channel Address Bit 2	37
11	TMUXC2	MUX Channel Address Bit 3	38
12	TDONE	Conversion Done	39
13	TCLK2	31.25 KHz	40
14	TSAMPLE	Sample	41
15	TCOVSTART	Conversion Start	42
16	TCLK2	62.5 KHz	43
17	TANALOGIN	MUX out analog	44
18	TANALOGOUT	A/D analog in	45
19			46
20			47
21			48
22			49
23			50
24			51
25			52
26			53
27			54

APPENDIX A



MN5200 SERIES

12 BIT
A/D CONVERTERS

DESCRIPTION

The MN5200 Series devices are 12 Bit Successive Approximation A/D Converters providing both parallel and serial outputs.

These hybrid converters are housed in miniature 24 pin glass/ceramic dual-in-line packages. Miniature size, low power consumption and adjustment free operation contribute to the reasons why these converters provide the user with the best possible selection for compact and efficient systems.

All converters are completely laser trimmed and totally adjustment free. Thus, one can operate without potentiometers with their cumbersome adjustments. Additionally, due to the highly stable thin film resistor networks, these converters provide long term maintenance free operation.

These converters are available in three input voltage ranges: 0 to -10 volts (MN5200/03), ± 5 volts (MN5201/04), and ± 10 volts (MN5202/05). For each of these input ranges, the user has the option of specifying a model complete with an internal reference or for improved absolute accuracy, a model which uses an external reference.

In all cases $\pm 1/2$ LSB linearity is guaranteed over the entire operating temperature range. Additionally all units are tested 100% for linearity and accuracy at their temperature extremes as well as at room temperature.

All models of the MN5200 Series may be procured for operation over the entire -55°C to +125°C military temperature range ("H" models) with the same end temperature operating characteristics as the commercial 0°C to 70°C range. In addition, full military temperature operation devices are available processed to the Class B requirements of MIL-STD-883 (inquire about Micro Networks' "Option B").

FEATURES

- Small
24 Pin DIP
- Totally adjustment-free
No full scale or zero adjustment necessary
- Low Power
700mW
- Fast
4 μ Sec/Bit
- $\pm 1/2$ LSB linearity worst case
- Hermetically sealed package
- Parallel and serial outputs
- Full Mil operation
-55°C to +125°C ("H" models)
Available fully screened & processed to the Class B requirements of MIL-STD-883

APPLICATIONS

- Remote Equipment
- Medical Instrumentation
- Aerospace
- Computer I/O Equipment



Micro Networks Corporation

324 Clark Street, Worcester, Massachusetts 01606 Telephone 617 852-5400 TWX 710-340-0067

MN5200 SERIES SUCCESSIVE APPROXIMATION 12 Bit A/D Converters

ABSOLUTE MAXIMUM RATINGS:

Operating Temperature	0 to 70°C (-55°C to +125°C "H" Models)
Storage Temperature	-65°C to +150°C
Positive Supply	+18 Volts
Negative Supply	-18 Volts
Logic Supply	+7 Volts
Analog Input	±25 Volts
Digital Outputs	Logic Supply
Digital Inputs	+5.5 Volts
Reference Supply (Models MN5203, 04, 05 only)	-15 Volts

SPECIFICATIONS (T_A=25°C, Voltages ±15, +5 unless otherwise stated)

PERFORMANCE:

INPUT RANGE	INPUT IMPEDANCE	HIGH PERFORMANCE (Int. Ref.)		HIGH ACCURACY (Ext. Ref= -10.000V)		
0 to -10V	6.7k	MN5200		MN5203		
+5V to -5V	6.7k	MN5201		MN5204		
+10V to -10V	13k	MN5202		MN5205		
		TYP.	MAX.	TYP.	MAX.	UNITS
Resolution		12	12			Bits
Linearity (0° to 70°C) (Note 1)		±½	±½			LSB
Zero Error		1	1			LSB
Zero Error (0° to 70°C) (Note 1)		2	2			LSB
Absolute Accuracy 25°C (Note 2)		2	2			LSB
Absolute Accuracy (0° to 70°C) (Notes 1 & 2)		±.4	±.1			%FSR
Conversion Time		50	50			µSec
Power Supply Requirements						
Current Drain +15 Volt Supply		23	28	23	28	mA
Current Drain -15 Volt Supply		15	19	5	6.3	mA
Current Drain + 5 Volt Supply		25	42	25	42	mA
Current Drain -10 Volt Reference				1.5	2.0	mA
Power Supply Rejection						
+15 Volts (Note 3)		±.02		±.02		%FSR/%Supply
-15 Volts (Note 3)		±.05		±.02		%FSR/%Supply
Power Consumption		695	915	567	744	mW

LOGIC RATINGS

	MIN.	TYP.	MAX.	UNITS
Input Logic Commands				
Logic "0"			.8	Volts
Logic "1"	+2.0			Volts
Loading		.5		TTL Load
Clock Input Pulse Width	100			nSec
Output Logic				
Logic "0"			.4	Volts
Logic "1"	+2.4	3.6		Volts
Serial Output				NRZ
Parallel Output (See Timing Diagram)				
Fanout-High	8			TTL Load
Fanout-Low	2			TTL Load

LOGIC CODING

MN5200/5203	MN5201/5204	MN5202/5205	MSB	LSB
OV	+5.0000	+10.000	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0
-5.000V	0	0	1 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0
-9.9976V	-4.9976	-9.995	1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1

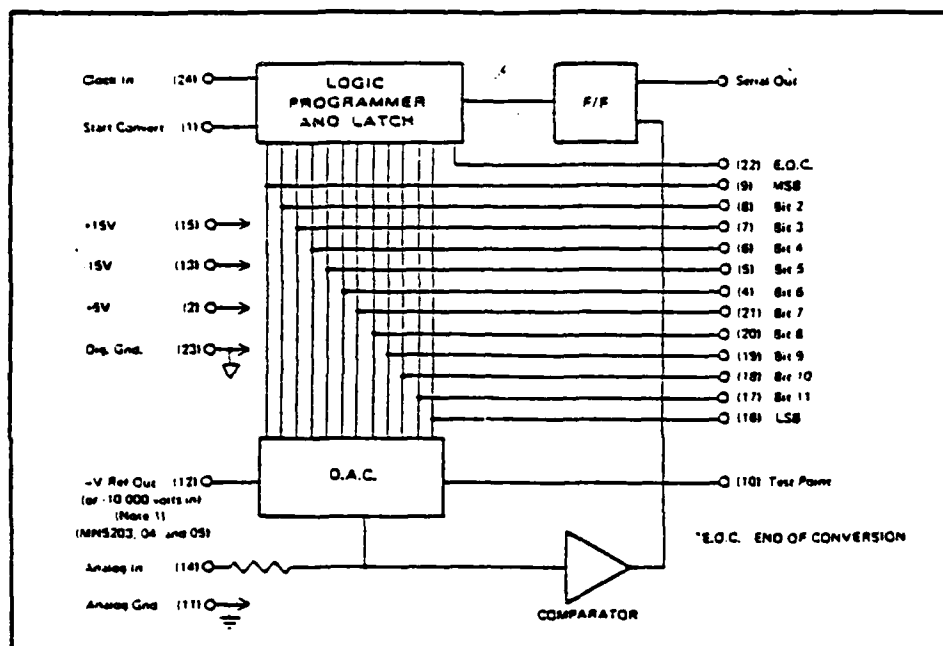
NOTE 1. For "H" models, the specification applies for operation over the temperature range of -55°C to +125°C.

NOTE 2. Absolute accuracy includes all errors, gain, zero, and linearity. All converters are tested 100% at the temperature extremes for linearity and absolute accuracy.

NOTE 3. For proper operation ±15 Volt power supplies tolerance should not be greater than ±3%.

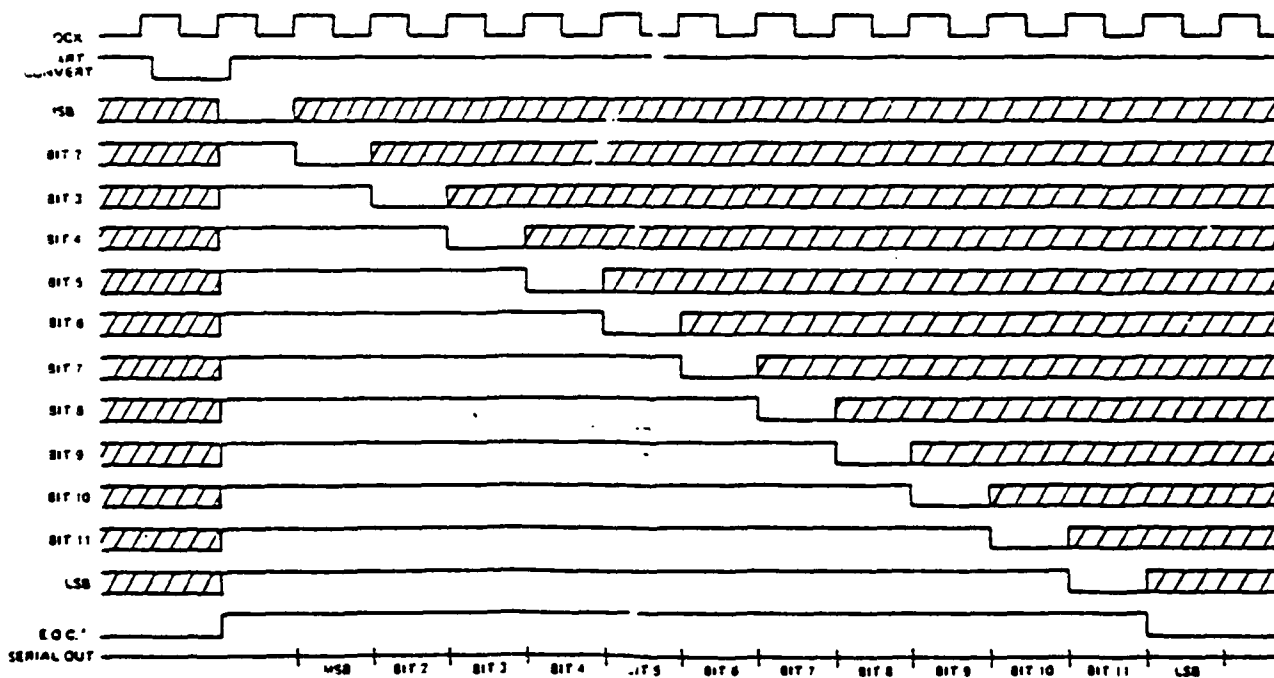
NOTE 4. FSR is the abbreviation for "Full Scale Range" and is equal to the peak to peak output voltage, i.e. 10 volts for ±5V range.

BLOCK DIAGRAM



NOTE 1. The maximum current which should be drawn from the -V Ref output (Available only on internal reference models) is 100 μ A.

TIMING DIAGRAM

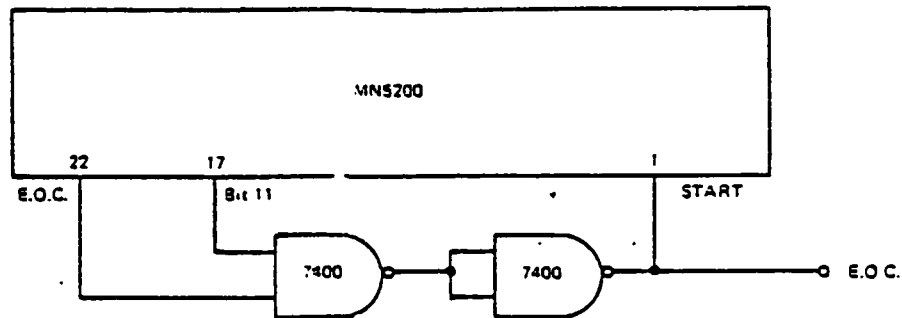


NOTES:

1. Shaded areas shown for parallel data outputs denotes states determined by data input immediate prior to shaded area.
2. For continuous operation connect start convert (Pin 1) to end of conversion (Pin 22).
3. Reset the converter by holding the start 'low' during a low to high transition of the clock. The start must be low for a minimum of 25 nSec prior to the clock transition. After the start is again set high the conversion will begin on the next low to high transition of the clock. The start may be set low at any time during a conversion to reset and begin again.
4. At the end of conversion the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
5. The serial output is non-return to zero.
6. For the user's design flexibility, digital and analog grounds are brought out separately and must be externally connected. For optimum results, this external connection should be made as close to the converter as is possible.

APPLICATION

10 BIT TRUNCATION FOR MNS200 IN RECYCLE MODE



(For more information on Truncation see our Micronetworks' Note AN-102.)

PIN DESIGNATIONS

Pin 1	Start	Pin 13	-15V
Pin 2	+5V	Pin 14	Analog in
Pin 3	Serial Out	Pin 15	+15V
Pin 4	Bit 6	Pin 16	LSB
Pin 5	Bit 5	Pin 17	Bit 11
Pin 6	Bit 4	Pin 18	Bit 10
Pin 7	Bit 3	Pin 19	Bit 9
Pin 8	Bit 2	Pin 20	Bit 8
Pin 9	MSB	Pin 21	Bit 7
Pin 10	Test Point (make no connections)	Pin 22	E.O.C. (end of conversion)
Pin 11	Analog Ground	Pin 23	DIG Grd
Pin 12	-V ref out (int. ref. models) -V ref in (ext. ref. models)	Pin 24	Clock Input

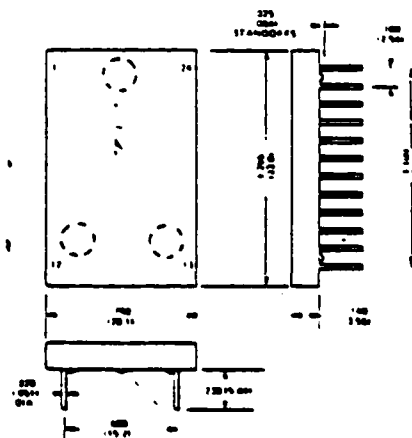
ORDERING INFORMATION

MODEL NUMBER MNS20X H/B
 Model selection _____
 Add "H" for -55 to +125°C operation _____
 Add "/B" for 100% screened (883 Class B) _____

Example

0 to 70°C ($\pm 5V$, Int. Ref.) MNS201
 -55 to +125°C Operation MNS201H
 -55 to +125°C and 100%
 screened *883 MNS201H/B

*Micro Networks Option "B"



Outline dimensions in inches (and millimeters).

MICROCONTROLLER TECHNICAL DESCRIPTION

APPENDIX C

1.0

System Organization

Figure 1 illustrates a typical processing system incorporating the Microcontroller. Operations that can be performed include:

- . direct control of I/O devices
- . transfer of data or control information between I/O and memory (M)
- . and interpretation or modification of words stored in memory

System input peripheral devices may include switches, discretes, A/D converters, memories, other computers, or any circuit having tri-state Data Bus compatibility. Output devices may include lights, graphic generators, discrete drivers, D/A converters, or any circuit capable of latching Data Bus information.

Memory can comprise any combination of Read Only Memory (ROM) and Random Access Memory (RAM) up to a maximum of 65,536 words.

ROM is used for permanent storage of programs, tables, fixed data, and fixed algorithms. RAM is required for temporary data storage and scratch pad operations. The type of memory and storage capacity is determined by the specific system application.

Information is transferred between I/O devices, memory and Microcontroller by means of a common, bidirectional 16-bit Data Bus.

Sixteen input and sixteen output (I/O) control signal lines are provided. Systems can use some or all of these signals depending on required I/O sophistication. Control signals can be used directly without additional gating of clocks, etc.

Fourteen I/O status (flag) inputs are provided. I/O devices can control these inputs at any time to signal the Microcontroller of busy/ready status, or other conditions that have occurred. The status inputs are tested with instructions and must be coordinated with programs that require them.

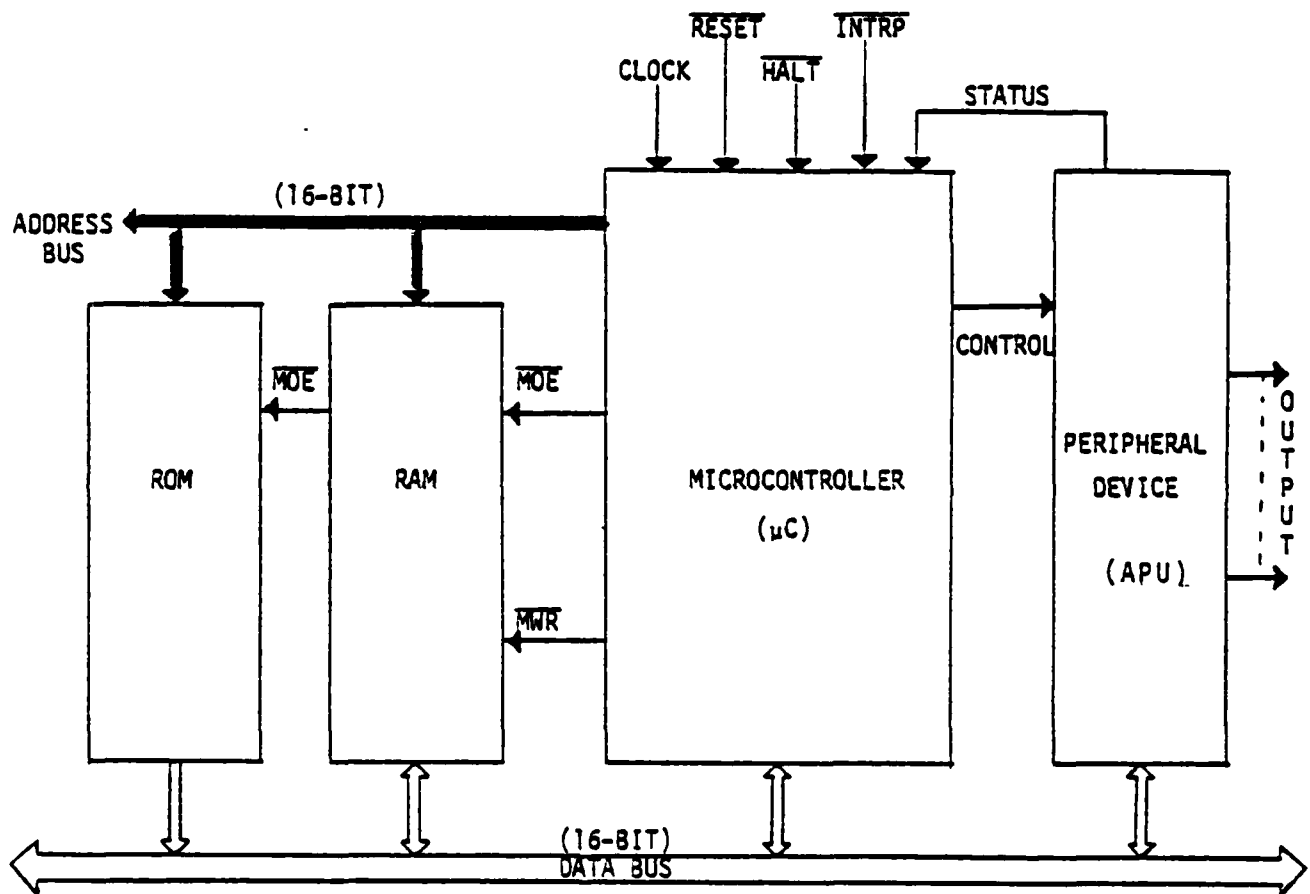


Figure 1 - Block Diagram of Typical Microcontroller System

A program interrupt line can be activated at any time by I/O circuits to obtain an immediate Microcontroller response. The interrupt causes the Microcontroller to suspend the current program and to execute a predetermined sequence of operations that are located at address zero. During the response, the Microcontroller ignores the interrupt line until a return from interrupt is executed. After servicing, execution of the interrupted program resumes.

Words are transmitted to and from memory by means of the common Data Bus. During a memory write cycle, the word to be written appears on the Data Bus and a memory write pulse ($\overline{MWR}$) is generated by the Microcontroller. During a memory read cycle, a memory read pulse ($\overline{MOE}$) is generated to gate the memory onto the common Data Bus.

The Microcontroller provides 16 memory address lines (Address Bus) with a capability of 65,536 words. A typical CRT display application usually requires not more than 4K words total of RAM and ROM.

Three additional lines complete the Microcontroller system interface. A single-phase clock input (0 to 9 MHz military, 0 to 10 MHz commercial) determines operating speed. A HALT control line and a ~~RESET~~ input are utilized by the associated Microcontroller Programming Adaptor for stop/step/run control and P-register zeroing.

2.0 Microcontroller Architecture

Microcontroller architecture, Figure 2, offers a unique design that applies 4-bit slice LSI technology to a specific 16-bit processing function. The design incorporates 4-bit processor slices, 4-bit address controllers, internal nanocontrol, and direct I/O decode that provide process/control capabilities comparable to much larger machines. Efficient internal operation enables the execution of more than 1.8×10^6 instructions per second.

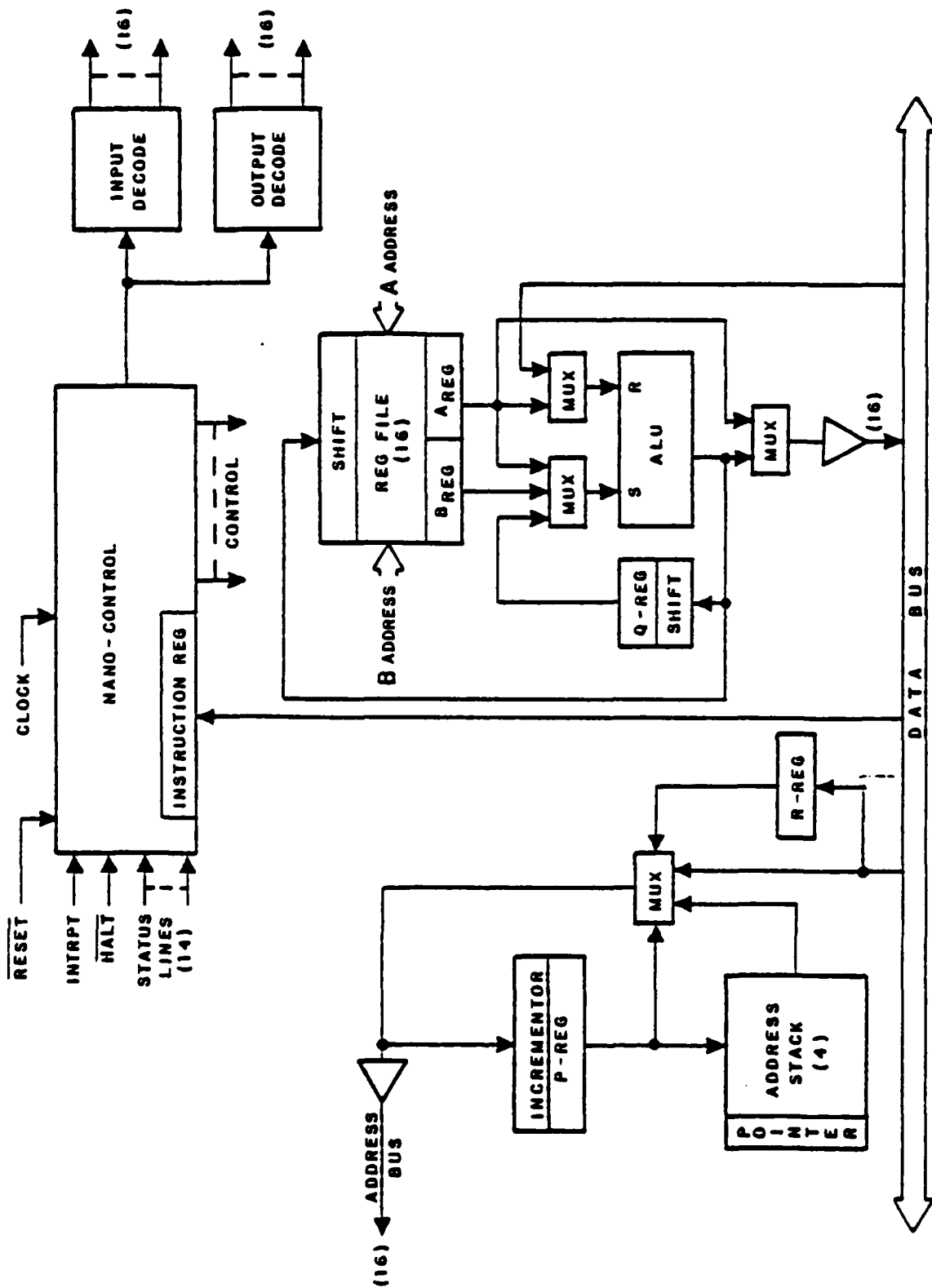


Figure 2 - Microcontroller Architecture

2.1 4-Bit Processor Slice

The 4-bit processor slice (AM2901) is a high speed cascadable element intended for use in processor/controller applications. It consists of a 16 word by 4-bit two port RAM, a high-speed ALU, and associated shifting, decoding, and multiplexing circuitry. The device provides three state Data Bus outputs and various condition flags from the ALU. See the data sheet for vendor detailed specifications.

2.2 4-Bit Address Controller Slice

The 4-bit address controller slice is a high-speed cascadable element intended for use in processor/controller applications. It contains a multiplexer that selects an address from either the direct input, the internal register, the four word deep push/pop stack, or the program counter. See the data sheet for vendor detailed specification.

2.3 Nanocontroller Circuits

The nanocontroller circuits, consisting of LSI Read Only Memory (ROM) elements and sequencing logic, provide high speed control sequencing from linear progression through a nonoinstruction map. See the schematic diagram, which includes the following functions.

<u>Function</u>	<u>Component Designator</u>
Instruction Register	U1, U2, U4
Sequencing Logic	U7, 3, 14, 15, 16, 17
Function Decode	U11, 12
Condition/Status Selectors	19, 20, 21, 8, 18, 13
Interrupt Logic	U6, U7
Clock Buffer	U5
Overflow Latch	U13

The Instruction Register (I-REG) consists of a 16-bit latch that is implemented with 3 HEX D-Flip/Flops and controlled by the instruction register clock (IRCK) and a clear line from the interrupt circuits. During execution the register retains the instruction code to provide Data Bus usage and memory overlap. In addition, the interrupt instruction (OPCODE 0) is readily injected into the program stream by the direct clear line.

Sequencing logic provides generated pulses and enables strobes for Microcontroller dynamic operation. Components include the sequencing counter (U3), ROM nanoprogram array (U9, U10), and synchronization/overlap latches (U14, 15, 16, 17).

The ROM nanoprograms are fixed in memory at absolute pages, allowing direct addressing by the instruction opcode. Addressing is accomplished with opcode (4-bit), condition/status (1-bit), and sequencer (4-bit).

Sequencer and synchronization latches are cleared at the end/start of every instruction and held for one clock cycle to provide sufficient memory ripple time. Overlap is accomplished by simultaneously latching a ROM program word and incrementing the sequencer. Hardware constraints demand that the last-plus-one nanoprogram word be identical to the initial state of the synchronization latches.

During the execution of a status/conditional transfer, the instruction page is selected as a function of the TRUE/FALSE signal (U13, pin 9), providing either the continuation or transfer sequence.

Operation decode, provided by ROMs U11 and U12, supplies direct control of 4-bit processor slices and condition/status circuits. The ROMs contain control maps that are addressed by opcode (4-bit), function code (4-bit), and functional mode change (1-bit).

During the execution sequence, the indirect addressing instructions require a functional mode change (MDCG) to provide transfer of Q-REG contents to the R-REG.

Condition selector (U21) and status selectors (U19, 20) provide the decode capability required for all conditional transfers/branching. The condition selector, addressed by the condition code, monitors the high/low state of ALU flags, as decoded by U8, to provide comparison data on internal arithmetic/logic registers. Status selectors, addressed by the status code, monitor the high/low condition flags that provide synchronization of I/O devices to microcontroller programs.

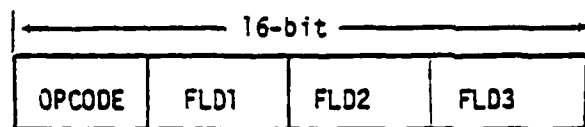
Interrupt logic provides the hardware injection of opcode 0 into the program stream. The INTRPT signal is delayed up to one instruction time to inhibit P-REG incrementation for a correct return. Execution of an interrupt instruction will mask all other interrupts, via strobe ($\overline{\text{IMSK}}$). Unmasking is accomplished with signal ($\overline{\text{RITP}}$) when a return from interrupt instruction is executed.

Direct input and output device (I/O) control is provided by demultiplexers U30, 31 and 32 and 33, respectively. The instruction, FLD3, directs the appropriate sequencing strobe ($\overline{\text{ISTB}}$ or $\overline{\text{OSTB}}$) to the selected device.

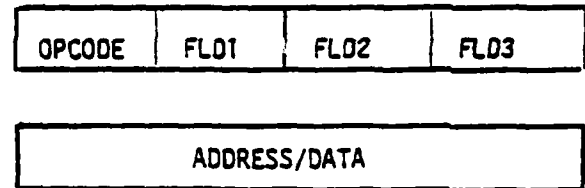
2.4 Instruction Format

Microcontroller operations are specified by instruction codes stored in external memory. A 16-bit format is applicable for most instructions, except for direct memory references and control transfers. The following diagram illustrates the Quad. 4-bit single/two-word instruction format.

Single Word Instruction:



Two Word Instruction:



OPCODE - Selects basic operational sequence.

FLD 1 - A-REG. address.

FLD 2 - B-REG. address.

FLD3 - Function code.

2.5 Instruction Timing

Instruction execution requires from 4 to 9 nanocontrol cycles.

Each time interval is equivalent to one clock cycle that produces instruction times extending from .444 to 0.999 usec. (military) or from .4 to .9 usec. (commercial). A reasonable combination of instructions provide Microcontroller execution of approximately 1.8×10^6 operations per second.

3.0 Instruction Repertoire

The Microcontroller provides the following instruction repertoire:

- . Register Operations
- . Memory Reference
- . Logic Operations
- . Arithmetic Operations
- . Branching
- . Conditional Branching
- . Interrupt and Subroutine Handling
- . Input/Output Transfer

The Instruction Definition, Table 1, illustrates 16-bit instructions split into one 4-bit opcode and three 4-bit operand fields (FLD). The opcodes provide 16 basic operation sequences, while FLD1/FLD2 address the affected Arithmetic/Logic (A/L) registers and FLD3 defines the proper A/L, I/O device, condition, status, or branching code. Five instructions require an additional 16-bit word that immediately follows the instruction.

The following paragraphs detail the sequence of events for each opcode execution.

3.1 Hardware/Software Interrupt (OPCODE: 0)

The Interrupt instruction is either programmed or hardware injected into the execution sequence. Present P-register position, P, for hardware interrupt and present P-register position plus one, P+1, for software interrupt, is 'PUSH'ed onto the address stack and control transferred to address 0, P = 0.

Table I
MICRO-CONTROLLER
INSTRUCTION SET SUMMARY

INSTRUCTION	16 BIT			
	OP CODE	FLD 1	FLD 2	FLD 3
Interrupt	0	-	-	-
Input	1	-	R _B	Device Code
Output	2	R _A	-	Device Code
Rotate/Shift	3	R _A	R _B	R/S Code
Arithmetic/Logic to R _B R _A /R _B → R _B	4	R _A	R _B	A/L Code
Arithmetic/Logic to R _B R _Q /R _A → R _B	5	R _A	R _B	A/L Code
Arithmetic/Logic to R _Q R _A /R _B → R _Q	6	R _A	R _B	A/L Code
Arithmetic/Logic to R _Q R _Q /R _A → R _Q	7	R _A	-	A/L Code
Fetch Direct to R _B (2 words) M _{p+1} → R _B	8	R _A	R _B	A/L Code
Store R _A /R _B Direct (2 word) R _A /R _B → (M _{p+1})	9	R _A	R _B	A/L Code
Fetch Indirect to R _B M _{RQ} /R _A → R _B	A	R _A	R _B	A/L Code
Store R _A /R _B Indirect R _A /R _B → M _{RQ}	B	R _A	R _B	A/L Code
Control Return	C	-	-	- J ₀
Conditional Transfer (2 word)	D	R _A	R _B	Condition Code
Status Transfer (2 word)	E	-	-	Status Code
Control Transfer (2 word)	F	-	-	- J ₀

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location. (Incrementing of P-REG inhibited if hardware injected)
- . P-REG 'PUSH'ed onto address stack
- . P-REG and Address Bus forced to zero via control line.
- . Wait for memory cycle.

3.2 Input (OPCODE: 1)

The Input instruction provides data transfer from a coded, peripheral device, which is connected to the Data Bus, to one of the 16 A/L registers. A decoded hardware strobe is provided for direct use as tri-state enable timing.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Tri-state gated device information is transferred to designated register R_B via Data Bus.

3.3 Output (OPCODE: 2)

The Output instruction provides data transfer from an A/L register to a coded peripheral device that is connected to the Data Bus. A decoded hardware strobe is provided for direct load enable timing.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Contents of designated register R_A are transferred to coded device via Data Bus.

3.4 Rotate/Shift (OPCODE: 3)

The Rotate/Shift instruction is implemented to provide maximum capability without additional hardware. Appendix C defines the A/L register configuration, rotate/shift capabilities, and fill characteristics.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Contents of designated registers R_A (and R_Q) are shifted and transferred to register R_B (and R_Q).

3.5 Arithmetic/Logic Register Operations (OPCODES: 4, 5, 6, 7)

The Arithmetic/Logic instructions perform the register to register operations as defined in Appendix C, with source/destination provided by opcodes 4, 5, 6, and 7.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Contents of designated register R_A , R_B , and/or R_Q are selected and the A/L result is transferred to register R_B or R_Q .

3.6 Direct Memory Fetch (OPCODE: 8)

The Direct Memory Fetch instruction transfers the next program word into one of the 16 A/L registers.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Next program word is transferred to designated register R_B and P-REG is incremented to next instruction.
- . Wait for memory cycle.

3.7 Store Direct to Memory (OPCODE: 9)

The Store Direct instruction transfers the contents of an A/L register to the memory location that is addressed by the next program word.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Next program word transferred to R-REG and P-REG is incremented to next instruction.
- . Contents of R-REG is multiplexed to Address Bus while contents of designated register R_A is transferred to memory.
- . P-REG is selected to Address Bus and wait for memory cycle.

3.8 Indirect Memory Fetch (OPCODE: A)

The Indirect Memory Fetch instruction transfers the contents of the memory location which is addressed by register R_Q , to one of the 16 A/L registers.

Execution Sequence:

- . Instruction is strobed into the I-REG and P-REG is incremented to next location.
- . Contents of register R_Q is transferred to R-REG.
- . R-REG multiplexed to Address Bus while contents of memory are transferred to designated register R_B .
- . P-REG is selected to Address Bus and wait for memory cycle.

3.9 Store Indirect to Memory (OPCODE: B)

The Store Indirect instruction transfers the contents of an A/L register to the memory location addressed by register R_Q .

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Contents of register R_Q is transferred to R-REG.

- . R-REG is multiplexed to Address Bus while contents of designated register R_A are transferred to memory.
- . P-REG is selected to Address Bus and wait for memory cycle.

3.10 Control Return (OPCODE: C)

The Control Return instruction "POP"s an address off the stack and transfers it to the P-REG to provide a subroutine return with interrupt control. If a return and enable interrupt is specified, ($Jo = 1$), hardware is unmasked to permit interrupt reoccurrence. If a return and disable interrupt is specified, ($Jo = 0$), hardware is masked to not permit interrupt reoccurrence.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Address stack is selected to Address Bus and transferred to P-REG.
- . Interrupt disable/enable performed.
- . "POP" occurs by decrementing stack pointer after memory cycle.

3.11 Conditional Transfer/Branch (OPCODE: D)

If the coded condition is "TRUE", the Conditional Branch instruction transfers the next program word to the P-REG. If "FALSE", P-REG is incremented to the next instruction.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Next program word is transferred to R-REG and P-REG is incremented to next instruction.
- . If condition "TRUE", R-REG is selected to Address Bus.
- . If "FALSE", P-REG is selected.
- . Wait for memory cycle.

3.12 Status and Unconditional Transfer/Branch (OPCODE: E)

If the coded status line is logic "HIGH", the Status Branch instruction transfers the next program word to the P-REG. If "LOW", P-REG is incremented to the next instruction.

Status code 0 is tied "HIGH" to provide an unconditional branch instruction.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Next program word is transferred to R-REG and P-REG is incremented to next instruction.
- . If status "HIGH", R-REG is selected to Address Bus, If "LOW", P-REG is selected.
- . Wait for memory cycle.

3.13 Subroutine Transfer/Branch (OPCODE: F)

The Subroutine Branch instruction transfers the next program word to the P-REG and "PUSH"es the next instruction location onto the address stack. The instruction will also, as a function of Jo, disable (Jo = 0) or enable (Jo = 1) hardware interrupt.

Execution Sequence:

- . Instruction is strobed into I-REG and P-REG is incremented to next location.
- . Next program word is transferred to R-REG and P-REG is incremented to next instruction.
- . R-REG is selected to Address Bus and P-REG is "PUSH"ed onto stack.
- . Interrupt disable/enable performed.
- . Wait for memory cycle

4.0 The power requirements of the Microcontroller are as shown in Table 2

TABLE 2(a). GENERAL DEVICE POWER CHARACTERISTICS

<u>DEVICE NAME</u>	<u>CIRCUIT DESIGNATORS</u>	<u>DEVICE TYPE</u>	<u>POWER</u>	
			<u>TYPICAL (MA)</u>	<u>MAXIMUM (MA)</u>
Hex Register	U1, U2, U4	54LS174	16	26
Counter	U2	54LS161	18.5	31.5
Quad and Gate	U5	54LS08	3.4	6.8
Dual D Flip Flop	U6, U7, U13	54LS74	4	8
Triple Nand Gate	U18	54LS10	1.2	2.3
Quad EXC-OR Gate	U8	54LS86	6.1	10
Quad Register	U14, U15, U16, U17	54LS175	11	18
Prom	U9, U10, U11, U12	HM7641	125	170
Multiplexor	U19, U20, U21	54LS151	6	10
Demultiplexor	U30, U31, U32, U33	54LS138	6.3	10
Microprocessor BIT-Slice	U25, U27, U28, U29	AM2901B	160	280
Microprogram Sequence	U22, U23, U24, U25	AM2911	80	130

TABLE 2(b). MICROCONTROLLER BOARD POWER REQUIREMENTS

<u>DEVICE TYPE</u>	<u>QUANTITY</u>	<u>POWER</u>	
		<u>TYPICAL (MW)</u>	<u>MAXIMUM (MW)</u>
54LS174	3	240	390
54LS161	1	92.5	157.5
54LS08	1	17	34
54LS74	3	60	120
54LS10	1	6	11.5
54LS86	1	30.5	50
54LS175	4	220	360
HM7641	4	2500	3400
54LS151	3	90	150
54LS138	4	126	200
AM2901B	4	3200	5600
AM2911	4	1600	2600
TOTAL, WATTS		8.182	13.073

5.0 MICROCONTROLLER PROGRAMMING (TEST) ADAPTOR

The Microcontroller Programming Adaptor (Appendix H, Figure 1) consists of binary/hexadecimal readouts, a keyboard input for operator communications, and an RS232 serial input port for bulk memory fill to provide laboratory ROM simulation and debugging assistance of microcontroller system hardware and software.

The laboratory unit is constructed in a 19 inch rack configuration for ease of mounting, interfacing and maintenance.

5.1 Operating Characteristics

A detailed explanation of functional modes and display/keyboard characteristics is provided in the Microcontroller Programming (Test) Adaptor User's Guide.

5.2 Electrical Design

The programming adaptor includes multiple display readout, four 16-bit latches, an arithmetic comparator, an RS232 interface, and keyboard/control hardware.

The circuits employed are standard configurations of T²L logic, keyboard switching, and LED displays.

Reference to Smiths drawing number 90-103-01, may assist in understanding the electrical design.

5.2.1 Hexadecimal Readouts

The readouts use Digi-Cap LED indicators driven directly from standard hex inverter buffers or D-type latches. Sixteen LEDs are provided for a direct binary presentation and they are physically grouped into four 4-bit segments to assist in hexadecimal recognition.

5.2.2 16-Bit Latches

Operator inputs are stored in four 16-bit latches configured to accept and shift hex data. The memory address latch is also configured to increment when pulsed by the STEP key.

5.2.3 Arithmetic Comparator

A 16-bit arithmetic comparator provides the Breakpoint Equal function for automatic stop and scope synchronization.

5.2.4 RS232 Interface

The RS232 serial interface, set up for 300 baud rate, converts data into 8 bit ASCII. A ROM maps the ASCII into hexadecimal data. A 'BLANK' code is decoded to provide an end-of-word load command and memory address incrementation.

5.2.5 Keyboard/Control Hardware

All keys are debounced and decoded for proper action by the associated control circuits. Back lighting is accomplished via T-1 type incandescent bulbs.

Hard logic is used to provide the interaction of keys and operating characteristics.

PROM/TIMING TECHNICAL DESCRIPTION

APPENDIX D

PROM MEMORY MODULE

1.0 INTRODUCTION

The Prom Memory and Timing Board was developed to provide (1) 8K of random addressable fixed memory data; (2) 17 discrete binary timing clocks from an internal or external oscillator; (3) a Synchronizer clock pulse for up to three input levels and a power up condition; (4) a Collection gate for 3 input signals and 1 latched timing event; and, (5) a handshake control and output for an event. Typically, the synchronized clock pulse can be used for a machine reset pulse when 5V power is applied or from three external control lines. The handshake control can be set by Refresh implement, reset by Refresh Acknowledge and provide a timing signal between these two events. The Input Collection gate can be used to collect interrupts from three sources and whenever the Refresh Implement cycle is active.

2.0 PROM AND TIMING BOARD KEY FEATURES

- a. The Prom Memory is organized to provide up to 8 bit and 16 bits memory in 1K memory increments up to 8K. (16 different memory sizes are available, e.g., 1K x 8 bits to 8K x 16 bits).
- b. The Prom chip selected (S82S181) is fully comparable with a Bipolar ROM chip (S82S281) should less power be required.
- c. The memory data output has tri-state outputs.
- d. The Prom Memory has minimal input loading (input current low = 150ua/ input current high = 40ua) which permits several memory chips to be connected to the same address bus without excessive loading.
- e. A separate memory enable line is provided to permit multiple memory addresses to be used.
- f. BIT circuitry is not required for the memory since a memory checksum under program control can determine the operational status of the prom memory matrix.
- g. The on-board timing outputs provide 17 unique timing clocks.
- h. The main timing clock can be provided from an on-board 18 MHz oscillator or from an external clock.
- i. An output pulse is provided whenever +5V power is applied.
- j. Three inputs are provided for generating a synchronized Machine Reset pulse.

- k. A latch with reset control is provided for storing an event (typically Refresh Implement) until acknowledged. The occurrence of an event is provided as an output from the Prom and Timing board and is also connected to the Interrupt Collection gate.
- l. An Interrupt Collection gate is provided for three unique interrupt lines and an event latch.
- m. Pull up resistors are provided for the three off-board interrupt lines and the three off-board machine reset lines.
- n. Numerous test points are provided for monitoring internal board operation such as memory chip select, timing clocks, resets, machine clear, oscillator clock (internal or external).
- o. Power is minimized through the use of LS circuits.

3.0 FUNCTIONAL DESCRIPTION

The three fundamental functions of the Prom and Timing board are memory, timing generation and Refresh/Reset/Interrupt logic. Detailed descriptions are outlined in the following paragraphs.

3.1 Prom Memory (Figure 1)

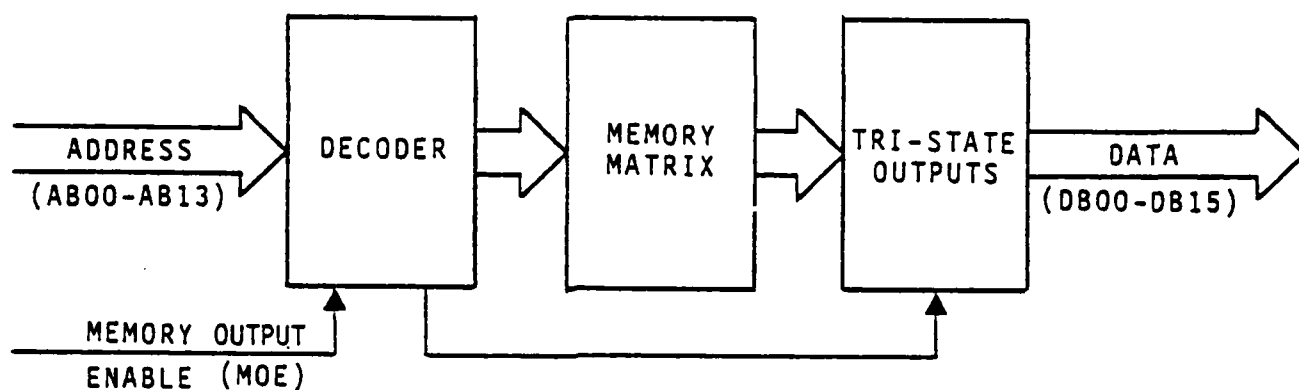
The Prom memory is controlled by 14 address lines and a memory enable control line. When data from Prom Memory is required, the memory is selected by the Memory On Enable (MOE) control line. The address is decoded and the data in the corresponding location in the memory matrix is presented to the data lines.

The Prom Memory consists of 16 - 1K x 8 bit 82S181 prom chips (U2-U17) and a 3 to 8 line decoder, 54LS138 (U1). (See Appendix A.) The 10 LSBs of the memory address (AB00-AB09) are presented to each prom chip to select 1 of 1024₁₀ locations. The outputs of a pair of prom chips are enabled by the decoding of Memory Address Lines AB10-AB13 in circuit U1 when MOE is low. Each of the 8 outputs of U1 is connected to a 1K Prom pair to provide 8K memory capacity. Table 1 is a chip select truth table. A Prom chip is selected whenever the CE1 is low.

For the DIWAC configuration U14-U17 are not installed, limiting the on-board memory capacity to 6K 16-bit words.

3.2 Timing Generator (Figure 2)

A block diagram of the Timing generator is shown in Figure 2. Seventeen system clocks are derived from an on-board 18 MHz $\pm 0.005\%$ oscillator or an external frequency source. The clock source is selected by the OSC EN control signal. The system clock is presented to two counter chains.

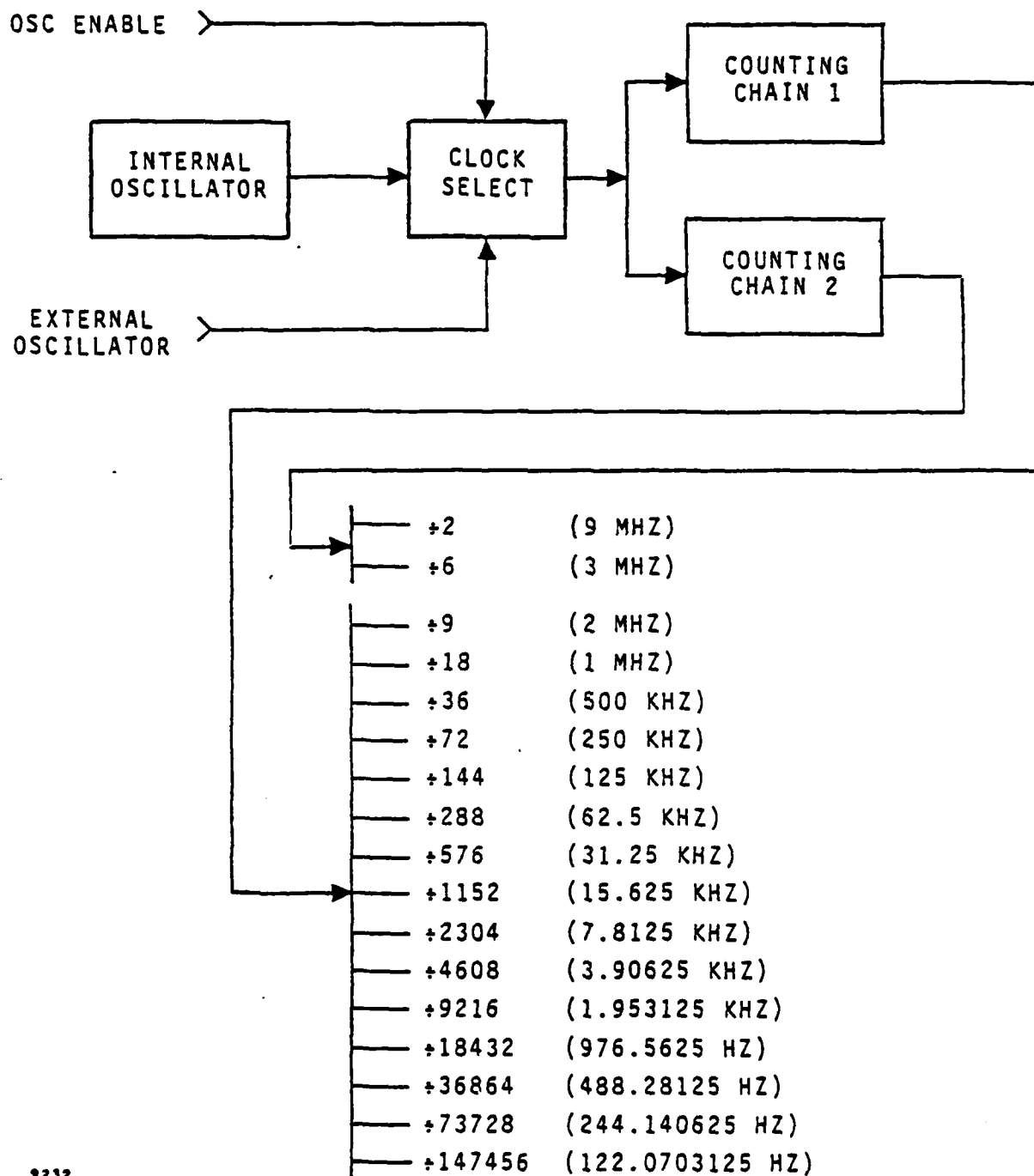


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FIGURE 1. PROM MEMORY BLOCK DIAGRAM

TABLE 1. MEMORY DECODER TRUTH TABLE

AB13	AB12	AB11	AB10	$\overline{\text{MOE}}$	CHIP SELECTED
X	X	X	X	H	None
L	L	L	L	L	U2/U3
L	L	L	H	L	U4/U5
L	L	H	L	L	U6/U7
L	L	H	H	L	U8/U9
L	H	L	L	L	U10/U11
L	H	L	H	L	U12/U13
L	H	H	L	L	U14/U15
L	H	H	H	L	U16/U17



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FIGURE 2. TIMING GENERATOR

The high frequency counter chain provides divide by 2 and 6 clocks. The low frequency counter chain provides 15 clocks in accordance with the relationship shown below:

$$\text{Master Clock Freq.} \times \frac{1}{9} \times \frac{1}{2^N} \text{ where } N = 0 \text{ to } N = 14$$

Circuits U20-U28 comprise the elements of the timing generator. U22 is an 18 MHz $\pm 0.005\%$ oscillator. If the OSC-EN is high, the on-board oscillator clock is passed through circuit U21-11. Circuit U21-8 passes the external and on-board clocks to two 4-bit synchronous counters for division.

NOTE

If an external oscillator is required, signal OSC-EN is low causing pin 10 of U21 to be high. The EXT OSC input at U21-9 is inverted through U21-8. If the on-board oscillator is used OSC-EN is high and an external oscillator is not connected. (U21-9 is held high by pull-up resistor R26.)

The selected system clock is presented to counters U20 and U24. Counter U20 is a 4-bit counter configured as a divide by six counter by connecting inputs B and C to ground and A and D to 5V. Outputs Q_B and Q_C from counter U20 are connected to Nand Gate U21 - 1, 2 and present a low to U20. The load input of counter U20 which causes A₉ to be preset into the counter when the next clock pulse occurs. (The count goes from 9 through 14 and presets - See Figure 3.)

The low frequency counter chain (U24-U28) consists of a $\div 9$ and four $\div 16$ counters. The divide by 9 counter (U24) is preset to a count of 4 (All inputs except Q_C are tied to ground) by presetting the counter to a count of 4 during the first clock pulse after Q_C and Q_D go high. Therefore, U24 counts from 4 through 12 between presets. (See Figure 4.)

The subsequent counters (U25-U28) in this chain are clocked at a 2 MHz rate with counts being propagated by the carry output of each series counter.

3.3 Reset/Refresh/Interrupt Logic

A simplified block diagram of the Reset/Refresh/Interrupt logic is shown in Figure 5. Any of four inputs (Reset 1, Reset 2, Reset 3 or 5V turn-on) cause a Machine Clear pulse (MACLR). The next 9 MHz clock synchronizes the pulse with system timing.

The Refresh Implement logic sets a latch when the refresh implement event occurs. The event is stored until a positive reset indication (RFAK) is received.

The Interrupt Collector Gate provides an interrupt signal whenever any of three signals (INT1, INT2, or INT3) or refresh implement occur.

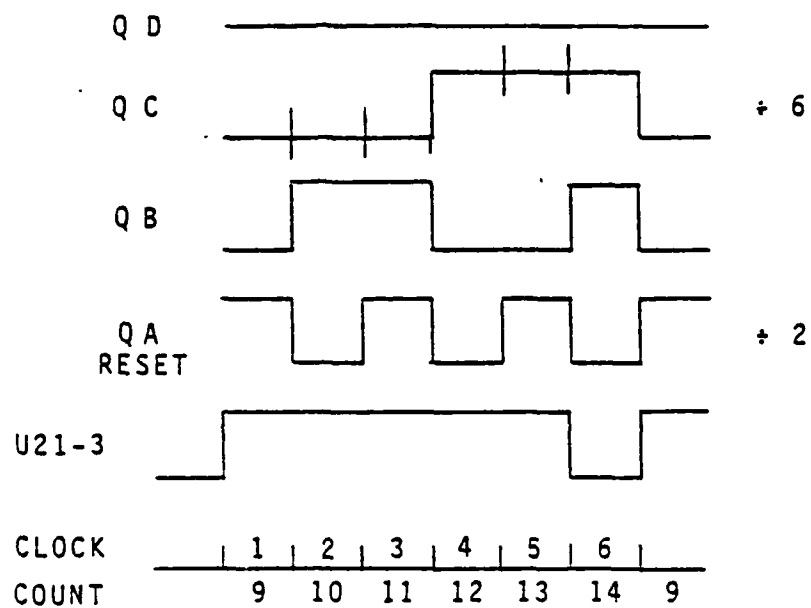


FIGURE 3. COUNTER U20 TIMING DIAGRAM

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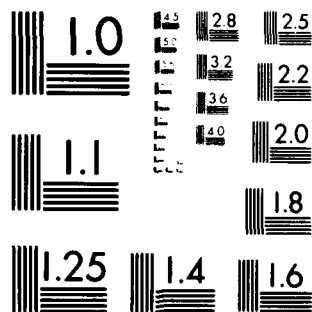
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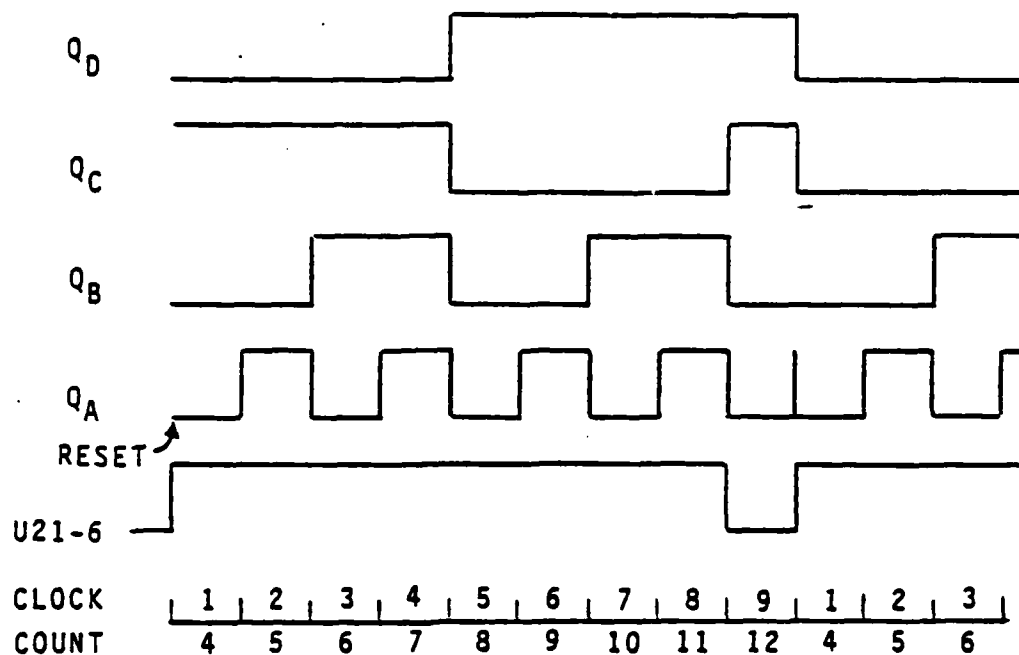
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FIGURE 4. COUNTER U24 TIMING DIAGRAM

The reset logic consists of circuits U19 and U18. A low at the input to U19 - 9, 10, or 12 from Reset 1, Reset 2 or Reset 3 cause U19 - 8 to go high. This high is clocked into latch U18 - 12 during the first occurrence of the 9 MHz clock (2 oscillator clock). When this occurs, U19 - 8 goes low. When the low signal is removed, the latch resets (U18 - 12 goes high). During the reset 9 MHz clock cycle the low signal is removed. Diode CR1, C17 and R13 provide a one-shot timing constant which cause a low on U19 - 13 until capacitor C17 charges to the high level threshold voltage of U19 - 13. When U19 - 13 is low, this condition is stored in latch U18 thereby providing a power-up Machine Clear.

The Refresh Implement latch (U18 - 5/6) is set on the positive edge of a Refresh Implement signal. The U18 - 5 output provides a storage of this condition until a Refresh Acknowledge (OUT09) is received. The refresh acknowledge is a low level which is connected to the direct reset of U18 which causes U18 - 5 to go low. U18 - 6 is connected to the Interrupt Collection Gate; thereby providing an interrupt signal when Refresh Implement occurs.

The output of the Interrupt Collection Gate U19 - 6 goes high whenever any of the three interrupt input signals (INT1, INT2, or INT3) go low or refresh implement occurs.

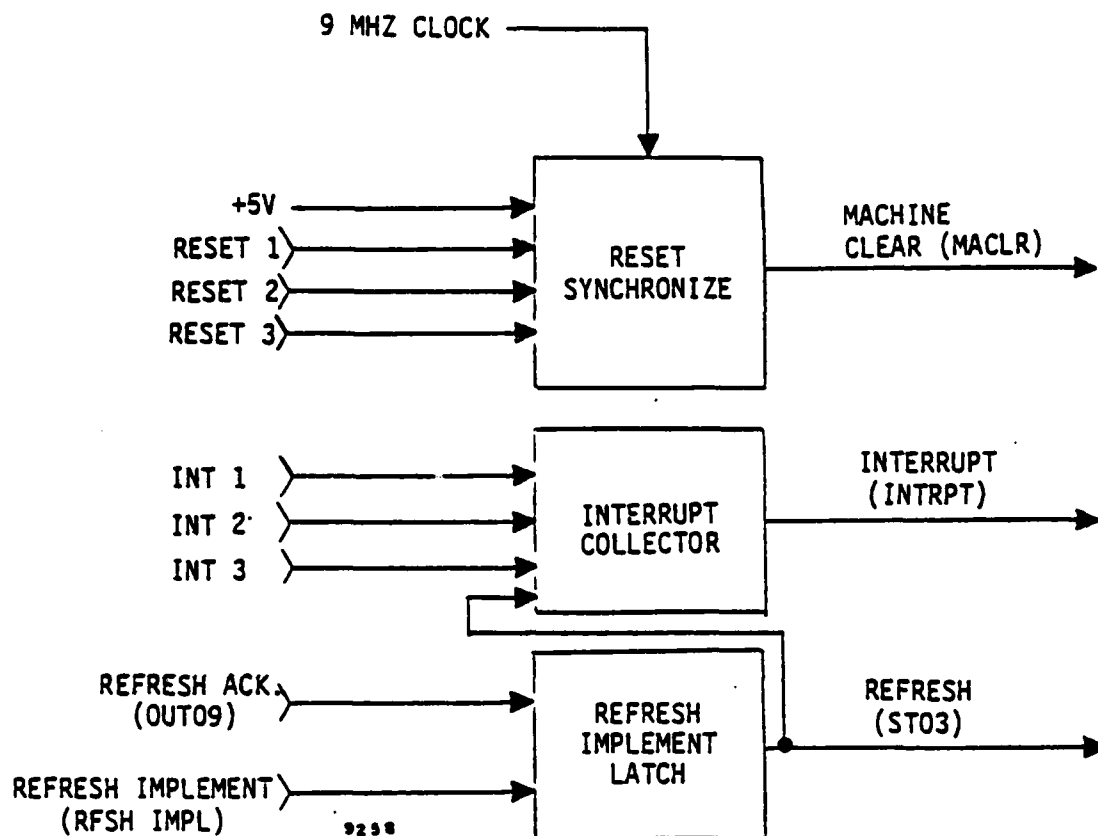


FIGURE 5. RESET/REFRESH/INTERRUPT LOGIC

4.0 INPUTS/OUTPUTS

The Prom Timing Board has three connectors; signal connectors P1A and P1B and test connector J1. Pinouts are shown in Tables 2, 3, and 4, respectively.

5.0 POWER CHARACTERISTICS

Table 5(a) delineates the type of device, circuit designators, device numbers and typical/maximum power for each device used. Table 5(b) summarizes the power requirements for 6K and 8K of Prom Memory.

TABLE 2. P1A PIN CONNECTIONS (PROM MEMORY)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	GND	28	DB03 Memory
2	GND	29	AB11 Memory
3	DB04 Memory	30	AB10 Memory
4	DB05 Memory	31	AB09 Memory
5	DB06 Memory	32	AB08 Memory
6	DB07 Memory	33	AB07 Memory
7	DB11 Memory	34	AB06 Memory
8	DB10 Memory	35	AB05 Memory
9	DB09 Memory	36	AB04 Memory
10	DB08 Memory	37	ST03 Interrupt
11	RESET 1 Interrupt	38	RFSH IMPL Interrupt
12	DB15 Memory	39	
13	RESET 2 Interrupt	40	
14	RESET 3 Interrupt	41	
15	INT 1 Interrupt	42	
16	INT 2 Interrupt	43	
17	INT 3 Interrupt	44	
18	DB14 Memory	45	
19	OUT 09 (RFAK) Interrupt	46	AB03 Memory
20	DB13 Memory	47	
21		48	AB01 Memory
22	DB12 Memory	49	AB13 Memory
23		50	AB02 Memory
24		51	AB12 Memory
25	DB00 Memory	52	+5V
26	DB01 Memory	53	+5V
27	DB02 Memory	54	

TABLE 3. P1B PIN CONNECTIONS (PROM MEMORY)

<u>Pin No.</u>	<u>Signal</u>		<u>Pin No.</u>	<u>Signal</u>	
1	+5V		28	9 MHz	Timing
2	+5V		29		
3			30		
4			31	EXT OSC	Timing
5			32	OSC EN	Timing
6	AB00	Memory	33		
7			34		
8			35	~~MACLR~~	Interrupt
9			36	MOE	Memory
10	INTRPT	Interrupt	37		
11	2 MHz	Timing	38		
12	1 MHz	Timing	39		
13	500 KHz	Timing	40		
14	250 KHz	Timing	41		
15	125 KHz	Timing	42		
16	62.5 KHz	Timing	43		
17	31.25 KHz	Timing	44		
18	15.625 KHz	Timing	45		
19	7.8125 KHz	Timing	46		
20	3.9 KHz	Timing	47		
21	1.95 KHz	Timing	48		
22	975 Hz	Timing	49		
23	487.5 Hz	Timing	50		
24	243.75 Hz	Timing	51		
25	121.825 Hz	Timing	52	GND	
26			53	GND	
27	3 MHz	Timing	54		

TABLE 4. J1 PIN CONNECTIONS (PROM MEMORY)

Pin No.	Signal	Pin No.	Signal
1		28	
2		29	
3		30	
4		31	0-1K ENB
5		32	1-2K ENB
6		33	2-3K ENB
7		34	3-4K ENB
8		35	4-5K ENB
9		36	5-6K ENB
10		37	6-7K ENB
11		38	7-8K ENB
12		39	3 MHz
13		40	9 MHz
14		41	Oscillator Clock (INT/EXT)
15		42	Reset
16		43	<u>MACLR</u>
17		44	INTRPT
18		45	2 MHz
19		46	
20		47	
21		48	
22		49	
23		50	
24		51	
25		52	
26		53	
27		54	

TABLE 5(a). GENERAL DEVICE POWER CHARACTERISTICS

DEVICE NAME	CIRCUIT DESIGNATORS	DEVICE NUMBER	POWER	
			TYPICAL (MA)	MAX (MA)
Proms	U2-U17	82S181I	140	185
Decoder	U1	54LS138	6.3	10
Dual Nand	U19	54LS20	0.8	1.5
4-Bit Counters	U20/U24-U28	54LS161	18.53	31.5
Hex Inverter	U23	54LS04	2.4	4.3
Quad Nand	U21	54LS00	1.6	3.0
Clock	U22			
Dual D FF	U18	54LS74	4	8

TABLE 5(b). PROM TIMING BOARD POWER REQUIREMENTS

DEVICE	V _{CC}	Qty	Typ (MW)	Max (MW)	Qty	Typ (MW)	Max (MW)
Proms	5v	12	8400	11100	16	11200	14800
Decoder	5v	1	31.5	50	1	31.5	50
Quad Nand	5v	1	8	15	1	8	15
Hex Inverter	5v	1	12	21.5	1	12	21.5
Dual D FF	5v	1	20	40	1	20	40
4-Bit Counters	5v	6	555	945	6	555	945
Dual Nand	5v	1	4	7.5	1	4	7.5
TOTAL (WATTS)			9.0305	12.179		11.8305	15.879

APPENDIX A

DESCRIPTION

The 82S180 and 82S181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S180 and 82S181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

The 82S180 and 82S181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S180/181, F or N, and for the military temperature range (-55°C to +125°C) specify S82S180/181, F.

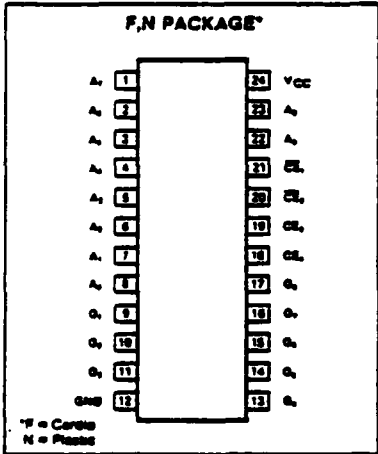
FEATURES

- Address access time:
N82S180/181: 70ns max
S82S180/181: 90ns max
- Power dissipation: 85µW/bit typ
- Input loading:
N82S180/181: -100µA max
S82S180/181: -150µA max
- On-chip address decoding
- Output options:
82S180: Open collector
82S181: Tri-state
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible

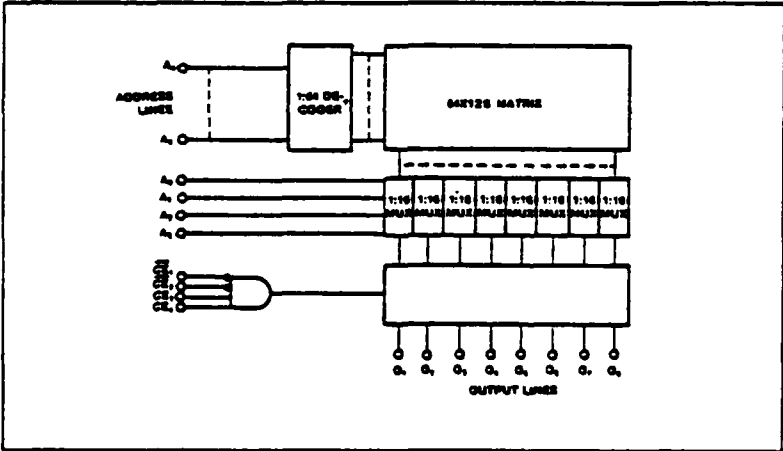
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _{OH} Output voltage		Vdc
High (82S180)	+5.5	
V _O Off-state (82S181)	+5.5	
T _A Temperature range		°C
Operating		
N82S180/181	0 to +75	
S82S180/181	-55 to +125	
T _{STG} Storage	-65 to +150	

82S180-F.N • 82S181-F.N

82S180-F.N • 82S181-F.N

DC ELECTRICAL CHARACTERISTICS N82S180/181: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
S82S180/181: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS ¹	N82S180/181			S82S180/181			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V_{IL} V_{IH} V_{IC}	Input voltage Low High Clamp $I_{IN} = -18\text{mA}$	2.0	-0.8	.85 -1.2	2.0	-0.8	.80 -1.2	V
V_{OL} V_{OH}	Output voltage Low High (82S181) $I_{OUT} = 9.6\text{mA}$ $\overline{CE}_1 = \text{low}, I_{OUT} = -2\text{mA}, \overline{CE}_2 = \text{low},$ $\overline{CE}_2 = \text{high}, \overline{CE}_4 = \text{high, high stored}$	2.4		0.45	2.4		0.5	V
I_{IL} I_{IH}	Input current Low High $V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$			-100 40			-150 50	μA
I_{OLX}	Output current Leakage (82S180) $\overline{CE}_1 = \text{high}, V_{OUT} = 5.5\text{V}, \overline{CE}_2 = \text{high},$ $\overline{CE}_3 = \text{low}, \overline{CE}_4 = \text{low}$			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S181) $\overline{CE}_1 = \text{high}, V_{OUT} = 0.5\text{V}, \overline{CE}_2 = \text{high},$ $\overline{CE}_3 = \text{low}, \overline{CE}_4 = \text{low}$			-40			-60	μA
I_{OS}	Short circuit (82S181) $\overline{CE}_1 = \text{high}, V_{OUT} = 5.5\text{V}, \overline{CE}_2 = \text{high},$ $\overline{CE}_3 = \text{low}, \overline{CE}_4 = \text{low}$ $V_{OUT} = 0\text{V}$	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current		140	175		140	185	mA
C_{IN} C_{OUT}	Capacitance Input Output $V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8			5 8		pF

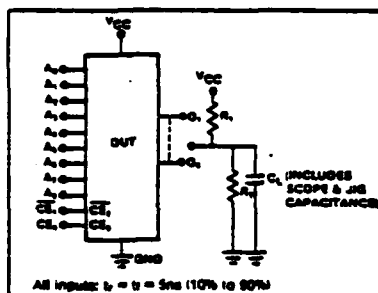
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1\text{k}\Omega$, $C_L = 30\text{pF}$
N82S180/181: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
S82S180/181: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82S180/181			S82S180/181			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
T_{AA} T_{CE}	Access time Output Output	Address Chip enable		50 20	70 40		50 20	90 50	ns
T_{CO}	Disable time Output	Chip disable		20	40		20	50	ns

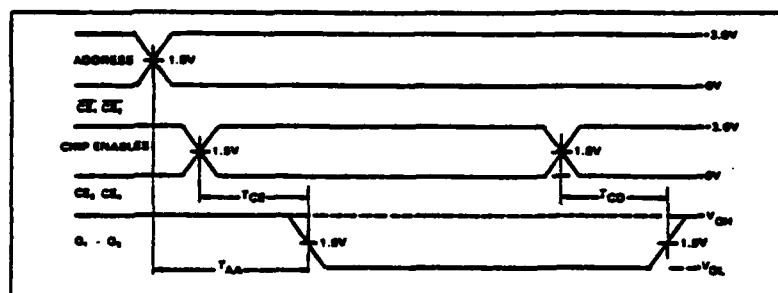
NOTES

- Positive current is defined as into the terminal referenced.
- Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = -25^{\circ}\text{C}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CCP} Power supply voltage To program ¹	$I_{CCP} = 375 \pm 75\text{mA}$, Transient or steady state	8.5	8.75	9.0	V
V_{CCH} Verify limit Upper		5.3	5.5	5.7	V
V_{CCL} Lower		4.3	4.5	4.7	V
V_S Verify threshold ²		1.4	1.5	1.6	V
I_{CCP} Programming supply current	$V_{CCP} = +8.75 \pm .25\text{V}$	300		450	mA
V_{IH} Input voltage High		2.4		5.5	V
V_{IL} Low		0	0.4	0.8	V
I_{IH} Input current High	$V_{IH} = +5.5\text{V}$			50	μA
I_{IL} Low	$V_{IL} = +0.4\text{V}$			-500	μA
V_{OUT} Output programming voltage ³	$I_{OUT} = 200 \pm 20\text{mA}$, Transient or steady state $V_{OUT} = +17 \pm 1\text{V}$	16.0	17.0	18.0	V
I_{OUT} Output programming current		180	200	220	mA
T_r Output pulse rise time		10		50	μs
t_p CE programming pulse width		0.3	0.4	0.5	ms
t_d Pulse sequence delay		10			μs
T_{PR} Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS} Initial programming pause	$V_{CC} = 0\text{V}$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$ Programming duty cycle ⁴				50	%
F_L Fusing attempts per link				2	cycle

NOTES

- Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.
- V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
- Care should be taken to ensure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle.
- Programming duty cycle is 50% after continuous programming at 100% duty cycle.
- This is an updated method of programming and does not obsolesce any programming systems presently being used.

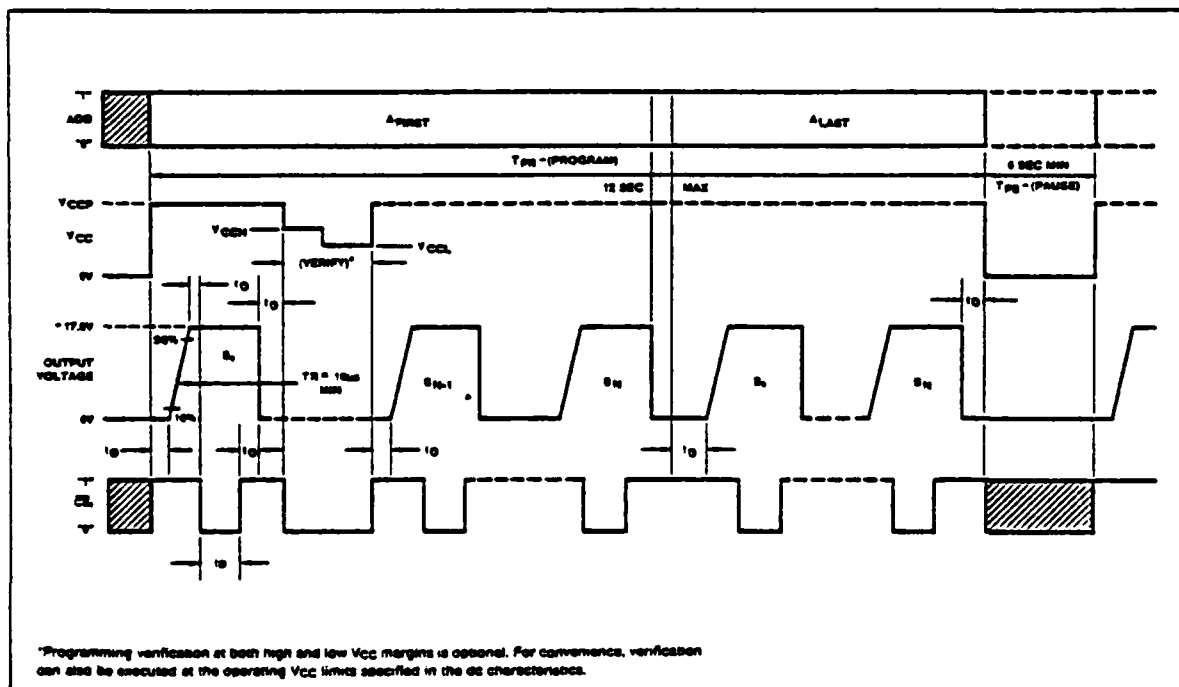
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82S160-F,N • 82S161-F,N

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10k\Omega$ resistor to V_{CC} . Apply $\overline{CE}_1$ = High, $\overline{CE}_2$ = Low, $\overline{CE}_3$ = High and $\overline{CE}_4$ = High.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After $10\mu s$ delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After $10\mu s$ delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After $10\mu s$ delay, remove +17V from the programmed output.
6. To verify programming, after $10\mu s$ delay, lower V_{CC} to $V_{CCV} = +5.5 \pm .2V$, and apply a logic low level to the $\overline{CE}_1$ input. The programmed output should remain in the high state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
8. After $10\mu s$ delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



DESCRIPTION

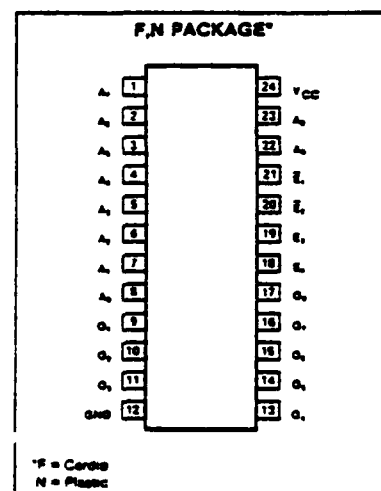
The 82S280 and 82S281 include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S280 and 82S281 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S280/281, F or N, and for the military temperature range (-55°C to +125°C) specify S82S280/281, F only.

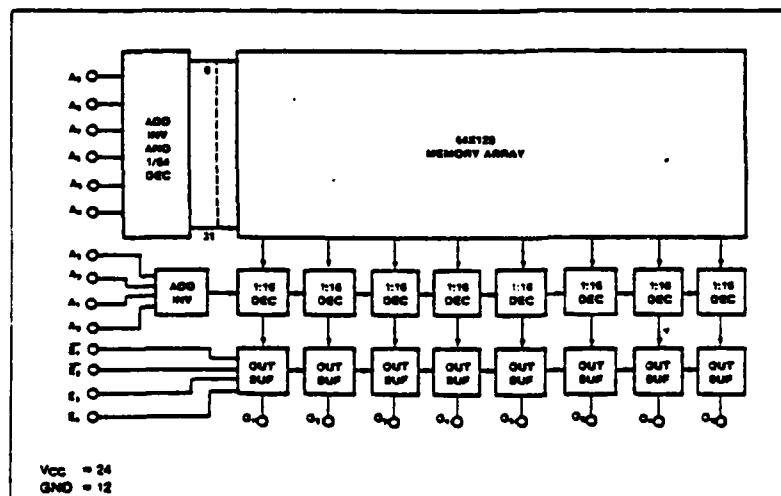
FEATURES

- Address access time:
N82S280/281: 70ns max
S82S280/281: 100ns max
- Power dissipation: 60mW/bit typ
- Input loading:
N82S280/281: -100μA max
S82S280/281: -150μA max
- On-chip address decoding
- Output options:
82S280: Open collector
82S281: Tri-state
- Enable = E1 • E2 • E3 • E4
- Fully TTL compatible

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VCC Supply voltage	+7	Vdc
VIN Input voltage	+5.5	Vdc
VO Output voltage	+5.5	Vdc
TA Off-state	+5.5	°C
TA Operating	0 to +75	
TA Storage	-55 to +125	
TSTG Storage	-65 to +150	

82S280-BU BIPOLAR ROM (1024X8)

82S280-F,N • 82S281-F,N

DC ELECTRICAL CHARACTERISTICS

N82S280/281: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S280/281: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS	N82S280/281 ¹			S82S280/281 ¹			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V_{IL} V_{IH} V_{IC}	Input voltage Low High Clamp	2.0	-0.8	.85 -1.2	2.0	-0.8	.80 -1.2	V
V_{OL} V_{OH}	Output voltage Low High	2.4		0.45 High stored	2.4		0.5	V
I_{IL} I_{IH}	Input current Low High			-100 25			-150 50	μA
$I_{O(OFF)}$ I_{OS}	Output current Hi-Z state Short circuit ³	-20		40 -40 -70	-15		100 -100 -85	μA mA
I_{CC}	V_{CC} supply current		100	140		100	150	mA
C_{IN} C_{OUT}	Capacitance Input Output		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
 N82S280/281: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S280/281: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82S280/281			S82S280/281			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
T_{AA} T_{CE}	Access time Output Output	Address Chip enable		40 20	70 40		40 20	100 50	ns
T_{CO}	Disable time Output	Chip disable		20	40		20	50	ns

NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = +5.0\text{V}$ and $T_A = +25^{\circ}\text{C}$.
3. No more than one output should be grounded at the same time.

RAM/BIT TECHNICAL DESCRIPTION

APPENDIX E

RAM AND BIT MODULE

1.0 INTRODUCTION

The RAM and BIT Board was developed to provide 1024 x 16 bits of Random Access memory, a frame watchdog timer and control/driver circuits for display of BIT status. The 256 location x 4 bit chip organization of the RAM memory provides byte/word capability of 256, 512, 768 and 1024 locations. The watchdog timer provides a timeout/microcontroller reset should frame reinitializing reset (refresh implement) be absent. The BIT logic/driver circuits provide the necessary logic and circuits to illuminate a DIWAC BIT indicator, a pilots BIT indicator and trigger a mechanical BIT indicator.

2.0 RAM AND BIT BOARD KEY FEATURES

- a. Read/Write Random Access Memory expandable from 256 locations x 1 byte to 1024 locations x 16 bits in 256 location increments.
- b. Buffered memory address lines to reduce address bus loading.
- c. Separate memory enable control to facilitate relocation of absolute memory address.
- d. A watch dog timer circuit which enables a 15.3Hz clock when the timer expires.
- e. BIT indication logic controlled by software and hardware faults.
- f. Permanent storage of any detected/declared failure.
- g. Delay of fault declaration to prevent erroneous fault indication.
- h. Drive provisions for three bit indicators (LEDs or mechanical).
- i. Sufficient test points to provide board fault isolation.
- j. Power is minimized through the use of LSI circuits.

3.0 FUNCTIONAL DESCRIPTION

3.1 Ram Circuit (Figure 1)

The elements comprising the RAM are address buffers, chip select decoder, RAM control buffers and the memory MUX. The address buffers are used to prevent the address bus from being loaded by the individual RAM chips.

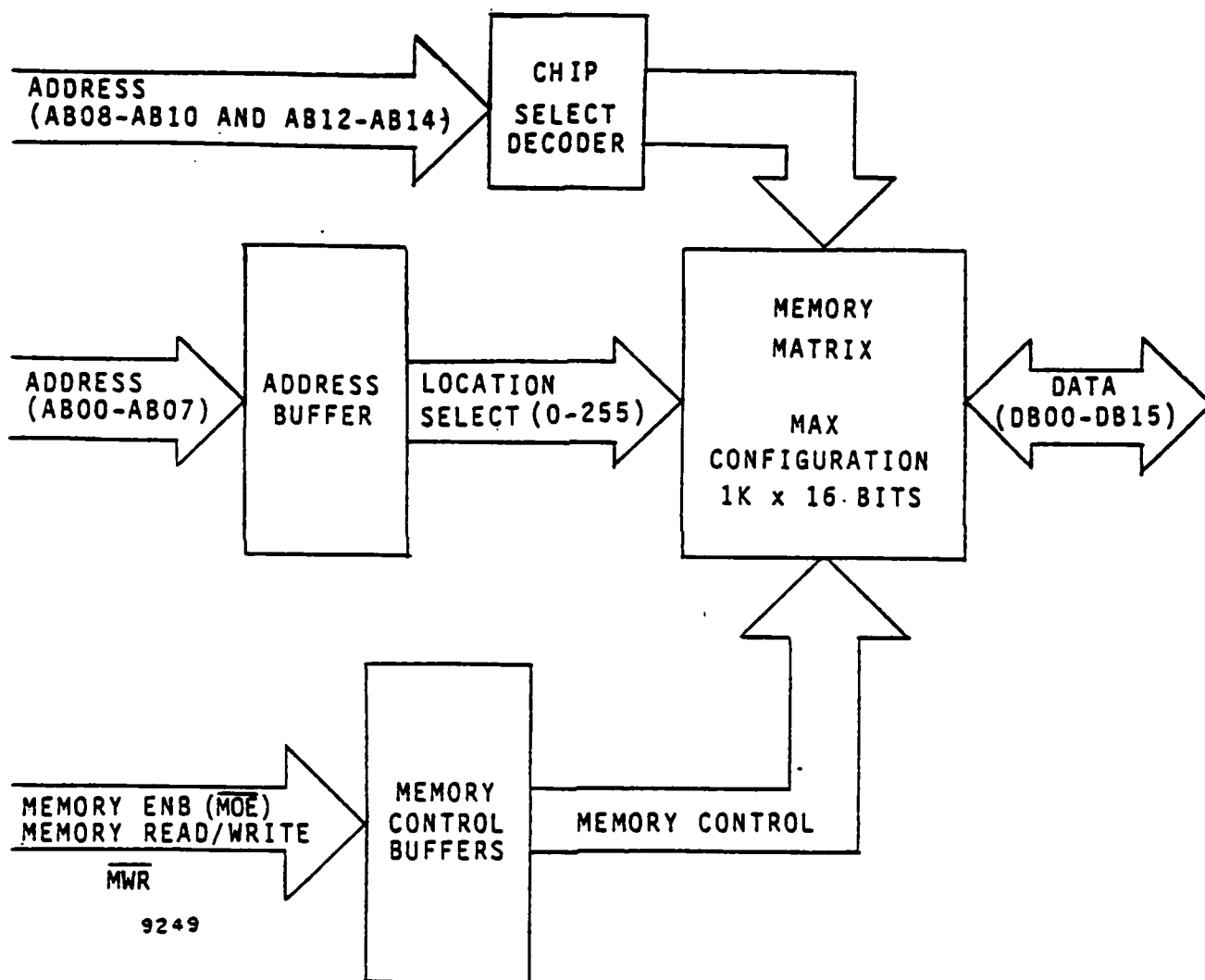


FIGURE 1. RAM MEMORY BLOCK DIAGRAM

The memory matrix is organized in 256 location x 16 bit banks. Four banks may be implemented for a total of 1024₁₀ locations. A particular bank is selected by decoding 6 bits of the address bus in the chip select decoder.

The Memory enable and read/write signals are used to control the operation of the RAM. The memory enable signal selects/deselects the entire RAM. The read/write signal controls the direction of memory data.

A BIT circuit is not provided for RAM since memory validation is confirmed by software tests.

3.2 Watch Dog Timer Circuit (Figure 2)

The watch dog timer consists of a divide by eight counter, timer and microcontroller start logic. (In DIWAC, a MACLR signal is generated whenever a reset is active or a power-up sequence is initiated.) A MACLR is stored in the microcontroller start logic until the software generated timer reset is initiated. This software controlled signal resets the MACLR store and starts the timer. If the timing period of the timer (45 msec) elapses without being restarted, a 15.3 Hz clock generates a reset pulse. The 15.3 Hz clock is obtained by counting a 122.1 Hz clock in the divide by 8 counter.

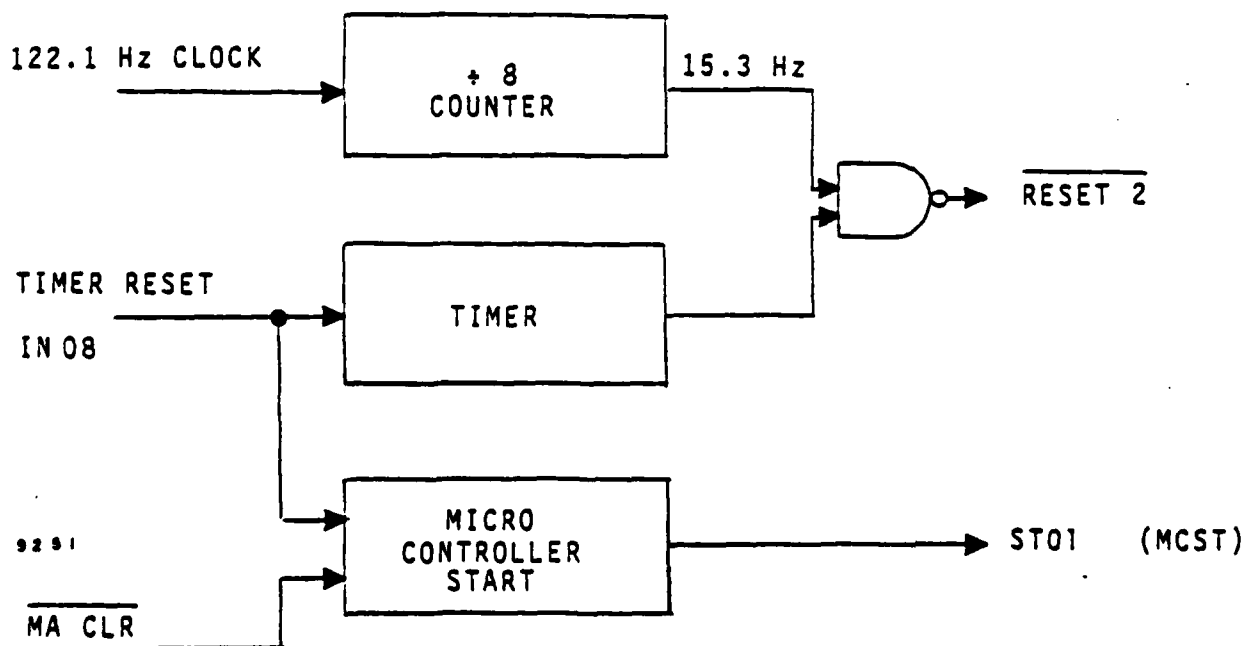


FIGURE 2. WATCH DOG TIMER

Through the use of software, an implied bit capability is provided for the watch dog timer. Typically, the processor hangs if the software resets, the watch dog timer reset or MACLR do not occur. This causes the BIT indicator circuit timer to expire.

3.3 BIT Indicator Drivers/Control Circuit (Figure 3)

The BIT indicator logic provides the drivers for three BIT status indicators, i.e., mechanical BIT flag, DIWAC BIT Indicator and the Pilots BIT Indicator. The DIWAC BIT indicator reflects the current status of the DIWAC and is on when NO-BIT alarm is present. The mechanical BIT flag is tripped and remains tripped at the first occurrence of a BIT alarm. The Pilot's BIT Indicator is illuminated and remains on after the first detection of a BIT alarm.

The BIT indicators are controlled by a timer and a BIT Latch. The timer is restarted under software control once per frame; however, if a failure occurs, the software controlled restart signal is inhibited and the timer expires. The expiration of the timer causes the BIT alarm to be stored in the BIT Latch. The BIT Latch can only be reset by a power-up condition.

The mechanical BIT flag is tripped with a pulse. The Pilot's BIT Indicator is driven on by the LED driver wherever the BIT latch is set.

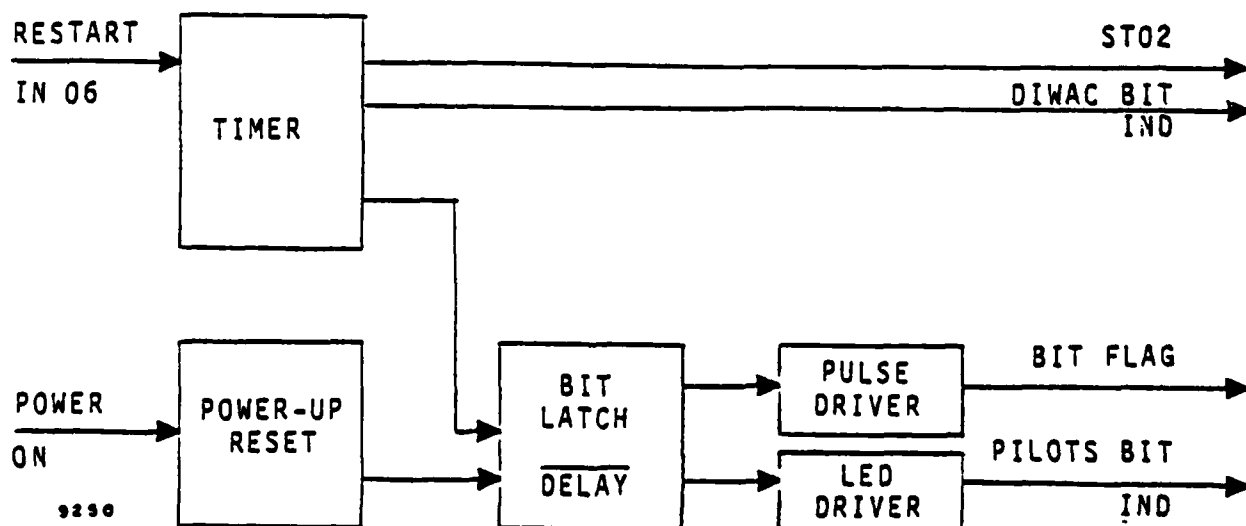


FIGURE 3. BIT INDICATOR DRIVERS/CONTROL

3.4 THEORY OF OPERATION

3.4.1 RAM

The 1K of RAM memory is comprised of circuits U1-U19. Memory banks U3-U6, U8-U11, U12-U15, and U16-U19 are selected by decoder U1. The truth table for decoder U1 is shown in Table 1. Each output of the decoder (CS1-CS4) when low enables 4 RAM chips (256 locations x 16 bits). The exact RAM location reference is obtained by the lower byte of the address bus (AB00-AB07). The address inputs are buffered by the non-inverting buffers in U2. The outputs of the U2 buffers are connected to the address inputs of all 16 RAM chips.

Memory Output Enable ($\overline{MOE}$) is passed through a non-inverting buffer (U7-4/16) and enables all RAM chips when low. The memory output enable control signal selects/or disables the RAM chip regardless of the memory address and offers further flexibility in selecting the absolute location of the RAM memory. The Memory Read/Write ($\overline{MWR}$) control signal is also buffered by a non-inverting buffer (U7-2/18) and is used to select RAM write when low and read when high. When RAM is enabled the data bus information (DB00-DB15) is stored in RAM when $\overline{MWR}$ is low and placed on the data bus when $\overline{MWR}$ is high.

Circuits U2 and U7 tri-state outputs are enabled by pins 1 and 19 being low.

TABLE 1. ADDRESS DECODER TRUTH TABLE

Address BIT						Active Decoder Output	Relative Memory Location	Selected Chips
AB14	AB13	AB12	AB10	AB09	AB08			
H	X	X	X	X	X		No Selection	
X	X	H	X	X	X		No Selection	
X	L	X	X	X	X		No Selection	
L	H	L	L	L	L	CS1 2000_{16}	or 2800_{16}	U3-U6
L	H	L	L	L	H	CS2 2100_{16}	or 2900_{16}	U8-U11
L	H	L	L	H	L	CS3 2200_{16}	or $2A00_{16}$	U12-U15
L	H	L	L	H	H	CS4 2300_{16}	or $2B00_{16}$	U16-U19

Special BIT circuits for RAM memory have not been provided since the RAM memory can be exercised and tested under software control. A typical software test sequence would move a portion of memory data (e.g., 5 words, 12 words, etc.) from one bank, store the data in CPU registers or RAM locations in another memory bank, store/recall data in the RAM memory locations vacated, and restore memory locations. This process is repeated until all memory locations are tested or non-recoverable faults occur.

3.4.2 Watch Dog Timer

The Watch Dog Timer provides a pseudo reset should consecutive refresh implement pulses be absent. The Watch Dog Timer consists of counter U20, one-shot U23, latch U23-9/8 and Nand Gate U21-3; the 122.1 Hz clock pulses are counted in counter U20. The 2^2 output of U2 (122.1 Hz/8 = 15.3 Hz) is presented to pin 1 of Nand Gate U21. The 15.3 Hz clock is gated through Nand Gate U21 causing RESET 2 to occur when pin 2 of U21 is enabled. U21-2 is enabled only when retriggerable one-shot (U23) is not retriggered before the one-shot timing constant expires. (The one-shot timing constant is $\approx$ 45 msec which is slightly less than 2 refresh implement frame times.) The retriggering of one-shot U23 is under software control (the positive edge of signal IN08).

When master clear (MACLR) occurs, latch U22-9 is set causing ST01 to go high. This latch is reset by input signal IN08.

BIT circuitry is not provided since the primary function of the watch dog timer is not exercised when Refresh Implement pulses are received. Moreover, the absence of Refresh Implement pulses does not constitute a DIWAC failure.

3.4.3 BIT Indicator Drivers and Control

The operational status profile of DIWAC is visually obtained by a DIWAC BIT Indicator, a Mechanical Indicator, and a Pilot's BIT Indicator. The mechanical indicator and pilot's BIT indicator are permanently set if a BIT alarm is detected during DIWAC operation. The DIWAC BIT indicator reflects the current status of the DIWAC (on for NO BIT Alarm pending). The mechanical indicator, once tripped, can only be manually reset; whereas, the pilot's BIT indicator once set, can only be reset by a power-up condition.

Circuits U25, U21-6, U21-8 and U22-5 are used to control the BIT indicators. Retriggerable one-shot U25 is used as a delay timer. Normally, the one-shot is retriggered under software control once per frame by the occurrence of signal IN06. The one-shot time constant is $\approx$ 90 msec. This time constant is $\approx$ twice that of the watch dog timer to ensure that an absence of the refresh implement frame reset does not cause a BIT alarm. (The watch dog timer expires and provides a pseudo Refresh Implement at 45 msec.) If a BIT alarm is detected, the software prevents signal IN06 from retriggering one-shot U25. If the one-shot timer constant expires, U25-3 goes low and is inverted through Nand Inverter U21-4, 5/6. This high clocks a high into the BIT alarm latch (U22-3 and causes the latch

to output (U22-6) to go low. Once the latch is set, it remains set until power is removed from the board. Resistor-capacitor network R5 and C22 provide a clear to the BIT alarm latch (U22-1) when power is applied to ensure the BIT alarm latch is initially in the reset position (U22-6 is high).

The DIWAC BIT Indicator is driven by the Q output of one-shot U25-5. This level is inverted by Nand Inverter U21-9, 10/8 when no BIT alarm. A high at the output of the Nand Inverter (U21-8) causes the DIWAC BIT Indicator to extinguish. Output connector signals DIWAC BIT indicator and DIWAC BIT IND facilitate the operation of a LED Indicator through current limited resistor R18.

The $\bar{Q}$ output of the BIT alarm latch (U22-6) is high when no BIT alarm has occurred. This high turns transistor Q1 on causing a low on pin 3 of comparator U24. Pin 2 of comparator U24 is fixed at +18V through resistor R10 and zener diode CR1. This keeps the output of comparator U24 high since the voltage applied to the comparator is +24V through resistor R11 and zener diode CR2, the high output of the comparator is +24V. When a BIT alarm is latched, the $\bar{Q}$ output of the BIT alarm latch (U22-6) goes low, causing transistor Q1 to turn off. The minus input of the comparator goes to +24V which causes the comparator output to go low. The low output of comparator U24 causes transistor Q2 to conduct and provide +28V on the Pilot's BIT IND signal line. A comparator low also causes transistor Q3 to conduct; however, capacitor C26 causes a high current base drive until capacitor C26 charges. This current pulse is suitable to trigger a magnetic latching relay.

Capacitor C24 is used to prevent the output of comparator U24 from going low when 28 volt power is applied.

BIT indicator drive circuitry and control logic has not been included since malfunctions in this logic could not be indicated.

4.0 INPUTS/OUTPUTS

The RAM and BIT board has three connectors, signal connectors P1A, P1B, and test connector J1. Pin and signal information is shown in Tables 2 through 4, respectively.

5.0 POWER CONSIDERATIONS

Table 5(a) delineates the type of device, circuit designators, device type and typical/maximum power for each device used. Table 5(b) summarizes the power requirements of the RAM and BIT logic.

TABLE 2. P1A PIN CONNECTIONS (RAM and BIT)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	GND	28	DB03 Data
2	GND	29	
3	DB04 Data	30	AB10 Address
4	DB05 Data	31	AB09 Address
5	DB06 Data	32	AB08 Address
6	DB07 Data	33	AB07 Address
7	DB11 Data	34	AB06 Address
8	DB10 Data	35	AB05 Address
9	DB09 Data	36	AB04 Address
10	DB08 Data	37	
11		38	
12	DB15 Data	39	
13	RESET 2	40	
14		41	
15		42	
16	122.1 Hz Clock	43	
17		44	
18	DB14 Data	45	AB14 Address
19		46	AB03 Address
20		47	
21		48	AB01 Address
22	DB12 Data	49	AB13 Address
23		50	AB02 Address
24		51	AB12 Address
25	DB00 Data	52	+5V
26	DB01 Data	53	+5V
27	DB02 Data	54	

TABLE 3. P1B PIN CONNECTIONS (RAM and BIT)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	+5V	28	
2	+5V	29	
3		30	
4	<u>IN08</u> IN Channel 8	31	
5		32	
6	AB00 Address	33	
7		34	
8		35	<u>MACLR</u> Master Clear
9	BIT Flag Mech. Latch	36	<u>MOE</u> Memory Output Enable
10	Pilot's BIT Indicator	37	
11	<u>DIWAC</u> BIT IND LED	38	
12	<u>DIWAC</u> BIT IND LED	39	
13		40	
14	28V BIT	41	
15		42	
16		43	
17	<u>IN06</u> in Channel 6	44	ST02 Microcontroller up
18		45	
19		46	ST01 Master Clear Status
20	<u>MWR</u> MEMORY READ/WRITE	47	
21		48	
22		49	
23		50	
24		51	
25		52	GND
26		53	GND
27		54	

TABLE 4. J1 PIN CONNECTIONS (RAM and BIT)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	BIT on Drive	28	
2	BIT ON/OFF	29	
3	Watch Dog Timer	30	
4	15.3 Hz	31	
5		32	
6		33	
7		34	
8		35	
9		36	
10		37	
11	TAB07	38	
12	TAB06	39	
13	TAB05	40	
14	TAB04	41	
15	TAB03	42	
16	TAB02	43	
17	TAB01	44	
18	TAB00	45	
19	<u>TMOE</u>	46	
20	<u>TMWR</u>	47	
21		48	
22		49	
23		50	
24		51	
25		52	
26		53	
27		54	

TABLE 5(a). GENERAL DEVICE POWER CHARACTERISTICS

<u>DEVICE NAME</u>	<u>CIRCUIT DESIGNATORS</u>	<u>DEVICE NUMBER</u>	<u>POWER</u>	
			<u>TYPICAL (MA)</u>	<u>MAX (MA)</u>
Decoder	U1	54LS138	6.3	10
Octal Buffers	U2, U7	54LS244	26	45
RAM	U3-U6, U8-U19	93L422	65	90
Counter	U20	54LS161	18.33	31.5
Quad Nand	U21	54LS00	1.6	3.0
Dual D FF	U22	54LS74	4	8
One Shot	U23, U25	54LS123	12	20
Comparator	U24	LM111	5.1 (24V)	6. (24V)
Driver Circuits	Q1-Q3		22.8 (28V)	22.8(28V)

TABLE 5(b). RAM AND BIT BOARD POWER REQUIREMENTS

<u>DEVICE</u>	<u>V_{cc}</u>	<u>Qty</u>	<u>Typical (MW)</u>	<u>Maximum (MW)</u>
Decoder	5	1	31.5	50
Octal Buffers	5	2	260	450
RAM	5	16	5200	7200
Counter	5	1	91.65	157.5
Quad Nand	5	1	8	15
Dual D FF	5	1	20	40
One Shot	5	2	120	200
Comparator	28	1	122.4	144
Driver Circuits	28	LOT	<u>638.4</u>	<u>638.4</u>
TOTAL			6.492 Watts	8.8949 Watts
5V			5.731 Watts	8.1125 Watts
28V			0.761 Watts	0.7824 Watts

APU TECHNICAL DESCRIPTION

APPENDIX F

ARITHMETIC PROCESSOR UNIT MODULE

1.0 INTRODUCTION

The solving of complex mathematical equations often requires the use of trigonometric operations, fixed and floating point numbers, double precision numbers and other mathematical operations. The Arithmetic Processor Unit (APU) was developed to facilitate mathematical operations in an Assembly language environment where speed of execution and available memory are at a premium.

The APU board provides a dual channel byte or word oriented scheme, capable of performing 43 mathematical operations. The specific mathematical operations are delineated in Table 1. The APU board contains Input/Output control, additional voltage regulation, Reset timing control and Input/Output timing signals.

2.0 ARITHMETIC PROCESSOR UNIT KEY FEATURES

- a. Two completely independent APU channels for increased throughput.
- b. Each APU channel can be operated in the byte or word mode.
- c. 43 different mathematical operations including floating power and fixed power arithmetic, trigonometric and algorithm operations.
- d. Complete operation of either APU channel is accomplished by typical I/O commands.
- e. Appropriate timing signals are provided to compensate for variations in data and mathematical operations.
- f. Independent power regulation for V_{DD} (+12 volts) is provided for each APU channel.
- g. Each APU channel is controlled by the driving processor (μ controller).
- h. Power-up and system resets are provided.
- i. APU commands, status and data are transferred on a single bidirectional bus.
- j. Test points are provided for monitoring of the operation of each APU channel.
- k. Validation of APU operation is accomplished by software thereby eliminating the need for on-board BIT.
- l. Each APU channel is implemented with separate circuits which permits a reduction in parts should only one APU channel be desired.

TABLE 1. MATHEMATICAL OPERATIONS

<u>OPERATION MNEMONIC</u>	<u>OPERATION DESCRIPTION</u>
<u>FIXED POINT 16 BIT</u>	
SADD	Add TOS to NOS. Result to NOS.
SSUB	Subtract TOS from NOS. Result to NOS.
SMUL	Multiply NOS by TOS. Lower half of result to NOS.
SMUU	Multiply NOS by TOS. Upper half of result to NOS.
SDIV	Divide NOS by TOS. Result to NOS.
<u>FIXED POINT 32 BIT</u>	
DADD	Add TOS to NOS. Result to NOS.
DSUB	Subtract TOS from NOS. Result to NOS.
DMUL	Multiply NOS by TOS. Lower half of result to NOS.
DMUU	Multiply NOS by TOS. Upper half of result to NOS.
DDIV	Divide NOS by TOS. Result to NOS.
<u>FLOATING POINT 32 BIT</u>	
FADD	Add TOS to NOS. Result to NOS.
FSUB	Subtract TOS from NOS. Result to NOS.
FMUL	Multiply NOS by TOS. Lower half of result to NOS.
FDIV	Divide NOS by TOS. Result to NOS.
<u>DERIVED FLOATING POINT FUNCTIONS</u>	
SQRT	Square Root of TOS. Result in TOS.
SIN	Sine of TOS. Result in TOS.
COS	Cosine of TOS. Result in TOS.
TAN	Tangent of TOS. Result in TOS.
ASIN	Inverse Sine of TOS. Result in TOS.
ACOS	Inverse Cosine of TOS. Result in TOS.
ATAN	Inverse Tangent of TOS. Result in TOS.
LOG	Common Logarithm (base 10) of TOS. Result in TOS.
LN	Natural Logarithm (base e) of TOS. Result in TOS.
EXP	Exponential (e^x) of TOS. Result in TOS.
PWR	NOS raised to the power in TOS. Result in NOS.
<u>DATA MANIPULATION COMMANDS</u>	
NOP	No Operation
FIXS	Convert TOS from floating point to 16-bit fixed point format.
FIXD	Convert TOS from floating point to 32-bit fixed point format.
FLTS	Convert TOS from 16-bit fixed point to floating point format.
FLTD	Convert TOS from 32-bit fixed point to floating point format.
CHSS	Change sign of 16-bit fixed point operand on TOS.
CHSD	Change sign of 32-bit fixed point operand on TOS.
CHSF	Change sign floating point operand on TOS.

TABLE 1. MATHEMATICAL OPERATIONS (CONT)

<u>OPERATION MNEMONIC</u>	<u>OPERATION DESCRIPTION</u>
<u>DATA MANIPULATION COMMANDS (CONT)</u>	
PTOS	Push 16-bit fixed point operand on TOS to NOS (Copy).
PTOD	Push 32-bit fixed point operand on TOS to NOS (Copy).
PTOF	Push floating point operand on TOS to NOS (Copy).
POPS	Pop 16-bit fixed point operand from TOS. NOS becomes TOS.
POPD	Pop 32-bit fixed point operand from TOS. NOS becomes TOS.
POPF	Pop floating point operand from TOS. NOS becomes TOS.
XCHS	Exchange 16-bit fixed point operands TOS and NOS.
XCHD	Exchange 32-bit fixed point operands TOS and NOS.
XCHF	Exchange floating point operands TOS and NOS.
PUPI	Push floating point constant " π " onto TOS. Previous TOS becomes NOS.

NOS = Next on Stack
TOS = Top of Stack

3.0 FUNCTIONAL DESCRIPTION

A block diagram of the APU board is shown in Figure 1. This diagram depicts the two independent APU channels and common ALU initialization/reset logic. Detailed block diagrams of APU channel 2 Output Control and Input Control are shown in Figure 2 and 3 respectively. (Since both channels are identical except I/O addressing, APU channel 2 has been used to represent block diagram operation.)

3.1 Arithmetic Processor Unit Output Control (Figure 2)

An APU channel output control consists of MS-Byte (DB08-DB15) and LS-Byte (DB00-DB07) command latches, output multiplexers, write/read control, chip select latch/control, data or command latch/control, channel I/O reset control, +12 volt regulator, initialization logic and a 9511A arithmetic processor (AP).

The MS-Byte out and LS-Byte out command latches store the resident processor (μ Controller) I/O request for transferring 8 bits from processor to APU. The transferred byte is interpreted as a data byte or a command by the 9511A AP depending on the setting of the Command/Data latch. If the MS-byte is selected, the OUT04 command is used. The OUT04 I/O command set the MS-byte latch which subsequently enables the MS-byte multiplexer and sets the Write latch. If the LS-byte is required, I/O command OUT03 is used. OUT03 causes the LS-byte latch to set, the LS-byte multiplexer to be enabled and the Write latch to set. Selecting either the MS-byte out or LS-byte out cause the chip select latch to set.

I/O command OUT05 is used to select 9511A AP data or command. When a command is requested, the data from the data bus is transferred to the 9511 AP via the selected LS-byte or MS-byte multiplexers. When 9511 AP data is requested, the data is transferred from the data bus via the LS-byte or MS-byte multiplexers to the 9511A AP.

Once a byte of data or command is transferred to the 9511A AP, all APU channel latches are reset to a quiescent condition. This is accomplished by an IN05 I/O command.

The +12 volt V_{DD} voltage required by the 9511A AP is obtained from the +20 volt to +12 volt regulator. The 9511A AP is reset by an external MACLR command. Since the reset of the 9511A AP requires five 3 MHZ clock periods, the Initialization control utilizes the 500KHZ system clock in conjunction with MACLR to reset the 9511A AP.

9511 AP signals ST08 and ST09 are used to control timing. The ST08 signal is used for data/command I/O transfers. ST09 is used to determine when the 9511A AP completed the execution of a command.

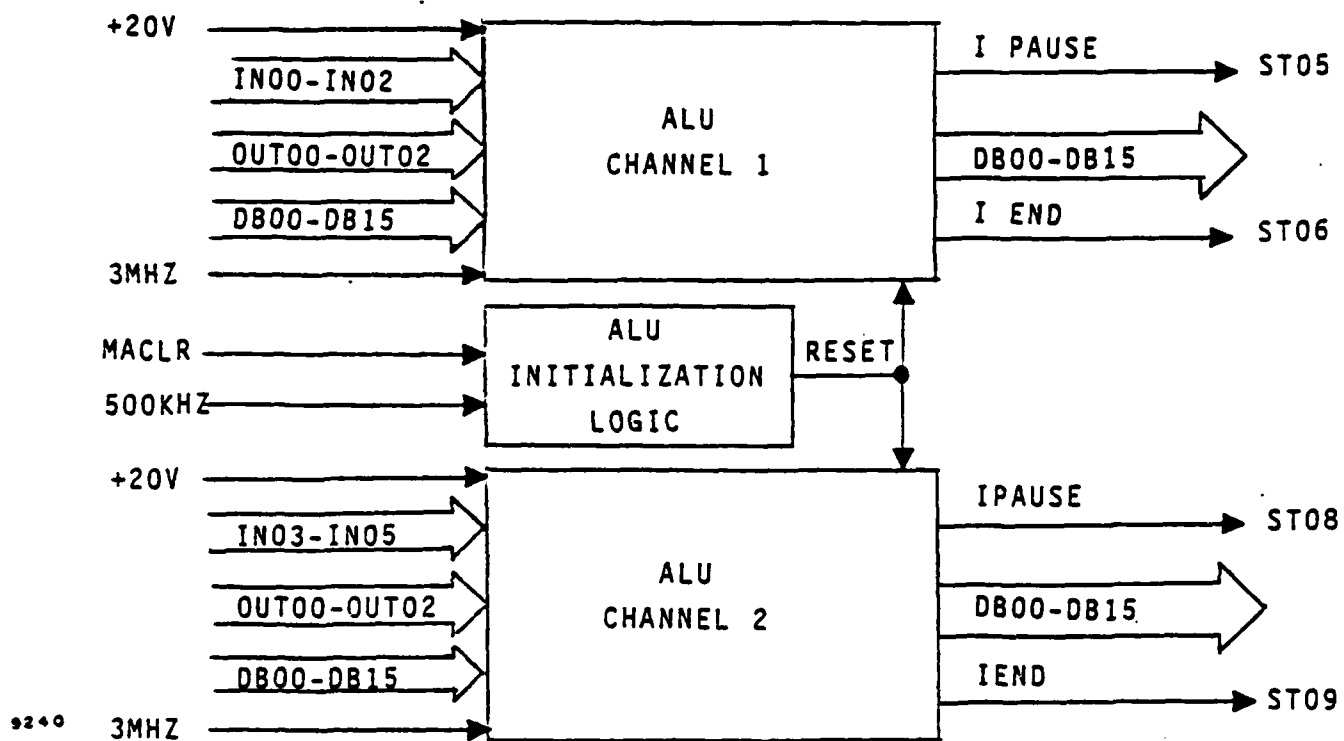


FIGURE 1. APU BLOCK DIAGRAM

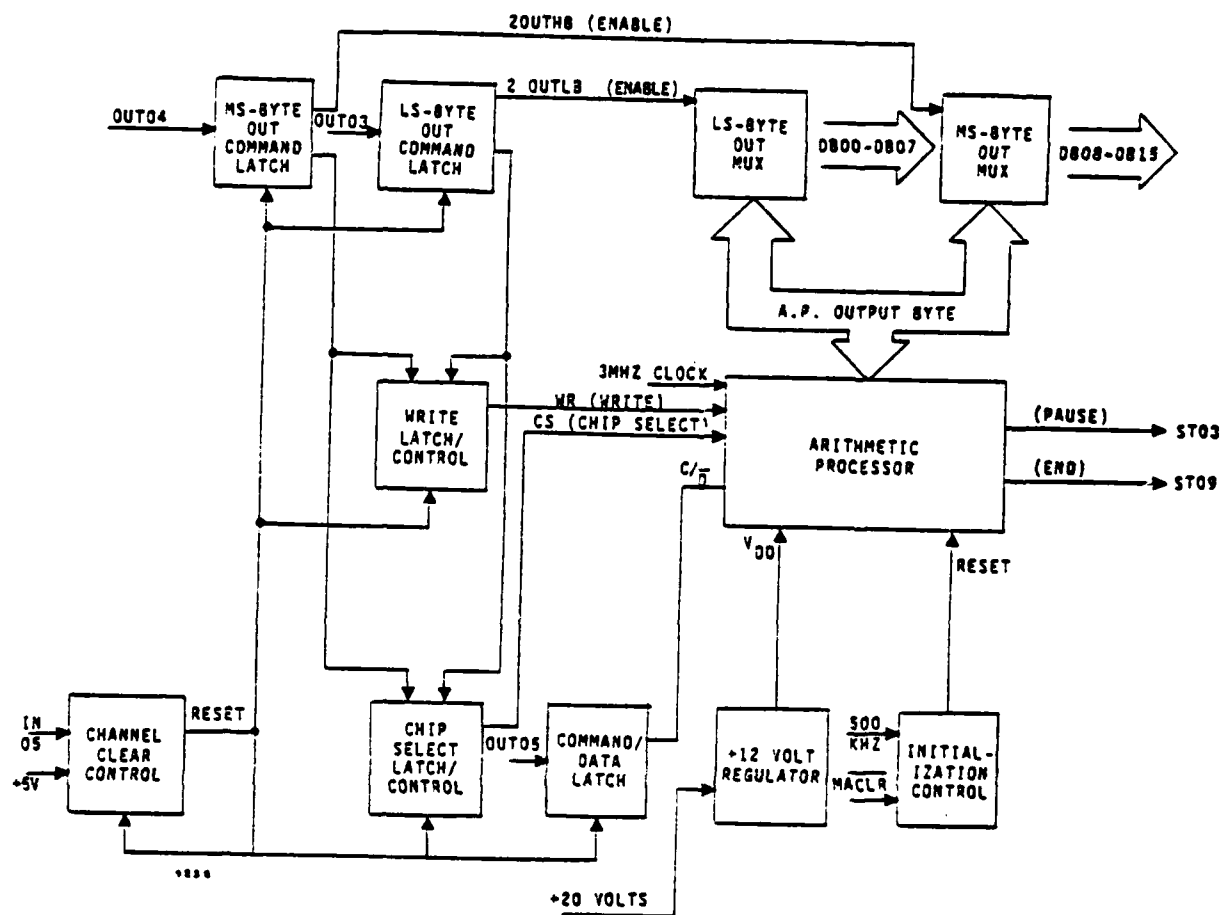


FIGURE 2. APU CHANNEL 2 OUTPUT CONTROL

3.2 Arithmetic Processor Unit Input Control (Figure 3)

The APU Input Control is used to transfer 9511 AP data or status to the resident processor (μ Controller). Since an APU channel is byte and word oriented and the 9511A AP is byte oriented, conversion from byte to word is accomplished by controlling the placement of a 9511A AP byte on the upper (DB08-DB15) or lower (DB00-DB07) portion of the data bus.

I/O commands associated with the APU Input Control are IN03, IN04, IN05 and OUT05. IN03 selects the LS-byte data bus position; whereas, IN04 selects the MS-byte data bus position. OUT05 selects the data transfer type, i.e., data or status. IN05 resets the APU channel logic.

The selection of MS-byte (IN04) or LS-byte (IN03) causes the respective latch to be set. The IN command latch enables the LS-byte in or MS-byte in multiplexer, sets the Read latch and sets the Chip Select latch. Depending on the setting of the command/data latch (I/O command OUT05), the data transferred from the 9511A AP to the data bus via the LS-byte/MS-byte multiplexer is status or resultant data. After the data transfer I/O command IN05 is used to clear all APU in channel logic. Signals ST08 and ST09 are available to the resident processor for determining data transfer timing and execution completion. The +12 volt required by the 9511 AP regulator is provided by converting +20 volts to the +12 volt V_{dd} voltage. The Initialization control provides a reset to the 9511A AP consistent with the reset duration requirements of the 9511A AP i.e., a minimum of five 3 MHz clock periods (500 KHz).

3.3 Typical Operational Sequences

The three primary factors which comprise the basic operation of an APU channel are Data, Command and I/O operation. Typically, data is transferred to an APU channel followed by an APU arithmetic command. Upon completion of the command, data is transferred from the APU to the resident processor. Status information is also available for determining the results/status of an APU channel. I/O operations include the transferring of data and the associated timing conditions.

Although all 9511A AP commands are implemented, only the following commands are used in the DIWAC program:

FADD	32-bit floating point add
FDIV	32-bit floating point divide
FIXS	32-bit floating point to 16-bit fixed-point conversion
FLTS	16-bit fixed point to 32-bit floating-point conversion
FMUL	32-bit floating point multiply
FSUB	32-bit floating-point subtraction
SQRT	32-bit floating-point square root
XCHF	Exchange 32-bit stack operands

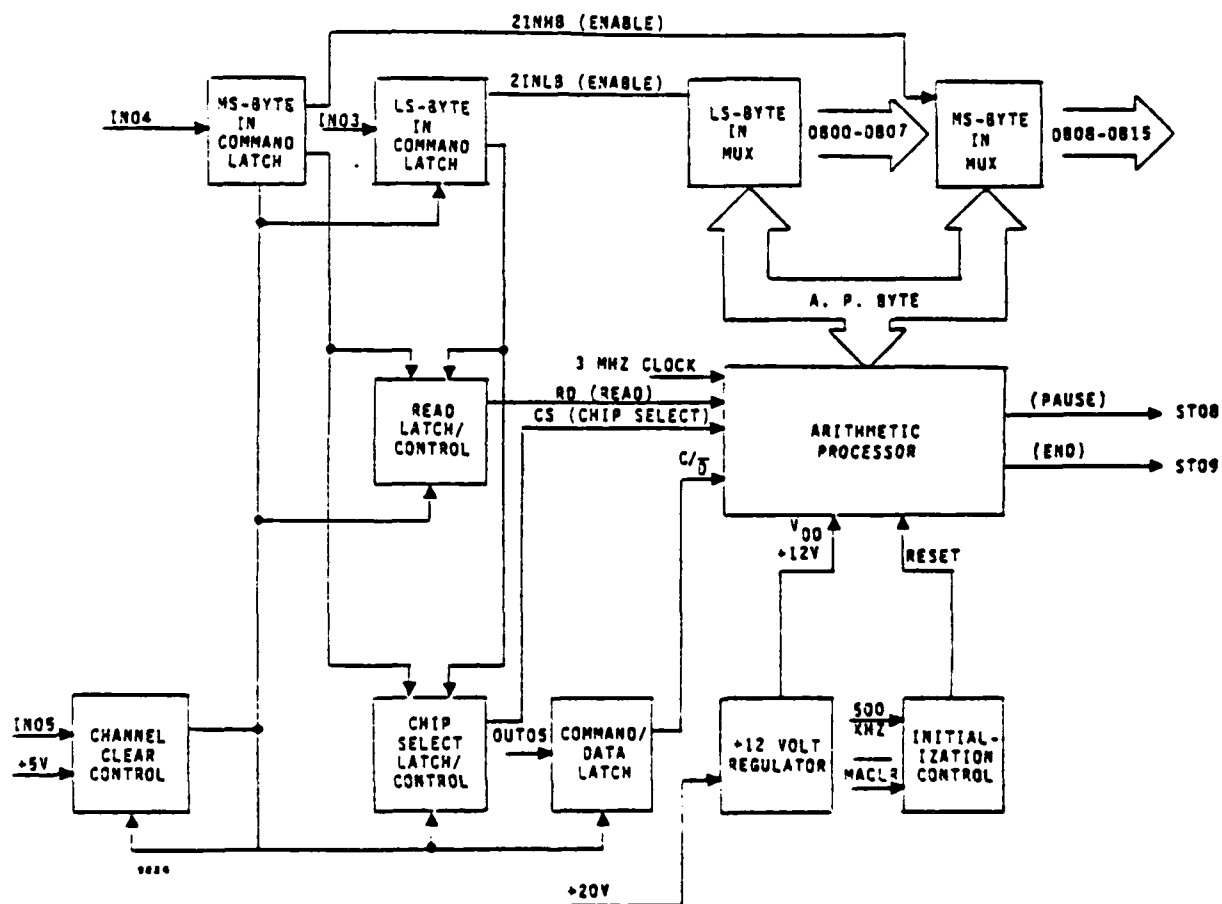


FIGURE 3. APU CHANNEL 2 INPUT CONTROL

The timing requirements between the 9511A APU and I/O data transfers, and the different time intervals required by the APU to execute a command require the monitoring of APU status signals to ensure proper operation. Use of the APU control signals is an integral part of the I/O operation.

As an example, consider a simple APU operation of FIXS (32-bit floating point to 16-bit fixed point conversion). Two 16-bit words (in a floating point format) are transferred to the APU channel followed by a FIXS command. After APU execution, one 16-bit word is returned plus APU Status. Table 2 provides a sample I/O sequence.

TABLE 2. APU I/O SEQUENCE

I/O Command IN05	Reset APU channel control
I/O Command OUT03	Transfer LS-byte of LS-word
Monitor Pause	Wait until transfer completed
I/O Command IN05	Reset APU channel control
I/O Command OUT04	Transfer MS-byte of LS-word
Monitor Pause	Wait until transfer completed
I/O Command IN05	Reset APU channel control
I/O Command OUT03	Transfer MS-byte of MS-word
Monitor Pause	Wait until transfer completed
I/O Command IN05	Reset APU channel control
I/O Command OUT04	Transfer MS-byte of MS-word
Monitor Pause	Wait until complete
I/O Command IN05	Reset APU channel control
I/O Command OUT05	Set Command/Data control to Command
I/O Command OUT03	Transfer command
Monitor END	Wait for command to be completed
I/O Command IN05	Reset APU channel control
I/O Command IN04	Set interface for Data Read
Monitor Pause	Wait until data available
I/O Command IN05	Read MS-byte of data; reset APU channel control
I/O Command IN03	Set interface for LS-byte data read
Monitor Pause	Wait until data available
I/O Command IN05	Read LS-byte of data; reset APU channel control
I/O Command OUT05	Set APU channel for Status Input
I/O Command IN03	Set interface for Status Read
Monitor Pause	Wait until data available
I/O Command IN05	Read status; reset APU channel control

NOTE: Execution complete monitoring could be an interrupt.

In the above example, 4 bytes of information was transferred to the APU. The 4 bytes were contained in 2 words which required the use of LS-byte and MS-byte transfers. After each transfer the interface was reset. The data transfer was ordered LSB to MSB. Prior to transferring the APU command byte, the APU was directed to the Command Mode. Once the command was transferred, the APU was monitored until the execution of the command was completed. The resultant data transfer is two bytes, MSB transferred first. Prior to each transfer, the APU was monitored to ensure data availability. After the data transfer, the APU was set to the Status Mode and status was read.

3.4 Detailed Theory of Operation

As shown in Figure 1, both APU channels are identical except for I/O commands and share common initialization logic. APU channel 2 has been selected for description as outlined through the following text. Table 3 delineates I/O command and interface strobes for each channel.

3.4.1 9511A Arithmetic Processor Chip

The basic element of an APU channel is a 9511A Arithmetic Processor Chip. Specific details of the 9511A device are contained in Appendix A, entitled "An 9511A Arithmetic Processor". However, general characteristics of this device are described below for continuity.

The 9511A AP is a 24 pin chip requiring 2 voltages (+5 Vcc and +12 Vdd) and ground. 8 bits of bi-directional data (DB0-DB7), reset, 3MHZ clock and control signals are also required.

The control signals and truth tables are provided in Tables 4 and 5 respectively.

TABLE 3. APU I/O INTERFACE

<u>FUNCTION</u>	<u>APU CHANNEL 1</u>	<u>APU CHANNEL 2</u>
MS-byte IN	IN01	IN04
MS-byte IN	IN00	IN03
MS-byte OUT	OUT01	OUT04
LS-byte OUT	OUT00	OUT03
Control Reset	IN02	IN05
Data/Command Select	OUT02	OUT05
Pause	ST05	ST08
End	ST06	ST09

TABLE 4. 9511A AP CONTROL SIGNALS

<u>SIGNAL</u>	<u>FUNCTION</u>	<u>DEFINITION</u>
Reset	Chip initialization	Active high - reset must be active for 5 - 3MHZ clock periods
C/ $\overline{D}$	Command/data input	Establishes type of data transfer Write - high command - low data Read - high status - low data
$\overline{RD}$	Read from chip	Active low - information from chip requested
$\overline{WR}$	Write to chip	Active low - information from chip requested
$\overline{CS}$	Chip select	Active low - conditions chip for data transfers
$\overline{PA}$	Pause	Low indicates data transfer not completed
$\overline{END}$	End	Active low - previous command has been completed

TABLE 5. ARITHMETIC PROCESSOR CONTROL TRUTH TABLE

<u>2C/$\overline{D}$</u> <u>(U6-5)</u>	<u>2$\overline{RD}$</u> <u>(U8-6)</u>	<u>2$\overline{WR}$</u> <u>(U13-11)</u>	<u>2$\overline{CS}$</u> <u>(U20-8)</u>	<u>FUNCTION</u>
X	X	X	H	N/A
L	H	L	L	Write data to APU
L	L	H	L	Read data from APU
H	H	L	L	Command to APU
H	L	H	L	Status from APU

3.4.2 Data Transfer to APU Channel

The data transfer timing sequences listed below are shown in Figure 4.

- a. Set data transfer mode to Data or Command
- b. Condition APU for output data transfer
- c. Reset APU channel

The selection of Command or Data transfer is accomplished by setting latch U6-5 high for command or low for data. Since U6-5 is normally low by a channel reset or power up condition, U6-5 is only required to be set when a Command transfer is required. This is accomplished by the positive clock signal at the completion of an OUT05 I/O command.

The APU is conditioned for transferring data by selecting I/O command OUT04 for the high byte or I/O command OUT03 for low byte data. At the completion of the respective I/O command, U5-5 goes high for high byte selection or U5-9 goes high for low byte selection. If U5-9 goes high (low-byte selection), DB00-DB07 data bus information is latched in octal latch U25. If U5-5 goes (high-byte selection), DB08-DB15 data bus information is latched in octal latch U27.

If U5-6 (high-byte selection) or U5-8 (low-byte selection) go low, Nand Gate output U12-6 goes high and Nor Gate output U16-1 to go low. This sets latch U18A and causes 2CS (Nand Inverter U20-8) to go low. The high output from latch U18A-4 and Nand Gate output U12-6 causes Nand Gate output U13-8 to go low and set latch U18B. 2WR is the inversion of U18B-7 and completes the Write cycle 9511A-1 condition inputs (see Table 4). 2WR (U13-11) causes U12-8 to go high thereby preventing U18A from being reset.

If a command is transferred to U30 (9511A-1 AP), end (U30-24) goes high until command execution is completed. If data bus transferred, (U30-17) goes low until the transfer is completed.

When a transfer to the APU is completed, the APU channel is reset by the permission of IN05 I/O command. At the completion of IN05, latch U7-8 goes low causing U14-3 to go high and U14-6 to go low. Resistor R18 and capacitor C12 provides a time delay for pulse stretcher. A low at Nand Gate Inverter Output (U14-6) resets U18B causing U18B-7 to go low and Nand Gate U13 to go high. This high removes the write select at 9511A-1 (U30) and the reset lock-out at Nand Gate U12-11 and causes latch U5-5 (high-byte select), latch U5-9 (low-byte select) and channel reset latch U7-9 to be cleared.

The output of Nand Gate U14-6 is inverted to a high and causes U12-8 to go low which resets the C/D latch (U6-5) and latch U18A to a low. When U18A-4 goes low the 2CS signal (U20-8) removes the 9511A-1 (U30) chip select. (It is noted that the RC (R18/C12) pulse stretcher ensures the output select latches (U5-5 or U5-9) are reset before the reset level to latch U18A is removed.)

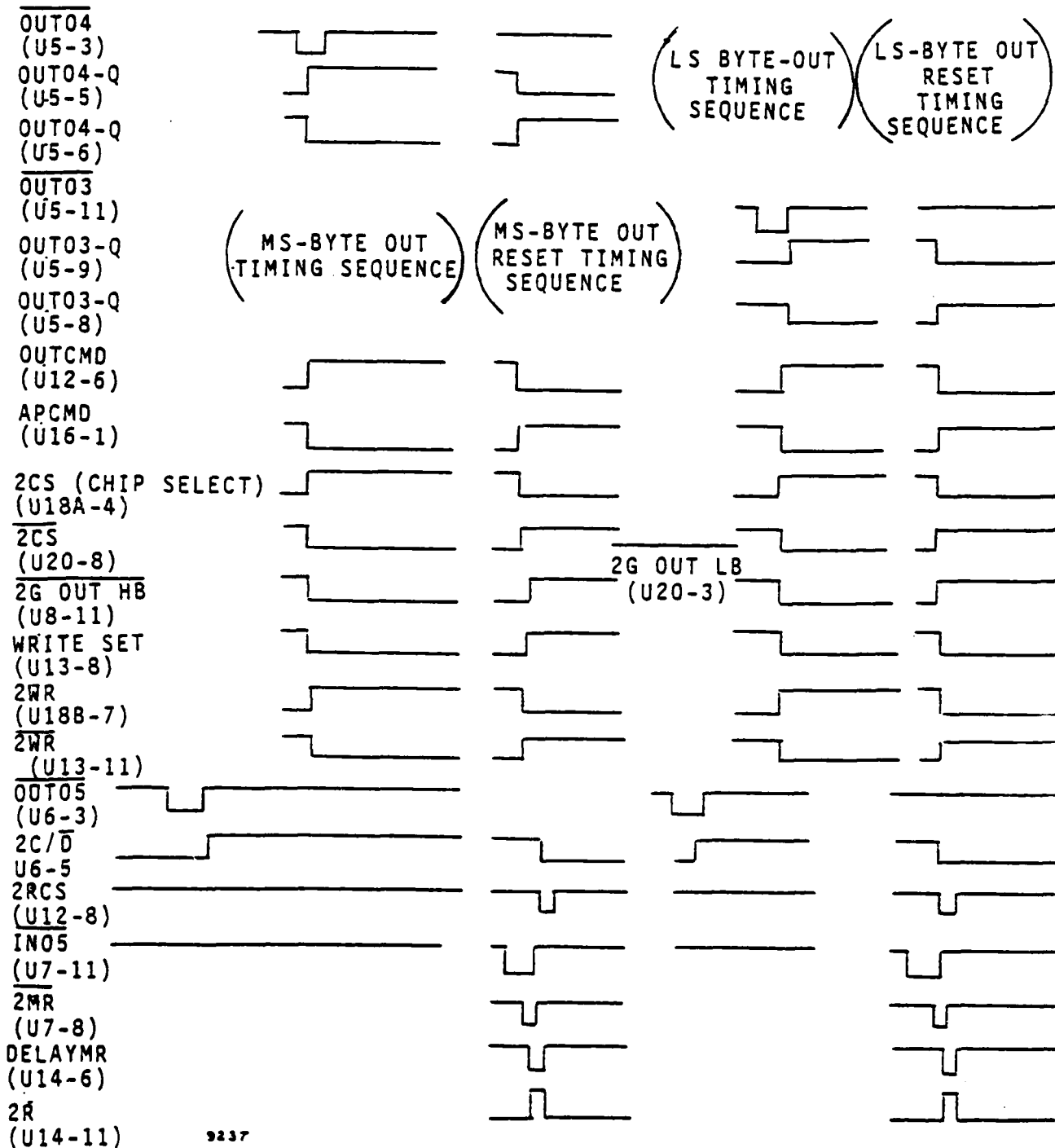


FIGURE 4. TYPICAL OUTPUT TIMING SEQUENCE

3.4.2 Data Transfer From APU Channel

The data transfer timing sequences listed below are shown in Figure 5.

- a. Set Data Transfer Mode to Data or Status
- b. Condition APU for output data transfer
- c. Transfer data
- d. Reset APU channel

The transferring of data from the APU requires the conditioning of 9511-1AP (U30) inputs, i.e., $\overline{CS}$ (PIN 18) low, $\overline{RD}$ (PIN-20) low, $\overline{WR}$ (PIN-19) high and C/D (PIN-21) high for status and low for data.

The selecting of status or data transfer (C/D) is accomplished by setting latch U6-5 high for status or low for data. Latch U6-5 is set low by a channel reset or power up; therefore, during I/O normal sequences latch U6-5 does not require a special I/O command for data request (reset condition). If status is required, the remission of I/O command OUT05 sets latch U6-5 which places a high at U30-21 (9511A-1 status request).

The APU channel is conditioned for transferring data by selecting I/O command IN04 for the high byte or I/O command IN03 for the low byte data. At the completion of the respective input command, the high byte input latch (U6-8) or the low byte input latch (U7-6) goes low by clocking a high into the respective latch. A low at U7-6 or U6-8 causes U13-3 to go high. This high is inverted to a low by U16-1 enabling Nand Gate U8-2 and causing U18A-4 to go high. This high causes U13-8 to go low and set latch U18B-7 to a high. Latch U18C-9 remains low. U18A-4 is inverted to a low by Nand Inverter U13-8. U30 is now conditioned for output data 2CS (U20-8) is low, 2RD (U8-6) is low, 2WR (U13-11) is high and 2C/D (U6-5) is low for data and high for status).

After each read request, Pause goes low until valid U30 data is present. When valid data is available, I/O command IN05 is used to transfer the data. During the active IN05 signal, IN05 is low and inverted to a high by Nand Inverter U8-8 enabling Nand Gates U14-10 and U20-4. If high byte is selected, Nand Gate input U14-9 is high enabling U28 octal buffers and placing U30 data on data bus bits DB08 to DB15. If low byte is selected, Nand Gate input U14-5 is high enabling octal buffers (U26) and placing U30 data on data bus bits DB00 - DB07.

When IN05 terminates and goes high, latch U7-8 is clocked low. This low is inverted to a high by Nand Gate U14-3 and inverted to a high by Nand Inverter U14-6. (Resistor R18 and capacitor C12 provide a pulse stretcher to ensure channel reset.) The low at U14-6 clears latches U7-9 (reset latch), U7-5 (low in latch), U6-9 (high in latch), and U18C-9 (channel 2 read latch). U14-6 is inverted to a high by Nand Gate U14-11 and enables the resetting of the CS latch and the C/D latch (U6-5) once the read latch is reset (inputs to Nand Gate U12-9/10/11 are all high causing the output to go low).

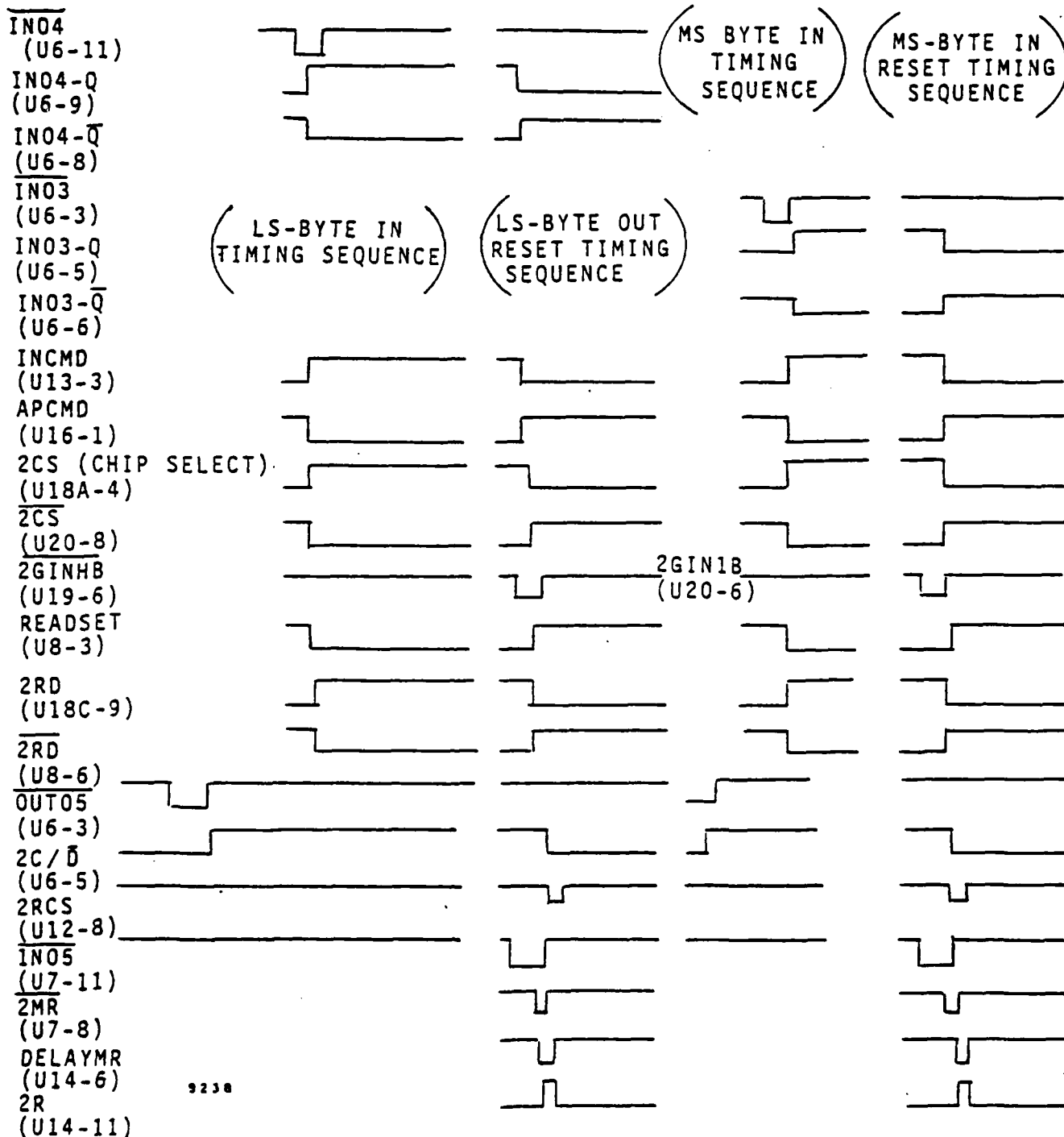


FIGURE 5. TYPICAL INPUT TIMING SEQUENCE

3.4.3 9511-1 AP Reset

The resetting of both APU channels is accomplished by latches U31-5 and U31-9. Since the reset to a 9511A-1 AP must last at least 5 clock cycles, the 500 KHz system clock is used. The reset is initiated by an active MACLR.

The Timing diagram shown in Figure 6 depicts reset timing cycles. The MACLR sets U31-5 to a high enabling latch U31-12. The next 500 KHz clock causes U31-8 to go low and reset latch U31-5 which places a low on the data input of latch U31-12. The high at latch U31-9 is applied to the reset of both 9511-1 chips (U29 and U30). The next clock resets U31-9, completing the cycle after latch U31-9 was high for one 500KHz clock period.

3.4.4 Power Up

Each APU channel is equipped with a power-up reset (R17, CR2, C8 for APU channel 2). When power is applied, a low is placed on Nand Gate input U14-2. This low causes the same channel reset as previously described when reset latch U7-8 goes low.

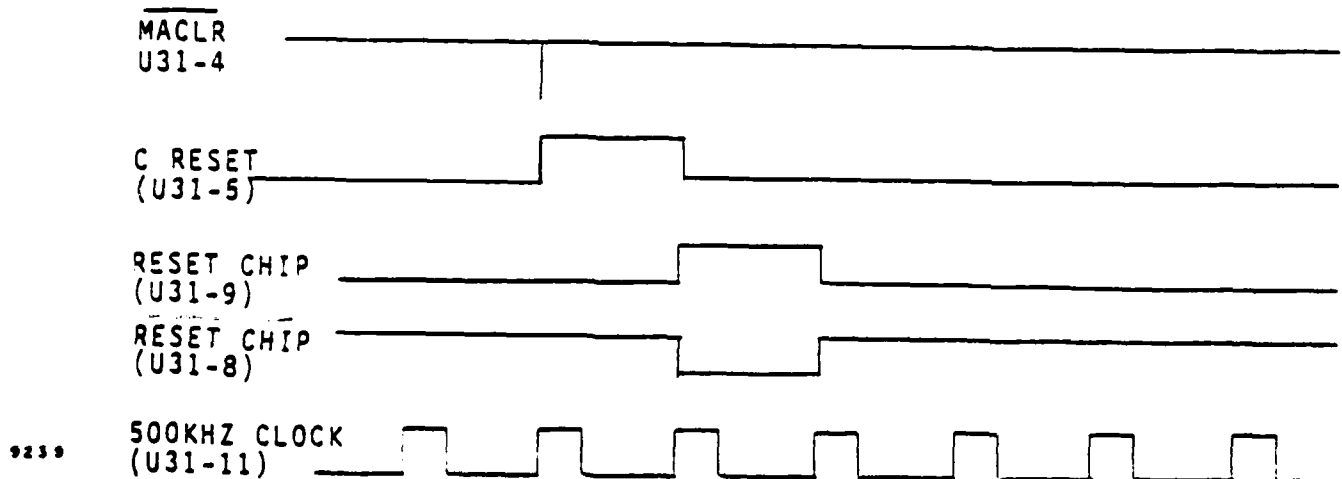


FIGURE 6. ARITHMETIC PROCESSOR CHIP RESET CONTROL

3.4.5 V_{DD} Supply

Each 9511A-1 AP +12 volt V_{DD} source is obtained from +20 volt source through voltage regulator circuits U32 and U33.

4.0 INPUT/OUTPUTS

The APU board has three connectors; signal connectors P1A, P1B and test connector J1. Pinouts are shown in Tables 6 through 8 respectively.

5.0 POWER CHARACTERISTICS

Table 9 (a) delineates the type of device, circuit designators, device types and typical maximum power. Table 9 (b) summarizes the power requirements for the total board.

TABLE 6. P1A PIN CONNECTIONS (APU)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	Ground	28	DB03 Data Bit
2	Ground	29	
3	DB04 Data Bit	30	
4	DB05 Data Bit	31	
5	DB06 Data Bit	32	
6	DB07 Data Bit	33	
7	DB11 Data Bit	34	
8	DB10 Data Bit	35	
9	DB09 Data Bit	36	
10	DB08 Data Bit	37	IN00 I/O Channel 0 in strobe
11	DB15 Data Bit	38	IN01 I/O Channel 1 in strobe
12		39	IN02 I/O Channel 2 in strobe
13		40	IN03 I/O Channel 3 in strobe
14		41	OUT00 I/O Channel 0 out strobe
15		42	OUT02 I/O Channel 2 out strobe
16		43	OUT03 I/O Channel 3 out strobe
17		44	
18	DB14 Data Bit	45	
19		46	
20	DB13 Data Bit	47	OUT04 I/O Channel 4 out strobe
21		48	
22	DB12 Data Bit	49	
23		50	
24		51	
25	DB00 Data Bit	52	+5V
26	DB01 Data Bit	53	+5V
27	DB02 Data Bit	54	

TABLE 7. P1B PIN CONNECTIONS (APU)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	+5V	28	
2	+5V	29	
3		30	
4	3MHZ 3MHZ Clock	31	OUT05 I/O Channel 5 out strobe
5		32	
6		33	
7		34	
8		35	$\overline{\text{MACLR}}$ Machine Clock
9		36	+20 Volts
10		37	
11		38	
12		39	
13	500KHz 500KHz System clock	40	ST05 APU 1 Pause
14	IN04 I/O Channel 4 in strobe	41	
15		42	
16	IN05 I/O Channel 5 in strobe	43	
17		44	
18		45	ST09 APU 2 $\overline{\text{END}}$
19		46	
20		47	ST08 APU 2 Pause
21		48	ST06 APU 1 $\overline{\text{END}}$
22		49	
23		50	
24		51	
25		52	Ground
26	OUT01 I/O Channel 1 out strobe	53	Ground
27		54	

TABLE 8. J1 PIN CONNECTIONS (APU)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1		28	
2		29	
3		30	T1CS Channel 1 chip select
4		31	T1RD Channel 1 APU read
5		32	T1WR Channel 1 APU write
6		33	T2CS Channel 2 chip select
7		34	T2RD Channel 2 APU read
8		35	T2WR Channel 2 APU write
9	T2APU0 APU 2 Data bit 0	36	
10	T2APU1 APU 2 Data bit 1	37	
11	T2APU2 APU 2 Data bit 2	38	
12	T2APU3 APU 2 Data bit 3	39	
13	T2APU4 APU 2 Data bit 4	40	
14	T2APU5 APU 2 Data bit 5	41	T1OUTH Channel 1 out hi-byte
15	T2APU6 APU 2 Data bit 6	42	T1OUTL Channel 1 out low-byte
16	T2APU7 APU 2 Data bit 7	43	T1C/D Channel 1 command/data
17		44	T1INHB Channel 1 in hi-byte
18		45	T1INLB Channel 1 in low-byte
19	T1APU0 APU 1 Data bit 0	46	
20	T1APU1 APU 1 Data bit 1	47	T2OUTH Channel 2 out hi-byte
21	T1APU2 APU 1 Data bit 2	48	T2OUTL Channel 2 out low-byte
22	T1APU3 APU 1 Data bit 3	49	T2C/D Channel 2 command/data
23	T1APU4 APU 1 Data bit 4	50	T2INHB Channel 2 in hi-byte
24	T1APU5 APU 1 Data bit 5	51	T2INLB Channel 2 in low-byte
25	T1APU6 APU 1 Data bit 6	52	
26	T1APU7 APU 1 Data bit 7	53	
27		54	

TABLE 9(a). GENERAL DEVICE POWER CHARACTERISTICS

<u>DEVICE NAME</u>	<u>CIRCUIT DESIGNATORS</u>	<u>DEVICE TYPE</u>	<u>POWER</u>	
			<u>TYPICAL (MA)</u>	<u>MAXIMUM (MA)</u>
Octal Buffer	U22, U24, U26, U28	54LS244	2.6	45
S-R Register	U17-U18	54LS279	3.8	10
APU	U29-U30	AM9511-1	50	100
Octal Latch	U21, U23, U25, U27	54LS374	27	45
Quad Nand	U4, U8, U10-U14, U19, U20	54LS00	1.6	3
3 Input Nand	U9, U12	54LS10	1.2	2.3
Quad Latch	U1-U3, U5-U7, U31	54LS74	4	8
Quad Nor	U15, U16	54LS02	2.4	4.3
Linear Regulator	U32, U33	723	52.3	103

TABLE 9(b). APU BOARD POWER REQUIREMENTS

<u>DEVICE NAME</u>	<u>V_{cc}</u>	<u>QUANTITY</u>	<u>TYPICAL (MW)</u>	<u>MAXIMUM (MW)</u>
Octal Buffer	5	4	520	900
S-R Registers	5	2	38	100
APU	5	2	500	1000
Octal Latch	5	4	540	900
Quad Nand	5	9	72	135
3 Input Nand	5	2	12	23
Quad Latch	5	7	140	280
Quad Nor	5	2	24	21.5
Linear Regulator	20	2	<u>2092</u>	<u>4140</u>
5 volt power			1846	3377.5
20 volt power			<u>2092</u>	<u>4140</u>
Total Power			3938 MW	7517.5 MW

APPENDIX A

Am9511

Arithmetic Processor
Advanced Micro Devices
Advanced MOS/LSI



DISTINCTIVE CHARACTERISTICS

- Fixed point 16 and 32 bit operations
- Floating point 32 bit operations
- Binary data formats
- Add, Subtract, Multiply and Divide
- Trigonometric and inverse trigonometric functions
- Square roots, logarithms, exponentiation
- Float to fixed and fixed to float conversions
- Stack-oriented operand storage
- DMA or programmed I/O data transfers
- End signal simplifies concurrent processing
- General purpose 8-bit data bus interface
- Standard 24 pin package
- +12 volt and +5 volt power supplies
- Advanced N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

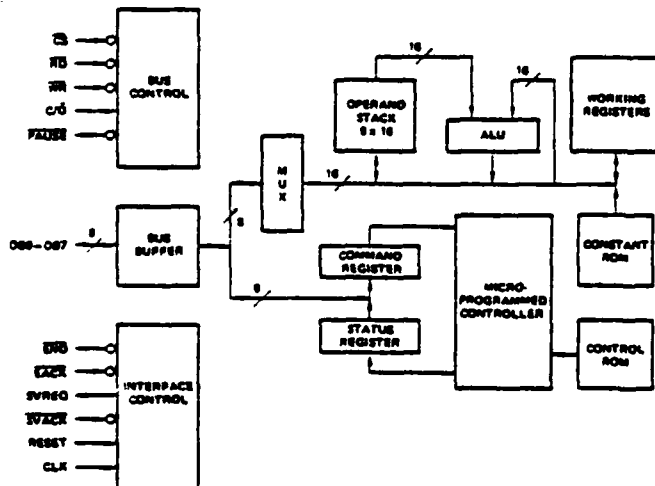
GENERAL DESCRIPTION

The Am9511 Arithmetic Processing Unit (APU) is a monolithic MOS/LSI device that provides high performance fixed and floating point arithmetic and a variety of floating point trigonometric and mathematical operations. It may be used to enhance the computational capability of a wide variety of processor-oriented systems.

All transfers, including operand, result, status and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end of execution signal that may be used as an interrupt by the CPU to help coordinate program execution.

BLOCK DIAGRAM



INTERFACE SIGNAL DESCRIPTION

VCC: +5 Volt power supply

VDD: +12 Volt power supply

VSS: Ground

CLK (Clock, Input)

An external timing source should be applied to the CLK pin. The Clock input may be asynchronous to the Read and Write control signals.

RESET (Reset, Input)

The active high Reset signal provides initialization for the chip. Reset terminates any operation in progress, clears the status register and places the Am9511 into the idle state. Stack contents are not affected by Reset. The Reset should be active for at least 5 clock periods following stable supply voltages and stable clock input. There is no internal power-on reset.

$\overline{CS}$ (Chip Select, Input)

$\overline{CS}$ is an active low input signal which conditions the read and write signals and thus enables communication with the data bus.

C/D (Command/Data, Input)

In conjunction with the $\overline{RD}$ and $\overline{WR}$ signals, the C/D control line establishes the type of transfers that are to be performed on the data bus.

C/D	$\overline{RD}$	$\overline{WR}$	Function
0	1	0	Enter data byte into stack
0	0	1	Read data byte from stack
1	1	0	Enter command
1	0	1	Read status

$\overline{RD}$ (Read, Input)

The active low Read signal is conditioned by $\overline{CS}$ and indicates that information is to be transferred from internal locations to the data bus. $\overline{RD}$ and $\overline{WR}$ are mutually exclusive.

$\overline{WR}$ (Write, Input)

The active low Write signal is conditioned by $\overline{CS}$ and indicates that information is to be transferred from the data bus into internal locations. $\overline{RD}$ and $\overline{WR}$ are mutually exclusive.

$\overline{EACK}$ (End Acknowledge, Input)

This active low input clears the end of execution output signal ($\overline{END}$). If $\overline{EACK}$ is tied low, the $\overline{END}$ output will be a pulse that is less than one clock period wide.

SVACK (Service Acknowledge, Input)

This active low input clears the service request output (SVREQ).

$\overline{END}$ (End Execution, Output)

This active low, open-drain output indicates that execution of the previously entered command is complete. It can be used as an interrupt request and is cleared by $\overline{EACK}$, RESET or any read or write access to the Am9511.

SVREQ (Service Request, Output)

This active high output signal indicates that command execution is complete and that post execution service was requested in the previous command byte. It is cleared by SVACK, by RESET, or by the end of a subsequent command that does not request service.

PAUSE (Pause, Output)

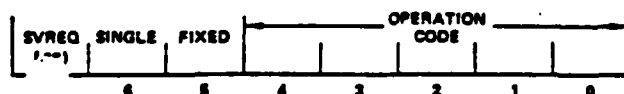
This active low output indicates that the Am9511 has not yet completed its information transfer with the host (or DMA) over the data bus. Whenever a data read or a status read operation is requested, PAUSE goes low. It returns high only after the data bus contains valid output data. When an existing command is still in the process of execution, and a data write, data read, or command write is requested, then PAUSE goes low for the remaining duration of the existing command plus any time needed for initiating a data read. In both cases, the host should neither change any information to the Am9511, nor (in the case of data read or status read) attempt to capture data from the Am9511 DB outputs until PAUSE has returned high. (See "Pause Operation" section on page 5).

DB0-DB7 (Bidirectional Data Bus, I/O)

These eight bidirectional lines provide for transfer of commands, status and data between the Am9511 and the CPU. The Am9511 will drive the data bus only when $\overline{CS}$ and $\overline{RD}$ are low.

COMMAND STRUCTURE

Each command entered into the Am9511 consists of a single 8-bit byte having the format illustrated below:



Bits 0-4 select the operation to be performed as shown in the table. Bits 5-6 select the data format for the operation. If bit 5 is a 1, a fixed point data format is specified. If bit 5 is a 0, floating point format is specified. Bit 6 selects the precision of

the data to be operated on by fixed point commands (if bit 5 = 0, bit 6 must be 0). If bit 6 is a 1, single-precision (16-bit) operands are indicated; if bit 6 is a 0, double-precision (32-bit) operands are indicated. Results are undefined for all illegal combinations of bits in the command byte. Bit 7 indicates whether a service request is to be issued after the command is executed. If bit 7 is a 1, the service request output (SVREQ) will go high at the conclusion of the command and will remain high until reset by a low level on the service acknowledge pin (SVACK) or until completion of execution of a succeeding command where bit 7 is 0. Each command issued to the Am9511 requests post execution service based upon the state of bit 7 in the command byte. When bit 7 is a 0, SVREQ remains low.

COMMAND SUMMARY

Command Code								Command Mnemonic	Command Description
7	6	5	4	3	2	1	0		
FIXED POINT 16 BIT									
sr	1	1	0	1	1	0	0	SADD	Add TOS to NOS. Result to NOS. Pop Stack.
sr	1	1	0	1	1	0	1	SSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
sr	1	1	0	1	1	1	0	SMUL	Multiply NOS by TOS. Lower half of result to NOS. Pop Stack.
sr	1	1	1	0	1	1	0	SMUU	Multiply NOS by TOS. Upper half of result to NOS. Pop Stack.
sr	1	1	0	1	1	1	1	SDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
FIXED POINT 32 BIT									
sr	0	1	0	1	1	0	0	DADD	Add TOS to NOS. Result to NOS. Pop Stack.
sr	0	1	0	1	1	0	1	DSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
sr	0	1	0	1	1	1	0	DMUL	Multiply NOS by TOS. Lower half of result to NOS. Pop Stack.
sr	0	1	1	0	1	1	0	DMUU	Multiply NOS by TOS. Upper half of result to NOS. Pop Stack.
sr	0	1	0	1	1	1	1	DDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
FLOATING POINT 32 BIT									
sr	0	0	1	0	0	0	0	FADD	Add TOS to NOS. Result to NOS. Pop Stack.
sr	0	0	1	0	0	0	1	FSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
sr	0	0	1	0	0	1	0	FMUL	Multiply NOS by TOS. Result to NOS. Pop Stack.
sr	0	0	1	0	0	1	1	FDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
DERIVED FLOATING POINT FUNCTIONS									
sr	0	0	0	0	0	0	1	SQRT	Square Root of TOS. Result in TOS.
sr	0	0	0	0	0	1	0	SIN	Sine of TOS. Result in TOS.
sr	0	0	0	0	0	1	1	COS	Cosine of TOS. Result in TOS.
sr	0	0	0	0	1	0	0	TAN	Tangent of TOS. Result in TOS.
sr	0	0	0	0	1	0	1	ASIN	Inverse Sine of TOS. Result in TOS.
sr	0	0	0	0	1	1	0	ACOS	Inverse Cosine of TOS. Result in TOS.
sr	0	0	0	0	1	1	1	ATAN	Inverse Tangent of TOS. Result in TOS.
sr	0	0	0	1	0	0	0	LOG	Common Logarithm (base 10) of TOS. Result in TOS.
sr	0	0	0	1	0	0	1	LN	Natural Logarithm (base e) of TOS. Result in TOS.
sr	0	0	0	1	0	1	0	EXP	Exponential (e ^x) of TOS. Result in TOS.
sr	0	0	0	1	0	1	1	PWR	NOS raised to the power in TOS. Result in NOS. Pop Stack.
DATA MANIPULATION COMMANDS									
sr	0	0	0	0	0	0	0	NOP	No Operation
sr	0	0	1	1	1	1	1	FIXS	Convert TOS from floating point to 16-bit fixed point format.
sr	0	0	1	1	1	1	0	FIXD	Convert TOS from floating point to 32-bit fixed point format.
sr	0	0	1	1	1	0	1	FLTS	Convert TOS from 16-bit fixed point to floating point format.
sr	0	0	1	1	1	0	0	FLTD	Convert TOS from 32-bit fixed point to floating point format.
sr	1	1	1	0	1	0	0	CHSS	Change sign of 16-bit fixed point operand on TOS.
sr	0	1	1	0	1	0	0	CHSD	Change sign of 32-bit fixed point operand on TOS.
sr	0	0	1	0	1	0	1	CHSF	Change sign of floating point operand on TOS.
sr	1	1	1	0	1	1	1	PTOS	Push 16-bit fixed point operand on TOS to NOS. (Copy)
sr	0	1	1	0	1	1	1	PTOD	Push 32-bit fixed point operand on TOS to NOS. (Copy)
sr	0	0	1	0	1	1	1	PTOF	Push floating point operand on TOS to NOS. (Copy)
sr	1	1	1	1	0	0	0	POPS	Pop 16-bit fixed point operand from TOS. NOS becomes TOS.
sr	0	1	1	1	0	0	0	POPD	Pop 32-bit fixed point operand from TOS. NOS becomes TOS.
sr	0	0	1	1	0	0	0	POPF	Pop floating point operand from TOS. NOS becomes TOS.
sr	1	1	1	1	0	0	1	XCHS	Exchange 16-bit fixed point operands TOS and NOS.
sr	0	1	1	1	0	0	1	XCHD	Exchange 32-bit fixed point operands TOS and NOS.
sr	0	0	1	1	0	0	1	XCHF	Exchange floating point operands TOS and NOS.
sr	0	0	1	1	0	1	0	PUPI	Push floating point constant "π" onto TOS. Previous TOS becomes NOS.

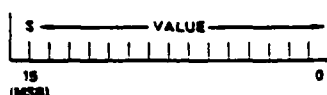
NOTES:

1. TOS means Top of Stack. NOS means Next on Stack.
2. AMD Application Brief "Algorithm Details for the Am9511 APU" provides detailed descriptions of each command function, including data ranges, accuracies, stack configurations, etc.
3. Many commands destroy one stack location (bottom of stack) during development of the result. The derived functions may destroy several stack locations. See Application Brief for details.
4. The trigonometric functions handle angles in radians, not degrees.
5. No remainder is available for the fixed-point divide functions.
6. Results will be undefined for any combination of command coding bits not specified in this table.

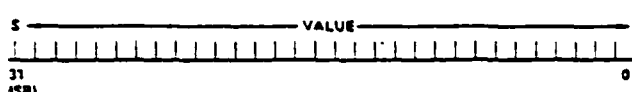
ATA FORMATS

The Am9511 Arithmetic Processing Unit handles operands in both fixed point and floating point formats. Fixed point operands may be represented in either single (16-bit operands) or double precision (32-bit operands), and are always represented as binary, two's complement values.

16-BIT FIXED POINT FORMAT



32-BIT FIXED POINT FORMAT



The sign (positive or negative) of the operand is located in the most significant bit (MSB). Positive values are represented by a sign bit of zero ($S = 0$). Negative values are represented by the two's complement of the corresponding positive value with a sign bit equal to 1 ($S = 1$). The range of values that may be accommodated by each of these formats is $-32,768$ to $-32,767$ for single precision and $-2,147,483,648$ to $-2,147,483,647$ for double precision.

Floating point binary values are represented in a format that allows arithmetic to be performed in a fashion analogous to operations with decimal values expressed in scientific notation.

$$(5.83 \times 10^2)(8.16 \times 10^1) = (4.75728 \times 10^4)$$

In the decimal system, data may be expressed as values between 0 and 10 times 10 raised to a power that effectively shifts the implied decimal point right or left the number of places necessary to express the result in conventional form (e.g., 47,572.8). The value-portion of the data is called the mantissa. The exponent may be either negative or positive.

The concept of floating point notation has both a gain and a loss associated with it. The gain is the ability to represent the significant digits of data with values spanning a large dynamic range limited only by the capacity of the exponent field. For

example, in decimal notation if the exponent field is two digits wide, and the mantissa is five digits, a range of values (positive or negative) from 1.0000×10^{-99} to 9.9999×10^{-99} can be accommodated. The loss is that only the significant digits of the value can be represented. Thus there is no distinction in this representation between the values 123451 and 123452, for example, since each would be expressed as: 1.2345×10^5 . The sixth digit has been discarded. In most applications where the dynamic range of values to be represented is large, the loss of significance, and hence accuracy of results, is a minor consideration. For greater precision a fixed point format could be chosen, although with a loss of potential dynamic range.

The Am9511 is a binary arithmetic processor and requires that floating point data be represented by a fractional mantissa value between .5 and 1 multiplied by 2 raised to an appropriate power. This is expressed as follows:

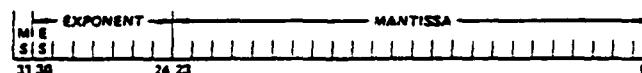
$$\text{value} = \text{mantissa} \times 2^{\text{exponent}}$$

For example, the value 100.5 expressed in this form is 0.11001001×2^7 . The decimal equivalent of this value may be computed by summing the components (powers of two) of the mantissa and then multiplying by the exponent as shown below:

$$\begin{aligned} \text{value} &= (2^{-1} + 2^{-2} + 2^{-5} + 2^{-8}) \times 2^7 \\ &= (0.5 + 0.25 + 0.03125 + 0.00290625) \times 128 \\ &= 0.78515625 \times 128 \\ &= 100.5 \end{aligned}$$

FLOATING POINT FORMAT

The format for floating point values in the Am9511 is given below. The mantissa is expressed as a 24-bit (fractional) value; the exponent is expressed as an unbiased two's complement 7-bit value having a range of -64 to $+63$. The most significant bit is the sign of the mantissa (0 = positive, 1 = negative), for a total of 32 bits. The binary point is assumed to be to the left of the most significant mantissa bit (bit 23). All floating point data values must be normalized. Bit 23 must be equal to 1, except for the value zero, which is represented by all zeros.

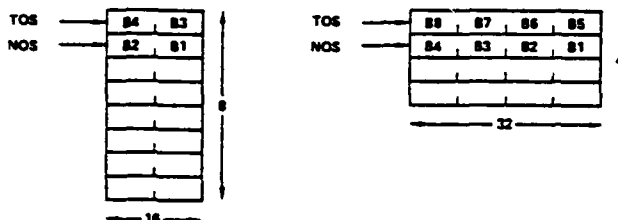


The range of values that can be represented in this format is $\pm(2.7 \times 10^{-20}$ to $9.2 \times 10^{18})$ and zero.

FUNCTIONAL DESCRIPTION

Stack Control

The user interface to the Am9511 includes access to an 8 level 16-bit wide data stack. Since single precision fixed point operands are 16 bits in length, eight such values may be maintained in the stack. When using double precision fixed point or floating point formats four values may be stored. The stack in these two configurations can be visualized as shown below:



Data are written onto the stack, eight bits at a time, in the order shown (B1, B2, B3, ...). Data are removed from the stack in reverse byte order (B8, B7, B6, ...). Data should be transferred into or out of the stack in multiples of the number of bytes appropriate to the chosen data format.

Data Entry

Data entry is accomplished by bringing the chip select ($\overline{CS}$), the command/data line ($C/\overline{D}$), and $\overline{WR}$ low, as shown in the timing diagram. The entry of each new data word "pushes down" the previously entered data and places the new byte on the top of stack (TOS). Data on the bottom of the stack prior to a stack entry are lost.

Data Removal

Data are removed from the stack in the Am9511 by bringing chip select ($\overline{CS}$), command/data ($C/\overline{D}$), and $\overline{RD}$ low as shown in the timing diagram. The removal of each data word redefines TOS so that the next successive byte to be removed becomes TOS. Data removed from the stack rotates to the bottom of the stack.

Command Entry

After the appropriate number of bytes of data have been entered onto the stack, a command may be issued to perform an operation on that data. Commands which require two operands for execution (e.g., add) operate on the TOS and NOS values. Single operand commands operate only on the TOS.

Commands are issued to the Am9511 by bringing the chip select ($\overline{CS}$) line low, command/data ($C/\overline{D}$) line high, and $\overline{WR}$ line low as indicated by the timing diagram. After a command is issued, the CPU can continue execution of its program concurrently with the Am9511 command execution.

Command Completion

The Am9511 signals the completion of each command execution by lowering the End Execution line ($\overline{END}$). Simultaneously, the busy bit in the status register is cleared and the Service Request bit of the command register is checked. If it is a "1" the service request output level (SVREQ) is raised. $\overline{END}$ is cleared on receipt of an active low End Acknowledge ($\overline{ACK}$) pulse. Similarly, the service request line is cleared by recognition of an active low Service Acknowledge ($\overline{SVACK}$) pulse.

Pause Operation

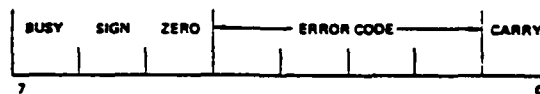
An active low Pause ($\overline{PAUSE}$) is provided. This line is high in its quiescent state and is pulled low by the Am9511 under the following conditions:

1. A previously initiated operation is in progress (device busy) and Command Entry has been attempted. In this case, the $\overline{PAUSE}$ line will be pulled low and remain low until completion of the current command execution. It will then go high, permitting entry of the new command.
2. A previously initiated operation is in progress and stack access has been attempted. In this case, the $\overline{PAUSE}$ line will be pulled low, will remain in that state until execution is complete, and will then be raised to permit completion of the stack access.
3. The Am9511 is not busy, and data removal has been requested. $\overline{PAUSE}$ will be pulled low for the length of time necessary to transfer the byte from the top of stack to the interface latch, and will then go high, indicating availability of the data.
4. The Am9511 is not busy, and a data entry has been requested. $\overline{PAUSE}$ will be pulled low for the length of time required to ascertain if the preceding data byte, if any has been written to the stack. If so $\overline{PAUSE}$ will immediately go high. If not, $\overline{PAUSE}$ will remain low until the interface latch is free and will then go high.
5. When a status read has been requested, $\overline{PAUSE}$ will be pulled low for the length of time necessary to transfer the status to the interface latch, and will then be raised to permit completion of the status read. Status may be read whether or not the Am9511 is busy.

When $\overline{PAUSE}$ goes low, the APU expects the bus and bus control signals present at the time to remain stable until $\overline{PAUSE}$ goes high.

Device Status

Device status is provided by means of an internal status register whose format is shown below:



BUSY: Indicates that Am9511 is currently executing a command (1 = Busy).

SIGN: Indicates that the value on the top of stack is negative (1 = Negative).

ZERO: Indicates that the value on the top of stack is zero (1 = Value is zero).

ERROR CODE: This field contains an indication of the validity of the result of the last operation. The error codes are:

- 0000 - No error
- 1000 - Divide by zero
- 0100 - Square root or log of negative number
- 1100 - Argument of inverse sine, cosine, or e^x too large
- XX10 - Underflow
- XX01 - Overflow

CARRY: Previous operation resulted in carry or borrow from most significant bit. (1 = Carry/Borrow, 0 = No Carry/No Borrow)

If the BUSY bit in the status register is a one, the other status bits are not defined; if zero, indicating not busy, the operation is complete and the other status bits are defined as given above.

Read Status

The Am9511 status register can be read by the CPU at any time (whether an operation is in progress or not) by bringing the chip select ($\overline{CS}$) low, the command-data line ($C/\overline{D}$) high, and lowering $\overline{RD}$. The status register is then gated onto the data bus and may be input by the CPU.

EXECUTION TIMES

Timing for execution of the Am9511 command set is shown in the table below. Speeds are given in terms of clock cycles and should be multiplied by the clock period being used to arrive at time values. Where substantial variation of execution time is possible, the minimum and maximum values are shown; otherwise, typical values are given. Variations are data dependent. Some boundary conditions that will cause shorter execution times are not taken into account. The listing is in alphabetical order of mnemonic.

Total execution times may require allowances for operand transfer into the APU, command execution, and result retrieval from the APU. Except for command execution, these times will be heavily influenced by the nature of the data, the control interface used, the speed of memory, the CPU used, the priority allotted to DMA and Interrupt operations, the size and number of operands to be transferred, and the use of chained calculations, etc.

COMMAND EXECUTION TIMES

Command Mnemonic	Clock Cycles	Command Mnemonic	Clock Cycles
ACOS	6304-8284	LOG	4474-7132
ASIN	6230-7938	LN	4298-6956
ATAN	4992-6536	NOP	4
CHSD	26-28	POPD	12
CHSF	16-20	POPF	12
CHSS	22-24	POPS	10
COS	3840-4878	PTOD	20
DADD	20-22	PTOF	20
DDIV	196-210	PTOS	16
DMUL	194-210	PUP1	16
DMUU	182-218	PWR	8290-12032
DSUB	38-40	SADD	16-18
EXP	3794-4878	SDIV	84-94
FADD	54-368	SIN	3796-4808
FDIV	154-184	SMUL	84-94
FIXD	90-336	SMUU	80-98
FIXS	90-214	SORT	782-870
FLTD	56-342	SSUB	30-32
FLTS	62-156	TAN	4894-5886
FMUL	146-168	XCHD	26
FSUB	70-370	XCHF	26
		XCHS	18

As mentioned, the above clock cycle execution times can be converted to μsec by multiplying by the clock period used. Several examples (minimums) are shown below:

Command Description	Am9511 (2MHz)	Am9511-1 (3MHz)
32-Bit Floating-Point Cosine (COS)	1920 μsec	1280 μsec
32-Bit Floating-Point e^x (EXP)	1897 μsec	1265 μsec
32-Bit Floating Point Multiply (FMUL)	73 μsec	49 μsec
16-Bit Fixed-Point Multiply, Lower (SMUL)	42 μsec	28 μsec
32-Bit Floating-Point Add (FADD)	27 μsec	18 μsec
16-Bit Fixed-Point Add (SADD)	8 μsec	5 μsec

OUTPUT INTERFACE TECHNICAL DESCRIPTION

APPENDIX G

OUTPUT INTERFACE MODULE

1.0 INTRODUCTION

The Output Interface Board was developed to satisfy the following requirements:

- a. An effective 16-bit serial interface
- b. the capturing of 5 bits and parity of parallel data
- c. the development of 7 precision reference voltages

The serial interface provides for 16 bits of parallel data to be converted to serial data and subsequently transmitted by a differential line driver. Alternatively, serial data received by differential line receivers is converted to 16 bits of parallel data. BIT is provided to test transceiver capability.

A parallel 16-bit interface is provided on the Output Interface Board for placing data on the data bus under positive control.

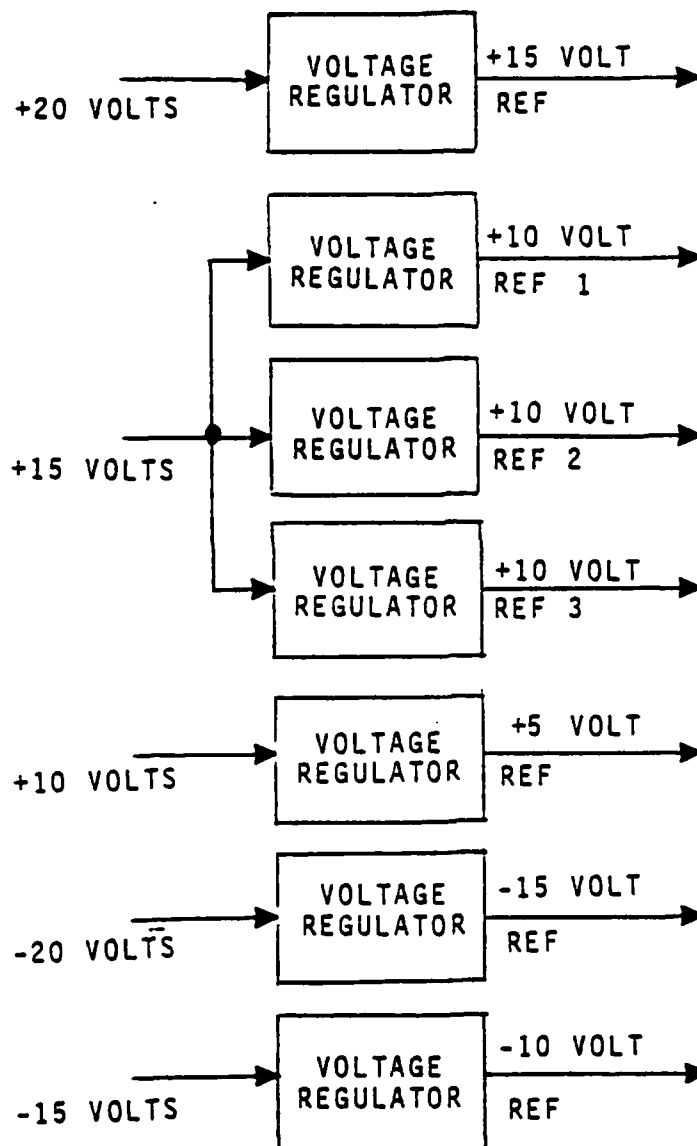
The Output Interface Board contains 7 regulators for obtaining precise reference voltages. Regulator source inputs and output voltages are shown in Table 1.

2.0 OUTPUT INTERFACE BOARD KEY FEATURES

- a. Provision for obtaining 7 reference voltages
- b. 16-bit parallel/serial and 16-bit serial/parallel conversion
- c. BIT of each UART channel
- d. Differential line transceivers for serial data
- e. Test points are provided for critical signals
- f. Transmitter and receiver status indicators
- g. Full Duplex operation is provided

3.0 FUNCTIONAL DESCRIPTION

A block diagram of the voltage regulation circuits provided by the Output Interface Board is shown in Figure 1 with source voltage and associated regulated output voltage shown in Table 1.



9230

FIGURE 1. VOLTAGE REGULATOR BLOCK DIAGRAM

TABLE 1. REGULATED VOLTAGE SOURCE AND REFERENCE

<u>Source Voltage</u>	<u>Output Reference Voltage</u>
+20 Volts	+15 Volts
+10 Volts	+ 5 Volts
-20 Volts	-15 Volts
-15 Volts	-10 Volts
+15 Volts	+10 Volts
+15 Volts	+10 Volts
+15 Volts	+10 Volts

The functional block diagram of parallel-serial interface is shown in Figure 2. The circuit is comprised of 2 8-bit UART channels working in synchronism to provide an effective 16-bit serial word transfer. When a transmit data is required, the data transmitter buffer signal of each UART (DTBRE1 and DTBRE2) is used to determine when another 16-bit word can be transferred. Both transmitters must be empty before data is transferred to the UARTs. Data is loaded into the UART by an OUT10 I/O command. The 8 bits of parallel data is converted to serial data, (1 start bit, 1 stop bit, 1 parity bit and 8 data bits) and transmitted by the output line drivers if BIT has not been selected.

When serial data is received from the line receivers, the serial data is converted to 8-bits of parallel data in each UART. The data ready (DE1 and DE2) indicates when an 8-bit word is in the receiver buffer. When the serial input data has been received by both UARTS the word can be transferred to the data bus via the input buffers. The gating of the data ready signals in the receiver synchronizer provides an indication when a 16-bit word can be transferred.

The BIT selector provides a method for testing each UART. This is accomplished by connecting the serial receive data UART input to the transmit output of the UART. In this position, transmit data sent to each UART can be converted to serial data, recovered to parallel data and transmitted back to the data bus.

A parallel buffer is provided for transferring 8 bits of parallel data to the lowest eight bits of the data bus whenever an IN07 I/O command is selected.

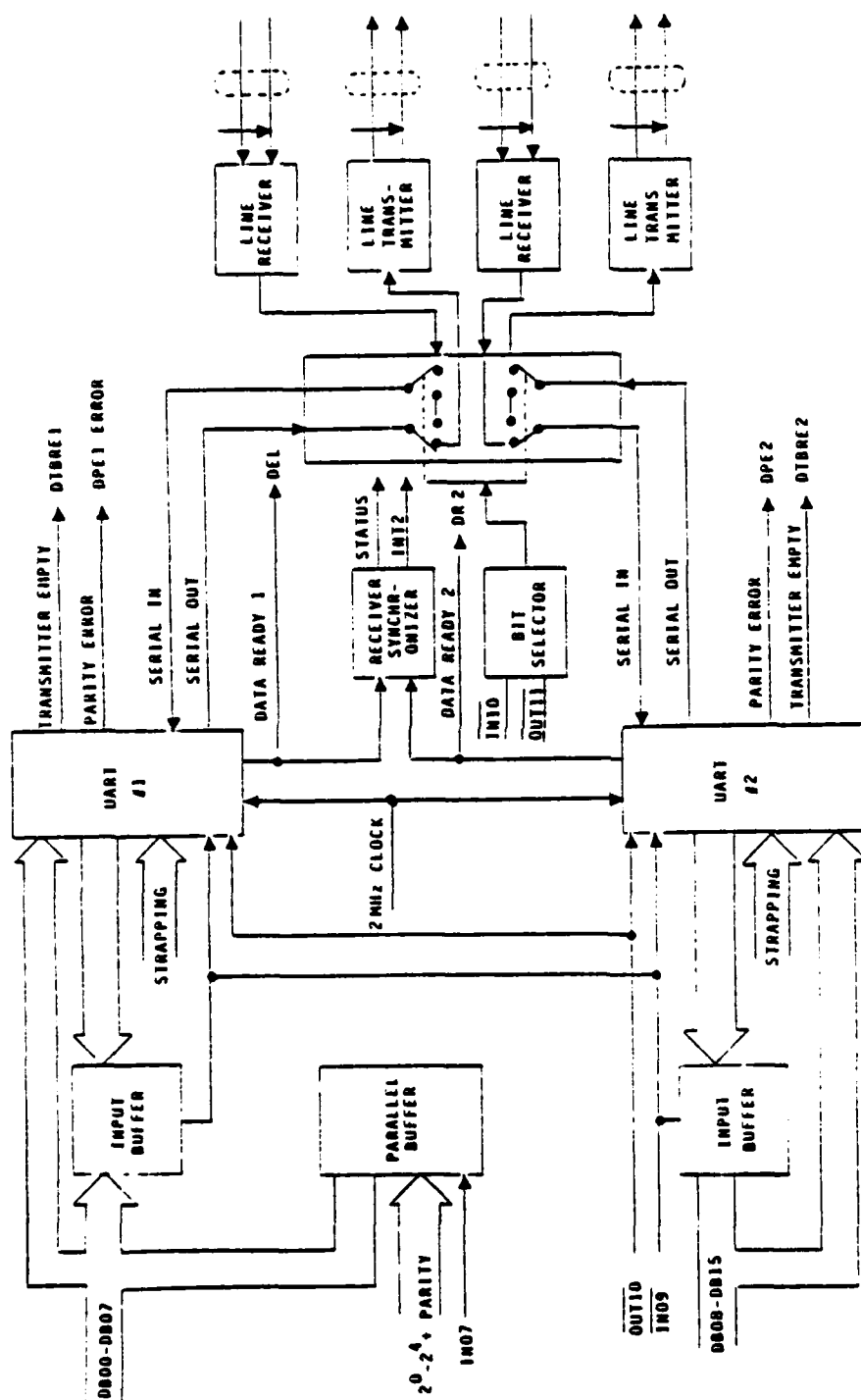


FIGURE 2. BLOCK DIAGRAM COMMUNICATION INTERFACE

3.1 Detailed Theory of Operation

3.1.1 Voltage Reference Circuits

The seven reference voltages (Table 1) are derived from positive voltage linear regulator circuits (U10, U11, U15, U16 and U17) and negative voltage regulator circuits (U12 and U13).

For positive regulator and negative voltage regulator detailed information, refer to Appendices A and B respectively.

The input source voltage of each regulator is as shown in Table 1. Each regulator also uses a 100 pf capacitor for frequency compensation.

- 3.1.1.1 Positive Low Voltage Regulation (2 volts to 7 volts). The +5v reference (U11) is obtained from the +10 volt source voltage. Resistors R54, R55, R56 and R58 provided the bias network for establishing the +5 volt reference. Equations 1 and 2 are used:

Equation 1:

$$V_{out} = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

Equation 2:

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

Where: $R_1 = R_{54} (10 \text{ K}\Omega)$

$$R_2 = \frac{R_{55} R_{56}}{R_{55} + R_{56}} \quad (<30.9 \text{ K}\Omega, \text{ since } R_{56} = 30.9 \text{ K}\Omega)$$

$$R_3 = R_{58} (6.8 \text{ K}\Omega)$$

$$V_{ref} = 7.15 \text{ volts}$$

$$V_{out} = 7.15 \text{ volts} \times \frac{30.9 \text{ K}\Omega}{30.9 \text{ K}\Omega + 10 \text{ K}\Omega} = 5.4 \text{ volts}$$

(Due to variation in V_{ref} , R55 is a selected in test (SIT) resistor for improving the accuracy of the output reference voltage.)

Current limiting is established through resistor R57, see Equation 3.

Equation 3:

$$I_{limit} \approx \frac{V_{sense}}{R_{SC}}$$

Where: $R_{SC} = R_{57} = 9.1\Omega$ and $V_{sense} = 0.65 \text{ volts}$,

$$I_{limit} \approx 71.5 \text{ ma.}$$

- 3.1.1.2 Positive High Voltage Regulators (7 volts to 37 volts). The regulated voltage is obtained through use of Equations 1, 2 and 3. Table 2 contains a cross reference of components, source and output voltages, circuit designators and current limiting value. A SIT resistor is used in each regulator to obtain the accurate output voltage.
- 3.1.1.3 Negative Voltage Regulators. The two negative voltage regulators (U12 and U13) establish output voltages in accordance with Equation 4.

Equation 4:

$$V_o = V_{ref} \left(\frac{R_B + R_A}{R_B} \right)$$

Where: $V_o = -15$ volts for U12 and $-10v$ for U13

$V_{ref} \approx -3.5$ volts

$R_A = 30.9 \text{ K}\Omega$ (R62 for U12 and R67 for U13)

$R_B = 10 \text{ K}\Omega$ (R60 for U12) and $20 \text{ K}\Omega$ (R65 for U13)

(SIT is trim for R_B - R61 for U12 and R66 for U13)

Resistor R59 (20Ω) limits the current of the -15 volt regulator (U12) to 80 MA. Resistor R64 (51Ω) limits the current of the -10 volt regulator (U13) to 30 MA.

3.2 Serial Interface

Two Universal Asynchronous Receiver Transmitter Circuits (UARTs) operating in tandem provide the bases of the serial interfaces. The remaining circuits provide for control, data routing, BIT and line transceiver capability. The UARTs employed are HD-6402-9 circuits. Detailed specifications of these circuits can be found in Appendix C. UART interface signal definitions are given in Table 3.

Control signals CLS1, CLS2, PI, EPE, and SBS select the character format. The format used which consists of 1 start and 1 stop bit, 8 data bits and odd parity is obtained by strapping CLS1 and CLS2 high and strapping PI, EPE and SBS low. Continual parity checking is provided by strapping PI low. Status flags are continually enabled since SFD is tied low. The strapping options are continually monitored by the UART by CRL being tied high.

The serial data rate is set at $1/16$ the data clock or $2\text{MHz}/16 = 125 \text{ KHz}$.

TABLE 2. HIGH VOLTAGE REGULATOR CHARACTERISTICS

Voltage Regulator Reference	Current Limit (mA)	Input Voltage (Volts)	Output Voltage (Volts)	Circuit Designator				
				R1 (K Ω)	R2 (K Ω)	R3 (K Ω)	Rtrim (K Ω)	RSC (K Ω)
U10		20 volts	15 volts	R51(10)	R2(10)	R49(4.7)	R53(SIT)	R50(9)
U15	32.5	15 volts	10 volts	R71(10)	R72(30.9)	R69(7.5)	R73(SIT)	R70(20)
U16	50.0	15 volts	10 volts	R76(10)	R77(30.9)	R74(7.5)	R75(SIT)	R75(13)
U17	50.1	15 volts	10 volts	R81(10)	R82(30.9)	R79(7.5)	R83(SIT)	R80(11)

TABLE 3. UART INTERFACE DEFINITION

Signal	Pin	Function
Ncc	1	Chip voltage
Ground	3	Chip ground
TBR1	26	Transmitter input buffer bit 20
TBR2	27	Transmitter input buffer bit 21
TBR3	28	Transmitter input buffer bit 22
TBR4	29	Transmitter input buffer bit 23
TBR5	30	Transmitter input buffer bit 24
TBR6	31	Transmitter input buffer bit 25
TBR7	32	Transmitter input buffer bit 26
TBR8	33	Transmitter input buffer bit 27
TBRE	22	Transmitter buffer empty
TBRL	23	Transmitter buffer load
TRO	25	Transmitter serial output
RBR1	12	Receiver buffer output 20
RBR2	11	Receiver buffer output 21
RBR3	10	Receiver buffer output 22
RBR4	9	Receiver buffer output 23
RBR5	8	Receiver buffer output 24
RBR6	7	Receiver buffer output 25
RBR7	6	Receiver buffer output 26
RBR8	5	Receiver buffer output 27
DRR	18	Data buffer full clear
DR	19	Data receiver buffer full
RRI	20	Serial input data
PE	13	Parity error in received byte
RRD	4	Recover buffer output enable
CLS2	38	Character select length 2
CLS1	37	Character select length 1
PI	35	Parity checking inhibit
EPE	39	Even parity enable
SBS	36	Stop bit select
SFD	34	Status flags disable
CRL	16	Control register load
MR	21	Master reset
RRC	17	Receiver register clock = 16 x receiver data rate
TRC	40	Transmitter register clock = 16 x transmit data rate

3.3 Output Sequence

The transmitter buffer register empty status of each UART (U2-22 and U8-22) is monitored and if found empty, 16 bits of data is placed on the data lines (DB00-DB15). An OUTIO I/O command causes the data DB00 -DB15 to be loaded into the UART transmitter buffer register. The data in the UART transmit buffer register is converted to serial data in accordance with the control format selection. The UART transmit buffer register empty signal goes low until the data is removed from the UART transmit buffer register and placed in the UART transmit register which provides for a one word storage.

The UART output serial data (U2-25 and U8-25) is connected to distribution switch U5. If the BIT mode is not selected, the serial data is transferred to the output line drivers (U3-5 and U3-11). If the BIT mode is selected, U2 transmit serial data U2-25 is connected to U2 receive serial data (U2-20) and U8 transmit serial data (U8-25) is connected to U2 receive serial data via switch U5. The truth table for switch U5 is given in Table 4.

The output line drivers (U3) is a differential non-inverting circuit. Device specifics are given in Appendix D.

TABLE 4. UARTS DISTRIBUTION SWITCH TRUTH TABLE

SIGNAL	INPUT	CONNECTION	CONTROL	FUNCTION
Transmit Out (U2)	2A1	2Y1 (U3-5 line driver)	H	Normal
Transmit Out (U2)	1A1	1Y1 (U2 receiver in)	L	BIT
Transmit Out (U8)	1A2	1Y2 (U8 receiver in)	H	Normal
Transmit Out (U8)	2A2	2Y2 (U3-11 line driver)	L	BIT
Receiver In (U2)	1Y1	1A1 (U4-1/2 line receiver)	H	BIT
Receiver In (U2)	2Y1	2A1 (U2 - transmitter out)	L	Normal
Receiver In (U8)	2Y1	2A1 (U8 - transmitter out)	L	Normal
Receiver In (U8)	2Y2	2A2 (U4-14/15 line receiver)	H	BIT

3.4 INPUT SEQUENCE

Serial data is received and converted to system logic levels by differential line receiver U3 (see Appendix E for line receiver specifics). The received data is transferred to the UARTS via switch U5 if BIT mode is not selected. Serial byte data is converted to parallel data in accordance with the control format and placed in the receiver buffer register. The DR (high) UART signal indicates that an input was processed by the UART and placed in the receiver buffer register. Each UART DR signal is monitored and when both UART DRs are high a full 16-bit word has been captured. The I/O command, IN09, is used to place the UART data on the data bus (DB00 - DB15). The low level of I/O command IN09 cause the DR to be reset and octal buffers U1 and U7 to be enabled and pass UART data. (UART control RRD is always low which constantly enables the UART output register).

The DR signals are gated by Nand gate U6-11. When both UART receiver buffers have data, both Nand gate inputs are high and cause INT2 (6-11) to go low. Nand gate output U6-11 is inverted by Nand gate inverter U6-3 to a high to provide a UART reverse buffer full status (ST10).

The converting of transmitter OUT to receiver IN is controlled by the UART BIT register U9. When I/O command IN10 is low, U9-9 goes low and enables BIT. BIT is reset by I/O command OUT11 which cause U9-9 to go high and enable the normal path of switch U5.

3.5 BALLISTIC DATA

8 bits of data; 20 - 24, parity and 2 lows, are transferred to data bus DB00 - DB07 whenever I/O command IN07 is low enabling octal buffer U14.

4.0 INPUTS/OUTPUTS

The Output Interface Board has three connectors: signal connectors P1A, P1B, and test connector J1. Pinouts and functions are shown in Tables 5 through 7 respectively.

5.0 POWER CHARACTERISTICS

Table 8(a) delineates the type of device and typical and maximum power consumption for each device. Table 8(b) summarizes the actual device power requirements for the Output Interface Board.

TABLE 5. P1A PIN CONNECTIONS (OUTPUT INTERFACE)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	LOGIC GROUND	29	
2	LOGIC GROUND	30	DTBRE1 UART1
3	DB04		Transmit buffer empty
4	DB05	31	DTBRE2 UART2
5	DB06		Transmit buffer empty
6	DB07	32	
7	DB11	33	
8	DB10	34	
9	PB09	35	
10	DB08	36	
11		37	
12	DB15	38	
13	ST10 Strobe 10	39	
14		40	
15	<u>OUT 11</u> Channel 11 Out	41	
16	<u>IN09</u> Channel 09 In	42	
17	<u>INT2</u> Interrupt 2	43	
18	DB14	44	<u>DR1</u> UART 1 Data Ready
19		45	<u>OUT10</u> Channel 10 Out
20	DB13	46	
21		47	
22	DB12	48	DR2 UART 2 Data Ready
23		49	
24		50	2MHZ Clock
25	DB00	51	
26	DB01	52	+5 Volts
27	DB02	53	+5 Volts
28	DB03	54	

TABLE 6. P1B PIN CONNECTIONS (OUTPUT INTERFACE)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	+5 Volts	24	Parity-Ballistic bit parity
2	+5 Volts	25	IN07 Channel 07 In
3	DPE2 UART 2 Parity error	26	
4	DPE1 UART 1 Parity error	27	
5	IN10 Channel 10 In	28	+15 Volts
6		29	+15 Volts
7		30	
8	DSI1+ Transmission Line	31	-15 Volts
	Receiver 1+	32	-15 Volts
9	DSI2- Transmission Line	33	
	Receiver 1-	34	+10 Volts
10	DSI3+ Transmission Line	35	
	Receiver 2+	36	
11	DSI4- Transmission Line	37	
	Receiver 2-	38	+20 Volts
12		39	
13	DSO1+ Transmission Line	40	-20 Volts
	Driver 1+	41	
14	DSO2- Transmission Line	42	+15 Volt Ref
	Driver 1-	43	+10 Volt Ref 1
15	DSO3+ Transmission Line	44	+10 Volt Ref 2
	Driver 2+	45	+10 Volt Ref 3
16	DSO4- Transmission Line	46	+5 Volt Ref
	Driver 2-	47	
17		48	-10 Volt Ref
18		49	-15 Volt Ref
19	20 Ballistic bit 20	50	
20	21 Ballistic bit 21	51	
21	22 Ballistic bit 22	52	Signal Ground
22	23 Ballistic bit 23	53	Signal Ground
23	24 Ballistic bit 24	54	

TABLE 7. J1 PIN CONNECTIONS (OUTPUT INTERFACE)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	T1TRO UART 1 Transmitter Out	28	
2	T1RRI UART 1 Receiver Input	29	
3	T2TRO UART 2 Transmitter Out	30	
4	TBITSEL BIT Select	31	
5	T2RRI UART 2 Receiver input	32	
6		33	
7		34	
8		35	
9		36	
10		37	
11		38	
12		39	
13		40	
14		41	
15		42	
16		43	
17		44	
18		45	
19		46	
20		47	
21		48	
22		49	
23		50	
24		51	
25		52	
26		53	
27		54	

TABLE 8(a). DEVICE POWER CHARACTERISTICS

DEVICE NAME	DEVICE TYPE	CIRCUIT DESIGNATION	VOLTS	POWER	
				TYP (MW)	MAX (MW)
UART	HD1B-6402-8	U2 and U8	5	4.75	9.5
OCTAL Buffers	54LS244	U1, U7, U14	5	130	225
OCTAL Buffers	54LS241	U5	5	130	225
Line Source	55114	U3	5	185	250
Line Receiver	55115	U4	5	160	250
Quad Nand	54LS00	U6	5	8	15
Dual D FF	54LS74	U9	5	20	40
Linear Regulator	723	U10	20	440	880
Linear Regulator	723	U15-U17	15	170	134.9
Linear Regulator	723	U11	10	220	440
Linear Regulator	μC1563	U12	-20	540	1020
Line Regulator	MC1563	U13	-15	210	390

TABLE 8(b). OUTPUT INTERFACE ACTIVE DEVICE POWER REQUIREMENTS

DEVICE NAME	DESIGNATOR	POWER TOTAL (MW)					
		5V	10V	15V	20V	-15V	-20V
UART	U2 and U8	9.5	19				
Octal Buffers	U1,U7,U14	390	675				
Octal Buffers	U5	130	225				
Line Driver	U3	185	250				
Line Receiver	U4	160	250				
Quad Nand	U6	8	15				
Dual D FF	U9	20	40				
Line Regulators	U10				440	880	
	U15-U17			510	1005		
	U11		220	440			
Line Regulators	U13					210	390
	U12						540 1020
Total		902.5	1466	220 440	510 1005	440 880	210 390 540 1020

APPENDIX A



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6402

CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)

JANUARY 1978

Features

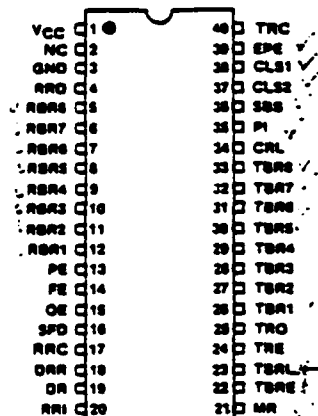
- OPERATION FROM D.C. TO 4.0MHz @10.0 VOLTS
- LOW POWER-TYP. 10mW @ 2.0MHz AND 5.0 VOLTS
- 4 TO 11 VOLT OPERATION
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UARTS
- SINGLE POWER SUPPLY.

Description

The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits operation clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Pinout

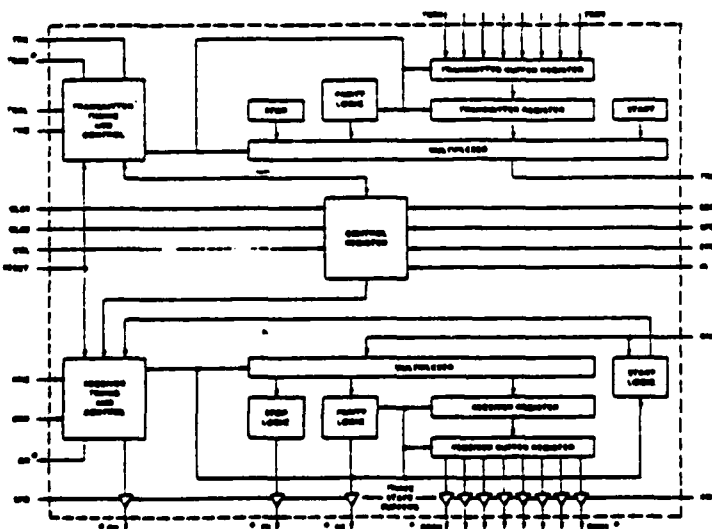


Control Definition

CONTROL WORD CHARACTER FORMAT

C	L	P	E	S	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

Functional Diagram



Specifications HD-6402A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6402A-9	-40°C to +85°C
Military HD-6402A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 10.0V ± 0.5V, TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V _{IH}	Logical "1" Input Voltage	70% VCC			V	
V _{IL}	Logical "0" Input Voltage			20% VCC	V	
I _{IL}	Input Leakage	-1.0		1.0	μA	0V ≤ V _{IN} ≤ VCC
V _{OH}	Logical "1" Output Voltage*	VCC - 0.01			V	I _{OUT} = 0
V _{OL}	Logical "0" Output Voltage*			GND + 0.01	V	I _{OUT} = 0
I _O	Output Leakage	-1.0		1.0	μA	0V ≤ V _O ≤ VCC
I _{CC}	Supply Current		5.0	500	μA	VCC = 10.5V, V _{IN} = VCC or GND
C _{IN}	Input Capacitance*		7.0	8.0	pF	
C _O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested.

A.C.

		VCC = 10.0V ① TA = 25°C			VCC = 10V ± 0.5V TA = Industrial or Military			UNITS	CONDITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX		
f _{clock}	Clock Frequency	D.C.		6.0	D.C.		4.0	MHz	
t _{pw}	Pulse Widths CRL, ORR, TBRL	75		100				ns	C _L = 50pF
t _{sw}	Pulse Width MR	350		400				ns	See Switching Time
t _{SET}	Input Data Setup Time	40		40				ns	Waveforms 1, 2, 3
t _{HOLD}	Input Data Hold Time	30		30				ns	
t _{pd}	Output Propagation Delays			50			70	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature. 10V data provided for information—not guaranteed.

Switching Waveforms

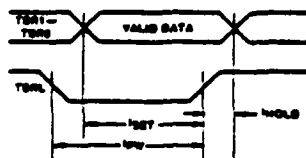


FIGURE 1
Data Input Cycle

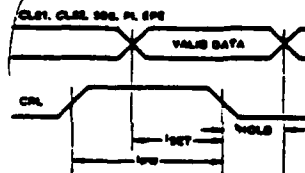


FIGURE 2
Control Register Load Cycle

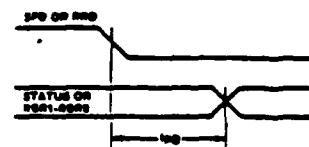


FIGURE 3
Status Flag Output Delays
or Data Output Delays

Specifications HD-6402

1-511-1002-6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Industrial HD-6402-9	-55°C to +125°C
Military HD-6402-2	

ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%. TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V _{IH}	Logical "1" Input Voltage	70% VCC			V	
V _{IL}	Logical "0" Input Voltage			20% VCC	V	
I _{IL}	Input Leakage	-1.0		1.0	μA	0V ≤ V _{IN} ≤ VCC
V _{OH}	Logical "1" Output Voltage	2.4			V	I _{OH} = -0.2mA
V _{OL}	Logical "0" Output Voltage			0.45	V	I _{OL} = 2.0mA
I _O	Output Leakage	-1.0		1.0	μA	QV ≤ V _O ≤ VCC
ICC	Supply Current		1.0	100	μA	V _{IN} = GND or VCC; VCC = 5.5V, Output Open
C _{IN}	Input Capacitance*		7.0	8.0	pF	
C _O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested

A.C.

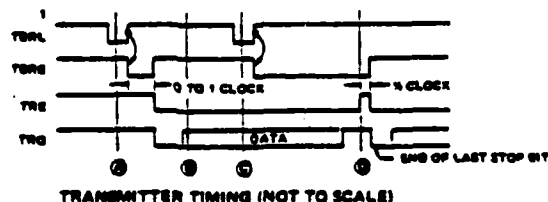
SYMBOL	PARAMETER	VCC = 5.0V TA = 25°C			VCC = 5.0V ± 10% TA = Indust. or MIL.			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
f _{clock}	Clock Frequency	D.C.		3.0	D.C.		2.0	MHz	
t _{pw}	Pulse Widths CRL, DRR, TBRL	150			150			ns	C _L = 50pF
t _{pw}	Pulse Width MR	350			400			ns	See Switching Time
t _{SET}	Input Data Setup Time	50			50			ns	Waveforms 1, 2, 3
t _{HOLD}	Input Data Hold Time	80			60			ns	
t _{od}	Output Propagation Delays			125			160	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature. 5V data provided for information—not guaranteed.

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. (A) Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. (B) The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later, data is transferred

to the transmitter register; TBREmpty is cleared; TBREmpty is set high; and serial data transmission is started. Output data is clocked by TRClock. The clock rate is 16 times the data rate. (C) A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



Specifications HD-6402C-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range (Industrial -9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ± 5%, TA = Industrial

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V _{IH}	Logical "1" Input Voltage	VCC -2.0			V	
V _{IL}	Logical "0" Input Voltage			0.8	V	
I _{IL}	Input Leakage	-10.0		+10.0	μA	0V ≤ V _{IN} ≤ VCC
V _{OH}	Logical "1" Output Voltage	2.4			V	I _{OH} = -0.2mA
V _{OL}	Logical "0" Output Voltage			0.45	V	I _{OL} = 2.0mA
I _O	Output Leakage	-10.0		+10.0	μA	0V ≤ V _O ≤ VCC
I _{CC}	Supply Current		1.0	800	μA	V _{IN} = GND or VCC VCC = 5.25V Output Open
C _{IN}	Input Capacitance*		7.0	8.0	pF	
C _O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested.

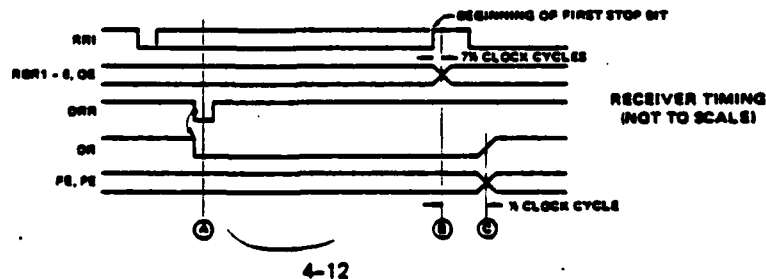
SYMBOL	PARAMETER	VCC = 5.0V TA = 25°C			VCC = 5.0V ± 5% TA = Industrial			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
f _{clock}	Clock Frequency	D.C.		2.0	D.C.		1.0	MHz	
t _{pw}	Pulse Widths CRL, ORR, TBR	200			225			ns	C _L = 50pF
t _{pw}	Pulse Width MR	500			600			ns	See Switching Time
t _{SET}	Input Data Setup Time	60			75			ns	Waveforms 1, 2, 3
t _{HOLD}	Input Data Hold Time	75			90			ns	
t _{pd}	Output Propagation Delays			150			190	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature. 5V data provided for information—not guaranteed.

Receiver Operation

Data is received in serial form at the Rinput. When no data is being received, Rinput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. (A) A low level on ORReset clears the DReady line. (B) During the first stop bit data is transferred from the receiver register to the RRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the

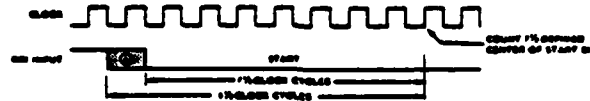
least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RRegister. (C) ½ clock cycle later DReady is reset to a logic high. PError and FError are evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.



Start Bit Detection

The receiver uses a 16X clock for timing. (A) The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7%. If the receiver clock is a sym-

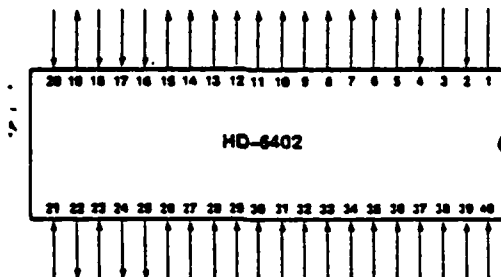
metrical square wave, the center of the start bit will be located within $\pm \frac{1}{32}$ clock cycle, $\pm \frac{1}{32}$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



Pin Assignment And Functions

PIN	SYMBOL	DESCRIPTION
1	VCC	Positive Voltage Supply
2	NC	No Connection
3	GND	Ground
4	RRO	A High level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RRR1 - RRR8 to a high impedance state.
5	RORS	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word format less than 8 characters are right justified to RRR1.
6	RRR7	See Pin 5 - RORS
7	RRR6	See Pin 5 - RORS
8	RRR5	See Pin 5 - RORS
9	RRR4	See Pin 5 - RORS
10	RRR3	See Pin 5 - RORS
11	RRR2	See Pin 5 - RORS
12	RRR1	See Pin 5 - RORS

PIN	SYMBOL	DESCRIPTION
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	SFO	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, OR, TERE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	ORR	A low level on ODATA RECEIVED RESET clears the data received output OR, to a low level.
19	OR	A high level on ODATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RR1	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.



PIN	SYMBOL	DESCRIPTION
21	MR	A high level on MASTER RESET clears PE, FE, OE, and OR to a low level and sets the transmitter output to a high level after 16 clock cycles.
22	TERE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TERL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1 - TBR8 into the transmitter buffer register. A low to high transition on TERL indicates data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transferred end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1 - TBR8. For character formats less than 8 bits the TBR6, 7, and 8 inputs are ignored corresponding to the programmed word length.

PIN	SYMBOL	DESCRIPTION
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation, Parity detecting and forces PE output low.
36	SBS	A high level on STOP BIT SELECT asserts 1.5 word bits for 8 character format and 2 word bits for other lengths. These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 8 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits)
37	CLS1	See Pin 37 - CLS2
38	CLS2	See Pin 37 - CLS2
39	EPB	When PI is low a high level on EVEN PARITY ENABLE generates and checks even parity. A low level asserts odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

SYNCHRO TRANSFORMER TECHNICAL DESCRIPTION

APPENDIX H

SYNCHRO TRANSFORMER MODULE

1.0 INTRODUCTION

The Synchro Transformer Board was developed to convert four groups of three-phase input synchro data to 4 groups of two-line resolver output data; to provide reference signals required for changes in amplitude and frequency of a modulation carrier and to provide a current measuring device to monitor UHF Homer data. The board also provides gating of +28 volt power output depending on the rms value of the 400 Hz reference signal that is also provided to inhibit BIT should 400 Hz fall below required values.

2.0 SYNCHRO TRANSFORMER BOARD KEY FEATURES

- a. Conversion of 4 sets of 3 input synchro data to 4 line resolver data through SCOTT T transformers.
- b. A DC reference of 400 Hz rms frequency for amplitude compensation.
- c. A DC reference of a 400 Hz reference frequency for subsequent frequency compensation.
- d. Low current measuring capability for UHF homer monitoring.
- e. Low voltage 400 Hz reference.
- f. Threshold detection of a 400 Hz phase and subsequent gating of +28 volts if the threshold is exceeded. This detection can be used to prevent permanent bit latches/indicators from setting if the 400 Hz is not present.

3. FUNCTIONAL DESCRIPTION

A block diagram of the Synchro Transformer board is shown in Figure 1. Four SCOTT T synchro transformers convert 3 wire (S1, S2 and S3) signals to 4-wire resolver signals. The synchro inputs are characterized by line to line amplitudes $\sin 0 \sin \omega t$, $\sin (0 + 120^\circ) \sin \omega t$ and $\sin (0 + 240^\circ) \sin \omega t$ where ω is the carrier frequency. The amplitude is 11.8 volts RMS and the frequency is 400 Hz. The resolver outputs are represented as $\sin 0 \cos \omega t$ and $\cos 0 \cos \omega t$ where ω is the carrier frequency, output amplitude is 11.8 volts and the frequency is 400 Hz.

The UHF homer extracts the input signal as a current reference above 0 volts and provides a fixed output when no current flows or an output reflecting the current flow.

The 115 volt 400 Hz, A phase input voltage is converted to 3V by a reference transformer. This 3 volt reference signal is used to develop a reference for sample pulse generation. The 3 volt reference is converted

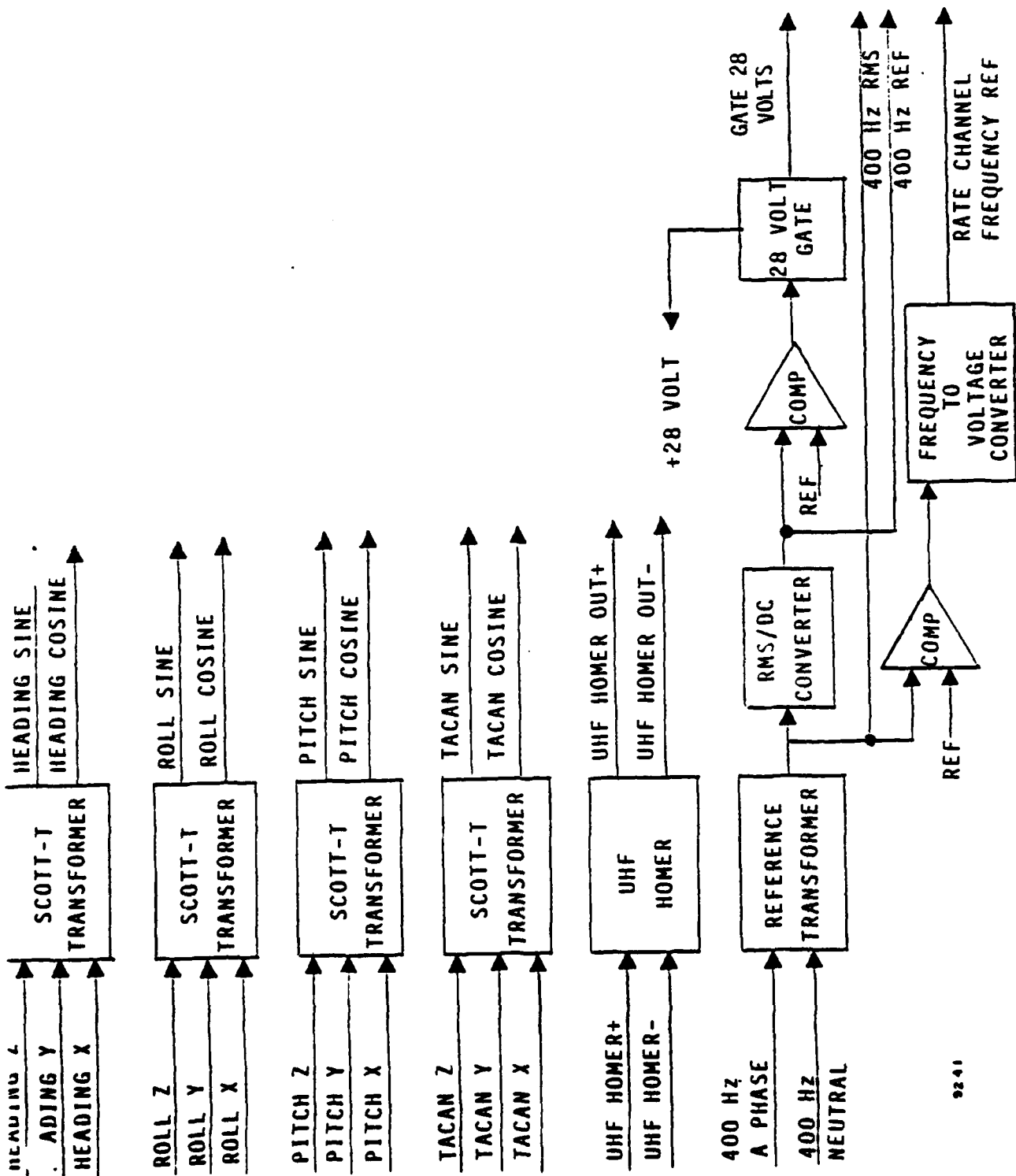


FIGURE 1. SYNCHRO TRANSFORMER BOARD BLOCK DIAGRAM

to a DC voltage which is directly proportional to the RMS value of the reference by the RMS to DC converter. The RMS DC level is used to compensate for data values obtained when variations in the 400 Hz generation system RMS value exist. The RMS-DC level is also compared to a reference threshold to determine if suitable 400 Hz RMS exists. If the DC-RMS value exceeds the threshold reference, 28 volts is gated on. If an insufficient DC-RMS value exists (below threshold), the comparator output inhibits the 28 volts. The gated 28 volts can be used to prevent a BIT failure as a result of loss of 400 Hz and processing of equations when analog data is inaccurate.

Variations in the frequency of the 400 Hz generation system are detected by a frequency to voltage conversion circuit. The detection is accomplished by converting the 3.0 volt reference signal to a square wave and converting the resultant square wave to a DC reference by the frequency to voltage conversion. This output signal can be used to compare analog measurements based on 400 Hz when the frequency varies.

3.1 Detailed Theory of Operation

3.1.1 SCOTT T Transformers

The transfer function of the 4 SCOTT T transformers (T1-T4) is shown in Figure 2. A transformer is provided for Heading, Roll, Pitch and TACAN signal attenuation.

3.1.2 RMS Reference Circuit

The A phase of the 400 Hz, 115 volt input power is converted to a $3V \pm 0.1\%$ output by transformer T5. The signal developed across transformer T5 is used as a low voltage system reference for off-board use (P1-13), for frequency to voltage conversion and for obtaining a DC level for RMS value. The RMS to DC converter (U5) computes the true RMS level of an AC input signal (400 Hz 3 volt reference) and provides an equivalent DC output level for DIWAC. The output of the RMS to DC converter (U5-6) is used by the A/D converter module for use in software comparison. The output of the RMS to DC converter is also used as a 400 Hz detector. A threshold reference voltage and the RMS to DC converter provide two inputs to a comparator. The threshold voltage is set to -15% of 3 volts by resistor divider network R21 and R2 and is 2.545 volts*. The comparator output (U6-11) controls transistor Q2, gating 28 volts to the BIT latch circuit. If the RMS-DC converter output falls below the threshold, Q2 is turned off.

$$* \left(\frac{28 \text{ Volts}}{9.76K + 0.976K} \times 0.976K \right)$$

3.1.3 Frequency to Voltage Conversion

U4 frequency to voltage converter (FVC) is used to change a waveform of a certain frequency to a DC voltage. When the input frequency to the FVC changes, the output voltage changes by an amount directly proportional to the frequency of the input waveform.

Comparator U3 is used to change a reference sine wave into a square wave. This square wave goes through an RC differentiator (capacitor C11 and resistor R11) which changes it to positive and negative voltage spikes or pulses. The FVC is triggered by the negative pulses.

The output of the FVC has ripple that must be filtered to get a smooth DC voltage. An RC low pass filter (capacitor C15 and resistor R17) connected to the output of the FVC removes ripple and noise. The FVC requires incoming pulses to be integrated. Resistor R16 and R15 and capacitor C12 provide the integration for an input frequency carrier at 400 Hz.

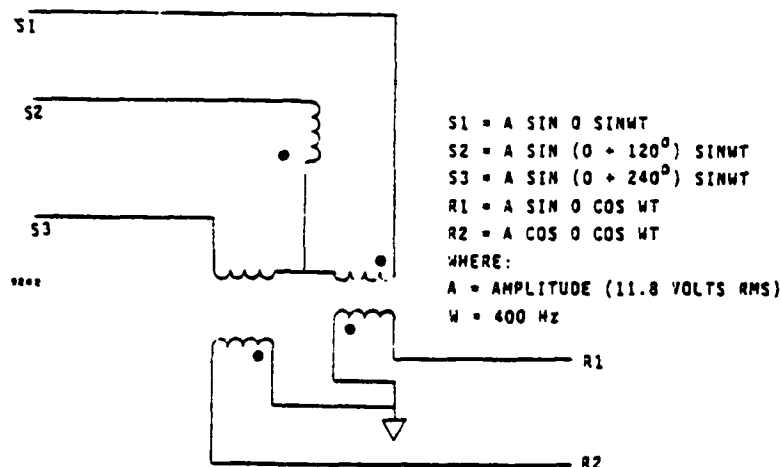


FIGURE 2. SCOTT T TRANSFORMER

3.1.4 UHF Homer

The UHF Homer circuit provides the facility for transforming low-level currents into a differential voltage. Operating under normal conditions, the UHF Homer can be considered as 2 amplifiers (U1 and U2) referenced to a base voltage. The voltage present at UHF Homer input (UHF Homer + IN and UHF Homer - IN) is amplified by current amplifier U2. The output of amplifier U2 is the amplifier gain times the input voltage or;

$$\frac{e_{OUT}}{\Delta e (UHF IN^+ - UHF IN^-)} = G = \frac{R_8}{R_6} = \frac{100 \text{ K}\Omega}{6.6 \text{ K}\Omega} = 15.15$$

The voltage input to amplifier U1 is a result of the current drop through resistors R4 and R5 or;

$$\Delta e = I_{RP} (I = \text{UHF Homer Input Current})$$

Where:

$$R_p = \frac{R_4 + R_5}{R_4 \times R_5} = 1.17 \text{ K}\Omega$$

Or:

$$\text{UHF IN}^- = \text{UHF IN}^+ - \frac{R_4 R_5 I}{R_4 + R_5}$$

Since amplifier U1 is a unit gain amplifier, the differential output between the outputs of amplifier U1 and U2 is:

$$\Delta v = U_1 \text{ OUTPUT} - U_2 \text{ OUTPUT}$$

$$\Delta v = \text{UHF IN}^+ - R_p I - G e$$

Where:

$$G e = G I R_p$$

$$\Delta v = \text{UHF IN}^+ - (R_p I - G I R_p) = \text{UHF IN}^+ - (1+G) I R_p$$

$$= \text{UHF IN}^+ - (16.15 \cdot 1.17 \text{ K}\Omega) I$$

$$= \text{UHF IN}^+ - 18.9 \text{ KI}$$

The UHF Homer is designed for two limit conditions. If the output of amplifier U1 exceeds 10.7 volts, diode CR1 becomes forward biased. Moreover, if no input current to the UHF Homer is provided, FET, Q1, is turned on causing a 10 volt input to the inverting input of amplifier U2. The output of amplifier U2 is equal to 10 volts

$$\left(\frac{R_8}{R_3} \cdot 10 \text{ volts} = \frac{100 \text{ K}\Omega}{100 \text{ K}\Omega} \cdot 10 \text{ volts} \right)$$

4.0 INPUTS/OUTPUTS

The Synchro Transformer board has one connector, P1. Connector signals are delineated in Table 1.

5.0 POWER CHARACTERISTIC

The power characteristics of the active devices are given in Table 2 (a) in terms of typical and maximum milliwatts. The total power used by all active devices on the Synchro Transformer board is given in Table 2 (b).

TABLE 1. P1 PIN CONNECTIONS (SYNCHRO TRANSFORMER)

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1		28	Cos Pitch T
2		29	400 Hz Neutral
3	Roll Y	30	400 Hz A Phase
4	Roll X	31	
5	Roll Z	32	Tacan Y
6	Sin Roll T	33	Tacan X
7	Heading Y	34	Tacan Z
8	Heading X	35	
9	Heading Z	36	Sin Tacan T
10	Cos Roll T	37	
11	Sin HDG T	38	Cos Tacan T
12	Cos HDG T	39	
13	400 Hz Ref	40	
14	Pitch Y	41	
15	Pitch X	42	UHF Homer + Out
16	Pitch Z	43	UHF Homer - Out
17	Rate Channel DC Ref (0-3 Vdc)	44	UHF Homer - In
18	Sin Pitch T	45	UHF Homer + In
19		46	
20	+28 Volts	47	-15 Volts
21		48	-15 Volts
22	+28 Bit	49	
23		50	
24	+10 Volts	51	
25	+10 Volts	52	+15 Volts
26		53	+15 Volts
27	Rate Channel Freq Ref	54	

TABLE 2(a). ACTIVE DEVICE POWER DISSIPATION

DEVICE NAME	CIRCUIT DESIGNATORS	DESCRIPTION	POWER (MILLIWATTS)							
			-15 VOLTS		+15 VOLTS		+28 VOLTS		+10 VOLTS	
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX
LM107	U1, U2	Amplifier	27	45	27	45				
LM111	U3, U6	Comparator					142.8	168	51	60
AD536	U5	RMS/DC Converter					28	56		
VFC32	U4	Freq to Voltage Converter	67.5	82.5						

TABLE 2(b). SYNCHRO TRANSFORMER BOARD POWER REQUIREMENTS

DEVICE NAME	CIRCUIT DESIGNATORS	QTY	POWER (MILLIWATTS)							
			-15 VOLTS		+15 VOLTS		+28 VOLTS		+10 VOLTS	
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX
LM107	U1, U2	2	54	90	54	90				
LM111	U3, U6	2					142.8	168	51	60
AD536	U5	1					28	56		
VFC32	U4	1	67.5	82.5						
TOTAL POWER			121.5	172.5	54.0	90.0	170.8	224	51	60

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