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A CORTICALLY IMPLANTABLE MULTIELECTRODE ARRAY FOR INVESTIGATING--ETC(U)
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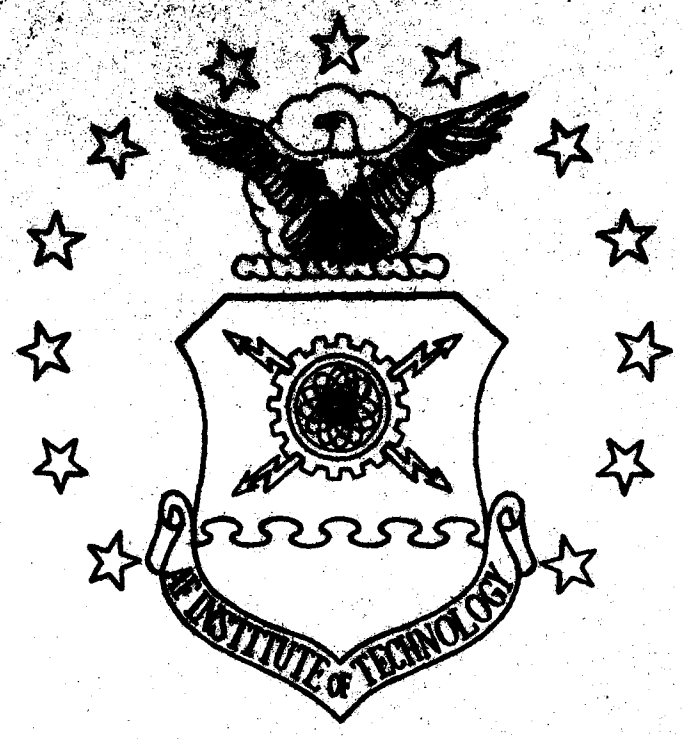

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A CORTICALLY IMPLANTABLE MULTIELECTRODE ARRAY FOR INVESTIGATING THE MAMMALIAN VISUAL SYSTEM

THESIS

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Capt USAF

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A CORTICALLY IMPLANTABLE MULTIELECTRODE ARRAY FOR INVESTIGATING THE MAMMALIAN VISUAL SYSTEM

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science

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by
George W. German III, B.S.
Capt USAF
Graduate Electrical Engineering
December 1981

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Preface

The importance of visual research was emphasized this year by the award of the Nobel Prize for Medicine to Hubel and Weisel for their investigation of signal processing in the visual system. Their research concentrated on the function of individual neurons within the striate cortex. This thesis proposes an operational device that may extend visual research from the investigation of single cortical neurons to the investigation of groups of associated neurons. Specifically, the AFIT Multielectrode Array could be used to analyze the bioelectric signals produced on the surface of the visual cortex in response to changes in the visual field.

I gratefully acknowledge the motivation generated by Dr. Matthew Kabrisky. His insight to the problems of visual perception provided the inspiration to continue this project. The technical assistance and facilities provided by the Air Force Avionics Laboratory were essential during the fabrication and testing phase. I also acknowledge the indebtedness to the Dayton NCR Integrated Circuits Laboratory for providing additional passivation samples.

A special thank-you goes to my family whose love, patience, and understanding gave me the fortitude to complete this research effort. A final thank-you belongs to our Creator, who gave us the ability to be curious, to analyze, and to resolve conflicts about the Universe surrounding us.

George W. German III

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Abstract

The research conducted during this study is a continuation of the Tatman-Fitzgerald (DTIC AD A080378, AD A100763) fabrication and testing of an implantable, multiplexed, multielectrode array that will be used to record the bioelectric signals emitted from the visual cortex of a live, visually functional animal. Primary emphasis of this study is the investigation of passivation materials that can be used to protect the AFIT Multielectrode Array from the harsh cerebrospinal environment encountered inside the cranium. Secondary emphasis is placed on analyzing the electrical characteristics of an AFIT JFET, designing an improved multiplexing drive circuit, and testing the system equipment with an operational device.

A CORTICALLY IMPLANTABLE MULTIELECTRODE ARRAY FOR INVESTIGATING THE MAMMALIAN VISUAL SYSTEM

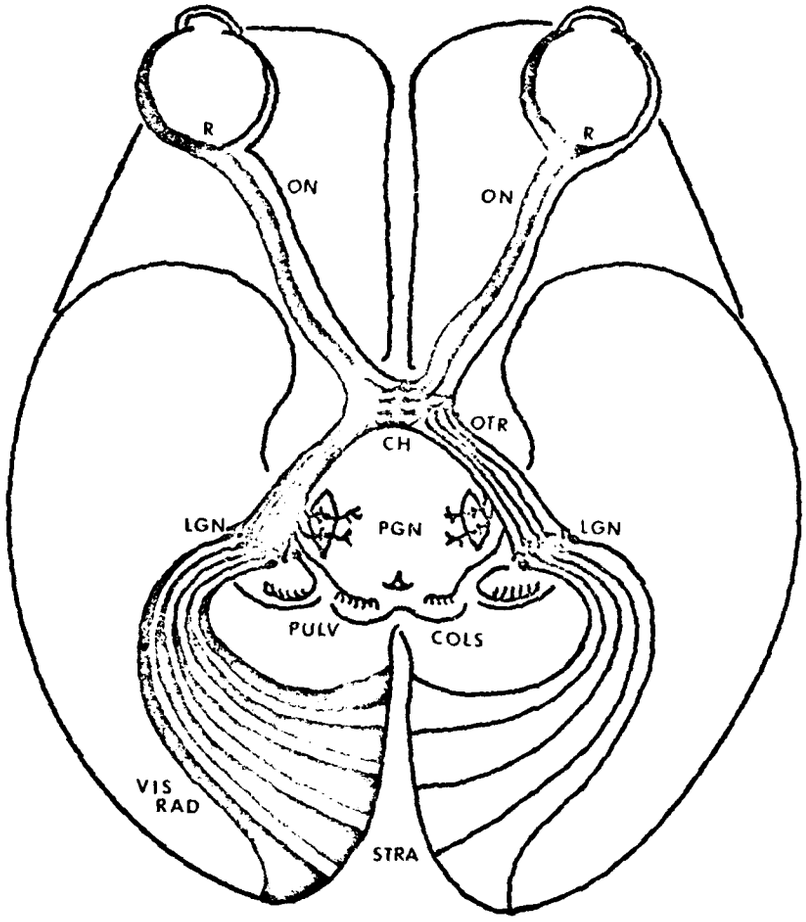
I. INTRODUCTION

"Few problems are more challenging than decoding the mass electrical activity of the human brain" (Ref 1:383).

SIGNIFICANCE

Fifteen years ago the world's population included as many as fifteen million blind people. Over the last decade and a half, these numbers have significantly increased. The latest statistics released by the National Society to Prevent Blindness reveals that the United States alone has more than 498,000 people without useful eyesight (Ref 2:5). To put things in better perspective, this year's production loss due to sightless people will amounted to over one billion man-hours. However impressive these figures are, they do not even begin to express the personal agony and frustration caused by sightless lives. Fortunately, the possiblity of giving sight to at least some of these totally blind people is beginning to generate a great deal of attention.

Historically, all of the spectacular advances for improving visual acuity have been limited to the eye itself. Figure 1 shows that the eye is only the beginning of the visual system. The major stumbling block in correcting other deficiencies in this system is lack of knowledge. Neurologists have anatomically charted the visual pathways from



R:	Retina	CH:	Optic Chiasma
ON:	Optic Nerves	STRA:	Striate Area
OTR:	Optic Tracts	COLS:	Superior Colliculus
LGN:	Lateral Geniculate Nucleus	PULV:	Pulvinar of Thalamus
PGN:	PregeniculateNucleus	VIS RAD:	Visual Radiations

(After Ref 3:289)

Fig. 1. The Visual Pathways

the retina of the eye, to the optic chiasma, to the lateral geniculate body, and then to the visual cortex. Analysis of these pathways led to the discovery of a homeomorphic mapping of the visual field onto the primary visual cortex (Brodmann's area 17). After this point, anatomical mapping becomes impossible. Area 17 contains an estimated 200 million neurons that interlace throughout the cortex, such that the limits of current knowledge become lost in the complexity of the mammalian brain.

The multielectrode array investigated in this thesis is planned as a prototype device useful in expanding the knowledge of the visual system. A much larger array could evaluate the organization of the visual cortex into the multi-neural modules of Basic Computational Elements (BCE) suggested by Kabrisky (Ref 4). Specifically, it will be able to determine the size, shape, and function of these BCE's. Evaluation of the data recorded from a set of arrays could provide a reasonably accurate mathmatical model of the visual transform function between Area 17 and Area 18. The ultimate goal of this type of research is to design a visual prosthetic device that will give sight to a multitude of visually handicapped individuals.

The second major significance of this research is in the field of pattern recognition. The best attempts by the largest computers available today have only resulted in primative Optical Character Reader-type pattern recognition devices. Unlike the eye, computers consume an inordinate amount of time performing a function the human brain literally

accomplishes in the blink of an eye. Also, computer algorithms are easily confused, and usually fail, under conditions of rotation, translation, scale-change, shape-change, and clutter. The problem of designing computer algorithms able to adjust to these parameters, even for the recognition of a single character of printed text, is extremely difficult. The task of building pattern recognition machines capable of identifying objects of interest to the Air Force, such as enemy tanks and aircraft, has not yet been accomplished. An analysis of the human visual system may provide the insight necessary to design pattern recognition devices that have the ability to quickly and accurately identify complex visual scenes, even in the presence of background clutter.

BACKGROUND

Neurocortical research can be divided into three distinct phases. Phase I is characterized by the work of Hubel and Weisel. Their primary mode of data collection was intracellular recording of single cortical neurons of anesthetized animals (Ref 5; Ref 6). While this was a noble beginning and did provide some meaningful data, their research contained three main drawbacks. First, because the electrode actually penetrates, hence damages the neuron under investigation, the data gathered may not represent normal activity. Wise has indicated that the majority of neural activity following an electrode insertion is caused by injury potential and is not a consequence of the normal function of the neuron (Ref 7:245). Second, analyzing the activity of one neuron out of

a group of 200 million neurons is like trying to determine the function of a large computer by investigating a single transistor. A better method would be to noninvasively analyze the fine-grained electroencephalographic (EEG) signals emitted by groups of related neurons. Third, in order to obtain useful data, the visual system must be operating as close to normal as possible. An anesthetized animal has a definite alteration of brain function that could drastically effect the results of subsequent testing. A preferable method would be to anesthetize the animal during the craniotomy, place the exposed area under a local anesethic, then allow the animal to completely recover from the general anesethic before any vision tests are initiated. This procedure should minimize the influence of drugs on the test results.

Phase II is characterized by the experiments conducted by DeMott (Ref 8; Ref 9). His 20 by 20 array of end-polished wire electrodes was an attempt to overcome the problems associated with invading a single neuron. DeMott's biggest technical problem was the management of the 400 individual wires attached to his array. His research did confirm that bioelectric signals could be recorded from the surface of the cortex without actually penetrating the cortical neurons. The University of Utah's transcutaneous plug (Ref 10; Ref 11) and the Stanford Ear Project (Ref 12), although much more complex than DeMott's wire bundle, also belong to this phase. The distinguishing feature of this phase is a one-to-one correspondence between recording sites and output lead wires. This arrangement requires N^2 lead wires for an N by N array.

As the size of the array expands, the number of lead wires increases by the square law, making the array physically unmanageable.

Brain research performed by bioengineering students at the Air Force Instiute of Technology may constitute Phase III of neurocortical research. Tatman, in consultation with Borky and Kabrisky, designed the first multiplexed multielectrode array for investigating the visual system (Ref 13). These photolithographically fabricated devices contain an array of Junction Field Effect Transistors (JFET) whose source lead is an electrode that can be capacitively coupled to the cortex. A large ground plane averages the bioelectrical signal over a large surface of the cortex and serves as a reference. Individual electrodes average bioelectrical signals over a much smaller area, such that any regional differences between the ground plane and each electrode can be recorded. The greatest advantage of this array is the multiplexing feature that reduces the minimum required lead wires for a N by N array to 2N. Further multiplexing in a more advanced device is possible as long as the maximum sampling rate for the fabricated device is not exceeded.

Fitzgerald solved many of the problems associated with the original photolithographic processing schedule (Ref 14). His experimentation resulted in a device that was operational in ambient air. Unfortunately, the device failed when subjected to the environment that would be encountered during implantation.

PROBLEM

The primary emphasis of this research concentrates on the investigation of passivation materials capable of shielding the multielectrode array from the harsh saline environment found inside a living animal. Once the device is encapsulated, it will be operationally tested in a saline solution chemically similar to cerebrospinal fluid. If the device withstands the ionic contaminants contained in saline it will be ready to implant in a live, visually functional animal. Data recorded from this first implant will determine if the device can respond to bioelectric signals emitted from the surface of the cortex.

Secondary emphasis deals with analyzing the electrical characteristics of an AFIT JFET, designing an improved multiplexing drive circuit, and testing the system equipment with an operational device.

SEQUENCE OF PRESENTATION

Although the emphasis of this research is placed on passivation materials, the sequence of presentation follows a more logical order. Chapter 2 discusses the operation of the multielectrode array, analyzes the switching characteristics of typical JFET's, and determines the electrical characteristics of the JFET's fabricated by the Tatman-Fitzgerald process. Chapter 3 evaluates the common failure modes of devices in contact with saline solution and investigates the passivation properties of common photolithographic materials.

Chapter 4 defines the design logic for an improved multiplexing drive circuit that can synchronously drive two multielectrode arrays. This capability is essential in investigating the mapping, timing, and operating characteristics of BCE's. Chapter 5 explores the integration of system components and the operational testing of the device using pseudobioelectric input signals. Chapter 6 summarizes the results of this research and provides recommendations for future research efforts.

II. SWITCHING CHARACTERISTICS

DESIRABLE SWITCHING CHARACTERISTICS

Chapter I indicated that the next phase in visual research was to obtain a large array of multiplexed electrodes, such that a large number of sampling sites can be enclosed in an easily manageable package. This multiplexing requires some type of anolog switching mechanism that will only allow specific electrodes to pass their input signal during any given time slice.

The Junction Field Effect Transistor (JFET) was used as the switching element in the AFIT Multielectrode Array because it most closely resembled the characteristics of the ideal switch:

1) Zero "ON" resistance (perfect conductor in the "ON" state).
2) Infinite "OFF" resistance (perfect insulator in the "OFF" state).
3) Zero switching time.
4) Zero noise.
5) Isolation of the signal source from the control signal.

Although a JFET is not a perfect switch, it is a reasonably close approximation. Typical n-channel JFET values for commercially fabricated JFET devices are given in Table I.

MULTIELECTRODE DESIGN

The AFIT Multielectrode Array is shown in Figure 2. The

TABLE I
N-Channel Switching Characteristics

	R(on)	R (off)	Switch Time	Noise
Values	50-200 ohms	1000 M ohms	20-50 nanoseconds	nearly noiseless
Reference	15:198	16:235	15:177	13:62

heart of this system is a 4 X 4 array of multiplexed analog JFET switches that regulate the passage of bioelectric signals sensed by an exposed electrode capacitively coupled to a cortical surface. Since the voltage developed in tissue decreases approximately as the square of the distance from the recording electrode, any surface electrode must be pressure-bonded to the cortex (Ref 17:214). Excess pressure must be avoided because any distortion of the cortical surface may present anomalies in the test results. Evoked potentials recorded by this procedure will be a summation of potentials reflecting the activity of numerous neurons underlying the electrode (Ref 18:498). The 0.016 square millimeter surface area of an AFIT electrode should provide the summation of approximately 1600 neurons (Ref 13:54).

The most unique feature of this array is its multiplex design. It is now possible to have an easily manageable bioelectric signal sensor that can be readily expanded to a large number of electrodes without a corresponding increase in the number of required lead wires. The stylized picture in Figure 3 shows that all the leads in each row are tied together. These row leads are the gate connections for the

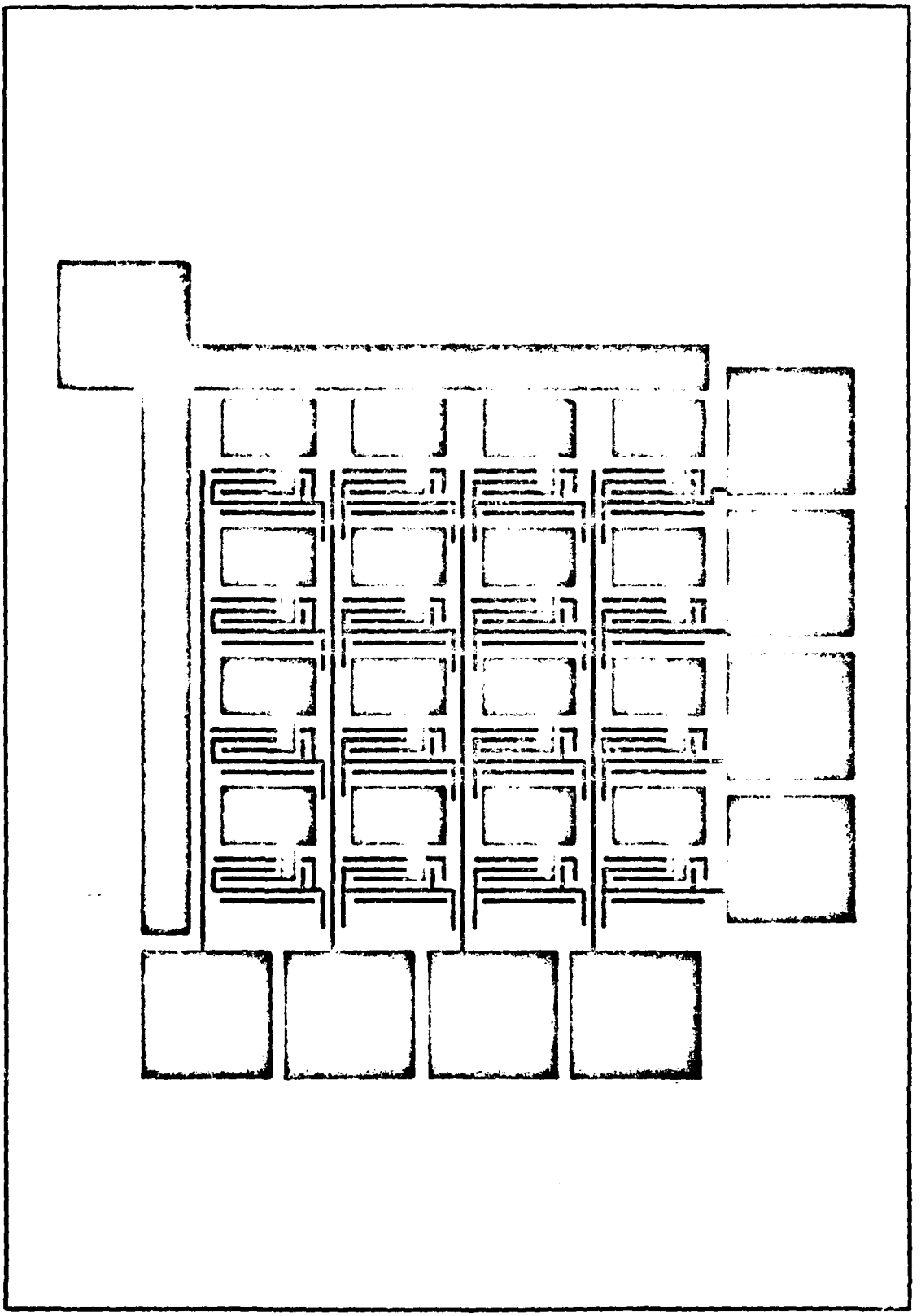


Figure 2: AFIT Multielectrode Array

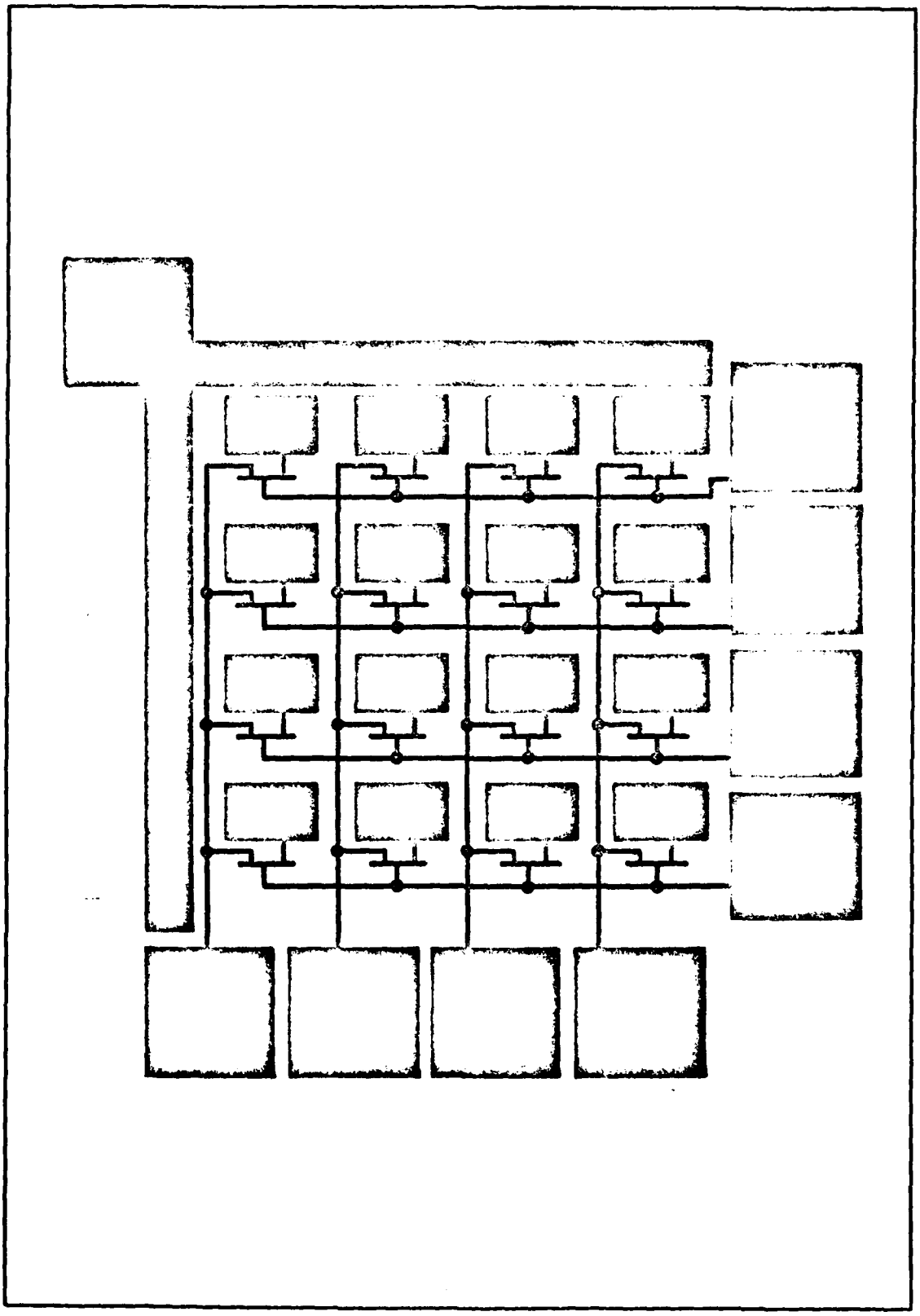
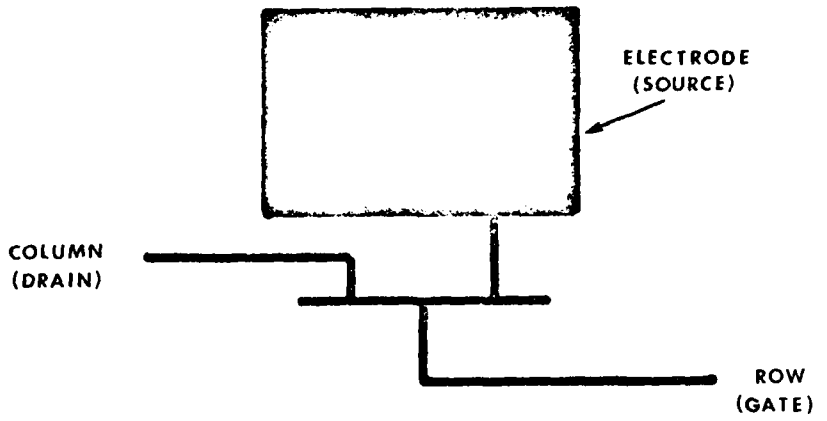


Figure 3: Stylized Geometry of AFIT Array

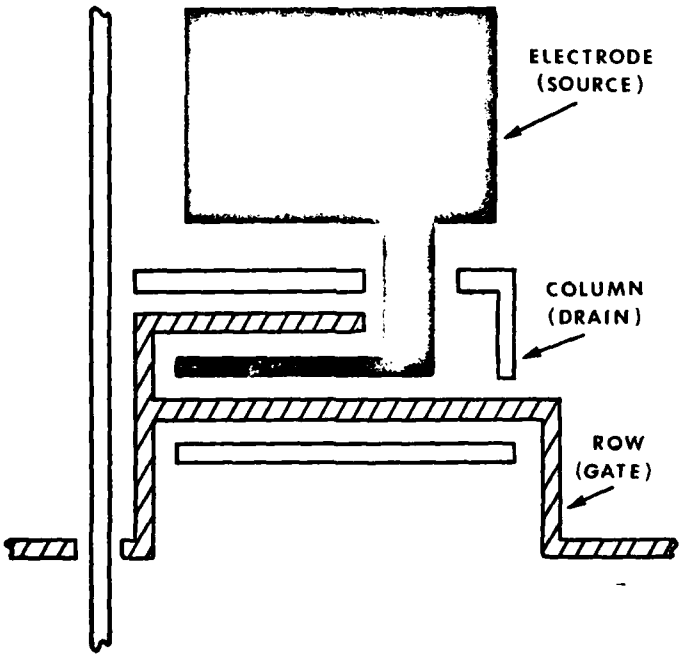
fabricated JFET's. In a similar fashion, all the leads in each column are tied together forming the drain connections for the JFET's. The electrodes are the source connections. The designation of the columns as the drain connections and the electrodes as the source connections has been reversed from the Tatman-Fitzgerald designation. The reason for this change is that the primary mode of operation for this device is to receive bioelectric signals from the electrode; therefore, I choose to call this the source. Since JFET's can typically pass signals equally in either direction during the "ON" state and block signals equally during the "OFF" state, this change is made only for conceptional simplicity and not for any change in function (Ref 19:193). Figure 4 shows the correspondence of the array design geometry with a typical JFET electrical schematic.

The multiplexing function is accomplished through the logic of the external drive circuitry discussed in Chapter 4. This logic controls the voltage applied to the row leads (gates) of the JFET's. During any clock cycle, three of the four rows are biased to the "OFF" state, while the fourth is in the "ON" state. In subsequent positive transitions of the clock pulse, the "ON" row cycles sequencially through the four available rows.

The JFET's in the "OFF" rows are nonconducting; therefore, the drains can not respond to signals sensed by the electrodes in those rows. In the "ON" state, the drain leads are conducting; therefore, they can pass the electrode-sensed bioelectric signals onto a recording device for storage.



a. JFET Schematic



b. AFIT JFET Geometry

(After Ref 13:57)

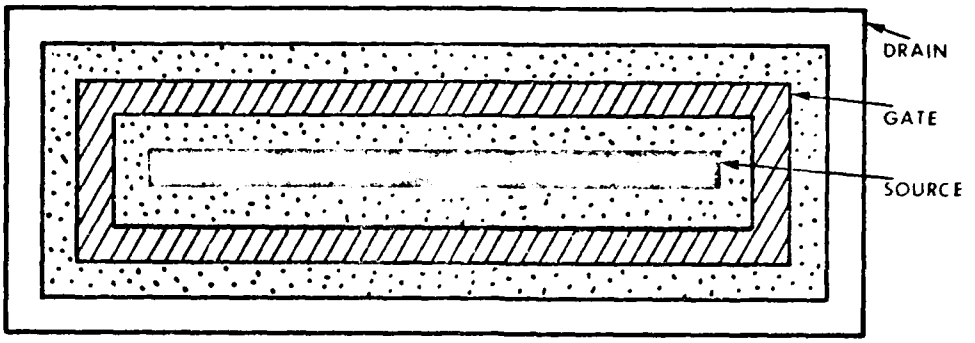
Figure 4: AFIT JFET Design

This design allows a time-shared sampling of input data. The original design of the AFIT Array called for an X-Y addressable electrode. During the testing phase, this capability was found to be unnecessary for this size of an array. With a simple 4 X 4 array, a 14-channel FM recorder can simultaneously record signals from all four column leads from two separate arrays. Analyzing the output of a specific electrode would only require interpreting the recordings for the specified channel on the recorder. This simplified the drive circuitry because only the row leads are required to be multiplexed. In the future, when the size of the array increases, it will be necessary to multiplex four-column blocks of column leads.

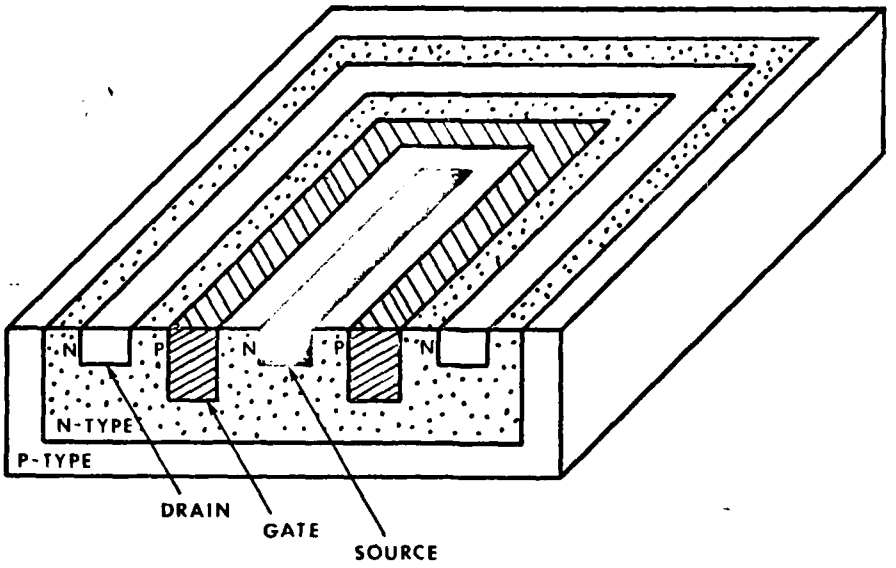
AFIT JFET OPERATION

Beneath all the diffusion masks of the AFIT JFET, lies the ring structure shown in Figure 5a. The outside ring is the drain, the middle ring is the gate, and the center is the source. Each ring is respectively connected to a column lead, row lead, and an electrode. Examination of the cross-section of this ring structure, shown in Figure 5b, helps explain the operation of the n-channel AFIT JFET.

A ground signal applied to the gate will not change the space charge within the channel that connects the source to the drain; therefore, the current through the channel is not effected. Since the resistance of the channel is on the order of 200 ohms, any signal at the electrode is transferred without distortion to the drain. If the gate is reverse biased



a. Ring Structure



b. Cross-section

(After Ref 13:64)

Figure 5: Internal Geometry of AFIT JFET

with a negative voltage, a depletion region is created in the channel. If the potential at the gate is driven more negative, the depletion region spreads across the width of the channel constricting the flow of current. A point is finally reached where the channel is completely closed. From Figure 5a, it is easily seen that this action completely isolates the source from the drain around the entire perimeter of the ring structure.

AFIT JFET SPECIFICATIONS

During the design phase, Tatman adjusted the geometric parameters of the device to obtain the desired calculated values for AFIT JFET characteristics. Once the device fabrication process was complete, Fitzgerald obtained experimental values for these characteristics from a series of 54 individual AFIT JFET's. The calculated and experimental values from their two studies are given in Table II.

In addition to the JFET testing conducted by Tatman and Fitzgerald, I examined another set of 80 individual AFIT JFET's. The family of curves for these JFET's, produced by a Tektronix Model 577-177 Curve Tracer, are shown in Appendix A. My original plan was to average these curves into a typical family of characteristic curves defining the JFET's manufactured by the Tatman-Fitzgerald process. It was assummed that all the JFET's would display characteristic curves within reasonably close tolerances. Although this was generally true within a specific array, it did not hold true between JFET's on different arrays. The difference in I_{dss} values

TABLE II
AFIT JFET Characteristics

	R (on)	R (off)	V (pinch)	Sw Time	Breakdown
Calculated Values	650 ohms	1000 M ohms	< 3 volts	4 nanosec	
Experiment Values	1600-3500 ohms	105 M-718 M ohms	0.6-2.2 volts		40 volts

for JFET's on different arrays varied as much as an order of magnitude. Even within a given array there are usually 2 to 3 JFET's that show substantially different I_{dss} values than the other JFET's on the array. Some of the possible reasons for this wide divergence in JFET characteristics are the following:

1) Less than optimum processing procedures (processing performed by students).

2) Less than optimum clean-room conditions (processing delayed or interrupted by equipment failures).

3) Excessive time span between the fabrication process and the application of the final passivation layer (various steps performed by different students at different times).

All of these factors contribute to increased contamination levels within the structure of an array. In most cases, contaminated devices do not function reliably or even within the design specifications. One solution to this problem is to contract a commercial firm to fabricate a set of high quality AFIT Arrays.

III. DEVICE PASSIVATION

PASSIVATION DEFINED

Rapid expansion of the microelectronics industry has required an intensive investigation of a property called passivation. Generally, passivation refers to protecting electronic circuits from contaminants. This task has become increasingly difficult because, as the distance between components decrease, contamination becomes a critically limiting factor in process design. At today's technological levels, contamination as low as a few parts per million is sufficient to seriously degrade or prevent the operation of microcircuits (Ref 20:S46).

Ionic contaminants occur from two primary sources. They are either introduced during the fabrication process or they diffuse into a device due to an external accumulation of contaminants. Both of these sources can be controlled by utilizing ultra-clean fabrication processes and by immediately sealing the completed electronic circuit (Ref 21:21). Over the years, engineers have compiled a mass of data on electrical protection of circuits in "normal" surroundings; however, the bioengineer interested in fabricating devices used for implantation in live animals cannot strictly rely on these studies to produce an operational device. The environment of an implanted device is not the relatively contamination-free milieu inside a sealed microcircuit. Rather, the implanted circuit will be exposed to a highly corrosive, cerebrospinal fluid (CSF) environment. The passivation mat-

erial must resist water for long periods of time, remain nontoxic to biological processes, withstand high electric fields, and be virtually impervious to an extremely high concentration of sodium ions. Also, the passivation application process for coating electronic devices must be easily controlled to provide a high density, uniform layer of protection. Once the passivation layer has been applied to the multielectrode array, contact windows must be etched through the passivation material to expose the bioelectric sampling electrodes.

All the materials studied in this research effort use one or more of the standard application methods of Diffusion, Chemical Vapor Deposition (CVD), R-F Sputter, Plasma Deposition, or Spin-on. Since all the materials have well defined etch rates for the application methods used, this aspect of passivation will not be explored in this study.

PASSIVATION PROPERTIES

Some of the desirable characteristics of common passivation materials are given in Table III. Table IV provides a quick reference used to compare the properties of different materials.

The first major passivation property is the ability to resist water. Hydrophobicity in any electronic circuit is desirable; however, in implanted devices hydrophobicity is mandatory because of constant contact with CSF. Any moisture that is absorbed by the device will cause electrical shorts at surface defects or at hot spots where current densities are

TABLE III
Passivation Properties

Material	Water Absorption	Ref	Toxicity	Ref	Dielectric Strength Volts/cm	Ref	Dielectric Constant	Ref
Silicon Dioxide	low	23	rating 1	27: II-67	6×10^6	20: 540	3.82	31: 493
Silicon Nitride	zero	23: 52	unknown		6×10^6	23: 52	5.50	8: 125
Aluminum Oxide	zero	22: 77	rating 1	27: II-88	1×10^6	28: 16-31	8.00	28: 16-31
Phosphorus Glass (PSG)	low	24: 121	unknown		13×10^6	27: 265	4.00	27: 265
Polyimide	good if >60K A	25: 2	low	26	1.6×10^6	30: 5	3.50	30: 5
Parylene	zero	26:	low	26: 780	6×10^6	28: 16-32	2.10	28: 16-32
Teflon	unknown		rating 1	27: II-244	6×10^6	28: 16-32	2.10	33: 169

TABLE IV
Desired Passivation Values

Property	Water Absorption	Toxicity	Dielectric Strength	Dielectric Constant
Desired Value	zero	nontoxic	high	high

high (Ref 22:778). All of the materials listed in Table III have sufficiently low water absorption rates to satisfy this requirement.

Even if the bulk material shows good resistance to water, it still may not insure the desirable hydrophobotic barrier. One major processing defect that allows water to easily penetrate a sealed device is thermal cracks. These cracks are caused by mismatched thermal coefficients of expansion for the different materials used in the fabrication process. All the materials in Table III have thermal coefficients on the order of 10^{-6} units per degree centigrade. This compares favorably with the coefficient of silicon; therefore, any of these materials should minimize the effects of thermal cracks (Ref 34:49).

The second major passivation property is toxicity. The prototype multielectrode array investigated here, is intended only as an acute preparation; therefore, passivation/tissue compatibility is not of great importance. As the device becomes more refined, longer implants are highly desirable and the toxic effects of foreign bodies must be considered.

While Table III toxicity values are not quantitative, they do give an indication of passivation/tissue compatibility. Clinical Toxicology of Commercial Products divides substances into six toxicity ratings from 1 (practically nontoxic) to 6 (supertoxic). Specifically, Rating 1 means that the probable lethal oral dose is in excess of 15 grams per kilogram of body weight (Ref 27:Sec II,4). For an eighty pound baboon, this would be comparable to directly ingesting over a pound of the substance. Some of the other materials listed in Table III have been extensively studied in medical applications and have good blood and tissue compatibility. Sufficient toxicity data is not available to classify these materials in the rating scheme given above. However, use in medical applications implies a low toxicity level. The remaining materials on Table III are not indexed on the Toxic Substance List (Ref 35). This lack of data should not be construed as confirmation of the nontoxic properties of these materials, only that no one has reported any toxic side-effects. Toxicity ratings for these materials must be determined before using them to passivate a chronically implantable array.

The third major passivation property is the electrical characteristics of the passivation material. Dielectric breakdown strength is one of the most important electrical properties to insure optimum device performance and stability (Ref 20:540). Essentially, the outer passivation layer acts as a dielectric material with CSF making ohmic contact on one side, and a metalization layer making ohmic contact on the other. This dielectric layer must be capable of resisting

electric fields as high as 2.5 kilovolts per millimeter for a visual prosthesis (Ref 36:281). In addition to the dielectric strengths of Table III, another figure of merit is the length of time under a specified field before breakdown occurs. Since time to breakdown varies almost as the square of the dielectric thickness (Ref 37:1371), an easy solution for an acute device is to make the passivation layer thicker. There has not been a definitive research effort to correlate the time to breakdown with the thickness of the passivation materials listed in Table III. Most researchers have used passivation layers in the range of 2,000 to 10,000 angstroms thick. For the most part, the passivation layers studied here are also within that range.

The fourth major passivation property is sodium ion permeability. Comparison of the other properties of the materials studied reveals that the values for the passivation properties have all been reasonably close. None of the other properties have presented a serious roadblock to obtaining an operational device. Passivation against the invasion of sodium ions has become the single remaining obstacle that must be solved before an actual implant experiment can be scheduled. The Fitzgerald thesis (Ref 14) suggested that one of the modes of sodium ion penetration is through surface defects called pinholes. A second mode of penetration is due to an excess of mobile sodium ions that migrate through the passivation material. These two characteristics are so critical that their analysis has been expanded in the next five sections.

PINHOLE DEFECTS

Pinholes are the microscopic, 0.1 to 20 micron diameter, surface defects usually caused by these factors: unsuitable substrate cleaning, insufficient substrate moisture removal, mismatch in thermal expansion between the substrate and the passivating material, and insufficient passivation thickness (Ref 26:783). These factors can cause the appearance of abrupt changes in passivation density or contour in critical areas of a circuit. Flaws of this nature can be modeled as a defect column that permits electrical shorts between the passivation layer and other parts of the circuit (Ref 22:775).

Theoretically, within a dielectric defect column, electrical breakdown may occur at fields as low as 10^{-4} volts per angstrom, which is the breakdown for air (Ref 38:1). Referring back to Table III, this is considerably lower than the dielectric strengths of any of the passivating materials. This is also at least an order of magnitude below the approximate 3×10^{-5} volts per angstrom field strength expected during the "OFF" state of a JFET (Ref 31:102). Experimental evidence indicates that the high conductance associated with dielectric breakdown is caused by the developement of a gaseous channel through the passivation layer (Ref 39:239). Figure 6 shows what happens when a high electric field creats a plasma discharge within a pinhole column. This discharge can redistribute the metalization and ultimately provide a conduction path through the passivation layer.

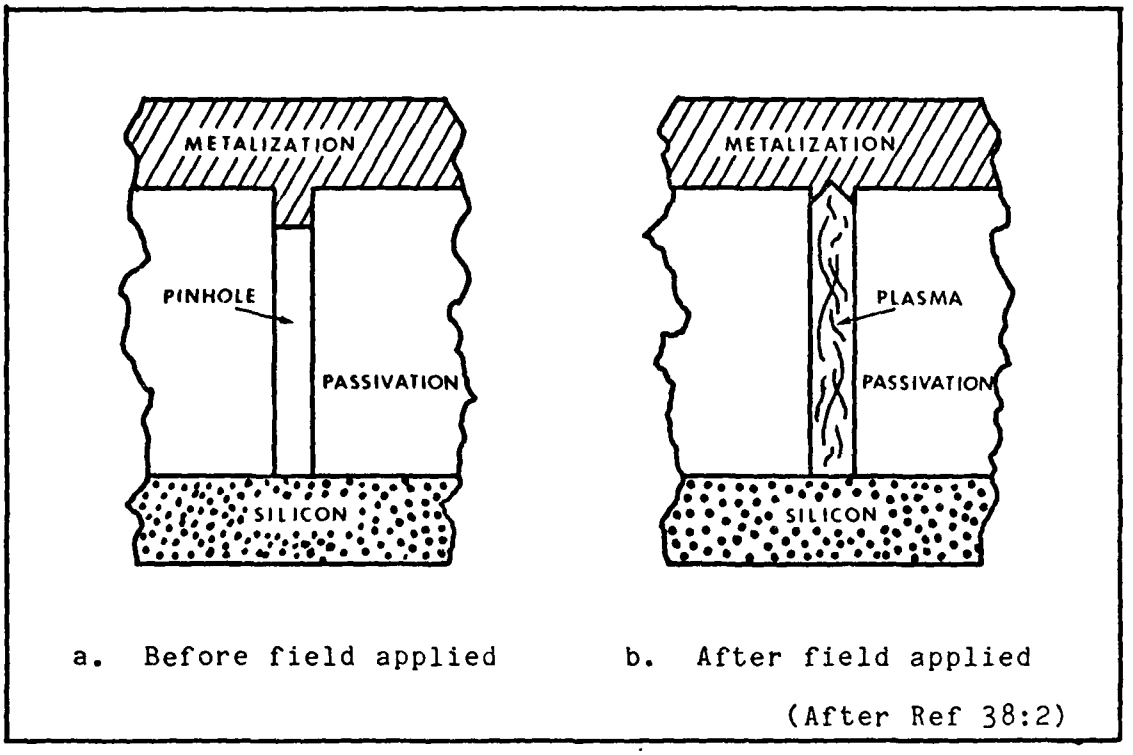


Figure 6: Plasma Discharge Within a Pinhole Column

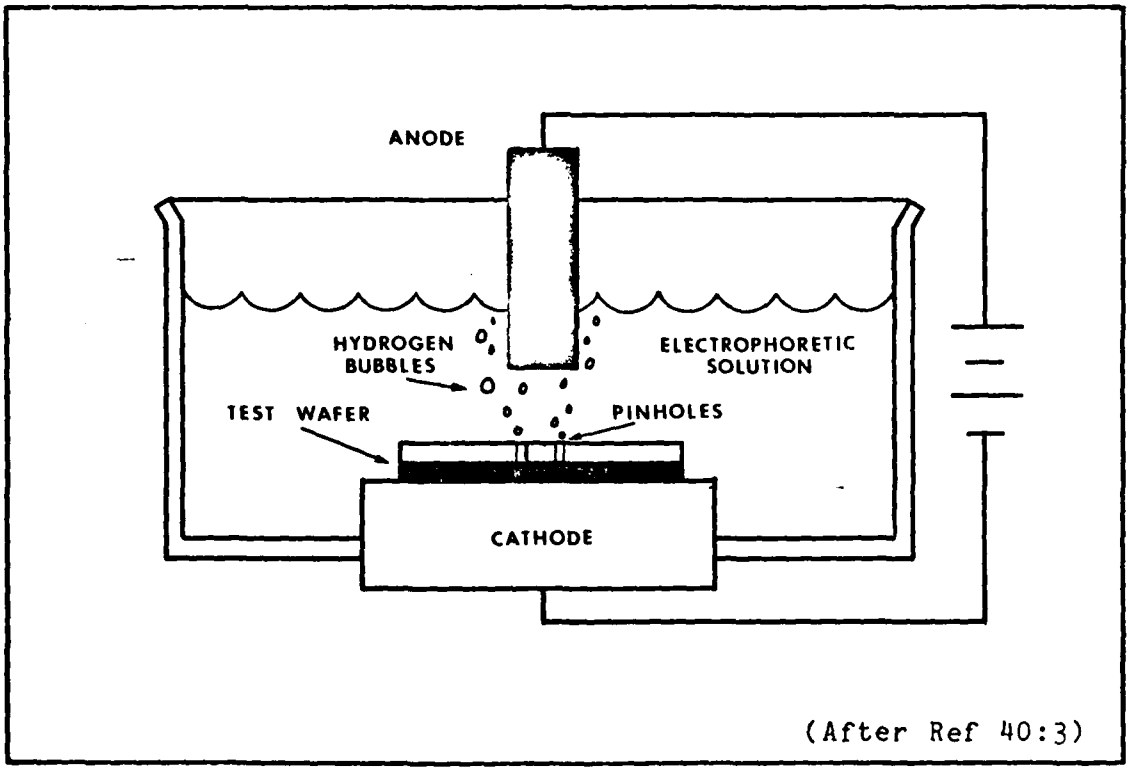


Figure 7: Dielectric Defect Detector

The NAVONIC Model 201 Dielectric Defect Detector was used to examine the number of pinholes in materials caused by various electric field strengths. This detector applies a high electric field between the substrate submerged in an electrophoretic solution (absolute methanol) and the anode suspended above the substrate, as shown in Figure 7.

At low voltages, anodic attack releases colloidal particals of insoluble oxy-salts from the anode metal. These submicron particals are propelled by the potential gradient toward any pinhole defects. Pinholes are observed as emerging trains of gaseous bubbles departing the defect site. Gas chromatographic analysis has identified these gas bubbles as hydrogen, probably due to the decomposition of the passivation material. At higher voltages, the insoluble salts accumulate on the surface of the passivation layer and cover areas up to one hundred diameters larger than those of the original defect. This "decoration" of the defect sites allows excellent microphotography of the effects of the dielectric breakdown caused by pinholes.

Table V shows the results of the pinhole testing of materials at various bias voltage levels. The pinhole count per square centimeter was taken after five minutes at the indicated voltage. This test profile was used to investigate the time variance of electric breakdown. The time element included with these tests caused the results to be somewhat higher than those reported by other researchers.

As Table V indicates, the most promising passivation

Table V
Pinhole Defects in Materials

Material	Application Process	Thickness (Angstroms)	Pinholes/cm2				
			10V	20V	30V	50V	100V
Silicon Dioxide	Steam Diffusion	4125	0	0	24	28	32
Silicon Dioxide	Dry Diffusion	1867	0	0	0	4	4
Silicon Dioxide	R-F Sputter	5400	4	28	68	68	68
Silicon Dioxide	CVD	6137	0	0	0	0	0
Silicon Dioxide	Low Temp CVD	5351	0	4	8	16	36
Silicon Nitride	R-F Sputter	5300	0	0	4	*	*
Silicon Nitride	Low Temp CVD	677	0	12	12	12	20
Silicon Nitride	Plasma	826	48	100	*	*	*
Silicon Nitride	Plasma	3832	200	*	*	*	*
Silicon Nitride	Plasma	4595	0	32	60	232	*
Aluminum Oxide	R-F Sputter	3400	12	24	44	128	*
8% PSG	Low Temp CVD	6422	0	0	0	0	4
Oxide + Polyimide	Dry Diff + Spin	1887	0	0	0	0	12

* pinholes were uncountable

materials appear to be high quality CVD silicon oxide, phosphosilicate glass (PSG), and the double layer of silicon dioxide and polyimide. These results are consistant with other research findings. The only unusual result was the large number of pinholes found in the plasma nitride layer. Since thin passivation layers contain more pinholes than thicker layers (Ref 41:1095), the 826 angstrom nitride sample was expected to have a substantial number of pinholes. However, Kern reports the pinhole density in a 5,000 angstrom layer of nitride is typically less than one per centimeter (Ref 23:35). In the 3,832 and the 4,595 angstrom nitride samples, there were so many pinholes that counting was impossible. One possible explanation may be that these samples were of low quality, as indicated by a typical refractive index of 1.88 rather than 2.0. As the quality of plasma nitride improves, the number of pinholes should drastically decrease.

IONIC DRIFT

A second form of instablity in passivating materials is due to ionic drift under the influence of an electric field. This problem could be eliminated if perfect insulators were available. However, all known materials are less than perfect insulators because they contain local imperfections within the crystal lattice that allow ionic contaminants to drift between interstitial sites within the material.

Sodium is one of the most difficult ionic contaminants to control because its high abundance in nature insures a

random distribution of sodium throughout a given material. In a static thermal-electric environment, there is insufficient activation energy to cause ionic drift of sodium contamination. As sufficient thermal or electrical energy is applied, sodium ions begin to migrate through the passivating material. The amount of drift is directly proportional to the number of mobile ions and their mobility (Ref 22:71).

Excluding external contamination sources, the number of mobile ions within a passivation layer is constant; therefore, the amount of ion drift in a specific sample is only a function of ion mobility. The activation energy necessary to cause ion drift must be sufficient to break the ionic sodium compound bond and then overcome the resistivity of the passivating material.

A common method of testing ionic drift within materials is to construct a capacitor test wafer that can be temperature-voltage biased to provide the necessary activation energy to cause ion mobility. Changes in the capacitor interface between the substrate and the passivation layer can then be recorded using the Capacitance-Voltage techniques discussed in the next section.

CAPACITANCE-VOLTAGE MEASUREMENTS

Passivation samples of various thickness were sandwiched between a 13 mil silicon substrate and a series of aluminum CVD dots. In future passivation research, smoother C-V curves can be obtained by applying a layer of CVD aluminum on the reverse surface of the silicon wafer. Total capacitance of

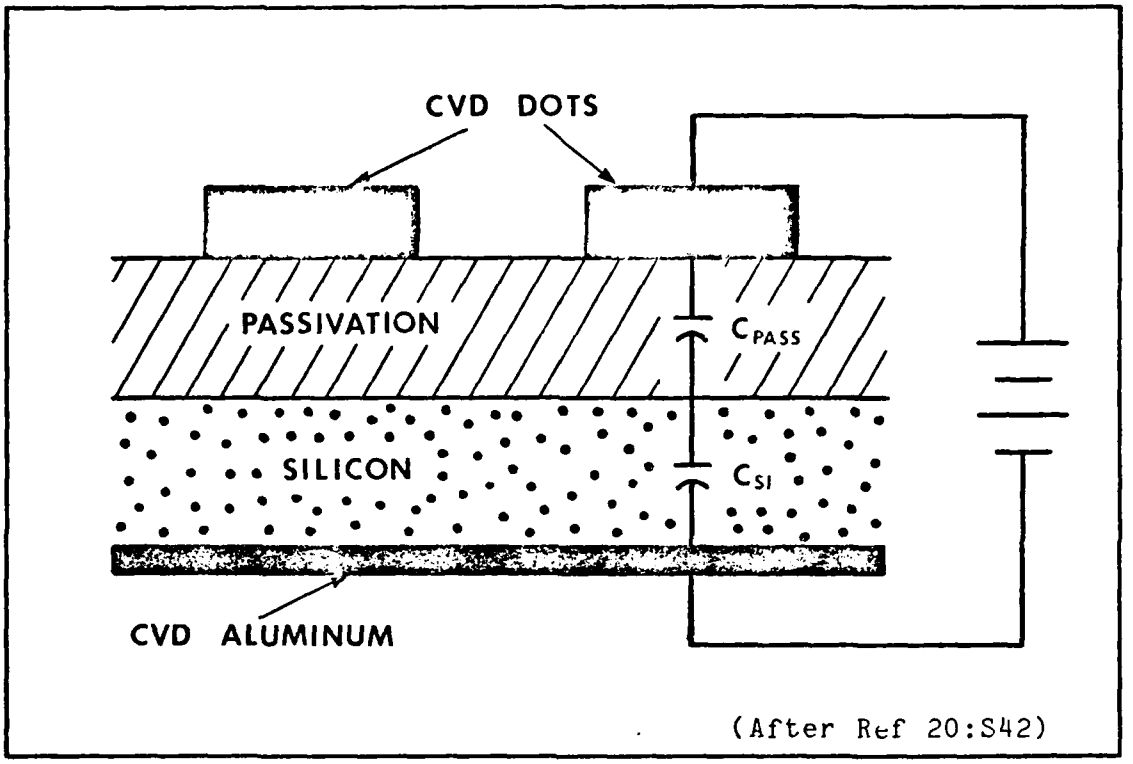


Figure 8: Equivalent Circuit for MIS Capacitance

the test wafer is the series capacitance of the silicon combined with the capacitance of the passivating material. An equivalent circuit of this network is superimposed over a cross-section of the Metal-Insulator-Silicon (MIS) capacitor shown in Figure 9.

A temperature-voltage aging process provides the activation energy to free the sodium ions and the bias to direct the ions in a specified direction. As mobile sodium ions drift through a passivating material, they begin to accumulate at the interfaces within the capacitor network (Ref 37:1375). A positive bias causes the sodium ions to migrate toward the silicon-passivation interface, where they induce an image charge in the silicon as shown in Figure 9a. A negative bias

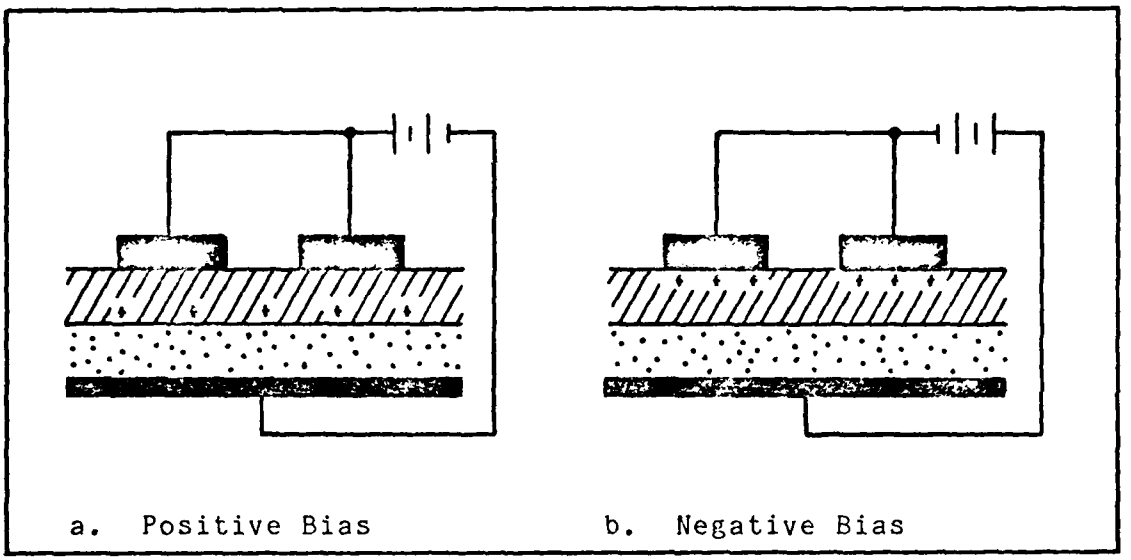


Figure 9: Electrical Effects of Mobile Ions

propels the ions toward the metal-passivation interface, causing an image charge primarily on the metal layer as shown in Figure 9b (Ref 20:S46).

The MIS capacitance is determined by applying a DC electric field between the CVD dots and the aluminum layer, thus setting the value of the silicon capacitance. A small-amplitude, 1 megahertz AC signal is then superimposed on the DC bias, giving rise to a differiental capacitance in the silicon space charge region (Ref 20:S42). The differiental capacitance, as a function of the applied DC field, can now be recorded as a Capacitance-Voltage (C-V) plot on an X-Y recorder.

A number of electrical and physical properties of materials can be determined from the analysis of the C-V curves obtained using this technique. The only property of concern in this study, is the evaluation of mobile ion density.

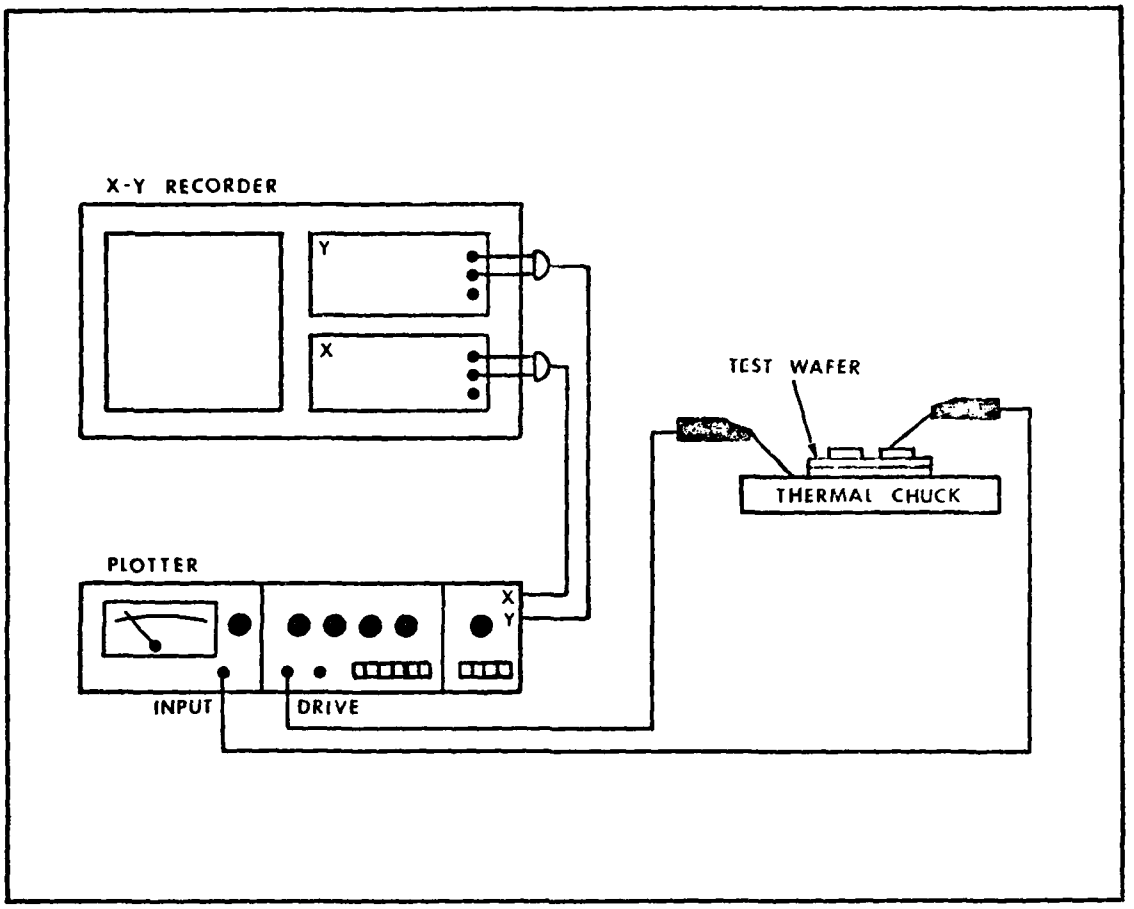


Figure 10: C-V Equipment Connections

Reference 42 contains a discussion of additional C-V analysis techniques.

CAPACITANCE-VOLTAGE TEST PROCEDURE

A Princeton Applied Research Model 410 C-V Plotter was connected to a test wafer as shown in Figure 10. Photoelectric effects of the test wafers necessitated covering the test stand with a light-impermeable shield prior to recording any C-V curves. The temperature-voltage aging profile used in this study consisted of the following steps:

1) Measure the room temperature C-V curve (Static Curve).

2) Apply a 30 volt positive bias.

3) Raise the temperature to 300 C and hold for 5 minutes.

4) Remove the voltage bias and cool to room temperature.*

5) Measure the positive bias C-V curve.

6) Apply a 30 volt negative bias.

7) Raise temperature to 300 C and hold for 5 minutes.

8) Remove the voltage bias and cool to room temperature.*

9) Measure the negative bias C-V curve.

10) Repeat steps 2-9 after evaporating saline solution over the CVD aluminum dot surface of the test wafer.

* A normal profile would maintain the bias during the cooling cycle; however, equipment limitations prevented this procedure. The process used in this step may have caused distortions in the C-V curves.

CAPACITANCE-VOLTAGE CURVE ANALYSIS

A perfect insulator would have absolutely no shift due to temperature-voltage aging, because it would effectively prevent ion mobility. Since there are no perfect insulators, any shift in the C-V curves due to temperature-voltage aging, is a function of the movement of ions contained within the passivaton material. The profile outlined in the last section results in a series of five curves for each passivation material. Ideally, the first three curves, called the Ambient

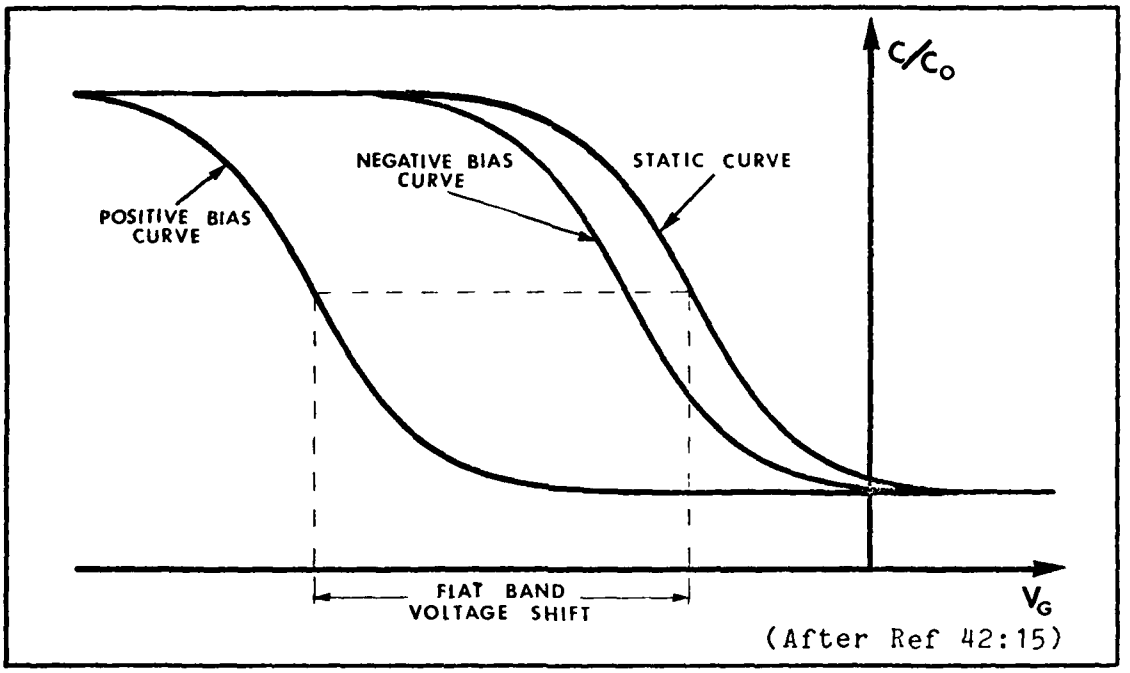


Figure 11: Ideal C-V Curves

Air Curves, should be similar to the curves in Figure 11. An explanation for the shift in the C-V curves is based on the motion of positive charges from the metal electrode migrating through the insulator and accumulating at the silicon surface. If a positive bias shifts the C-V curve to the left, it would indicate that a negative ion was the cause of the contamination. A shift to the right would indicate the presence of a positive ion contaminant. During the analysis of a particular passivation sample, curves with the least shift due to aging are the most interesting.

Under the influence of a negative bias, the curve should shift back towards the Static Curve. The difference between the Static Curve and the Negative Bias Curve is a function of ion trapping at the silicon interface state (Ref 42:16).

This property of ion mobility is not of primary importance to this study and will not be discussed further.

The flatband voltage shift, indicated graphically where the C-V curve changes from a positive to a negative curvature, is a direct measure of the field enhancement at the silicon-passivation interface and can be used to determine ion density. Formulas for calculating the actual numerical value of ion density, are found in References 21, 42, and 43. In this study, only the relative ion density, indicated by the difference between flatband voltage shifts, is important.

The Positive Bias Ambient Air Curve gives an indication of the contamination level due to the fabrication processes. The Positive Bias Concentrated Saline Curve shows the response of the passivation layer to external contamination. The difference between these two curves is an indication of the alkali barrier potential of the passivation layer. Appendix B is a catalog of the family of C-V curves for commonly used insulating films. Results of these curves are tabulated in Table VI.

Correlation of the best results from the pinhole tests and the best results from the C-V curves is shown in Table VII. The two most promising passivation materials for coating implantable microelectric devices are the 8% PSG sample and the double layer of silicon dioxide and polyimide. Although the Dry Diffusion silicon dioxide also appears to be a good passivation layer, the 1100 C temperature required to grow the oxide would cause thermal cracking of the metalization layers. This is the main reason silicon dioxide is used only

as an interior mask rather than a final passivation layer.

An interesting observation is the extremely good alkali protection provided by the plasma silicon nitride, even though it has the highest pinhole count. One possible explanation is the "gettering", or trapping effect of silicon nitride, that effectively prevents alkali ion drift (Ref 21:22). As the quality of plasma nitride improves, the passivation properties will also improve.

The Air Force Avionics Laboritory is experimenting with various techniques for obtaining a uniform density, high quality silicon nitride by using a low-temperature plasma nitride deposition process. Weekly results have shown that the quality of plasma nitride obtained from their Technics Planar Etch II have steadily improved. This improvement is directly proportional to the knowledge gained about the correct gas flows, temperatures, and pressures used to deposit nitride. Once this deposition process is perfected, it could become the solution to the implanted device passivation problem. Since plasma deposited silicon nitride represents such a good opportunity for obtaining a high-quality, easily deposited, easily etched, saline protection barrier, continued testing of plasma nitride is strongly recommended.

TABLE VI
C-V Curve Analysis

Material	Application Process	Thickness Angstroms	Δ V Ambient	Δ V Saline	Δ V Difference
Silicon Dioxide	Steam Diffusion	4125	+ 27V	+27V	0V
Silicon Dioxide	Dry Diffusion	1867	+ 35V	+37V	2V
Silicon Dioxide	R-F Sputter	5400	*	*	*
Silicon Dioxide	CVD	6132	+ 35V	+ 2V	33V
Silicon Dioxide	Low Temp CVD	5351	+ 17V	+20V	3V
Silicon Nitride	R-F Sputter	5300	-110V	+ 8V	118V
Silicon Nitride	Low Temp CVD	677	+ 23V	+64V	41V
Silicon Nitride	Plasma	826	+ 12V	+13V	1V
Silicon Nitride	Plasma	3832	+ 90V	+50V	40V
Silicon Nitride	Plasma	4595	- 14V	-23V	9V
Aluminum Oxide	R-F Sputter	3400	- 7V	- 8V	1V
8% PSG	Low Temp CVD	6422	+ 16V	+15V	1V
Oxide + Polyimide	Dry Diffusion	1885	- 27V	-28V	1V

* C-V curves for this sample were completely flat; therefore, no data can be shown.

TABLE VII
Passivation Results

Material	Application Process	Thickness Angstroms	50V Pinholes	C-V ΔV Difference
Silicon Dioxide	Steam Diffusion	4125	28	0V
Silicon Dioxide	Dry Diffusion	1867	4	2V
Silicon Dioxide	CVD	6137	0	33V
Silicon Dioxide	Low Temp CVD	5351	16	3V
Silicon Nitride	Plasma	826	*	1V
Silicon Nitride	Plasma	4595	232	9V
Aluminum Oxide	R-F Sputter	3400	128	1V
8% PSG	Low Temp CVD	6422	0	1V
Oxide + Polyimide	Dry Diffusion	1887	0	1V

* pinholes were uncountable

IV. EXTERNAL DRIVE CIRCUIT

REDESIGN DECISION

Multiplexing features of the AFIT Multielectrode Array were designed into the device from the beginning. However, the control signals necessary to drive the multiplexer are contained in an external drive circuit. Several experiments planned for the implantation phase of this research require synchronous multiplexing of at least two AFIT Arrays positioned in different areas of the visual cortex. Unfortunately, the Fitzgerald drive circuit was built to test only a single array.

This conflict presented two alternative options. A second drive circuit exactly like the Fitzgerald circuit could be built; or a new circuit capable of synchronously driving two arrays at the same time could be designed. The Fitzgerald circuit was built on the premise that the array must be X-Y addressed, but after the circuit was completed, it was realized that only the row leads required multiplexing. The unnecessary column multiplexing components greatly influenced the decision to redesign the drive circuitry.

DESIGN CRITERIA

Complementary Metal Oxide Semiconductor (CMOS) devices are the components of choice for designing the drive circuit for the following five primary reasons (Ref 44:209):

1) Low power dissipation (less than 10mW per active gate).

2) Small propagation delays (25 nanoseconds per gate).

3) Low noise immunity.

4) Fast operating speeds (equal or greater than 5 megahertz).

5) Operation possible at various supply voltage levels.

Using battery power eliminates most of the 60 cycle hum caused by AC power line sources. Throughout the drive circuit, V_{DD} is connected to +6 volts and V_{SS} is connected to -6 volts. Circuit ground is the center tap of these two voltages. The reason for this convention will become apparent in the following discussion of the design process.

The drive circuit has three primary objectives. First, it must supply a ground signal to three row leads, producing the "OFF" state in all the JFET's on those rows. Second, it must supply a pinchoff voltage of approximately -1.5 volts to the fourth row lead producing the "ON" state in the JFET's on this row. Third, it must cycle the "ON" state sequentially through all the rows.

CONTROL DESIGN

The first two objectives are accomplished by using a CMOS MC14016B Quad Analog Switch (Ref 45:5-45) in the configuration shown in Figure 12.

When the control signal is at a logic "1", the bilateral switch is closed, creating a typically 300 ohm resistance across the switch. For all practical purposes, this is a short between the switch input signal (ground) and the gate of

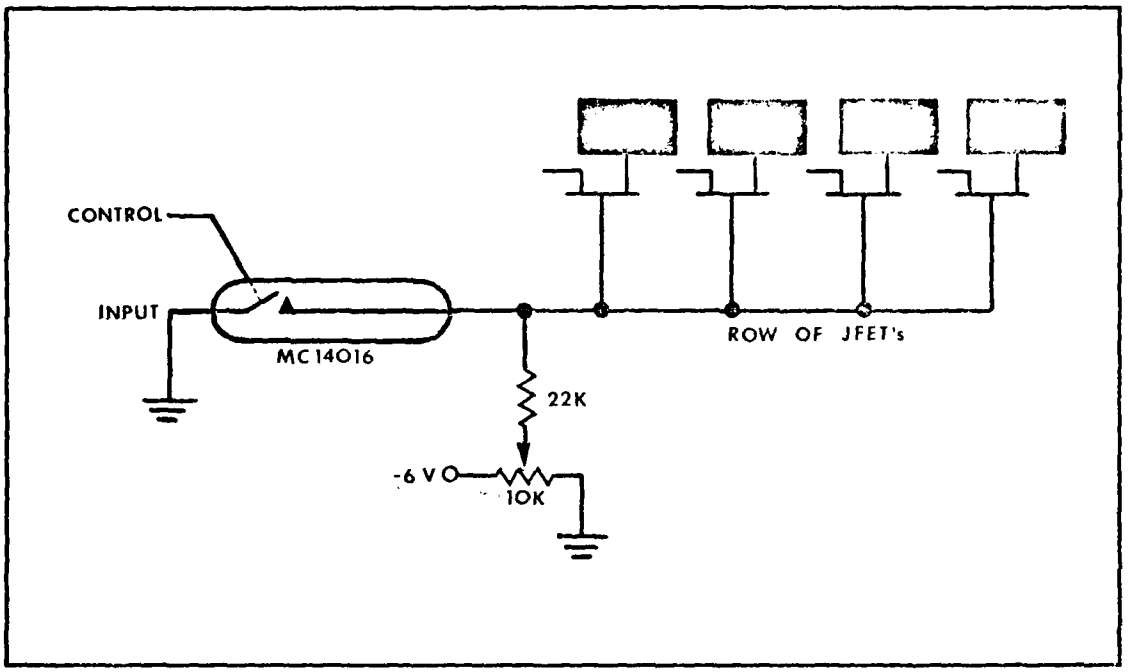


Figure 12: Gate Control Signal

all the JFET's on that row. A ground potential at the gate produces the "ON" state, causing signals sensed by the electrodes to pass directly to the drain where they can be recorded.

When the control signal is at a logic "0", the bilateral switch is open, creating a typically 1000 M ohm resistance across the switch. Essentially, this is an open circuit that allows the pinchoff voltage selected by the variable 10 K ohm resistor to be applied to the row lead. The pinchoff voltage closes the source-drain channel, causing the row to change to the "OFF" state. This isolates the signals sensed by the source electrode from the drain; therefore, nothing can be recorded.

Each MC14016 has four analog switches; therefore, a single device can control an entire 4 X 4 array. Additional

MC14016's can be added if the size of the array is increased.

LOGIC DESIGN

The third objective of the drive circuit, multiplexing, is accomplished through the use of a CMOS CD4029A Presettable Up/Down Counter (Ref 46:452). This four-bit binary counter has two modes of operation. It can either be manually set using the JAM INPUTS, or it can be automatically sequenced by an external clocking device. Both of these modes are useful in the application presented here.

In the manual mode, any four-bit output sequence can be set. This mode is useful for testing and for examining the response of a specific row. In the automatic mode, the four-bit output is advanced one count at each positive transistion of the clock. This is the normal mode of operation during an actual implant.

Device fan-out for the CD4029 could probably drive two 4 X 4 arrays; however, as the size of the array increases, this would no longer be true. This problem is avoided by constructing two independent branches for the drive circuit, linked together by a common clock signal. Each branch is capable of controlling one array. Synchronization of these branches in the automatic mode is accomplished by manually setting the starting point of each branch to the same value, then switching to the automatic mode of operation.

In larger arrays, it will be necessary to use the full range of the 16 count binary output of the CD4029 to provide the logic needed for the MC14016 Analog Switch. The 4 X 4

array cnly requires a portion of this capability, so the excess logic states must be combined as shown in Table VIII. The logic circuits necessary to implement this truth table are shown in Figure 13. CMOS CD4001A Quad NOR Gates (Ref 46:392) are used for the NOR operation. Since a CMOS inverter is not available, a CMOS MC14502B Strobed Hex Inverter (Ref 45:5-235) is used for the negation operation. Tying the INHIBIT pin 12 and the OUTPUT DISABLE pin 4 to V_{SS}, converts this 3-state device into a normal inverter.

TABLE VIII
Counter Output Truth Table

Binary Output					Row Control Signal			
Q4	Q3	Q2	Q1		R1	R2	R3	R4
0	0	0	0		1	0	0	0
0	0	0	1		1	0	0	0
0	0	1	0		1	0	0	0
0	0	1	1		1	0	0	0
0	1	0	0		0	1	0	0
0	1	0	1		0	1	0	0
0	1	1	0		0	1	0	0
0	1	1	1		0	1	0	0
1	0	0	0		0	0	1	0
1	0	0	1		0	0	1	0
1	0	1	0		0	0	1	0
1	0	1	1		0	0	1	0
1	1	0	0		0	0	0	1
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1	1	1	0		0	0	0	1
1	1	1	1		0	0	0	1

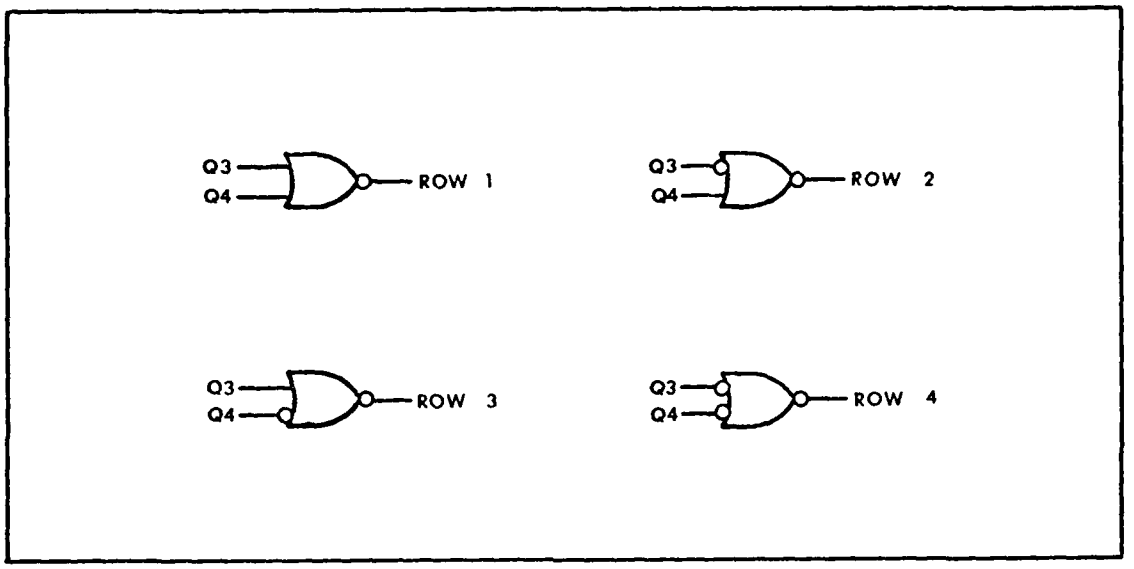

Figure 13: Logic Design

CLOCK CIRCUIT

An internal, battery-operated clock is needed to drive the CD4029 Counter. A CMOS clock generator was not available, so a TTL SN74LS124 Dual Voltage-Controlled Oscillator (Ref 47:7-123) can be interfaced into the CMOS network, as shown in Figure 14. The conversion from TTL to CMOS requires the establishment of a few operating conventions:

1) Device ground (pin 8) is connected to the drive circuit -6 volt supply.

2) The device supply voltage (pin 16) is connected to a 1 K trim pot, so that the operating voltage between pin 8 and pin 16 can be adjusted to maintain 7 volts.

3) The ground shown in Figure 15 is the drive circuit ground (midpoint of +6 and -6).

This device contains two independent oscillators; however, the two supply inputs (pins 15 and 16) are for two separate

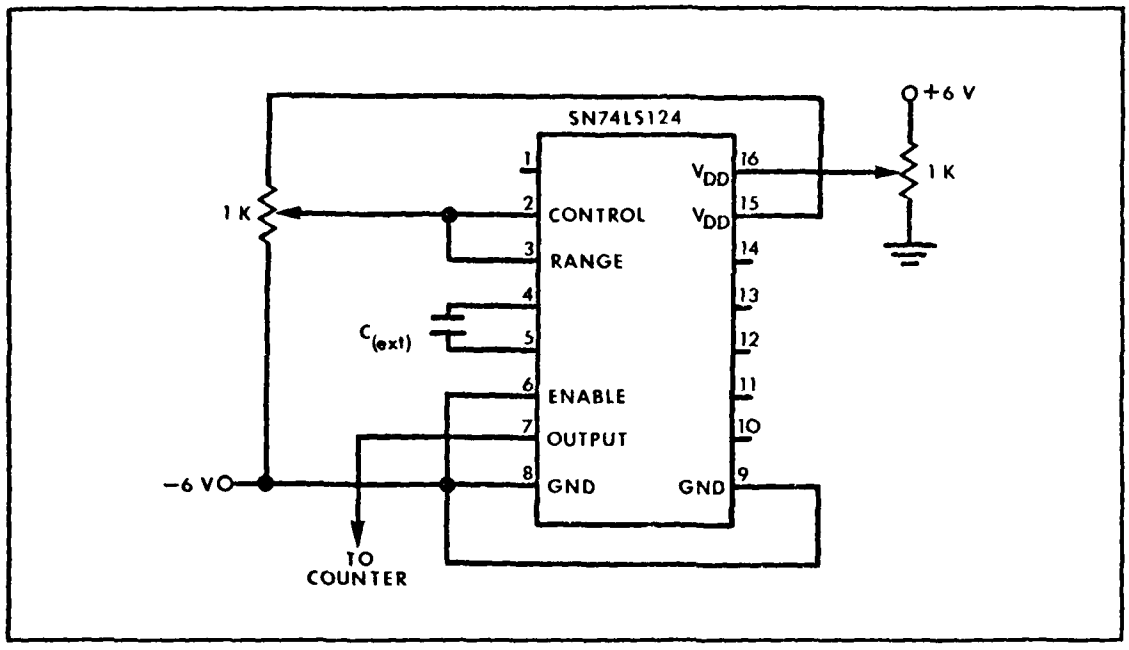

Figure 14: Clock Circuit

functions within each oscillator and must both be connected to a voltage supply before either oscillator will operate. This also applies to the two device grounds (pins 8 and 9).

The output oscillation frequency is approximated by the following formula for an SN74LS124:

$$f\ (out) = \frac{0.0001}{C\ (ext)} \qquad \text{(Ref 47:7-123)} \qquad (1)$$

where:

f (out) = output frequency

C (ext) = external capacitance in farads

This external capacitance is easily changed as needed to obtain the desired output frequency. A 1000 picofarad capa-

citor provides the 1600 Hertz Nyquist sampling rate required by a 4 X 4 array. Fine tuning of the output frequency is accomplished by adjusting the 1 K variable resistor connected to the Frequency Control (pin 2) and the Frequency Range (pin 3).

ROW MONITOR LIGHT

When using the manual mode it is convenient to have a visual indication of which row is in the "ON" state. This requires converting a TTL HP 5082 7340 Hexidecimal Indicator into a useful component for a CMOS circuit. The wiring diagram is shown in Figure 15. The diodes and pull-up resistors are used to clip off the negative switching pulse from the Counter. Isolation from negative voltages is mandatory to prevent damage to the Hexidecimal Indicator.

CIRCUIT AND TIMING DIAGRAMS

Additional components needed to complete the drive circuit are:

1) Automatic/Manual switch
2) Manual set switches
3) Input bus structure
4) Voltage supply (two 6 volt batteries)
5) 10 K load resistors for the column leads

The integration of all the components for a single branch of the drive circuit is shown in Figure 16. "R" is the control logic signal sent to a particular row, "C" is the input from

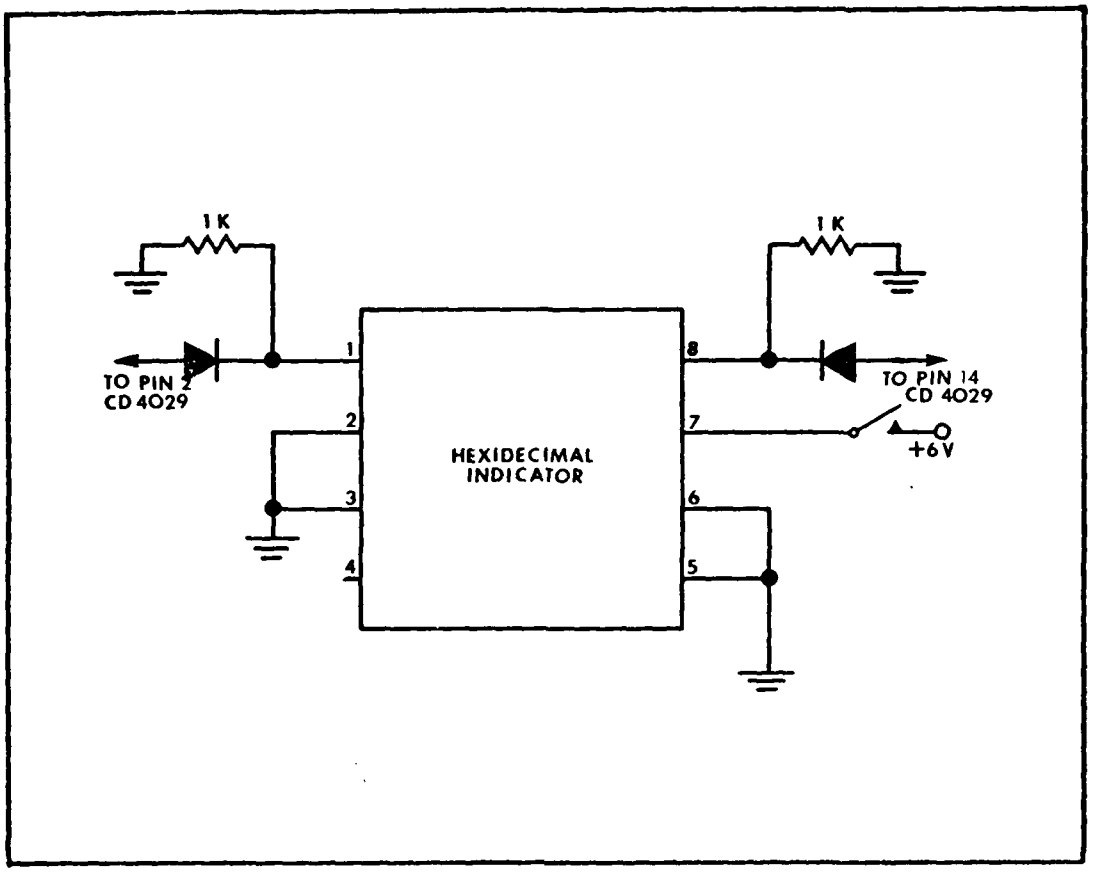

Figure 15: Row Monitor Wiring Diagram

a column, and "B" is the output to a bioamplifier. The second branch duplicates this portion of the drive circuit; therefore, is not shown. The only connection between the two branches is through the common clock source. The component layout of the complete wirewrap Drive Circuit is shown in Figure 17. Testing of this drive circuit produced the timing diagram shown in Figure 18. The four control logic timing diagrams are the control signals for the MC14016 Analog Switches. The four row input timing diagrams are the outputs from the Analog Switches.

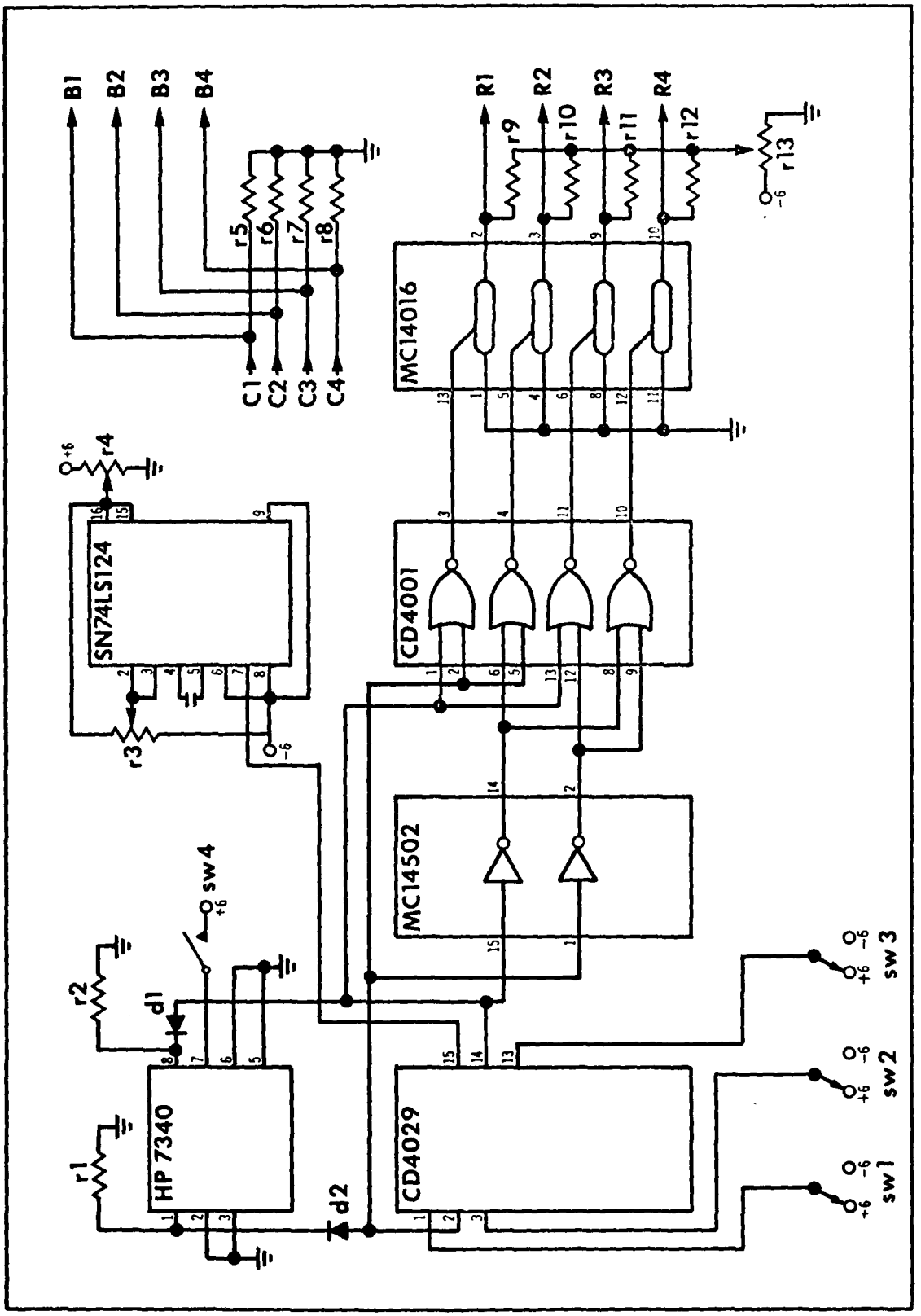

Figure 16: Drive Circuit Wiring Schematic

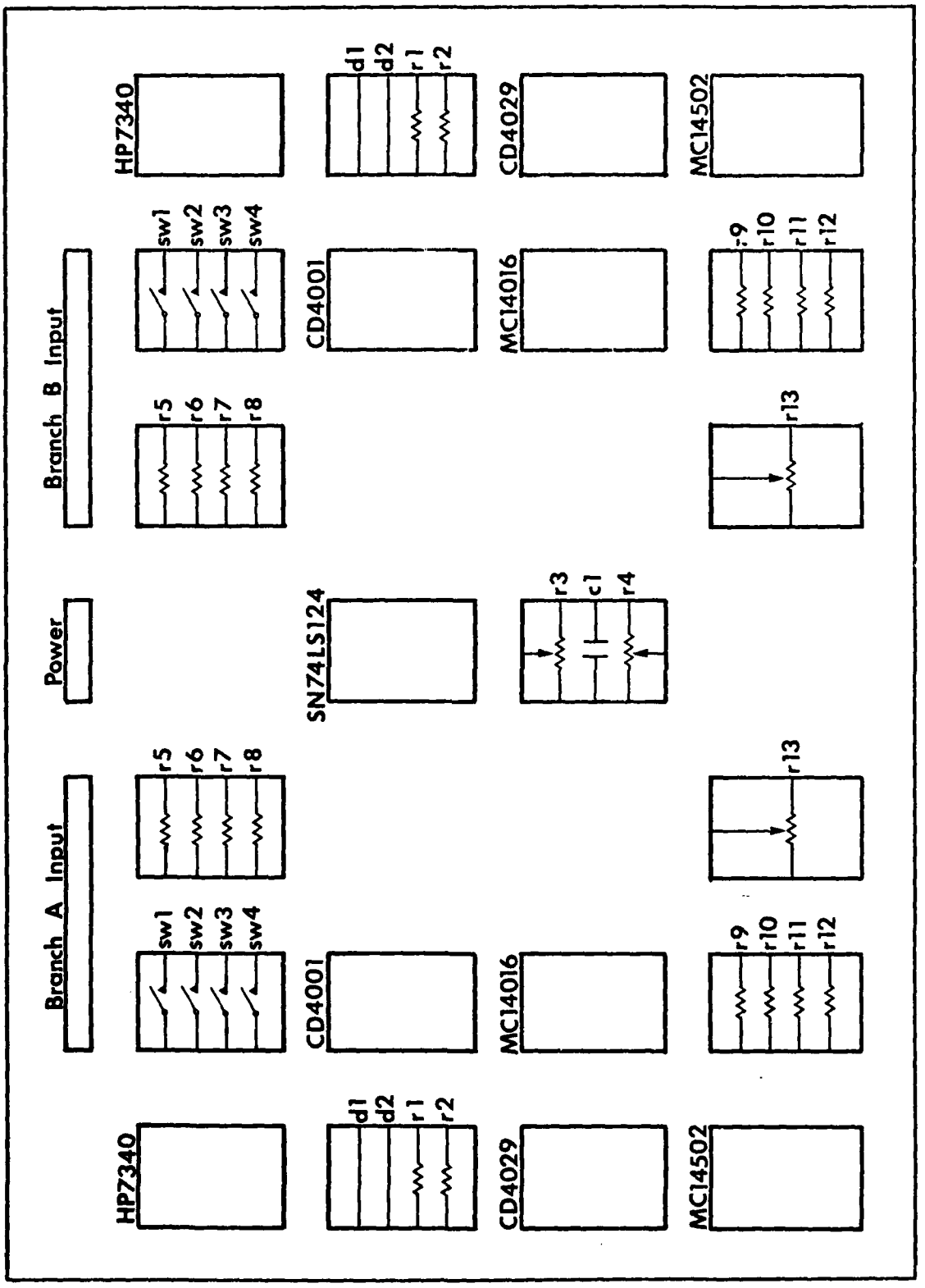

Figure 17: Component Layout

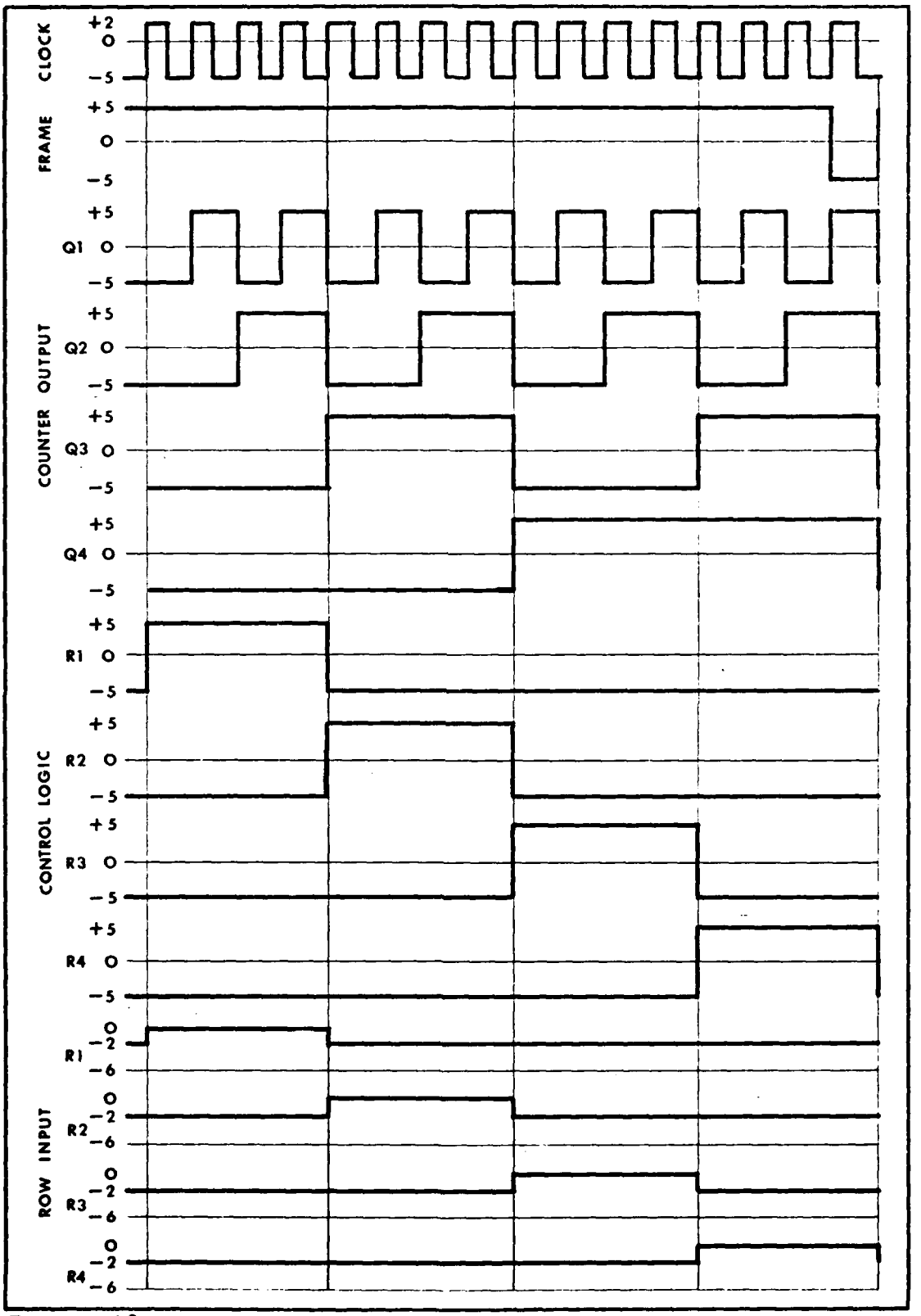

Figure 18: Drive Circuit Timing Diagram

V. SYSTEM INTEGRATION

EQUIPMENT REQUIREMENTS

The equipment needed to operationally test an AFIT Multielectrode Array is listed below:

1) One AFIT Multielectrode Array
2) Four Wavetek Model 148 Oscillators
3) One Multiplexer Drive Circuit
4) Four Princeton Applied Research Model 113 Biomedical Amplifiers
5) One Ampex Model FR 1300 FM Tape Recorder
6) One Microscope
7) One Needle Probe Assembly

The equipment is connected via shielded cable, as shown in Figure 19. Integration of this equipment is described sequentially from the initiation of the bioelectric signal until the signal is finally recorded on the FM recorder.

DeMott has reported that EEG signal strengths on the surface of the visual cortex vary between 200-500 microvolts (Ref 9:26). The anticipated frequency bandwidth of these signals should be between 0 and 50 Hertz. The Wavetek Model 148 Oscillator is capable of producing various low distortion wave shapes within this signal strength/bandwidth range without the use of external voltage divider networks.

A five-station needle probe assembly was constructed to provide a stable platform for the Array. Each of the five stations contains a 7-mil diameter needle probe mounted on an

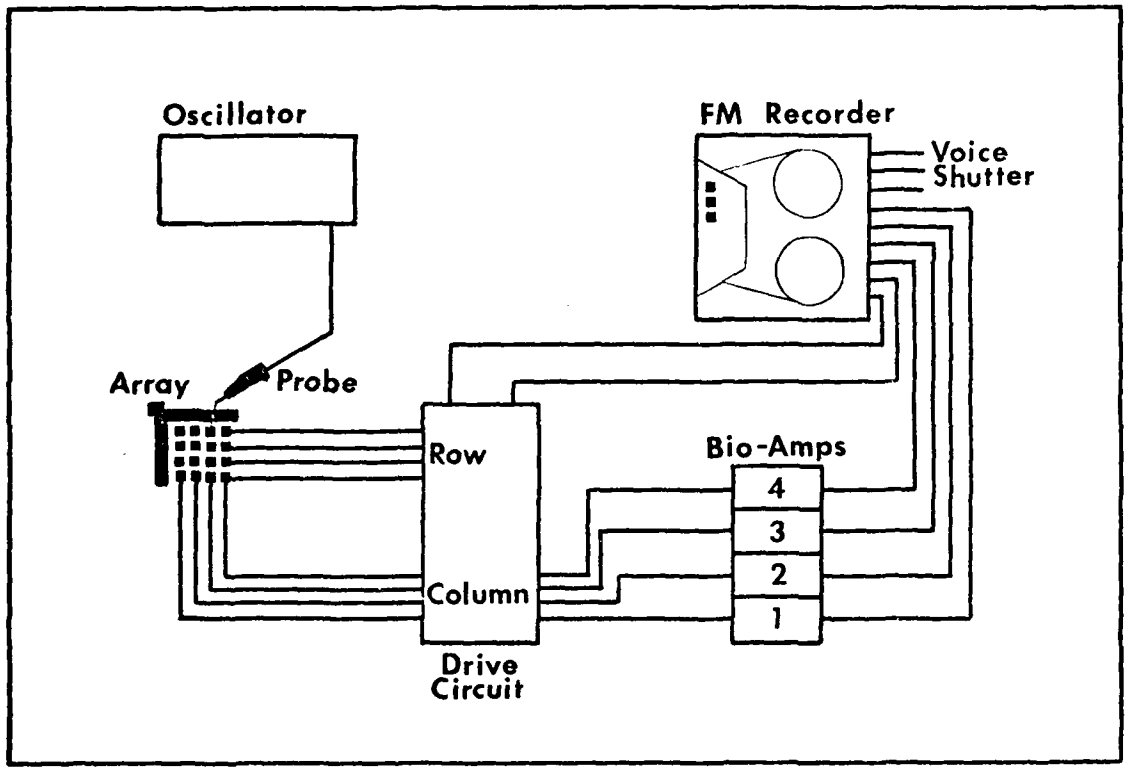

Figure 19: System Equipment Integration

adjustable 3-axis framework. A microscope is required to accurately position four of the needles onto four separate electrodes on an array. The output of a Wavetek oscillator is connected to each of these probes, so that a pseudo-bioelectric signal can be injected onto the electrode. The fifth needle probe can be inserted into the array ground plane.

The array row and column leads are then connected to the multiplexer drive circuit. The signal developed across each column load resistor is amplified by a separate low-noise PAR-113 amplifier.

Following amplification, the signals are recorded on four separate channels of the FM recorder. Each channel of

the recorder becomes a patchwork of all the signals received from all the electrodes on a specified column. Because of this layered recording structure, it is necessary to record the frame pulse and the clock pulse generated by the drive circuit. The frame pulse is a benchmark produced on the last pulse of a 16-count time slice. Along any column-lead channel of the recorder, the signal following the frame pulse is from the first electrode in the specified column.

Other recorder channel inputs needed during an actual implant are:

1) A voice input to verbally record procedures, status, stimulus, and animal response.

2) An input to signal onset/cessation of a stimulus. This could be from an electronic shutter connected to a visual image projector or an equivlent signal from a CRT stimulus.

3) Four column inputs from a second array, if simultaneously recording the response of two separate areas of the visual cortex.

AMBIENT AIR TESTS

The purpose of testing the array in ambient air is to insure proper operation of all the equipment before subjecting the array to the sodium enriched environment experienced during an implant. During the test cycle performed in this study, the bioamplifier gain was set at 10. Amplitude of the input signal was varied from 0 to 1 volts over a frequency range from 0 to 10,000 Hertz. In all cases, the output signal duplicated the input signal with very little distortion. The major cause of spurious inputs was due to excessively

long lead wires from the array to the bioamplifier. Figure 20 is a timing diagram for a typical 1000 Hertz sampling rate test. The amplitude of the input signal was 5 millivolts; however, a 500 cps frequency was used to highlight the signal reproduction for the graphic display shown in Figure 20.

The spike at the leading and trailing edges of each time slice is well documented in other studies and is not strictly an anomaly of an AFIT JFET (Ref 19:224). When the analog data is later digitized and stored on a computer, it will be important to filter out the area surrounding these switching spikes. As the required sampling rate increases with the number of electrodes on an array, the distortions caused by this spike become a limiting design factor. One method of overcoming this drawback is to implant several smaller arrays, rather than a single large array. Smaller arrays have the added benefit of more easily conforming to the contours of the cortex.

SALINE TESTS: POLYIMIDE

Insufficient time prevented the normal passivation of an AFIT Array and then opening contact windows to expose the electrodes. This situation could have prevented the saline testing of an AFIT Array covered with a passivation layer. A solution to this problem required taking a step backwards into the "Wire-bundle" phase of neurocortical research. The following paragraphs discribe how this was accomplished.

One inch strands of 0.0007 inch diameter gold wire were ultrasonically bonded to each electrode of a standard AFIT

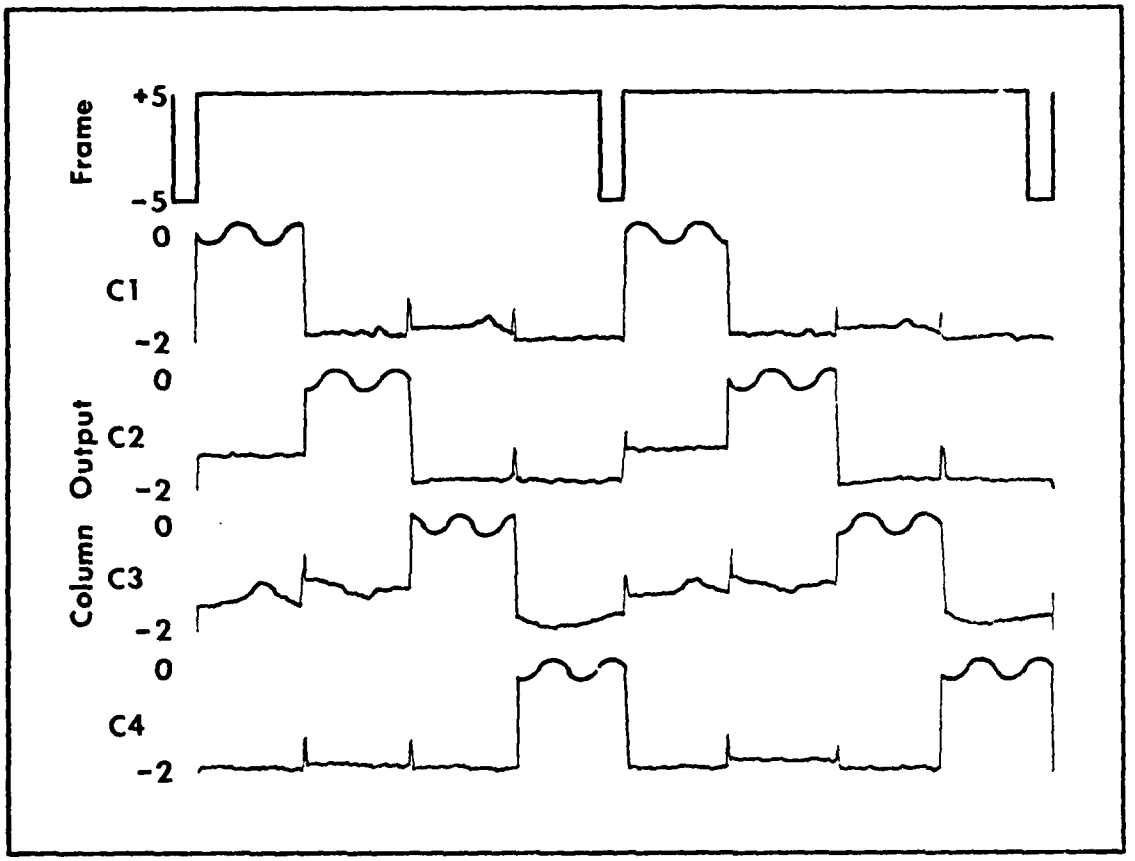

Figure 20: Timing Diagram

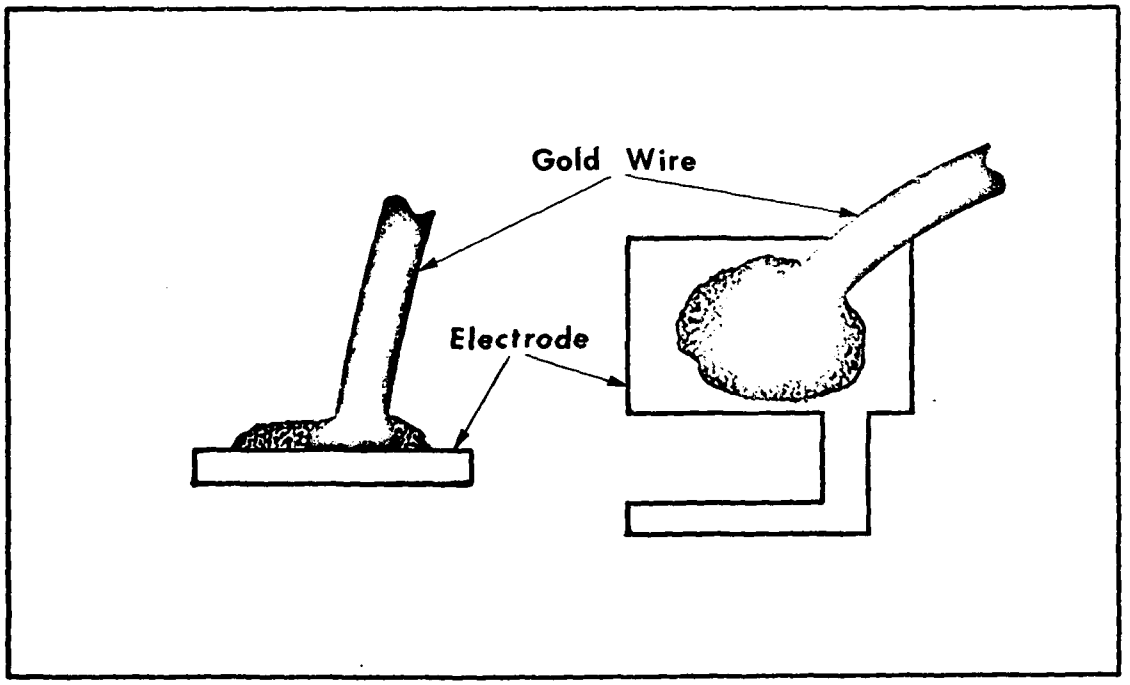

Figure 21: Wire Bonded Electrode

Array as shown in Figure 21. The wires were then separated and aligned perpendicular to the surface of the array. Adhesion promotor and then Polyimide (PI-2545) was spun-on at 1500 rpm for 15 seconds. Even at this spin speed, the slowest available, the centrifugal force tended to pull the thin wire strands outward. Fortunately, visual inspection confirmed that the wires maintained their relative position. The array was then bake-cured at 160 degrees centigate for one hour. The gold wires were clipped parallel to the surface of the passivation layer exposing the electrodes. This procedure converts a photolithographic array into a 4 X 4 wire-bundle. The array was then mounted on the needle probe assembly for testing in ambient air. Due to a fabrication defect, the JFET's on the passivated array displayed only resistive curve tracer characteristics. The test profile was continued to analyze the sodium/moisture permeability of Polyimide passivation.

First, the array was subjected to a high relative humidity environment by covering the electrodes with deionized (DI) water. A curve tracer was used to display a family of resistive curves for the defective JFET. For test purposes, a 20-volt gate-source potential was used to bias the JFET. The curve tracer was continuously monitored for any indication of shift in the resistive curves for the device. After being in a saturated DI water environment for one hour, the device continued to display absolutely stable resistive curves. This indicates that Polyimide can effectively seal the circuit from moisture.

The next phase of the test cycle substituted saline solution for the DI water. The JFET showed stable resistive curves for the first 30 minutes. Then a brownish substance was observed floating on top of the saline. This was probably due to a chemical reaction between the saline and the Polyimide. This indicates that the Polyimide probably was not completely cured prior to the test. Longer cure times at higher temperatures may provide a more stable Polyimide passivation layer.

Shortly after the brown substance appeared, the resistive curves began a slow parallel shift in the negative direction. One hour and forty-five minutes into the test cycle, the device failed catastrophically. Primary failure points cluster around the row and column leads.

Although these tests are inconclusive, they do indicate that Polyimide has the capability to shield an array from the destructive effects of saline, if only for a short while. One hour and forty-five minutes is a drastic improvement over the 30-second time-to-failure reported by Fitzgerald (Ref 14:84). This length of time is sufficient to obtain at least a minimal amount of data during an actual implant. This could confirmation that the AFIT Multielectrode Array can record bioelectric signals emitted from the visual cortex of a living animal.

VI. CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

The conclusions based on this research are basically two-fold. First, the characteristics of the AFIT JFET are not sufficiently uniform to determine a standard family of curves for devices fabricated by the Tatman-Fitzgerald process. Regardless of the differences in the characteristic curves, the switching parameters required by this application are surprisingly uniform over a wide spectrum of devices; therefore, the basic design of the array is sufficient for detecting and recording bioelectric signals from the surface of the visual cortex. Testing of 134 AFIT JFET's (54 from Fitzgerald and 80 from this study) indicates that the values for R (on), R (off), V (pinchoff), and V (breakdown) are well within the design specifications.

The second conclusion is that there are two, possibly three passivation materials (8% PSG, the double layer of silicon dioxide and polyimide, and possibly silicon nitride) capable of adequately protecting an AFIT Array for the time interval required to record data from the visual cortex. The most important significance of the AFIT Array is that this data is time multiplexed allowing simultaneous monitoring of a large area of the visual cortex. So much data can be recorded from a single array, even a small 4 X 4 array, that proper analysis could consume a considerable time. The knowledge acquired by analyzing the data gathered from multiplexed

improving visual acuity.

RECOMMENDATIONS

The strongest recommendation I can present is to get the student out of the device manufacturing cycle. Fabrication of silicon devices requires highly skilled technicians to produce a reliable device that has guaranteed operating characteristics. Several commercial "Chip Foundries" specialize in producing small quantities of custom-designed integrated circuits. Current cost for n-channel, silicon gate wafers is approximately $130 to $400 per completed wafer for production runs of 50 wafers (Ref 48:18). Since nine arrays are fabricated on each two-inch wafer, this would provide 450 individual arrays for additional testing and implantation.

The second recommendation is for continued research of possible passivation materials. Toward the end of this research project, a quantity of teflon and paralene became available. Other researchers have produced good passivation results from these two materials (Ref 49:671). One or both of them may provide the alkali barrier needed to shield a chronically implanted device from the sodium ion. Other recommendations for further research include:

1) Convert the external drive circuit into a Large Scale Integrated (LSI) device (separately or on the same chip as the electrodes).

2) Design or purchase a small-size, low-wattage power source and R-F transmitter. Integration of the array, drive circuit, power source, and transmitter into a single implantable unit will allow long term chronic implants, without the associated fear of transcutaneous infection.

3) Define a comprehensive surgical protocol. This protocol must be approved by the Veterinary Sciences Division of the Air Force Aerospace Medical Research Laboratory before any surgical procedure can be performed.

4) Digitize the analog bioelectric signals recorded during an implant.

5) Design an analysis profile that can interpret the mass of data obtained during a recording session.

6) Perform a large number of implants on lower-order mammals (gain experience before a primate implant).

This is a particularly exciting period for neurocortical research because we are at the brink of significant discoveries about how the brain processes visual signals. The next step is the recording and analysis of the bioelectric signals produced by the mammalian visual system. The AFIT Multielectrode Array could become the tool necessary to gather this vital information.

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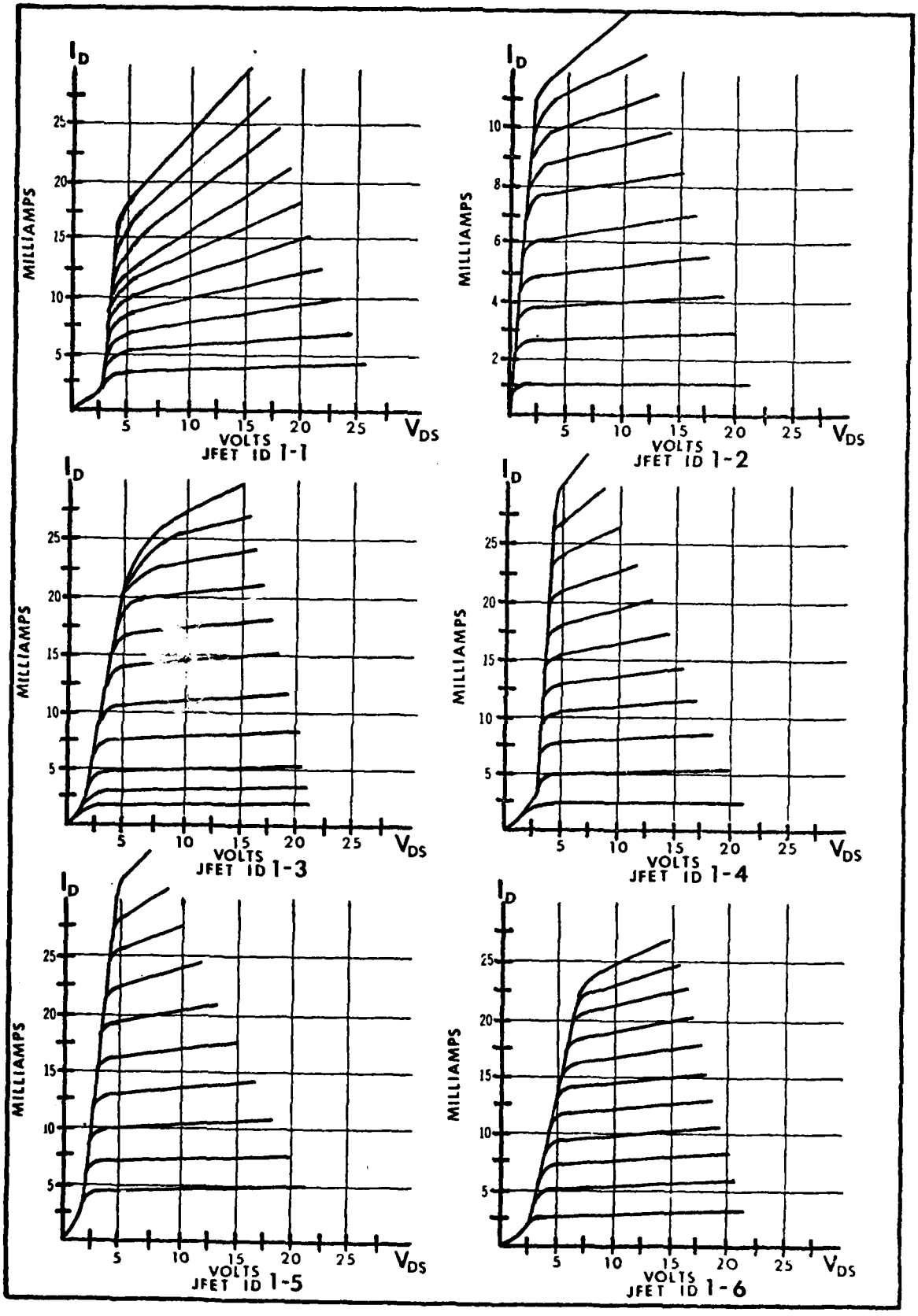
A. AFIT JFET CHARACTERISTIC CURVES

The family of characteristic curves contained in this appendix were obtained from a Tektronics Model 577-177 Curve Tracer. In all cases, the voltage step change between two adjacent V_{GS} lines is established at 0.5 volts. The format for JFET identification numbers is: Array number-JFET number.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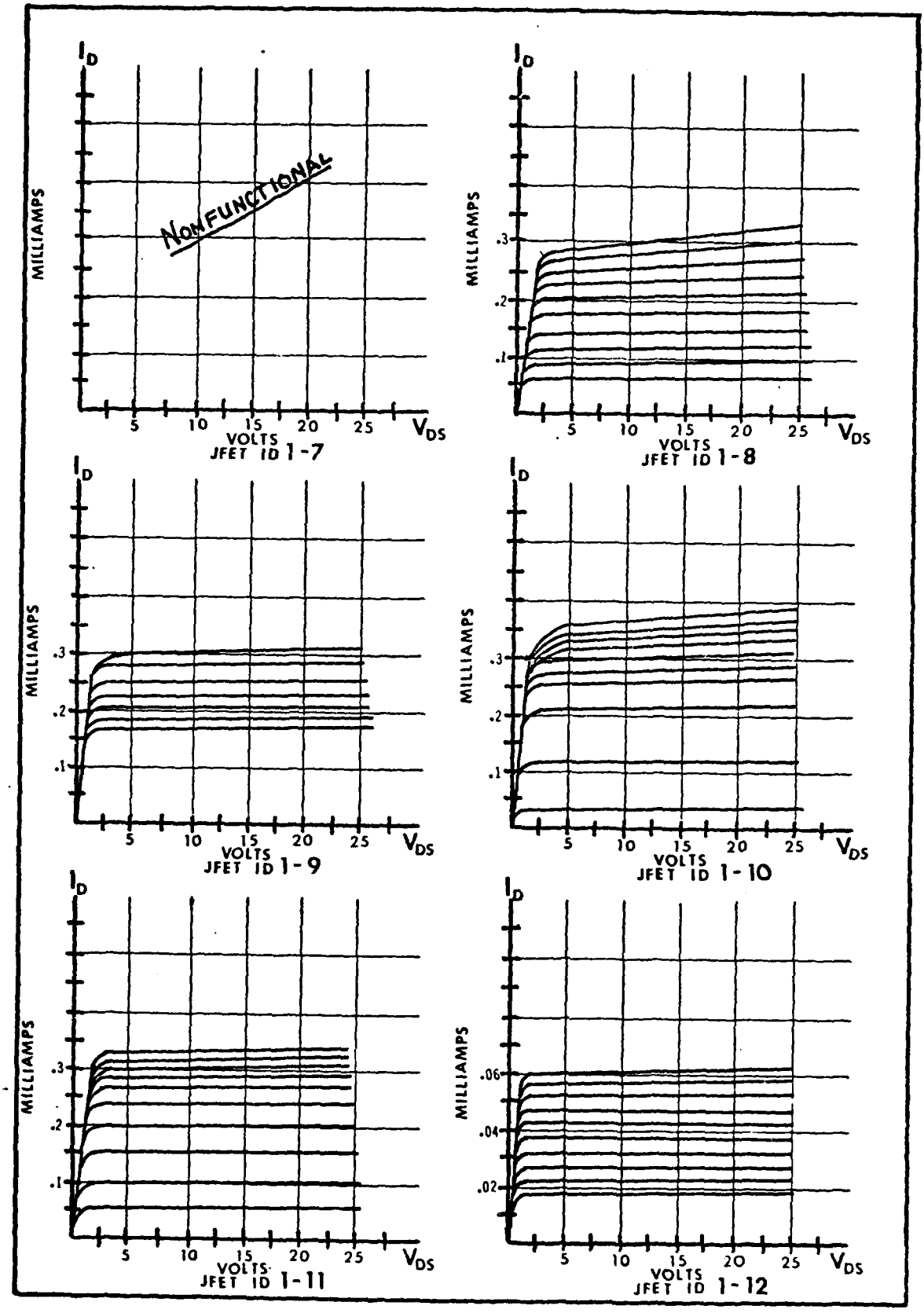
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.1
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VOLTS
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.3
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.1
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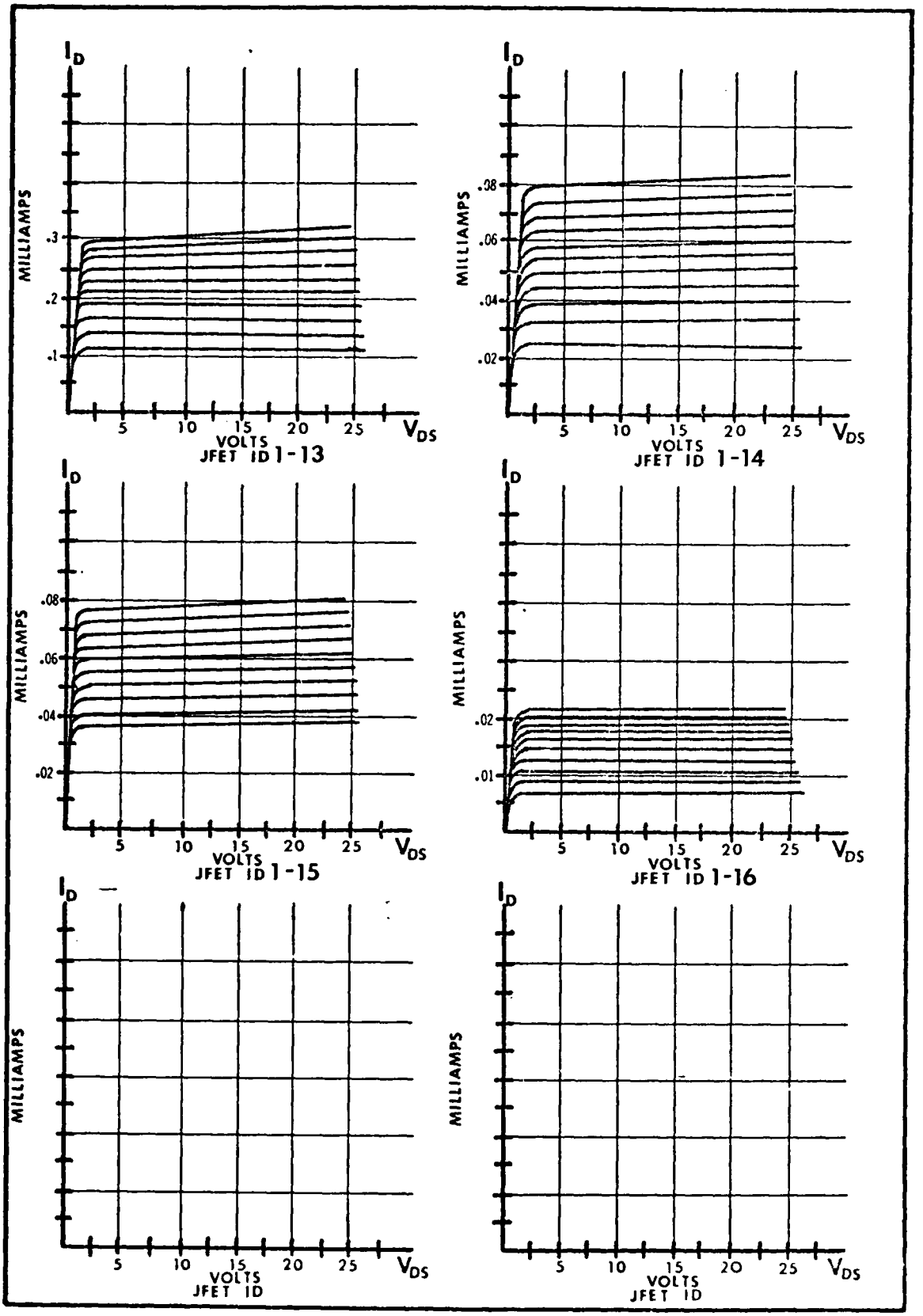
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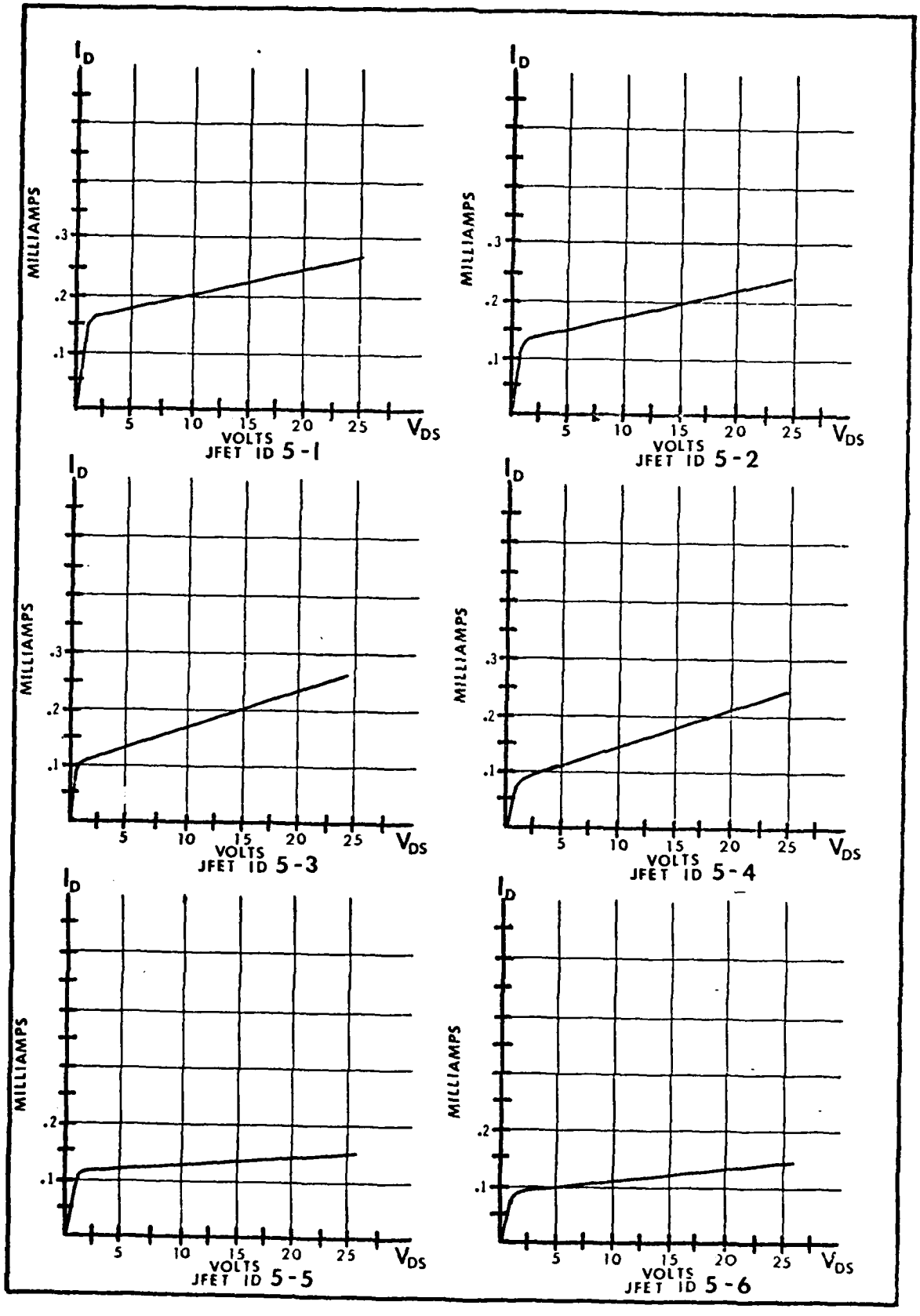
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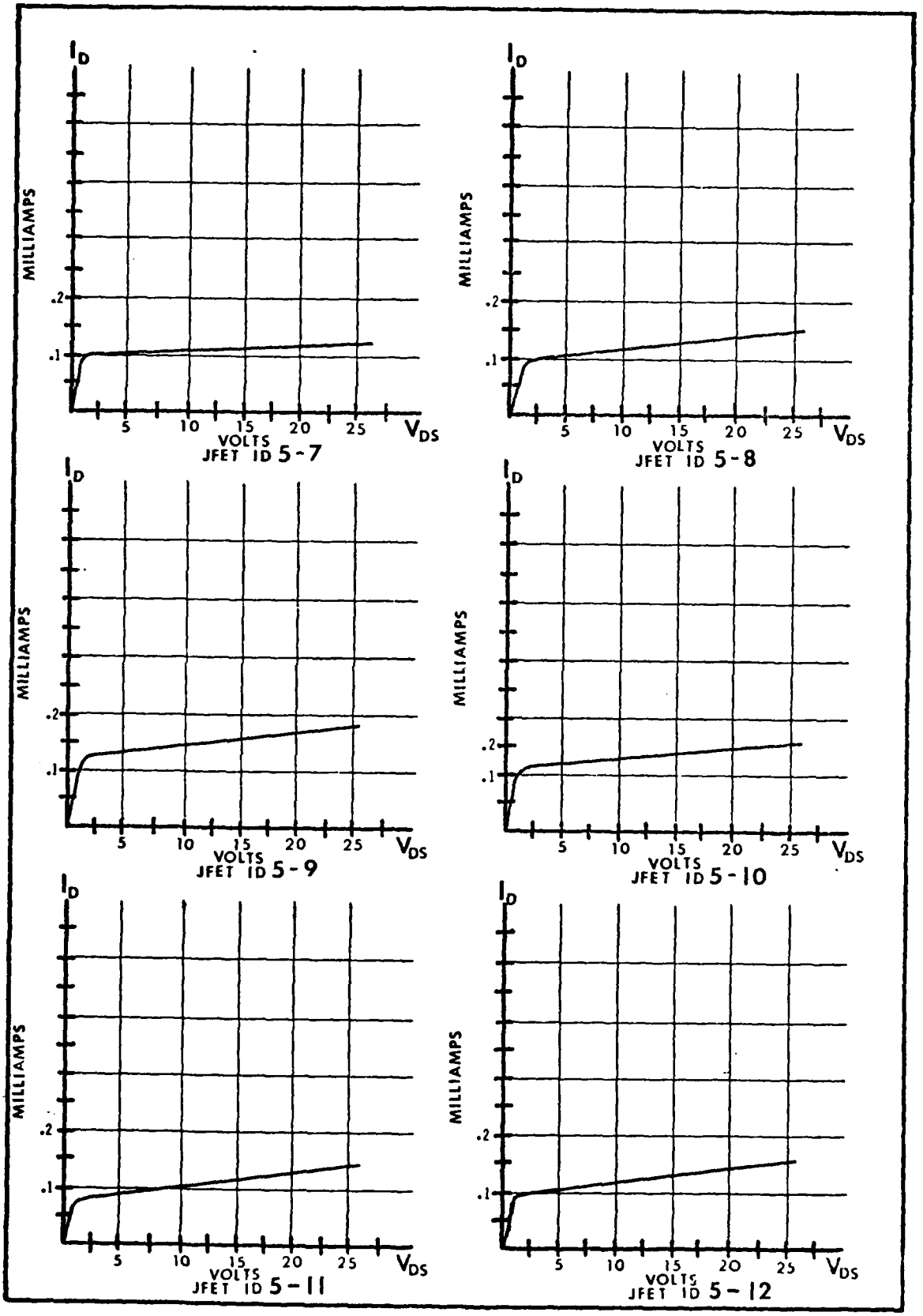
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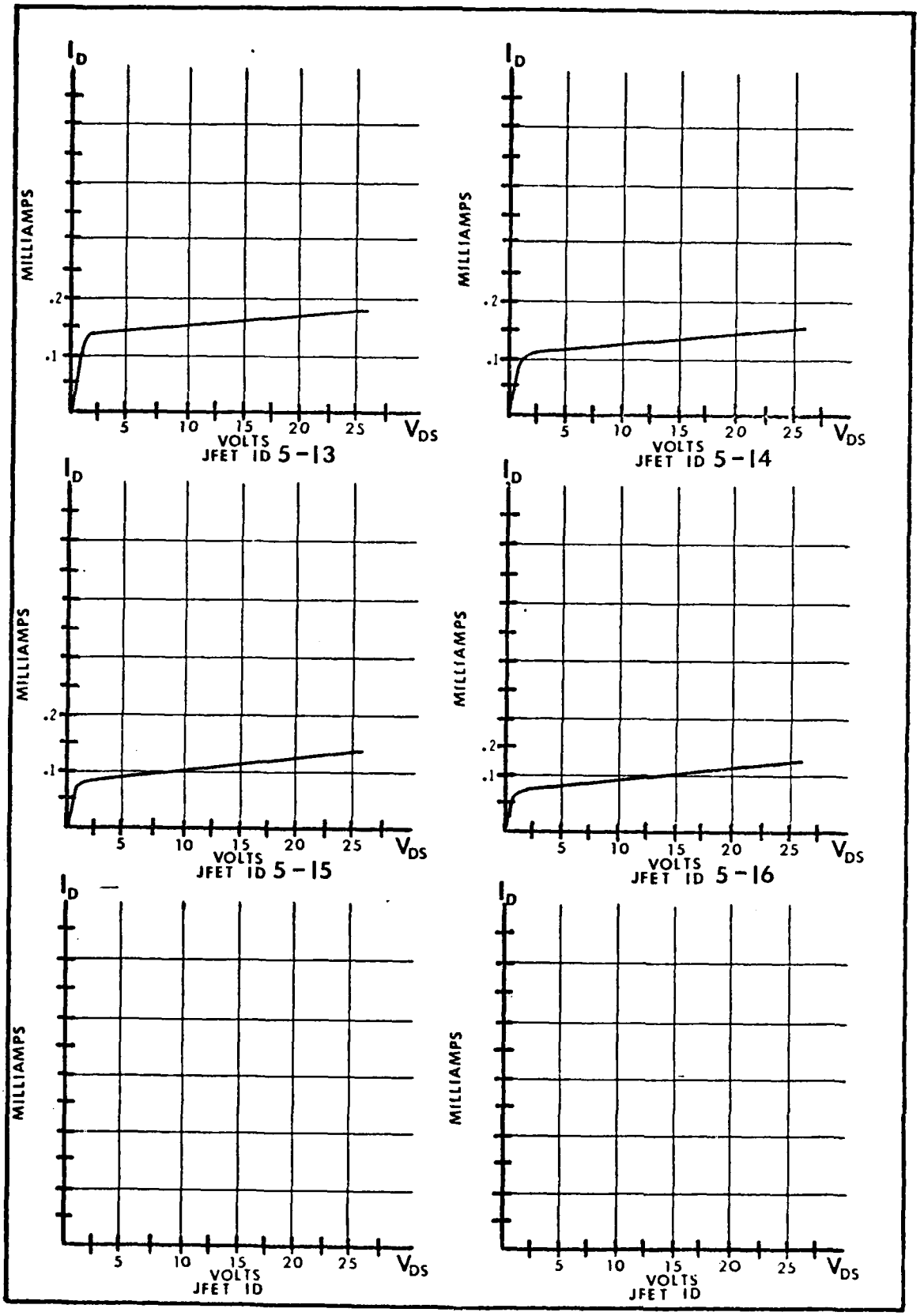
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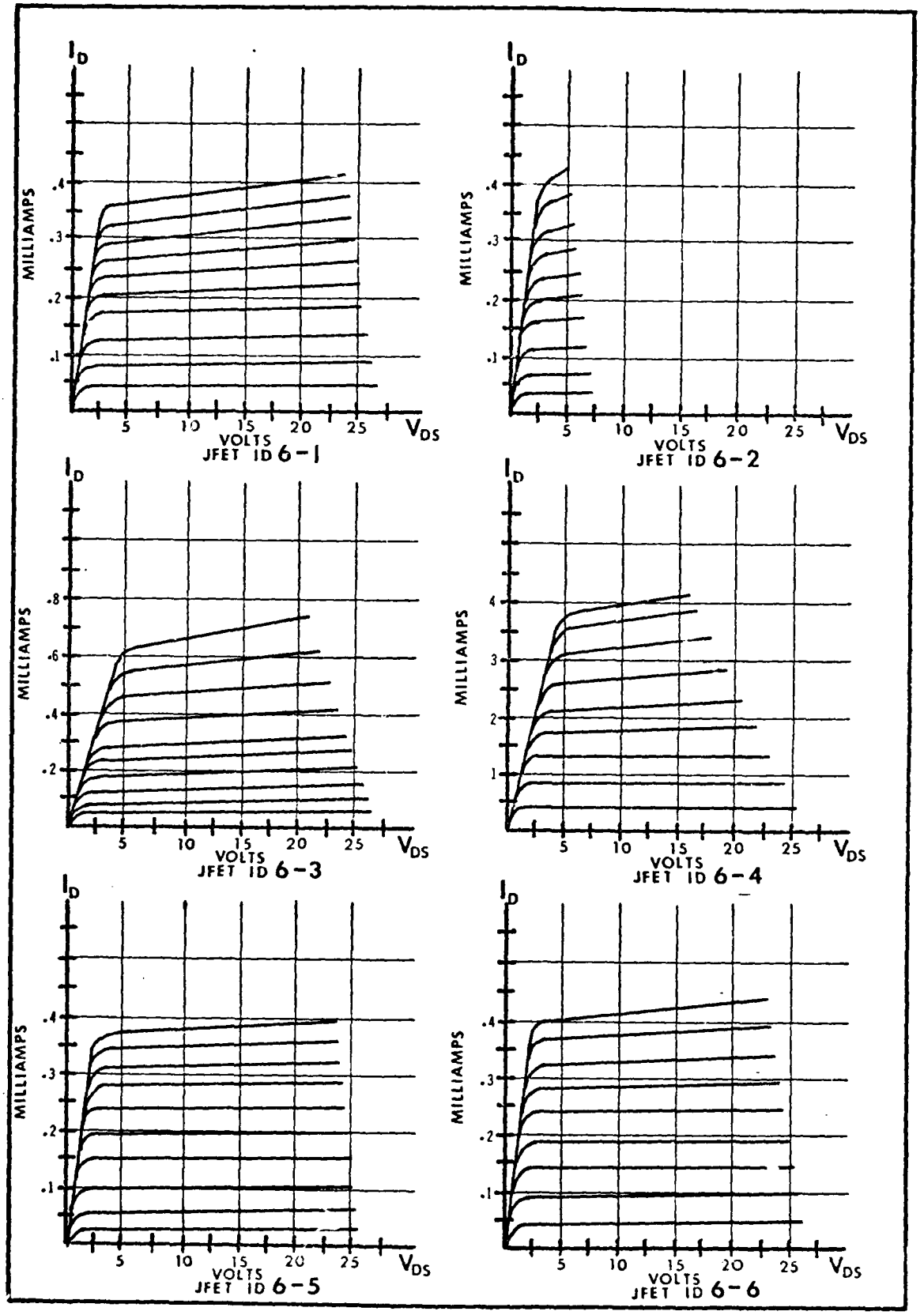
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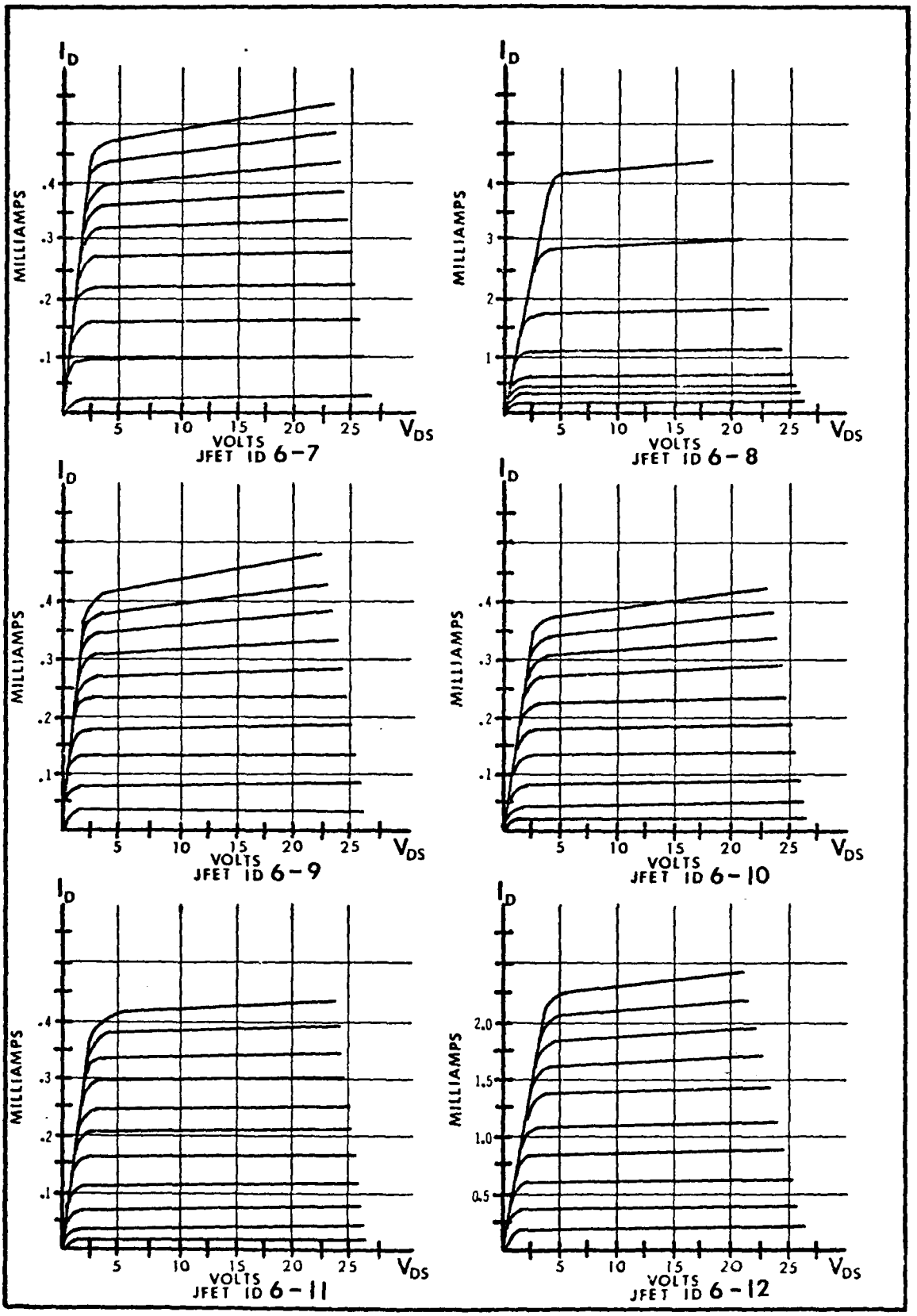
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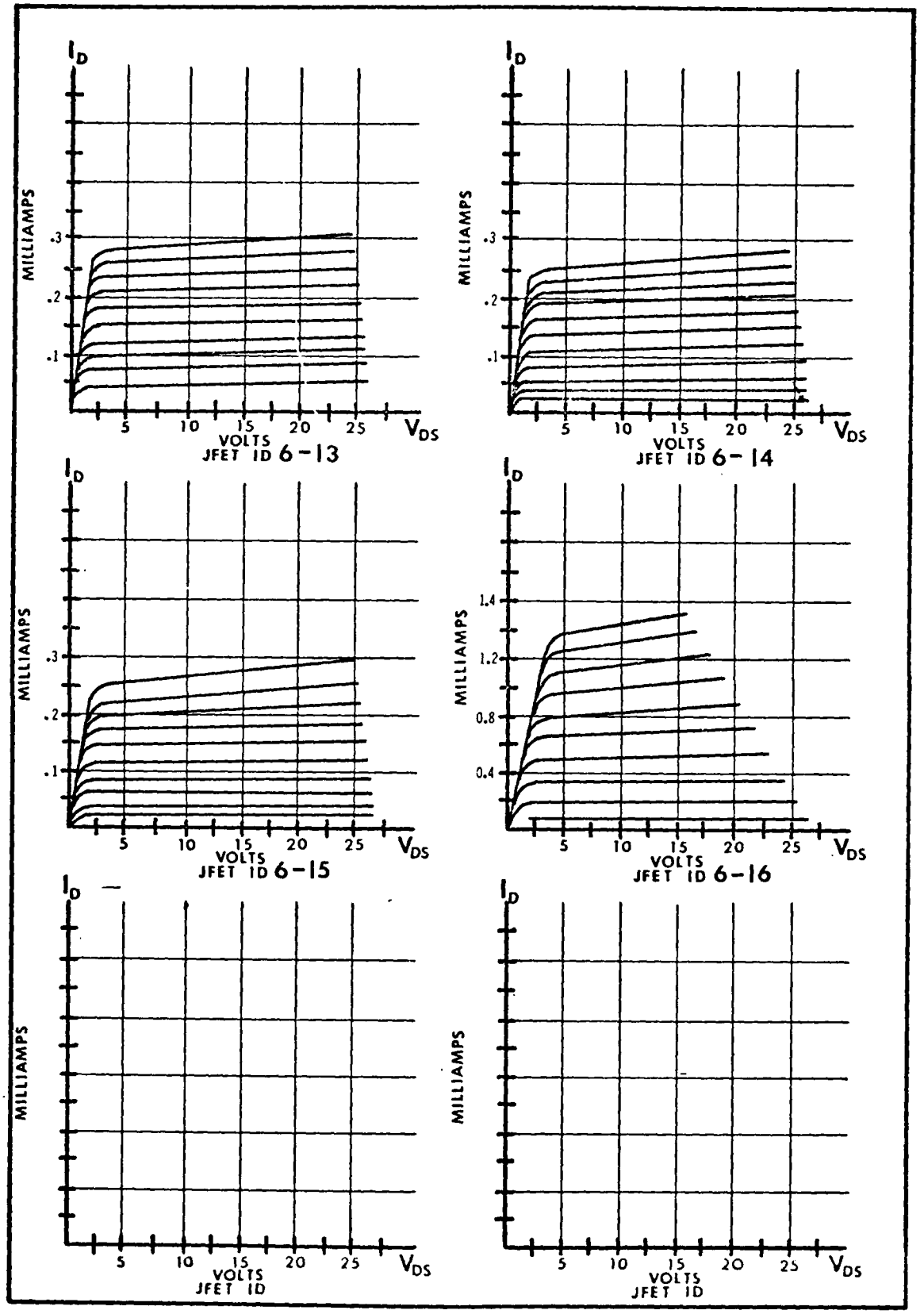
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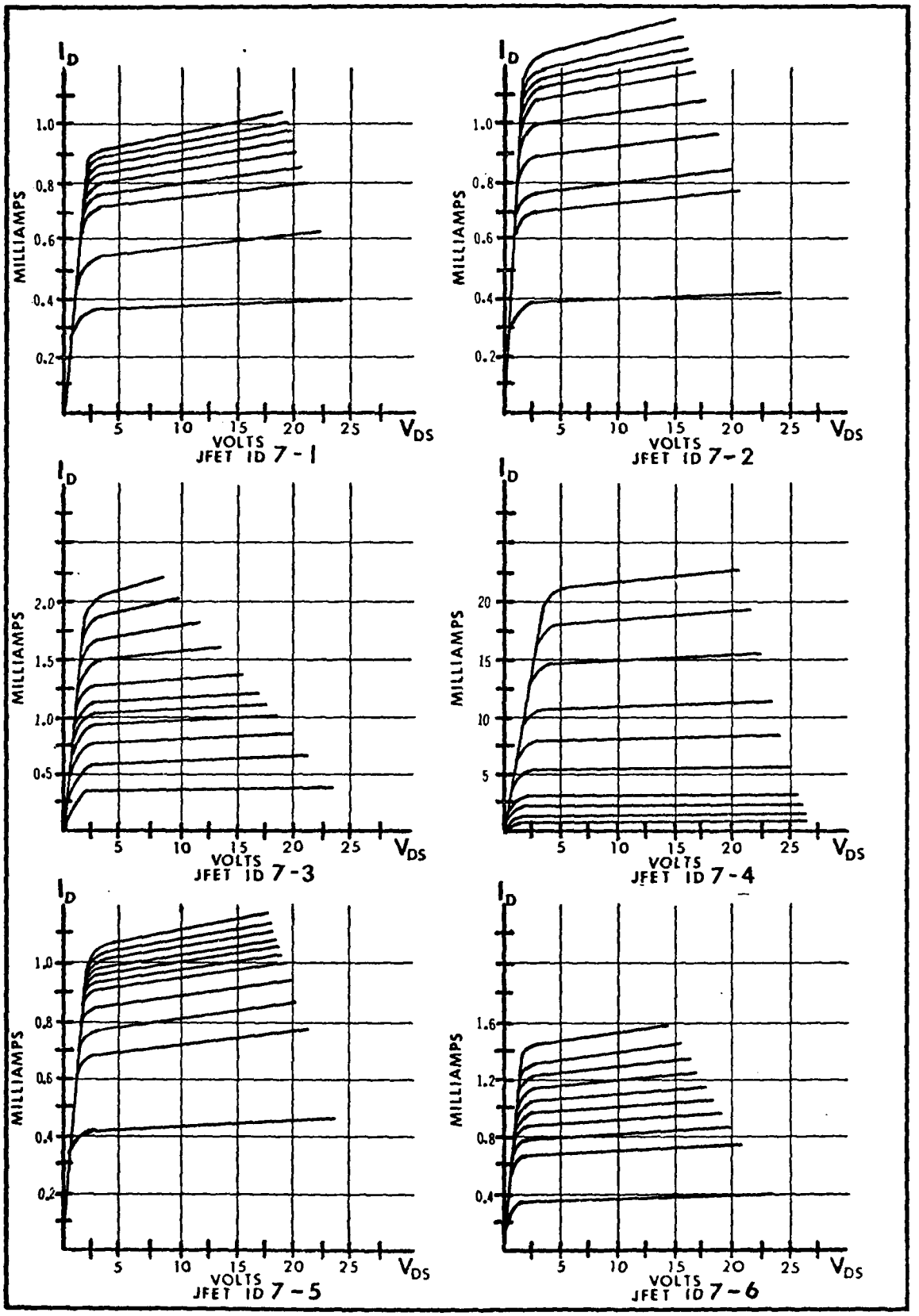
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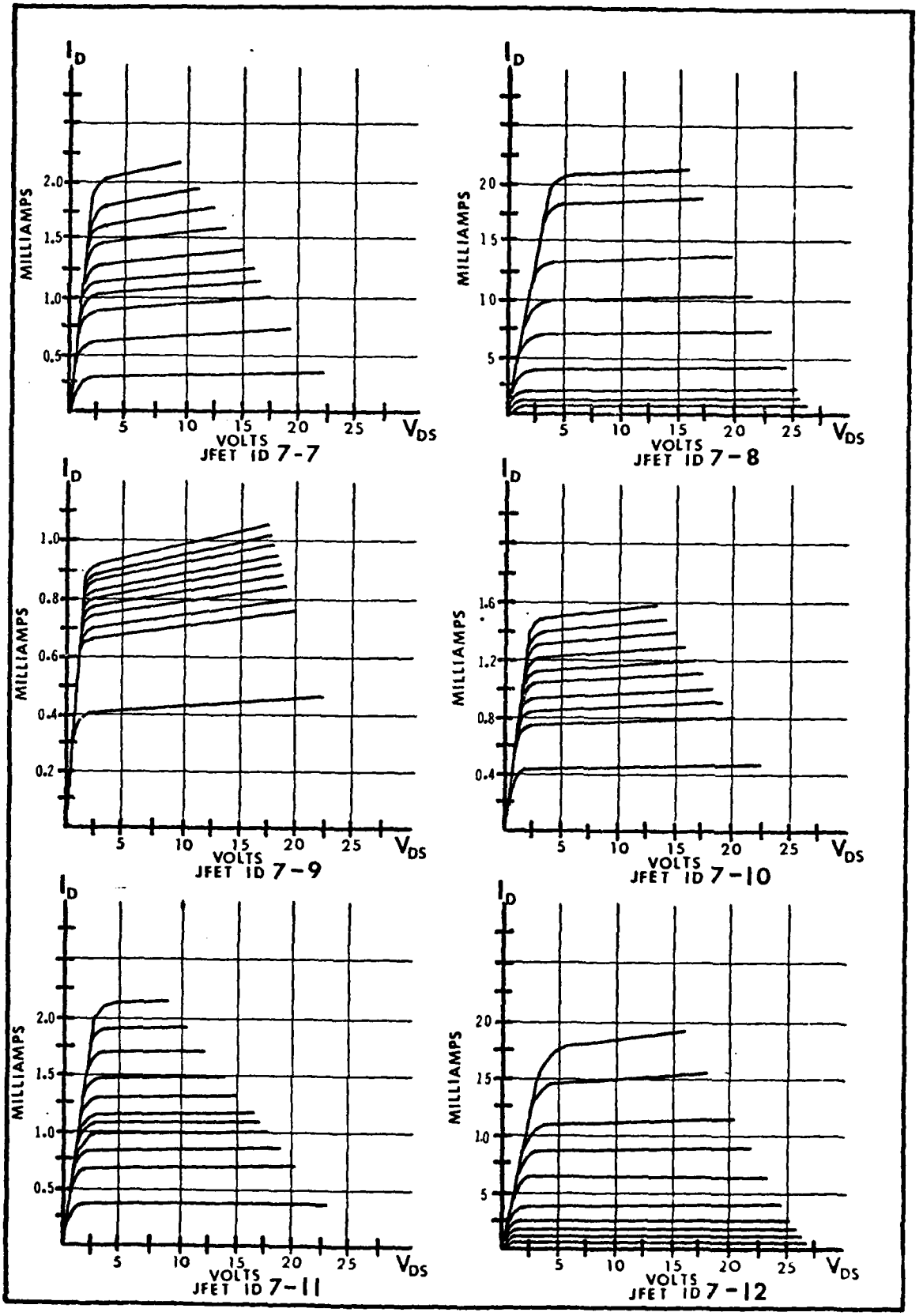
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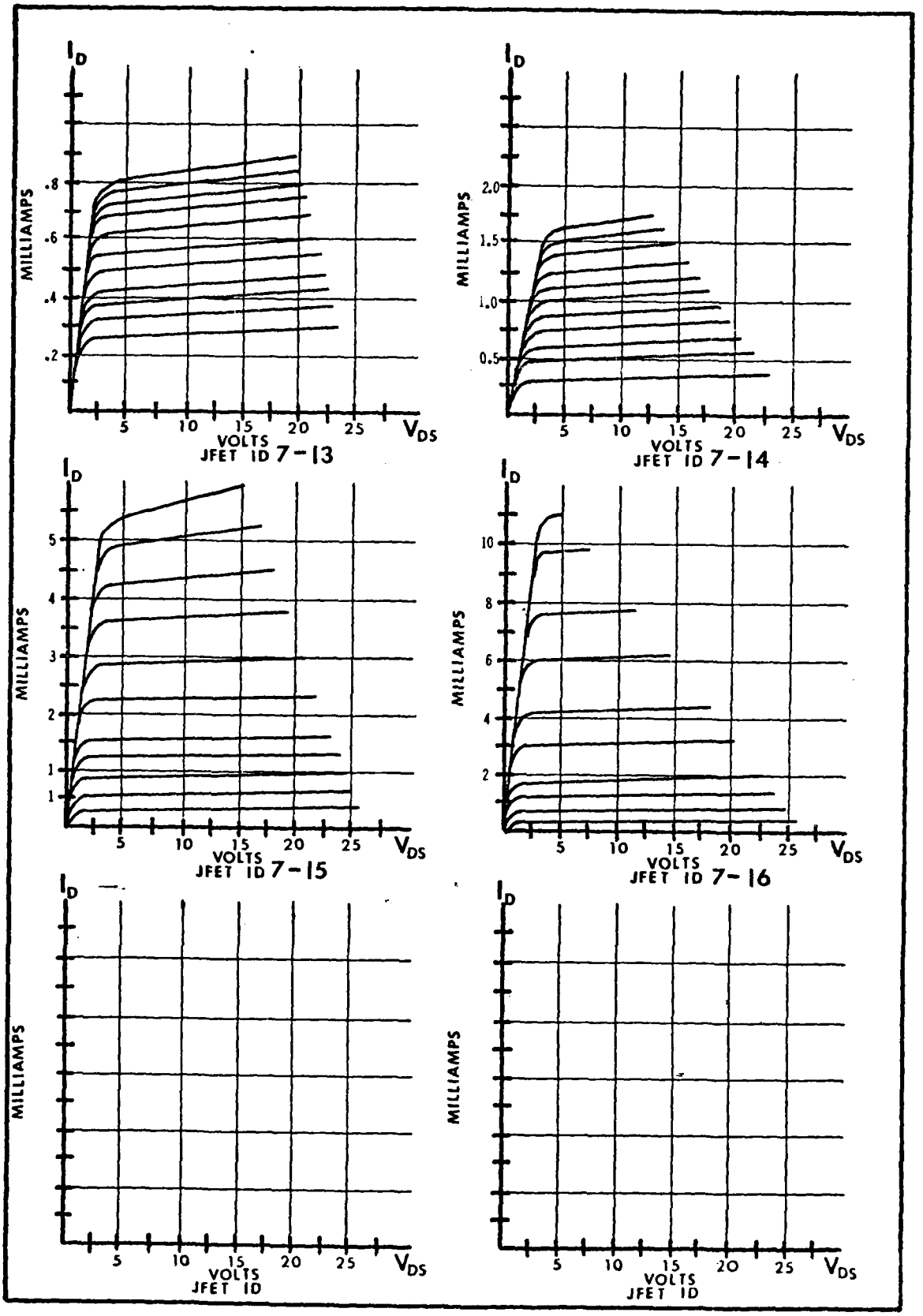
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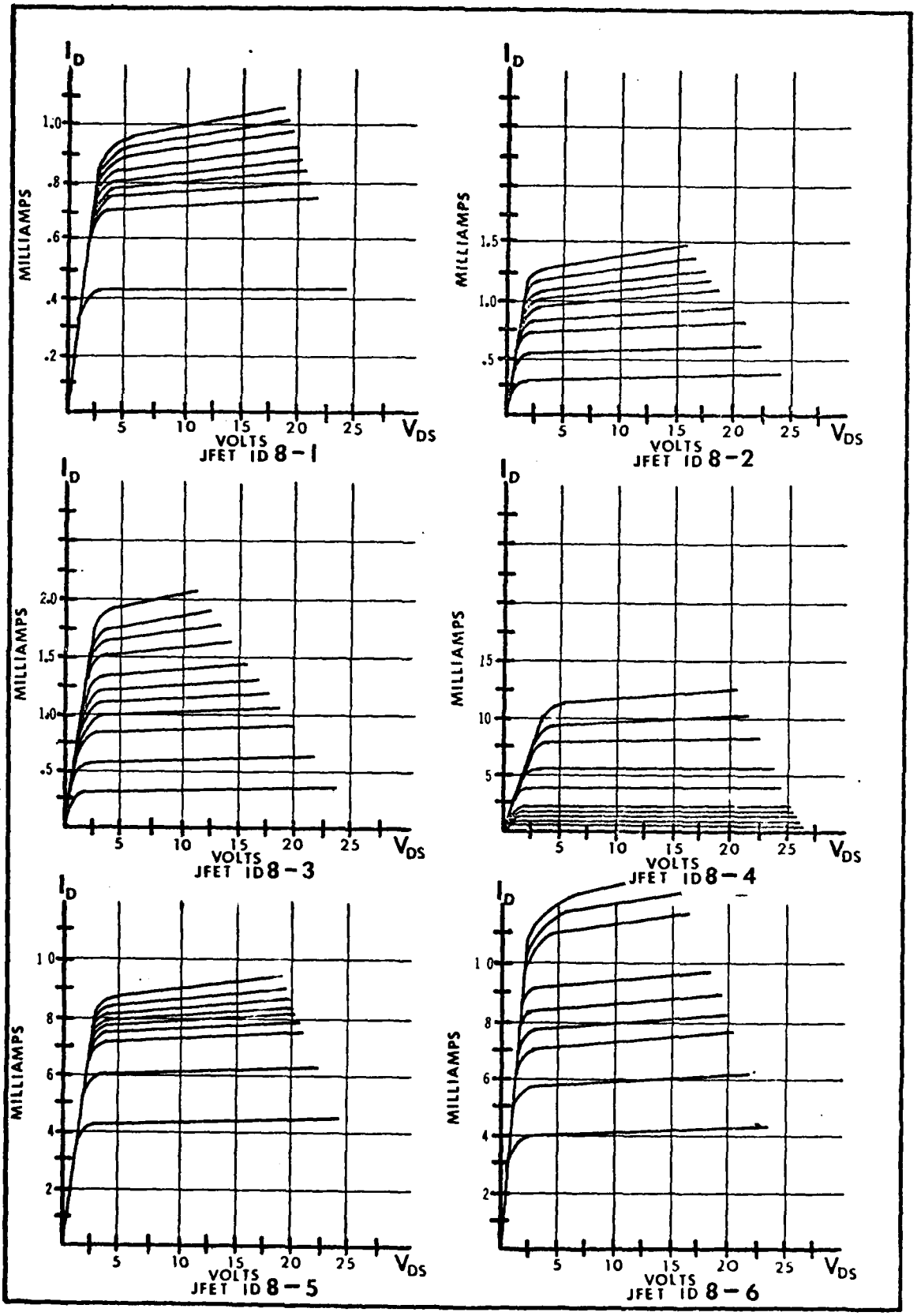
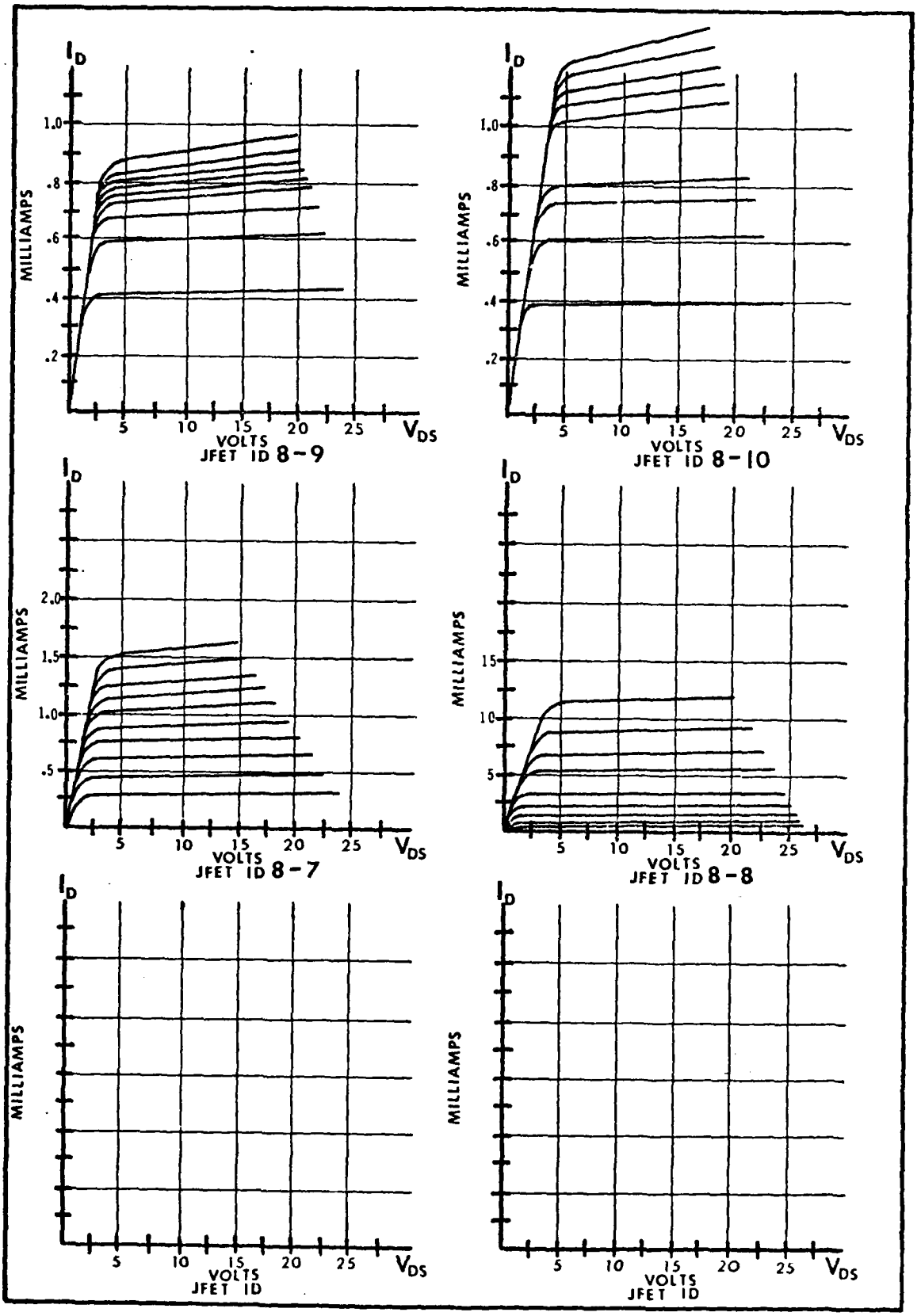
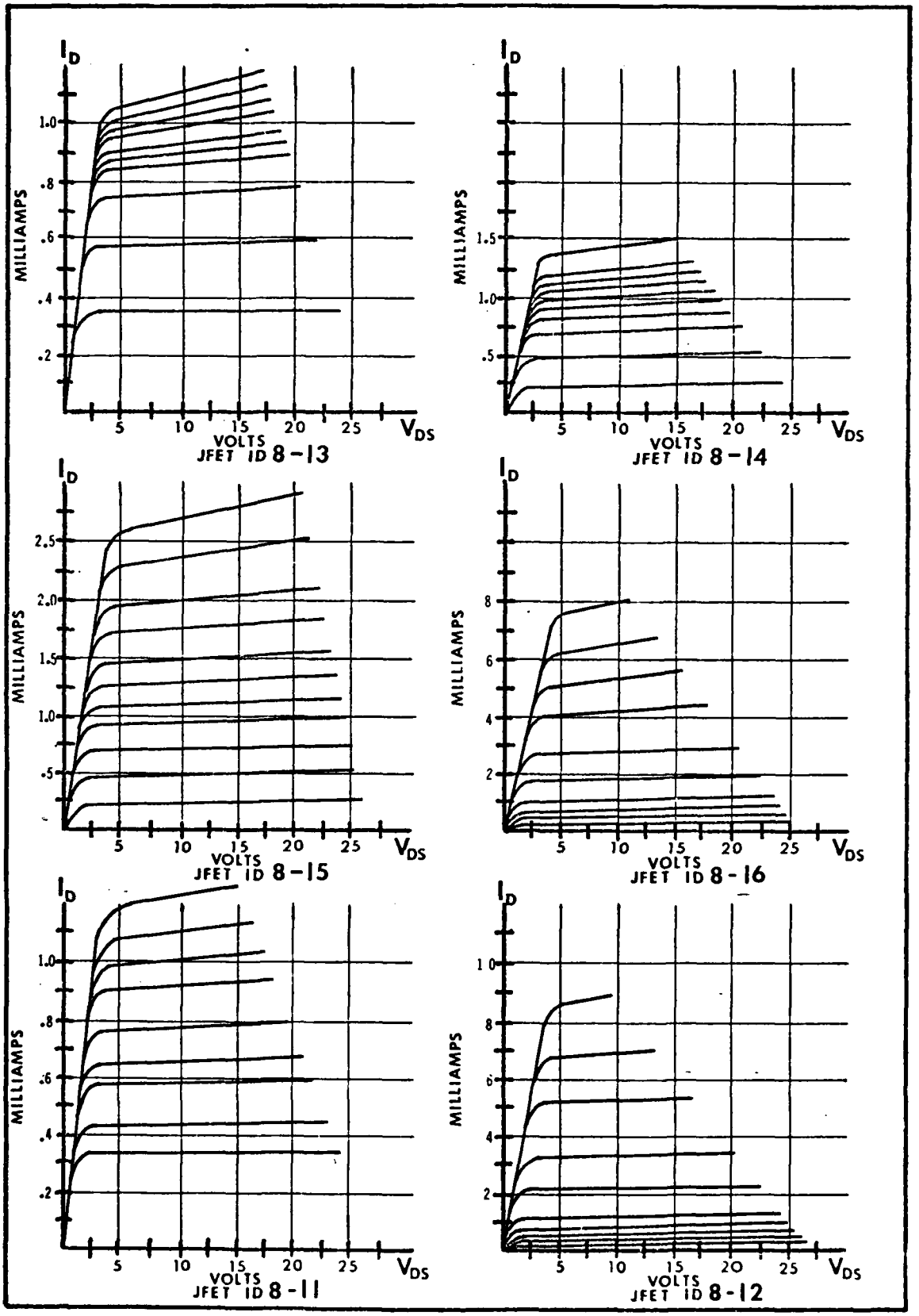
MILLIAMPS
5
4
3
2
1
1
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 7-15
I_D
MILLIAMPS
10
8
6
4
2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 7-16
I_D
MILLIAMPS
5
10
15
20
25
V_{DS}
VOLTS
JFET ID
I_D
MILLIAMPS
5
10
15
20
25
V_{DS}
VOLTS
JFET ID

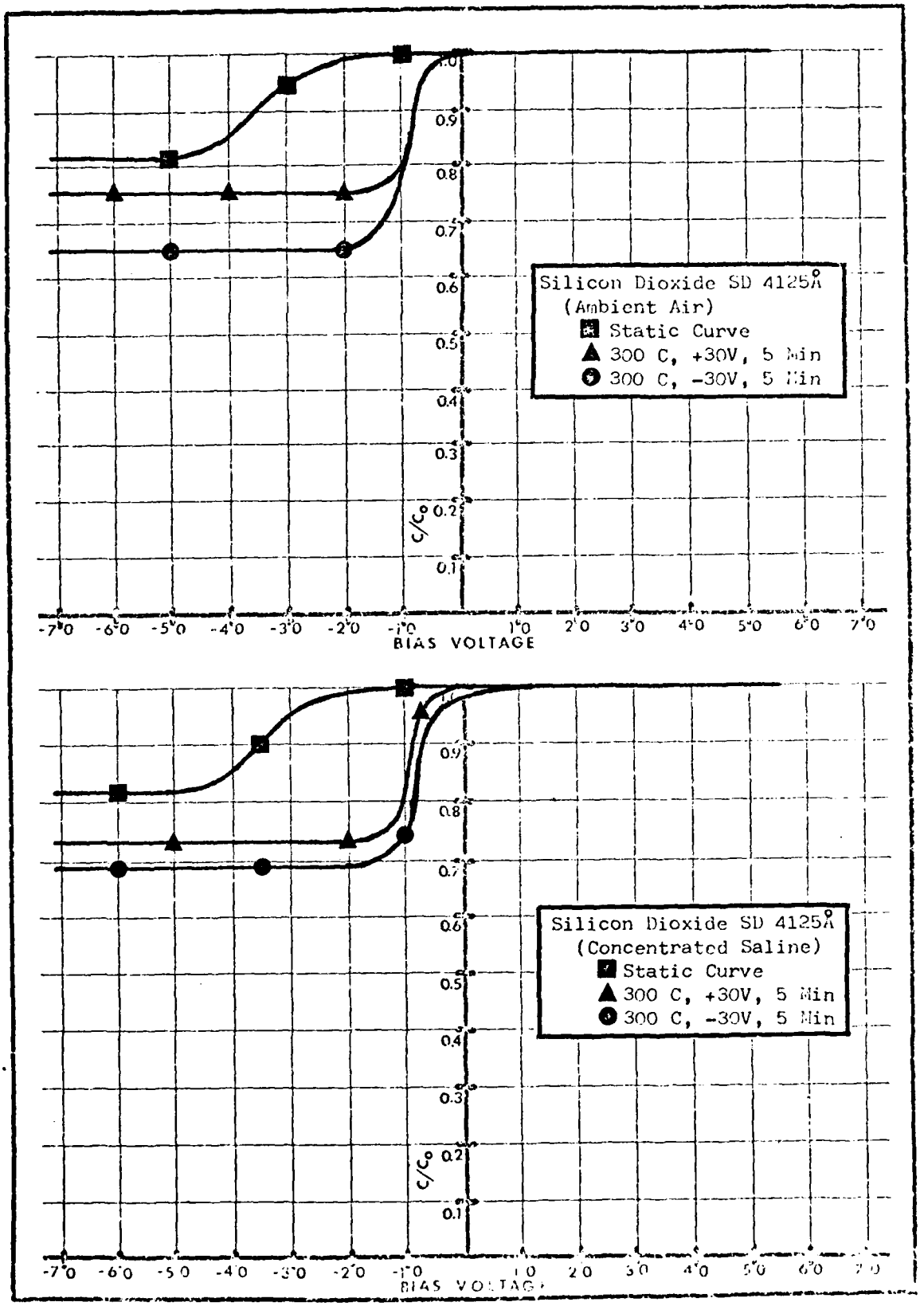

I_D
MILLIAMPS
1.0
.8
.6
.4
.2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-1
I_D
MILLIAMPS
1.5
1.0
.5
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-2
I_D
MILLIAMPS
2.0
1.5
1.0
.5
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-3
I_D
MILLIAMPS
15
10
5
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-4
I_D
MILLIAMPS
10
8
6
4
2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-5
I_D
MILLIAMPS
10
8
6
4
2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-6

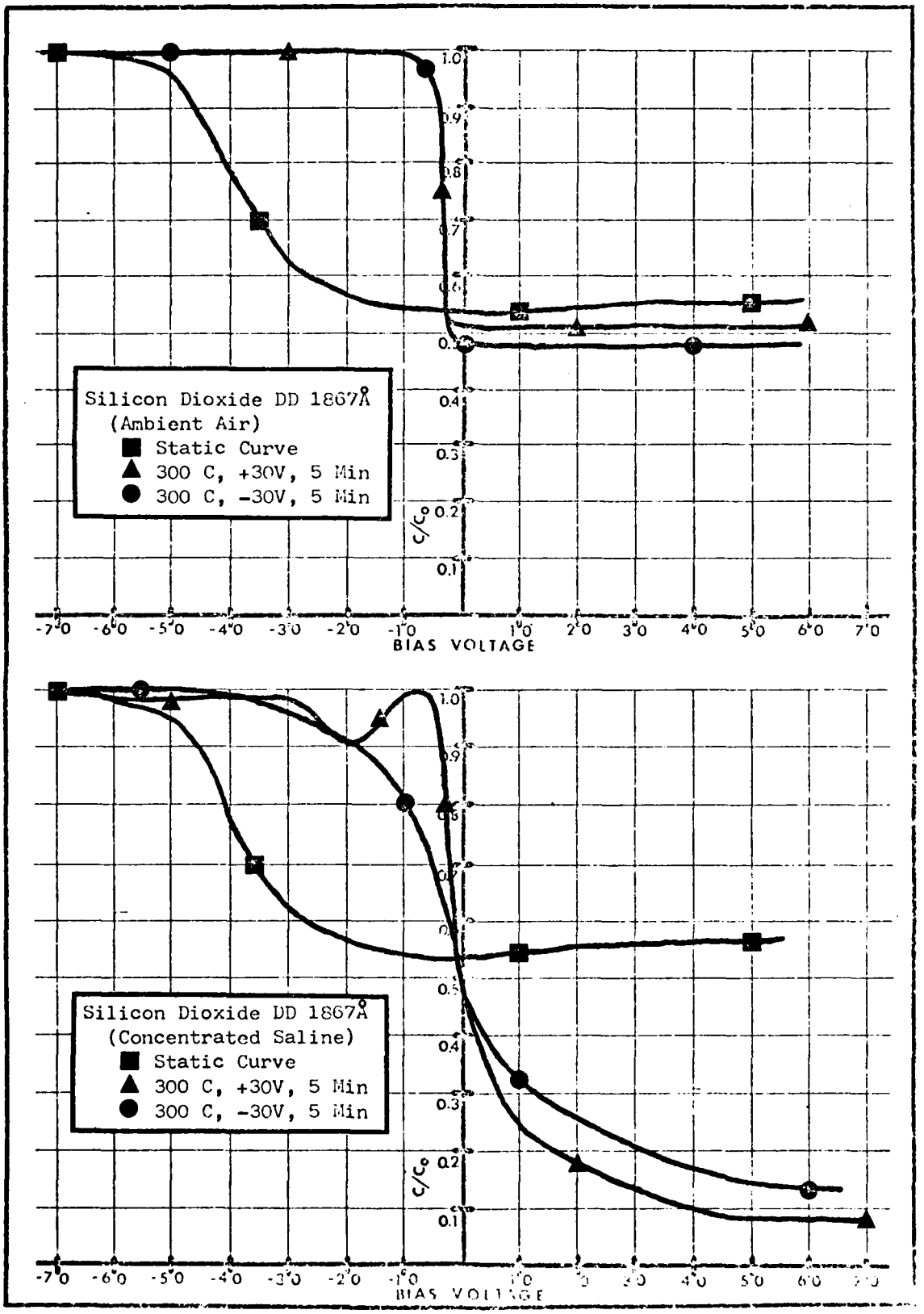

I_D
MILLIAMPS
1.0
.8
.6
.4
.2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-9
JFET ID 8-10
2.0
1.5
1.0
.5
JFET ID 8-7
15
10
5
JFET ID 8-8
JFET ID

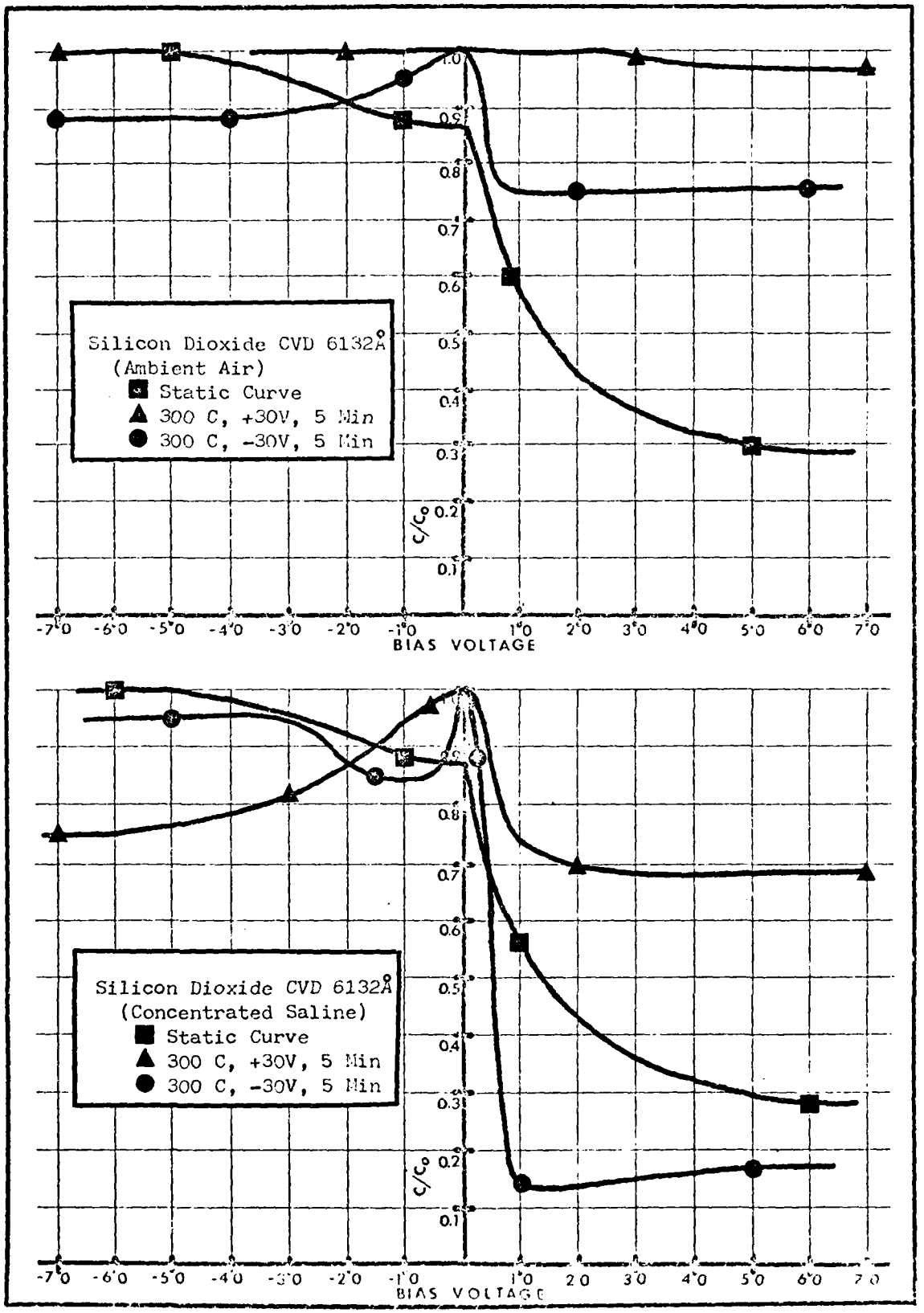

I_D
MILLIAMPS
1.0
.8
.6
.4
.2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-13
I_D
MILLIAMPS
1.5
1.0
.5
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-14
I_D
MILLIAMPS
2.5
2.0
1.5
1.0
.5
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-15
I_D
MILLIAMPS
8
6
4
2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-16
I_D
MILLIAMPS
1.0
.8
.6
.4
.2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-11
I_D
MILLIAMPS
10
8
6
4
2
5
10
15
20
25
V_{DS}
VOLTS
JFET ID 8-12

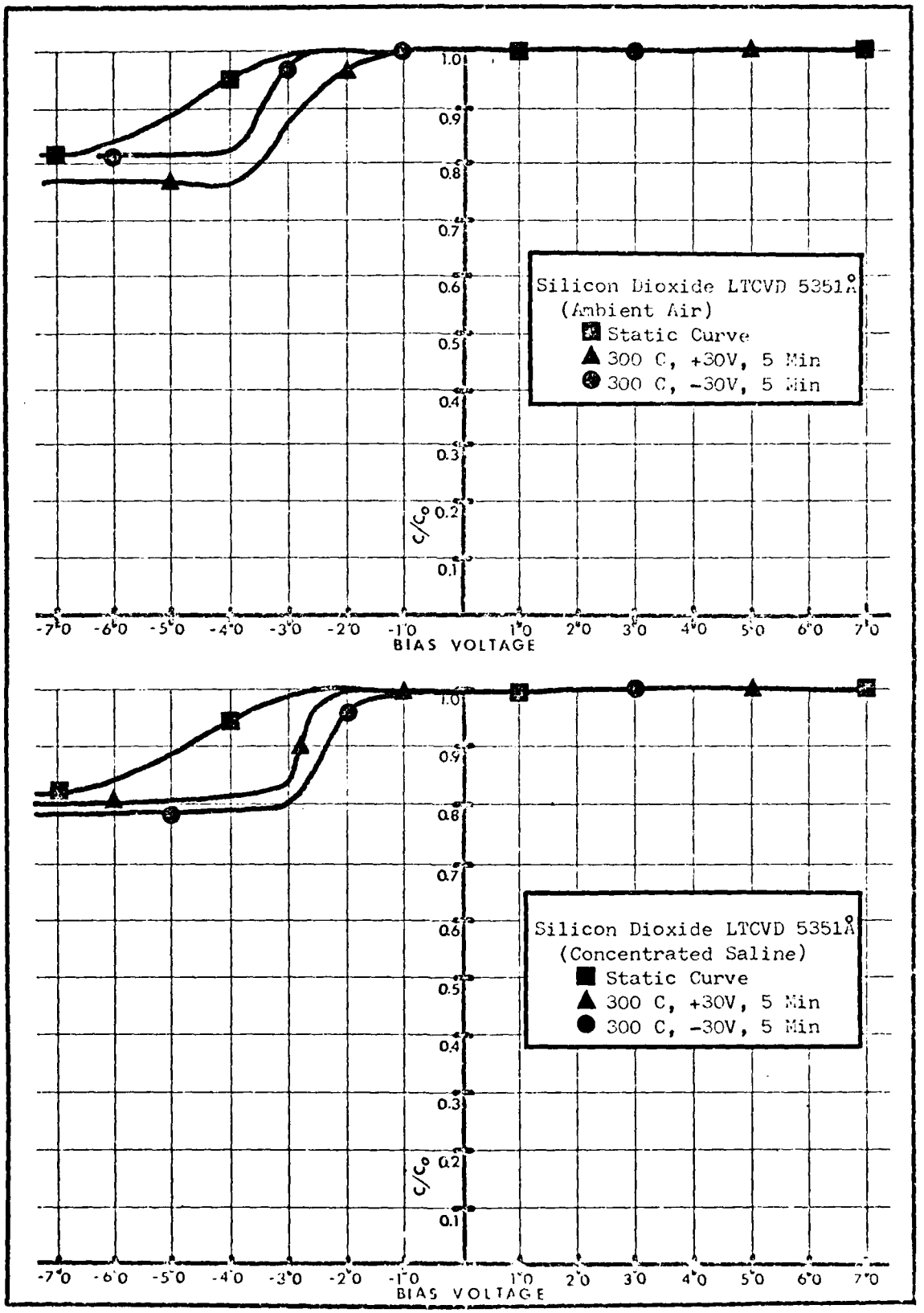
B. CAPACITANCE-VOLTAGE FAMILY OF CURVES

The family of Capacitance-Voltage Curves contained in this appendix were obtained from a Princeton Applied Research Model 410 C-V Plotter. The top set of curves is plotted in an ambient air environment. The bottom set of curves is plotted in a concentrated saline environment. The static curve is the same in both sets and was plotted before conducting any temperature-voltage aging.


Silicon Dioxide SD 4125Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/C°
BIAS VOLTAGE
Silicon Dioxide SD 4125Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/C°
BIAS VOLTAGE


Silicon Dioxide DD 1867Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
Silicon Dioxide DD 1867Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE


Silicon Dioxide CVD 6132Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
Silicon Dioxide CVD 6132Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE


Silicon Dioxide LTCVD 5351Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
Silicon Dioxide LTCVD 5351Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE

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A CORTICALLY IMPLANTABLE MULTIELECTRODE ARRAY FOR INVESTIGATING--ETC(U)
DEC 81 G W GERMAN

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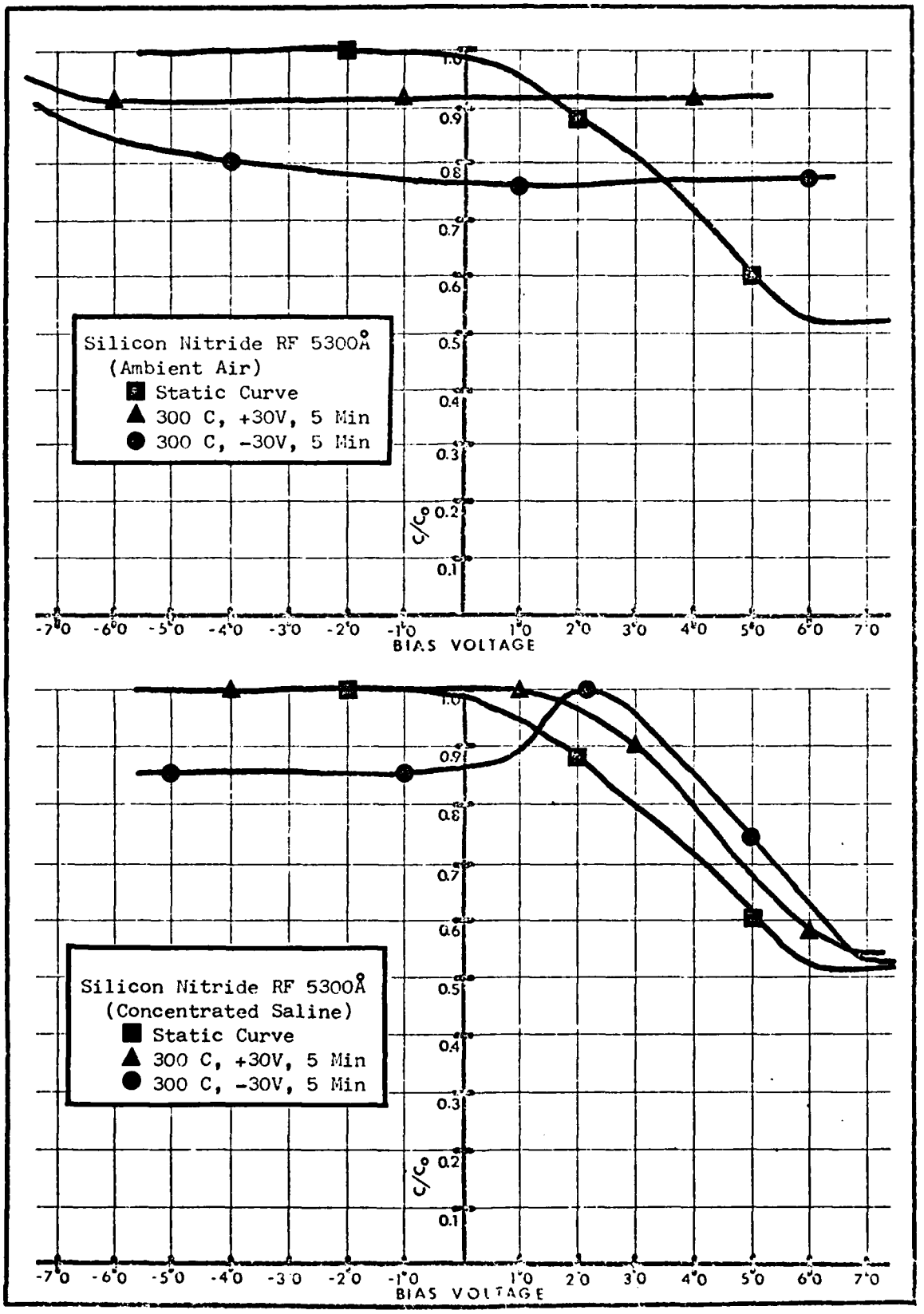
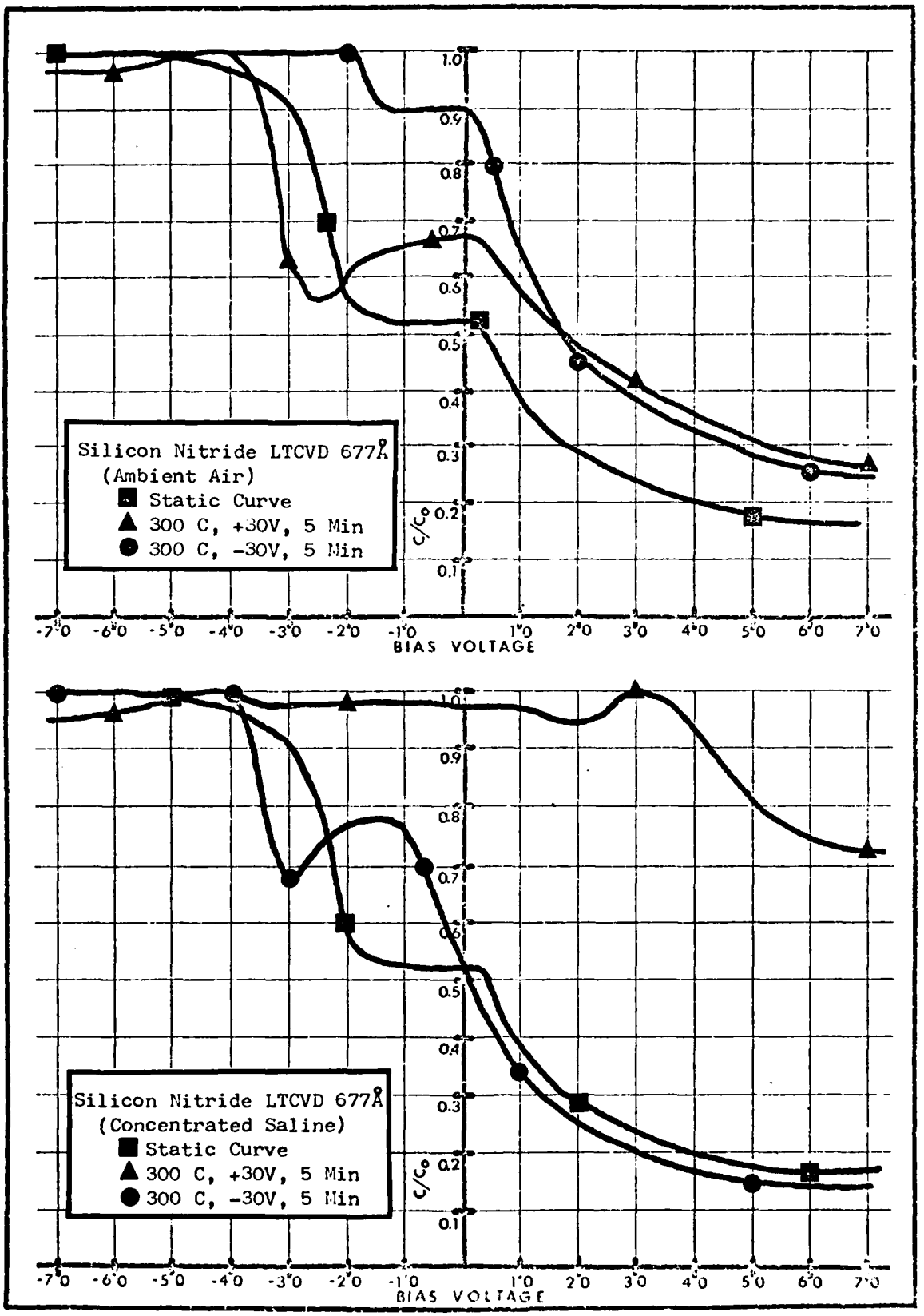
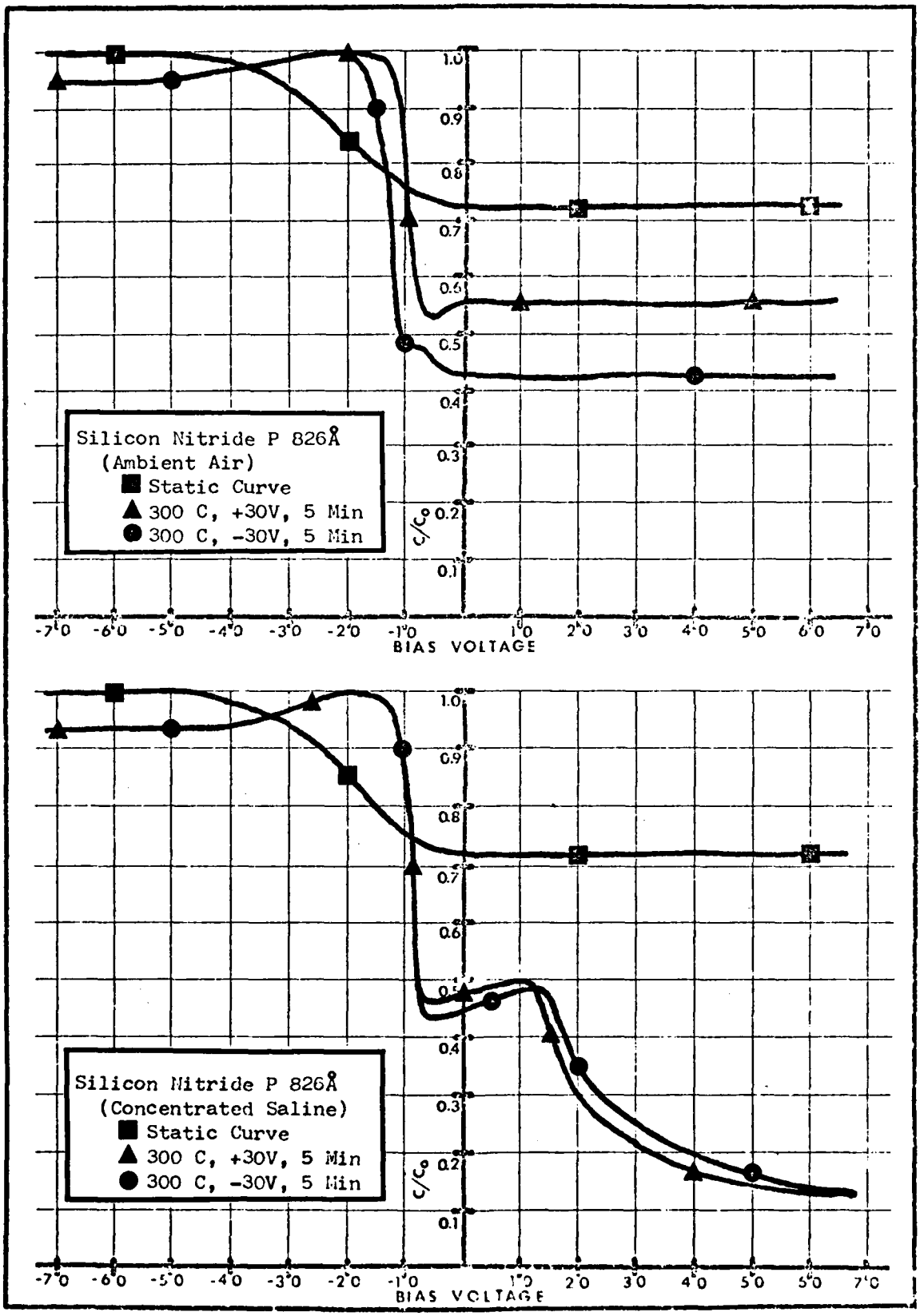
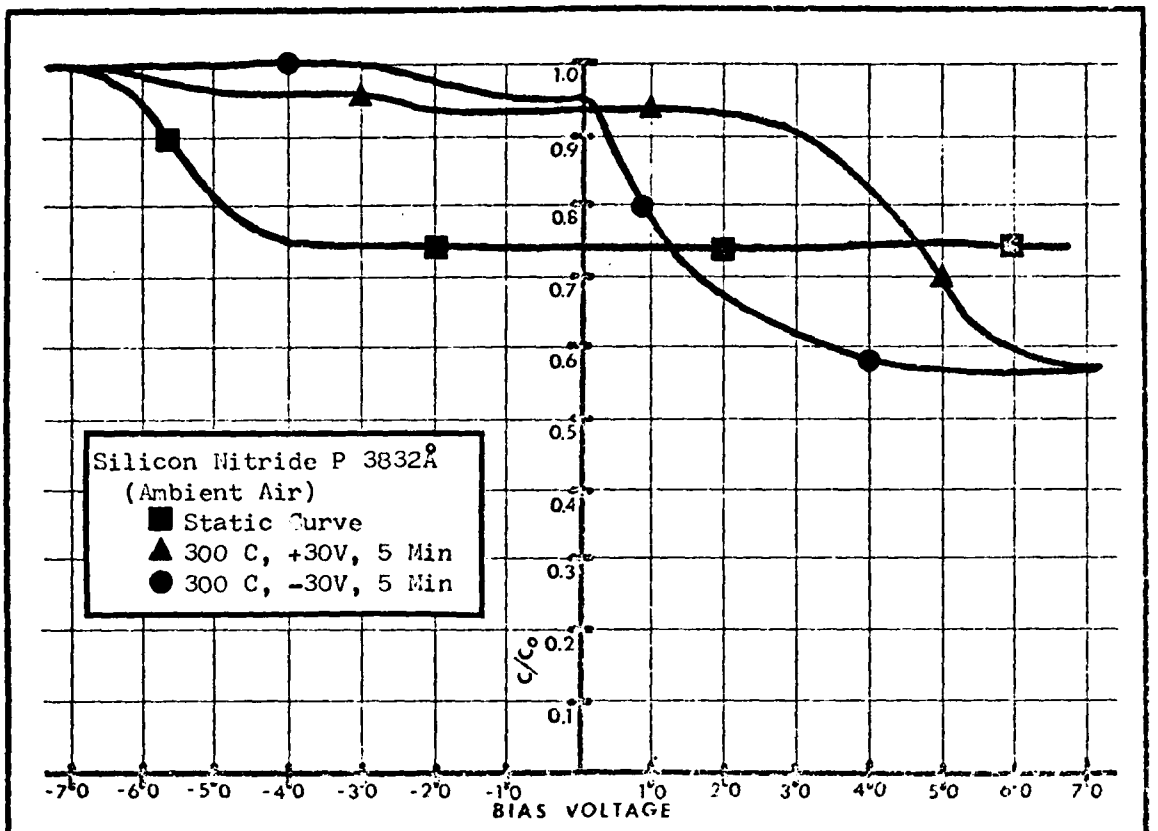
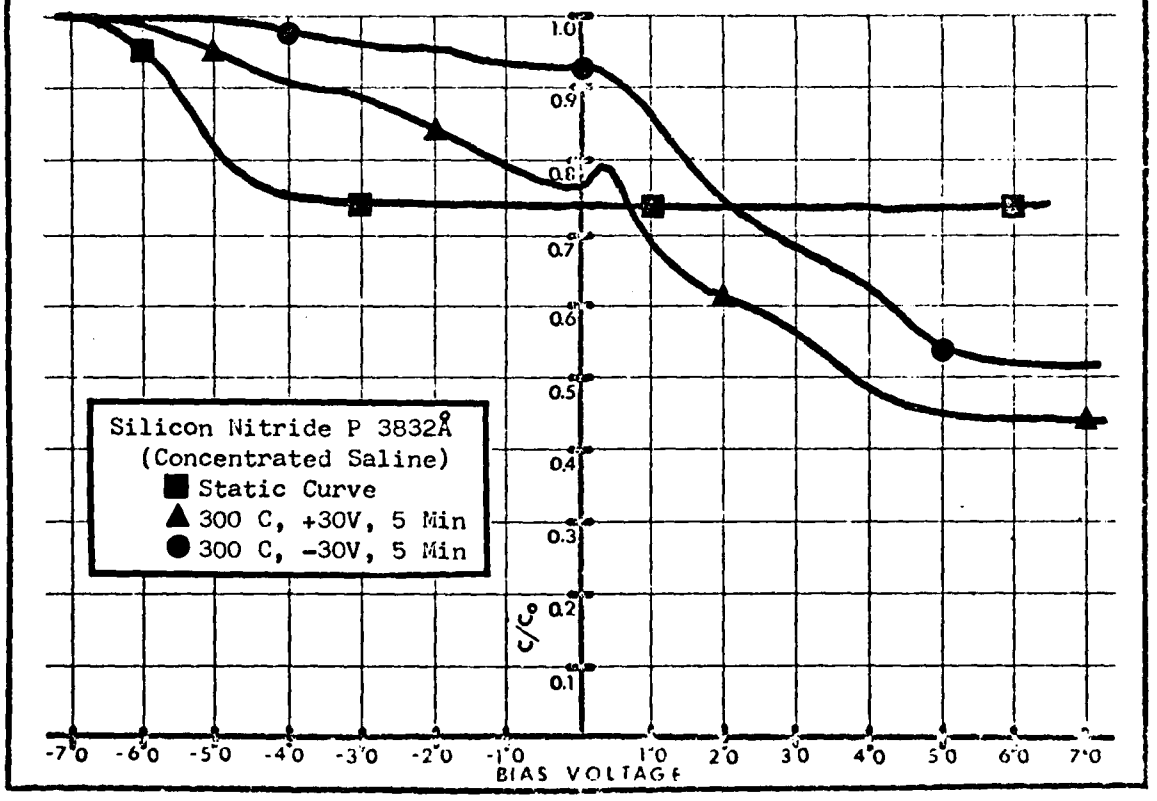
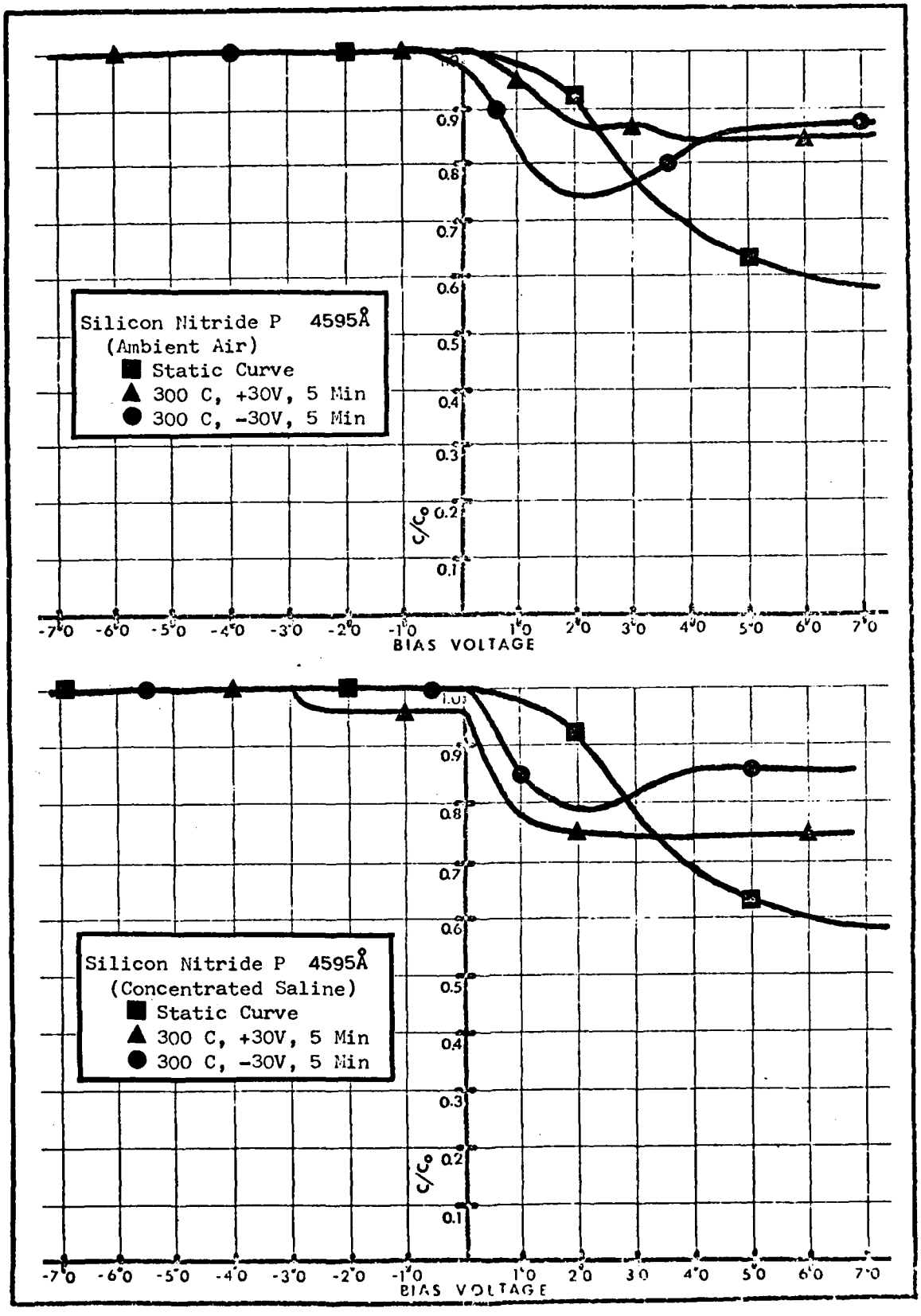

Silicon Nitride RF 5300Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/C°
BIAS VOLTAGE
Silicon Nitride RF 5300Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/C°
BIAS VOLTAGE

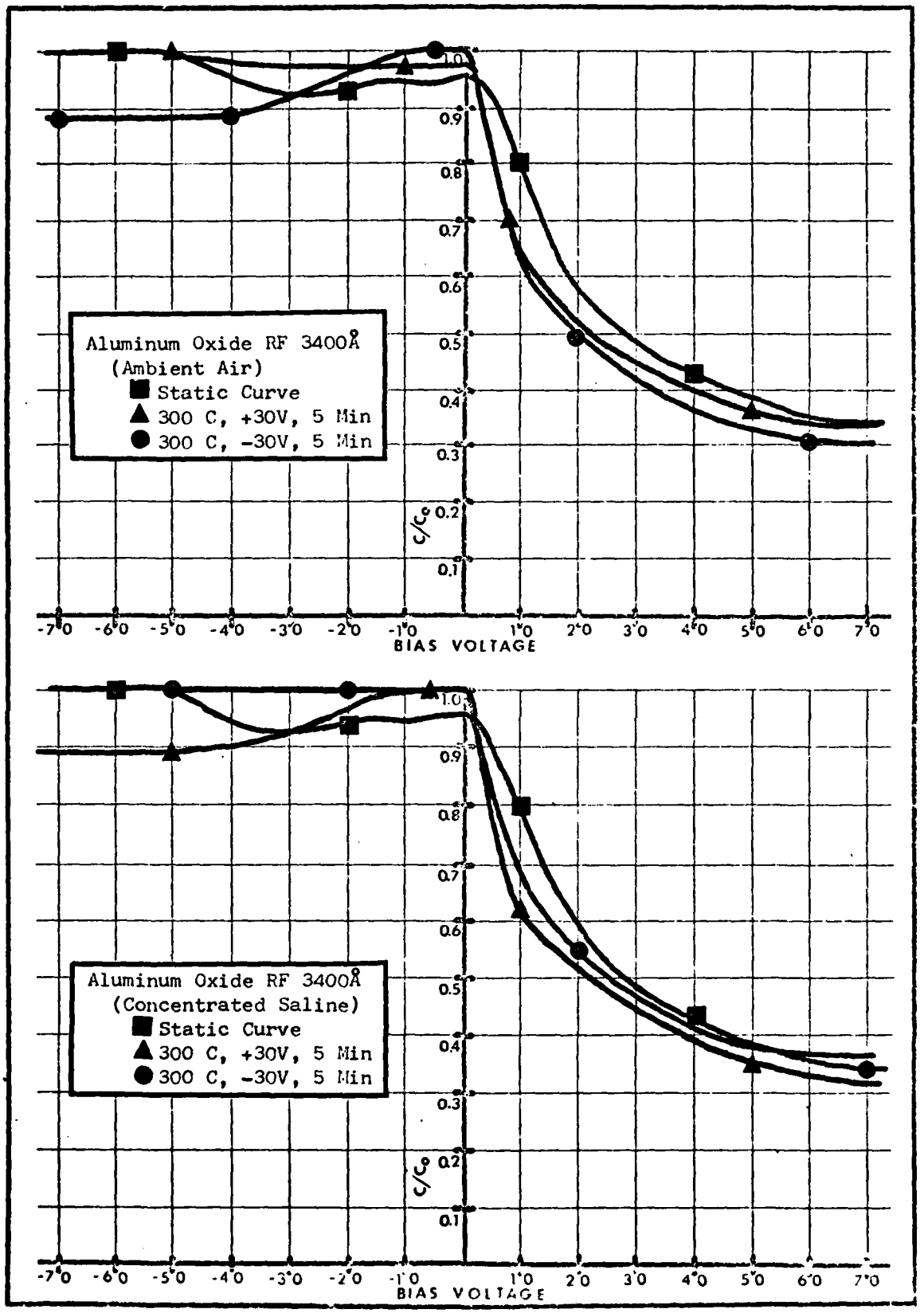

Silicon Nitride LTCVD 677Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
Silicon Nitride LTCVD 677Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE

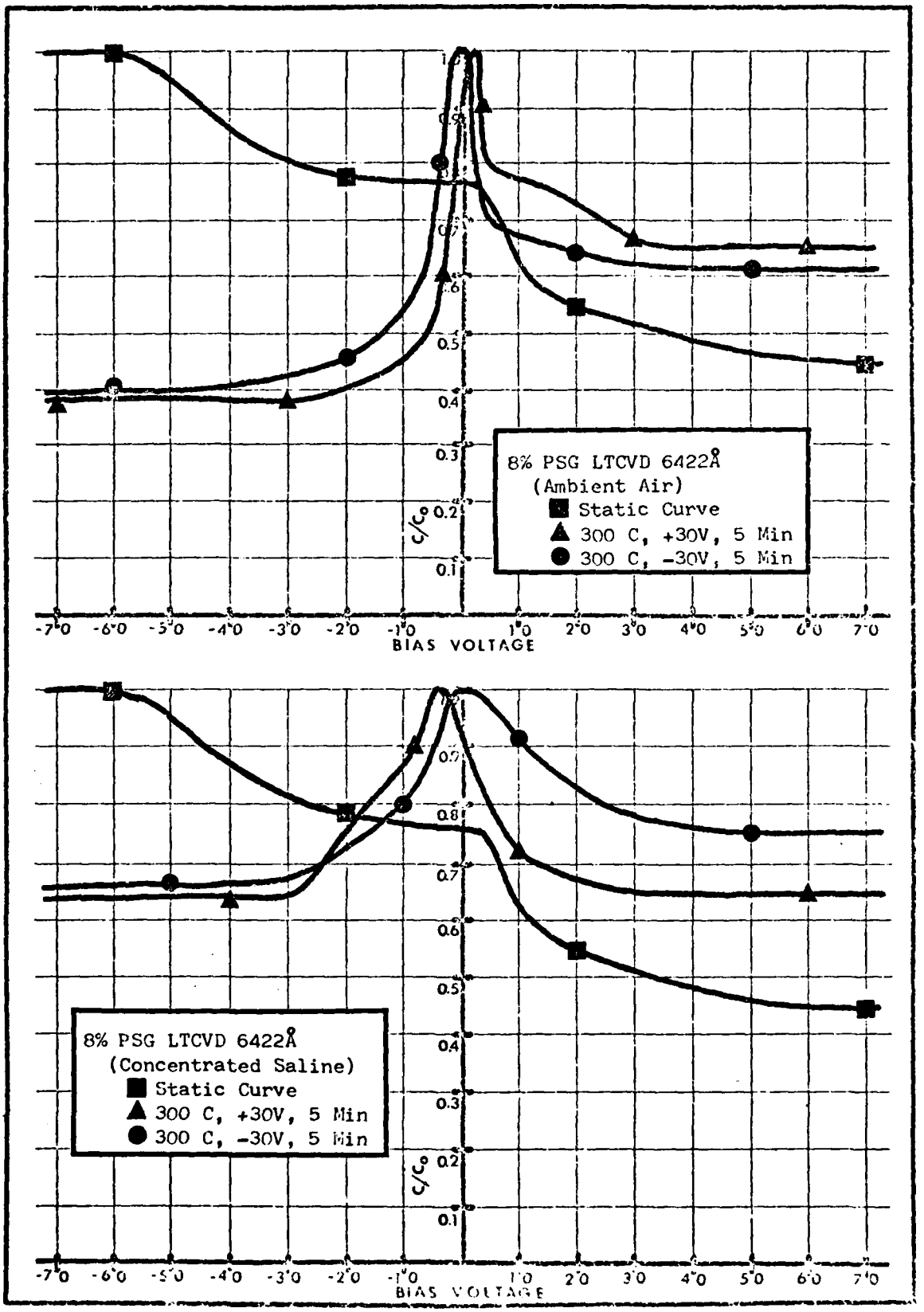

Silicon Nitride P 826Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
Silicon Nitride P 826Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE

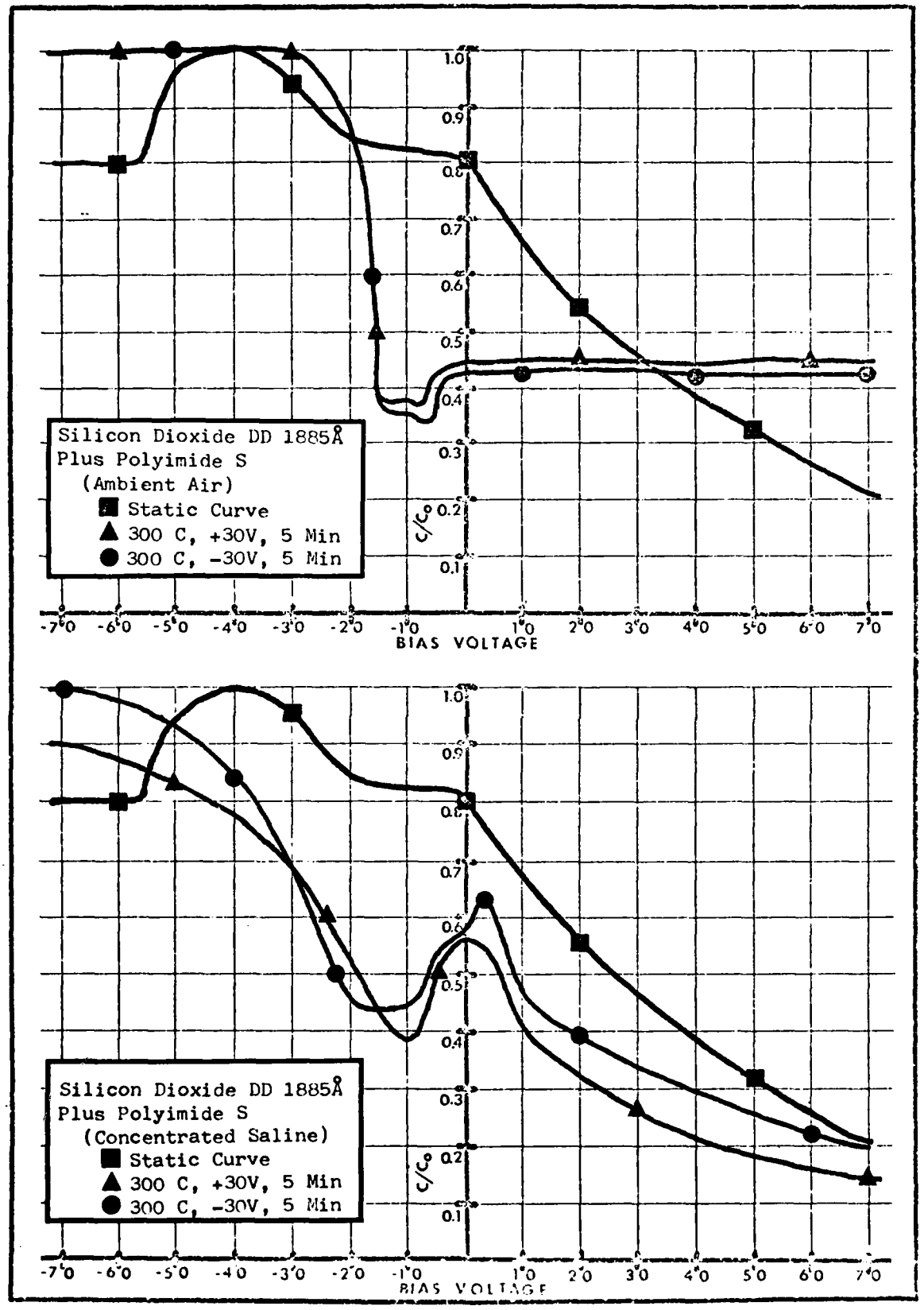

Silicon Nitride P 3832Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
-7'0 -6'0 -5'0 -4'0 -3'0 -2'0 -1'0 1'0 2'0 3'0 4'0 5'0 6'0 7'0
BIAS VOLTAGE


Silicon Nitride P 3832Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
-7'0 -6'0 -5'0 -4'0 -3'0 -2'0 -1'0 1'0 2'0 3'0 4'0 5'0 6'0 7'0
BIAS VOLTAGE


Silicon Nitride P 4595Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
Silicon Nitride P 4595Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE


Aluminum Oxide RF 3400Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
Aluminum Oxide RF 3400Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE


8% PSG LTCVD 6422Å
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
8% PSG LTCVD 6422Å
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE


Silicon Dioxide DD 1885Å
Plus Polyimide S
(Ambient Air)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE
Silicon Dioxide DD 1885Å
Plus Polyimide S
(Concentrated Saline)
Static Curve
300 C, +30V, 5 Min
300 C, -30V, 5 Min
C/Co
BIAS VOLTAGE

Vita

George W. German III was born October 4, 1946 in Shreveport, Louisiana. He graduated from Texas High School, Texarkana, Texas in May 1964. After a year at Texarkana Jr. College, he enlisted in the Air Force and served as a Link Trainer Instructor at Chanute AFB, Keesler AFB, and Moody AFB. He was accepted into the Airman's Education and Commissioning Program and received a Bachelor of Science degree in Electical Engineering from Oklahoma State University in May 1972. After Officer Training School, Lt German completed Undergraduate Pilot Training at Reese AFB in November 1973. During subsequent flying assignments he flew F-4E's and C-130's at Homestead AFB, Seymour-Johnson AFB, Keesler AFB, and Incirlik AB. He was assigned to the Air Force Institute of Technology in June 1980.

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Device Passivation
Multiplexed Implant
Multielectrode Array
Microelectrode Array

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The research conducted during this study is a continuation of the Tatman-Fitzgerald (DTIC AD A080378, AD A100763) fabrication and testing of an implantable, multiplexed, multielectrode array that will be used to record the bioelectric signals emitted from the cortex of a live, visually functional animal. Primary emphasis of this study is the investigation of passivation materials that can be used to protect the AFIT Multielectrode Array from the harsh cerebrospinal environment encountered inside the

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cranium. Secondary emphasis is placed on analyzing the electrical characteristics of an AFIT Array, designing an improved multiplexing drive circuit, and testing the system equipment with an operational device.


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