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M/A-COM SILICON PRODUCTS INC BURLINGTON MA
MANUFACTURING TECHNOLOGY PROGRAM FOR HIGH BURNOUT SILICON SCHOT--ETC(U)
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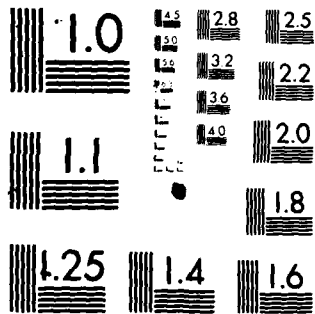
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**MANUFACTURING TECHNOLOGY PROGRAM
FOR HIGH BURNOUT SILICON SCHOTTKY-
BARRIER MIXER DIODES FOR NAVY
AIR-TO-AIR AVIONICS**

**NAVAL RESEARCH LABORATORY
WASHINGTON, D.C. 20375**

**TECHNICAL
REPORT**



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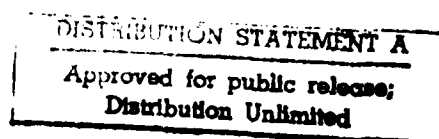
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MANUFACTURING TECHNOLOGY PROGRAM
FOR
HIGH BURNOUT SILICON SCHOTTKY-BARRIER MIXER
DIODES FOR NAVY AIR-TO-AIR AVIONICS

FINAL REPORT
CONTRACT NO. N00173-79-C-0107

PREPARED BY:
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ABSTRACT

This report describes the establishment of low cost semiconductor processes to manufacture low barrier height high burnout X-band silicon Schottky barrier diodes in production quantities. These devices are thermal compression bonded in a rugged low cost pill (ODS-119) package. They exhibit an overall low noise figure of 7.0 dB (single side band) at 0.5 mW of local oscillator power level and RF burnout of 12 watts ($\tau = 1 \mu\text{sec}$ and 10^3 Hz rep. rate). Reliability and ruggedness of the design has been demonstrated by tests taken from MIL.S. 19500F.

I.0 INTRODUCTION

Under U.S. Navy Contracts N00173-C-0029 and N00173-78-C-0126, Microwave Associates has developed low barrier height, high burnout X-band silicon Schottky-barrier diode with a 12 watt RF burnout ($\tau = 1 \mu\text{sec}$, 10^3 Hz rep. rate) characteristics (see Table I and Figures 1 and 2). These devices are thermal compression bonded in a rugged pill (ODS-119) package and exhibit an overall low noise figure of 7.0 dB (single side band) at a 0.5 mW of local oscillator power level.

The purpose of this manufacturing technology program was to establish production processes and technologies for the manufacture of low barrier height and high burnout Schottky-barrier diodes to be used in advanced radar systems for the U.S. Navy. The objective was to demonstrate pilot production fabrication processes in order to realize lower manufacturing costs through applications of high yield processing techniques.

The program consists of a two-phase effort: (a) establishing low cost semiconductor processing and tooling techniques for the pilot line and (b) manufacturing phase, for a period of twenty-four months.

PHASE I

- Low Cost semiconductor chip processing
- Cost reduction in packaging and diode fabrication
- Cost reduction in DC and RF testing (computer-controlled probe stations)

PHASE II

- Pilot line production
- Quality control testing
- Failure Analysis

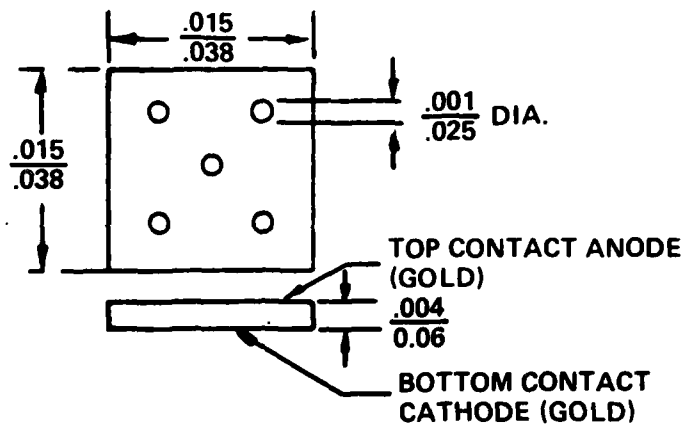
Most of the cost in manufacturing a Schottky chip is in processing of the silicon wafer. The processing of a wafer can be in excess of \$1,000, while the silicon wafer with an epitaxial layer costs in the order of

PERFORMANCE OF X-BAND SCHOTTKY DIODES

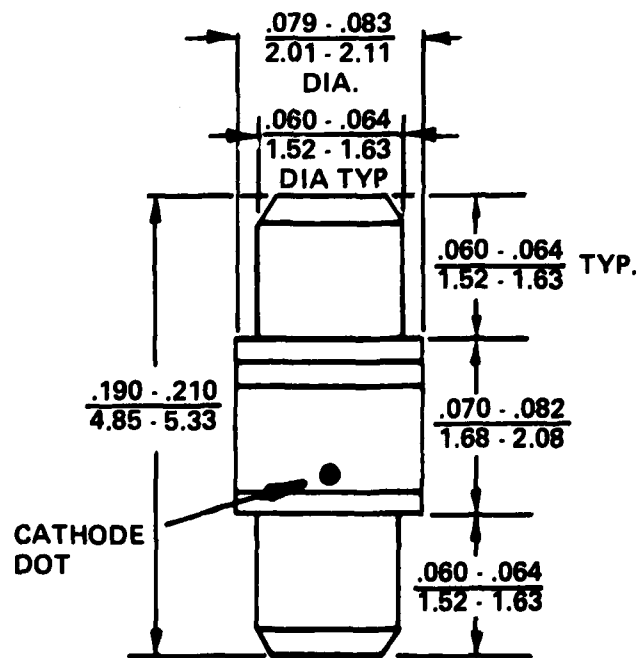
DIODE PARAMETERS	RF PERFORMANCE		
	BEFORE NAVY CONTRACTS	AFTER N00173-77-C-0029	AFTER N00173-78-C-0126
NOISE FIGURE AT 9.375 GHz	7.0 dB	7.0 dB	7.0 dB
L.O. POWER	0.5 mW	1.0 mW	0.5 mW
RF BURNOUT: $F_0 = 9.375$ GHz $\tau = 1 \mu s$ $D_u = 0.001$	2 WATTS	10 WATTS	12-15 WATTS
RF BURNOUT: $F_0 = 9.375$ GHz $\tau = 3$ ns $D_u = 0.001$	15 WATTS	80 WATTS	100-150 WATTS

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TABLE I



(a) SCHOTTKY CHIP



(b) CERAMIC MQM (STYLE 119)

FIGURE 1

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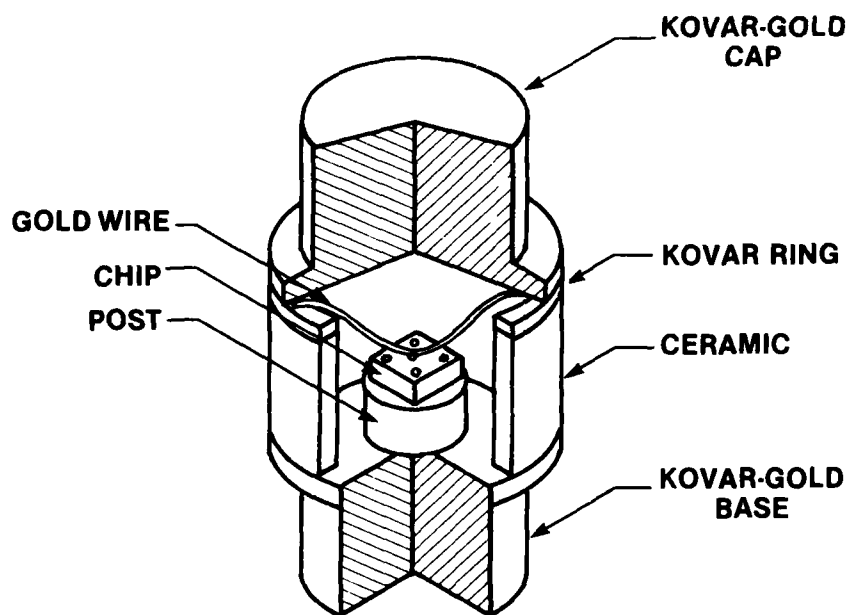


FIGURE 2 MULTIDOT PACKAGED SCHOTTKY DIODE

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\$15. Therefore, the objective is to (1) reduce processing step costs, (2) increase the number of chips per wafer, (processing cost is independent of wafer size), and (3) improve the yield.

The processing steps include wafer characterization, oxide growth, photoresist masking, etching of Schottky windows in oxide, metallization, testing and scribing.

2.0 PROGRAM OBJECTIVES & SCOPE

2.1 Purpose and Objective of Program

The purpose of this program was to establish Pt/Ni-Ti-Mo-Au metallization process using a high volume magnetron sputtering system and low cost processing techniques for the manufacture of low barrier height, high burnout, X-band Schottky barrier diodes for advanced Navy radar systems.

The objective was to demonstrate pilot production fabrication processes in order to realize lower manufacturing costs (from \$30.00 to \$10.00 per diode in production quantities) through the application of high yield processing techniques such as: 3 inch silicon wafer processing, low cost sawing, semi-automated bonding, and computer controlled diode testing stations.

Both the purpose and objective of this contract have been achieved. We have developed new processes and technologies for the manufacture of silicon low barrier height high burn-out X-band Schottky barrier diodes for advanced Navy radar systems. The diode which is the result of this effort meets all contract specifications. We fully expect to sell production quantities of these diodes at a unit price of \$10.00 each or less.

3.0 PROGRAM SCOPE

The program consisted of a two-phase effort for a period of 24 months.

3.1 The specific tasks of this program included:

3.1.1 Establish semiconductor processing and tooling techniques for quantity production diodes using the diode designs developed under NRL Contract No. N00173-77-C-0029 and N00173-78-C-0125.

3.1.2 Establish tolerance limits such that performance requirements are met at minimum cost.

3.1.3 Establish automatic testing procedures and test equipment to provide adequate and sufficient probing of the product at least cost.

3.1.4 Fabricate production diodes in sufficient quantities (1000) to determine that process controls can be maintained when adapted to new process production.

3.1.5 Describe new electrical parameters in MIL-STD-750 format specifications.

3.1.6 Prove out and report data on all fabrication, assembly, processing and measuring steps and procedures to produce the diodes.

3.1.7 Document and report piece-part dimensions, materials, reagents of all manufactured and purchased components.

3.1.8 Initiate a pilot run of 300 preproduction samples and qualify diodes for system implementation.

3.2 Phase I Requirements

The laying out of all semiconductor chip processing steps, package parts and diode fabrication steps. The simplification of all parts for manufacturing ease, work simplification analysis on both assembly of the device and testing, and the adaptation of all required assembly and test jigs, fixtures and tooling to maximize efficiency and minimize required labor and skill.

3.3 Phase 2 Requirements

All manufacturing drawings and process specifications will be finalized. Required manufacturing flow, inspection procedures, and test methods will be fully documented prior to preproduction start-up.

This step will be the preproduction run to prove out all aspects of the manufacturing technology program including documentation derived in 3.2. Three hundred prototypes will be built during this run. One hundred units will be used for qualification testing.

3.3.1 A MIL-STD-19500 format specification shall be prepared based on the electrical, mechanical parameters and performance of these three hundred diodes.

3.2.2 A step-stress testing procedure shall be performed on a reasonable sample of these preproduction diodes in addition to those tests required for system qualification. These step-stress tests will also prove the success of the established manufacturing techniques. The number of candidates and specific type tests called out in MIL-STD-750 shall be determined by mutual agreement.

3.4 Diode Specification

The 300 hundred prototype samples to be built under Phase 2 shall meet the following specifications:

<u>Diode Parameters</u>	<u>Proposed Contract Specifications</u>
NF at 9.375 GHz	7.0 dB (max) SSB
LO Power	0.5 mW
RF Burn Out at	12 W
$F_o = 9.375$ GHz	
$\tau = 1$ μ sec	
$D_u = 0.001$	

4.0 TECHNICAL REPORT - PHASE I

Phase I of this Program consisted of optimizing the processing and of transferring the process technology to high throughput systems to increase yields and reduce cost. Process specifications were written and documented. Engineering samples were fabricated, DC and RF tested, and shipped on schedule.

4.1 Wafer Processing

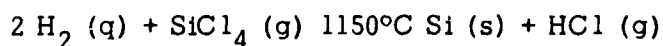
Operating procedures have now been established for all phases of wafer processing. These processes are outlined in Table II. Specifications for these processes have been written and documented. Test lots of wafers have been processed to confirm process repeatability and yield. Process steps are summarized in Figure 3. Specific areas of work are discussed in the following sections.

4.2 Silicon Epitaxial Wafer Characterization

The epitaxial layers to be used must have, (a) a very low crystallographic imperfection density in order to ensure minimization of avalanche noise, (b) excellent surface morphology, and, (c) exactly the correct epitaxial layer doping level, abrupt interface, and thickness to ensure lowest possible device series resistance.

4.3 Silicon Wafer Processing and Evaluation

Epitaxial growth was accomplished by the hydrogen reduction of silicon tetra-chloride as given below:



Hydrogen is bubbled through silicon tetra-chloride liquid, under controlled saturation conditions, whereby a constant partial pressure of hydrogen is maintained by mass flow controls. A mass flow controlled partial pressure of dopant gas is injected and thoroughly mixed in an inlet chamber prior to entering the epitaxial growth reaction chamber, thereby enabling closely controlled dopant (resistivity) and growth rate control. The substrates are placed on a silicon carbide-coated graphic susceptor, heated

<u>OPERATION</u>	<u>EQUIPMENT</u>	<u>CONTROLS</u>
1) Grow Silicon Crystal	Semi-Metals Crystal Puller Model 5108	Micrometer
2) Slice Crystal	Dual Micromatic Model #1427	Actual Slice
3) Check Resistivity	Jandell Four Point Probe	Actual Slice
4) Etch Slices	Micro Air Hood	Visual Timed
5) Polish Slices	Semi-Metals Polisher Model #22	Visual
6) Grow EPI Layer	Applied Materials AMV 1200	Mass Flow Controllers
7) Check EPI Layer Thickness	HPL000 Mercury Probe and Phites Bevel & Stain	Measure
Check EPI Layer Resistivity	Mercury Probe & Phites Bevel & Stain	Actual Slice
8) Clean Wafers	Micro Air Hood	Visual
9) Chemical Vapor Deposit Oxide	ASM LTO System	Alpha Step Surface Profiler & Rudolph Auto El Ellipsometer
10) Open Window for Schottky & Junction	Cobilt CA-800 Photo Aligner	Visual
		Vickers-Image-Shere microscope

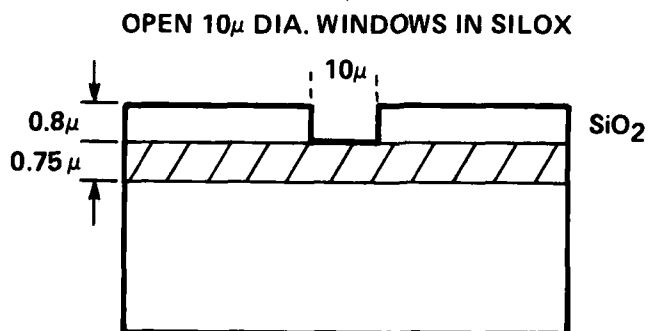
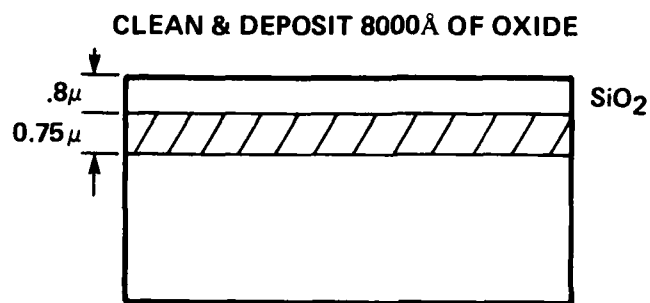
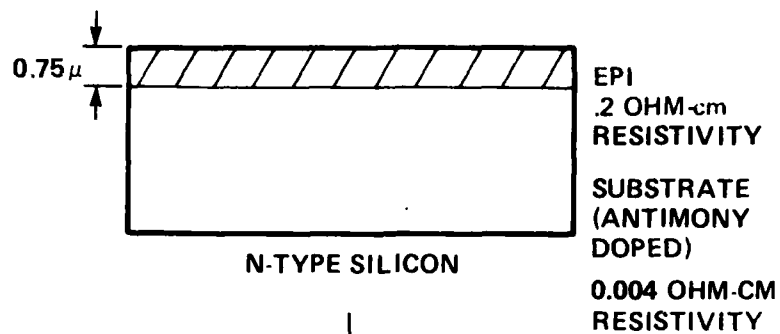
TABLE II SCHOTTKY BARRIER DIODE CHIP FABRICATION

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<u>OPERATION</u>	<u>EQUIPMENT</u>	<u>CONTROLS</u>
11) Etch Windows	Plasma Therm Model PK-12	End Point Detector
12) Strip Resist	IPC Model 2005X Plasma System	End Point Detector
13) Metal (Pt. -Ni.)	Materials Research Corp	Alpha-Step
14) Sinter	Lindburg Diffusion Furnace	Timer
15) Metal (T/W-Au)	Materials Research Corp	Alpha-Step
16) Mask Metal for Etch	Cobilt CA-800 Photo Aligner	Visual-Vickers Scope
17) Etch Metal	IPC Model 2005X Plasma System	End Point Detector
18) Strip Resist	IPC Model 2005X Plasma System	End Point Detector
19) Plate Buttons	Power Supply, Au Bath	Unitron Model TM25 Scope
20) Mount & Lap Back	Speed Fram Model 12B Lapper	Micrometer
21) Metalize Back	Ni Bath-Au Bath-Power Supplies	"Tape Test" -Visual
22) Dismount & Clean	Micro Air Hood	Visual
23) Electrical Probe Wafer	M/A Automatic Probe Station with HP-3000 Computer	
24) Dice Wafer	Disco-I	Micro Processor
25) Dice Approval	Nikon IC Inspection	Visual Inspect
	Microscope	

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TABLE II (CONTINUED)

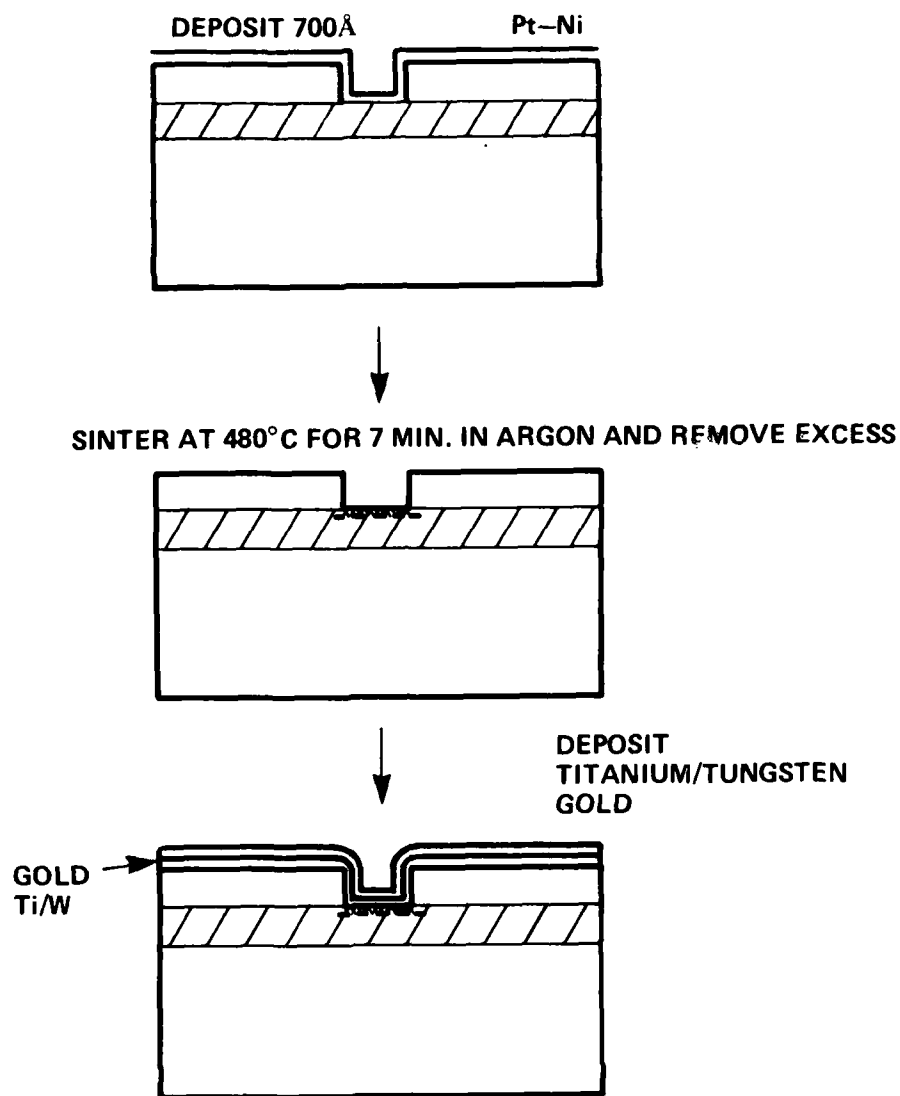


PROCESS STEPS FOR HIGH BURNOUT,
BARRIER SCHOTTKY DIODE

LOWER BARRIER PtNi-Ti/W-Au

FIGURE 3 (a)

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FIGURE 3 (b)

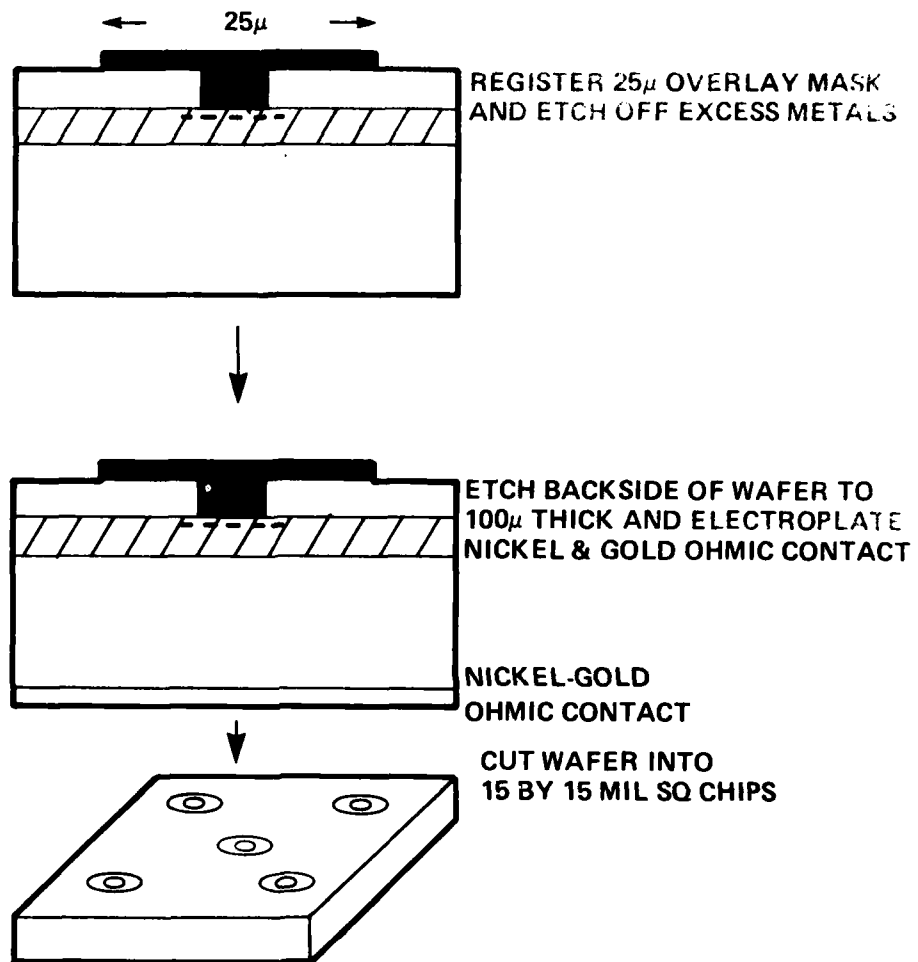


FIGURE 3 (c)

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to ~1150°C (optical pyrometer temperature), where they are etched in-situ by HCl vapor to remove any possible surface mechanical damage. After purging for a given time and stabilizing partial pressures of the reactant gases, these gases are allowed into the epitaxy chamber whereby controlled growth is accomplished.

Epitaxial growth was performed in an AMV-1200 vertical reactor (See Figure 4).

4.4 Characterization of Epitaxial Wafers

The following techniques are available to characterize and evaluate silicon epitaxial wafers:

- (a) Infrared Spectrometer to evaluate epitaxial thickness^[1].
- (b) Copeland Inversion Profiler^[2].
- (c) Spreading Resistance (Four Point Probe)^[4].
- (d) Differential Capacitance Profile or Mercury Probe^[4].
- (e) Bevel and Stain^[5].
- (f) Digi-tab FTG-12 Thickness Monitor^[6].

The Copeland Inversion Profiler^[2], surface spreading resistance probe^[3], and mercury probe^[4], can characterize epitaxial layer concentration (resistivity), and a portion of, if not the entire epitaxial layer/substrate interface. The actual data attainable by each method is a function of layer thickness and carrier concentration.

For measurement and characterization of epitaxial thickness, uniformity across each wafer, and distribution throughout a given run, the available techniques are: infrared spectrometer^[1], digi-tab FTG-12 thickness monitor^[6], and bevel and stain method^[5]. Again, the utility of each technique is a function of the layer thickness, substrate type, and optical constants.

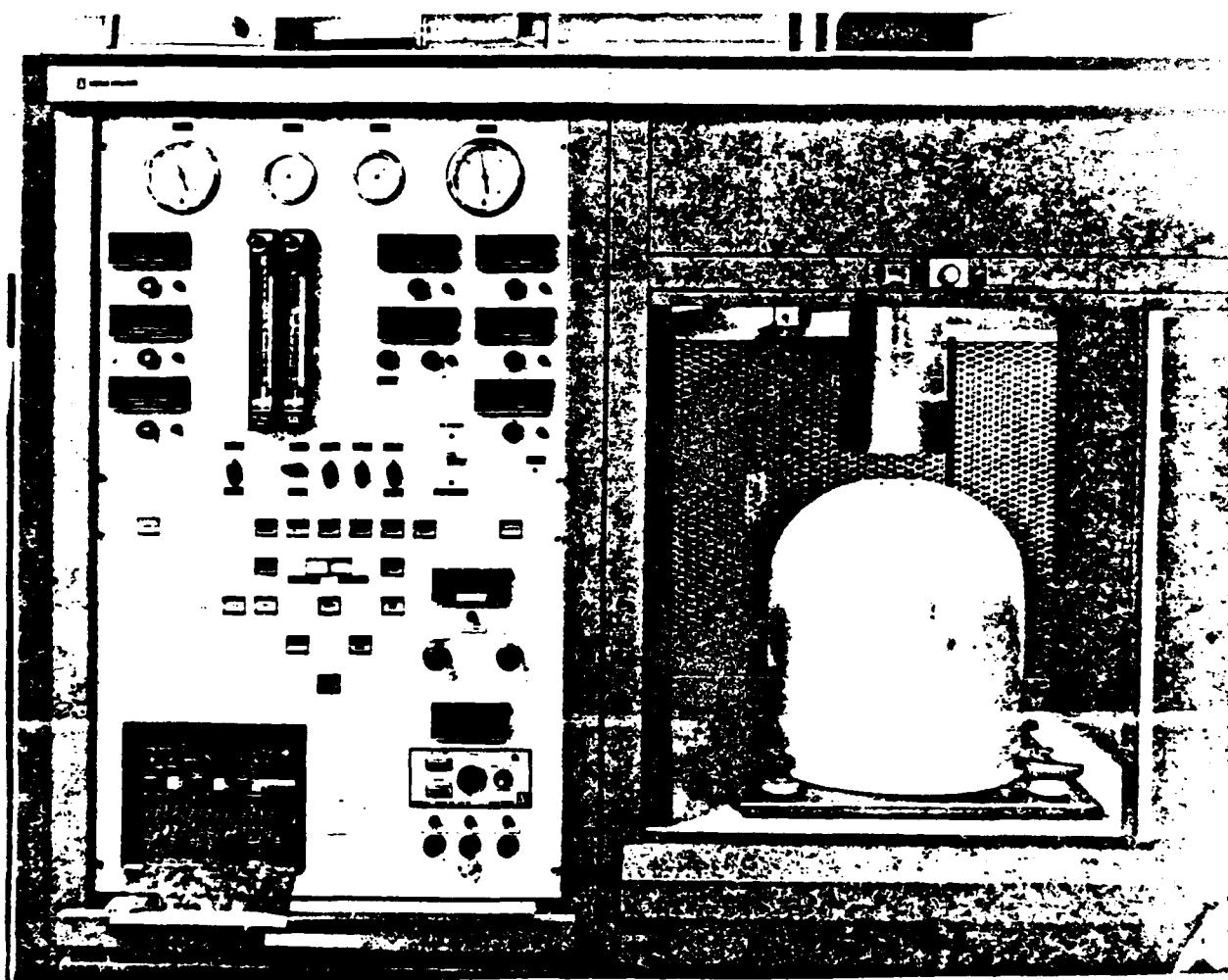


FIGURE 4 AMV-1200 VERTICAL EPITAXIAL REACTOR

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Epitaxial layers of thickness less than $\leq 0.5 \mu\text{m}$ and of low resistivity $\leq 0.5 \Omega \text{ cm}$ are very difficult to measure accurately. Most of the previously mentioned techniques such as, Infrared Spectrometer, (only good for epi thickness $\geq 5 \mu\text{m}$, and Copeland Profiler, (only good for $\geq 2 \mu\text{m}$), are not reliable and do not give reproducible measurements.

A mercury probe with HP1000 computer, (see Figure 5) and bevel and stain methods being evaluated for the measurements of epitaxial thickness and resistivity. The mercury probe set-up consists of an automatic bridge, DC power supply, digital voltmeter, mercury probe, and HP1000 computer. The mercury probe's template forms non-destructive 20 mil Schottky junctions on an epitaxial silicon. Computer varies the reverse bias voltage and then plots capacitance versus voltage and doping density versus junction depth using the following equation:

$$N = \frac{C^3}{q \epsilon A^2 \frac{dC}{dV}} \quad \text{and} \quad X = \frac{\epsilon A}{C}$$

- A = junction cross sectional area
- C = junction capacitance
- q = charge of n-electron
- ϵ = material dielectric constant
- N = material carrier density
- X = depth at which N is measured

Various measurement steps are given in Figure 6. This method is fast and non-destructive. It gives an accurate value of doping density (carrier concentration) of the epitaxial layer approximate value of the epitaxial thickness. Typical doping curves and contour maps of 3" wafers are shown in Figure 7. This method is fast and non-destructive.

Unfortunately, in many cases (especially highly doped layers), Schottky diodes formed by a mercury contact breaks down before the epitaxial layer is fully depleted. So another method to measure the epitaxial layer thickness accurately was required.

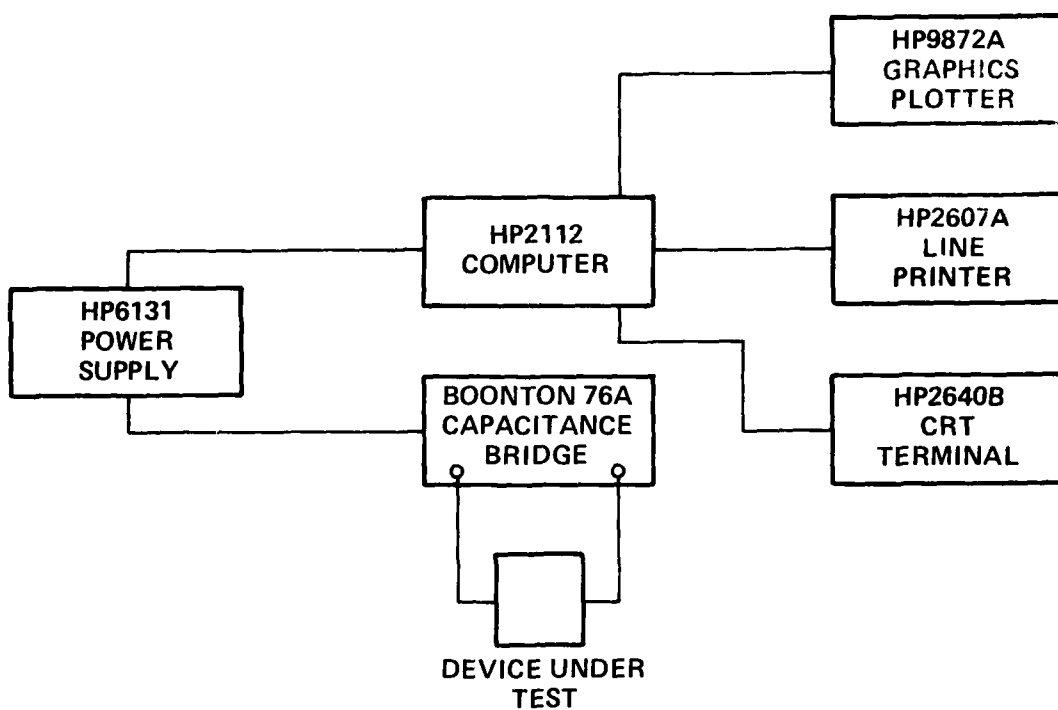
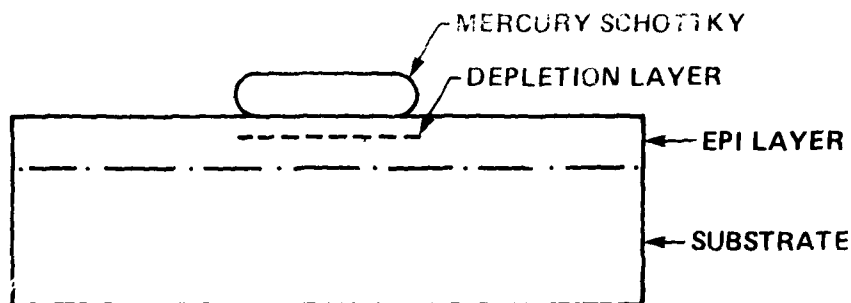


FIGURE 5 AUTOMATIC DOPING PROFILE MEASUREMENT SYSTEM

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- A) FORM Hg SCHOTTKY
- B) MEASURE JUNCTION CAPACITANCE AS A FUNCTION OF VOLTAGE (REVERSE BIAS)
- C) CALCULATE DOPING PROFILE AND DEPTH:

$$N = \frac{C^3}{q \epsilon A^2 \frac{dc}{JV}}$$

$$X = \frac{\epsilon A}{C}$$

A = JUNCTION CROSS-SECTIONAL AREA

C = JUNCTION CAPACITANCE

N = MATERIAL CARRIER DENSITY

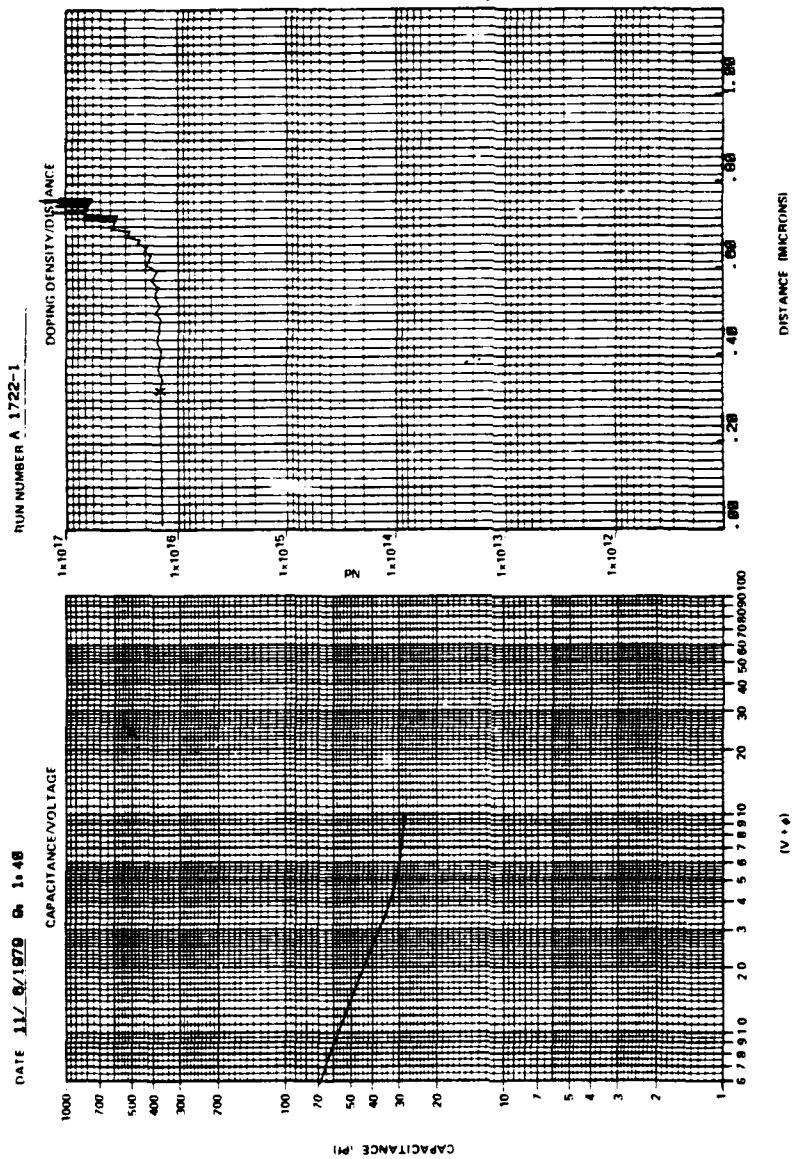
q = CHARGE OF ELECTRON

X = POSITION (DEPTH) AT WHICH n IS DETERMINED

ϵ = MATERIAL DIELECTRIC CONSTANT

FIGURE 6 MERCURY PROBE CALCULATIONS

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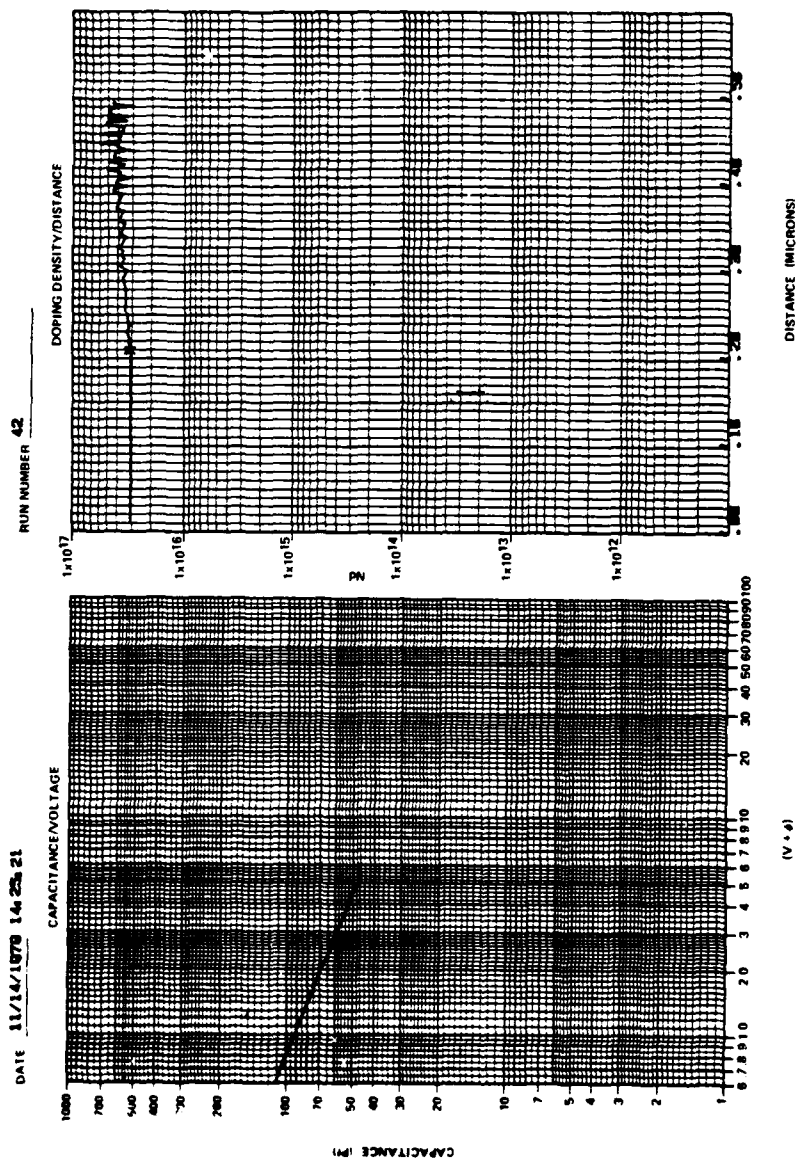
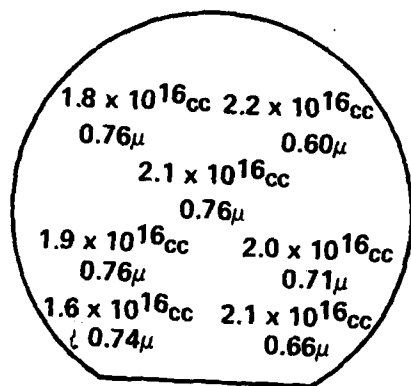
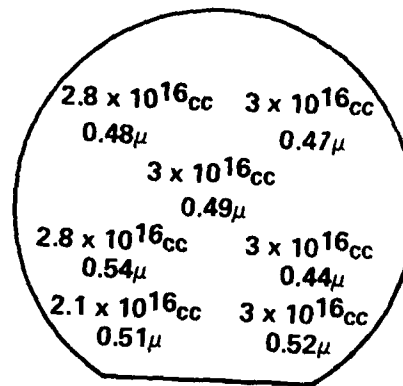


FIGURE 7 (b) ACTUAL PLOT

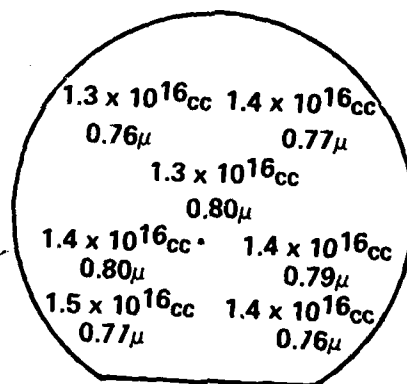
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A-1742



A-1722

FIGURE 7 (c) MAP OF Hg PROBE MEASUREMENTS ON 3" WAFER

D-19368

This was achieved by using a Philtec Model 2015-D Bevel and stain system. The process involves cutting a groove of cylindrical shape into a specimen (epitaxial silicon wafer n/n+), and then staining the groove in a manner which delineates the less negative layers. Then under magnification, two variables are measured which can be substituted into a simple equation to calculate the thickness of epitaxial layers as shown in Figure 8. The experimental measured parameters in Figure 8 are X and Y; and R is the known radius cylinder. The comparison between mercury probe and Philtec results are given in Table III and show that for a low doped material (wafers A-1722 and A-1743), the results are approximately the same by the two techniques, but differ for moderately doped material (wafer A-1743) due to premature breakdown of mercury Schottky diodes.

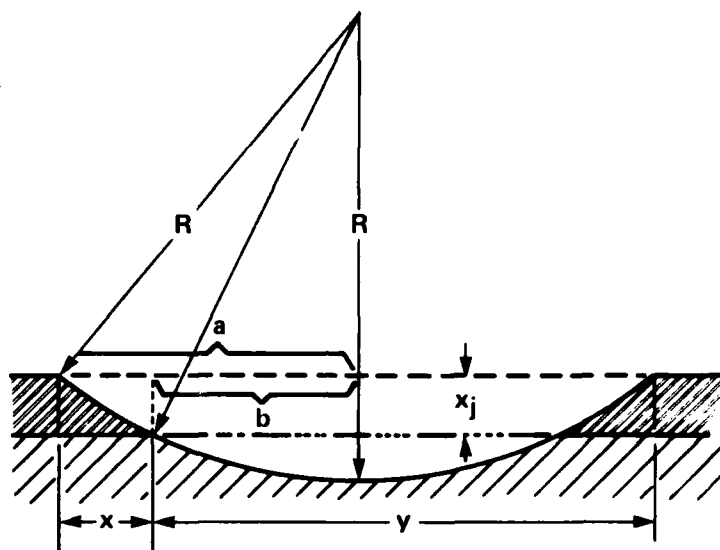
This bevel and stain technique provide the method for the precise measurement of ultra thin epitaxial layers. The mercury probe and Philtec bevel and stain techniques enable us to completely characterize 3 inch epitaxial wafers. The wafers which do not meet the required specifications will be rejected and thus reduce the overall cost of the production diodes. The bevel and stain techniques also provide a method of detecting a layer (unwanted) between a substrate and an epitaxial layer.

4.5 Measures for Reducing Wafer Processing Costs

Efforts were concentrated on transferring the technology process to higher throughput systems, specifically in the areas of: (a) conversion from RF sputtering to automatic magnetron sputtering, (b) conversion from wet (chemical) to dry (plasma) etching and stripping, and (c) dicing of wafers.

4.6 High Volume Planar Magnetron Sputtering System

The planar magnetron sputtering process was invented by John Chapin^[11] in 1972. It was further improved to its present stage of very versatile production sputtering system by Materials Research Corporation and Vacuum Industries. It overcomes many of the problems of RF sputtering such as slow rate, poor uniformity, poor power efficiency, and radiation damage.



$$X = a - b$$

$$Y = a + b$$

$$X_j = \sqrt{R^2 - b^2} - \sqrt{R^2 - a^2}$$

WHEN $b \ll R$

$$X_j = R \left[1 - \frac{1}{2} \frac{b^2}{R^2} - 1 + \frac{1}{2} \frac{a^2}{R^2} \right]$$

$$X_j = \frac{1}{2} \frac{a^2 - b^2}{R}$$

$$X_j = \frac{1}{2} \frac{(a + b)(a - b)}{R}$$

$$X_j = \frac{1}{2} \frac{XY}{R}$$

FIGURE 8 PHILTEC BEVEL AND STAIN METHOD

D-19369

WAFER #	PHILTEC	MERCURY PROBE
A-1722	0.80	0.76 0.79
A-1742	0.72	0.50
A-1743	0.78	0.76

TABLE III COMPARISON OF RESULTS

D-19370

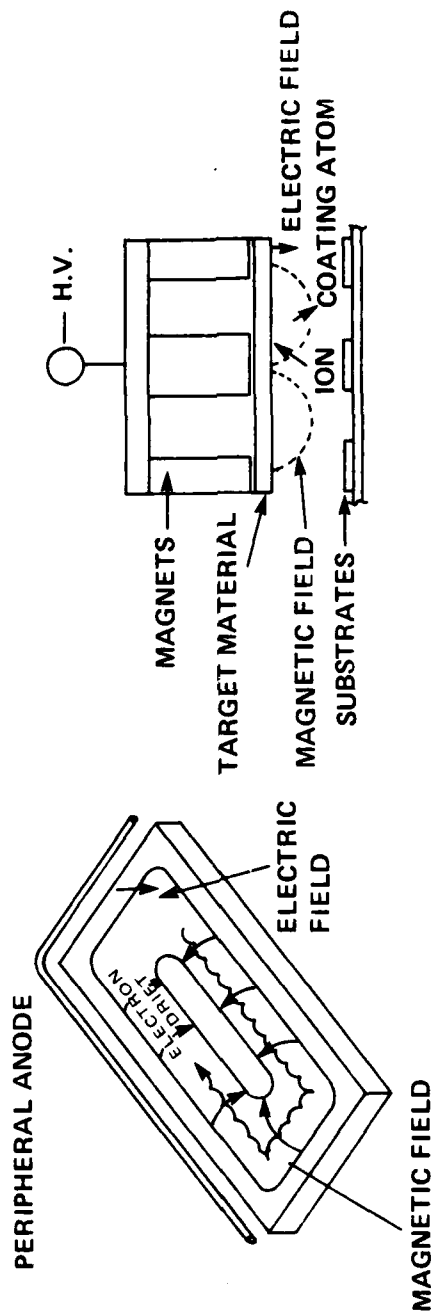


FIGURE 9 PLANAR MAGNETRON CATHODE

D17119

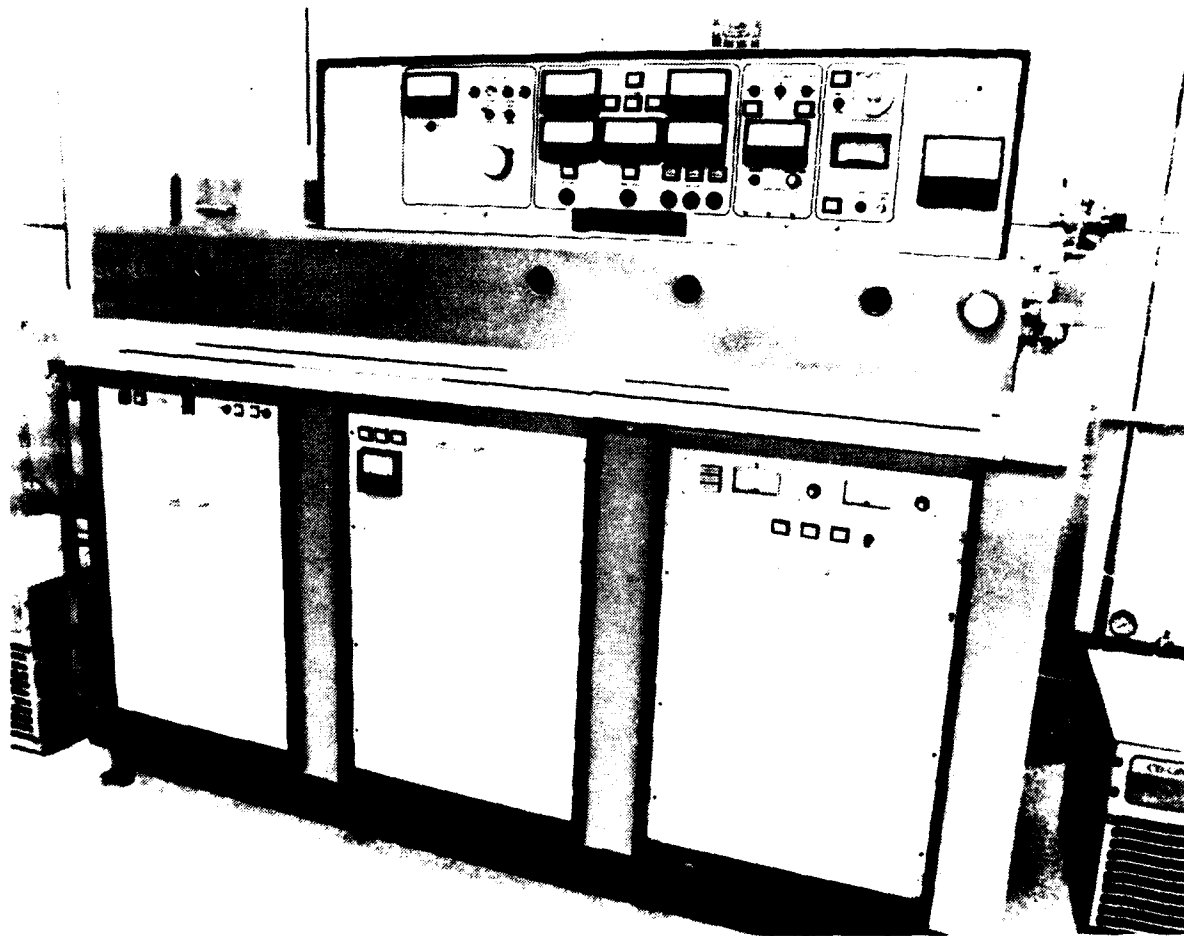


FIGURE 10 MRC MAGNETRON 900 METAL DEPOSITION SYSTEM

D 1645P

The planar magnetron technique is based on a closed magnetic field loop (see Figure 9) using a planar sputtering target. The concept evolved in part from the Penning's magnetron which was patented in 1933^[12] and work performed by Van Vorous, Mullaly, Karstendick, and others with magnetically field enhanced rectangular box type sputtering sources and quadruple filled sources.

Magnetron sputtering is currently being employed for production metallization of microelectric circuits, microwave power and low noise semiconductor devices. Typical materials deposited are aluminum, aluminum-silicon, titanium-tungsten, alloy, platinum, titanium, molybdenum, palladium, gold and others.

Sputtering offers a reliable method of depositing alloys and mixtures with assurance that the film composition will not change from deposition to deposition. The source material will last for a large number of depositions without the need for replenishment.

An added advantage of magnetron sputtering is that the entire deposition process can be automatic such as, evacuation, substrate heating, sputter etching, argon backfill and deposition. This means that the quality of the vacuum metallization is no longer dependent upon the skill of the operator. Magnetron sputtering along with micro-processor automation of the equipment assures the same uniformity, run after run, on multi-production shifts day after day.

Advantages of magnetron sputtering to that of RF diode sputtering are:

(a) Large batch loading can be accomplished in magnetron sputtering (see Figure 10) MRC 903. Presently at Microwave Associates, Inc., we have the capability of metallizing 132 three-inch wafers per one eight hour shift, as compared to only 18 three-inch wafers in the RF diode systems (Model MRC-90).

(b) Precise deposition control ($\pm 200 \text{ \AA}$ units) can be accomplished in the micro-processor system where the depositing material can be sensed 60 times/minute and adjustments to deposition thicknesses are made each second to insure precise thickness control, run after run. Operator hands on time is reduced to 1/3 that of the operator's time in operation of manual RF diode systems (Model-90).

SYSTEM	3" WAFER/DAY	UNIFORMITY	OPERATOR TIME/HANDS ON	TOTAL FACTORED COST/WAFER PT-TI-Mo-Au	PT-TI-W-AU
MAGNETRON MRC-903	132	$\pm 200 \text{ \AA}$	1/3 LESS	80¢/W	60¢/W
RF MRC-90	18	$\pm 500 \text{ \AA}$	---	\$9.00/W	\$8 /W



TABLE IV. COMPARISON OF DIFFERENT METALLIZATIONS

Test lots of wafers were run through this system and preliminary specifications established. Results showing cost reductions are summarized in Table IV.

4.7 Plasma Etching of Silox Photo-Resist and Metallization

A plasma etcher (IPC-Model 2005-X) is being used to etch silox, photo-resist and unwanted titanium and molybdenum metals from silicon wafers. This process offers many advantages over wet chemistry techniques such as, (a) higher batch yields, (b) residue-free etching, (c) minimum undercutting, and (d) faster and less expensive than wet chemical etching.

The equipment consists of a quartz chamber inductively coupled to a high frequency oscillator (13.56 MHz) (see Figure 11). The chamber is evacuated to between 0.01 and 0.1 torr and then filled with the etch gas ($\text{CF}_4 - \text{O}_2$ for refractory metals and for silicon nitride, anhydrous HF for silox). The RF power is then switched on and reactive gas is excited forming a plasma of atomic fluorine, free ions, radicals and electrons. Atomic fluorine is considered to be a major reactant for etching exposed surfaces. Photo-resist, which etches slower, is used to mask surfaces. The IPC "Dry-Ox" System utilizes a special process to selectively etch oxides without attacking the underlying silicon. An oxygen plasma is used to strip photo-resist from the wafers after they are etched.

The plasma process yields much greater uniformity within a run and better reproducibility from run-to-run. Once the process is established by engineering personnel, the operator need only load and unload the system. Uniformity of better than $\pm 5\%$ reproducibility run-to-run has been experienced. In wet chemical etching, wafers are generally etched one at a time and the process is time consuming, unreliable and dependent upon the operator's judgement. Comparison of typical process times for wafer etching and removal of photo-resist are shown in Tables V and VI.

4.8 Low Cost Dicing of Wafers

Once processing is complete, the wafer must be cut into chips. Previously, the wafers were saw cut with the Tempress Saw Model-602, which is a high cost and low yield operation, typically ten three-inch wafers per day. Initially, we had hoped to replace this operation with laser scribing in

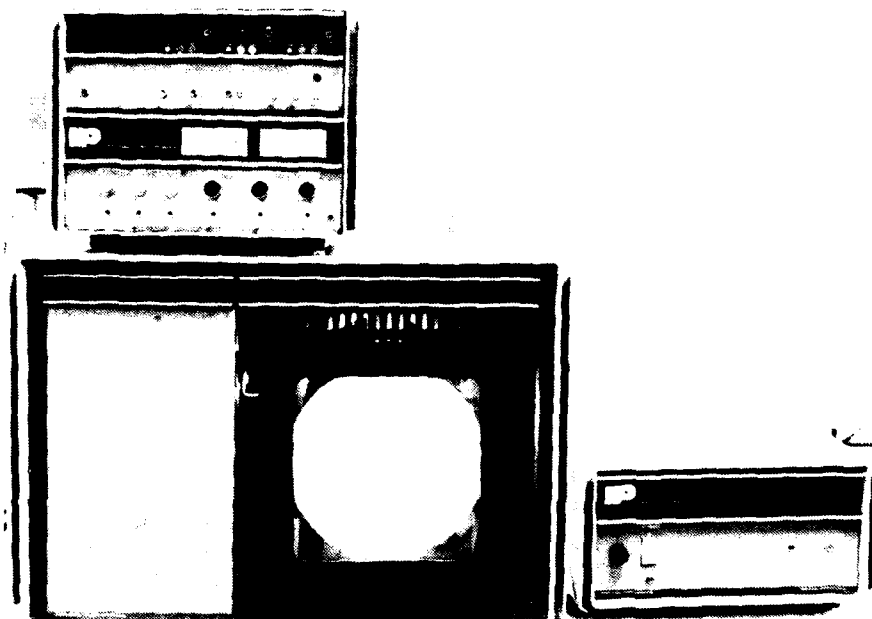


FIGURE 11 INTERNATIONAL PLASMA CORPORATION PLASMA
ETCHER FOR NITRIDE AND OXIDE ETCH

D-16466

TYPE	CYCLE TIME	3" WAFERS/CYCLE	AVG REWORKS	WEEKLY MATERIALS COST	TOTAL COST/WAFER
PLASMA	15 MIN	50	2%	<\$ 1	\$ 0.10
WET CHEMICAL	15 MIN	4	5%	\$ 50	\$ 1.30
J-1000R712D	15 MIN	4	15%	\$ 37	\$ 1.25

TABLE V. COMPARISON OF METHODS OF RESIST STRIPPING



TYPE	CYCLE TIME	WAFER/CYCLE	UNIFORMITY	YIELD	WEEKLY MATERIAL COST	TOTAL COST/WAFER
PLASMA	3-15 MIN	50	± 5%	90%	\$ 5	10 - 15¢
WET CHEMICAL	1-5 MIN	1	±10%	80%	\$ 100	\$2.00

TABLE VI. COMPARISON OF METHODS OF ETCHING WAFERS



the Quantrix Model 603-C, which offers much higher throughput (up to 150 wafers per day) and improved yields. However, because of continued maintenance problems, with a down-time of over 60%, it was decided to investigate one of the new high-speed automated saws, in this case the Disco I. After experimentation and optimization of operating parameters, this was the most cost effective method of cutting wafers. Results of this work are summarized in Table VII. We are now using Disco II, a fully automated version of the Disco I.

TYPE	3" WAFERS/DAY	METHOD	KERT LOSS	% YIELD	DOWNTIME	FACTORED COST/WAFER
TEMPRESS	8	SAW	2 MILS	75%	20%	\$30
LASER SCRIBE	150	SCRIBE	0.5 MIL	80%	60%	\$21
DISCO (I)	24	SAW OR SCRIBE	0.8-2.0 MILS (ADJUSTABLE)	85%	10%	\$ 8.5
DISCO (II)*	48	SAW OR SCRIBE	0.8-2.0 MILS (ADJUSTABLE)	85%	10%	\$ 4.25

TABLE VII. COMPARISON OF VARIOUS METHODS OF DICING WAFERS

DA

7.0 AUTOMATIC WAFER PROBE TESTING

Microwave Associates, Inc. designed and built an automatic test system for wafer probing and testing packaged Schottky barrier diodes. The test system measures junction or total capacitance at various bias voltages, breakdown voltage, leakage current at various bias voltages, and forward voltage drop for various forward currents. The system has been designed specifically for static discharge sensitive Schottky barrier diodes. Techniques for transient suppression have been used to avoid damaging the devices being measured. Specific measures have been taken to obtain capacitance data with high accuracy and reproducibility. A Boonton 76A, the highest sensitivity capacitance bridge available today, is used for the capacitance measurements. By processing data on forward voltage versus forward current the DC slope resistance of the diodes can be obtained.

The automatic system uses an HP 9825 as the system controller. A dual floppy disc data storage unit is utilized to swap subroutines in and out of the controllers read and write memory quickly. The techniques of swapping subroutines quickly enhances the apparent size of the system's read and write memory capability. Figure 12 shows a block diagram of the system. This system can provide a printed record of all devices tested.

On a second automatic test system for silicon junction devices, a wafer prober has been modified to measure accurate capacitance of microwave diodes. A special probe and shielding arrangement was developed so that the fringing capacitance is invariant to position across the slice with ± 0.001 pF. This design permits device junction capacitance to be measured to the same accuracy, namely ± 0.001 pF. The measurement technique has been very successful in providing accurate data for C-V profile analysis and parameter distribution data for the silicon devices.

For this program, the wafer prober has been modified for accurate capacitance measurements and interfaced to the automatic test kit for Schottky barrier diodes (see Figure 13). The resulting automatic test system permits both accurate C-V profile analysis of the Schottky barrier diode slices and complete 100% wafer level DC testing of the diodes. This data is being analyzed for patterns of parameter distribution across each slice for feedback on the success or failure of various processing methods. The test system also allows us to mark and avoid packaging any bad diodes, thereby reducing package and labor overhead cost.

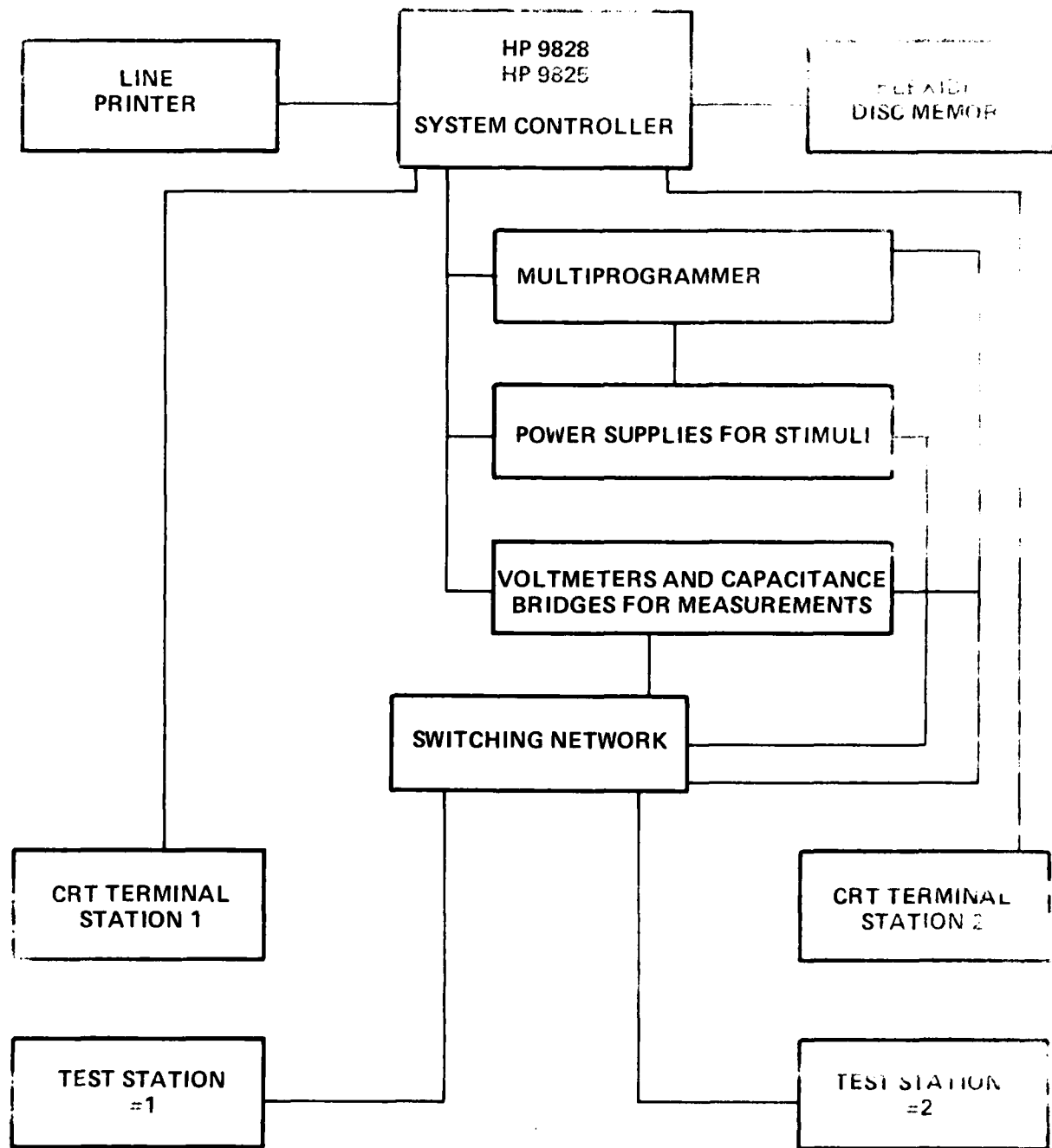


FIGURE 12 DUAL STATION AUTOMATIC TEST SYSTEM FOR
PACKAGED SCHOTTKY BARRIER DIODE

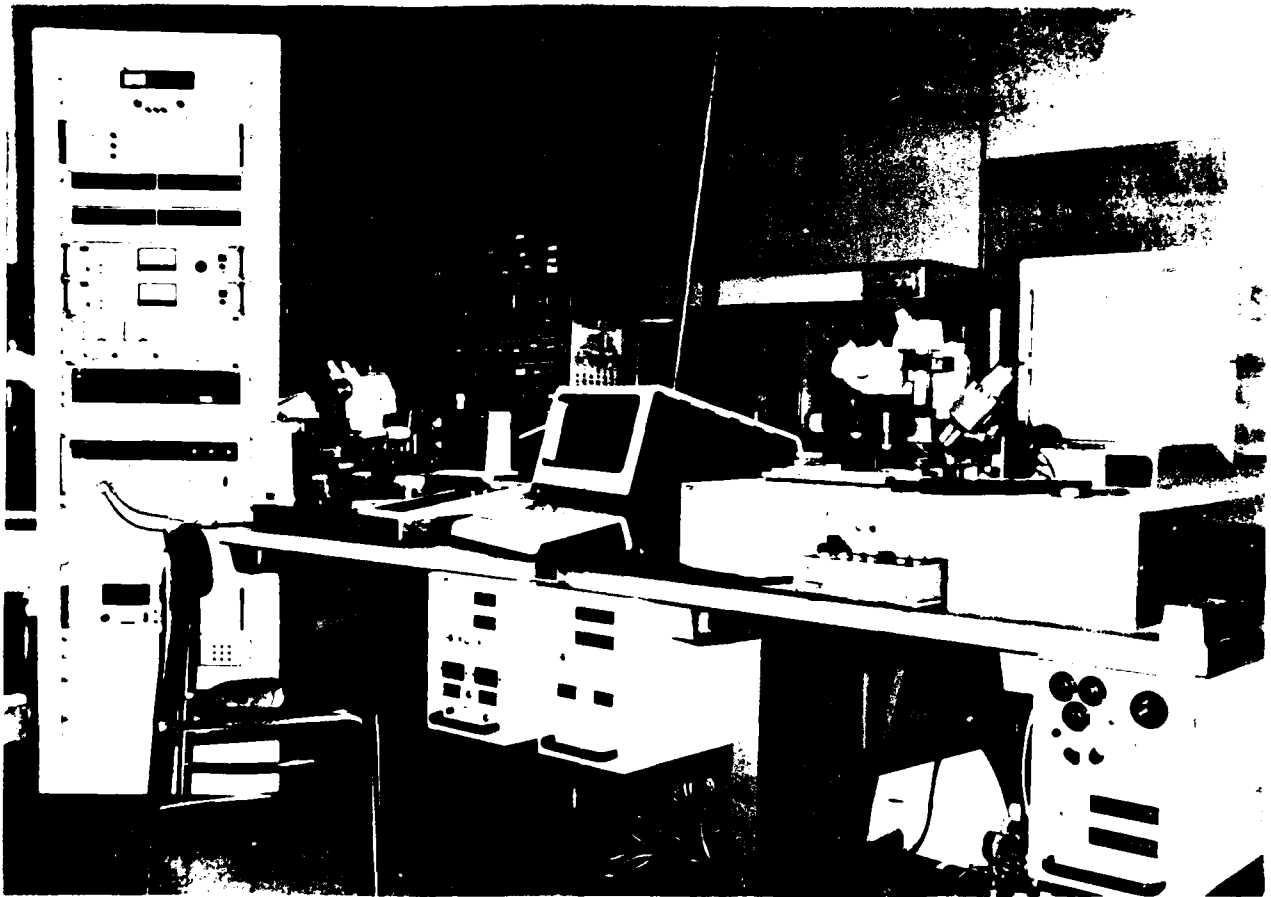


FIGURE 13 COMPUTER CONTROLLED AUTOMATIC SCHOTTKY
WAFER PROBER

D 17136

6.0 MEASURES FOR REDUCING CHIP PACKAGING COSTS

6.1 Low Cost Ceramic Package Assembly

Efforts were directed at reducing the cost of assembly labor. The standard ceramic, ODS-119 package assembly is shown in Figure 14. In the case of low cost packages, the brazing alloy is directly deposited on both ends of the ceramic cylinders. This process provides a more uniform deposition of the brazing alloy, thus elimination of the brazing washers as shown in Figure 15 and 16.

This low cost package assembly eliminates the two small washers, which previously had to be handled individually by an assembler, and also enables us to mechanize the assembly process. This also improves the quality of the final product with increased production capability and reduces the overall cost of the package assembly as shown in Table VIII.

Copper cap and base are used to further reduce the cost of the package from 0.45¢ to 0.39¢ each. Further cost reduction of the package may be realized by substituting palladium, nickel or silicon-platinum for gold plating of the package (see Table IX).

6.2 Low Cost Semi-Automatic Bonding and Capping

Chip bonding is performed on a Mech-El hot gas bonder. A gold tin solder preform is picked up by a vacuum tip and placed on the package pedestal. Next, a silicon chip is picked up and placed in the same manner so that it is resting on top of the solder preform. The operator then releases a stream of hot forming gas which melts the solder and attaches the chip to the package pedestal (see Figure 17).

Thermocompression wire bonders are used to wire bond semiconductor chips inside the ceramic package. In the past, Kulicke and Soffa Model 420-D thermocompression wire bonders were used exclusively.

On the Kulicke and Soffa wire bonders, the operator must control two hand operated micro-manipulators and one foot pedal. One micro-manipulator controls the position of the bonding tips, while the other controls the position of the gold wire. The foot pedal operates the wire feed.

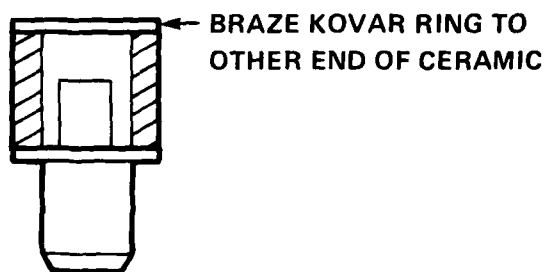
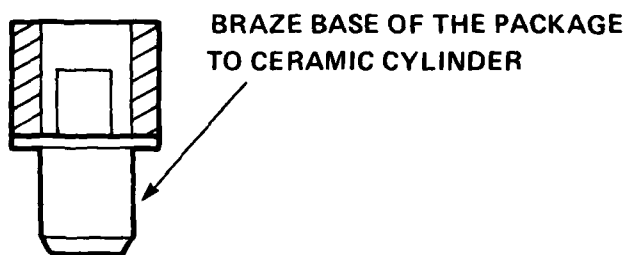
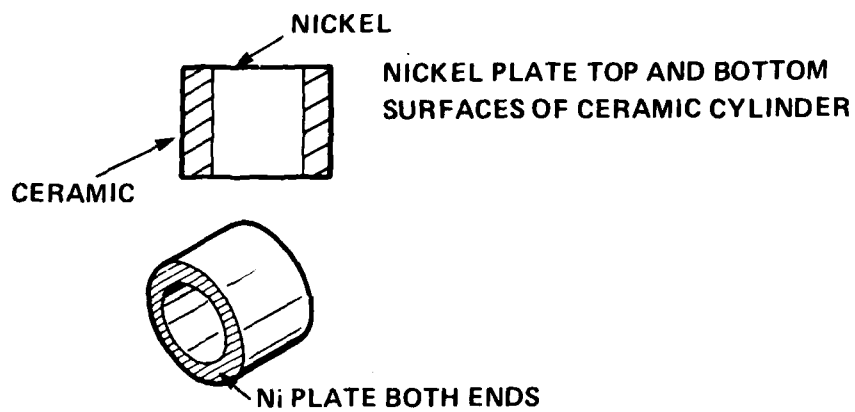


FIGURE 14. STANDARD CERAMIC PILL (ODS-119)
PACKAGE ASSEMBLY

D-17112

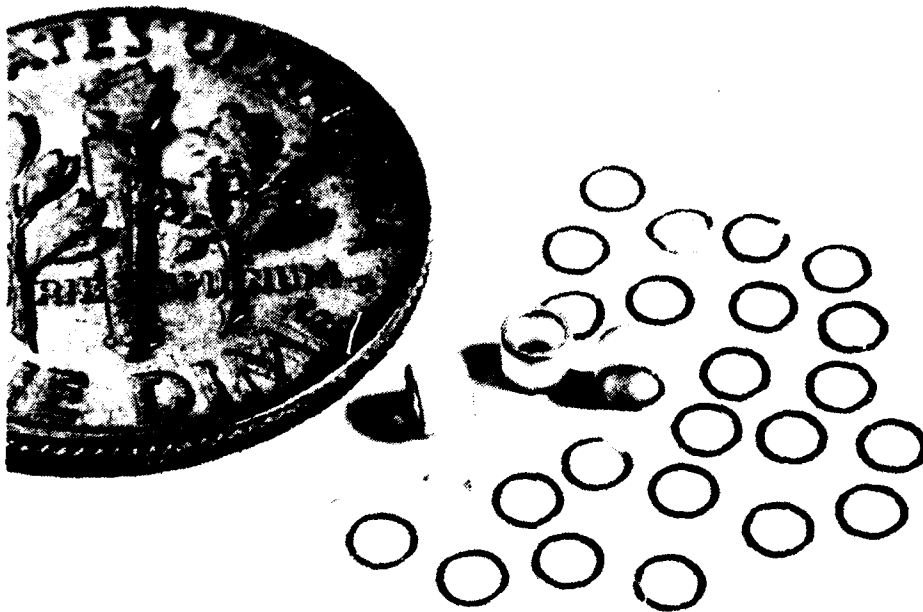


**FIGURE 15 CERAMIC PILL PACKAGE ASSEMBLY WITH BRAZING ALLOY
SEPARATE WASHERS (PRESENT METHOD)**

D-17135

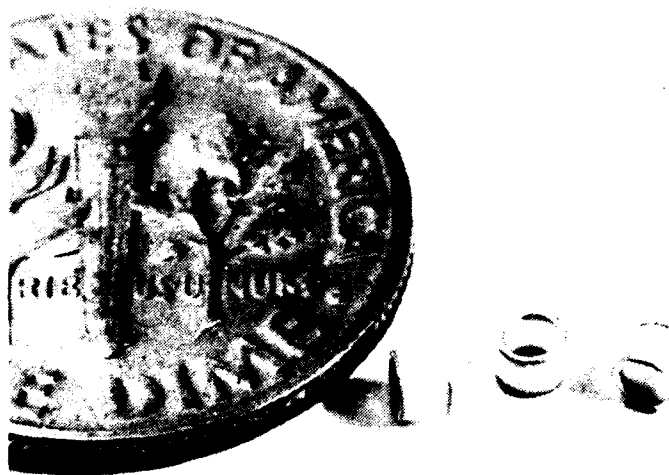
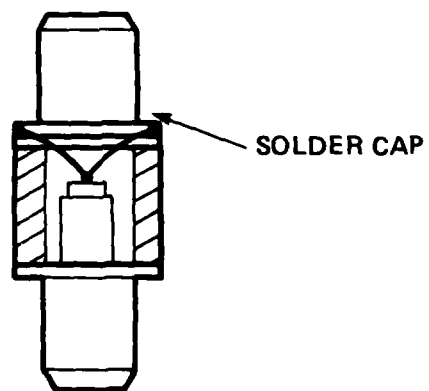
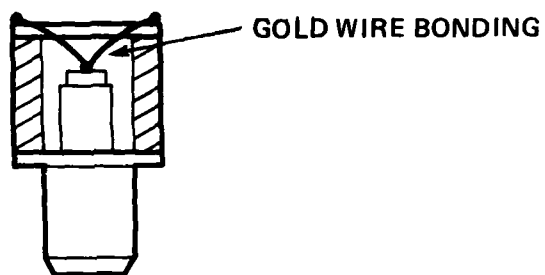
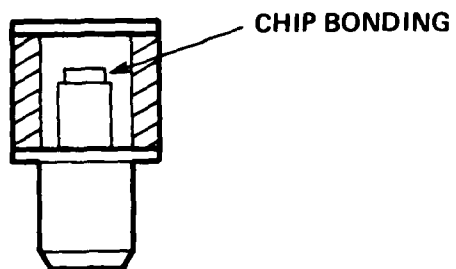


**FIGURE 16 LOW COST CERAMIC PACKAGE ASSEMBLY WITH BRAZING
ALLOY DEPOSITED ON CERAMIC**

D-17134



D-17113

FIGURE 17 DIODE PACKAGING

	<u>PAST</u>			<u>PRESENT</u>
KOVAR CAP	6.3¢		COPPER CAP	1.2¢
KOVAR BASE	6.0¢		COPPER BASE	1.8¢
OTHER PARTS	<u>5.0¢</u>		OTHER PARTS	<u>5.0¢</u>
TOTAL COST	17.3¢		TOTAL COST	8.0¢

REDUCED TOTAL PIECE PART COST 9.3 CENTS BY SWITCHING FROM KOVAR CAP
BASE TO COPPER CAP BASE.

TABLE VIII
DESIGN IMPROVEMENTS - PIECE PART
COST REDUCTIONS

METAL	PRICE/TROY OZ.	COST/UNIT
GOLD (PRESENT PROCESS)	\$ 600	\$ 0.032
PALLADIUM - 80%	\$ 160	\$ 0.0038
NICKEL - 20%		
(PROPOSED)		
SILVER (PROPOSED)	\$ 50	\$ 0.0014

PLATING COST COMPARISONS (100 MICROINCHES)

TABLE IX



The operator positions the wire by using the micro-manipulator and the wire feed pedal. When the wire is in position, the operator moves the bonding tip into position by using the other micro-manipulator and then makes a thermocompression bond. When it is time to break the wire, the operator does so by applying pressure on the wire with the bonding tip.

Since these bonders were slow and inefficient, we have switched to the West Bond Model-7416 wire bonder (see Figure 18). The main feature of the West Bond Model-7416 wire bonder is that the gold wire is fed through the bonding tip. Therefore, the wire and the tip move as one unit, and the wire always remains under the bonding tip, sparing the operator the added burden of controlling the wire replacement with one hand while manipulating the bonding tip with the other.

Another important feature of the West Bond is that the wire feed and the wire cut-off steps are performed automatically. Separate wire feed and wire cut-off steps are not required. Also, the West Bond has only one hand operated micro-manipulator and only one foot operated switch. This system is capable of handling 750 chips per day as compared to 150 chips per day by the present Kulicke and Soffa System Model 420-D.

The final step in the assembly process is capping. A gold tin solder washer is placed on the kovar ring and then a cap is placed on top of the solder washer. The entire assembly is placed in an oven to melt the solder and attach the cap.

In the past, the assembler handled each package, solder washer and cap separately. These three parts were placed in a capping boat which held 100 units. The capping boat was then sent through a furnace to melt the solder. We now use a GTI sealer, Model-700, for capping. The caps are shaker loaded into a 675 position graphite boat. The packages are also placed in a 675 position boat after being wire bonded. The boat the packages are placed in is compatible with the graphite boat. The solder washers are placed on top of the caps and then the packages are transferred into the graphite boat so that they are now resting on top of the cap and solder washer combination. This graphite boat is then placed into the sealer. A current is passed through the graphite which produces the heat to melt the solder.

The overall cost reduction is shown in Table X.

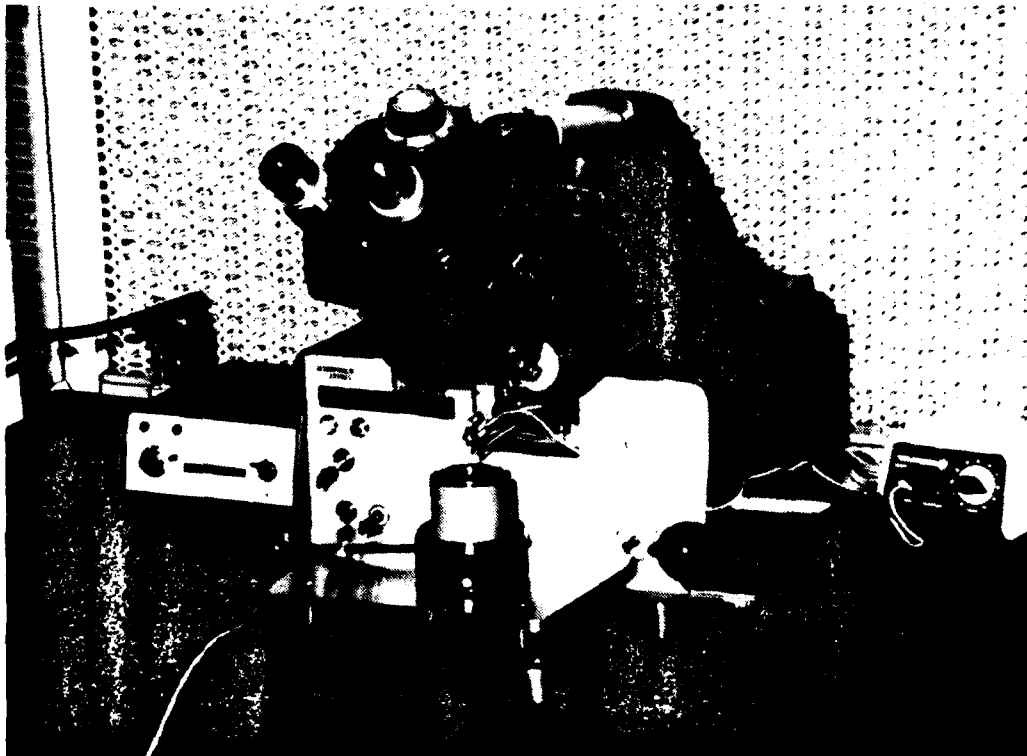


FIGURE 18 SEMI-AUTOMATIC WEST BOND MODEL 7416
THERMOCOMPRESSSION WIRE BONDER

D-17133

		<u>PAST RATE</u>	<u>NEW RATE</u>
1.	ELIMINATE TWO MINIATURE BRAZING WASHERS	1000/HOUR	10,000/HOUR
2.	BOND CHIPS IN 100 POSITION BOAT	100/HOUR	150/HOUR
3.	WEST BOND WIRE BONDERS INSTEAD OF KULICKE AND SOFFA WIRE BONDERS	60/HOUR	120/HOUR
4.	WIRE BOND IN 100 POSITION BOAT	120/HOUR	160/HOUR
5.	USE DAP SEALER FOR CAPPING INSTEAD OF BELT FURNACE	200/HOUR	1000/HOUR
6.	ELIMINATE HANDLING OF SOLDER WASHER	1000/HOUR	1500/HOUR

TABLE X
PRODUCTION ADVANCEMENTS

7.0 Composite Platinum - Nickel Schottky Diode

This approach consists of sputtering sequentially 100 Å of platinum and 260 Å of nickel on n-type epitaxial silicon wafers with windows etched in silox. The wafer is then baked at 450°C under hydrogen atmosphere for silicide formation. The nickel migrates through the platinum layer and forms with the epitaxial silicon a nickel silicide below with the platinum silicide. The nickel silicide lowers the barrier height of platinum Schottky diodes without degrading appreciably the RF burnout performance of the device. The current versus voltage characteristics of Pt Schottky and (Pt-Ni) composite Schottky diodes are shown in Figure 19. The ideality factor and barrier height are given below

	Pt-Ti-Mo-Au	(Pt-Ni)-Ti-Mo-Au
Ideality Factor (η)	1.06	1.06
Barrier-Height (ϕ)	0.80 volts	0.65 volts

This barrier height lowering of (Pt-Ni) composite Schottky diode is sufficient to meet the contractual goal of 7.0 dB noise figure (SSB) at a local oscillator power of 0.5 mW. The RF burnout resistance and performance was measured at local oscillator power of 1.0, 0.75, and 0.50 mW. Results shown in Table XI indicate that at 0.5 mW, the diodes exhibit RF burnout of 15 - 20 watts and noise figure of 6.5 dB. These diodes meet the overall objectives of the present contact.

7.1 RF Testing of (Pt-Ni) Schottky Barrier Diodes

(Pt-Ni-Ti-Mo-Au) and standard Pt-Ti-Mo-Au Schottky diodes were tested for NF, IF impedance and rectified current. The diodes were tuned for low VSWR (less than 1.5) at various power levels at 9.375 GHz in a broadband tunable mount (developed under Contract Number N00173-77-C-0029). Noise figure, IF impedance, and rectified current were measured at different

A = (Pt-Ni) SCHOTTKY
B = STANDARD Pt

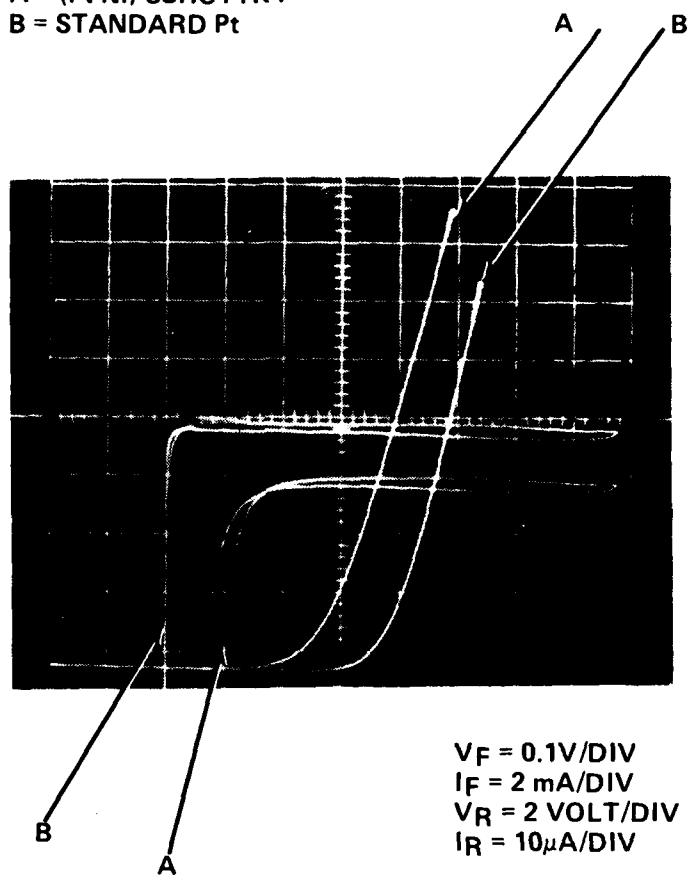


FIGURE 19 CHARACTERISTICS OF STANDARD Pt-Ti-Mo-Au AND (Pt-Ni)-Ti-Mo-Au SCHOTTKY BARRIER DIODES

D-17371A

DEVICE NO.	RF PARAMETERS											RF BURNOUT ($t = 1 \mu\text{sec}$) POWER WATTS)
	1 mW			0.75 mW			0.5 mW			ZIF (OHMS)		
	NF (dB)	IDC (mA)	ZIF (OHMS)	NF (dB)	IDC (mA)	ZIF (OHMS)	NF (dB)	IDC (mA)				
1	6.0	1.15	380	6.5	0.9	540	6.5	0.5	540		15.0	
2	6.0	1.2	380	6.5	0.9	520	6.5	0.5	520		12.5	
3	6.0	1.2	380	6.5	0.9	520	6.5	0.5	520		15.0	
4	6.0	1.25	360	6.25	1.0	560	6.5	0.5	520		14.0	
5	6.0	1.2	380	6.5	0.9	520	6.5	0.5	540		15.5	
6	6.0	1.2	380	6.5	0.9	520	6.5	0.5	540		22.0	
7	6.0	1.2	380	6.5	0.9	520	6.5	0.5	540		15.0	

TABLE XI RF CHARACTERISTICS OF X-BAND LOW BARRIER
HEIGHT (Pt/Ni-Ti-Mo-Au) SCHOTTKY BARRIER
DIODES

D-21683

local oscillator power levels. Noise figure of the amplifier was 1.5 dB and a 16 ohm load resistor was used for the measurements. Results are given in Figure 20 to Figure 22. The (Pt-Ni) and standard Pt-Schottky diodes exhibit low noise figure of 6.5 dB (SSB) at +1 dBm power level but (Pt-Ni) Schottkys exhibit lower noise figure at -3 dBm power level. This is due to lowering of the barrier height due to nickel. Similar results were observed in rectified current and IF impedance characteristics.

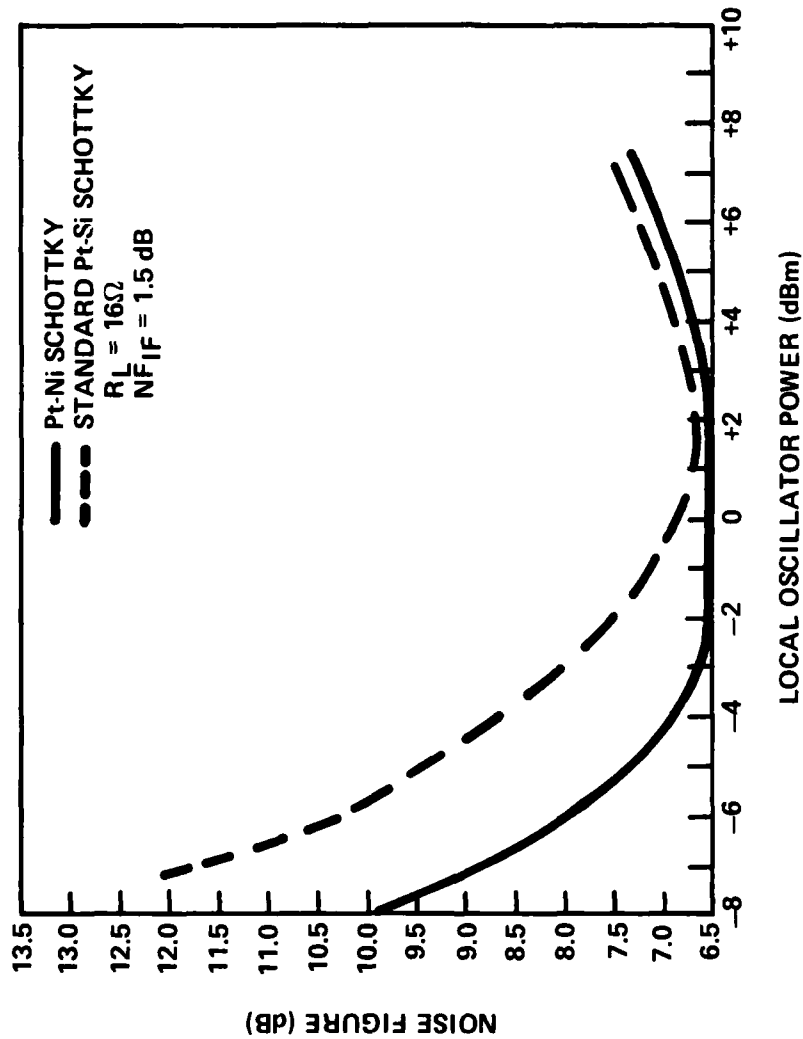


FIGURE 20 NOISE FIGURE VS LOCAL OSCILLATOR POWER AT 9.375 GHz

D-17329

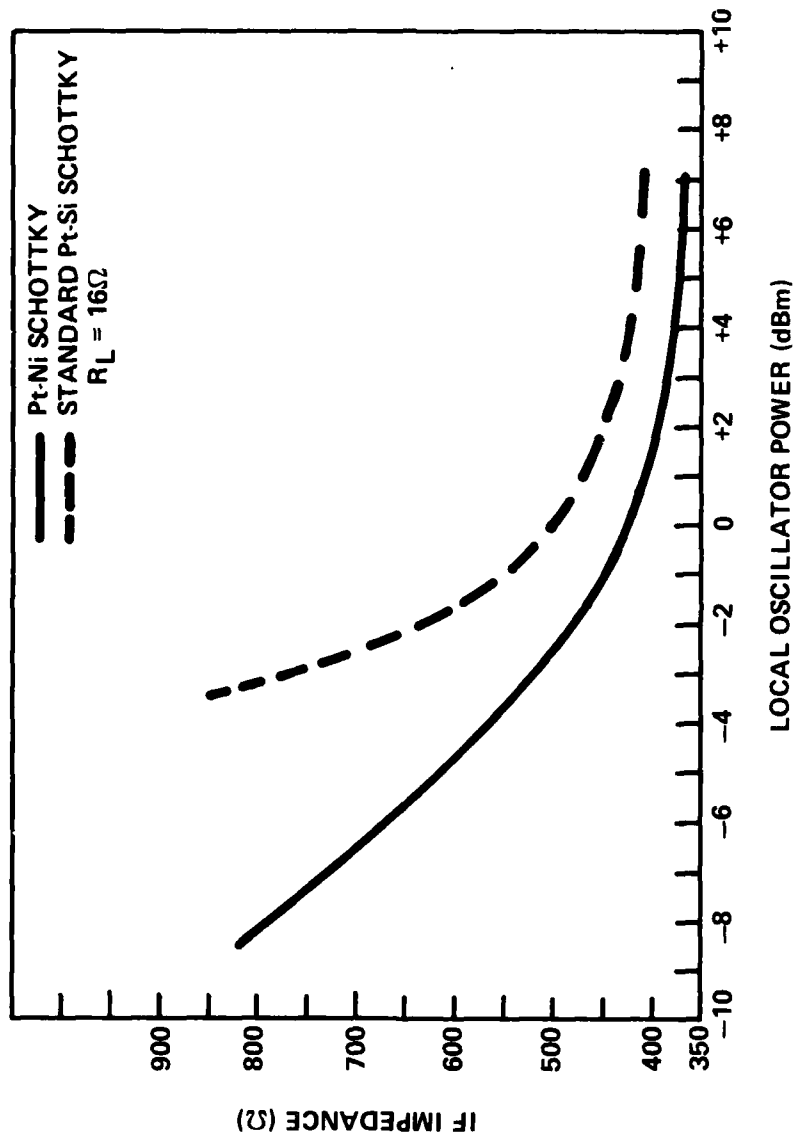


FIGURE 21 IF IMPEDANCE VS LOCAL OSCILLATOR POWER AT 9.375 GHz

D-17330

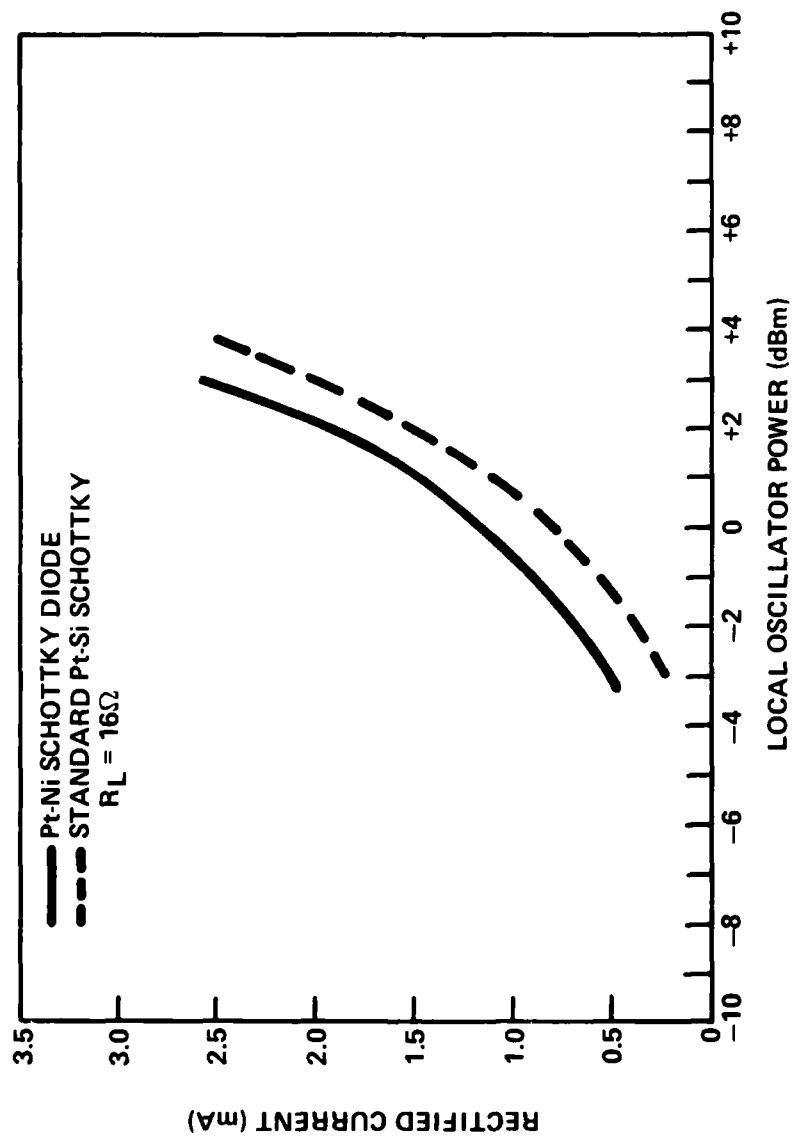


FIGURE 22 RECTIFIED CURRENT VS LOCAL OSCILLATOR POWER AT 9.375 GHz

D-17328

8.0 TECHNICAL REPORT - PHASE II (Manufacturing Phase)

8.1 Introduction

Final Pilot Line production of diodes for this contract was commenced on June 15, 1981. Process and specifications were documented on the Wang Processor System (see Table XII). Ten (10) three inch silicon wafers were processed following the procedures established earlier in the program.

8.2 Production Line

The production line for manufacturing the required diodes is shown in Figure 23 and 24. The process steps and equipment utilized are outlined in Table XIII. Manufacturing cost of the complete diodes is summarized in Table XIV. Labor time and yields are summarized in Table XV.

8.3 Environmental/Reliability Testing

The extensive RF burnout tests using test set up shown in Figure 25, environmental reliability and step stress tests were conducted on a reasonable sample of the preproduction diodes. These tests showed that the diodes are capable of handling 12 watts peak power ($\tau = 1 \mu\text{sec}$, 1 KHz rep rate) and are rugged enough to stand 200°C temperature for 1000 hours. The failure analysis was also conducted on degraded and RF burnout devices using scanning electron microscope and microspot auger analyzer.

8.4 Jan Format Design Reliability Testing

Two hundred diodes were randomly selected from the pilot line for Jan Format Testing using appropriate tests taken from Tables IB(b) and V in MILS-19500 F. The verification testing schedule is shown in Table XVI. The testing was monitored by a resident DCASR-QAR. The diodes passed all the subgroups and thus demonstrate the reliability and ruggedness of the device design. (For details see Appendix C).

8.5 JEDEC Registration

This diode was assigned identification No. 1N6477 for JEDEC release No. 6983, dated November 10, 1981. For details see Appendix B.

Microwave
Associates

Manufacturing
Flowsheet

Rev. A
Date 10/29/91

Title: Schottky Pt - Ni Bondable

Starting Material Spec. 7146
No. Slices In Out

Map# 4E390 Run#
Date Start
Date Fin.
Job#

#	Operation	Spec.	Process Variables	Op.	Qty.	Date
1	Prod. Control					
2	Slice I.D.	DF0001				
3	RCA Clean	DF0016				
4	I.T.D.	DF0025	8000 Angstroms			
5	Prod. Control					
6	Photo I-Sch.	PR0023	Mask #			
7	Etch Ox. Photo	PR0033				
8	Wafer #		Dot size	Comments		
9	A					
10	B					
11	C					
12	D					
13	E					
14	F					
15	G					
16	H					
17	Q.C. Inspection		GAI 3.52.1			
18	RCA Clean	DF0016				
19	Prod. Control					
20	20:1 Dip	DF0104				
21	Pt - Ni Dep.	MT0023				
22	Sinter	DF0116	Time: 7 mins. Temp: 480deg.C			
23	Excess Rem.	DF0088				
24	RCA Clean	DF0016				
25	Prod. Control					
26	I/W - Au Dep.	MT0026				
27	Excess Met. Ph.	PR0022	Mask #			
28	Q.C. Inspection		GAI 3.52.1			
29	Excess Met. Etch	DF0026				
30	Plasma Strip	IBD				
31	Mount. Wafers	DF0014				
32	Ink. Etch. Barr.	DF0033	4.5 - 5.0 mil thick			
33	Sand blast waf.	DF0008				
34	Ni strike	MT0065				
35	Au Plate	MT0066				
36	Dismount Wafer	DF0011				
37	Solvent Clean	DF0017				
38	Button Plate	MT0078				
39	Prod. Control					
40	W. r.r. Mount	DS0017				
41	Die Sep. Disc	DS0016				
42	Clean Saw Cut	DS0006				
43	Q.C. Inspection		QCIS 3.56			

TABLE XII

D-21247

Electrical Evaluation Sheet

$$R_s > V_{f1mA} > V_{b10\mu A} > C_j >$$
[illegible]

B. > > > > >

> > > > >

> > > > >

> > > > >

> > > > >

A set of five horizontal handwriting practice lines. Each line consists of a solid top line, a dashed middle line, and a solid bottom line. Small arrows are placed at the beginning of each line to indicate the starting point and direction of the writing stroke. The arrows point to the right, indicating a left-to-right writing direction.

Q

```
> Rs > Vf1mA > Vb10uA > Cj >
```

Handwriting practice lines for the letter 'I'.

J > > > > >

> > > > >

> > > > >

> > > > >

> > > > >

[illegible][illegible]

D-21248

Rs : Vfilm : Vb10uA : C1 : > Rs : Vfilm : Vb10uA : C1

2. Rs. 2 Yf1mA 2 Vb10u0 1 C1

F

[illegible]

F

[illegible][illegible]

Q > > > > >

> > > > >

> > > > >

> > > > >

> > > > >

[illegible]

P

D-21249

Microwave
Associates

Silicon Material
Specifications

Rev. A
Date 10/29/81

Material Spec. # 7146

Epitaxial Thickness .75 microns

Measurement Technique IR Hg X Other

Epitaxial Resistivity 0.05 ohm-cm

Measurement Technique Hg X other

Percentage Sampling Plan 10 50 100

Substrate Resistivity .002 ohm-cm

Substrate Dopant As X Sb B other

Wafer Size 1 1/2 2 3 X

Wafer Thickness 12 mils

Orientation 1-1-1

P/P+ or N/N+ N/N+

Special Instructions

D-21251

Microwave

Special

Rev. A

Associates

Instruction Sheet

Date 10/29/81

M/A P/N 4E390

D-21270

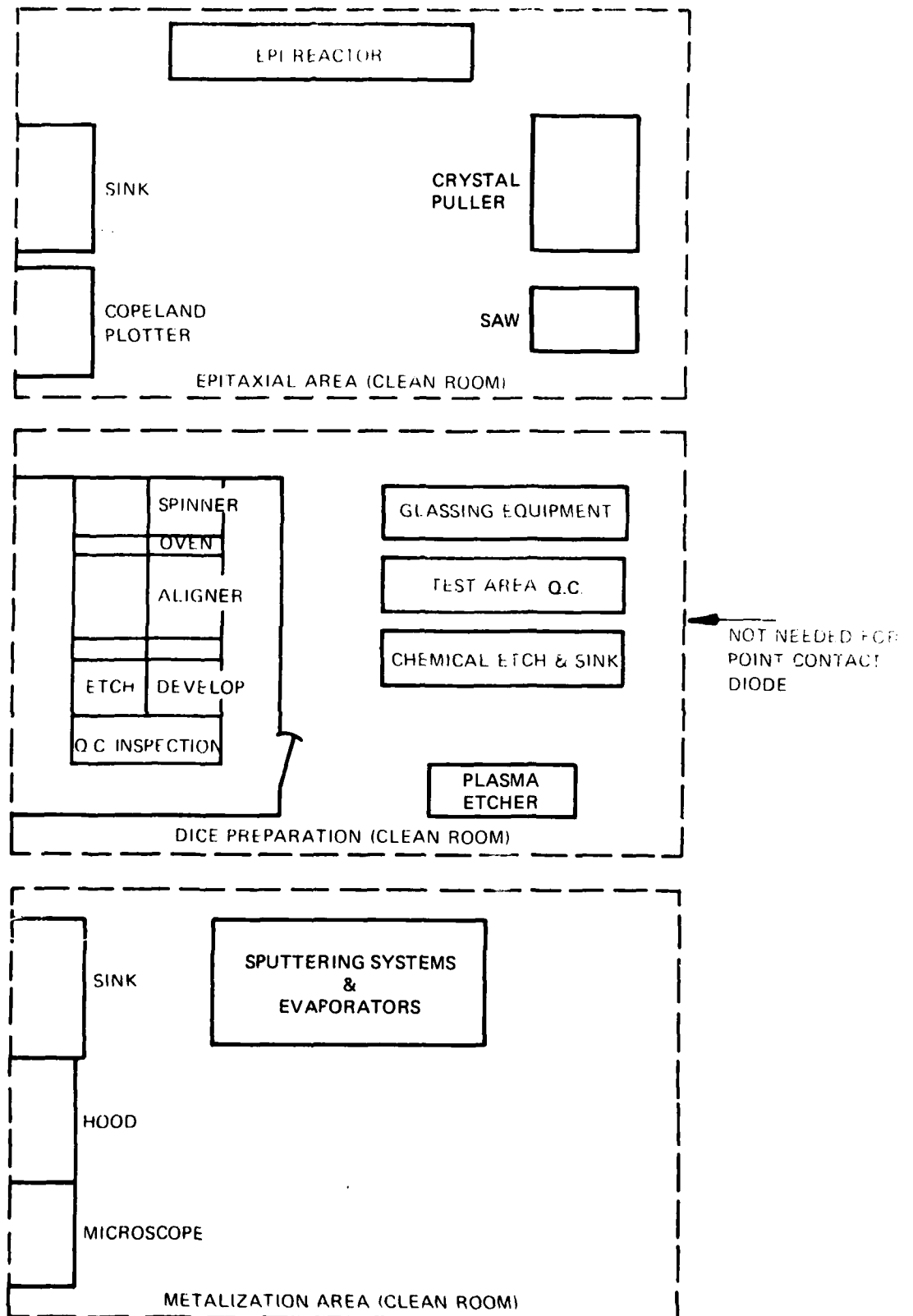


FIGURE 23 MIXER DIODE DICE PREPARATION AREA

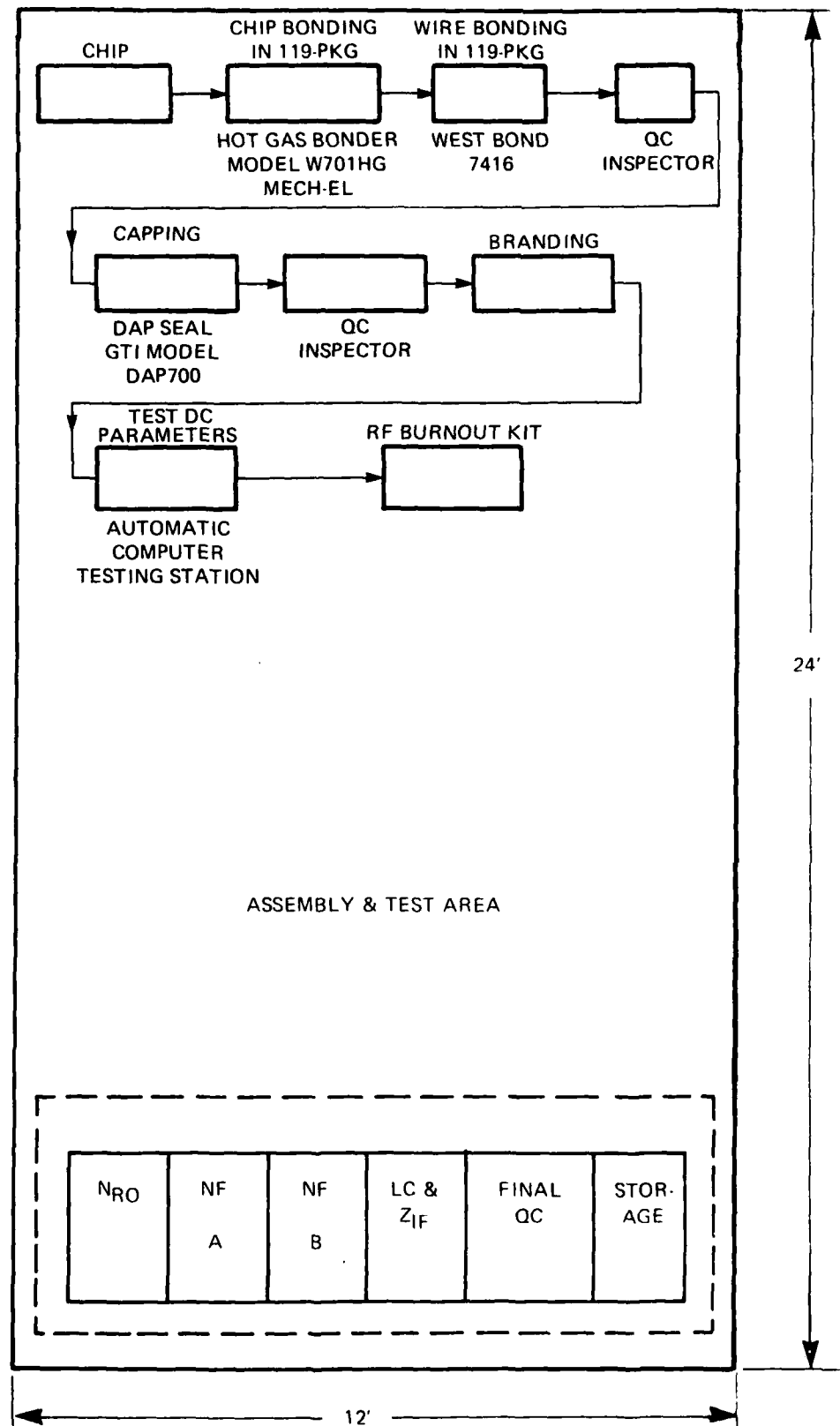


FIGURE 24 MIXER DIODE FABRICATION AND TEST AREA

<u>OPERATION</u>	<u>EQUIPMENT</u>	<u>CONTROLS</u>
1) Grow Silicon Crystal	Semi-Metals Crystal Puller Model	
2) Slice Crystal	Dual Micromatic Model #1427	Micrometer
3) Check Resistivity	Jandell Four Point Probe	Actual Slice
4) Etch Slices	Micro Air Hood	Visual Timed
5) Polish Slices	Semi-Metals Polisher Model #22	Visual
6) Grow EPI Layer	Applied Materials AMV 1200	Mass Flow Controllers
7) Check EPI Layer Thickness	HP1000	Measure
Check EPI Layer Resistivity	Mercury Probe and Phites Bevel & Stain	Actual Slice
8) Clean Wafers	Micro Air Hood	Visual
9) Chemical Vapor Deposit Siliox Glass	ASM LTO System	Alpha Step
		Surface Profiler
10) Open Window for Schottky Junction	Cobilt CA-800 Photo Aligner	Visual
		Vickers-Image-Shere microscope

TABLE XIII. SCHOTTKY-BARRIER DIODE CHIP FABRICATION

<u>OPERATION</u>	<u>EQUIPMENT</u>	<u>CONTROLS</u>
11) Etch Windows	IPC Model 2005X Plasma System	End Point Detector
12) Strip Resist	IPC Model 2005X Plasma System	End Point Detector
13) Anneal	Lindburg Diffusion Furnace	Timer
14) Metallize	Materials Research Corp MRC-903-1 Magnatron	Alpha-Step Surface Profiler
15) Mask Metal for Etch	Cobilt CA-800 Photo Aligner	Visual - Vickers Scope
16) Etch Metal	IPC Model 2005X Plasma System	End Point Detector
17) Strip Resist	IPC Model 2005X Plasma System	End Point Detector
18) Plate Buttons	Electroplate in Au Bath	Unitron Model TM25 Scope
19) Mount and Lap Back	Speed Flam Model 12B Lapper	Micrometer

TABLE XIII (cont'd) SCHOTTKY-BARRIER DIODE CHIP FABRICATION

<u>OPERATION</u>	<u>EQUIPMENT</u>	<u>CONTROLS</u>
20) Metallize Back	Materials Research Model MRC903-2	Alpha-Step Surface Profiler
21) Dismount and Clean	Micro Air Hood	Visual
22) Electrical Probe Wafer	M/A Automatic Probe Station with HP-3000 Computer	
23) Dice Wafer	Disco-I	Micro processor
24) Dice Approval	Nikon IC Inspection Microscope	Visual Inspect

TABLE XIII (Cont'd) SCHOTTKY-BARRIER DIODE CHIP FABRICATION

METHOD	PRESENT COST	COST AFTER COMPLETION OF THE CONTRACT
● Processing Silicon Chip	\$ 2.00	\$ 0.50
● Chip Approval MIL Specs	\$ 5.00	\$ 1.10
● Diode Mfg. Cost	\$ 8.00	\$ 3.00
● Initial DC & RF Test	\$25.00	\$ 9.00
● Final Screen & MIL Std Testing	\$30.00	\$10.00
TOTAL	\$30.00	\$10.00

TABLE XIV. COST REDUCTION SUMMARY OF HIGH BURNOUT
SCHOTTKY-BARRIER DIODE

OPERATION	LABOR-TIME	LABOR-TYPE	YIELD
Gen. Runsheet- Define Process Limits	.5 hr	Eng	100%
Slice ID	10 min - 8 wafer lot	Operator	100%
RCA Clean	1 hr.	Operator	100%
L.T.O.	2 hr.	Tech	100%
Photo I	3 hrs.	Operator	95%
Etch Oxide	.5 hr.	Tech	85%
RCA Clean	1 hr.	Operator	100%
Pre-metal Dip	10 min.	Operator	100%
Metal I (Pt-Ni)	1.5 hr.	Tech	100%
Sinter	.5 hr.	Operator	100%
Excess Remove	.5 hr.	Operator	100%
RCA Clean	1 hr.	Operator	100%
Metal II (T/W-Au)	2.5 hrs.	Tech	100%
Photo II	3 hrs.	Operator	95%
Metal Etch	.5 hr.	Tech	90%
Strip Resist	.5 hr.	Operator	98%
Mount Wafers	.5 hr.	Operator	98%
Barrel Etch	1 hr.	Operator	90%
Sandblast	.5 hr.	Operator	95%
Ni Strike	.5 hr.	Operator	100%
Au Plate	1 hr.	Operator	100%
Dismount Wafer	.5 hr.	Operator	98%
Clean	.5 hr.	Operator	100%
Plate Button	1 hr.	Operator	100%
Eng. Evaluate	.5 hr.	Eng.	--
Wafer Mount	.25 hr.	Operator	98%
Die Separate	.25 hr.	Tech	90%
Tach. Probe	.5 hr.	Tech	75%
Dismount & Clean	.5 hr.	Operator	95%
TOTALS- Op.Time 16.95 hrs			
Tech Time 7.75 hrs			
Eng Time 1 hr			

TABLE XV HIGH BURNOUT-SCHOTTKY LABOR CHART

D-21240

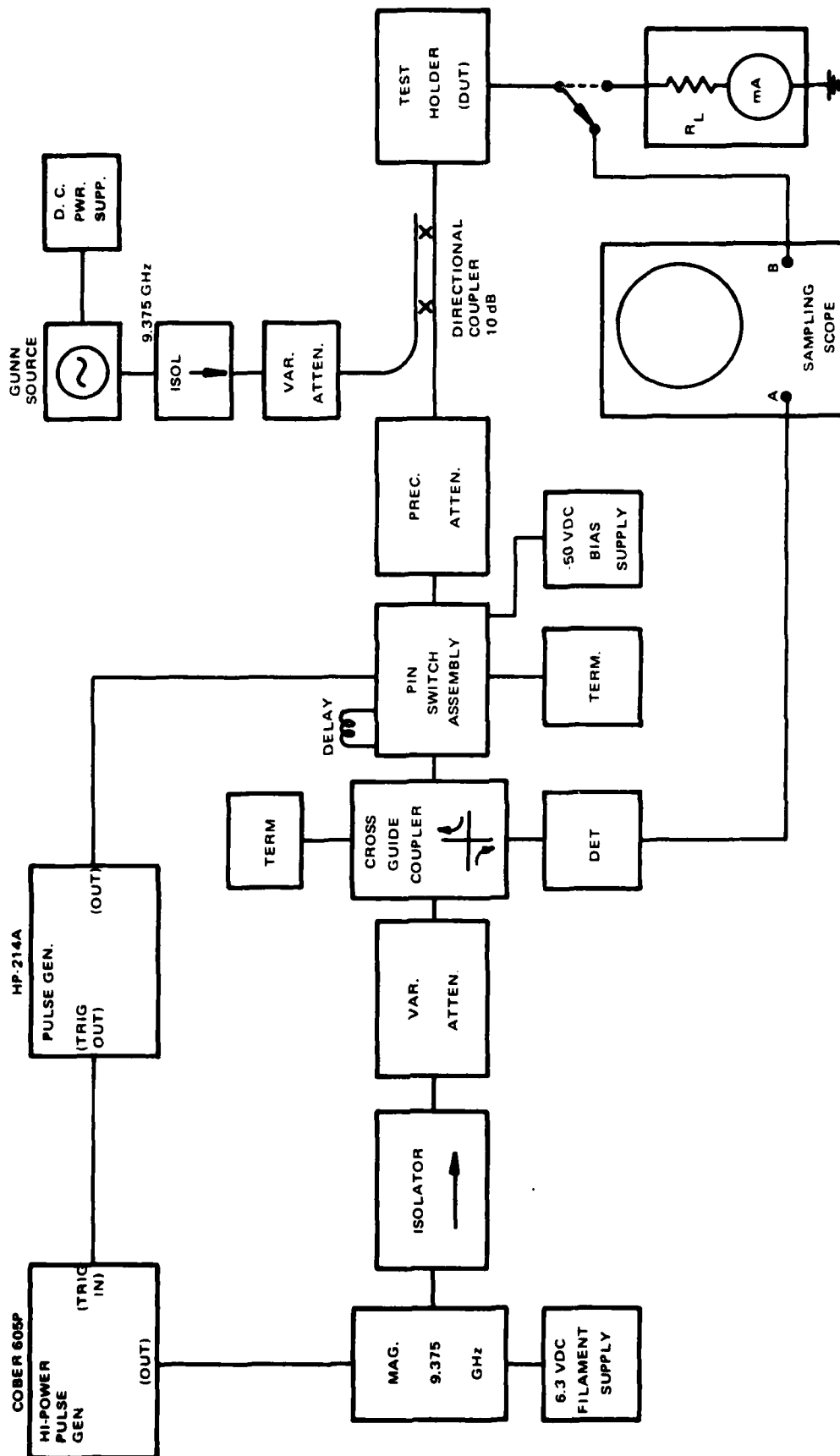


FIGURE 25 X-BAND RF PULSE BURNOUT SYSTEM ($\tau = 3$ nsec)

TABLE XVI
LIFE & ENVIRONMENTAL TEST SCHEDULE/SUMMARY

NR!

7/10

11A

MIL-STD-750

MICROWAVE ASSOCIATES, INC.
LIFE & ENVIRONMENTAL TEST SCHEDULE/SUMMARY

Semiconductor Division

GROUP C (CONTINUED)

Issue # _____ Initiated By: _____ Date: _____

FILED PAGE 3 OF 3 PAGES

#1981481	LOI DATE
	CODE

11/1 Type 11/1-87-2

Class 5-6-4-C-9-5

M/A SO No. N/A

[illegible]

CUSTOMER LEGEND

Customer

JPL

Customer P.O.

N/A

Part No.

N/A

Other Dwg.

N/A

Methods Per

MIL-STD-750

MICROWAVE ASSOCIATES, INC.

LIFE & ENVIRONMENTAL TEST SCHEDULE/SUMMARY

Semiconductor Division

GROUP C PER MIL-S-19500F

Issue #

Initiated By:

Date:

MISC

PAGE 2 OF 3 PAGES

1981-4814

LOT DATE

CODE

M/A Type

MIL-STD-750

Class

Schedule

M/A SO No.

N/A

PROGRAM REQUIREMENTS										Diffusion No.		Job No.	REMARKS	Test Oper.
Examination/Test	Method No.	Test Conditions	Test Limits	Estimated		Actual								
				Start Date	Comp. Date	Start Date	Comp. Date							
SUB CP1	Physical Dimension	2066	0.25-1.19 DRAWING	15	15	0	15	10/19	10/23	11/4	11/4	3/11 238-252 to 85	J.J.	
SUB CP2	Glass Strain							10/19	10/20	10/27	10/27	3/11 253-274	J.J.	
	Thermal Shock	1056	Cond. A	10	22	0	22	10/21	10/22	11/4	11/5		J.J.	
	Terminal Strength	2036	Cond. 7 Torque	22	0	22		10/23	10/23	11/5	11/5		J.J.	
	Fine Leak	1071		22	0	22		10/26	10/26	11/6	11/7		J.J.	
	Gross Leak	1071		22	0	22		10/27	11/6	11/10	11/10		J.J.	
	Moisture Resistance	1021		22	0	22		11/9	11/9	11/20	11/21		J.J.	
	External Visual	2071		22	0	22		11/9	11/9	11/20	11/21		J.J.	
	Elect End Points			22	0	22		11/10	11/12	11/20	11/24	3/11 275-296	J.J.	
SUB CP3	Shock	2016	3 planes 1500 G's 0.5ms	10	22	0	22	10/19	10/23	11/3	11/3	3/11 275-296	J.J.	
	Vibration		2000 X's	22	0	22		10/26	10/30	11/3	11/3		J.J.	
	Var. Freq.	2056		22	0	22		11/2	11/4	11/3	11/3		J.J.	
	Constant Acceleration	2006	2000 X's 3 planes 1, 2, Y	22	0	22		11/5	11/9	11/3	11/3		J.J.	
	Elect End Pts.			22	0	22						3/11 275-296	J.J.	

CUSTOMER LEGEND

MIL-STD-750

PAGE 1 OF 3 PAGES

#1921-4819 LOT DATE

M/A Type N/A L-88-C

Class Schottky

M/A SO No. 11/A

MICROWAVE ASSOCIATES, INC.

LIFE & ENVIRONMENTAL TEST SCHEDULE/SUMMARY

Semiconductor Division

GROUP B PER MIL-S-19500F

Initiated By: _____ Date: _____

Issue #

PROGRAM REQUIREMENTS												Diffusion No.		Test Oper.	
Examination/Test		Method No.	Test Conditions		L	Q	N	Test Limits		Estimated		Actual			Job No.
					P	T	E			Start Date	Comp. Date	Start Date	Comp. Date		
SUB CP 1	Solderability	2026			15	15	0	15		10/26	10/28	11/3	11/11	from (C5) 5/11 201-215	W88
	Resistance to Solvents	1022								10/29	11/2			not applicable.	W88
SUB CP 2	Thermal Shock	1051	25 cycles	Test Cond. C-1	10	22	0	22		10/19	10/21	10/29	10/30	5/11 216-237	40
	Fine Leak	1071	Cond. II		22	22	0	22		10/22	10/22	11/2	11/3		40
	Gross Leak	1071	Cond. C		22	22	0	22		10/23	10/23	11/3	11/4		40
	Elect. End Pts.				22	22	0	22		10/26	10/28	11/4	11/10	to (C4) 5/11 51-95	W88
SUB CP 3	Steady State Life (operating)	1027	340 hours	405.6	5	45	0	45		10/2	10/11	10/2	10/19		40
	Elect. End Pts.					45	0	45		10/6	10/16	10/19	10/19	to (C2) 5/11 33	W88
SUB CP 4	Decap Int. Visual	2075			-	1	0	1		10/19	10/25	10/19	10/19		W88
	Bond Strength	2037			20	11	0	11		10/11	10/22	10/19	10/19	Qty. refers to Bond Pulls. 5/11 34-44	W88
SUB CP 5	Thermal Resistance		(N/A)		15	15				10/26	10/30			from (C1) 5/11 238-252	W88
SUB CP 6	HI Temp. Life/Storage	1032	340 hours		7	32	0	32		10/22	10/22	10/19	10/19	5/11 1-32	30
	Elect. End Pts.					32	0	32		10/2	10/13	10/9	10/11	to (C3) 5/11 33	W88

TABLE XVI (Cont'd)

8.6 Pilot Line Diodes

Three hundred pilot line diodes were shipped to Naval Research Laboratories, after completing the Jan Format Design Reliability Testing.

8.7 Product Data Sheet

This diode is being manufactured in production quantities at Microwave Associates and is now available for sale. A data sheet on these diodes is already published (see Appendix A) and circulated.

9.0 DELIVERABLES

Three engineering samples, each consisting of 25 diodes and pilot run of 300 preproduction samples were fabricated. Test data of these devices are given in Tables XVII to XX. All devices were shipped to the Naval Research Laboratory.

MICROWAVE ASSOCIATES, INC.

SEMICONDUCTOR DIVISION

DIODE TEST DATA

PAGE OF

M.A. PART NO.	LOT NO.	S.O. NO.	QUANTITY	SAMPLE	DATE	START	COMP.
CUSTOMER		CUSTOMER PART NO.	CUSTOMER ORDER NO.	OTHER DRAWINGS		T _A = 25 ± 3°C Unless Noted	
PARAMETER							
TEST CONDITIONS	V _B	R _S	C _T	NF	V _B	R _S	C _T
LIMITS							
Environmental Test(s)	DC & RF Characteristics of Silicon Ion Implant Schottky-barrier diodes						
	(volts)	(Ω)	(pF)	(dB)	(volts)	(Ω)	(pF)
10 kev							
#1	5.4	23	0.27	8.0	#26	11	25
#2	5.4	22	0.27	8.3	#27	8	25
#3	5.6	22	0.27	8.1	#28	10.5	25
#4	5.6	22	0.27	8.5	#29	9.0	24
#5	5.7	22	0.27	8.2	#30	9.0	27
30 kev							
#6	4.0	16	0.76	>15			
#7	3.9	16	0.74	>15			
#8	5.0	23	0.43	>15			
#9	4.7	26	0.38	>15			
#10	4.1	26	0.41	>15			
40 kev							
#11	.50	19	0.42	>15			
#12	1.90	20	0.37	>15			
#13	1.20	20	0.33	>15			
#14	1.50	21	0.40	>15			
#15	1.50	24	0.20	>15			
20 kev							
#16	1.20	19	0.42	>15			
#17	1.50	18	0.48	>15			
#18	1.80	15	0.56	>15			
#19	1.50	21	0.48	>15			
#20	2.20	20	0.49	>15			
10 kev							
#21	2.20	21	0.48	>15			
#22	2.60	9	0.73	>15			
#23	1.40	12	0.60	>15			
#24	2.50	9	0.53	>15			
#25	2.80	8	0.67	>15			

TABLE XVII
TEST DATA - 1ST ENGINEERING
SAMPLES (diodes
from various runs)

TESTER/DATE

MICROWAVE ASSOCIATES, INC.

SEMICONDUCTOR DIVISION DIODE TEST DATA

PAGE OF

M.A. PART NO.		LOT NO.		S.O. NO.		QUANTITY		SAMPLE		DATE		START COMP.	
CUSTOMER NRL			CUSTOMER PART NO.			CUSTOMER ORDER NO.			OTHER DRAWINGS			T _A = 25 ± 3 °C Unless Noted	
PARAMETER	NF*	Z _{IF}	RF**		V _B	R _s	C _T						
TEST CONDITIONS	dB	ohm	Burnout Watts		(10 μA) Volts	ohm	pF						
LIMITS	7.0		12										
Environmental Test(s)	SECOND ENGINEERING SAMPLES ***												

Diode No.													
1	6.90	420	BO/14		14.0	16	0.27						
2	6.80	425	BO/18		14.0	17	0.27						
3	6.8	410			14.0	15	0.26						
4	6.90	410			14.0	14	0.27						
5	6.8	405			14.0	15	0.27						
7	6.9	420			14.5	14	0.25						
8	6.7	400			14.0	18	0.27						
9	6.75	390			13.5	15	0.27						
10	6.8	390			13.5	15	0.28						
14	6.9	400			14.0	15	0.27						
16	6.8	405			14.0	18	0.26						
20	6.9	400			14.0	15	0.26						
21	6.75	430	12		14.0	15	0.26						
22	6.9	420	12		14.0	18	0.25						
23	6.8	400			14.0	17	0.26						
24	7.0	420	12		14.0	16	0.26						
25	6.75	400			14.0	15	0.25						
26	6.8	420	BO/16		14.0	16	0.26						
27	6.75	400			14.0	17	0.26						
28	6.8	420	12		14.0	16	0.24						
29	7.0	430	BO/17		14.0	17	0.25						
30	6.8	410			14.0	17	0.24						
31	6.9	425	12		14.0	16	0.26						
32	6.9	420	BO/18		14.0	16	0.26						
33	6.75	405			14.0	15	0.27						

TEST CONDITIONS :

* $f_{LO} = 9.375 \text{ GHz}$; $P_{LO} = 0.5 \text{ mW}$; $R_L = 10 \text{ ohms}$; $NF_{IF} = 1.3 - 1.5 \text{ dB}$

** $f = 9.375 \text{ GHz}$; $t = 1 \mu\text{sec}$; Rep. Rate = 10^3 Hz

*** CONTRACT OBJECTIVES: $NF = 7.0 \text{ dB}$; RF Burnout = 7.0 dB ; $P_{LO} = 0.5 \text{ mW}$

TABLE XVIII SECOND ENGINEERING SAMPLE DATA

ELECTRICAL/MECHANICAL TEST DATA

PAGE OF

M.A. PART NO.	#	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	START	COMP.
---------------	---	---------	-----------------	----------	--------	-------	-------

CUSTOMER	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS	T _A = 25°C Unless Noted
----------	-------------------	-----------------------------	----------------	---------------------------------------

Environmental Test(s)	3rd & FINAL ENGINEERING SAMPLES
-----------------------	---------------------------------

PARAMETER	DC & RF CHARACTERISTICS OF SILICON (Pt - Ni) Schottky Diodes
-----------	--

TEST CONDITIONS	RUN # NRL88-2
-----------------	---------------

LIMITS	
--------	--

1	V _{B(10A)}	R _S	C _T	Z _{IF}	I _{DC}	N _F
---	---------------------	----------------	----------------	-----------------	-----------------	----------------

Device No.	Volts	Ohms	(pF)	Ohms	mA	dB
------------	-------	------	------	------	----	----

1	3.60	12	0.25	480	0.75	6.70
2	3.40	11	0.28	540	0.70	6.70
3	3.60	12	0.27	540	0.70	6.80
4	3.60	11	0.28	540	0.70	6.70
5	3.60	11	0.27	510	0.70	6.90
6	3.50	12	0.25	460	0.70	6.60
7	3.40	12	0.26	460	0.70	6.70
8	3.60	11	0.27	480	0.70	6.90
9	3.40	11	0.26	470	0.70	6.60
10	3.60	11	0.27	490	0.70	6.90
11	3.40	11	0.27	470	0.70	6.80
12	3.60	12	0.27	480	0.65	6.50
13	3.60	10	0.28	510	0.70	6.90
14	3.60	11	0.27	500	0.70	6.80
15	3.40	11	0.29	500	0.70	6.70
16	3.50	12	0.28	510	0.70	6.80
17	3.70	12	0.27	490	0.70	6.70
18	3.40	11	0.29	490	0.70	6.90
19	3.40	11	0.27	480	0.70	6.70
20	3.80	12	0.25	530	0.75	6.80
21	3.60	11	0.27	500	0.70	6.90
22	3.50	12	0.25	510	0.70	6.80
23	3.60	12	0.27	530	0.70	6.80
24	3.30	12	0.25	490	0.75	6.90
25	3.40	12	0.27	540	0.75	6.80

#1 - 21 tested
to 10 WATTS

burnout @ 28
burnout @ 22
burnout @ 25
burnout @ 30

* Test Conditions
f₁₀ = 9.375 GHz, P₁₀ = .5mW
R_L = 100 Ω
NF_{IF} = 1.3 - 1.5 dB
f = 9.375, τ = 1 μsec.,
Rep Rate = 10³ HZ

TABLE XIX Third Engineering Samples

ELECTRICAL MECHANICAL TEST DATA

PAGE 1 OF 9

PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	START	END
CUSTOMER	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS				
NRL 88-2							

PARAMETER							
TEST CONDITIONS: PLo = .50 mW R _L = 100 Ω fo = 9.375 GHz							
LIMITS							
	NF	ZIF	Idc		NF		
Device	dB	ohms	mA		dB		
1	6.90	560	.75		7.00		
	6.80	560	.70		6.90		
	6.90	560	.70		7.00		
	6.70	550	.75		6.80		
5	6.80	565	.80		6.90		
	6.90	540	.70		7.00		
	6.70	550	.70		6.90		
	6.90	565	.70		7.00		
10	6.80	540	.70		6.90		
	6.90	550	.75		7.00		
	6.70	560	.75		6.90		
	6.80	560	.70		6.90		
15	6.80	560	.80		6.80		
	6.90	560	.70		6.90		
	6.80	540	.70		7.00		
	6.70	550	.70		7.00		
20	6.80	540	.75		6.90		
	6.90	560	.70		7.00		
	6.80	540	.75		6.90		
	6.70	550	.75		6.80		
25	6.90	550	.70		7.00		
	6.80	560	.70		7.00		
	6.80	540	.70		6.90		
	6.70	540	.70		6.90		
30	6.80	550	.75		6.90		
	6.90	540	.75		7.00		
	6.90	550	.70		7.00		
	6.90	560	.70		6.90		
35	6.70	570	.70		6.80		
	6.80	540	.70		6.90		
	6.90	550	.70				
	6.90	540	.70				
38	6.80	550	.75				
	6.70	530	.75				
	6.90	540	.75				

TABLE XX

ELECTRICAL MECHANICAL TEST DATA

PAGE 3 OF 9

MIL PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	START	STOP
CUSTOMER		CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS			
NRL 88-2				UNLESS NOTED			

PARAMETER						
TEST CONDITIONS						
P _{Lo} - .50 mW R _i = 100 Ω f _o - 9.375 GHz						
LIMITS						
DEVICE NO.	NF	ZIF	I _{dc}	NF	RF - 1 sec Watts	
	dB	ohms	mA	dB		
77	7.00	560	.70	7.00		
	6.90	540	.75	6.90		
	6.80	540	.70	6.80		
80	6.70	540	.70	6.70		
	7.00	550	.75	7.00		
	7.00	560	.70	7.00		
	6.90	550	.70	6.90		
	6.70	550	.70	6.70		
85	7.00	550	.75	7.00		
	7.00	540	.70	7.00		
	6.80	540	.70	6.80		
	6.80	550	.70	6.80		
	6.70	550	.70	6.70		
90	6.80	540	.75	6.80		
	7.00	540	.75	7.00		
	6.80	520	.80	6.80		
	7.00	540	.70	7.00		
	6.60	520	.80	6.60		
95	6.70	540	.70			
	6.80	560	.70		29	
	6.70	540	.75		31	
	6.90	560	.70		32	
	6.60	540	.75		28	
100	6.70	560	.70		30	

ELECTRICAL MECHANICAL TEST DATA

PAGE 4 OF 9

M.A. PART NO.	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	START	END
CUSTOMER	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS			
NRL 88-2			UNLESS NOTED			

TEST CONDITIONS

PARAMETERS

TEST

CONDITIONS

P_{Lo} = .50 mW R_L = 100 Ω f_o = 9.375 GHz

LIMITS

DEVICE NO.	NF	ZIF	I _{dc}
	dB	ohms	mA
101	6.80	560	.70
102	6.5	560	.75
103	6.5	530	.75
104	6.60	580	.75
105	6.60	580	.70
106	6.60	570	.70
107	6.70	560	.70
108	6.80	570	.75
109	6.70	570	.70
110	6.70	580	.70
111	6.70	570	.70
112	6.70	580	.75
113	6.60	570	.70
114	6.70	560	.70
115	6.70	570	.70
116	6.70	560	.70
117	6.70	560	.70
118	6.70	560	.70
119	6.70	560	.70
120	6.70	560	.70
121	6.70	560	.70
122	6.60	560	.70
123	6.80	560	.75
124	6.80	560	.70
125	6.80	560	.70
126	6.80	560	.70
127	6.70	560	.75
128	6.70	570	.70
129	6.70	570	.70
130	6.80	560	.70
131	6.60	560	.70
132	6.70	560	.70
133	6.70	550	.70
134	6.70	560	.75
135	6.70	560	.70
136	6.80	560	.70
137	6.70	570	.70
138	6.60	560	.70

ELECTRICAL MECHANICAL TEST DATA

PAGE 5 OF 9

1. PART NO.	2.	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	TEST START	TEST STOP
CUSTOMER		CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS		UNLESS NOTED	
NRL 88-2							

PARAMETERS			
TEST CONDITIONS	PLo - .50 mW	$R_L = 100 \Omega$	$f_o = 9.375 \text{ GHz}$
UNITS	NF	ZIF	Idc
Device	dB	ohms	mA
139	6.70	560	.70
140	6.80	560	.70
141	6.70	560	.75
142	6.70	560	.70
143	6.70	560	.70
144	6.80	560	.70
145	6.60	560	.70
146	6.60	560	.70
147	6.70	570	.70
148	6.60	560	.70
149	6.60	560	.70
150	6.70	560	.70
151	6.70	560	.70
152	6.80	560	.70
153	6.70	560	.70
154	6.70	560	.70
155	6.80	560	.70
156	6.7	560	.70
157	6.70	560	.70
158	6.70	560	.70
160	6.60	560	.70
161	6.80	560	.70
162	6.70	560	.70
163	6.70	560	.70
164	6.70	560	.70
167	6.80	560	.70
168	6.70	560	.70
169	6.80	560	.70
170	6.70	560	.70
171	6.70	560	.70
172	6.80	550	.70
173	6.70	560	.70
174	6.70	560	.70
175	6.80	560	.70
176	6.60	560	.70
177	6.70	560	.70
178	6.80	560	.70
179	6.70	560	.75

ELECTRICAL MECHANICAL TEST DATA

PAGE 6 OF 9

Q.A. PART NO. = LOT NO. SALES ORDER NO. QUANTITY SAMPLE START
CUSTOMER: NRL 88-2 CUSTOMER PART NO. CUSTOMER PURCHASE ORDER NO. OTHER DRAWINGS
Unless Noted

Environmental
Notes:

PARAMETER:

TEST
CONDITIONS:P_{Lo} = .50 mW R_L = 100 Ω f_o = 9.375 GHz

LIMITS

	NF	ZIF	I _{dc}	NF
Device No	dB	ohms	mA	dB
180	6.70	560	.70	
	6.80	560	.70	
	6.80	580	.70	
	6.70	560	.70	
	6.70	560	.70	
	6.70	560	.70	
	6.60	570	.70	
	6.70	560	.70	
	6.70	560	.70	
	6.70	560	.75	
190	6.80	560	.70	
	6.50	560	.70	
	6.60	560	.70	
	6.70	560	.70	
	6.70	560	.70	
	6.70	560	.70	
	6.70	560	.75	
	6.80	560	.70	
	6.80	560	.75	
	6.60	560	.70	
200	6.70	560	.70	
	6.80	560	.75	
	7.00	480	.80	
	7.00	490	.80	
	6.75	490	.80	
	6.90	570	.85	
	7.00	480	.75	
	7.00	500	.80	
	7.00	500	.95	
	6.50	520	.75	
210	7.20	560	.80	
	6.85	540	.80	
	6.90	500	.80	
	6.80	440	.85	
	7.00	540	.80	
	7.00	560	.75	
	7.00	560	.75	7.00
217	6.80	520	.80	6.80

ELECTRICAL MECHANICAL TEST DATA

PAGE 7 OF 9

PART NO.	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	START	END
CUSTOMER	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS			
NRL 88-2			Unless Noted			

PARAMETER						
TEST CONDITIONS	PLo - .50 mW	$R_L = 100 \Omega$	$f_o = 9.375 \text{ GHz}$			
LIMITS						
	NF	ZIF	Idc	NF		
Device	dB	ohms	mA	dB		
218	7.00	560	.75	7.00		
	7.00	560	.75	7.00		
220	7.00	540	.80	7.00		
	7.00	570	.80	7.00		
	7.00	520	.80	7.00		
	7.00	560	.80	7.00		
	6.90	550	.80	6.90		
	7.00	530	.80	7.00		
	7.00	560	.80	7.00		
	7.00	520	.80	7.00		
	7.00	520	.80	7.00		
	7.00	560	.80	7.00		
230	7.00	540	.75	7.00		
	7.00	540	.70	7.00		
	7.00	530	.80	7.00		
	7.00	560	.80	7.00		
	6.90	560	.75	6.90		
	7.00	560	.80	7.00		
	6.75	540	.75	6.70		
	6.50	570	.80	6.50		
	6.45	540	.80			
	7.00	540	.75			
240	6.60	490	.75			
	6.80	540	.70			
	6.25	540	.80			
	6.65	540	.80			
	6.55	550	.70			
	6.45	540	.80			
	7.00	650	.80			
	6.80	550	.80			
	6.80	550	.75			
	7.00	520	.85			
250	7.00	600	.70			
	6.90	550	.80			
	6.20	560	.80			
	6.50	560	.75			
	6.60	460	.75			
255	6.50	550	.70			

ELECTRICAL MECHANICAL TEST DATA

PAGE 8 OF 9

MA PART NO.	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	START	STOP
CUSTOMER		CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS		
NRL 88-2						

PARAMETERS					
TEST CONDITIONS	PLO -	50 mW	$R_L = 100 \Omega$	$f_o = 9.375 \text{ GHz}$	
LIMITS					
	NF	ZIF	Idc	NF	
Device No.	dB	ohms	mA	dB	
256	6.90	580	.75	6.90	
257	6.50	590	.75	6.70	
258	7.00	580	.70	7.00	
259	6.70	570	.70	7.00	
260	6.80	560	.70	7.00	
261	6.70	590	.70	6.70	
262	6.50	590	.70	6.80	
263	6.40	570	.75	7.00	
264	6.50	590	.70	7.00	
265	6.90	570	.75	6.90	
266	6.80	560	.70	6.80	
267	6.50	600	.70	6.90	
268	6.50	550	.70	6.60	
269	6.40	540	.65	6.90	
270	6.90	570	.70	6.90	
271	6.60	620	.70	6.80	
272	6.50	570	.70	7.00	
273	6.90	550	.75	6.90	
274	6.90	580	.70	6.90	
275	6.90	570	.75	6.90	
276	6.80	560	.75	6.80	
277	6.90	580	.65	6.90	
278	6.70	570	.70	6.70	
279	7.00	560	.70	7.00	
280	6.60	560	.70	6.60	
281	6.40	580	.70	6.40	
282	6.50	560	.80	6.50	
283	6.90	560	.70	6.90	
284	7.00	600	.70	7.00	
285	6.60	640	.70	6.60	
286	6.40	540	.70	6.40	
287	6.30	540	.75	6.30	
288	6.75	540	.75	6.75	
289	6.70	560	.70	6.70	
290	6.40	540	.70	6.40	
291	7.00	540	.75	7.00	
292	7.00	550	.80	7.00	
293	6.00	550	.75	6.00	

ELECTRICAL MECHANICAL TEST DATA

PAGE 9 OF 9

1. PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	2. START	3. STOP
CUSTOMER		CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS			
NRL 88-2				Unless Noted			

CONTENTS

PARAMETERS

TEST CONDITIONS: $P_{Lo} = .50 \text{ mW}$ $R_L = 100 \Omega$ $f_o = 9.375 \text{ GHz}$

LIMITS

	NF	ZIF	Idc	NF
Device	dB	ohms	mA	dB
294	6.70	570	.70	6.70
	7.00	570	.70	7.00
	6.40	540	.80	6.40
	6.90	550	.70	
	6.70	530	.70	
	6.60	560	.75	
+ 300	6.50	560	.75	

10.0 CONCLUSION

High burnout, low barrier height silicon Schottky barrier diodes have been manufactured in production quantities. Low cost production measures, such as 3 inch silicon epitaxial wafers, plasma etching, semi-automatic bonding, low cost pill package, semi-automatic bonding and computerized semi-automatic DC and RF testing were introduced to reduce the cost of the diode.

These devices are thermal compression bonded in a rugged low cost pill (ODS-119) package. They exhibit an overall low noise figure of 7.0 dB (single side band) at 0.5 mW of local oscillator power level and RF burnout of 12 watts ($\tau = 1 \mu\text{sec}$, and 10^3 Hz rep. rate).

Reliability and ruggedness of the diode design has been demonstrated by tests taken from MIL-S-19500 F.

AD-A116 260

M/A-COM SILICON PRODUCTS INC BURLINGTON MA F/6 13/8
MANUFACTURING TECHNOLOGY PROGRAM FOR HIGH BURNOUT SILICON SCHOT--ETC(U)
FEB 82 Y ANAND, S ELLIS N00173-79-C-0107

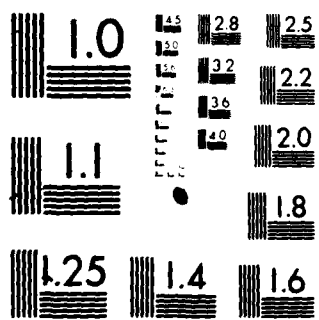
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

11.0 FUTURE WORK

Future generations of Navy missiles such as Phoenix, AMRAAM, CRUISE, HARM and Harpoon will be using Schottky barrier beam lead diodes to satisfy the requirements of microwave integrated circuitry. It is recommended that Navy should initiate the Manufacturing Technology Program to manufacture low barrier height, high burnout Schottky barrier diodes in production quantities. This will reduce the price of previous beam lead diodes of \$30 per diode to \$10 in production quantities.

The resultant diodes from this program will be more rugged, low barrier height and with high burnout resistance to RF pulses and also less susceptible to handling damage (static charge).

COST REDUCTION SUMMARY OF HIGH BURNOUT SCHOTTKY BARRIER DIODE

METHOD	PRESENT COST	COST PER DIODE AFTER COMPLETION OF THE CONTRACT
• PROCESSING SILICON CHIP	\$ 2.00	\$ 0.50
• CHIP APPROVAL MIL SPECS	\$ 5.00	\$ 1.25
• DIODE MFG. COST	\$ 8.00	\$ 4.00
• INITIAL dc & RF TEST	\$30.00	\$10.00

D-21259

TABLE XXI



APPENDIX A



**M/A-COM
SILICON PRODUCTS, INC.**

MA-4E390 Series

High Burnout, Lower Barrier Schottky Mixer Diodes*

L—Ka-Band Operation

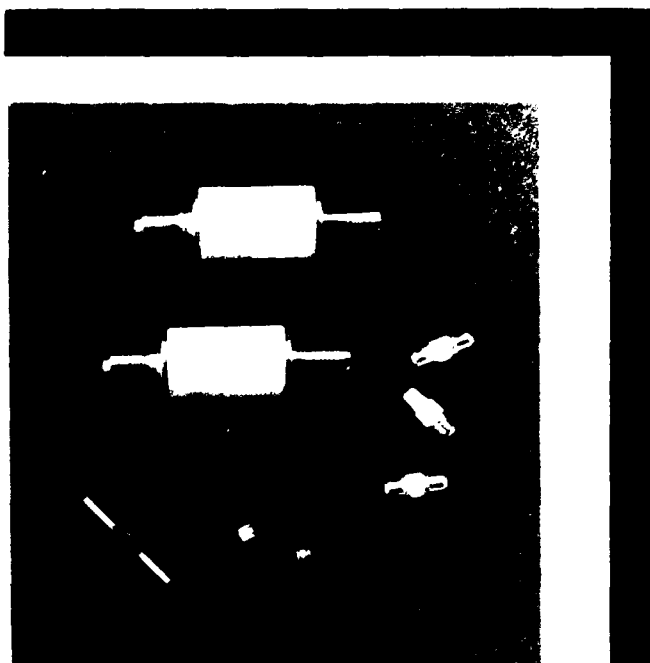
Description

These specially fabricated Schottky Barrier Mixer Diodes offer exceptional resistance to RF burnout while retaining desired operating characteristics. These silicon diodes are of planar epitaxial construction. The fabrication methods include highly accurate thicknesses and material resistivity coupled with tightly controlled photolithography, metallization and passivation techniques. The results are uniform RF and IF impedances provided by the very tight tolerances in junction capacitances. Separate devices are designed for use in L-Band through Ka-Band.

High reliability versions screened to MIL-STD-750 are available. The tables at the rear of this bulletin give the recommended screening and inspection procedures.

The case styles recommended for optimum RF performance along with high reliability capability are of the bonded diode construction with ceramic metallized hermetic seals. These case styles are the 119, 120, and 186. The 119 case style is recommended for waveguide or coaxial broadband applications through Ka-Band. It is also utilized in stripline circuits where the diodes are mounted in a coaxial section at the end of stripline circuit boards.

* Developed under Navelex funding and improved under Navy's manufacturing technology program.



Features

- **HIGH BURNOUT LEVEL**
- **LOWER BARRIER HEIGHT**
- **LOW NOISE FIGURE**
- **PASSIVATED CHIP CONSTRUCTION**
- **UNIFORM ELECTRICAL CHARACTERISTICS**

HIGH RELIABILITY

The 120 case style lends itself conveniently to stripline applications and can be modified in an alternative configuration with 4 x 20 mil straps connected to anode and cathode for easy mounting.

Applications

The MA-4E390 series of lower barrier silicon Schottky diodes shows optimum noise performance at 0 dBm and is recommended for mixer applications where low L.O. power is available and high resistance to burnout is required.

SEMICONDUCTOR DEVICES

Burlington, Massachusetts 01803 ■ Telephone (617) 272-3000 ■ TWX: 710-332-6789 ■ Telex: 94-9464

Bulletin No. 4225

Specifications @ $T_A = 25^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

SCHOTTKY BARRIER MIXER DIODES ^{1,2,3}			
Model Number	MA-4E390	MA-4E391	MA-4E392
Test Frequency (GHz)	1-8	8-12	12-18
Maximum Noise Figure (dB) ⁴	6.5	7.0	7.5
Maximum VSWR (Ratio)	1.5	1.5	1.5
IF Impedance (Ohms)	300-500	300-500	300-500

Typical Performance For MA-4E390

RF PARAMETERS ^{3,4}									RF BURNOUT ($\tau = 1 \mu\text{s.}$) POWER (Watts)
1 mW			0.75 mW			0.5 mW			
NF (dB)	I _{DC} (mA)	Z _{IF} ⁵ (Ohms)	NF (dB)	I _{DC} (mA)	Z _{IF} ⁵ (Ohms)	NF (dB)	I _{DC} (mA)	Z _{IF} ⁵ (Ohms)	
6.5	1.2	420	6.6	0.9	450	6.8	0.5	500	12.0

Summary of Model Numbers, Frequency Ranges and Applicable Case Styles

Model Number ⁶	Frequency Range (GHz)	Case Styles ⁷
MA-4E390	1-8	119, 120, 186, 54, 3, 135 and 185
MA-4E391	8-12	119, 120, 186, 54, 3, 135 and 185
MA-4E392	12-18	119, 120, 54, 135 and 185
MA-4E393	18-26	119, 120, 135, and 185
MA-4E394	26-40	120, 135 and 185

NOTES:

- All units available as matched pairs by adding the suffix "M". Matching criteria for packaged pairs: $\Delta NF_0 = 0.3 \text{ dB}$, maximum. $\Delta Z_{IF} = 25 \text{ ohms}$, maximum. Matching criteria for chips: $\Delta C = 0.5 \text{ pF}$, maximum at $V_R = 0$; $\Delta V_F = 10 \text{ mV}$ maximum at $I_F = 1.0 \text{ mA}$.
- R_S is typically 8.0 ohms .
- Junction capacitance at zero volts is typically 0.1 pF .
- Test condition: Noise figure is single sideband measured with 30 MHz IF , $NF_{IF} = 1.5 \text{ dB}$ maximum and L.O. power = 1.0 mW . Excess gas tube noise at 9.375 GHz is $15.3 \pm 0.5 \text{ dB}$; 16.0 GHz gas tube noise is $16.0 \pm 0.5 \text{ dB}$.
- Test frequency: 1 kHz .
- These diodes are thermo-compression bonded in all case styles except in case styles 3, 54, and 135. The maximum solder temperature for all case styles except 120 is 230°C for 5 seconds. For case style 120, maximum solder temperature is 200°C for 5 seconds.
- Case style 135 is a chip.

MAXIMUM RATINGS

Incident RF Peak Pulse Power (in X-Band)	12 Watts
1 μs	12 Watts
3 ns.	80 Watts
DC Forward Current	40 mA
Temperature	-65°C to $+150^\circ\text{C}$
Operating	-65°C to $+200^\circ\text{C}$
Storage	

ENVIRONMENTAL RATINGS PER MIL-STD-750

	Method	Level
Temperature Storage	1031	-65°C to $+150^\circ\text{C}$
Temperature, Operating	1026	-65°C to $+150^\circ\text{C}$
Temperature, Cycling	1051	5 cycles, -65°C to $+125^\circ\text{C}$
Thermal Shock	1056	5 cycles, 0°C to $+100^\circ\text{C}$
Moisture Resistance	1021	10 days, 90% RH, -10°C to 65°C
Shock	2016	5 blows, X_1, Y_1, Z_2 at 1500 G
Vibration Fatigue	2046	32 hours each X, Y, Z at 15 G
Vibration Variable Frequency	2056	Four 4 minute cycles, X, Y, Z at $20 \text{ G min. max. } 2000 \text{ Hz}$
Constant Acceleration	2008	1 minute each X, Y, Z at $30,000 \text{ G}$

Typical Performance Curves

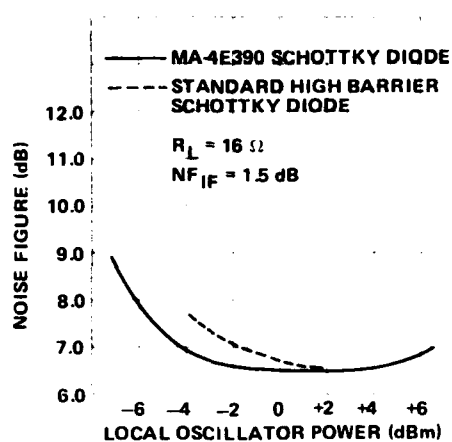


FIGURE 1. Noise Figure vs. Local Oscillator Power

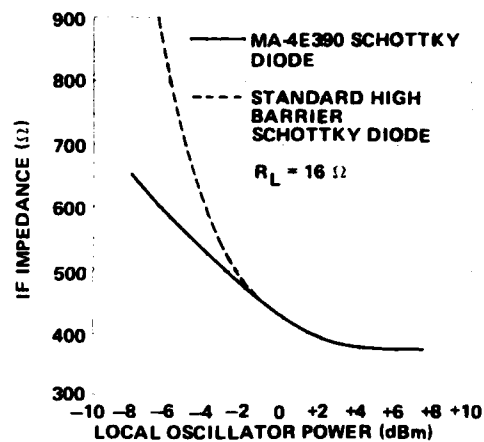


FIGURE 2. IF Impedance vs. Local Oscillator Power

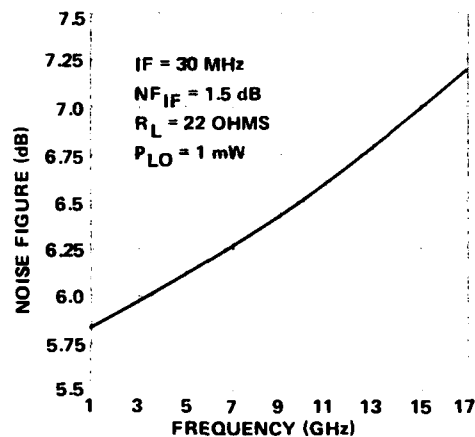


FIGURE 3. Noise Figure vs. Frequency

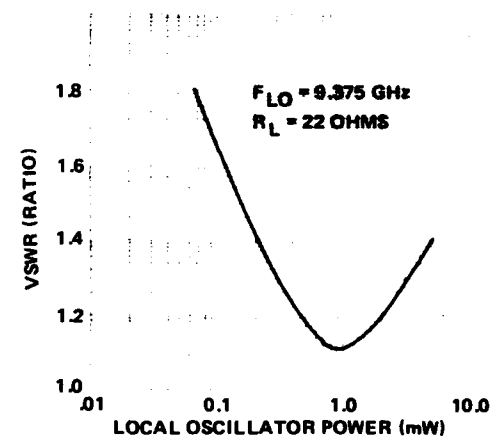
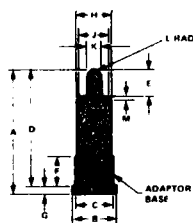


FIGURE 4. VSWR vs. Local Oscillator Power

Case Styles

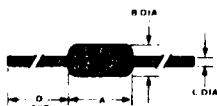
3



Dimension	0.800	0.840	20.32	21.34
A	0.292	0.296	7.42	7.52
B	0.246	0.250	6.25	6.35
C	0.753	0.783	19.13	19.89
D	0.180	0.190	4.57	4.81
E	0.193	0.199	4.90	5.05
F	0.047	0.057	1.19	1.45
G	0.222	0.240	5.64	6.10
H	0.195	0.215	4.95	5.46
I	0.092	0.094	2.34	2.19
J	0.030	0.046	0.76	1.17
K	0.020	0.030	0.51	0.76

Typical Values

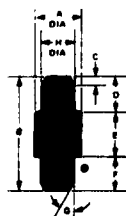
54



A	0.145	0.165	3.68	4.19
B	0.068	0.075	1.72	1.91
C	0.014	0.016	0.35	0.41
D	1.000	1.500	25.40	38.10

Typical Values

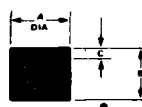
119



Dimension	0.078	0.088	1.98	2.18
A	0.190	0.210	4.83	5.33
B	0.009	0.015	0.23	0.38
C	0.060	0.064	1.52	1.63
D	0.070	0.082	1.78	2.08
E	0.080	0.084	1.52	1.83
F	25°	35°	25°	35°
G	0.060	0.084	1.52	1.83

Typical Values

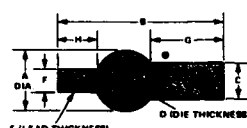
120



Dimension	0.051	0.055	1.30	1.40
A	0.040	0.050	1.02	1.27
B	0.015	0.015	0.38	0.38

Typical Values

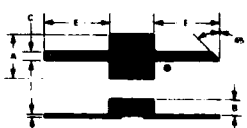
185



A	--	0.015	--	0.38
B	0.036	0.038	0.91	0.97
C	0.007	0.009	0.18	0.23
D	0.003	0.005	0.08	0.13
E	0.0003	0.0005	0.008	0.013
F	0.004	0.006	0.10	0.15
G	0.016	--	0.41	--
H	0.009	--	0.23	--

Typical Values

186



Dimension	0.044	0.044	0.75	0.75
A	0.019	0.021	0.48	0.51
B	0.019	0.021	0.48	0.51
C	0.019	0.021	0.48	0.51
D	0.019	0.021	0.48	0.51
E	0.019	0.021	0.48	0.51
F	0.019	0.021	0.48	0.51
G	0.019	0.021	0.48	0.51
H	0.019	0.021	0.48	0.51

Typical Values

Application Notes

1. Electrical Test		
2. High Temperature Storage	1031	$t = 168$ hours, $T = 150^{\circ}\text{C}$
3. Thermal Shock (Temperature Cycling) 10 Cycles	1051	-65°C to $+150^{\circ}\text{C}$
4. Fine Leak Test	1071	Condition H
5. Gross Leak Test	1071	Condition C, Step 1
6. Constant Acceleration	2006	20,000 g's, Y_1 only
7. Radiographic Inspection	2076	
8. Electrical Test: $V_F @ 10$ mA, $C_T @ V = 0\text{V}$, $F = 1$ MHz		
9. Burn-In	1038	Condition B, $t = 168$ hours $T = 100^{\circ}\text{C}$, $I_F = 10$ mA Maximum $\Delta V_F = \pm 10\%$ Maximum $\Delta C_T = \pm 10\%$
10. Electrical Test: $V_F @ 10$ mA, $C_T @ V = 0\text{V}$, $F = 1.0$ MHz		
11. Calculate Drift, ΔV_F and ΔC_T		
12. Final Visual	2071	

Subgroup 1 Physical Dimensions	2066	Per Case Style in this Bulletin	15	
Subgroup 2 Solderability	2026	Unit Aging	20	
Subgroup 3 Temperature Cycle (10 Cycles) Thermal Shock Hermetic Seal, Fine Leak Hermetic Seal, Gross Leak Moisture Resistance End Points: Noise Figure IF Impedance	1051 1056 1071 1071 1021	-65°C to $+150^{\circ}\text{C}$ Condition A Condition H Condition C, Step 1 See Electrical Characteristics See Electrical Characteristics	10	NF Z_{IF}
Subgroup 4 Shock—Non-operating Vibration Variable Frequency Constant Acceleration End Points: Same as Subgroup 3	2016 2056 2006	1500 G, $t = 0.5$ ms, 5 blows, X_1 , Y_1 , Y_2 Non-Operating 20,000 Gs, X_1 , Y_1 , Y_2	10	
Subgroup 5 High Temperature Life End Steps: Per Step 8, Table III Drift Criteria same as Step 11, Table III	1031	$T_A = 150^{\circ}\text{C}$, $t = 1000$ hours	$\lambda = 5$	
Subgroup 6 Steady State Operating Life End Points: Per Step 8, Table II Drift Criteria same as Step 11, Table III	1026	$I_F = 10$ mA, $T = 25^{\circ}\text{C}$, $t = 1000$ hours	$\lambda = 5$	

APPENDIX B

JEDEC

Solid State Products Engineering Council



ANNOUNCEMENT

of

2001 Eye Street, N.W.
Washington, D.C. 20006
(202) 467-4871

Electron Device Type Registration

Release No. 6983

November 10, 1981

The Solid State Products Engineering Council announces the registration of the following electron device designation:

1N6477

according to the ratings and characteristics found on the attached data sheets on the application of

Microwave Associates, Inc.

Burlington, MA.

All data submitted for registration, whether designated mandatory or not, become part of the formal registration. Upon publication of the release, commercial data sheets must include all data exactly as registered with all registered data identified by asterisks.

JOINT ELECTRON DEVICE ENGINEERING COUNCIL

REGISTRATION DATA

DIODE, MICROWAVE MIXER

I. General Description

This device is a silicon schottky barrier diode N/N +, high burnout, lower barrier, silicon diode designed primarily for use as a first detector in the frequency range of 1GHz to 18GHz.

II. Mechanical Data

A. Outline

OD-S-119 - Figure 1

B. Polarity

This is a reversible polarity device.

III. Maximum Ratings

A. Temperature

1. Storage temperature range, T_{stg} -55°C to 150°C

B. Current

1. Average rectified current, I_o @ .45V 1.0mA

C. Voltage

1. Peak inverse voltage at 10 μ A $\geq$ 3.0V

D. Power dissipation, 25°C ambient or case temperature

R_{θ} = 25 ohms

1. Peak power

t_p = 1 μ s, D_u = 0.001 12 Watts

2. Single Spike Power

t_p = 3nsec; D_u = 0.001 max. 80 Watts

JEDEC TYPE NUMBERIV. Electrical Characteristics, 25°C Ambient Temperature

Min.

Max.

A. Dynamic - Holder Per Figure 21. Over-all noise figure, N_{fo}

6.5 dB

 $f_o = 9.375\text{GHz}$, $F_{IF} = 30\text{MHz}$, $I_o = 1.0\text{mA}$
 or $P_{LO} = 1\text{mW}$, $R_L = 25\text{ ohms}$
2. Conversion Loss, L_c

5.5dB

 $f_o = 9.375\text{GHz}$, $F_{IF} = 30\text{MHz}$, $I_o = 1.0\text{mA}$ or
 $P_{LO} = 1\text{mW}$, $R_L = 25\text{ ohms}$
3. IF impedance, Z_{if}

250

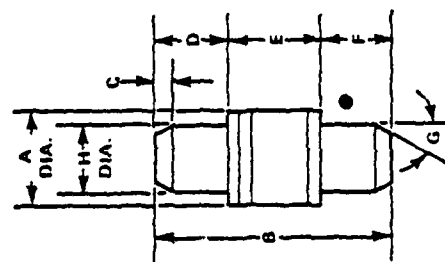
450 ohms

 $f_o = 9.375\text{GHz}$, $F_{IF} = 30\text{MHz}$, $I_o = 1.0\text{mA}$ or
 $P_{LO} = 1\text{mW}$, $R_L = 25\text{ ohms}$

4. VSWR

 ≤ 1.5
 $f_o = 9.375\text{GHz}$, $F_{IF} = 30\text{MHz}$, $I_o = 1.0\text{mA}$ or
 $P_{LO} = 1\text{mW}$, $R_L = 25\text{ ohms}$

IN6477



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.078	0.086	1.98	2.18
B	0.190	0.210	4.83	5.33
C	0.009	0.015	0.23	0.38
D	0.060	0.064	1.52	1.63
E	0.070	0.082	1.78	2.08
F	0.060	0.064	1.52	1.63
G	25°	35°	25°	35°
H	0.060	0.064	1.52	1.63

$C_P = 0.15 \text{ pF Typical}$
 $L_S = 0.50 \text{ nH Typical}$

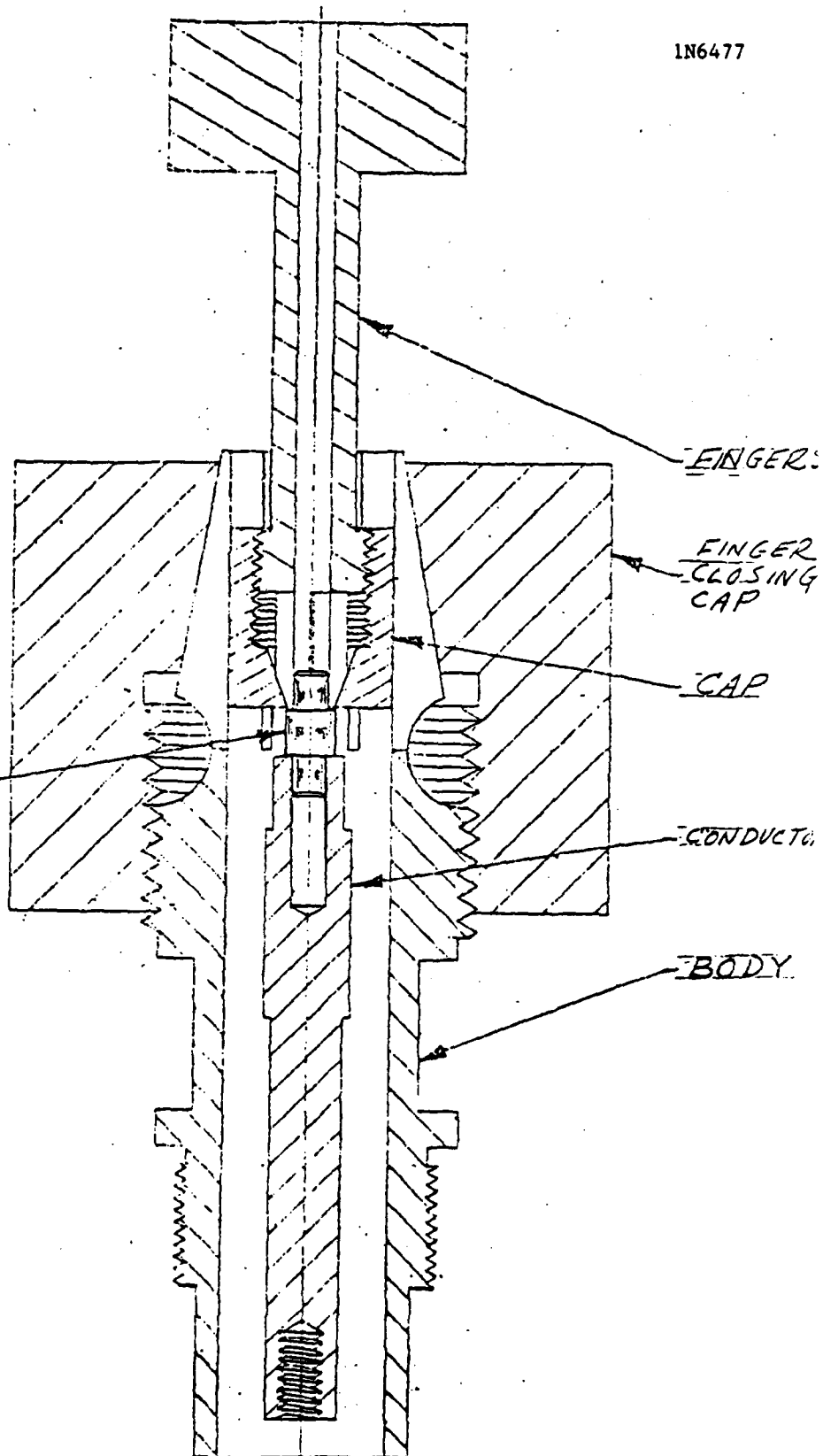
OD-S-119

FIGURE 1

JS-3
RDF-3

1N6477

OD-S-119
DIODE



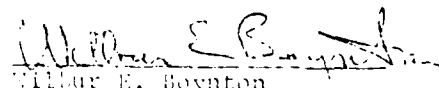
HOLDER
FIGURE 2

JS-3
RDF-3

APPENDIX C

Evaluation Of
High Burnout, Lower Barrier
Schottky Mixer Diodes
Contract #N00173-79-0107

The Schottky Barrier Mixer Diodes evaluated here were specially fabricated to offer exceptional resistance to RF burnout while retaining desired operating characteristics. They were developed under Naval Research Contract #N00173-79-C-0107.


William E. Boynton
Quality Engineer
April 15, 1982

Report No. _____

Page _____

Administrative Data

1.0 Purpose of Test:

To evaluate the high burnout X-Band Silicon Schottky Barrier Mixer diode developed on contract #N00173-79-C-0107 to the quality conformance requirements of MIL-S-19500.

2.0 Manufacturer:

Microwave Associates (M/A-COM)
Burlington, MA

3.0 Manufacturer's Type or Model No.:

NRL-88-2

4.0 Drawing, Specification or Exhibit:

Statement of work from above contract.

5.0 Quantity of Items Tested:

184

6.0 Security Classification of Items:

Not classified

7.0 Date Test Completed:

November 24, 1981

8.0 Test Conducted By:

Microwave Associates Inc. - Silicon Products*
Quality Dept.

9.0 Disposition of Specimens:

Hold for disposition

10.0 Abstract:

The units were tested in accordance with this quality conformance requirements of MIL-S-19500 for JAN type devices. Groups A,B and C testing was satisfactorily performed by Microwave Associates quality assurance personnel and audited by DCAS quality representative. These devices met all applicable requirements

Report No. _____

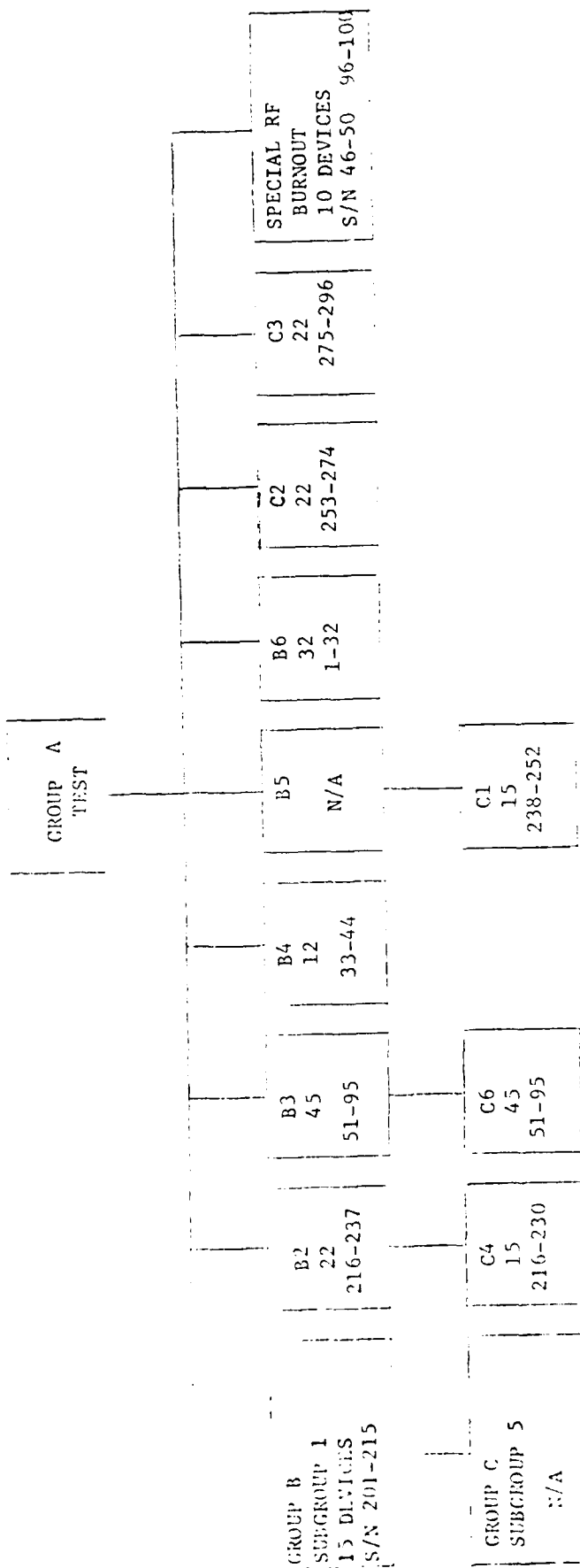
Page 2



MICROWAVE
ASSOCIATES, INC.
BURLINGTON, MASS

HIGH BURNOUT LOWER BARRIER SCHOTTKY DIODE EVALUATION

ALLOCATION OF TEST SAMPLES



CUSTOMER LEGEND

Customer 111
Customer P.O. 111
Part No. 111
Other Dwg. 111
Methods Per 111-570-750

MICROWAVE ASSOCIATES, INC.
LIFE & ENVIRONMENTAL TEST SCHEDULE/SUMMARY

Semiconductor Division

GROUP B PER MIL-S-19500F

Issue #

Initiated By:

Date:

MIL-STD-883C
PAGE 1 OF 3 PAGES
#192-481 LOT DATE
M/A Type MIL-883C
Class Schottky
M/A SO No. 111

PROGRAM REQUIREMENTS		Test Conditions		Test Limits		Estimated		Actual		Diffusion No.		Test Oper.
						Start Date	Comp. Date	Start Date	Comp. Date	Job No.	REMARKS	
SUB CP 1	Solderability	2026				10/12	10/28	11/3	11/11	5/11 201-215	from (5)	158
	Resistance to Solvents	1022				10/12	11/2			Mat. replace.		158
SUB CP 2	Thermal Shock	1051	25 cycles Test Cond. C-1			10/19	10/21	10/29	10/30	5/11 216-237		10
	Fine Leak	1071	Cond. H			10/12	10/22	11/2	11/3			11
	Gross Leak	1071	Cond. C			10/12	10/23	11/3	11/4			11
	Elect. End Pts.					10/12	10/28	11/4	11/10		to (9)	158
SUB CP 3	Steady State Life (operating)	1027	340 hours 40°C			10/12	10/14	10/2	10/19	5/11 51-95		10
	Elect. End Pts.					10/12	10/16	10/19	10/19		to (7)	158
SUB CP 4	Decap Int. Visual	2075				10/19	10/25	11/2	11/16	5/11 33		158
	Bond Strength	2037				10/11	10/12	11/2	11/16	Qty. refers to Bond Pulls. 5/11 34-44		158
SUB CP 5	Thermal Resistance		(N/A)			10/12	10/30			5/11 238-252	from (1)	158
SUB CP 6	HI Temp. Life/Storage	1032	360 hours			11/2	10/3	11/2	10/3	5/11 1-32		158
	Elect. End Pts.					10/12	10/13	10/9	10/9			158

CUSTOMER LEGEND

Customer 116
 Customer P.O. 11A
 Part No. 11A
 Other Dwg. 11A-22-2
 *Methods Per 11A-22-2

MICROWAVE ASSOCIATES, INC.
 LIFE & ENVIRONMENTAL TEST SCHEDULE/SUMMARY

Semiconductor Division

GROUP C PER MIL-S-19500F

Issue #

Initiated By:

Date:

MISC. PAGE 2 OF 3 PAGES

11A-22-2 LOT DATE CODE

M/A Type 11A-22-2

Class 11A-22-2

M/A SO No. 11A

PROGRAM REQUIREMENTS				Test Limits	Estimated		Actual		Diffusion No.	Test Oper.	
Examination/Test	Method No.	Test Conditions			Start Date	Comp. Date	Start Date	Comp. Date			
SUB GP1 Physical Dimension	2066	2066-119 THERMAL SHOCK				10/19	10/23	11/4	11/4	111238-252 10 (65)	H.
SUB GP2 Glass Strain						10/19	10/20	10/27	10/27	111253-274	H.
Thermal Shock	1056	Cond. A				10/21	10/22	11/4	11/5		H.
Terminal Strength	2036	Cond. 7 Torque				10/22	10/22	11/5	11/5		H.
Fine Leak	1071					10/22	10/22	11/5	11/5		H.
Gross Leak	1071					10/22	10/22	11/6	11/7		H.
Moisture Resistance	1021					10/27	11/6	11/10	11/10		H.
External Visual	2071					11/9	11/9	11/10	11/10		H.
Elect End Points						11/10	11/12	11/10	11/24	111275-296	D.C.
SUB GP3 Shock	2016	3 planes 1500 G's 0.5ms				10/19	10/23	11/3	11/3		H.
Vibration						10/19	10/20	11/3	11/3		H.
Var. Freq.	2056					10/19	10/20	11/3	11/3		H.
Constant Acceleration	2006	20K4-3 planes X, Y, Z				11/2	11/4	11/3	11/3		H.
Elect End Pts.						11/5	11/9	11/3	11/11	111275-296	D.C.

CUSTOMER LEGEND

Customer NRL
 Customer P.O. N/A
 Part No. N/A
 Other Dwg. MIL-STD-750
 *Methods Per MIL-STD-750

MICROWAVE ASSOCIATES, INC.
 LIFE & ENVIRONMENTAL TEST SCHEDULE/SUMMARY

Semiconductor Division

GROUP C (CONTINUED)

MISC. PAGE 3 OF 3 PAGES
 #1981-4819 LOT DATE
 CODE
 M/A Type NRL-88-2
 Class Schottky
 M/A SO No. N/A

Issue # _____ Date: _____ Initiated By: _____

PROGRAM REQUIREMENTS														Diffusion No.		Test Oper.	
Examination/Test		*Method No.	Test Conditions		L	O	B	N	Test Limits		Estimated		Actual		Job No.		REMARKS
					T	T	E	E			Start Date	Comp. Date	Start Date	Comp. Date			
SUB GP4	Salt Atmosphere	1041	.6% Salt Solution		15	15	0	15	24 Hrs.		10/29	11/4	11/10	11/11	S/N 216-230 from (B2)		RJ
SUB GP5	Barometric Pressure		N/A		15	15	—	—			10/19	10/23	—	—	S/N 201-215 to (B1)		N/A
SUB GP6	Steady State Life (Operating)	1026	1000 hrs.		—	45	—	45			10/16	11/13	10/19	11/13	Samples from GP (B3) to be continued.		JD
	Elect. End Pts.				45	0	45	45			11/16	11/18	11/16	11/20	 S/N 51-73		C.D.B
SPECIAL TEST																	
R.F. BURROW																	

MICROWAVE ASSOCIATES, INC.

SEMICONDUCTOR DIVISION

ELECTRICAL/MECHANICAL TEST DATA

PAGE 1 OF 9

M.A. PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	START	9/21/81
	1981-4819					COMP	10/9/81
CUSTOMER	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS				
NRL 88-2			T _A = 25°C Unless Noted				

Environmental
Test(s)

QUAL TEST

PARAMETER

TEST
CONDITIONSP₁₀ = .50 mW R_L = 100 Ω

f = 9.375 GHz

LIMITS

GROUP A

POST
TEST

NF

Z_{IF}I_{DC}

NF

Device
No.

dB

ohms

mA

dB

1

6.90

560

.75

7.00

6.80

560

.70

6.90

6.90

560

.70

7.00

6.70

550

.75

6.80

5

6.80

565

.80

6.90

6.90

560

.70

7.00

6.70

550

.70

6.90

6.90

565

.70

7.00

6.80

540

.70

6.90

10

6.90

550

.75

7.00

6.70

560

.75

6.90

6.80

560

.70

6.90

6.80

560

.70

6.90

6.90

560

.70

6.90

15

6.80

540

.70

7.00

6.70

550

.70

7.00

6.80

540

.75

6.90

6.90

560

.70

7.00

6.80

540

.75

6.90

20

6.70

550

.75

6.80

6.90

550

.70

7.00

6.80

560

.70

7.00

6.80

560

.70

6.90

6.70

540

.70

6.90

25

6.80

550

.75

6.70

6.90

540

.75

7.00

6.90

540

.75

7.00

6.80

550

.75

7.00

6.90

550

.70

7.00

30

6.90

560

.70

6.70

6.70

570

.70

6.80

6.80

540

.70

6.90

6.90

550

.70

7.00

6.90

540

.70

7.00

35

6.80

550

.75

7.00

6.70

530

.75

7.00

6.90

540

.75

7.00

GOVT. PROPERTY
RESTRICTED TO THE
USE OF THE GOVT.

B-4



JUN 1981

MICROWAVE ASSOCIATES, INC.

SEMICONDUCTOR DIVISION

ELECTRICAL/MECHANICAL TEST DATA

PAGE 2 OF

M.A. PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	DATE	START	9/21/81
	1951-4819						COMP	11/20/81
CUSTOMER	CUSTOMER PART NO.		CUSTOMER PURCHASE ORDER NO.		OTHER DRAWINGS			
NRL 88-2					T _A = 25°C Unless Noted			

Environmental
Test(s)

QUAC TEST

PARAMETER

TEST
CONDITIONSP_{LO} = 150 mWR_L = 100 Ωf₀ = 9.375 GHz

LIMITS

Group A

Post
TEST

RF = 1 mW

UF Z_{IF} I_{DC}

NF

Watts

Device
No.

dB ohms mV

dB

39

6.80 560 .70

6.90 540 .70

6.80 540 .75

6.70 540 .70

6.80 550 .70

6.70 540 .70

45

6.90 550 .70

6.8 530 .75

6.9 450 0.75

6.8 520 0.7

6.9 520 0.7

50

6.9 550 0.7

7.00 540 .70

6.80 560 .70

7.00 560 .70

6.80 560 .70

55

6.90 540 .70

6.90 565 .70

7.00 540 .70

7.00 540 .70

6.90 540 .75

60

7.00 540 .70

6.90 550 .70

7.00 560 .70

6.80 550 .70

6.90 550 .75

65

7.00 540 .70

6.90 540 .70

6.90 560 .70

6.70 550 .80

6.80 540 .70

70

6.90 540 .70

7.00 550 .70

7.00 540 .70

6.90 530 .70

6.80 540 .70

75

6.90 540 .70

6.90 540 .70

6.90 540 .70

6.90 540 .70

B-4

15

19.5

31

19

20

RF Burnout

B3 + C6

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MICROWAVE ASSOCIATES, INC.

SEMICONDUCTOR DIVISION

ELECTRICAL/MECHANICAL TEST DATA

PAGE 3 OF

M.A. PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	DATE	START	9/21/81
	1901-4819						COMP	11/20/81
CUSTOMER	CUSTOMER PART NO.		CUSTOMER PURCHASE ORDER NO.		OTHER DRAWINGS		T.A. 2533	
NRL 88-2							Unless noted	

Environments: Test(s)		QUAL TEST									
PARAMETER											
TEST CONDITIONS		P _{LO} = .50 mW			P _L = 100uW			f _o = 9.375 GHz			
LIMITS		GROUP A			POST TEST						
		NF	ZIF	IDC	NF			RF =	YAC		
Device No.		dB	ohms	mA	dB			Watts			
77	7.00	560	.70	7.00							
	6.90	540	.75	6.90							
	6.80	540	.70	6.80							
80	6.70	540	.70	6.70							
	7.00	550	.75	7.00							
	7.00	560	.70	7.00							
	6.90	550	.70	6.90							
	6.70	550	.70	6.70							
	7.00	550	.75	7.00							
85	7.00	540	.70	7.00							
	6.80	540	.70	6.80							
	6.80	550	.70	6.80							
	6.70	550	.70	6.70							
	6.80	540	.75	6.80							
	7.00	540	.75	7.00							
90	6.80	520	.80	6.80							
	7.00	540	.70	7.00							
	6.60	520	.80	6.60							
95	6.70	540	.70	6.70							
	6.80	560	.70								
	6.70	540	.75								
	6.90	560	.70								
	6.60	540	.75								
	6.70	560	.70								
100	6.70	560	.70								



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MICROWAVE ASSOCIATES, INC.

SEMICONDUCTOR DIVISION Page 7

ELECTRICAL/MECHANICAL TEST DATA

PAGE 4 OF

M.A. PART NO. NRL-88-2	= 1981-4819	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	START 9/21/81	COMP 9/21/81
CUSTOMER	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS		T _A = 25°C Unless Noted		

Environmental Test(s)	QUAL TEST									
PARAMETER										
TEST CONDITIONS	GROUP A									
LIMITS	P _{LO} = 0.5mW, R _L = 100Ω, f _o = 9.375 GHz									
	NF	Z _{IF}	I _{DC}							
Device No.	dB	ohms	mA							
101	6.8	560	0.7							
102	6.5	560	0.75							
103	6.5	530	0.75							
104	6.6	580	0.75							
105	6.6	580	0.7							
106	6.6	570	0.7							
107	6.7	560	0.7							
108	6.8	570	0.75							
109	6.7	570	0.70							
110	6.7	550	0.70							
111	6.7	570	0.70							
112	6.7	580	0.75							
113	6.6	570	0.70							
114	6.7	560	0.70							
115	6.7	570	0.70							
116	6.7	560	0.7							
117	6.70	560	0.7							
118	6.7	560	0.7							
119	6.7	560	0.7							
120	6.7	560	0.7							
121	6.7	570	0.7							
122	6.6	560	0.7							
123	6.8	560	0.75							
124	6.8	560	0.70							
125	6.8	560	0.7							
126	6.8	560	0.70							
127	6.7	560	0.75							
128	6.7	570	0.70							
129	6.7	570	0.70							
130	6.8	560	0.70							
131	6.6	560	0.70							
132	6.7	560	0.70							
133	6.7	570	0.7							
134	6.7	560	0.75							
135	6.7	570	0.70							
136	6.8	560	0.70							
137	6.7	570	0.70							
138	6.7	570	0.70							

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MICROWAVE ASSOCIATES, INC.

SERIES 1000

ELECTRICAL/MECHANICAL TEST DATA

PAGE 5 OF

M.A. PART NO.	= 1981-4819	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	DATE START 9/21/81 COMP 9/21/81
CUSTOMER NRL 80-2	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS	T _A = 25°C Unless Noted		

Environmental Test(s)	QUAL TEST		
PARAMETER	GROUP A		
TEST CONDITIONS	P _{LO} = .50 mW R _L = 100Ω f ₀ = 9.375 GHz		
LIMITS			
	NIF	Z _{in}	I _{DC}

Device No.	dB	ohms	mA
139	6.7	560	0.7
140	6.8	560	0.7
141	6.7	560	0.70
142	6.7	560	0.70
143	6.7	560	0.70
144	6.8	560	0.70
145	6.6	560	0.70
146	6.6	560	0.70
147	6.7	570	0.70
148	6.6	560	0.70
149	6.6	560	0.70
150	6.7	560	0.70
151	6.7	560	0.70
152	6.8	560	0.70
153	6.7	560	0.70
154	6.7	560	0.70
155	6.8	560	0.70
156	6.7	560	0.70
157	6.7	560	0.70
158	6.7	560	0.70
160	6.6	560	0.70
161	6.8	560	0.70
162	6.7	530	0.70
163	6.7	560	0.70
164	6.7	570	0.70
165	6.8	560	0.70
166	6.7	560	0.70
169	6.8	530	0.70
170	6.7	530	0.70
171	6.7	560	0.70
172	6.8	560	0.70
173	6.7	560	0.7
174	6.7	570	0.7
175	6.8	520	0.7
176	6.6	560	0.7
177	6.7	520	0.7
178	6.8	510	0.7
179			

Supply availability to MILC 4000 will
be maintained until production



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SEMICONDUCTOR DIVISION

ELECTRICAL/MECHANICAL TEST DATA

PAGE 6 OF

M.A. PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	DATE	START	9/21/81
	1981-4919						COMP	11/16/81
CUSTOMER	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.		OTHER DRAWINGS		T _A = 25°C		
NRL 88-2						Unless Noted		

Environmental Test(s)	QUAL TEST							
PARAMETER	GROUP A				POST TEST			
TEST CONDITIONS	P _{LO} = .50 mW				R _L = 100 Ω		f ₀ = 9.375 GHz	
LIMITS								
	NF	Z _{IF}	I _{DC}		NF			
Device No	dB	ohms	mA		dB			
180	6.70	560	.70					
	6.80	560	.70					
	6.80	580	.70					
	6.70	560	.70					
	6.70	560	.70					
	6.70	560	.70					
	6.80	570	.70					
	6.70	560	.70					
	6.70	560	.70					
	6.70	560	.75					
190	6.80	560	.70					
	6.50	560	.70					
	6.60	560	.70					
	6.70	560	.70					
	6.70	560	.70					
	6.70	560	.70					
	6.70	560	.75					
	6.80	560	.70					
	6.80	560	.75					
	6.60	560	.70					
200	6.70	560	.70					
	6.80	560	.75					
	7.00	490	.80					
	7.00	490	.80					
	6.75	490	.80					
	6.90	570	.85					
	7.00	480	.75					
	7.00	570	.80					
	7.00	500	.95					
	6.50	520	.75					
210	7.20	560	.70					
	6.85	500	.80					
	6.90	570	.80					
	6.70	440	.80					
	7.00	800	.80					
	7.00	560	.75					
	7.00	560	.75					

C5 + B1

C5 + C4

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C5-1E

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ELECTRICAL/MECHANICAL TEST DATA

PAGE 7 OF

M.A. PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	DATE	START	9/21/81
	1981-4819						COMP	11/10/81
CUSTOMER	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS					
N12L 88-2			T _A = 25°C Unless Noted					

Environment(s)	QUAL TEST							
PARAMETER	GROUP A				POST			
TEST CONDITIONS	P _{LO} = .50 mW				R _L = 100Ω			
LIMITS					f = 9.375 GHz			
Device No.	NF	2IF	IDC	NF				
218	dB	dBm	mA	dB				
	7.00	560	.75	7.00				
	7.00	560	.75	7.00				
220	7.00	540	.80	7.00				
	7.00	570	.80	7.00				
	7.00	520	.80	7.00				
	7.00	560	.80	7.00				
	6.90	550	.80	6.90				
	7.00	530	.80	7.00				
	7.00	560	.81	7.00				
	7.00	570	.80	7.00				
	7.00	580	.87	7.00				
	7.00	560	.80	7.00				
230	7.00	540	.75	7.00				
	7.00	540	.70	7.00				
	7.00	530	.80	7.00				
	7.00	560	.80	7.00				
	6.90	560	.75	6.90				
	7.00	560	.80	7.00				
	6.75	540	.75	6.70				
	6.50	570	.80	6.50				
	6.45	540	.80					
	7.00	540	.75					
240	6.60	6190	.75					
	6.80	540	.70					
	6.25	540	.80					
	6.65	500	.80					
	6.55	550	.70					
	6.45	540	.80					
	7.00	650	.80					
	6.80	550	.80					
	6.80	550	.75					
	7.00	520	.85					
250	7.00	600	.70					
	6.90	550	.80					
	6.20	560	.80					
	6.50	560	.75	7.00				
	6.60	560	.75	6.70				

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ELECTRICAL/MECHANICAL TEST DATA

PAGE 8 OF

M.A. PART NO.	1981-4819	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	DATE	START	9/21/81
CUSTOMER	RRL-88-2	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.	OTHER DRAWINGS	T _A = 25°C Unless Noted			

QUAL TEST									
PARAMETER	GROUP A				POST TEST				
TEST CONDITIONS	P _{LO} = .50 mW				RL = 100 Ω	f ₀ = 9.375 GHz			
LIMITS									
	NF	2IF	IOG		NF				
Device No.	dB	dBm	mA		dB				
956	6.90	580	.75		6.90				
257	6.50	590	.75		6.70				
258	7.10	580	.70		7.00				
259	6.70	570	.70		7.00				
260	6.80	560	.70		7.00				
261	6.70	590	.70		6.70				
262	6.50	590	.70		6.80				
263	6.40	570	.75		7.00				
264	6.30	590	.70		7.00				
265	6.90	570	.75		6.90				
266	6.80	530	.70		6.80				
267	6.50	600	.70		6.90				
268	6.50	550	.70		6.60				
269	6.40	500	.65		6.90				
270	6.90	570	.70		6.90				
271	6.60	620	.70		6.80				
272	6.50	570	.70		7.50				
273	6.90	550	.65		6.90				
274	6.90	580	.70		6.90				
275	6.90	570	.75		6.90				
276	6.80	560	.75		6.80				
277	6.90	580	.65		6.90				
278	6.70	570	.70		6.70				
279	7.00	560	.70		7.00				
280	6.60	560	.70		6.60				
281	6.40	580	.70		6.40				
282	6.50	560	.80		6.50				
283	6.90	560	.70		6.90				
284	7.00	600	.70		7.00				
285	6.60	640	.70		6.60				
286	6.60	540	.70		6.40				
287	6.30	540	.75		6.30				
288	6.75	540	.75		6.75				
289	6.70	560	.70		6.70				
290	6.40	500	.70		6.40				
291	7.10	540	.75		7.00				
292	7.20	550	.80		7.00				

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ELECTRICAL/MECHANICAL TEST DATA

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M.A. PART NO.	=	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE	DATE	START	9/11/81
	1981-4819						COMP	11/9/81
CUSTOMER	CUSTOMER PART NO.		CUSTOMER PURCHASE ORDER NO.		OTHER DRAWINGS			
NRL 88-2					T _A = 25°C Unless Noted			

Environmental Test(s)	QUAL TEST							
PARAMETER	GROUP A				POST TEST			
TEST CONDITIONS	P _{LO} = .50 mW				R _L = 100 Ω			
					f ₀ = 9.375 GHz			
LIMITS								
	NF	2IF	IF		NF			
Device No.	dB	ohms	mA		dB			
294	6.70	570	.70		6.70			
	7.00	570	.70		7.00			
	6.40	540	.80		6.40			
	6.90	550	.70					
	6.70	530	.70					
	6.80	560	.75					
4300	6.50	560	.75					

1981-4819

Group B
Subgroup 4

REPORT OF

INTERNAL VISUAL DESIGN VERIFICATION (DECAP)

M/A. TYPE # NRL-88-2

SALES ORDER # _____

CUSTOMER TYPE # _____

PURCHASE ORDER # N00173-79-C-0107REFERENCE SPECIFICATIONS MIL-S-19500

S/N 33

PROCEDURE:

DEID UNIT BY REFLOWING SOLDER AT CAP.
EXAMINE INTERNAL CONSTRUCTION FOR CONDITION OF
CHIP, WIRE, THERMOCOMPRESSON BOND, SOLDER,
ALIGNMENT OF PARTS AND EXISTANCE OF FOREIGN MATERIALS

RESULTS:

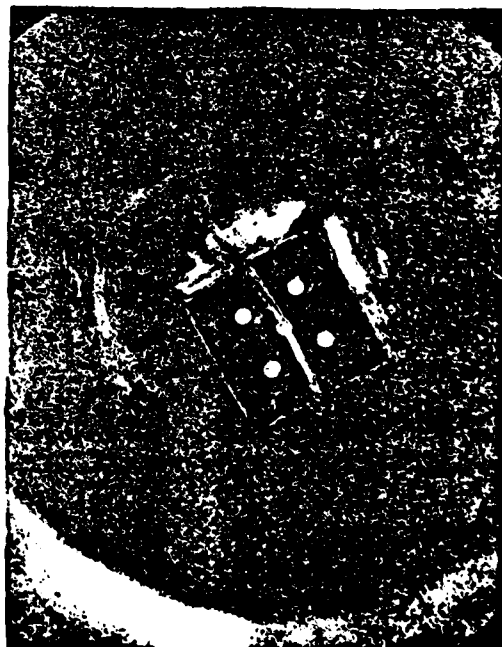
ALL PARTS, BONDS
AND SOLDER JOINT
WERE NORMAL
(SEE PHOTO)

CONCLUSIONS:

UNIT MEETS THE
REQUIREMENTS OF
THE APPLICABLE
SPECIFICATIONS

U. Boynton 11/6/81

Report No. _____



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BURLINGTON, MASS.

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SEMICONDUCTOR DIVISION

BURLINGTON, MASS. 01803

1991-4819

BOND PULL TEST RESULTS

CUSTOMER

N. R. L.

Group B

Subgroup 4

CUSTOMER P.O. NO.

N00173-79-C-0107

CUSTOMER PART NO.

W/A SALES ORDER NO.

W/A PART NO.

SPECIAL SCHOTTKY DIODE

PULL TEST PER

MIL-STD-750 METHOD COND

NUMBER OF UNITS IN LOT

11

NUMBER OF UNITS SAMPLED

11

FREQUENCY OF SAMPLING

QUAL TEST

BOND IDENTIFICATION

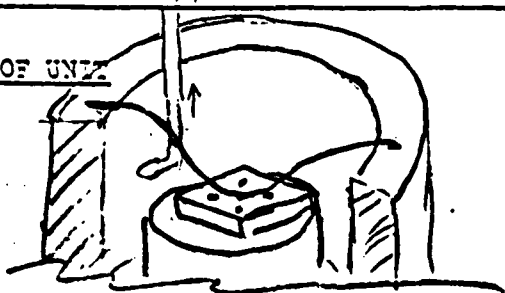
GOLD WIRE (.0007") THERMAL COMPRESSION BOND

MINIMUM PULL STRENGTH

1.5 GRAM.

<u>UNIT NO.</u>	<u>FORCE</u>	<u>UNIT NO.</u>	<u>FORCE</u>	<u>UNIT NO.</u>	<u>FORCE</u>	<u>UNIT NO.</u>	<u>FORCE</u>
1	1.4	11	1.5	1		1	
2	2.6	2		2		2	
3	7.5	3		3		3	
4	3.7	4		4		4	
5	2.5	5		5		5	
6	2.7	6		6		6	
7	0.8	7		7		7	
8	1.7	8		8		8	
9	3.7	9		9		9	
10	1.5	10		10		10	

SKETCH OF UNIT



COMMENTS

UNIT #8 WIRE BROKE MID SPAN
ALL OTHERS LIFTED METAL FROM CH

W. Boynton 11/5/8

MICROWAVE ASSOCIATES, INC.

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SEMICONDUCTOR DIVISION

ELECTRICAL/MECHANICAL TEST DATA

PAGE OF

M.A. PART NO. NRL-88-2	CT# 1781-4819	LOT NO.	SALES ORDER NO.	QUANTITY	SAMPLE 15	DATE START 11/4/81 COMP. 11/4/81
CUSTOMER NRL	CUSTOMER PART NO.	CUSTOMER PURCHASE ORDER NO.			OTHER DRAWINGS T _A = 25±3°C Unless Noted	

Environmental Test(s)	Group C Subgroup 1									
PARAMETER	A	B _A	B _C	C	D	E	F	G		
TEST CONDITIONS										
LIMITS min	.078	.060	.060	.190	.070	.060	.060	30°		
max	.086	.064	.064	.210	.082	.064	.064			
Device No.	138	.080	.060	.061	.206	.078	.062	.064	✓	
139	.080	.060	.061	.206	.081	.062	.062	✓		
140	.078	.060	.060	.205	.080	.064	.063	✓		
141	.079	.061	.061	.205	.082	.063	.062	✓		
142	.078	.060	.061	.205	.081	.061	.063	✓		
143	.070	.060	.061	.207	.081	.064	.062	✓		
144	.078	.061	.061	.207	.082	.063	.062	✓		
145	.078	.060	.061	.207	.080	.062	.064	✓		
146	.079	.060	.061	.206	.082	.062	.064	✓		
147	.078	.060	.061	.205	.081	.062	.064	✓		
148	.079	.060	.061	.206	.082	.061	.063	✓		
149	.079	.060	.061	.205	.081	.061	.062	✓		
150	.079	.060	.061	.206	.082	.063	.064	✓		
151	.080	.060	.061	.206	.081	.063	.063	✓		
152	.079	.060	.061	.206	.081	.064	.062	✓		

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4. TITLE (and Subtitle) Manufacturing Technology Program for High Burnout Silicon Schottky-Barrier Mixer Diodes for Navy Air-To-Air Avionics		5. TYPE OF REPORT & PERIOD COVERED Final Report May 1979 to Nov. 1981
7. AUTHOR(s) Dr. Yoginder Anand Steven Ellis		6. PERFORMING ORG. REPORT NUMBER
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11. CONTROLLING OFFICE NAME AND ADDRESS Naval Research Laboratory Washington, D.C. 20375		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		12. REPORT DATE February 1982
		13. NUMBER OF PAGES 88
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18. SUPPLEMENTARY NOTES Schottky Barrier Diodes High Burnout Mixer Diodes Mixer Diodes		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report describes the establishment of low cost semiconductor processes to manufacture low barrier height high burnout X-band silicon Schottky barrier diodes in production quantities. These devices are thermal compression-bonded in a rugged low cost pill (ODS-119) package. They exhibit an overall low noise figure of 7.0 dB (single side band) at 0.5 mW of local oscillator power level and RF burnout of 12 watts ($\tau = 1 \mu\text{sec}$ and 103 Hz rep. rate). Reliability and ruggedness of the design has been demonstrated by tests taken from MIL.S. 19500F.		

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