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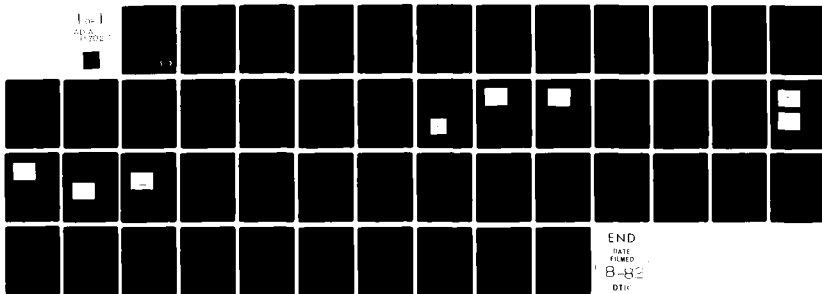
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DNA SUPPORT SERVICES

D. Snowden

J. Harrity

IRT Corporation

P.O. Box 80817

San Diego, California 92138

31 January 1981

Final Report for Period 15 January 1980—31 January 1981

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PREFACE

Two main areas are covered in this report: the latchup window research and the standards development support. Both of these activities of IRT Corporation were funded by DNA under Contract DNA 001-80-C-0106. The Task I report has been prepared by Dr. Donald Snowden who is responsible for the latchup window research program. The Task II report was prepared by Mr. John Harrity, who represents IRT and DNA on the F-1.11 Subcommittee of the ASTM Committee on Electronics and the Space Parts Working Group, with input from Dr. Norman Lurie who has been serving on the ASTM E10.07 Subcommittee on Radiation Effects on Electronic Materials and Devices.



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TASK I: LATCHUP WINDOW RESEARCH (D. Snowden)

I. INTRODUCTION

In a previous study at IRT a new, until then unreported, latchup behavior was discovered in several CD 4000 series CMOS devices. It was found that latch-up would occur in these devices over only a restricted range of dose rate of high energy electron irradiation. At dose rates both above and below this range, latch-up was not induced. We have termed this phenomenon a "latch-up window." In addition to being of interest from a general technical point of view, an understanding of this phenomenon is of importance since it brings into question the validity of conventionally practiced latch-up screening procedures.

In the present study, samples were obtained of the three device types which had been found previously to exhibit the latch-up window, the CD4047A, CD4061A, and CD4094B. These devices were screened using the IRT Linac to determine which specific ones exhibited the latch-up window, which latched normally, and which did not latch.

Mask sets for each of the device types were obtained from RCA through the generous assistance of Mr. Eugene Reiss, Manager of Engineering, High Reliability Products at the RCA Somerville plant. Complete latch-up path analysis has been carried out using these sets for the CD4047A and the CD4094B and a partial analysis has been performed for the CD4061A. In the first two of these devices the only potentially latchable paths involve input protection circuitry and include the n substrate and the p-well(s) as the second and third elements of the pnpn latchable paths. In the third device this type of path is present and, in addition, the possibility of a different path exists.

Samples of both latching and nonlatching devices of types CD4047A and CD4094B were de-lidded and electrically probed both with and without pulsed excitation from a GaAs laser diode which produces light with photon energy greater than the band gap of silicon and hence produces hole-electron pairs in the device just as high energy electrons do. Two major differences occur in this hole-electron production. While high energy electrons produce carrier pairs uniformly throughout the material, laser photons

produce carriers only in the optical absorption length, $\sim 2 \times 10^{-3}$ cm at the wavelength used. In addition, device metallization produces shadowing with optical excitation, i.e., carriers are not generated under metallized regions. Carriers can be expected to reach these regions by diffusion, however, in reduced concentration. Finally, with the laser diodes used, only a portion of the chip could be illuminated at any one time at sufficient intensity.

Latching behavior was induced in several CD4047's and in one CD4094B. No definite latchup window was seen in any of these devices. Voltage probing during latching verified the paths identified from analysis in the CD4047A and partially verified the paths in the CD4094B.

A possible mechanism has been identified to explain the latchup window. In this mechanism, increase in the conductivity of the substrate and/or p-well portion of the latchable path due to carrier generation by the ionizing radiation serves to inhibit latchup at high dose rates. Unfortunately, it was not possible to verify this mechanism during the present program since a latchup window was not seen with laser photon ionization, probably because insufficient photon flux was available. Alternatively, shadowing due to metallization may also play a role in this failure.

In the following sections we describe the electron screening of the devices, the mask-set analysis, and the device probing. The latchable paths are described and the proposed mechanism for the creation of the latchup window is discussed. Finally we suggest additional experimental studies which would further clarify the latchup window phenomenon and would test the proposed mechanism.

2. FIRST OBSERVATIONS OF THE LATCHUP WINDOW EFFECT

IRT was performing a test program for Sandia National Laboratories when the latchup window effect was first observed. In that program small lots of 69 CMOS CD-4000 series integrated circuit part types were surveyed. The goal of that program was to demonstrate the efficacy of neutron irradiation and anneal in raising the upset threshold and eliminating latchup.^(1,2) To accomplish this ten parts of each part type

¹Gammill, Paul E., "The Effect of Neutron Irradiation on the Latchup and Logic Upset of the RCA CD-4000 A- and B-Series CMOS Integrated Circuits on a Gamma-Dot ($\dot{\gamma}$) Environment," Sandia Laboratories Report SAND80-0333, March 1980.

²Harrity, J. W., and Gammill, P.E., "Upset and Latchup Thresholds in CD-4000 Series CMOS Devices," Poster Paper A-7, 1980 Annual Conference on Nuclear and Space Radiation Effects held at Cornell University, Ithaca, New York, July 15-18, 1980.

were tested, five of which were from the same lot, but which had been exposed to 10^{14} n/cm² and annealed. The upst and latchup thresholds for all units were measured in each of two operating states. On three different part types the latchup window was observed in some units of the non neutron-irradiated parts.

Figures 1, 2 and 3 show the electrical configuration used in the testing of these three part types. IRT's automated Latchup Screen Test System (LSTS) was used to bias and control the circuits during the tests. This system contains programmable power supplies for biasing the test device and for providing comparison voltages for comparators which monitor output voltage and power supply current levels. The logic system of the LSTS performs functional testing of the device under test, and controls firing of the Linac and timing of the post-radiation test of the return to normalcy. All tests were performed with a V_{DD} of 10V and the V_{SS} pin grounded. Logic high input of +9V was used and input low was 0V. Any input pin which did not have to be exercised during establishment of the test bias conditions was tied either to +10V or to ground. Output voltages were monitored with the LSTS comparators. These outputs labeled V01 and V02 were also tied to line driver inputs which drove 50-ohm terminated signals to oscilloscopes in the data area. The LSTS which operates essentially in the dc mode loads these outputs with approximately 600 pf. The bias supply is a stiff supply with 1-ohm source impedance due to the current monitoring circuit, but the dynamic impedance of the bias source at short times is much lower than this due to the bypass capacitors located within eight inches of the test device. The bypass capacitors consist of 10 μ F nonpolar electrolytics paralleled with 0.01 μ F ceramic disks. This combination provides the capability of supplying very high initial surges of current (exceeding 5A) but with a time constant which assures that currents measured with the LSTS at 50 μ s or later times reflect true values. During these tests the timing for latchup detection and determination was set for 500 μ s. Oscilloscope photographs showed latchup currents equilibrating to a steady-state value in most cases by 100 μ s. When latchup was detected at 500 μ s, the power supplies were automatically crowbarred to prevent damage to the test device.

Steady-state latchup currents observed in the CD4047A devices ranged from 175 to 340 mA; in the CD4061A devices they were all about 150 mA; and in the CD4094B units they were in the 300 to 400 mA range.

The window was observed first in the testing of the CD4094. S/N 1 appeared to have a very narrow window, as latchup was only observed once in the V_{01} -Hi state and not at all in the V_{01} -Lo state. S/N 4 appeared to have a normal response; however, one

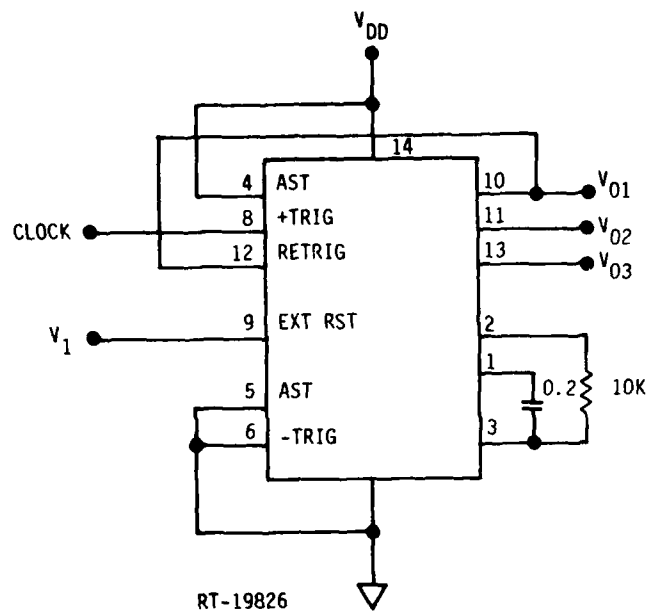


Figure 1. Electrical hook-up for latch-up screening of CD4047A

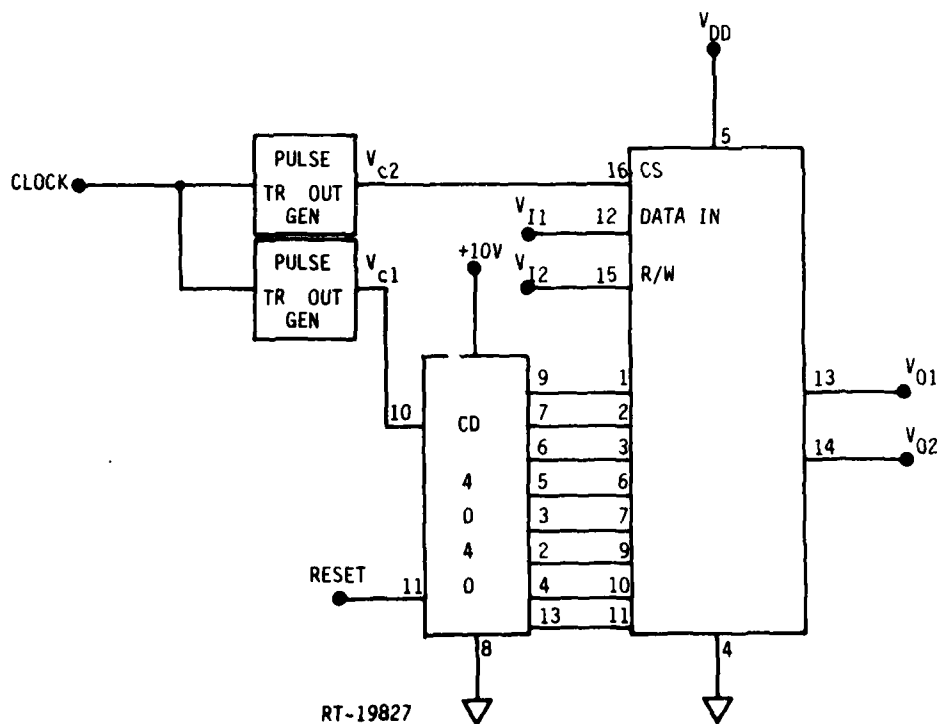


Figure 2. Electrical hook-up for latch-up screening of CD4061A

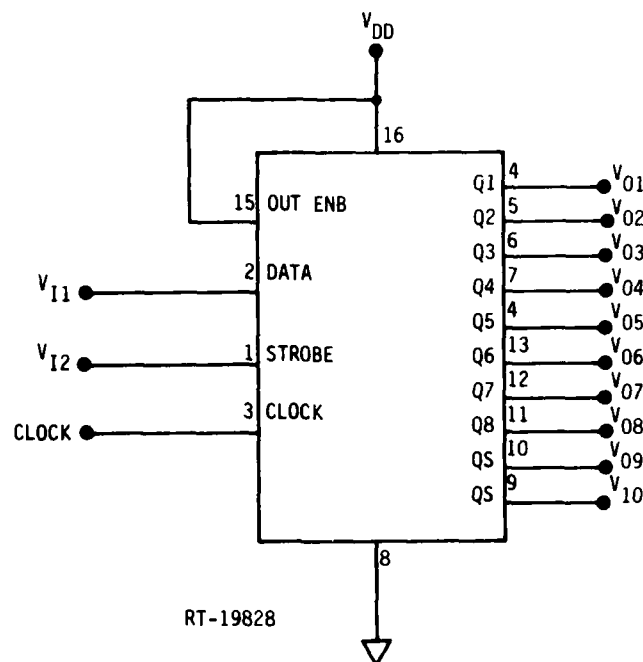


Figure 3. Electrical hook-up for latch-up screening of CD4094B

pulse at 4.6×10^{10} with V_{01} low did not result in latchup. S/N 5 also appeared normal, but time did not permit an extensive investigation of all units. Data from S/N 2, 3, and 4 are presented in Table 1.

Because of time constraints no extensive measurements were made on the CD4061 units which also demonstrated this latchup window effect. The spot check data which were taken to demonstrate the effect are presented in Table 2. Again, as can be seen from these data, not all units respond in the same manner, but S/N 4 is the only unit which did not display evidence of a latchup window.

The latchup window effect also observed in the CD4047, however, no data were recorded on these devices other than the data specifically required for the tests being performed.

It should be noted that it is entirely possible that this effect is present in other devices tested in this program but that it was not observed. As there was no known reason to irradiate units at a level above latchup threshold, and as one of the goals of the test program was to minimize the total dose delivered to the test samples, it is only by a fluke that this window was observed. After it was seen in the CD4094, spot checks were made at higher levels in those types showing latchup. However, it was not

Table 1. CD 4094 Latchup Window Data Obtained Prior to Present Program

S/N 2			S/N 3			S/N 4		
V ₀₁ -LO		V ₀₁ -HI	V ₀₁ -LO		V ₀₁ -HI	V ₀₁ -LO		V ₀₁ -HI
Dose Rate	Latchup	Dose Rate	Dose Rate	Latchup	Dose Rate	Dose Rate	Latchup	Dose Rate
6.6 x 10 ⁸	No	6.8 x 10 ⁸	4.0 x 10 ⁹	No	4.6 x 10 ⁹	1.77 x 10 ⁹	No	2.4 x 10 ⁹
7.9	→	7.7	5.1	→	5.1	2.24	→	3.2
4.6 x 10 ⁹	Yes	7.2 x 10 ⁹	5.5	Yes	5.2	2.36	Yes	4.3
5.5	→	7.3	7.3	→	5.4	3.5	→	5.2
6.5	→	8.4	8.7	→	5.8	3.9	→	5.4
8.7	→	9.1	9.9	→	6.3	5.0	→	5.8
1.12 x 10 ¹⁰	→	1.17 x 10 ¹⁰	1.13 x 10 ¹⁰	→	6.7	8.5	→	7.2
1.37	→	1.39	1.20	→	8.5	1.31 x 10 ¹⁰	→	9.1
2.0	→	1.95	1.32	→	9.4	2.5	→	1.20 x 10 ¹⁰
2.6	→	2.5	1.43	→	9.9	3.2	→	1.58
2.9	→	3.6	2.5	No	1.13 x 10 ¹⁰	4.1	→	2.3
3.2	→	4.3	3.3	→	1.18	4.6	No	2.8
3.9	→	4.6	4.6	→	1.39	→	→	3.0
4.6	→	→	→	→	1.78	→	→	3.7
	→	→	→	→	2.2	→	→	4.3
	→	→	→	→	3.9	→	→	→
	→	→	→	→	4.6	→	→	→

Table 2. CD 4061 Latchup Window Data Obtained Prior to Present Program

S/N	V ₀₁	Low Level Nonlatch Dose Rate	Low Level Latch Dose Rate	High Level Nonlatch Dose Rate
1	LO	5.04×10^8	5.67×10^8	8.0×10^8
1	HI	3.15×10^8 3.57×10^8	3.78×10^8 5.04×10^8	1.03×10^9 2.02×10^9 1.08×10^{10}
2	LO	3.57×10^8 4.20×10^8	4.62×10^8	3.68×10^9
2	HI	3.57×10^8	4.41×10^8 5.04×10^8	2.52×10^9
3	LO	2.94×10^8 3.99×10^8	5.04×10^8	2.33×10^9
3	HI	3.15×10^8	4.41×10^8	2.73×10^9
4	LO	DID NOT LATCH		3.30×10^{10}
4	HI	1.68×10^8 2.31×10^8	2.94×10^8 2.71×10^9 3.30×10^{10}	
5	LO	DID NOT LATCH		3.68×10^{10}
5	HI	1.68×10^8	2.94×10^8 3.99×10^8	1.70×10^9

feasible to cover the whole dose rate range in fine enough steps to preclude missing a narrow latchup window if one exists in any of the other part types.

3. ELECTRON SCREENING

A total of 134 devices, all manufactured by RCA, were subjected to the standard latch-up screening procedure described in Section 2 using the IRT Linac to provide a 65 ns pulse of ionizing radiation. Special care was taken to determine if a latch-up window was present. Table 3 lists the devices, their source, and the numbers in which latch-up and a latch-up window were seen. The devices obtained from Sandia National Laboratories were provided through the courtesy of Mr. Paul Gammill and were from the same production line as those units in which the latch-up window was originally seen. All of these devices were in metal-lidded ceramic packages except the CD4094B, P1-P9, which were in plastic packages.

Table 3. Devices Subjected to Latchup Screening

Type	Number	Source	Number Latching	Number with Latch-Up Window
CD4047A	25 (C1-C25)	Commerical Purchase	7	0
	25 (S1-S25)	Sandia	18	0
CD4061A	25 (S1-S25)	Sandia	25	4
CD4094B	25 (C1-C25)	Commercial Purchase	0	0
	9 (P1-P9)	IRT Stores	6	6
	25 (S1-S25)	Sandia	7	6

The device circuit configurations used for the electron-induced latch-up testing (and subsequently for the laser induced latch-up testing) are shown in Figures 1 through 3. Table 4 shows the results of the electron-induced latch-up screening. Devices not shown in this table did not latch up.

4. LATCH-UP PATH ANALYSIS

As indicated in the introduction, overlay sets, functional or schematic diagrams and chip photographs were obtained from RCA with the help of Mr. Eugene Reiss. This material, which is RCA proprietary, was obtained on a confidential basis and consequently none of it can be reproduced here. Hence, in some cases it is necessary that we discuss the latch-up analysis in somewhat general terms.

The complete latch-up analysis procedure of Crowley and Stultz (Ref 3) has been carried out for the CD4047A and the CD4094B and a partial analysis was carried out for the CD4061A. This procedure proved to be straightforward, although somewhat tedious. Primarily, limitations of time and funds precluded the complete analysis for the CD4061A. This analysis did however proceed considerably slower than that for the other two devices since the available mask-set was reproduced on a smaller scale and was very difficult to see.

As a minor addition to the Crowley and Stultz procedure, useful for CMOS devices, it was found helpful to generate a modified schematic with all gates and

³J. L. Crowley, F. A. Junga, and T. J. Stultz, "Technique for Selection of Transient Radiation-Hard Junction Isolated Integrated Circuits," IEEE Trans. Nucl. Sci. NS-23, 1703, (1976) and subsequent unpublished work of Crowley and Stultz. The analysis procedure is summarized in Appendix A.

Table 4. Summary of High Energy Electron Latchup Behavior (65 ns Pulse).*

Device Number	V _I (Pin 9)	Latch Threshold** [rad(Si)]	Device Number	V _I (Pin 9)	Latch Threshold** [rad(Si)]
<u>CD4047A</u>			<u>CD4047A</u>		
C3	V _{DD} Gnd	210 - 225 165 - 240	S10	V _{DD} Gnd	170 - 180 150 - 185
C4	V _{DD} Gnd	280 - 320 No latch	S12	V _{DD} Gnd	165 - 200 150 - 170
C10	V _{DD} Gnd	180 - 210 200 - 235	S13	V _{DD} Gnd	170 - 200 120 - 165
C17	V _{DD} Gnd	220 - 240 205 - 225	S14	V _{DD} Gnd	185 - 210 170 - 215
C18	V _{DD} Gnd	215 - 245 195 - 215	S16	V _{DD} Gnd	170 - 195 140 - 180
C22	V _{DD} Gnd	190 - 195 150 - 155	S17	V _{DD} Gnd	225 - 245 150 - 185
C24	V _{DD} Gnd	200 - 215 155 - 180	S18	V _{DD} Gnd	215 - 270 200 - 230
S1	V _{DD} Gnd	125 - 225 155 - 185	S19	V _{DD} Gnd	210 - 245 195 - 230
S2	V _{DD} Gnd	165 - 230 150 - 180	S20	V _{DD} Gnd	200 - 215 140 - 180
S3	V _{DD} Gnd	180 - 210 105 - 150	S22	V _{DD} Gnd	200 - 245 170 - 200
S5	V _{DD} Gnd	170 - 200 135 - 170	S23	V _{DD} Gnd	195 - 210 170 - 195
S6	V _{DD} Gnd	180 - 210 150 - 170	S24	V _{DD} Gnd	210 - 245 140 - 170
S8	V _{DD} Gnd	195 - 215 125 - 170			

* For most of the thresholds two doses are indicated. At the first the threshold was not reached; at the second it was exceeded, i.e., these numbers bracket the threshold and indicate the accuracy to which it is known.

** Rounded to nearest 5 rads

Table 4. Summary of High Energy Electron Latchup Behavior (65 ns Pulse).*
(Continued)

Device Number	V ₁₁ (Pin 12)	Latch Threshold [rad(Si)]**	Nonlatch Threshold [rad(Si)]**	Device Number	V ₁₁ (Pin 12)	Latch Threshold [rad(Si)]**	Nonlatch Threshold [rad(Si)]**
CD4061A (V ₁₂ is at GND in all Cases)				CD4061A (V ₁₂ is at GND in all Cases)			
S1	V _{DD} Gnd	9 - 11 10 - 11		S14	V _{DD} Gnd	8 - 10 10 - 11	
S2	V _{DD} Gnd	9 - 10 Not tested		S15	V _{DD} Gnd	9 - 12 10	
S3	V _{DD} Gnd	10 - 11 13 - 14	25 - 28 25 - 26	S16	V _{DD} Gnd	10 10 - 11	
S4	V _{DD} Gnd	9 - 10 10		S17	V _{DD} Gnd	8 - 10 10 - 12	
S5	V _{DD} Gnd	8 - 10 10		S18	V _{DD} Gnd	10 - 11 10 - 12	
S6	V _{DD} Gnd	12 - 13 12 - 15	20 - 27	S19	V _{DD} Gnd	10 - 12 10 - 12	
S7	V _{DD} Gnd	9 - 11 10 - 13		S20	V _{DD} Gnd	10 - 11 9 - 11	
S8	V _{DD} Gnd	10 - 12 10 - 11		S21	V _{DD} Gnd	9 - 10 10	
S9	V _{DD} Gnd	8 9 - 10		S22	V _{DD} Gnd	10 - 11 8 - 11	
S10	V _{DD} Gnd	11 - 13 10 - 11		S23	V _{DD} Gnd	12 - 16 Not tested	31 - 34
S11	V _{DD} Gnd	12 - 14 Not tested	31 - 38	S24	V _{DD} Gnd	10 - 12 11 - 13	
S12	V _{DD} Gnd	8 - 11 Not tested		S25	V _{DD} Gnd	10 10 - 15	
S13	V _{DD} Gnd	7 - 10 10 - 13					

*For most of the thresholds two doses are indicated. At the first the threshold was not reached; at the second it was exceeded, i.e., these numbers bracket the threshold and indicate the accuracy to which it is known.

**Rounded to nearest rad.

Note: Not shown in these data is that devices exhibiting a latch-up window sometimes again latched at dose above the window.

Table 4. Summary of High Energy Electron Latchup Behavior (65 ns Pulse).*
(Continued)

Device Number	Latch Threshold [rad(Si)]**	Nonlatch Threshold [rad(Si)]**
CD4094B (V_{I1} (Pin 1) and V_{I2} (Pin 1) are at Gnd. No devices latched with V_{I1} at V_{DD})		
P1	110 - 120	135 - 155
P2	140 - 145	160
P3	340 - 370	395 - 410
P4	300	720 - 740
P5	135 - 150	1200 - 1250
P9	245 - 265	720 - 745
S3	330 - 380	380 - 440
S10	335 - 350	350 - 390
S16	320 - 375	440
S18	300 - 345	465 - 500
S19	320 - 360	505 - 560
S21	320 - 375	575 - 650
S23	350 - 360	360 - 420
S24	345 - 375	490 - 550

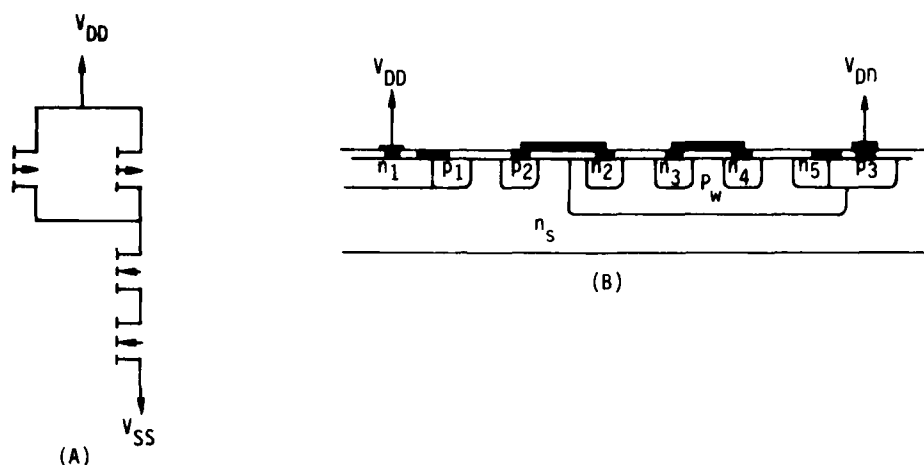
*For most of the thresholds two doses are indicated. At the first the threshold was not reached; at the second it was exceeded, i.e., these numbers bracket the threshold and indicate the accuracy to which it is known.

** Rounded to nearest 5 rads

associated circuitry removed. This considerably simplifies the search for four layer paths, and in many cases isolates various structures from one another, except for their interconnection through the substrate and/or the p-wells. From the modified schematic, various classes of circuit configurations, many of which are repetitive, can be identified.

A straightforward procedure which assures that all four layer paths are considered was given by Leavy and Scott (Ref 4) in a document which was evidently a precursor to Reference 3 but which followed Crowley and Stultz' earlier work. For each circuit type or region a cross-sectional view is drawn and each p and n region is identified. Figure 4 illustrates such a diagram. We have modified Leavy and Scott's procedure to the extent that the n substrate and p-well regions are labeled n_s and p_w rather than with a numerical subscript as used for the other regions. This serves as a reminder that

⁴J. F. Leavy and L. Scott, unpublished. The procedure is summarized in Appendix D.



**Figure 4. (a) Representative circuit element (drawn without gates)
(b) Cross-sectional view of (a) with elements labeled
for analysis**

interconnection can exist between different circuit types through these regions. Next, following Leavy and Scott we generate a list containing each p -region and all n -regions contiguous with each. Next, again in a systematic way, all possible pnpn paths are enumerated and finally each such path is examined to see if all of the junctions can simultaneously be forward biased. Those that can form the class of potentially latchable paths.

4.1 CD4047A. Monostable/Astable Multivibrator

For this device, in addition to the mask set and the chip photograph, a detailed schematic was available. During the course of identification of each of the devices from the schematic on the mask set, several minor errors in the schematic were identified, consisting primarily of an interchange of gate connections on a number of pairs of devices. While none of these would effect the normal operation of the device or its latch-up behavior, they proved to be extremely troublesome and time consuming to sort out. Less of a problem was the discovery of two nonoperative devices on the chip, which did not appear on the schematic.

The only potentially latchable pnpn paths found in this device included the n -substrate, which is electrically connected to pin 14, V_{DD} (positive bias), as the first n element, and one of the p -wells, which are electrically connected to pin 7, V_{SS}

(ground), as the second p-element. This path is latchable only if inputs or outputs are biased outside of the range of V_{DD} to V_{SS} or if a voltage drop occurs across the substrate or p-well region during operation. The former situation was not true during testing nor would it be true under normal operation; the latter requirement is a possibility.

The only latchable path found in the CD4047A is illustrated in Figure 5. The input at positive bias (see Figure 1) is pin 4, ASTABLE. Grounded inputs are pins 5, 6, and 8; ASTABLE, -TRIGGER, and +TRIGGER. In addition, pin 9, EXTERNAL RESET, can be at either positive bias or grounded as shown in Table 4. For each of these inputs the structure shown, which may participate in the latch-up, is part of the input protection circuitry. The most likely path to latch is pin 4 to pin 5 since junctions (A) and (C) are physically close together. In addition, with pin 9 positive, the pin 9 to pin 8 path also has (A) and (C) relatively close.

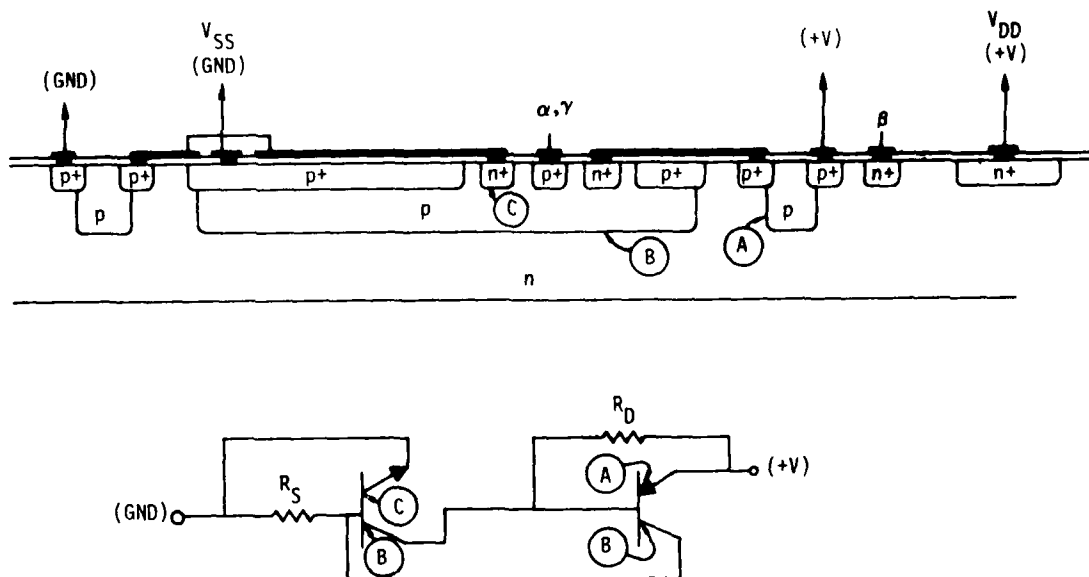


Figure 5. Latchable path involving input protection circuitry, n-substrate and p-well

Also shown in Figure 5 is a schematic diagram of the latchable path, again with the junctions identified. Here the points labeled (B) are both part of the same junction. This diagram also illustrates that for junctions (A) and (C) to be forward biased a voltage drop must occur in R_S and R_D respectively; that is, in the substrate

from V_{DD} to (A) and in the p-well from (C) to V_{SS} . If these resistances are too small or if insufficient current flows, this voltage drop may not be sufficient. Since the pin 8 connection to n+ is physically very close to the V_{SS} connection to the p-well, the pin 9-pin 8 path described above may not be latchable.

4.2 CD4061A (256-Word by 1-Bit Static RAM)

As indicated above, only a partial analysis of the CD4061A has been carried out. This analysis has shown the existence of a number of potentially latchable paths based on input protection circuitry and entirely analogous to those described for the CD4047A. What has not been shown is whether or not any other types of paths may exist in this device. If the same sort of design rules have been used in this device as in the CD4047A (and the CD4094B, to be discussed below) it is probable that other paths do not exist. This however has not been shown.

The complete analysis of this device will require generation of a schematic diagram since none is available.

4.3 CD4094B (8-Stage Shift-and-Store Bus Register)

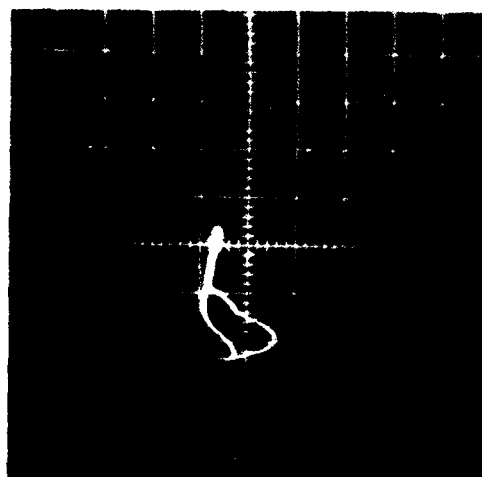
A complete analysis has been carried out for the CD4094B. As part of this analysis, schematic diagrams of the various functions of the device were prepared to complement the functional diagram which was obtained along with the mask-set. In this device modular circuit functions are repeated multiple times. Hence, in addition to the detailed and functional diagrams, an interconnect list was prepared showing the specific connecting paths of the various circuit modules.

The only potentially latchable paths, again assuming that all input potentials are between V_{SS} and V_{DD} , are similar to those identified in the CD4047A shown in Figure 5, and involve the input protection circuitry. Pin 15, OUTPUT ENABLE, is the only pin held at V_{DD} . Pins 1, STROBE; 2, DATA; and 3, CLOCK are all held at ground and hence are possible negative ends of latchable paths. However, as seen in Table 4, latching only occurs if pin 1 is at V_{SS} . Hence, apparently only pin 1 can serve as the negative end of the path. This is reasonable since the structures associated with pins 1 and 15 are adjacent on the chip.

5. EXPERIMENTAL STUDIES

5.1 Latchable-Path Verification

In order to verify that the paths identified in the mask set analysis were indeed capable of latchup, the I-V characteristics of these paths were measured using a Tektronix 575 Transistor Curve Tracer. Figure 6 shows the curve tracer output for the path from pin 4 to pin 5 of a CD4047A, with all other pins floating. A typical latching characteristic is seen with fold-back of voltage at a given current. For this device, as shown, the increasing current trace goes to a higher voltage before fold-back, while the decreasing current trace drops to a lower value before this happens. Not all paths or devices behave in exactly this same way as can be seen in Figure 7, the I-V characteristic for CD4094B, S1 taken between pins 15 and 3. In this case, one trace does not show fold-back. The exact shape of the curves also depends on the dynamics of the curve tracer sweep. (The voltage sweep in the curve tracer used here is a half sine wave with a repeat time of approximately 8 ms.) For the CD4047A shown in Figure 6, the initial breakover point occurred as the amplitude of the voltage sweep was increased to approximately 2.5 V; subsequently it dropped back to the lower value shown in the figure. For the CD4094A the sweep had to go to ~ 3 V initially to obtain the latching characteristic.



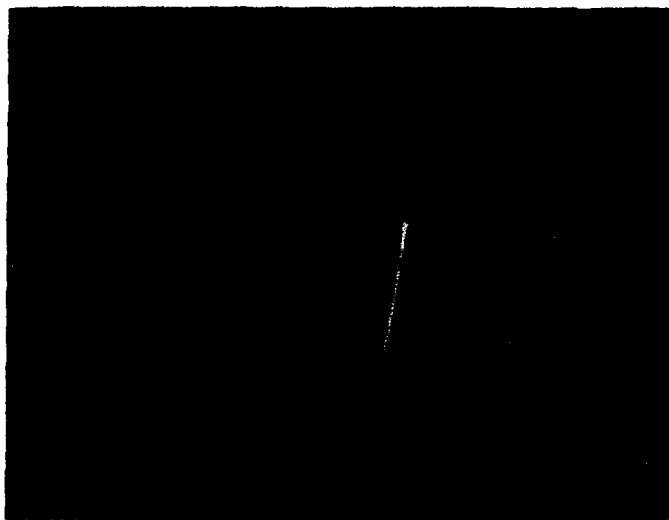
HORIZONTAL: VOLTAGE SWEEP, 0.5 V/div.

VERTICAL: CURRENT 0.05 mA/div.

SERIES RESISTOR: 100 k Ω

Figure 6. I-V characteristics of path Pin 4-Pin 5 for CD4047A, No. C3.

It must be emphasized that the only purpose of this test was to verify that the paths, identified in the analysis of the mask set as being capable of latching under suitable bias conditions, can indeed show a latching behavior. No attempt was made



HORIZONTAL: VOLTAGE SWEEP 0.2 V/div
 VERTICAL: CURRENT 0.02 mA/div
 SERIES RESISTOR: 100 k Ω

Figure 7. I-V characteristic showing potentially latchable path between pins 15 and 3 in CD4094B, S16.

during these tests to duplicate the biases used under normal operation since by definition a latch-up induced by over-voltage stress occurs under *other than normal* conditions. Hence the magnitude of the voltages which characterize the latching characteristic in this test are of no significance; all that has been learned is that a latch-up can occur under some bias conditions. Indeed this is the reason why some paths, which are seen to latch under over-voltage stress, do not latch in normal operation, with operating biases.

Latch-up induced by over-voltage stress was seen between most of the inputs of the CD4061A as well except that the magnitude of the overshoot voltage was small, typically <0.1 V. One important difference with the CD4061A was that a latchable characteristic was seen between pins 5 (anode) and 4 (cathode), i.e., between V_{DD} and V_{SS} . Figure 8 illustrates this characteristic for CD4061A, S7. Such a characteristic was not seen between V_{DD} and V_{SS} for either the CD4047A or the CD4094B. This would seem to imply that another potentially latchable path exists in the CD4061 not involving the input connections. It is unfortunate that time did not permit a complete analysis of the CD4061 mask set to verify the existence of this other path.*

* Indirect evidence for the existence of a different type of path is given by the observation, Table 4, that in the CD4061A's showing a latch-up window, relatch occurred at still higher dose rates. Since it seems likely that all paths of a similar type would latch in the same range of dose rates, this suggests two types of paths.



HORIZONTAL: VOLTAGE SWEEP 0.2 V/div
 VERTICAL: CURRENT 0.02 mA/div
 SERIES RESISTOR: 100 k Ω

Figure 8. I-V characteristic in CD4061A, S7 between V_{DD} and V_{SS}

It is important to recognize that while observation of I-V characteristics of the form shown in Figures 6 through 8 are necessary for latchable paths, they are not sufficient to show that latching will occur under normal operation, since it is also necessary that the proper forward bias on each of the three junctions be present as well. This is assured in the curve tracer measurements since the latch-up is induced by over-voltage stress. The bias across the entire path is increased until each junction is sufficiently forward biased to inject carriers into the adjacent one.

5.2 LASER EXCITATION OF DEVICES

As indicated above, the output from a laser diode was used to irradiate portions of the chip to induce latch-up. It is instructive to compare the carrier generation rate from a laser pulse with that due to high energy electrons.

With 1.38 eV photons (9000 Å emission from a GaAs laser diode) a 1 W, 100 ns pulse will generate 4.53×10^{11} hole-electron pairs. If this pulse is incident on an area of 10^{-2} cm^2 , and if we assume an optical attenuation coefficient of 500 cm^{-2} at this wavelength, 2.25×10^{16} carriers/cm³ will be generated. For high energy electron generation in silicon 3.65 eV will produce one carrier pair. Hence 1 rad(Si) generates 4.0×10^{13} carrier pairs/cm³. Therefore, under these conditions, 1 W (or 100 W/cm^2) of laser light is equivalent to 567 rads of high energy electrons.

If the lifetime of the generated carriers is short compared to the pulse width, dose rate rather than dose is the proper unit for comparison. Since the high energy electron pulse used in the latch-up screening was 65 ns and the optical pulse was 100 ns, the high energy electron dose rate equivalent to the optical pulse generation rate is less: 100 W/cm^2 in a 100 ns pulse corresponds to a 65 ns, 368 rad(Si) electron pulse.

5.2.1 Experimental Set Up

The de-lidded chips were mounted for testing in a standard socket, either DIP or flat pack, which was held on an xy translation stage under a stereo microscope. A micromanipulator probe was provided for determining voltage on various metallization points on the chip.

Either an LD-65 or an LD-67 laser diode obtained from Laser Diode Laboratories, Inc. was used as an ionizing source. Two different optical systems were used for illumination of the chips with pulsed laser light. In the first system, a parallel beam of light was directed with a suitable mirror down one of the eyepiece tubes of the microscope. Optical alignment was extremely critical to obtain maximum optical flux at the image position, and was apparently associated with difficulties in directing all of the light through the various aperture stops in the optical path of the microscope. This technique provided an extremely small optical image and consequently a high optical power density. With the microscope operating at x12 magnification, it was estimated that the image area was $8 \times 10^{-8} \text{ cm}^2$. This value was determined by measuring the optical demagnification of a visible light source and applying this value to the known emitting area of the laser diode.

In the second optical set-up the image of the laser diode was focused with a 60 mm diameter, 80 mm focal length lens onto the chip with a magnification of 4.6. The image area in this set up was 0.015 cm^2 using an LD-65 diode and 0.028 cm^2 using an LD-67. These areas were determined by mounting an 0.34 mm diameter pin hole in a 25 μm thick stainless steel sheet on the xy stage at the laser diode image and measuring the signal on a PIN diode detector under the pin hole as a function of the pin hole position. The areas given are for the half-power point dimensions. Provision was made in this setup to move the image across the chip when an external voltage probe was in contact with the chip, which would prevent motion of the xy stage. The diode was mounted on a horizontal translation fixture and a turning mirror in the optical path was provided with a rocking motion to provide image motion orthogonal to that provided by the horizontal translation of the diode.

In order to obtain a visual indication of the image location on the chip, a small, 2 W Sylvania concentrated arc lamp, Number A2P, was mounted adjacent to the laser diode. The horizontal translation stage was used to move the arc lamp to the normal position of the laser diode and its image on the chip was viewed through the stereo microscope. Verification of the coincidence of the image locations was made using the PIN diode signal from the light focused through the fixed pin hole described above.

The power incident on the sample was measured using a calibrated RCA C30809 silicon PIN photodetector. The detector was biased at 45 V and had a 4.7Ω load resistor. The output sensitivity of this circuit was 2.8 V/watt. Since it was found that the output of the PIN diode became nonlinear at about a 1 V signal, apparently due to the high flux density on a small portion of the diode, the total intensity of the image was measured with an attenuator inserted in the optical path. The attenuation of this attenuator was measured to be 35.7.

Throughout the course of the laser probing experiments, difficulties were encountered with degradation of the optical output of the laser diodes with time. Each of four diodes exhibited this behavior with the output eventually becoming too low to be of use in these experiments. Conversations with the diode manufacture did not reveal any reason associated with the manner in which the diodes were operated which would cause this relatively rapid degradation. Although not included in the published specifications, we were told that typical diodes have a 10,000 hour lifetime when operated with a 100 ns pulse at a 500 Hz rate at their maximum rated current. It was suggested to us that sometimes "bad" batches of diodes are produced. Whatever the cause of the degradation it severely limited the total amount of laser probing we were able to accomplish during this program.

5.2.2 Results of Optical Probing

IR probing has been carried out on several samples of both the CD4047A and the CD4094B. Latching behavior was observed in three samples of the CD4047A and in one sample of the CD4094B. No samples of the CD4061A were tested.

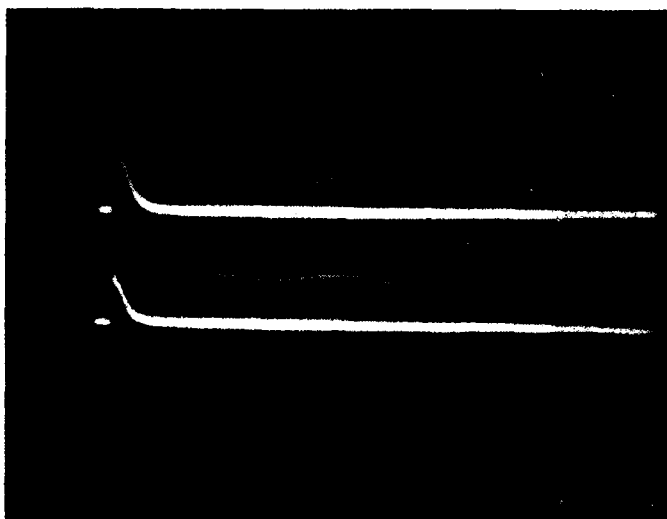
Initial latching attempts were made using the small area, high flux density illumination obtained by focusing through one eyepiece of the stereo microscope. For these experiments the flux incident on the sample was $\sim 10^{-2}$ watts giving a flux density of 1.3×10^5 watts/cm². This corresponds to a dose of 7×10^5 rad(Si). This is of course well above the measured threshold for latch-up. However no latch up was seen in any of the devices tested. We conclude that this is due to the extremely limited area

illuminated. Two effects could be in play here. First, some of the junctions in the latch-up path are extended in area and hence sufficient current might not be injected across the complete junction. Second, the three junctions in most of the paths are a considerable distance from each other and thus the entire latch-up path would not be illuminated with the finely focused beam. Either of these facts could be responsible for our failure to induce latch-up in these experiments.

Latching was induced using the lower flux density, larger-area focusing system. A series of measurements was made on CD4047A, C3 excited with 100 ns IR pulses with a total power of 1.9 W and a power density of 62 W/cm^2 . A latching behavior was induced which typically persisted for 80 to 100 μs and then self-quenched. This behavior was not entirely reproducible from shot to shot. The time to quench would, in some cases, vary and more importantly the latch would frequently not occur under apparently identical conditions. Figures 9 and 10 are oscilloscope photographs of the behavior. In Figure 9 the voltage on the p-well, in the vicinity of the n+ diffusion tied to pin 5, and the device current are shown. In Trace 2 of Figure 10 the voltage on the n-substrate near the p diffusion connected to pin 4 is shown. These traces were taken with the diode repetitively pulsed at a rate of about 500 Hz; both Trace 2 and Trace 3 have multiple sweeps showing both the latched condition and the nonlatching behavior. Comparison of the current dependence in the two figures shows some of the nonrepeatability observed. In addition, the upper trace in Figure 10, the voltage on pin 13, the oscillator output, shows that this pin was switched from low to high by the IR pulse (the oscillator was not running during these measurements).

These results show that the path identified above during the mask analysis does indeed latch. Pin 4 is the anode of this path; pin 5 is certainly one cathode. In addition, pins 6 and 8 are also tied to n+ diffusions in the same p-well and probably are also cathodes. Pin 9 is less likely to be a cathode since its n+ diffusion is farther from the others and in a separate p-well. Specific measurements were not made to check this.

Some evidence was seen for a window in this device in that the latching apparently could not be induced at a somewhat higher intensity of the IR. However, because of the rather sporadic nature of this latch and also due to the fact that the location of the light excitation on the chip was so critical to obtain latching, it was not definitely shown that an actual window was being observed. For instance, if the physical location of the light output from the laser diode were to shift slightly with diode current, the image location might also shift, causing cessation of the latching. Since none of the CD4047A's evaluated in the present study exhibited a latch-up window



SWEEP: 10 μ s/div

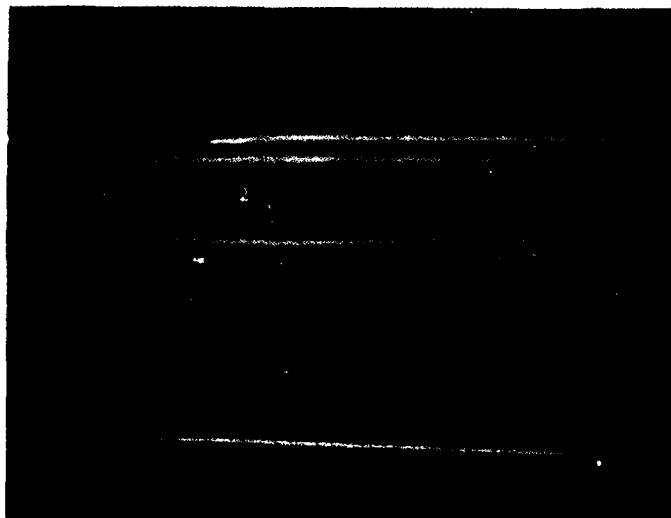
UPPER

TRACE: VOLTAGE AT POINT γ , (FIGURE 5)
IN p-WELL NEAR PIN 5 PRO-
TECTIVE CIRCUITRY
2V/div

LOWER

TRACE: I_{DD}
50 mA/div

Figure 9. Latchup in CD4047A, C3



SWEEP: 10 μ s/div

TRACE 1: VOLTAGE ON PIN 13,
OSCILLATOR OUTPUT
5V/div

TRACE 2: VOLTAGE AT POINT β
(FIGURE 5), n-SUBSTRATE
NEAR PIN 4 PROTECTIVE
CIRCUITRY
1V/div

TRACE 3: I_{DD}
50 mA/div

TRACE 4: LASER DIODE CURRENT
20 A/div

NOTES:

1. TRACES 1 AND 3 DELAYED BY APPROXIMATELY 20 μ s FOR CLARITY.
2. ALL TRACES ARE DOUBLE EXPOSURES SHOWING LATCHING AND NONLATCHING RESPONSES.

Figure 10. Latchup in CD4047B, C3

with electron excitation, it is probable that an actual window was not induced with optical excitation.

We have also measured the resistance of typical paths in the p-well and substrate to terminals 7 and 14, the contacts for V_{SS} and V_{DD} both in the dark and during a light pulse, i.e., the values of the resistors R_S and R_D in the equivalent schematic of Figure 5. Figure 11 shows the voltage and current between point α in the p-well (this



SWEEP: 0.5 μ s/div

UPPER: VOLTAGE (PIN 7 TO A)
0.5V/div

LOWER: CURRENT (PIN 7 TO A)
20 mA/div

NOTE: THE LOWER TRACE IS OFFSET FROM
THE UPPER BY APPROXIMATELY 1.5 μ s.

Figure 11. Measurement of the resistance change, due to input IR pulse, of the path between pin 7 (V_{SS}) and point α on the p-well (Figure 5)

point is geometrically farthest from the metallization contact from V_{SS} to the well) and pin 7 during IR excitation. Table 5 summarizes the resistances measured and also shows the current needed to give a 0.7 V drop. Since these currents are small compared to the total current drawn during the latch, this again tends to verify the suggested latching path.

Table 5. Latching Path Resistance Measurements in CD 4047A, C3

Path	R(Ω)		I(mA) for 0.7 V	
	Dark	Light	Dark	Light
$V_{SS}-\alpha$	274	121	2.6	5.6
$V_{SS}-\gamma$	201	88	3.5	7.9
$V_{DD}-\beta$	52	39	13.0	18.0

*(Points α and γ are in the p-well at different distances from the V_{SS} contact. Point β contacts the substrate.)

We do not have a definite explanation for the cessation of latching. As can be seen from Figures 9 and 10, however, it is due to a gradual dropoff in current such that forward bias of the junctions cease. This dropoff might be due to diffusion of carriers out of the current path of the latch. However, it is not obvious why this mechanism would occur for IR excitation and not for high-energy electron excitation, in which the latch was seen to last longer.

Two other CD4047A's were also studied. These show very similar behavior with the latch also lasting up to 100 μ s. One of these was even more sporadic and variable than C3 described above.

CD4049B, S16 was tested with an IR pulse intensity of up to 5.8 W or 199 W/cm². In this device a definite latch was seen lasting almost 100 ms. Figure 12 shows the current, the voltage on the p-well and an output voltage as a function of time. The current was measured with a Tektronix current probe with a time constant of 1.3 ms. Hence, the actual time dependence of the current is not seen, only the values at the beginning and end of latch. Initially the current is $\sim$ 500 mA and decays to $\sim$ 200 mA at the end of latch. As this current decreases the voltage on the p-well also decays and when it reaches $\sim$ 0.7 V the latch condition terminates since the p-well/n junction can no longer be forward biased. There are three possible n-diffusions which can form this junction with the p-well. They are associated with the protection circuitry for pins 1, 2, and 3, all of which were at ground during these tests.

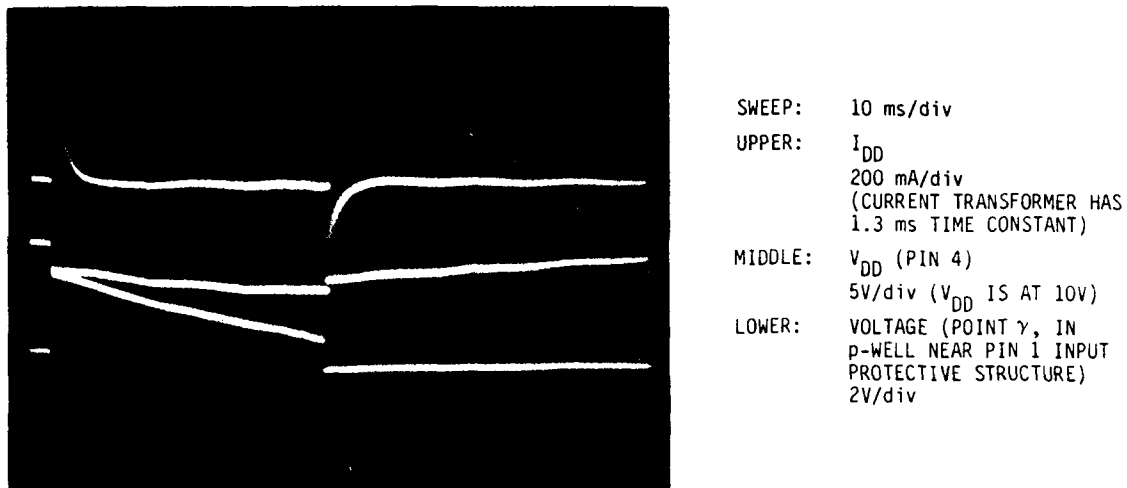
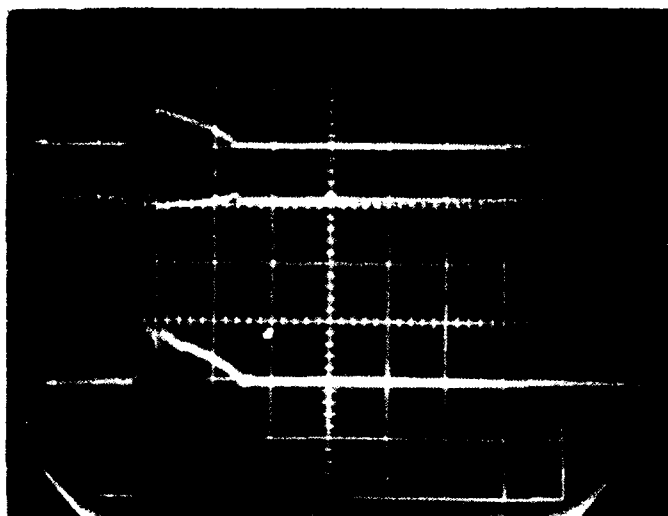


Figure 12. Latchup in CD4094B, S16

A puzzling observation was made regarding identification of the anode region of the latchup path. The bias on the n-substrate near pin 15, which was identified during the mask analysis as the only possible anode, was measured during latch and was not sufficient to allow forward bias of that diode. This may have been an artifact of the measurement since no metallization was available for probing in the immediate vicinity of the p-diffusion connected to pin 15. Hence the actual junction potential might have been appreciably different from that measured on the metallization. Some evidence for this is given by measurements of this potential in two other devices S19 and S21 which,

although not latching, did show a sufficient voltage swing at this point. This is illustrated in Figure 13. With a different current pattern occurring in the absence of latch-up it is possible that the somewhat remote probing point could measure more accurately the junction voltage in this case. In any event these measurements do show that, at least under some circumstances, the bias between the substrate and the p-diffusion connected to pin 15 can be sufficient to forward bias that diode.



SWEEP: 1 μ s/div
 UPPER: I_{DD} 400 mA/div
 MIDDLE: VOLTAGE ON PIN 2, 5 V/div
 LOWER: VOLTAGE AT POINT β , AN n-SUBSTRATE NEAR PIN 15

Figure 13. Response of CD4094B, S21 to IR pulse

The intention to probe various locations on the chip in an attempt to identify the front half of the latching path were thwarted when the chip burned out during a latch. This occurred when the value of the current limiting on the power supply was increased. The dropoff on pin 4 during latch, as seen in Figure 12, was found to be due to a corresponding decrease in supply voltage. (To preclude a repetition of this accident a circuit was subsequently implemented to turn off the supply voltage after 5 ms. Earlier implementation of this circuit would, however, have prevented the observation that the latch was terminated by the p-well voltage falling below 0.7 V.)

As mentioned above, two other CD4094B's, Nos. S19 and S21, were studied under conditions similar to those under which S16 latched. Latching was not induced in either of these samples. Although peak current reached ~ 400 mA, it decayed within ~ 2 μ s or less. It should be noted that latching was induced in S16 only with the light on the chip positioned very carefully. Indeed, minor changes in mechanical alignment of the optical system, due, for instance, to accidentally bumping the table, would cause the latch to

be lost. Slight readjustment of the optical alignment would restore it. Consequently, it may be that the proper optical alignment was never achieved with S19 and S21, although a careful search was made in both. It should be mentioned that all three devices latched at almost identical electron doses in the Linac screening of these devices.

6. LATCH-UP WINDOW MODEL

Although we have failed to induce a latch-up window in any of the devices when excited with infrared, the analysis and the experimental measurements have suggested a possible mechanism for creation of the window, i.e., for suppression of latch-up at doses above a range in which latch-up did occur. Unfortunately, since this region could not be reached through excitation with the optical fluxes available, a direct experimental test of the proposed mechanism has not been possible. There are however some experimental results, which we will discuss below, which provide circumstantial evidence for the mechanism.

As previously discussed the only latchable paths present in either the CD4047A and the CD4094A include the n-substrate and the p-well as the second and third elements in the four-layer latchable path. Since these regions are also the contact regions for the positive and negative biases, V_{DD} and V_{SS} , it is necessary that voltage drops occur across both of these regions between voltage input points and the first and third junctions, respectively, in the latchable path. These occur across the resistors R_D and R_S in Figure 5. The values of the resistance of each of these elements depends of course on the resistivity of the n-substrate and the diffused p-well and on the geometry of the device. The values of these resistances, both with the chip in the dark and illuminated with an IR pulse with power density of 62 W/cm^2 , were shown in Table 3. The important observation is that these resistances are sufficiently high that a moderate current provides the voltage drop needed to allow forward bias of the junction. The mechanism proposed which would prevent latch-up at high doses for paths of this type is based on the fact that R_S and R_D become smaller at higher dose rates, as more carriers are photogenerated. At some dose rate there is insufficient current through these resistors to allow forward bias of the appropriate junctions and latch-up is not possible. Unfortunately the fraction of the total latch current which flowed through R_S or R_D was not measured. If this had been done it would be possible to estimate the incident flux above which latch-up would not occur and that of the latch-up threshold.

Indirect evidence for the proposed latch-up inhibition mechanism is given in measurement of the resistivity of a section of the p-well under optical excitation in a CD4047A (C5) which was shown under Linac irradiation not to latch up. One path, $V_{SS} - \alpha$, was seen to be much more photosensitive in C5 than the equivalent path in device C3 which did latch and for which the resistance data were shown in Table 3. For C3 (latchable) the resistance of this path while illuminated was 121Ω while for C5 (nonlatchable) it was 36Ω . The dark resistance of the paths were similar, 274Ω and 248Ω , respectively. In addition the photo resistance in device C3 was measured after the output of the laser diode had begun to degrade. The power was not specifically measured at the time C5 was tested, but it was probably a factor of two lower than its value when C3 was measured. The photo resistances for $V_{SS} - \gamma$ and $V_{DD} - \beta$ were similar in the two devices. The fact that one path in the p-well was much more sensitive in one device while another path in the same well was similar in the two devices indicates a considerable nonuniformity in the p-well diffusion in C5. Evidently the carrier lifetime in a part of this well in C5 was appreciably longer than in C3, although this was not measured. These observations point out that an increase in photoconductivity in a part of the sample, forming in this case R_S , can inhibit latch-up. This is the opposite of the current fixes for latchup which are now used. Gold doping or neutron irradiation kill lifetime and are used to reduce gains so as to stop latchup.

A second piece of indirect evidence for the validity of the proposed mechanism is shown in data such as that of Figure 12. Here we see, in the lower trace, that when the bias voltage between V_{SS} and the p-well in the vicinity of one of the junctions participating in the latch process drops below ~ 0.7 V as the total current drops off, the latch-up is terminated. We do not have a definitive explanation of why the total current is dropping off in this device. Possibly heating of the device is occurring, changing the regions in which current flows, or possibly simply carrier diffusion out of the latching region is taking place. Either could cause the observation of Figure 12.

An alternate explanation of a possible reason for inhibition of latch-up at higher doses should also be mentioned, although we have made no measurements to investigate the validity of this possibility. At higher doses the increased carrier densities could cause a change in the gain of the two interconnected transistors forming the latch-up path. This could cause a reduction in the loop gain which sustains the latching. No attempts were made to measure these gains in the present program. While such measurements would probably be possible if suitable metallization points for probing were available, these measurements would require breaking of various metallization paths and should be the last measurements planned to be made on a chip.

7. SUMMARY AND CONCLUSIONS

In this study a number of important accomplishments have been achieved:

1. Mask sets have been analyzed completely for two CMOS devices, CD4047A and CD4094B, and potentially latchable paths have been identified which involve input protection devices and which include portions of the n-substrate and the p-well in the path. A partial analysis has been carried out for the CD4061A and similar paths have been shown to exist in this device.
2. It has been demonstrated that latch-up can be induced in de-lidded devices with IR radiation from a pulsed laser diode source. Two advantages of this type of excitation over high energy electron irradiation for study purposes are (a) selected areas of the chip can be irradiated to aid in determination of the region responsible for latch-up, and (b) voltage probing can be carried out relatively easily during irradiation to further evaluate latch-up path mechanisms.
3. A possible mechanism for creation of a latch-up window involving the increase of photoconductivity of the substrate and p-well with increasing dose rate has been proposed. Some indirect evidence for the validity of this model has been found.
4. The possibility of the existence of a different type of latchable path in the CD4061A has been indicated from I-V measurements.

Complete identification and verification of the mechanism responsible for the latch-up window has not been accomplished in the present program. The primary reason for this was the inability to induce a window in any device with laser excitation. Evidently a sufficiently high optical flux was not available from the laser diodes used in spite of the fact that comparison of carrier generation rates with IR to those of high energy electron doses which did induce a window would indicate the contrary. The highest optical flux obtained over a large area was 199 W/cm^2 in a 100 ns pulse corresponding to 1126 rads. This should have been more than sufficient (by about a factor of three) to produce the latch-up window in the devices tested. While there may be some errors in the assumptions used for comparison of generation rates by high energy electrons and by IR, or in the calibration factors used in determining the doses of either of the ionizing radiations, it is unlikely that they would amount to a large factor. More likely, shielding of the optical radiation by the metallization, which was

recognized as a potential problem at the outset of this program, requires use of a higher flux of IR to produce a given effect than would be calculated from a simple comparison of carrier generation rates. It is also quite probable that larger areas of the chip must be covered by the incident IR pulse. Whatever the cause it is clear that future measurements must be made with a higher power laser as the optical source. Although the highest powered, commercially available single diode sources were used here (these diodes were rated at 20 W peak output and one sample reached 30 W), diode arrays are available which have reasonable drive current requirements and which have power outputs up to several hundred watts. Since it has been found in this program that areas up to several square millimeters should be illuminated, the output area of these arrays would not be a problem.

With the higher-power broader-area illumination it should be possible to observe the latchup window and, with suitable voltage probing under various levels of illumination, the proposed window mechanism could be investigated and parameters on the photoresponse of the substrate and well could be determined which would explain the window effect. Future work in this area should use a high powered laser diode array.

The second major area for investigation of the latch-up window effect would be completion of the analysis and experimental testing of the CD4061A. As indicated above, this device may contain another different type of latchable path, other than that associated with the input protection circuitry. After identification of this path (or paths) from the mask set analysis, experimental measurements should be made to determine if it can sustain window action. These studies would serve to determine if a different mechanism for window formation were possible.

TASK II: STANDARDS SUPPORT (J. Harrity)

1. INTRODUCTION

In the area of standards support IRT represents DNA in the ASTM subcommittee F1.11 and E10.07 and the Space Parts Working Group Hardness Assurance Committee. Planned participation in a newly formed subcommittee on radiation effects on LSI devices of the Space Parts Working Group Committee on Large Scale Integrated (LSI) Circuits did not materialize as the organizers decided that there was not yet enough expertise in the area for meaningful standards to be prepared.

2. ASTM SUBCOMMITTEE E10.07

Dr. Norman Lurie attended meetings of this subcommittee in New Orleans, Louisiana in January and in Ithaca, New York in July. He participated in discussions covering several different standards on dosimetry worked on by this committee with special emphasis on shepherding the three neutron dosimetry standards, originally developed at IRT under DNA auspices, through final review, balloting, and acceptance. These three standards, E720, E721 and E722, are now bona fide ASTM standards published in Part 45 of the ASTM Book of Standards.

Dr. Lurie feels that the directions this subcommittee is taking in the development of dosimetry standards are drifting out of his particular area of expertise. In addition, his work at IRT is moving into different areas of experience, so he feels that IRT and DNA would be better served if another of IRT's scientists were to represent them at the E10.07 meetings. IRT will make recommendations to DNA on a suitable replacement in the near future.

3. ASTM SUBCOMMITTEE F1.11

Mr. John Harrity attended working meetings of this subcommittee at St. Petersburg, Florida in February and at Hilton Head, South Carolina in June. A third meeting is scheduled for Palo Alto, California the first week in November.

Mr. Harrity participated in reviews and discussions of many standards documents and prepared a revision to F526 dealing with calorimeters for dosimetry in linear accelerator experiments. This revision covered the use of calorimeters using thermistors as temperature sensing elements in addition to the use of thermocouples specified in the original version. He has been preparing equipment for a round-robin test of this standard and of F675 "Test for Nonequilibrium Transient Photocurrents in p-n Junctions." Plans for these two round-robin tests will be presented for subcommittee approval at the November meeting. Editing for the subcommittee has been one of Mr. Harrity's chores in the past; however during this calendar year all documents reaching a stage at which editing would normally be done have either been prepared by himself or by Bob Scace of NBS, whose close association with the committee editor and long experience with ASTM documents precludes the necessity for any editing at the subcommittee level, so no editing has been required.

4. SPACE PARTS WORKING GROUP - HARDNESS ASSURANCE COMMITTEE

This group holds meetings contiguous to those of the ASTM F1.11 subcommittee, so it too met in St. Petersburg, Florida in February and Hilton Head, South Carolina in June and will meet again the first week in November in Palo Alto, California. During this year the chairmanship of this group passed from Clyde Lane of RADC to El Wolicki of NRL. A smooth transition was experienced as Dr. Wolicki has long been active in the group and as Clyde will still continue attendance when possible, although his current duties preclude his devoting the time necessary to chair the meetings.

A document prepared by Bob Scace on dose rate testing of the response of linear integrated circuits has been reviewed and comments incorporated in new drafts. Aside from this, most of the committee effort has gone into reviewing and updating earlier drafts of two guidelines documents, "Neutron Hardness Assurance Guidelines for Semiconductor Devices" and "Hardness Assurance Guidelines for Total-Dose Radiation Effects on Electronic Piece Parts." These two documents have undergone extensive revision in both content and format during this past year, and it appears to be the general consensus that, with perhaps minor corrections, the drafts which will be reviewed at the Palo Alto meeting should complete these two important documents.

5. SUMMARY OF STANDARDS ACTIVITIES

Below is a list of activities which took place in these standards groups during the last year.

STATUS OF STANDARDS WORKED ON DURING 1980

ASTM E10.07

- | | |
|-------------|---|
| E720 | "Standard Guide for the Selection of a Set of Neutron Activation Foils for Determination of Neutron Spectra Used in Radiation-Hardness Testing of Electronics." Approved by Society. |
| E721 | "Standard Method for Determining Neutron Energy Spectra with Neutron Activation Foils for Radiation-Hardness Testing of Electronics." Approved by Society. |
| E722 | "Standard Practice for Characterizing Neutron Energy Fluence Spectra in Terms of an Equivalent Monoenergetic Neutron Fluence for Radiation-Hardness Testing of Electronics." Approved by Society. |
| E10.07-79-2 | "Standard Method for Calculation of Absorbed Dose in Materials from Neutrons by Application of Threshold-Foil Measurement Data." Approved by E10, awaiting Society ballot. |
| E10-07-80-1 | "Standard Method for Calibration of Dosimeters Against an Adiabatic Calorimeter for Use in Flash X-Ray Fields." Awaiting results of subcommittee ballot. |
| E10-07.80-2 | "Standard Method for Determining Radiation Absorbed Dose Using the Fricke Dosimeter" (A method to replace D1671) - Currently in work. |
| E10.07-80-3 | "Standard Method for Determining Radiation Absorbed Dose Using the Ferrous-Sulfate Cupric-Sulfate Dosimeter" (A method to replace D2954) - Currently in work. |
| E10.07-80-4 | "Standard Method for Determining Radiation Absorbed Dose Using the Ceric-Sulfate Dosimeter." (A method to replace D3001) - Currently in work. |
| No-No.-yet | "Exposure of Polymeric Materials to High Energy Radiation" (A method to replace or revise D1672) - Currently in work. |

ASTM F1.11

- | | |
|------|---|
| F526 | Revision "Dose Measurement for Use in Linear Accelerator Pulsed Radiation Effects Tests." Approved by committee awaiting Society ballot - R-R in preparation. |
|------|---|

F528	"Method of Measurement of Common - Emitter D-C Current Gain of Junction Transistors." Accepted by Society - Round Robin (R-R) in progress.
F616	"Method for Measurement of MOSFET Drain Leakage Current." Accepted by Society - R-R in progress.
F617	"Method for Measurement of MOSFET Saturated Threshold Voltage." Accepted by Society - R-R in progress.
F618	"Method for Measurement of MOSFET Saturated Threshold Voltage." Accepted by Society - R-R in progress.
F632	"Method for Measurement of Small-Signal Common-Emitter Current Gain of Transistors at High Frequencies." Accepted by Society - R-R plan to be revised, R-R not yet started.
F675	"Method of Test for Nonequilibrium Transient Photocurrents in p-n Junctions." Accepted by the Society - R-R plan prepared, R-R not yet started.
F676	"Method of Measurement of Nonsaturated TTL Sink Current." Accepted by Society - R-R in progress.
New-1	"Measurement of Threshold for Upset of Digital Integrated Circuits." Currently under development.
New-3	"Measurement of Neutron Recovery Characteristics." Currently under development.
New-4	"Measurement of Total Gamma Dose Recovery Characteristics." Currently under development.
New-5	"Standard for Device Burnout Testing." Preliminary study to determine research effort required underway.
New-6	"Method for Measurement of Dose Rate Response of Linear Devices." Under development.
New-7	"Practice for Performing Total Dose Irradiations of Electronic Devices." Under development.
New-8	"Practice for Performing Neutron Irradiations of Electronic Devices." Under development.
New-9	"Method of Measurement of Leakage Current of Two-Terminal Devices." Under development.

SPWG-Hardness Assurance Committee

1. "Dose Rate Response of Linear Integrated Circuits." Has been reviewed and revised, submitted to military for incorporation into MIL-STD System.

2. "Neutron Hardness Assurance Guidelines for Semiconductor Devices." Extensively reviewed and reworked; still in development, but nearing finished version.
3. "Hardness Assurance Guidelines for Total-Dose Radiation Effects on Electronic Piece-Parts," still in development, but nearing finished version.

APPENDIX A

**SUMMARY OF THE PROCEDURE PROPOSED BY CROWLEY AND STULTZ
TO DISCOVER POTENTIALLY LATCHABLE PATHS (REFERENCE 3)**

To carry out the proposed procedure, it is necessary to have on hand, in addition to the device being evaluated: (1) overlay sets and/or composite drawings which show the processing steps used to fabricate the device, (2) electrical schematics of the device, and (3) a photograph of the completed chip.

The initial step is to verify that 1, 2, and 3 all pertain to the device being evaluated. In some cases a complete electrical schematic will not be available and must be generated as part of the analysis. Next, the overlays are ordered to correspond to the actual processing steps. All external leads are identified and labeled on the photograph and the appropriate overlays. Next, each individual component is identified on the overlays and keyed to the corresponding component on the electrical schematic (it is at this point that the schematic must be generated if it is not otherwise available). Components common to a single-junction, isolated area are also identified at this time. The existence of repetitive subcircuits is also noted.

Next, a catalogue of all possible four-layer paths is prepared (the technique of Reference 4, see Appendix B, is useful here). Finally, the bias conditions of each of these paths during device operation is evaluated to see if proper forward bias on the appropriate junctions is possible. Those for which such bias is possible are candidates for latchup and must be electrically evaluated to see if they actually latch under appropriate conditions.

APPENDIX B

**SUMMARY OF THE PNPN PATH TRACING TECHNIQUE PROPOSED
BY LEAVY AND SCOTT (REFERENCE 4)**

The procedure proposed is as follows:

1. List each separate p region (identified by a subscript).
2. For each p region, list all contiguous n regions (again identified by separate subscripts). This yields a listing of all possible pn junctions.
3. For each n region list all contiguous p regions. From this prepare a list of all possible pnp paths. Although not specifically stated by Leavy and Scott, paths with the same p region at the beginning and end should not be listed here.
4. Now, using each of the paths of 3, determine the four-layer paths using the list of 2. Again, paths which double back on themselves should not be listed. This procedure produces all four-layer pnpn paths.

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