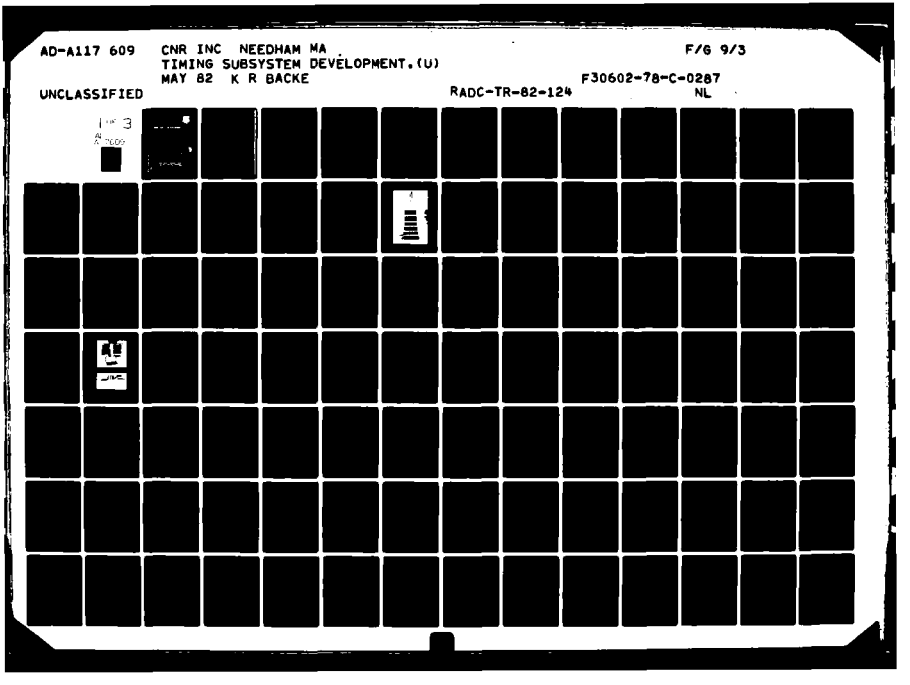
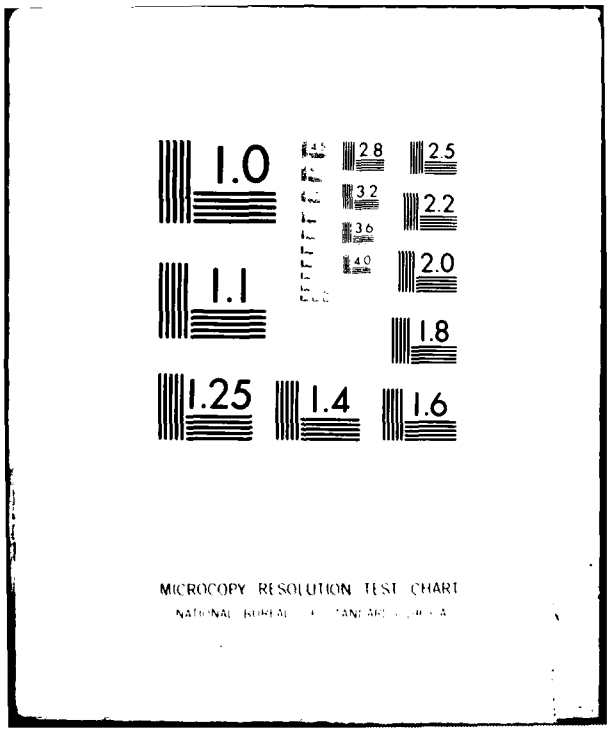
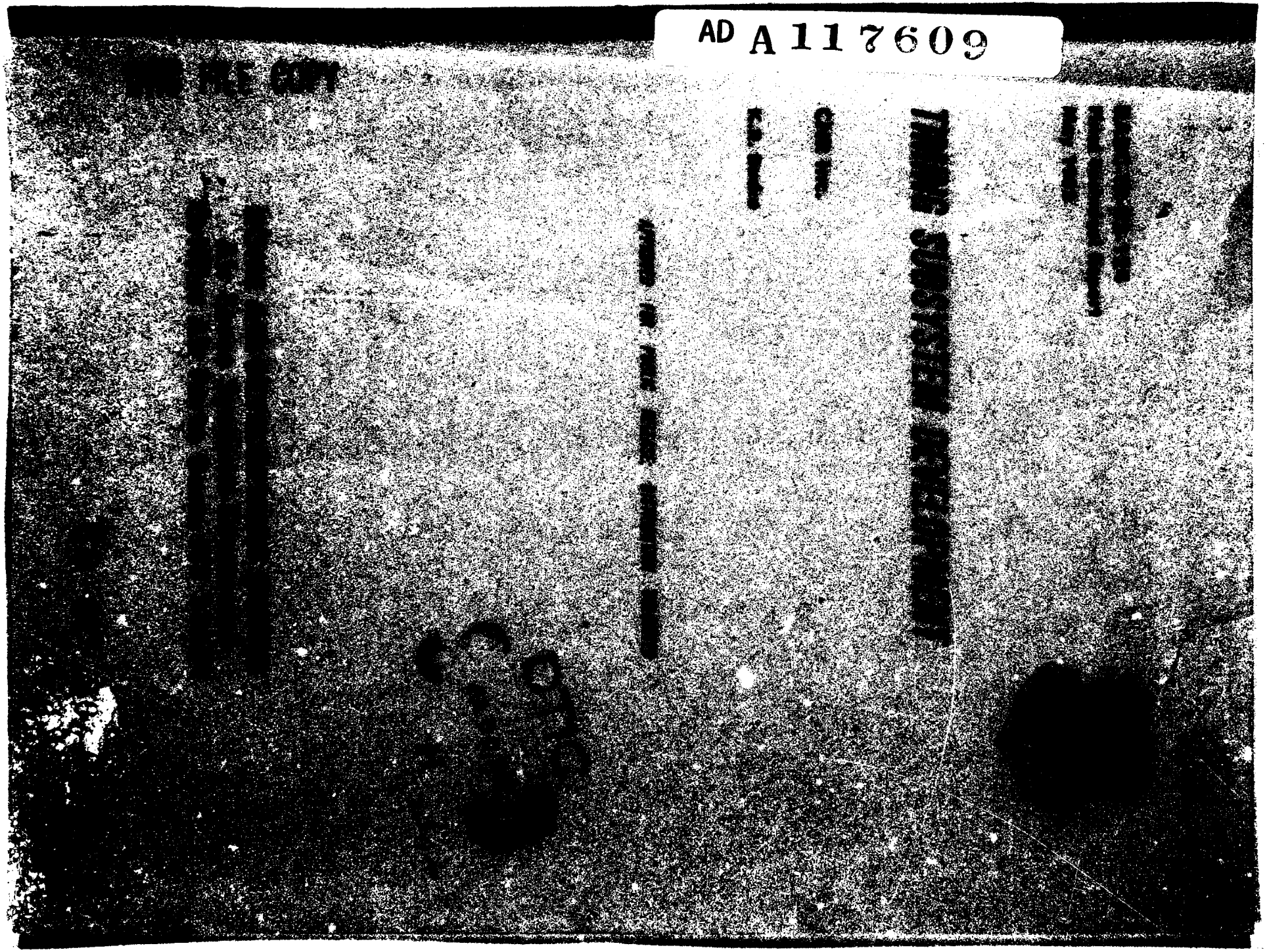
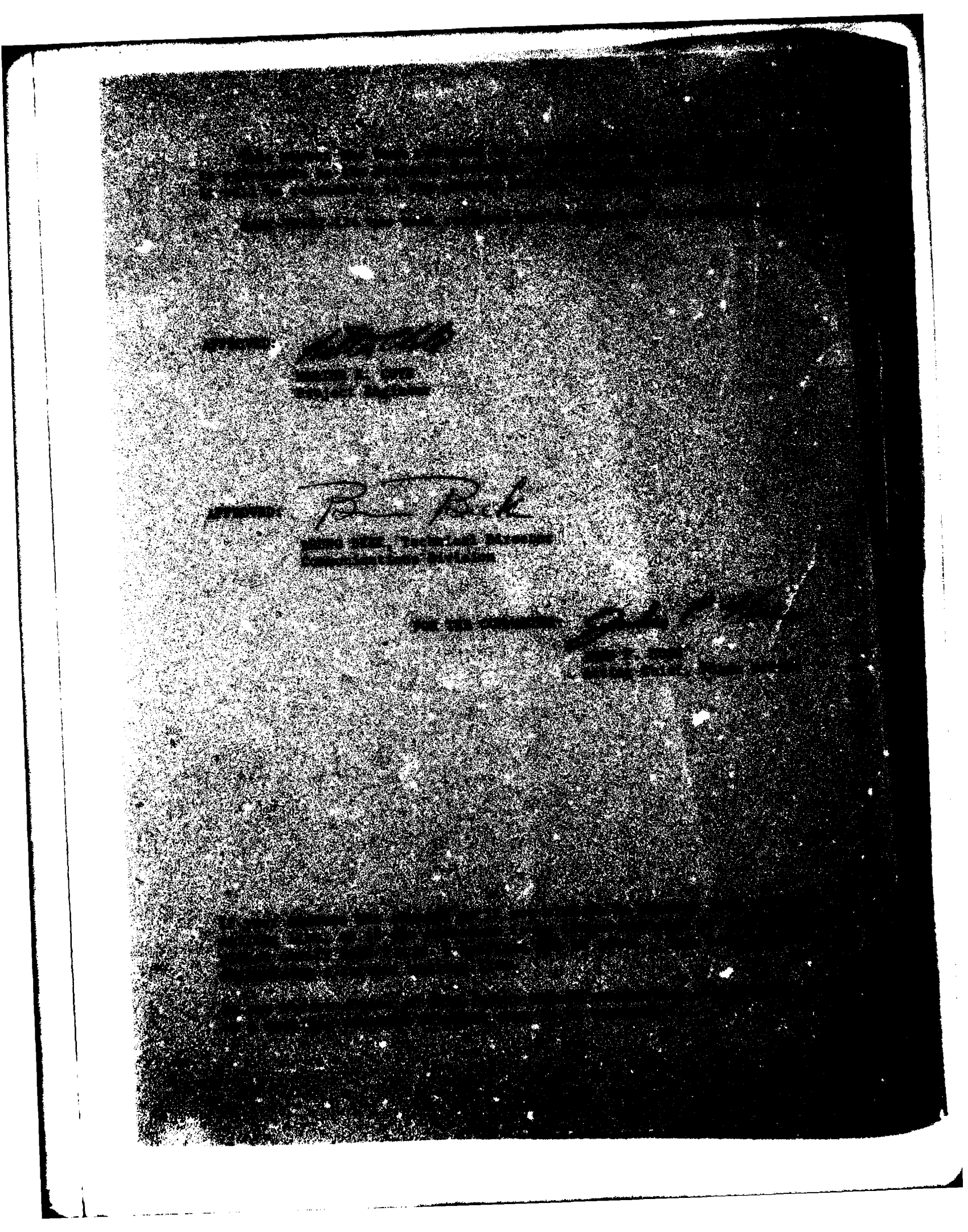
AD-A117 609 CNR INC NEEDHAM MA F/G 9/3
TIMING SUBSYSTEM DEVELOPMENT.(U)
MAY 82 K R BACKE F30602-78-C-0287
UNCLASSIFIED RADC-TR-82-124 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART





UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER RADC-TR-82-124	2. GOVT ACCESSION NO. AD-A117609	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) TIMING SUBSYSTEM DEVELOPMENT		5. TYPE OF REPORT & PERIOD COVERED Final Technical Report September 78 - July 81
		6. PERFORMING ORG. REPORT NUMBER N/A
7. AUTHOR(s) K.R. Backe		8. CONTRACT OR GRANT NUMBER(s) F30602-78-C-0287
9. PERFORMING ORGANIZATION NAME AND ADDRESS CNR, Inc. 220 Reservoir Street Needham MA 02194		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 33126F 21570405
11. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (DCLW) Griffiss AFB NY 13441		12. REPORT DATE May 1982 13. NUMBER OF PAGES 222
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Same		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Walter E. Cote (DCLW)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Digital Networks
Network Synchronization
Timing Technique
DCS Timing
Timing Subsystem

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

In the predominatly digital DCS, a requirement exists to coordinate clocks at geographically distinct nodes to handle switched ditigal traffic and provide a general system timing capability. Aside from the characteristics of the clocks, medium, and link equipment, the synchronization technique itself is an important aspect in considering overall network performance. This document presents the findings of a program in which three experimental timing subsystem prototypes were designed, fabricated and field

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

tested in a small network of troposcatter and microwave communications links. The purpose of this effort was to implement and evaluate the performance of each of five candidate timing techniques in a network environment. These candidates are; Independent Clocks, Master/Slave, Mutual Synchronization, Time Reference Distribution, and Improved Time Reference Distribution. This report includes discussions of the timing subsystem, measurement plan, and evaluation of the capabilities and performance characteristics of the candidate clock disciplining methods. Recommendations are presented based on the findings of the field tests and an evaluation of the design of both hardware and software portions of the timing subsystem prototype.

PREFACE

This final report, covering the period September 1978 to July 1981, was prepared by CNR, Inc. of Needham, MA, under Contract No. F30602-78-C-0287 with Rome Air Development Center, Griffiss Air Force Base, Rome, New York.

The special-purpose microprocessor-based Timing Subsystem hardware was designed by Mr. D. J. Miller who was also responsible for overall project management. Mr. K. R. Backe designed and implemented the control and computational software and performed much of the field engineering and data reduction tasks associated with the experimental test portion of the program.

Those involved in this project wish to acknowledge the enthusiastic support and assistance provided by the RADC Project Engineer, Mr. W. Cote. Invaluable assistance was also given by the RADC Site Supervisory Engineers, Mr. J. Findley and Mr. D. Mangold. Many other RADC personnel, including Mr. W. Voss, Mr. W. Schneider, Mr. J. Pritchard and Mr. J. Krause also made substantial contributions to the successful operation of field equipment and the authors thank them for their efforts.

TABLE OF CONTENTS

Section		Page
1	INTRODUCTION	1-1
2	EQUIPMENT DESCRIPTION	2-1
	2.1 Timing Subsystem	2-1
	2.1.1 Node Control Computer	2-3
	2.1.2 Link Termination	2-8
	2.1.3 Time Interval Measurement	2-17
	2.1.4 Node Frequency Standards	2-18
	2.2 Timing Subsystem Software Development	2-20
	2.2.1 Microcomputer Development System	2-22
	2.2.2 Development Station as Network Controller	2-26
3	TEST BED	3-1
	3.1 Tandem Network	3-3
	3.2 Link Configuration	3-6
	3.2.1 GAFB-Stockbridge-Verona LOS Link	3-6
	3.2.2 Verona-Youngstown TROPO Link	3-9
	3.3 Node Configuration	3-12
	3.3.1 Timing Subsystem	3-12
	3.3.2 Network Controller	3-12
	3.3.3 Frequency Measurement Terminal	3-17
	3.4 Test Bed Master Clock	3-19
4	EQUIPMENT DELAY MEASUREMENTS	4-1
	4.1 Equipment Delay Measurement Procedures	4-1
	4.2 Timing Subsystem Equipment Delay	4-2
	4.3 Line-of-Sight Equipment Delay	4-7
	4.3.1 LOS Modem Delay	4-7
	4.3.2 LOS Radio Delay	4-9
	4.4 Troposcatter Equipment Delay	4-12
	4.4.1 TROPO Modem Delay	4-12
	4.4.2 Delay Characteristics of the TRC-132A Radios	4-13
	4.5 Tandem Network Delay Elements	4-13

TABLE OF CONTENTS (Continued)

Section		Page
5	PERFORMANCE TESTS AND DATA PRESENTATION	5-1
	5.1 Time/Frequency Synchronization Hierarchy	5-1
	5.2 Candidate Timing Techniques	5-5
	5.2.1 Independent Clocks	5-5
	5.2.2 Master/Slave	5-6
	5.2.3 Mutual Synchronization	5-7
	5.2.4 Time Reference Distribution	5-8
	5.3 Laboratory Tests	5-11
	5.3.1 Auxiliary Reference Operation	5-11
	5.3.2 Network Operation	5-12
	5.4 Performance Assessment	5-22
	5.4.1 Performance Measurement System	5-22
	5.4.2 Methods of Verifying Network Performance	5-25
	5.5 Field Tests	5-26
	5.5.1 Two-Node Master/Slave (TROPO)	5-27
	5.5.2 Two-Node Master/Slave (LOS)	5-32
	5.5.3 Three-Node Tandem Master/Slave	5-32
	5.5.4 Three-Node Tandem Time Reference Distribution	5-36
	5.5.5 Three-Node Tandem Master Slave; Master with Large Frequency Offset	5-38
	5.5.6 Three-Node Tandem Master/Slave with Slave VCO	5-41
	5.6 Interpretation of Test Results	5-44
	5.6.1 Summary of Field Tests	5-46
	5.6.2 System Time Transfer	5-52
6	RECOMMENDATIONS	6-1
	6.1 Future Timing Subsystem Design Considerations	6-1
	6.1.1 Advanced Development Model	6-1
	6.1.2 Processor Type	6-2
	6.1.3 Data Buffer Design and Placement	6-5
	6.1.4 Error Detection/Correction	6-9
	6.1.5 Node Frequency Standards	6-12
	6.1.6 Software Design	6-13

TABLE OF CONTENTS (Continued)

Section			Page
	6.2	Network Survivability	6-15
		6.2.1 Self-Organizing Features	6-15
		6.2.2 Backup Modes of Operation	6-17
		6.2.2.1 AN/GSQ-183 Frequency Control Set	6-18
		6.2.2.2 AN/GSQ-183 as a Backup Frequency Source	6-20
	6.3	Network Timing Accuracy	6-24
		6.3.1 Precise Time Availability	6-25
		6.3.2 Dissemination of Precise Time	6-27
		6.3.3 Compliance with Federal Standard 1002	6-28
	6.4	Timing Technique Evaluation	6-29
	6.5	Future Work in Network Synchronization	6-34
Appendix			
A		SOFTWARE IMPLEMENTATION OF TIME REFERENCE DISTRIBUTION TECHNIQUES	A-1

LIST OF ILLUSTRATIONS

Figure		Page
2.1	Timing Subsystems with Network Controller	2-2
2.2	Block Diagram of Timing Subsystem Showing Interfaces with Link Multiplexers	2-4
2.3	Node Control Computer Functional Block Diagram	2-5
2.4	Parallel I/O Board	2-9
2.5	Node Control Processor	2-10
2.6	Clock Data TRIP Format	2-13
2.7	Transmit Link Termination Processor (XMIT LTP) Block Diagram	2-15
2.8	Receive Link Termination Processor (RCV LTP) Block Diagram	2-16
2.9	Block Diagram of T.I. Measuring Unit	2-19
2.10	Top-Level Software Loop	2-23
2.11	Control Flow for Node Control Computer Software Modules	2-24
2.12	Microcomputer Development System	2-25
2.13	Software Development Cycle	2-27
3.1	RADC Test Sites	3-4
3.2	Test Bed Tandem Network	3-5
3.3	Microwave Tower Survey Points (Stockbridge, Verona, Bldg. 3)	3-7
3.4	Normal Connection of Quaternary Baseband Modem to Microwave Radios	3-8
3.5	Youngstown Troposcatter Facilities (TRC-132)	3-10
3.6	Typical Modem Diversity Configuration	3-11
3.7	Node Configuration (GAFB)	3-13
3.8	Node Configuration (Verona)	3-14

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
3.9	Node Configuration (Youngstown)	3-15
3.10	Network Controller to Timing Subsystem Interconnection Scheme	3-18
4.1	Equipment Connections for Link 1 Equipment Delay Measurement	4-4
4.2	Link Interconnections for TS Back-to-Back Operation	4-5
4.3	LOS Back-to-Back Test Setup for Delay Measurement	4-8
4.4	TROPO Modem Back-to-Back Setup	4-14
4.5	Tandem Network - One-Way Equipment and Path Delay Components	4-18
5.1	Categorization of Network Synchronization Techniques	5-4
5.2	Auxiliary Reference Test Setup	5-13
5.3	Self-Reference Test Setup	5-14
5.4	Typical Acquisition Behavior of Timing Subsystem	5-16
5.5	Two-Node Performance Evaluation Test Setup	5-17
5.6	Three-Node Performance Evaluation Network (Delta)	5-19
5.7	Laboratory Tests of TRD Organizational Capabilities	5-21
5.8	Timing Subsystem Performance Measurement System	5-23
5.9	Two-Node Network with TROPO Link (Verona - Youngstown)	5-28
5.10	Typical C-Band TROPO Received Signal Levels (Quad Diversity)	5-30
5.11	Seneca, NY, vs. Youngstown and Verona (Master/ Slave TROPO)	5-31
5.12	Two-Node Network with LOS Link (Verona-Stockbridge-GAFB)	5-33

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
5.13	Seneca, NY, vs. Verona and GAFB (Master/Slave LOS)	5-34
5.14	Three-Node Tandem Network with LOS and TROPO Links	5-35
5.15	Three-Node Tandem Master/Slave Performance Curves	5-37
5.16	Three-Node Tandem Time Reference Distribution Performance Curves	5-39
5.17	Three-Node Tandem Master/Slave with Large Drift Performance Curves	5-40
5.18	Three-Node Tandem Master/Slave with Slave VCO	5-42
5.19	Useful Adjustment Range of Voltage-Controlled Oscillator	5-43
5.20	Summary of Network Configurations	5-48
5.21	Seneca, NY, LORAN-C Station Cesium Frequency Standard vs. Test Bed Rubidium Frequency Standards	5-50
5.22	LORAN-C; Dana, IN, vs. U.S. National Time Standard NBS, Boulder, CO (NBS-6)	5-54
5.23	Block Diagram of a Digital Troposcatter Link	5-55
5.24	Clock Error and Path Delay Calculations for Single- and Double-Ended TRIP Exchanges	5-58
6.1	2048-Bit Elastic Buffer	6-8
6.2	AN/GSQ-183 Frequency Control Set	6-19
6.3	Integration of the Interim Subsystem as an Alternative Reference	6-21
6.4	Integration of the Interim Subsystem as a Backup Node Clock	6-22

LIST OF TABLES

Number		Page
2-1	Comparison of Frequency Standards	2-21
4-1	Summary of Wired Link MUX/DEMUX Rates	4-3
4-2	Summary of Timing Subsystem Equipment Delay (Loop Back)	4-6
4-3	Delay Measurements for Philco-Ford Baseband Modem	4-10
4-4	GAFB, Verona, Stockbridge LC-8D Radio Delay Measured at Baseband Interface	4-11
4-5	Delay Measurements for DAR-IV TROPO Modem	4-25
4-6	TRC-132A Delay Measurements at Verona and Youngstown	4-16
5-1	Time/Frequency Synchronization Hierarchy	5-2
5-2	Comparison of Clock Adjustment Techniques	5-45
5-3	Glossary of Terms for Network Experiments	5-47
5-4	Summary of Network Parameters for Field Tests	5-49
5-5	Summary of Network Synchronization Performance	5-53
6-1	Typical Per-Second Execution Times for Timing Subsystem Microprocessor	6-4

SECTION 1

INTRODUCTION

This report is intended to support the long-term objective of digital signal synchronization within the Defense Communications System (DCS). The work described in this document covers a 3-1/2 year program consisting of design, development, fabrication, test and evaluation of three Timing Subsystem (TS) prototypes. The results obtained and recommendations presented should provide insight to the future advanced development model of a DCS timing subsystem which will distribute coordinated timing signals at each node.

The planned DCS digital transmission network can be visualized in its most elementary form as a collection of nodes interconnected by radio links or cascades of links. Bit streams originating from geographically-separated sources enter the node and typically require multiplexing for retransmission to a common destination node. However, the loss of proper timing in a synchronous digital system is catastrophic. When bits do not fall in their assigned time slots, all received information is meaningless -- a totally unacceptable situation. This characteristic makes the timing/synchronization function one of the most important functions in a digital communications system [1.1]. Problems have occurred in the timing relationship between different digital communications networks that were not originally engineered to communicate with one another. In some cases, these problems were overcome by the addition of variable storage buffers and adequate clocks to control them, while in other cases modification of equipments might also be required. Even after these corrective measures, it might be necessary to occasionally interrupt traffic to reset the variable storage buffers. It is not always possible at the time of equipment development to predict just what system interfaces will be required during the lifetime of an equipment. Therefore, design of the equipment to meet a minimum timing compatibility standard is highly desirable for avoiding future problems. Such a timing compatibility standard should follow a well-developed DCS timing plan. See [1.1].

In the past few years, various methods of avoiding or minimizing these undesirable phenomena have been proposed, including independent highly stable atomic clocks [1.2], mutual

frequency averaging [1.3], hierarchical master/slave [1.4], and self-organizing master/slave [1.5]. More recently, consideration has been given to the use of network facilities for systemwide transfer of a time reference [1.6] [1.7], and theoretical models have been used to predict relationships between time transfer accuracy and link parameters. To satisfy normal communication requirements, relative time synchronization of the nodes is sufficient, i.e., the node clocks need not be phased identically as long as their mutual average frequency offsets are zero. On the other hand, transfer of a time reference throughout a network is equivalent to the requirement that node clocks be synchronized with zero phase offset. The additional hardware required for time reference transfer does not appear to be significant for a production timing subsystem model, and the benefits of a systemwide time reference certainly justify further examination.

The DCS network involves a large number of links and nodes with various categories of transmission media, including line-of-sight microwave (LOS), troposcatter (TROPO), satellite, and cable. The variety of transmission equipment that is available now, or planned as part of the all-digital network, makes a complete and comprehensive evaluation of system performance difficult; therefore, an emphasis in the experimental work reported on here has been toward timing technique synchronization performance on a small (three node) Test Bed.

This effort, under contract with CNR, Inc., Needham, MA, was conceived to produce three Timing Subsystem prototypes in order to provide the necessary measurement and processing capabilities to implement and evaluate a series of timing technique candidates. Although many techniques for timing and synchronization have been proposed and studied, as yet a direct comparison in the field had not been attempted. The modes of operation are Independent Clocks, Mutual Synchronization, Master/Slave, Time Reference Distribution, and Improved Time Reference Distribution. The candidates were implemented in nodal software. Laboratory as well as field evaluation determined the capabilities and performance characteristics of each method. Valuable insight was gained concerning the implementation difficulty or other pecularities associated with the timing technique candidates. Perhaps overlooked as a simple task, the practice of keeping all the link equipment operational

proved to be far more difficult than originally anticipated. Setup and shakedown time as well as equipment maintenance efforts were compounded due in part to the distance between sites. Node-to-node communication was through TROPO and LOS links.

Three Timing Subsystem prototypes were constructed to enable network-level timing and synchronization experiments on the RADC (Rome, NY) Test Bed. The results of this comparison are presented in this report. Also included are a brief description of the Timing Subsystem hardware and software components as illustrated in Section 2. This section labels the major functional portions of the equipment as well as the methodology behind the design and implementation of nodal software to control and orchestrate processing, link input/output and performance monitoring tasks. Although not actually part of the Timing Subsystem, the role of the microcomputer development system as both a software development facility and a network controller is also discussed in this section.

Section 3 labels the criteria and follows the series of events leading to the final network configuration used for both two-node and three-node timing experiments. Detailed descriptions of link equipment connections to the timing subsystem enhance the presentation of the tandem network radio links. Next, an account of node equipment connections brings to light the scheme used to evaluate clock performance during timing technique tests. Finally, a choice of Test Bed master clock is made and selection criteria reviewed.

The first equipment delay measurements are revealed in Section 4 which is devoted to itemizing modem, radio and path delays of link equipment used for network synchronization tests. A look at the procedure used for measuring equipment delay automatically through the Timing Subsystem's back-to-back error measurement facilities precedes tabularized results for both LOS and TROPO paths. Where precise measurements were not possible, findings from a previous CNR, Inc. effort [1.8] supplement the data. Section 4 closes with a "roadmap" summary of all the one-way delay elements of the tandem network.

A review of the candidate timing techniques and how each fits into a general classification of a time/frequency synchronization hierarchy, sets the framework for the ensuing description of both laboratory and field tests presented in

Section 5. Included in this chapter is a discussion of the methodology behind the performance measurement system using both the Timing Subsystem's and Frequency Measurement Terminal's (FMT) [1.9] time interval measurement capabilities. This serves to clarify the presentation of results of the network synchronization tests. Section 5 closes with a summary of the experiment program and node parameters for each test. A review of the time transfer mechanism and error computation techniques is also included.

Section 6 contains recommendations for a future timing subsystem advanced development model as well as interim subsystem (AN/GSQ-183) interfacing and operation when used as a backup frequency source. Section 6 continues by discussing network timing accuracy considerations, timing technique candidates and general recommendations for future work in network synchronization. Appendix A contains summaries of the software implementations of Time Reference Distribution [1.6] and Improved Time Reference Distribution [1.7] as interpreted by CNR, Inc.

REFERENCES

[1.1] H. A. Stover, "Attributes for Timing in a Digital DCS," Defense Communications Engineering Center, Publication No. 1-80, July 1980.

[1.2] W. O. Woolsey, et al., "Network Bit Synchronization Atomic Clock Versus Frequency Averaging," ECOM-0040-F, July 1968.

[1.3] M. W. Williard, "Analysis of a System of Mutually Synchronized Oscillators," IEEE Trans. on Comm. Tech., Vol. COM-18, No. 5, October 1970, pp. 467 - 483.

[1.4] B. R. Saltzberg and H. M. Zydney, "Network Synchronization," BSTJ, Vol. 54, No. 5, May 1975, pp. 879 - 892.

[1.5] J. G. Baart, et al., "Network Synchronization and Alarm Remoting in the Dataroute," IEEE Trans. on Comm., November 1974, pp. 1873 - 1877.

[1.6] H. A. Stover, "Time Reference Concept for the Timing and Synchronization of the Digital DCS," DCASEF TC39-73, July 1973.

[1.7] H. A. Stover, "Improved Time Reference Distribution for a Synchronous Digital Communications Network," 8th Annual PTTI Conference Record, November 1976, pp. 147 - 166.

[1.8] CNR, Inc., "System Timing and Synchronization," Final Report under Contract No. F30602-76-C-0347 with RADC, May 1978.

[1.9] Frequency Measurement Terminal Instruction Manual, U.S. Dept. of Commerce, National Bureau of Standards, Time and Frequency Division, Boulder, CO, November 1975.

SECTION 2

EQUIPMENT DESCRIPTION

Three prototype Timing Subsystems were tested in a small network TEST Bed at RADC. The Timing Subsystems (TS's) are responsible for clock data transmissions between nodes and the updating of local references. Between nodes there is an exchange of clock control data, as shown by the "Time Reference Information Packets" (TRIP's). These data packets spurt between all connected nodes at a rate of 4 kb/s beginning at every second. Their primary function is the transfer of clock control data and node reference information.

Network control is accomplished by telephone access to each of the TS's through the couplers and modems provided by a Frequency Measurement Terminal (FMT) located at each site. It is through these means that each Timing Subsystem and FMT may be interrogated and experimental results obtained.

2.1 Timing Subsystem

The basic function of a Timing Subsystem is to combine locally-made timing measurements with timing information transmitted from other nodes in order to compute the local node clock error relative to a master reference. The nature of this reference is determined by the particular synchronization technique being evaluated. Then, based on the computed clock error, the TS corrects its local node clock and transmits local timing information to other nodes.

Figure 2.1 shows a photograph of the three Timing Subsystems and the Network Controller. Each subsystem consists of a double bay chassis with a total rack mountable equipment space of 84 inches. Following is a list of the removable assemblies and the rack space each occupies:

Left Side

- Power Supply Drawer (10")
- Spare (16")
- Card Cage (16")

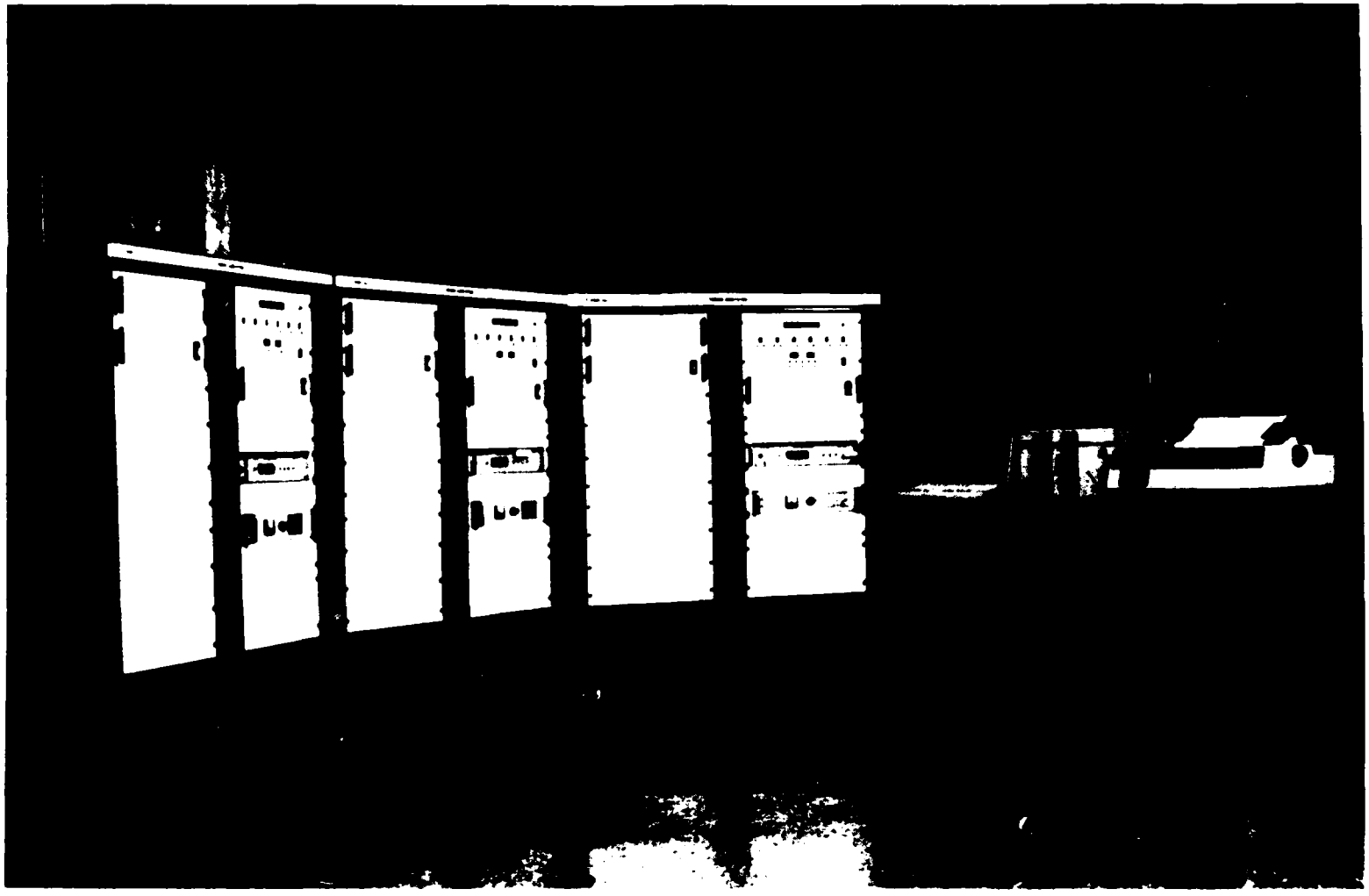


Figure 2.1 Timing Subsystems with Network Controller

Right Side

- Display Panel (10")
- Frequency Distribution Unit (5")
- Spare (5")
- Phase Microstepper (3")
- Spare (3")
- Distribution Amplifier (3")
- Spare (3")
- Spare (10")

Figure 2.2 shows a block diagram of a Timing Subsystem. The locally-made timing measurements are performed by the Time Interval Measurement unit, and timing information from other nodes is extracted from the Receive Link Termination Processors (RCV LTP's). The node control computer computes the local node clock error and corrects the clock (node frequency standard) with a software controlled phase microstepper (or VCO). Local timing information is transmitted to the nodes via the Transmit Link Termination Processors (XMIT LTP's).

2.1.1 Node Control Computer

The Timing Subsystem (TS) computer is microprocessor-based equipment designed around the Motorola 6800 series of devices. Control and computational hardware are located on a single wire-wrap board while I/O devices are split between two additional boards. Flexibility of the TS is enhanced by the extensive use of programmable I/O for controlling external equipment.

In this subsection, we briefly describe each of the major hardware building blocks incorporated within the node computer. Figure 2.3 shows a functional block diagram of the node control computer giving an indication of the breakdown of processing functions. Notice the Interrupt Dispatcher is the routine that orchestrates software execution with the TS programs.

The Node Control Processor (NCP) consists of the following major elements, each of which is described briefly in this subsection. A more complete hardware description is contained in [2.1]:

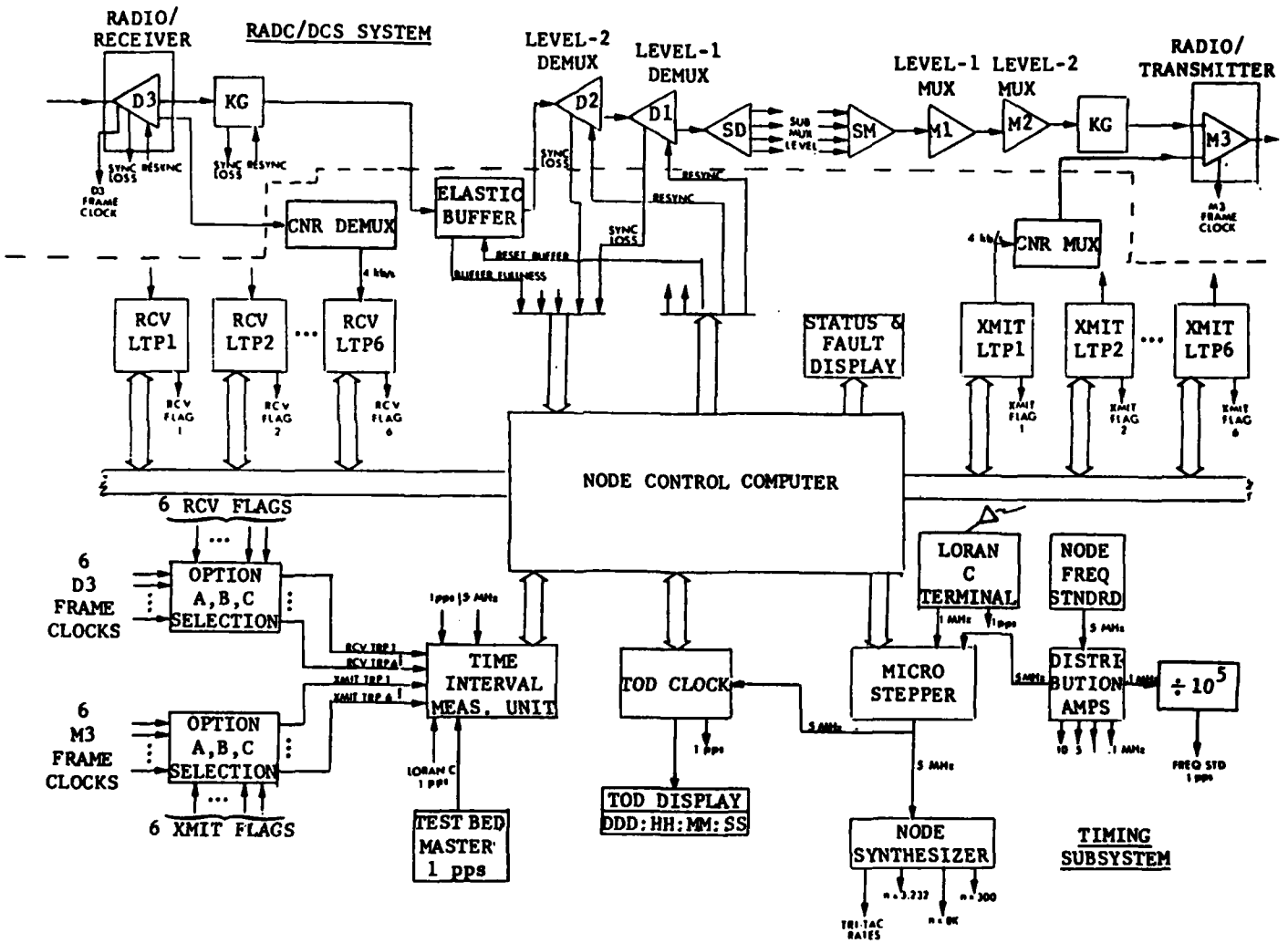


Figure 2.2 Block Diagram of Timing Subsystem Showing Interfaces with Link Multiplexers

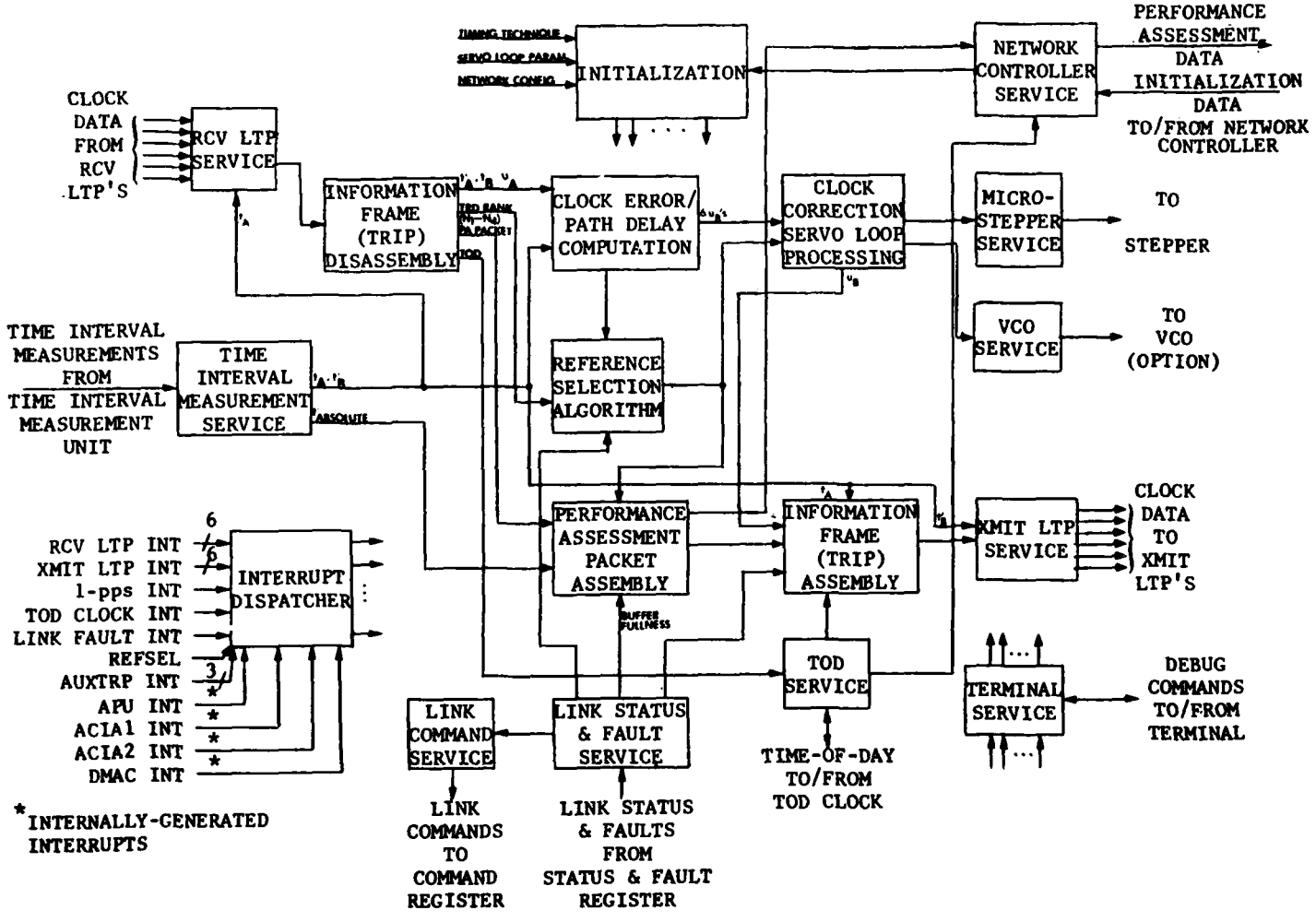


Figure 2.3 Node Control Computer Functional Block Diagram

- Microprocessor
- Random Access Memory (RAM)
- Read Only Memory (ROM)
- Arithmetic Processing Unit (APU)
- Serial/Parallel I/O
- Link Termination I/O
- Interrupt Priority Encoder

The heart of the Timing Subsystem is the Motorola M6800 microprocessor. When executing the node control programs, the M6800 is the controlling device within the equipment. Through the programmable capabilities of many external I/O devices, the microprocessor can transmit and receive information, read status, control external devices, and supervise node computational processing. The following list describes some of the features of this device. A more detailed description may be found in [2.2].

Some of the more important features of the MC6800 microprocessing unit that contribute to the "ease of use" in a system are:

- 8-bit bidirectional data bus
- 16-bit address bus - 65K bytes of addressing
- 72 instructions - variable length
- Seven addressing modes (direct, relative, immediate, indexed, extended, implied, and accumulator)
- Interrupt vectoring
- Two accumulators
- Index register
- Program counter
- Stack pointer and variable length stack
- Condition code register (6 codes)
- Separate nonmaskable interrupt

Briefly, computer memory in the Timing Subsystem is divided into two sections: Random Access Memory (RAM) and Read Only Memory (ROM).

The M6800 microprocessor has the capability to address up to 65K (2^{16}) locations from its 16-bit address bus. The Timing Subsystem has 8K (2^{13}) bytes of RAM storage available for use by the microprocessor for scratchpad, parameter storage, pointers, buffers, etc. This is volatile semiconductor memory that does not save bits when power is removed. Below is a list of some of the more important functions RAM is used for:

- Process scheduling tables
- Programmable parameter storage
- XMIT, RCV buffers
- XMIT, RCV pointers
- System monitor pointers and scratchpad
- PLL and arithmetic scratchpad
- Performance assessment data storage
- Diagnostic buffers and pointers
- System stack

Node control programs reside in ROM located on the CPU board. Vectoring to the entry point of the system programs is automatic upon application of AC power. Program development was made easier with a microcomputer development system used during the program. The development station also has a ROM programmer to load and burn ROMs for installation in the Timing Subsystem. Included in the development system's capabilities is a hardware emulator that was used to debug the Timing Subsystem computer sections.

The Arithmetic Processing Unit (APU) is a monolithic device that provides high performance fixed and floating point arithmetic and a variety of floating point trigonometric and mathematical operations.

All transfers, including operand, result, status, and command information, take place over the 8-bit system data bus. Operands are pushed onto an internal stack and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered. Reference [2.3] further describes this device.

Transfers to and from the APU are handled directly by the microprocessor. Upon issuing a command to the APU, the device is polled by the CPU until APU execution is completed. This method of control is perhaps not the most efficient use of processor time; however, it greatly simplifies program control and software overhead. Additionally, worst-case APU computation times are not slow enough to require use of Direct Memory Access (DMA) or APU interrupt capabilities.

2.1.2 Link Termination

The Timing Subsystem computer hardware contains a significant number of I/O devices to facilitate external communication with the node. Summarized below are each type of I/O hardware and its associated functions. Figures 2.4 and 2.5 depict all devices under direct microprocessor control.

Parallel I/O is handled by Peripheral Interface Adapters (PIA) under microprocessor control. Each PIA supports the following functions:

- Two 3-bit bidirectional data buses for interface to peripherals
- Two programmable control registers
- Two programmable data direction registers
- Four individually-controlled interrupt input lines; two usable as peripheral control outputs
- Handshake control logic for input and output peripheral operation

These devices are interfaced with various external hardware and allow direct microprocessor control of the following functions:

- Commands and status for front panel display for all six links
- Microstepper control and data interface
- Time interval measurement unit address selection and data interface
- All other front panel display indicators
- VCO option data port
- Time-of-day (TOD) clock interface

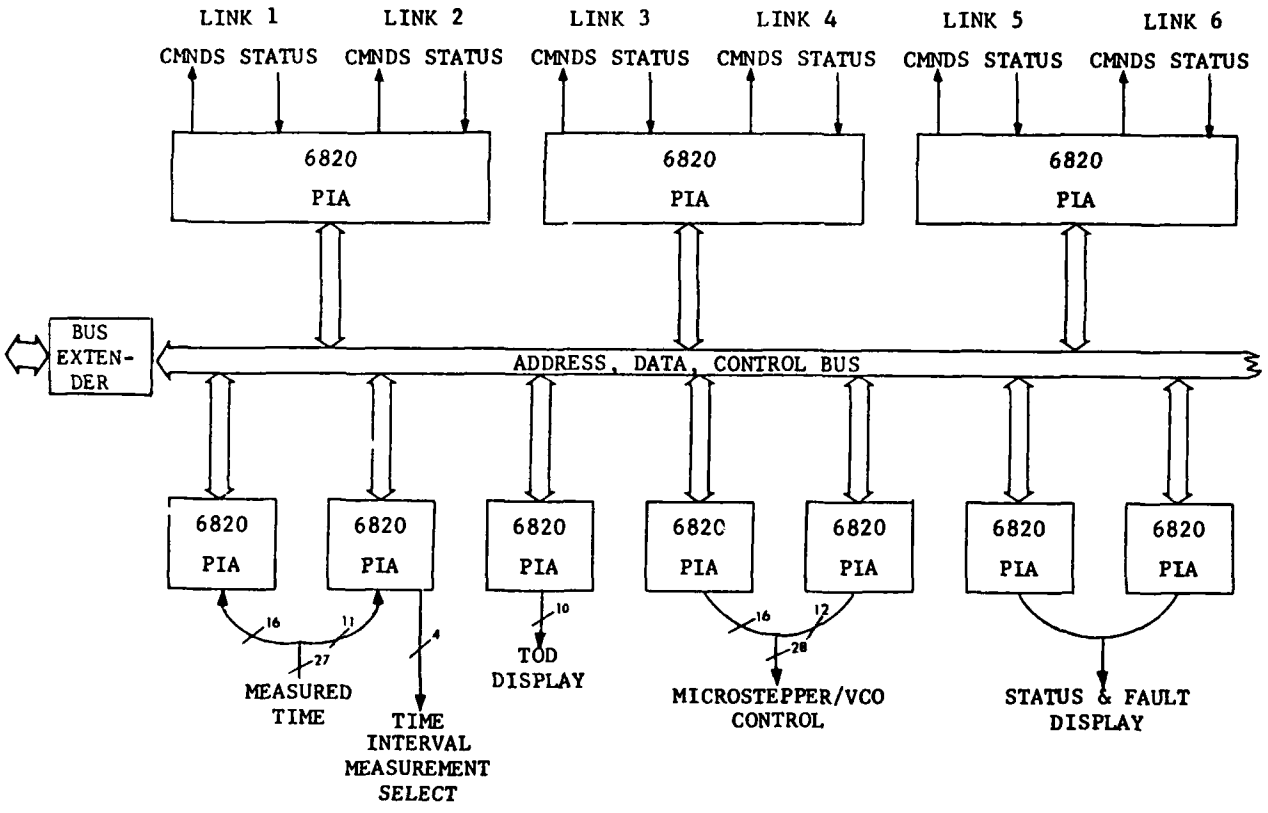


Figure 2.4 Parallel I/O Board

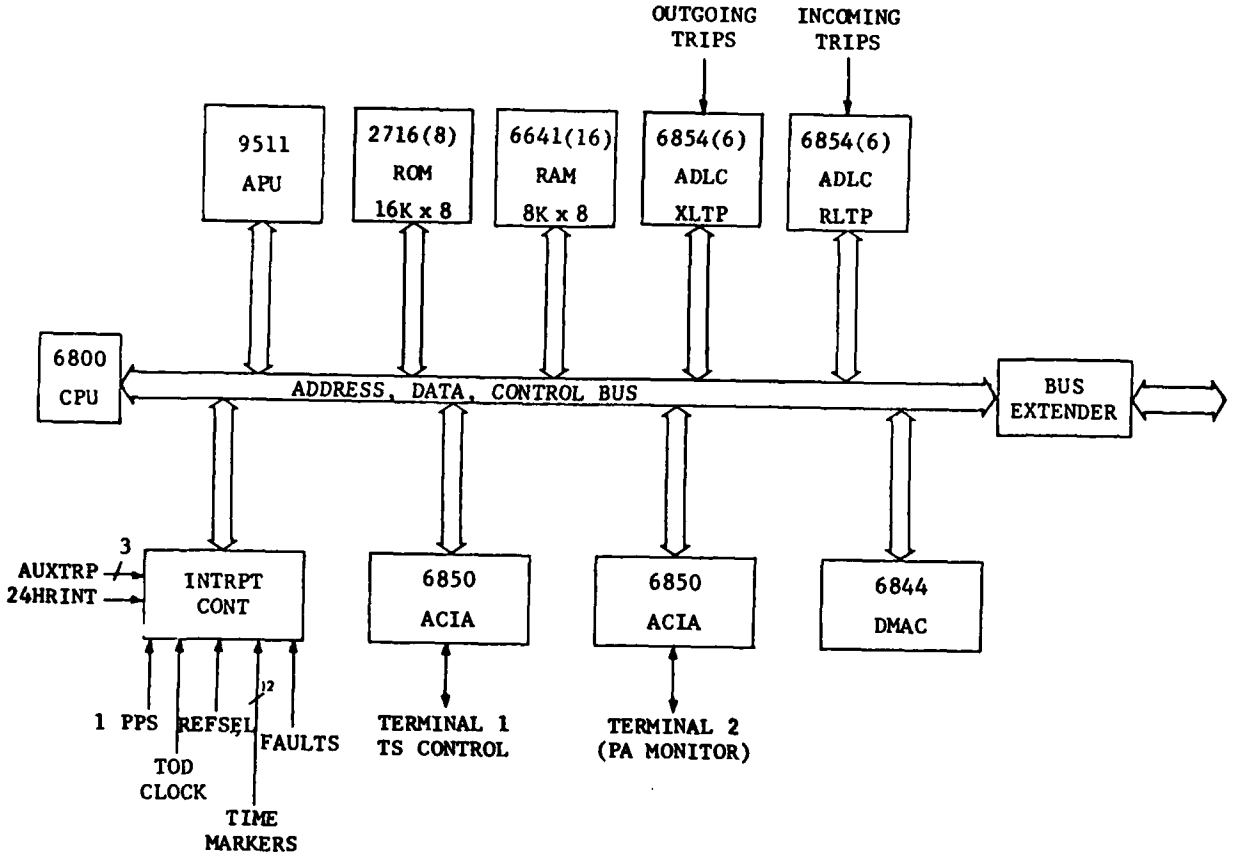


Figure 2.5 Node Control Processor

The Link Termination Processors (LTP's) support the clock data communications through the service channel multiplexers. In particular, they support the Synchronous Data Link Control (SDLC) protocol with the following functions:

- Zero insertion and deletion for runs of 1's
- FLAG, ABORT, and GO AHEAD bit sequences
- Frame check sequence generation and transmission (CRC-CCITT, $\chi^{16} + \chi^{12} + \chi^{5} + 1$)
- Error checking at receiving station
- Secondary station address comparison with frame address (optional)

Clock data is transmitted in an SDLC information frame (TRIP). The frame contains timing information necessary for clock correction.

These devices service the complex protocol required for transmit and receive data patterns. There are 12 ADLC devices in the TS hardware.

A third type of I/O device under computer control is the Asynchronous Communication Interface Adapter (ACIA). These provide a convenient RS-232 standard interface for the operator's console. It is used along with a programmable dual baud rate generator. Significant features include the following:

- 8- and 9-bit transmission
- Optional even and odd parity
- Parity, over-run, and framing error checking
- Programmable control register
- Up to 500-kb/s transmission
- Double-buffering

The clock data is transmitted in an SDLC information frame (TRIP). It is used to send initialization data around the network, and also contains timing and status information necessary for clock correction.

The data format for a TRIP is shown in Figure 2.6. It contains all of the clock update parameters for the link in question, as well as performance assessment parameters. The clock update parameters include the following:

Node Status - sync and overflow condition flags for radios and buffers; also, loop mode, e.g., acquisition and tracking.

Transmit Time (t'_A) - measured time of previous outgoing TRP signal relative to 1 pps.

Receive Time (t_B) - measured time of previous incoming TRP signal relative to 1 pps.

Clock Error (u_A) - current estimate of clock error.

TRD Rank and Merit Parameters - TRD decision parameters N_1, N_2, N_3, N_4.

Second Count - time in seconds at last 1-pps tic at transmit node (stored in a shifted binary pattern).

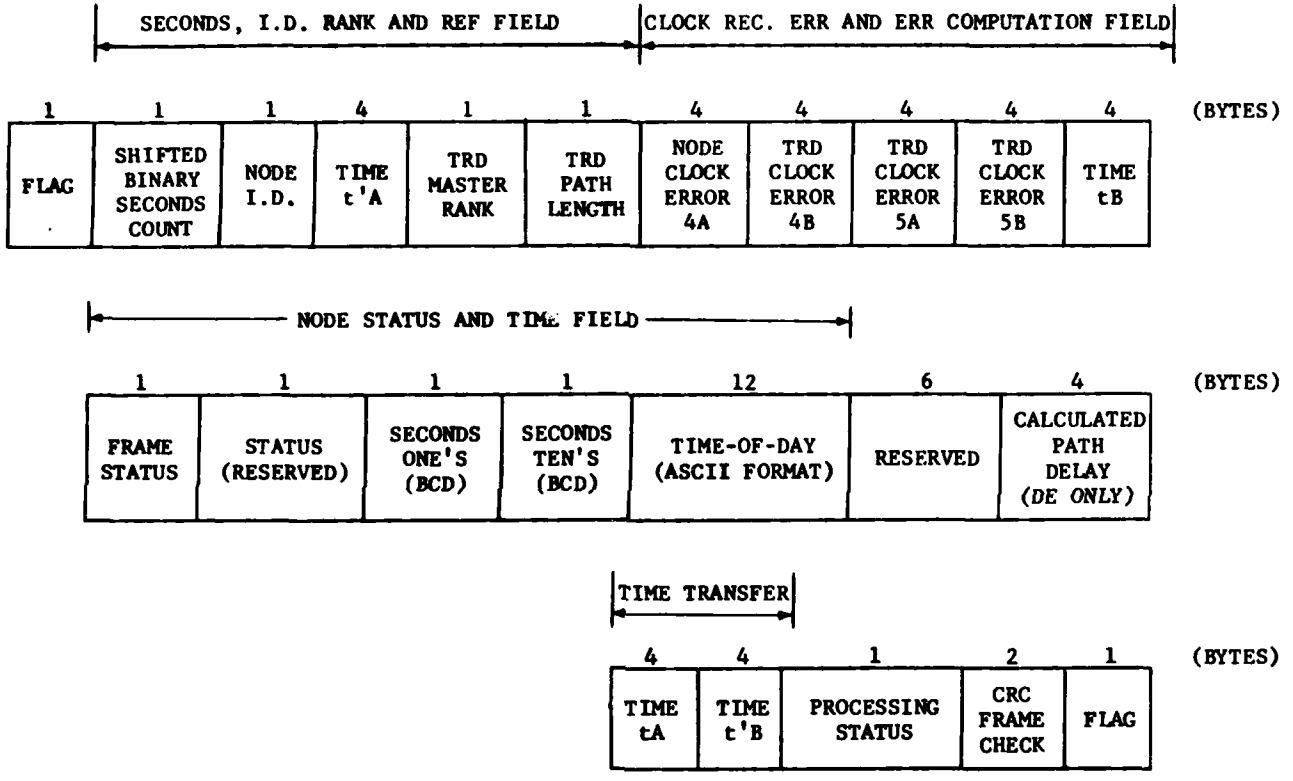
The number of bits allowed for each of these parameter fields is seen near the bottom of Figure 2.6, along with the standard SDLC control address, flag, and frame check fields.

The remaining packet capacity is allocated to performance assessment parameters. In addition, provision has been made for transmission of date and time of day resolved down to 1 minute; this is transmitted only on the minute boundaries in order to conserve space in the 1-second data transmissions. The performance assessment parameters include the following:

Current Reference/References in Use - For TRD, the node currently being referenced by the transmit node; for mutual sync, the references used in the formation of the clock correction signal.

Buffer Fullness - The relative fullness of each of the six FIFO's at the transmit node.

Absolute Clock Error - Time difference between TEST BED master 1 pps and local node reference 1 pps.



[TOTAL NUMBER OF BYTES = 67]

[TOTAL NUMBER OF BITS = 536]

Figure 2.6 Clock Data TRIP Format

Finally, it should be noted that time-of-day variables are transmitted as 8-bit ASCII (for a total of 96 bits) when the time marker message is transmitted (once per second). Other parameters are single bit flags, addresses (8-bit bytes), or floating point variables (24-bit mantissa plus 7-bit exponent plus a sign bit). The total bit count comes to 536 bits, which sets the minimum data rate requirement at 536 b/s.

Figure 2.7 shows a functional block diagram of a transmit LTP. It communicates with the node control computer through a data bus interface. Data bytes to be sent out through the LTP are passed from the data bus interface to a FIFO, and then converted to serial form by the shift register. The cyclic reducdancy error check sequence is added at this point, and the data then passes through a zero insertion circuit. This circuit insures that no data byte will look like a flag byte. The output data is scanned by the flag detect circuit to indicate the transmission of a flag, which is used as a TRP for Option C [2.4].

Figure 2.8 shows a functional block diagram of a receive LTP. Incoming data passes through a zero deletion circuit (performs complementary function of XMIT LTP zero insertion circuit) to a serial in, parallel out shift register. The data bytes then are fed to a FIFO and get to the node control computer through a data bus interface. The incoming data has the cyclic redundancy error check sequence verified; errors are indicated in a status register which can be read by the node control computer. The flag detect circuit provides the TRP output to the time interval measurement unit for Option C.

All of the functions of a link termination processor are implemented with a single LSI integrated circuit - Motorola's Advanced Data Link Controller (MC6854). This circuit supports a 1 Mb/s data rate, bit-oriented protocols (SDLC, ADCCP, HDLC), error checking (CRC16), and has an easy interface to the 6800 microprocessor.

Due to the extensive use of interrupts within the Timing Subsystem, a custom interrupt encoder that essentially prioritizes 24 levels of hardware interrupts handles the interrupt

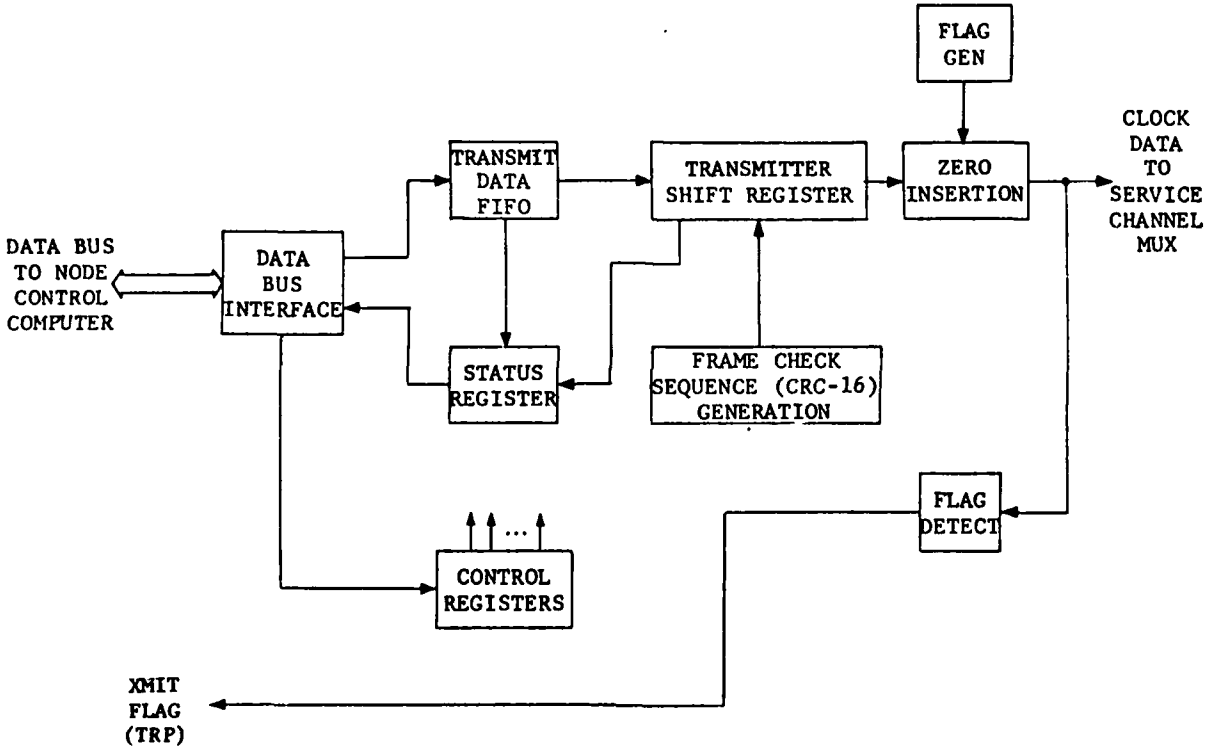


Figure 2.7 Transmit Link Termination Processor (XMIT LTP) Block Diagram

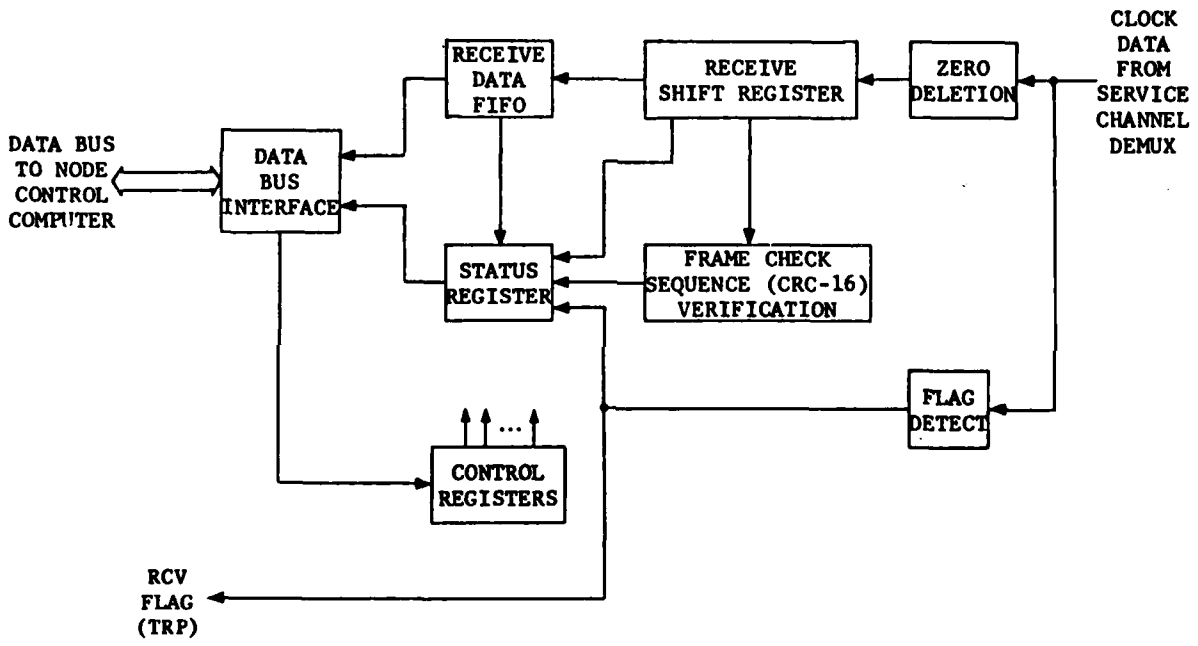


Figure 2.8 Receive Link Termination Processor (RCV LTP) Block Diagram

routing chores. Each of the incoming interrupts is ANDed with a programmable mask register producing an enabled and disabled interrupt request line. A holding register latches each request line and guarantees synchronism with the microprocessor states by using the same process clock as the MPU. Next, as hardware interrupts are received, a cascaded priority encoder arrangement allows interrupt service based on hardware priority. The software interrupt vector is generated by a set of ROMs with each interrupt having a unique jump table location. Control is transferred to the location pointed to by the address found in the jump table.

2.1.3 Time Interval Measurement

The basic measurement capability of the Timing Subsystem is the recording of time intervals between once-per-second pulses via the Time Interval Measurement Unit. This single board interval counter contains 14 read-only registers and one write-only select register. The node computer first selects a channel and then reads a number showing elapsed time from the source (adjustable 1-pps output from the Timing Subsystem) to the pulse from the selected channel. Measurements are latched in the output register indefinitely depending on the state of the select word and in the internal registers for a period of one second.

Each of the Time Reference Pulses (TRPs) has a period of one second, so the maximum measurement interval is one second. The system has 10-ns resolution because the measurement is made with counters clocked at a 100-MHz rate. The number of bits used to describe the time interval at the 100-MHz rate is 1 s/10 ns = 10^8 and $2^{26} < 10^8 < 2^{27}$. Therefore, a 27-bit counter is used.

There may be up to 15 incoming time interval measurements each second to be recorded for subsequent transfer to the node control computer. This is done with 10 27-bit registers whose outputs are multiplexed to the computer. The operation is as follows: The local 1-pps reference resets the counter which then proceeds to count 10-ns time intervals. Upon arrival of a time reference pulse, the counter contents are strobed into one of the registers, and an interrupt is issued to the computer. The interrupt service routine now outputs the multiplexer select signals and reads in the measurement data.

The six outgoing time interval measurements are under control of the transmit Link Termination Processors. Therefore, the measurements can be done sequentially, using only one 27-bit storage register. Operation goes as follows: The local 1-pps reference resets the counter and issues an interrupt to the computer. The computer responds by initiating a transmission through one of the LTP's. The TRP from this LTP strobes the counter contents into the register. The computer now reads the measurement data from the register and initiates the next LTP transmission. This continues until all six transmit LTP transmissions are complete.

Figure 2.9 shows a block diagram of the TIM board.

2.1.4 Node Frequency Standards

The choice of frequency source for the Timing Subsystem station standard centers around cost and site equipment availability. If at a given site, a frequency standard is not available, the Timing Subsystem must employ its own internal frequency source to allow stand-alone operation. During the design phase of the program, it was anticipated that, in certain tests, the Timing Subsystems would be equipped with atomic standards. Therefore, space was provided in the chassis for such units. However, two of the three TS prototypes also contained Voltage Controlled Oscillators (VCO) to enable stand-alone operation for performance comparisons using more stable oscillators [2.5]. This device was the station standard whenever an atomic standard was not available. Under these circumstances, its output was used to drive the station synthesizer and frequency distribution system. The characteristics of the quartz oscillator are quite satisfactory for the intended applications where the Timing Subsystem is operated in disciplined modes. Furthermore, the high servo update rate of 1 per second is well-matched to the use of quartz frequency sources in the subsystems.

Whether from an external source or an internal oscillator, the TS requires a 5-MHz frequency source to be used as station standard time. Also, a method to adjust that source based on servo loop corrections must be present. The two alternatives are a voltage controlled oscillator or a phase microstepper. The former is controlled by the node computer via a D/A interface while the latter is manipulation directly by the computer through a parallel interface.

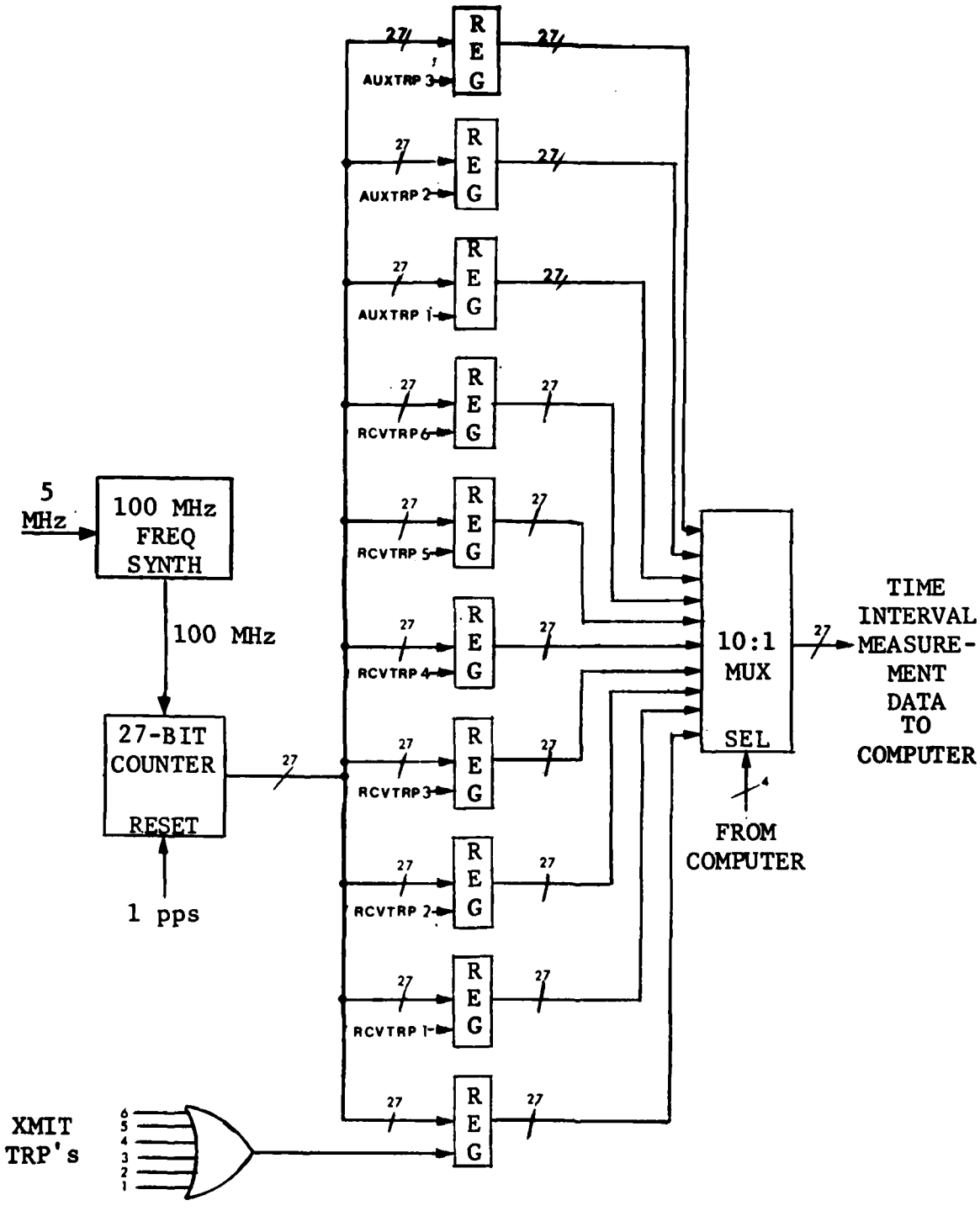


Figure 2.9 Block Diagram of T.I. Measuring Unit

The inherent stability, both short term and long term, of the frequency standard plays only a minor role for the case of a slaved clock but a much more important one for the case of a network master source (undisciplined). Therefore, a disciplined clock need not be of highest quality (i.e., quartz). A direct comparison of frequency sources may be found in Table 2-1.

2.2 Timing Subsystem Software Development

During the early stages of the program, it was proposed to design a rather general purpose microcomputer capability into the Timing Subsystem hardware. It was essential that a combination of minimal complexity, low cost and ease of programming be incorporated in such a design. This most certainly ruled out an external general-purpose microcomputer as a TS controller because it involved more hardware and software capability than was needed plus the obvious factor of increased cost. Clearly, a custom designed but general-purpose "microcomputer on a board" was the most cost effective approach. With extensive use of programmable I/O hardware and a floating point arithmetic device, the Timing Subsystem was given the powerful data handling and computational capabilities required to terminate up to 6 links, provide error processing for each as well as general nodal timing tasks. Design effort was minimal and followed standard microprocessor applications suggestions. The previous subsection describes in further detail the computer-based hardware.

Timing Subsystem software was a natural candidate for modular construction. Considering that most processing functions are triggered by external events (TRP pulses, 1-pps events, etc.) modularity became a necessity. Software tasks were broken down into functional pieces and coding performed after detailed flowchart analysis. The orchestration of many external interrupts and the relative asynchronism between them required the use of a process arbitration function to be implemented in software. This process, called the Interrupt Dispatcher, is responsible for scheduling events and arbitrating between routines requesting service. In the special case when there are no scheduled processes, the Interrupt Dispatcher will transfer control to the system monitor software to detect any pending commands. Thus, the Timing Subsystem software allows interactive operation with a user even when the system is fully loaded. Maximum flexibility is achieved by incorporating this small monitor as a part of the nodal software. Most

TABLE 2-1

COMPARISON OF FREQUENCY STANDARDS

Standard	Short-Term Stability		Long-Term Stability		
	1 sec	100 sec	Accuracy	Adjustment	Drift Rate
Cesium Atomic Beam Resonator	5×10^{-12}	10^{-12}	1×10^{-11}	7×10^{-13}	None
Rubidium Gas Cell Resonator	5×10^{-12}	5×10^{-13}	5×10^{-11}	2×10^{-12}	1×10^{-11} per month
Quartz Crystal Oscillator (VCO)	3×10^{-11} typ	10^{-11}	--	2.5×10^{-6} typ	1×10^{-9} per day typ

commands are issued with a single keystroke. Figure 2.10 depicts the top level software loop just mentioned.

Once system operation has begun via keyboard command, all timing functions are automatic and the operator's terminal may be used as an interactive monitor.

Control flow for the software modules is shown in Figure 2.11. Notice that several processes execute immediately without notifying the Interrupt Dispatcher. These routines share in common highest priority and minimal execution time, thus eliminating the need for process arbitration. A more detailed software description may be found in [2.1].

To encapsulate the philosophy behind Timing Subsystem software development, it is important to realize that given the hardware to perform link termination time interval measurement and frequency distribution tasks, then adding microprocessor interfacing for control of this equipment, the groundwork for a powerful and flexible device is set. By using the same hardware and merely manipulating software, any number of timing functions or system configurations may be implemented. In this light, the Timing Subsystem may be considered a fully-programmable frequency measurement device capable of automatic clock disciplining.

2.2.1 Microcomputer Development System

Timing Subsystem software development was made less cumbersome through the use of a microcomputer development system. Apart from its powerful software aids, including disk operating system and file management, edit, assembly and debug programs, it represents a general microcomputer product easily adapted to many applications requiring processing, storage and display capabilities.

The development systems hardware includes a dual floppy disk drive, keyboard, CRT, line printer, RS-232C interface, and in-circuit emulator. Also built in is an IEEE-488 instrument interface. The system is pictured in Figure 2.12.

Through the use of the development system, editing, assembly and linkage chores were handled conveniently. All software was coded directly in assembly language. Instructions

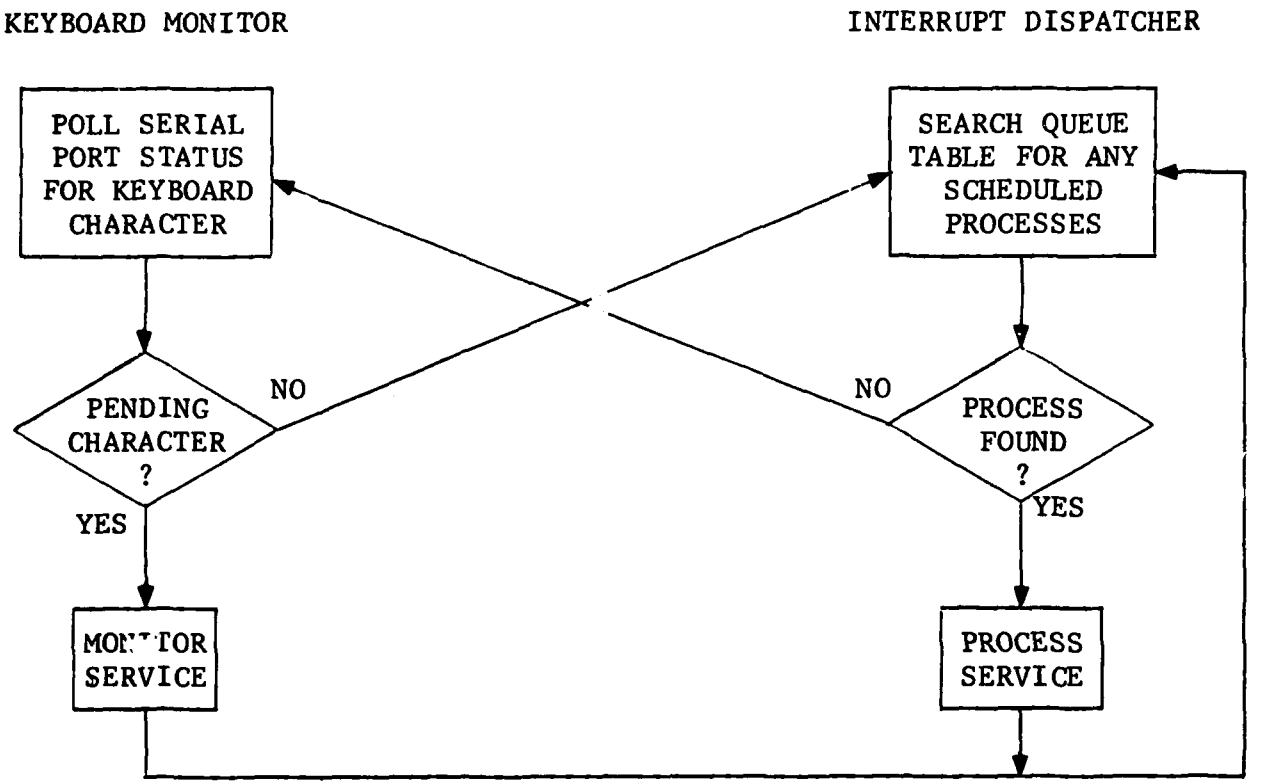


Figure 2.10 Top-Level Software Loop

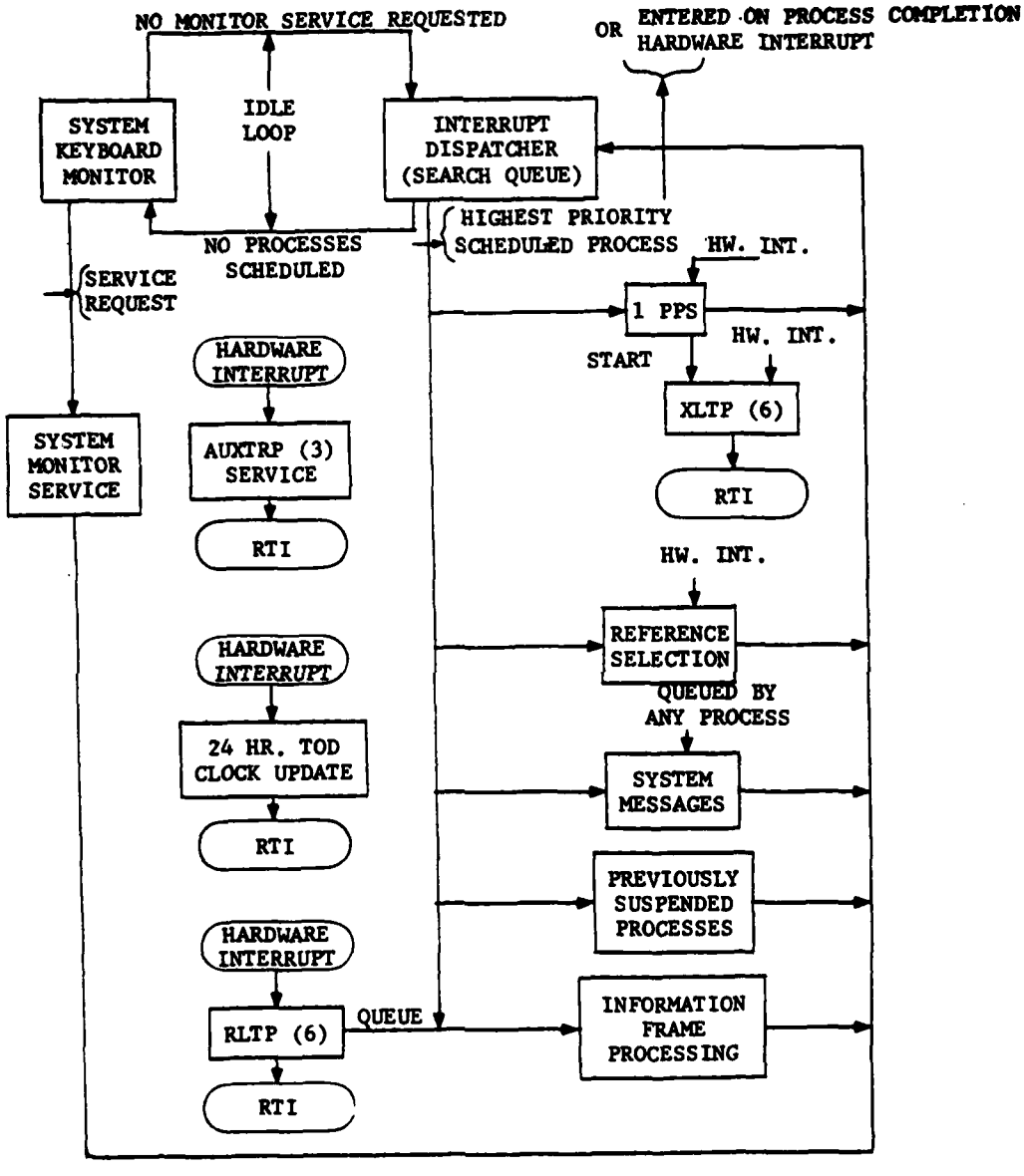
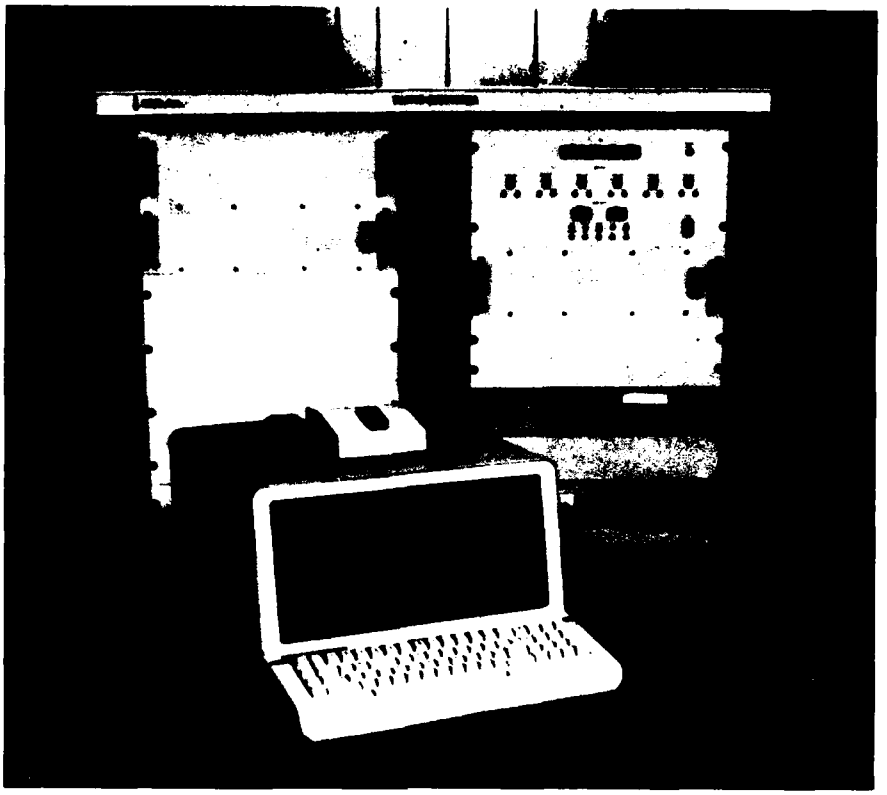
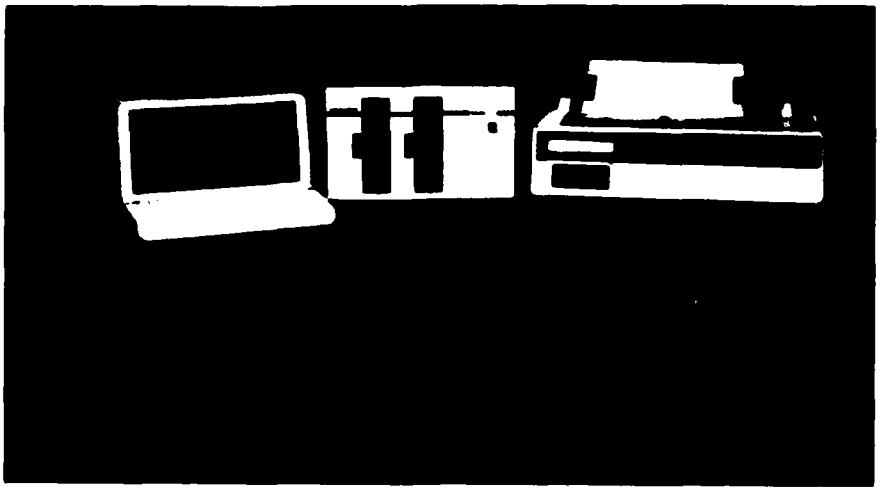


Figure 2.11 Control Flow for Node Control Computer Software Modules



(a) Timing Subsystem with Development System and PROM Programmer



(b) Development System with Disk Drive and Printer

Figure 2.12 Microcomputer Development System

and addressing modes are that of the Motorola 6800 microprocessor family. Included with the development system was an In-Circuit Emulator (ICE) package designed with an emulator card and a cable attached to a probe which plugs in directly to the socket of the removed microprocessor. The development station may be instructed to emulate the 6800 microprocessor functions. Trace, break, single step and the ability to view the internal states of the micro further simplified debugging tasks.

The software development scheme as shown in Figure 2.13 clarifies the technique used to create and modify programs. Once modular section tasks are defined, an assembly language source file (or many source files) is assembled and linked with other program sections. These sections are positioned to the memory locations actually used in the Timing Subsystem. Once loaded into the microcomputer memory, the binary object code is copied into ROM (actually EPROM) exactly as it appears in the development system. Intermediate debugging was aided by using the emulator feature (as described earlier) thus avoiding repeated ROM erase-burn cycles.

2.2.2 Development Station as Network Controller

The network controller's role is to set up an experiment by means of parameter transfers to the TS's, and then become a passive monitor. Resync and reorganization tasks are handled exclusively by the TS's. The controller/TS interaction is designed so that sets of parameters in the disk files may be downloaded to the remote TS's, thereby avoiding the necessity of travel by personnel to unattended sites merely to change a switch setting. As far as performance monitoring is concerned, various status, measurement, and error variables will be continually broadcast in an unreserved portion of the TRIP's and, by means of a suitable routing scheme, will eventually find their way to the network controller.

The essence of the approach, then, is to provide a central control and monitoring function in the network to set up and oversee the three Timing Subsystems. This unit will plug into any one of the TS's and yet be capable of acquiring data or interrogating any of the remaining TS's which will normally be at remote sites. The controller, although capable of stand-alone operation for file handling, editing, and assembly, will

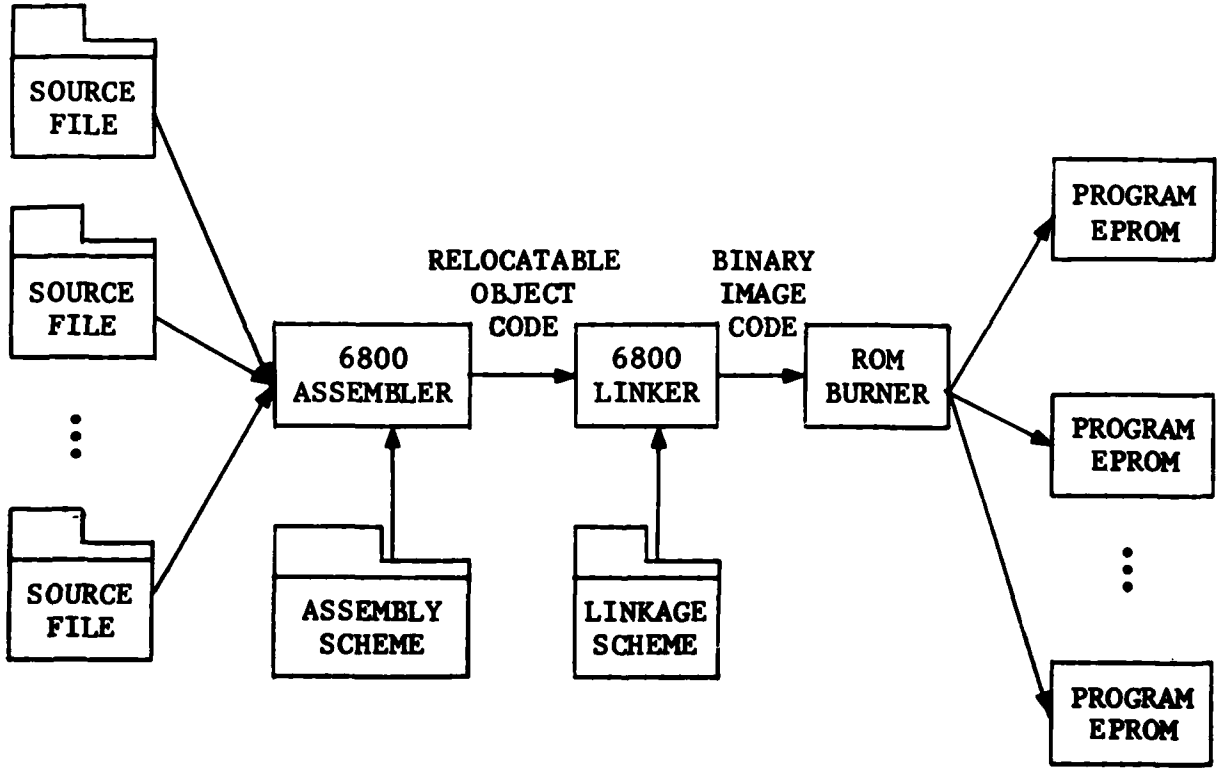


Figure 2.13 Software Development Cycle

be considered as an integral part of the TEST Bed network. Data files will be stored on the disks with parameter entries in the files selected to represent a given network synchronization technique and TS operational mode. Network initialization parameters may be taken from the disk file and transferred to the TS via the RS-232C control port. This technique essentially mimics operator keystrokes but does so at a much higher rate.

Performance assessment data is gathered and maintained by each TS from the past 24 hours of operation. Data transfer from the node may be requested by the operator through a printing terminal or the development station connected to that node.

Although a network management scheme was not implemented, provisions for incorporating node management through TRIP's already exists. Using such a technique, the network controller would pass setup and parameter information to each node from a central location. Each TS would be assigned a reference number and would interpret management data intended only for the local node. Additionally, performance assessment results would be sent from all nodes to arrive at the network controller.

For this program, a single telephone interface was set up at each site using the data couplers provided by the Frequency Measurement Terminals. Nodal management, setup, and parameter transfers were accomplished by accessing each TS individually. Through this technique all control and monitoring functions were handled from a single location. This was appropriate for a smaller network but perhaps a larger network would benefit from a node management protocol gaining TS control through TRIP exchanges sourced from a central location.

REFERENCES

[2.1] CNR, Inc., "Timing Subsystem Development Computer Program Manual", under Contract No. F30602-78-C-0287, September 1981.

[2.2] Motorola, Inc., M6800 Programming Reference Manual, 1976.

[2.3] Advanced Micro Devices, Inc., Am9511 Arithmetic Processor, 1978.

[2.4] CNR, Inc., "Timing Subsystem Development Design Plan", under Contract No. F30602-78-C-0287, March 1979.

[2.5] Hewlett-Packard, Cesium Beam Frequency Standard Training Manual, 1966.

SECTION 3

TEST BED

Originally, four Timing Subsystem prototypes were to be built and tested in several small networks representing both loop (delta) and tandem configurations. These subsystems would, ideally, have been placed at four distinct sites and interconnected with at least one redundant link to allow comparison of clock performance under realistic conditions. However, in the effort of minimizing hardware expenses, it was agreed that only three Timing Subsystems would be built. This limited the variety of network configurations possible although the use of both TROPO and LOS microwave paths to support a timing function could still be accomplished.

The Time Reference Distribution techniques were intended to be advantageous in a larger network where link redundancy and closed loop timing paths (contributing to potential network instability) are likely to exist. Clearly, in a three-node network, the candidate timing techniques would be expected to behave similarly if not identically insofar as our measurement capabilities could detect (with the exception of independent clocks). With these thoughts in mind, we were forced to dismiss the idea of rigorously testing each of the timing technique candidates. Instead, we emphasized the importance of developing a Timing Subsystem capable of supporting the measurement and link termination duties required as well as possessing a great deal of flexibility (due largely to its programmable nature) in the field. However, even limited exposure to the network synchronization experiments performed provided much information and helped to clarify potential problems at the system level. This topic is explored in further detail in Section 6.

A small network of microwave and troposcatter links was configured at RADC, Rome, NY. Here we briefly review the equipment and other resources available at the site installations. In addition, we describe the particular communication links and associated equipment used during the field test phase of this program. First, we offer a review of the events and selection processes that led to the final network used.

The RADC test sites include both line-of-sight microwave and troposcatter facilities. Enough atomic clocks, digital modems, radio equipment and test equipment was kept at each site to support the test effort. The site selection process was influenced more by the type of radio link (i.e., microwave, TROPO) and the operational status of communications equipment than by the availability of support (i.e., test instruments) gear. However, it seemed wise to include both LOS microwave and troposcatter links in our experiments especially since a previous study by CNR, Inc., [3.1] had sufficiently demonstrated that supporting a timing function over a fading channel was feasible. We intended using a TROPO channel for an internode link. At the time, the Verona to Youngstown TROPO path was available. This link was supported by the AN/TRC-132A radio set and quad diversity DAR-IV digital modem. Since this was the only TROPO path available, a tandem network was the only choice for network configuration.

The selection of microwave links involved a few more factors. Originally, two Timing Subsystems were installed at Griffiss AFB to allow the configuration of a loop or delta network from Griffiss to Stockbridge to Verona to Griffiss. In fact, this proposed network also included an up-down satellite link between the nodes at GAFB. However, the satellite radio set had suffered a blown klystron shortly before our arrival and a new tube would take months to be delivered. The satellite link was subsequently scratched from the test plan. After inspecting site equipment and reviewing operational status of radios and modems, it was determined that RADC facilities could provide two microwave links. The first link was an 8 kHz LOS routed between Verona and GAFB (Building 3) through a repeat at Stockbridge. The second was a direct 14 GHz link between Verona and GAFB (Building 3) using Terracom TCM-608B commercial equipment. This more recently installed wideband radio set was not operational at experiment time so in order to test the Timing Subsystems in a tandem network, one of the two TS's at GAFB was shipped to the Youngstown site. No timing experiments were performed with a delta style network. This decision was made with respect to the following factors:

- The satellite link would not be available for use during the experimental tests. This eliminated the possibility of forming a delta network with radio links. Although a direct wire connection could be

used between the nodes at GAFB, it would be of little value since the satellite link total transit time would be on the order of 250 ms and link characteristics would be of great interest if it were to support a timing function.

- It was not clear when the TCM-608B radio terminals would become operational. Several months had already elapsed which were occupied with equipment shakedown and delay calibration tests (see Section 4) while the faulty equipment was serviced. A wait and see attitude was adopted for a short time, however, it soon came down to a simple choice. In the effort of separating all nodes to different geographical locations, it was imperative that one of the subsystems be removed from GAFB and installed at Youngstown (at one end of the TROPO link). This required a commitment to abandon any delta network testing. Given the choice, a tandem network was preferred so a subsystem was shipped there. Additionally, if the TCM-608B radio set did become operational, it could be used as a redundant GAFB to Verona link. Since its path was direct vs. routed through Stockbridge, a different propagation delay time could be expected as compared to the GAFB-Stockbridge-Verona microwave link.

The final network configuration is shown in Figure 3.1. The network consisted of a three-node tandem configuration with one TROPO and one LOS microwave link. The Verona test site was the middle node. This is the only network in which timing experiments were conducted.

3.1 Tandem Network

The previous discussion described how equipment availability reduced the testing and limited the network configuration possibilities to a three-node, two-link tandem network. Figure 3.2 shows the layout of this network. Note that the center node is the Verona test site. Also, link control functions were carried out through public telephone lines as depicted. In this subsection, we describe the equipment involved with both the troposcatter and microwave radio links.

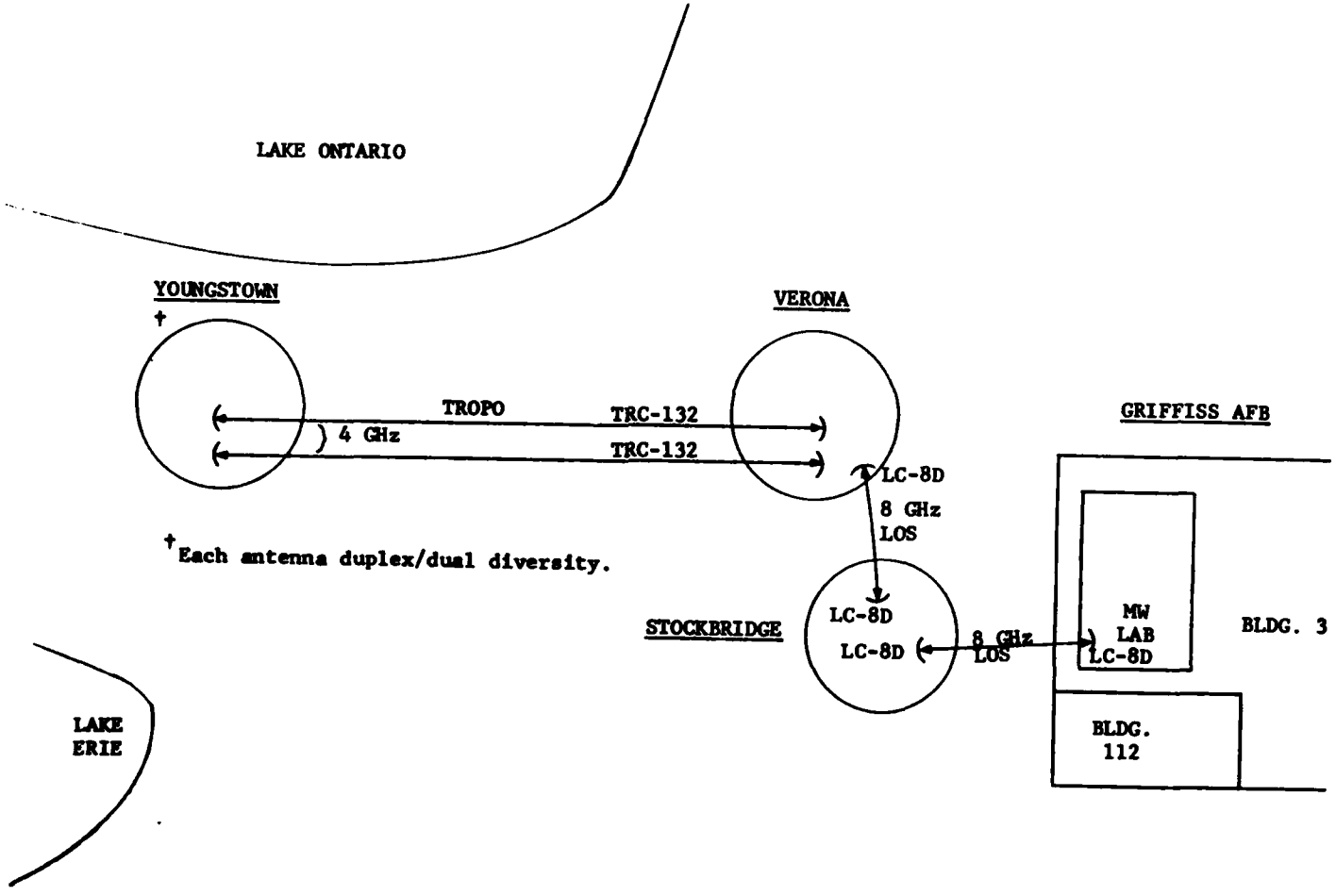


Figure 3.1 RADC Test Sites

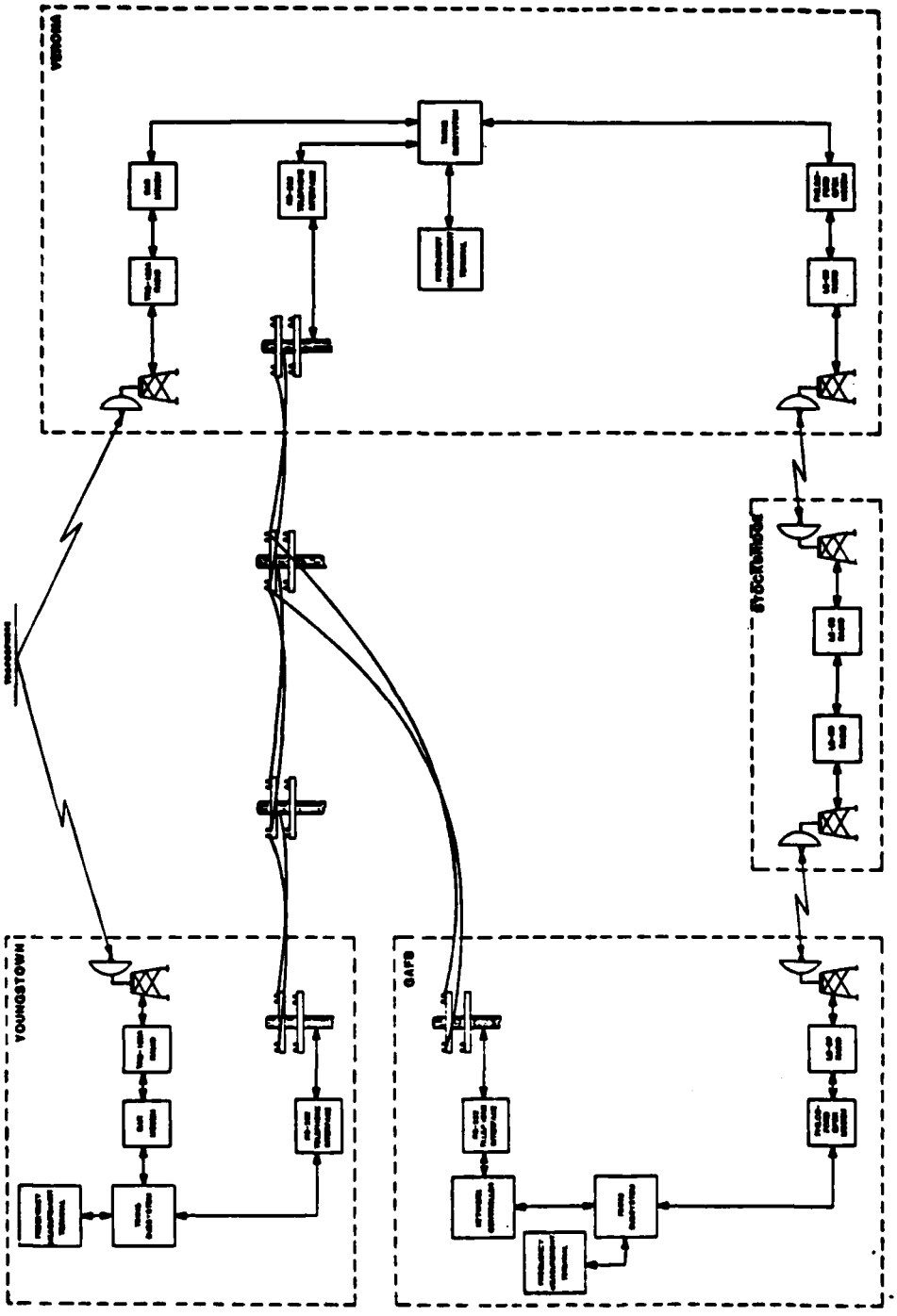


Figure 3.2 Test Bed Tandem Network

3.2 Link Configuration

3.2.1 GAFB-Stockbridge-Verona LOS Link

This microwave link operates at 8 GHz using Philco Ford modems (Quaternary Baseband) [3.2] [3.3] and radios (LC-8D) Stockbridge is an IF repeat stage only and no modems are used. A direct link between GAFB and Verona (14 GHz TCM-608B radio set) did not become operational during the test program so it is not considered here although Figures 3.3 and 3.4 show the Philco-Ford QPSK microwave modems connected to the Timing Subsystems implying that such a link was used, these connections were made to evaluate equipment delays as detailed in Section 4.

Dish-to-dish slant range path length surveys were performed in summer 1977 to re-establish site locations [3.1] [3.4]. Although this information is not necessary for frequency alignment tests, absolute clock (phase) alignment requires an accurate estimate of propagation and equipment delays. Figure 3.3 depicts the microwave range path distances.

Note that the total path length is about 25.7 miles, 17.8 miles from GAFB to Stockbridge and 7.9 miles from Stockbridge to Verona. The corresponding atmospheric signal delay is approximately 138 μs.

It should be noted that although this is a two-frequency, full-duplex link, only simplex operation was available (Verona to GAFB). This condition remained throughout the testing period despite efforts by site personnel to find the problem.

The Quaternary Baseband Modem can be divided into two major sections; a transmitter section and a receiver section. The transmitter section includes all the circuits necessary for the transformation of a binary signal into a four-level baseband waveform. The receiver section comprises all of the circuits necessary to convert a four level baseband waveform into a decoded and regenerated binary data signal. A block diagram illustrating the interrelationship of these two major sections with each other and with the microwave radios is presented in Figure 3.4.

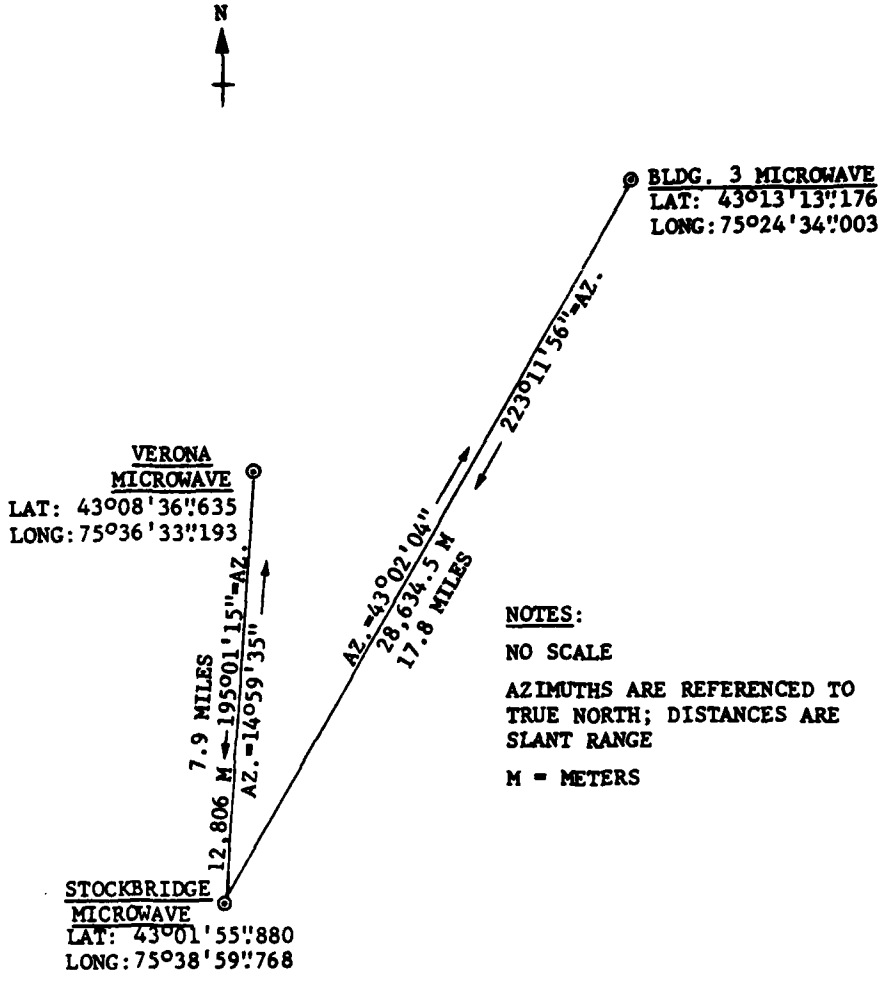


Figure 3.3 Microwave Tower Survey Points (from [3.1])
(Stockbridge, Verona, Bldg. 3)

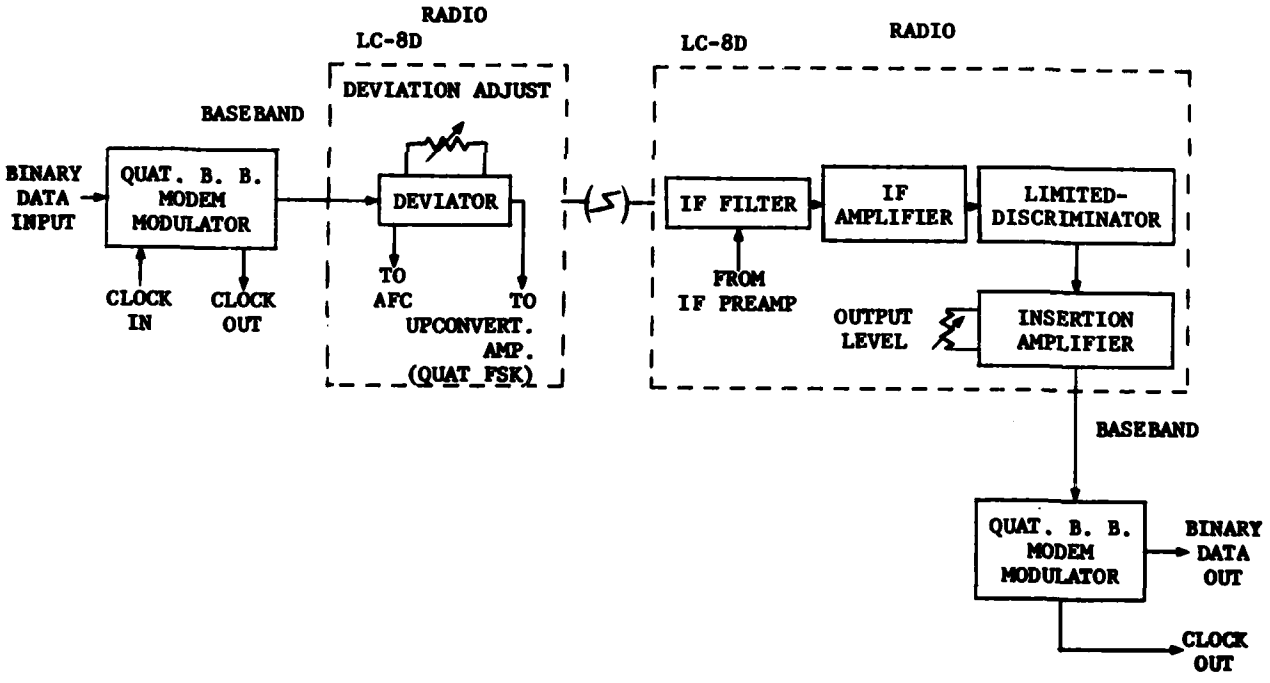


Figure 3.4 Normal Connection of Quaternary Baseband Modem to Microwave Radios

Quaternary Baseband Modem is designed to interface at baseband with a Philco-Ford LC-8D or similar FDM type microwave radio. The modem is basically an AM modulator and demodulator which generates and receives a baseband four-level 1 volt p-p signal. When interfaced with FDM type microwave radios, the AM modulator produces quaternary frequency shift keyed modulation of the carrier signal.

All external connections (except power) to the Modem are made at the BNC connectors on the front of the module. No modifications to the radio equipment were required for achieving satisfactory performance.

3.2.2 Verona-Youngstown TROPO Link

This test range is comprised of two test sites at Youngstown and Verona. One quadruple-diversity AN/TRC-132A radio set is installed at each site. This 4.4 - 5.0 GHz (C-Band) radio set can provide full duplex operation. The path length is approximately 168 miles so typical propagation delay would be about 910 μs.

A detailed layout of the AN/TRC-132 equipment at Youngstown is shown in Figure 3.5. This diagram shows the interconnections between shelters as well as each of the functional blocks in the system.

A Raytheon DAR-IV high-speed digital TROPO modem was used at each end of the link to provide efficient megabit data transmission. The DAR (Distortion Adaptive Receiver) modem technique developed by Raytheon provides several unique features. Among these, are simple QPSK modulation, adaptive matched filter detection, optimum path diversity combining and optimum in-band gain. The modem used a 70 MHz IF to carry an analog order wire signal and one or two asynchronous 15.44 megabit data streams at transmission rates of 1.75 megabits and 3.5 megabits, respectively see [3.5]. The typical modem diversity configurations is shown in Figure 3.6.

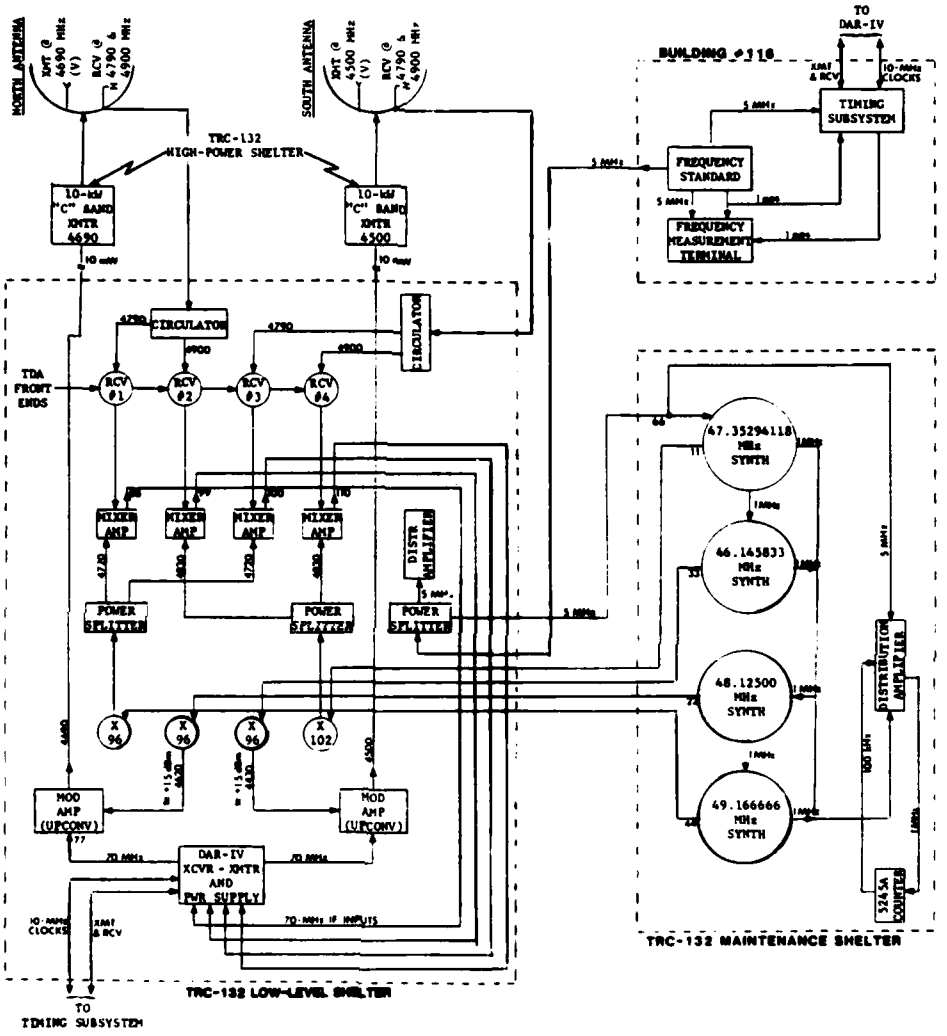


Figure 3.5 Youngstown Troposcatter Facilities (TRC-132)

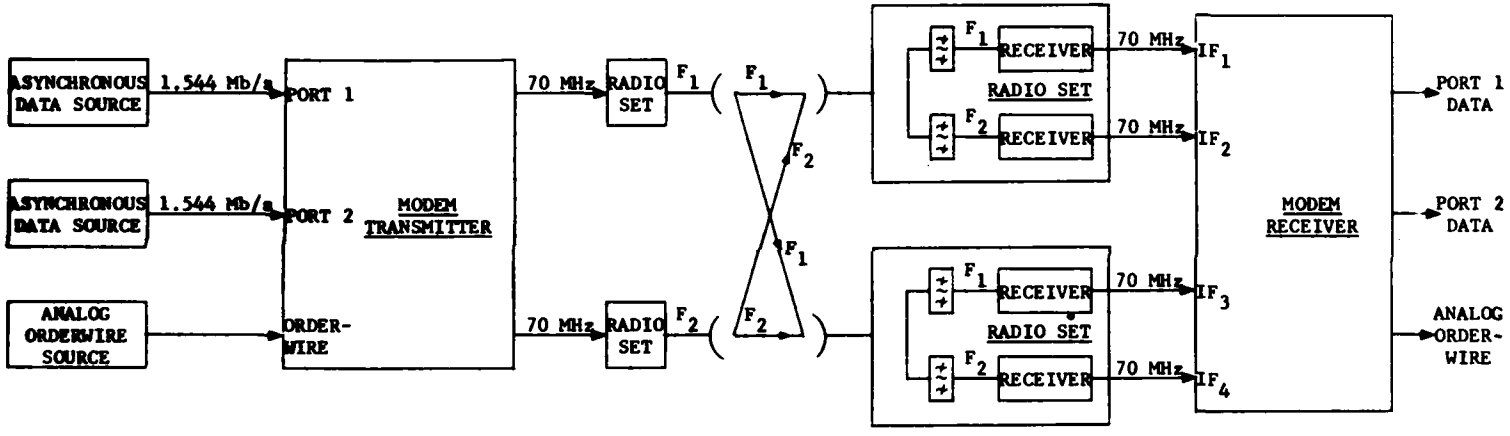


Figure 3.6 Typical Modem Diversity Configuration

3.3 Node Configuration

3.3.1 Timing Subsystem

At each site, the Timing Subsystems were connected to modems and the Frequency Measurement Terminal. At the Youngstown and Verona sites, it was necessary to provide an external frequency source for the TS because these units did not include internal quartz oscillators. The rubidium frequency standard housed in the FMT was used for this purpose as well as providing the frequency source for the FMT measurement capability. In addition, at each site, the FMT was configured to measure and average both LORAN-C and TS adjusted output 1-pps events. This scheme provided the measurement capability needed to verify network performance. Each Timing Subsystem can measure and average up to 3 external 1-pps signals, and as a redundancy measure, rubidium and LORAN-C 1-pps outputs were connected directly to the TS auxiliary TRP ports. It was a simple matter to verify TS tracking performance when using the rubidium 1-pps output as a reference input to the Timing Subsystem. Shakedown tests demonstrated that both the FMT and TS interval measurement and averaging facilities performed as expected.

Figures 3.7, 3.8 and 3.9 depict the equipment connections to the Timing Subsystem. Notice that although the connections to the QPSK LOS modems are shown, the GAFB to Verona (direct) link was not used. However, as Section 4 reveals, the TS data rates were wired to conform to the radio MUX rates should the link be used in future tests.

3.3.2 Network Controller

The Network Controller allows central control and monitoring of each Timing Subsystem within a network. Typically, the operator would choose a timing experiment, enter the parameters at the terminal keyboard and download experiments through a single node. Resync and reorganization tasks would be handled exclusively by the TS's. The essence of this approach is to centralize the setup and monitoring function to avoid unnecessary travel to remote sites merely to change a switch setting. Section 2.2.2 describes the purpose of the Network Controller and the equipment involved.

During software development, it was decided to abandon the idea of committing the microcomputer development system to the

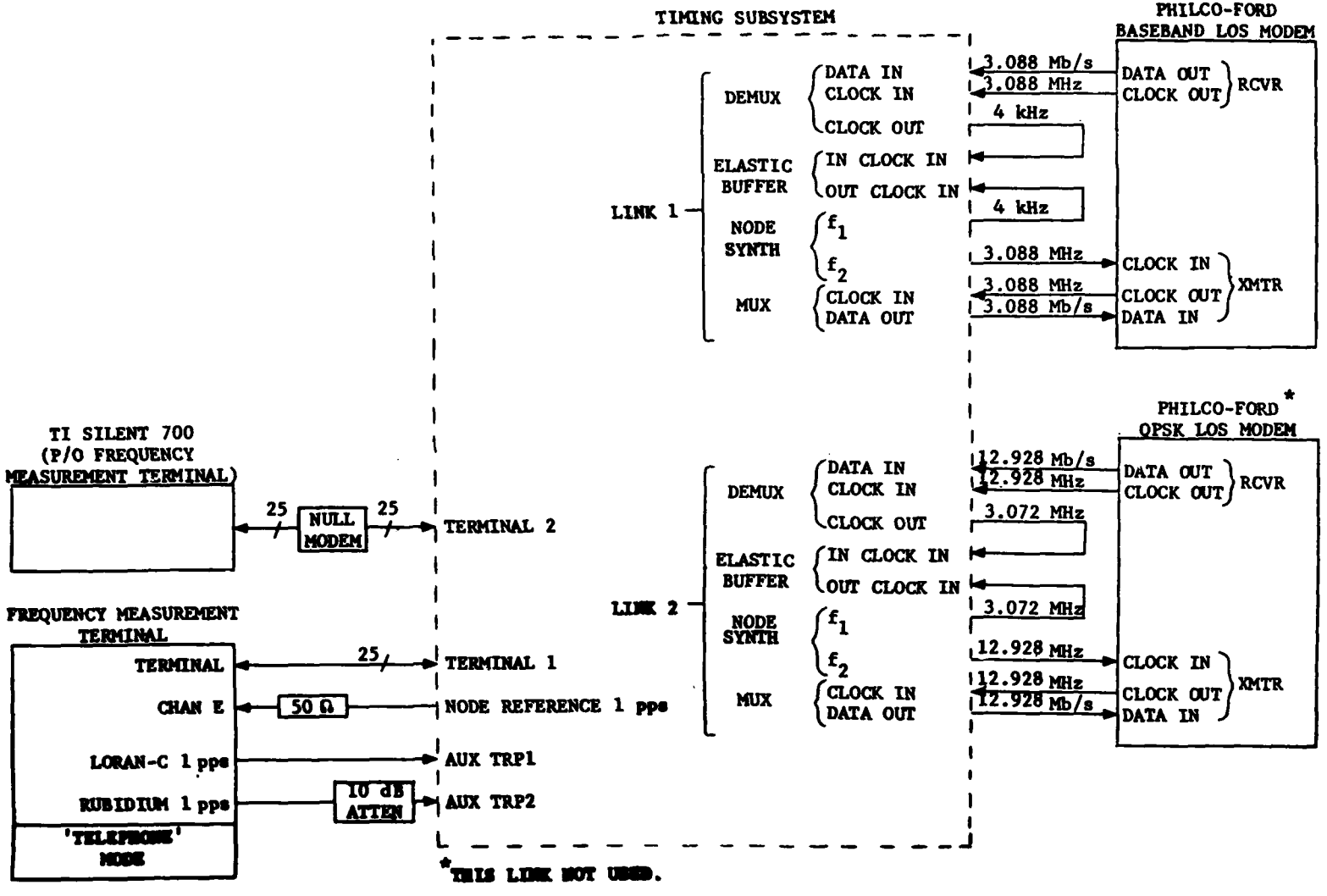


Figure 3.7 Node Configuration (GAFB)

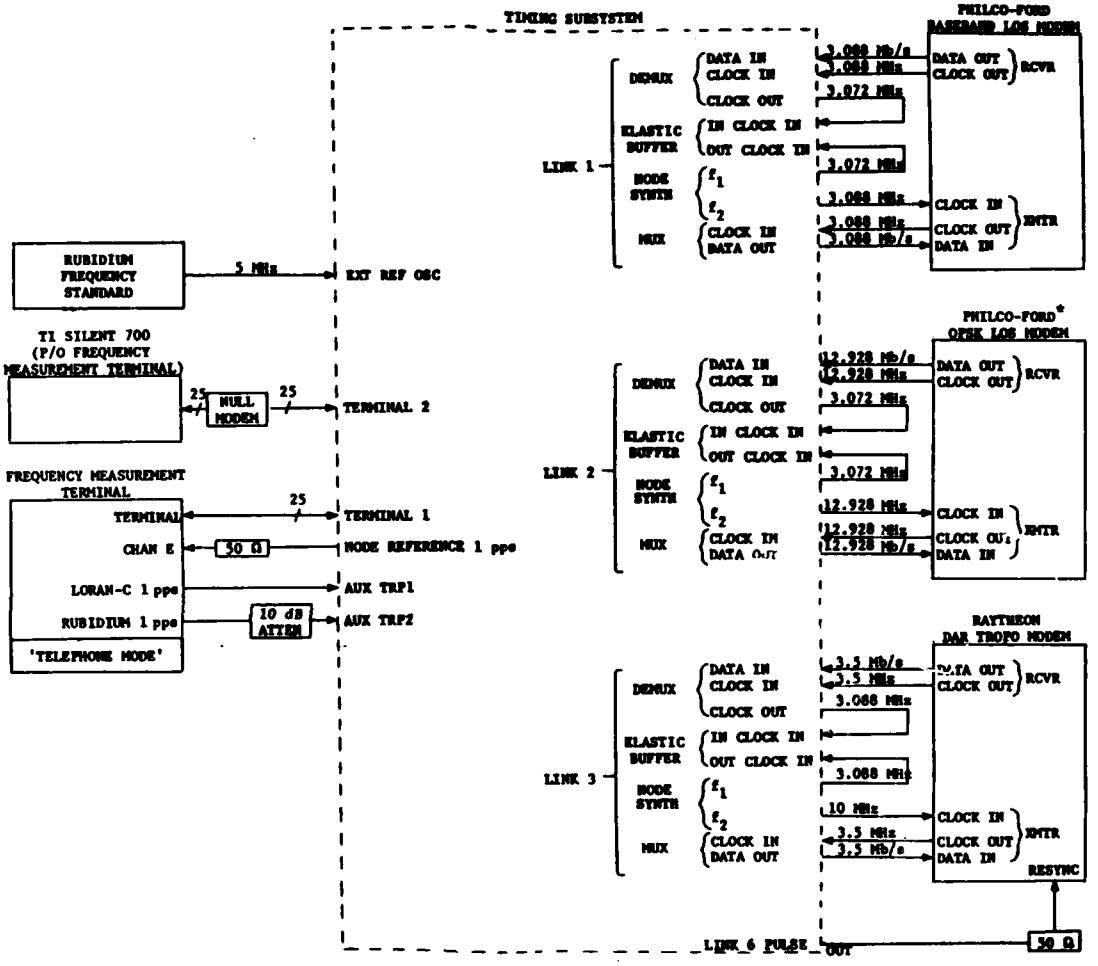


Figure 3.8 Node Configuration (Verona)

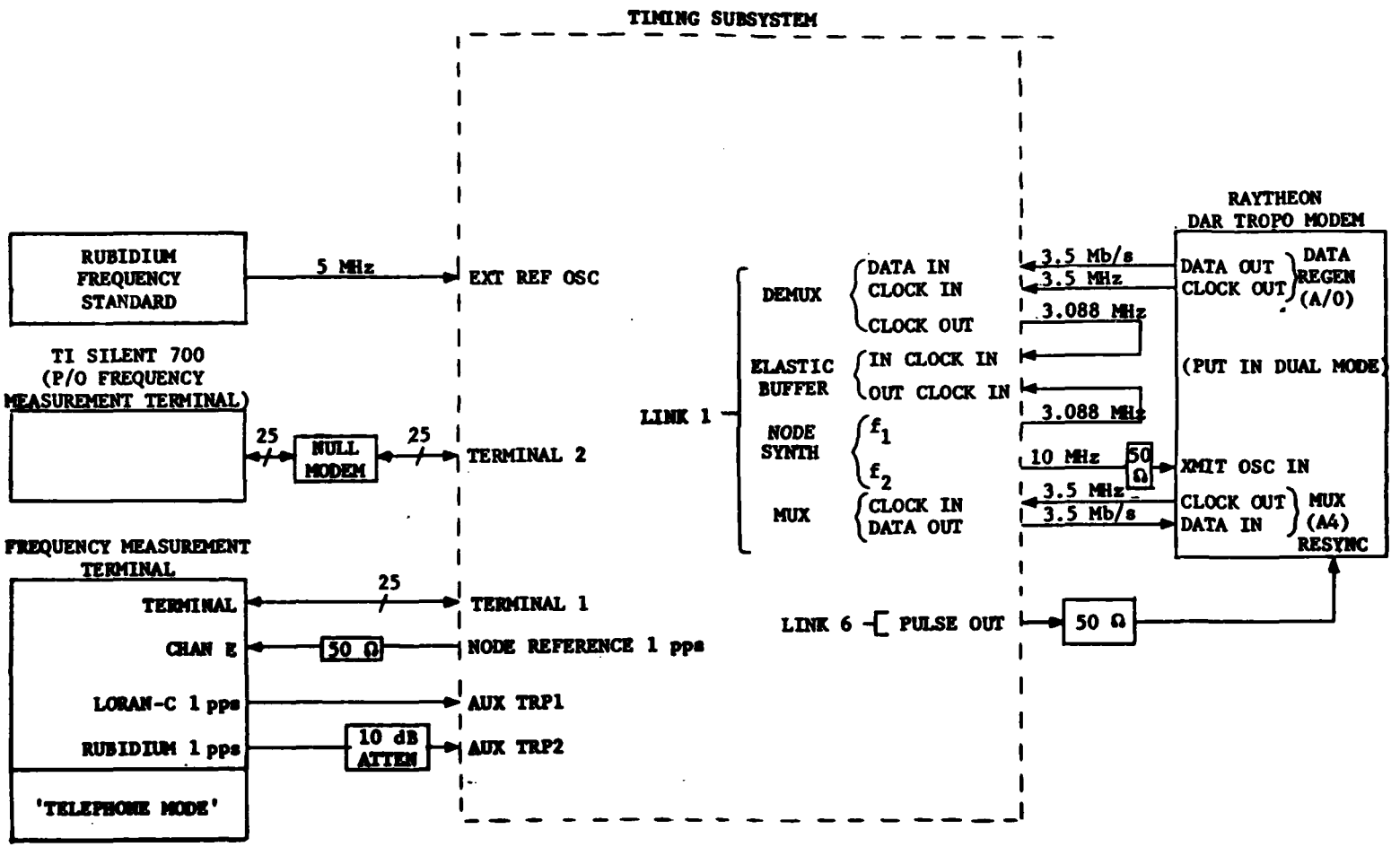


Figure 3.9 Node Configuration (Youngstown)

Network Controller function as originally intended. This decision was based on many factors that became evident during the course of the program. The following paragraphs describe some of the reasons.

First, shortly after the design phase, it was agreed that the use of supervisory and/or nodal management traffic in addition to that needed to support the timing function, would unnecessarily burden the channel by increasing the complexity to the point where actual timing data would seemingly be lost in the midst of a nodal management protocol. Granted, a convenient feature of the Network Controller was that of centralizing network control functions, but the effort of implementing this one feature alone would result in significant increases in software effort from an already large and comprehensive package. Considering it was not a contractually required function, it was agreed to leave this aspect for future considerations; i.e., an advanced development model, and concentrate on Timing Subsystem operational software. Additionally, this represented no great hardship to the success of the experimental program because each TS is in its own right a programmable device with its own simple system monitor and in a small network of three modes, a central monitoring function was not essential.

In fact, a solution was worked out that was nearly as effective and required almost no additional equipment: a small, portable communications terminal was named the Network Controller and carried out its function through the use of commercial telephone lines. This is indicated in the diagram of the tandem network as shown earlier. This was made easier by using the already existing modems and data couplers resident in each of the Frequency Measurement Terminals (FMT) located at each test site. The next subsection describes in more detail the role of the FMT in the experimental program. In this light, TS interrogation was a simple matter of dialing the number for the site FMT and insuring that the TS E/A interface was connected to the FMT as well. An essentially direct connection to the TS could be made from any telephone. Considering the small size of the network and the extra mobility and convenience gained with a portable terminal, network control and test setups were never difficult although occasionally, the telephone lines themselves impeded data traffic. One solution would be to install a higher quality or permanent data line but it was unnecessary for this program.

Figure 3.10 shows the network controller interconnection scheme with a single Timing Subsystem.

A direct cable connection to the Timing Subsystem was used when development engineers were actually located at a site. In effect, the role of Network Controller was reduced to that of an interactive monitor because all control and debugging was performed through a direct connection rather than through internode data communication links. This greatly simplified some of the more mundane tasks of the experimental program such as equipment shakedown and single node performance monitoring when removed from a network. Performance assessment during a network synchronization experiment was accomplished by requested memory dumps of saved averages of clock performance stored at each node. Also, status requests provided a quick method to check on the operation status of a given node during an experiment. Reference [3.6] provides a complete summary of the capabilities of TS monitor software.

3.3.3 Frequency Measurement Terminal

The Frequency Measurement Terminal (FMT) was developed under contract by the National Bureau of Standards, Time and Frequency Division. It is a flexible frequency measurement device incorporating an integral LORAN-C receiver and LORAN-C pulse monitoring equipment, a CPU containing time of day readout, time interval measurement unit as well as a digital modem, serial interface, associated memory, pulse shaping circuits, printing terminal, and finally a rubidium frequency standard. All equipment is housed in a single width rack.

Besides being capable of monitoring LORAN-C or TV Line 10 performance as compared with the local rubidium standard, the FMT was used as an integral part of the general node performance assessment scheme. The FMT has the ability to measure 1pps pulses on as many as 5 input channels compared to the source 1pps pulse provided by the rubidium standard. Therefore, not only may the local rubidium frequency standard be used as a node reference but by connecting the adjustable 1pps output from the Timing Subsystem to the FMT, and in turn, connecting the frequency standard output 1pps directly to the TS (while leaving the FMT source 1pps from the frequency standard intact) for time interval measurement, a redundant TS to rubidium measurement facility is established. This also provides an easy way to compare the TS adjustable output to any other

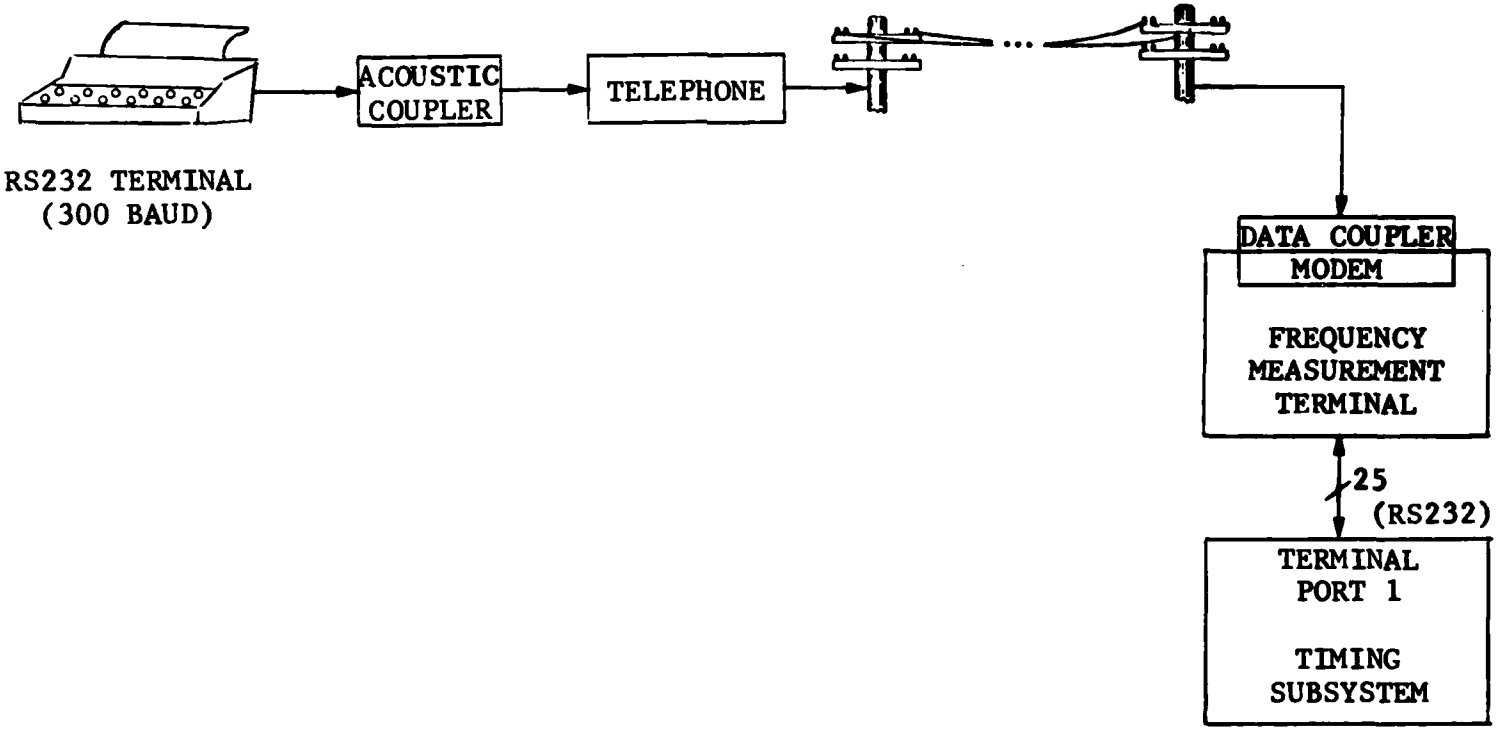


Figure 3.10 Network Controller to Timing Subsystem Interconnection Scheme

externally applied 1-pps signal (such as LORAN-C). Once the relative drift between say, a received LORAN-C pulse and the local rubidium standard is known, then the Timing Subsystem adjustable clock may be compared to the LORAN-C pulse for performance evaluation. This is precisely the technique used during network synchronization test.

The FMT uses an internal time interval counter with a 100-MHz time base to yield a resolution of 10 ns in the least significant digit. Together with a plus or minus one-count ambiguity inherent to the counter itself, other internal factors contribute to an uncertainty of about 50 ns in each individual time interval measurement; but some external factors must be considered also.

The accuracy of FMT calibrations is most certainly limited by the instability of TV and LORAN-C propagation paths. If two terminals are within line-of-sight range of the same TV station, their differential path delay might vary by as much as 20 ns. If the terminals are separated by a greater distance so that a TV microwave distribution path is involved, the differential delay may occasionally change by several hundred microseconds. By comparing the results from three different networks, however, the uncertainty in TV propagation delay can be resolved to within 100 ns generally.

LORAN-C is capable of supporting absolute timing accuracy of about 100 ns over long distances. If differential measurements are made at sites separated by only 400 kilometers or less, the results using LORAN-C are apt to be substantially better.

It is expected that, by proper choice of statistical weighting factors for LORAN-C and TV data, the overall uncertainty in calibrations using the FMT will fall between 10 ns and 100 ns. A more reliable estimate of uncertainty will depend ultimately upon further operating experience with the system and a thorough analysis of actual measurement data. See [3.7].

3.4 Test Bed Master Clock

Each Frequency Measurement Terminal (one located at each of three nodes) receives LORAN-C radio signals from a single source: the Northeast chain master at Seneca, NY. This station with a peak pulse power of 800 kW is located within 120 miles

of each of the receivers at the test sites. Since the LORAN-C receivers in the FMT's were receiving Seneca, its timing pulses would be a convenient, accurate, and traceable network reference to which TS performance may be compared.

The high quality of LORAN-C frequency and time signals is due to a number of things. Each station is controlled by a cesium standard. Careful control and monitoring of the signals by the U.S. Naval Observatory allows a user to achieve rapid, accurate results. Groundwave signals provide state-of-the-art frequency and time calibrations. As is the case with the Test Bed network, groundwave signals may be reliably received at distances of 1500 miles or more for a station of at least 300 kw peak pulse power. For the test program, we were concerned only with groundwave performance.

The ability of the LORAN-C timing receiver to indicate accurate time readings is dependent upon the relative strength of the received signals and the level of the local noise interference. As a result, accuracy deteriorates at receiver locations far away from the stations. For timing purposes, long-term averaging is used to achieve more reliable results. This is precisely the function of the FMT. Up to eight days of 4-hour averages of pulse receive time vs. local time reference (on-site rubidium) at one sample per second, are saved in the processor. Armed with this information, one may easily determine the relative frequency drift between each of the local timing references and the Seneca LORAN-C timing. This is the basis for demonstrating network performance. Therefore, the network frequency standard may be considered to be the cesium beam atomic frequency standard located at Seneca, NY. If desired, frequency drift comparisons may be made directly to NBS standards, in Boulder, Colorado.

LORAN-C is one of the principal methods of intercomparing the atomic standards at NBS, the USNO and the National Research Council in Canada. This scheme is also extended to the European LORAN network and affords a means for the BIH to compare all of the world's main time scales. The results reported for this system of intercomparison are impressive - approaching 1 part in 10^{13} over several months [3.8].

Typical values for groundwave reception over land could easily approach a few parts in 10^{12} for a one-day average. Corrections to LORAN data are provided by the USNO, and the NBS

also monitors and reports daily LORAN phase readings. Users who want very accurate results from LORAN-C must correct the observed data by using the published corrections. This information is available by TWX on a daily basis from the USNO.

For timing, the accuracy of the groundwave at a particular location depends upon several factors that contribute to the errors in the measurements. The approximate errors are:

1. Error in transmitted signal, < 0.2 microsecond.

2. Errors caused by propagation path, up to 0.2 microsecond over water; up to 1 microsecond over land.

3. Receiver error, 0.02 microsecond typical.

4. Errors caused by atmospheric noise and interference, up to 0.5 microsecond for interference. Longer averaging times can be used with noisy signals.

REFERENCES

[3.1] CNR, Inc., "System Timing and Synchronization," Final Report on Contract No. F30602-76-C-0347 with RADC, May 1978.

[3.2] Philco-Ford Corp., Willow Grove, PA, "Microwave Data Transmission Test Program - QPSK Modems," Final Report, November 1974.

[3.3] Philco-Ford Corp., Willow Grove, PA, "Microwave Data Transmission Test Program - Quaternary Baseband Modem," Final Report, November 1974.

[3.4] CNR, Inc., "System Timing and Synchronization Test Plan," Contract No. F30602-76-C-0347 with RADC, January 1977.

[3.5] Raytheon Co., "Operation and Maintenance Manual for Distortion Adaptive Receiver (DAR)," Contract No. F30602-77-C-0008 with RADC, 1977.

[3.6] CNR, Inc., "Timing Subsystem Development Computer Program Manual," Contract No. F30602-78-C-0287 with RADC, September 1981.

[3.7] Frequency Measurement Terminal Instruction Manual, U.S. Dept. of Commerce, National Bureau of Standards, Time and Frequency Division, Boulder, CO, 1977.

[3.8] National Bureau of Standards, "Time and Frequency User's Manual," NBS Technical Note 695, Time and Frequency Division, Boulder, CO, 1977.

SECTION 4

EQUIPMENT DELAY MEASUREMENTS

This section presents the findings of equipment delay measurements performed as part of the equipment shakedown tests at each site prior to network timing experiments. Equipment delay times, as well as path propagation times, must be known or measured in advance for any network timing experiment requiring absolute clock alignment (i.e., zero phase offset). Although not essential to network performance where frequency tracking is the desired result, these measurements further reinforce methods of verfiying system operation.

A word of caution is in order; path and equipment delay reciprocity is a function of both the propagation medium and link transmission equipment. Although recent field experiments have shown that path delay (on the average) may be assumed equal in both directions [4.1], it is wise to measure, or at least know, the delay differential arising from transmission directions as well as the various equipments and frequencies used.

4.1 Equipment Delay Measurement Procedures

Briefly described is the method used to obtain precise delay information of both the Timing Subsystem itself as well as any external equipment, such as modems and radios.

The Timing Subsystem has the capability to measure the time difference between outgoing and incoming Time Reference Pulses (TRP's) that leave or enter the TS at the link termination points. The node control computer extracts timing information from bit patterns on the serial bit streams to and from the TS. An error computation is performed, and the TS determines the elapsed time from a transmitted TRP to a corresponding received TRP. Through this mechanism, TS as well as external equipment delays may be determined. Measurement resolution is ± 10 ns as dictated by the 100-MHz counters on the time interval measurement board.

4.2 Timing Subsystem Equipment Delay

This subsection describes steps necessary to measure equipment delay times of the Timing Subsystem and any interconnected modems or radios in the data path. For simplicity, only connections to link 1 are detailed. However, be reminded that for each link used, all lower numbered links must either be in use or connected back-to-back; that is, if link 2 only is to be used, link 1 must be strapped back-to-back for proper operation of link 2. This is necessary because each link's transmit interrupt sequence starts the next link's sequence. (See Section 3.2.3 of [4.2] for more information on link transmit service.)

Connecting a communications path to the Timing Subsystem is a straightforward matter. The node synthesizers are wired to provide the data rates described in Table 4-1. These are the data rates used in the tandem network configured (also shown in this table) during the field test portion of this program.

To find the equipment delay through a link, refer to Figure 4.1 for the recommended equipment interconnection scheme. Figure 4.2 details link connections (back panel) required to measure equipment delay of the TS itself. By inspecting the nodal error terms, equipment delay may be found as a 32-bit fixed-point (hexadecimal) number where one count equals 10 ns (i.e., normalized to 10^{-8} seconds). See [4.2] and the clock data TRIP format shown in Section 2 to locate the raw bit patterns used to interval computation. The Timing Subsystem automatically saves a series of elapsed time delay measurements for inspection at the operator's convenience. Again, Section 4.3 of [4.2] describes the detailed data-logging procedures. They are omitted here but a summary of TS back-to-back equipment delays is in Table 4-2.

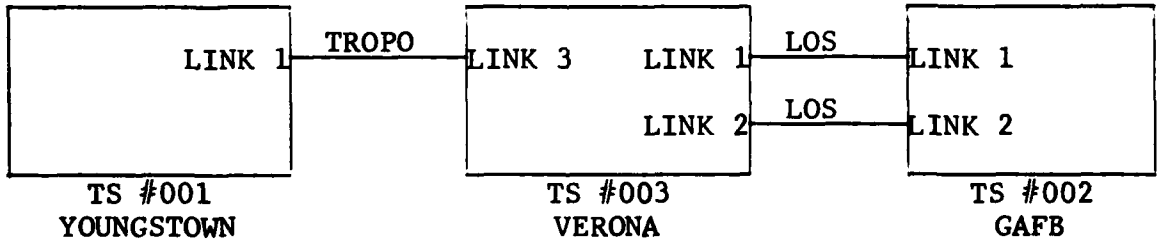
Note, for instance, that each of the measured back-to-back Timing Subsystem delays seems to hover around the 500-μs mark. This corresponds well to an expected value since the 4-kHz (250-μs period) data rate determines the bit-detection times. That is, the round-trip delays as shown in the table are made up of four components: one bit period transmit time, one bit period receive time, mux time, and demux time for a typical value (LOS) of 250 μs, 250 μs, 0.5 μs, and 0.5 μs, respectively. Other

TABLE 4-1

SUMMARY OF WIRED LINK MUX/DEMUX RATES

	TS #001 (Youngstown)	TS #002 (GAFB)	TS #003 (Verona)
Link 1	3.5 Mb/s (TROPO)	3.088 Mb/s (LOS)	3.088 Mb/s (LOS)
Link 2	3.088 Mb/s (LOS)	12.928 Mb/s (LOS)	12.928 Mb/s (LOS)
Link 3	4.0 kb/s (SAT)	4.0 kb/s (SAT)	3.5 Mb/s (TROPO)

SAMPLE NETWORK (TANDEM)



Note: All link terminations are 78Ω-balanced NRZ format.

TS #002 to TS #003 Link 2 (LOS) - Not Used
TS #001 to TS #002 Link 3 (SAT) - Not Used

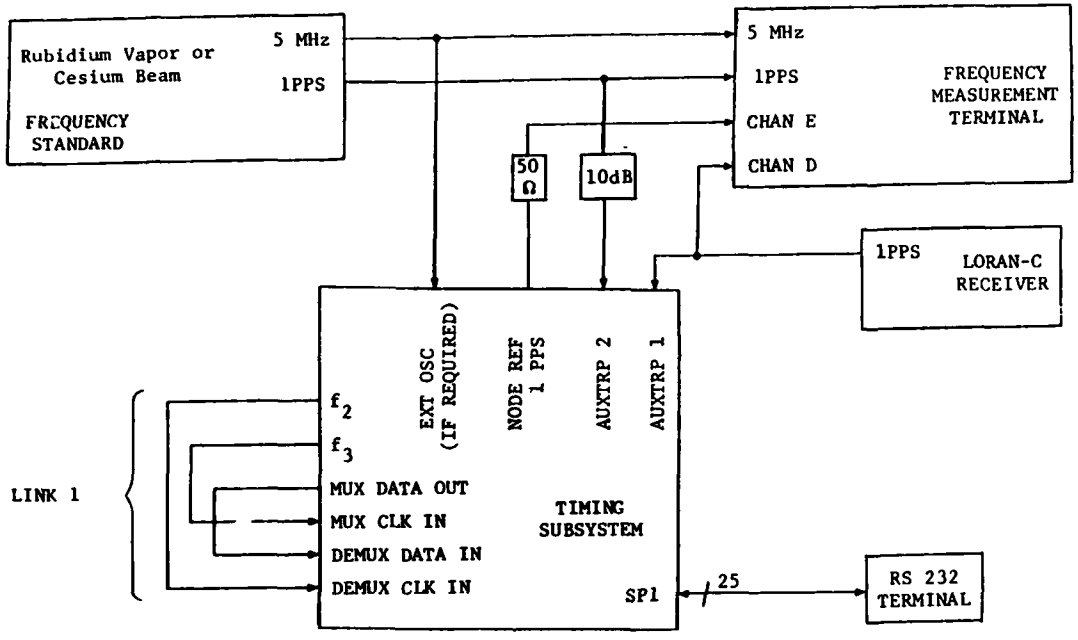


Figure 4.1 Equipment Connections for Link 1 Equipment Delay Measurement

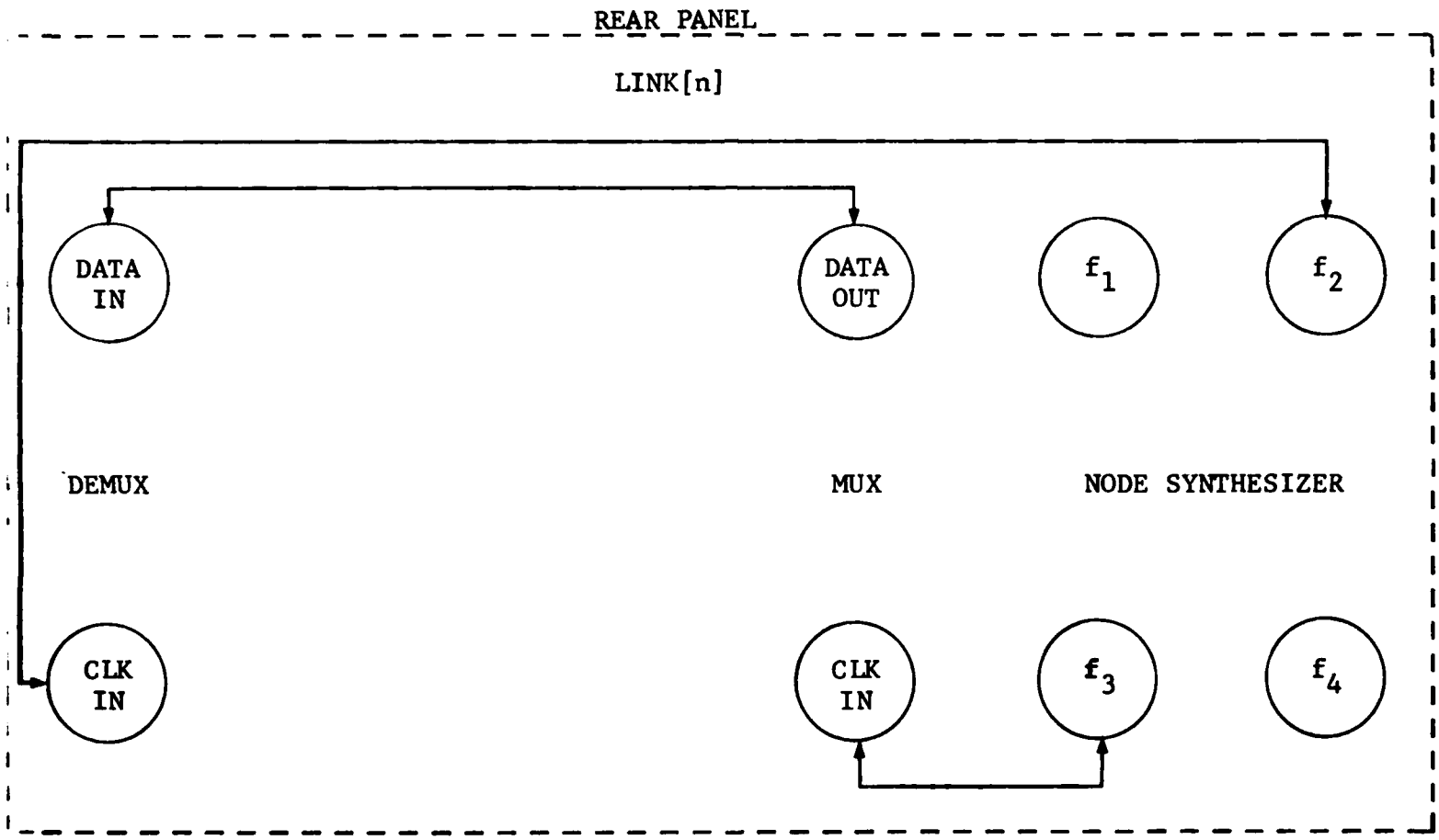


Figure 4.2 Link Interconnections for TS Back-to-Back Operation

TABLE 4-2

SUMMARY OF TIMING SUBSYSTEM EQUIPMENT DELAY (LOOP BACK)

	Link 1		Link 2		Link 3	
	Rate/Type	TS Delay	Rate/Type	TS Delay	Rate/Type	TS Delay
TS #001 (Youngstown)	3.5 Mb/s (TROPO)	507.07 μs (With Modem)	3.088 Mb/s (LOS)	Not Used	4.0 kb/s (SAT)	Not Used
TS #002 (GAFB)	3.088 Mb/s (LOS)	500.99 μs	12.928 Mb/s (LOS)	500.29 μs	4.0 kb/s (SAT)	Not Used
TS #003 (Verona)	3.088 Mb/s (LOS)	501.00 μs	12.928 Mb/s (LOS)	500.27 μs	3.5 kb/s (SAT)	507.20 μs (With Modem)

Figure 5.3 Self-Reference Test Setup

Mission Bit Stream (MBS) rates show slight changes in delay, as seen in Table 4-2. All 4-kHz data (at TS) rates are determined by the node synthesizer which is phase-locked to the node standard 5-MHz frequency source.

4.3 Line-of-Sight Equipment Delay

The single LOS route included two Philco-Ford baseband modems and four Philco-Ford LC-8D microwave radios. An IF repeat station was configured at Stockbridge. Total path length was about 25.7 miles.

In order to measure equipment delays throughout the link, each portion was isolated. Figure 4.3 shows the LOS back-to-back setup including modems and radios. Actually, three interconnection schemes were used to determine individual equipment delays at each site. First, the Timing Subsystem delay was measured. Second, the modem was connected, and TS + modem delay was measured. Third, the radio set was added and TS + modem + radio delay was measured. Finally, modem and radio (including associated cabling) delays were extracted by subtraction. The dotted lines in Figure 4.3 show the stages of interconnection used to isolate equipment delay. Remember, the sum total of TS + modem + radio delay includes both transmit and receive sections; any difference in delay will result in a differential that would manifest itself as a phase offset when performing double-ended measurements. For most single-ended schemes, frequency averaging is the desired result; therefore, equipment delay compensations need not be included.

4.3.1 LOS Modem Delay

Back-to-back delay tests were carried out for the Philco-Ford Quaternary Baseband Modems [4.3] when connected to the Timing Subsystem.

First, it should be recognized that the Timing Subsystem requires a transmit clock from the modem for its own transmit mux. However, it was found that the modem lost receiver sync whenever the Timing Subsystem was not transmitting data; that is, no provision was made to provide bit transitions between TRIP bursts. It was decided to incorporate a PN generator at each transmit mux in the TS to keep the modem receiver in-lock. Subsequently, this simple modification was wired in and the problem was eliminated.

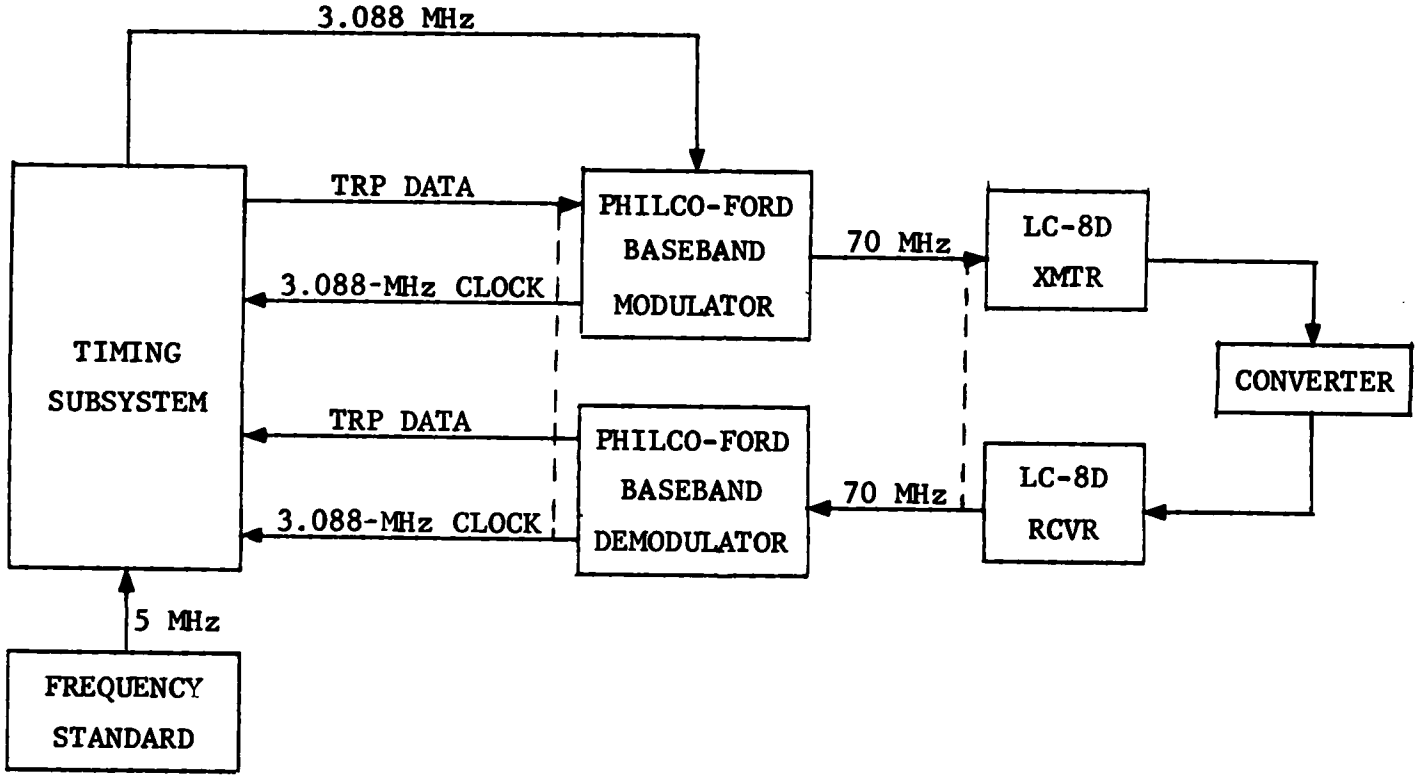


Figure 4.3 LOS Back-to-Back Test Setup for Delay Measurement

Secondly, there are clock-phasing controls on the front of the modem, one for the transmit section and one for the receive section. It is known that a timing variation of tens of nanoseconds can be introduced by these controls within the range of satisfactory modem performance and, overall, a whole bit of variation is possible. Once the equipment delay has been measured, the knob setting must remain intact for all subsequent timing technique tests.

The measurements for both the GAFB and Verona equipment are shown in Table 4-3. The Timing Subsystem delay component was measured separately and subtracted from back-to-back tests with the modem transmitter connected directly to the receiver. The resulting delay values are shown in Table 4-3.

No delay uncertainty was anticipated for this equipment because it does not include an internal multiplexer. Measurement resolution was 10 ns.

4.3.2 LOS Radio Delay

Delay measurements were carried out on the LOS radios (Philco-Ford LC-8D) at the Griffiss and Verona sites. Although Stockbridge was used as an IF repeat station for the microwave link, a measurement capability was not available there; therefore, delay figures based on measurements from the other radios and [4.1] were used.

The equipment configuration for the GAFB radio is identical to that shown in Figure 4.3 described earlier. Extracting radio delay required connecting both the TS and modem, whose delays were previously determined, to the radio. Then, the measured delay of all of the equipment, less that of the TS and modem, left pure radio delay.

Since the measurements for this program agreed quite well with those of a previous CNR effort, presented here are the data for the GAFB, Verona, and Stockbridge sites in Table 4-4. In that program, the test setup for the Verona and Stockbridge radios involved injecting baseband tones into the modulator. The tones ranged from 50 kHz to 1500 kHz. The loopback was at the RF output level. Both A and B side delays are included. For the GAFB radio, the measurement resolution was 10 ns, as dictated by the TS.

TABLE 4-3

DELAY MEASUREMENTS FOR PHILCO-FORD BASEBAND MODEM

	Modem #1 (GAFB) TS #001	Modem #2 (Verona) TS #003
Data Rate	3.088 Mb/s	3.088 Mb/s
Scrambler	Off	Off
Receiver Timing Adjust	Fully CCW	Fully CCW
Transmit Timing Adjust	Fully CCW	Fully CCW
TS + Modem	505.02 μs	505.06 μs
Modem	4.03 μs *	4.05 μs *

*Any cabling between the modem and TS was included as part of the modem delay.

TABLE 4-4

GAFB, VERONA, STOCKBRIDGE LC-8D RADIO DELAY MEASURED AT BASEBAND INTERFACE

	Radio Section	Frequencies	Baseband Frequency	RF Back-to-Back Delay	Comments
GAFB	A Side:	TX - 8.290 GHz RX - 7.965 GHz	3088 kHz	500 ns	Test using Timing Subsystem as measuring device
	B Side:	TX - 8.390 GHz RX - 8.075 GHz	3088 kHz	500 ns	
Stockbridge	A Side:	TX - 7.965 GHz RX - 8.290 GHz	1500 kHz	437 ns	Previous CNR effort. Baseband tones injected into modulator. Time interval counter measured delay.[4.2]
	B Side:	TX - 8.390 GHz RX - 8.075 GHz	1500 kHz	431 ns	
Verona	A Side:	TX - 8.075 GHz RX - 8.390 GHz	1500 kHz	445 ns	
	B Side:	TX - 8.075 GHz RX - 8.390 GHz	1500 kHz	481 ns	

4.4 Troposcatter Equipment Delay

The TROPO route from Youngstown to Verona was configured as a full-duplex C-band link using DAR-IV modems and the AN/TRC-132A radio set. The equipment configuration at each site was identical.

First, the delay through the modem in loopback mode was investigated. Internal modulator/demodulator data streams were intercepted to provide framing and signaling formats required by the Timing Subsystem. Delay was measured by looping back at IF. Second, the radio set delay was investigated. In the effort of saving time and concentrating on the experimental program, radio delay was not actually measured; if required, the results from a similar measurement series, performed on the same equipment [4.1], were used.

4.4.1 TROPO Modem Delay

The DAR (Distortion Adaptive Receiver) modem is designed to provide efficient megabit data transmission over troposcatter links. It was used in quad diversity mode at a 3.5-Mb/s transmission rate (dual mode). Minor modifications were made to this equipment to extract timing and framing information in addition to basic signal level conversion to meet TS link termination requirements. Modifications allowed the Timing Subsystem to clock the DAR multiplexer. The multiplexer combines two 1.544-Mb/s user data streams with a 192-kb/s orderwire channel to form a 3.5-Mb/s data output stream. To eliminate the timing ambiguities in passing through the multiplexer, the TS output data stream was applied directly to the QPSK modulator. Also, the mux output clock from the DAR was used to correctly time data into the QPSK modulator.

In addition, the Timing Subsystem frequency synthesizer was wired to generate a 10-MHz clock for the modem so that proper data phasing would be possible. Finally, since the multiplexer was bypassed in the modem transmitter, the demultiplexer was bypassed in the modem receiver. See [4.4] for a description of the DAR modem.

Occasional receiver sync problems were handled by sending a pulse to the modem to force receiver resync. Due to the long tracking loop time constants, this action was needed only periodically. A receiver loss-of-sync light on the modem indicated the need to resync.

Figure 4.4 shows the TS modem back-to-back setup to measure modem delay (TS delay was measured first). Table 4-5 shows the results of this measurement series.

4.4.2 Delay Characteristics of the TRC-132A Radios

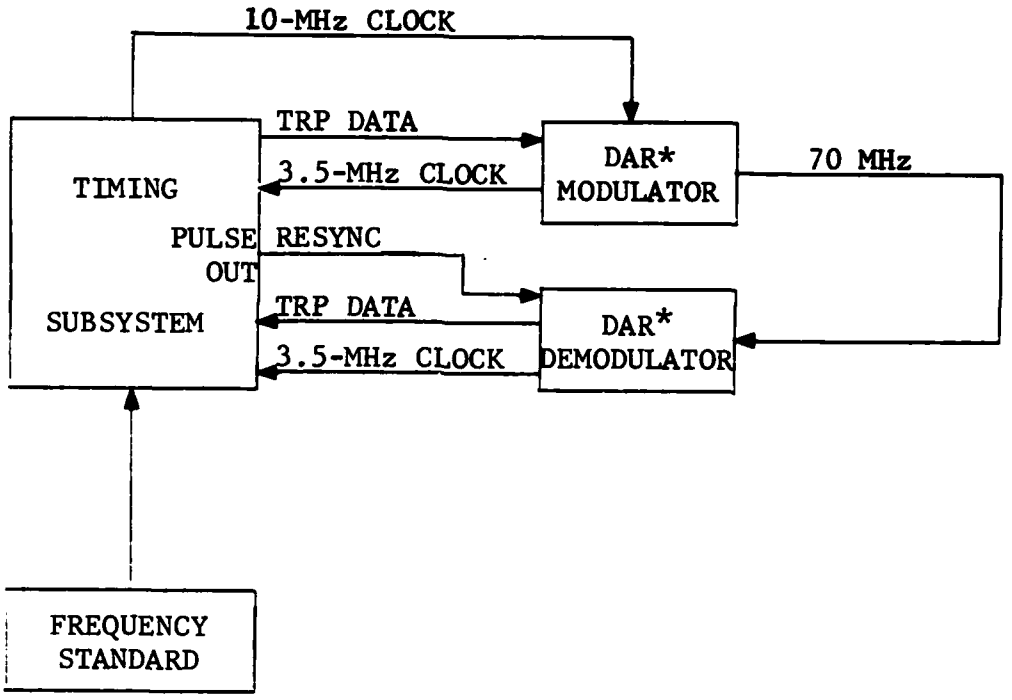
In an effort to obtain a better understanding of the delay variability occurring in the receiver and transmitter components of the system, a comprehensive set of tests was undertaken by CNR in a previous effort [4.1]. The use of a variable frequency tone probing technique was dictated by the desire to obtain preliminary equipment delay data prior to the availability of the digital pseudo-noise (PN) phase-encoded probing system. Furthermore, this approach allowed measurement of the FM modulator and demodulator portions of the radio which had a low frequency cutoff at around 100 kHz, thereby ruling out interfaces with the PN equipment.

The main objective was to isolate the various delay components in the transmitter and receiver as far as possible, and to establish the delay sensitivity to carrier offset, temperature, and probing tone frequency. Moreover, it was expected that differences in radios of the same family would also be observed.

Some of the delay measurement data are presented in Table 4-6, where the back-to-back radio delay is shown as a function of unit, carrier frequency, and tone frequency. All of these measurements were taken with the narrowband TRC-132A filters in place.

4.5 Tandem Network Delay Elements

To summarize, the findings of the equipment delay measurement program are presented in roadmap form. Note that single direction delays are present; that is, half the magnitude of the results of the back-to-back (transmit - receive tests. From the findings of the CNR effort entitled "System Timing and Synchronization" [4.1], we may assume that path delays are essentially the same in both directions (on the average). This is a critical assumption and one that may be credited for the success of supporting a timing function in full-duplex operation. As stated earlier, differential delay differences for equipment



*MODIFIED TO PROVIDE FRAMING AND SIGNAL LEVEL CONVERSION

Figure 4.4 TROPO Modem Back-to-Back Setup

TABLE 4-5

DELAY MEASUREMENTS FOR DAR-IV TROPO MODEM

	Modem #6 (Verona) TS #003	Modem #4 (Youngstown) TS #002
Data Rate	3.5 Mb/s	3.5 Mb/s
Xmit Osc In	10 MHz	10 MHz
Mode Select	Dual	Dual
OG Alarm	Normal	Normal
TS + Modem + Cables	507.20 μs	507.10 μs
Modem	6.19 μs *	6.09 μs *

*Any cabling between the modem and TS was included as part of the modem delay.

TABLE 4-6

TRC-132A DELAY MEASUREMENTS AT VERONA AND YOUNGSTOWN
(D''LAY IN MICROSECONDS)*

		Carrier Frequency (MHz)	400 kHz		500 kHz	
			With Mod/ Demod	Alone	With Mod/ Demod	Alone
Youngstown (20°C)	EX1, PA1 RX2	4500 4900	1.424	0.280	1.440	0.280
Youngstown (20°C)	EX2, PA2 RX1	4690 4790	1.437	0.293		
Verona (25°C)	EX2, PA2 RX1	4900 4500	1.409	0.262	1.421	0.254
Verona (25°C)	EX2, PA2 RX3	4900 4500	1.414	0.267	1.421	0.254

*From [4.2]

will be manifested as phase error when processing double-ended transfers. Since it was not possible to measure equipment delay other than in back-to-back modes, unidirectional delay could not be extracted experimentally. For most purposes, assuming equal delay in either direction is adequate and may be found by halving the round-trip delay. Figure 4.5 depicts the equipment and path delay elements for signal travel in either direction.

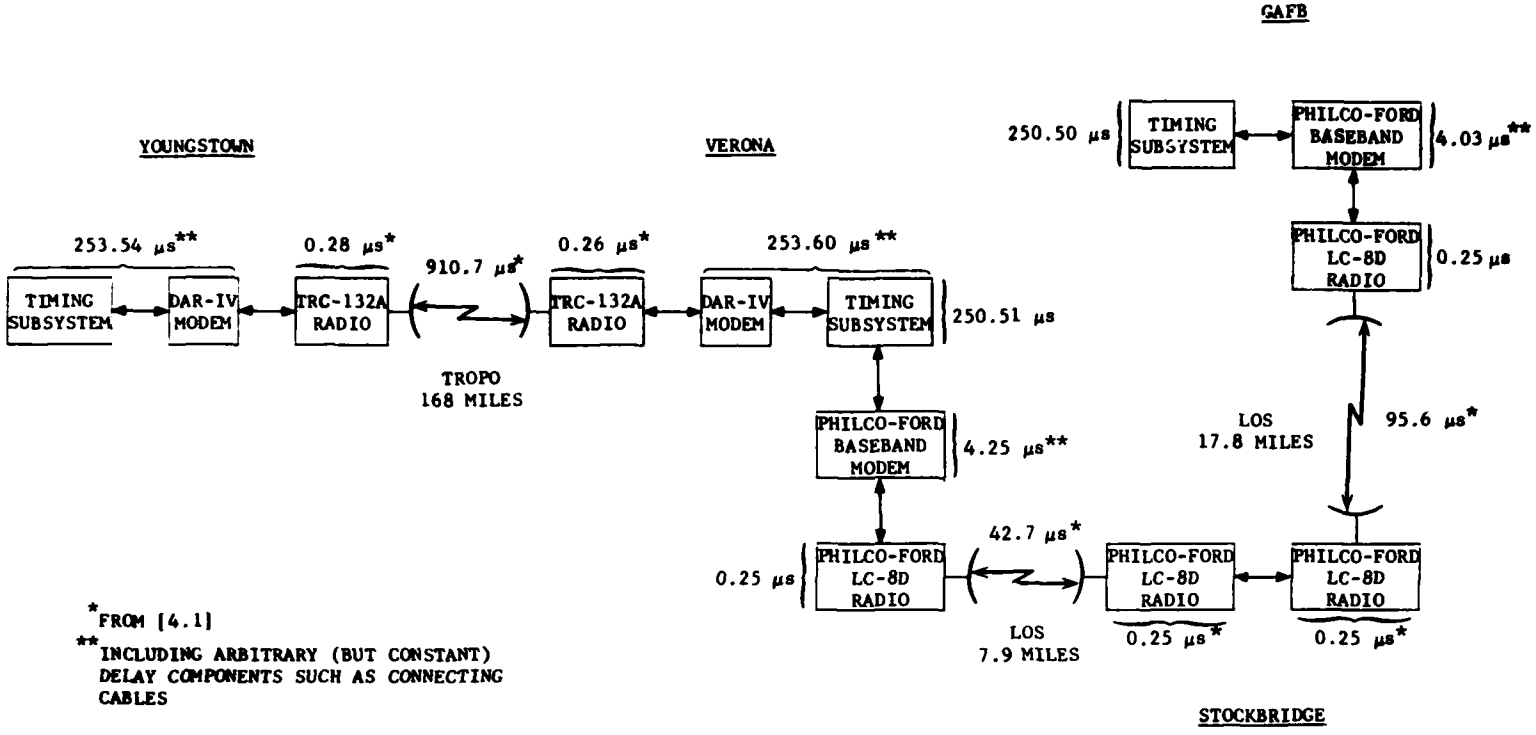


Figure 4.5 Tandem Network - One-Way Equipment and Path Delay Components

REFERENCES

[4.1] CNR, Inc., "System Timing and Synchronization," Final Report on Contract No. F30602-76-C-0347 with RADC, May 1978.

[4.2] CNR, Inc., "Timing Subsystem Development Computer Program Manual," Contract No. F30602-78-C-0287 with RADC, September 1981.

[4.3] Philco-Ford Co., "Microwave Data Transmission Test Program - Quaternary Baseband Modem," Final Report, RADC-TR-74-319, with RADC, December 1974.

[4.4] Raytheon Co., "Operation and Maintenance Manual for Distortion Adaptive Receiver (DAR)," Contract No. F30602-77-C-0008 with RADC.

SECTION 5

PERFORMANCE TESTS AND DATA PRESENTATION

In this section a review of each of the candidate timing techniques as applied to network synchronization as well as laboratory and field tests performed using portions, or all, of the tandem network described in Section 3 is presented. Section 5 closes with an interpretation of obtained results including methods used to verify clock performance.

5.1 Time/Frequency Synchronization Hierarchy

Many of the system and link control techniques have common features. The intention of this section is to summarize the important parameters and issues for a representative number of the suggested candidates. These candidates may be broadly classified into Relative Time Synchronization and Precise Time Dissemination types.

It will be assumed that the reader is reasonably conversant with each method, thereby allowing the presentation to be more concise. References to the many relevant synchronization studies that have been funded in the past are provided for the reader who needs more background. For a direct comparison of the alternative network timing and synchronization techniques, the reader is referred to [5.1]. Despite the abundance of information available on the various network synchronization techniques, a formal classification scheme does not seem to have evolved.

The classification scheme outlined here serves the purpose of defining the various synchronization conditions under which a system may operate.

In Table 5-1, we have classified five levels of network synchronization, beginning with the lowest level of independent uncoordinated clocks and progressing through to the highest level which involves universal time dissemination. There are two main groups: one collection lumped under "relative time synchronization", and a second called "precise time dissemination". The former group represents techniques which are sufficient to

TABLE 5-1

TIME/FREQUENCY SYNCHRONIZATION HIERARCHY

Level 1:	Independent Node Clocks No coordination	Relative Time Synchronization
Level 2:	Frequency Synchronization All clocks at same average frequency; system insensitive to phase steps	
Level 3:	Relative Time Synchronization Coordination of time reference at each node with incoming time reference events	
Level 4:	Network Time Reference Sync All clocks in network synchronized to internal network time	Precise Time Dissemination
Level 5:	Time Synchronization with an External Reference (e.g., Universal Time)	

satisfy network synchronization for communications purposes, while the latter techniques offer the enhancement of a precise time reference at every node. Further subdivisions are possible depending on the detailed node and link distribution scheme.

Figure 5.1 further refines the generic time and frequency synchronization technique categorization. The distinction between precise time and relative time is in the sense previously discussed; the relative time signals are lacking in known ambiguity to the resolution desired, e.g., years, days, seconds, or cycles. Independent clocks, pulse stuffing, and mutual sync all qualify as relative time synchronization techniques which involve a fixed structure. Adaptive relative time distribution and the so-called relative time distribution tree are two variations of the Master/Slave (M/S) concept. For the latter category, an invariant time tree is selected for the network so that all clocks are related to a single master, either by direct Master/Slave connection or, after a succession of Master/Slave links, through the network. The adaptive scheme differs primarily in that it is possible to dynamically alter the Master/Slave tree configuration. Usually, such a scheme is categorized as a self-organizing Master/Slave type, and the best example of an actual implementation is the Canadian DATAROUTE. A similar breakdown is possible for the precise time synchronization candidates. Basically, there are fewer choices here because the idea of time transfer implicitly involves the use of a master reference; one definition of time must be agreed upon, and all nodes then attempt to slave to this reference.

The adaptive precise time reference distribution approach bears the same relationship to the precise time distribution tree as discussed for the analogous relative time techniques, i.e., the former is able to reorganize in times of adversity so that while the master/slave structure is retained, the choice of master is not fixed, and the distribution of timing is over a variable tree structure.

Finally, it should be observed that, in Figure 5.1, another level of system distinction for five of the listed network synchronization schemes is shown. Refer in Figure 5.1 to the choice of double- or single-ended link synchronization. In summary, one can say that this distinction is between techniques involving an exchange of measurements between nodes, thereby eliminating most of the clock, phase, or time shift attributable to path length, and the alternative of calibrating and averaging

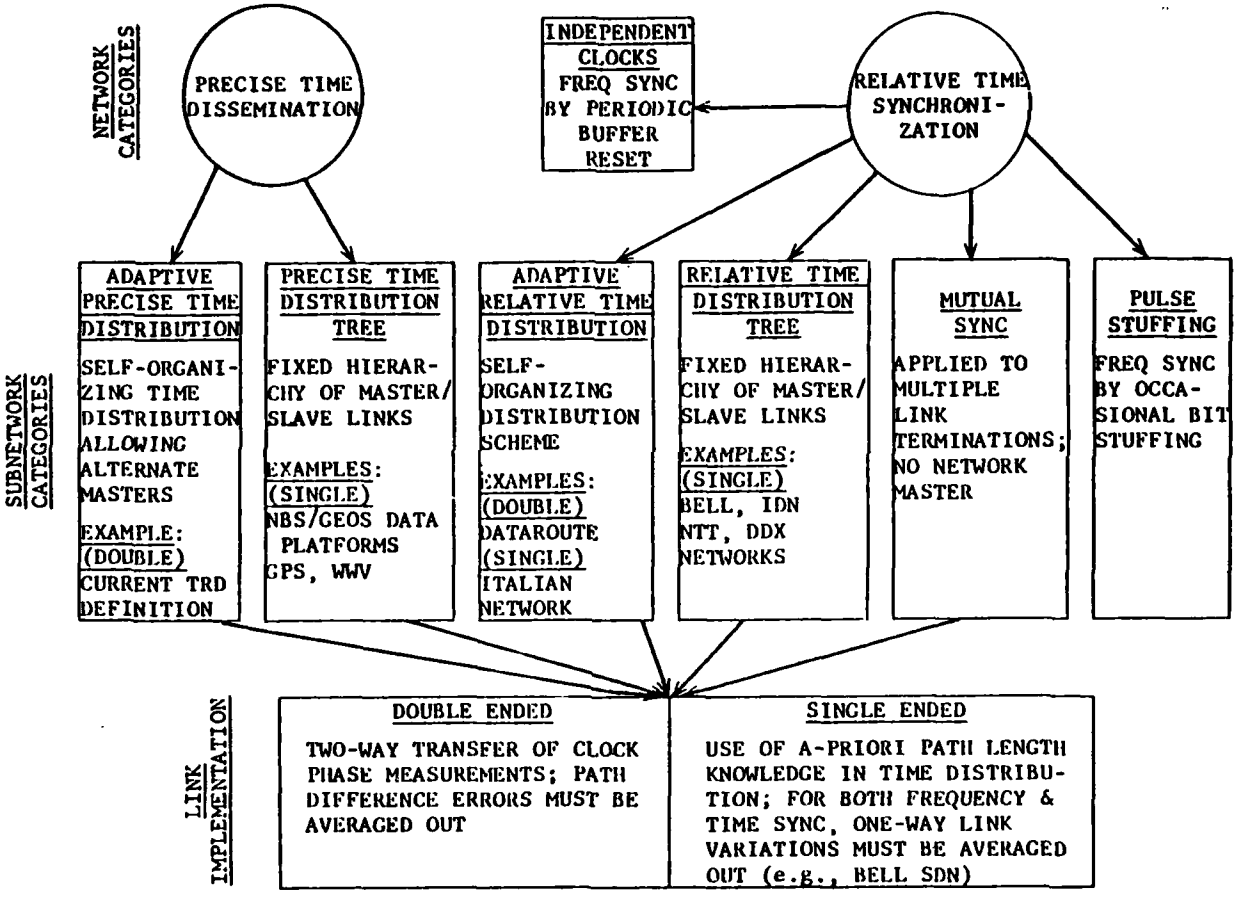


Figure 5.1 Categorization of Network Synchronization Techniques

out path effects. A good example of this is the transfer of time or frequency via a (stationary) satellite path. If the satellite ephemeris is known, the delay of the received signal relative to the system reference clock can be computed and subtracted out to form a clock error. With two-way transmissions and exchange of clock error signals via a data link, path length changes can be accounted for without such detailed calculations. See [5.1] - [5.4] for information on this subject.

5.2 Candidate Timing Techniques

The main thrust of this program was to design, fabricate, and test three experimental models of candidate Timing Subsystems. Each prototype provided the capability of operating in one of the five system timing modes of operation. These five modes are:

- Independent Clock
- Master/Slave
- Mutual Synchronization
- Time Reference Distribution
- Improved Time Reference Distribution

This section describes each of the timing technique candidates as implemented in the Timing Subsystem processor. The reader is referred to [5.4] for a treatment of the software involved in each of these techniques. A presentation of the Time Reference Distribution concepts, as interpreted and implemented by CNR, may be found in Appendix A. In this section are details of some of the more important attributes of Time Reference Distribution as compared to the other candidates.

5.2.1 Independent Clocks

This constitutes the simplest of all techniques for synchronization, at least from a conceptual point of view. The individual nodal clocks are assumed to be sufficiently stable so that link buffers of reasonable length can maintain bit integrity over a period of, say, 50 days. Clearly, the buffer is filled or depleted at a rate determined by the difference in nodal clock and incoming data rates.

The accumulation of data continues until the buffer overflows or underflows, and the time to reach this condition is determined by the clock stability and path delay variation, as well as by the length of the buffer. Even clocks with the same

long-term average frequency will show an apparent instantaneous difference at the buffer as a result of propagation delay variations, and when there is a constant average frequency offset between the two node clocks, the elastic store fills or depletes linearly with time. The operation of resetting the buffer when it overflows naturally gives rise to detrimental system effects; data is lost (or repeated) resulting in loss of Bit Count Integrity (BCI) and synchronization difficulties. Hence, the level at which the buffer is introduced is a critical choice given the BCI effects that high-level demux's have on lower-level units at the time of sync loss.

The best approach that can be adopted for totally independent node clocks is to use highly stable references such as atomic clocks, with a large enough buffer to maintain BCI over a predetermined period. After loss of BCI, the system must be reinitialized.

There are several types of frequency standards in common use today, including the cesium atomic beam resonator, the rubidium gas cell resonator, and the quartz crystal oscillator. The first of these is a primary standard giving good long-term stability without requiring any other reference for calibration. The last two are designated secondary standards, meaning that calibration of some kind is necessary at intervals, depending on the desired accuracy. The two mentioned above have the advantage of compactness and portability in contrast to cesium standard. The three types of frequency standards are compared in Table 2-1 and discussed in Section 2.

5.2.2 Master/Slave

Networks employing a fixed Master/Slave timing distribution contain a single predetermined master clock chosen at the outset of a timing experiment. The Master/Slave technique used during this program is the fixed hierarchy type and is not as demanding in terms of clock stability as the independent clock method.

The key idea is that individual nodes take their timing information from only one of the terminated links at that node in a prearranged way. The choice is made so that timing signals originating at the master clock, are disseminated through the network via interconnected links, each slave deriving its clock control from only one of those links, and passing timing information to other directly-connected nodes. This is handled in such a way that every node receives a suitable reference from a single link connected to one of its neighbors.

Master/Slave synchronization is defined as a system using directed control in which timing information is distributed in only one direction over any duplex link. The direction of control is always away from the designated master, and transmission time delays or equivalent delays not accounted for will result in an absolute time offset relative to the master. However, M/S is a frequency-averaging technique and the long-term average frequency of all nodes should be the same.

For the field test platform, network masters, chosen for the M/S experiments, were either an internal oscillator in the TS or an external reference such as LORAN-C or laboratory frequency standard. Using such a technique may provide time dissemination where the accuracy is dependent on system time transfer parameters and more general delay elements. Timing Subsystem hardware was fully capable of supporting either scheme for network master. Generally, in a Master/Slave network timing experiment, an external (but local) frequency source was connected to the TS, and the TS was programmed to track the 1-pps output of the frequency source. This TS was designated network master.

Setting up an experiment required choosing network topology, tracking loop bandwidth, and equipment and atmospheric delay times (if reduced phase error were desired). Once network parameters were determined and each node programmed to begin operation, timing information contained in exchanged TRIP data packages allowed all nodes to run at the same frequency.

In summary, it is essential that the network hierarchy be predetermined by the operator and that each chosen slave receives timing information over a single link in such a way that all slaves may trace a reference path back to the network master.

5.2.3 Mutual Synchronization

The technique of Mutual Synchronization (MS) is one in which each node has a clock that may be adjusted in frequency so as to reduce the timing error between itself and some average of the rest of the network. The general approach calls for a weighted sum of phase errors for all incoming data clocks to be used as a control signal to pull the node clock frequency. The network therefore attempts to reach a stable frequency of operation using the notions of feedback control. The method has the advantage that removal of any one node from the network still leaves the

system in synchronism, although in this situation and others, a transient disturbance will propagate around the network until a stable equilibrium frequency has been reached.

Each operating link is assigned a weighting factor between 0 and 1, and all clock error calculations are based on a normalized sum of all link weights as applied to calculated clock errors over each link. Thus, the resulting node clock error contains information from each operating link. This technique minimizes the net phase difference. Nodal clocks contribute directly to the control of all directly-connected nodes and indirectly to control of all other nodes in the network. A highly connected network contains many feedback paths contributing to potential instability because each node in a duplex communication pair exhibits some control on the opposite side.

It seems rather obvious that Mutual Sync systems are inherently self-organizing as it is simply a matter of adjusting link weighting factors upon elimination of nodes or links from the network. This is true only if all incoming links to a given node are equally weighted, thus maintaining balance within the network.

5.2.4 Time Reference Distribution

In the Time Reference Distribution (TRD) approach to network timing, individual node clocks are subjected to occasional correction using timing information being continually passed around the network from node to node [5.5]. In this regard, there are some similarities with the double-ended frequency averaging method where linked nodes exchanged timing data via a service channel. However, the Time Reference Distribution system goes well beyond this concept. Because all of the node clocks are ranked in an order of increasing importance, the network has the capability of locking itself totally to the highest ranked clock currently in operation. This technique [5.6] has been discussed for synchronization of the Western Union digital network [5.7] and the DATRAN [5.8] network.

The Time Reference Distribution scheme offers superior advantage in network control as far as survivability is concerned.

The distinctive feature of Time Reference Distribution is that a network with reasonably stable clocks at each node is forced to take corrective action at these nodes on the basis of

network time references that are continually passed around the system. All nodal clocks are rank-ordered, and the timing of each incoming link is compared with the local clock in the derivation of a timing error for that link. This error signal is transmitted back to the originating node which is likewise computing its own nodal clock error for the link. With the ensuing exchange of clock error signals between both ends of the link, each of the two nodes has the capability of computing the true nodal clock time difference with virtually no dependence on path delay. This can be expressed more precisely in the following way.

Mathematically, the situation can best be described by considering the transmission from two nodes, A and B, of a time reference pulse (TRP). Node B measures the elapsed time of the incoming TRP from node A relative to its own clock, resulting in a quantity t_A. Similarly, at node A the TRP from node B is measured relative to the local clock producing t_B. Defining the clock TRP emission times on a reference time scale to be T_A and T_B, and the path delay from A to B as τ_{AB}, it can be shown that

$$t_A = T_A + \tau_{AB} - T_B$$

and

$$t_B = T_B + \tau_{BA} - T_A$$

Hence, the clock difference, $(T_A - T_B)$, can be computed as:

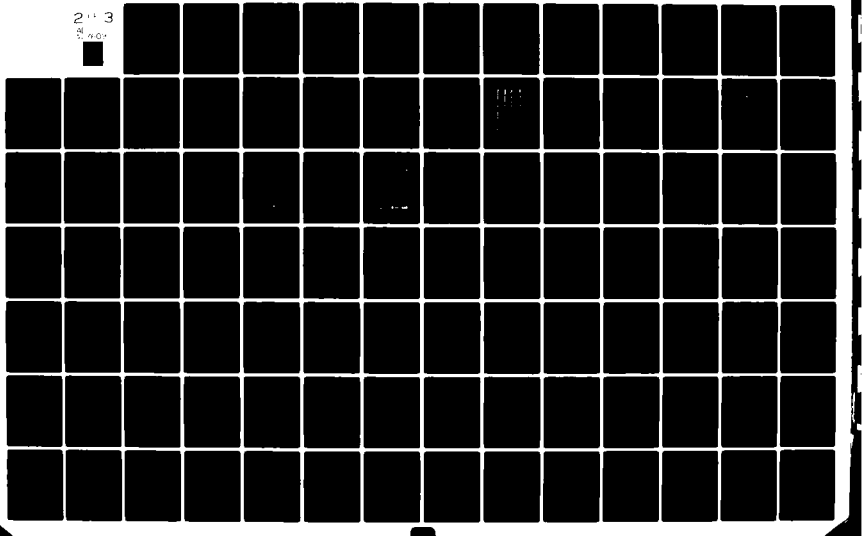
$$T_A - T_B = \frac{1}{2}\left[(t_A - t_B) + (\tau_{BA} - \tau_{AB})\right]$$

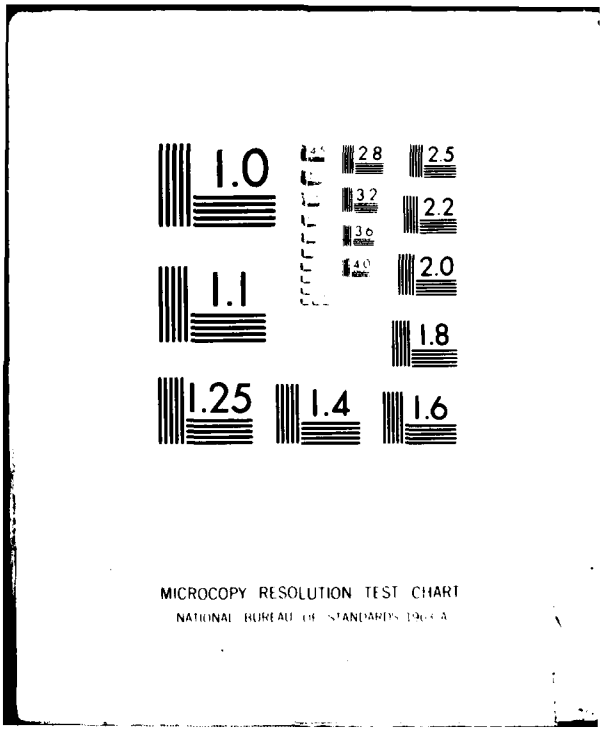
When the path delay in both directions is identical, it is apparent that

$$T_A - T_B = \frac{1}{2}(t_A - t_B)$$

and once the measurements t_A and t_B are available at both nodes, the clock offset can be calculated.

AD-A117 609 CNR INC NEEDHAM MA F/G 9/3
TIMING SUBSYSTEM DEVELOPMENT.(U)
MAY 82 K R BACKE F30602-78-C-0287
UNCLASSIFIED RADC-TR-82-124 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

Apart from the requirement of timing error exchange, the Time Reference Distribution technique functions in a manner which is very similar to that of hierarchical Master/Slave. The control signals, which must be transferred around a Time Reference Distribution controlled network, may be summarized as follows for a single node:

(1) The local time measurement (t_A) for a particular incoming link (returned to the originating node)

(2) The rank of the node being used as a master timing node for the local node (D1)

(3) A measure of the path quality for the master node supplying the local clock (D2)

(4) The rank of the local node clock (D3)

The three latter items are used with a set of prearranged selection rules* in the manner described earlier. The network then locks onto the timing data of highest rank.

In summary, Time Reference Distribution is essentially a directed control approach with additional features to improve accuracy, speed at which a network can bring clocks into phase with the master, and a greatly enhanced survivability factor due to self-organizing capabilities and clock rank-ordered topology. In fact, the most recent change to the Time Reference concept is that of Phase Reference Combining which statistically combines errors from all links. A list of the five most important features of Improved TRD, or most desirable characteristics, for synchronous networks are:

- Directed control
- Double-endedness
- Independence of clock error measurements and corrections
- Self-organization
- Phase reference combining

*Selection rules are discussed in Appendix A.

5.3 Laboratory Tests

An important phase of the in-house development schedule was the system test program. With simple test equipment it was easy to determine the performance of a single TS or a small network of two or three units. The ability to track an external reference signal without TRIP packages is a very useful feature of the TS hardware. In this mode, a 1-pps signal, applied to one of the auxiliary reference ports, is sufficient to enable tracking of the signal via a few commands from the operator. This is the most basic mode of operation of the Timing Subsystem. Auxiliary reference operation allows several very simple, yet useful, nodal configurations. First, a single mode can be instructed to discipline its internal clock to that of an external reference pulse. Secondly, a master node can be configured to reference an external source rather than its own clock, thus providing network synchronization to any local clock at the master node site. Finally, and most importantly, an external time reference, such as UTC (NBS) or UTC (USNO) may be applied to the Timing Subsystem (after 1-pps decoding in the LORAN-C or satellite receiver), thus passing universal time throughout a network (directed control only) with no penalty in TS hardware complexity.

Also discussed in this section are the types of network level experiments run in-house used to observe the behavior of the candidate timing techniques under simulated network conditions. Of course, all data paths were through direct wire connections to each TS. However, network stress could easily be introduced through the operator's terminal or by physically removing a data path or node.

5.3.1 Auxiliary Reference Operation

One of the more fundamental measurement capabilities of the Timing Subsystem is the technique of slaving the nodal clock to an externally-applied 1-pps reference. Simply stated, this pulse is allowed to gate the time interval measurement unit, and processed errors are then applied to the software-controlled digital Phase-Locked Loop (PLL) for clock corrections. First, the external pulse (in this case supplied by a pulse generator) was applied to one of the three external TRP ports located at the rear panel. Secondly, a performance verification facility (Time Interval Measurement Counter) was connected to both the input pulse and the adjusted output pulse from the Timing Subsystem. Therefore, by measuring the elapsed time between these pulses, one is

effectively measuring the error signal that the TS is attempting to reduce. Figure 5.2 shows the layout of the test setup. Note that there are three Auxiliary Time Reference Pulse (AUXTRP) input ports. Connecting the reference signal to any one of the three will suffice as long as the node computer is instructed as to which port to reference. This is accomplished by the appropriate command at the operator's terminal.

If desired, the operator may inspect the Performance Assessment (PA) buffer within the computer memory for a series of averages of clock error and the average difference between the TS timing source and each of the three external reference ports. This information is available from the operator's keyboard.

In addition, a self-reference mode of operation can be specified. In this setup, the unadjusted node standard 1-pps is applied directly to one of the auxiliary reference ports. This effectively allows disciplining of the nodal reference clock to the phase of the external frequency source. Again, performance is monitored via the time interval counter or the automatic PA averaging feature. Figure 5.3 depicts the test setup for self-reference operation.

Although no formal performance curves are available, it was determined that the Timing Subsystem was working properly. Further experimentation involved removing the reference pulse and observing TS behavior. It was decided at this point that a 30-second guard time would be incorporated in the nodal software that would disallow any major clock alterations and "coast" (using previous loop output history) for a maximum of 30 seconds if no error measurement data were available. This feature prevents the TS from cycling through startup and acquisition phases if a new error term were not available each second. This is especially important when confronted with a high error rate. Remember that the TS utilizes error-detection hardware but is forced to discard a frame when the errors are present. Section 6.1.4 recommends error-correction [illegible]ment as an important element of nodal hardware - when pass[illegible]ing and status information in a single frame through the s[illegible]vice channel, continuous errors resulting in data elimination cannot be tolerated.

5.3.2 Network Operation

The first attempt at network synchronization involved a simple Master/Slave experiment with the master clock disciplined

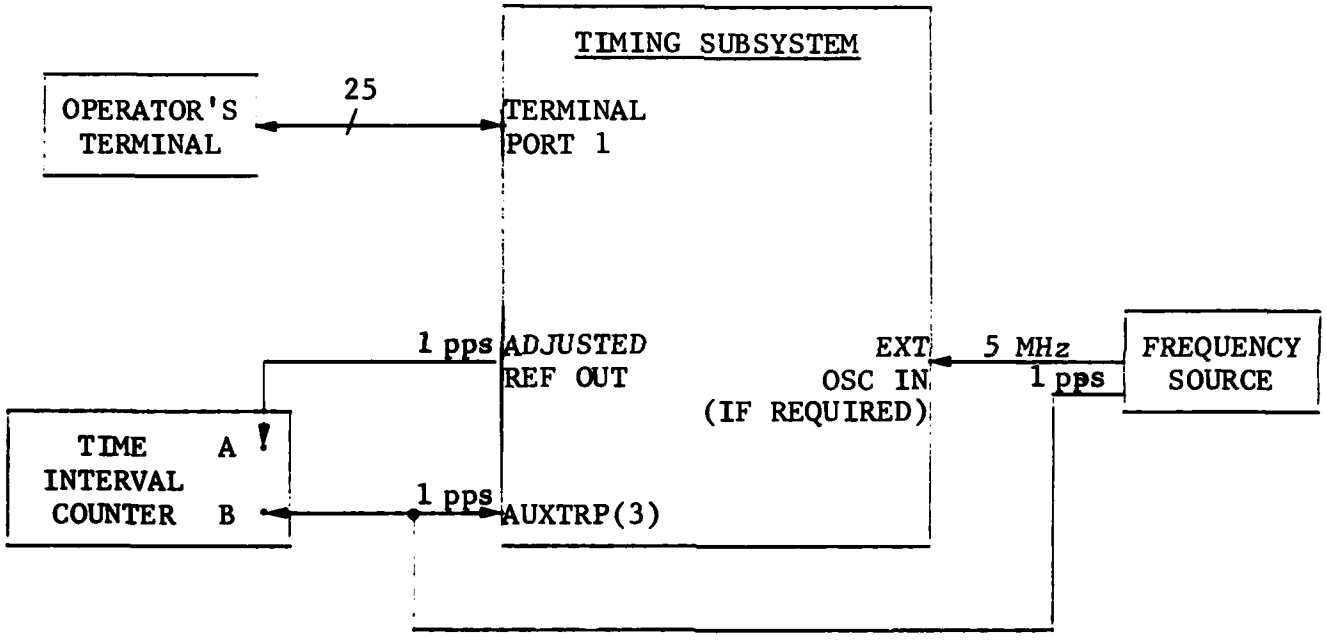
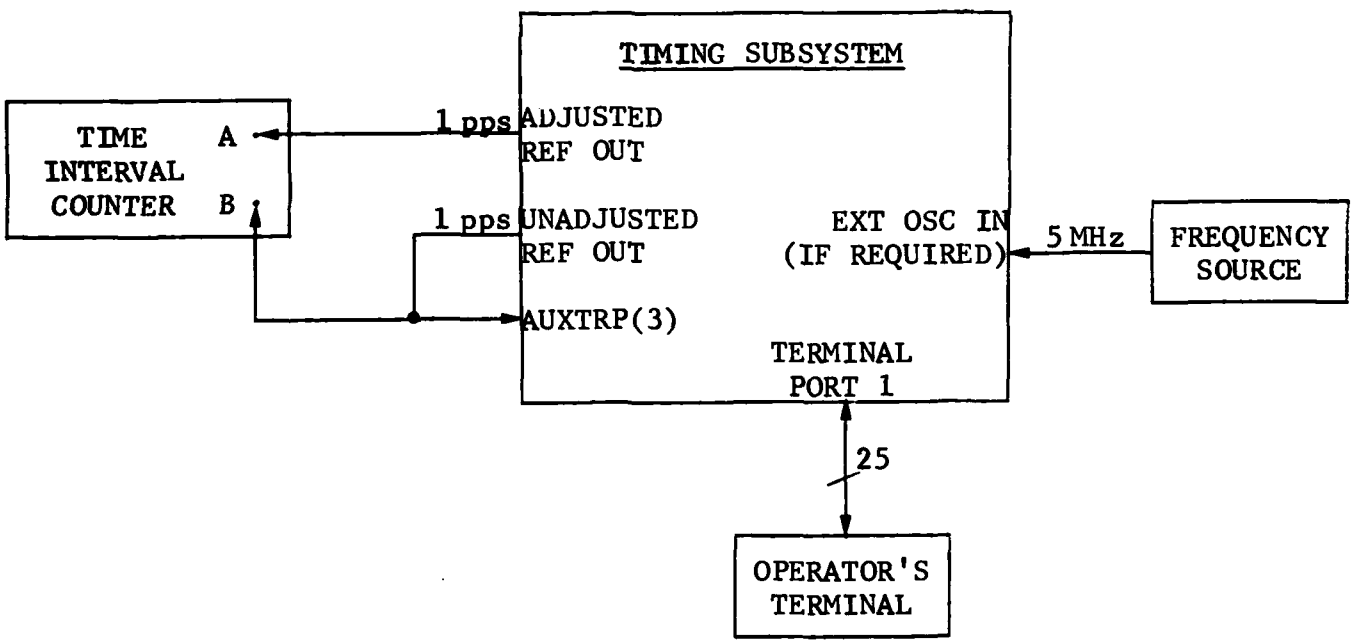


Figure 5.2 Auxiliary Reference Test Setup


TIMING SUBSYSTEM
TIME INTERVAL COUNTER
A
B
1 pps
ADJUSTED REF OUT
1 pps
UNADJUSTED REF OUT
EXT OSC IN (IF REQUIRED)
5 MHz
FREQUENCY SOURCE
AUXTRP(3)
TERMINAL PORT 1
25
OPERATOR'S TERMINAL

to an external 1-pps source. Although no formal acquisition and tracking performance data were taken, it was clear by the use of the interval counter that the two subsystems were in close frequency alignment.

Startup behavior was observed very carefully for possible overshoot, inaccuracy, or measurement foldover error conditions. The coarse delay loop implemented in software was capable of stopping the node-adjustable clock over a range of 4 μs to 1 second with $\pm$4-μs accuracy. To eliminate the possibility of erroneous measurements, clock error was sampled over a 3-second interval before a coarse delay adjustment was initiated. The overall stability and accuracy of the coarse delay adjustment loop can be attributed to the use of a multi-stage software loop technique and careful calibration (i.e., measurement) of instruction execution times. Once the coarse error adjustment has brought the clock to within 4 μs of zero error, acquisition begins and the phase microstepper is instructed to slew at 100 ns/s so as to further reduce clock error. Tracking is initiated when the error falls within a programmable tracking region threshold. For typical coarse and fine thresholds of 4 μs and 150 ns, respectively, the time to reach tracking when a node enters the network is approximately 43 seconds for the worst case; but, more often, times in the 15 - 25 second range were observed. Figure 5.4 is a representative curve of the acquisitional behavior of the Timing Subsystem. Notice that startup mode reduces the error from the starting point (4 μs - 1 s) to $\pm$4 μs within three seconds.

Further two-node testing included: Master/Slave, both with and without an external reference for the master, each tested using the phase microstepper and VCO methods of clock adjustment; Mutual Synchronization; and Time Reference Distribution. In each case, node behavior was of prime importance since it had been sufficiently demonstrated that the software PLL was working; i.e., the Timing Subsystem was certainly able to acquire and lock onto a reference signal as well as to pass timing information over wired links. Therefore, the in-house network-level testing was focused on the characteristics of TS behavior in a simulated network environment when interacting with other nodes.

To evaluate nodal performance in a two-node network, a connection scheme was devised to monitor each TS. Figure 5.5 shows the connections for a single link two-node performance evaluation network. Additionally, a three-node delta configuration performance evaluation network was wired to monitor all

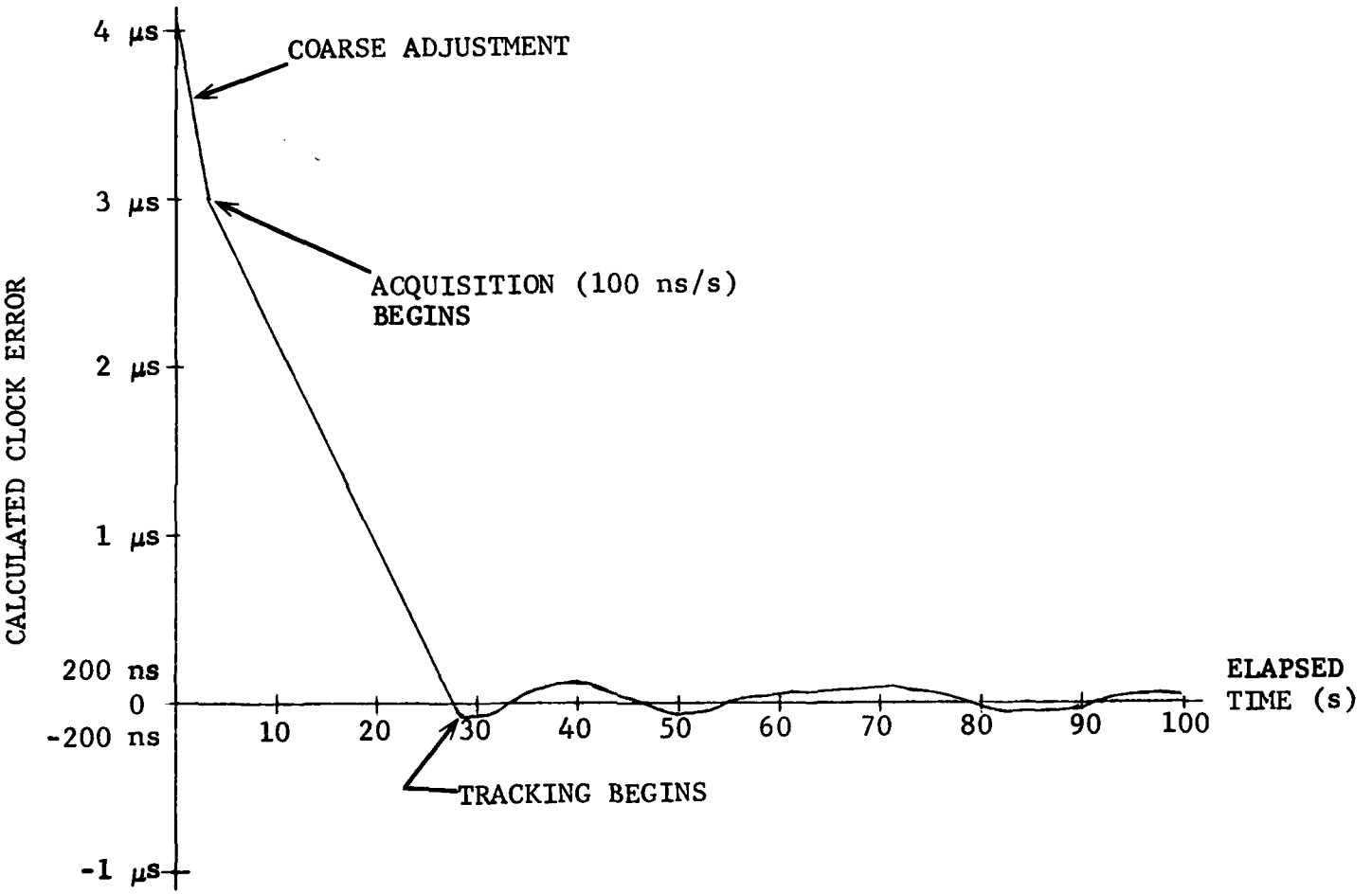


Figure 5.4 Typical Acquisition Behavior of Timing Subsystem

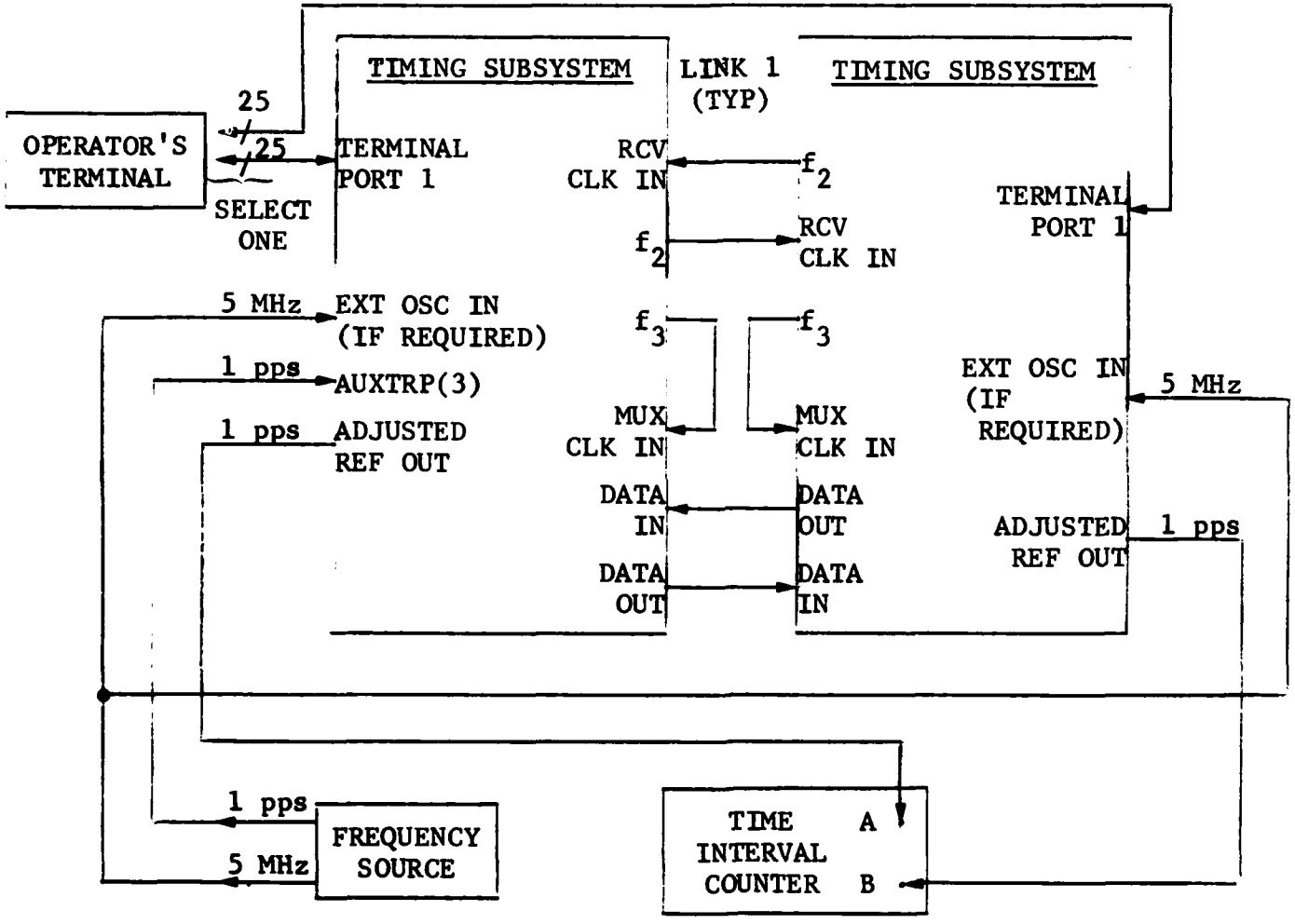


Figure 5.5 Two-Node Performance Evaluation Test Setup

three TS's, as shown in Figure 5.4. Notice the redundant link between TS2 and TS3; this was an important aspect of tests involving network reorganization features (TRD). The TS is forced to choose the best path from all paths to receive timing information. By assigning link merits (demerits) for each communications path, any given node should be able to choose the path of total least demerit from the master.

In summary, directed control (M/S, MS, TRD) experiments performed satisfactorily as expected. Master/Slave not only was the simplest timing algorithm to implement in software but also was the easiest to set up for an experiment in a network (except Independent Clock). Master/Slave was always capable of frequency synchronization but, including equipment delays from back-to-back measurements, resulted in reduced phase error as well. Although simple Master/Slave is not a phase-coherent technique, the addition of phase-reference combining, or other TRD-like features, would further enhance M/S performance without greatly complicating matters. On the other hand, Mutual Synchronization was found to be somewhat cumbersome and unreliable on the whole. Additional error signal filtering was required to decrease the possibility of an unstable network. Laboratory tests revealed that MS was somewhat unpredictable in behavior and a problem with starting up the network was observed. Simply put, how do nodes just entering the network avoid perturbing the current mutual system? How do two nodes, attempting Mutual Synchronization, begin from gross clock misalignment? In attempting to overcome these problems, less confidence was placed in this technique due to previously mentioned implementation difficulties. For this and other reasons described in Section 6, Mutual Synchronization was considered an unsuitable timing technique for DCS use.

Finally, the last series of laboratory tests concerned the interaction of three nodes. Master/Slave experiments demonstrated that directed control could easily align clocks in frequency through several levels of interconnected nodes. This was observed in a tandem configuration with the master referencing an external frequency source. This was also proved on a delta-style network with a redundant link. Since each slave subsystem was instructed to find timing information on a single predetermined link, redundancy or closed timing loops should not affect the directed control path from master to slaves.

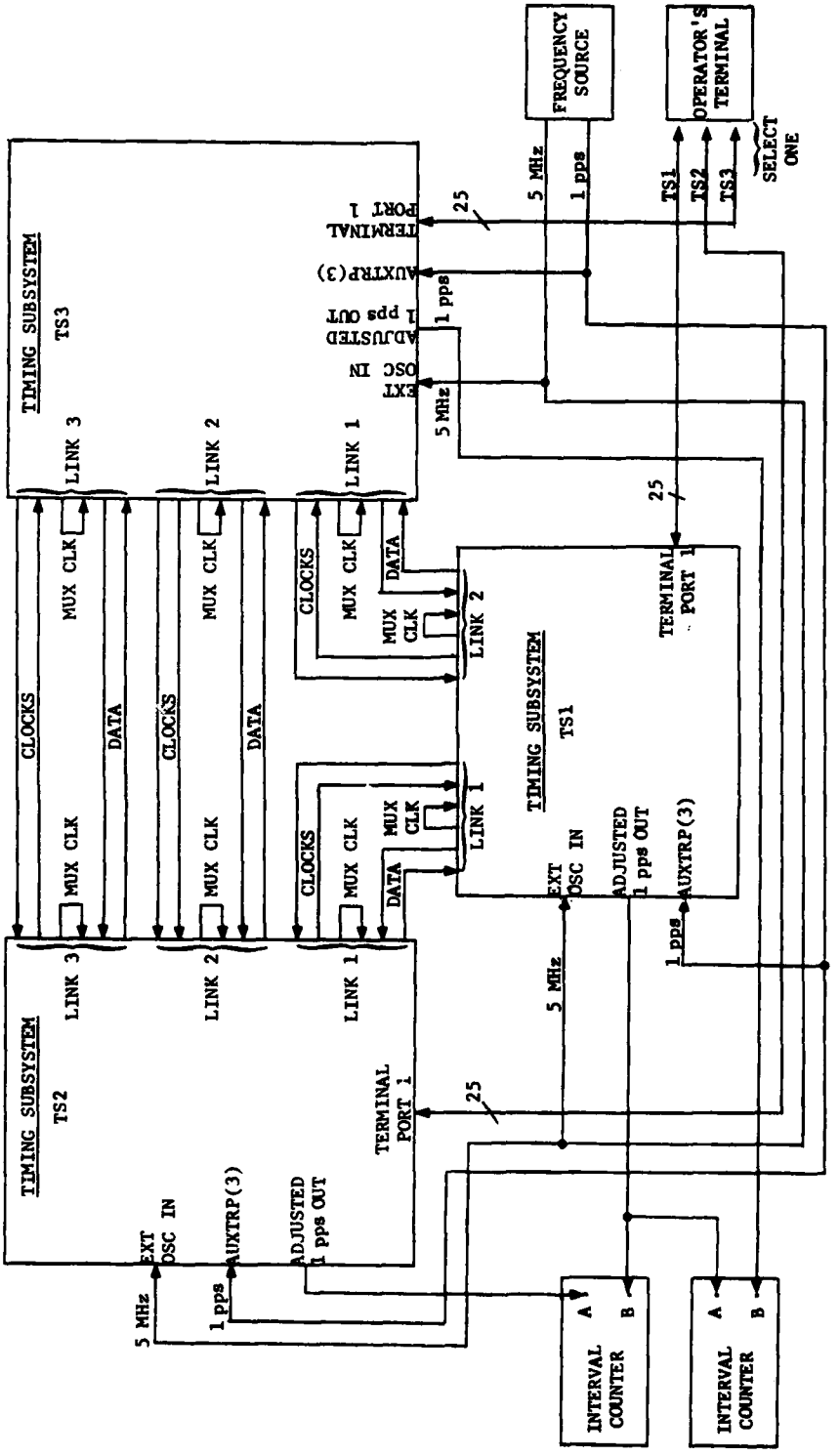


Figure 5.6 Three-Node Performance Evaluation Network (Delta)

Laboratory experiments with Time Reference Distribution (both original and improved versions) were focused primarily on network self-organization features. As mentioned earlier, Figure 5.6 shows the network used to evaluate self-organization experiments. To illustrate the tests undertaken, a simple experiment was conceived to exercise the hierarchy rules of TRD as interpreted and implemented in software by CNR. For this series of experiments, the original Time Reference Distribution [5.5] with obsolete data handler was used. As far as network hierarchy is concerned, Improved Time Reference Distribution [5.6] behaves in the same manner except link qualities are assessed on statistical parameters rather than on integer link demerits found in the original version. Following Figure 5.7 the sequence of events used to demonstrate TRD self-organization capabilities were:

Definition of Terms

TS[n]	Timing Subsystem number n
L[n]	Link number n
R=[n]	Node clock rank n (lower numbers = better clocks)
D=[n]	Link demerit (lower numbers = better links)

State 1: Each Timing Subsystem is assigned a unique clock rank and each path is assigned a demerit. Upon reaching steady-state network operation, the bold arrow(s) show the path of the resultant directed control.

State 2: TS1 rank was degraded; TS2 rank was improved. A switch of network master to TS2 was observed. Directed control following paths of least demerit to subservient nodes was observed.

State 3: Link 3 demerit was raised to 5. A resulting path switch was observed to maintain path of least total demerit to nodes lower in the hierarchy.

State 4: TS3 rank was improved so as to be the best in the network. Link 4 demerit was improved. A master switch and path switch were observed, as indicated on the diagram.

State 5: Link 1 was removed. Link 3 demerit was improved. Link 4 demerit was degraded. TS2 rank was improved so as to be the best in the network. TS3 rank was degraded. Again, the algorithm switched master to TS2. Directed control path was over links of least

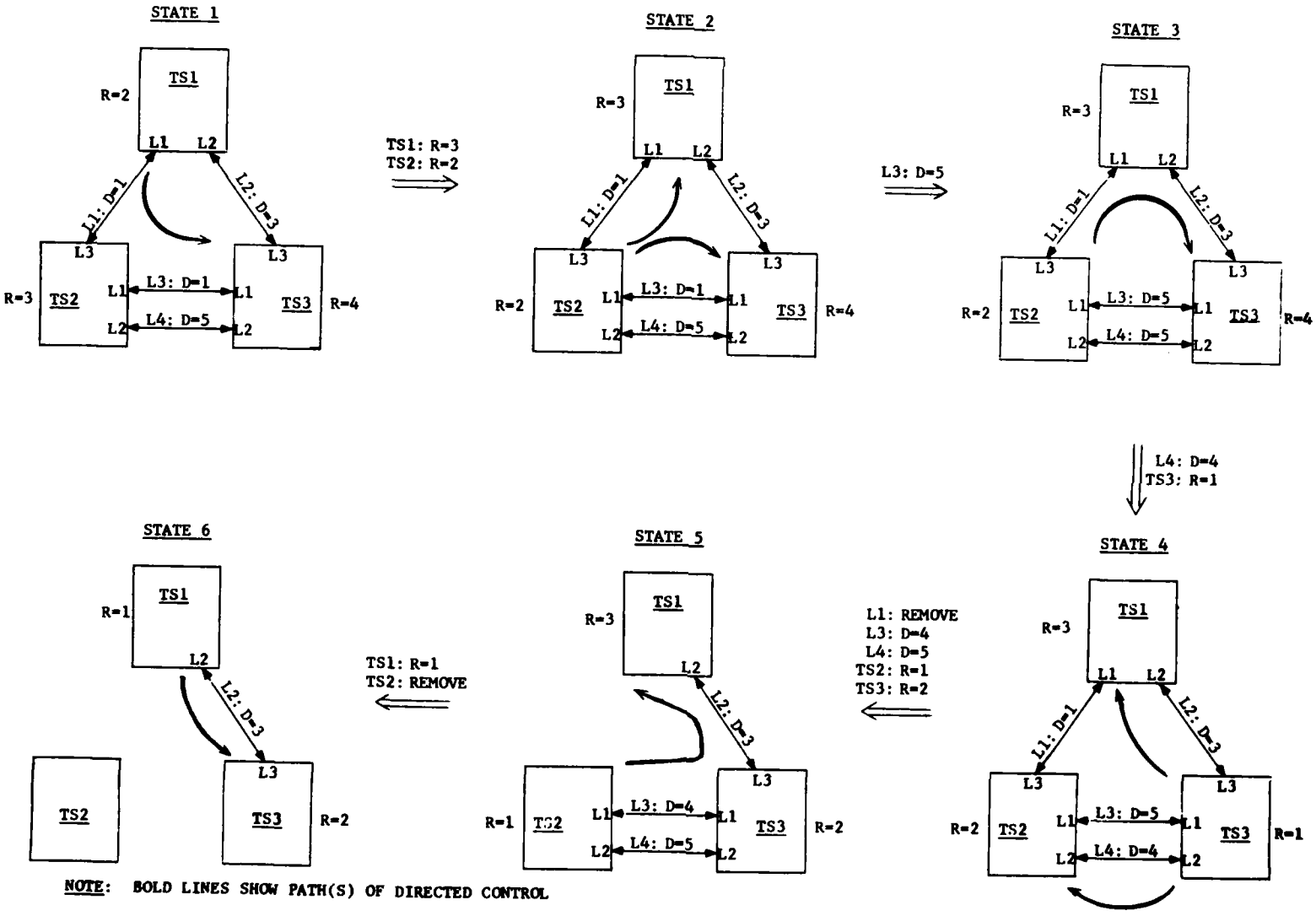


Figure 5.7 Laboratory Tests of TRD Organizational Capabilities

demerit so as to maintain lowest total path demerit to any node lower in the hierarchy.

State 6: Links 3 and 4 were removed. TS1 rank was improved to best in network. TS2 was removed from network as a result of eliminating links 1, 4, and 5. Path switch and master switch observed according to TRD hierarchy rules.

Clearly, the TRD hierarchy experiments were successful. Although long-term stability and accuracy data were not acquired, it seemed that TRD performed as well as simple Master/Slave. Additional long-term tests were not possible due to time limitations. However, it seemed certain that TRD would function properly in the field.

5.4 Performance Assessment

It was evident from the outset of the field test program that a conscientiously-applied performance measurement technique was as important as the tests themselves; that is, verifying that a given node is transmitting and receiving data over a link is no guarantee that synchronization exists at the network level. Through a redundant set of connections to the Frequency Measurement Terminal and a LORAN-C receiver at each site, a performance measurement system was configured to enable assessment of synchronization performance at both nodal and network levels. References [5.9] and [5.10] provide further insight into the use of universal time as a network timing source.

5.4.1 Performance Measurement System

The basic function of the Performance Measurement system is to record averages of time interval measurements from various interconnected devices. The measurement system consisted of the following devices located at each site: Timing Subsystem, Frequency Measurement Terminal with LORAN-C receiver, and a frequency standard. Figure 5.8 shows how this equipment was wired.

The Frequency Measurement Terminal should be considered an integral part of a network timing experiment. It not only provides time interval measurement capabilities for up to three external clocks but also houses a remote telephone data coupler which can be used to query the Timing Subsystem from a distant location. Each Frequency Measurement Terminal (FMT) also contains a LORAN-C receiver whose 1-pps output is typically

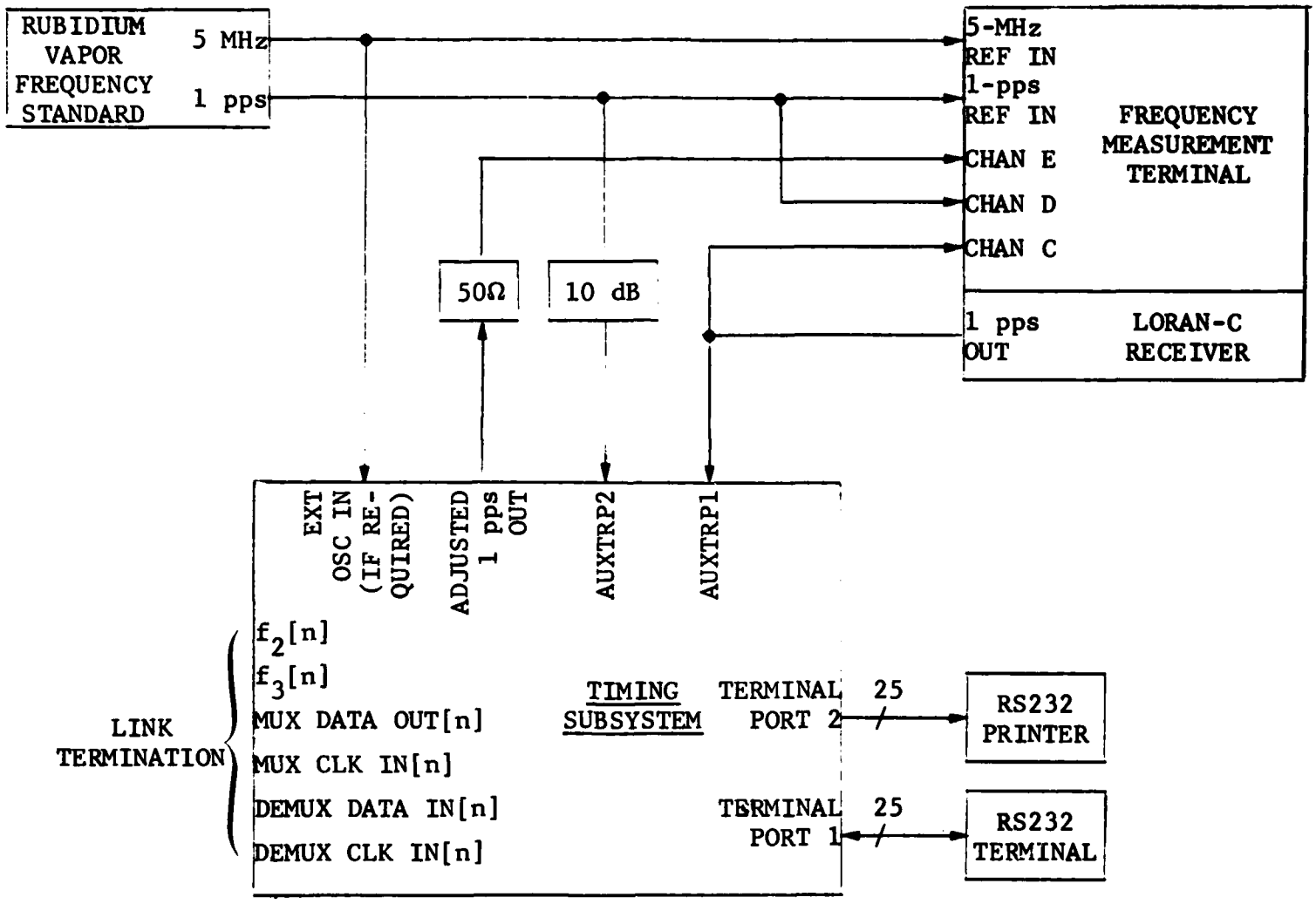


Figure 5.8 Timing Subsystem Performance Measurement System

connected to measurement channel C on the central processor. Comparing LORAN-C readings with the applied 1-pps source clock to the FMT results in a plottable drift rate which can easily be compared to LORAN-C readings at NBS and, ultimately, the U.S. National Time Standard. Through these means, any external clock applied to an FMT housing an integral LORAN-C receiver may be compared rather easily with any other time source directly connected to any other FMT unit.

For detailed instructions on setup conditions and operation of the FMT, the reader is asked to consult [5.11].

The performance measurement system gathers time interval measurement averages from both the FMT and Timing Subsystem. The measurement capabilities are briefly described below.

- A rubidium frequency standard, located at each site, was considered the node frequency standard and was used to provide 5-MHz and 1-pps references for both the FMT and TS; that is, all FMT measurements are elapsed time from the frequency standard pulse (1 pps) to the pulse being measured. The TS uses the 5-MHz reference for a timing source and the 1-pps reference to compare against the node adjustable clock.
- The FMT can directly compare the decoded LORAN-C pulse with that of the frequency standard, thus providing a path to an external reference (Seneca, NY, LORAN-C station with cesium beam standard) to which all nodes may be compared. This is the method by which universal time may be introduced into the network.
- Redundancy exists between TS and FMT measurements of LORAN-C and frequency standard pulses to further reinforce performance curves. In more detail, the FMT measures elapsed time between the frequency standard 1-pps and LORAN-C as well as frequency standard vs. TS adjusted 1-pps output. Similarly, the TS measures elapsed time between its adjusted 1-pps output and the frequency standard 1-pps as well as TS vs. LORAN-C.
- The FMT keeps continuous running averages over 4-hour intervals, each consisting of 200 samples.
- The Timing Subsystem saves 24 hours of 10-minute averages of 600 samples each in volatile memory that is available to the operator.

5.4.2 Methods of Verifying Network Performance

Once a timing experiment has begun, all data logging is automatic. The Timing Subsystem has the capability to store 10-minute averages of 600 samples each for 24 hours. Each sample average contains:

(1) Time-of-day at end of sample period
(2) Average nodal clock error (as calculated)
(3) Average of node clock vs. AUXTRP1
(4) Average of node clock vs. AUXTRP2
(5) Average of node clock vs. AUXTRP3

It is obvious that, in order to find the drift rate between the node adjustable clock and an external clock, it is necessary to connect the external clock 1-pps output to one of the three external TRP (AUXTRP) ports. With this connection and a Frequency Measurement Terminal at each site, the user has the facilities to compare an external local clock to any other in the network as well as to the U.S. National Time Standard through LORAN-C or TV Line-10 readings at remote FMT's.

A Frequency Measurement Terminal, located at the National Bureau of Standards, Boulder, Colorado, is driven by the U.S. National Time Standard. This terminal also receives transmissions from the LORAN-C transmitter stations at Dana, Indiana, Fallon, Nevada, and from each of the three network-affiliated television stations in their local area.

The drift rate ($\Delta t/T$) of the clocks used to drive the FMT's, located at the RADC sites relative to the U.S. National Bureau of Standards in Boulder, Colorado, can be measured as follows:

- Put the Local Frequency Measurement Terminal in the telephone mode.
- Call the Frequency Measurement Terminal located at the National Bureau of Standards, Boulder, Colorado.
- Read out the eight days of stored data from the LORAN-C channel (C) and each of the network television channels. Procedure is described in [5.11].
- Compare the time difference readings at NBS with the time difference readings taken at the local terminal for the LORAN-C data and data from each of the three network television channels (the LORAN-C data is far more accurate than the TV data).

- **Plot the drift rate ($\Delta t/T$) for the 8-day period. Continue plotting this data for subsequent periods as long as it is necessary to satisfy local requirements.**

The Frequency Measurement Terminals will accept one pulse-per-second outputs from up to three additional clocks and will measure, identify, and record minutely time differences, averaged over 4-hour periods, between the clock in the terminal and each of the three external clocks. Drift rates ($\Delta t/T$) between the clock in the terminal and the clock being calibrated can be calculated for as long a period as is necessary to satisfy local requirements.

Delay may be added (subtracted) from the external clock being calibrated until the time difference between it and the clock in the FMT is zero plus or minus any time error in the terminal clock relative to the USNO or NBS master clocks as maintained in the log for the clock in the terminal.

Drift rate ($\Delta t/T$) can be calibrated for the external clock using the procedures outlined above. These procedures will calibrate the drift rate of the external clock relative to the clock in the terminal. To calibrate the external clock relative to the USNO or NBS master clocks, a second drift rate $(\Delta t/T)'$ must be calculated using the measured drift rate data of the external clock relative to the terminal clock and the measured drift rate data of the terminal clock relative to the USNO or NBS master clocks. This second drift rate $(\Delta t/T)'$ calculation is then used to calibrate the external clock, as outlined earlier.

5.5 Field Tests

Following a brief review of the manner in which performance data was gathered, a section is devoted to each of the timing technique experiments performed on the single-ended tandem network described in Section 3. It was not feasible to exercise each candidate timing technique so emphasis was placed on the frequency alignment (directed control) techniques. No experiments were run using Independent Clock, Mutual Synchronization, or Improved Time Reference Distribution candidates for reasons previously discussed.

Included with a description of each network test is a diagram of the network used and a brief evaluation of timing technique performance. Performance curves depict the frequency

offset of each node as compared to the Seneca, NY, LORAN-C Test Bed Master. Specific difficulties and obstacles affecting the measurement process are noted where applicable.

One point worth noting concerns the node setup and initialization parameters. No attempt was made to experiment with various clock control loop parameters. Additionally, although equipment delays were measured and path delays were known from published material, no attempt was made to use the data in the TS as a means to minimize clock phase offset between nodes in a single-ended measurement. Also, no precise time experiments were undertaken. However, it would not be difficult to use equipment and path delay quantities to reduce phase error - merely a tedious task and not of prime importance for this experiment series.

A tabularized summary of parameters used in the network experiments will be presented in Section 5.6.

5.5.1 Two-Node Master/Slave (TROPO)

A simple single-ended directed-control test was performed over the 168-mile TROPO range in the Youngstown-to-Verona direction. A diagram of the equipment used at each site is shown in Figure 5.9. Quad diversity was used to maximize reception levels and minimize bit errors.

Almost immediately it was observed that even with a strong received signal level and the normally moderate TROPO Bit Error Rate of about 10^{-6} [5.2], the Timing Subsystem was rejecting TRIP's at about one per five or six frames received. Although this observation was not surprising, it emphasizes the importance of error-correction equipment for error-free TROPO reception. This problem is further compounded if a double-ended transfer was attempted. Double-ended clock error calculations require buffering of frames from the current and the previous exchange at each node, thus quadrupling the error-free TRIP requirements over single-ended transfers.

Careful monitoring of TS status through the debugging capabilities of the TS software revealed that TROPO fading was perturbing the bit stream to the point where frame boundary flags were not being received, thus causing frame over-runs and, often times, receiver aborts. Moreover, these "endless" frames were overwriting TRIP memory storage locations and destroying data from other channels - a totally unacceptable condition.

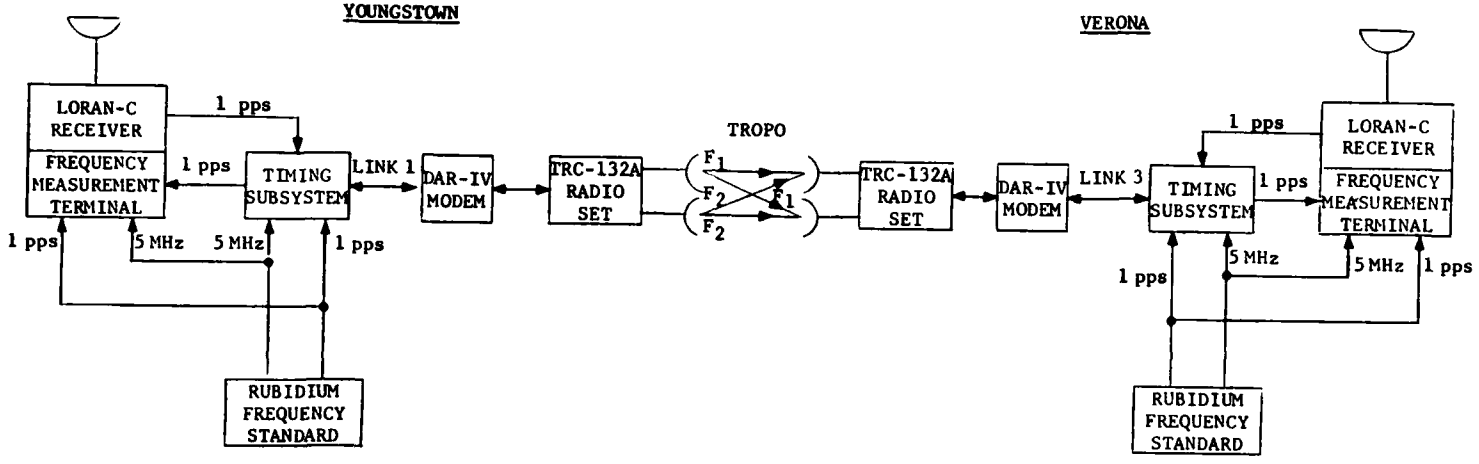


Figure 5.9 Two-Node Network with TROPO Link (Verona - Youngstown)

The cure for this problem involved a change in software for the Receive Link Termination Processors (RLTP). The Computer Program Manual for Timing Subsystem Development [5.4] describes in detail, with accompanying flowcharts, the RLTP processing scheme for incoming data. Incorporated was a byte-count check for each incoming byte or byte pair. If the byte count did not exceed the predetermined frame length (not including flags or CRC check bits), then the received bytes were committed to memory. If the byte count was exceeded before receiving a closing flag, then the RLTP was automatically aborted, the TRIP ignored, and the search for a new opening flag was begun. Implementation of this check resolved the problem caused by the characteristics of the fading channel. As an aid to development, the TRIP frame length (in bytes) was kept as a programmable feature, thus allowing a variety of frame lengths to be chosen.

For a look at typical TROPO received signal levels for C-band quad diversity, refer to Figure 5.10. Notice that fairly large signal level excursions are observed at about an 8 - 10 Hz rate and that relatively deep fades occur about one to two times per second. This chart is from the June 1981 series of experiments.

Summarizing Timing Subsystem performance over TROPO links may be simply stated: For truly reliable performance, error-correction equipment is required. This is especially true since both timing and status information are sent and received over the service channel (option C, Section 5.1.2.3 of [5.2]). However, there is no doubt that a fading dispersive channel can support a timing function with very acceptable accuracy.

This experiment duration was approximately 28 hours. With the Youngstown node tracking the local rubidium frequency standard and the frequency difference between the site rubidium and the received LORAN-C from Seneca known a-priori, it was a simple matter to plot the performance of the master and slave clocks relative to a single reference. Figure 5.11 shows the relative frequency rates of the three locations. Seneca, assumed to be the Test Bed Master, is the baseline and has zero frequency offset. The cumulative error of the sites shows up as a slight frequency difference as compared to Seneca. However, it does not matter what that offset is as long as both master and slave exhibit zero relative frequency offset. Without exceeding the measurement capabilities, it was determined that this Master/Slave experiment was performing satisfactorily. In fact, the slight frequency

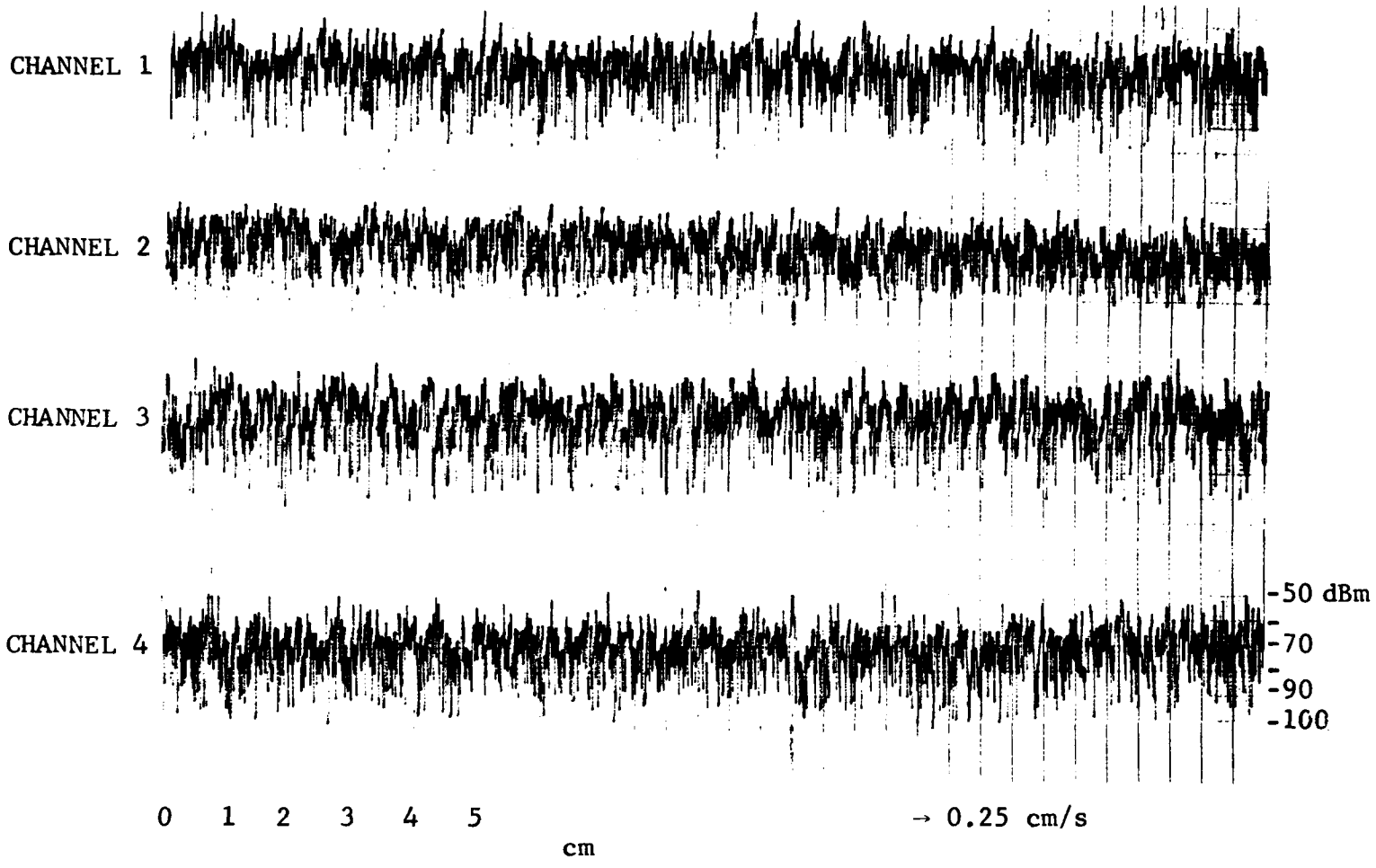


Figure 5.10 Typical C-Band TROPO Received Signal Levels (Quad Diversity)

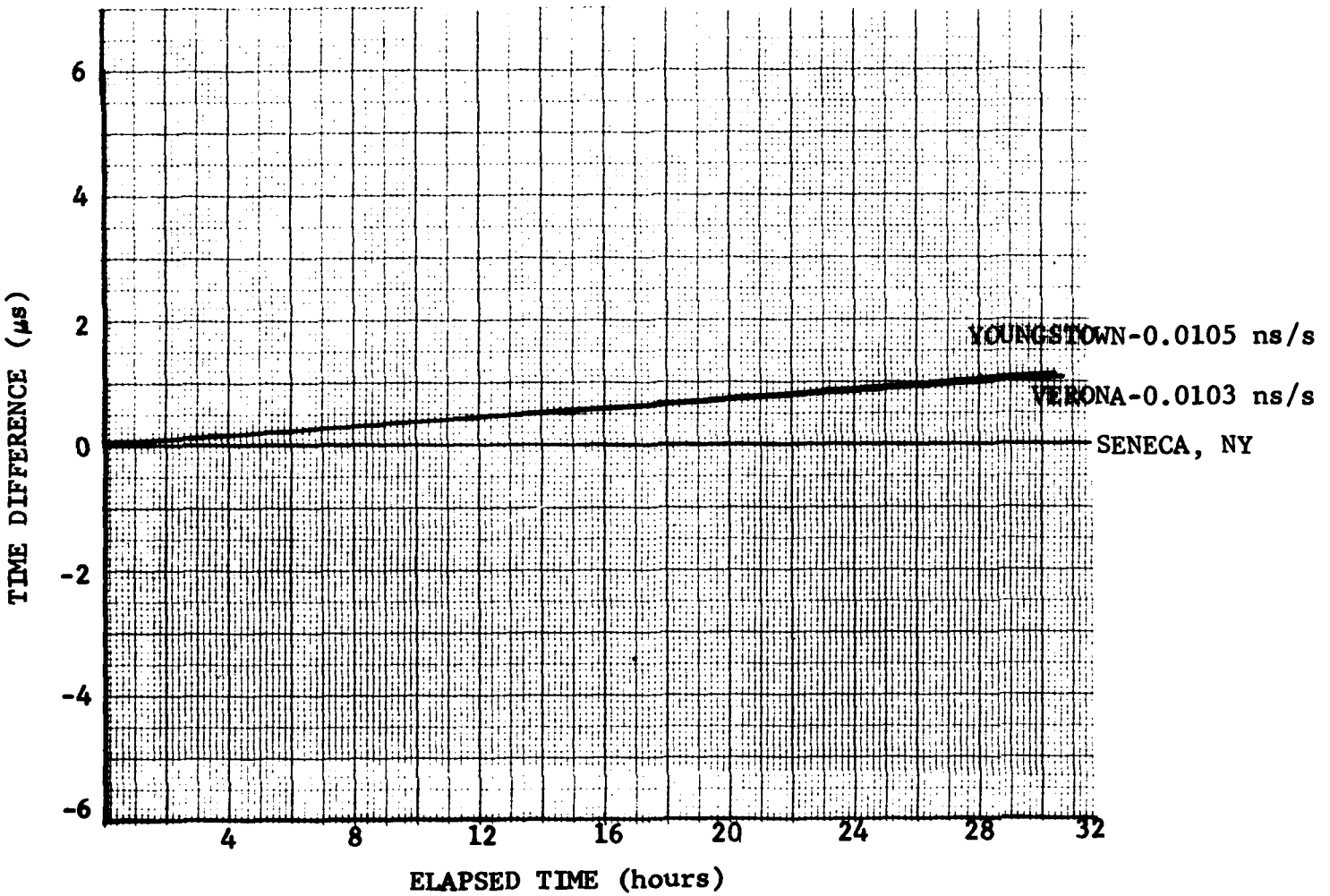


Figure 5.11 Seneca, NY, vs. Youngstown and Verona (Master/Slave TROPO)

difference between the sites is probably due to cumulative roundoff errors in the sample averages and the linear regression process. No attempt was made to detail short-term fluctuations and perturbations because many of these effects are lost in longer-term averages computed by both the TS and the FMT. As a result, we wish only to point out the overall trends of the nodes as compared to an outside reference. With this in mind, Master/Slave over TROPO links results in very acceptable frequency alignment.

5.5.2 Two-Node Master/Slave (LOS)

A similar Master/Slave experiment was conducted over the LOS microwave link. This was a single-ended experiment with Verona as master and GAFB as slave. Figure 5.12 shows the network equipment connections. Run duration was approximately 40 hours at which point power was lost at Verona and an indefinite coast was observed at the slave site (GAFB). This behavior would be typical of that of a stressed network. When the master is lost, all subservient nodes must rely on past clock correction history (retained in PLL memory) rather than ceasing operation. This usually results in better performance than no clock corrections at all.

Figure 5.13 depicts the relative frequency of each site compared to the Seneca reference. The master clock (Verona) was disciplined to follow the site rubidium standard. This was a logical choice because the history of the rubidium's performance compared to Seneca was already known, so its drift could be predicted after power was lost. The frequency plots are purposely smoothed by regression to better visualize the longer-term trends. Unfortunately, time did not permit longer run durations but, clearly, the experiment was a success and satisfactory frequency alignment was obtained.

5.5.3 Three-Node Tandem Master/Slave

A single-ended tandem network was configured according to the diagram in Figure 5.14. With Youngstown as master, timing control was in the Youngstown-Verona-GAFB direction. Expected performance would be the following: Each slave node should discipline its clock so that the sum of the frequency offset of the rubidium standard plus that of the Timing Subsystem should equal the frequency offset of the Youngstown rubidium (all referenced to the Seneca LORAN-C pulses). This was observed during a

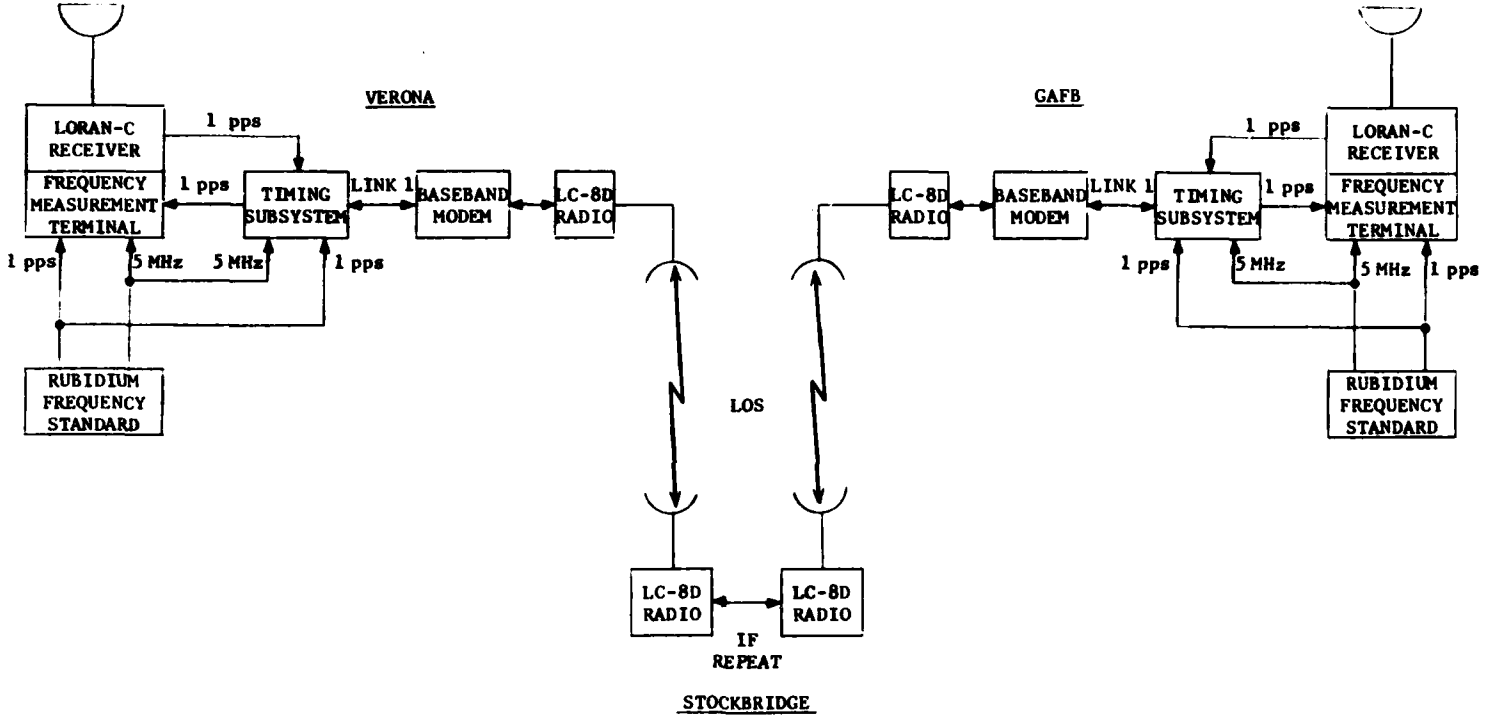


Figure 5.12 Two-Node Network with LOS Link (Verona-Stockbridge-GAFB)

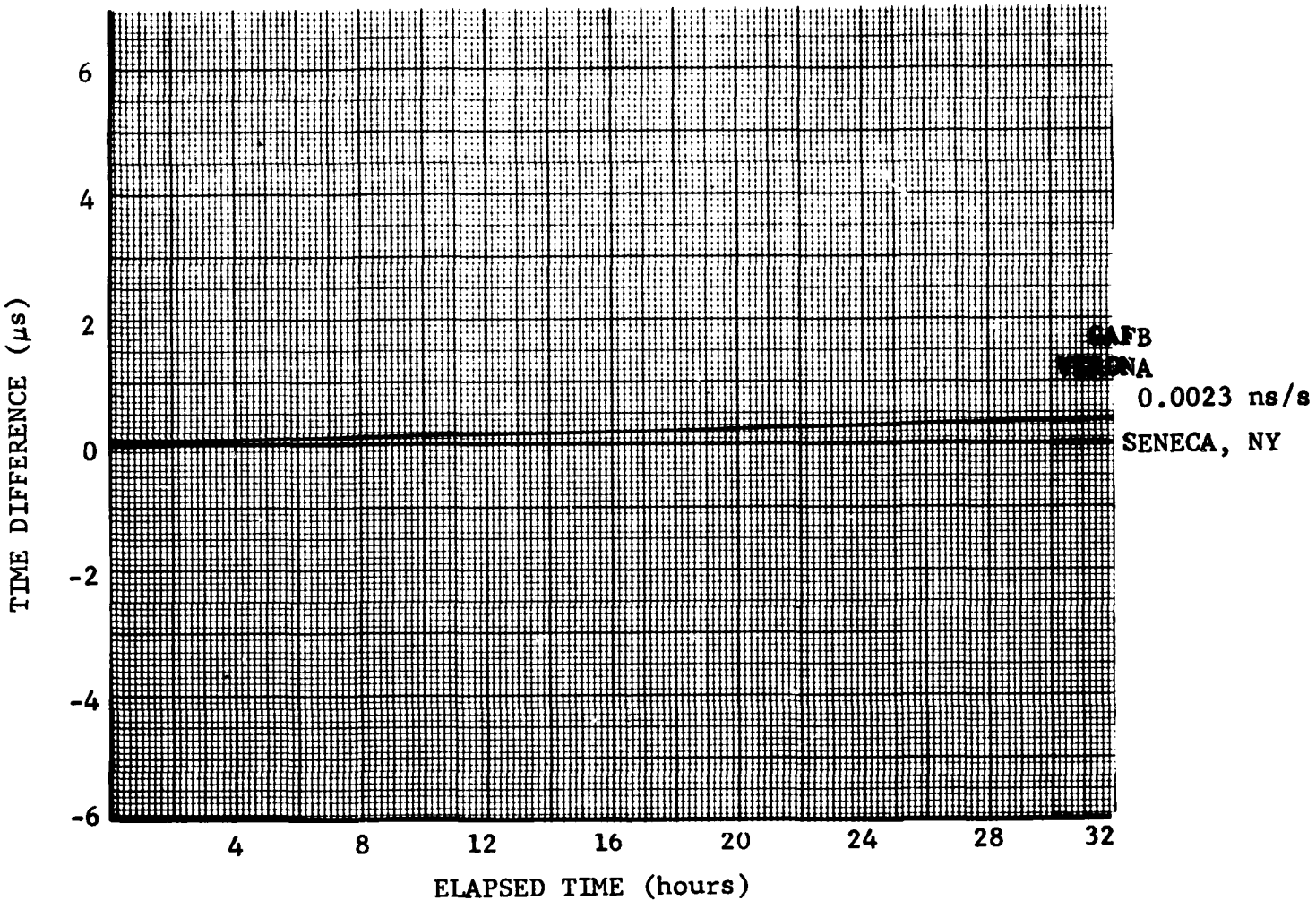


Figure 5.13 Seneca, NY, vs. Verona and GAFB (Master/Slave LOS)

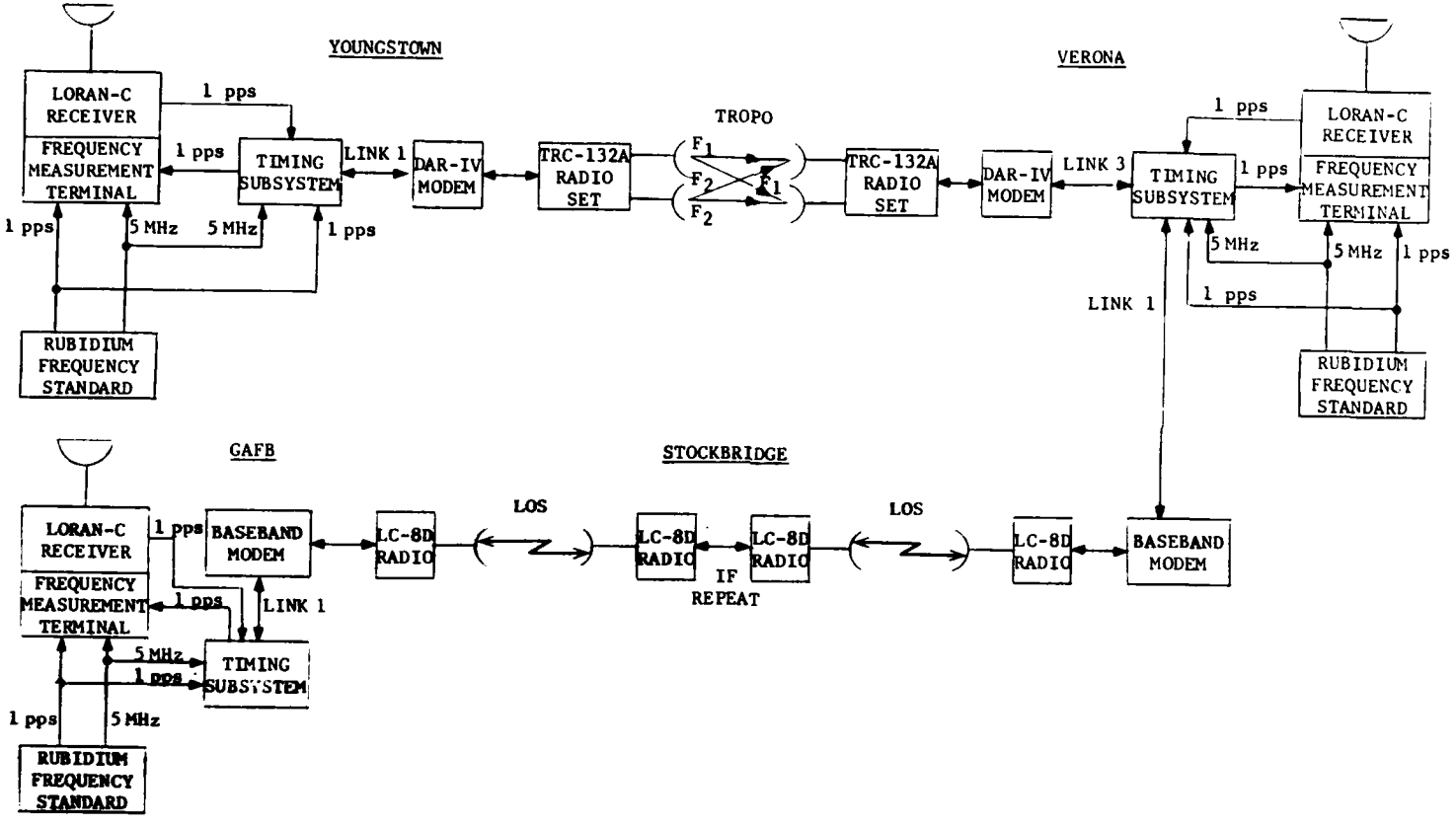


Figure 5.14 Three-Node Tandem Network with LOS and TROPO Links

32-hour run, the results of which are plotted in Figure 5.15. It is evident that each of the slave nodes had sufficiently altered the frequency of the site standard so that they were closely following the master's frequency. No detectable frequency offset was found, at least to the limits of the measurement facilities (about one part in 10^8 on a per-second basis). Both slave nodes closely followed the frequency offset of the Youngstown master as compared to the Seneca LORAN-C transmissions. This plot merely presents the frequency trends of each node; it is not intended to detail small fluctuations in clock frequency. The primary reason for this smoothing is dictated by the averaging techniques used by the Timing Subsystem and the Frequency Measurement Terminal; that is, short-term fluctuations in clock adjustments are masked by the averaging which combines hundreds of samples over a known interval. Essentially, a long-term (four hours) average, as used in the FMT, is suitable for comparing long-term frequency offsets.

5.5.4 Three-Node Tandem Time Reference Distribution

The TRD experiment demonstrated the performance of the original TRD technique as described in [5.5]. Since the Improved TRD technique was meant to be used with double-ended transfers, it was not attempted; however, indications are that it would behave similarly to TRD with perhaps small improvements in phase accuracy. The Test Bed measurement facilities were not equipped to measure node-to-node precise phase conveniently.

Each node in the tandem network was assigned a unique rank with Youngstown being the highest ranking clock, Verona second, and GAFB third. This was not an arbitrary assignment because the use of single-ended transfers dictated the direction of control, being from Youngstown to Verona to GAFB. In addition, the transmission links were assigned a demerit rating with the LOS link being rated about five times better than the TROPO link. Both clock and link ratings are integer quantities so that choosing a specific value is secondary with respect to choosing a precedence.

With the node parameters determined, the network was instructed to begin operation. It was immediately observed, through inspection of incoming link data, that a network hierarchy was formed in just several iterations (e.g., several seconds). Once in steady-state operation, the network behaved identically to the three-node Master/Slave experiment just

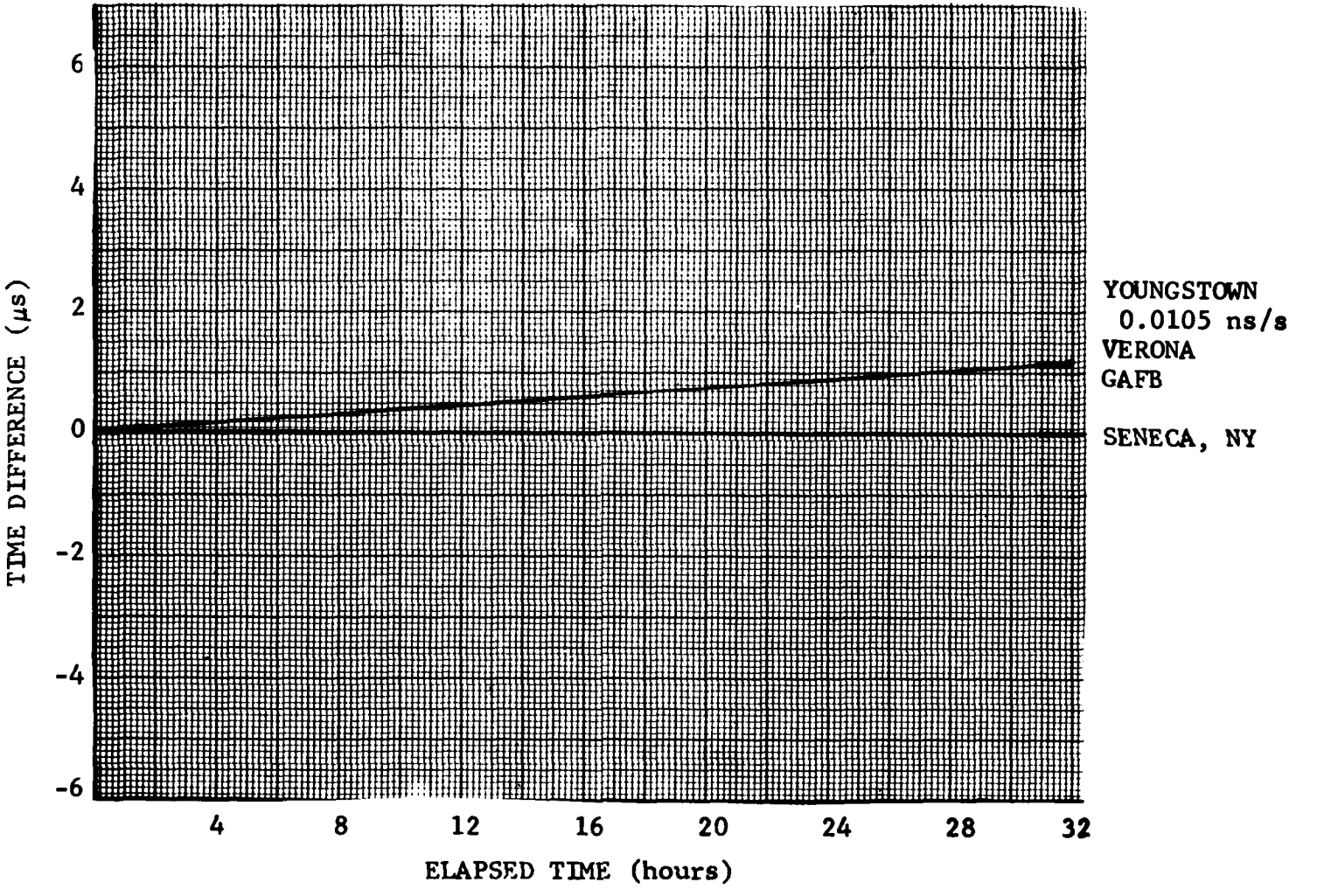


Figure 5.15 Three-Node Tandem Master/Slave Performance Curves

described. It would be expected that TRD should have improved accuracy over simple M/S (by virtue of combining the computed error of the node's neighbor with its own), but this was not detectable with the available performance assessment equipment. Certainly, as shown in the plot in Figure 5.16, three-node tandem TRD performed at least as well as the similar M/S experiment. Each slave node had adjusted its clock to be equal in frequency to that of the network master (Youngstown) node.

5.5.5 Three-Node Tandem Master/Slave; Master with Large Frequency Offset

Perhaps the most demanding experiment in terms of clock correction capability, three-node tandem Master/Slave with the master incorporating a large frequency offset, demonstrated network behavior under slightly less than ideal conditions. The network configuration was identical to that pictured in Figure 5.14 and nodal parameters identical to the first tandem M/S experiment described in Section 5.5.3. In addition, the Youngstown node (master) was instructed to slew its clock at 2.7994 ns/s (arbitrary) through the phase microstepper. This added frequency offset would enhance measurements by moving away from the zero frequency offset region. Remember that Seneca was chosen as the Test Bed master and that each site's rubidium standard frequency offset was known a-priori. The extra offset will make the frequency differences between each site's rubidium standard and Seneca more pronounced, thus facilitating performance assessment procedures.

Figure 5.17 shows the frequency of each node (obviously identical) compared with the Seneca LORAN-C. Note the change of scale on the vertical time difference axis. This shows quite a substantial (about three parts in 10^8) frequency offset from the normally free-running frequency standard at Youngstown. The experiment demonstrated that each slave node also adjusted the frequency of its clock to match that of the master. Note that the maximum adjustment range for the phase microsteppers used in this experiment is ± 100 ns/s, or one part in 10^7 per second; that is, the device is capable of handling quite a large frequency range.

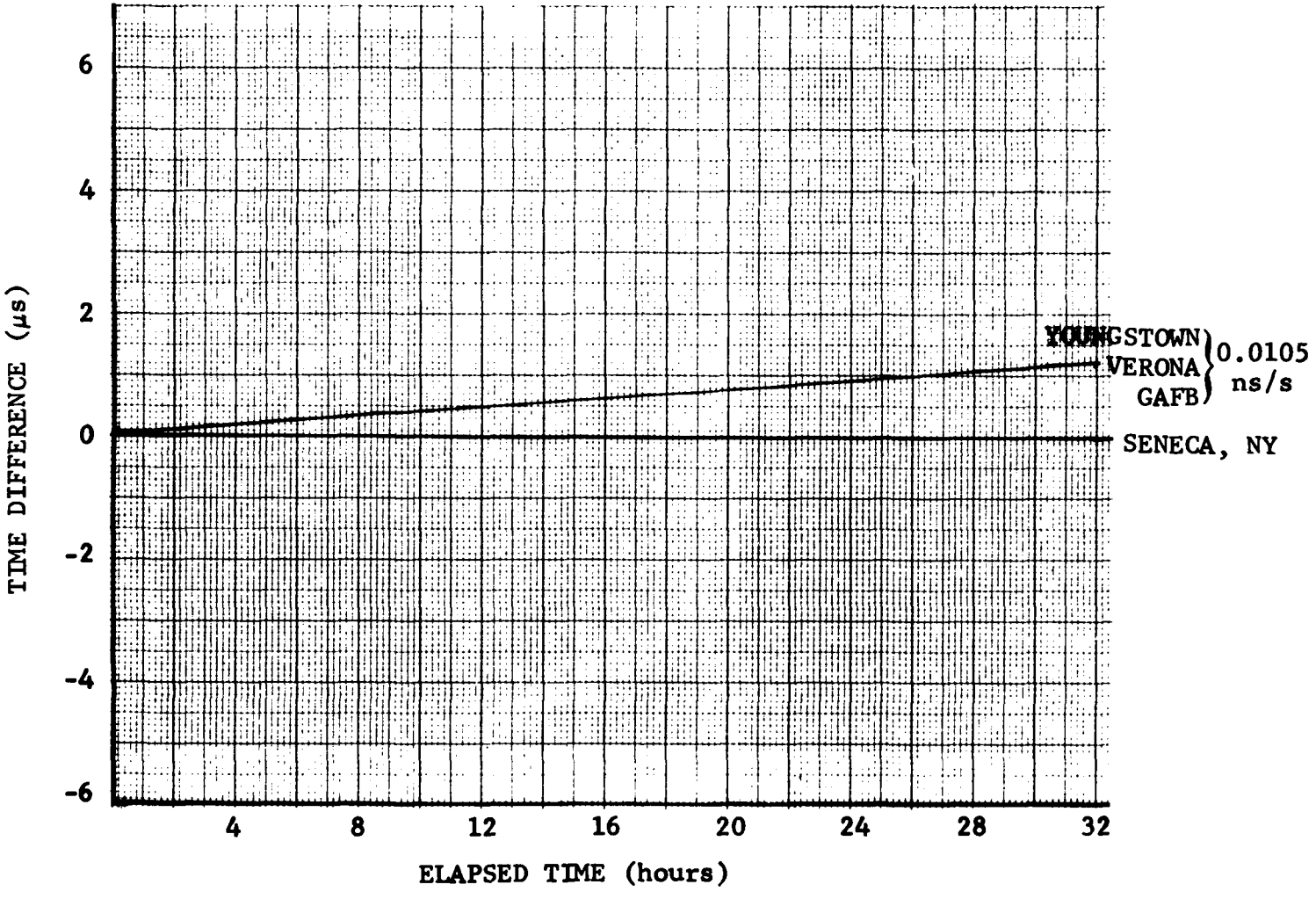


Figure 5.16 Three-Node Tandem Time Reference Distribution Performance Curves

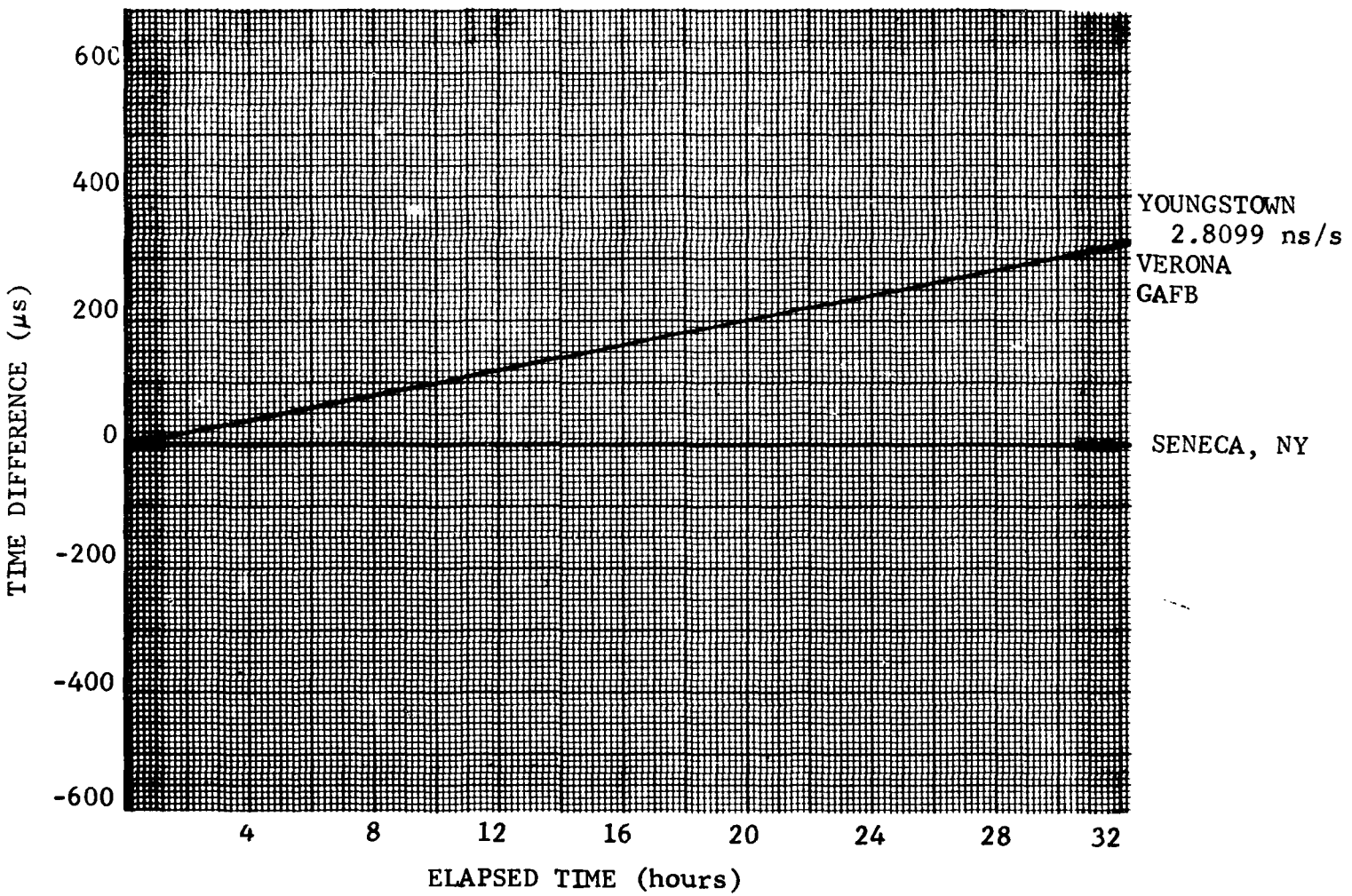


Figure 5.17 Three-Node Tandem Master/Slave with Large Drift Performance Curves

5.5.6 Three-Node Tandem Master/Slave with Slave VCO

This final experiment called for the use of an adjustable VCO for slave clock alignment instead of the rubidium frequency standard and phase microstepper combination. The VCO was selected as an option and a cost-reducing method of adjusting the node frequency. The VCO and associated D/A hardware are contained within the Timing Subsystem. Clock corrections were made via an algorithm relating the adjustment voltage to the resulting frequency change. Two Timing Subsystems were built with VCO hardware included, but only the GAFB machine was configured as a slave VCO in the tandem M/S experiment. Nodal software accommodated both methods all of the time by sending control words to both phase microstepper and VCO ports whether they were connected or not.

Before presenting a brief comparison of the two clock adjustment techniques, refer to Figure 5.18 for the performance curves for this experiment. Note that each node again has tracked the master (Youngstown) frequency, including the large offset dialed in for the previous experiment. It seems that the VCO performed admirably even with a large frequency difference to correct for. Noticeable short-term variations were observed by connecting a scope to the node adjusted and unadjusted frequencies and comparing the relative drift between them. Actually, the short-term instability can be readily accounted for although we did not attempt to plot them because of the inherent uncertainty from the long averages employed by the performance measurement system. Overall, the frequency trends of each node are quite in line with the expected results.

To clarify the mechanism responsible for short-term VCO variations, refer to the frequency adjustment range plot (Figure 5.19) of a typical VCO used in the TS design. Notice that the transfer is nonlinear overall, but may be considered piecewise linear between any two points within, say, one volt of each other. Ideally, to maximize the accuracy of the clock adjustment scheme, the frequency vs. voltage characteristic should be carefully measured and plotted, a transfer function derived, and a "smart" software driver designed to provide control from given error calculations. However, no two VCO crystals exhibit exactly the same transfer characteristics or, for that matter, have the same range or center frequency. Therefore, at best, implementing the VCO control software is a compromise; but, as described earlier, satisfactory performance can be achieved

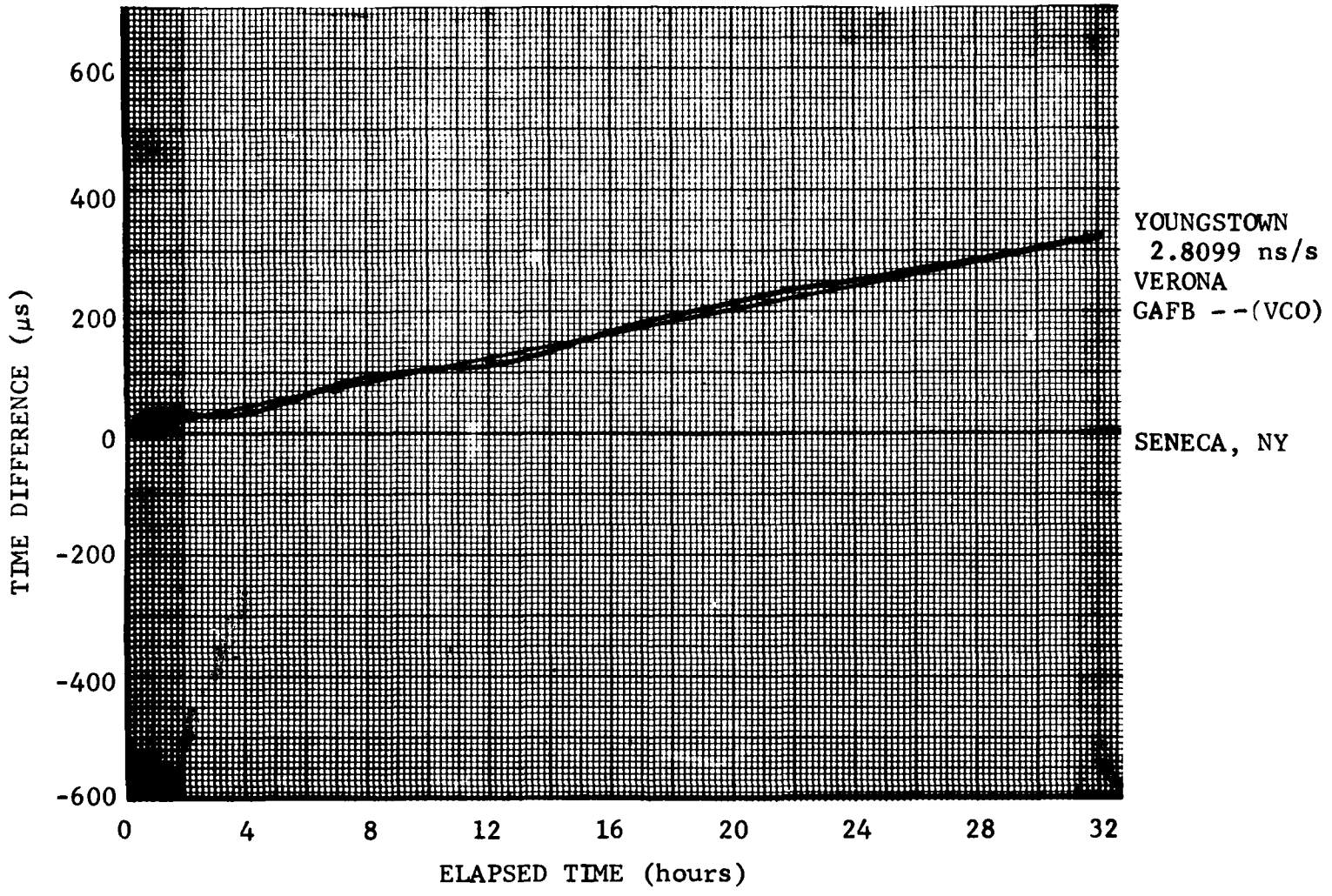


Figure 5.18 Three-Node Tandem Master/Slave with Slave VCO

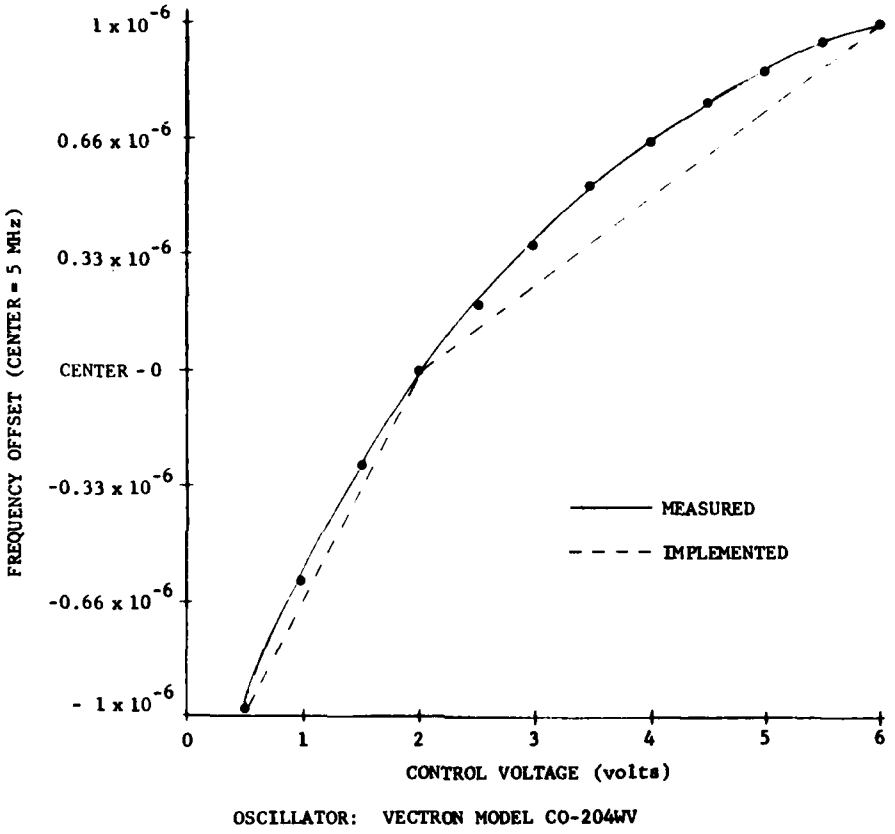


Figure 5.19 Useful Adjustment Range of Voltage-Controlled Oscillator

at minimal cost. Actually, it was decided to describe the VCO transfer characteristics as two linear segments of different slopes, intersecting at the center frequency, as shown by the dotted lines in Figure 5.19. Actual error was maximum at the midpoint of each of these segments. One of the primary reasons for describing the VCO characteristics this way was to minimize software overhead. It was imagined that most of the corrections would be at, or near, the center frequency, thus reducing the computational burden and eliminating much of the interpolation process needed when off-center. Also, frequency corrections are made on a relative basis to avoid glitches caused if the computer were to set the VCO by starting at either boundary (for a baseline reference) and stepping the desired number of counts. The relative move technique insured smooth adjustments each iteration. Overall, the approach and implementation were selected to reduce software overhead while maintaining a satisfactory level of performance. In that light, it was a successful endeavor.

Table 5-2 highlights some of the features of both the phase microstepper and VCO methods of clock adjustment. Notice that there is a significant cost differential between the devices and that the microstepper requires an external frequency source as well. This factor alone is of enough importance to lead us to the recommendation (see Section 6) that VCO's be used at all less important nodes, or at least at sites where a frequency standard is not already present.

5.6 Interpretation of Test Results

In this section we summarize the findings of each of the six experiments held with two-node and three-node networks. A brief account of the methodology used to determine network performance is also described. Included are several tables: a node parameter summary for each experiment; and a summary of frequency offsets of each node compared to the Test Bed master 1 pps from Seneca. The latter table discloses the undisciplined (free-running) frequency offset of each site standard compared to Seneca, as well as disciplined clock frequency offsets during experiment runs.

Armed with this information, the reader should review the performance curves in Section 5.5 and compare disciplined and undisciplined clock frequency offsets relative to the Test Bed master. An example of an experiment evaluation session highlights Section 5.6.1.

TABLE 5-2

COMPARISON OF CLOCK ADJUSTMENT TECHNIQUES

Specification	Phase Microstepper*	Voltage-Controlled Oscillator**
Resolution	1×10^{-13}	6.4×10^{-11}†
Accuracy	1×10^{-9}	-
Maximum Slew Rate	±100 ns/s	±160 ns/s
Total Dynamic Range	1×10^{6}	2.5×10^{3}
Control Word Format	6-Decade BCD	12-Bit Binary
CPU Control Method	Parallel I/O to Phase Microstepper	Parallel I/O to D/A Converter to Oscillator
Cost	$ 3500††	Approx. $ 500+

NOTES:

*Phase Microstepper is Austron Model 2055A

**Voltage-Controlled Oscillator is Vectron Model CO-204WV

†12-bit D/A conversion for control voltage

††Requires external frequency source

+Requires D/A conversion circuitry for CPU control

Finally, Section 5.6 closes with a brief review of time transfer requirements (including clock error and path delay calculations) for network synchronization.

5.6.1 Summary of Field Tests

In order to simplify the presentation of the network experiment series described in Section 5.5, the reader is referred to several tables and diagrams. Table 5-3 contains a glossary of terms used in describing network configurations and parameters. Note that the use of the VCO implies that the frequency source is contained with the Timing Subsystem, and no external reference need be applied. Performance measurement is carried out as normal using the site rubidium standard as the time interval measurement driver for the FMT. The VCO was used only on the GAFB subsystem. All others used an external 5-MHz reference supplied by the site rubidium standard.

Figure 5.20 summarizes the network configurations for each experiment. These diagrams show the nodal frequency sources, clock adjustment technique, and the path of directed control. For the TRD experiment, clock ranks and link demerits are also shown.

A list of nodal and network parameters are located in Table 5-4. Notice the delay figures listed. These are based on actual equipment delay measurements, but their use in frequency alignment experiments is optional. This is the case for all of the experiments conducted at RADC. TRD is capable of phase tracking, but it was not evaluated in this manner.

The Seneca, NY, LORAN-C station was considered to be the Test Bed master. This station is a slave to the Dana, IN, east coast chain master. Since experiments were concerned with frequency alignment, the first step to calibrate the network was to measure the frequency offset of each of the three site rubidium standards and to compare them to the cesium beam standard at Seneca. Through the Frequency Measurement Terminals, located at Youngstown, Verona, and Griffiss AFB, we were able to plot long-term frequency offset for each rubidium standard. The standard was used as a driving (source) 1 pps in each case, thus providing a direct comparison of received, LORAN-C, and rubidium outputs. The results of this measurement series is plotted in Figure 5.21. Notice that data was gathered over a period of about eight days through averages from the FMT. With Seneca

TABLE 5-3

GLOSSARY OF TERMS FOR NETWORK EXPERIMENTS

D - Link Demerit for TRD

DE - Double-Ended Time Transfer

FMT - Frequency Measurement Terminal

G - Griffiss Air Force Base Node

IC - Independent Clock Timing Technique

I/TRD - Improved Time Reference Distribution Timing Technique

L[n] - Timing Subsystem Link #

LOCAL - Internally-generated Frequency Source (within TS)

LOS - Line-of-Sight Microwave Link

M/S - Master/Slave Timing Technique

MS - Mutual Synchronization Timing Technique

MSTEP - Phase Microstepper

N - Node

Rb - Rudidium Frequency Standard

SE - Single-Ended Time Transfer

T - Tandem Network Configuration

TRD - Time Reference Distribution Timing Technique

TRIP - Time Reference Information Packet

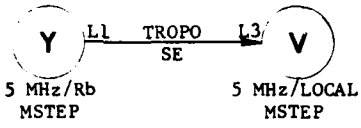
TROPO - Troposcatter Link

V - Verona Node

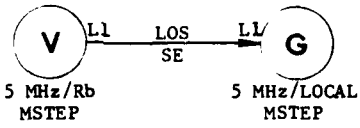
VCO - Adjustable Oscillator Internal to Timing Subsystem

Y - Youngstown Node

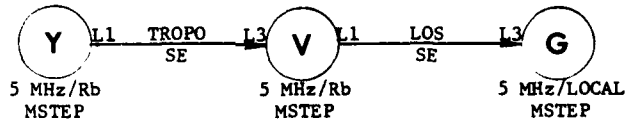
EXPERIMENT (1). TWO-NODE M/S



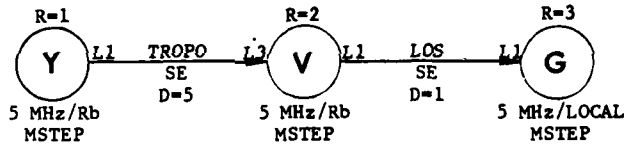
EXPERIMENT (2): TWO-NODE M/S



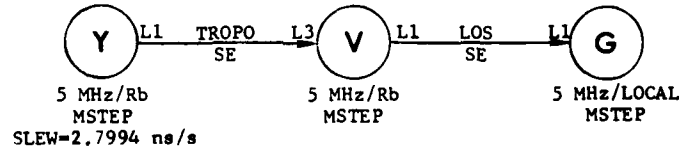
EXPERIMENT (3): THREE-NODE TANDEM M/S



EXPERIMENT (4): THREE-NODE TANDEM TIME REFERENCE DISTRIBUTION



EXPERIMENT (5): THREE-NODE TANDEM M/S: MASTER WITH LARGE FREQUENCY OFFSET



EXPERIMENT (6): THREE-NODE TANDEM M/S WITH REMOTE SLAVE QUARTZ OSCILLATOR

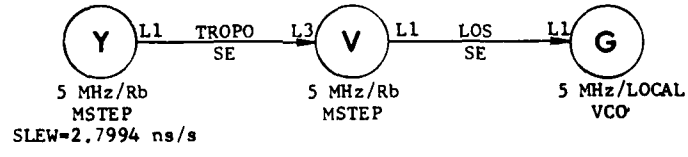


Figure 5.20 Summary of Network Configurations

TABLE 5-4

SUMMARY OF NETWORK PARAMETERS FOR FIELD TESTS

	EXP #	TYPE	SE LINK(S)	TS FREQ SOURCE	PHASE ADJUST	DIRECTED CONTROL	DELAY FIGURE (μs)			LOOP PARAMETERS		RUN LENGTH HRS.	MISC.
							LINK 1	LINK 2	LINK 3	τ	k		
YOUNGSTOWN	1	2N-M/S	TROPO	5 MHz/Rb	MSTEP	Y → V	-507.07	N/A	N/A	10	2×10^{-2}	36	Slaved to site rubidium
	2	NOT USED											
	3	3N-T-M/S	TROPO/LOS	5 MHz/Rb	MSTEP	Y → V → G	-507.07	N/A	N/A	10	2×10^{-2}	24	Prop Delay = 910.70 μs
	4	3N-T-TRD	TROPO/LOS	5 MHz/RB	MSTEP	Y → V → G	-507.07	N/A	N/A	10	2×10^{-2}	18	L1:D = 5
	5	3N-T-M/S	TROPO/LOS	5 MHz/Rb	MSTEP	Y → V → G	-507.07	N/A	N/A	10	2×10^{-2}	20	Master Slew at 2.799 ns/s
	6	3N-T-M/S	TROPO/LOS	5 MHz/Rb	MSTEP	Y → V → G	-507.07	N/A	N/A	10	2×10^{-2}	24	Master Slew at 2.799 ns/s
VERONA	1	2N-M/S	TROPO	5 MHz/Rb	MSTEP	Y → V	505.95	N/A	-507.20	10	2×10^{-2}	36	Master Slew at 2.799 ns/s
	2	2N-M/S	LOS	5 MHz/Rb	MSTEP	Y → G	505.95	N/A	-507.20	10	2×10^{-2}	40	Power failure at 40 hours
	3	3N-T-M/S	TROPO/LOS	5 MHz/Rb	MSTEP	Y → V → G	505.95	N/A	-507.20	10	2×10^{-2}	24	
	4	3N-T-TRD	TROPO/LOS	5 MHz/Rb	MSTEP	Y → V → G	505.95	N/A	-507.20	10	2×10^{-2}	18	L1:D = 1, L3:D = 5
	5	3N-T-M/S	TROPO/LOS	5 MHz/Rb	MSTEP	Y → V → G	505.95	N/A	-507.20	10	2×10^{-2}	20	
	6	3N-T-M/S	TROPO/LOS	5 MHz/Rb	MSTEP	Y → V → G	505.95	N/A	-507.20	10	2×10^{-2}	22	Verona slaved to site rubidium
GAFB	1	NOT USED											
	2	2N-M/S	LOS	5 MHz/Local	MSTEP	V → G	-505.52	N/A	N/A	10	2×10^{-2}	40	Master lost at 40 Hours
	3	3N-T-M/S	TROPO/LOS	5 MHz/Local	MSTEP	Y → V → G	-505.52	N/A	N/A	10	2×10^{-2}	24	
	4	3N-T-TRD	TROPO/LOS	5 MHz/Local	MSTEP	Y → V → G	-505.52	N/A	N/A	10	2×10^{-2}	18	L1:D = 5
	5	3N-T-M/S	TROPO/LOS	5 MHz/Local	MSTEP	Y → V → G	-505.52	N/A	N/A	10	2×10^{-2}	20	Master Slew at 2.799 ns/s
	6	3N-T-M/S	TROPO/LOS	5 MHz/Local	MSTEP	Y → V → G	-505.52	N/A	N/A	10	2×10^{-2}	22	GAFB uses local VCO

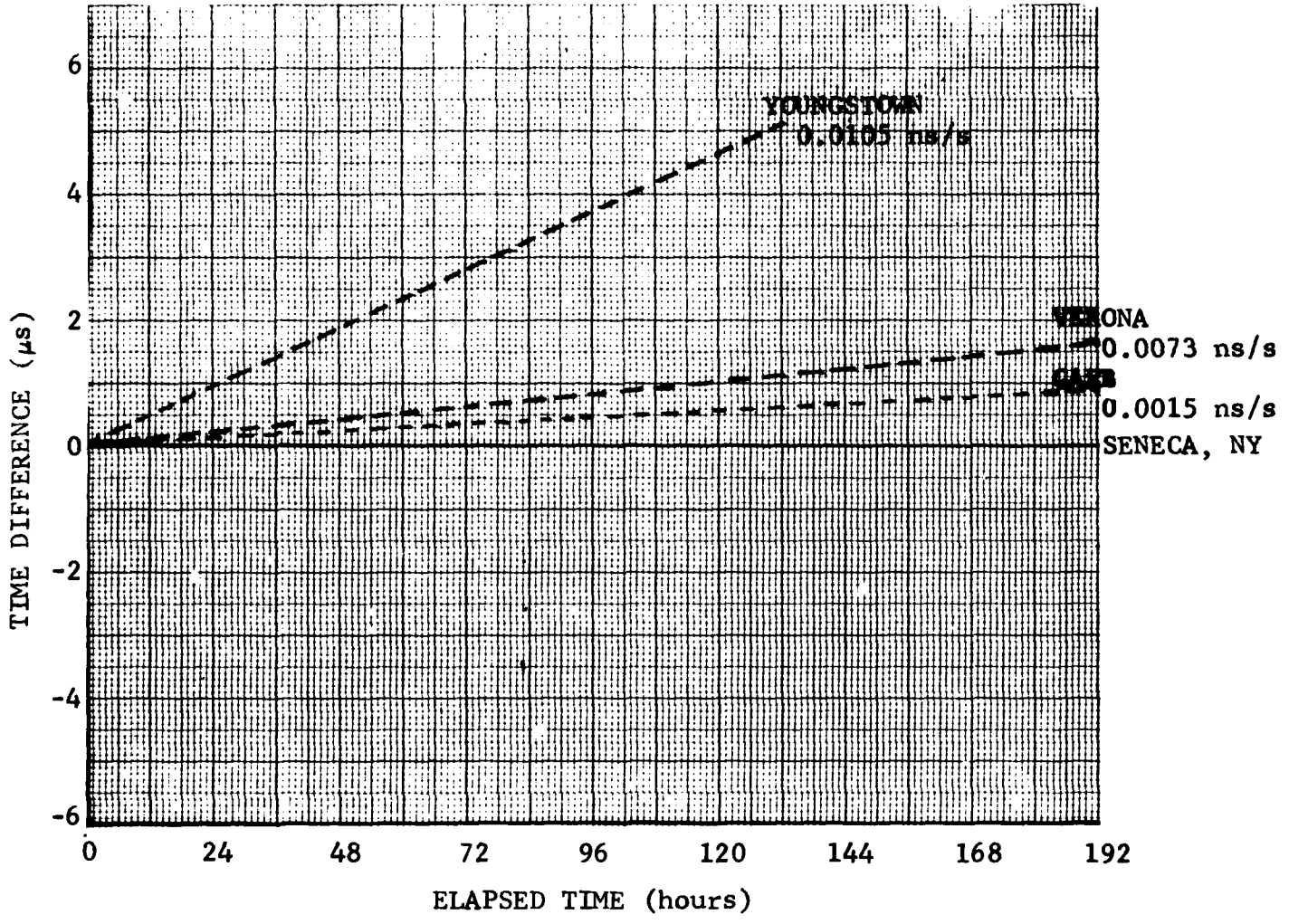


Figure 5.21 Seneca, NY, LORAN-C Station Cesium Frequency Standard vs. Test Bed Rubidium Frequency Standards

as a reference (i.e., zero frequency offset), the relative drift rates of each of the sites is plotted. Small variations are smoothed and incorporated in these "best fit" frequency trend lines. Notice that all rubidium standards are drifting in the same direction. This frequency comparison is the basis for evaluating node performance through measurements at any location. This is especially important since the rubidium standards are the reference for each site, and two of the three Timing Subsystems (not GAFB) use them directly as an external timing source. All TS performance assessment measurements are made relative to the site standards.

Typically, an experiment evaluation session would proceed as follows:

- Select a Test Bed master through which the performance of each node may be compared.
- Determine the frequency offset of each site frequency standard compared to the Test Bed master.
- Configure the network for a timing experiment including node parameters and connections for performance assessment measurements.
- Allow experiment to run for at least 24 hours so that acquisitional effects, and other short-term perturbations, do not significantly affect the measurement series.
- Compare the time interval measurements of the Timing Subsystem adjustable clock with those of the free-running node frequency standard. These measurements can be collected through either the FMT or TS, or both.
- Plot the frequency offset between the TS adjusted clock and the site standard (maintain directionality).
- Add or subtract the frequency offset of the site standard as compared to the Test Bed Master. The result is the total frequency offset of the TS adjusted clock as compared to the Test Bed Master. Frequency comparisons may be either node-to-node or node-to-Test Bed Master.

This technique is precisely that used to present node evaluation data in Section 5.5. Table 5-5 summarizes the performance of the network synchronization tests. Notice, in directed control experiments, that all nodes run at the same total offset compared to the Test Bed master, and that all slave nodes run at zero frequency offset compared to the network master. This is also true for experiments 5 and 6 where a large frequency offset was incorporated into the master node. Nodal performance may be ultimately compared to time standards at NBS, but this exercise is left to the reader. A plot of LORAN-C performance, compared to the U.S. National Time Standard (NBS-6), is shown in Figure 5.22. This plot covers the time period over which the experiments were run (except experiment 1). These readings, however, are compared to the Dana, IN, LORAN-C station, and interpreting time at Seneca would require published phase delay tables and additional calculations. It is not necessary to go to this amount of trouble unless the operator intended to verify precise time tracking directly.

5.6.2 System Time Transfer

The material in the previous section indicates that, for normal communication requirements, relative time synchronization of the nodes is sufficient, i.e., the node clocks need not be phased identically as long as their mutual average frequency offsets are zero. On the other hand, transfer of a time reference throughout a network is equivalent to the requirement that node clocks be synchronized with zero phase offset; and with the additional ability to remove ambiguity, the aligned clocks serve as the basis for a time-of-day distribution system.

A brief review of the parameters involved in system-wide time transfer will first be given; more specific accounts of time transfer methods are given later in this section. Consider, in particular, the transfer of time over a single link as depicted in Figure 5.23. In this example, a troposcatter propagation path is shown but, of course, other transmission media are of direct applicability.

The primary function of the link is the transfer of digital data between the nodes in both directions. At any node, incoming data is clocked into a buffer by clock signals derived from the receiver-demodulator bit tracking loop. This clock signal exhibits fluctuations and drift behavior as a result of transmit clock variations, medium variability, and tracking loop dynamics.

TABLE 5-5

SUMMARY OF NETWORK SYNCHRONIZATION PERFORMANCE*

		FREQUENCY OFFSET AS COMPARED TO LORAN-C SENECA, NY		
EXPERIMENT	TYPE	YOUNGSTOWN	VERONA	GAFB
Site Standard	Free Running Rubidium Standard	1.05×10^{-11}	7.3×10^{-12}	1.5×10^{-12}
1	2N-M/S	1.05×10^{-11} (Master)	1.03×10^{-11}	--
2	2N-M/S	--	2.3×10^{-12} (Master)	2.3×10^{-12}
3	3N-T-M/S	1.05×10^{-11} (Master)	1.05×10^{-11}	1.05×10^{-11}
4	3N-T-TRD	1.05×10^{-11} (Master)	1.05×10^{-11}	1.05×10^{-11}
5	3N-T-M/S Master-Lrg. Freq. Offset	2.8099×10^{-9} (Master)	2.8×10^{-9}	2.8×10^{-9}
6	3N-T-M/S Slave VCO	2.8099×10^{-9} (Master)	2.8×10^{-9}	2.81×10^{-9}

*Read across to determine node-to-node frequency offset.

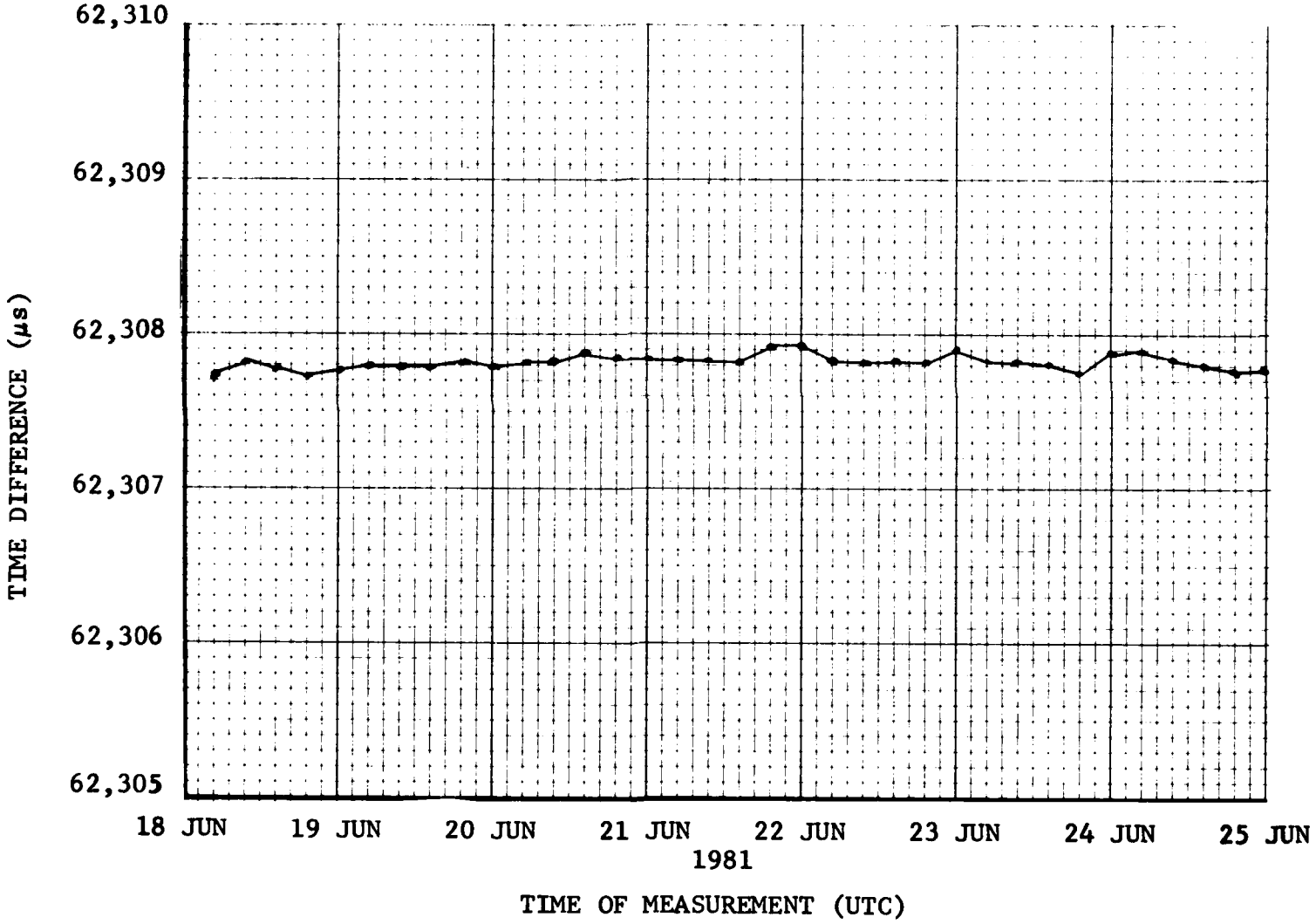
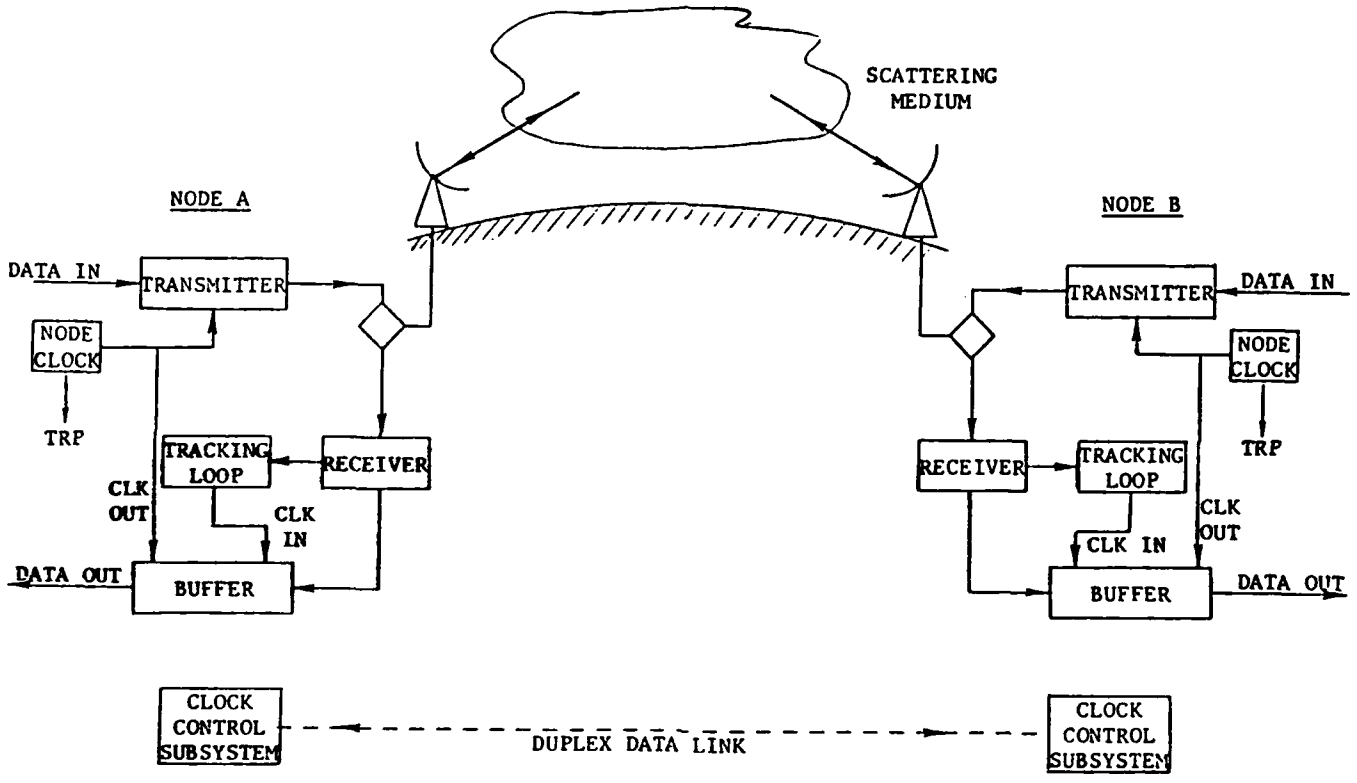


Figure 5.22 LORAN-C; Dana, IN, vs. U.S. National Time Standard NBS, Boulder, CO (NBS-6)



TRP = CONCEPTUAL TIME REFERENCE PULSE

Figure 5.23 Block Diagram of a Digital Troposcatter Link

In a synchronous network, the received data is later clocked out of the buffer by the node clock and multiplexed or switched with data from other terminated links for retransmission; the primary objective is to coordinate the collection of node clocks so that the buffers do not overflow or deplete. In addition, a time-keeping function for the node clock would involve the desire to meet the above objective with zero phase offset between the node clocks. Time is kept by the clocks at each end of the link in terms of a periodic sequence of time reference pulses (TRP's) which are synchronous with the high-rate data clock. If ambiguity issues are ignored in this discussion, it can be simply stated that the time transfer objective is to align the two TRP transmissions. At node B, this is achieved by comparing the arrival time of a pulse transmitted from node A with the locally-generated pulse time, i.e., the node B clock pulse. Time transfer from A to B can then be implemented using this measurement, denoted t_A, in one of two ways:

(1) Single-ended transfer, where t_A is viewed as a combination of clock offset, average path/equipment delay, plus a zero mean fluctuating component. That is, if the average delay through the link is known a-priori, sufficient averaging of t_A should yield the clock offset and allow a correction to be made.

(2) Double-ended transfers, where a similar measurement, denoted t_B, is carried out at node A, and the quantities t_A and t_B are exchanged by the two nodes. The difference parameter t_A-t_B, computed at either or both ends, is then proportional to the clock offset, provided the transmission time is identical in both directions. To the extent that this is true, t_A-t_B may be used directly as a clock correction signal.

In both of these situations, the medium and equipment delay variations control the time transfer accuracy. For single-ended systems, variability around a long-term mean, in terms of both magnitude and spectral width, is the essential ingredient. Double-ended transfer methods depend for their success on similar parameters expressed instead in terms of bidirectional path delay differences; namely, the time structure and magnitude of the difference, along with residual biases which are not accounted for a-priori.

It should be emphasized that the clock updating procedure is usually carried out with quite long averages of the measured arrival time data, ranging from day-long averages to hundreds of seconds for quartz standards. Thus, the short-term medium effects will be virtually eliminated. Assume for the moment, then, that the clocks at either end are aligned and much more stable than the incoming TRP signal which is perturbed on an instantaneous basis by the medium fluctuations. With this situation, the path delay itself can be established and, if variable, tracked in time. In the event of link disruptions, the demultiplexers and decryption units may lose sync, and the availability of a network time reference at the node is available to support the reframing operation.

To further detail the basic error computation chores for each node in a network, a brief but concise account of clock error and path delay calculations for single- and double-ended TRIP exchanges is presented. Refer to Section 2.1.1 for the format of each data package (TRIP) as sent between nodes.

The ultimate node reference signal is the 1 pps derived from the on-site phase-shifted frequency standard. Remember that the network time synchronization objective is the alignment of all such 1-pps references throughout the system. In Master/Slave and Mutual Sync approaches, the relative variation of the 1 pps after buffer reset is the important consideration; that is, absolute phase or time relationships are unimportant throughout the network, but accumulated phase variations are indicative of buffer fullness. Therefore, controlling one will control the other if the station clock frequencies all originate from the corrected station standard.

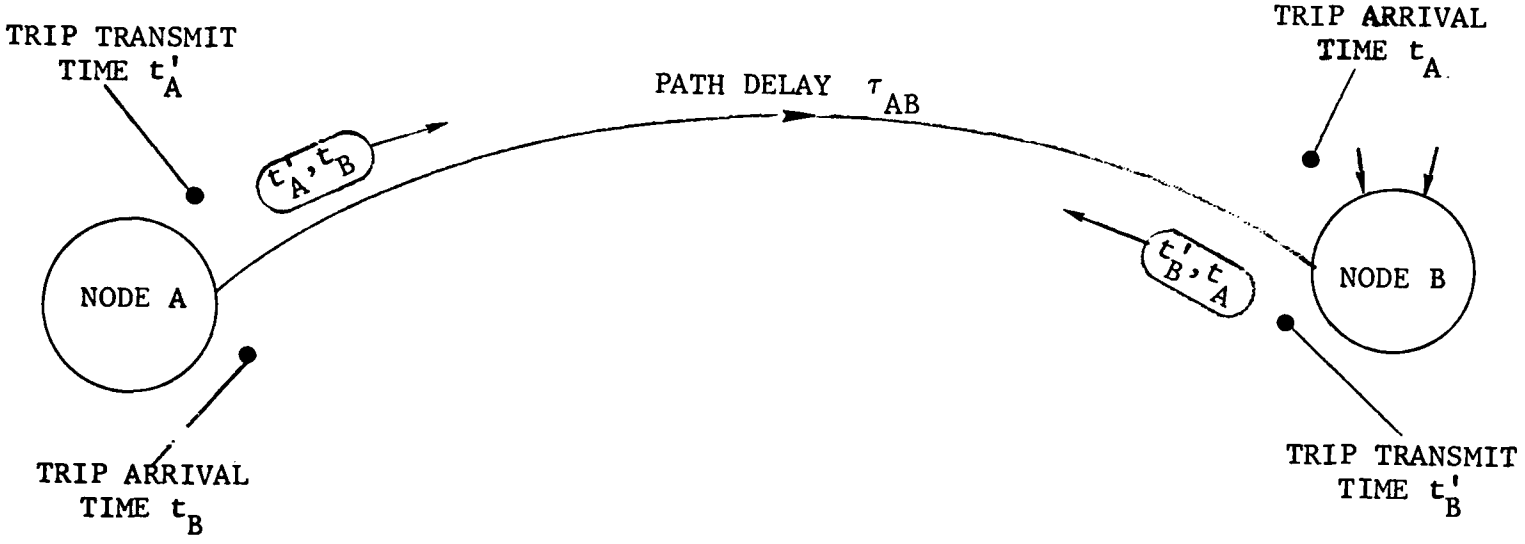
Determining clock error depends on the synchronization technique specified but, as a general rule, it will consist of elapsed time measurements from the other end of the link (from a given node) as well as locally-made time measurements. For clarity, we list the time transfer parameter definitions and references. A TRIP timing exchange is shown in Figure 5.24. All parameters are to be determined as elapsed time measurements.

t'_A = Node A transmitted TRIP relative to Node A reference

t_B = Received Node B TRIP relative to Node A reference

t'_B = Node B transmitted TRIP relative to Node A reference

t_A = Received Node A TRIP relative to Node B reference



TRIP ARRIVAL TIME AT B (RELATIVE TO A) $= t'_A - t_A + \tau_{AB}$

TRIP ARRIVAL TIME AT A (RELATIVE TO B) $= t'_B - t_B + \tau_{BA}$

} SINGLE-ENDED COMPUTATION

CLOCK ERROR (EQUAL DELAYS) $u = \frac{1}{2}(t'_A - t_A - t'_B + t_B)$

$=$ CLOCK A - CLOCK B (START-TO-STOP TIME)

} DOUBLE-ENDED COMPUTATION

PATH DELAY $\tau_{AB} = \frac{1}{2}\left[(t_A + t_B) - (t'_A + t'_B)\right]$ ASSUMING $\tau_{AB} = \tau_{BA}$

Figure 5.24 Clock Error and Path Delay Calculations for Single- and Double-Ended TRIP Exchanges

Figure 5.24 depicts the relationships between the TRIP data packets and the actual elapsed time measurements above. Single-ended computation requires only a single TRIF transfer from the "master" (assume that the receiving node is performing clock error computation) to the "slave". For precise time (phase) alignment, we must include a delay compensation term which takes into account all equipment and path delay components. Otherwise, phase errors will be introduced which may accumulate throughout the network. The delay term is not required for frequency averaging techniques.

Double-ended computations require a two-way TRIP exchange. Assuming that propagation delay is the same in each direction, clock error computations effectively eliminate the equipment and path delay components. In fact, an alternate double-ended computation may yield path delay directly.

Time Reference Distribution involves an additional term in order to provide node-to-node phase coherence. This term is the error of the neighboring node (or nodes) from which the current error computation is based (at the local node). Phase reference combining allows precise time distribution throughout a network and ensures that phase errors do not harmfully propagate and/or lead to potential network instability. If the information over multiple paths (in a large highly-connected network) is optimally combined, it is possible to establish a greater timing accuracy at all nodes in the network. Improved Time Reference Distribution provides such a capability. See Section 5.2.4, Appendix A, [5.5], and [5.6].

Substantial effort went into the measurement of medium delay variability for TROPO and LOS links [5.2]. Although there were not too many surprises in the resulting data, it should be emphasized that many other important issues were examined and analyzed in the support of these experiments; the critical evaluation of equipment characteristics has brought forward some particularly valuable results, and, overall, the major role of the field program has been one of developing keenness of insight into time transfer problems. Presented in this document are the many facets of the time transfer and system integration tasks that would not have been uncovered without the stimulus of a field testing effort.

Addressing more directly now the results of the medium parameter tests are the following conclusions [5.2]:

- Path length variation for LOS links is relatively unimportant; according to a rather modest data set, it is limited to about $\pm 10^{-5}$ variation around the nominal path length. The principal effect is considered to be refractivity changes with corresponding variations in the speed of propagation. A single-ended time transfer system with a time constant of a few minutes would suffice. Data buffering requirements amount to less than 1 bit over normal length links.
- For TROPO links, there is considerable timing jitter in the recovered clock. This has an influence on acquisition performance. When the timing reference is averaged over periods of 10 minutes or more, the long-term path length variations are left. This latter category exhibits swings of ± 200 ns over periods of several hours.
- Reciprocity of the TROPO paths is not likely on an instantaneous basis. However, with the short-term fluctuations averaged out, forward and return links are expected to have the same delay down to the 20-ns level. This was confirmed by the results of TROPO path length measurements in a non-diversity configuration.
- Single-ended time transfer is not viable for TROPO links unless long-time constants are used (e.g., several days) and stable frequency standards are available at both ends of the link. With very long-time constants, the tracking loop transient behavior becomes more severe in terms of overshoots, particularly when two clocks offset in frequency are being synchronized.

Finally, some comments on the merits of different types of frequency standards and their performance when used with TROPO and LOS links. Although time constants of several hours or more are normally recommended for atomic standards, there appears to be no particular advantage to such long averaging times for LOS links. In fact, there appears to be no fundamental argument against the use of quartz standards on most, or all, of the LOS

links during normal operational periods. If node clocks must run in the independent clock mode, then the long-term stability does become important, but this appears to be the only real factor against quartz standards. For TROPO links, longer time constants are necessary to smooth out medium variability. A time constant of an hour or so is quite adequate for double-ended systems, and quartz clocks would be expected to function satisfactorily. However, for a single-ended TROPO path, a time constant of a day or two is necessary; this, in turn, necessitates the use of high-quality standards at the connected nodes.

REFERENCES

[5.1] Harris Corp., "Study of Alternative Techniques for Communication Network Timing/Synchronization," Final Report under Contract DCA100-76-R-0028, March 1977.

[5.2] CNR, Inc., "System Timing and Synchronization," Final Report under Contract F30602-76-C-0347 with RADC, May 1978.

[5.3] W. F. Hamilton, "Propagation Delay Calculation," NBS, Time and Frequency Measurement Seminar, NBS, Boulder, CO, 18 - 20 June 1974.

[5.4] CNR, Inc., "Timing Subsystem Development Computer Program Manual," Contract No. F30602-78-C-0287 with RADC, 1981.

[5.5] H. A. Stover, "Time Reference Concept for the Timing and Synchronization of the Digital DCS," DCASEF TC39-73, July 1973.

[5.6] H. A. Stover, "Improved Time Reference Distribution for a Synchronous Digital Communications Network," 8th Annual PTTI Conference Record, November 1976, pp. 147 - 166.

[5.7] R. G. DeWitt, "Network Synchronization Plan for the Western Union All-Digital Network," Telecommunications, Vol. 8, No. 7, July 1973, pp. 25 - 28.

[5.8] F. T. Chen, et al., "Timing Synchronization of the DATRAN Digital Data Network," National Telecommunications Conference Record, New Orleans, December 1975, pp. 15-12 - 15-16.

[5.9] H. A. Stover, "Communications Network Timing," DCEC Technical Report TR 43-75, September 1975.

[5.10] H. A. Stover, "Coordinated Universal Time (UTC) as a Timing Basis for Digital Communications Networks," paper presented at EASCON, 1974.

[5.11] Frequency Measurement Terminal Instruction Manual, U.S. Dept. of Commerce, National Bureau of Standards, Time and Frequency Division, Boulder, CO, 1977.

SECTION 6

RECOMMENDATIONS

This section contains comments and suggestions concerning the Timing Subsystem and related network synchronization topics. Included are discussions on possible TS improvements and more general future design considerations for an advanced development model. The topic of network security and fallback modes of operation are briefly reviewed. Following is a discussion of precise time distribution within a synchronous network. A brief evaluation of the candidate timing techniques is revealed along with implementation difficulties or other drawbacks encountered during the course of this program. Finally, topics for future work in network synchronization are presented including a summary of features considered desirable for a future Timing Subsystem.

6.1 Future Timing Subsystem Design Considerations

This section summarizes conclusions and recommendations for future development of the DCS Timing Subsystem based on the analysis and experimentation carried out in this program. Presented here are the general hardware design constraints dictated primarily by equipment interfacing issues. Included is a brief summary of the software design and recommendations for further development in that area. Also, discussions of processor type, data buffer design and placement, topics in error detection/correction, and choice of node frequency standards are presented.

After reading this section, it should be clear that the current Timing Subsystem design is capable of supporting a timing function over much larger networks than actually examined.

6.1.1 Advanced Development Model

Throughout this effort it has been emphasized that the CNR Timing Subsystem proved to be versatile, efficient, and flexible equipment easily configured and/or programmed to perform several timing functions. It is felt that future subsystems should continue to possess these qualities because of the relatively low cost of microprocessor-based hardware. In fact, it would make

sense not to sacrifice a proven, dependable equipment design solely for the purpose of streamlining packaging or minimizing IC count. Instead, a significant portion of future development effort should be aimed at software enhancement through an effective advanced software development scheme. It would seem feasible to provide additional capabilities in the measurement and large-scale network performance platforms, at minimum cost, while retaining hardware compatibility with present and future equipment for simplified field efforts.

Ideally, many of the important system-related decisions should be made by examining the behavior of a large-scale model of the network. For development purposes, a network with LOS and TROPO simulators may be configured at one location, but the size of such a network would be limited by equipment availability. However, it should be stated that more network-level testing would be required before any specific timing technique endorsement could be made (see Section 6.4).

In summary, an advanced development model should be enhanced over the existing Timing Subsystem primarily in the software end of the spectrum. Field efforts demonstrated that the subsystem hardware was capable of much more demanding applications than encountered during network tests. Thus, the current hardware design should prove to be more than adequate for future applications. Increased software capability could then be added at minimal cost while improving the user friendliness, monitorability, and performance assessment features of the system.

6.1.2 Processor Type

If one were to choose a single strength in the Timing Subsystem design, it would be the fact that the equipment was conceived around a general-purpose microcomputer capability; that is, the CPU section contains the elements essential to any small computer yet is ideally suited for the TS application. Moreover, flexibility is an integral part of the design; the Timing Subsystem is fully programmable in nature and many external events are serviced, monitored, or controlled by the microprocessor.

The choice of processor type, in general, is highly subjective in nature. This program has sufficiently demonstrated that a single 8-bit "no frills" microprocessor (M6800, see [6.1]) is capable of handling the software burden with adequate overhead. Additionally, future software enhancement would not be

limited by speed or computational constraints so the current CPU design would have no trouble handling some added tasks. Recall that the microprocessor routes arithmetic chores to an external arithmetic processor that provides fixed and floating-point operations. This is an essential part of the design considering PLL implementation, TRD, and other functions that require a high-speed, 32-bit floating-point capability [6.2].

The original choice of microprocessor type was strongly influenced by existing development capability at RADC as well as more general compatibility issues. Whichever microprocessor were to be used, only minor differences in CPU design and interrupt protocol, for example, would surface. Other differences would make themselves evident in software, but overall design and development costs for any of the more popular 8-bit micros would be comparable.

As an alternate view of the situation, one may argue that one of the newer, more powerful 16-bit microprocessor devices would be more suitable in the Timing Subsystem design. However, it is clear that the 8-bit microprocessor is not taxed beyond its capability; in fact, sufficient headroom exists to allow advanced development without the need for redesigning the computer section of the Timing Subsystem. Generally, 16-bit micros provides 10 - 25 times more throughput than most 8-bit devices, but it is certain that much of this speed and capability would go unused.

In summary, almost any popular 8-bit microprocessor would do the job satisfactorily - providing a complete family of I/O support devices were available. The current Timing Subsystem design and processing load is fully within the limitations of the Motorola 6800 device family with ample overhead, even in worst-case conditions. For a look at the typical processing times per one-second iteration, see Table 6-1. This table serves to illustrate and partition the execution times of various program sections encountered each second. Recall that Timing Subsystem operation is based on a once-per-second repetition rate and that several of the basic program modules are synchronous to that rate. Other asynchronous or conditional events are noted in the comments column and should be considered when computing the total-per-second execution time based on a particular preprogrammed TS configuration. Notice, however, that for a typical processing load encountered during a Master/Slave experiment terminating two links, the total execution time is approximately 36.45 ms occupied per second. The largest

TABLE 6-1

TYPICAL PER-SECOND EXECUTION TIMES FOR TIMING SUBSYSTEM MICROPROCESSOR*

Task	Execution Time	Comments
Interrupt Dispatcher Overhead and Interrupt Latency	180 μs	For a typical configuration
Once-per-second Service Performance Assessment Service Fault Check	12,500 μs	Checks for buffer ovf, unf, reference change, etc. Keeps running averages of clock error and error compared to 3 AUXTRP's Begins link 1 transmit sequence Updates clock correction
Transmit Bytes	40 μs/byte	2,680 μs for 67 bytes total per link 16,080 μs for 6 link max
Receive Bytes	50 μs/byte	3,350 μs for 67 bytes total per link 20,100 μs for 6 link max
Frame Processing	55 μs/link	Frame assembly overhead per link
Reference Selection PLL Loop Update	11,300 μs	Completes clock error for SE or DE transfers Determines operating mode Implements PLL algorithm Performs timing technique algorithm Assembles outgoing TRIP's
Misc. Bookkeeping	120 μs/link	Per operating link
Timing Algorithm (includes Error Computation) — IND CLK	20 μs	Overhead time only
Timing Algorithm (includes Error Computation) — M/S	60 μs	Mostly bookkeeping
Timing Algorithm (includes Error Computation) — MS	1,100 μs	Includes floating point
Timing Algorithm (includes Error Computation) — TRD	520 μs	Finds best path to master, determines hierarchy
Timing Algorithm (includes Error Computation) — Improved TRD	3,275 μs	Additional computation and bookkeeping overhead
Total (per second)	36,450 μs	For a typical 2-link configuration with M/S
	64,485 μs	Worst Case (6 links Improved TRD)

*Motorola M6800 with 1-MHz clock.

computational burden can be imposed by running Improved TRD while terminating six active links. The resulting execution time is approximately 64.49 ms per second. Field test configurations resulted in processing times similar to the former example. Execution times are determined by adding instruction execution times or, in some cases, by direct measurement.

6.1.3 Data Buffer Design and Placement

Now look at the buffering capability provided by the Timing Subsystem prototype. The buffers in question are used primarily for protection against timing transients which may occur in a system with coordinated clocks or, more likely, to take up the differences in data transmitted between nodes when independent clocks are set up in the network.

A few general comments will help to orient the reader before more specific recommendations are put forward [6.3]:

- Present technology allows buffers for level 2 (up to 13 Mb/s) to be built at only a marginally higher cost than buffers for level 1 or below. Above about 1K bits of storage there is virtually no cost differential and, more important, the incremental cost of adding storage beyond this value is quite small compared with the initial cost of control circuitry.
- When buffering is carried out at one of the lower levels, all upstream equipment must be clocked from the recovered modem clock which will exhibit jitter and other medium effects (e.g., frequency offset for satellites). To avoid the presence of this jitter in equipment, it must be placed on the downstream side of the buffer.
- At some stations, switching and combining of data streams from several remote sources must be achieved. This can only be done with synchronously clocked data, implying that the data must have already passed through a buffer by the time it is presented for combining. For example, if digroups (1.544 Mb/s) with different geographical origins are to be combined at a level-2 MUX, they must have been subjected to buffering either at level 2 or at level 1.

- At the output of the radio, data must be buffered in such a way that resets correspond to the deletion or insertion of an integer number of level-1 and level-2 frames. We dismiss the possibility of extending this concept to lower level submultiplexers because of the increased storage requirements. However, the possible avoidance of level-1/level-2 TDM resynchronization is in itself appealing enough, particularly when a major portion of the traffic is PCM voice. In terms of the effects on voice channels, it was our objective to reduce the resetting operation to the loss of, at most, two PCM samples for each voice channel passing through the buffer.
- To successfully employ such a strategy, it is necessary to know the TDM frame format, and to examine the consequences of implementing multiple frame resets with buffers at different levels, e.g., at level 2. A jump by a whole level-2 TDM frame may not throw that DEMUX out-of-sync, but still not safeguard the level-1 DEMUX's. Alternatively, if the buffers are at level-1, such resets do not affect the level-2 DEMUX's in any way.
- The level-2 TDM rate specifications allow for input port strapping (i.e., output ports at the DEMUX); hence, the buffer design must accommodate various rates if it is to be used at level 1. This is rather awkward when one considers that the total number of bits of storage required at a level-2 DEMUX output is invariant regardless of the division of the total MBS bit rate into various port rates, strapped or otherwise. Obviously, the designer is forced to develop an 8-port flexible buffer unit with programmable rate structure (and movable storage boundaries), or he must design for the worst-case rate (i.e., maximum) and develop other identical buffers to satisfy the worst-case number of ports. These design issues give added weight to the selection of a level-2 buffer design.
- Other considerations mainly involve cost and reliability of a few large fast buffers vs. a larger number of smaller slower buffers of comparable total capacity. A large buffer is probably cheaper than a number of smaller ones of similar total capacity, unless reliability requirements (MTBF is probably a

function of size) or the high data rate required dictate a more expensive approach (either a different technology or more expensive components). The consequences of a failure of a larger buffer are more serious than those of a failure in one of a number of smaller buffers which might be used instead.

There exist six elastic stores in each Timing Subsystem corresponding to one for each of the terminated links at a node. These buffers are placed at the output of the digital radio demultiplexer and, therefore, must operate at speeds up to 13 Mb/s. Strictly speaking, the DCS specifications implicitly require two such buffers at each link termination, since the DCS radios are designed to accept two separate MBS data lines. However, only single line terminations were implemented at the RADC Test Bed and, as an experimental model, the total subsystem buffer capacity was more useful when structured as 6 double-length buffers rather than 12 single-length buffers.

The buffer size (2K bits) was determined on the basis of a minimum size requirement for independent clock operation. Starting half full, with two parts in 10^{11} difference in input and output clock frequencies, it will overflow or underflow in 1100 hours (about 46 days); with one part in 10^{8} relative clock frequency, the time is 2.2 hours.

An attractive possible application for relatively large buffers is the preservation of multiplexer synchronization during buffer reset. If buffer capacity exceeds the length of the framing pattern (e.g., superframe or super-superframe), when it gets nearly full, its fullness can be decreased in one jump by a number of bits equal to the framing pattern length. CNR has examined a buffer design to include this feature. If the TDM 1193 superframe needs to be preserved, the total buffer size must be in excess of 25K bits and the step resets must be of a corresponding magnitude. It would appear, however, that the 1193 superframe carries only pulse stuffing information, which will not be relevant in a synchronous network. Obviously, it is necessary to have additional information concerning the 1193 frame format to pursue the design further [6.5].

A buffer design (Figure 6.1), using cascaded 64 x 4 FIFO modules, is used. Using FIFO's rated to operate at data rates up to 10^{7} words per second, or 40 Mb/s, this buffer can easily

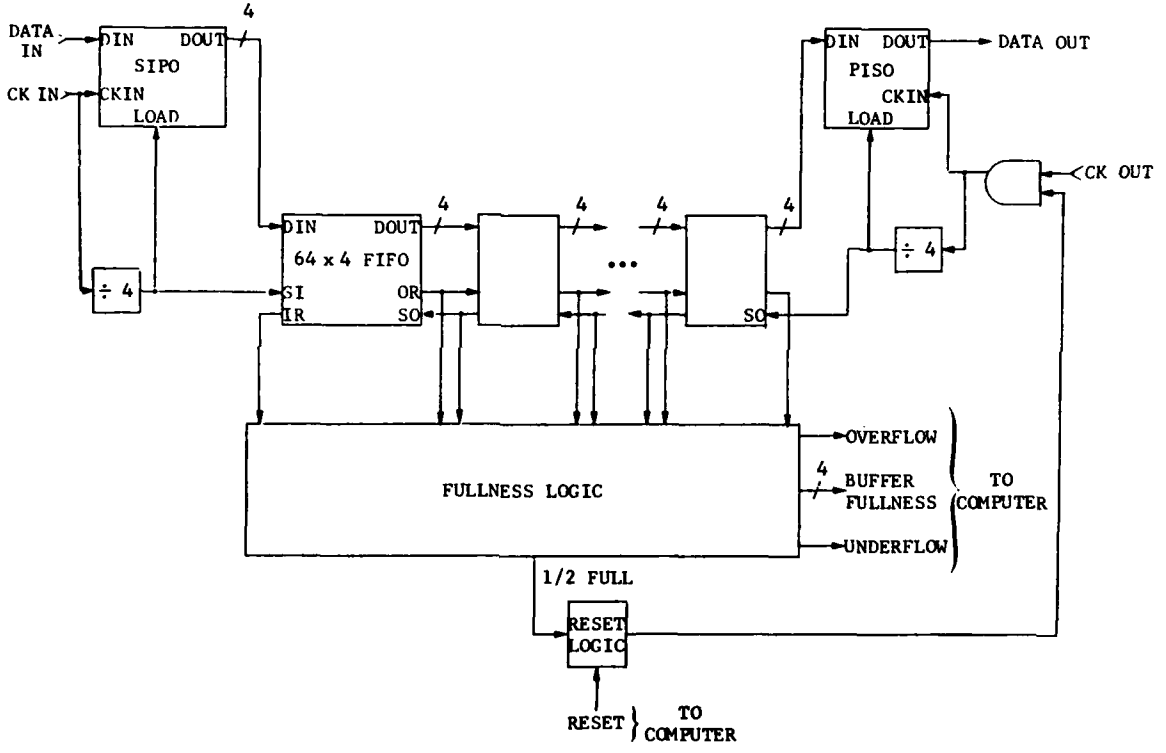


Figure 6.1 2048-Bit Elastic Buffer

handle the 12.928-Mb/s data rate of the level-2 multiplexer MBS. Four-bit serial-to-parallel and parallel-to-serial registers interface the input and output bit streams with the 4-bit wide FIFO, which have TTL-compatible inputs and outputs. A numeric display indicates buffer fullness in eighths of full capacity: 1 = less than 1/8 full; 2 = 1/8 to 1/4, etc.; 8 = more than 7/8 full. A reset circuit which initially loads the FIFO half-full is included; the output clock is gated off and the FIFO cleared; when the FIFO is half-full, the output clock is allowed to start [6.4].

This design proved to be quite reliable in the field. Buffer fullness status was available to the computer and, subsequently, to the front display panel and the operator.

Continued use of this design is recommended.

6.1.4 Error Detection/Correction

The transfer of clock data throughout the network requires some thought, particularly with regard to error control and centralized network control.

Reliability for the clock control data link is paramount. It is quite obvious that the data being transferred between nodes is highly intolerant of errors; the adaptive reorganization merit and ranking parameters, for example, must be carefully protected to eliminate the possibility of inadvertent network timing errors or reconfiguration.

The task of designing the data link is complicated even further by the following considerations:

- Error patterns observed on the links will tend to be burst-like as a result of channel fading, particularly for TROPO and LOS systems.
- Although the DCS specifications call for quite low error rates (e.g., 5×10^{-9} for LOS, 5×10^{-5} for TROPO, 99.99% of the time) [6.5], data link integrity is even more important during periods of jamming when the error rates will be much higher. Therefore, a high tolerance to errors is necessary.

From these statements one can formulate some important guidelines which apply to our data link design. Briefly, there are certain data items that must be delivered with virtually zero error probability or, as an alternative, not at all; i.e., gaps in the clock updating procedure are preferable to the use of invalid data. Then it must be accepted that, during times of stress, the raw bit error rate may be quite high (e.g., approaching 0.5). These two facets of the data communications design task are rather ominous considering the narrow range of options they leave open.

The necessity of achieving close to zero error probability strongly suggests that a dependable error detection scheme is mandatory; error correction is of value since it may be useful in bolstering the effective data transfer rate. The use of several data modes is also advocated. One can exploit the fact that, in a heavy jamming situation, only the more essential data need be conveyed between nodes. Thus, one should contemplate a backup low data rate mode of operation. The unused capacity would then serve to enhance the reliability of the remaining data bits by allowing additional redundancy.

Error will occur in the transmission of data from one point to another and, if the information content is highly critical as it is in the case of clock control, plans must be made for dealing with the errors. There are two fundamental categories for improving the reliability of a data link. The first, commonly called ARQ (Automatic Repeat Request), involves transmission by blocks. Each block has a number of parity bits appended. At the receiving end, the parity bits are recomputed from the data and compared with the received parity bits. If there are no discrepancies, the block is accepted; otherwise, the sending station is notified and the complete block must be transmitted. This is referred to as an error detection scheme. It is the job of the decoder to detect the presence of most errors, while correction may be carried out by retransmission.

Forward Error Control (FEC), on the other hand, is more complicated and involves attempts by the decoder to determine the location of the errors from the pattern of discrepancies between received and recalculated parity bits. With FEC there is an error correction mechanism. Depending on the nature of the error patterns, FEC systems may be able to correct a maximum number (say, t) random errors or, alternatively, a burst of errors having a span of B bits. Composite error detection/error correction schemes using both ARQ and FEC can also be devised.

In most situations, particularly TROPO, the errors will not be independent random events, primarily because of channel fades and we must evaluate and compare the performance of ARQ and FEC techniques carefully to see how they perform in a burst error environment.

While ARQ errors may be corrected by retransmission of a block, the FEC must attempt correction on the fly. Thus we see that, although FEC may not be able to achieve such low overall error rates as ARQ, the latter has a variable and possibly low transmission efficiency. There is no doubt that a combination of both has merit [6.6],[6.7].

There are several ARQ variants. By far, the most common is the stop and wait system, whereby the transmitter waits after each block for a positive acknowledgement before sending the next block. Then there are two versions of the so-called continuous ARQ approach. With sequential numbering of the outgoing blocks, the receiver is able to request retransmission of a particular block. This can be done in a pull-back manner; the transmitter discounts any higher numbered blocks it may have sent in the interim, and retransmits a complete sequence of blocks, starting at the block found to be in error. This keeps the blocks in sequence. Alternatively, the transmitter can retransmit only the block found to be in error, in which case the blocks would be received out of order.

FEC performance is more sensitive to the distributional nature of the errors, e.g., burst or random. The easiest way of achieving protection against both kinds is to use interleaved codes; with a relatively low cost approach, modest improvements can be achieved with this method. The FEC schemes available are successful to one degree or another in reducing the bit error rate. But the fact remains that errors must be virtually eliminated for some of the more sensitive clock data. Consequently, a high level of error detection performance is still required.

The preceding paragraph suggests that the principle of operation for the data link should be based on ARQ with a very low residual undetected error rate by judicious choice of parity check code. However, it is apparent that additional FEC capabilities will be required between the SDLC line controller and the service channel multiplexer to maintain good performance during periods of jamming when the error rate will be quite high.

A full investigation of the requirements for such an FEC unit appears necessary. However, three key topics can be itemized at this point:

- Delay through the FEC must be carefully controlled if the clock data channel is being used to convey node time, as in option B described in [6.5].
- With the channel data rate selected as 4 kb/s, and an information rate that is on the order of 500 b/s, there is significant redundant channel capacity available for use by the coding scheme.
- Contingency plans can be formulated for minimizing the data transfer requirements during jamming situations. Such a reduction will allow the use of even lower rate codes in the FEC application.

Finally, note that the burst nature of the error distributions existing on TROPO links creates additional difficulties which can only be solved with specialized coding and decoding equipment.

6.1.5 Node Frequency Standards

This section is intended to clarify the difference between a disciplined oscillator used in a network timing experiment and a frequency standard, including when each should be used.

A frequency source option was used on one of the Timing Subsystems. It consisted of a Voltage-Controlled Crystal Oscillator (VCO) with a D/A interface to provide computer control of this device. The reason for this option was twofold. First, it was to be determined by experimentation if a disciplined quartz oscillator could perform well when slaved to a more elaborate frequency standard. Second, if such a frequency source was cost-effective in a large network, would it be feasible to incorporate VCO's at many less critical nodes; that is, nodes that are not directly contributing to the timing function, without seriously compromising the synchronization performance of the network?

Although each test site had on-hand a rubidium frequency standard at the minimum, for the VCO performance test, the frequency standards served only as a reference for clock comparison; i.e., the Timing Subsystem that had its own internal oscillator

did not need an external frequency source applied for the clock adjustment mechanism. Instead, this VCO operated at the same center frequency (5 MHz) and had an adjustment range of 1.6 parts x 10^7 (similar to that of the phase microstepper). A small penalty in software overhead to develop a driver was encountered over that for the phase microstepper.

Summarizing the findings, it was noticed that the VCO, when operated as a slave (i.e., disciplined mode), performed well and certainly within the limits for overall network accuracy as specified for the DCS. Also, considering the cost to install rubidium frequency standards (about five times higher than a VCO) and phase microsteppers at each node, it would be good practice to consider the use of quartz VCO's at many of the less important nodes. However, it is strongly recommended that the higher quality frequency sources be distributed in some logical fashion.

6.1.6 Software Design

Timing Subsystem software is highly modular in design due largely to the asynchronism of events external to the processor. Timing is based on a once-per-second update rate provided by dividing down the adjusted 5-MHz node frequency source. Incoming and outgoing TRIP's interrupt the processor for service when two bytes are buffered and ready to be transferred. Prioritized events are handled by an Interrupt Dispatcher which is in charge of determining the sequence of module execution according to a set of predetermined priorities. A small system monitor, embedded in the software, provides basic interrogation and debugging capabilities as well as being the interface between the operator and the Timing Subsystem [6.8].

The success of the software effort is due largely to the modularity of the package. Routines are divided along functionality lines, which simplified software planning and development. All code is reentrant.

It is strongly recommended that future work allow the enhancement of existing programs to avoid a completely new hardware and software design. For example, an advanced development model may include the following salient features:

- An enhanced operating system to increase user friendliness and provide English-like commands and more natural dialog.
- Increased tolerance to perturbed incoming data streams. (This implies error correction facilities.)
- More complete performance assessment capabilities. Since this is the only means by which long-term performance is verified, it makes sense to provide a comprehensive evaluation of nodal clock behavior for a given length of time. External clock comparisons should also be maintained in this fashion.
- A simple efficient network management scheme would be most valuable in larger networks. For this program, node management was carried out on a node-by-node basis by telephone connection through the Frequency Measurement Terminals located at each site. However, a management protocol could be devised to set parameters remotely via bit patterns contained in unused portions of the TRIP format or by extending the TRIP itself. (There exists sufficient overhead for up to a tenfold increase in TRIP length.)

These improvements could be built around the already solid and field-proven processing base. Interrupt-driven routines are scheduled by a software Interrupt Dispatcher, and the system monitor responds to the operator when scheduled processes have completed. (See Section 2.2 of this report and Section 3 of [6.8] for a more complete analysis of the current software design.) Some of the more fundamental routines which are currently employed and would remain as the foundation of an advanced model are:

- Link I/O byte-oriented operations. These are interrupt-driven routines for both transmit and receive sequences. Programs are based on a single chip implementation of the SDLC protocol (including 16-bit CRC check for error detection).
- Clock error computation based on single-ended or double-ended transfers. Additional computation (double-ended) produces path delay or TRD error information.

- Normalization for computed clock errors.
- Software delay routine. This calibrated multi-stage loop coarse adjusts the node clock with an accuracy of $\pm 4\,\mu s$ over a one-second range.
- PLL algorithm. Includes PLL state equations and programmable time and gain constants.
- Interrupt Dispatcher. Schedules routine execution based on a predetermined priority scheme. Relays control to the operating system when CPU is idle. (See Section 3.2.1 of [6.8].)

Summarizing, it is encouraged that an advanced development model incorporate several modifications to the original software design. These changes would not affect the underlying processing routines but serve to enhance an already efficient and reliable software package.

6.2 Network Survivability

The DCS network must be designed for satisfactory operation under conditions of hostility. There is an underlying premise, therefore, that no single node should be critical to the functioning of the remainder of the network. When one or more nodes are eliminated, the surviving nodes should be capable of continued operation.

In Section 6.2.1 we examine the issues of survivability and security by comparing the different clock control techniques in stress situations requiring reorganization of the timing distribution scheme. In Section 6.2.2 we cover the subject of backup modes, where it is envisioned that normal operation with, say, Master/Slave, Mutual Sync, or TRD, is ruled out for the complete network, or at least for large portions of it.

6.2.1 Self-Organizing Features

When segments of the network are in a condition of stress, it is likely that the timing distribution tree for the remainder of the network will have to be reorganized. This is the essence of survivability, and its importance for a military network is patently clear. Of course, there are more mundane reasons for implementing automatic time distribution recovery; clock and transmission equipment failures in the network are inevitable and contingency plans must be formulated to cover these events.

The purpose of this section is to assess the relative degree to which the synchronization technique provides a survivable network. Comparison of directed and mutual control can be made in cases where references are not available. For the references which are available, mutual and directed control techniques differ considerably because each node in the mutual system is always using all of its incoming link data, whereas a node in the directed control system derives timing from only one of the connected links. Transients can occur in the mutual system, but the directed control system is affected only if the reference on the chosen timing link is removed. With either technique, those features which tend to minimize instantaneous frequency and phase errors will tend to improve network survivability [6.9],[6.10]. With directed control, the sooner a node can find a new reference once an old one has been removed, the better from a survivability standpoint. Thus, self-organization is quite important to the survivability of a direct control network.

Both mutual and directed control systems have similar problems when no references are available. Both must rely on previous clock correction history in order to maintain synchronism. Accordingly, the stability of the local clocks is of critical importance. However, performance with no references available is based on the history of external stress events and individual clock behavior. Therefore, those features which reduce the complexity of this error history during normal operation will increase the potential for survivability during periods when references are not available [6.9].

Of the synchronization techniques considered, the TRD approach is unique in the survivability features it offers. It is sufficient to say here that the capacity to automatically reorganize is the feature of TRD that sets it apart from the others; namely, Master/Slave, Mutual Sync, and Independent Clocks. This self-organizing capability should be recognized as a characteristic that does not necessarily have to be associated with TRD; that is, the time distribution functions and the reorganization functions are essentially separate. We can contemplate the development of a relative time synchronization scheme which has these self-structuring features; it would be equivalent then to a Master/Slave scheme with an adaptively reorganized distribution tree.

It can be safely concluded that the self-organizing aspects of the currently formulated TRD technique are of great benefit, and bring to the overall network a level of resilience that cannot be matched by other approaches. Of the remaining choices, the Independent Clock method is in a class of its own and need not be discussed. Then, the Mutual Synchronization technique should be considered as having reasonable survivability characteristics. Despite the potential for operation without the need for a clock control data link, there are questions of stability which arise when the structure of the network is undergoing change. These issues are best addressed with large-scale network simulation tools; it is not likely that the small network, set up as part of this contract, will offer insight to behavior for network problems such as these. Finally, it is recognized that the Master/Slave technique, at least in its classical form, is not well-suited to coping with network stress.

There is a temptation to treat these candidate techniques in isolation, as separate and unalterable methodologies. But, as pointed out above, certain features of one may be applicable to others. The self-organizing features of TRD should not be associated with TRD exclusively, for example. Another important point is that reorganization without control data linking is a very desirable goal; that is, it may be feasible to formulate reference selection rules on the basis of the received TRP signals alone. Clearly, there will be a sacrifice in terms of selection optimality. On the other hand, the physical structure of the DCS network is likely to remain relatively invariant, and preplanned timing recovery strategies, including reference selection, should be easy to test by means of simulation. Furthermore, with a reliable enough backup mode of operation, the reference selection process could be undertaken at a fairly leisurely pace to minimize the possibility of network instability.

6.2.2 Backup Modes of Operation

When one considers the topic of survivability, the idea of a backup mode is immediately brought to mind. Here we will be concentrating on two particular backup configurations. It should not be concluded that these are the only two, but they are generally considered as likely candidates. These backup concepts involve:

- Use of AN/GSQ-183 timing terminal; i.e., a LORAN-C based external frequency source

- Network operation with highly stable independent standards

Both modes will be considered subsequently.

First is an outline of the functional properties of the AN/GSQ-183 Frequency Control Set, which is intended for use as an interim timing subsystem in DCS.

6.2.2.1 AN/GSQ-183 Frequency Control Set

The AN/GSQ-183 Frequency Control Set uses the worldwide LORAN-C transmissions to obtain high resolution frequency references and a calibration at a network node. The system generates a 1-MHz output signal with variability of a microsecond or better. It may be phase-locked to either a 1-MHz local reference or to the incoming LORAN-C signal.

The principal components are shown in Figure 6.2. The CV-3094 frequency multiplier consists of a combiner to supply a 1-MHz reference to the LORAN receiver. This signal is derived from either the primary or secondary RF oscillators (0 - 1632) using an automatic selection procedure in the event of oscillator failure. The CV-3094 also ensures that the system output (1 MHz) is slaved to the best reference choice, i.e., either the LORAN-C groundwave or the alternate local reference. When neither of these signals is available, each RF oscillator is put into a coast mode using digital control signals, as shown. This unit and the oscillators can function independently of the LORAN receiver using alternative 1-MHz frequency sources (sine or square wave).

The R-1776 receiver is a solid-state unit designed to track the LORAN-C signals. It features an all-electronic phase-tracking servo system, with 20-ns resolution.

The 0 - 1632 oscillators consist of a voltage-controlled crystal oscillator with digital control signals and provision for manual slewing of frequency to assist in acquisition. The digital servo memory retains the crystal aging rate when the loop is opened. Finally, the CV-3093 frequency multiplier consists of three identical modules, each of which synthesizes 96 kHz and 1.2288 MHz from a 1-MHz input signal.

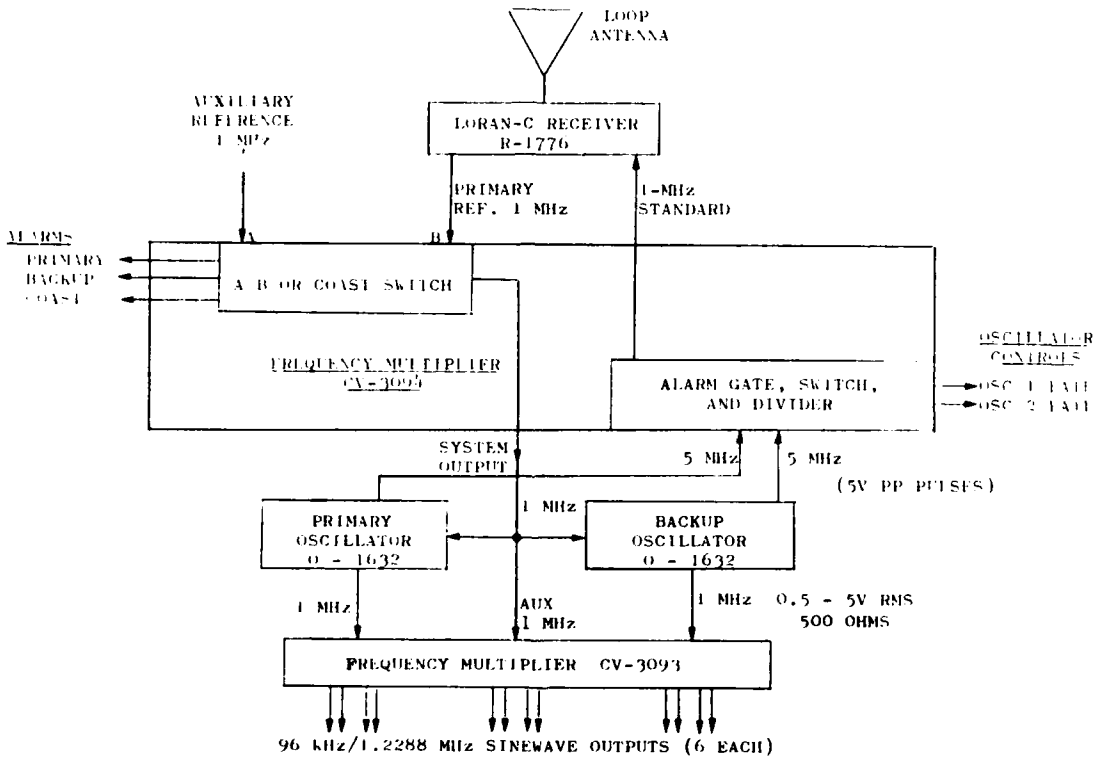


Figure 6.2 AN/GSQ-183 Frequency Control Set

6.2.2.2 AN/GSQ-183 as a Backup Frequency Source

The AN/GSQ-183 output may be visualized as a frequency reference with excellent long-term stability traceable back to an atomic standard via the LORAN-C path. However, quite severe path length variations are evidenced, and this is equated with unwanted phase and frequency jitter on the output signal.

There are at least two ways of integrating the AN/GSQ-183 signals into the Timing Subsystem. In discussing two obvious possibilities, we shall also touch on the subject of Independent Clock operation as a backup mode.

The two figures which follow, Figures 6.3 and 6.4, provide a pictorial statement of the two integration choices alluded to above. Some explanation of the symbols and notation shown is required first. Without getting into the subtleties of the complete loop design, it can be said that one or more arrival time measurements from terminated links will be processed and combined to produce a clock correction signal. In its simplest form, this is a clock phase error. Figure 6.3(a), for example, has three terminated links, and for each a time of arrival or phase measurement is made relative to the local node clock. Figure 6.3(b) is the transfer function block diagram equivalent of (a). The inputs are represented as phase variables θ_1, θ_2, θ_3, and, after being compared with the node clock phase θ_0, the differences are passed to the control loop filter.

The LORAN-C external reference is represented in terms of the phase of the originating standard θ_*, and a propagation-induced phase perturbation (i.e., noise) θ_n. The total is designated θ_L. The method suggested in Figure 6.3 is to simply treat the external LORAN signal as another equivalent reference. This is implemented by generating a standard TRP with repetition rate of one per second. This derived timing event is compared with the local TRP, and the resulting time interval measurement is used in the clock updating. For Time Reference Distribution, the LORAN TRP would not be used explicitly since it is incapable of providing precise time data; its role is limited to stable relative time transfer. Consider, then, the situation where none of the links can provide a reliable time transfer path. Then, backup operation would consist of maintenance of the node clock phase so that the relative time between the local TRP and the LORAN TRP was preserved. The loop would serve to lowpass filter the LORAN time variation; thus, the loop time constants would be chosen to smooth out θ_n in Figure 6.3 and hold the node

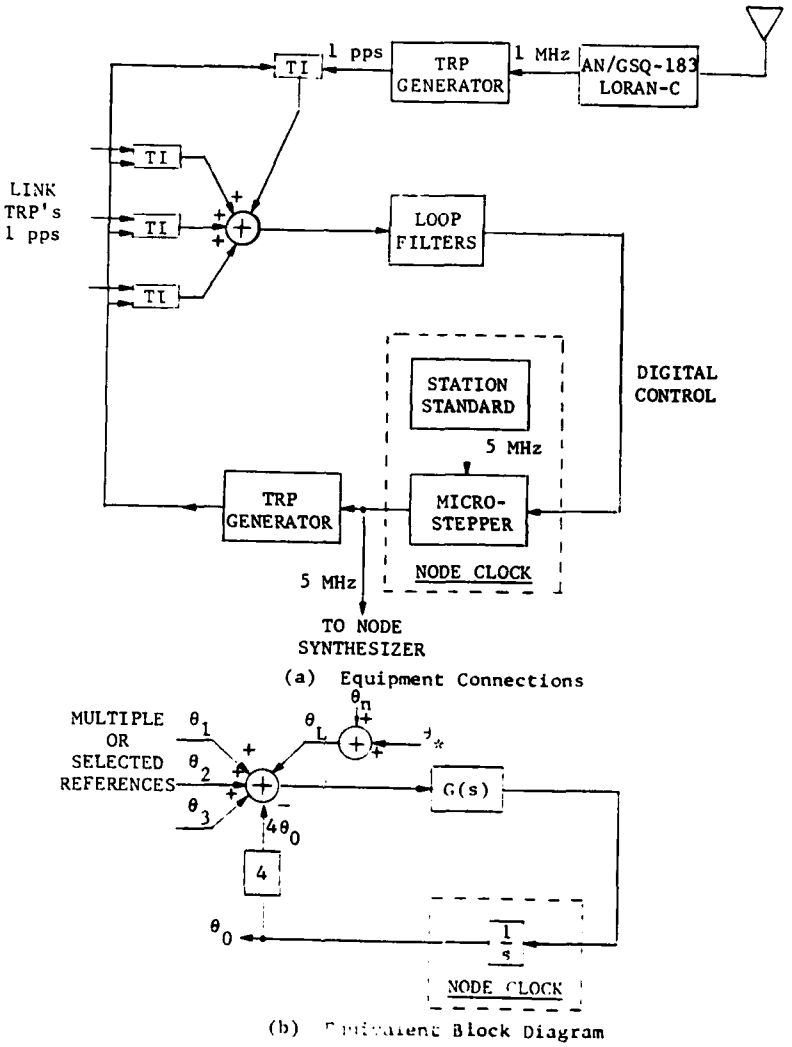
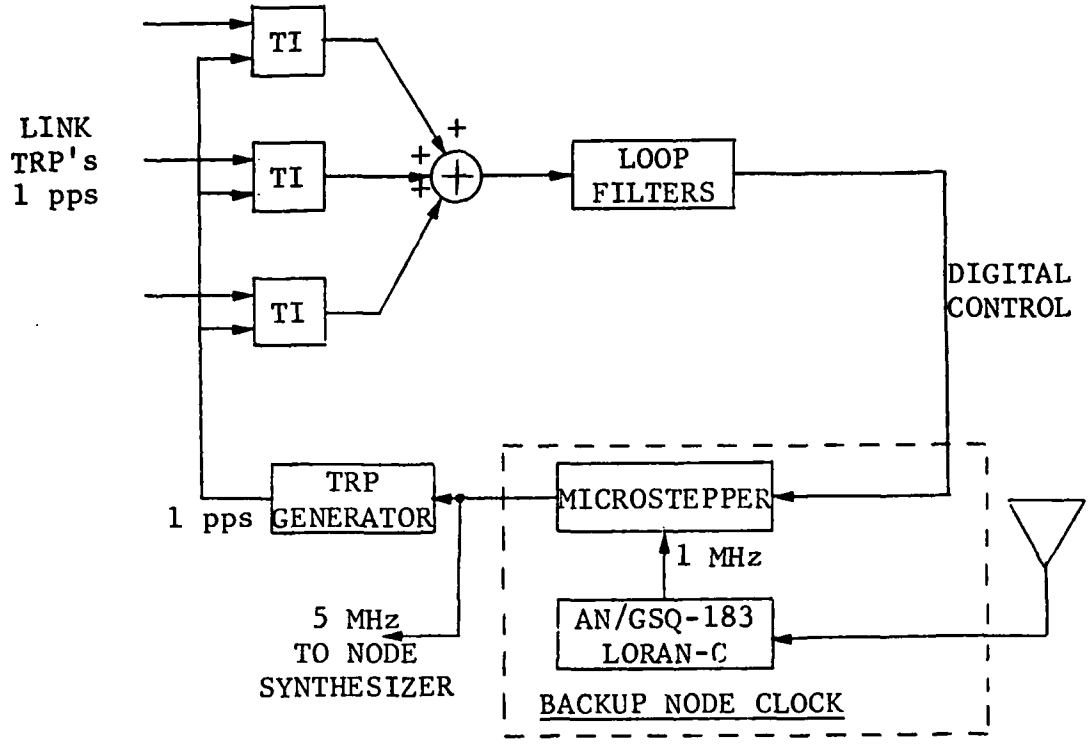
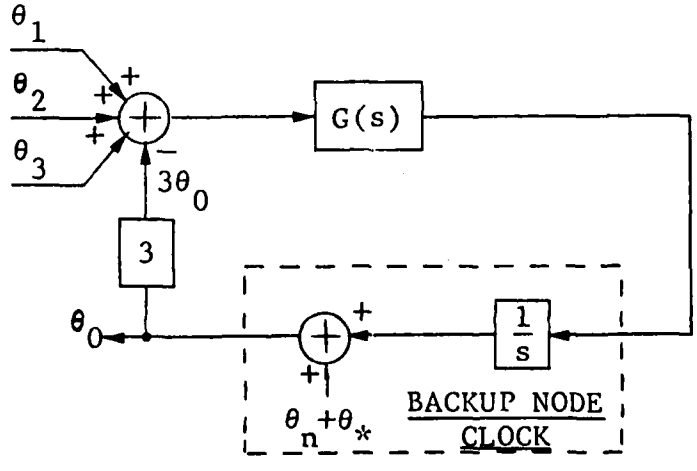


Figure 6.3 Integration of the Interim Subsystem as an Alternative Reference



(a) Equipment Connections



(b) Equivalent Block Diagram

Figure 6.4 Integration of the Interim Subsystem as a Backup Node Clock

clock output to a constant relative time with respect to the LORAN standard. With this form of backup, there is no stringent stability requirement for the local standard since it is effectively locked to the LORAN atomic standard.

The important aspect of this mode is that the LORAN-C TRP signal can be subjected to a set of standard consistency and rejection rules in the same way that link termination TRP's are. Hence, loss of the LORAN reference because of transmission or medium disruptions should be detectable. Then, the local station standard resorts to stand-alone operation as an independent clock. This safety mechanism represents a second level of backup for the node.

The other approach, depicted in Figure 6.4, is more straightforward, and perhaps more representative of circumstances where the station standard had failed. As shown, the LORAN 1 MHz is used as a direct substitute for the station standard. While link references remain valid and reliable, the servo loop can operate with them as shown. The output signal phase, marked by the symbol θ_0, is not the same as the direct LORAN phase. The loop provides highpass filtering of the LORAN phase. This means that any low-frequency fluctuations in θ_L cause the loop to produce a counteracting phase stepper control voltage; therefore, as far as θ_0 is concerned, there is no effect. The node, therefore, depends on the long-term stability of the incoming link references rather than on the LORAN-C signal.

When the node must operate completely without the link references, it would make sense to open the loop to obtain the LORAN-C long-term stability at the node. This is done quite simply by clamping the phase stepper control voltage at zero. Then the microstepper output is used directly by the node synthesizer. If we compare this open loop operation of the configuration in Figure 6.4 with that shown in Figure 6.3, it is seen that while they are basically both locked to the LORAN signal, the latter lowpass filters the incoming LORAN signal and, in addition, allows the node to revert to independent clock operation without reconfiguration.

The recommendation for backup node operation would, therefore, be to use the "pseudo link" configuration of Figure 6.3 except when the station standard has failed completely, in which case the configuration in Figure 6.4 must be utilized, either open loop or closed loop.

In concluding this section, it should be remarked that, apart from sheer physical destruction of network transmission equipment, the main stress-inducing element will probably be in the nature of electronic jamming. While the jamming may be effective enough to disable the normal time transfer capabilities, it should be realized that other more rugged communications options, such as spread-spectrum transmissions, will often be available. With the maintenance of precise time at both ends of a link, even in periods of disruption, some modest level of communication will be feasible. This points out the importance of establishing backup clock synchronization strategies to support such emergency communications systems if they exist on a line.

6.3 Network Timing Accuracy

The advantages of referencing precise time are numerous. Although the stated accuracy goal for DCS is 2 μs between any two nodes in the network [6.11], apparent accuracy can be enhanced by referencing precise time at one or more nodes in the network. This section is concerned with the availability of precise time and the methods by which to use it. Finally, a brief review of Federal Standard 1002 reveals that TS compatability currently exists and compliance is already "built in" to the TS prototypes.

Some of the potential benefits of having precise time traceable to the United States Naval Observatory (USNO) or National Bureau of Standards (NBS) are directly related to the fact that an increased distribution of universal time would result. This distribution aids in the general availability of precise time to users who may otherwise have difficulty obtaining it. Networks which disseminate precise time traceable to USNO or NBS have more potential to interoperate with the DCS, resulting in increased survivability. Also, monitorability is enhanced by allowing comparison of precise time at any point in the network with the external source.

In summary, the benefits of precise time at major nodes in a network are listed below:

- Aids monitorability and self-reorganization
- Reduces phase disturbances and improves frequency accuracy
- Improves bit synchronization and signal-to-noise performance

- Improves free-running accuracy following failure
- Further distributes precise time to potential users
- Precise time is useful in assisting synchronization of spread-spectrum equipment and in providing synchronization for TDMA networks [6.10]
- Navigation systems could use the DCS timing to increase their reliability and capability [6.10]

In comparing the different techniques, the major question to be raised is the size of the frequency step between primary and backup timing sources. The bigger the frequency step, the faster the buffers will fill or empty and the greater the probability of bit slip. As is mentioned in several places in this report, it appears likely that a Time Reference Distribution approach would be ultimately referenced to a world-wide time standard such as UTC. Similarly, potential backup timing sources, such as LORAN-C, are also referenced to UTC. Thus, it can be anticipated that a switch to a backup timing source in a network based on TRD will result in a smaller frequency step than any of the other techniques since both primary and backup systems could be referenced to the same ultimate source [6.10].

6.3.1 Precise Time Availability

This section refers to universal broadcasts of time or frequency signals derived from a precise standard. Included in this category are, for example, the NBS WWV broadcasts, LORAN-C and Omega navigation systems, TV transmissions, and satellite broadcasts [6.12].

The utility of a time/frequency broadcast in network synchronization should be clear. Each control node in the network listens in on the timing signal and synchronizes its own clock accordingly. There are three issues of importance in considering the various possible signals:

(1) Potential timing accuracy
(2) Geographical coverage
(3) Propagation disturbances

The WWV broadcasts originate from a cesium beam standard maintained by NBS, but generally speaking the accuracy of synchronization that can be obtained is typically 1 ms [6.13], which would not be adequate for application to network synchronization.

Some of the navigation systems offer better prospects. LORAN-C, which is a pulsed 100-kHz carrier, gives accuracies of 1 - 2 μs when the groundwave components can be received directly. Skywave reception, a necessity for intercontinental coverage, results in accuracies of 50 μs, which is not really satisfactory either. Similarly, the Omega VLF signals, being lower in frequency, usually provide accuracies that are even worse, typically tens of μs. Difficulties arise with Omega at locations near the transmitter where groundwave-skywave interference degrades the signal quality.

The most appealing method of disseminating time or frequency for most purposes is by the use of satellite broadcasts. With satellites, one obtains the combination of high visibility and high bandwidth transmissions, which are not usually available with a ground-based approach. Two distinct strategies can be adopted in satellite broadcast systems, i.e., one-way and two-way broadcasts. In a one-way broadcast, the user receives the transmitted signal either directly from an on-board satellite clock or from a ground-based master clock via the satellite acting as a time transponder. The user is normally provided with orbital or path length and rate parameters as part of the transmission. He is then able to make frequency and/or time corrections to the incoming signal.

The other alternative is the two-way system, which requires no transfer or orbital parameters. Instead, the method requires an exchange of timing error signals between the master and slave stations. The two-way timing system allows each slaved node clock to compute the total master/slave path delay and, by suitable processing of error signals, synchronizes itself exactly with the originating node. With a satellite broadcast, the two-way system is quite attractive because it does not require knowledge of the satellite position although, clearly, more transmitting and receiving equipment is necessary.

Examples of satellite timing systems, operating in a one-way node, include TRANSIT [6.14] and TIMATION [6.15]. Accuracies are limited to a few microseconds. One-way experiments, using satellites simply as transponders, have been carried out with ATS-1 and ATS-3 [6.16], LES-6, and TACSAT [6.17],[6.18]. In these particular experiments, accuracies as high as 10 μs were obtained. More recently [6.19], one-way transponding experiments were carried out using WWV as a standard, and the ATS-3 satellite as a transponder. The resulting accuracy was better than 25 μs.

Although the emphasis in this section is seen to be predominantly on time dissemination rather than frequency dissemination, it should be pointed out that the slave nodes do not require exact time synchronization to function correctly in a digital communications network. For example, the incoming clock can differ from the node clock by a fixed phase (and, hence, path delay) without any adverse consequences. Clearly, it is the magnitude of dynamic phase excursions which affect buffer overflow/underflow statistics, and these phase variations are derived from an integral of the instantaneous frequency difference. Two-way clock error exchanges, therefore, seem of less value than a knowledge of the rate of change in satellite position, i.e., the Doppler shift perceived at the receiver. If, for example, the path delay via a satellite was changing slowly with time (e.g., at a constant rate), the two-way clock correction scheme would maintain precise synchronization between the master and slave clocks regardless of the path delay. However, the incoming data rate would then be slightly higher than the transmitted rate, reflecting, of course, the steady depletion of bits stored in the transmission "buffer", and the slave node buffer would fill at a corresponding rate. In effect, the total number of bits stored in the medium plus node buffer remains invariant with perfectly synchronized clocks.

Precise time may be made available to DCS equipment without penalizing development or implementation costs. Survivability, however, becomes a factor with ground-based systems, such as LORAN-C, where global time signals are provided by relatively few stations. Also, the sheer physical size of the transmitting antenna structure makes it an easy target for enemy fire. Overall, the benefits of precise time cannot be denied, and its use is recommended. In this light, the use of satellites becomes even more desirable since satellite transferred timing is also derived from ground-based sources.

6.3.2 Dissemination of Precise Time

Precise time can be distributed by any system that is double-ended and has directed control. Some of the Improved TRD features are actually designed to further enhance this idea, but the aforementioned two requirements are the basic ones needed. For example, phase reference combining, as described in [6.9] and [6.10], further improves the accuracy of precise time dissemination.

It has been demonstrated in [6.9] that the inclusion of precise time does not degrade the performance of the system. In fact, the only drawbacks are slightly increased channel overhead and processor computational burdens, but these may be deemed insignificant.

In [6.9], a double-ended system with node B slaved to node A is assumed. Without precise time, the system Phase-Locked Loop (PLL) deriving the nodal frequency at node B would be driven by the estimated phase error similar to that used in a precise time system such as TRD [6.20]. The measured phase error has an ambiguity of some arbitrary number of cycles. However, once the phase error difference between the nodes and its relationship to the times of the clocks are defined, then the measured phase error is a constant, and any changes in clock times cause corresponding changes in measured phase error. Assuming equal path delay in both directions, the correction term (consisting of clock time differences) is equal to the actual timing error. To convert a normal double-ended system into a precise time system, we must include an additional term comprised of the phase difference correction term as does Improved TRD [6.20]. This correction term is a constant and can be estimated through infrequent transmissions of a time-of-day mark. Thus, there is no performance penalty associated with the inclusion of precise time since the nodal frequencies are determined only as they would be in a system without precise time. Phase and frequency accuracy are the same. The dissemination of precise time results in improved monitorability. When reorganization is used, the improved monitorability will result in faster response time for reorganization which, in turn, improves survivability. In addition, future users will have an alternate source of precise time readily available.

6.3.3 Compliance with Federal Standard 1002

The DCS timing subsystem must comply with Federal Standard 1002 to facilitate interoperability between telecommunications facilities and systems of the Federal Government without measurably reducing the survivability or flexibility, or increasing equipment or system complexity or cost.

Federal Standard 1002 states that "the time and frequency reference information utilized in applicable Federal Government telecommunications facilities and systems shall be referenced to (known in terms of) the existing standards of time and frequency

maintained by the U.S. Naval Observatory, UTC (USNO), or the National Bureau of Standards UTC (NBS)". Furthermore, "the accuracy of this time and frequency information with respect to UTC (USNO) or UTC (NBS) shall be commensurate with the individual system design and interface requirements". The above statements may be interpreted as specifying that the DCS synchronization subsystem reference universal precise time [UTC (USNO) or UTC (NBS)] and to provide the vehicle with which the reference may be distributed throughout the network. In addition, how accurately these references are maintained depends on the capability of the synchronization system and limitations imposed by interfacing requirements.

The current design of the Timing Subsystem affords easy compliance to the above-mentioned Federal Standard. Each TS prototype can reference any one of three auxiliary external sources in 1-pps format. Accuracy limitations imposed are dictated by the resolution of the time interval measurement system which is 10 ns for the current design. This is especially applicable for the case of directed control where only one node need reference an external precise time reference. This (master) node is then configured to follow the reference via its internal PLL tracking system. Slave nodes then indirectly follow the universal time reference. Other aspects of network synchronization are not directly impacted by the Standard. These include self organization, independence of clock error measurement and correction, and phase reference combining features [6.9].

One of the more compelling reasons for recommending the DCS reference precise time is to comply with Federal Standard 1002. This is not seen as an obstacle but rather as a desirable feature in any large network, since compliance to the Standard does not present any hardship. Presently, DCA is committed to provide DSCS terminals which are slaved to precise time via satellite time transfer.

6.4 Timing Technique Evaluation

It would be exceedingly difficult to summarize the performance of each candidate timing technique by a direct comparison of features. Correspondingly, it is not just a matter of saying that candidate A is better than candidate B; each technique has its own merits and none of them are considered superior in all evaluation categories. However, during the course of this program, it became clear that, at least from observed network

synchronization, the performance of each technique would be, within given measurement capabilities, nearly identical. This is due primarily to the fact that such a small (three-node) network was configured. Although it was not possible to thoroughly analyze the advantages and tradeoffs associated with each of the synchronization techniques as applied to large networks, much insight was gained as to the implementation difficulty and "ease of use" once in the field. The reader is referred to [6.9] and [6.10] for discussions of timing technique performance in larger networks. Much of the comparison for this program was carried out at the network level; that is, link characteristics were not investigated in detail as a previous CNR effort [6.5] evaluated TROPO and LOS link performance when used to support a timing function.

For a review of each of the timing technique candidates, see Section 5.2; they will not be repeated here. To begin the comparison, the reader is reminded that each of these techniques was implemented with identical Timing Subsystem hardware; no modifications were required when specifying different timing algorithms since they existed totally in software. Each Timing Subsystem contains a precision time interval counter, FIFO, and level-1 MUX, thus eliminating the need for retrofit or redesign of service channel MUX. Some problems occur when extracting framing pulses from existing equipment (e.g., modems) for SDLC TRIP transmission, but these problems are not difficult to overcome. The next section addresses some of these issues.

Much of the field effort was spent getting on-the-air and keeping the link equipment operational. Thankfully, the Timing Subsystems proved to be extremely reliable and not one failure was experienced (a bad batch of power supplies and a lightning strike slowed progress somewhat) once in the field. As explained in Sections 3 and 5, only a single-ended tandem network was possible, dictated by the equipment that was working. The lack of a double-ended link precluded the use of Time Reference Distribution as it was intended to be used. This is especially true for the Improved Time Reference Distribution technique in which phase reference combining is introduced to enhance system accuracy [6.20]. Double-endedness is a necessary feature to preserve precise time and to eliminate path delay factors across a link. However, for the sake of an exercise, the original Time Reference Distribution scheme [6.21], as modified by the

Clarkson College study [6.22], was run successfully when tried with single-ended transfers (see Section 5.5.4 for details of this experiment).

Much of the experimental program was spent investigating the performance of a simple or tandem Master/Slave scheme. Although only single-ended transfers were possible, the overall simplicity of this technique, as a main or fallback system, should not be overlooked. This has been emphasized by several studies [[6.5], [6.9], and [6.10], for example), and is emphasized here again. Other than Independent Clocks, Master/Slave required the least software and channel overhead. However, its merit as a wartime system is questioned, especially to its lack of self-organization capabilities. Clearly, some form of clock control distribution would be desired, or perhaps an adaptive reorganization scheme such as that employed by the Canadian Dataroute [6.23],[6.24].

Such features are fundamental to the Improved TRD technique which has the qualities most often associated with a survivable system. As listed in Section 5.2.4, these are:

- Directed control
- Double-endedness
- Independence of clock error measurements and corrections
- Self-organizing
- Phase reference combining

Without going into further detail about these concepts, the reader is referred to [6.20] and [6.25] - [6.28] which offer more complete studies.

Mutual Synchronization offers very little over other techniques except to distribute references to all nodes in the network. Reference [6.9] demonstrates that MS is, at best, a somewhat unstable system with system-wide errors compounding if a nodal clock goes bad. Mutual systems that reference a single master may have added merit, but they will not be discussed here. Laboratory tests only strengthened our position that mutual control systems should <u>not</u> be considered for large networks where many closed loop timing paths and instability would most certainly be the result. In-house tests confirmed that the potential for network instability is great - even in smaller systems. Careful prefiltering of calculated clock error must be observed.

In short, it is suggested that Mutual Synchronization not be considered for use in DCS as a wartime system because the other techniques, or perhaps combinations of them, offer superior advantages over the mutual system, especially in large networks.

In contrast, the simplest method, that of Independent Clock, has been shrugged off by some as totally unacceptable and by others as a technique worth some careful consideration. The concept of Independent Clock has some merit, especially when one considers the precision frequency standards and large FIFO buffers available (to absorb frequency offsets). With high-quality equipment, buffer resets could be anticipated only after several days, for the worst case. Also, installation costs are moderate, but a host of processing and loop control equipment could be eliminated. In the effort of maximally utilizing available time, CNR did not test Independent Clocks in the field, although it is not difficult to predict performance via a few calculations or a simple simulation. Instead, it is stated that if it were not for a periodic interruption of traffic, this technique would most likely be given more credit.

Finally, it should be clear that recommendations are narrowed down to Master/Slave and TRD choices. Without choosing either one it should be stated that Improved TRD was not completely exercised on the Test Bed network due to the lack of transmission facilities to provide double-ended transfers. However, it is clear that Improved TRD has been designed to incorporate all of the "suggested attributes" [6.26],[6.29] for timing in the future DCS.

The distinctive feature of Time Reference Distribution is that a network with reasonably stable clocks at each node is forced to take corrective action at these nodes on the basis of perceived clock errors which are continually passed around the network from node to node. As in the previous discussion (Section 5.2.4 and Appendix A), all nodal clocks are rank-ordered and the timing of each incoming link is compared with the local clock in the derivation of a timing error for that link. This error signal is transmitted back to the originating node which is likewise computing its own nodal clock error for the link. With the ensuing exchange of clock error signals between both ends of the link, each of the two nodes has the capability of computing the true nodal clock time difference with virtually no dependence on path delay.

The selection rules ensure that no closed loops are set up, mainly because of the reduction in rank which occurs for a clock signal as it is passed through additional links. The principal advantages of the Time Reference Distribution technique over other synchronization methods, such as independent stable clocks or Master/Slave configurations, can be stated as follows:

(1) The most accurate clock available in the network always governs the complete system.

(2) Self-monitoring of node performance is enhanced by the availability of the various link time error signals.

(3) Propagation of medium delay variation is minimized by the cancellation of path delay in the formulation of error signals.

(4) Successful system operation is not dependent upon the continued operation of any one node. In the event of failure of the current master node, the system reorganizes to find an alternative master substitute. The resulting transition would be smooth provided the local clock-circuit time constant was long compared with the time to reorganize and/or sufficiently large data buffers were available to absorb transient effects.

(5) Network growth and change are easily accommodated (e.g., upgrading of clocks at the nodes).

With the additional refinements built into the proposed Time Reference Distribution technique [6.20], there is ample evidence that TRD should perform well in a large network, especially when referenced to universal time (its intended application)[6.27].

It should be recognized that recommendations are based on several criteria. First, much of the initial reaction to each technique was formed when implementing each in software. At that time, the ease of putting the algorithms into code was discovered as well as any problems with interpretation. For this comparison Improved TRD was more difficult to interpret and implement with TRD, Mutual Sync, Master/Slave, and Independent Clocks following. Appendix A contains a review of the TRD techniques, including flowcharts of the algorithms.

Secondly, laboratory tests revealed the characteristics of each technique at the network level. Several experiments were run demonstrating, for instance, the general behavior of directed control systems, including the self-organizational capabilities of TRD. Each candidate technique appeared to work well (within the bounds of the test equipment limitations). Mutual Sync proved to be somewhat temperamental, and even with additional error prefiltering, never performed satisfactorily (see Section 5.2.3). Overall, the TRD techniques seemed to be most promising although defining and inputting nodal parameters was rather tedious. In contrast, Independent Clocks and Master/Slave required minimal setup time.

Finally, field tests, though limited, further reinforced the preferences formed in the laboratory. No surprises were found in TS behavior and, in general, the directed control (including TRD) experiments performed admirably.

In summarizing the capabilities of the techniques, it should be evident that each will work when applied properly. Although it would be difficult to endorse a particular technique in light of a somewhat limited experimental program, enough insight has accumulated to allow a certain degree of acceptance with previous findings; for example, it seems apparent that any one of the candidate techniques is applicable at the highest level of the DCS hierarchy (with great reservations about Mutual Synchronization). Also, due to the connectivity of the network, the lowest level nodes should be slaved to their corresponding intermediate or highest level node. This is due to the limited connectivity that characterizes the lowest level nodes [6.10]. Therefore, it is felt that Master/Slave is a good choice for the lowest levels of network hierarchy, while the reorganizational and phase accuracy traits of TRD are well-suited for use on the higher levels of network topology where survivability, accuracy, and monitorability are the essential ingredients.

6.5 Future Work in Network Synchronization

Throughout the test program, the Timing Subsystem proved to be reliable, efficient equipment. Every precaution was observed to build a system capable of meeting the interfacing requirements for both current and future DCS equipment while incorporating programmability. Based on experience gained in this contract, it is possible to make recommendations concerning

the general approach to network synchronization and the adoption of a timing technique by the DCS. This section labels some of the more practical obstacles encountered in the field as well as suggestions for an advanced development model based on the current TS design and operating experience in a network environment.

Without a doubt, before a strong synchronization technique recommendation can be made, much more testing in a larger (say, at least six nodes) Test Bed should be conducted. Surely, if such a task were to be undertaken, based on experience, network synchronization experiments should be limited to Master/Slave and Improved TRD, or some combination thereof. Master/Slave could provide the simple reliable base for timing distribution (directed control) while the self-organizing and increased accuracy features of Improved TRD may be used to enhance this already field-proven technique [6.28].

One of the major advantages of directed control is the potential cost savings associated with the use of quartz standards in place of atomic standards at the hundreds of less significant nodes provide justification for development of the Timing Subsystem to accommodate them. Throughout this report we have endeavored to highlight design features which will enhance the performance of quartz standards. An example is the attention we have given to automatic tracking of the local standard frequency drift and offset that occur with aging. It should be realized that the DCS network can be expected to run for very long periods with a single high-quality master standard, and such intervals provide the subservient nodes an opportunity to qualitatively assess the offset and drift of their own station standards. Then, in times of network stress when independent clock operation may be called for, this knowledge can be used to compensate the local standard with better results than without clock correction.

A major portion of the field effort for this program was spent trying to get 'on-the-air'. The sheer quantity of equipment associated with even a small network requires a truly dedicated technical staff to maintain and operate it, especially at geographically distant sites. For larger networks, the staffing burden becomes even greater. Currently, surveys have shown that networks with relatively simple timing schemes have required the skills of engineering-level personnel to deploy and operate the associated timing equipment because the lack of a

ready supply of digitally-oriented field personnel was noted [6.9]. However, the subsystem type or its features had little influence on deployment difficulties. Therefore, overall simplicity and high monitorability should be considered desirable traits. Future timing subsystems should provide automatic self-monitoring and be able to warn personnel of an approaching fault condition. This may be implemented with control software as necessary, although signal or power supply monitoring may require additional hardware considerations. Hardware status indicators should be available to site personnel at all times.

The area of equipment reliability, although briefly addressed, is not considered a problem as indications have shown that timing and synchronizing equipment is highly reliable. This was substantiated by zero failures in the field after periodic operation over a span of about six months. Frequency standards also are quite reliable and should serve to enhance overall network reliability.

Additionally, further development in Timing Subsystem software could provide added features. Since the TS contains a general-purpose microcomputer capability, programming options are virtually unlimited. It is, however, important to rigorously define not only the nodal processing and data flow techniques but also to specify the nature and extent of interaction with the operator. It makes sense to utilize software capabilities to the fullest extent; feedback to a node operator perhaps being one of the more urgent possibilities. Powerful monitor software would greatly improve operability and lessen the need for highly experienced or engineering-level personnel at each installation. System status directly output to the user could serve as an early warning system for pending problems. Overall "ease of use" would be greatly improved by user friendly, English-like dialog. Significant changes in the node software may be incorporated without jeopardizing the hardware design or capabilities.

Clearly, network testing on a larger scale than possible during this program would then provide additional information necessary to confirm these preliminary findings. The Timing Subsystem is certainly capable of operating in a larger network. Link redundancy must be thought of as an important factor in a larger network; that is, how will a timing candidate cope with a closed loop timing path? It is not practical to resolve this question here, but experimentation with a technique such as Improved TRD could provide insight to this problem. Another

area worth at least some investigation is the effect of clock control loop bandwidth on the performance of network synchronization. Although the TS incorporates a multi-stage PLL algorithm with programmable parameters, the testing schedule did not allow experimentation in this area, and it is suggested that future work address this subject. For the sake of the test plan, loop parameters similar to those in the CNR effort, under Contract F30602-76-C-0347, were used because they were chosen as effective for the communications links employed (see [6.5]).

The Timing Subsystem development program has sufficiently demonstrated that communication link termination, clock control and correction, network synchronization, and performance assessment capabilities can be implemented using a single microcessor-controlled device. Furthermore, there is ample evidence that the current design can support the interfacing and processing requirements for an advanced development model well into the foreseeable future. It has been recommended that the next generation Timing Subsystem incorporate improved operating software while maintaining the basic design and programmability of the system. As many options as possible have been left open to enhance flexibility and to insure that future applications can be handled without the need for large expenditures or redesign.

Recently, a set of desirable attributes has been suggested for adoption into the digital DCS to increase the suitability for wartime use [6.27]. These attributes address both the hardware associated with the timing system and the desired features of the synchronization technique itself. The main approach is to provide a more reliable, survivable system capable of supporting a timing function in a hostile environment. Including these attributes into the Timing Subsystem is well within the capabilities of hardware and software. Many of these features are inherent in the design of the system, while others require incorporation into the timing technique currently residing in software. Overall, the current Timing Subsystem design provides a firm base for development of future subsystems intended to possess the fundamental characteristics considered essential ingredients of the DCS or other communications systems.

REFERENCES

[6.1] M6800 Programming Reference Manual, Motorola, Inc., 1976.

[6.2] Am9511 Arithmetic Processor, Advanced Micro Devices, Inc., 1978.

[6.3] CNR, Inc., "Timing Subsystem Development," Proposal P-97 to Rome Air Development Center, February 1978.

[6.4] CNR, Inc., "Timing Subsystem Development Design Plan," Contract No. F30602-78-C-0287 with Rome Air Development Center, March 1979.

[6.5] CNR, Inc., "System Timing and Synchronization," Final Report on Contract No. F30602-76-C-0347 with RADC, May 1978.

[6.6] D. Chase, et al., "Troposcatter Interleaver," Final Technical Report, RADC-TR-76-213, CNR, Inc., July 1976.

[6.7] D. Chase, et al., "Troposcatter Interleaver Study Report," Final Technical Report, RADC-TR-75-19, CNR, Inc., February 1975.

[6.8] CNR, Inc., "Timing Subsystem Development Computer Program Manual," Contract No. F30602-78-C-0287 with RADC, September 1981.

[6.9] M. Williard, et al., "DCS Synchronization Subsystem Optimization/Comparison Study," Harris Corp., Final Report, November 1979.

[6.10] Harris Corp., "Study of Alternative Techniques for Communication Network Timing/Synchronization," Final Report, March 1977.

[6.11] H. Stover, "A Time Reference Distribution Concept for Time Division Communication Network," Paper presented at 5th Annual PTTI Meeting, November 1973.

[6.12] J. L. Jespersen, et al., "Characterization and Concepts of Time-Frequency Dissemination," Proc. IEEE, Vol. 60, May 1972, pp. 502 - 521.

[6.13] J. L. Jespersen and L. Fey, "Time Telling Techniques," IEEE Spectrum, May 1972, pp. 51 - 58.

[6.14] R. B. Kershner, "Transit Program Results," Astronautics, Vol. 5, May 1961, pp. 30 - 38.

[6.15] R. L. Easton, "The Role of Time Frequency in Navy Navigation Satellites," Proc. IEEE, Vol. 60, May 1972, pp. 557 - 563.

[6.16] L. E. Gatterer, et al., "Worldwide Clock Synchronization Using a Synchronous Satellite," IEEE Trans. Instr. and Measurement, Vol. IM-17, December 1968, pp. 372 - 378.

[6.17] D. W. Hanson and W. F. Hamilton, "One-Way Time Synchronization via Geostationary Satellites at UHF," IEEE Trans. Instr. and Measurement, Vol. IM-20, August 1971, pp. 147 - 153.

[6.18] D. W. Hanson and W. F. Hamilton, "Clock Synchronization from Satellite Tracking," IEEE Trans. Aerospace and Electronic Systems, Vol. AES-7, September 1971, pp. 895 - 899.

[6.19] D. W. Hanson and W. F. Hamilton, "Satellite Broadcasting of WWV Signals," IEEE Trans. Aerospace and Electronic Systems, Vol. AES-10, September 1974, pp. 562 - 573.

[6.20] H. A. Stover, "Improved Time Reference Distribution for a Synchronous Digital Communications Network," Proc. PTTI Meeting, November 1976, pp. 147 - 166.

[6.21] H. A. Stover, "Time Reference Concept for Timing and Synchronization of the Digital DCS," DCASEFTC 39-73, July 1973.

[6.22] Clarkson College of Technology, "A Study of Microprocessor Implementation of Time Reference Distribution," RADC Phase Report TR 77-20, June 1977.

[6.23] J. G. Baart, et al., "Network Synchronization and Alarm Remoting in the Dataroute," IEEE Trans. on Comm., November 1974, pp. 1873 - 1877.

[6.24] S. Harting and D. Swanton, "A 1.544 Mbps Multiplexer for the Data Route," National Telecommunications Conference Record, New Orleans, December 1975, pp. 7-17 - 7-20.

[6.25] H. A. Stover, "Communications Network Timing," DCEC Technical Report TR 43-75, September 1975.

[6.26] H. A. Stover, "Suggested Attributes for Timing in a Digital DCS, " Paper presented at 11th Annual PTTI Meeting, November 1979.

[6.27] H. A. Stover, "Attributes for Timing in a Digital DCS," DCEC Engineering Publication No. 1-80, July 1980.

[6.28] H. A. Stover, "Overview of Timing/Synchronization for Digital Communications System," Paper presented at the 10th Annual PTTI Meeting, November 1978.

APPENDIX A

SOFTWARE IMPLEMENTATION OF TIME REFERENCE DISTRIBUTION TECHNIQUES

This presentation of TRD interpretation is intended to be used as a guide to the techniques employed by CNR to implement these algorithms in software. The organization is as follows:

- The first section describes TRD as presented in [1] and the Clarkson College Report [2] which includes an obsolete data handler not specified in the original TRD proposed by H. Stover [1],[3].

- The second section describes an Improved TRD Technique [4] which includes several refinements to enhance monitorability and improve accuracy.

Each technique is presented along with flowcharts to aid in visualizing the sequence of events within the algorithms.

1.0 Time Reference Distribution

This method of Time Reference Distribution is a modified version of self-organization which has been shown to organize a network as well as reorganize it after a disturbance. It ensures the automatic selection of the highest ranking node as the master node as well as transmission of information to each node from this master node by a path of minimum demerit. In addition, once the network has been organized, each node knows its position with respect to the master node in the hierarchy structure along which information is disseminated throughout the network.

TRD consists of a simple set of rules which permit each node to choose its time reference from that particular neighboring node which will result in the local node getting its ultimate time reference from the best clock in the network over the best transmission path from that ultimate reference clock. When failures occur somewhere in the network, problems can result unless sufficient time is allowed for obsolete information to be swept from the network following a failure. Since information about a failure progresses only one node farther from the failed node (or the node associated with a failed link)

for each information transfer, many information transfers might be required before obsolete information is replaced [2].

This problem resulted because nodes were permitted to make decisions based on obsolete information following a failure in the system. The problem can be avoided by assuring that any node which must change to an alternate reference as the result of a failure in the network waits a sufficient length of time for obsolete information to be replaced in the adjacent node from which the reference will be taken. Several different approaches are possible for determining the number of information exchanges to wait before accepting an adjacent node as a reference. For the type of operation of interest, this does not appear to be a critical factor so long as the waiting time is at least great enough [2].

The TRD process is an implementation of the algorithm specified in the Clarkson College Report [2]. The algorithm is identical to the H. Stover Report [3] except that Dr. Perreault's proposed solution to the obsolete data problem is implemented. See Figure 1.

The first part of the algorithm performs the selection of the best available reference according to the rules specified in both reports. These rules applied in order are:

Rule 1: A node initially entering the network will temporarily reference its own clock until a better selection is made.

Rule 2: Whenever the link or neighboring node which a node uses for its immediate time reference fails, the node will temporarily reference its own clock until an alternate selection is made.

Rule 3: If a neighboring node being used as the immediate reference should have a change in its ultimate reference to one of a lower rank, the local node will temporarily reference its own clock until an alternate selection (which could be the same one again) is made.

Rule S1: Select the neighboring node that has the best N1, if inconclusive apply S2

Rule S2: Select the neighboring node of those selected by S1 that has the best N2, if inconclusive apply S3

Rule S3: Select the neighboring node of those selected by S2 that has the best N3

The actual reference switch cannot be done with only these rules or the problem of obsolete data existing in the network during reorganization can occur. An update counter can be provided at each node and used as parameter N4 in addition to parameters N1, N2 and N3.

The solution to this problem proposed in the Clarkson College Report involves the application of three more rules in order using the local and received update counter (N4) values:

Rule D1: When the tentative best reference is the node itself, the update counter is decremented by 1 (to a minimum of 0).

Rule D2: If the received update count from the tentative choice is smaller than the local update count, the tentative reference selection is confirmed and the received update count is incremented by 1, and thereafter used at that node.

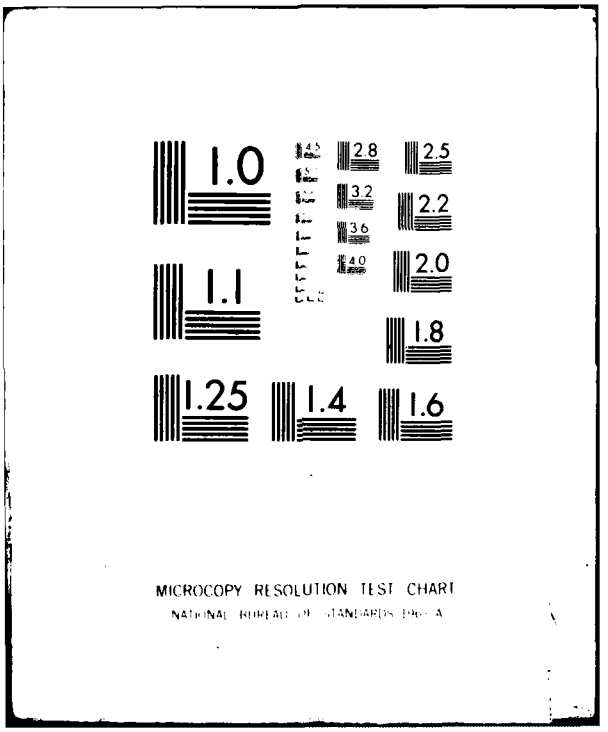
Rule D3: Otherwise, the node uses itself for a reference and increments its own update counter by 1.

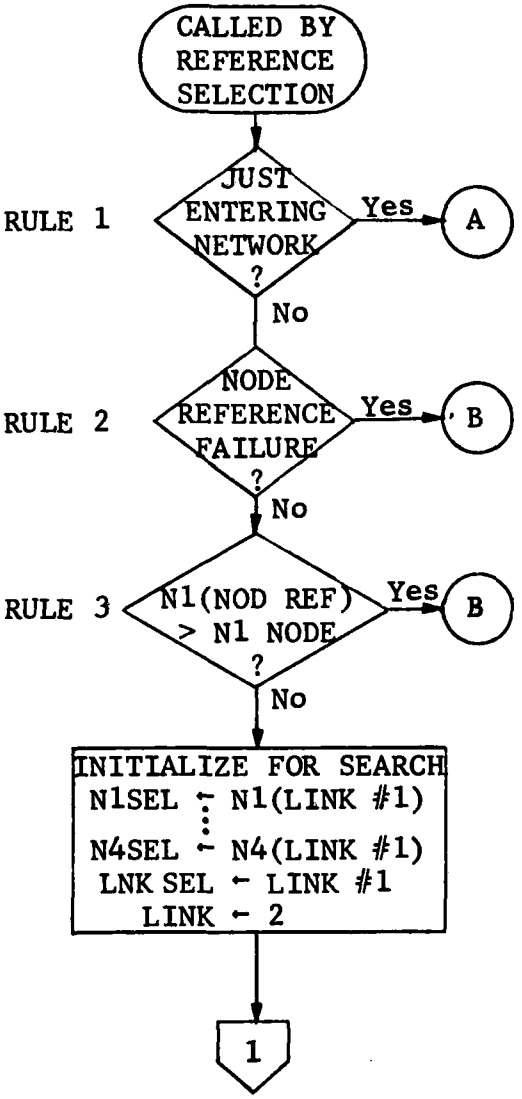
The reader is referred to References [1], [2], [3] for further discussion of this algorithm.

2.0 Improved Time Reference Distribution

The Improved Time Reference Distribution technique described here also selects the highest ranking clock as master. Within this approach, the natural hierarchy determined by the network connectivity is employed; instead of only supplying timing information over the best path (of least total demerit) to each node, the nodes determine the error in their local clocks by either using information from all neighboring

AD-A117 609 CNR INC NEEDHAM MA F/G 9/3
TIMING SUBSYSTEM DEVELOPMENT.(U)
MAY 82 K R BACKE F30602-78-C-0287
UNCLASSIFIED RADC-TR-82-124 NL


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A



N1 - ULTIMATE REFERENCE RANK
N2 - PATH DEMERIT (CUMULATIVE)
N3 - NODE RANK
N4 - UPDATE COUNTER

Nm SEL - Nm OF SELECTED NODE
LNK SEL - SELECTED NODE #
Nm(LINK) - Nm OF (NODE # = LINK)
NOD REF - NODE # OF LINK TO BE USED AS IMMEDIATE MASTER

Figure 1 TRD Reference Selection

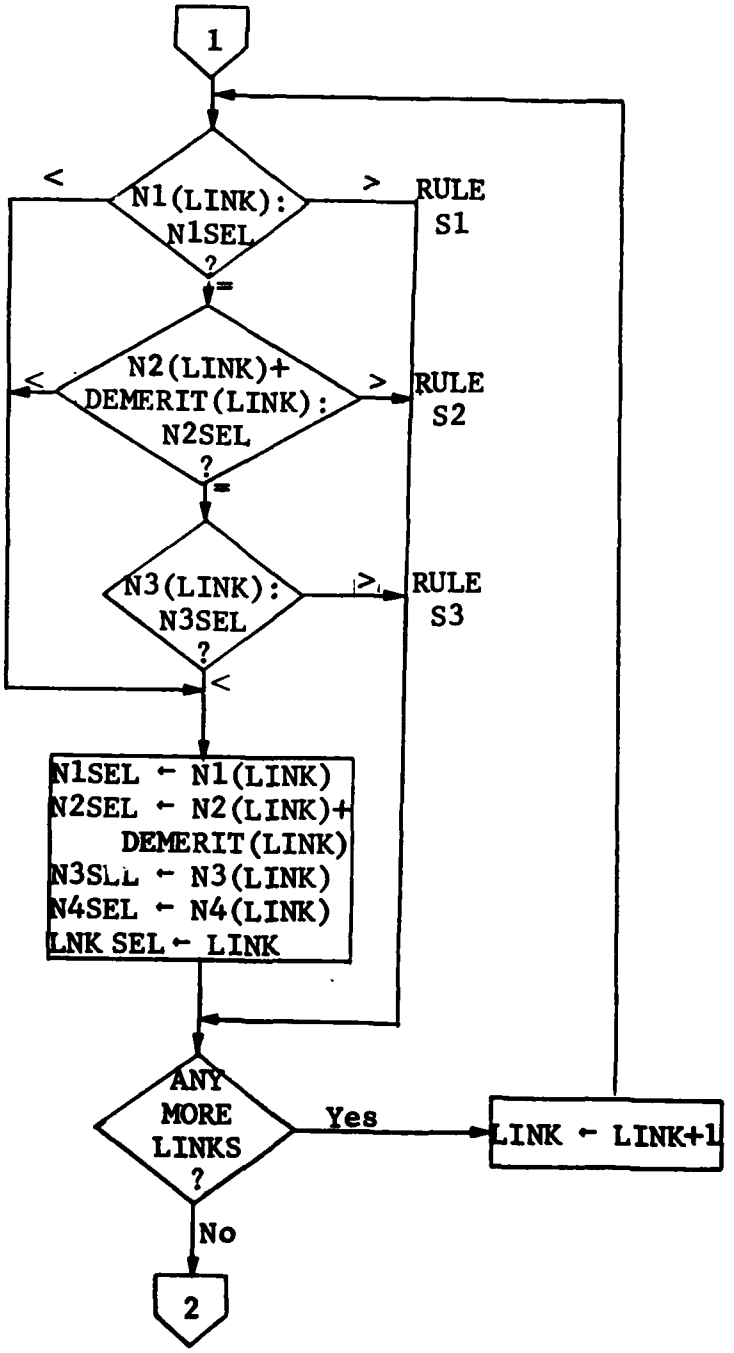


Figure 1 (Continued)

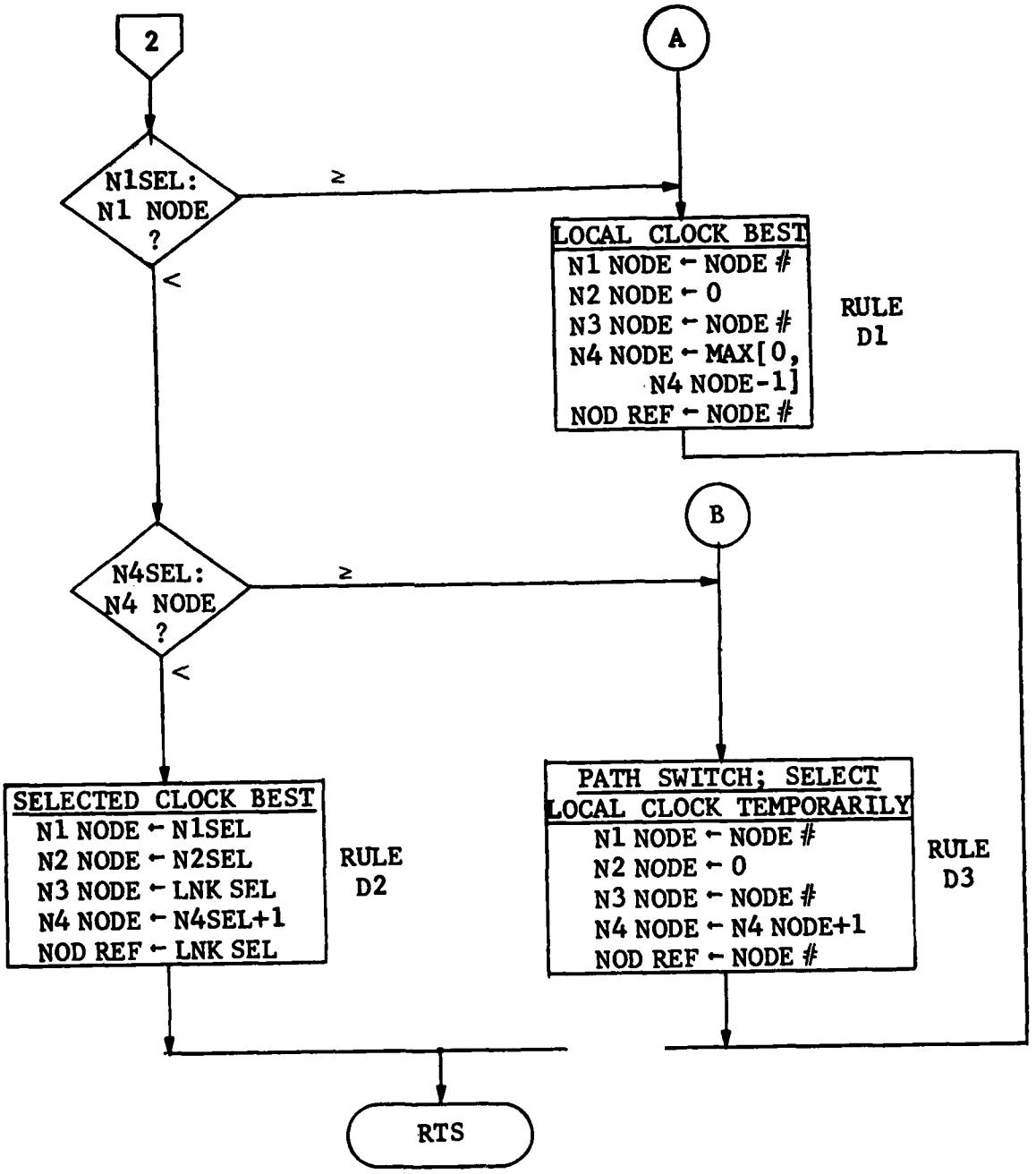


Figure 1 (Continued)

(directly connected) nodes higher in the hierarchy than the local node or by using information from all neighboring nodes not lower in the hierarchy. To do this, information is exchanged between neighboring nodes and there are a set of procedures or rules for applying this information. Furthermore the selection of the paths for distribution of the time reference and the measurement of the error in the local clock are independent of the correction of the errors in any of the other nodal clocks. This permits error correction in any clock to be made with minimum perturbations of the network while still not interfering with the accurate measurement of the error in any other clock. This is accomplished by having each node in the network inform its neighbors of the measured but uncorrected error in its own clock [4].

The Improved Time Reference Distribution technique as defined in [4] is implemented in software. In lieu of presenting the entire discussion, the following paragraphs are excerpts from [4] and should provide a basic understanding of this algorithm.

> Quite a large number of desirable characteristics can be listed for the timing subsystem of a large digital communications network. Although it cannot be proved that these characteristics are necessary, many of them are widely accepted as desirable. These include: (1) Any node should be able to obtain all required timing information from its neighbors (directly connected nodes) without need to communicate with more distant nodes; (2) The timing subsystem should accommodate failures or destruction of major parts of the network and still remain operational; (3) Timing perturbations at a node should not propagate to other parts of the network (i.e., when one node makes a correction or other change in its clock, it is not desirable for this to propagate through the network like falling dominoes); (4) There should be no closed timing loop that could potentially contribute to system instability; (5) The timing subsystem should permit systematic self-monitoring to provide early detection of malfunctions so that they can be corrected before they interrupt communications traffic; (6) The communications timing subsystem should be compatible with other timing subsystems such as those employed for navigation; and (7) The timing subsystem should be self-organizing, initially and following failures.

An error in a clock at any level of the timing hierarchy should not affect the measurement of the clock error at any node lower in the hierarchy. Further, the selection of the paths for distribution of the time reference and the measurement of the error in the local clock should be independent of the correction of the errors in any of the other nodal clocks. This permits error correction in any clock to be made with minimum perturbations of the network while still not interfering with the accurate measurement of the error in any other clock. This can be accomplished very simply by having each node in the network inform its neighbors of the measured but uncorrected error in its own clock.

Two classes of timing information are maintained at each node:

Class 1 Timing information is based only on information received from nodes higher in the hierarchy than the local node.

Class 2 Timing information is based on information received from all nodes not lower in the hierarchy.

In order to provide an effective self-organizing method of accurately distributing a time reference through a digital communications network, information is exchanged between neighboring nodes. This information is applied in compliance with a set of rules. These rules are discussed in the text after the following list of information which is transmitted by each node to its neighbors:

INFO 1. Rank of the clock used as the master time reference for the local clock. (This information is used to assure that the highest ranking clock in the network is used as master and to establish the order of precedence to master when a master fails.)

INFO 2. Number of links between the local node and its master time reference. (This information is used to establish the desired hierarchy.)

INFO 3. Time of the clock at the remote end of the link (including the effect of the time required for the signal to transit from the remote node to the local node) as measured by the clock at the local node.

INFO 4A. Measured but uncorrected error in the local clock based on information from those neighbors higher in the timing hierarchy than the local node. (The term measured error as used here includes errors obtained by mathematically combining other measurements and the error in this measured error will be called its inaccuracy.)

INFO 4B. Same as 4A, except based on information from those neighbors not lower in the hierarchy than the local node.

INFO 5A. Estimated inaccuracy, stated as a variance (or standard deviation), of the local clock based on information from all neighboring nodes higher in the hierarchy than the local node.

INFO 5B. Same as 5A, except based on information from all neighbors not lower in the timing hierarchy than the local node.

Notice that the two classes of information under item 4 and the two classes of information under item 5 are distinguished by the sources of information used to obtain them and also by the nodes that make use of them. When the rules for their use are also considered, it will be observed that they prevent the formation of the closed feedback paths.

Each node applies the following set of rules for the use of the information received from its neighbors.

RULE 1 A node initially entering the network will use its own clock as its time reference until a better reference can be determined. Its own clock provides a basic time reference to which the node always returns when it has no better reference available. Under these conditions, the local node supplies the rank of its own clock to its neighbors as INFO 1.

RULE 2 The first type of information received from neighboring nodes, INFO 1, provides the local node with the rank of the clock used as the master time reference by each of its neighbors. If one or more neighbors' reference clocks outrank the local clock, the node will select those neighbors (or the single neighbor) referencing the highest ranking master and use them (or it) in determining its own time reference, i.e., measuring the error in its own clock. The rank of the master time reference used by the selected neighbors will be supplied to all neighbors as INFO 1, i.e., the rank of the clock used as master for the local node. Continued application of this rule by all nodes will result in all nodes referencing the same highest ranking master clock.

RULE 3 If the local node is referencing its own clock, there are no links between the local node and its master reference and this information is supplied to its neighbors as INFO 2. The second type of information, INFO 2, as received from its neighbors provides the local node with information about the number of links between each neighboring node and that neighbor's master time reference. Unless the clock at the local node outranks the master reference of all of its neighbors, the number of links between the local node and the master is greater by one than that of the neighbors (or neighbor) selected by Rule 2 which have the least number of links between themselves and their master. This information is supplied to the neighboring nodes as INFO 2. Continued application of this rule will result in establishing the desired natural hierarchy. INFO 2 information as transmitted to neighboring nodes and as received from them indicates the position in the hierarchy of the local node relative to each of its neighbors.

RULE 4 The third type of information, INFO 3, as received from neighboring nodes provides the local node with the time difference between the local clock and the clock at each neighboring node (including the signal transit time from the local node to the neighboring node.) INFO 3 as transmitted to the corresponding neighboring node is subtracted from this information, and the difference is divided by 2. This provides a measurement of the actual time difference (no transit time included) between the local clock and the clock at each neighboring node.

RULE 5 Each neighboring node not higher in the hierarchy than the local node transmits to the local node, as INFO 4A, the Class 1 measured but uncorrected error of its own clock, i.e., the error determined using information from that neighbor's neighbors that are higher in the hierarchy than the neighbor. Similarly, each neighbor higher in the hierarchy than the local node transmits to the local node, as INFO 4B, the Class 2 measured but uncorrected error in its own clock, i.e., the error determined using information from that neighbor's neighbors that are not lower in the hierarchy than the neighbor. As received, thi this information gives a measured but uncorrected error for each neighboring node. To this is added the difference between the local clock and each neighboring clock as determined by Rule 4.

The result is a set of error measurements for the local clock based on information from each of its neighbors. (The reason for using Class 1 information from some neighbors and Class 2 information from others is to avoid closed feedback paths while still making very effective use of the available information.)

Figures 2, 3 and 4 depict the application of TRD rules 1 - 5 including an obsolete data handler similar to the previous TRD version discussed in the first section of this Appendix.

The following rules are represented by flow diagrams in Figure 5. Each portion delineated by the rules described below.

RULE 6 Each neighboring node not higher in the hierarchy than the local node transmits to the local node, as INFO 5A, the estimated inaccuracy, stated as a variance (or standard deviation), of its Class 1 measured error. Similarly, each neighboring node higher in the hierarchy than the local node transmits to the local node, as INFO 5B, the estimated inaccuracy, stated as a variance (or standard deviation), of its Class 2 measured error. This information, as received, is the estimated inaccuracy of the measured but uncorrected error associated with each neighboring node. Add to each member of this set of information (directly if stated as variances or as the square root of the sum of the squares if stated as standard deviations) the estimated inaccuracy of the

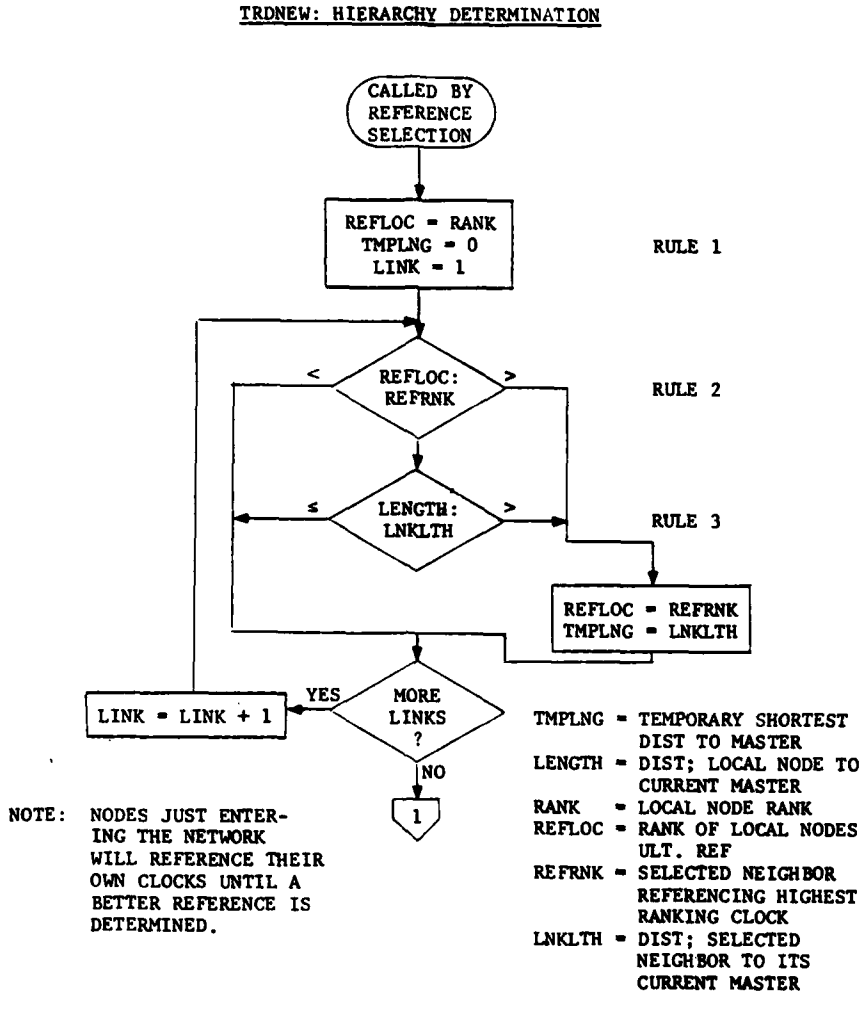


Figure 2 TRD Hierarchy Determination

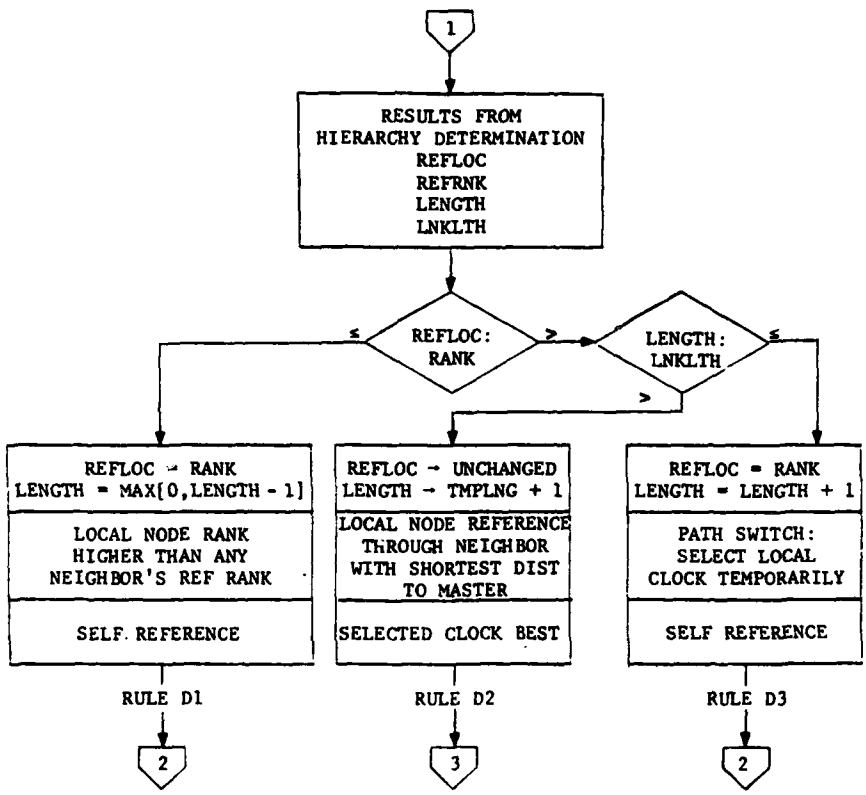


Figure 3 TRD Obsolete Data Handler

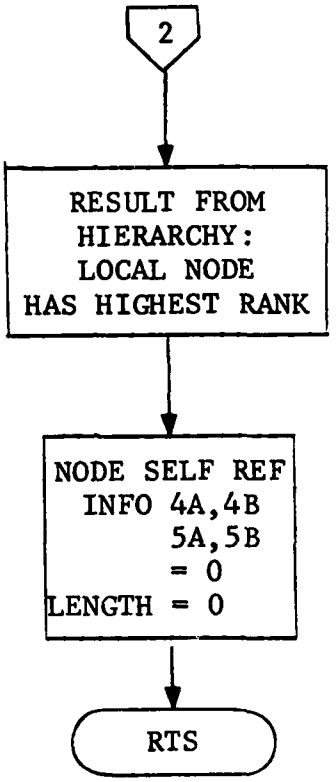


Figure 4 TRD Self Reference

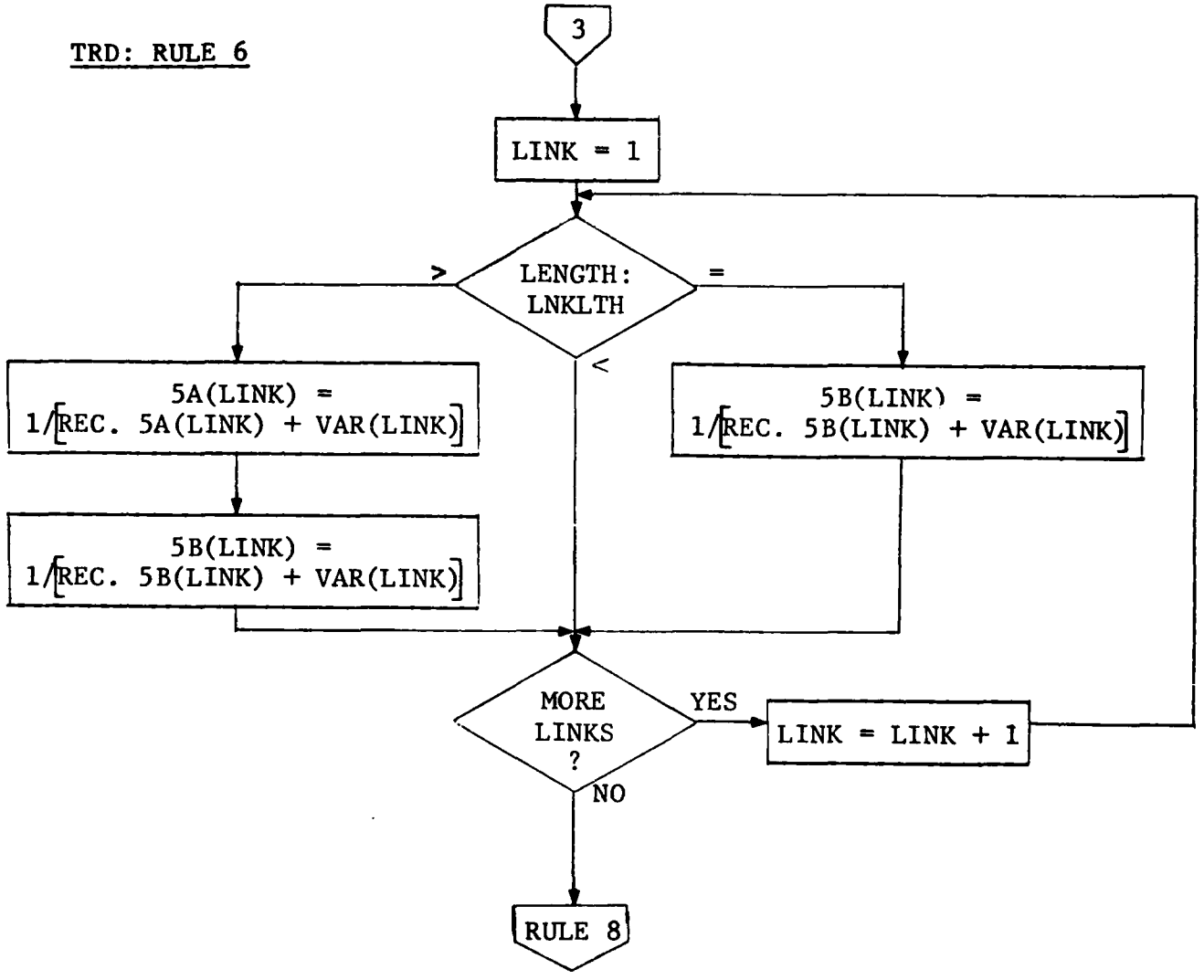


Figure 5 TRDNEW Error Computation

TRD: RULE 8

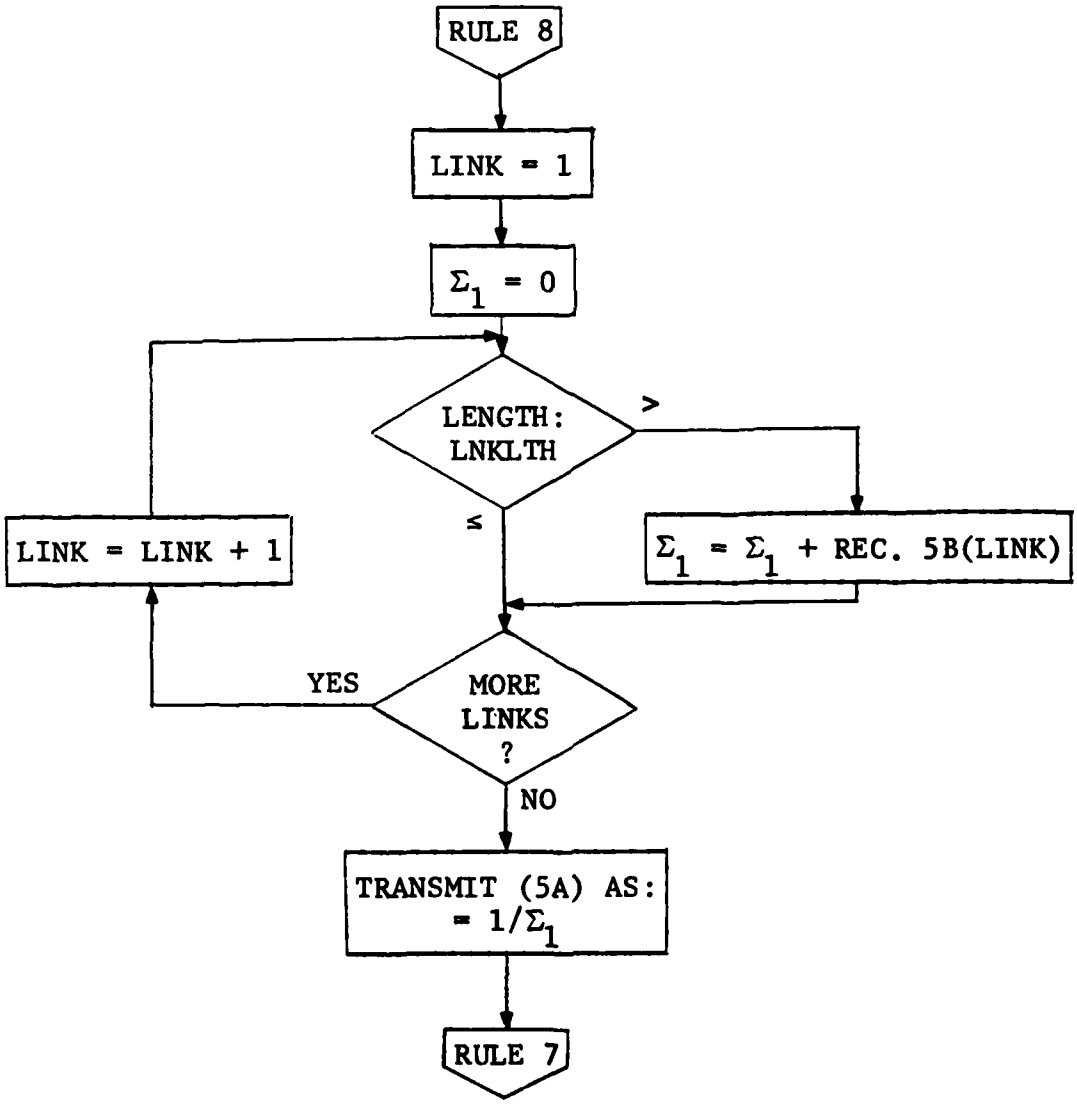


Figure 5 (Continued)

TRD: RULE 7

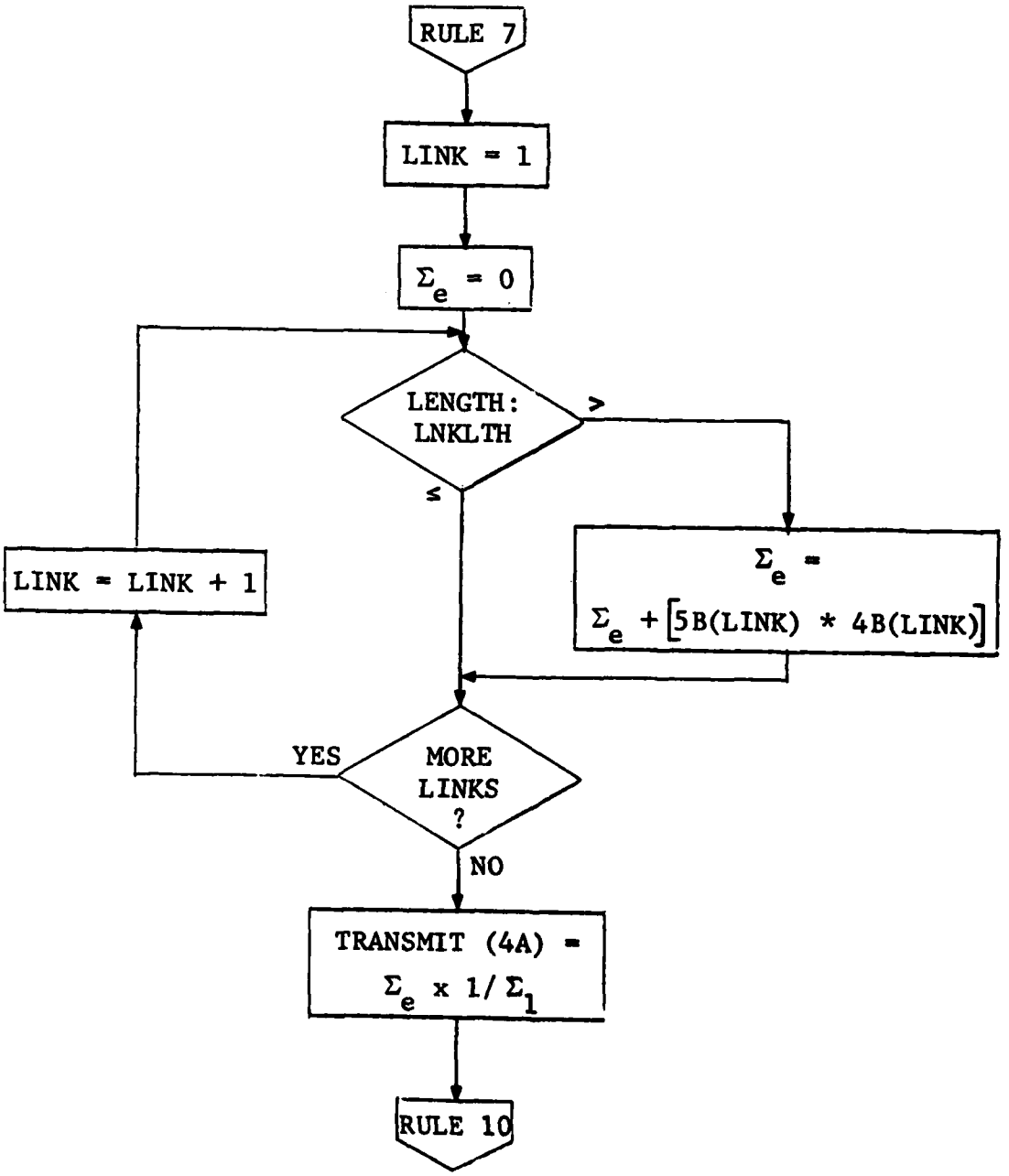


Figure 5 (Continued)

TRD: RULE 10

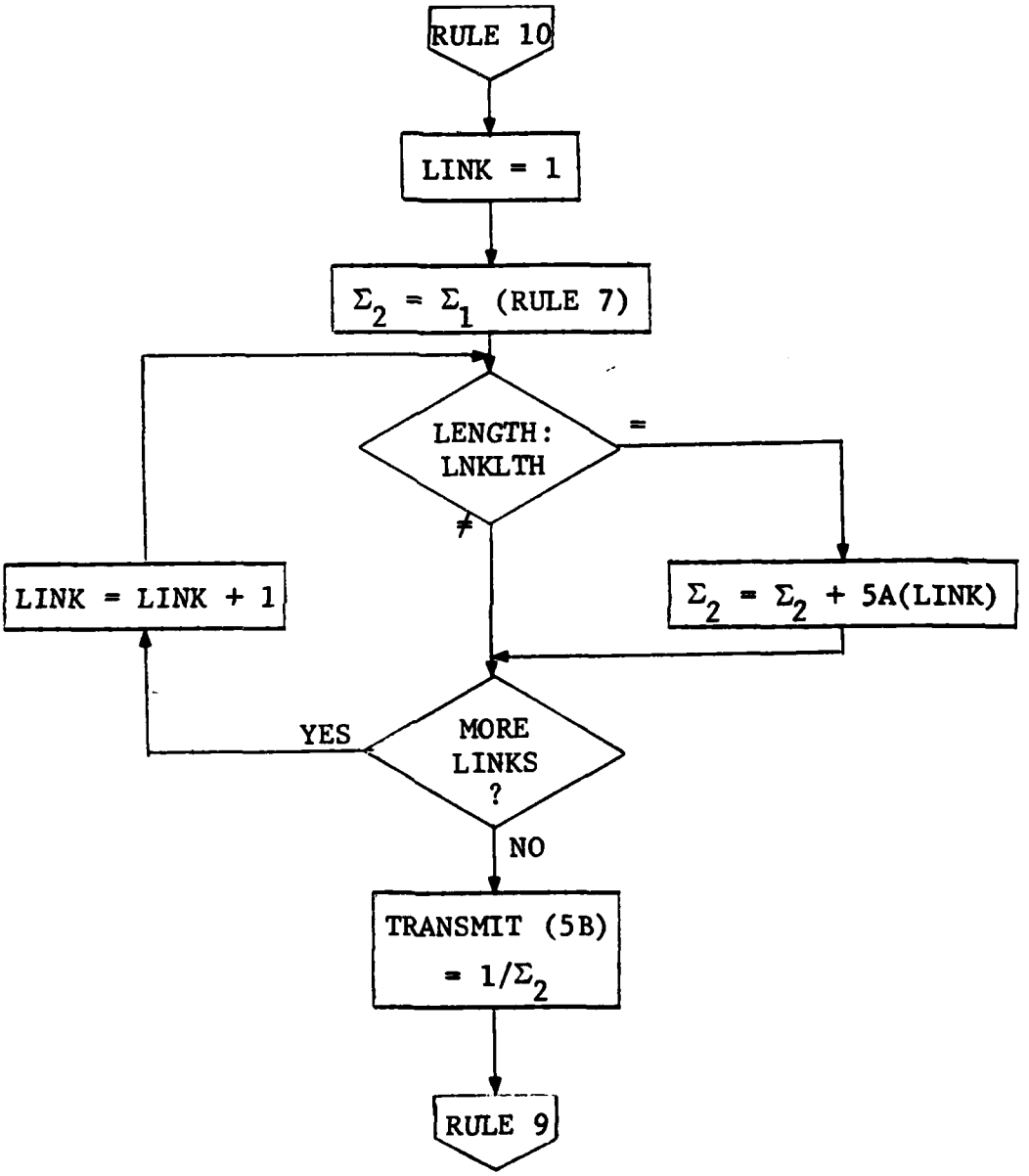


Figure 5 (Continued)

TRD: RULE 9

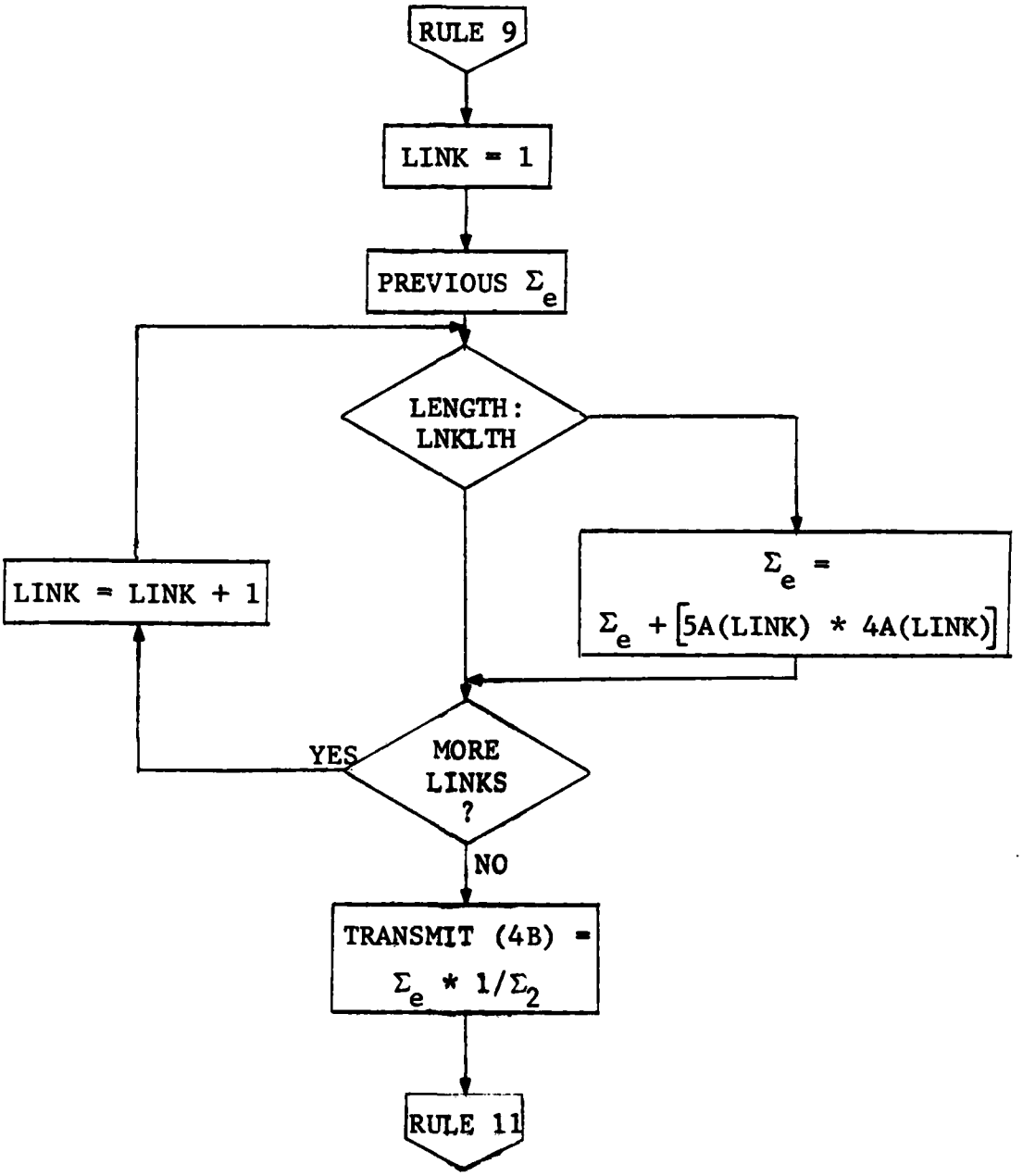


Figure 5 (Continued)

link between each neighbor and the local node as determined during engineering design. The result is a set of inaccuracies for the set of measured errors in the local clock based on information from each neighbor.

The estimated inaccuracy attributed to the link between the local node and a neighbor as established during engineering design includes several parameters. It includes an effect due to the differences in signal transit time in the two directions of the duplex link which includes delay differences in the transmitters and receivers at the two ends of the link. It also includes inaccuracies in the equipment used to measure timing differences between the received signal and the local clock.

RULE 7 From the set of error measurements for the local clock as determined by Rule 5, and the associated inaccuracies determined by Rule 6, only those for neighbors higher in the timing hierarchy than the local node are selected. These error measurements are combined to determine a Class 1 measurement of the error in the local clock, i.e., one based on neighbors higher in the hierarchy than the local node. This is supplied as INFO 4A, the measured error in the local clock, to all neighbors not lower in the timing hierarchy than the local clock.

RULE 8 From the set of inaccuracies determined by Rule 6 only those for neighboring nodes higher in the hierarchy than the local node are selected. These are combined to determine the inaccuracy for the measured error in the local clock based on information from neighbors higher in the hierarchy than the local node. This information is supplied as INFO 5A to all neighbors not lower in the timing hierarchy than the local node.

RULE 9 From the set of error measurements for the local clock as determined by Rule 5 and the associated inaccuracies determined from Rule 6, all those for neighbors not lower in the hierarchy than the local node are selected. These error measurements are combined to determine a Class 2 measurement of the error in the local clock, i.e., one based on all those neighbors not lower in the timing hierarchy than the local node. This is

supplied as INFO 4B, the measured error in the local clock, to all neighbors lower in the timing hierarchy than the local clock.

RULE 10 From the set of inaccuracies determined by Rule 6 all those for neighbors not lower in the timing hierarchy than the local node are selected. These inaccuracies are combined to determine the inaccuracy for the measured error in the local clock based on information from all those neighbors not lower in the timing hierarchy than the local node. This inaccuracy information is provided as INFO 5B to all neighbors lower in the timing hierarchy than the local node.

The combining of information over several different paths, in addition to providing more accurate time measurements at many nodes remote from the master, reducing the need for massive reorganization of the network following some failures as required when using only the best path, also provides the possibility for quantitative evaluation of the fitness of the timing subsystem. Since each time error measurement (the term measurement as used here includes the mathematical combination of measurement information from different sources) has a corresponding estimated inaccuracy, these time error measurements and their corresponding inaccuracy estimates can be used to provide a quantitative alarm system. This leads to Rule 11.

RULE 11 Rule 5 provides a set of error measurements for the local clock based on information from each neighboring node. Rule 6 provides a corresponding set of inaccuracies for these error measurements. Rule 9 provides a combined measurement for the error in the local clock. Rule 10 provides a corresponding inaccuracy for the combined measurement. The combined measurement as determined by Rule 9 is subtracted from each member of the set of error measurements determined by Rule 5. The resulting set gives the difference between each individual measurement and the combined measurement. The inaccuracy (stated as a variance) determined by Rule 10 is added to each member of the set of inaccuracies obtained by Rule 6 (also stated as a variance) and the square root of each member of this set is taken to obtain a set of estimates of the standard deviations of the clock error

measurements based on information from each neighbor relative to the combined clock error measurement. Each member of the set of differences between individual measurements and the combined measurement is divided by the estimate of the corresponding standard deviation to obtain a normalized set of ratios. These ratios provide levels of alarms as the value climbs from 2 to 5. A level 5 alarm has a chance of one in a million of occurring in a normally operating system.

The alarm system is described in the flow diagram of Figure 6.

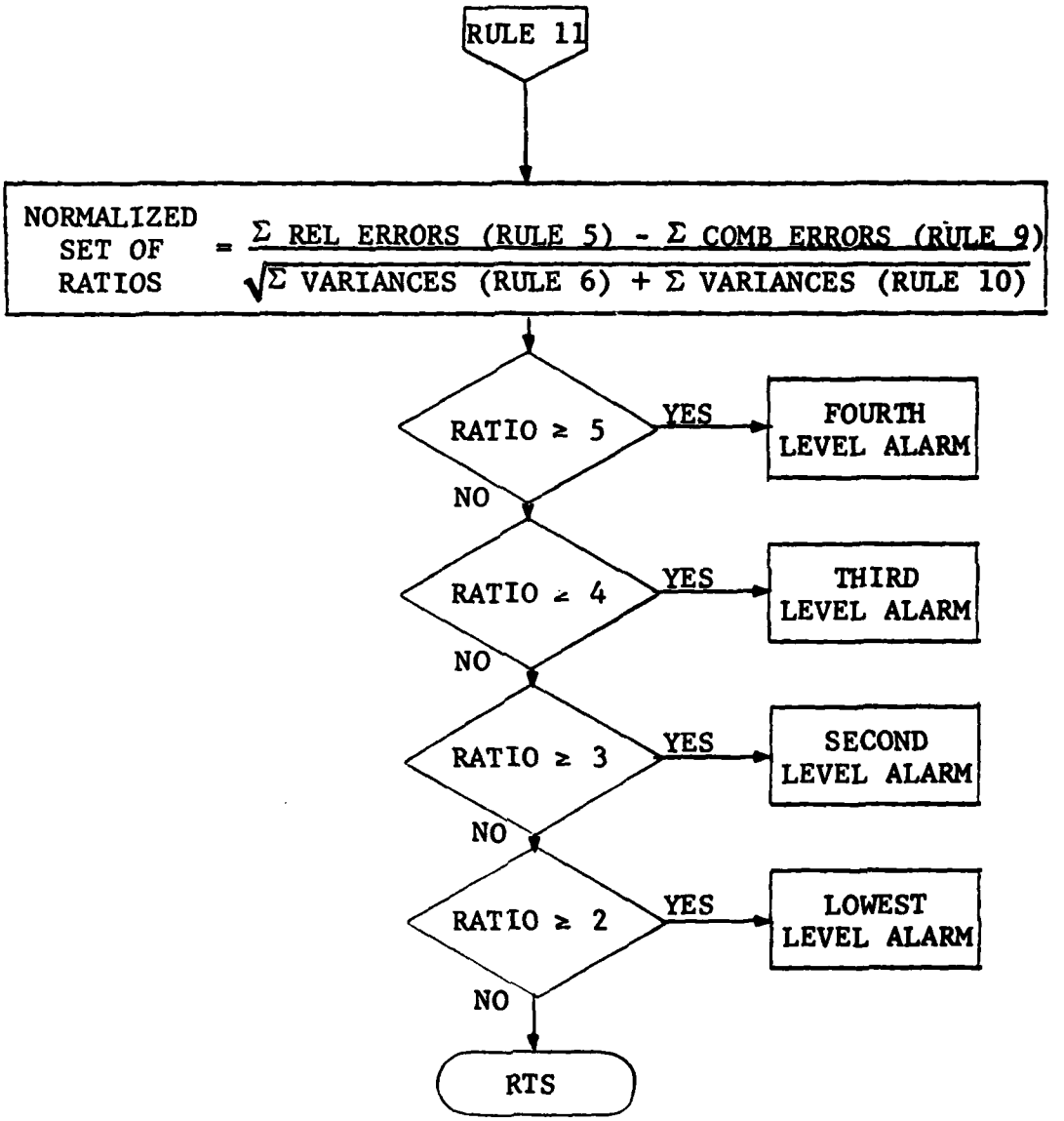


Figure 6 TRDNEW Quantitative Alarm System

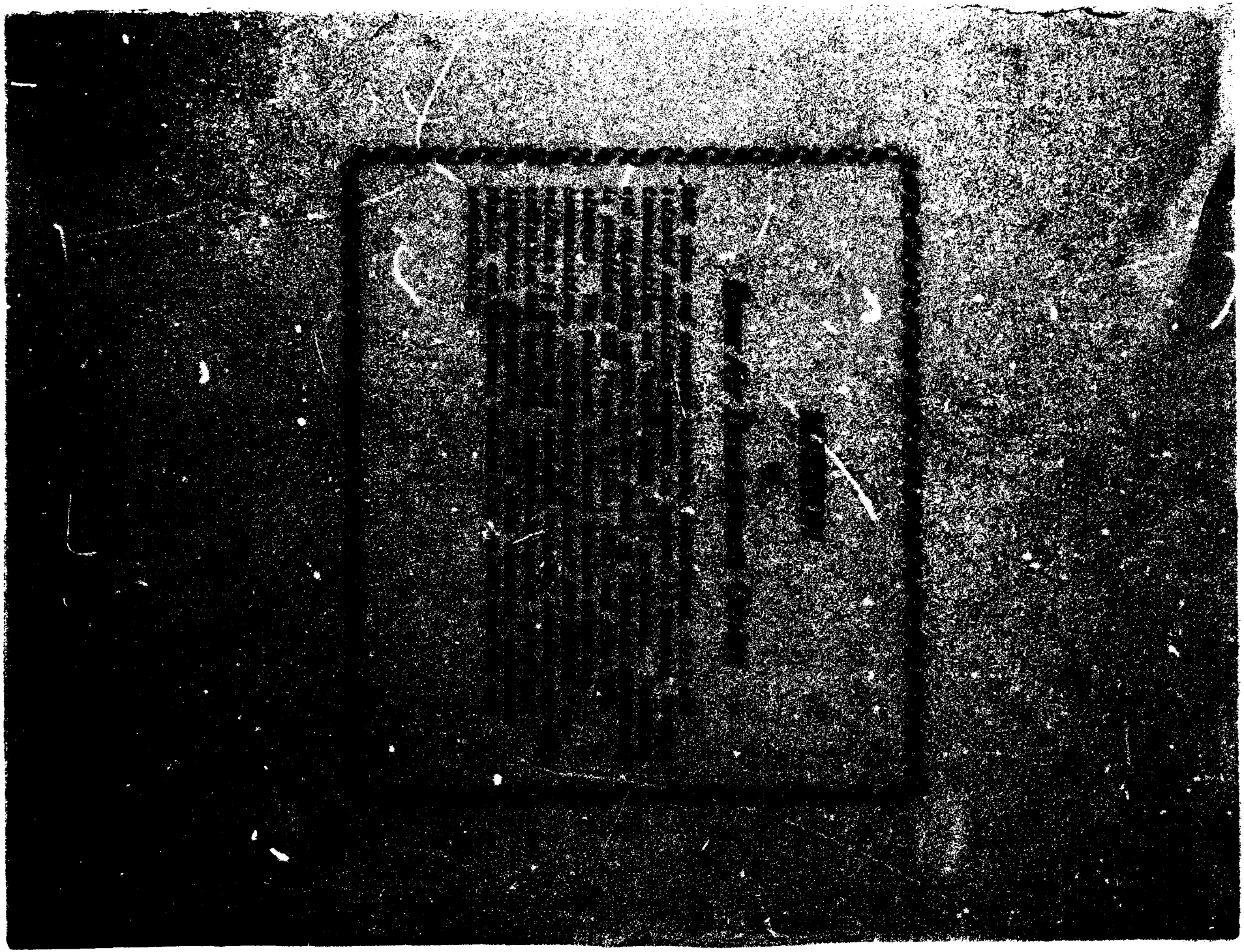
REFERENCES

[1] DCASEFTC 39-73 "Time Reference Concept for Timing and Synchronization of the Digital DCS," H. A. Stover, July 1973.

[2] Clarkson College of Technology, "A Study of Microprocessor Implementation of Time Reference Distribution," RADC Phase Report TR 77-20, June 1977.

[3] H. A. Stover, "Communications Network Timing," DCEC Tech. Report TR 43-75, September 1975.

[4] H. A. Stover, "Improved Time Reference Distribution for a Synchronous Digital Communications Network," Proceedings PTTI Meeting, November 1976, pp. 147 - 166.




DATE
ILME
8