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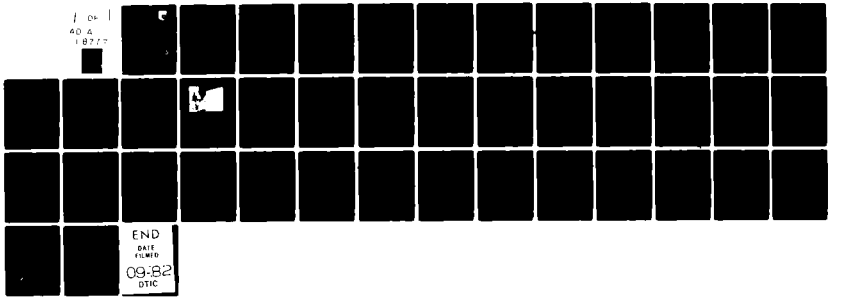

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GaAs SURFACE PASSIVATION FOR DEVICE APPLICATIONS

C. L. Anderson
M. D. Clark

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, California 90265

JULY 1982

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Dietrich W. Langer

DIETRICH W. LANGER, Project Engineer
Electronic Research Branch
Avionics Laboratory

FOR THE COMMANDER

Philip E. Stover

PHILIP E. STOVER, Chief
Electronic Research Branch
Avionics Laboratory

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This report describes the progress in the fifth six-mon period of a program to develop deposited dielectrics for GaAs device applications. Three applications of the dielectrics have been investigated on this program: (1) isolation of control electrodes, (2) passivation of the GaAs surface, and (3) encapsulation of completed circuits. The dielectrics studied have included silicon oxynitride and mixtures of →

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silicon nitride with germanium nitride.

During this reporting period the activities performed emphasized a parametric study of plasma-enhanced deposition (PED) of silicon nitride. The overall process involves cleaning of the sample, anodic oxidation of the GaAs surface, stripping of the anodic oxide, an optional final wet-chemical surface preparation step, pre-deposition plasma-enhanced treatment of the walls of the deposition system or "preburn" (which may involve a concurrent sample surface treatment), optional plasma etching of the sample surface, and deposition of the dielectric. We have analyzed the effects of variations in (i) oxide stripping and final wet-chemical preparation procedures, (ii) preburn, (iii) plasma etches, and (iv) deposition procedures on the electrical properties of the GaAs/silicon nitride interface. None of the procedures investigated yielded interfaces useful for fabrication of practical GaAs insulated-gate transistors or integrated circuits.

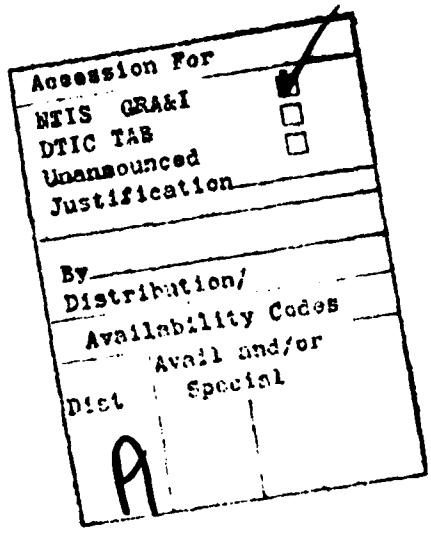
In addition, we have performed preliminary studies to determine appropriate parameters for the plasma-enhanced deposition of germanium nitride and mixtures of silicon nitride with germanium nitride.

PREFACE

The work reported here is supported by the Avionics Laboratory and the Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, under contract F33615-78-C-1444, Project Number 2305, Task Number 2305R1. The monitoring engineer is Capt. R. L. Johnson (AFWAL/AADR). The program objective is to investigate the passivation of gallium arsenide and the application of dielectric thin-film overlays in metal-insulator-semiconductor field-effect transistors.

This work is being performed by Hughes Research Laboratories, Malibu, California 90265. Contributions to this work have been made by C. L. Anderson, M.D. Clark, A. J. Mohr, and R. A. Jullens.

This is the fifth interim report. The first, second, and third were published as AFAL-TR-79-1057, AFAL-TR-79-1234 and AFWAL-TR-80-1149, respectively, with the same title. This report covers the period 15 June 1980 through 14 December 1980. The submittal date of this report was September 1981.



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INTRODUCTION AND SUMMARY

The goal of this program is to develop dielectrics that will serve the following three purposes in gallium arsenide device technology:

- Passivation -- reduction of the number of electrically active center ("surface states") at the semiconductor surface so that the surface potential can be modulated by control electrodes ("gates") overlying the dielectric.
- Isolation -- insulation of control electrodes from each other and from the substrate.
- Encapsulation -- overcoating of operational circuits to reduce their sensitivity to environmental influences.

To serve these three purposes, Hughes Aircraft Company is developing a variety of deposited dielectrics. Techniques for depositing these dielectric materials are being developed under Hughes internal funding. Evaluation and optimization of these materials for GaAs device applications are being performed under the subject contract.

The following materials were originally proposed for development under this program:

- $Ga_xAl_yO_z$ (gallium-aluminum oxide), referred to as (Ga, Al)O
- $Ga_xSi_yO_z$ (gallium-silicon oxide), or (Ga, Si)O
- $Al_xSi_yO_z$ (aluminum-silicon oxide), or (Al, Si)O
- SiO_xN_y (silicon oxynitride)
- (Si,Ge)N (silicon-germanium nitride).

Three basic techniques for depositing these materials were originally proposed:

- Pyrolytic chemical vapor deposition (CVD)
- Plasma-enhanced deposition (PED)
- Photochemical deposition (PCD)

We reported in AFAL-TR-79-1057 the successful use of our proprietary plasma-deposited glass as an isolation dielectric in GaAs MESFET ICs. In AFAL-TR-79-1234, we reported the application of this dielectric as an encapsulant for discrete GaAs MESFETs with the loss of only 0.5 dB gain at 9.7 GHz. Because of the demonstrated utility of this dielectric for isolation and encapsulation applications, this program was redirected to investigate the application of deposited dielectrics solely for passivation applications.

During the course of this program, a considerable body of experimental evidence was accumulated by ourselves and others indicating that oxidation of the GaAs surface leads to the development of high interface state densities near the middle of the GaAs bandgap and hence to interfacial electrical properties which are undesirable for insulated gate devices. Accordingly, all work on oxides as passivating layers for GaAs under this program was terminated during the previous semi-annual reporting period.

During the present reporting period, the work performed on this program consisted primarily of a parametric study of procedures for preparing GaAs/silicon nitride structures by plasma-enhanced deposition. The overall process involves a significant number of steps including (a) cleaning of the wafer, (b) anodic oxidation of the wafer, (c) stripping of the oxide, (d) a final wet-chemical surface treatment (optional), (e) pre-deposition plasma treatment of the walls of the deposition system or "preburn" (which may include exposure of the wafer surface to the plasma), (f) plasma etching of the wafer surface (optional), and (g) the actual dielectric deposition. A standard procedure for steps (a) through (c) leading to reproducible surface properties of the wafer as determined by ellipsometry was developed during the third semester of this program and was reported in the third interim report (AFWAL-TR-80-1149). A large-scale high-vacuum-compatible plasma-enhanced deposition system developed under Hughes internal funding was completed during the same period and applied to this program. A baseline process for steps (e) and (g) was developed under this program and was reported in the third interim report. A description of the baseline process is presented as Section 2 of the present report.

During this reporting period the effects of variations in steps (c), (d), (e), (f), and (g) on the electrical properties of the GaAs/Si_3N_4 interface were investigated. Fifty-five deposition runs were performed. The results of these studies are reported in Section 3 of this report.

Preliminary studies of the conditions appropriate for deposition of Ge_3N_4 and Si_3N_4/Ge_3N_4 mixtures were also performed during this reporting period. The results of these studies are presented in Section 4.

SECTION 2

BASELINE PLASMA-ENHANCED DEPOSITION PROCESS FOR SILICON NITRIDE

Much of the effort expended during the first two years of this program was directed towards development of a reliable process for preparing high-quality oxygen-free silicon nitride films by plasma-enhanced deposition (PED) and towards identification of wet-chemical surface preparation procedures which result in consistent surface properties of the GaAs wafers introduced into the PED system. Since most of the remainder of this report deals with the effect of variations of the sample preparation and deposition process on the electrical quality of the GaAs/Si_3N_4 interface, this section is provided to fully document the baseline process for reference purposes and to expl in the rationale for this process. For those who wish to omit the discussi or the rationale for selection of the particular baseline process, a concis description of the process is provided in Section 2C.

A. CLEANING AND ETCHING PROCEDURES

The apllication of deposited dielectric films to the passivation of GaAs for device applications relies on the premise that the surface "oxide" film of unknown composition that exists on the sample surface immediately prior to the deposition of the dielectric is sufficiently thin and tenuous that the surface properties can be controlled by the deposited dielectric. Accordingly, the development of surface cleaning and etching procedures which result in a thin "oxide" layer of reproducible properties was addressed during the third semester of this program and reported in AFWAL-TR-80-1149.

Prior to the final surface etching step, all samples were cleaned by a standard cleaning procedure designed to remove organic contaminants and any excess Ga on the wafer surface resulting from epitaxial growth. This cleaning procedure, which has been found to be successful for a wide variety of applications is described in Table 1.

To investigate the effectiveness of etching for minimizing residual oxide, we employed our Gaertner L116 ellipsometer to measure the apparent complex index of refraction, $N_s^* = N_s + iK_s$, of the substrate immediately after etching.

Table 1. Cleaning Procedure for GaAs Wafers

Distinguish four categories and modify general cleaning procedure per instructions below.

A. New polished wafers

B. Epitaxial wafers

C. Ion implanted wafer not yet annealed

D. Photoresist processed wafers

General Procedure:

1. Tricholoroethylene (TCE) to boiling (boil 3 min)
2. TCE to boiling (boil 3 min)
3. Cold methanol/acetone dip (80% acetone/20% methanol)
4. DI H_2O rinse (1 min)
5. 50% HCl/DI H_2O (3 min)
6. DI H_2O rinse (2 min)
7. Isopropyl to boiling (boil 2 min)
8. Blow or spin dry
9. Inspect

Category A: Complete procedure

Category B: Change step 5 only if excess Ga is present. Use hot 50% HCl/DI H_2O, but do not boil.

Category C: Eliminate steps 4 and 5.

Category D: Change step 3 to boiling acetone (3 min).

Note: Use only the following solvents and chemicals: Allied Chemical, Semiconductor Low Mobile Ion Grade Mallinckrodt, Transistor Grade

DI H_2O – 18 MΩ

Or as approved by supervisor.

Neither the thickness nor the index N_f of a very thin film can be precisely determined unless a true N_s^* is accurately known. Unfortunately, N_s^* is not known with sufficient accuracy to permit such a detailed analysis. However, the effect of a thin, transparent film on the measured N_s^* is to decrease N_x and increase $|K_s|$ over that of an ideal substrate ($K_s < 0$ for an absorbing substrate). This will be the case for $1 < N_f < N_s$, assuming $|K_s| << N_s$. From our measurements, together with published absorption data, our best estimate of the ideal N_s^* of GaAs at a 632.8 nm wavelength is 3.89 - 0.19i. For an oxide film, we expect $N_f < 3.89$ so that the effectiveness of an etch can be judged by the degree to which it minimizes $|K_s|$ and maximizes N_s. The value of K_s is the most sensitive indicator of a surface film.

The initial etches evaluated were NH_4OH:30% H_2O_2:H_2O (5:2:240 by volume) and 1 M NaOH:0.76M H_2O_2 (1:1 by volume). Ellipsometric analysis indicated that the NH_4OH:H_2O_2 etch leaves the least oxide, while the NaOH:H_2O_2 etch is slightly more uniform.

During our cleaning studies, we encountered several wafers of GaAs that were heavily contaminated with particulate matter and "scum" that had apparently resulted from the use of improper packing material by the suppliers. The solvent/HCl cleaning procedure of Table 1 was not completely effective for removing these heavy deposits since such deposits are not normally encountered on polished GaAs wafers. We found that most of the remaining contamination could be effectively removed by growing about 100 nm of native anodic oxide and then etching away the oxide with 1M NH_4OH. The oxide is grown at room temperature in an electrolyte of composition 17 g ammonium pentaborate per 100 ml of ethylene glycol. A proprietary method is used to electrically contact the backside of the wafer so that the entire front side can be anodized. To ensure uniformity, the wafer is illuminated during anodization. The cathode of the anodization cell is Pt foil.

Several etchants were evaluated on wafers that had received this additional anodization/stripping step after the Table 1 cleaning procedure. Effectiveness of cleaning was judged by ellipsometry as described above.

The following etches were evaluated:

(1) NH_4OH:30% H_2O_2:H_2O (5:2:240)

(2) 1 M NaOH:0.76 M H_2O_2 (1:1)

(3) HCl:H_2O:30% H_2O_2 (1:1 "a few drops")

(4) Br_2:CH_3OH (1% Br_2 by volume)

(5) HF:H_2O (10% HF by volume)

(6) HCl:H_2O (50% HCl by volume)

Etches (5) and (6) attack native oxide but do not etch GaAs at room temperature. These etches generally give comparable results, although Br_2:CH_3OH is somewhat less effective than the others. However, when applied either to samples that have or have not been cleaned by anodic oxide growth and stripping, none of the etches give a surface significantly superior to that obtained by anodic cleaning only. Furthermore, etches (1) through (4), which attack GaAs, cause some degradation of surface morphology because of non-uniform etching, whereas anodic cleaning essentially replicates the original polished surface. Consequently, wet chemical cleaning by the procedures of Table 1 follwed by anodic oxide growth and stripping without subsequent GaAs etching was selected as the baseline wafer preparation process.

B. DESCRIPTION OF THE HUGHES RESEARCH LABORATORIES PLASMA REACTOR

The quality of the PED films prepared for this contract improved significantly when construction of the new PED system shown in Figure 1 was completed. This system was built using Hughes internal funding. A photograph of the actual system, without the screen enclosure used to prevent interference of the rf with the control electronics, is provided in Figure 2. In this system, the reducing gases (silane, germane, etc.) are introduced through a side port, rather than through a tube passing down the axis on the rf coil. This arrangement reduces that amount of surface area in the most intensely excited region of the plasma and precludes the possibility of a plasma being generated within the delivery tube for the reducing gases.

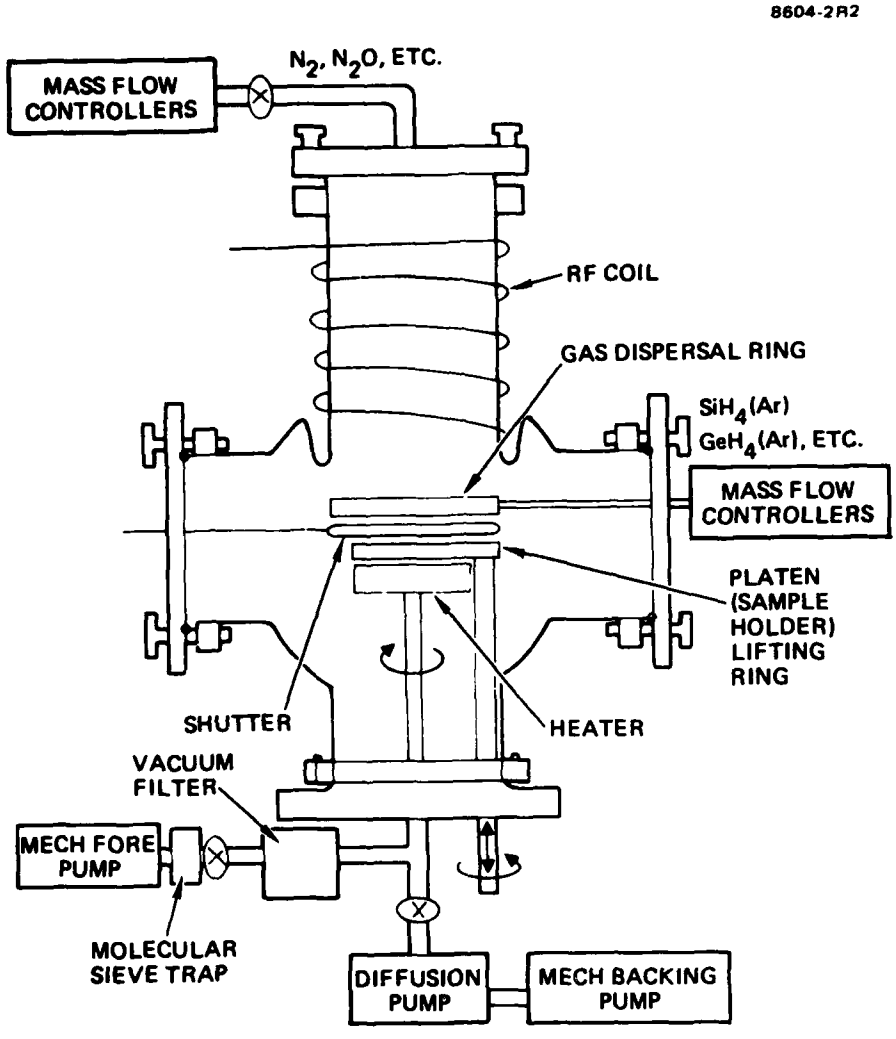

Figure 1. Schematic of the Hughes Research Laboratories deposition (PED) system.

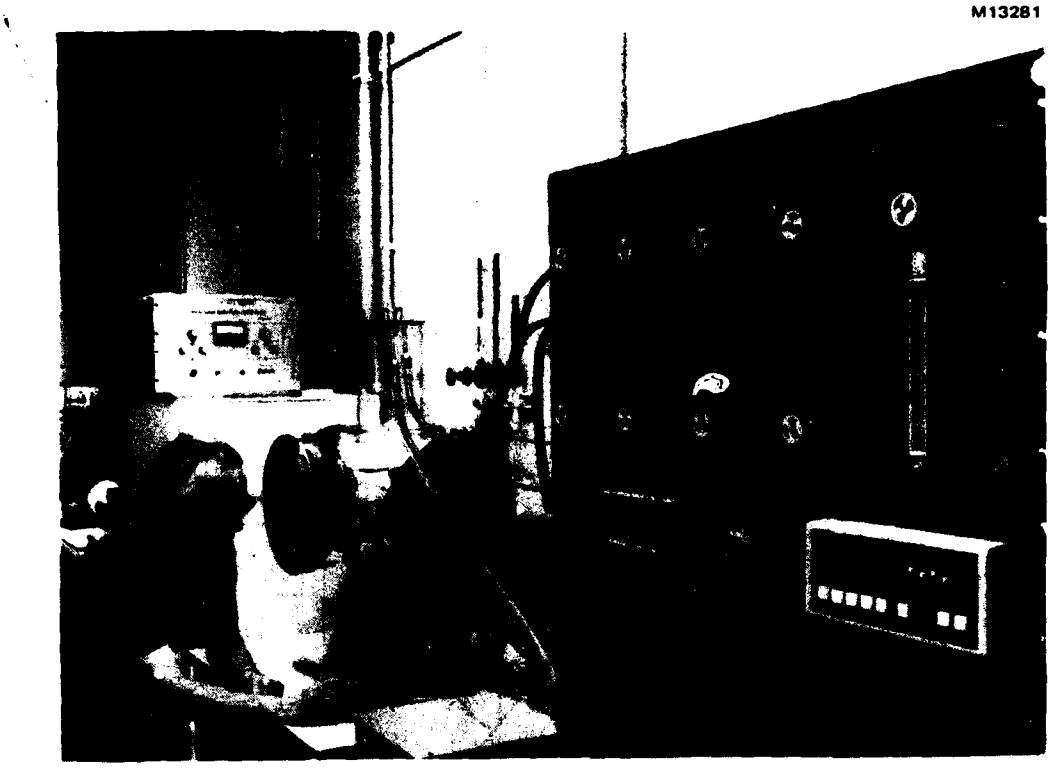

Figure 2. Large-Scale High-Vacuum-Compatible Plasma-Enhanced-Deposition System.

The dispersal ring for the reducing gases is attached to a bellows assembly and is capable of oscillating in both horizontal axes over the heater assembly. The heater itself is capable of rotation. The use of these mechanical motions results in very uniform deposition over large areas (typically ±2.5% over a 2-in. diameter wafer). Samples introduced into the system are placed on a 16 cm diameter "platen" or sample holder which is capable of accepting four 5-cm-diameter circular wafers. The platen itself consists of a heavy Al annular ring over which a sheet of heavy Al foil is stretched and to which the Al foil is clamped. During those stages of the deposition process which involve exciting the plasma the platen rests on an Al sample heater. Because the sample heater tends to deform slightly at elevated temperatures, the use of a stretched Al foil membrane in the platen allows the platen to conform to the heater surface and results in superior themal contact compared to that which would be achieved using a rigid platen.

The platen (sample holder) can be lifted off the heater using a lifting ring controlled by a push-pull/rotary feedthrough and removed from the system through the access door in the front of the chamber. During pumpdown, the platen can be positioned away from the heater to maintain a low sample temperature. Once high-vacuum conditions are achieved, the samples can be rapidly heated to deposition temperature by placing the sample holder plate onto the heater assembly. This provision reduces the possibility of baking contaminants onto the sample surface prior to deposition.

A mechanical shutter is provided to permit covering the sample during a "preburn" procedure used to outgas the chamber before deposition. The central chamber itself is a large sphere to reduce outgassing of the walls resulting from the proximity to the heater assembly.

During a typical deposition cycle, the system is evacuated to high vacuum conditions ($< 5 \times 10^{-5}$ mm Hg, or 7×10^{-3}/Pa) before reactive gases are introduced. The diffusion pump is then valved off and the actual depositions performed under evacuation by a large-capacity rotary pump protected by a vacuum particle filter. All gas flow rates are controlled by mass flow controllers. Deposition pressure is monitored by two capacitance manometer absolute pressure gauges. Because the accuracy of these gauges degrades after numerous

depositions, a reference gauge which is valved off during deposition cycles has been provided. It is used to calibrate the "working" gauge at periodic intervals.

C. DESCRIPTION OF BASELINE PROCESS

1. Stage 1: Sample Cleaning

The GaAs wafer is wet-chemically cleaned using the procedures of Table 1.

2. Stage 2: Anodic Oxidation

The wafer is oxidized at room temperature in an electrolyte consisting of 17 g ammonium pentaborate dissolved in 100 ml of ethylene glycol. A proprietary method is used to contact the back side of the wafer electrically over a large area so that the entire front side can be anodized. To ensure uniformity the wafer is illuminated during anodization. The cathode of the anodization call is Pt foil. Approximately 100 nm of native anodic oxide is grown using a current density of roughly ^{1}mA cm^{-2} and a final voltage of 50 V. Following anodization, the wafer surface is rinsed with 18 MΩ-cm deionized water and blown dry in filtered dry nitrogen. The oxidized surface of the wafer is then coated with a thick layer of photoresist which is allowed to air dry at room temperature. Typically the wafer is then diced by scribing the back side and cleaving.

3. Stage 3: Oxide Stripping

Prior to deposition, the photoresist is stripped from the oxidized surface of the wafer with acetone. The anodic oxide is removed by a 2 min etch in 1 M NH_4OH. The sample is then rinsed in 18 MΩ- cm deionized water and blown dry in filtered dry nitrogen.

4. Stage 4: Final Wet-Chemical Treatment of Wafer Surface (optional)

This step is not performed in the baseline process.

5. Stage 5: Sample Loading

The sample is immediately loaded into the deposition system by placing it on the platen (sample holder) which has been pre-heated to 200°C. (The temperature of the sample heater has been kept constant during each run performed to date. This temperature has, however, been varied from run to run.) One variation from the baseline process which has been explored during this reporting period is loading the sample onto the platen while the platen is detached from the sample heater and is at room temperature. This condition is described in the tables in Section 3 as "cold platen".

Following sample loading, the system is roughed down using the large mechanical forepump, then the system is pumped down to high vacuum ($< 5 \times 10^{-5}$ mn Hg or 7×10^{-3}Pa) using the diffusion pump and backing pump. In the "cold platen" cases the platen is placed on the sample heater after high vacuum conditions have been achieved. The high vacuum valve is then closed.

6. Stage 6: Nitrogen Plasma Preburn

The system is outgassed by performing a nitrogen plasma preburn. Nitrogen is admitted into the system through the mass flow control system. Simultaneously, the valve on the large forepump is opened. The nitrogen flow rate is allowed to stabilize, then the chamber pressure is regulated using the forepump valve as a throttle valve. The mechanical shutter over the sample is closed. The rf supply is then turned on, exciting the plasma.

Baseline preburn conditions are as follows:

N_2flow rate	16 sccm
Chamber pressure	100 mTorr (13 Pa)
RF power	100 W
Hot plate temperature	200°C
Shutter position	Closed
Duration	10 min

Following the preburn the plasma is entinguished by turning off the rf supply. The nitrogen flow is then discontinued.

7. Stage 7: Plasma Etch (Optional)

This step is not performed in the baseline process. If employed, a plasma etch is performed in the same manner as the preburn except that an etching gas is admitted and the shutter is normally open to expose the sample to the etching plasma.

8. Stage 8: Deposition

Following the preburn (and plasma etch process if employed) the system is again pumped down to high vacuum by shutting the forepump valve and opening the high vacuum valve. When a pressure below 5×10^{-5} mm Hg (7×10^{-3} Pa) has been achieved, the high vacuum valve is closed again. Nitrogen and a gas mixture of 1.5% SiH_4 in Ar are admitted into the chamber through the mass flow control system. Simultaneously the forepump valve is opened. Once the nitrogen and dilute silane flows have stabilized, the pressure is regulated using the forepump valve. The rf power supply is then turned on to ignite the plasma.

Baseline deposition conditions are as follows:

N_2 flow rate	16 sccm
Flow rate of 1.5% SiH_4 in Ar	90 sccm
Chamber pressure	250 mTorr (33 Pa)
RF power	30 W
Hot plate temperature	200°C
Hot plate rotation	on, 6 rpm
Shutter position	open
Silane dispersal ring motion	on (passes over the hot plate 6 times per minute)
Duration	12 min

Following the deposition, the rf power supply is turned off. The nitrogen and dilute silane flows are then terminated and the system is allowed to pump down to forepump vacuum (a few micrometers of Hg). This step allows the dilute silane remaining in the system to be removed. The system is then vented to permit sample removal. These parameters result in a deposition rate of about 7.5 nm/min and consistently give films with refractive indices between 1.90 and 2.05 at a wavelength of 632.8 nm.

Using the above parameters, films were deposited on pyrolytic carbon and examined by Rutherford backscattering (RBS). The RBS data indicated a Si/N ratio appropriate for Si_3N_4 and an upper limit on the O/N ratio of about 0.08.

Capacitance-voltage (C-V) and conductance voltage (G-V) data for a typical n-GaAs/baseline PED silicon nitride/Al capacitor are shown in Figures 3(a) and 3(b), respectively. The vertical axis of the G-V figure is the capacitance equivalent of the conductance (i.e., G/ω where ω is the angular frequency and $\omega = 2\pi f$ where f is the conventional frequency). These data exhibit the typical problems associated with GaAs/dielectric interfaces. In particular, the C-V data exhibit strong frequency dependence of the accumulation capacitance.

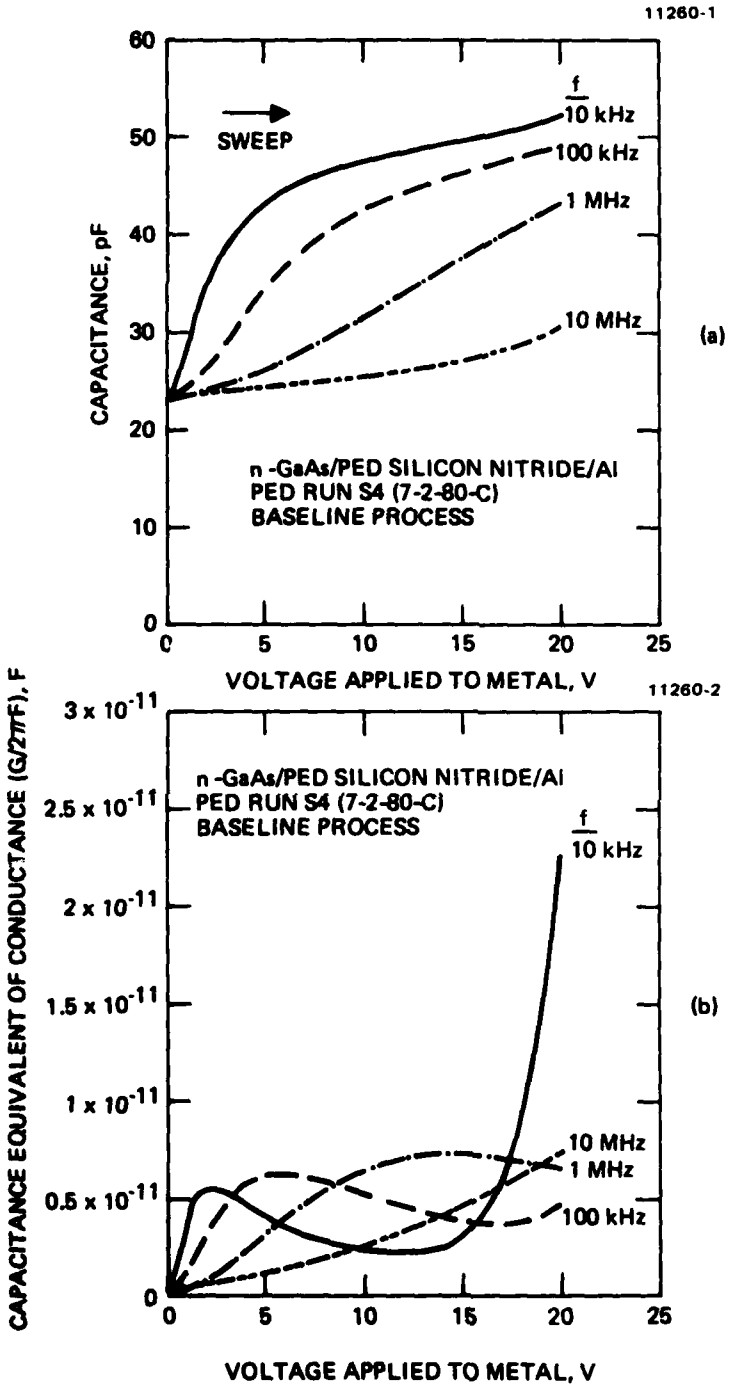

Figure 3. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor employing a dielectric layer prepared by the baseline process.
(a) Capacitance voltage characteristics.
(b) Conductance voltage characteristics.

SECTION 3

PARAMETRIC STUDY OF THE EFFECTS OF PED PROCESS VARIATIONS ON THE ELECTRICAL PROPERTIES OF THE GaAs/PED SILICON NITRIDE INTERFACE

During this reporting period, 51 PED silicon nitride deposition runs were performed in an effort to identify process parameters which exhibit a significant influence on the electrical properties of the GaAs/PED silicon nitride interface. These runs can be conveniently grouped into four categories, based on the type of variation in the process involved in the respective runs. The process variations employed in each group are summarized as follows: (a) small variations in the standard procedure (loading procedure, temperature, silane flow rate); (b) preburn procedure; (c) final wet chemical treatment of the sample surface; and (d) plasma etching of the sample after preburn. The four groups are discussed individually in the following four subsections.

A. RUNS INVOLVING SMALL VARIATIONS FROM STANDARD PROCEDURE

Ten runs were performed in this group. The variations from the baseline procedure employed in the individual runs are summarized in Table 2. Standard runs S4 and S8 yielded films with refractive indicies of 2.12 and 2.06, respectively, with associated film thicknesses of 74 and 83 nm. The runs performed with 100 SCCM of the SiH_4/Ar mixture exhibited films with refractive indicies of 2.17 and 2.02, with associated thicknesses of 85 and 95 nm. Run S7, performed with 80 SCCM SiH_4/Ar produced a film with refractive index of 1.93 and thickness of 91 nm. Thus the optical properties and thickness of the deposited films are not strongly sensitive to the silane content of the plasma. None of the remaining runs of this group yielded films with refractive index or thickness outside the range encompassed by the six runs just described. Thus the film properties are (fortunately) relatively insensitive to small variations in the baseline process.

Of the nonstandard runs in this group, the most promising from the point of view of interfacial peroperties were those performed at 300°C. The C-V and G-V characteristics from an n-GaAs/300°C PED Si_3N_4/Al capacitor from run S10

Table 2. Deposition Conditions for Silicon Nitride Runs Exploring Small Variations from Standard Procedure

Run	Deviation from Standard Procedure
S1	cold platen
S2	100°C
S3	80 sccm SiH_4/Ar
S4	(Standard run)
S5	100 sccm SiH_4/Ar
S6	300°C
S7	80 sccm SiH_4/Ar
S8	(Standard run)
S9	100 sccm SiH_4/Ar
S10	300°C

are shown in Figures 4(a) and 4(b), respectively. These data are qualitatively very similar to those of Figures 3(a) and 3(b) in that both samples exhibit substantial frequency dispersion of the accumulation capacitance and comparable conductance behavior (both in magnitude and variation with frequency). Thus, performing the preburn and deposition at 300°C yields comparable results to the standard 200°C process.

B. RUNS INVOLVING VARIATIONS IN PREBURN PROCEDURE

Twenty-five runs were performed to determine the effect of variations in the preburn procedure on interfacial electrical properties. Prior to initiating the first runs in this series, a revision was made in the baseline process: the second pumpdown of the system to high-vacuum conditions following the preburn was eliminated. The justification for this revision was that it reduced the total exposure time of the system to the ambient following the preburn, thereby reducing the extent of uncontrolled oxidation of the sample surface. There have been no observations that this revision of the standard procedure

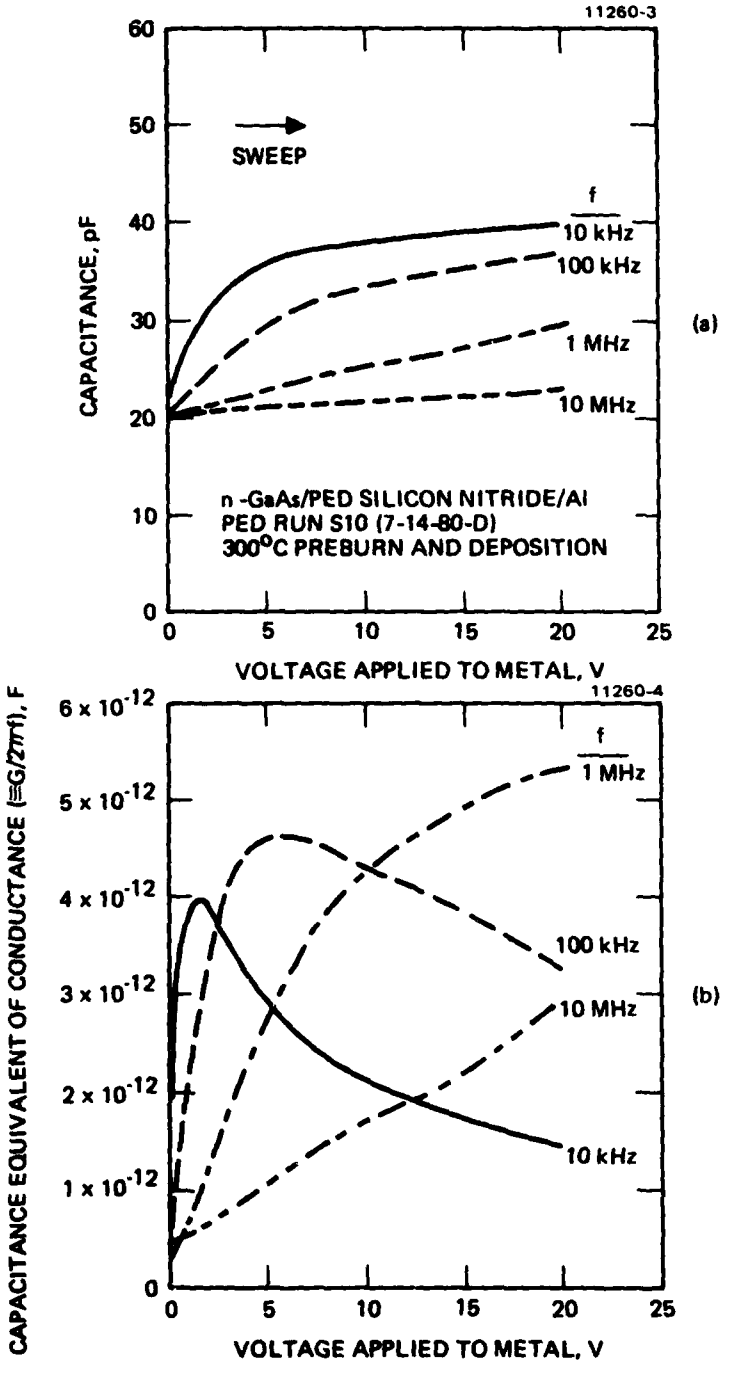

Figure 4. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor employing a dielectric deposited at 300°C.
(a) Capacitance voltage characteristics
(b) Conductance voltage characteristics

is either deleterious or beneficial; it does, however, simplify the deposition sequence, which is clearly desirable in its own right.

The deviations of each run in this group from the revised standard procedure are listed in Table 3. Most of the runs employed N_2 preburns. This group, however, also included preburns involving N_2 + NH_3, NH_3, and CF_4 gases. Neither NH_3 nor CF_4 is believed to etch GaAs in a plasma. Therefore, these runs are treated as involving preburn variations rather than plasma etch stages.

The primary observation to be made concerning runs for this group is that exposure of the sample surface to the preburn can be beneficial to the final electrical properties of the interface.

Figures 5(a) and 5(b) illustrate the electrical characteristics of an MIS capacitor incorporating a film grown on a sample which had been loaded cold, heated to 300°C after pumpdown to high vacuum, and exposed to a 2-min N_2 preburn (run S19). Compared to the data for a 300°C film deposited on a sample which had been covered during the preburn (Figures 4(a) and 4(b)), the data from run S19 exhibit reduced frequency dispersion between 10 kHz and 1 MHz, greater voltage dependence of the 10 MHz capacitance, narrower conductance peaks, and a peak in the 1 MHz conductance curve (not seen in Figure 4(b)). All these features are indicative of a reduction in interface state density.

The effect of the duration of the exposure to the N_2 preburn is small, as can be seen from comparison of Figures 5(a) and 5(b) with Figures 6(a) and 6(b). In the latter case, the sample was exposed to a 10-min N_2 preburn. There is little qualitative difference between these data.

The second observation to be drawn from this group of runs is that preburns in hydrogenated gases can be beneficial. Of the runs involving preburns in gases other than N_2, the most promising was S50, in which the sample was exposed to a 5-min preburn in N_2 + NH_3 after a 5-min N_2 preburn with the shutter closed. Electrical data are similar to those of Figures 5(a), 5(b), 6(a) and 6(b) except that the peak conductance values are substantially lower and the conductance peaks occur at slightly lower voltages. (The capacitance values in Figure 7 are slightly lower than in Figures 5 and 6, but the ratio of conductance to capacitance in Figure 7 is definitely superior to that in

Table 3. Deposition Conditions for Silicon Nitride Runs Exploring Variations in Preburn Procedure

Run	Deviations from Revised Standard Procedure (no second pumpdown)
S11	Shutter open during preburn
S12	Shutter closed during first minute of "deposition", then opened
S13	Room temperature; shutter open during preburn
S14	Room temperature; shutter closed during first minute of "deposition", then opened
S15	300°C; cold platen, shutter open during preburn
S16	300°C; cold platen, shutter open during 20 min preburn
S17	300°C; cold platen, no preburn
S18	300°C; cold platen, shutter open during 30 sec preburn
S19	300°C; cold platen, shutter open during 2 min preburn
S20	300°C; cold platen, shutter open during NH_3 preburn
S21	300°C; cold platen, shutter open during 2 min NH_3 preburn
S22	300°C; cold platen, shutter open during 30 sec NH_3 preburn
S23	300°C; cold platen, 10 min NH_3 preburn
S29	Cold platen, no preburn, shutter closed during first minute of "deposition", then opened
S33	300°C; cold platen, no preburn, shutter closed during first minute of "deposition", then opened
S34	300°C; no preburn
S35	300°C; cold platen, no preburn
S38	CF_4 preburn (CF_4 fed through etching gas line)
S39	Cold platen, shutter open during 30 sec CF_4 preburn
S40	Cold platen, shutter open during CF_4 preburn
S43	Cold platen, shutter open during 20 W preburn
S44	Cold platen, no preburn, 500 m Torr deposition pressure
S49	Mixed preburn - N_2 5 min then NH_3/N_2 5 min - run interrupted by mass flow-control failure
S50	5 min preburn, shutter closed, in 16 SCCM N_2, 200 W, 100 mTorr, followed by 5 min preburn, shutter open, in 16 SCCM N_2 + 16 SCCM NH_3, 200 W, 100 mTorr
S51	5 min preburn, shutter closed, in 16 SCCM N_2, 200 W, 100 mTorr, followed by 5 min preburn, shutter open, in 16 SCCM N_2 + 16 SCCM NH_3, 300 W, 500 mTorr (uninterrupted repeat of S49)

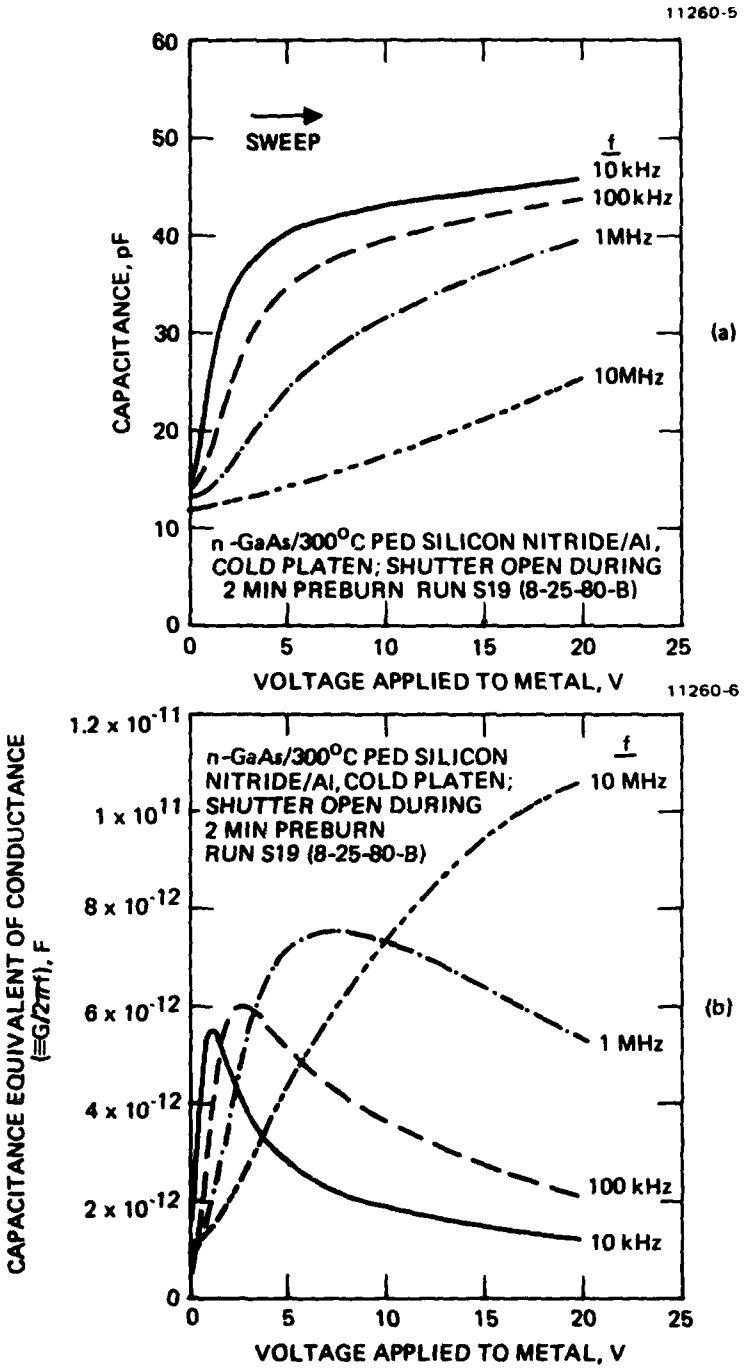

Figure 5. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric deposited at 300°C after the sample had been loaded onto a cold sample holder heated to 300°C after pumpdown and exposed to a 2 min N_2 preburn.
(a) Capacitance voltage characteristics
(b) Conductance voltage characteristics

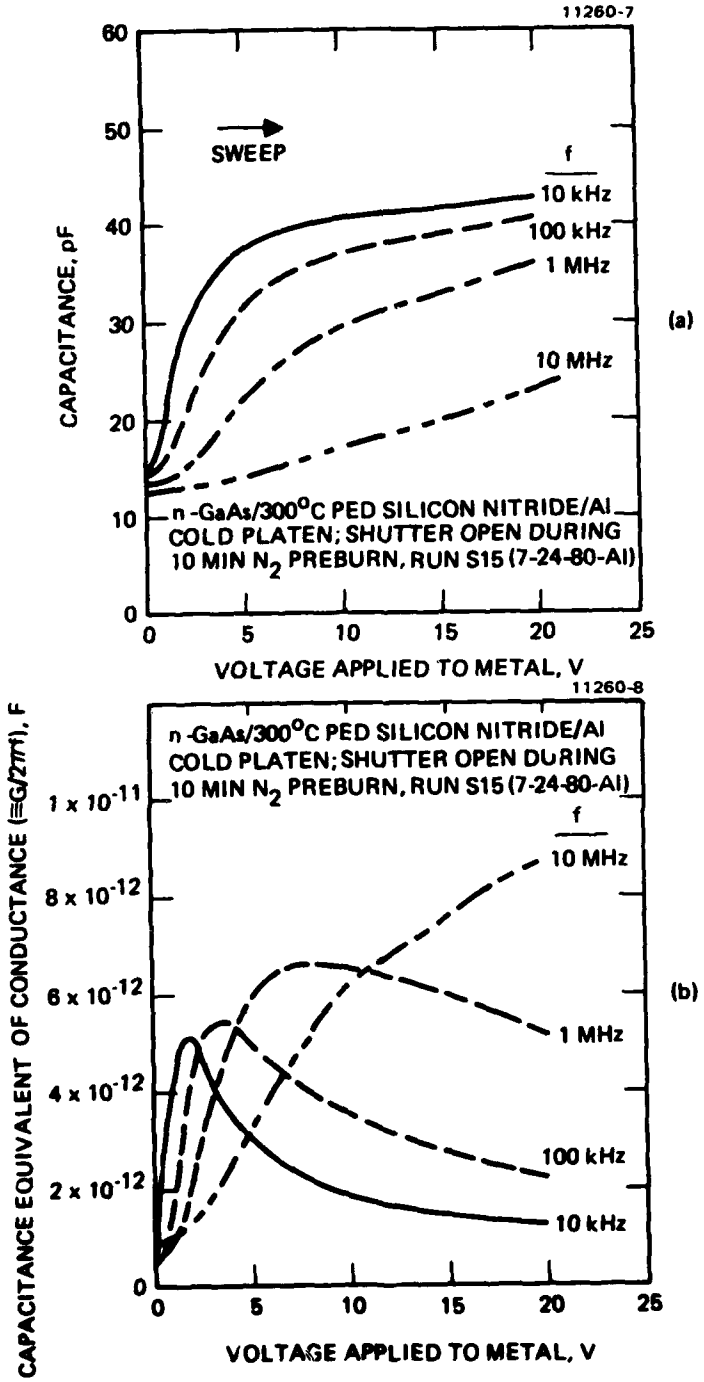

Figure 6. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor employing a dielectric deposited at 300°C after the sample had been loaded onto a cold sample holder, heated to 300°C after pumpdown, and exposed to a 10 min N_2 preburn.

(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

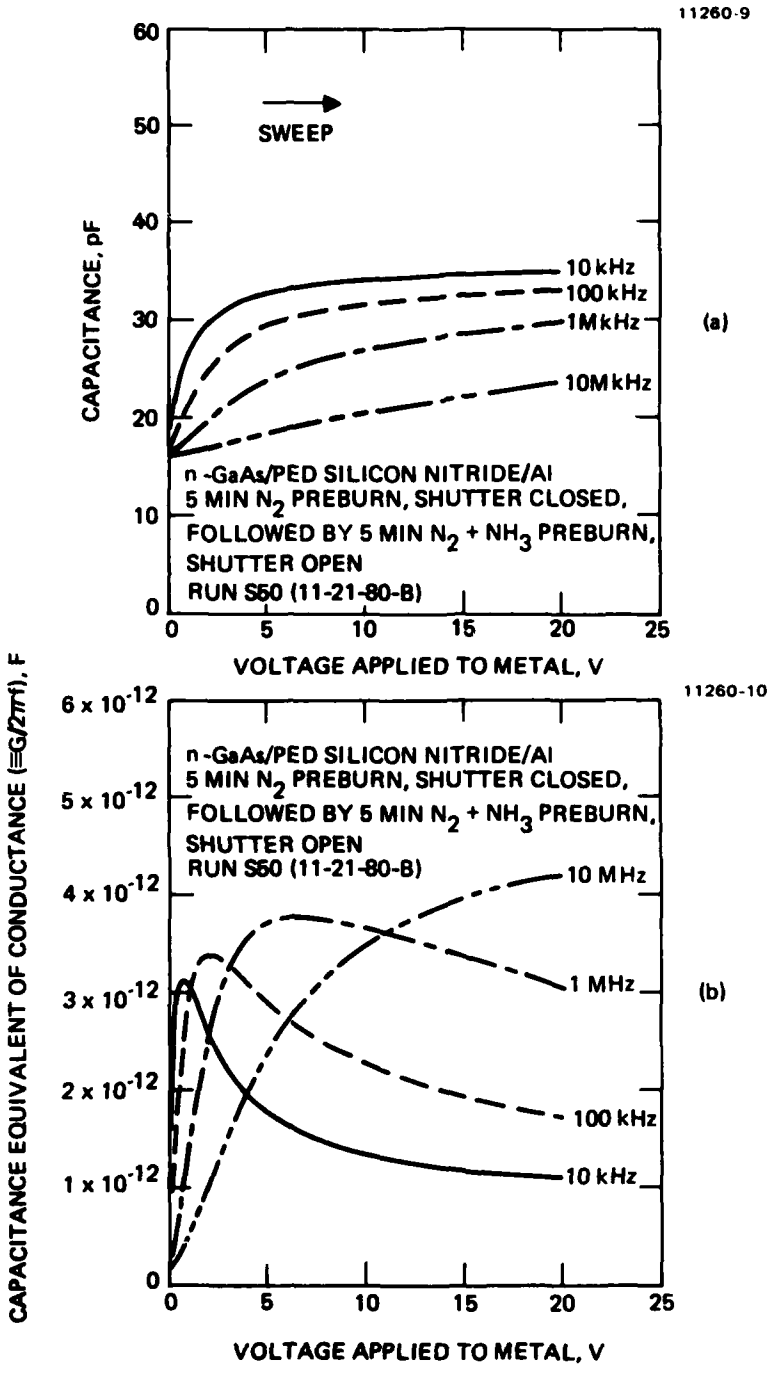

Figure 7. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric deposited after a 5 min N_2 preburn with the shutter closed followed by a 5 min N_2 + NH_3 preburn with the shutter open.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

the former two figures.) Thus the exposure to the mixed N_2 + NH_3 preburn appears to have resulted in improved interfacial properties.

C. RUNS INVOLVING VARIATIONS IN FINAL WET CHEMICAL TREATMENT OF THE SAMPLE SURFACE

Eleven runs were performed involving variations in the final wet chemical treatment of the GaAs surface prior to insertion into the vacuum chamber. The deviations of the deposition parameters for these runs from the revised standard procedure (baseline process without second pumpdown of system to high vacuum following preburn) are summarized in Table 4. For runs S24, S26, S28, S30, S31 and S32, the sample was dipped in methanol plus "a few drops" of HCl after the baseline oxide strip and placed in the deposition system wet. For run S36, the sample was dipped in methanol plus "a few drops" of HF after the baseline oxide strip and placed in the deposition system wet. For run S37, the anodic oxide was removed in $HF:H_2O$ (1:9 by volume); the sample was then rinsed in 18 M Ω-cm deionized water and blown dry with filtered dry nitrogen gas before insertion into the deposition chamber.

Multifrequency C-V and G-V measurements were performed on MIS capacitors prepared from films deposited on n-GaAs samples in each run. None of these process variations resulted in any significant improvement in interface properties over those achieved by the baseline process (Figure 3).

D. RUNS INVOLVING PLASMA ETCHING OF THE SAMPLE AFTER PREBURN

Six deposition runs plus two control runs (in which no deposition was performed) were carried out to analyze the effects of plasma etching of the sample surface with chlorinated species prior to deposition. The deviations of these eight runs from the revised standard procedure (baseline process without pumpdown to high vacuum following preburn) are summarized in Table 5.

The initial experiments were done with pure CCl_4. Rapid etching was observed along with visual evidence of a surface residue. The presence of a dielectric residue was verified by observation of MIS structure capacitances much lower than would be expected for the SiN_x dielectric alone. The MIS

Table 4. Deposition Conditions for Silicon Nitride Runs Exploring Variations in Final Wet Chemical Treatment of Sample Surface

Run	Deviation from Revised Standard Procedure (No Second Pumpdown)
S24	300°C; dip in methanol + HCl after oxide strip, cold platen, no preburn
S25	300°C; 1 M HCl oxide strip, cold platen, no preburn
S26	Dip in methanol + HCl after oxide strip, cold platen, no preburn
S27	1 M HCl oxide strip, cold platen, no preburn
S28	Dip in methanol + HCl after oxide strip, cold platen, no preburn, shutter closed during first minute of "deposition", then opened
S30	300°C; dip in methanol + HCl after oxide strip, cold platen, no preburn, shutter closed during first minute of "deposition", then opened
S31	300°C; dip in methanol + HCl after oxide strip, cold platen, NH_3 preburn
S32	300°C; dip in methanol + HCl after oxide strip, cold platen
S36	300°C; dip in methanol + HF after oxide strip, cold platen, no preburn
S37	300°C; HF oxide strip, cold platen, no preburn
S41	5 min $5NH_4OH:2H_2O_2:24OH_2O$ oxide strip, cold platen, no preburn
S42	5 min $5NH_4OH:2H_2O_2:24OH_2O$ oxide strip followed by methanol dip, cold platen, no preburn

Table 5. Deposition Conditions for Silicon Nitride Runs Exploring Plasma Etching of Wafer Surface After Preburn

Run	Deviations from Revised Standard Procedure (No Second Pumpdown)
S45	CCl_4 plasma etch, shutter open, 30 W, 50 mTorr, 1 min
S46	CCl_4 plasma etch, shutter open, 100 W, 100 mTorr, 1 min
S47	CCl_4 plasma etch, shutter closed, 30 W, 50 mTorr, 30 sec
S48	CCl_4 + N_2 plasma etch, CCl_4 pressure set to 50 mTorr, then 16 sccm N_2 added, shutter open, 30 W, 30 sec
S52	Plasma etch in 5 sccm CCl_2F_2 + 16 sccm N_2, shutter open, 30 W, 100 mTorr, 15 sec
S52C	Control experiment for S52 - no deposition performed after plasma etch
S53C	Control experiment for S53 - no deposition performed after plasma etch (performed before S53)
S53	Plasma etch in 5 sccm CCl_2F_2 + 16 sccm N_2, shutter open, 30 W, 100 mTorr, 2 min

capacitors also exhibited high leakage and high ac loss. The etching residue was thought to be polymerized decomposition products of the etch gas. Nitrogen was added to etch gas in an unsuccessful attempt to eliminate the residue.

Results obtained in other Hughes projects indicated that CCl_2F_2 was superior to CCl_4 for GaAs plasma etching. Furthermore, less residue was expected with CCl_2F_2 since the fluoride compounds of carbon are generally more volatile than the chloride compounds. A mixture of 1.6 sccm CCl_2F_2 + 16 sccm N_2 was used at 100 mTorr pressure and 30 W rf power for etch times of 15 sec and 2 min. Capacitance data showed little evidence of a dielectric residue but, as with CCl_4 etching, leakage and ac loss were so high that measurements for accumulation bias greater than $\sim$3 V could not be made. Considering the negative results obtained with CCl_4 and CCl_2F_2, we decided to delay further in situ etching experiments until a source of carbon-free etch gas, e.g. HCl or Cl_2, could be attached to the system.

SECTION 4

PLASMA ENHANCED DEPOSITION OF GERMANIUM NITRIDE AND SILICON NITRIDE/GERMANIUM NITRIDE MIXTURES

During this reporting period, four runs were performed to identify deposition parameters suitable for preparing germanium nitride films with acceptable dielectric properties by plasma-enhanced deposition (PED), and two runs were performed to establish preliminary parameters for the deposition of Si_3N_4/Ge_3N_4 mixtures.

A baseline process for the deposition of PED germanium nitride was established early in this semester. Deposition parameters giving films with an index of refraction expected for Ge_3N_4 were initially determined by ellipsometry. A film about 50 nm thick was then deposited on pyrolytic carbon and analyzed by Rutherford backscattering (RBS). The RBS spectrum was interpreted as showing no oxygen contamination. However, because of problems with the RBS system that prevented normal plotting of the data, determination of the Ge/N ratio from these data was not attempted. The GeN_x deposition parameters established as base line are as follows:

Nitrogen plasma preburn:

- Shutter: Closed
- Temperature: 200°C
- N_2 flow rate: 16 sccm
- System pressure: 100 mTorr
- RF power: 100 W
- Duration: 10 min

Deposition:

- Temperature : 200°C
- Hot plate rotation: on (6 rpm)
- N_2 flow rate: 16 sccm

Flow rate of 1.5% GeH_4 in Ar: 80 sccm

Germane dispersal ring motion: on (passes over hot plate 6 times per minute)

System pressure: 250 mTorr

RF power: 50 W

Deposition rate: ∿9 nm/min

Deposition time: 10 min

All other procedures employed were identical to the baseline silicon nitride process described in Section 2C. One run, G1, was performed using the baseline process. This run yielded films with an index of refraction of 1.92. MIS capacitors incorporating the baseline germanium nitride films exhibited large frequency dispersion under accumulation bias similar to that observed for PED silicon nitride films. In addition, the germanium nitride films exhibited an irreversible decrease in capacitance when the applied field exceeded $\sim 10^6$ V cm^{-1}.

The remaining three germanium nitride runs were performed without a second pumpdown to high vacuum after the preburn stage (similar to the revised standard PED silicon nitride procedure). In run G2, the sample was loaded onto a cold platen and no preburn was performed. For run G2, the sample was loaded onto a cold platen and the preburn was performed with the shutter open. Run G3 was performed at 300°C after the sample was loaded onto a cold platen, heated to 300°C after pumpdown to high vacuum, and no preburn performed. Samples from all three runs exhibited high conductance values with frequency and bias dependence indicative of high insulator leakage current.

The two runs attempting deposition of silicon nitride/germanium nitride mixtures were performed using revised standard silicon nitride process with the following exceptions: for run SG1, the sample was dipped into methanol after the standard oxide strip, loaded onto a cold platen wet, and heated to 200°C after pumpdown to high vacuum. The deposition was performed with gas flows of 16 sccm N_2, 86 sccm of 1.5% SiH_4 in Ar and 4 sccm of 1.5% GeH_4 in Ar; for run SG2, the same procedures as in run SG were employed, and the gas flows were

16 sccm N_2, 82 sccm of dilute SiH_4 and 8 sccm of dilute GeH_4. Run SG1 yielded films with an index of refraction of 1.89 and a thickness of 101 nm. Corresponding values from run SG2 were 2.05 and 87 nm.

Subsequent to these experiments, it was discovered that the performance of the Rutherford backscattering (RBS) system used to analyze the oxygen content of the baseline germanium nitride films was impaired by partial failure of the data display system. The films were not, in fact, oxygen-free. New RBS data taken after correction of the display problem indicate this material has an O:N ratio of about 3:2. Modification of the process to reduce the oxygen content of the films will be performed early next semester of this program.

Electrical characteristics of MIS capacitors incorporating dielectric films from runs SG1 (low Ge content) and SG2 (high Ge content) are presented in Figures 8(a) and 8(b), and 9(a) and 9(b), respectively. Comparison of Figures 8(a) and 8(b) with Figures 3(a) and 3(b) indicates that the film with low Ge content exhibits interfacial electrical properties somewhat inferior to the baseline PED silicon nitride film. The conductance for the silicon germanium nitride film does not peak at 1 MHz and the peaks for 10 kHz and 100 kHz for this film are very broad and occur at higher voltages than do those for Si_3N_4 film. The silicon germanium nitride sample also exhibits a shoulder in the 1 MHz and 10 MHz conductance curves which is reflected in an abrupt change of slope in the capacitance curves at about 1 V.

The sample prepared with higher Ge content (run SG2) exhibits much worse electrical properties than either the baseline Si_3N_4 film or silicon germanium nitride film with lower Ge content.

Thus our initial attempts to produce films of silicon germanium nitride did not result in improvements of the interfacial electrical properties over those obtained by the baseline PED silicon nitride process. The initial results appear to indicate that the interfacial properties degrade with increasing Ge content.

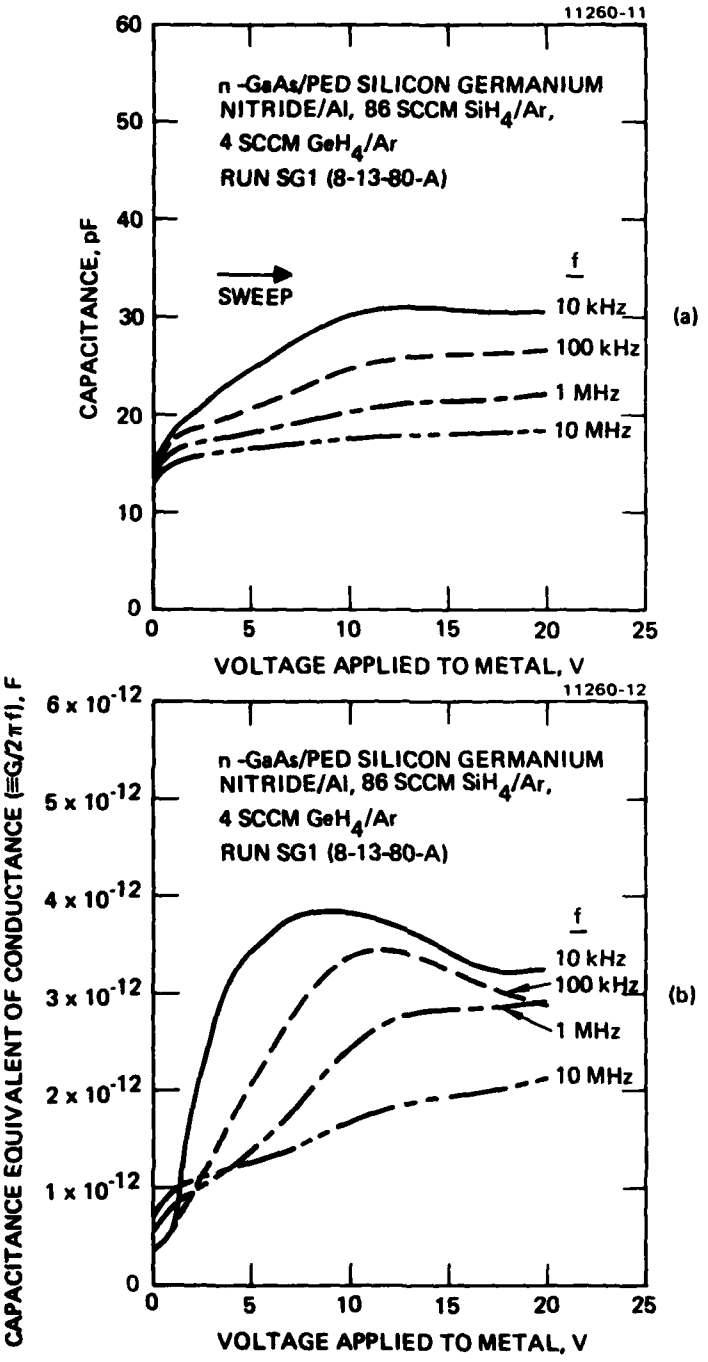

Figure 8. Characteristics of a n-GaAs/PED silicon germanium nitride/Al capacitor deposited with gas flows of 16 sccm N_2, 86 sccm of 1.5% SiH_4 in Ar, and 4 sccm of 1.5% GeH_4 in Ar.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

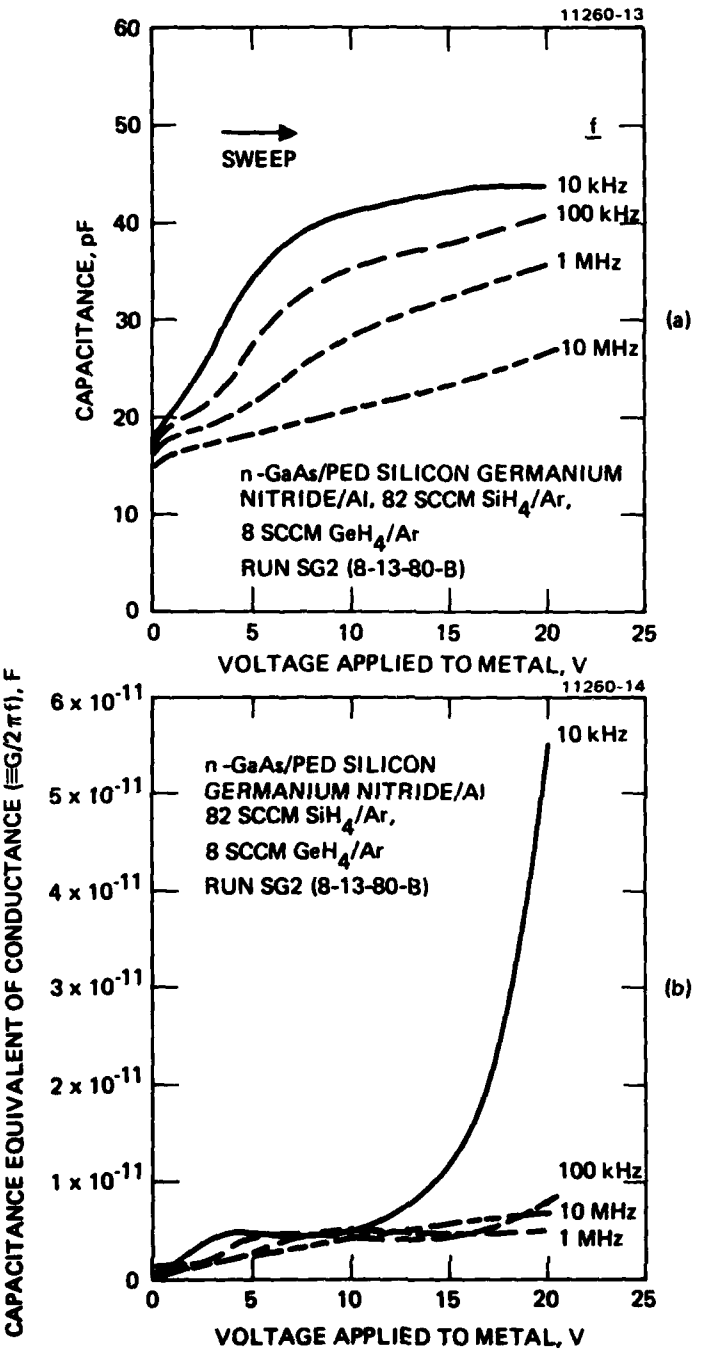

Figure 9. Characteristics of a n-GaAs/PED silicon germanium nitride/Al capacitor deposited with gas flows of 16 sccm N_2, 82 sccm of 1.5% SiH_4 in Ar, and 8 sccm of 1.5% GeH_4 in Ar
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

SECTION 5

CONDUCTANCE METHOD INTERFACE ANALYSIS

Our capability for conductance method analysis of MIS interface properties has been enhanced with a data acquisition and analysis program for our automated C-V measurement system. The program is a modified version of one provided to us by Dr. Millard G. Mier of the Air Force Avionics Laboratory. The program employs a model of the structure that consists of a loss-free insulator capacitance, C_{ox}, in series with a space charge region admittance $G_p + j\omega C_p$. The program controls measurement of the composite admittance $G_m + j\omega C_m$ as a function of ω and bias voltage, and the computes G_p and C_p. The C_{ox} value employed for analysis is the larger of two 10 kHz measurements, one for the Si monitor sample and one for the GaAs sample, with both measurements made under high accumulation bias. Following analysis, the data are plotted for each bias voltage as $G_p/\omega C_{ox}$ vs. ω (Goetzberger plot) and $G_p/\omega C_{ox}$ vs. C_p/C_{ox} (Cole-Cole plot).

Determination of the insulator-semiconductor interface state density versus semiconductor surface potential by the conductance method is based on the interface model of E.H. Nicollian and A. Goetzberger[1]. The first step in the analysis is accurate determination of C_p and $G_p(\omega)$ for each gate test voltage. For a loss-free insulator (for which C_{ox} is independent of ω), these parameters are given by:

$$\frac{C_p}{C_{ox}} = \frac{1 - C_m/C_{ox}}{\left(1 - C_m/C_{ox}\right)^2 + \left(G_m/\omega C_{ox}\right)^2} - 1 \qquad (1)$$

and

$$\frac{G_p}{\omega C_{ox}} = \frac{G_m/\omega C_{ox}}{\left(1 - C_m/C_{ox}\right)^2 + \left(G_m/\omega C_{ox}\right)^2}. \qquad (2)$$

The surface potential is computed from C_p and the substrate doping concentration, and the surface state density computed either by fitting the shape of the experimental $G_p/\omega C_{ox}$-ω curves to theoretical curves[1] or by the distance between the two $G_p/\omega C_{ox} = 0$ intercepts of a Cole-Cole plot[2].

The results of application of this method to samples made in this program are typified by the data for sample S15 shown in Figure 10. Figure 10(a) is the Goetzberger plot and Figure 10(b) is the Cole-Cole plot. Surface state density cannot be obtained from these data because the $G_p/\omega C_{ox}$ curves do not exhibit peaks; i.e., according to the model, there should be two intercepts at which $G_p/\omega C_{ox}$ approaches zero.

Failure of the conductance method with these samples is primarily a consequence of the very high surface state density that prevents attainment of strong accumulation of gate voltages less than the breakdown voltage of the insulator. This behavior makes accurate determination of C_{ox} very difficult. An accurate C_{ox} is necessary because the values of C_p and G_p computed from Equations 1 and 2 are very sensitive to C_{ox} in the strong accumulation regime where $C_m/C_{ox} \rightarrow 1$. C_{ox} measured from a witness samples, e.g., a n^+ or p^+ Si substrate, is uncertain because of difficulty in obtaining precisely the same film thickness of both substrates and the possible existence of a thin native oxide insulator film on either sample.

An additional uncertainty factor is dielectric loss in the PED insulator. It appears that these materials generally exhibit dielectric loss. Consequently, the insulator must be modeled as a complex admittance, $C_{ox}(\omega) + j\omega G_{ox}(\omega)$. Expressions for C_p and G_p comparable to Equations 1 and 2 can be derived for the case of a lossy insulator. However, the problem of an accurate analysis is then compounded by the need for measurements of C_{ox} and G_{ox} as a function of ω.

Owing to these measurement undertainties, the conductance method is of little utility for analyzing the samples made thus far. The method does not yield reliable quantitative parameters for these samples and qualitative behavior can be judged more readily from plots of multifrequency $C_m(V)$ and $G_m(V)$.

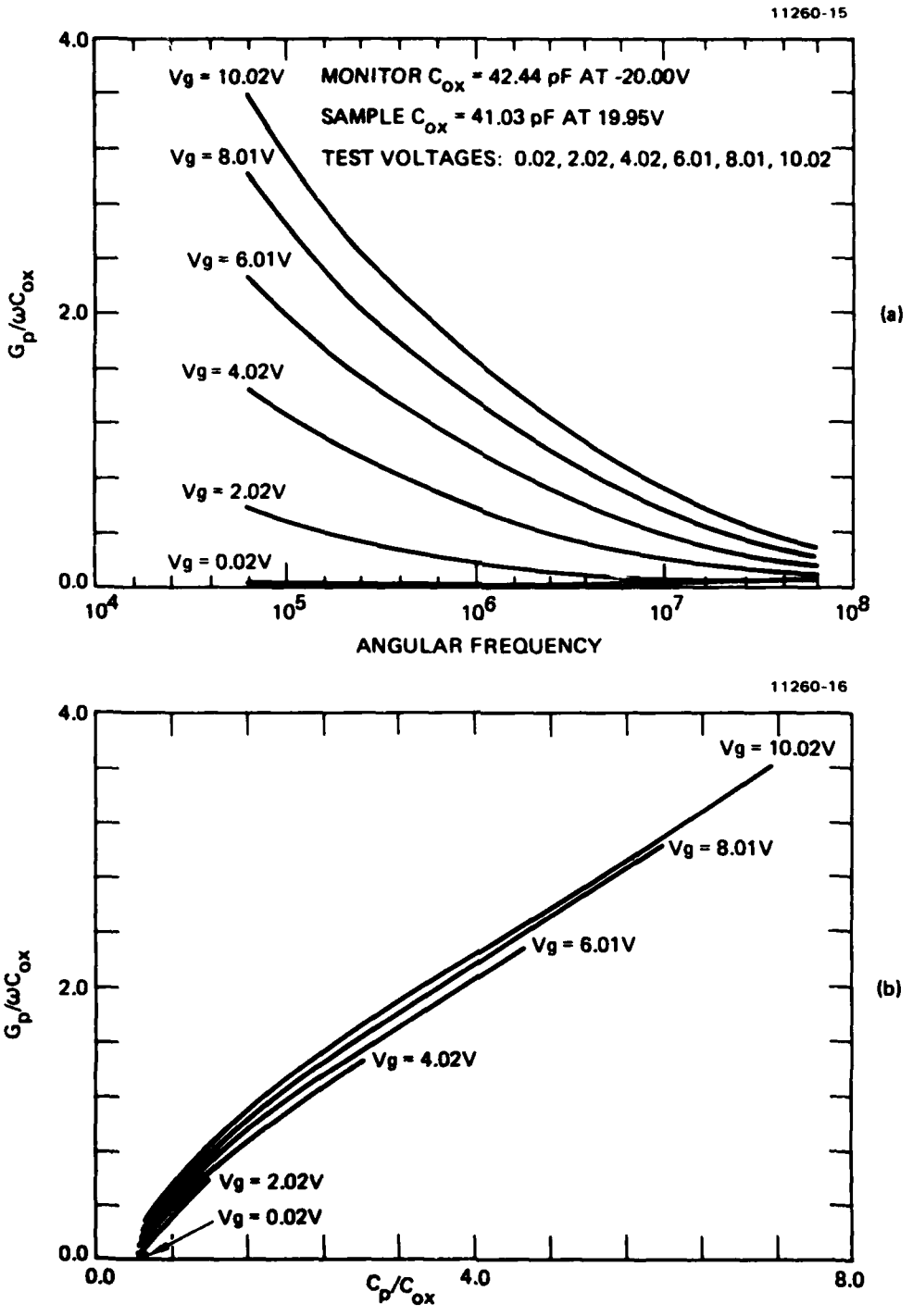

Figure 10. Goetzberger plot (a) and Cole-Cole plot (b) for Sample S15.

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2. P. Chr. Malmin, Phys. State. Sol. (a), 8, 597 (1971).


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