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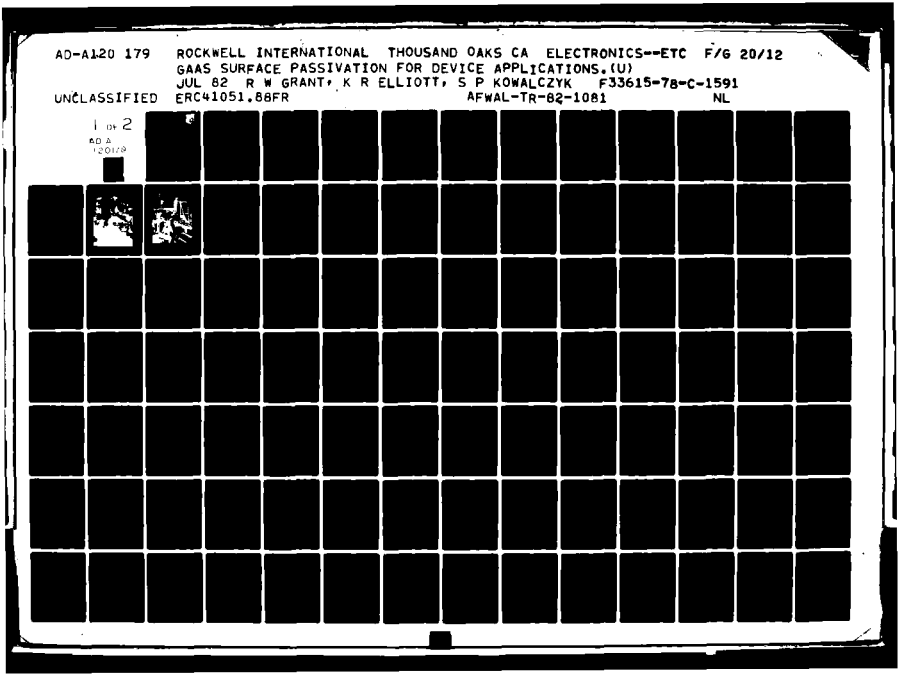

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GaAs SURFACE PASSIVATION FOR DEVICE APPLICATIONS

R.W. Grant, K.R. Elliott, S.P. Kowalczyk, D.L. Miller,
J.R. Waldrop and J.R. Oliver

Rockwell International Microelectronics Research and Development Center
1049 Camino Dos Rios
Thousand Oaks, CA 91360

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Final Report for the period 12/03/79 through 08/31/81

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Avionics Laboratory
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Dietrich W. Langer

DIETRICH W. LANGER
Project Engineer
Electronic Research Branch
Avionics Laboratory

FOR THE COMMANDER

Philip E. Stover

PHILIP E. STOVER, Chief
Electronic Research Branch
Avionics Laboratory

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Two approaches were pursued in an effort to achieve a GaAs MIS technology. The first approach attempted to reproduce promising literature-reported C-V results on MBE-grown AlAs/$Al_{1-x}Ga_xAs$/GaAs heterojunction structures. The insulator was formed on these structures by thermal oxidation of the outer AlAs/$Al_{1-x}Ga_xAs$ layers. Although several samples involving both n- and p-type structures were prepared, the C-V results showed only deep depletion characteristics with substantial hysteresis and the insulators

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formed by thermal oxidation were relatively poor. Substantially improved insulators were prepared by using either plasma oxidation or deposited insulators. However, the C-V characteristics of the resulting MIS devices were similar to those obtained by using the thermal oxidation process. It was concluded that it may be as difficult to obtain a useful insulator/$Al_{1-x}Ga_xAs$ interface from an MIS viewpoint as it is to obtain a good insulator/GaAs interface. A reanalysis of the promising literature reported C-V results on the thermally oxidized AlAs/$Al_{1-x}Ga_xAs$/GaAs heterojunction structure has indicated some apparent internal inconsistency. While studying MBE-grown samples in this program, a novel technique to protect reactive $Al_{1-x}Ga_xAs$ surfaces from air exposure degradation was developed. The technique involves the deposition of a $\approx 10^3$Å thick layer of elemental As from the As MBE source onto a cooled MBE-grown $Al_{1-x}Ga_xAs$ sample. Experiments have shown that a contamination-free and well-ordered $Al_{1-x}Ga_xAs$ surface can be prepared by evaporating the elemental As at $\geq 300^0$C within another UHV system even after the MBE grown sample has been stored in air for several days. This technique may be important for combining MBE with other device fabrication processes. In particular, XPS surface potential measurements on MBE grown GaAs(100) and (110) p-type surfaces protected by this technique have determined a surface band bending of < 0.2 eV which indicates that these surfaces may be promising candidates for deposited insulator GaAs MIS applications.

The second approach studied to obtain a GaAs MIS structure involved the use of deposited insulators. C-V results were obtained on MIS structures which involved insulators prepared by evaporation of SiO_x or by reactive deposition of $Si_xO_yN_z$. These results and other considerations suggested that oxygen-free insulators may be needed for GaAs MIS applications. A UHV system was developed for the deposition of AlN. The AlN was deposited onto thermally cleaned GaAs substrates by a reactive deposition process. Good insulator properties were obtained for the deposited AlN. Although the C-V characteristics of the MIS structures fabricated by using the deposited AlN showed subatantial hysteresis, these preliminary results when compared to calculations for an ideal MIS structure suggest that both accumulation and inversion were obtained. The rationale which indicates that the AlN/GaAs interface could be attractive for GaAs MIS applications is discussed.

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I. INTRODUCTION

This is the final report for Contract #F33615-78-C-1591 entitled "GaAs Surface Passivation for Device Applications." A primary goal of this program was to investigate dielectric/GaAs interfaces which could be useful for a GaAs MIS technology. The development of GaAs MIS devices has been adversely affected by a lack of understanding and inability to control dielectric/GaAs interface properties. A generally useful GaAs MIS technology would be applicable to a number of digital and analog circuit applications; in particular, this technology could facilitate the fabrication of enhancement mode FETs with wide dynamic range for direct coupled logic applications at multigigabit data rates.

This program was initiated in July 1978. The program was divided into two phases. The first phase was conducted by personnel in Anaheim, CA and concentrated on investigating the use of ion-implantation techniques to modify a GaAs surface prior to forming a dielectric by oxidation. Although encouraging results relative to modifying the GaAs surface to permit uniform oxide growth were obtained, it was concluded that further development work to optimize the ion-implantation MIS approach would be outside the scope of this program. The final report for Phase 1 of the program was published as AFWAL-TR-80-1018; the Summary and Conclusions Section of that technical report are reproduced here in Appendix II.

Phase 2 of the program (initiated in December 1979) was conducted by personnel in Thousand Oaks, CA. Two approaches to obtain a GaAs MIS technology were pursued simultaneously. One approach involved the use of lattice-matched molecular beam epitaxy (MBE) grown $Al_{1-x}Ga_xAs$/GaAs interfaces. A dielectric/$Al_{1-x}Ga_xAs$ interface was subsequently fabricated thereby eliminating the dielectric/GaAs interface from the MIS structure. The second approach involved the formation of dielectric/GaAs interfaces by using deposited insulators. In most cases, the interface and/or insulator composition were

characterized by x-ray photoemission spectroscopy (XPS) in order to correlate compositional information with MIS properties.

The organization of this report is described here. Section II discusses the instrumentation which was used to prepare the MBE samples and characterize the MIS structures. Section III documents the samples which were used for MIS fabrication and discusses a novel technique which was developed to protect the surfaces of MBE grown samples from degradation due to air exposure. In Section IV, investigations of MIS structures fabricated on MBE grown $Al_{1-x}Ga_xAs$ samples are reported. This work suggests that it will be as difficult to obtain useful oxide/$Al_{1-x}Ga_xAs$ interfaces from an MIS viewpoint as it is to obtain good oxide/GaAs interfaces. An analysis of previously published results which suggested promising C-V results for an MIS device fabricated with an oxide/$Al_{1-x}Ga_xAs$/GaAs structure indicates some apparent internal inconsistency in the results. Investigations of oxides deposited on GaAs by evaporation techniques within the ultra high vacuum (UHV) XPS system are discussed in Section V. The results reported in Sections IV and V in addition to other work, indicate that it will be difficult to use an oxide as the dielectric in a GaAs MIS structure. Preliminary attempts to prepare a non-oxygen containing insulator (Si_xN_y) are discussed in Section VI. This work demonstrated the need to develop a UHV system for depositing non-oxygen containing insulators on atomically clean GaAs surfaces. This development and experiments to prepare nitrides as insulators for GaAs MIS applications are reported in Section VII. Promising, although very preliminary I-V and C-V results are presented for the AlN/GaAs interface. The rationale which suggests that further study of the AlN/GaAs interface could produce important MIS results is discussed in Section VIII. Sections IX and X summarize the second phase of this program and provide references. Three papers were published based on work supported or initiated by this program; these papers are reproduced in Appendix I.

II. INSTRUMENTATION

In this section, the MBE apparatus (used to prepare $Al_{1-x}Ga_xAs$ samples for MIS fabrication) and other equipment (C-V, G-V, I-V, XPS and SAM) used to characterize MIS structures are discussed.

1. MBE

The apparatus used to prepare the MBE samples which were studied in this program is shown in Fig. 1. This apparatus was designed and constructed in 1977 at MRDC, Thousand Oaks, for the growth of GaAs and $Al_{1-x}Ga_xAs$. The MBE machine has extensive LN_2 cryoshrouding to maintain excellent vacuum conditions during epitaxy, a cryogenic 10K sorption pump to provide a high pumping speed for CO, and an airlock substrate insertion system. This airlock was utilized in some experiments to provide an initial oxidation of the samples in an H_2O-free O_2 atmosphere.

2. C-V, G-V, and I-V

The MIS structures investigated in this program were electrically characterized with C-V, G-V, and I-V measurements. Most C-V measurements were obtained at 1 MHz with an automatic C-V profiler which utilizes a PAR 410 C-V plotter. Unless otherwise indicated, the samples were in the dark at room temperature and the sweep rate was 1.1 V/s. Variable frequency C-V and G-V measurements were carried out by using a Hewlett Packard 4270A C-V bridge and a voltage ramp. I-V measurements were performed with an automated instrument capable of measuring small currents ($< 10^{-10}$ amp).

3. XPS

A Hewlett-Packard 5950A electron spectrometer was used for the XPS investigations of surface chemistry and potential in this program. A photograph of this instrument is shown in Fig. 2. The spectrometer has been modified to obtain ultra-high vacuum ($< 10^{-10}$ torr) and provide various in situ

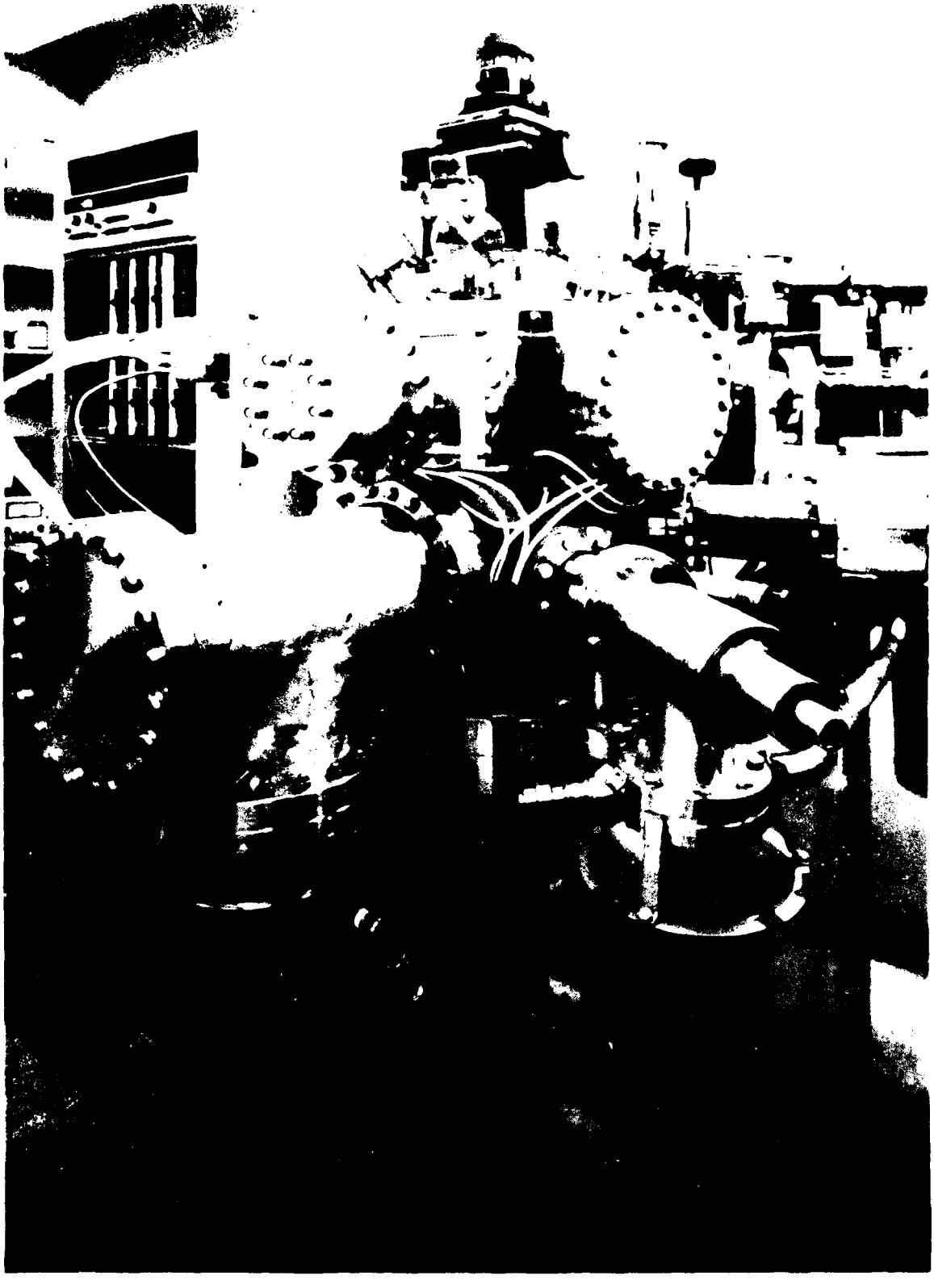


Fig. 1 Photograph of MBE apparatus.

Fig. 2 Photograph of XPS apparatus.

specimen treatments. These treatments include sample heating, insulator and atomic-beam deposition, ion etching and low energy electron diffraction (LEED) analysis capability.

The ability of XPS to determine surface chemistry by analyzing chemical shifts is well known.[1] The technique also provides a convenient method to determine the surface potential of a sample.[2,3] The determination of surface potential is illustrated briefly here. Figure 3 shows a schematic band diagram for GaAs. In this figure, all binding energies are referred to the Fermi level (E_F). The conduction-band minimum is E_c^{GaAs}, the valence-band maximum is E_v^{GaAs}, the As3d core-level binding energy is E_{As3d}^{GaAs}, the Fermi-level position relative to E_v^{GaAs} is Δ, and W is the depletion width. The (b) and (i) notations refer to bulk- and interface-quantities respectively. For a flatband condition $\Delta(b) = \Delta(i)$. The bulk doping characteristics determine $\Delta(b)$. The typical electron escape depth ($\approx$ 25 Å) is much shorter than the typical semiconductor depletion width. Thus an XPS measurement of a clean GaAs surface or a surface with a very thin overlayer ($<$ 25 Å) will determine $E_{As3d}^{GaAs}(i)$ as shown in the figure. Because $E_{As3d}^{GaAs} - E_v^{GaAs} = 40.73$ eV is known[3] with good precision, it is therefore possible to directly measure the interface Fermi-level position, $\Delta(i)$, of a semiconductor sample.

4. SAM

A Scanning Auger Microprobe (SAM) PHI Model 595A was used to obtain depth analysis profiles. The SAM was equipped with a 5keV Ar^+ ion sputter gun. The depth profiles were obtained by a series of sputter-Auger analysis steps.

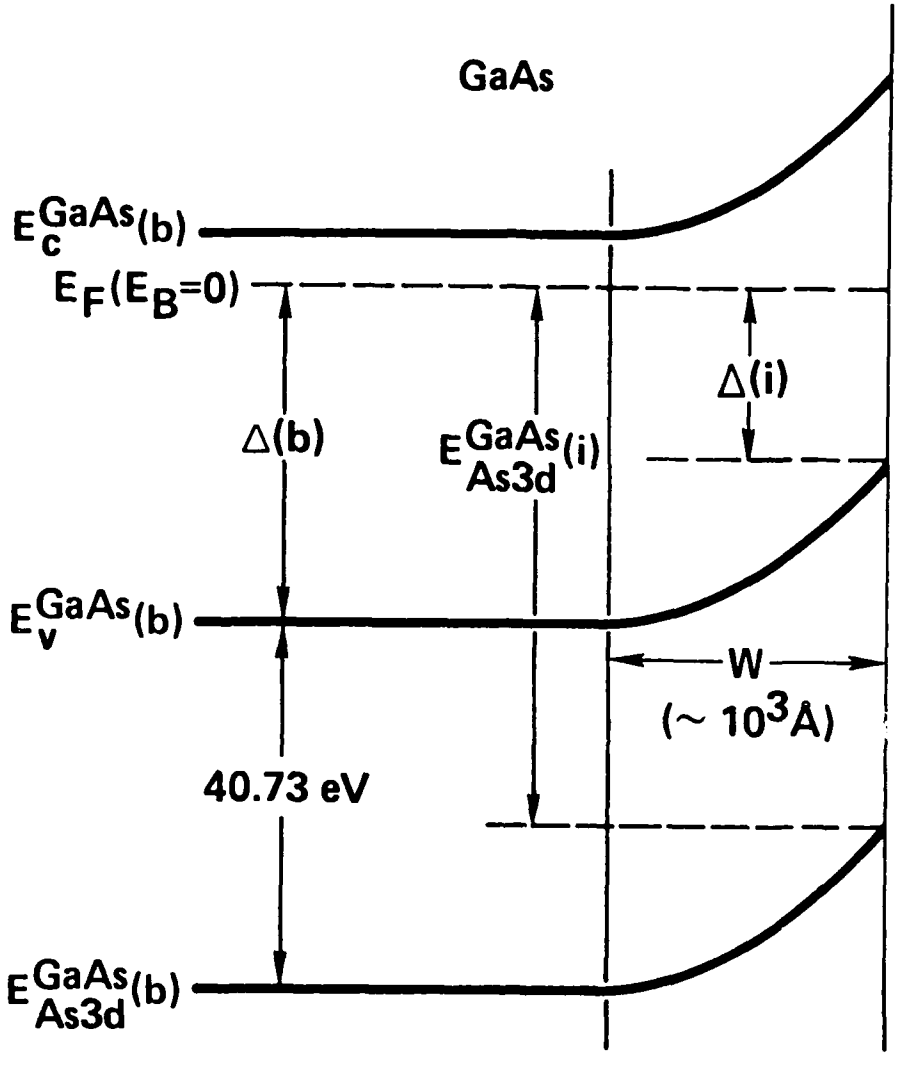


Fig. 3 Schematic energy-band diagram which illustrates the XPS measurement of interface Fermi level for GaAs.

III. SAMPLE DESCRIPTION

In this section, the $Al_{1-x}Ga_xAs$ samples used in this program are described. In addition a novel technique useful for protecting surfaces of MBE grown $Al_{1-x}Ga_xAs$ samples from air oxidation is discussed.

1. MBE Prepared Samples

It has been suggested (see e.g., Ref. 4 and 5) that one method to obtain a useful MIS structure would be to form a lattice matched heterojunction interface to GaAs. This approch should minimize the formation of electrically active states at the GaAs interface. The second component of the heterojunction can be insulating or a suitable insulator can be formed on this component. Particularly promising C-V results have been reported by Tsang et al[4] where dielectric layers were formed by thermal oxidation of graded $Al_{1-x}Ga_xAs$ epitaxial layers grown by MBE. The outer layer of the structure is AlAs. A second layer graded from AlAs to $Al_{0.5}Ga_{0.5}As$ is located between the AlAs and GaAs layer. Due to the large difference in oxidation rate of AlAs and GaAs, it is expected that an oxide layer growth can be controllably stopped within the graded $Al_{1-x}Ga_xAs$ layer. Most of the MBE grown samples described in this section were prepared to investigate this concept of forming an MIS structure.

Samples designated as #411, 412, and 413 were grown by MBE. These three structures are illustrated schematically in Fig. 4a. All three were grown in an identical manner except for the $Al_{1-x}Ga_xAs$ layer between the n-type GaAs and the AlAs layer. The substrate in each case was n^+ Se-doped GaAs grown at MRDC. This was prepared by using a Br-methanol etch on a rotating felt pad. The substrate was then soldered to the Mo MBE substrate holder heating block with indium metal, followed by a 10 sec etch in flowing $H_2O/H_2O_2/NH_4OH$ (10:1:1). This substrate preparation procedure typically leads to an oxidized GaAs containing a trace of carbon, as seen by Auger Electron Spectroscopy.

MBE SAMPLES

SAMPLE # 411 412 413

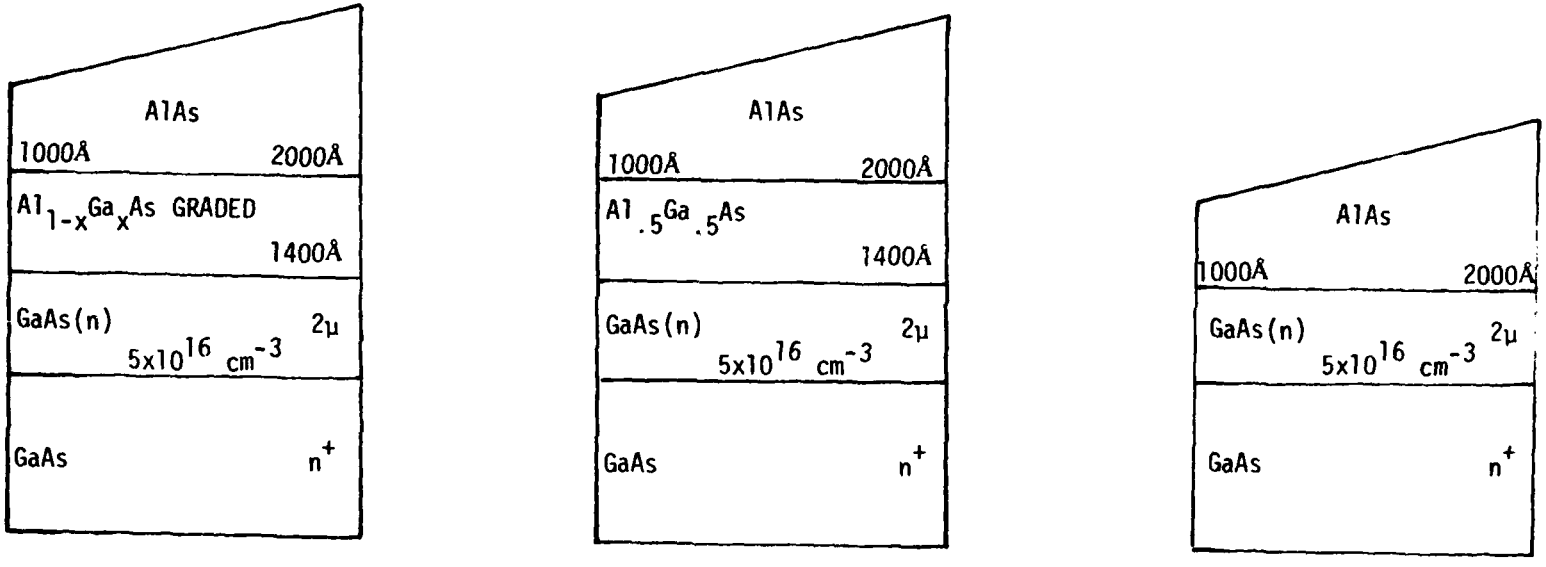


Fig. 4a Schematic illustration of structure for MBE samples #411, 412, and 413.

MBE SAMPLES

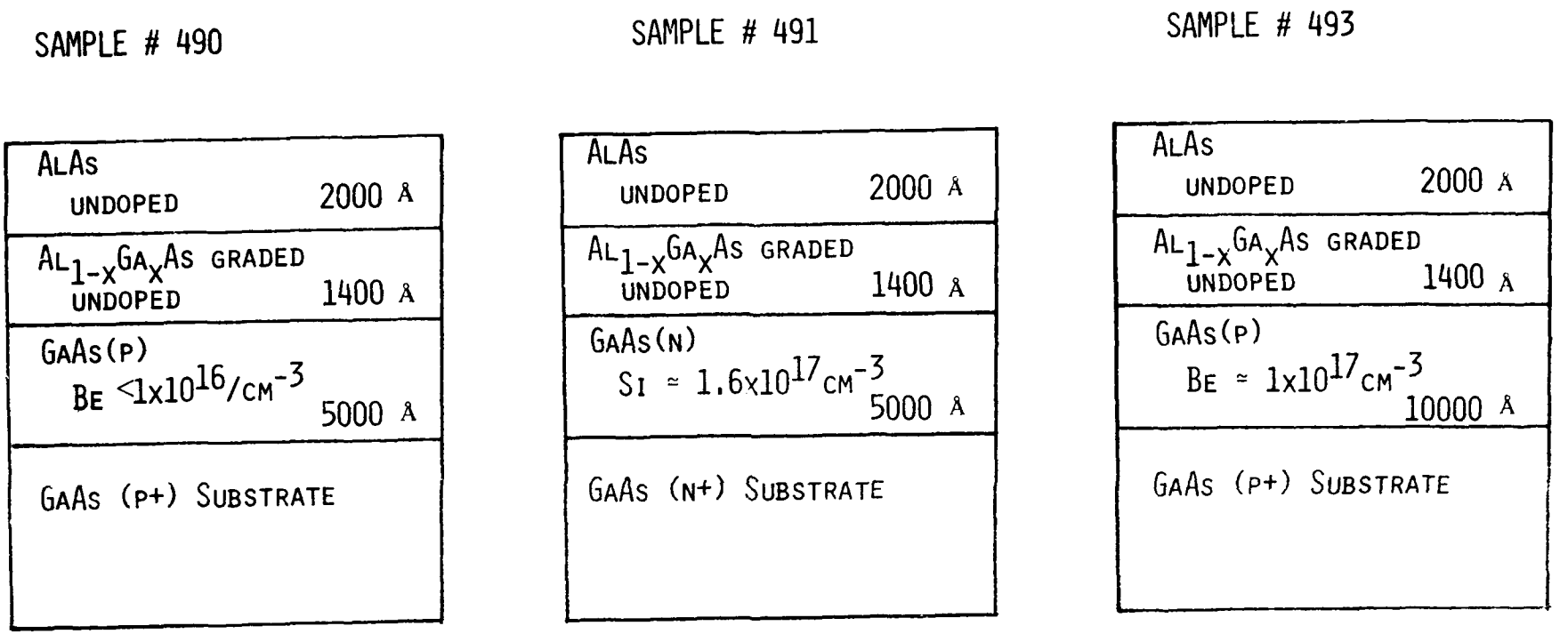
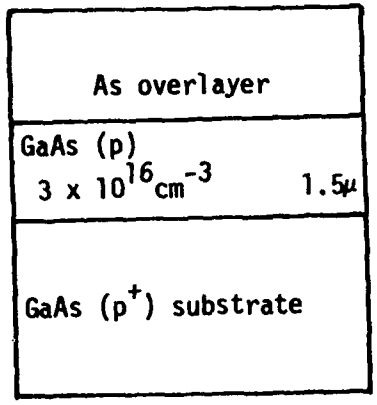


Fig. 4b Schematic illustration of structure for MBE samples #490, 491, and 493.

SAMPLE # 595



SAMPLE # 594

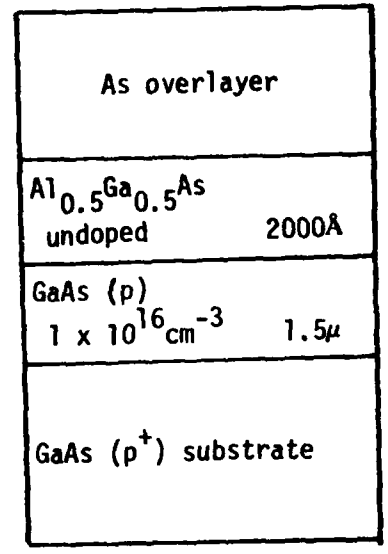


Fig. 4c Schematic illustration of structure for MBE samples #595 and 594.

The oxide was removed from the GaAs substrate by heating the substrate in about 10^{-6} torr of As_4 (from elemental 6N As) to 580°C for 10 min. Epilayer growth was done with a substrate temperature of approximately 550°C, growth rate of 1.0 μm/hr, and a ratio of As_4 to Ga partial pressures of 20:1, as measured by a movable ion gauge. Tin was used to dope the GaAs layer to $5 \times 10^{16}/cm^3$. The n-type GaAs layers were 2 μm thick.

$Al_{1-x}Ga_xAs$ intermediate layers were grown on two of the three samples. For sample #411, the Al content was initially set at x = 0.5 by opening the Al source shutter with the Al flux set equal to the Ga flux. The composition was then graded linearly to x = 1.0 over a 1400 Å thickness by gradually reducing the Ga source temperature. For sample #412, the Al content remained at x = 0.5 during the entire 1400 Å intermediate layer growth. Sample #413 had no intermediate $Al_{1-x}Ga_xAs$ layer. Substrate temperature for the $Al_{1-x}Ga_xAs$ intermediate layer growth, and for growth of the top AlAs layer, was increased to about 590°C. This somewhat higher substrate temperature has been used most successfully in the MBE growth of low threshold double-heterostructure lasers[6] and leads to a lower density of traps and recombination centers in the $Al_{1-x}Ga_xAs$ than more conventional MBE substrate temperatures of 550-580°C. The $Al_{1-x}Ga_xAs$ intermediate layers were not intentionally doped, and therefore are expected to be semi-insulating.

Following the $Al_{1-x}Ga_xAs$ intermediate layer (or the n-type GaAs layer in sample #413), undoped AlAs was grown epitaxially at ≈ 590°C by shutting the Ga shutter, leaving the Al and As_4 fluxes unchanged. The thickness of the AlAs layer was varied linearly along the length of the samples by using a Mo shutter to gradually cover a portion of the grown layer. In this way, the AlAs thickness was varied from about 1000 Å to about 2000 Å across each sample.

Following growth of the AlAs top layer, each sample was cooled to ≈ 420°C and withdrawn into the MBE chamber airlock. Cooling during the transfer process resulted in the temperature dropping to about 400°C by the time the sample was within the airlock. Pure O_2 was then used to backfill the

airlock to about 0.1 atm, and the sample and Mo block were allowed to cool in O_2 to room temperature, which took about 30 min.

Three additional samples identified as #490, 491, and 493 were prepared in a manner similar to that discussed above except for the changes discussed here. Schematic diagrams of these sample structures are shown in Fig. 4b. Samples #490, 491, and 493 were grown at 620°C substrate temperature, rather than the ≈ 550-590°C used for #411, 412, and 413. Data accumulated in a number of laboratories have shown that $Al_{1-x}Ga_xAs$ grown by MBE at 620°C and above is markedly superior to material grown at lower temperatures in terms of carrier mobility, luminescence, and deep-level content. Therefore, it was hoped that $Al_{1-x}Ga_xAs$ grown at this higher substrate temperature would yield better MIS structures than the material used for the #411, 412, and 413 samples.

For samples #490, 491, and 493, Si (rather than Sn) was used as the doping for the n-type GaAs buffer layers. This was done to eliminate doping of the $Al_{1-x}Ga_xAs$ graded transition layer due to the Sn surface segregation phenomenon. In MBE growth of GaAs, Sn is incorporated into the growing film from a surface accumulation, which rides along on the growth surface. This mechanism delays the transient response of the system to changes in dopant flux, and also makes Sn doping sensitive to substrate temperature, alloy composition, and As/Ga flux ratio. Therefore, a Sn-doped sample of the type prepared here (and also used in Ref. 4) would be expected to have n-type doping extending into the $Al_{1-x}Ga_xAs$ graded region. The depth of this unintentional doping will depend on the details of the growth process. The use of Si as a dopant eliminates this effect. Therefore, for samples #490, 491, and 493, the doping ends abruptly at the GaAs-$Al_{1-x}Ga_xAs$ interface.

A third change was to grow samples #490 and 493 with a p-type buffer layer. This was done to take advantage of the difference in band discontinuities for the conduction- and valence-bands in the GaAs-$Al_{1-x}Ga_xAs$ heterojunction. The band structure for these samples is shown in Fig. 5, for an idealized case which does not show band-bending effects for clarity. The

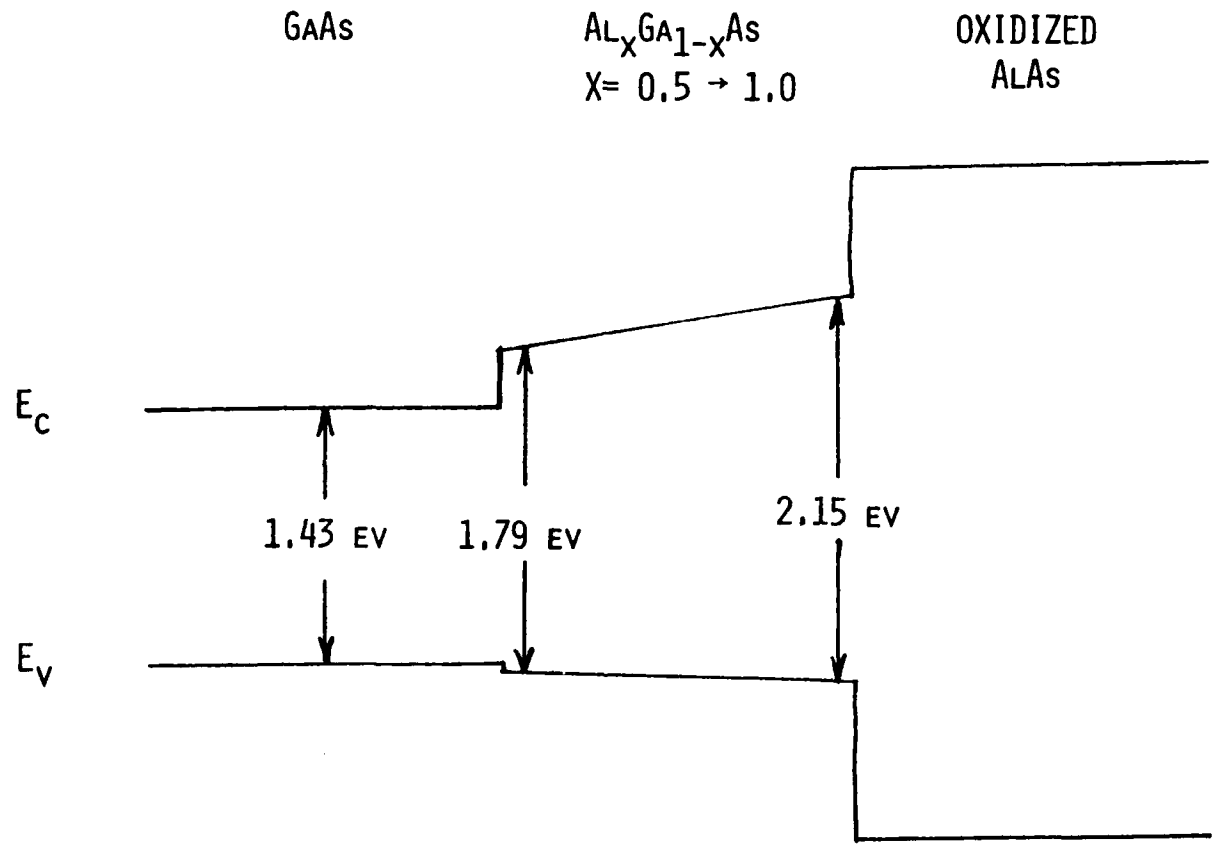


Fig. 5 Idealized flat-band diagram constructed assuming that ≈ 88% of the energy-band gap discontinunity between GaAs and $Al_{0.5}Ga_{0.5}As$ is associated with the conduction-band minimum (E_c) and ≈ 12% with the valence-band maximum (E_v).

important point of this illustration is that the discontinuity in the conduction band at the GaAs-$Al_{1-x}Ga_xAs$ interface is considerably larger than the corresponding discontinuity in the valence band. This diagram assumes that approximately 88% of the bandgap difference falls in the conduction band, with the remaining 12% in the valence band for all $Al_{1-x}Ga_xAs$/GaAs heterojunctions; Dingle et al[7] have determined this distribution for a $Al_{0.2}Ga_{0.8}As$/GaAs heterojunction. Our own measurements on AlAs/GaAs heterojunctions[8] also show that the conduction-band discontinuity is substantially larger than the valence-band discontinuity. Therefore, it may be easier to invert p-type GaAs by confining electrons in the GaAs with the larger (≈ 0.33 eV in this case) conduction-band discontinuity than to invert n-type GaAs by confining holes with the smaller (≈ 0.05 eV) valence-band discontinuity. This assumes that injection of minority carriers into the $Al_{1-x}Ga_xAs$ is largely responsible for a lack of inversion in these structures.

For samples #490, 491, and 493 the AlAs top layer was oxidized in a separate furnace following growth. The samples were contained in a molybdenum holder which was placed in a quartz tube. The tube was flushed with gaseous O_2 (99.6% purity) for several mins before inserting into a tube furnace which was maintained at 400 ± 10°C. A small flow of O_2 was maintained during the oxidation. These oxidation conditions were chosen to duplicate the work reported in Ref. 4 as nearly as possible.

Two important modifications were made to the MBE apparatus before preparing samples #588, 594, 595, and 621. The first was the addition of an antechamber with a heated substrate stage. This allows substrates to be degassed before their introduction into the growth chamber which significantly reduces the amount of water vapor introduced to the growth chamber with each new substate. The second modification was the use of a newly designed Ga oven, which has contributed significantly to improved material quality. Both of these modifications should have improved the quality of the $Al_{1-x}Ga_xAs$ material.

Schematic diagrams which illustrate the structure of samples #594 and 595 are given in Fig. 4c. Sample #595 was a 1.5 μm thick p-type GaAs layer, doped with Be to 3×10^{16} cm^{-3}, grown on a p^+ GaAs substrate, and capped with an arsenic layer for passivation of the surface. The GaAs layer was grown at 580°C. The arsenic overlayer was condensed by cooling the substrate to below room temperature in the arsenic beam used for epilayer growth. This overlayer was estimated to be several thousand angstroms thick. The As overlayer has been found to be resistant to oxidation, and to leave a clean, well-ordered GaAs surface when desorbed at ~ 350°C in UHV (see Section III 2).

Sample #594 was a 1.5 μm thick p-type GaAs layer, doped with Be to 1×10^{16} cm^{-3}, covered with 2000 Å of $Al_{0.5}Ga_{0.5}As$, and then capped with an arsenic passivating layer. Substrate temperature was about 620°C for this run, in an attempt to decrease the impurity content of the $Al_{0.5}Ga_{0.5}As$.[9]

Two growth runs, #588 and 621, were carried out to prepare sets of (100) and (110) oriented GaAs samples which were capped with protective As° layers. Both runs intended to prepare p-type GaAs material doped with $\approx 5 \times 10^{16}$ cm^{-3} of Be. Unfortunately technical difficulties caused the Be flux to be considerably less than expected for run #588 and as noted in Section III 2b, metal point contact measurements made on a (100) sample from this growth run suggest that the sample may have been n-type. These samples were used for XPS surface potential measurements (Section III 2b).

Several GaAs and AlAs samples were grown by MBE on GaAs substrates to test the protective elemental As capping technique which was developed to transfer MBE samples into other vacuum systems without surface contamination (see Section III 2). Samples were prepared with both thin (~ 25 Å) and thick (> 1000 Å) GaAs or AlAs outer layers to test the technique.

2. Arsenic Coating Technique

MBE is a powerful technique for the growth of epitaxial layers. Among the advantages of MBE is that the growths are carried out in UHV ambient and under well controlled growth conditions. A variety of novel and potentially

useful epitaxial structures can be grown by MBE. One major problem in surface studies of MBE growths is how to transfer the growths from a MBE system to another vacuum system through air without oxidation and/or contamination. We have developed a novel and simple method for transferring samples from either of the Rockwell MBE systems to our HP5950A XPS spectrometer. The method is based on the use of a protective elemental As overlayer. This technique did not require any modification of the existing MBE system. The transfer procedure was tested on a variety of MBE grown specimens, with both AlAs and GaAs epilayers. The AlAs is extremely reactive to oxygen and thus provides a rather stringent test case.

The technique consists of growing the desired semiconductor layer in the conventional manner. Next, the key step of depositing the protective layer of elemental As is carried out. Arsenic is condensed on the surface of the epitaxial layers as rapidly as possible following the epilayer growth. This As comes from the arsenic beam used during the growth of the epilayers, and consists of As_4 derived from the sublimation of elemental arsenic. The metal (Ga and/or Al) and dopant sources are abruptly shuttered to terminate the layer growth, while the As_4 beam remains impinging on the surface of the wafer. At typical MBE growth temperatures (550-650°C), no condensation of As occurs (As has a very low sticking coefficient to itself at these temperatures) but the As_4 beam prevents surface decomposition. At the conclusion of the epilayer growth, the substrate heater is turned off and the edge of the substrate holder is brought into contact with the MBE system's liquid nitrogen cooled shroud to speed cooling of the holder. The substrate remains within the central portion of the As_4 beam. After the temperature falls below ~ 450°C, the As_4 flux is reduced by ~ 90%. This step is not necessary but is used to conserve the As charge. The specimen is cooled to slightly below room temperature. Such a temperature is necessary to condense a sufficiently thick As overlayer. This layer is approximately 100-1000 A thick although layers as thin as ~ 15 A thick have been successfully used. The sample is next transferred to the XPS system through air. This step takes about 15 min. Once the sample is again in a UHV ambient, the "as-grown" surface is regenerated by

heating the sample to ~ 300-350°C to desorb the As overlayer. As indicated in the next section (III 2a) this yields an atomically clean and ordered surface as determined by XPS and LEED. Surface potential measurements are reported in Section III 2b.

a. Surface Chemistry Analysis

The As° coating technique has been successfully employed to protect a number of both thin (≈ 25 Å) and thick (≈ 1000 Å) epilayers which include AlAs and GaAs. Figure 6 shows typical results from an AlAs growth. The As overlayer itself is remarkably resistant to oxidation as can be seen from the very small As oxide peak noted in the figure. Samples have been stored in air for 5 days without oxidation of the epilayer and with almost neglible oxidation of the As cap.

This technique may be important for combining MBE with other technologies for device fabrication (e.g., after a MBE growth, another processing step such as ion implantation, MO-CVD epitaxial growth etc. could be carried out in another vacuum system). Also this technique should not be limited to the $Al_{1-x}Ga_xAs$ system, but may include other III-V and II-VI compounds. Instead of As, the appropriate volatile non-metallic component of the desired compound could be used as the cap material (see Table 1 for a partial list of possibilities).

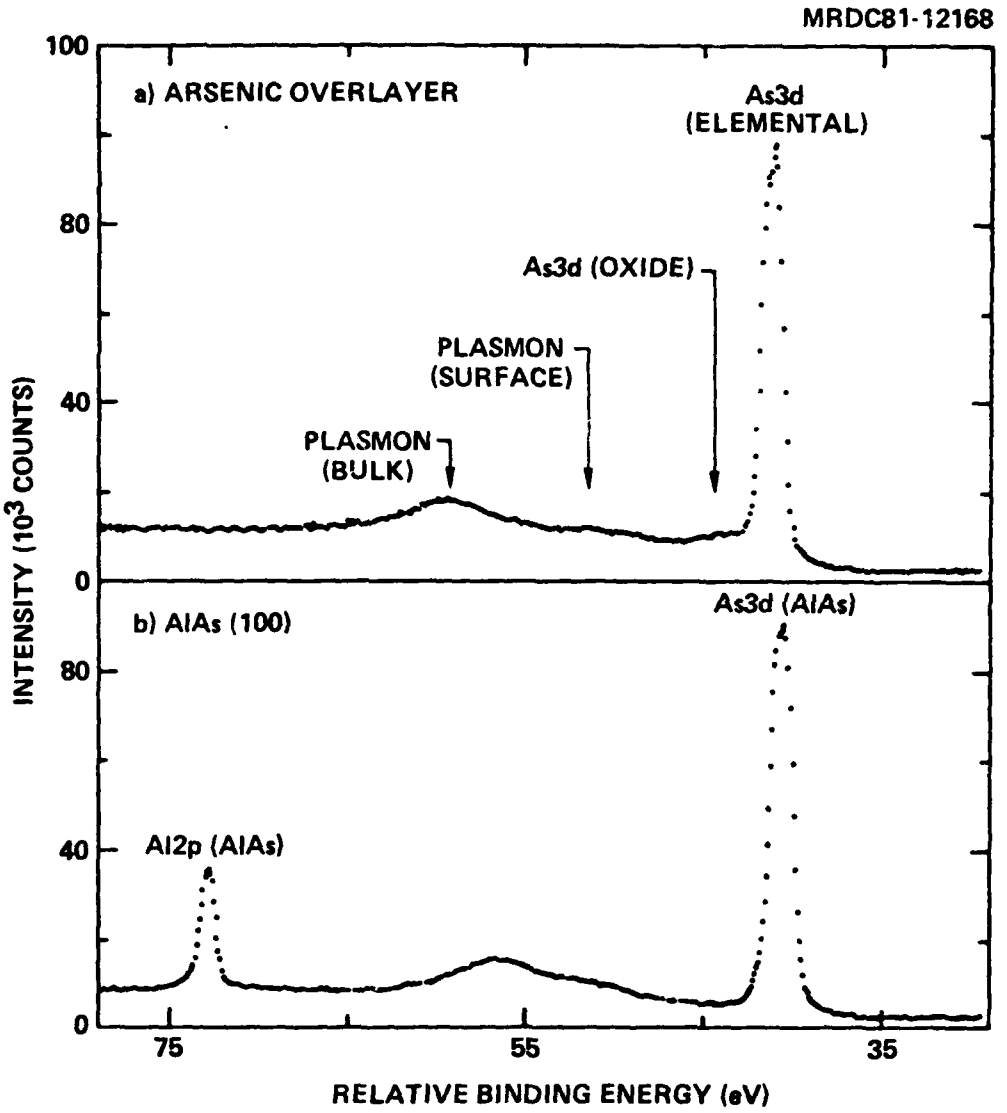


Fig. 6 (a) XPS spectrum of As3d core level from the protective elemental As overlayer for an AlAs sample that had been stored in air for 5 days. (b) XPS spectrum of Al2p and As3d core levels from the underlying AlAs epilayer after the protective As overlayer had been desorbed.

Table 1

Partial List of Materials Which Could Employ
The Protective Capping Technique

	Materials			Protective Layers
	AlAs	GaAs	InAs	As
III-V	AlSb	GaSb	InSb	Sb
	AlP	GaP	InP	P
	ZnS	CdS	HgS	S
II-VI	ZnSe	CdSe	HgSe	Se
	ZnTe	CdTe	HgTe	Te

Ternaries and Quaternaries such as $Al_{1-x}Ga_xAs$, $Hg_{1-x}Cd_xTe$ and $InAs_{1-x}Sb_x$ are also possibilities.

b. Surface Potential Measurements

As discussed in Section II 3, XPS can be used to determine the surface potential of a sample. The perfectly cleaved (110) surface is the only GaAs surface that has been found to be unpinned.[10,11] It is of interest to determine the surface potential for MBE grown GaAs samples which have been protected by the As° capping method. During the MBE growth run #588, both (100) and (110) samples of GaAs were prepared. The samples were intended to be doped p-type (in the mid 10^{16} cm^{-3} range), however, as mentioned in Section III 1, the intentional doping was considerably lighter than expected. Subsequent metal point contact measurements suggested that the (100) sample was actually doped n-type while the measurements on the (110) sample gave an ambiguous result. XPS surface-potential measurements were carried out on these samples. The results are shown in Fig. 7 where E^{GaAs}_{As3d} and $\Delta(i)$ are plotted for several sequential surface treatments. The E^{GaAs}_{As3d} values were determined as described in Ref. 12. The elemental As layer was removed from the surface by

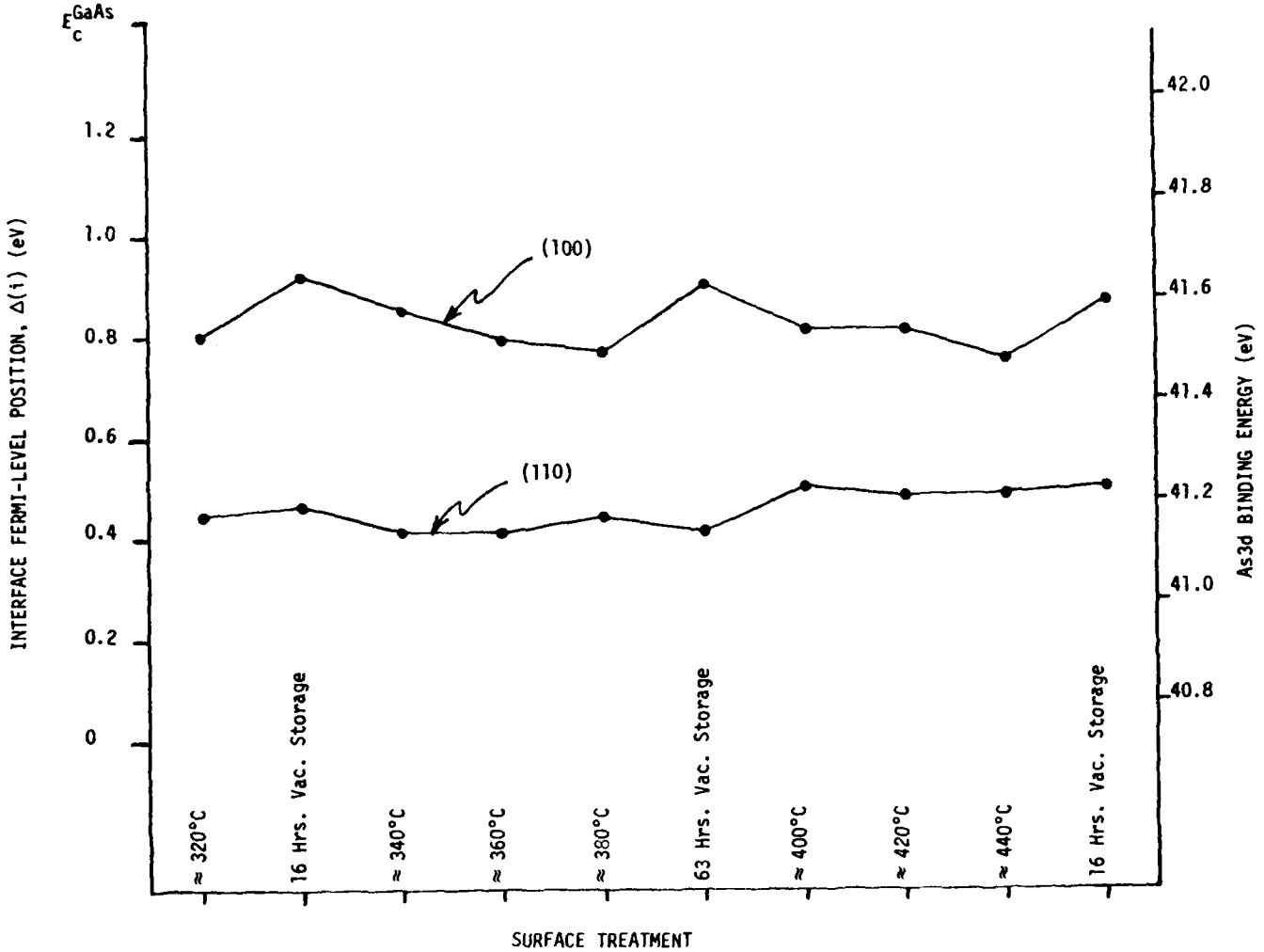


Fig. 7 Interface Fermi-level position and As3d binding energy in GaAs for (100) and (110) samples of MBE growth #588.

heating to ≈ 320°C. Subsequent thermal treatments and vacuum storage (in 10^{-9} torr) caused only small variations in $\Delta(i)$.

The results presented in Fig. 7 show that in all cases the E_F of these two samples was pinned. Previous studies[12] of thermally cleaned GaAs surfaces (cleaned at ≈ 550°C) have shown that n-type surfaces are pinned at about 0.75 eV above E_v while p-type surfaces are pinned at about 0.45 eV above E_v. By comparison with these previous results,[12] the data in Fig. 7 suggest that the (100) surface is n-type while the (110) surface is p-type.

A similar set of measurements was carried out on the 5×10^{16} cm^{-3} p-type samples produced in growth run #621. The results are presented in Fig. 8 where again $\Delta(i)$ and $E_{As\,3d}^{GaAs}$ are plotted for several sequential surface treatments. The first faint LEED patterns appeared at ≈ 340°C while good LEED patterns were observed at ≈ 360°C and above. The surface band bending is seen to be a minimum in the temperature range near ≈ 360°C where the first good LEED patterns are observed. The lowest $\Delta(i)$ is ≈ 0.30 eV for both the (100) and (110) p-type surfaces. At higher temperatures $\Delta(i)$ approaches values of ≈ 0.45 eV for both surfaces which is similar to the values that we have previously observed on thermally cleaned bulk (100) and (110) p-type GaAs surfaces.[12]

For a doping of 5×10^{16} cm^{-3} (p-type) the Fermi level in the bulk should be at about 0.125 eV above E_v. For a $\Delta(i)$ = 0.30 eV, this would correspond to a band bending of ≈ 0.175 eV or a surface charge of ≈ 3×10^{11} proton charges cm^{-2}. This is the lowest band bending that we have observed on any p-type surface (we have not studied the cleaved (110) surface) which of course suggests that these surfaces may have relatively low defect densities. The observation of increased band bending after heating the surfaces above ≈ 425°C suggests that surface stoichiometry changes and/or defect generation may be occuring. These results indicate that the As° protected MBE grown GaAs surface prepared by heating in the temperature range of ≈ 360°C is a promising candidate surface on which to deposit an insulator for MIS applications.

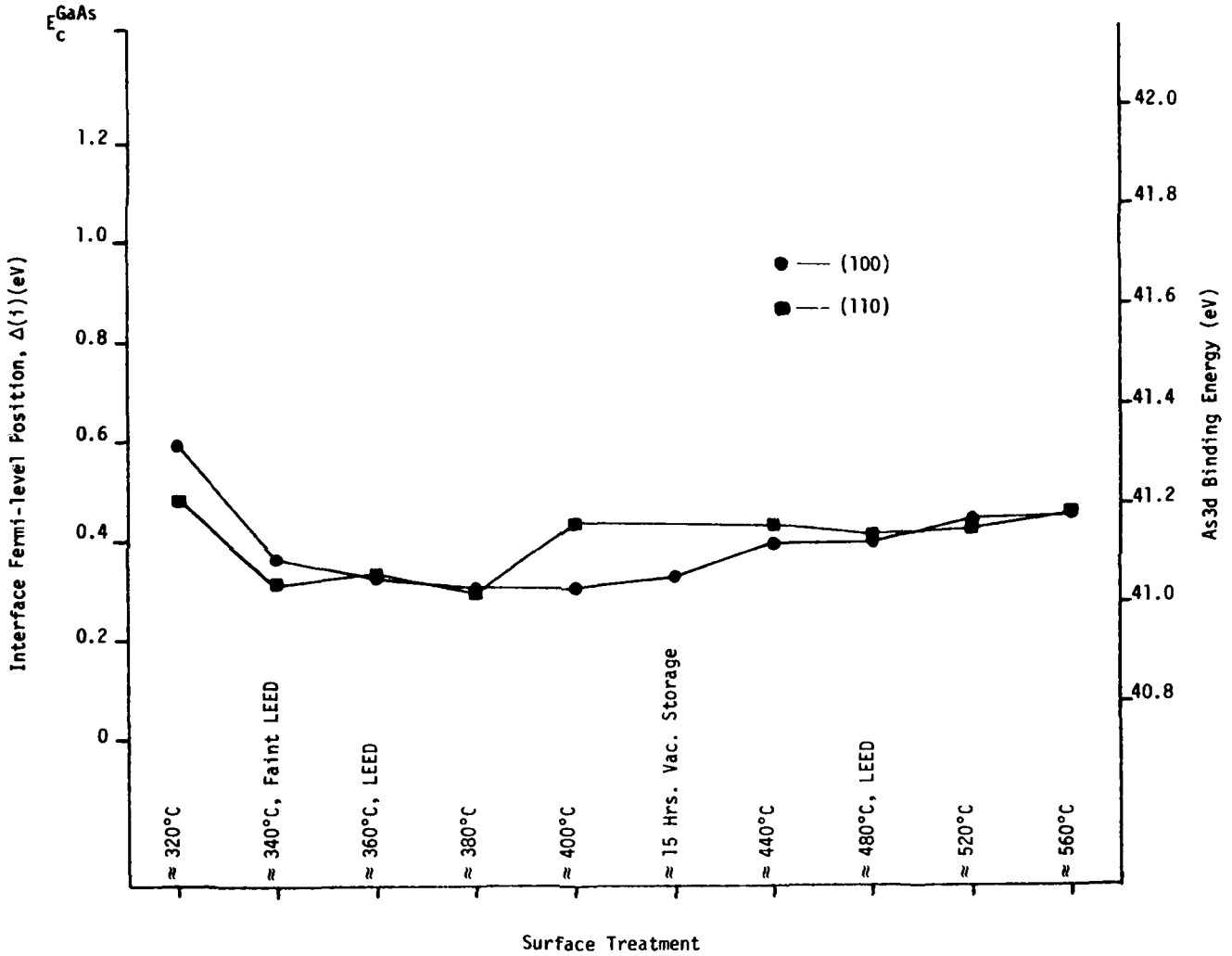


Fig. 8 Interface Fermi-level position and As3d binding energy in GaAs for (100) and (110) samples of MBE growth #621.

3. Bulk GaAs Samples

Several Bridgman grown bulk GaAs (100) samples were utilized for MIS and XPS investigations in this program. These samples were purchased from Crystal Specialties, Inc. The samples were supplied as 15-20 mil thick wafers with one side having a chemical-mechanical polish. Both n- and p-type samples were used. The nominal doping characteristics of the samples as supplied by the vender where n ($\approx 1 \times 10^{17}$ cm^{-3}) and p ($2\text{-}4 \times 10^{16}$ cm^{-3}).

IV. MIS INVESTIGATION OF $Al_{1-x}Ga_xAs$ STRUCTURES

A major part of this program was concerned with attempts to reproduce the MIS results reported by Tsang et al.[4] The dielectric layers were formed by thermal oxidation of MBE grown $AlAs/Al_{1-x}Ga_xAs/GaAs$ structures. These investigations on both n- and p-type samples are discussed in Section IV 1. Because the insulators formed by thermal oxidation were all found to exhibit excessive leakage, additional efforts were made to utilize the lattice matched MBE grown $Al_{1-x}Ga_xAs/GaAs$ interface in a MIS structure but to form the insulator by either plasma oxidation of the $Al_{1-x}Ga_xAs$ layer or by deposition of another insulating material onto the $Al_{1-x}Ga_xAs$ layer. These latter studies are reported in Sections IV 2 and IV 3. In Section IV 4 we have reanalyzed the published results of Ref. 4 and have found some inconsistencies in these results.

1. Thermal Oxidation

In an effort to reproduce the work of Ref. 4, thermal oxidation of $AlAs/Al_{1-x}Ga_xAs/GaAs$ structures was carried out at 400°C in pure O_2.

a. n-Type Samples

As mentioned in Section III 1 samples #411, 412, and 413 were initially oxidized within the MBE apparatus by exposure to O_2 (0.1 atm). The samples were rapidly cooling during this exposure and perhaps only were exposed to temperatures near 400°C for ≈ 0.5 min.

C-V characteristics for these three samples were taken over the range of 1 kHz to 1 MHz. Comparative results are shown in Fig. 9 at 1 MHz; there was essentially no change in the characteristics at lower frequencies. Sample #412 showed the least amount of hysteresis, while #413 showed the largest. The degree of hysteresis for all three samples did not appreciably change with AlAs layer thickness. Hence, the hysteresis is probably due to energetically deep interface acceptor traps.

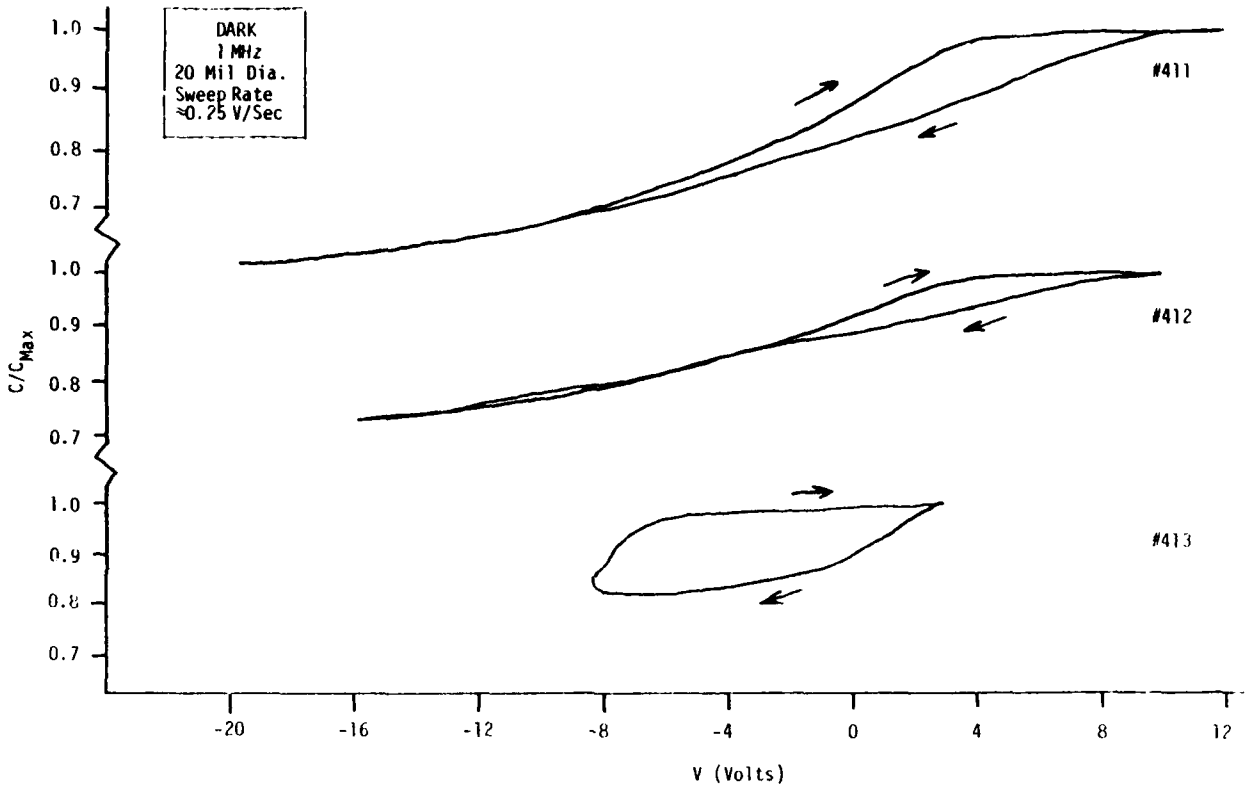


Fig. 9 Typical C-V results for MBE samples #411, 412, and 413 after initial oxidation.

Figure 10 shows the C-V characteristic for sample #411 with a superimposed ideal characteristic (dashed line) for a donor density of 5×10^{16} cm^{-3}. The experimental curve clearly does not show significant inversion at high reverse bias. Also evident is the shift in the C-V characteristic due to a net negative charge at the interface. Figure 11 shows the same curve in comparison with the C-V characteristic under white light illumination. The hysteresis in this case has been substantially decreased, indicating that some of the deep acceptors have been filled with holes. A similar decrease of the hysteresis can be obtained by further oxidation of sample #411 at 400°C for two hours, as shown in Fig. 12. This suggests that the deep acceptor states may lie at the interface between the AlAs and the $Al_{1-x}Ga_xAs$ layers.

Figure 13 shows the G-V curves during white light illumination for sample #411 before and after oxidation. Similar results were obtained for sample #412, but the dark conductance of sample #413 was too high to show any conductance peaks. The conductance peaks for samples #411 and 412 appear only under illumination, a further confirmation that these are due to minority carrier (acceptor) traps which lie below mid-gap. Note that after oxidation these traps disappear, consistent with the C-V results in Fig. 12.

The fact that the conductance peaks in Fig. 13 do not shift in voltage with changes in frequency indicates that these peaks are due to discrete trap levels in the bandgap. One can estimate the energy and density of the major trap level at -4 V based on the results of Fig. 13. We will assume that this trap level is completely filled as a result of the illumination. For an interface state capacitance C_s, the conductance at the maximum is given by

$$G = \frac{C_s \omega^2 \tau}{1 + \omega^2 \tau^2} \qquad (1)$$

where τ is the reciprocal of the trap emission rate and ω is the signal frequency. Comparing the results at 1 kHz ($G = 45\ n\mho$) and 10 kHz ($G = 65\ n\mho$)

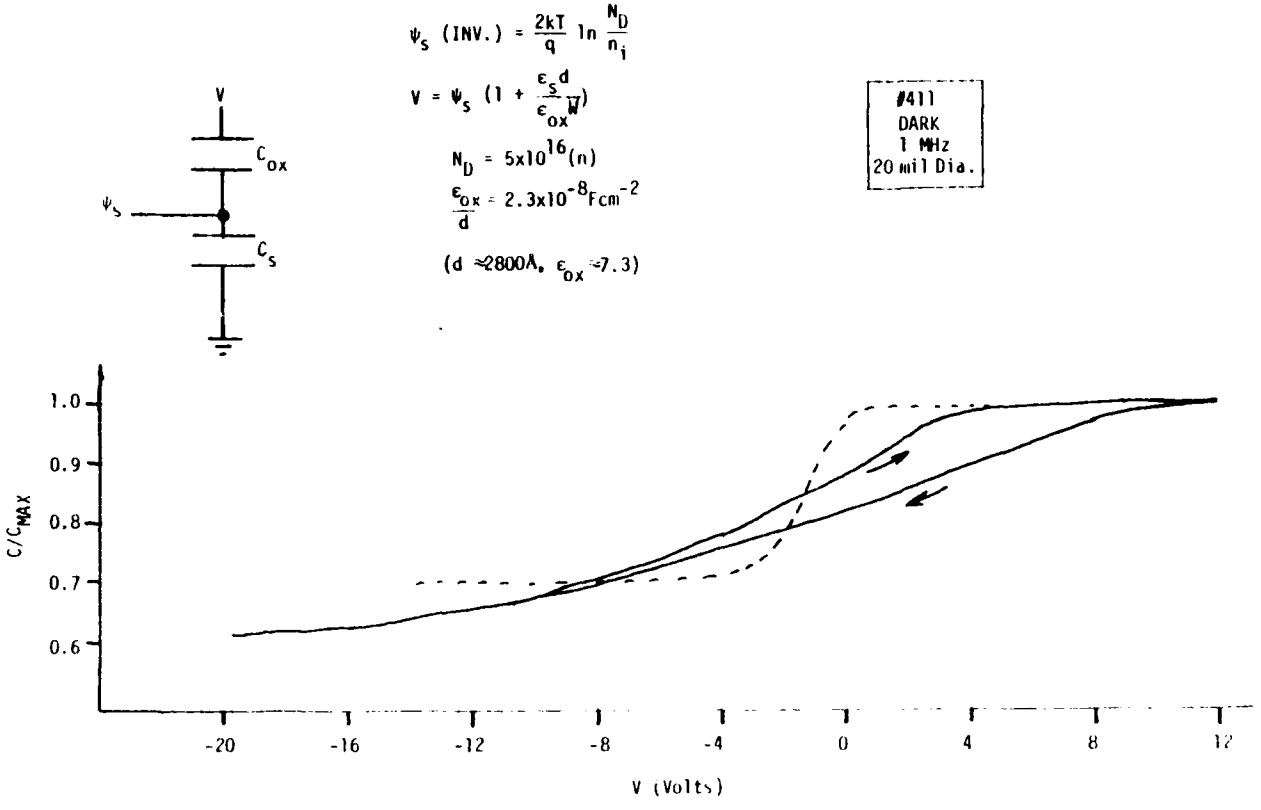


Fig. 10 Observed and ideal (dashed curve) C-V for sample #411.

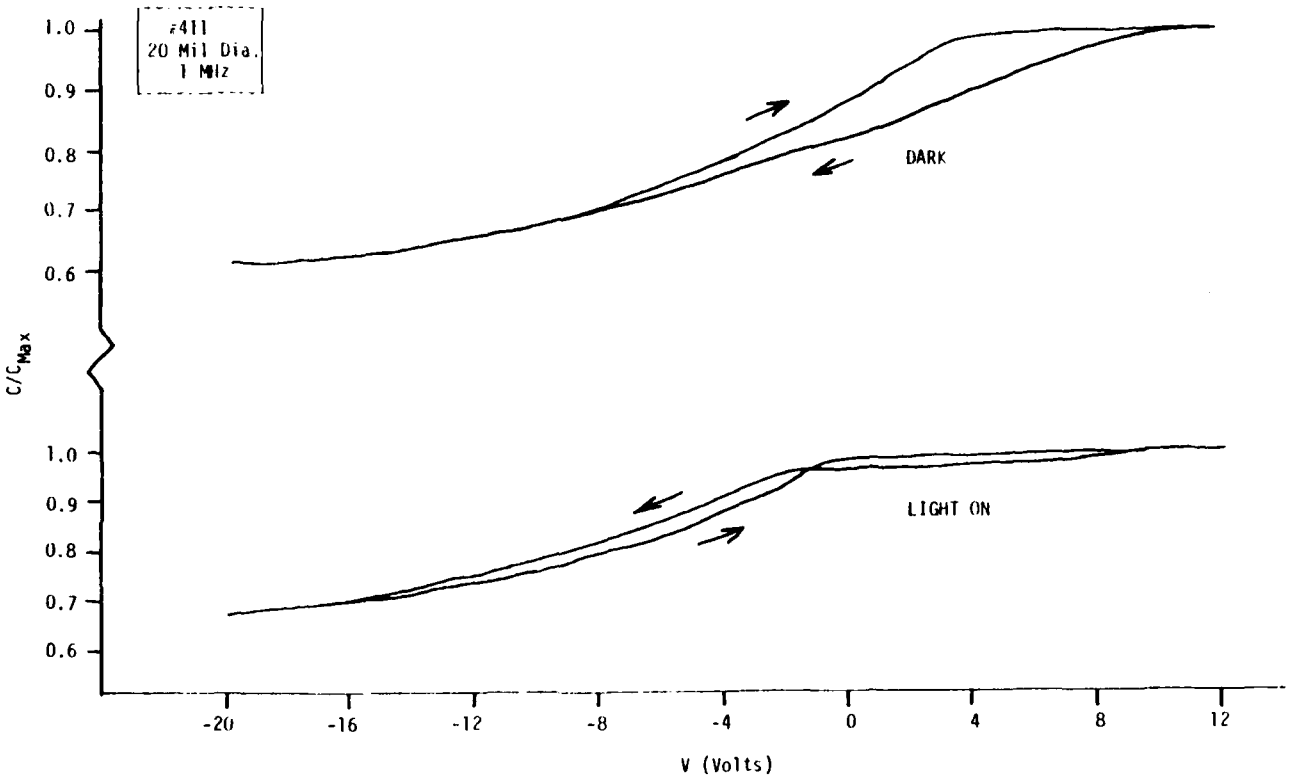


Fig. 11 Effect of illumination on C-V for sample #411.

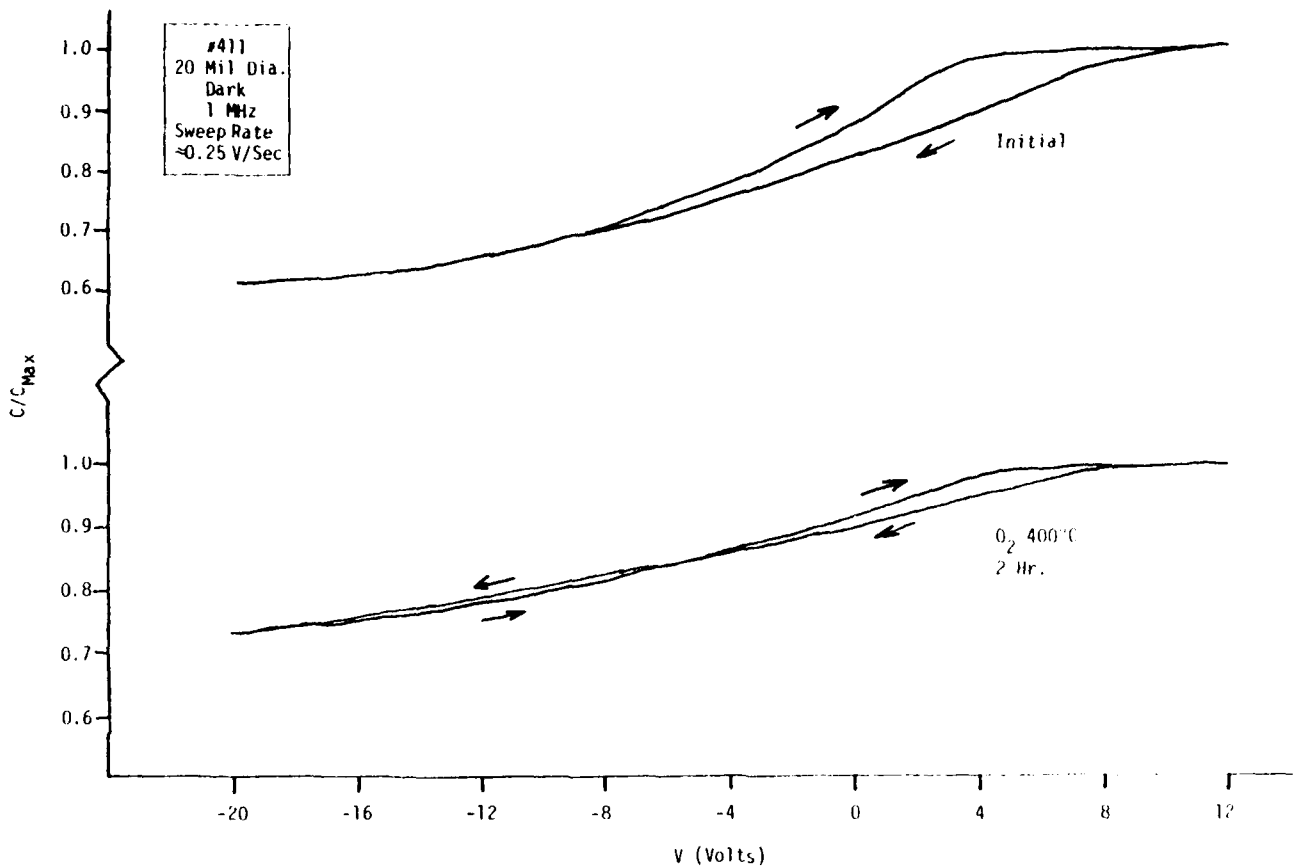


Fig. 12 Effect of subsequent oxidation on C-V for sample #411.

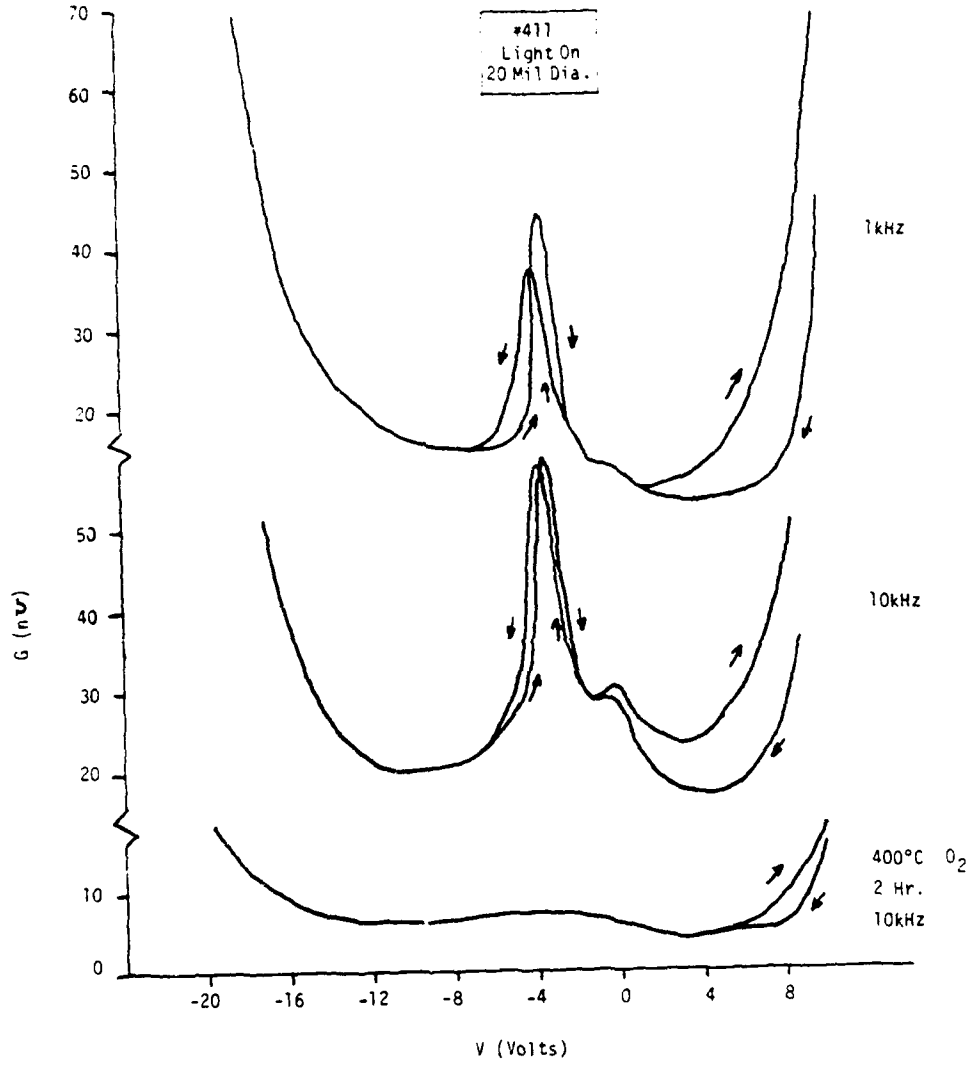


Fig. 13 G-V measurements for sample #411.

by using Eq. (1), we obtain a time constant of $\tau = 2.3 \times 10^{-4}$ s. The interface state density N_{ss} is given by

$$N_{ss} = \frac{C_s}{qA} \tag{2}$$

where A is the contact area. By using the calculated value for τ and the measured conductance in Eq. (1), C_s is found to be 15.3 pF, and hence from Eq. (2), $N_{ss} = 4.8 \times 10^{11}$ cm^{-2} eV^{-1}. An estimate of the trap energy can be made from the relation

$$E_a = \frac{kT}{q} \ln(N_v \bar{v} \tau \sigma_p) \tag{3}$$

where N_v is the valence-band density of states, $\bar{v}$ is the thermal velocity, and σ_p is the hole capture cross section. Assuming a typical value of $\sigma_p = 10^{-14}$ cm^2, E_a is estimated to be $\sim$ 0.4 eV above the valence band.

To assess the actual effect of the initial oxidation procedure applied to samples #411, 412, and 413, a piece of sample #411 was analyzed by sputter profiling in the SAM. Figure 14 shows the result of sputtering for 180 min. The sputter time axis is proportional to depth, with the sputter rate $\approx$ 30 Å/min.

From the sputter profile it is apparent that the initial oxidation procedure resulted in only a superficial AlAs oxidation, the top layer remained essentially pure AlAs. However, the sputter profile also reveals that the $Al_{1-x}Ga_xAs$ middle layer was graded in the desired manner, going from 100% Al to 50% Al at the GaAs interface. Thus as mentioned above, a portion of sample #411 was reoxidized at 400°C for 2 hrs in O_2 with the intent of

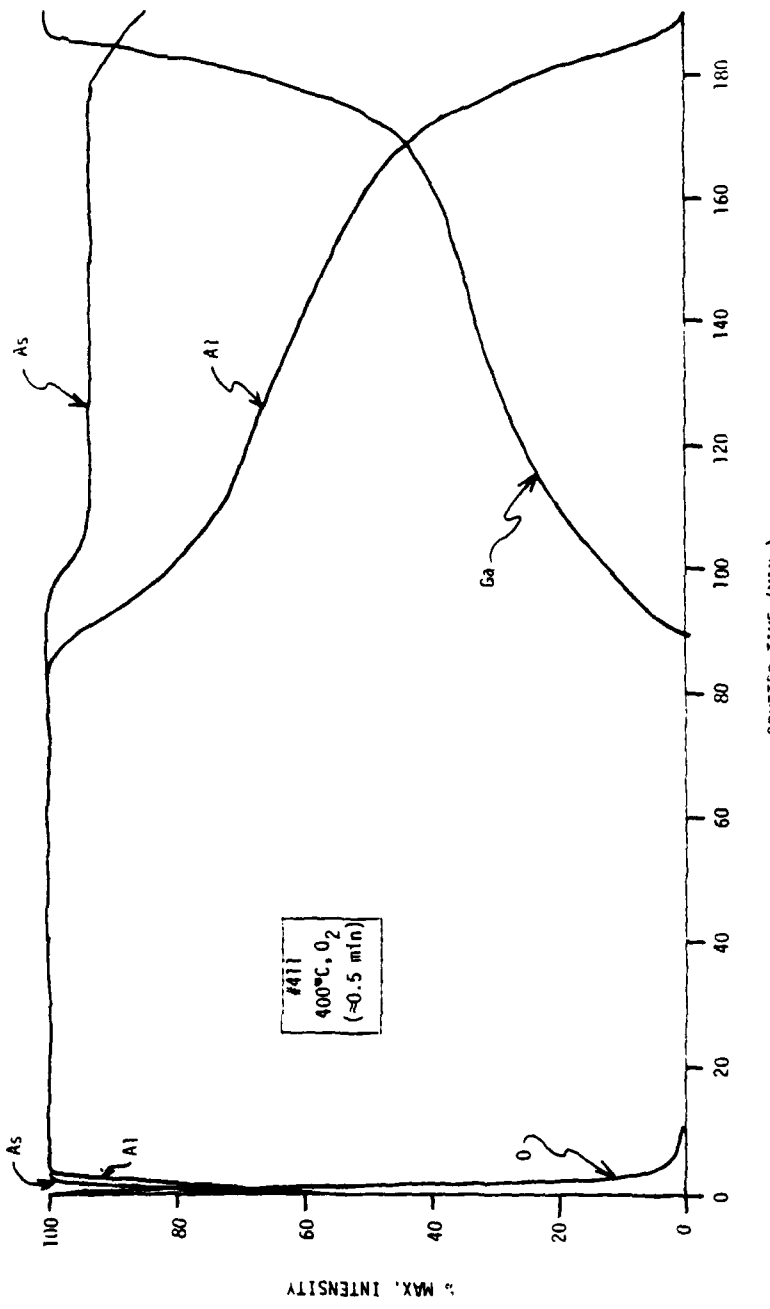


Fig. 14 Depth profile obtained with SAM after initial oxidation of sample #411.

increasing the oxide thickness. This procedure had a substantial effect on C-V and G-V results (Figs. 12 and 13).

An additional set of experiments was carried out on a portion of sample #411 (the sample had been stored in a vacuum box for ≈ 4 months prior to this set of experiments). The sample was oxidized sequentially for increasing lengths of time at 400°C in O_2 (a small O_2 flow was maintained during the oxidation). After each oxidation a row of 10 mil diameter metal dots was evaporated into the sample surface through a contact mask and C-V data were collected. The rationale behind this set of experiments was to correlate C-V results with depth of oxidation for a single sample in an attempt to move the oxide interface systematically through the $Al_{1-x}Ga_xAs$ layer. The total accumulated oxidation times were 10, 60, 330, 1575, and 10,455 min respectively. C-V measurements on the initial sample (this sample had been superficially oxidized for ≈ 0.5 min) showed considerable nonuniformity in behavior for different capacitors. A selected example is shown in Fig. 15a (top). For the other five series of experiments, the uniformity of characteristics was markedly better. In Fig. 15a (middle), a C-V measurement is shown following the 10 min oxidation. The "oxide" capacitance has increased substantially and there is a large hysteresis and shift of the flat-band voltage due to interface charge storage (the interface charge decreases noticeably after storage in the dark for many minutes). Figure 15a (bottom) is a C-V measurement after 60 min of oxidation. Little change in characteristics was observed as compared to the 10 min oxidation. It was observed that the charge storage effect could be "erased" by exposure to microscope light. Figure 15b (top) is a C-V measurement taken after 330 min of oxidation. Little change in the C-V characteristics was observed as compared to the previous 2 sets of measurements. It was observed that the flat-band voltage was nearly a linear function of forward-bias voltage applied to the sample. Figure 15b (bottom) is a C-V measurement obtained after 1575 min of oxidation. The C-V characteristics are similar to the results for the previous 3 sets of measurements, although an increase in oxide capacitance is observed which may be significant. Figure 15c shows C-V measurements obtained after

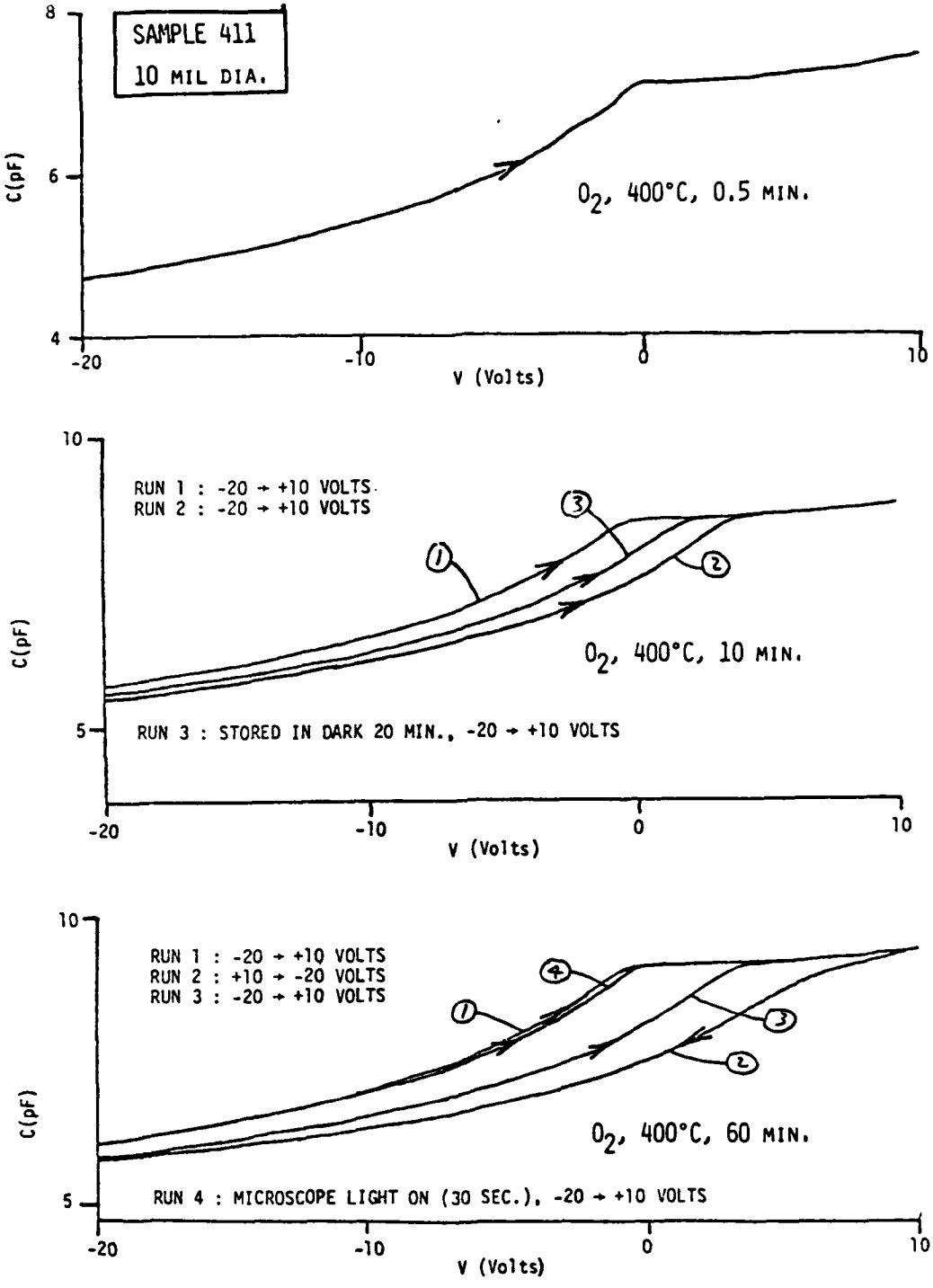


Fig. 15a C-V measurements for sample #411 after sequential oxidations, (top) 0.5 min oxidation, (middle) 10 min oxidation, (bottom) 60 min oxidation.

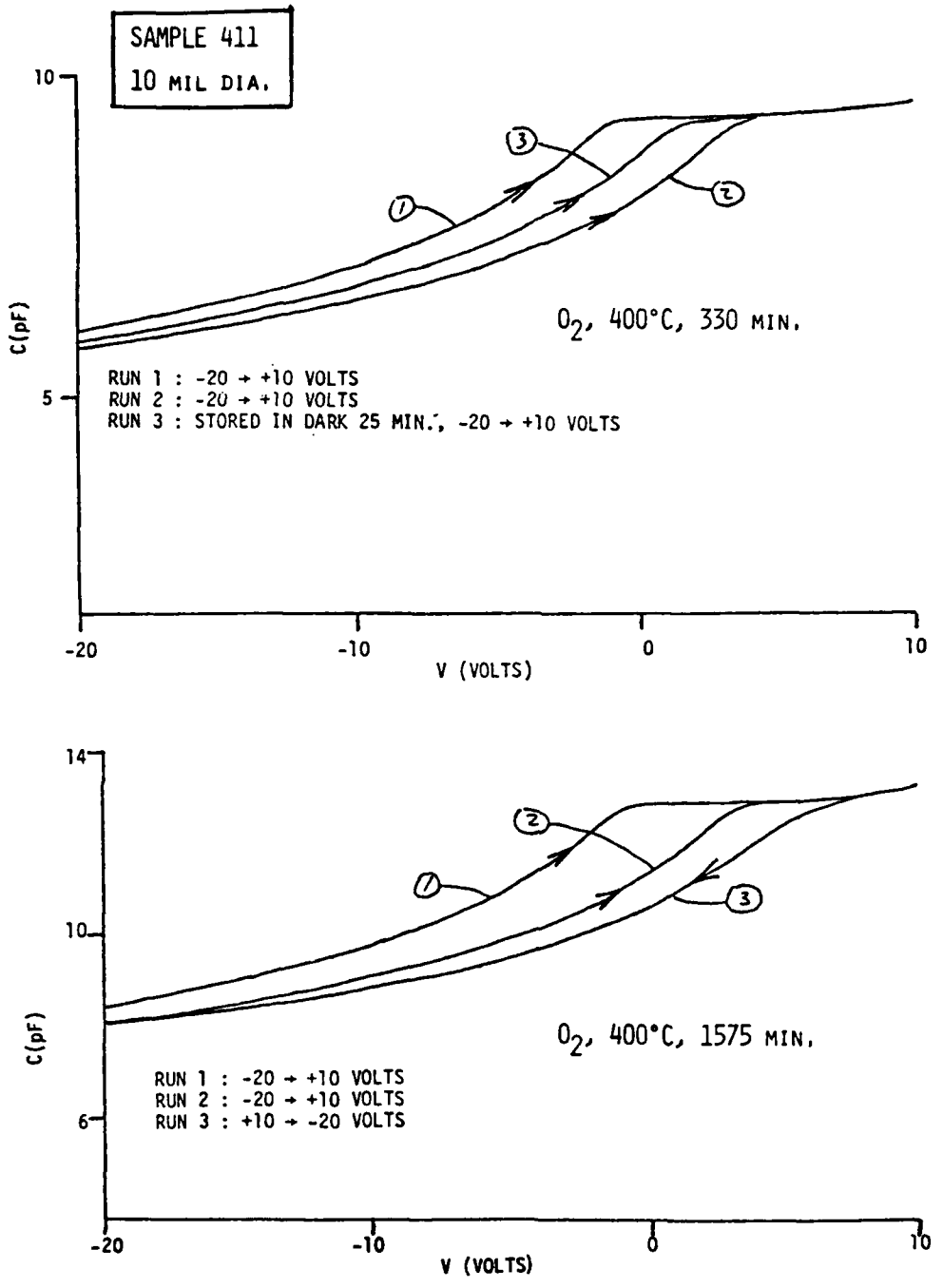


Fig. 15b C-V measurements for same sample as in Fig. 15a after sequential oxidations, (top) 330 min oxidation, (bottom) 1575 min oxidation.

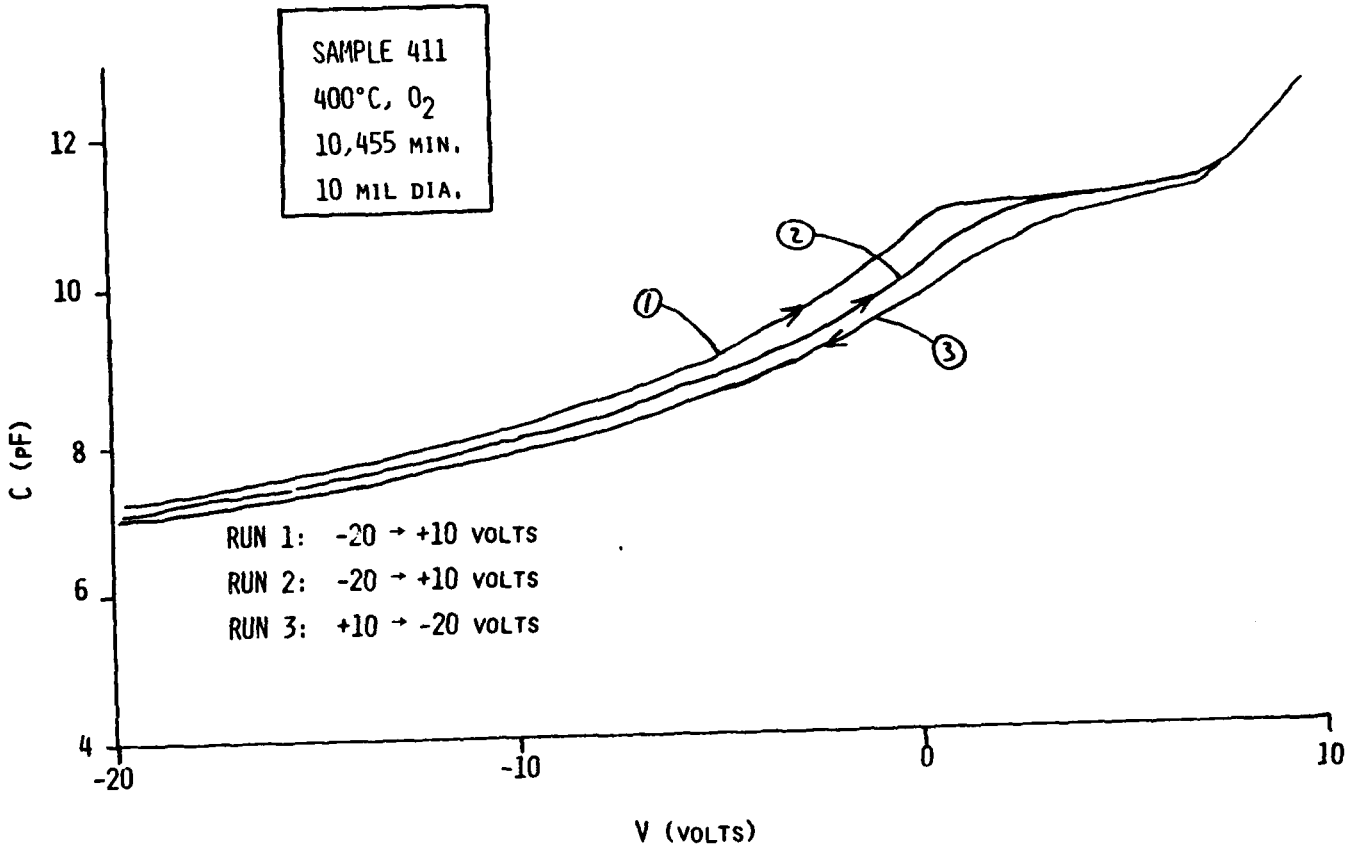


Fig. 15c C-V measurements for same sample as in Fig. 15a after 10,455 min oxidation.

10,455 min of oxidation. The devices after this amount of oxidation were considerably more leaky than the previous devices and forward breakdown occurred at ≈ 8 volts.

At the conclusion of this series of sequential oxidations carried out on sample #411, a SAM depth profile was obtained by a series of sputter-Auger analysis steps. The result of this Ar^+ sputtering depth profile is presented in Fig. 16. The sputter time axis of Fig. 16 is related to depth within the sample and the sputter rate is ≈ 20 Å/min. The graded $Al_{1-x}Ga_xAs$ layer is reached after sputtering ≈ 4×10^3 s while the GaAs layer is reached after ≈ 9×10^3 s of sputtering. The important result is that the oxygen signal extends all the way to the GaAs layer and seems to decrease at approximately the same rate as the Al signal. Therefore, after 10,455 min of oxidation, this sample appeared to be oxidized completely through the graded $Al_{1-x}Ga_xAs$ layer.

An XPS depth profile was also obtained on this same sample. Difficulties experienced in aligning the sputter crater and the x-ray beam made this profile a bit more difficult to interpret although the basic conclusions are the same as those drawn from the SAM profile (Fig. 16). The XPS data obtained within the graded $Al_{1-x}Ga_xAs$ layer showed that the Al was oxidized while the Ga was not oxidized. Although this result could be an artifact of the sputtering process our previous experience suggests that this explanation is unlikely.

Sample #491 (as was sample #411) was an attempt to reproduce the published C-V results of Ref. 4. C-V results for this sample are shown in Fig. 17. The data are reminiscent of data taken for sample #411. There is a large hysteresis which depends on the direction of the scanning voltage. This hysteresis is consistent with charge storage at the interface and has been discussed above. The effect of a longer oxidation anneal is shown in the figure. There is only a small change between a 200 min and a 1040 min oxidation which indicates a slightly thicker insulator for the longer oxidation.

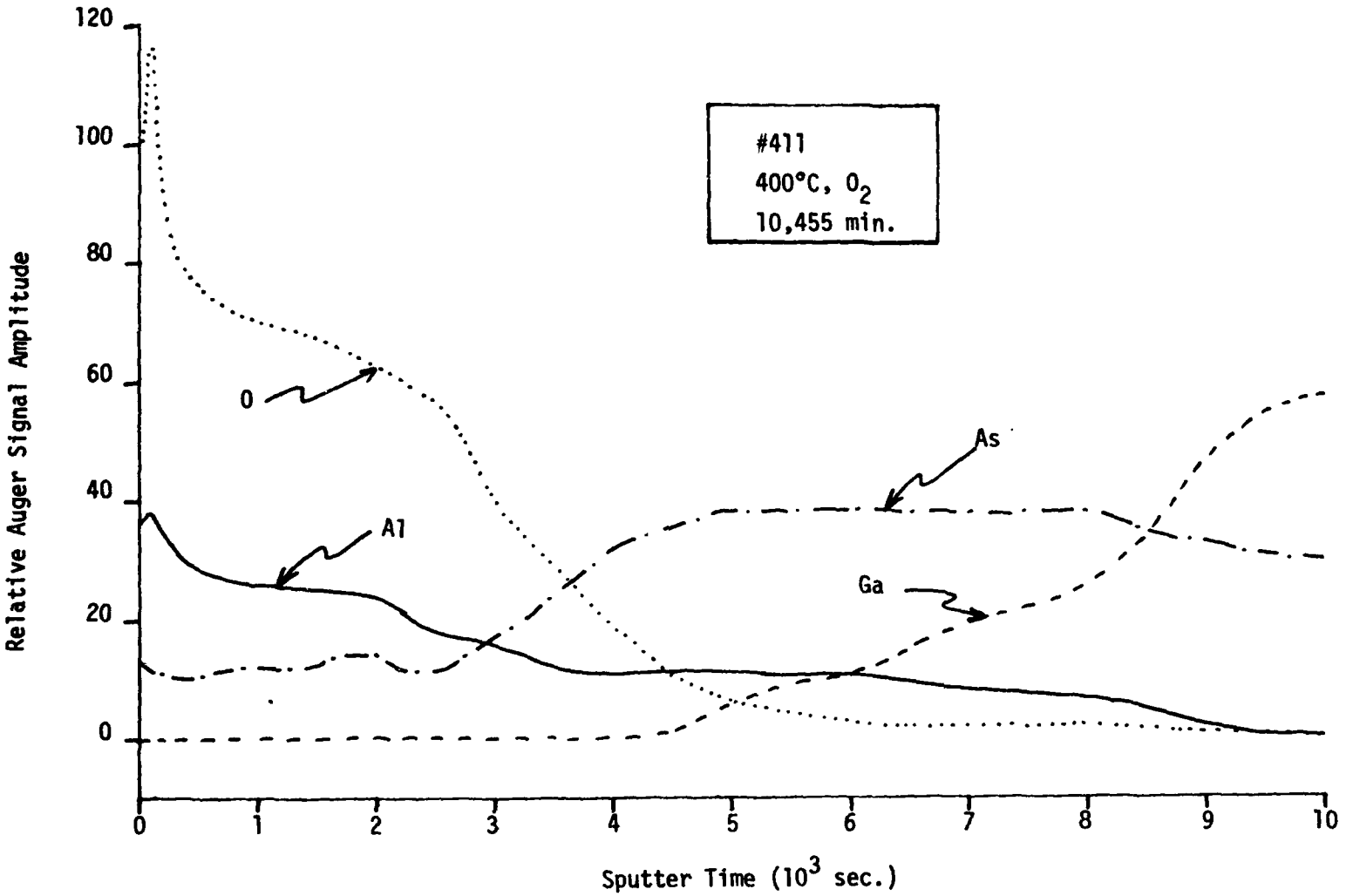


Fig. 16 Depth profile obtained with SAM for sample #411 after oxidation in O_2 at 400°C for 10,455 min.

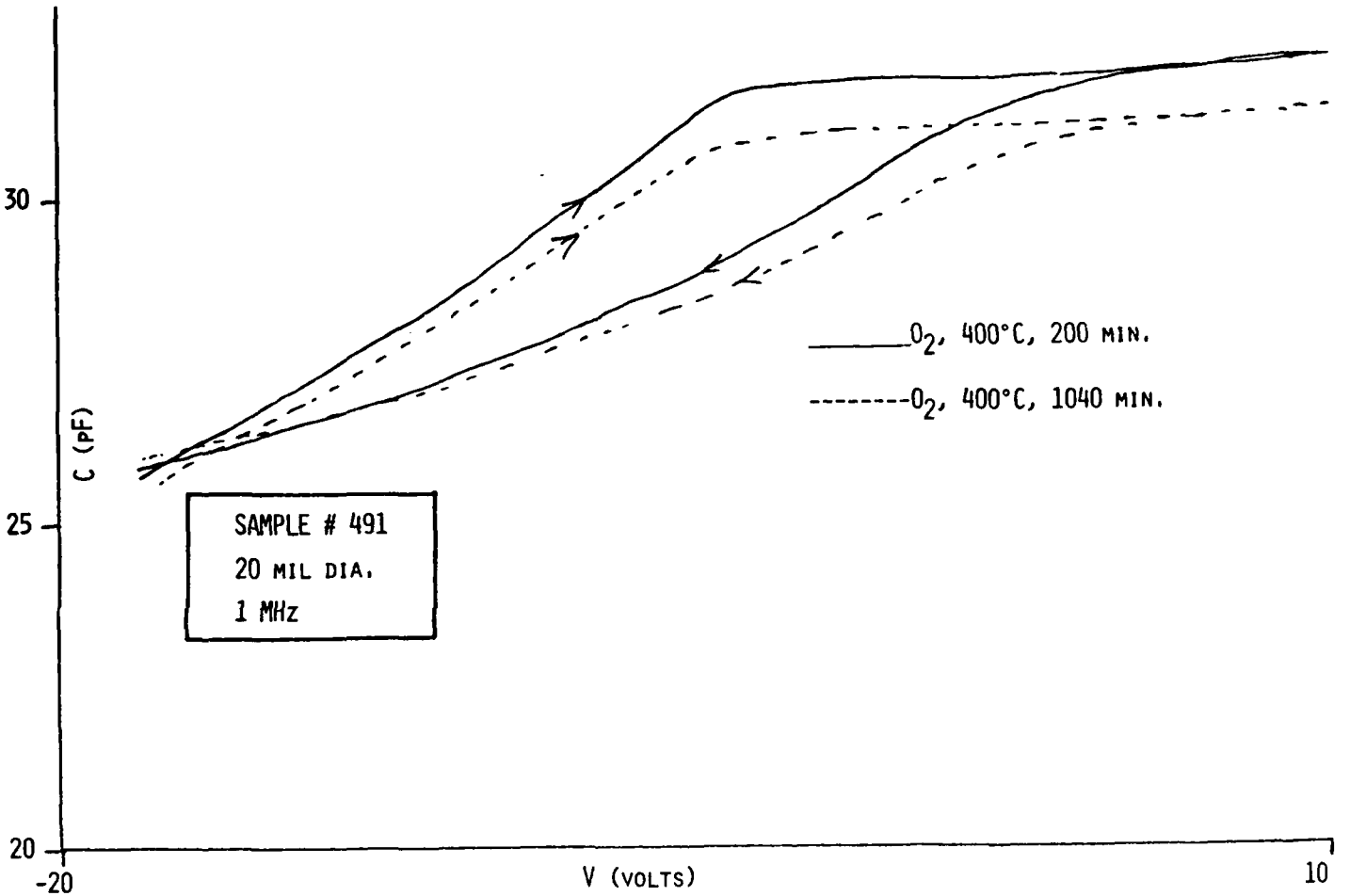


Fig. 17 C-V measurements for sample #491.

These results indicate a complete oxidation of the AlAs and suggest that a significant portion of the $Al_{1-x}Ga_xAs$ is also oxidized under these conditions.

The I-V measurements for sample #491 with a 200 min oxidation indicate a leakage current of 10^{-9} amps at 6 volts forward bias for a 20 mil dia. dot. The thickness of the insulating layer is not known but can be estimated to be in excess of 2000 A.

b. p-Type Samples

As discussed in Section III 1, the larger conduction-band discontinuity for $Al_{1-x}Ga_xAs$/GaAs heterojunctions as compared to the valence-band discontinuity suggests that it might be easier to invert p-type structures rather than n-type. Samples #490 and 493 were prepared to test this idea.

The C-V characteristics for sample 490 are indicated in Fig. 18. Although at first glance the sample appears to be going into inversion, further analysis has shown that a more likely explanation is that the sample has depleted through to the substrate. Such an interpretation was shown to be correct by analyzing the C-V characteristics for a device with the thermal oxide removed and a contact to the $Al_{1-x}Ga_xAs$ epilayer. The device was very leaky but yielded a capacitance consistent with the width of the GaAs layer.

Sample #493 was similar to #490 but with a thicker, more heavily doped GaAs layer. C-V measurements are shown in Fig. 19. There is a small flat-band voltage shift of -0.6 volts for these samples which indicates a positive interface charge. The samples show a small amount of hysteresis but do not give any indication of inversion. The I-V curves indicate breakdown at very low forward voltages of about -2 to -4 volts. Typically for a forward voltage of -2 volts, currents of 3×10^{-8} amps are observed for a 20 mil diameter device. The thickness of the insulator is not known with great certainty.

To summarize Section IV 1, we have been unable to reproduce the promising C-V results reported in Ref. 4. Sample #493 shows the most satisfactory C-V curves, showing minimal hysteresis compared to the other structures. A

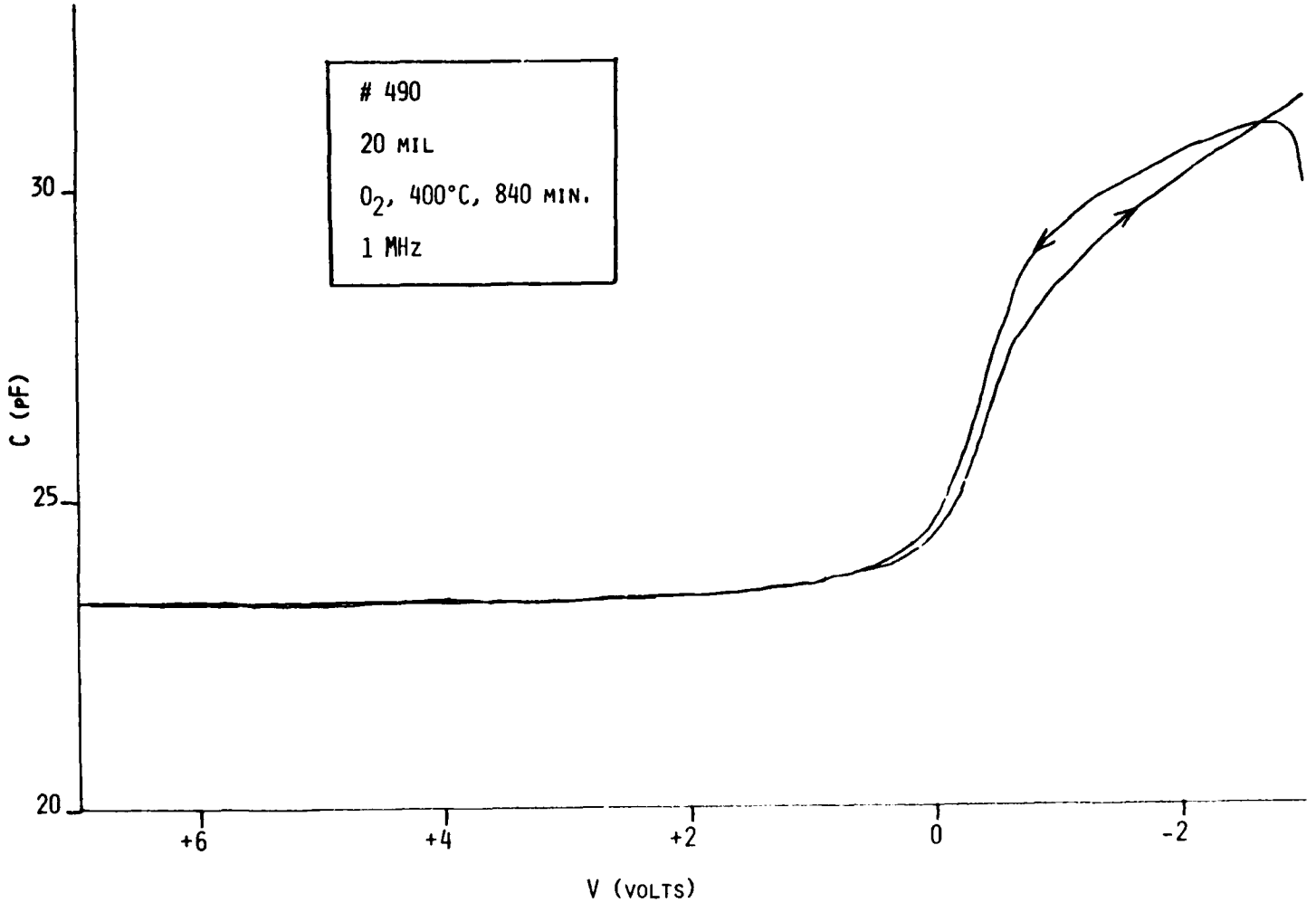


Fig. 18 C-V measurements for sample #490.

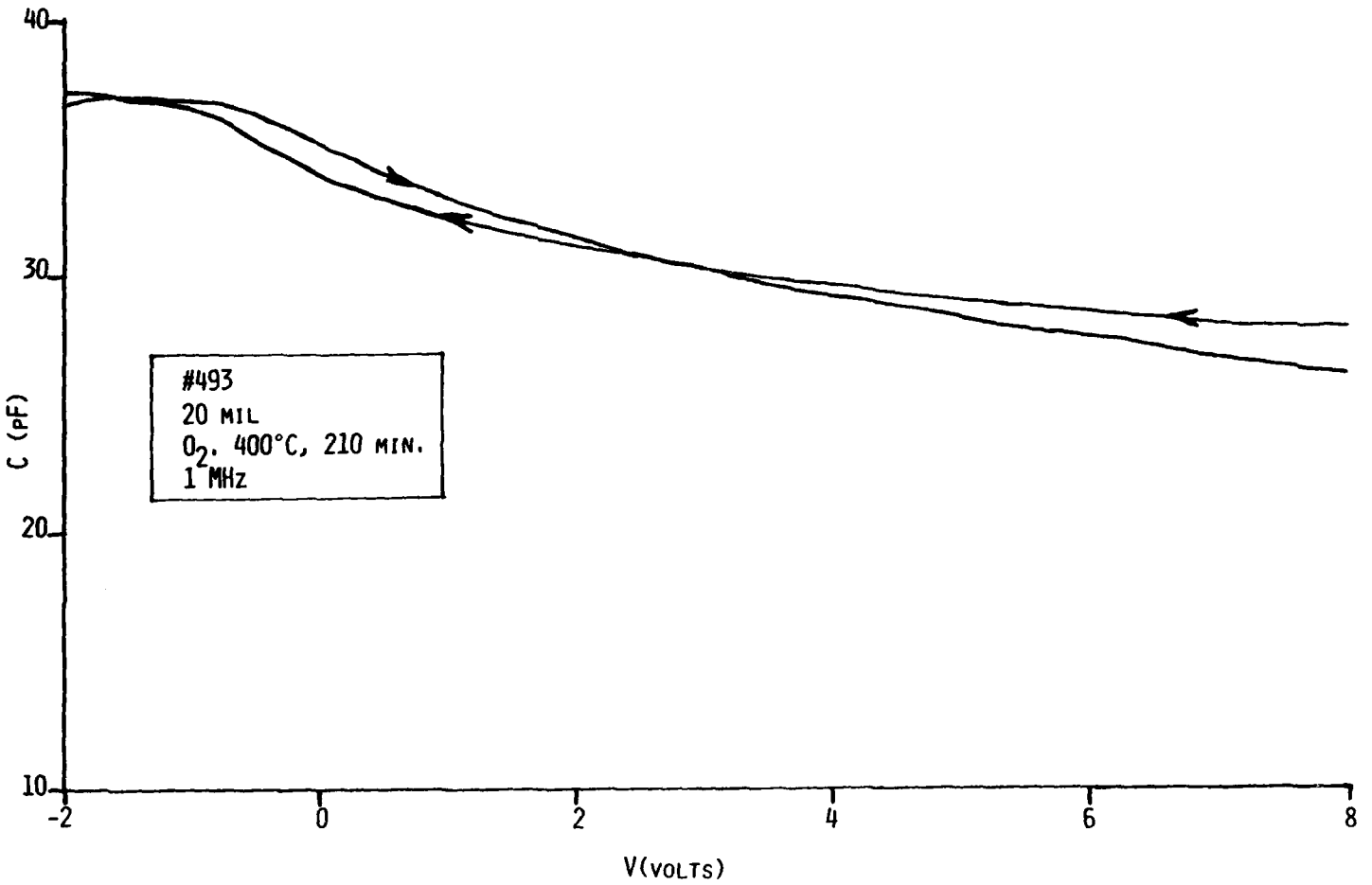


Fig. 19 C-V measurements for sample #493.

persistent problem with the devices discussed in Section IV 1 is that the thermal oxide is very leaky, which may effectively prevent inversion in any of the devices. In the next two sections the use of various other insulators as a substitute for the thermal oxide is discussed.

2. Plasma Oxidation

The dielectric formed by thermal oxidation of $Al_{1-x}Ga_xAs$ was found to be leaky and subject to breakdown making interpretation of the C-V measurements difficult. A dielectric with better insulating properties was needed. As a result we developed and investigated the properties of plasma oxidized GaAs surfaces for this purpose. Plasma oxides have been reported with relatively low interface state densities and low leakage currents.[13]

Plasma oxides were grown in a modified LFE PDS/PDE301 barrel etcher. Oxygen gas flowed through the etcher so that the net pressure ranged from 1 to 5 torr. A discharge was provided by an rf generator with a power of 100-300 watts. The sample was placed on an electrically grounded aluminum plate. No oxide growth was observed on an insulating plate. It was found that the rate of oxide growth was only weakly dependent on substrate bias but was strongly dependent on sample temperature and consequently on rf induced heating. The thickness of the film was generally self-terminating between 1000 Å and 2000 Å as determined by color charts previously published.

Oxide films formed in this manner had low leakage (less than 10^{-10} amps for 2×10^{-3} cm^2 area at 10 V forward bias for films ~ 1000 Å thick. Under these conditions the current in thermally oxidized samples was normally $> 10^{-6}$ amps.

The plasma oxidation technique described here was used on sample #412. The AlAs layer was removed on this sample leaving a layer of $Al_{0.5}Ga_{0.5}As$ on the n-type GaAs. The surface was plasma oxidized producing a highly resistive oxide layer on the remaining $Al_{0.5}Ga_{0.5}As$ layer. C-V curves for this structure are shown in Fig. 20. The device shows large hysteresis (~ 4 V) and a large flatband voltage shift like that observed for the thermally

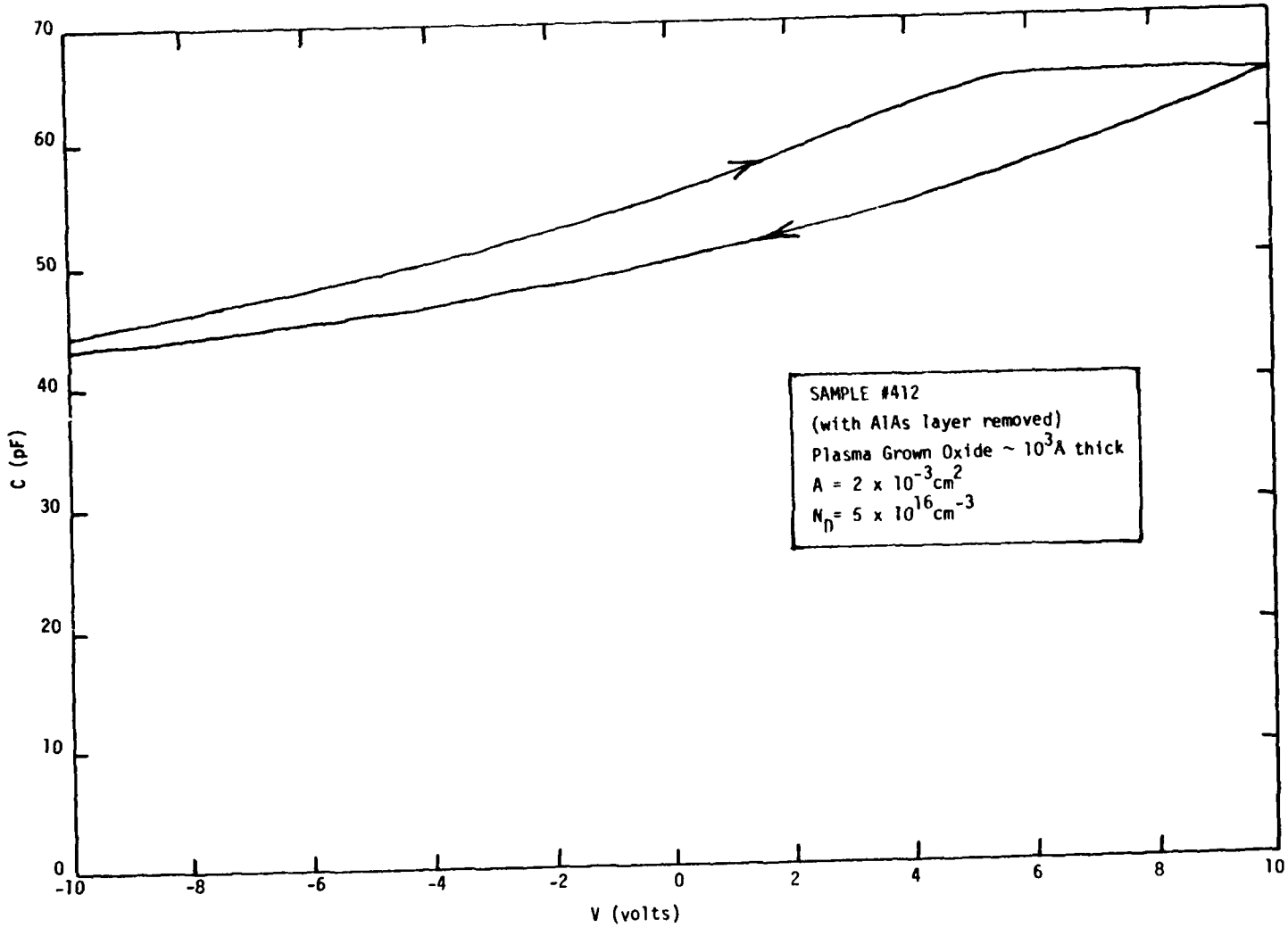


Fig. 20 C-V for plasma-grown oxide on sample #412 (which had AlAs layer removed).

oxidized devices. We do not see any indication of inversion but rather a deep depletion curve.

Such results indicate a large density of states ($\approx 10^{12}$ cm^{-2}) at one (or both) of the interfaces in this system. The interface between the plasma oxide and the $Al_{1-x}Ga_xAs$ is the likely site for these states as the $Al_{1-x}Ga_xAs$-GaAs interface should be relatively defect free. Annealing in N_2 did not change the C-V curves appreciably but did result in an increase in the leakage current through the oxide.

3. Deposited Insulators

An effort was also made to improve the insulating properties of the dielectric on metal-insulator-$Al_{0.5}Ga_{0.5}As$-GaAs structures by using deposited insulators. In this section we describe results obtained with plasma CVD deposited $Si_xO_yN_z$ and evaporated Ta_2O_5.

a. $Si_xO_yN_z$

The LFE PDS/PDE plasma etcher was modified to be compatible with either plasma oxidation or with $Si_xO_yN_z$ growth. $Si_xO_yN_z$ films were formed by leaking 1% silane diluted by argon into the discharge of an ambient gas which was either high purity nitrogen, forming gas (10% H_2, 90% N_2) or ammonia. Similar results were obtained for all three gases. The power dissipated during the discharge was typically 100-300 watts. The partial pressures used were typically 2-10 torr for the SiH_4 + Ar mixture and 1-3 torr for the forming gas, nitrogen, or ammonia. The growth rate was very sensitive to the partial pressure of the silane mixture. Films obtained from this system have very low leakage currents typically less than 10^{-9} amps at 10 V across a 1000 A thick film in a MIS capacitor with an area of 2×10^{-3} cm^2.

Figure 21 compares the I-V curves for three deposited insulators from our laboratory. These are sputtered SiO_2, sputtered Si_xN_y, and the plasma CVD $Si_xO_yN_z$. The SiO_2 films (~ 1000 A thick) are quite leaky compared to the Si_xN_y films shown in the figure. Although it is difficult to compare the

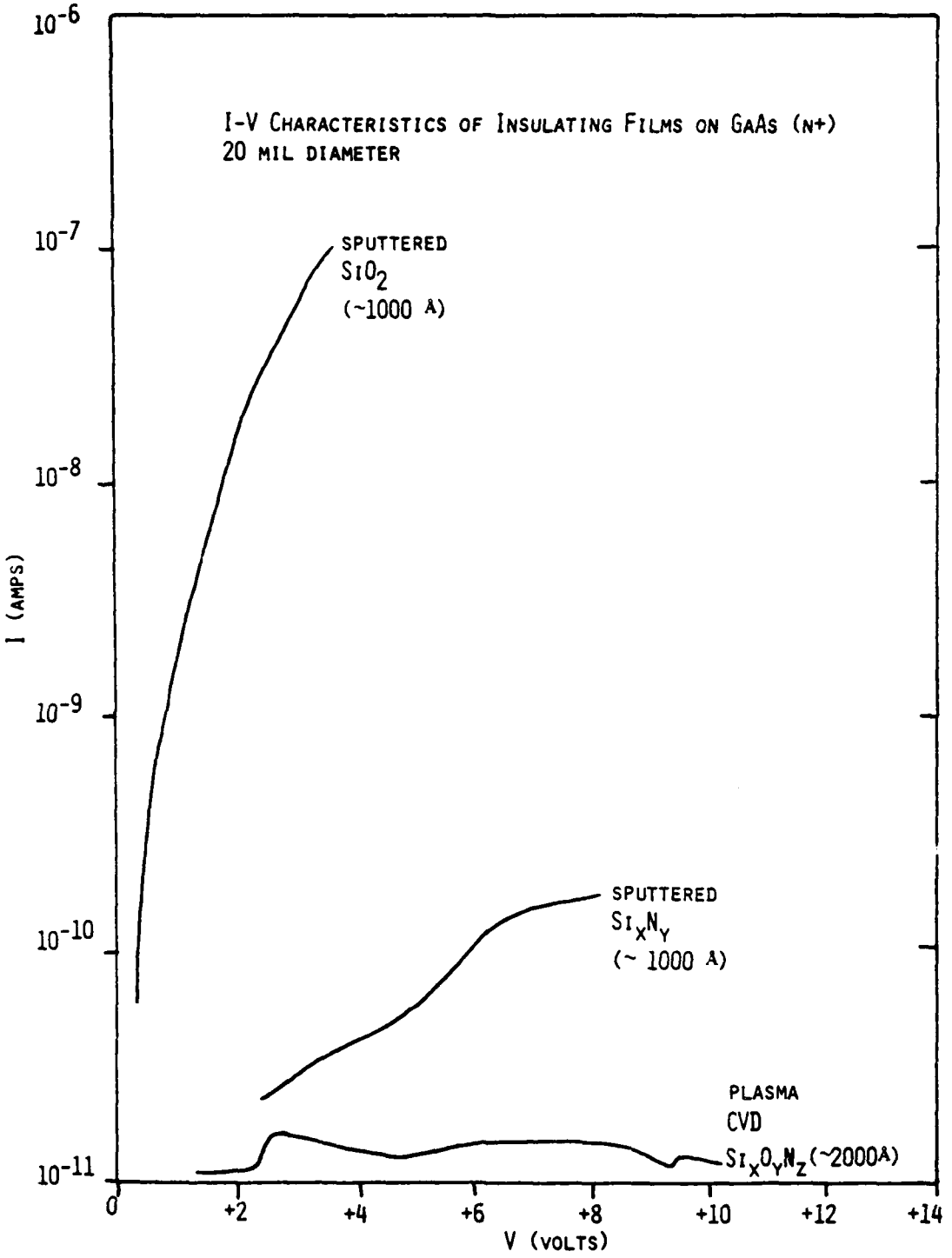


Fig. 21 Comparison of I-V characteristics for sputtered SiO_2, sputtered Si_xN_y, and the plasma CVD $Si_xO_yN_z$ insulators deposited on GaAs (n^+).

sputtered Si_xN_y film with the plasma CVD $Si_xO_yN_z$ film because they have different thicknesses, the sputtered film appears to show greater leakage. The current levels in the plasma CVD $Si_xO_yN_z$ are near the sensitivity limit of the instrument. Thus the plasma CVD $Si_xO_yN_z$ film appears to be the best insulator of those investigated.

Samples #491 and #493 were covered with a thin layer of $Si_xO_yN_z$. C-V curves for these samples gave the same flatband voltages and hysteresis characteristically observed with the thermal oxide. This apparently resulted from a layer of oxidized AlAs or $Al_{1-x}Ga_xAs$ at the interface.

b. Ta_2O_5

In another effort to improve the insulating properties of the dielectric on metal-insulator-$Al_{0.5}Ga_{0.5}As$-GaAs structures, Ta_2O_5 was evaporated onto sample #412. The top AlAs layer was removed before the Ta_2O_5 was deposited. The resulting structure was metal-Ta_2O_5-$Al_{0.5}Ga_{0.5}As$-GaAs (n-type). C-V curves for this device are shown in Fig. 22. Initially the device exhibits a low (< 1 V) flatband voltage which indicates little interface charge. On successive scans, the apparent interface charge builds up as indicated by the shift in flatband voltage to successively higher values. When the bias voltage reverses, depletion occurs immediately which indicates that the charge is trapped at the interface.

This behavior is consistent with results that were reported above for this sample. Since the charge storage seems to be at the $Al_{1-x}Ga_xAs$-insulator interface, the reduction of this storage is a necessary prerequisite for good MIS devices.

The results of this section and the previous one (IV 3a), suggest that the inherent problem of having a large density of interface states may not be removed by the two insulator approach. The problems associated with the large density of interface states may be transferred away from the GaAs-oxide interface to a region in the dielectric (the $Al_{1-x}Ga_xAs$-oxide interface). As a result it may be still difficult to change the interface

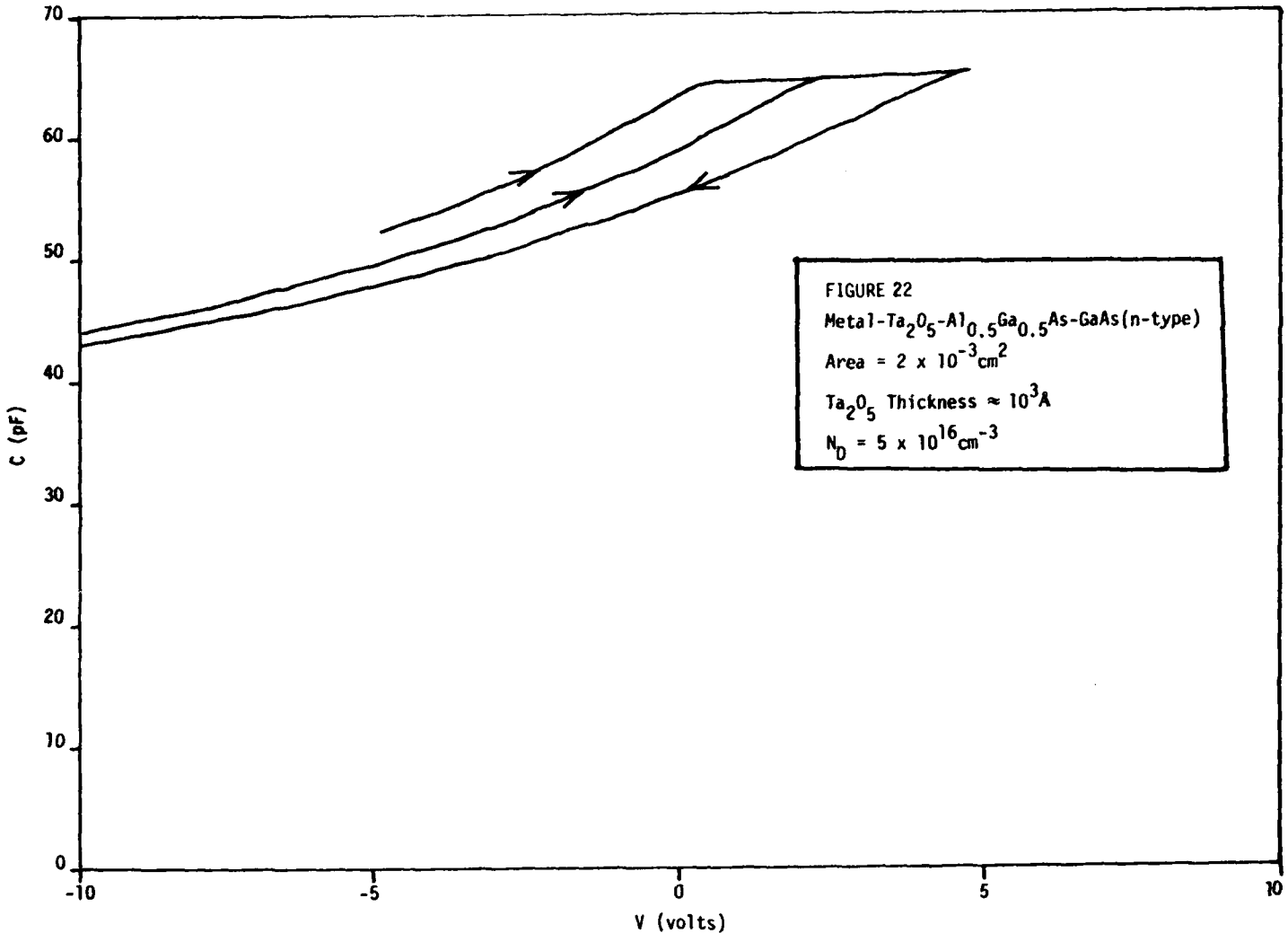


Fig. 22 C-V measurements for sample prepared by evaporating Ta_2O_5 onto sample #412 after top AlAs layer was removed.

potential and large hysteresis due to charge transfer between these states and the GaAs may be still observed.

4. Discussion of Previous MBE Results

In view of our (and others)[14] difficulty in reproducing the C-V results for the MBE grown structures reported in Ref. 4, we have re-examined the published data and find some apparent internal inconsistency. In Fig. 23 the published C-V data of Tsang et al[4] is reproduced. Additional stated parameters are: 2×10^{-3} cm^2 Au dot, $C_i = 3.7 \times 10^{-8}$ F/cm^2, $N_D = 8 \times 10^{16}$ cm^{-3}, where C_i is the measured insulator capacitance and N_D is the active GaAs layer doping. Since the data look very close to an ideal C-V curve, we will use only the elementary analysis applicable to an ideal MOS structure. For example, at inversion, the data show $C/C_i = 0.7$, where C is the total MOS capacitance. This immediately implies that at inversion the capacitance of the semiconductor is:

$$C_S^{inv} = \frac{(\frac{C}{C_i})}{1 - (\frac{C}{C_i})} C_i = \frac{0.7}{0.3} C_i = 8.6 \times 10^{-8} \text{ F/cm} \quad . \tag{4}$$

For a semiconductor, the AC capacitance at inversion is:

$$C_S^{inv} = \epsilon_S / W_m \tag{5}$$

where W_m is the depletion width and $\epsilon_S = 1.11 \times 10^{-12}$ F/cm^2, the dielectric constant for GaAs. Thus, $W_m = 1.11 \times 10^{-2}/8.6 \times 10^{-8} = 1.29 \times 10^{-5}$ cm = 1290 A is the measured value for W_m.

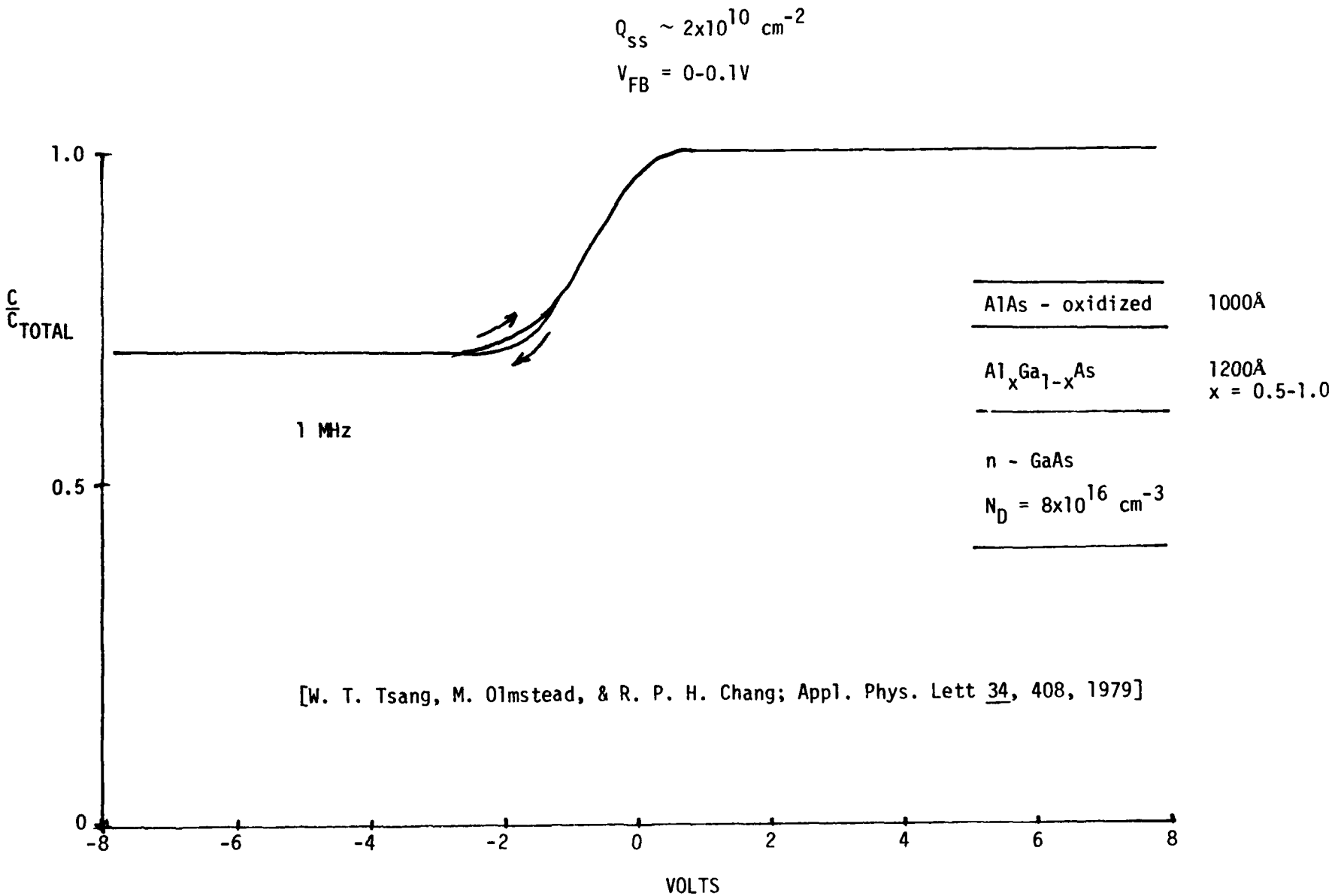


Fig. 23 C-V measurements for thermally oxidized MBE grown sample of AlAs/graded $Al_xGa_{1-x}As$/GaAs replotted from Ref. 4.

This value for W_m must be consistent with:

$$W_m = (2\varepsilon_S V_S^{inv}/qN_D)^{1/2} \tag{6}$$

which is the depletion width at inversion as a function of doping. For GaAs, $V_S^{inv} \sim 1.4$ V, thus,

$$N_D = 2\varepsilon_S V_S^{inv}/qW_m^2 = 1.13 \times 10^{17}\ cm^{-3} \tag{7}$$

is the actual measured value for N_D. This is consistent with the stated value of $8 \times 10^{16}\ cm^{-3}$.

The other parameter directly available from Fig. 23 is the gate voltage, V_g, at inversion, which is measured as ~ 2.1 V. This value of V_g should be compatable with:

$$V_g = (Q_B/C_i) + V_S^{inv} \tag{8}$$

which states that the voltage across the insulator and semiconductor equals the gate voltage at inversion, $Q_B = (2\varepsilon_S qN_D V_S^{inv})^{1/2} = 2.3 \times 10^{-7}\ coul/cm^2$. Thus $(Q_B/C_i) = 6.3$ V (5.4 V for the quoted $8 \times 10^{16}\ cm^{-3}$ doping). In the absence of significant interface charge, which the data show to be the case, this simple analysis indicates that although the capacitance values measured for "flatband" and "inversion" are consistent with the stated oxide thickness and n-type layer doping, the gate bias at inversion should be ~ 7 V rather than the ~ 2V shown. Interface charge would increase V_g, thus our calculated V_g is a minimum value. We presently have no explanation for the low gate voltage at inversion shown in the data of Fig. 23.

V. INSULATORS DEPOSITED ON GaAs IN XPS SYSTEM

In parallel with the effort to utilize $Al_{1-x}Ga_xAs$/GaAs interfaces in MIS structures (as described in Section IV), a second approach to form MIS structures with deposited insulators on GaAs was also pursued. These deposited insulator studies are documented in Sections V, VI, and VII. In this Section (V) insulators which were deposited onto GaAs substrates within the UHV XPS sample preparation chamber are discussed; these studies made use of XPS for interface and insulator composition analysis.

1. SiO_x Evaporation

Ten MIS samples which utilized bulk grown GaAs (100) substrates were prepared by SiO_x evaporation within the UHV sample preparation chamber of the XPS system. Investigations of these samples are discussed in this Section (V1). The ten samples were prepared in sets of two during five independent experiments. The five sets of samples are identified as X1 through X5. For each preparation, one n($\approx 1 \times 10^{17}$ cm^{-3}) and one p($\approx 2 \times 10^{16}$ cm^{-3}) sample were prepared. The initial surface treatments were chosen to produce surfaces which had either a few monolayers of Ga_2O_3 present or were clean (prepared by heating the samples to $\approx$ 560°C) as monitored by XPS. Surfaces of these two types are known to have substantially different surface potentials.[2]

The insulator was prepared by evaporating SiO_x onto the sample surfaces within the XPS sample preparation chamber. In most cases the samples were at room temperature, however for sample "X2" the sample was at $\approx$ 460°C. As discussed in the next paragraph, the composition of the insulator, as determined by the Si^{4+}/reduced Si ratio, could be varied substantially by changing the ambient for the SiO_x deposition. In Table 2, the initial surface preparation conditions, the ambient condition during the SiO_x deposition, and the insulator composition as determined by XPS analysis are summarized for samples X1 through X5.

Table 2

Deposited SiO_x Experiments

Sample No.	Surface Preparation	SiO_x Deposition Conditions	Insulator Composition
X1	Thermally Cleaned 6×10^4L O_2 at ≈ 460°C Stored in Vac. 9 hrs.	Vacuum Evaporation Sample at R.T.	Reduced Si Present
X2	Heated to ≈ 460°C to Form Ga_2O_3	3×10^{-5} torr O_2 UV Sample at ≈ 460°C	Small but Detectable Amount of Reduced Si
X3	Thermally cleaned 6×10^4L O_2 at ≈ 460°C	3×10^{-5} torr O_2 UV Sample at R.T.	No Reduced Si Detected
X4	Heated to ≈ 460°C to Form Ga_2O_3	3×10^{-5} torr O_2 UV Sample at R.T.	No Reduced Si Detected
X5	Thermally Cleaned	1×10^{-4} torr O_2 UV Sample at R.T.	No Reduced Si Detected

During the course of these experiments it was observed by XPS that the composition of the deposited SiO_x could be varied substantially by changing the ambient. In Fig. 24 an XPS spectrum of SiO_x evaporated in vacuum is shown. The figure illustrates the elemental purity of the insulator as only photoelectron lines associated with Si2p (binding energy ≈ 100 eV), Si2s (≈ 150 eV), O1s(≈ 530 eV) and an oxygen Auger line at ≈ 980 eV are visible. At the top of Fig. 25 an XPS spectrum in the binding-energy region of Si2p is shown for the SiO_x starting material (before evaporation). By using the chemical shift scale of Adachi and Helms,[15] the major Si2p peak is identified as

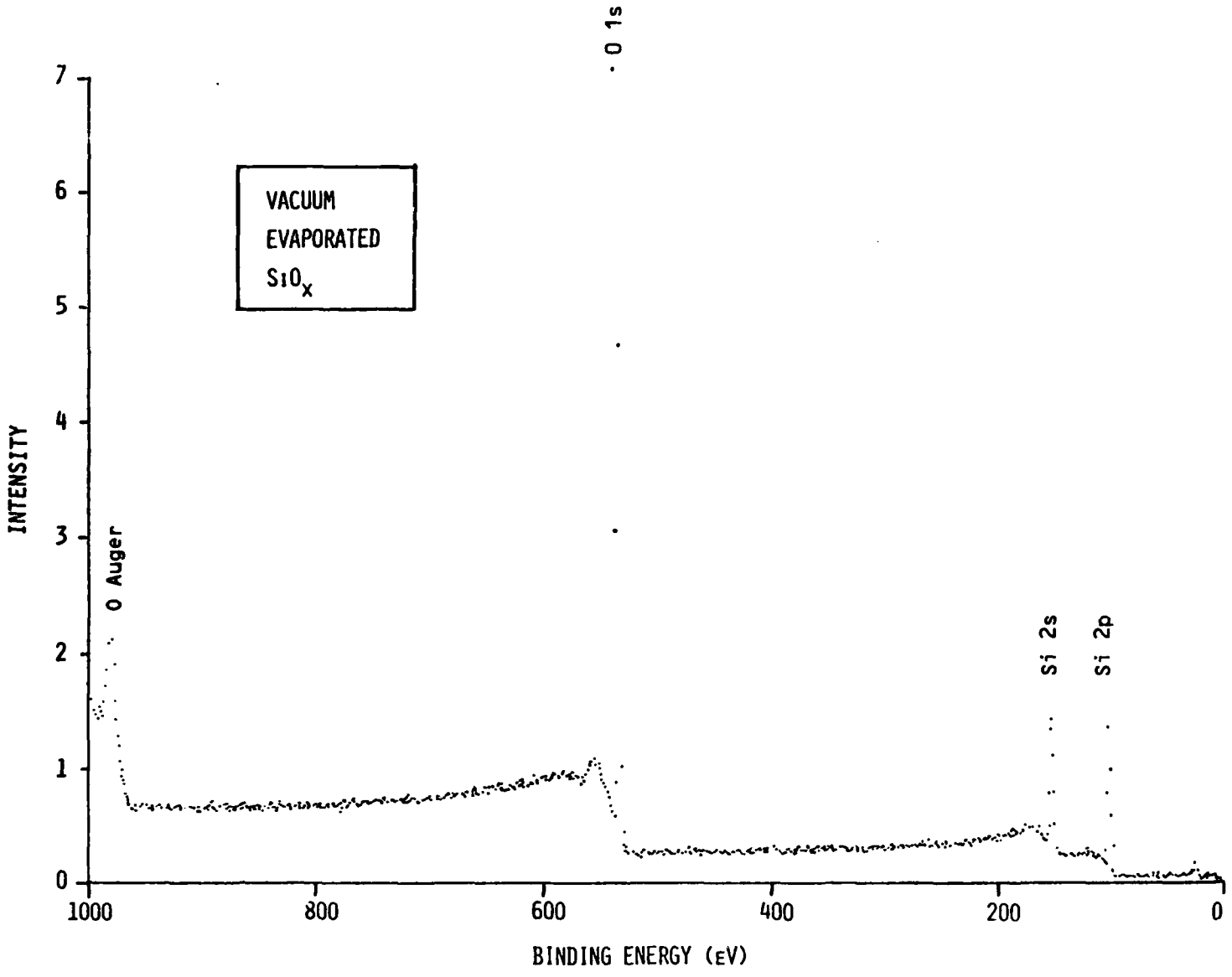


Fig. 24 XPS spectrum of evaporated SiO_x.

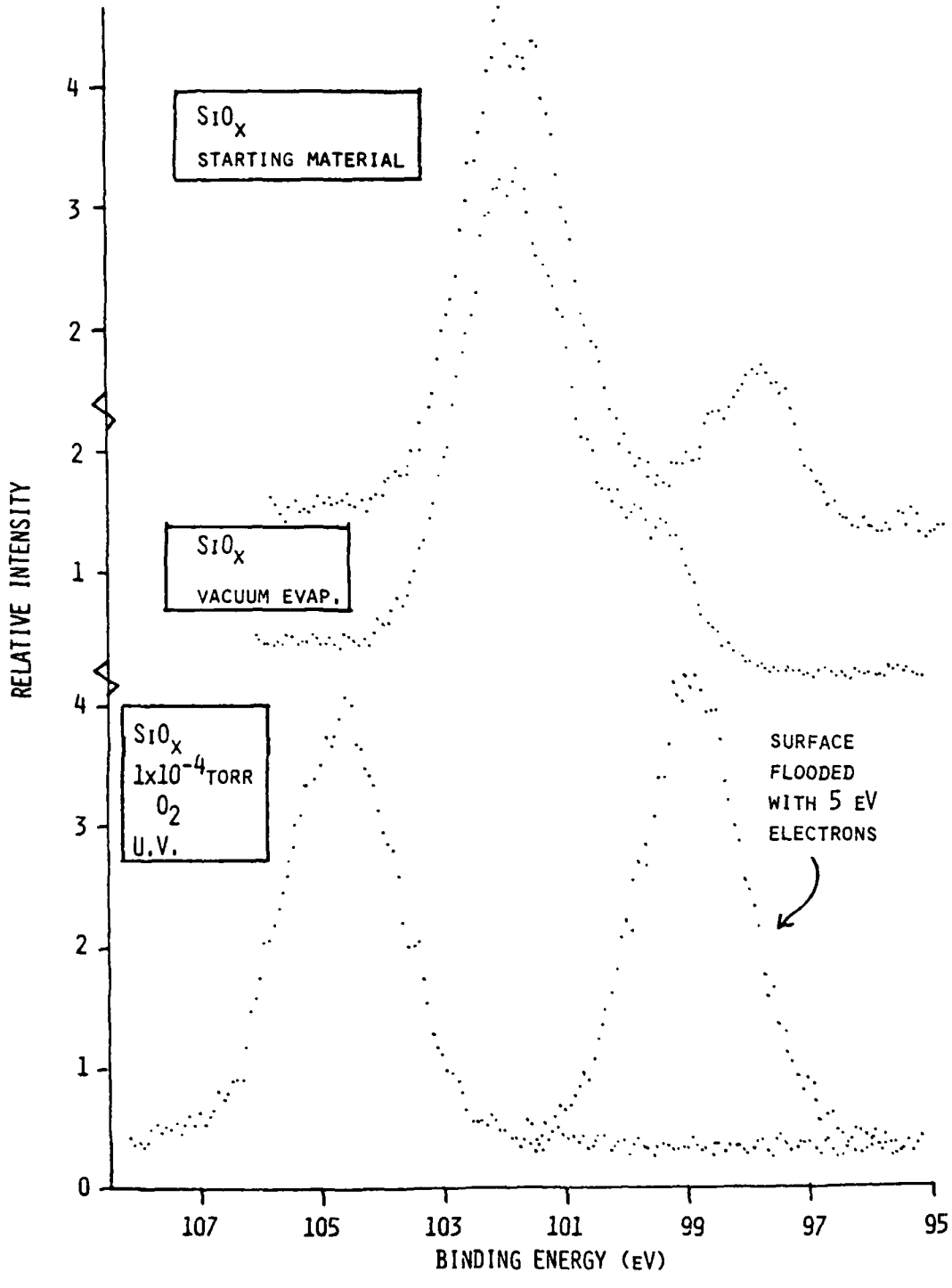


Fig. 25 XPS spectra in binding energy region of Si2p line for (top) SiO_x material before evaporation (middle) SiO_x after vacuum evaporation and (bottom) SiO_x after evaporation in O_2 with presence of UV light.

Si^{4+} while the less intense peak is associated with Si°. Evaporation of this same starting material in vacuum (or in ≈ 10^{-5} torr O_2) produces a film which contains reduced Si (spectrum in middle of Fig. 25). From the chemical shift scale of Ref. 15, this reduced form of Si is most likely Si^{2+}. Photochemical reactions can be induced by ultraviolet (UV) excitation (see e.g., the discussion of Al_2O_3 growth on GaAs by evaporation of Al in O_2 by Yokoyama et al).[16] This possibility was investigated for the SiO_x deposition. Evaporation of the SiO_x source material with the sample preparation chamber filled to 10^{-4}-10^{-5} torr of O_2 which was illuminated by UV radiation produced a film with only one detectable Si oxidation state as indicated by the two XPS spectra shown at the bottom of Fig. 25. This sample charged positively under illumination by the XPS x-ray beam and consequently the relative binding-energy scale cannot be compared directly with the spectra at the top and middle of Fig. 25. The sample charging effect is easily observed by flooding the sample surface with 5 eV electrons and noting the large shift in the apparent Si2p binding energy (see bottom of Fig. 25). The relative binding-energy difference between the Si2p and O1s photoelectron peaks indicates that this sample is SiO_2 to within the analysis limits of the XPS technique.

As discussed below, the dielectric properties of the deposited SiO_x improve markedly as the amount of reduced Si is decreased. C-V and I-V measurements were caried out on the X1-X5 samples. To facilitate these measurements, metal dots of 10 and/or 20 mil diameters, were evaporated onto the sample surfaces through a contact mask. The metal dots were ~ 200 A Cr followed by ~ 2000 A of Au.

In the first of these samples, X1, a few monolayers of Ga_2O_3 were formed by heating the GaAs surface to ≈ 460°C during exposure to 6×10^4 L of oxygen. This was followed by vacuum evaporation of ≈ 1000 A of SiO_x. Typical results are shown in Fig. 26a for C-V measurements on these samples. For the p-type sample a deep depletion curve is observed for a large positive bias. Although the estimated change in the surface potential is large enough for inversion to occur, leakage through the oxide apparently prevents accumulation

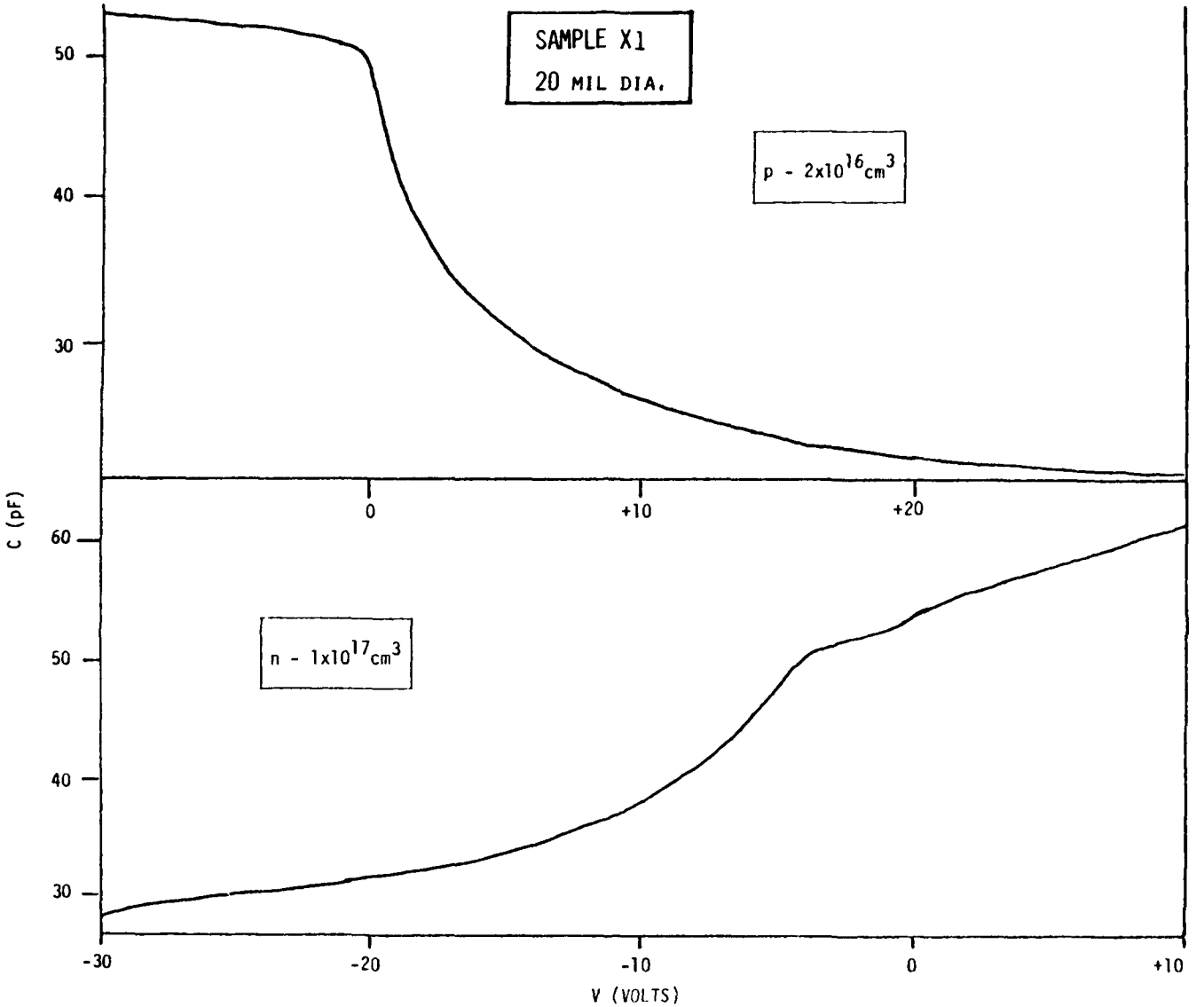


Fig. 26a C-V measurements for sample X1.

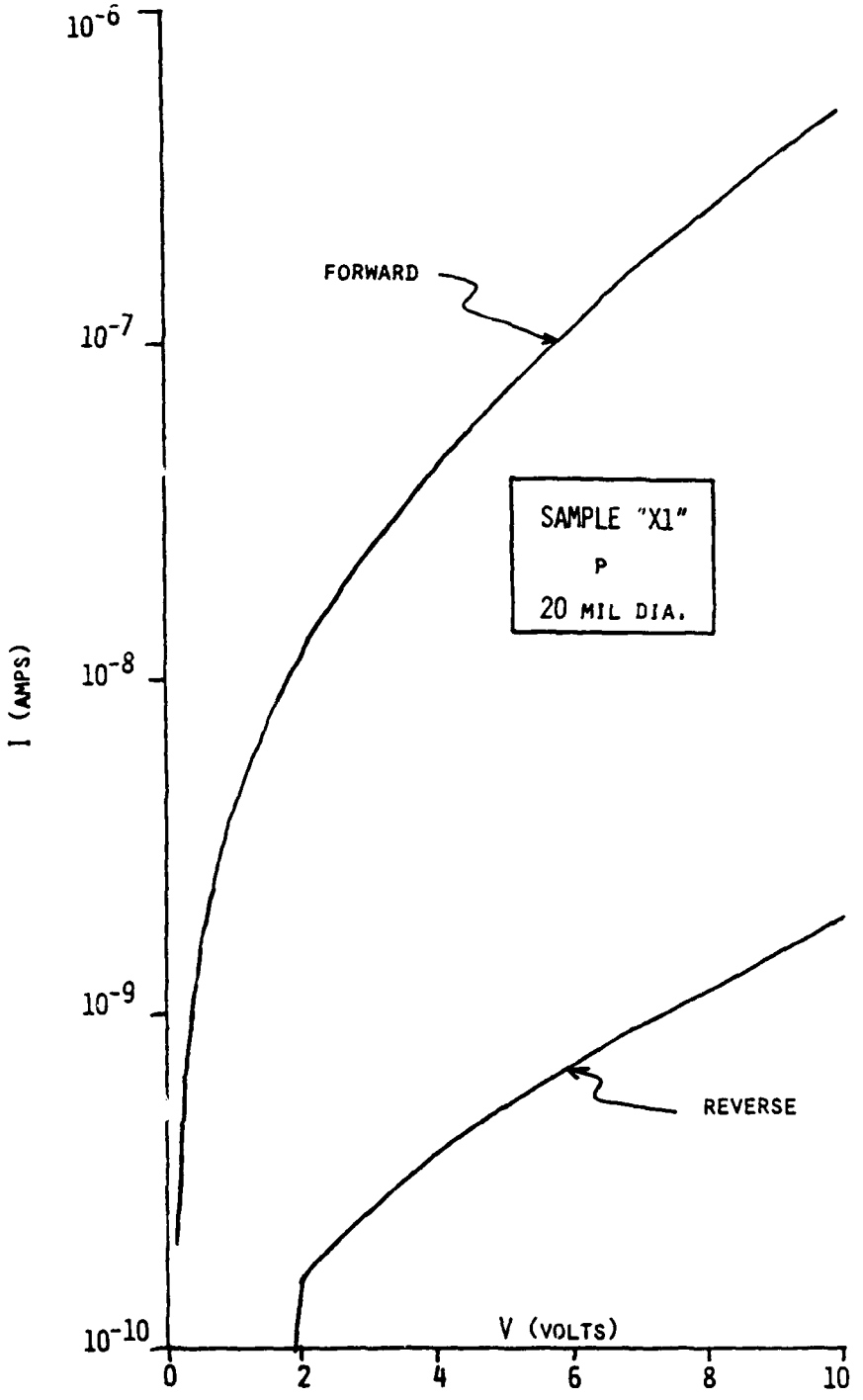


Fig. 26b I-V measurements for sample X1 (p-type)

of electrons in the inversion layer.[17] At reverse bias the device appears to go into accumulation. The n-type sample shows a C-V curve which is not interpretable by standard methods. Although the curve shows some indication of deep depletion, no accumulation or inversion behavior is identifiable.

Characteristic I-V curves for the p-type samples are shown in Fig. 26b. Under forward bias the electric field is across the insulator and a relatively high current density is observed at relatively low fields (5×10^{-5} amps/cm^2 for 2×10^5 V/cm). This behavior is consistent with the absence of inversion in the C-V measurements.

Samples X2 through X5 were made by depositing SiO_x photochemically on the GaAs as described above. As shown in Fig. 27 this oxide showed superior dielectric properties compared to the evaporated SiO_x. In this figure the I-V characteristics are shown for two devices produced with similar oxide thicknesses by vacuum evaporated and photochemically produced SiO_x. The device with the SiO_x photochemically produced oxide has a leakage current which is two orders of magnitude less than the device with the evaporated SiO_x. Although there is considerable scatter in leakage currents between devices, the better devices produced by the two techniques consistently exhibited this trend.

It was hoped that the superior dielectric properties of the photochemically produced SiO_x would yield devices which would show inversion without hysteresis in the C-V characteristics. This did not turn out to be the case. Some typical C-V curves are shown in Figs. 28a-d for these samples. Most of the C-V curves are not directly interpretable. Those which are interpretable show deep-depletion and considerable hysteresis. One possible explanation for this behavior is that the leakage current through the oxide eliminates charging of the semiconductor interface and the consequent hysteresis associated with slow interface states.

One of the samples, X3, which showed good leakage characteristics was sent for evaluation to Dr. B. Bayraktaroglu at the Air Force Wright Aeronautical Laboratories (AFSC) where frequency dependent C-V and G-V

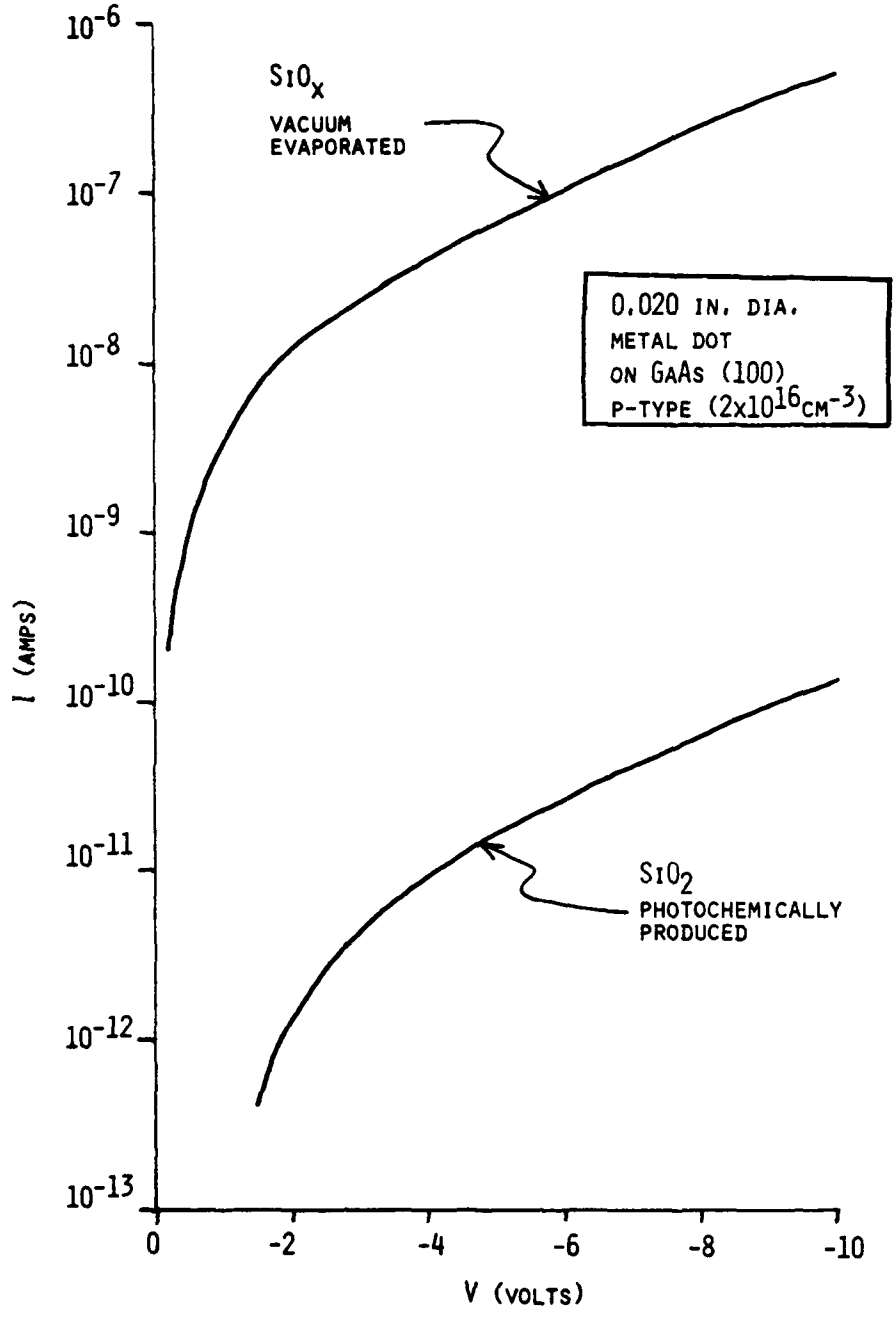


Fig. 27 Comparison of leakage currents for vacuum evaporated SiO_x and photochemically produced SiO_2 insulators.

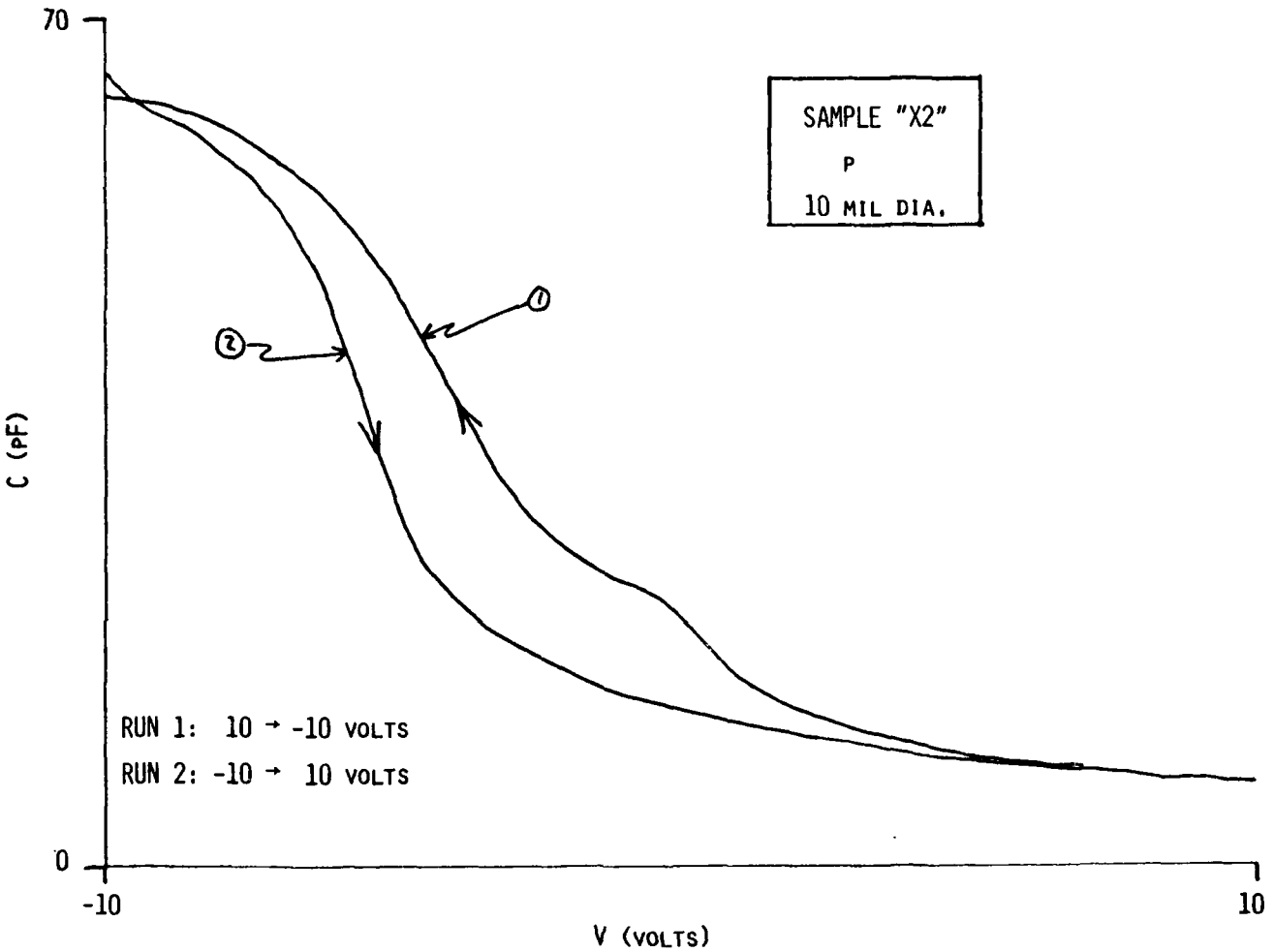


Fig. 28a C-V measurements for sample X2 (p-type).

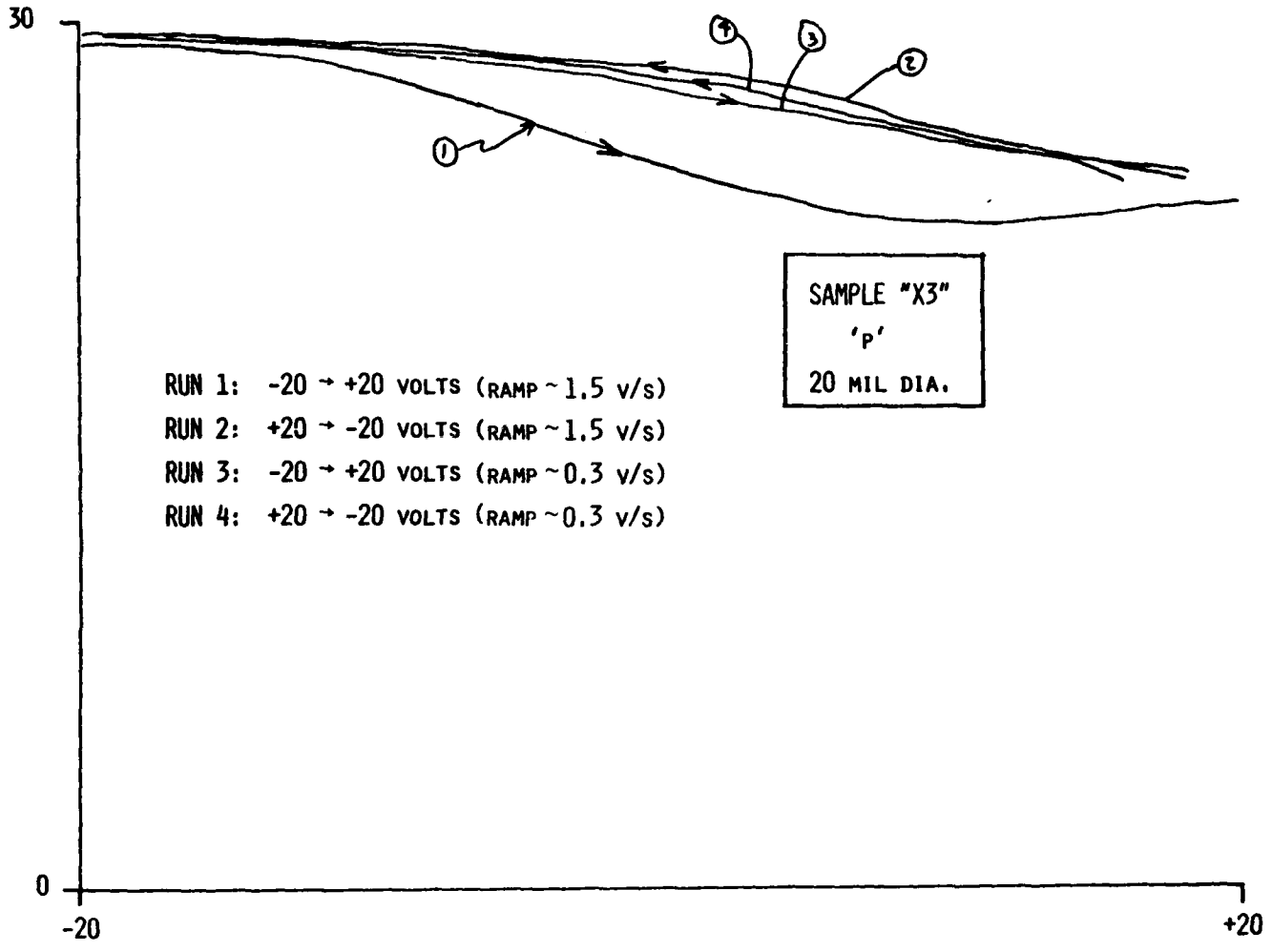


Fig. 28b C-V measurements for sample X3 (p-type).

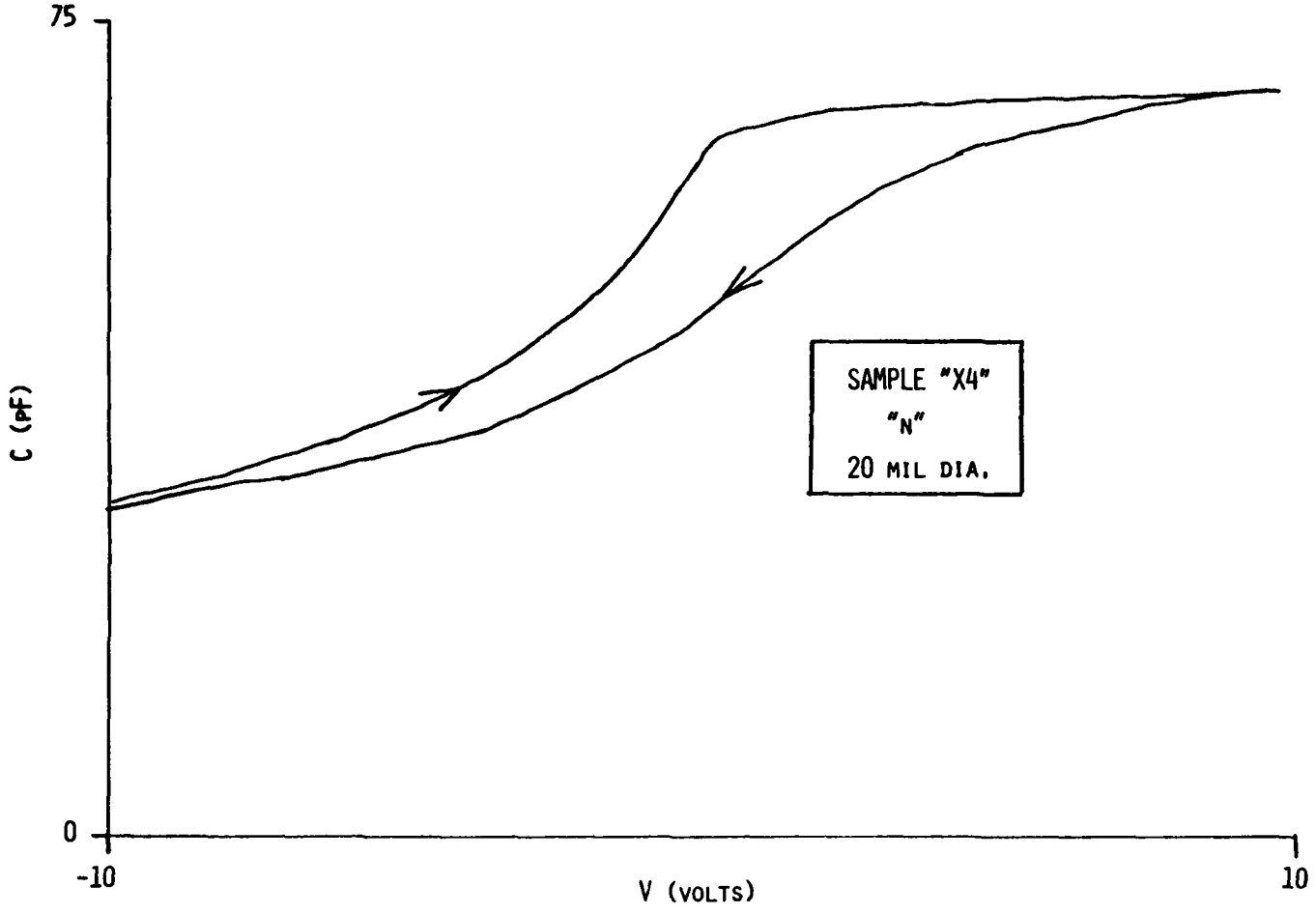


Fig. 28c C-V measurements for sample X4 (n-type).

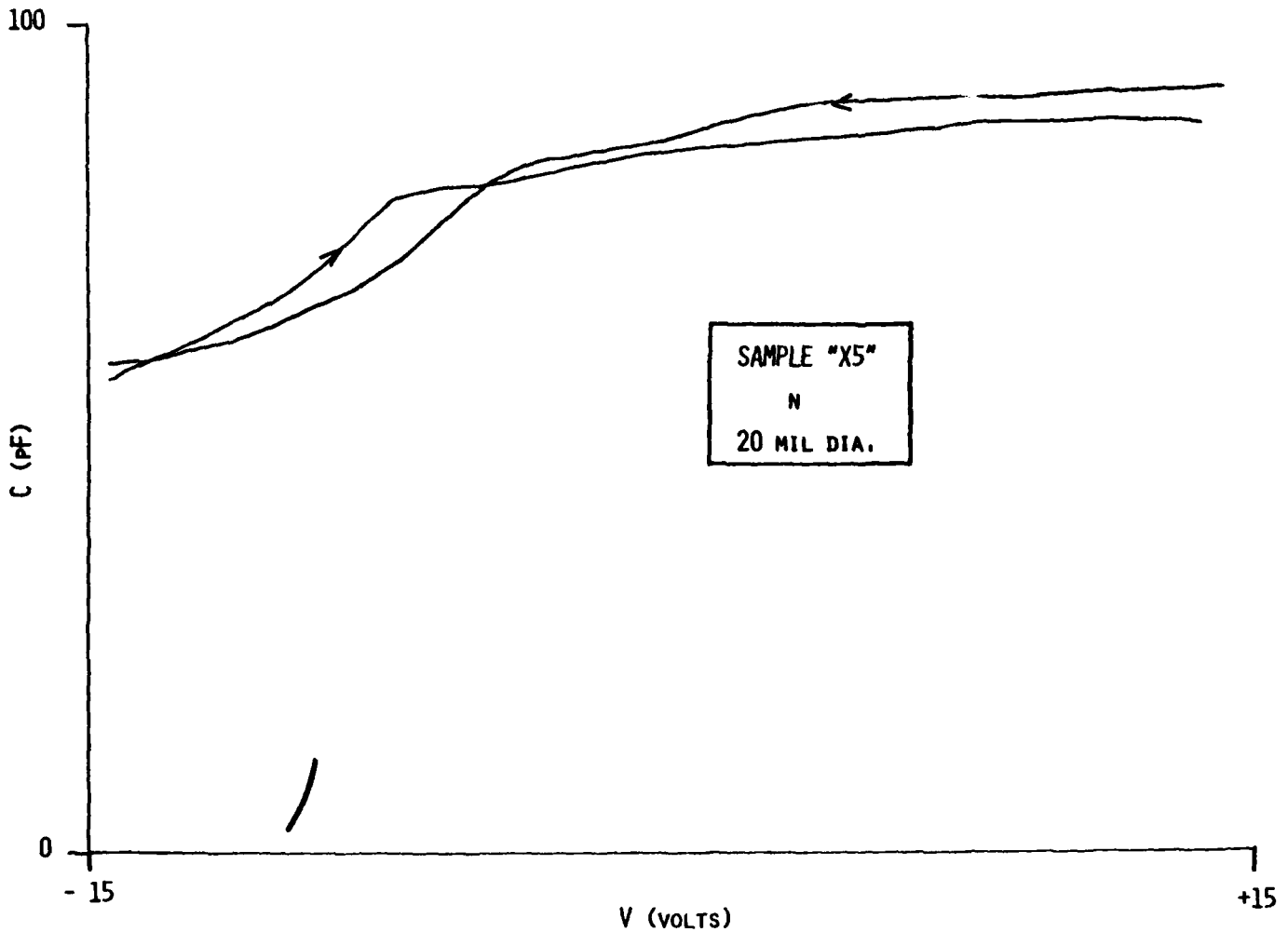


Fig. 28d C-V measurements for sample X5 (n-type).

measurements were made.[18] Hysteresis in the C-V and G-V curves was observed. The C-V curves were difficult to study due to the small change in capacitance with applied voltage. The G-V curves produced distinct peaks at all test frequencies. Such peaks indicate the presence of states at the interface. Typical examples of some of these data are shown in Figs. 29a and b.

In an effort to improve the properties of the samples made by photochemically deposited SiO_2 on a GaAs surface, selected samples were annealed under various conditions. It was found that by annealing in forming gas (a dilute H_2 in N_2 mixture) hysteresis in the C-V curves of the deposited SiO_2 samples could be appreciably reduced. As an example, Fig. 30 shows results on sample X4 (n-type) after a forming gas anneal at 400°C. These data can be compared with the data shown in Fig. 28c before the sample was annealed. It is observed that hysteresis in the C-V curves has been reduced to less than 1 V.

In spite of the reduction in hysteresis, the C-V curve indicates that there is a large flatband voltage shift indicative of a large density of interface states. In addition, the anneal is observed to have a detrimental effect on the dielectric properties of the device showing increased leakage current through the oxide. Such an increase in the leakage current may be responsible for the decreased hysteresis.

In conclusion, none of the SiO_x insulating layers currently investigated was capable of satisfactorily passivating the GaAs surface suitably for device applications. Inversion was not observed for any device while only devices with unacceptably large leakage showed interpretable C-V curves without hysteresis.

2. Aluminum Oxide Formation

Efforts to develop a technique for depositing Al_2O_3 on GaAs surfaces within the UHV sample preparation chamber of the XPS system are described in this section. Previously reported studies[2] indicated that high temperature oxidation of a thermally cleaned n-GaAs (100) surface results in a surface which is covered with Ga_2O_3 (see Table 3 which summarizes the typical

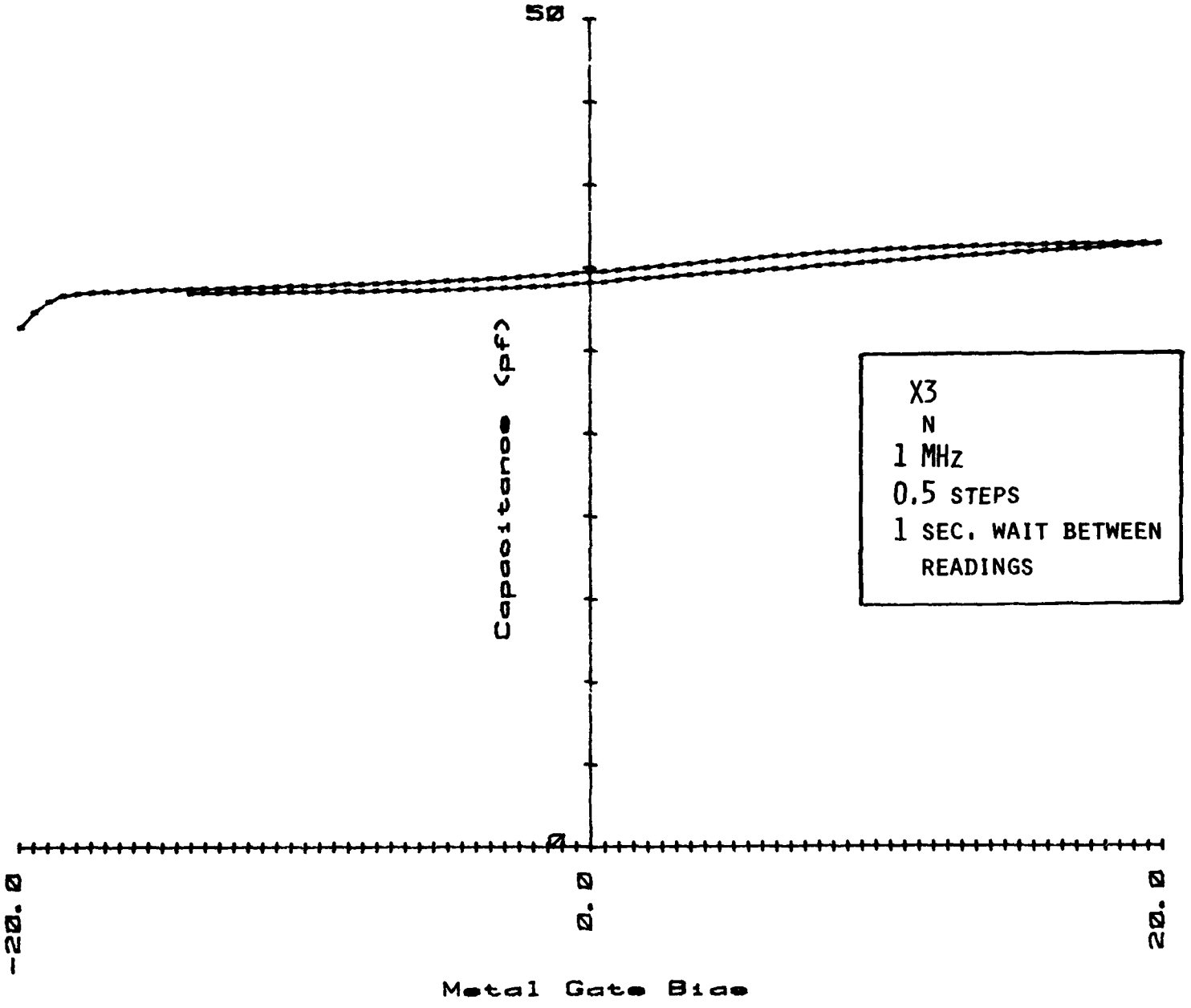


Fig. 29a C-V measurements for sample X3 (n-type) obtained by B. Bayraktaroglu (WPAFB).

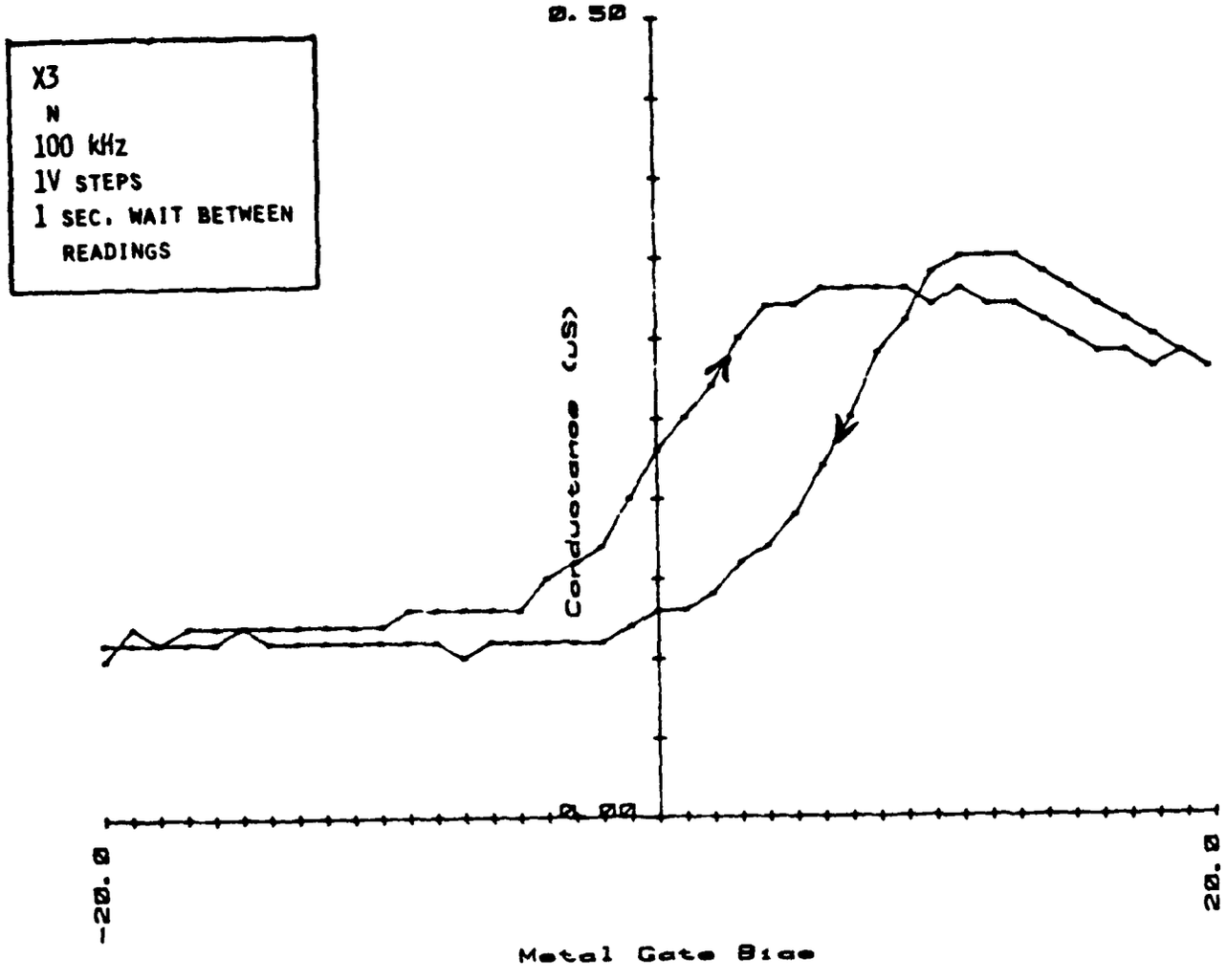


Fig. 29b G-V measurements (at 100 kHz) for sample X3 (n-type) obtained by B. Bayraktaroglu (WPAFB).

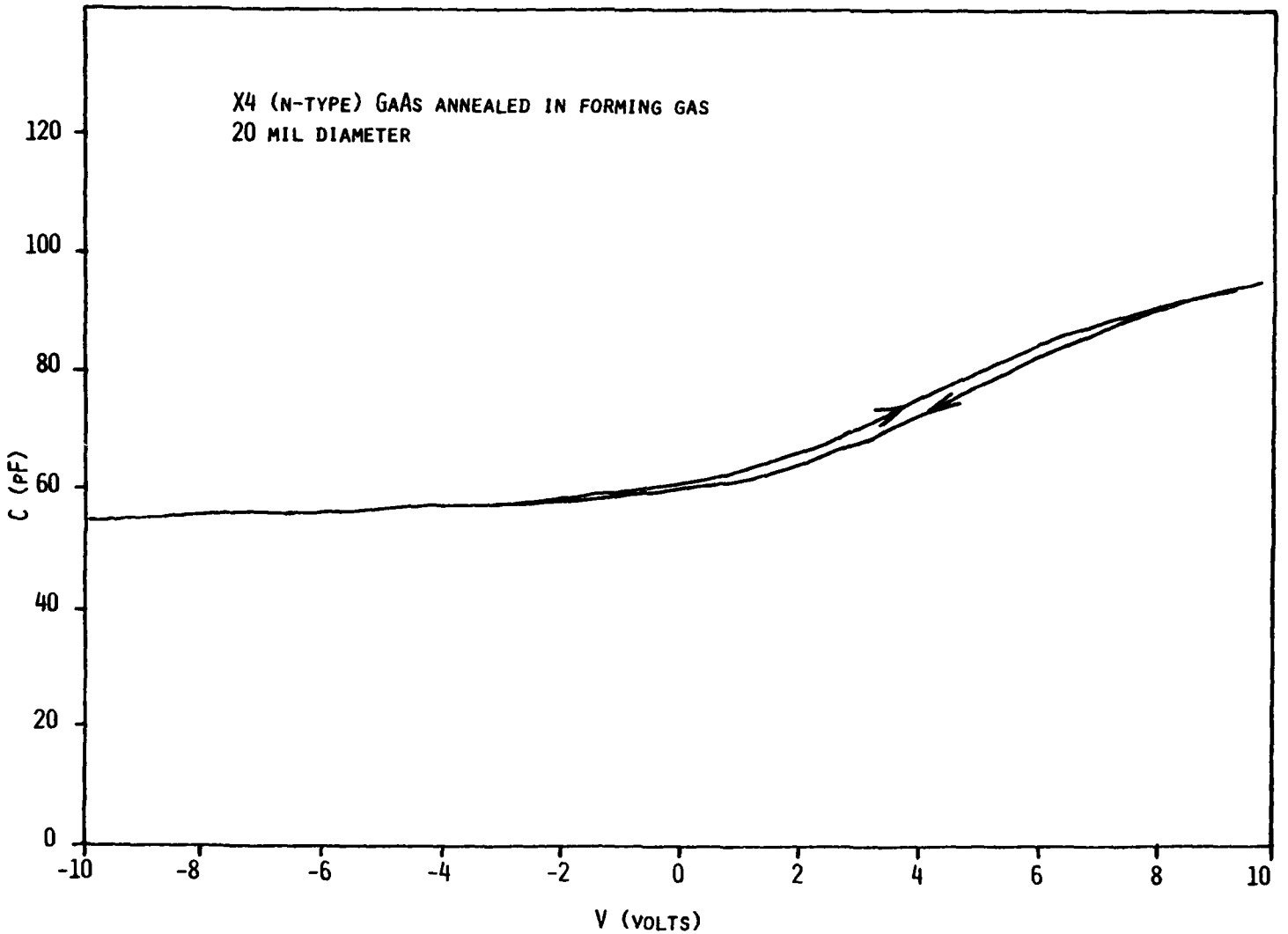


Fig. 30 C-V measurements for sample X4 (n-type) which was annealed in forming gas at 400°C.

chemistry and surface potential variations of such a surface) and decreases surface band bending by ~ 0.2 eV. This suggests that a useful structure would be to grow a thin interfacial Ga_2O_3 oxide on GaAs and to deposit a thick dielectric layer on this surface. Thus, an initial attempt was made to grow an Al_2O_3 dielectric layer. The results are shown in Figs. 31a-c. The lower portions of Figs. 31a and 31b show the Ga3d and As3d core-level spectral regions before Al deposition but after growth of the Ga_2O_3 layer which is indicated by the asymmetry to high binding energy of the Ga3d level. Aluminum oxide growth was attempted by slow (~ 1 A/s) deposition of Al metal in an ambient of 1×10^{-4} torr O_2. Figure 31c shows that a chemical reaction occurs upon deposition of submonolayer amounts of Al. First, the gallium oxide is reduced and, secondly, some Ga metal is produced as indicated by the Ga3d line asymmetry to lower binding energy. Figure 31b shows the potential shift as monitored by the As3d level. After the Al deposition the bands are pinned at the "clean" surface position. Figure 31c curve (a) shows that Al oxide is formed. Further deposition of Al in an ambient consisting of water vapor and O_2 resulted only in a thick Al metal deposition, see Fig. 31c curve (c), with no obvious difference from Al deposited under UHV conditions without O_2 ambient. Conclusions drawn from these experiments are: (1) a surface chemical reaction occurs which involves the reduction of gallium oxide by Al metal, i.e., $Ga_2O_3 + 2\ Al\ (m) \rightarrow 2\ Ga\ (m) + Al_2O_3$. This reaction might be expected from consideration of the relative heats of formation. (2) the Al which getters the Ga_2O_3, pins the GaAs energy bands at the "thermally cleaned" surface position. (3) Under the conditions employed in this experiment, after the oxygen available in the form of Ga_2O_3 is consumed, the Al deposit is metallic and not oxide.

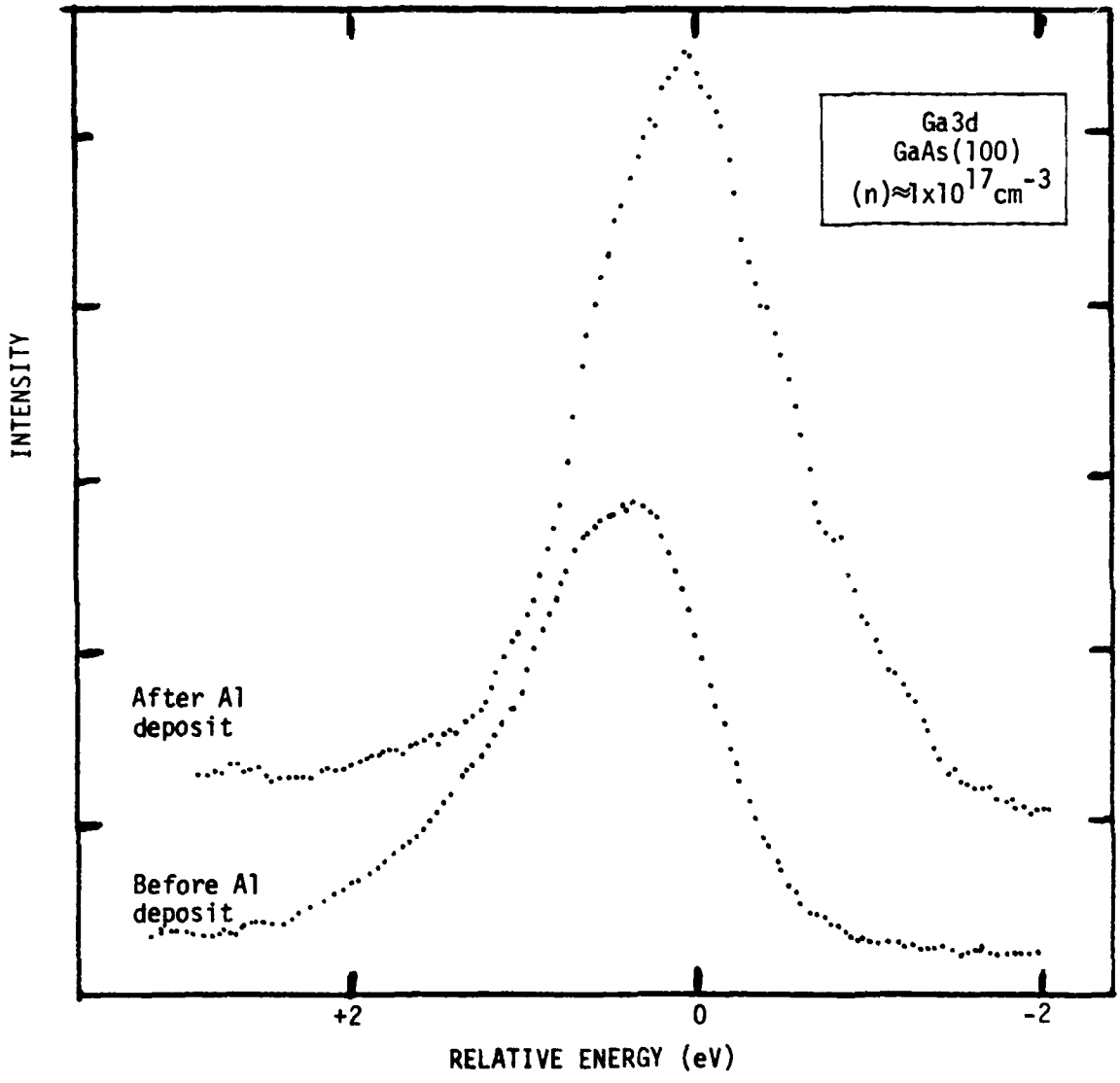


Fig. 31a XPS spectra which illustrate effect of Al deposition on Ga3d line shape. See Section V 2 for details.

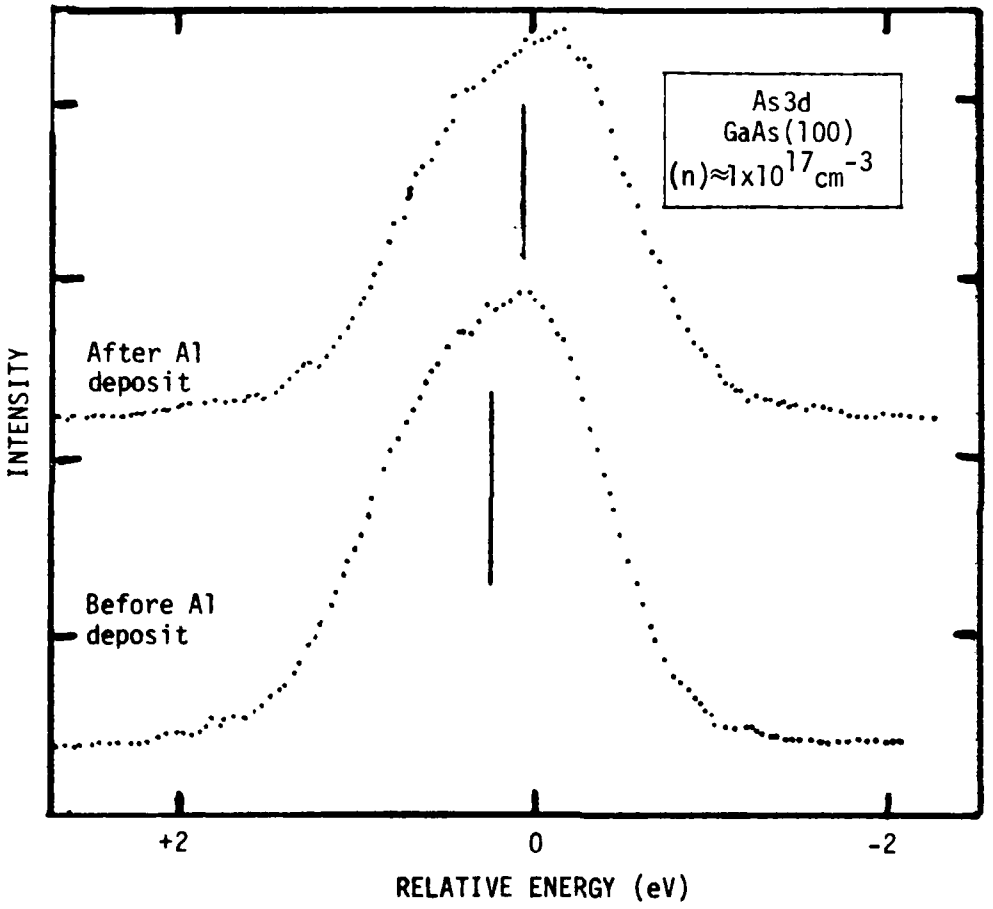


Fig. 31b XPS spectra which illustrate effect of Al deposition on As3d line shape. See Section V 2 for details.

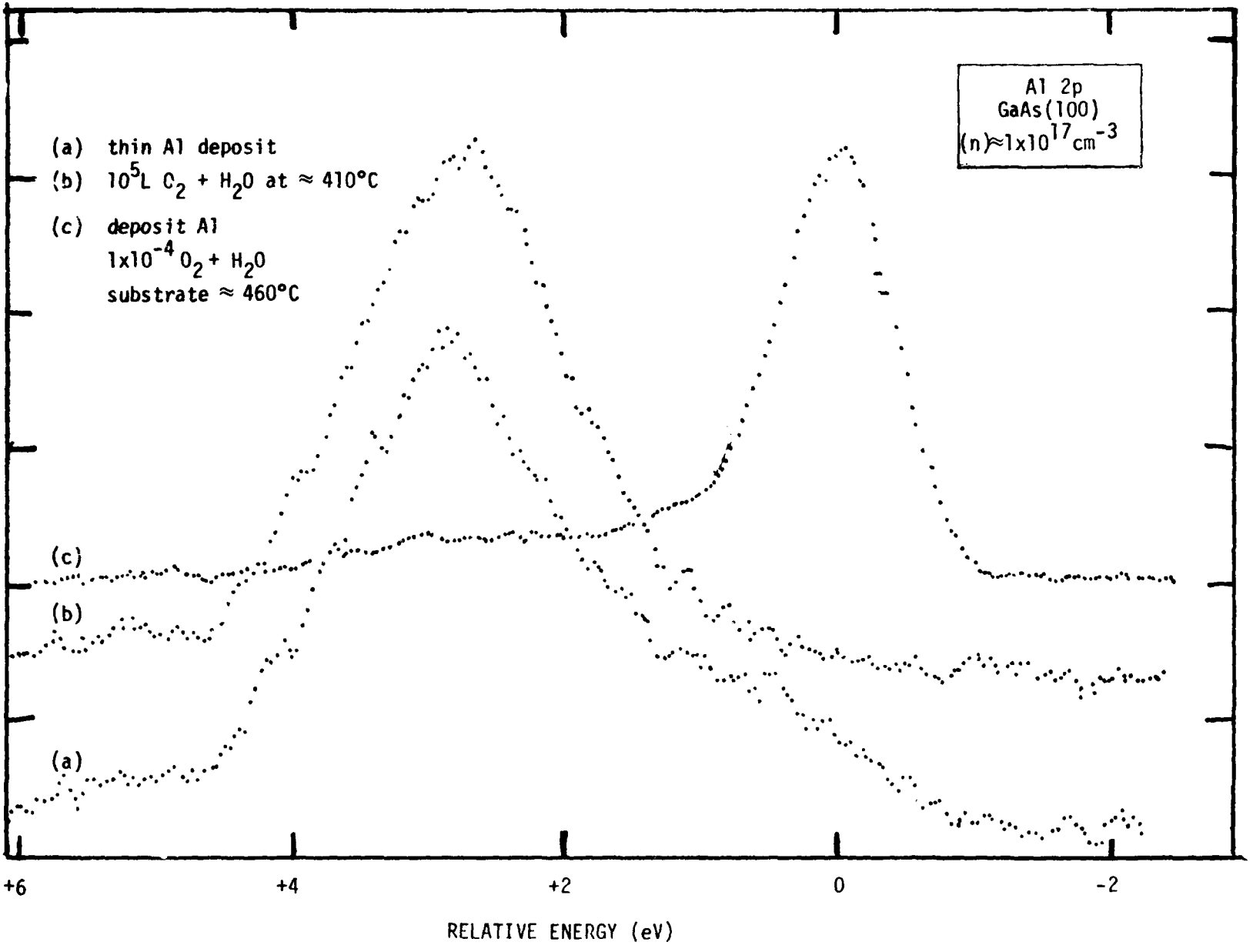


Fig. 31c XPS spectra in region of Al2p line for Al deposited on GaAs surface.

Table 3

XPS Results for Oxidation and Deposition of Al on GaAs (100)

(n-type, $\approx 1 \times 10^{17}$ cm^{-3})

Treatment	Relative As3d Binding Energy in GaAs (eV)	Remarks
Chem. etch	+0.2	$Ga_2O_3 + As_2O_3$
$\approx$ 570°C	0.0	Clean
2×10^4 L O_2 at $\approx$ 460°C	+0.2	Ga_2O_3
Few monolayers Al deposited in 10^{-4} torr O_2 (25°C)	0.0	Ga3d asymmetric to low binding energy $Ga_2O_3 + 2Al \rightarrow 2Ga + Al_2O_3$

Previous studies[19] have shown that thermal oxidation of aluminum usually results in polycrystalline oxide films of poor quality. A study was carried out to investigate the growth of aluminum oxide by other methods with the goal of finding a method which would allow growth of Al oxide at room temperature. The preparation methods were compared by using XPS. The studies included (A) slow evaporation of Al in O_2 background under UV irradiation (Hg lamp), (B) and (D) heating of film at $\approx$ 510°C under O_2 exposure, (C) deposition of Al during O_2 exposure on a heated substrate, and (E) deposition of Al under conditions of O_2 plasma discharge onto a room temperature substrate. The XPS spectra in the Al2p region which were observed during these studies are shown in Figs 32a-c. The Al metal 2p level has a binding energy of $\approx$ 72.6 eV relative to the Fermi level. All spectra in Figs. 32a-c are referenced to Al metal. Figure 32a shows the results for deposition under UV irradiation. This film is mostly Al metal but also has at least two different oxides with chemical shifts of $\approx$ 3.0 and $\approx$ 2.0 eV, the former being similar to the

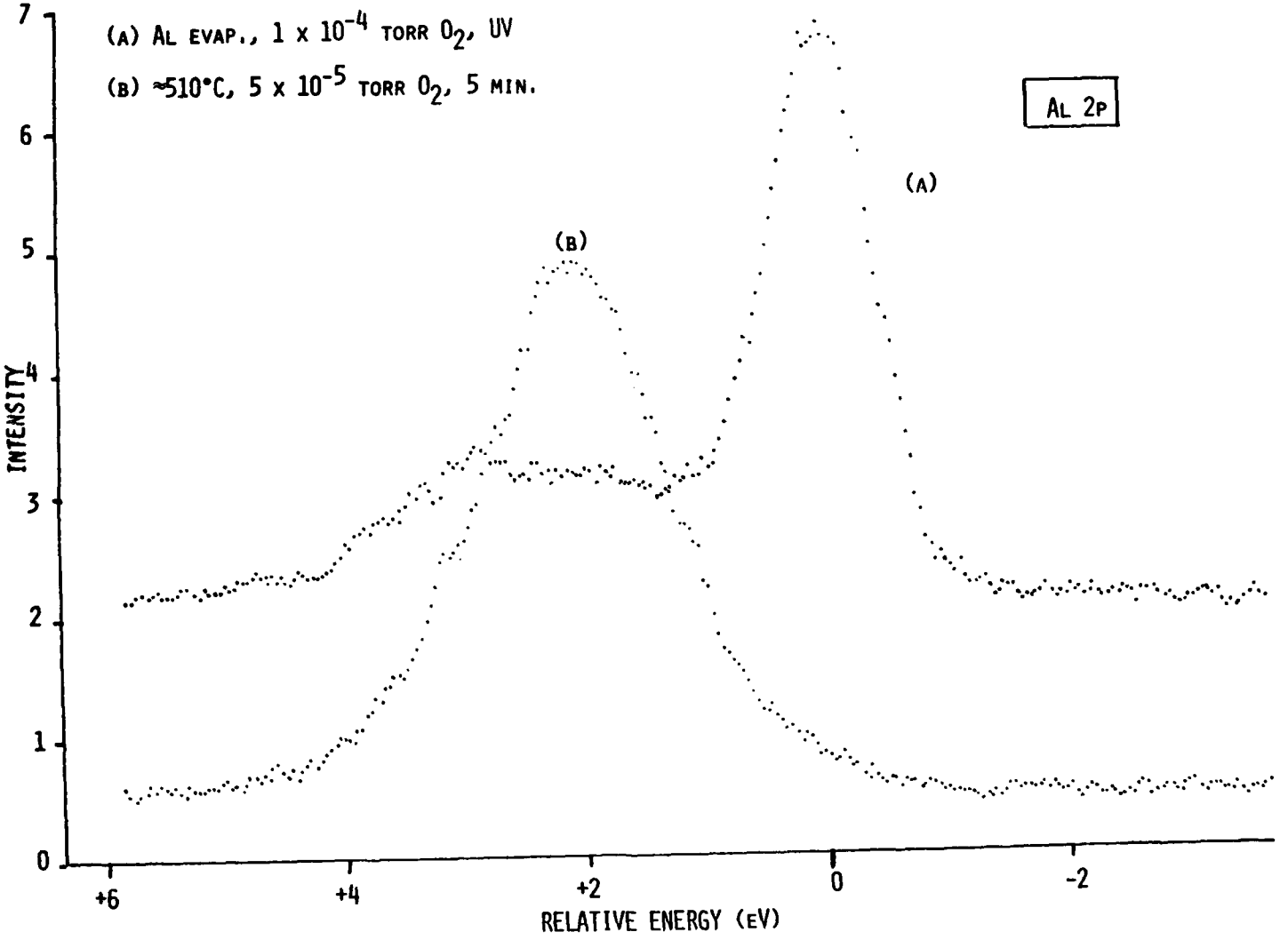


Fig. 32a XPS spectra in region of Al2p line for (A) evaporation of Al in O_2 with UV light present, and (B) oxidation of Al film in (A) at ~ 510°C.

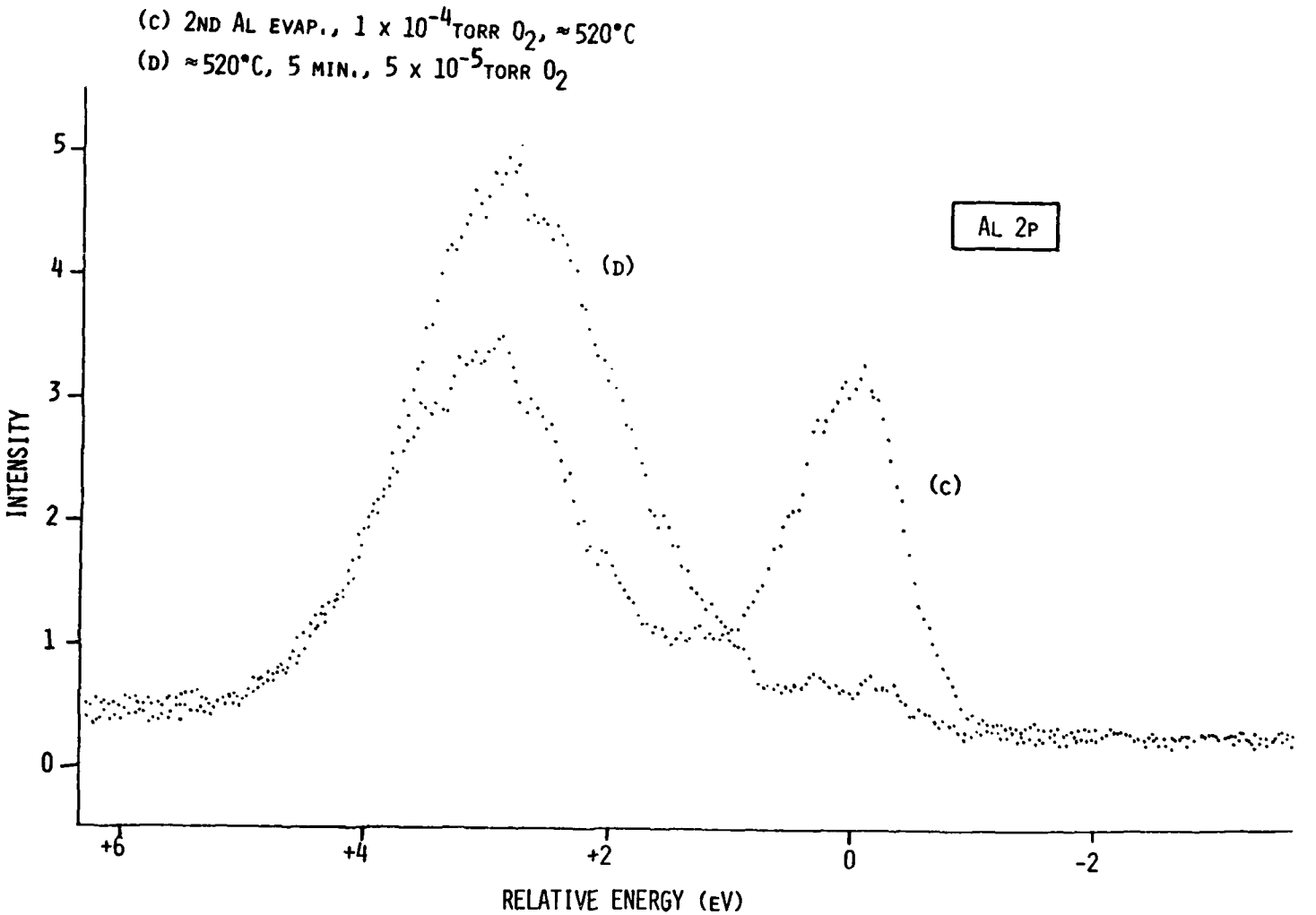


Fig. 32b XPS spectra in region of Al2p line for (C) additional Al evaporated in O_2 onto the surface characterized as spectrum (B) in Fig. 32a while this surface was at 520°C and (D) oxidation of sample in (C) at ~ 520°C.

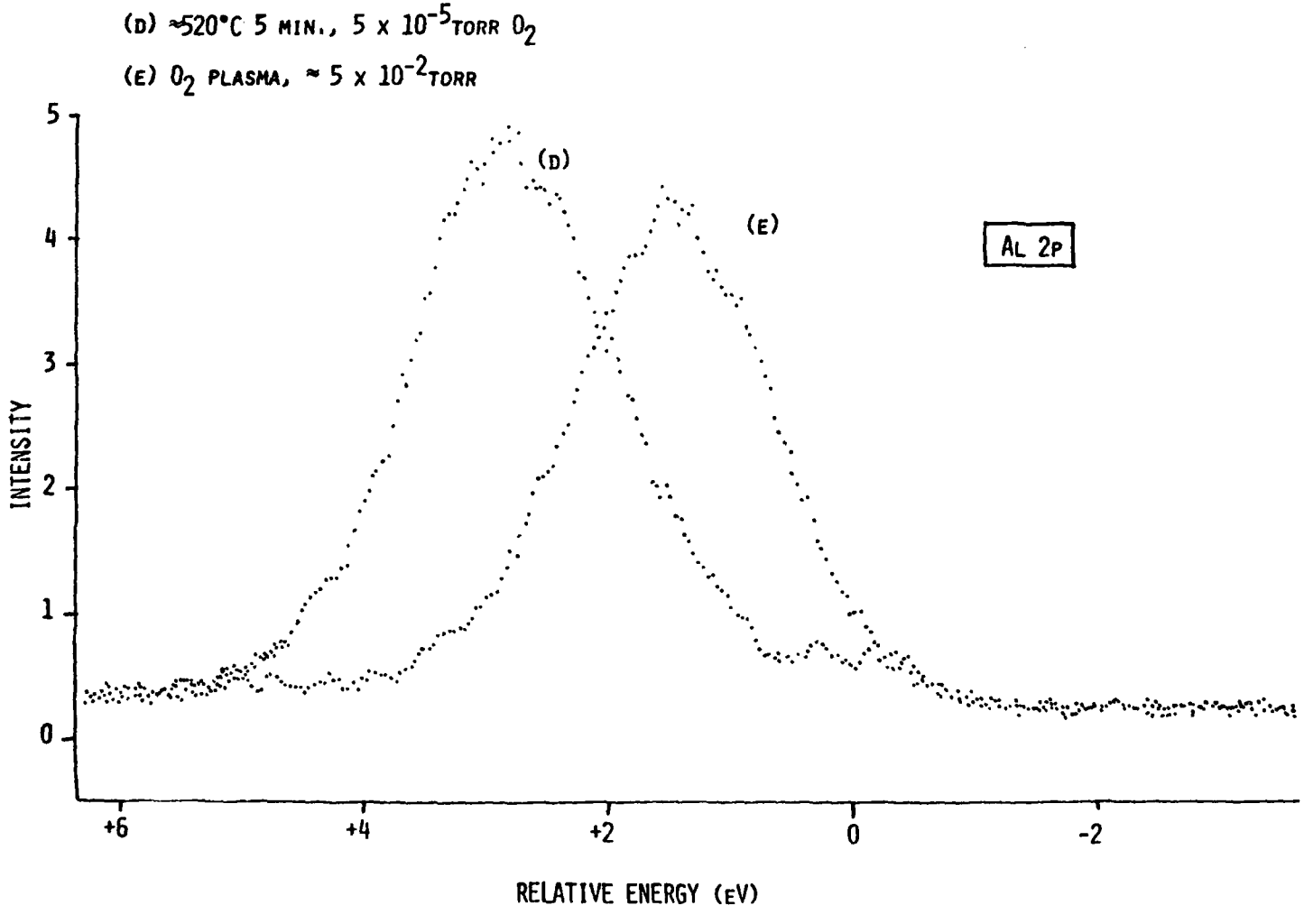


Fig. 32c XPS spectra in region of Al2p line. Spectrum labeled (D) is repeated from Fig. 32b for reference. Spectrum (E) was obtained after deposition of Al onto the sample at room temperature while in the presence of an O_2 plasma discharge.

characteristic ≈ 2.8 eV shift of bulk Al_2O_3 and the latter being some intermediate form of oxide. A slower deposition rate could possibly yield a film that is totally oxide. Heating this film to ≈ 510°C in 5×10^{-5} torr O_2 almost totally converts this film to the intermediate oxide. Another film investigated was one prepared by Al deposition in 1×10^{-4} torr O_2 onto a substrate at ≈ 520°C. This preparation leads to a mixture of Al metal and Al oxide with the ≈ 3.0 eV chemical shift and is thus similar to bulk oxide. Again the deposition rate was probably too fast for total oxidation. Further heating this film converts the film almost totally to aluminum oxide. The third preparation was Al deposition through a plasma discharge in O_2 onto a room temperature substrate. This sample was totally an aluminum oxide, however, the chemical shift was ≈ 1.4 eV. The intermediate oxide (with chemical shift of ≈ 1.4 eV) is typical of the initial stages of Al metal oxidation at low O_2 exposures[20,21] and low temperatures.[22] This is the first observation in which a relatively thick film of the intermediate oxide was prepared at room temperature. These investigations have shown that the oxidation of Al is more complex than might first be expected. The chemical nature of the intermediate Al oxides is unknown.

It appeared that efforts to develop a process for depositing Al_2O_3 that could be used in an MIS device structure would be beyond the scope of this program and therefore further work in this direction was discontinued. The work initiated in this Section on the interaction of Al with native oxides on GaAs surfaces was subsequently extended to include several other metals as part of an independent study. Two papers were published based on these extended studies; these papers are reproduced in Appendix I.

VI. $Si_xO_yN_z$ DEPOSITED ON GaAs

As discussed in Section IV 3a, the LFE PDS/PDE plasma etcher was modified to facilitate $Si_xO_yN_z$ deposition. Experiments which involved deposition of this material on GaAs surfaces are discussed in this Section.

C-V curves for three samples are shown in Figs. 33a, b, and c. The data in Fig. 33a correspond to a sample which was given an HF etch prior to insulator deposition. In Fig. 33b, the sample was left in a forming-gas plasma for 10 min before deposition. For Fig. 33c, the sample was left in the forming gas plasma for 30 min prior to deposition.

All three of these samples (Figs. 33a-c) show flatband-voltage shifts consistent with a large density of interface states. For the sample with no plasma pretreatment (Fig. 33a), the lowest interface-state density occurs with a flatband voltage ≈ 5 V. For the other two samples the shift is large enough to effectively pin the Fermi level. As a result it seems desirable to minimize the time of exposure of the semiconductor surface to the plasma.

Additional and more detailed C-V measurements were performed on the sample (see Fig. 33a) which was only given the light HF etch immediately prior to $Si_xO_yN_z$ deposition (thickness ≈ 1.2×10^3 Å). Figure 34a shows C-V curves taken at three different scan rates (each progressively slower) as the voltage is ramped from -10 to 10 V. The most notable feature is that at a capacitance near 32 pF, the curves flatten and level off. Figure 34b shows three curves taken with the voltage being ramped in the opposite direction. Similar behavior is observed in all these cases. For slower scan speeds the curves remain relatively flat at larger voltages than for faster speeds. In the presence of light the same type of behavior is observed with the curve leveling of at the same value of the capacitance (Fig. 35). These curves suggest that inversion is being obtained at positive bias where the curves flatten. Normally one would expect a strictly flat curve under inversion conditions. However, since the minority carrier generation rate is small, a finite time is required to build up an inversion layer. In the presence of light, this time becomes

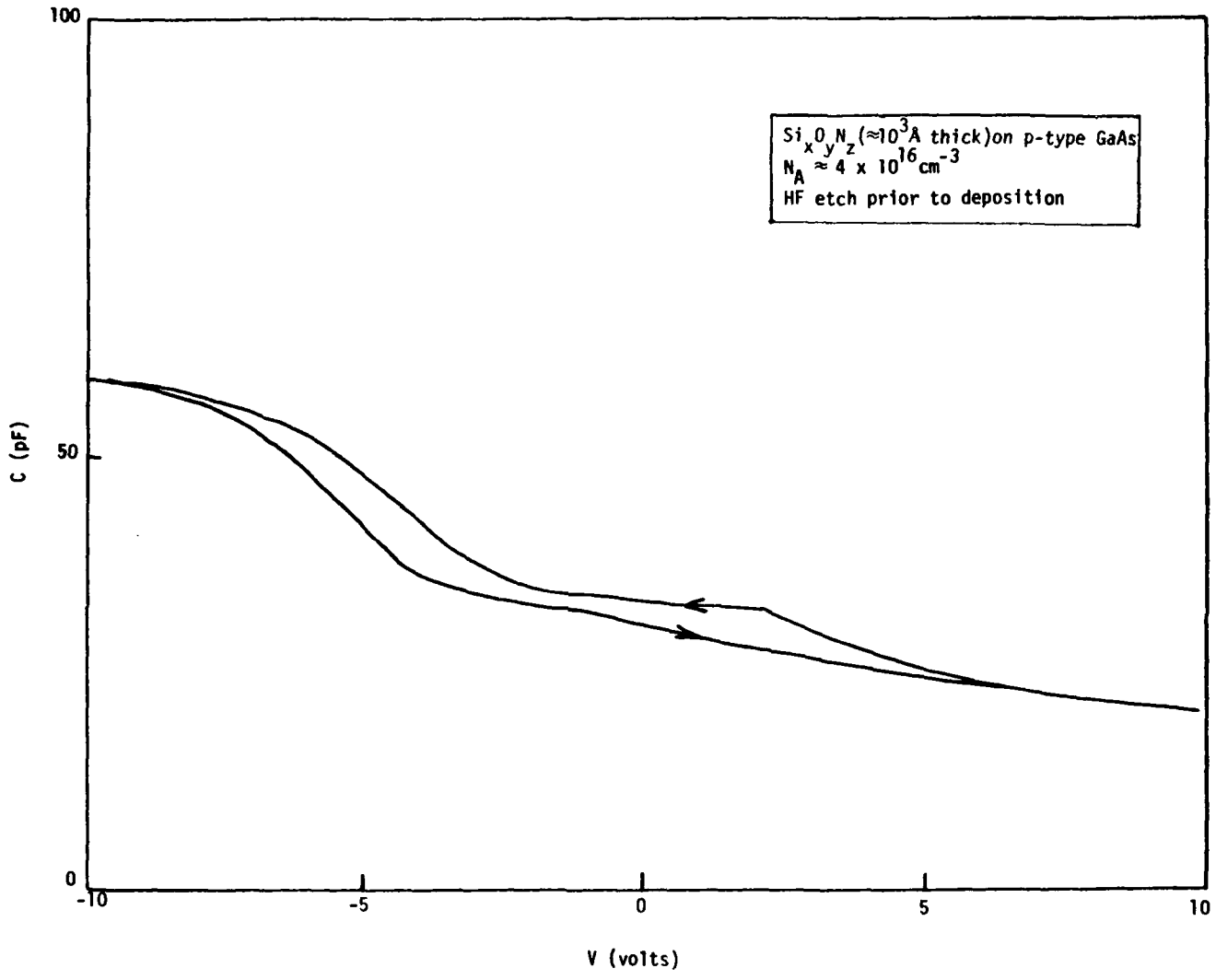


Fig. 33a C-V for $Si_xO_yN_z$ deposited on p-type GaAs which had been etched in HF just prior to deposition.

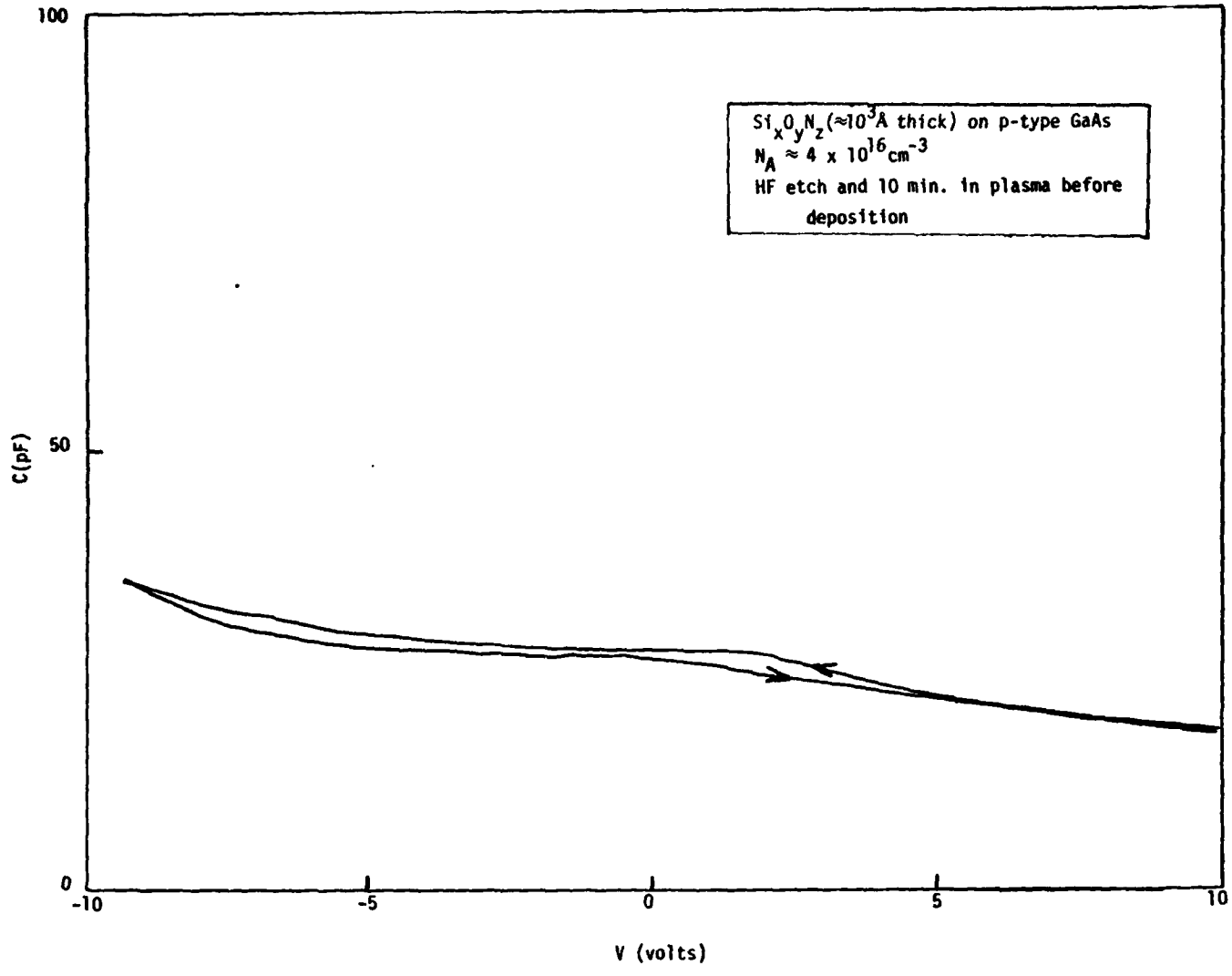


Fig. 33b C-V for $Si_xO_yN_z$ deposited on sample similar to that studied in Fig. 33a but which was exposed to a forming-gas plasma for 10 min prior to deposition.

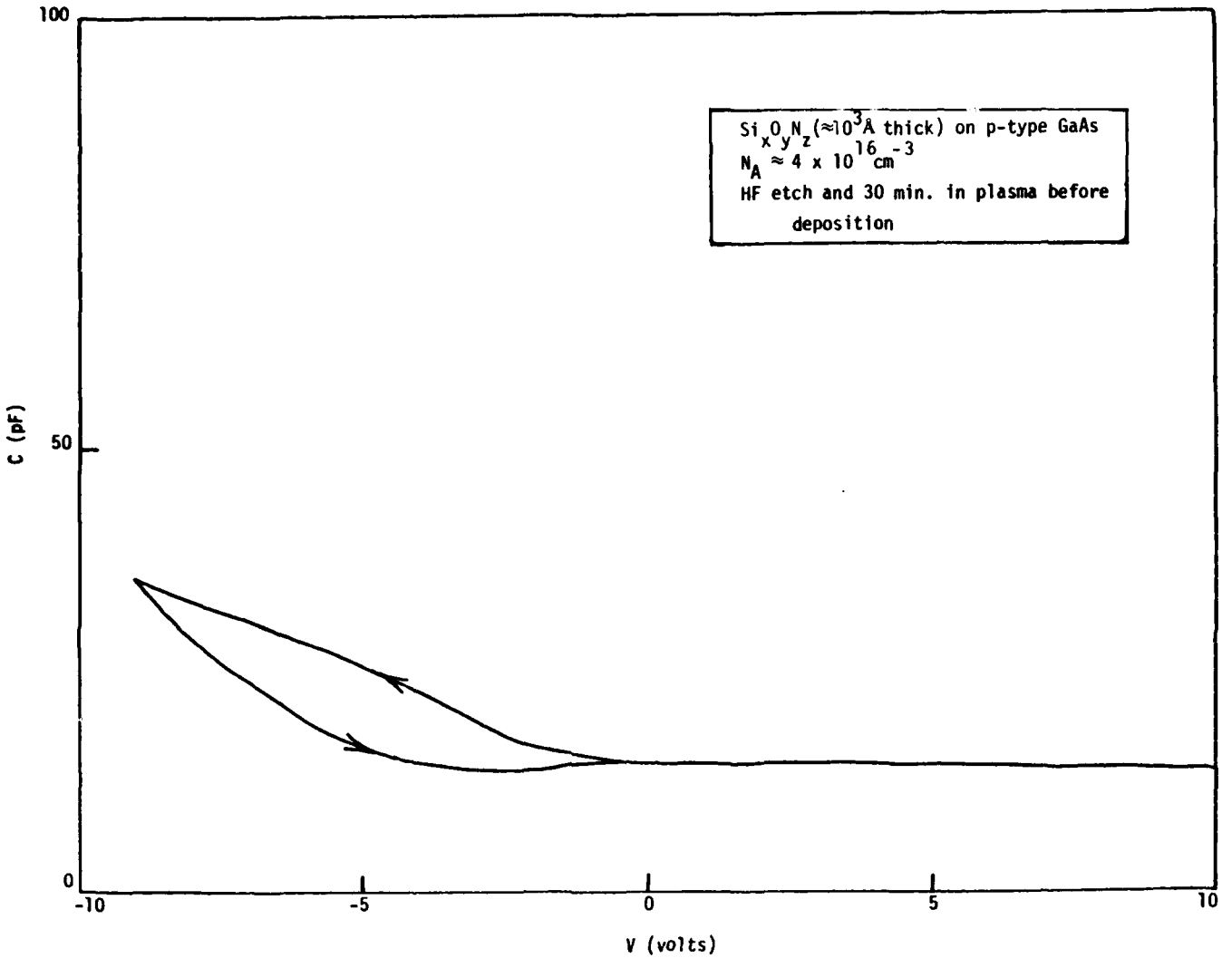


Fig. 33c C-V for $Si_xO_yN_z$ deposited on sample similar to that studied in Fig. 33a but which was exposed to a forming-gas plasma for 30 min prior to deposition.

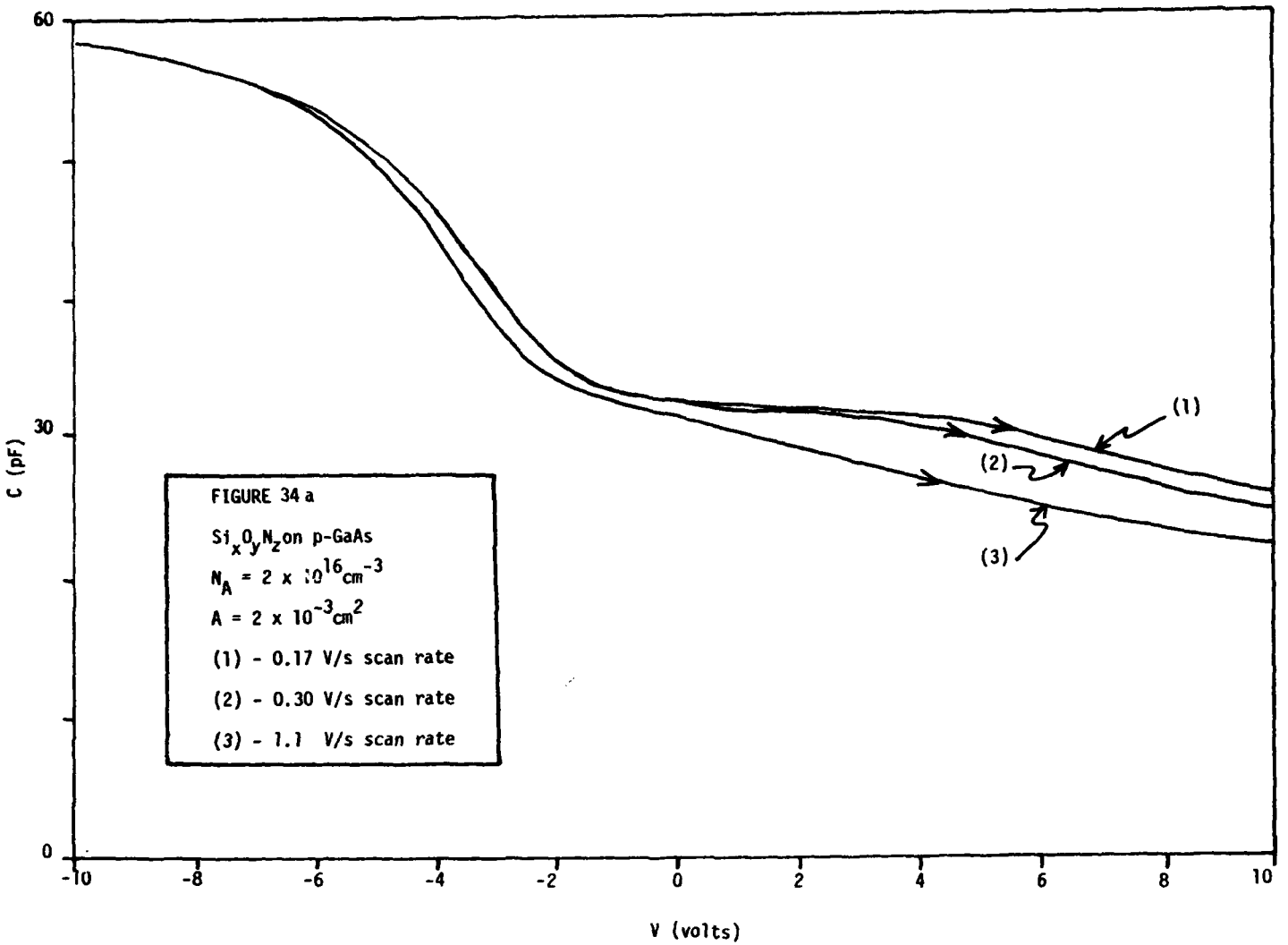


Fig. 34a C-V measurements on the same sample described in Fig. 33a as a function of + dV/dt scan rate.

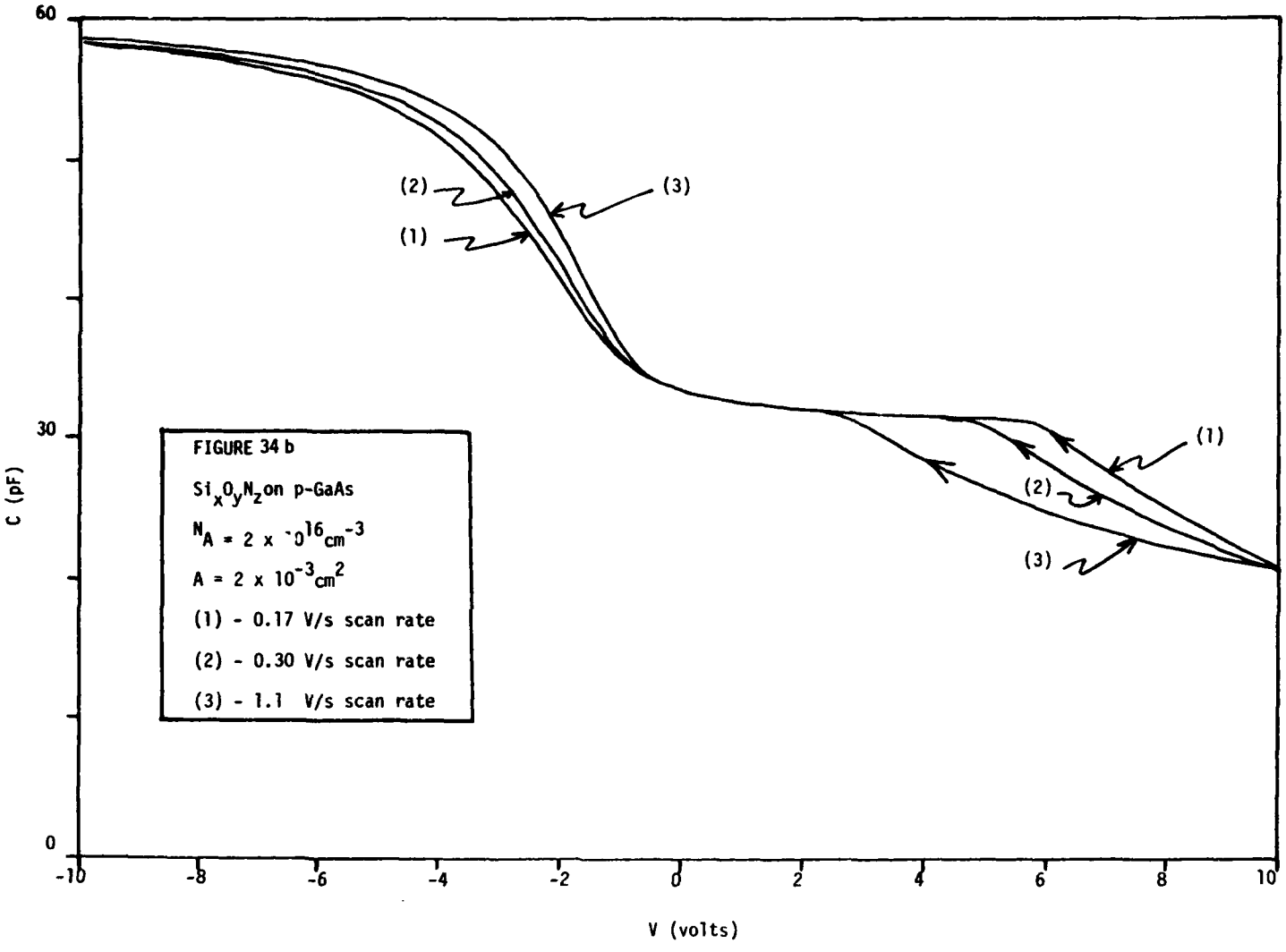


Fig. 34b C-V measurements on the same sample described in Fig. 33a as a function of - dV/dt scan rate.

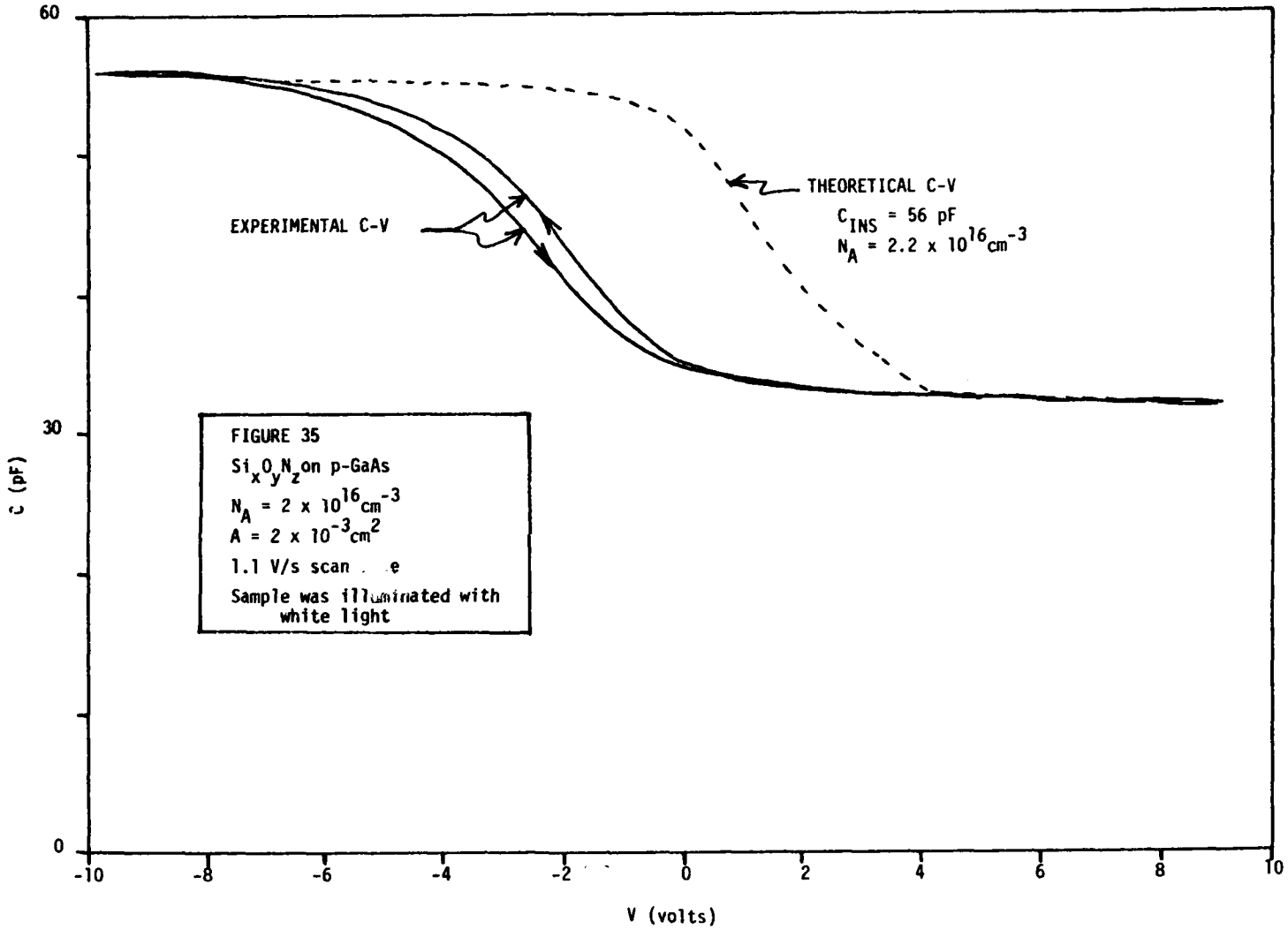


Fig. 35 C-V measurements on the same sample described in Fig. 33a but illuminated with white light. Theoretical curve (dashed) calculated for parameters shown in figure.

considerably shorter. Thus, under positive bias, initially deep depletion is observed. After the inversion layer builds up, the C-V scan shows transient effects. This is verified by the theoretical calculation of the C-V characteristics as shown by the dashed line in Fig. 35. From the shift of the flatband voltage, the interface state density can be estimated to be about 5×10^{11} cm^{-2}. A reduction in this density by about a factor of 10 would be sufficient to produce a device quality interface.

A heater was added to the system in order that the sample could be heated prior to deposition. Such a procedure is necessary to take advantage of the As coating technique described in Section III 2. With this technique an As overlayer is deposited on a sample in situ within the MBE growth chamber. This overlayer can subsequently be removed at a relatively low temperature by heating the sample in the $Si_xO_yN_z$ deposition chamber prior to $Si_xO_yN_z$ deposition. In this way, the formation of native oxide on the surface should be minimized.

Initial results indicated that the arsenic was removed in part by the reaction of a forming-gas plasma with the coated substrate. After the initial reaction a residue remained which was not attacked by the plasma and which could only be removed by subsequent heating to temperatures above 400°C. Due to the residual film, $Si_xO_yN_z$ layers formed without the subsequent heating showed poor morphology and were filled with pinholes resulting in devices with large leakage currents. Films formed by heating above 400°C had much lower leakage curents ($\sim 4 \times 10^{-10}$ amps at 10 V with area = 2×10^{-3} cm^2).

A C-V curve for sample #595 from which the As° protecting layer was removed by heating prior to $Si_xO_yN_z$ deposition is shown in Fig. 36. This C-V curve shows very strong pinning, in fact considerably more than observed (Fig. 33a) for samples which were etched in HF with no other kind of surface treatment. For preparation of samples with low interface-state densities by the As overcoating technique a cleaner system may be necessary. The LFE system used was not capable of providing an ultraclean low oxygen environment. During the

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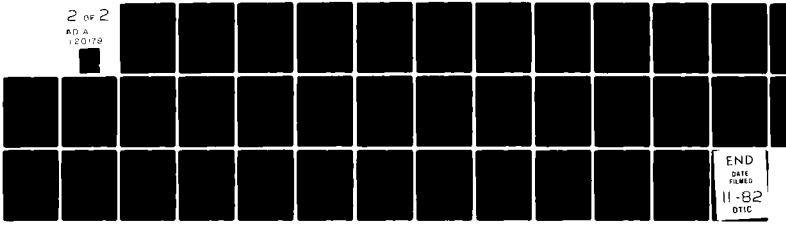

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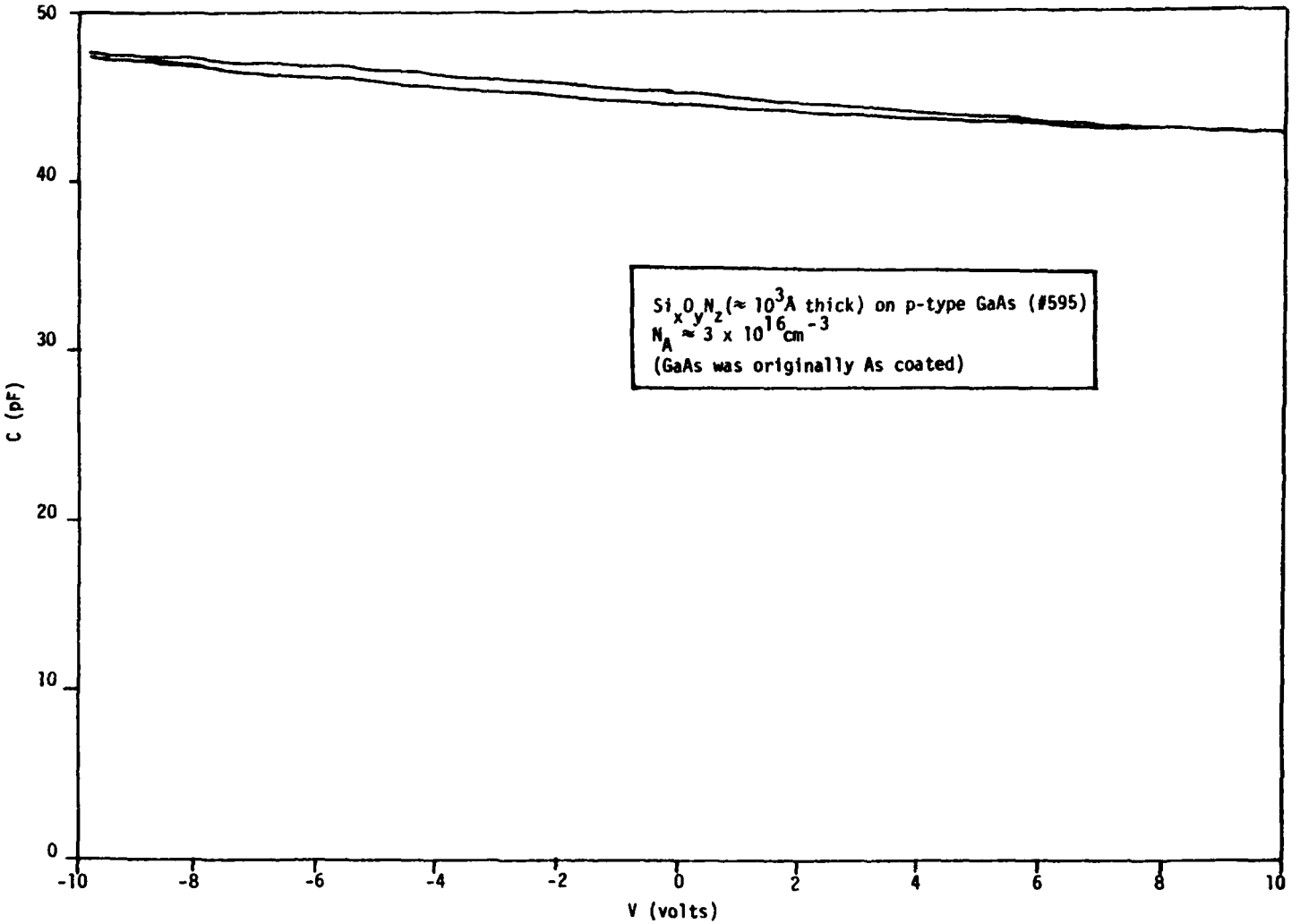

Fig. 36 C-V for $Si_xO_yN_z$ deposited on MBE grown sample #595 which had been protected by As° prior to deposition.

heating cycle the surface may have reacted with oxygen and as shown below, the $Si_xO_yN_z$ film composition contained substantial oxygen.

The $Si_xO_yN_z$ film composition produced in the LFE PDS/PDE plasma etcher was analyzed by XPS. A typical XPS spectrum from such a sample is shown in Fig. 37. The sample had been sputtered (3.5 keV Ar^+) in an effort to remove the surface contamination. The important feature is the large oxygen peak in the spectrum. Although this peak is observed to decrease somewhat as the film is sputtered away, the film seems to contain always more than 30% oxygen. Due to the high reactivity of oxygen with silane, such a reaction is hard to avoid in a system which is not initially pumped to pressures below 10^{-6} torr. The LFE system is not compatible with this kind of pumpout procedure. The substantial presence of oxygen in the $Si_xO_yN_z$ indicates that the surface of the As° protected MBE grown film may not have been as clean as anticipated and may explain the strong surface pinning observed in Fig. 36. It is suspected that native oxides present in even very small amounts at the GaAs interface may produce a substantial density of interface states. In an effort to prepare and maintain (prior to insulator deposition) as clean a GaAs surface as possible, a UHV deposition system was developed. Experiments which utilized this system are discussed in the next section.

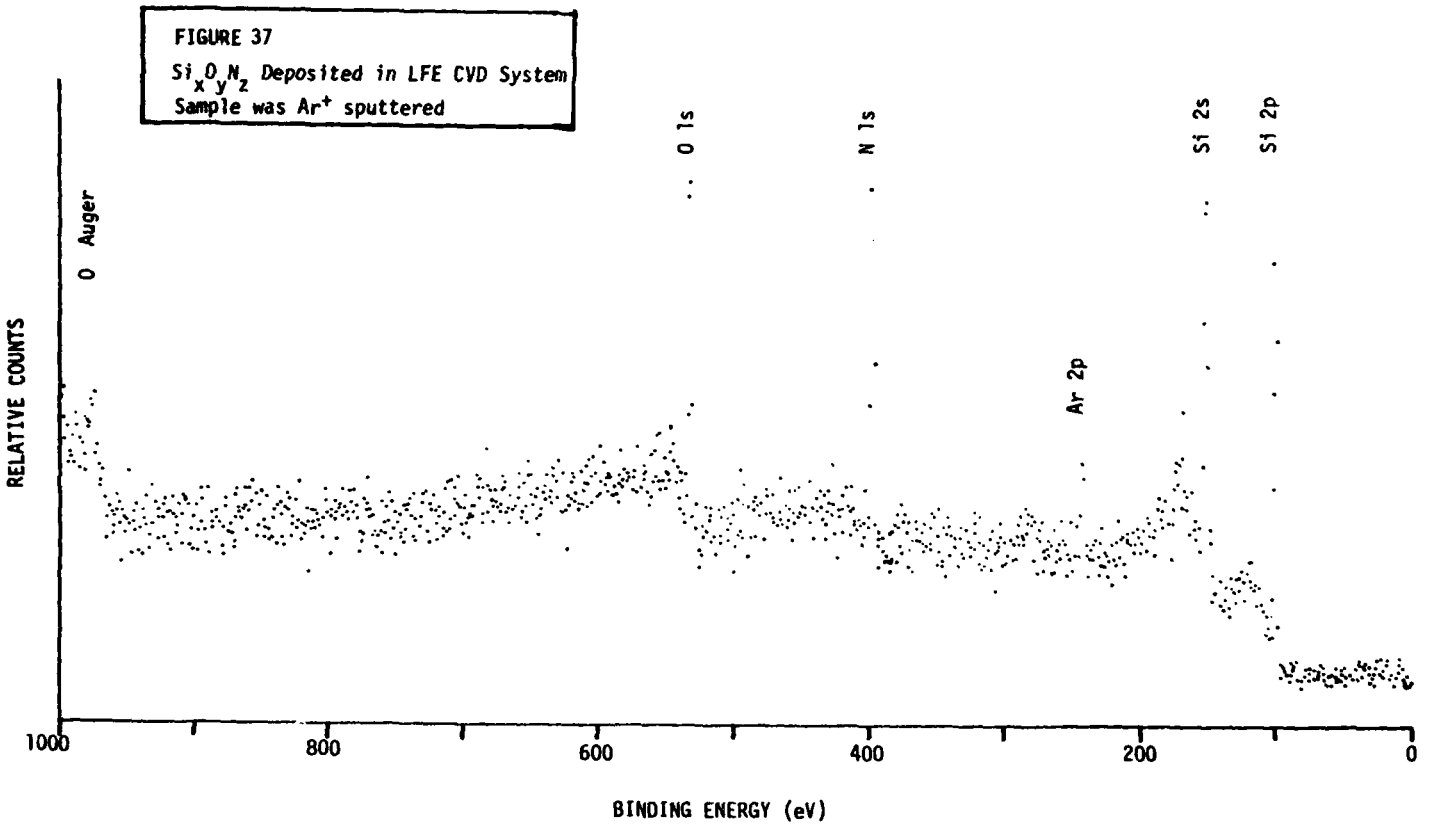

Fig. 37 XPS spectrum of $Si_xO_yN_z$ film prepared in the LFE PDS/PDE plasma etcher after removal of surface contamination by Ar^+ sputtering.

VII. DEVELOPMENT AND APPLICATIONS OF UHV DEPOSITION SYSTEM

It has been observed[23] that a wide variety of materials, including oxygen, cause Fermi-level pinning when deposited onto clean cleaved GaAs (110) surfaces even at coverages as small as a fraction of a monolayer. The clean cleaved GaAs (110) surface does not exhibit Fermi-level pinning.[10,11] Thus very small amounts of native oxides present on the GaAs surface prior to insulator deposition may be responsible for substantial interface state densities. To minimize even very low level oxygen contamination it may be necessary to utilize a UHV insulator deposition system. The LFE system discussed in the last Section (VI) was not compatible with UHV operation. Thus development work on a new ion pumped UHV system was initiated. After bakeout the system base pressure is in the 10^{-10} torr range. The system is equipped with a mass analyzer so that the composition of the residual gas can be monitored. A heated sample holder was added to the system to facilitate As removal from MBE grown As overcoated GaAs samples (see Section III 2). Initial system operation showed that base pressures of $< 5 \times 10^{-9}$ torr could be routinely obtained after a 1 day pumpdown and bakeout procedure.

1. Evaporated Insulators

Our first attempts at insulator deposition with the UHV system involved Ge_xN_y and Na_3AlF_6 (cryolite). The GaAs was part of sample #595 ($N_A = 3 \times 10^{16}$ cm^{-3}) which has been previously described; the As overlayer coating was removed by heating the sample in vacuum at $\approx$ 450°C. $Ge_xO_yN_z$ has been found to give encouraging results when deposited on GaAs; the MIS samples have low leakage and low interface state densities.[24] We attempted to evaporate Ge_xN_y onto GaAs by using material obtained from a commercial vendor. The film which was obtained on the GaAs was subsequently examined by using XPS. These results are shown on Fig. 38. We observed Ge and O in the film, but no nitrogen. The gas analyzer in the high vacuum deposition system indicated a large evolution of nitrogen during the evaporation which suggests that the Ge_xN_y starting material was decomposing. Examination of the starting

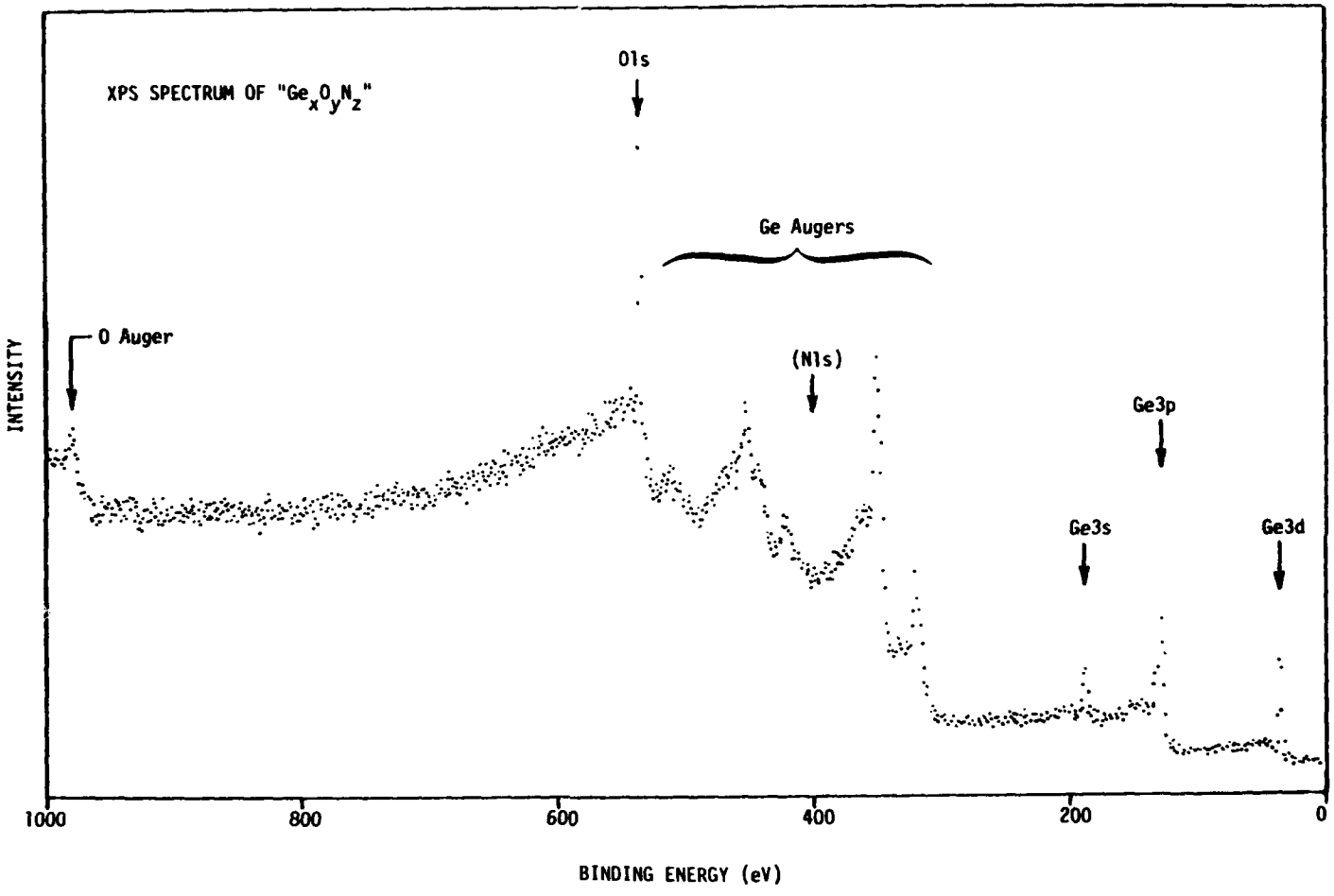

Fig. 38 XPS spectrum of film obtained by evaporation of Ge_xN_y in UHV system.

material by XPS indicated that it was contaminated by oxygen. Thus, apparently the starting material, $Ge_xO_yN_z$, decomposes on heating so that a GeO_2 film is deposited on the GaAs.

The GeO_2 films in general showed poor adhesion and durability. I-V measurements indicated relatively high leakage ($> 10^{-5}$ amp at < 5 V for 2×10^{-3} cm^2 dots on a $\sim$ 1000 Å thick film). C-V measurements are shown for one of these samples in Fig. 39. The curves indicate that there is strong surface pinning.

Na_3AlF_6 was also evaporated onto a cleaned GaAs substrate. XPS analysis indicated a relatively pure film. Unfortunately, the films that we produced tended to have high leakage currents and low breakdown voltages. A typical C-V curve is shown in Fig. 40. These characteristics suggest depletion and accumulation with low hysteresis. However, due to the sizable leakage currents, these data should be interpreted with caution.

2. Reactive Deposition of Nitrides

The reactive deposition of nitrides on oxide free GaAs surfaces was investigated. Experiments were carried out to prepare Ge_xN_y, Al_xN_y and Si_xN_y by thermally evaporating Ge, Al, and Si in a high purity ammonia ambient (about 10^{-3} to 10^{-4} torr) onto clean GaAs substrates (the substrates were at temperatures between room temperature and $\approx$ 600°C). The oxide free GaAs surface was prepared by using an As overcoated MBE grown GaAs sample (#595) on which the As was removed by thermal evaporation. Preliminary results indicate that insulating films can be prepared by using either Ge or Al as the source material; however, deposition of an insulating film was not observed for Si evaporation.

XPS measurements indicated that oxygen was present in the films prepared by using Ge or Al. The compositions of these films actually were Ge_xO_y and $Al_xO_yN_z$. The oxygen contamination in this series of experiments was found to be at least partially due to a leaky valve on the ammonia cylinder.

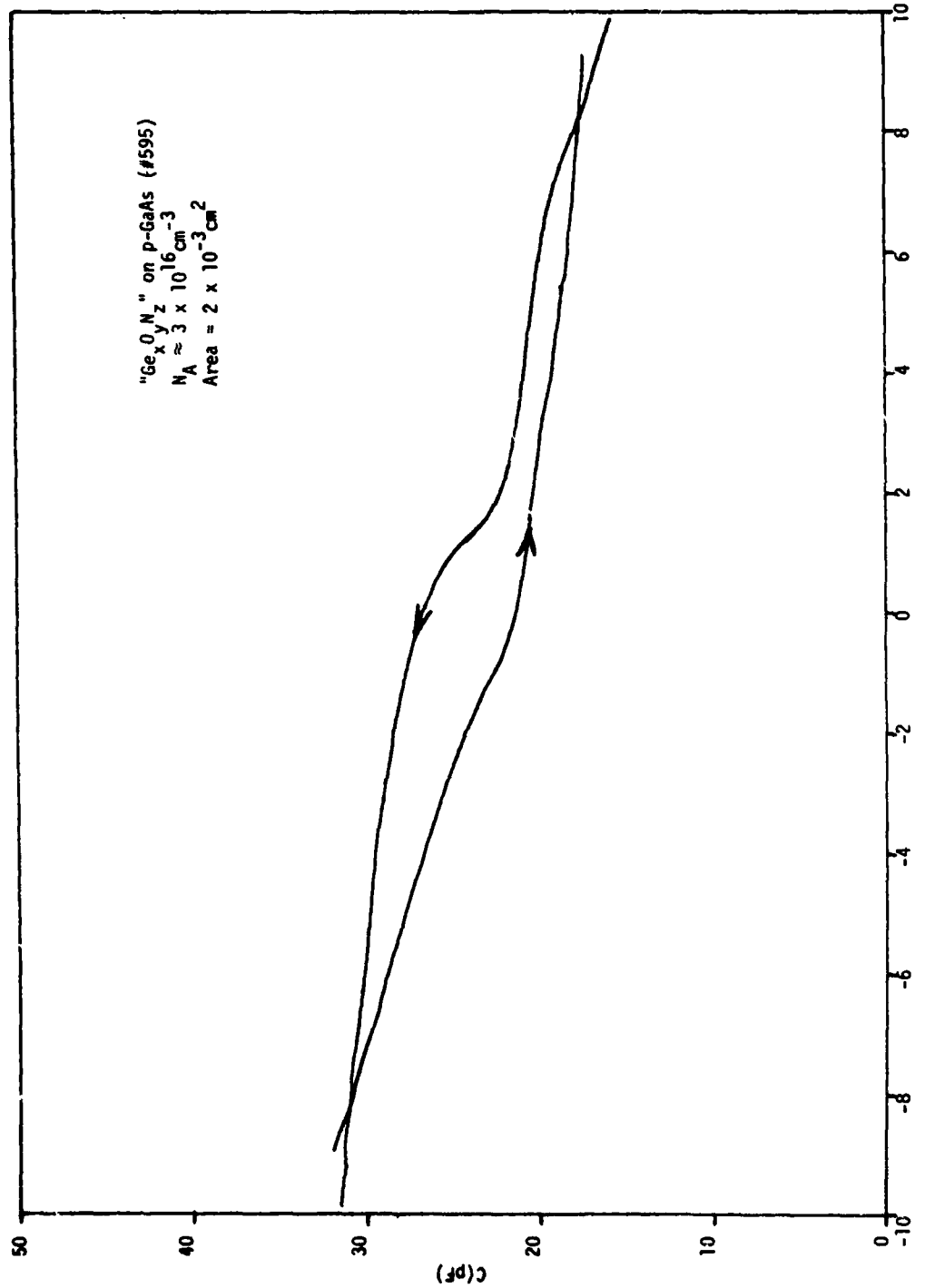

Fig. 39 C-V measurements of GeO_2 film deposited on sample #595.

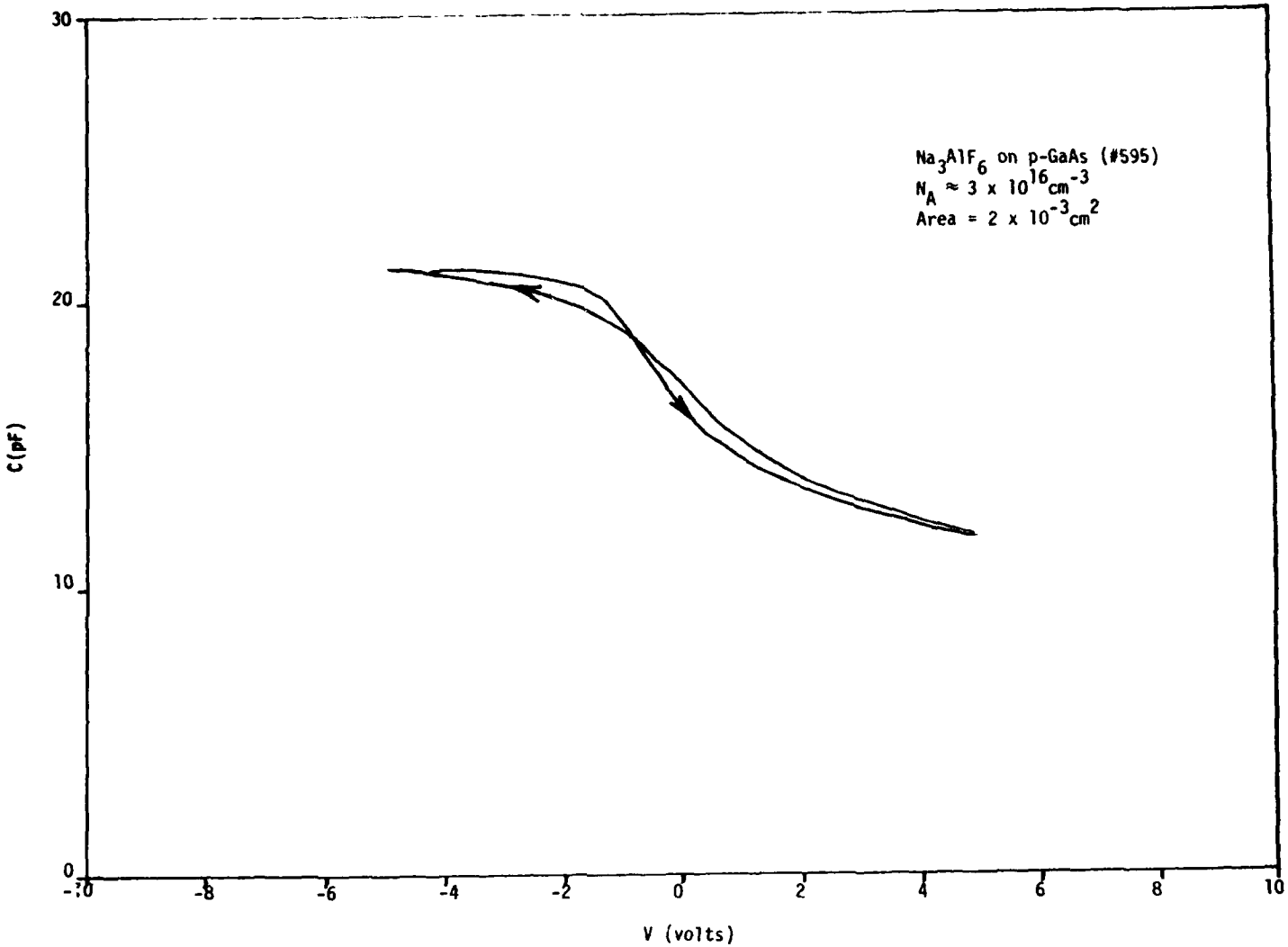

Fig. 40 C-V measurements of Na_3AlF_6 film deposited on sample #595.

The results of C-V and I-V measurements on the Ge_xO_y films were similar to those discussed in Section VII 1. Two $Al_xO_yN_z$ films were prepared; one was found to be moderately insulating whereas the other showed considerable leakage. XPS measurements showed that the better insulating film contained more nitrogen. This film was prepared with the GaAs substrate in the temperature range of 400-600°C (the UHV deposition system as yet has no good means to control the substrate temperature). Results of C-V and G-V measurements are shown in Fig. 41. The C-V measurements show evidence of both accumulation and inversion. The G-V measurements show a peak at 1-2 V reverse bias. The hysteresis is moderate (1-2 V) and would correspond to an interface charge of $\approx 5 \times 10^{11}$ cm^{-2}. These results are encouraging because it was known that oxygen was contaminating the system. Consequently, further experiments aimed specifically at characterizing the AlN/GaAs interface were performed and are described in the next section (VII 3).

3. AlN Deposition

At the conclusion of this program a final set of experiments was carried out in an effort to prepare and characterize the AlN/GaAs interface. Difficulties experienced with oxygen contamination of the ammonia source (mentioned in Section VII 2) were corrected by obtaining a new cylinder of high purity (6 nines) ammonia.

The reactive deposition technique utilized to prepare the AlN is similar in some respects to MBE. The substrate is initially cleaned in UHV by heating to a temperature high enough to remove native oxides from the surface or by using the As protected MBE grown surface technique which is described in Section III 2. Following the substrate cleaning procedure the sample is heated to a suitable temperature in the presence of an ammonia flux from a gas nozzle and an aluminum flux from a heated source. Under appropriate conditions, the ammonia reacts with the aluminum to form a film of aluminum nitride on the surface of the GaAs substrate. Such a procedure can be contrasted with normal MBE growth of aluminum arsenide where the growth apparatus is similar

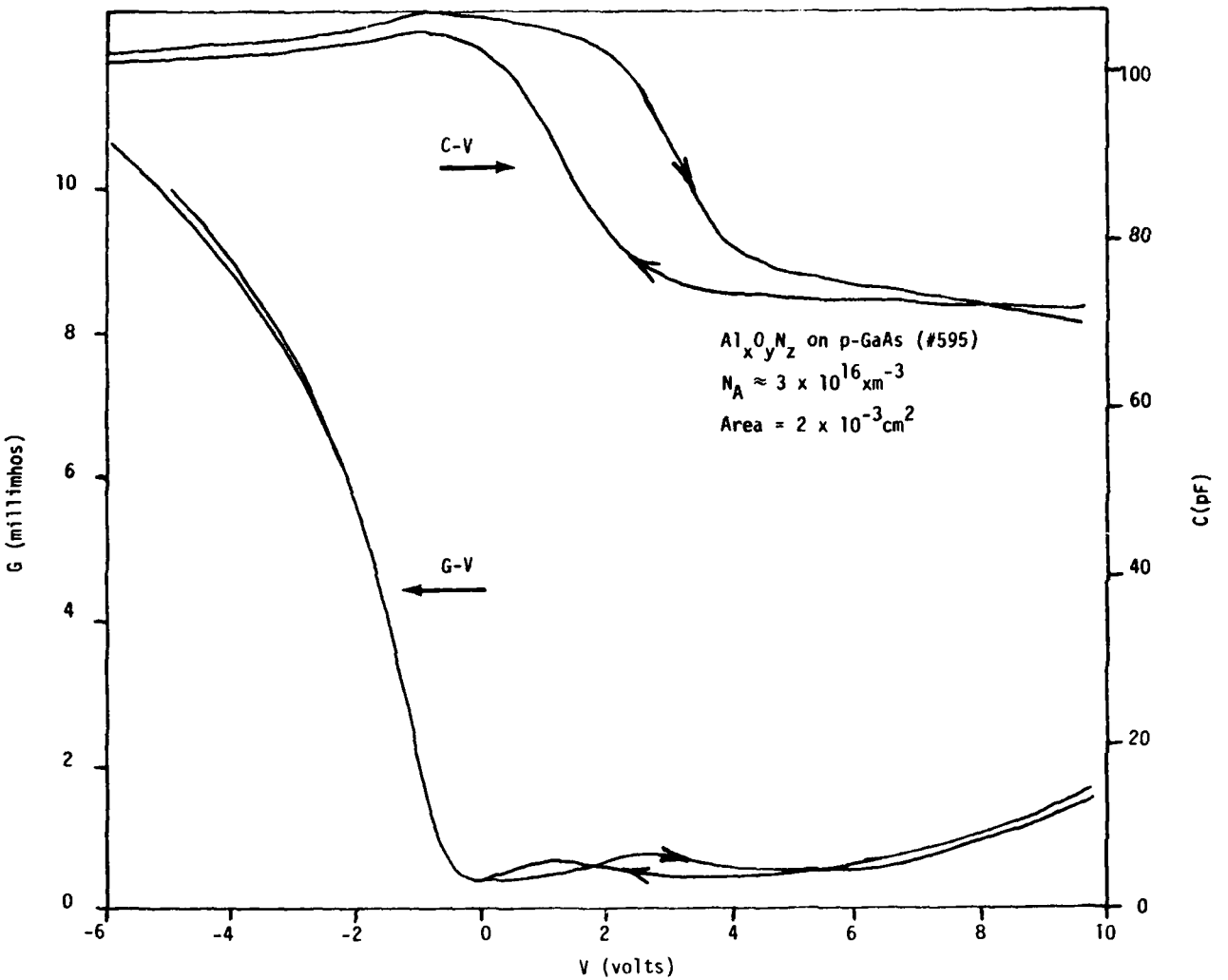

Fig. 41 C-V and G-V measurements for $Al_xO_yN_z$ film deposited on sample #595.

except that the ammonia flux is replaced by an arsenic flux. In both cases the sticking coefficient of the aluminum is close to 1 whereas the effective sticking coefficient of the reacting ammonia or the arsenic depends on the amount of absorbed aluminum.

The last set of experiments were carried out by using bulk grown p-type GaAs (100) sustrates. Preliminary studies indicated that the substrate must be heated to obtain good insulating films; this implies a thermally activated process for the AlN formation. The substrates were heated to ≈ 500°C in an ammonia flux which resulted in a system pressure of 10^{-5} to 10^{-4} torr. Al was deposited onto this heated susbtrate. I-V and C-V measurements on MIS capacitors produced from these samples were performed and the results are shown in Figs. 42 and 43. Figure 42 shows the I-V characteristics of an MIS capacitor on p-type GaAs, $N_A \sim 3 \times 10^{16}$ cm^{-3} in forward bias. At the voltage of -10 V across the device we measure a leakage current of 10^{-9} amps showing the excellent insulating properties of the AlN layer. The C-V characteristics for the same device are shown in Fig. 43. Although there is substantial hysteresis in the C-V curves, the curves show flat regions at strong forward and reverse bias, suggestive of accumulation and inversion conditions occurring in the device. Also presented in the figure is a theoretical curve for an ideal MIS structure calculated for C_i = 75 pF and $N_A \simeq 1.2 \times 10^{16}$ cm^{-3}. Very similar shapes of the theoretical and experimental curves are obtained without invoking large interface state densities. This strongly suggests that both accumulation and inversion are being observed. The sharp transition between the inversion and accumulation portions of the C-V curve supports this interpretation. If a large density of interface states were present, we would expect a much broader transition region. As indicated on the figure the hysteresis in the C-V curve can be accounted for by assuming a fixed interface charge. We feel that this hysteresis is primarily due to trapping at levels in the AlN insulator which occurs when carriers are injected from the semiconductor or metal. Since these results are only preliminary we do not consider the hysteresis to be discouraging. Also, as discussed previously, annealing treatments may help to reduce the hysteresis.

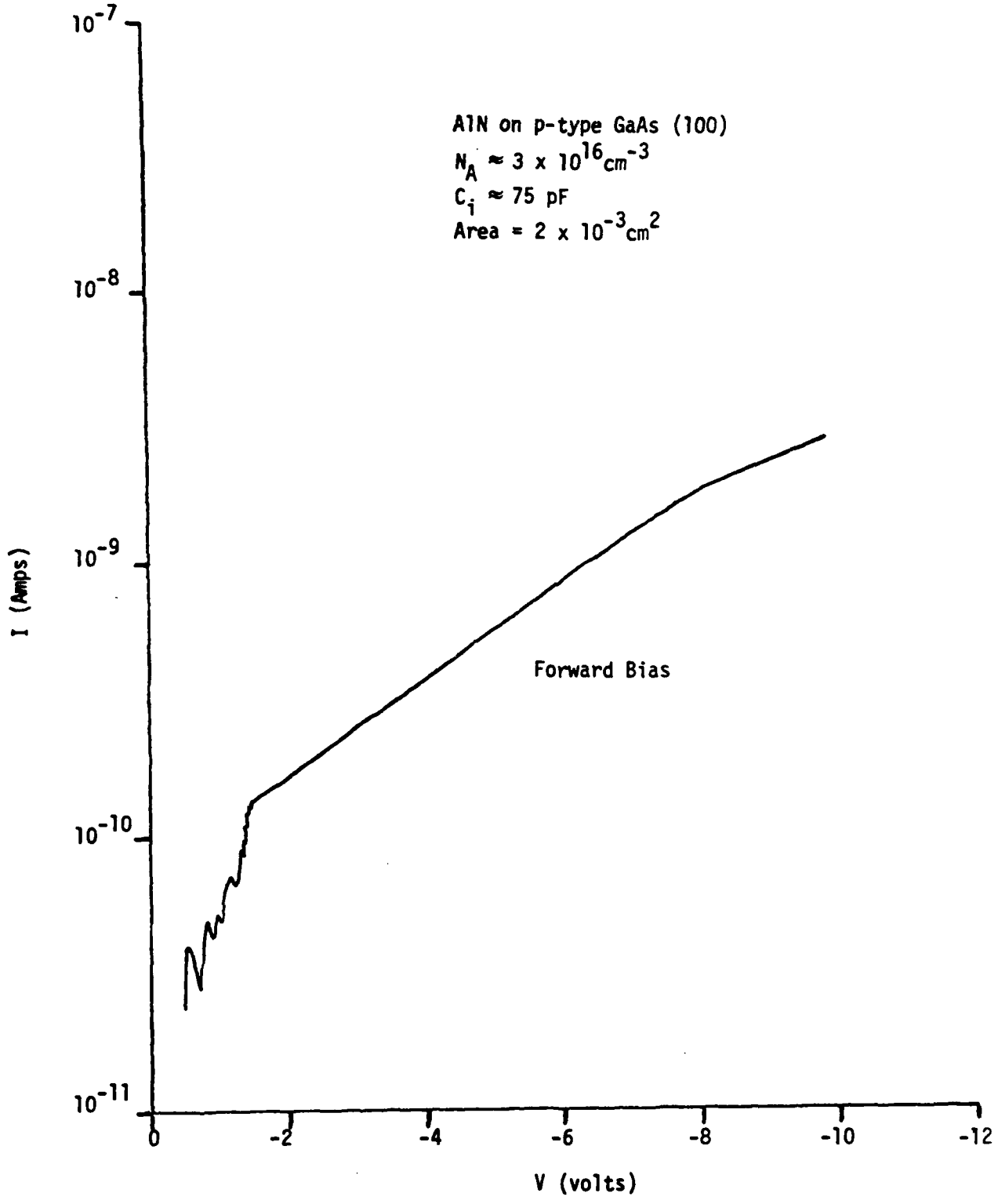

Fig. 42 I-V measurements for an AlN film deposited on sample #595.

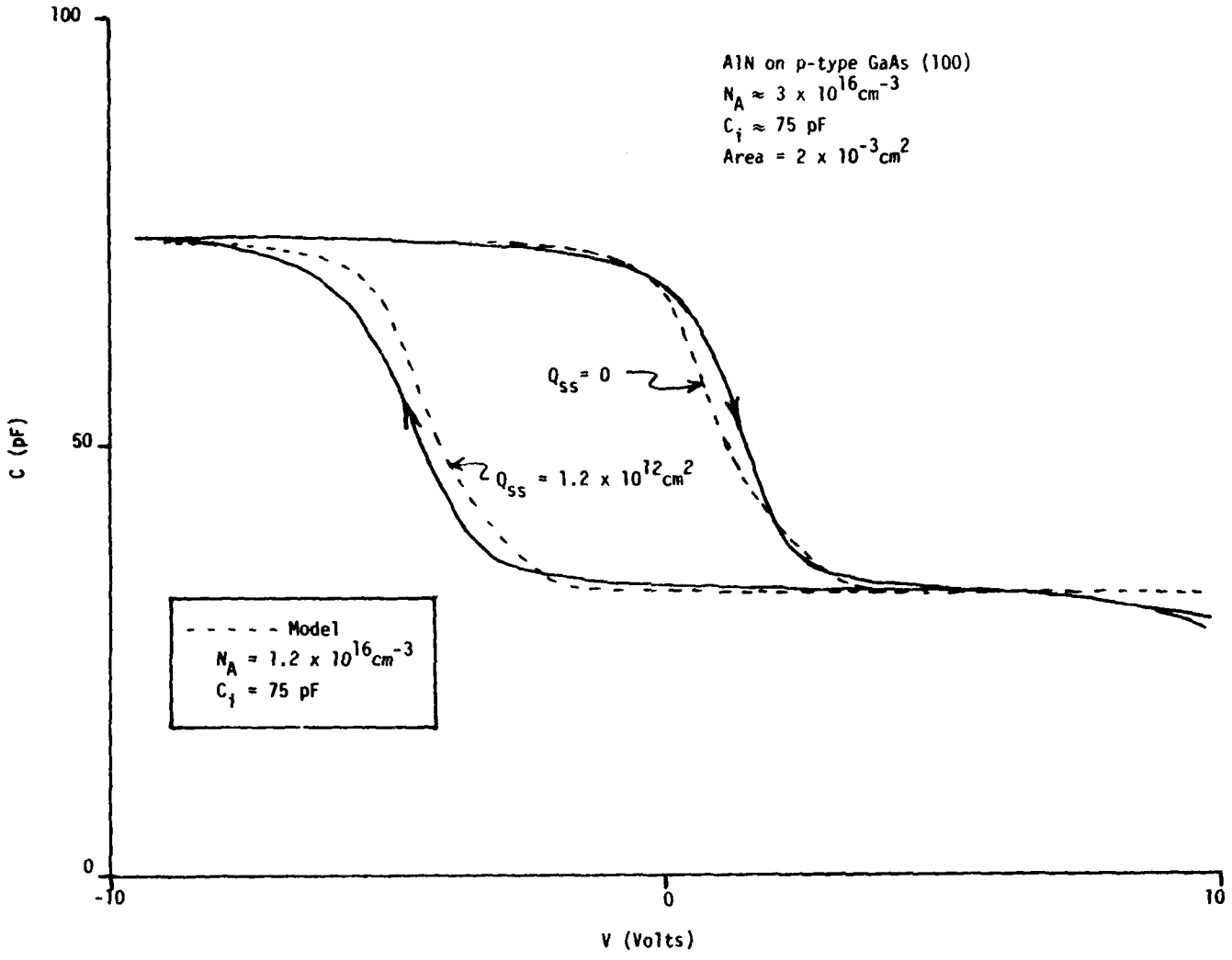

Fig. 43 C-V measurements for the same capacitor described in Fig. 42.

We have also made some variable frequency C-V measurements on these devices. These results are quite similar to those discussed above and indicate very low dispersion in the C-V characteristics at frequencies as low as 100 Hz. These results support our interpretation of the C-V characteristics since the capacitance associated with a large density of interface states could lead to a great deal of frequency dispersion in the C-V characteristics.

Although the AlN/GaAs MIS results reported here are very preliminary, we believe they are encouraging and should be pursued further. There are several reasons why the AlN/GaAs interface could be attractive for MIS applications. These reasons are discussed in the next Section (VIII).

VIII. RATIONALE FOR FURTHER STUDY OF AlN/GaAs MIS STRUCTURES

By far the largest effort to develop a practical GaAs MIS technology has involved the use of native oxides as insulators. This effort was motivated in part by the remarkable success achieved with the SiO_2/Si MIS structure. The basic oxidation techniques that have been tried for GaAs MIS device applications include anodic, thermal, and various types of plasma oxidation. In addition some deposited oxide insulators have been studied. A few references to those previous efforts have already been given in this report. No effort to provide a complete set of literature references will be made; instead it is noted that reasonably extensive literature coverage can be found in other published works.[25-28] Although some of the results reported in these previous studies which involve oxides show promise, it is clear that no generally useful GaAs/oxide interface has yet been discovered. Most C-V measurements reported in these previous oxide studies show large hysteresis, flat band voltage shifts, and deep depletion characteristics. Of course, it has been suggested[4] that a possible way to avoid these difficulties is to fabricate an oxide/$Al_{1-x}Ga_xAs$/GaAs structure. Our own efforts (Section IV) and those of others[14] suggest that it will be as difficult to obtain a useful oxide/$Al_{1-x}Ga_xAs$ interface as it is to obtain a good oxide/GaAs interface.

Two major difficulties seem to be encountered in trying to use an oxide as an MIS insulator for GaAs. The first difficulty was already mentioned in Section VII and involves the fact that photoemission studies[23] have observed that Fermi level pinning of GaAs (110) surfaces occurs for even small fractional monolayer coverages of oxygen. It has been suggested[23] that this observed Fermi-level pinning is due to the formation of defects near the metal/GaAs interface and it is further suggested that the driving force for defect formation comes from the heat of adsorption of the material being evaporated onto the semiconductor surface. The evidence in support of a defect model for Fermi-level pinning at compound semiconductor interfaces has been recently reviewed.[29,30] These defects may be a source of interface states.

The second difficulty involves the instability of the oxide/GaAs interface. The chemistry associated with oxidation of III-V compounds is complex and has recently been reviewed.[31,32] The most common oxides present on a GaAs surface are Ga_2O_3 and As_2O_3. It has now been clearly demonstrated[33,34] that As_2O_3 present in the interface, is unstable and is reduced to form elemental As. Phase diagram studies[35] indicate that the reaction $As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As$ is favored thermodynamically and readily occurs. It has been suggested[36] that elemental arsenic may be a major source of interface traps and thus play a significant role in determining GaAs MOS characteristics. Even when non-oxygen containing deposited insulators are used, the initial GaAs surface will in general have several monolayers of native oxide present prior to deposition. The presence of these few monolayers of oxides may be sufficient to cause unacceptable densities of interface states from either a defect and/or elemental As formation origin.

It is necessary to consider how one might eliminate these potential sources of interface states. The use of an oxygen free insulator deposited onto an atomically clean GaAs surface should eliminate the difficulty encountered with elemental As formation. In addition, by using a wide bandgap III-V compound as the deposited material, it should be possible to minimize defect related interface levels. The isoelectronic nature of a wide bandgap III-V compound relative to GaAs could minimize intrinsic defects (e.g., vacancies and antisites) and extrinsic states due to the formation of electrically active centers associated with impurities.

Only a few III-V compounds are suitable for use as insulators on semiconductors. Table 4 shows the properties of some of these materials. For good insulating behavior the compound should have a bandgap in excess of 3 eV, preferably as high as possible. Of these the nitrides BN, AlN and GaN and the phosphide BP would be expected to have good insulating properties.

Table 4

Properties of Insulating III-V Compounds

Compound	E_{gap} (eV)	Structure	Lattice Constant(s) A
BN	~ 7.5	Zincblende	a = 3.62
		Wurtzite	a = 2.55, c = 4.23
AlN	6	Wurtzite	a = 3.11, c = 4.98
BP	~ 6	Zincblende	a = 4.54
GaN	3.4	Wurtzite	a = 3.18, c = 5.16

BP and GaN are not stable with respect to heating and must be ruled out as useful materials. In addition, the low purity of most BP renders it conducting.

The most promising materials for use as insulators are AlN and BN. Of these AlN is easier to produce. Whereas many impurities form electrically active centers in GaAs, both Al_{Ga} and N_{As} are electrically inactive and the material is stable in vacuum to high temperatures. Also, unlike most Al containing III-V compounds, AlN is also stable in air. The large bandgap of AlN (6 eV) makes it normally a very good insulator. It can be prepared relatively easily by a number of techniques. AlN and GaAs have virtually identical thermal expansion coefficients. As a result, strain at the GaAs/AlN interface associated with thermal cycling is minimal and good adhesion is normally obtained. This makes AlN a superior capping material for ion implantation studies.[37]

In addition, there is reason to believe that the growth of AlN on a GaAs surface will help to eliminate intrinsic defect related states. As mentioned above, a large density of such states may be produced near a GaAs surface by exposure to oxygen, by exposure to other contaminants, or by surface damage. There will be a tendency for Al and N to annihilate such

defects. For example, if the defects are surface vacancies the reactions $V_{As} + N \rightarrow N_{As}$ and $V_{Ga} + Al \rightarrow Al_{Ga}$ can occur. The resulting electrically inactive N_{As} and Al_{Ga} centers should not have detrimental effects on the MIS properties of the AlN/GaAs interface.

We believe that the considerations presented in this section coupled with the encouraging preliminary experimental results reported in Section VII 3 provide a basis for justifying further study of the AlN/GaAs interface for MIS applications.

IX. SUMMARY

In Phase 2 of this program two approaches were pursued in an attempt to obtain a useful GaAs MIS technology. The first approach involved the utilization of lattice matched MBE grown $Al_{1-x}Ga_xAs$ interfaces which presumably have a low interface state density because of the success achieved in the fabrication of high quality optoelectronic devices with this heterojunction. The insulator is formed on the $Al_{1-x}Ga_xAs$ surface which results in an insulator/$Al_{1-x}Ga_xAs$/GaAs MIS device structure. Several attempts were made to reproduce the promising C-V results reported by Tsang et al[4] in which the insulator is formed by thermal oxidation (in O_2) of an outer AlAs/$Al_{1-x}Ga_xAs$ layer. C-V results showed only deep depletion characteristics with substantial hysteresis. A persistant problem with all the MIS devices was that the thermal oxide was a relatively poor insulator. In an effort to improve the quality of the insulator the thermal oxide was replaced by plasma oxidation of the $Al_{1-x}Ga_xAs$ layer and by deposition of $Si_xO_yN_z$ and Ta_2O_5. In both cases substantially improved leakage characteristics of the MIS devices were obtained. However, the C-V characteristics of the resulting MIS devices were quite similar to those obtained by using the thermal oxides. It was concluded that the bandgap of $Al_{1-x}Ga_xAs$ (E_g for AlAs is 2.2 eV) is not large enough to prevent charge transfer from GaAs to the insulator/$Al_{1-x}Ga_xAs$ interface. This suggests that the inherent problem of having a large density of states at the insulator/GaAs interface is transfered to the insulator/$Al_{1-x}Ga_xAs$ interface and that it may be as difficult to obtain useful insulator/ $Al_{1-x}Ga_xAs$ interfaces from an MIS viewpoint, as it is to obtain good insulator/GaAs interfaces. The C-V results of Ref. 4 have been reanalyzed and some apparent internal inconsistency was found.

Investigations of oxides deposited on GaAs surfaces were carried out in the UHV environment of the XPS sample preparation chamber. Reasonably good dielectric properties were obtained for a SiO_2 film prepared by a photochemical process which involved SiO_x evaporation. This material was deposited on GaAs surfaces which had been thermally cleaned and on which thin layers of

Ga_2O_3 had been formed. C-V measurements showed deep depletion and large hysteresis characteristics which suggested that it will be difficult to use a deposited oxide as the dielectric for a GaAs MIS structure.

Techniques to deposit non-oxygen containing insulators on GaAs surfaces were investigated. An LFE PDS/PDE plasma etcher was modified to facilitate $Si_xO_yN_z$ deposition. MIS measurements and XPS determination of the $Si_xO_yN_z$ composition suggested that a UHV environment would be necessary to obtain an oxygen free insulator/GaAs interface.

An ion-pumped UHV insulator deposition system was developed (base pressure in the 10^{-10} torr range). Although only a limited number of experiments were carried out with this system (which is in need of further refinement for optimum performance) some promising results were obtained with the AlN/GaAs interface. This interface was prepared by a reactive deposition process which involved evaporating Al onto a thermally cleaned and heated GaAs substrate in an NH_3 ambient. Excellent insulating properties were obtained for the AlN layer. Although the C-V measurements for MIS structures fabricated with the AlN/GaAs interface showed large hysteresis, the curves show flat regions at strong forward and reverse bias which suggest the attainment of accumulation and inversion. The shape of the C-V curves can be adequately modeled without invoking large interface state densities and the hysteresis can be accounted for by assuming a fixed interface charge which may be due to trapping at levels in the AlN. Based on recent experimental and theoretical studies, there are several reasons why one might expect the AlN/GaAs to be attractive for MIS applications. It is suggested that further study of this interface would be useful.

During the study of MBE grown samples in this program, a novel method of protecting reactive $Al_{1-x}Ga_xAs$ surfaces from degradation due to air exposure was developed. The technique involves cooling the MBE grown sample to slightly below room temperature in an As_4 flux from the As MBE source. In this manner a $\sim 10^3$ Å thick layer of As° is deposited onto the sample surface. The sample can then be removed and transferred in air into another

UHV system. After UHV conditions are again achieved, the As° layer can be removed by heating to > 300°C. XPS and LEED studies have shown that the resulting $Al_{1-x}Ga_xAs$ surface is free of contamination and well ordered. In addition, XPS surface potential measurements indicated an unusually low band bending for p-type GaAs (100) and (110) surfaces heated to ≈ 360°C. These surfaces may be promising candidates for future GaAs MIS applications which involve deposited insulators.

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APPENDIX I

Three papers were published based on work supported or initiated by this program. These papers which are reproduced in this appendix are:

1. "Protection of Molecular Beam Epitaxy Grown $Al_xGa_{1-x}As$ Epilayers During Ambient Transfer," J. Vac. Sci. Technol. 19, 255 (1981).

2. "Reactivity and Interface Chemistry During Schottky-Barrier Formation: Metals on Thin Native Oxides of GaAs Investigated by X-Ray Photoelectron Spectroscopy," Appl. Phys. Lett. 38, 167 (1981).

3. "Interfacial Chemical Reactivity of Metal Contacts with Thin Native Oxides of GaAs," J. Vac. Sci. Technol. 19, 611 (1981).

Protection of molecular beam epitaxy grown $Al_xGa_{1-x}As$ epilayers during ambient transfer

S. P. Kowalczyk, D. L. Miller, J. R. Waldrop, P. G. Newman, and R. W. Grant

Rockwell International, Microelectronics Research and Development Center, Thousand Oaks, California 91360

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A method for the protection of reactive compound semiconductor surfaces during transfer from a molecular beam epitaxy apparatus through ambient for further processing or experimental characterization is demonstrated for GaAs and AlAs. This method is likely to be applicable to other compound semiconductors.

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Molecular beam epitaxy (MBE) has become a powerful technique for the fabrication of epilayers and abrupt heterojunctions of compound semiconductors.[1] One of the most important compounds is the ternary $Al_xGa_{1-x}As$, which has such applications as solar cells, heterojunction lasers, and field-effect transistors. Surfaces of this material are especially reactive near $x = 1.0$. It is of interest to investigate the surface properties of these materials, particularly the surface atomic geometry and the interfacial reactions which occur with deposited metals, insulators, or controlled gas exposure. MBE is an attractive epitaxial growth technique for the preparation of single crystal semiconductor surfaces because of the ultrahigh vacuum (UHV) ambient. A typical MBE apparatus contains, however, a limited amount of surface analytical instrumentation. Although several systems designed to combine MBE growth with extensive analysis capabilities are available commercially, they are very expensive. Thus it is useful to have a simple procedure to transfer a MBE grown sample to another vacuum system through ambient while preserving its clean ordered surface. Two approaches to this type of sample transfer have been tried previously. One is the use of an UHV transfer device.[2] This presupposes compatibility of the transfer device with both the MBE system and the systems to which the sample is being transferred. Such a device can often be very complicated mechanically. Also for a sample such as AlAs, which is extremely reactive, the transfer device is required to operate in the 10^{-10} Torr range. A second technique is to deposit a less reactive material as a protective coating; the coating is removed by ion milling after the transfer.[3,4] This technique is not suitable for studying very thin films of ~20 Å thickness, and may be difficult to apply to very reactive materials. For some applications, sputter damage of the resulting surface may be a complication.

In this communication, we report a relatively simple technique for transferring reactive compound semiconductor samples from an MBE system to other UHV systems through air while preserving the as-grown surface. This technique did not require addition to or modification of the MBE system. We have demonstrated this technique for AlAs, GaAs and for AlAs–GaAs and GaAs–AlAs heterojunctions. The method we have developed is based on the use of a protective elemental As overlayer. The semiconductor layers are grown by MBE on GaAs substrate material in the conventional manner.[1] The GaAs substrates are mounted with In to Mo plates which are then clamped tightly to our standard MBE substrate holders by using Ta screws. This allows the samples to be demounted from the MBE holder without heating to melt the In solder. After growth of the desired semiconductor layer, a protective layer of elemental As is deposited. The thickness of this layer is usually greater than 100 Å, although we have successfully used an As layer as thin as ~25 Å. The sample is then transferred from the MBE apparatus *through air* to another apparatus. In our case, about ten samples have been transferred from an MBE system (constructed at Rockwell International) to an x-ray photoelectron (HP5950A) spectrometer—LEED system. This step takes about 15 minutes. Once the sample is under the desired vacuum conditions (for AlAs, in the 10^{-10} Torr range), the specimen is heated gradually to ~300°–350°C to desorb the As overlayer. This yields an atomically clean and ordered AlAs surface as determined by XPS and LEED.

The key step of this protective method is the growth of the As overlayer. Arsenic is condensed on the surface of the epitaxial layers as rapidly as possible following the epilayer growth. This As comes from the arsenic beam used during the growth of the epilayers, and consists of As_4 derived from the

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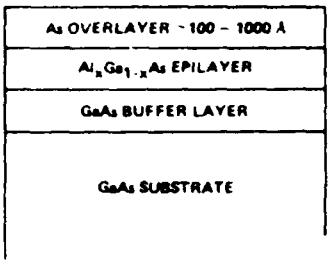

FIG. 1 A typical structure grown by MBE in this study and successfully transferred to an XPS apparatus without contamination of the $Al_xGa_{1-x}As$ surface

sublimation of elemental arsenic. The metal (Ga and/or Al) and dopant sources are abruptly shuttered to terminate the layer growth, while the As_4 beam remains impinging on the surface of the wafer. At typical MBE growth temperatures (550°–650°C), no condensation of As occurs (As has a very low sticking coefficient to itself at these temperatures) but the As_4 beam prevents surface decomposition. At the conclusion of epilayer growth, the substrate heater is turned off and the edge of the substrate holder is brought into contact with the MBE system's liquid nitrogen cooled shroud to speed cooling of the holder. The substrate remains within the central portion of the As_4 beam. After the temperature falls below ~450°C, the As_4 flux is reduced by ~90%. This step is not necessary but is used to conserve the As charge. The specimen is cooled to slightly below room temperature. Such a temperature is necessary to condense a sufficiently thick As overlayer.

A typical sample structure which has been transferred between MBE and XPS systems is shown in Fig. 1. These samples were used for studies of the valence band of AlAs[5] and GaAs–AlAs heterojunction band discontinuities.[6] Figure 2 shows XPS core-level spectra in the region of Al 2*p* and As 3*d* lines. This sample had been stored in air for 5 days before insertion into the XPS system. The upper spectrum in the figure is from the As overlayer. We observe elemental As and a trace amount of As_2O_3. After heating the sample to ~300°–350°C, the spectrum of clean AlAs is obtained (lower portion of Fig. 2). No O, C, or other contaminant could be detected, and good LEED patterns were obtained from the samples prepared by this technique.

In summary, we have developed and demonstrated a simple method for the protection of reactive $Al_xGa_{1-x}As$ surfaces. With this technique a surface prepared by MBE can be transferred in air to another vacuum system for either experimental studies, characterization, or further processing. While this method has been demonstrated for GaAs, AlAs, and AlAs–GaAs heterojunctions, it should be applicable to other III–V or II–VI binary (and ternary or quaternary) systems as well. The method consists of the deposition at or slightly below room temperature, of a protective elemental overlayer (~100–1000 Å) of the higher vapor-pressure phase, nonmetallic component of the semiconductor. Thus As was used for GaAs and AlAs and could presumably be used for other arsenides. It seems likely that Sb, S, Se, and Te can be used for some antimonides, sulfides, selenides, and tellurides, respectively. The condensed overlayer protects the surface from contamination and oxidation during transfer between UHV systems. After transfer, the protective layer is easily removed by low temperature annealing to yield clean and oriented surfaces. This technique may also be applicable for other growth techniques such as metal-organic chemical vapor deposition.

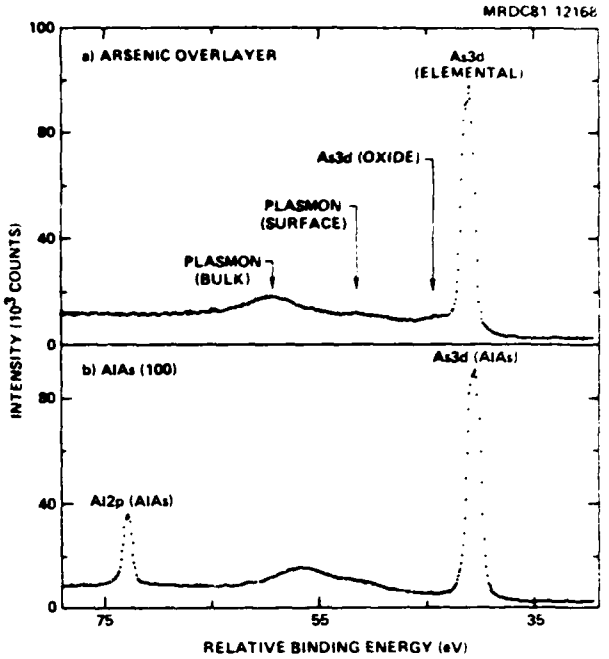

FIG. 2 (a) XPS spectrum of As 3*d* core level from the protective elemental As overlayer for an AlAs sample that had been stored in air for 5 days. (b) XPS spectrum of Al 2*p* and As 3*d* core levels from the underlying AlAs epilayer after the protective As overlayer has been desorbed. The binding-energy scale is relative to the AlAs valence-band maximum.

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Reactivity and interface chemistry during Schottky-barrier formation: Metals on thin native oxides of GaAs investigated by x-ray photoelectron spectroscopy

Steven P. Kowalczyk, J. R. Waldrop, and R. W. Grant
Rockwell International Electronics Research Center, Thousand Oaks, California 91360

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The room-temperature interfacial chemical reactions of overlayers of several diverse metals (Au, Cu, Al, Mg, Cr, and Ti) with thin native oxide films (~ 10 Å) on GaAs (100) surfaces were investigated with x-ray photoelectron spectroscopy (XPS). The reactivity of these metals with the native oxides of GaAs ranged from inert to complete reduction for the oxides and is well predicted by bulk thermodynamic free energies of formation. Variations in band bending during Schottky-barrier formation were monitored by XPS. The implication of the observed interface chemistry for Schottky-barrier modeling is discussed.

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Schottky-barrier junctions are the basis of a large number of compound semiconductor electronic devices, including microwave diodes, field-effect transistors, solar cells, photodetectors, and CCD's; thus knowledge of interfacial phenomena occurring during formation of Schottky-barrier contacts is of significant importance. A fundamental understanding of these phenomena is especially crucial as the prospect of very large scale integrated circuit technology becomes imminent. The primary experimental thrust of surface science experiments has been limited to ideal (abrupt) contacts, that is, metals deposited under ultrahigh vacuum (UHV) conditions on atomically clean and crystallographically ordered semiconductor surfaces.[1-5] However, typical fabrication procedures for a Schottky-barrier device generally are such that a native oxide film is present on the semiconductor surface prior to metal deposition. For this reason modeling of practical Schottky-barrier devices generally assumes the presence of a thin (10–100 Å) interfacial insulator film between the metal and semiconductor.[6]

This letter reports x-ray photoelectron spectroscopy (XPS) investigations of Schottky-barrier formation at GaAs (100) interfaces in the presence of a thin native oxide surface layer. GaAs surfaces that had two different initial oxides were studied. The room-temperature chemistry was investigated for the metals Au, Cu, Al, Mg, Cr, and Ti with an interfacial oxide layer during sequential stages of contact formation. A range of reactivity was found, from chemically inert (Cu and Au) to complete consumption of the native oxide layer (Al, Mg, Cr, and Ti). We have also used XPS to monitor the GaAs interface band bending during Schottky-barrier formation and find that the Schottky-barrier height is relatively independent of the composition of the initial thin native oxide layer.

The ability of XPS to detect the chemical state of the

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component atomic species in a molecule or solid is well known,[7] including numerous applications to surface chemistry.[8,9] The surface sensitivity of XPS is due to its ~25-Å sampling depth. The capability of XPS to monitor surface- or interface-potentials to high accuracy is less well known.[10,11] Chemical information is obtained from *chemical shifts* of core-level binding energies. These shifts are the result of changes to valence-electron distribution. For example, the binding energy of the As 3*d* level in As_2O_3 is ~3.4-eV higher than in GaAs. For a semiconductor, band bending rigidly shifts all core-level binding energies with respect to the Fermi level, thus one can monitor the *potential shift* of a particular valence state to measure interface potentials. Details of potential-shift measurement and its application to interface potentials can be found in Ref. 11. The present work utilizes both capabilities.

The XPS instrumentation used for these measurements is a HP 5950A electron spectrometer with monochromatized AlK_α ($h\nu = 1486.6$ eV) x-ray source and UHV modifications ($< 9 \times 10^{-11}$ Torr). The sample treatment chamber included an evaporator and a quartz crystal thickness monitor for controlled metal depositions. The sample holder incorporates a resistive heater capable of producing sample temperatures up to 1000 °C.

The samples were all bulk grown *n*-type ($\sim 5 \times 10^{16}$ cm^{-3}) GaAs,[12] which had been wafered and polished to give a (100) surface. Two types of GaAs (100) surfaces were prepared. Each surface was first treated with a standard sulfuric acid 4:1:1 (H_2SO_4, H_2O_2, H_2O) etch for approximately 1 min, quenched in H_2O, then inserted into the introduction chamber of the XPS spectrometer system within a few minutes. XPS analysis of relative peak heights shows that this procedure results in a ~10-Å-thick mixed oxide consisting of both As_2O_3 and Ga_2O_3 (see Fig. 1) and an associated large surface band bending (~ 0.7 eV).[11] A second set of samples with a different type of oxide was prepared by heating the above mixed oxide to ~450 °C in a vacuum of 10^{-9} Torr for ~5 min. Such sample heating could occur during a device processing step. This heat treatment results in a surface oxide layer with about the same thickness but solely with the composition Ga_2O_3 from the reaction

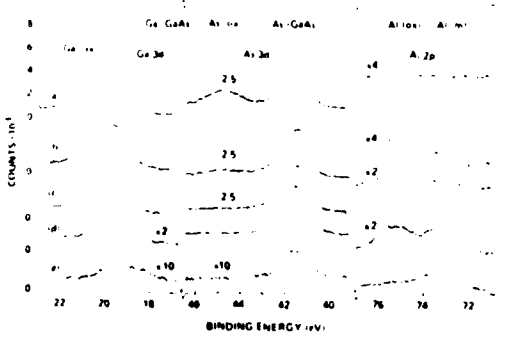

FIG. 1. The Ga 3*d*, As 3*d*, and Al 2*p* core-level spectra from *n*-GaAs (100) with the sequential treatment of (a) etch, (b) submonolayer deposit of Al, and (c–e) increasing thickness of Al deposit.

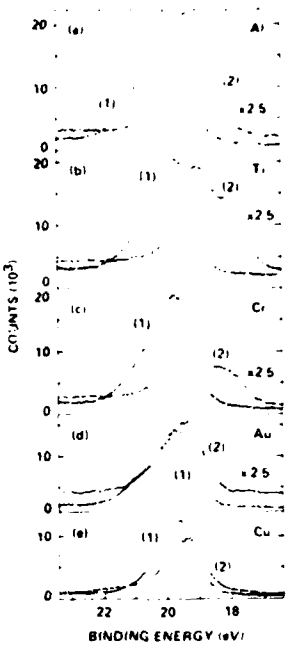

FIG. 2. The Ga 3*d* spectra of heat treated *n*-GaAs (100) with Ga_2O_3 surface layer. 1: Before metal deposition and 2: after metal deposition. Metals: (a) Al, (b) Ti, (c) Cr, (d) Au, and (e) Cu.

$$As_2O_3 + 2\,GaAs \rightarrow Ga_2O_3 + 2\,As_2\uparrow \quad (1)$$

in which additional GaAs substrate is consumed.[11] The Ga_2O_3 covered surface is associated with a low band bending (~ 0.3 eV).[11,13] The difference in surface potential is ~0.4 eV between these two surfaces. A sample with each of the oxides was prepared for deposition of the metals Au, Cu, Al, Mg, Ti, and Cr. Three regimes of deposited metal thickness were studied: (i) submonolayer, (ii) ~1–3 monolayer, and (iii) thick, >50 Å.

In Fig. 1 the XPS Ga 3*d*, As 3*d*, and Al 2*p* core-level peaks are shown for the initial mixed oxide surface, (a), and for four successive Al metal depositions, (b)–(e), which were made onto a mixed-oxide-covered GaAs substrate. The peaks arising from the Ga and As in the GaAs substrate [labeled Ga (GaAs) and As (GaAs)] are clearly distinguishable from the chemically shifted Ga and As contributions arising form the thin oxide film [labeled Ga(ox) and As(ox)]. With the first two depositions of Al, ~5 Å, (b)–(c), the Al consumes As_2O_3 and becomes Al_2O_3 via the room-temperature solid-state reaction

$$2\,Al + As_2O_3 \rightarrow Al_2O_3 + As_2\uparrow, \quad (2)$$

the Ga_2O_3 is unaffected. The elemental As produced is apparently desorbed from the surface. Once the As_2O_3 is entirely consumed, additional Al, deposited in (d)–(e), reacts with the Ga_2O_3 via the reaction

$$2\,Al + Ga_2O_3 \rightarrow Al_2O_3 + 2\,Ga. \quad (3)$$

In spectrum (e) the elemental Ga produced by this reaction is apparent as a low binding-energy peak at ~18.3 eV; also, only when both oxides are completely reduced is metallic Al observed, as in (d) and (e). The total amount of Al deposited was ~40 Å. A similar sequence of depositions were made for

Ti, Cr, Au, and Cu metal overlayers. Ti and Cr were more reactive than Al in that both oxides were reduced *simultaneously* rather than *sequentially*, the chemical behavior was otherwise similar. For Au and Cu deposition, on the other hand, neither oxide was chemically affected and no reduction of oxide was observed. All surfaces which had the mixed As_2O_3 and Ga_2O_3 oxides exhibited little change of surface band bending upon deposition of metal overlayers.

In Fig. 2 a series of Ga 3*d* peaks, (a)–(e), from GaAs substrates that had the Ga_2O_3 surface are shown for a ~15-Å deposition, labeled (2), of Al, Ti, Cr, Au, and Cu, respectively. In all the initial spectra, labeled (1), the pronounced shoulder on the high binding-energy side of the Ga (GaAs) main peaks is due to the Ga_2O_3 oxide film. In this series of spectra both chemical effects and a GaAs band-bending change are evident as a result of metal deposition. For example, in cases (a)–(d) a binding-energy shift of the main Ga (GaAs) peaks to ~0.4-eV lower binding energy is readily discernible. As discussed earlier, this type of shift corresponds to a change in band-bending potential in the GaAs. In this case, we are observing a change in interface band bending in the GaAs as a Schottky-barrier contact is being formed by the presence of a metal. For Al, Ti, and Cr, (a)–(c), this band-bending change is accompanied by Ga_2O_3 reduction and the formation of Ga alloys or compounds with the deposited metal, as evidenced by disappearance of the Ga(ox) shoulder and the appearance of the low binding-energy structure. Although not shown, Mg metal overlayers had identical behavior. Once again, Au and Cu produced no chemical reaction with the Ga_2O_3 layer, although a significant increase in GaAs band bending still occurs.

The driving force for these chemical reactions is the change in free energy of formation ΔG. The use of bulk ΔG values provides a useful rule of thumb[9] for predicting all of the interfacial reactions observed in this work. However, because this predictive guide is based on bulk thermodynamic properties and does not consider interfacial contributions, it should be employed with caution.

Our results have several implications for understanding the formation of Schottky-barrier contacts. Two of the important aspects of this work are that, (i) the chemical reactivity and (ii) the pinning position of the surface Fermi level can both be contactlessly monitored in the same XPS measurement during contact formation. Figure 1 shows that an initial layer of native oxide is completely consumed by reaction with certain deposited metals *at room temperature* to thus produce a new and different oxide (such as Al_2O_3 in Fig. 1). Figure 2 demonstrates another important concept, namely that a band-bending variation can occur during Schottky-barrier contact formation in the presence of a surface oxide. If a surface is prepared with a low surface band bending (such as the Ga_2O_3 surface of Fig. 2), the deposition of metal on the *thin* native oxide layer acts to shift the surface Fermi level to result in a higher band bending and thus a higher Schottky-barrier height. This new pinning position is approximately the same whether there is a chemical reaction (Ti, Cr, Al, Mg) or not (Au and Cu). Thus the distinct interfacial native oxide, which is conventionally assumed in present Schottky-models, either does not exist or does not insulate the semiconductor from the effects of a metal overlayer. Therefore the interfacial oxide layer as is presently used in modeling Schottky-barrier heights is not appropriate for GaAs.

Since GaAs is a prototypical covalent compound semiconductor, we expect that the observed interface effects are general phenomena on compound semiconductor surfaces. We note that the metals which react with native oxides may be preferred in actual devices because they would presumably have better contact-adhesive properties.

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[12] From Crystal Specialities, Inc.
[13] A Ga_2O_3 surface layer can alternatively be prepared by heating the initial oxide to ~570 °C in UHV for several minutes to produce a clean surface (which gives a characteristic LEED pattern) and subsequent oxidation by exposure to ~10^4 LO_2 at ~480 °C.

Interfacial chemical reactivity of metal contacts with thin native oxides of GaAs

Steven P. Kowalczyk, J. R. Waldrop, and R. W. Grant

Rockwell International, Microelectronics Research and Development Center, Thousand Oaks, CA 91360

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X-ray photoemission spectroscopy (XPS) was used to investigate the chemical reactivity and band-bending variation of native oxide covered surfaces of GaAs (100) during Schottky-barrier formation. The GaAs surfaces prior to metal deposition had thin ~10 Å overlayers of either As_2O_3 and Ga_2O_3 or only Ga_2O_3. A variety of metals, some chemically inert (Au, Cu, and Ag) and some chemically reactive (Al, Mg, Cr, and Ti), were studied on both types of oxide surfaces. The chemical reactions occurred at room temperature and were well predicted by bulk thermodynamic free energies of formation.

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I. INTRODUCTION

Metal–semiconductor contacts are ubiquitous in semiconductor electronics, with Schottky-barrier contacts being of particular fundamental and practical importance. To date the primary emphasis in surface science experiments applied to contacts has been to study the phenomena associated with ideal Schottky-barrier contacts, that is, metals deposited onto clean and ordered seminconductor surfaces under ultrahigh vacuum conditions (see e.g. Refs. 1–4). When Schottky-barrier contacts are formed during the fabrication of a typical device, however, there is generally a thin native oxide film present on the surface of the semiconductor. Consequently, the modeling of Schottky-barrier contacts in devices usually assumes the existence of a 10–100 Å thick insulating native-oxide film between the metal and the semiconductor.[5] The question naturally arises as to the interface chemistry during Schottky-barrier contact formation in the presence of a native oxide layer on a semiconductor. Furthermore, a current trend in the development of fast electronic circuits is to utilize very small devices, with active regions being envisioned as small as 50 to 200 Å. The constraints imposed by small dimensions on reliably fabricating such devices make it incumbent to develop an understanding of the microchemical processes at various semiconductor interfaces. Presently, GaAs has received the most attention as the prototypical compound semiconductor for advanced high-performance electronic devices.

This paper reports the investigation, by x-ray photoemission spectroscopy (XPS), of the room temperature chemical reactions of the metals Au, Ag, Cu, Al, Mg, Ti, and Cr with thin native oxides on GaAs (100) surfaces. The reactions were followed as a function of increasing metal thickness from submonolayer amounts to ≥25 Å. The metals were either inert (Au, Ag, and Cu) or reactive (Al, Mg, Ti and Cr), with the former leaving the native oxide layer intact and the latter causing removal of the native oxide by a chemical displacement reaction. In addition to chemical analysis, XPS was also used to observe changes in interface Fermi-level $\Delta E_F'$ position (band-bending) during the early stages of Schottky-barrier formation.

II. EXPERIMENTAL DETAILS

A HP5950 electron spectrometer was used for the XPS measurements. This system possesses a monochromatized Al K α ($h\upsilon$ = 1486.6 eV) x-ray source; the electrons from most of the core levels measured in these studies had escape depths of ~25 Å. The features of this system include a custom ultrahigh vacuum preparation chamber ($P \sim 1 \times 10^{-10}$ Torr), resistively heated metal evaporators, quartz crystal thickness monitor, sample heater, and LEED instrumentation

The application of XPS for the detection of the chemical state of the component atomic species in solids is well established. The chemical-state information is easily obtained via the chemical shifts of core-level binding energies which are sensitive to the valence-electron distributions (e.g., the As 3*d* core-level binding energy in As_2O_3 is ~3.4 eV higher than it is in GaAs). Concurrently with monitoring the chemical state, XPS can be employed to monitor changes in E_F' during interface formation. The $\Delta E_F'$ can be measured because, for a semiconductor, changes in band bending rigidly shifts all core-level binding energies of a particular valence state with respect to the Fermi level ($\Delta E_F'$ = final binding energy − initial binding energy). This aspect of XPS is more fully discussed by Grant *et al.*[6]

The samples were all bulk grown *n*-type (~5×10^{16} cm^{-3}) GaAs, which had been wafered and polished to give a (100) surface and 20 mil thickness.[7] All surfaces were given a sulfuric acid etch (4:1:1–H_2SO_4, H_2O_2, H_2O) for approximately 1 min, quenched and rinsed in H_2O, blown dry with N_2, mounted on molybdenum plates with indium, and inserted into the introduction chamber of the XPS system within several minutes. The XPS analysis of the relative peak intensities shows that this procedure yields an oxide surface of ~10 Å thickness with a mixed composition of As_2O_3 and Ga_2O_3 and an associated large surface band bending of ~0.7 eV.[6,8,9] A second type of surface was prepared by heating the etched surface in a vacuum of ~5×10^{-9} Torr for 5 min at ~450°C. This treatment results in the loss of As_2O_3 via the reaction

$$As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + \frac{4}{x} As_x \uparrow. \quad (1)$$

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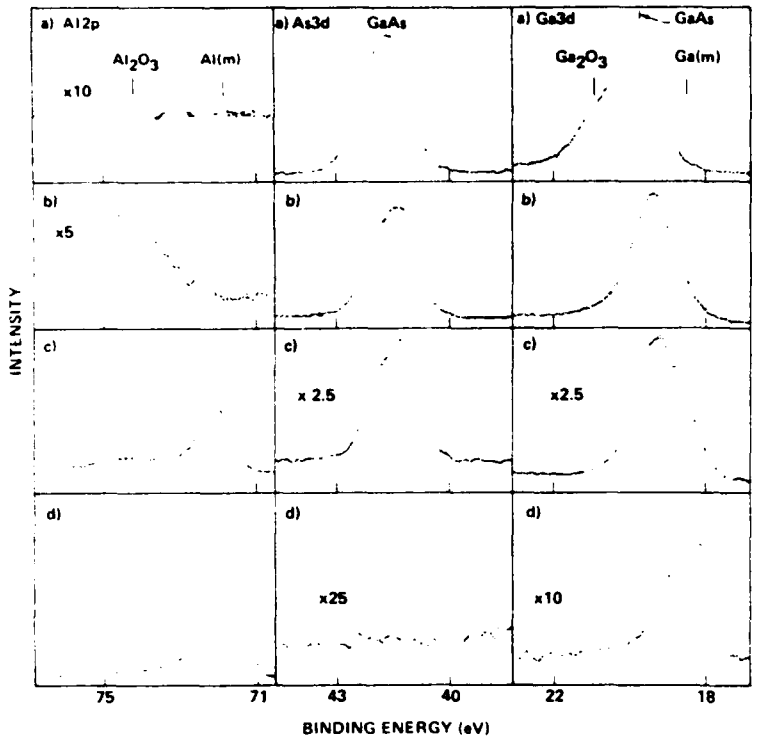

FIG. 1. XPS spectra of the Al 2*p* (left), As 3*d* (center), and Ga 3*d* (right) core levels for an increasing amount of an Al deposit, (a)–(d) on a Ga_2O_3 covered GaAs surface. Al film thicknesses determined by assuming uniform coverages are 0, ~3, ~16, and >100 Å for (a)–(d), respectively.

The surface is now covered with Ga_2O_3 and is associated with a low band bending; the difference in surface potential between these two types of surfaces can be as much as ~0.4 eV.[6,8-10]

III. RESULTS AND DISCUSSION

Characteristic spectra from our study of the interaction of metals with the native oxides of GaAs are given in Figs. 1–6. Fig. 1 illustrates several of the topics we wish to cover in this paper. This figure shows the various interfacial phenomenon which occur with increasing Al deposit on the Ga_2O_3 (low band-bending) surface of GaAs (100). We see from the Al 2*p* spectrum [Fig. 1(b)] that the initial Al reacts with the Ga_2O_3 via

$$2Al + Ga_2O_3 \rightarrow Al_2O_3 + 2Ga. \quad (2)$$

After all the Ga_2O_3 is reacted, a metallic layer is formed [Figs. 1(c) and (d)]. Figures 1(c) and (d) also show a shift of the metallic Al 2*p* core level to lower binding energy with increasing Al thickness. The As 3*d* core level exhibits no evidence of chemical change [Fig. 1(a)–(d)]; however, between Figs. 1(a) and (b) there is evidence of $\Delta E_F'$ of several tenths of an eV, which indicates an increase of band bending with the first submonolayer deposit of metal. The Ga 3*d* spectrum of Fig. 1(a) shows the presence of two chemical forms of Ga, Ga_2O_3 (high binding-energy component) and GaAs (the more intense component). With the initial Al deposit, three observations can be made: (1) a gradual decrease of Ga_2O_3 with increasing Al [via Eq. (2)], (2) a potential shift [between 1(a) and (b), which is the same as that seen with the As 3*d* core level, and (3) a new component to lower binding energy which is characteristic of Ga metal liberated by Eq. (2). Finally, for the thickest coverages such that the GaAs interface cannot be sampled by XPS [see As 3*d* spectrum in Fig. 1(d)], we observed out-diffused metallic Ga "floating" on the surface [see the Ga 3*d* spectrum in Fig. 1(d)]. Figures 2–6 illustrate these points in more detail for other metals.

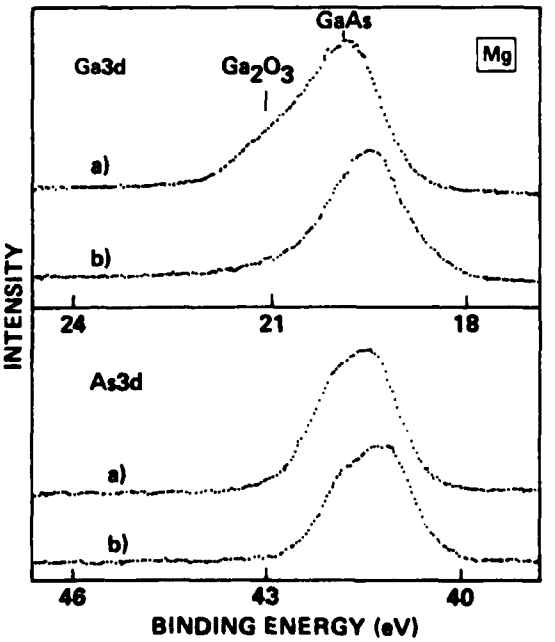

FIG. 2. XPS spectra from a Ga_2O_3 covered GaAs surface of Ga 3*d* (upper panel) and As 3*d* (lower panel) core levels; (a) before a submonolayer deposit of Mg, (b) after a submonolayer deposit of Mg.

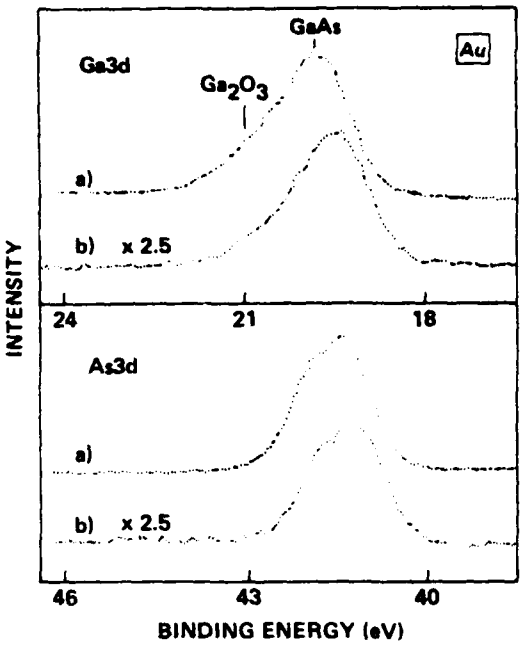

FIG. 3. XPS spectra from a Ga_2O_3 covered GaAs surface of Ga 3*d* (upper panel) and As 3*d* (lower panel) core levels, (a) before a Au deposit, (b) after a Au deposit.

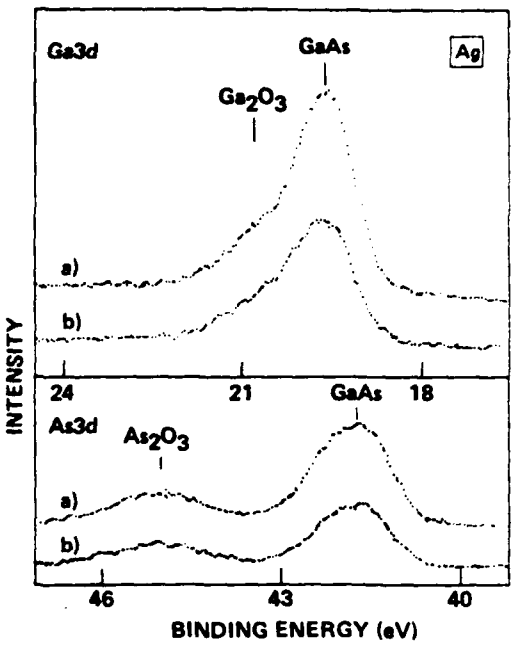

FIG. 5. XPS spectra from a As_2O_3–Ga_2O_3 covered GaAs surface of Ga 3*d* (upper panel) and As 3*d* (lower panel) core levels; (a) before initial Ag deposit, (b) after initial Ag deposit.

Figures 2 and 3 show spectra which illustrate the behavior of a reactive metal (Mg) compared to a non-reactive metal (Au) deposited on the Ga_2O_3 surface. In Fig. 2 the reduction of the Ga_2O_3 by Mg and the liberation of free Ga via the reaction

$$3Mg + Ga_2O_3 \rightarrow 3MgO + 2Ga \qquad (3)$$

can easily be seen by comparison of the two Ga 3*d* spectra of the upper panel. The initial small deposit of Mg has slightly reduced the high binding-energy shoulder due to Ga_2O_3 of Fig. 2(a) and a small low binding-energy shoulder indicative of free Ga is detectable. Further Mg deposit causes complete reduction of Ga_2O_3 and increased Ga. A concomitant potential shift of E_F which corresponds to higher band bending can be observed in both the As 3*d* and Ga 3*d* lines from GaAs in Fig. 2 (Ti and Cr depositions behave similarly to Mg). The potential shift is *not* due to chemical reactions with the native oxide as the potential shift is also present when there is no such chemical reaction, as for example in the case of Au (Fig. 3) or Cu. On the Ga_2O_3 surface we have observed a significant increase of band bending even for the smallest submonolayer depositions of metals that we have studied, regardless of chemical reaction.

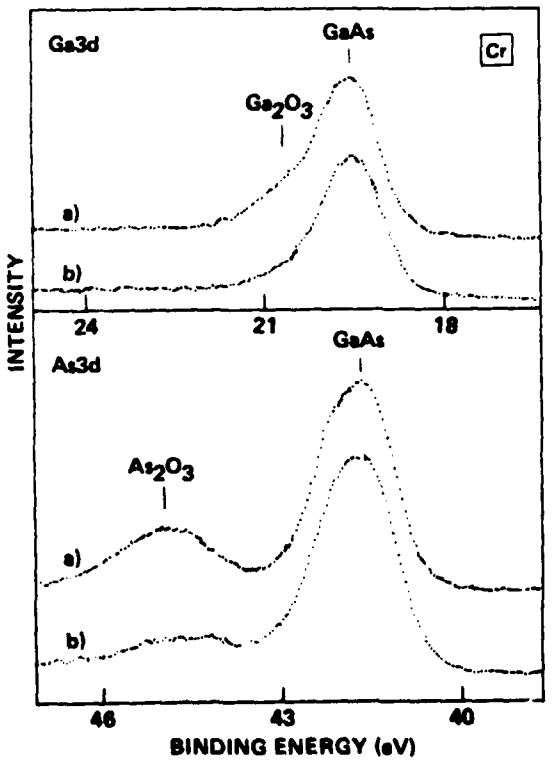

FIG. 4. XPS spectra from a As_2O_3–Ga_2O_3 covered GaAs surface of Ga 3*d* (upper panel) and As 3*d* (lower panel) core levels; (a) before a submonolayer Cr deposit, (b) after a submonolayer Cr deposit.

Figures 4 and 5 (Cr and Ag deposition, respectively) show Ga 3*d* and As 3*d* spectra on the mixed As_2O_3–Ga_2O_3 surface where Cr is an example of a reactive metal and Ag of a non-reactive metal. Figure 4 shows the decrease in both Ga_2O_3 and As_2O_3 with an initial deposit of Cr. Further deposit leads to complete reduction of the mixed native oxide and formation of a Cr oxide via

$$2M + N_2O_3 \rightarrow M_2O_3 + 2N \qquad (4)$$

where M = Cr and N is either Ga or As (Ti deposition acts similarly to Cr). In contrast, Al reacted sequentially, first with the As_2O_3, after the As_2O_3 was *totally* reduced, then it reacted to reduce the Ga_2O_3. Figure 5 shows the result of the initial

TABLE I. Summary of interfacial chemistry and $\Delta E_F'$ for several metals deposited on native oxide surfaces of GaAs.

Metal	$As_2O_3 + Ga_2O_3$ surface Reacted	$\Delta E_F'$ [7]	Ga_2O_3 surface Reacted	$\Delta E_F'$ [7]	Oxide product	ΔG (kcal)[4-6] Ga_2O_3 reaction	ΔG (kcal)[4-6] As_2O_3 reaction
Au	no	0.0	No	−0.2	Au_2O_3	+278	+177
Ag	no	0.0	—[1]	—[1]	AgO	+249	+148
Cu	no	0.0	no	−0.2	CuO	+149	+ 48
Al	yes[2]	0.0	yes	−0.2	Al_2O_3	−138	−239
Mg	—[1]	—[1]	yes	−0.2	MgO	−169	−270
Ti	yes[3]	0.0	yes	−0.2	Ti_2O_3	−107	−208
Cr	yes[3]	0.0	yes	−0.2	Cr_2O_3	− 11	−112

[1] This surface was not studied.
[2] The metal-oxide reactions occurred sequentially, with As_2O_3 reacting first.
[3] Both oxides, Ga_2O_3 and As_2O_3, reacted simultaneously with the deposited metal.
[4] ΔG for the reaction $2M + 2N_2O_3 \rightarrow M_2O_3 + 2N$ (M = Au, Al, Ti, or Cr; N = Ga or As) or $3M + N_2O_3 \rightarrow 3MO + 2N$ (M = Ag, Cu, or Mg; N = Ga or As). It can be seen that the difference in ΔG for the As_2O_3 and Ga_2O_3 reactions is the difference in G for Ga_2O_3 and As_2O_3 (−101 kcal/mole).
[5] The free energies used to calculate the ΔG's were obtained from *Handbook of Chemistry and Physics*, 58th ed., edited by R. C. Weast (CRC Press, Cleveland, 1977) and *Lange's Handbook of Chemistry*, edited by J. A. Dean, (McGraw-Hill, New York, 1979).
[6] Other possible oxide products were also considered (namely Ag_2O, Ag_2O_3, Cu_2O, TiO_2, TiO, Ti_3O_5, and Ti_4O_7). For a particular metal the sign of ΔG did not change for these alternative oxide products.
[7] $\Delta E_F'$ was measured by the change of the As 3*d* binding energy upon the addition of ~1 monolayer metal. In the case of Cr, the Ga 3*d* level was used because of overlap between Cr 3*p* and As 3*d* levels.

Ag deposit; there is no reduction of either oxide, only an attenuation of substrate signal with increasing Ag (Au and Cu behaved similarly to Ag on this surface). On the mixed oxide surface, no change of E_F' independent of reactivity of deposited metal was observed.

The chemical reactivity results for both types of native oxide surface are summarized in Table I along with the effect of the deposited metal on the surface Fermi-level position. We note that the chemical reactivity of the metals for reducing the native oxide and producing a metal oxide can be simply and, in all the cases we have studied, reliably predicted by the change of free energy of formation ΔG.[11] We emphasize that these reactions occurred at *room temperature*.

Table II indicates our observations regarding outdiffusion of Ga or As from the native oxide covered samples; these observations are compared with results on atomically clean GaAs (100) surfaces.[2] This outdiffusion may be an indication of

TABLE II. Summary of outdiffusion characteristics from GaAs (100) interfaces.[1]

Metal	$As_2O_3 + Ga_2O_3$ surface	Ga_2O_3 surface	Clean surface (Ref. 2)
Au	As	As	Ga,[3] As [3]
Ag	As	—[2]	none
Cu	none	As[3]	—[2]
Al	Ga	Ga	Ga
Ti	none	none	none
Cr	no Ga[4]	no Ga[4]	no Ga[4]

[1] These results are for coverages of ~50 Å of metal.
[2] This surface was not studied.
[3] Thicker metal deposits (>100 Å) showed no surface concentration of this element.
[4] As outdiffusion was not investigated as the Cr 3*p* core level overlapped the As 3*d* core level.

important processes occurring at interfaces, such as nonabruptness and the formation of defects.

An additional observation concerns a size effect on the metal core-level binding energies. As already seen in Fig. 1(b) for Al, after the reaction to form Al_2O_3 was complete the binding energy of the metallic Al 2*p* core level shifted to lower binding energy with deposition thickness [1(c) and (d)]. This effect is more easily observed for the metals which do not react and thus have no complications due to chemically shifted oxide components. Figure 6 shows the evolution in shape and binding energy of the Cu $2p_{3/2}$, Ag $3d_{3/2,5/2}$, and Au $4f_{5/2,7/2}$ core levels with increasing metal coverages. We see dramatic shifts in core-level binding energies of the metals (Cu, Ag, Au, Al, Ti, Cr) to lower binding energy with increasing coverage until the bulk binding energy is attained.[12] The smallest deposits also show broadened linewidths (by almost 50% in some cases) in comparison to those of the thickest bulk-like films. We also have observed similar effects for Au and Pd deposited on clean *n*-type GaAs (100) surfaces.[13] For example, the Au $4f_{7/2}$ core level shifted from 85.02 eV for initial small submonolayer coverages to the bulk value of 84.00 eV[14] for thick bulk-like films. In the case of the Pd $3d_{5/2}$ level, a shift of ~1.45 eV has been observed.[12] S. T. Lee and co-workers have recently systematically studied the binding energy for vacuum deposited Au clusters on amorphous carbon, SiO_2, and Al_2O_3; they find a range of binding energies for the Au $4f_{7/2}$ from 85.0 eV for coverages of $\sim 10^{13}$ atoms/cm^2 to 84.0 eV for $\sim 10^{16}$ atom/cm^2 coverages.[15] Similar shifts have been observed for Ni, Cu, Ag, and Au ions implanted into inert matrices.[16] Size-effect shifts are due to a combination of electronic-structure changes[17] and extra-atomic relaxation[18] and are largely independent of substrate. The broadening at low coverages may be due to reduced electronic screening in the final state as proposed by Ascarelli *et al.*[19] or a large range of characteristic sizes.

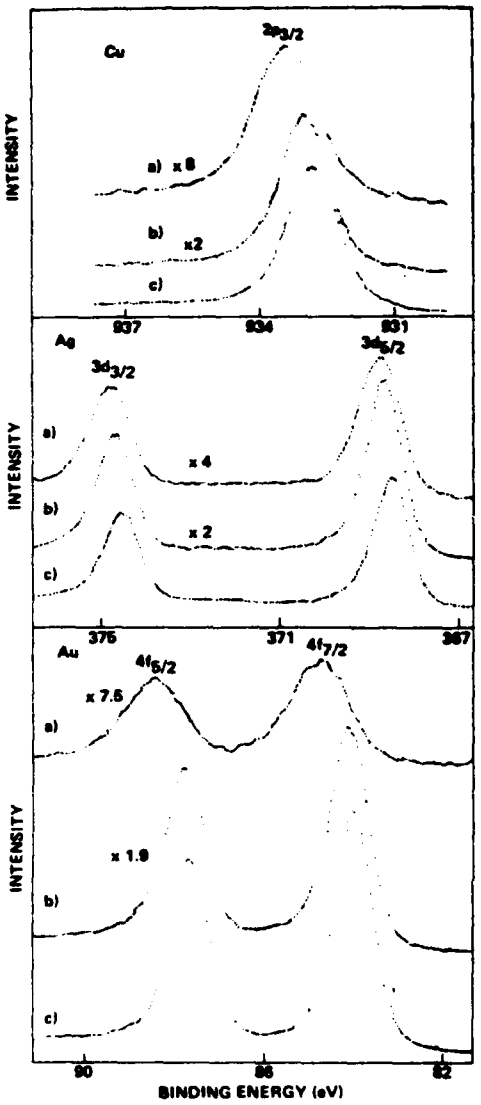

FIG. 6. XPS spectra of the Cu $2p_{3/2}$ (upper panel), Ag $3d_{3/2}$, $3d_{5/2}$ (middle panel), and Au $4f_{5/2}$, $4f_{7/2}$ (lower panel) core levels for increasing metal thickness, (a)–(c). The film thickness determined by assuming uniform coverages for Cu are ~2, ~16, and >100 Å; for Ag, ~7, ~19, and >100 Å; and for Au, ~2, ~12, and >100 Å.

IV. SUMMARY AND CONCLUSIONS

We have used XPS to study metal-contact interfacial chemical reactivity on two types of thin native oxide covered GaAs (100) surfaces. The contact metals examined were Al, Ti, Cr, Mg, Cu, Ag, and Au. Both the interfacial chemistry and Fermi-level position were monitored during the contact formation and a number of observations were made:

(1) For the metals Cu, Ag, and Au, $\Delta G > 0$ for the reduction of As_2O_3 and Ga_2O_3. These metals did not exhibit reduction of the native oxides.

(2) For the metals Mg, Al, Ti, and Cr, $\Delta G < 0$ for the reduction of As_2O_3 and Ga_2O_3. Sufficient deposit of these metals at room temperature led to complete reduction of the native oxides and formation of a new metal oxide at the interface.

(3) For the $Ga_2O_3 + As_2O_3$ (high band bending) surface, deposition of either reactive or non-reactive metal did not change E_F^i.

(4) For the Ga_2O_3 (low band bending) surface, deposition of the smallest amounts of metal, either reactive or non-reactive, shifted E_F^i by several tenths of an eV which caused E_F^i for both types of native oxide surfaces to have the same Fermi-level position.

(5) Outdiffusion of Ga and As from the native oxide covered surfaces was similar to that from atomically clean surfaces.

(6) Metal core-level binding energies and the corresponding linewidths decrease with increasing metal coverages.

Our results are relevant to modeling of Schottky-barrier contacts in devices. For device contacts it is common to assume the presence of a distinct thin insulating native oxide film which acts to isolate the semiconductor from the metal at the metal–semiconductor interface.[5] We have shown that many metals chemically react to eliminate the initial native oxide film on GaAs to produce an interface region which consists of a non-insulating mixture of metal and metal oxide. Even when no gross chemical effect is observed, changes in band bending are still observed for the inert metals on Ga_2O_3 surfaces. Thus Schottky-barrier contacts to GaAs should not be modeled by assuming an insulating oxide interfacial layer. These observations support defect models of Fermi-level pinning of Schottky barriers on GaAs.[6,20] Since GaAs is a prototypical compound semiconductor, analogous interface phenomena can be expected for other compound semiconductors.

ACKNOWLEDGMENTS

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APPENDIX II

As mentioned in the Introduction (Section I), this program was divided into two phases. The final report for Phase 1 of the program was published as AFWAL-TR-80-1018. The Summary and Conclusions Section of Phase 1 (Section IV of AFWAL-TR-80-1018) is reproduced here.

ION IMPLANTATION AND ANNEALING

The ion implantation and encapsulation experiments have indicated that silicon dioxide, deposited on a thin native oxide, provides the most effective encapsulant for high-temperature annealing of gallium arsenide surfaces implanted with a high dose of phosphorus ions. Annealing can be performed at temperatures up to 775° using SiO_2 without decomposition of the semiconductor. However, further improvements in film quality are needed to achieve some of the higher annealing temperatures which have been reported in the literature.

The post-implant annealing experiments have demonstrated the ability of the high-dose phosphorus implant to significantly reduce decomposition under the encapsulant during high-temperature processing. This may have implications far beyond the immediate scope of this program.

The electron diffraction patterns indicate that the high-dose phosphorus implants do not result in massive lattice damage, although a more sensitive technique, such as ion backscattering, will be required to detect the defect levels which have been observed in earlier implants into GaAs.

Ion microprobe results indicate that there is no significant diffusion of phosphorus into the substrate during either post-implant annealing or hot substrate implantation. This indicates that the depth of the implanted region can be well controlled so that the advantageous properties of the underlying GaAs substrate can probably be utilized in subsequent MIS devices.

OXIDATION

Oxides grown on the unannealed phosphorus-implanted surfaces have generally shown somewhat less decomposition and damage than those which were annealed with an encapsulant. The implant dose and energy variations which were studied have narrowed the range of parameters for which acceptable oxides result. For unencapsulated surfaces it has been found that ions implanted at doses from 1 to 2 × 10^{16} cm^{-2} and energies from 30 keV to 60 keV result in oxides with the fewest visible defects. Encouragingly, these oxides are visually similar to those grown on $GaAs_{1-x}P_x$, and suggest that further improvements could lead to similar electrical properties.

Oxides grown on both unannealed and annealed aluminum implanted surfaces show significant decomposition and gallium flow for conditions approximating those giving good results with phosphorus.

The C-V characteristics of oxides grown at 600°C in dry O_2 over phosphorus implanted GaAs exhibit hysteresis and deep depletion somewhat similar to oxides grown on single-crystal $GaAs_{1-x}P_x$. D-c conductivity measurements indicate leakage current densities about an order of magnitude higher (for the same field) than those for oxides grown on $GaAs_{1-x}P_x$.

CONCLUSIONS

The work has shown encouraging results relative to modifying the GaAs surface by implantation to permit uniform oxide growth. However, a device quality (electric) dielectric has not been achieved. A number of questions remain concerning the optimum dielectric growth procedure, as well as the impact of the implanted layer upon the insulator-semiconductor interface characteristics. Since many of these questions can only be answered by more in-depth analysis and experiments outside the scope of this program, work on this approach was concluded.