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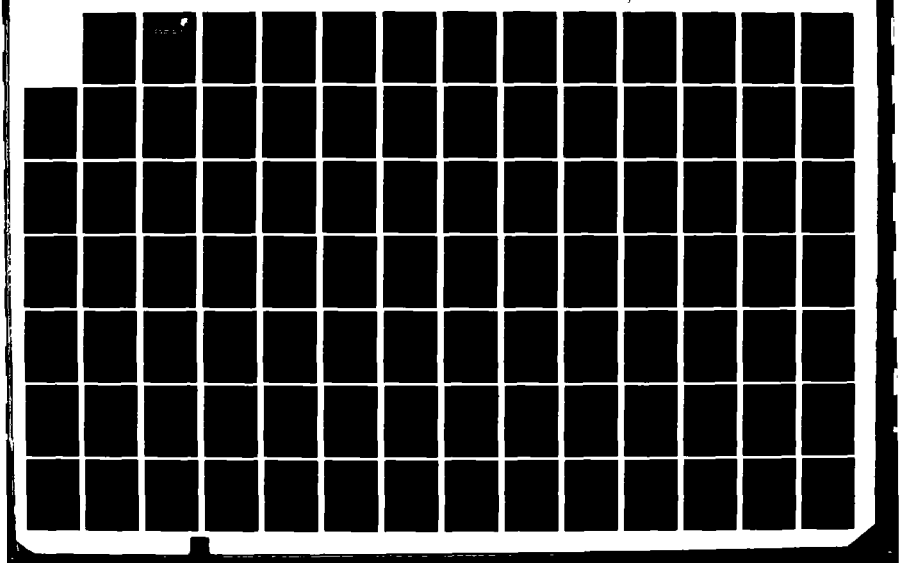

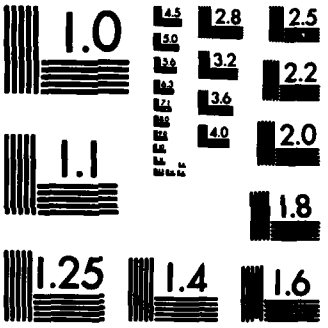

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July 1982

A FOUR-PHASE MODULATION SYSTEM FOR USE WITH AN ADAPTIVE ARRAY

The Ohio State University

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report discusses the use of four-phase modulation in a communication system with an adaptive array. A system is described that provides protection against both conventional (i.e., noise and cw) and smart (in particular, repeat) jamming with rapid acquisition of the signal at the receiver.

This report first discusses four-phase modulation techniques and how they can be used with an adaptive array. Reference signal generation for the

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LMS adaptive array is discussed for these modulation techniques. A communication system is then described that uses one of these modulation techniques. The four-phase signal consists of two orthogonal biphase signals. One signal contains a short code for rapid acquisition. The other contains a long code for protection against smart jammers. A several step signal acquisition technique is also described for the system. The short code timing is first acquired by a sliding correlation method. With the short code used in reference signal generation, the long code timing is rapidly acquired by the Rapid Acquisition by Sequential Estimation method. The long code is then used in reference signal generation.

This report then analyzes the system theoretically. The acquisition procedure is analyzed to show the rapid acquisition of the signal with the system. Acquisition of the short code by a delay lock loop is first analyzed. The code tracking error is then determined. Finally, the long code acquisition method is analyzed with both theoretical and simulation results. Nonlinear and linear codes are also analyzed for use in the system.

An experimental system was implemented to demonstrate the feasibility of the system and to verify analytical results. Optimal parameters for this system were determined using analytical results. The circuitry for the system is described, and experimental results are shown. Analytical and experimental results demonstrate both rapid signal acquisition and protection against conventional and smart jamming with this system.

Block 18 (Cont'd)

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PREFACE

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The material contained in this report is also used as a dissertation submitted to the Department of Electrical Engineering, The Ohio State University as partial fulfillment for the degree Doctor of Philosophy.

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CHAPTER I

INTRODUCTION

An adaptive antenna is an array of antenna elements whose pattern is automatically controlled [1,2]. The signal from each element of the array is multiplied by a controllable weight, which adjusts the amplitude and phase of that signal. The pattern of an adaptive antenna is automatically changed to null interfering signals and optimize desired signal receiption.

Adaptive antennas can be combined with spread spectrum communication techniques [3] to yield even greater interference rejection capabilities. With a system that combines the temporal processing of spread spectrum with the spatial processing of adaptive antennas, protection can be obtained against a wide variety of jamming techniques.

The weights in an adaptive array may be controlled by several techniques. The techniques include those employed in the LMS array [1] and in the Applebaum array [2]. In the LMS array, the weights are adjusted to obtain the least mean-square error between the array output and a so-called reference signal. This reference signal is a locally generated signal that allows the array feedback to differentiate between the desired signal and interference. It must be a signal correlated with the desired signal and uncorrelated with any interference. In the Applebaum array, a steering vector is used instead of a reference signal to maintain a strong response in the direction of the desired signal. The weights are then adjusted to minimize interference from other directions.

The Applebaum array is easier to implement because no reference signal is required. However, if the angle of arrival of the desired signal is not known, then one must use the LMS array with a reference signal.

This report concentrates on the problem of generating a reference signal with a four-phase modulated signal. The most difficult part of the problem is the acquisition of the signal by the receiver. The problem is especially difficult if the timing of the pseudonoise code used in the spread spectrum system must be acquired by the receiver.

A reference signal generation technique has been previously described for spread spectrum signals using biphase modulation [4].

In this technique, the desired signal is modulated with a pseudonoise code combined with data at a lower symbol rate than the code. Thus, the desired signal is a spread spectrum signal. The code timing is acquired at the receiver by a sliding correlation method. To determine the correct code timing, the code generated at the receiver is correlated with the received signal for all possible timing offsets [5]. The biphase reference signal generation technique works well but does have two shortcomings. First, it is vulnerable to repeat jammers with biphase remodulation. Second, short codes must be used for reasonable acquisition times, and short codes may not have adequate security for many applications.

Four-phase modulation is considered in this report as a means to improve upon the biphase system. Previous studies of four-phase modulation [6,7,8] have shown it to have several advantages over biphase. First, four-phase signals transmit twice the information in the same bandwidth as biphase signals [6, p. 305]. Second, the four-phase signal can be structured as two orthogonal biphase signals. Thus, an additional biphase signal is available to increase system capabilities. The GPS system [7] demonstrates an example of the use of this signal structure. Third, the four-phase signal may be affected less than a biphase signal by cw jamming when a hardlimiter is used in the receiver [8]. Biphase modulation may be lost when hardlimited with cw interference. However, some residue modulation remains when a four-phase signal with cw interference is hardlimited.

This report presents a four-phase modulation system that may be used with an LMS adaptive antenna. The modulation system is a spread spectrum communication system and it is assumed that the location of the desired transmitter is not known at the receiver. System code timing must be acquired by the receiver. A four-phase system had been developed that overcomes the shortcomings of the previous biphase system [4], without sacrificing the system's rapid acquisition and conventional (i.e., noise and cw) jamming protection capabilities. This four-phase system is described here.

The four-phase signal consists of two orthogonal biphase signals. One signal contains a short code for rapid acquisition. The other contains a long code to be used for protection against smart jammers (jammers that the biphase system is vulnerable to). A reference signal generation technique and a signal acquisition technique are developed for the four-phase signal. This report analyzes the signal acquisition technique in detail. Analytical and experimental results demonstrate both rapid acquisition and protection against conventional and smart jamming with the four-phase system.

Chapters II through V of this report discuss four-phase modulated signals and their use with an adaptive array. Chapter II discusses several methods for combining two codes to generate a four-phase signal and discusses the problem of generating reference

signals for this four-phase signal. Chapter III describes several methods for combining data with the codes and discusses the problem of generating reference signals for the data modulated signal. As will become clear, the reference signals discussed in Chapters II and III may be only partially correlated with the desired signal. Chapter IV discusses the performance of the adaptive array with a partially correlated reference signal. A particular type of four-phase modulated signal is chosen in Chapter V, and a communication system is developed for this signal.

Chapters VI through X analyze this four-phase system theoretically. Chapter VI studies the acquisition of the short code timing by the receiver. Chapter VII studies the short code tracking error after acquisition. The next step in the signal acquisition process, the long code acquisition, is studied in Chapter VIII. Chapter IX discusses the communication security of various types of long codes. Chapter X discusses the communication security of the system when conventional (e.g., noise and cw) and/or smart jamming (e.g., repeat jammers) are present at the receiver.

Finally, Chapter XI describes an experimental four-phase system based on the analysis in Chapters VI through X, and discusses the experimental results obtained with this system. Experimental results are compared with the analytical results of these chapters. The summary and conclusions are given in Chapter XII.

CHAPTER II

FOUR-PHASE MODULATION TECHNIQUES WITH TWO CODES

A. Introduction

This chapter describes a previous biphase system [4] used for interference rejection and examines the four-phase modulation techniques that can be used to improve the system. Section B describes the previous biphase system. The shortcomings of this system are then discussed. Four-phase modulation is shown to overcome these shortcomings. Section C describes the various four-phase modulation techniques. One problem to be solved with four-phase modulation is the generation of a reference signal for the adaptive array in the system. Section D discusses reference signal generation with the four-phase signal. Results are summarized in Table 1.

B. The Biphase System

This section discusses a biphase spread spectrum communication system [4] developed for use with an LMS adaptive array. The section first describes the LMS array and then the biphase modulation technique.

A block diagram of an N element LMS adaptive array [1] is shown in Figure 1. The signal received by the i-th element, $y_i(t)$, is split with a quadrature hybrid into an inphase signal, $X_{I_i}(t)$, and a quadrature signal, $X_{Q_i}(t)$. These signals are then multiplied by a controllable weight, W_{I_i} or W_{Q_i}. The weighted signals are summed to form the array output, $s_0(t)$. The array output is subtracted from a reference signal (described below), $r(t)$, to form the error signal, $e(t)$. The element weights are generated from the error signal and the $X_{I_i}(t)$ and $X_{Q_i}(t)$ signals by using correlation feedback loops as shown in Figure 2.

The purpose of the reference signal is to make the array track the desired signal. The reference signal must be a signal correlated with the desired signal and uncorrelated with any interference. Generation of the reference signal with a biphase modulated signal is described below.

Table 1

Four Phase Modulation Techniques and Locally Generated Correlated Signals

Case No.	s(t) (Received desired signal)	$s_\ell(t)$ (Locally generated signals)	Correlation between s(t) and r(s)
1	$\sin(\omega_1 t+\alpha(t)+\beta(t))$ $[\beta(t) = b_m\pi/2$ only] (coherent encoding only)	$\sin(\omega_2 t+\alpha(t)+\psi)$ $\sin(\omega_2 t+\alpha(t)+\beta(t)+\psi)$	$\frac{1}{2}$ 1
2	$\sin(\omega_1 t+\alpha(t)+\beta(t))$	$\sin(\omega_2 t+\alpha(t)+\beta(t)+\psi)$	1
3	$\sin(\omega_1 t+\alpha(t)+\alpha(t)/2+\beta(t))$ $[\beta(t) = b_m\pi/2$ only] (coherent encoding only)	$\sin(\omega_2 t+\alpha(t)+\alpha(t)/2+\psi)$ $\sin(\omega_2 t+\alpha(t)+\alpha(t)/2+\beta(t)+\psi)$	$\frac{1}{2}$ 1
4	$\sin(\omega_1 t+\alpha(t)+\alpha(t)/2+\beta(t))$	$\sin(\omega_2 t+\alpha(t)+\alpha(t)/2+\beta(t)+\psi)$	1
5	$\frac{1}{\sqrt{2}}\sin(\omega_1 t+\theta(t))$ $+\frac{1}{\sqrt{2}}\cos(\omega_1 t+\phi(t))$	$\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)$ $\frac{1}{\sqrt{2}}\sin(\omega_2 t+\phi(t)+\psi)$ $\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)+\frac{1}{\sqrt{2}}\cos(\omega_2 t+\phi(t)+\psi)$	$\frac{1}{2}$ $\frac{1}{2}$ 1
6	$\frac{1}{\sqrt{2}}\sin(\omega_1 t+\theta(t))$ $+\frac{1}{\sqrt{2}}\cos(\omega_1 t+\phi(t)+\theta(t))$	$\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)$ $\frac{1}{\sqrt{2}}\sin(\omega_2 t+\phi(t)+\theta(t)+\psi)$ $\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)+\frac{1}{\sqrt{2}}\cos(\omega_2 t+\phi(t)+\theta(t)+\psi)$	$\frac{1}{2}$ $\frac{1}{2}$ 1

where

$$\alpha(t) = \left\{ \begin{array}{l} \pi a_m \\ \text{or} \\ \alpha_m = \alpha_{m-1} + \pi a_m \end{array} \right\} \quad (m-1)\,\Delta \le t \le m\,\Delta$$

$$\beta(t) = \left\{ \begin{array}{l} \pi/2b_m \\ \text{or} \\ \beta_m = \beta_{m-1} + \pi/2b_m \end{array} \right\} \quad (m-1)\,\Delta \le t \le m\,\Delta$$

$$\theta(t) = \left\{ \begin{array}{l} \pi a_m \\ \text{or} \\ \theta_m = \theta_{m-1} + \pi a_m \end{array} \right\} \quad (m-1)\,\Delta \le t \le m\,\Delta$$

$$\phi(t) = \left\{ \begin{array}{l} \pi b_m \\ \text{or} \\ \phi_m = \phi_{m-1} + \pi b_m \end{array} \right\} \quad (m-1)\,\Delta \le t \le m\,\Delta$$

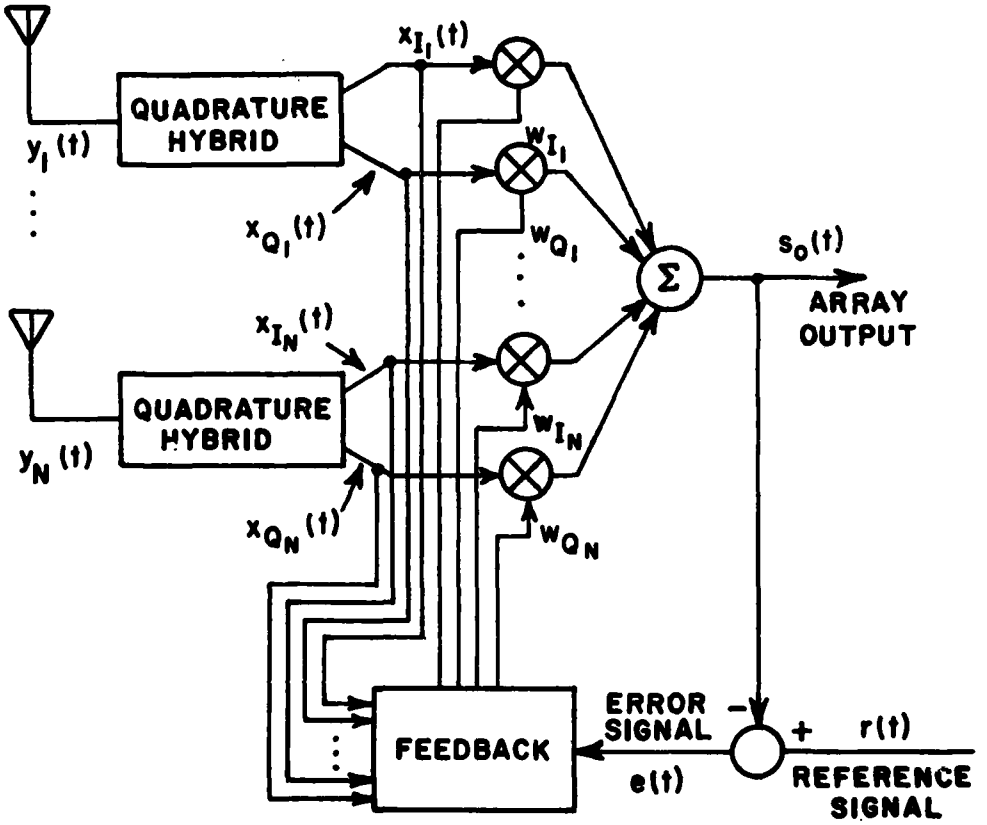

Figure 1.--Block diagram of an N element LMS adaptive array.

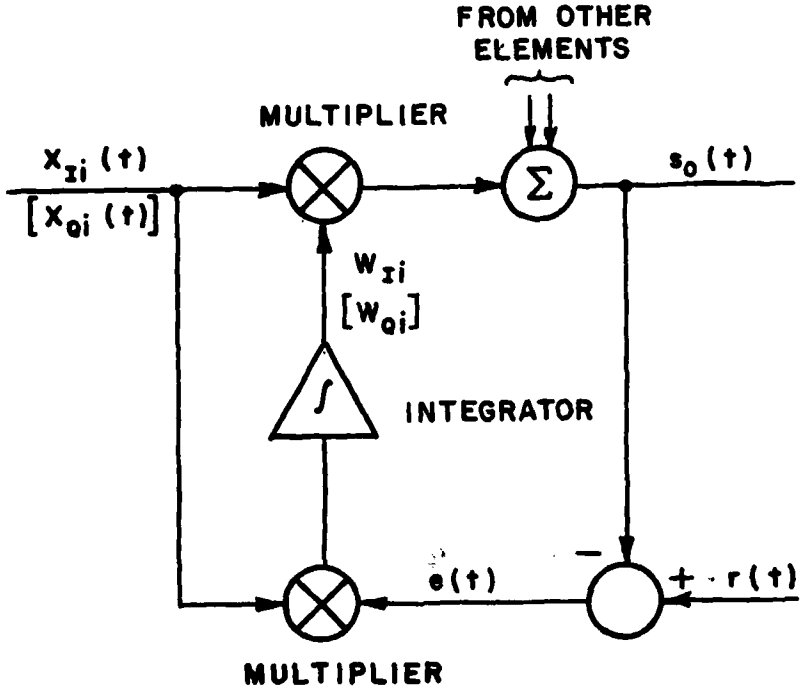

Figure 2.--Correlation feedback loop for the adaptive array.

The binary phase shift keyed or biphase signal described in [4] can be written as

$$s(t) = A \sin(\omega_1 t + \zeta(t)), \tag{1}$$

where A is an amplitude constant, ω_1 is the carrier frequency and $\zeta(t)$ is a binary waveform whose value switches between 0 and π. The waveform $\zeta(t)$ is made up of the modulo 2π sum of two symbol streams, $\alpha(t)$ and $\gamma(t)$. $\gamma(t)$ is the useful information (or data) sent over the communication system. The data symbol interval has a duration of T_b seconds. $\alpha(t)$ is a pseudonoise code, i.e., a maximum length linear shift register sequence [9]. The code symbol interval has a duration of Δ seconds (one chip interval). Thus, $\zeta(t)$ can be written as

$$\zeta(t) = \text{modulo } 2\pi(\alpha(t) + \gamma(t)), \tag{2}$$

where

$$\alpha(t) = \pi a_m \qquad \text{for } (m-1)\,\Delta \le t < m\Delta \tag{3}$$

and

$$\gamma(t) = \pi d_i \qquad \text{for } (i-1)\,T_b \le t < iT_b \ . \tag{4}$$

In the above equations, a_m (equal to 0 or 1) is the m-th code symbol and d_i (equal to 0 or 1) is the i-th data symbol. The data symbol interval is greater than the code symbol by the ratio

$$k = T_b/\Delta, \tag{5}$$

where k is an integer and is defined as the spreading ratio. It is assumed that the data symbol transitions coincide with the code symbol transitions.

It should be noted that, in many practical systems, the code and data symbols are differentially encoded. In these systems $\zeta(t)$ is given by

$$\zeta(t) = \alpha(t) + \gamma(t), \tag{6}$$

where

$$\alpha(t) = \alpha_m = \alpha_{m-1} + \pi a_m \qquad \text{for } (m-1)\,\Delta \le t < m\Delta \tag{7}$$

and

$$\gamma(t) = \gamma_i = \gamma_{i-1} + \pi d_i \qquad \text{for } (i-1)\,T_b \le t < iT_b. \tag{8}$$

For the biphase modulated signal, a reference signal can be generated from the array output signal as shown in Figure 3. The array output is first mixed with a locally generated signal given by

$$s_\ell(t) = B \sin(\omega_2 t + \alpha(t) + \psi), \tag{9}$$

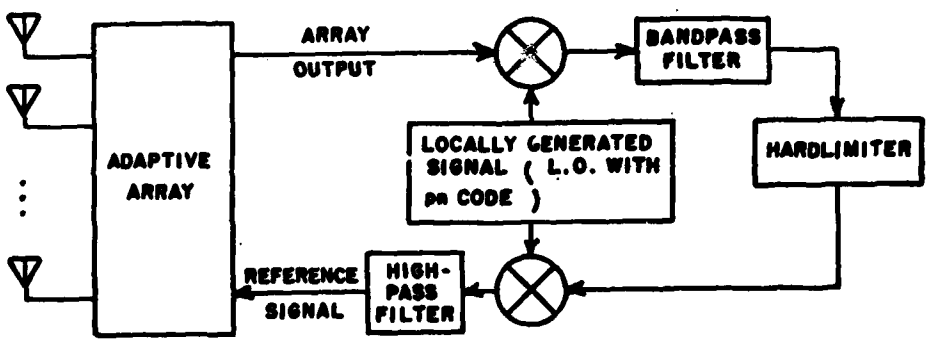

Figure 3. Reference signal generation loop with the adaptive array.

where B is an amplitude constant, ω_2 is the local oscillator (LO) frequency, and ψ is the phase difference between $s_\ell(t)$ and $s(t)$ in Equation (1) at t equal to 0. When the codes of the locally generated signal and the array output signal are synchronized, the lower frequency component of the mixer output is given by

$$s(t)\, s_\ell(t) = \frac{AB}{2} \sin((\omega_1-\omega_2)t + \gamma(t) + \psi). \qquad (10)$$

Thus, the lower frequency component has a bandwidth corresponding to the data rate. The mixer output is passed through a filter with this bandwidth. The desired signal component is, therefore, unchanged by the filter. The filter output is then hardlimited so that the reference signal will have constant amplitude. The hardlimiter output is mixed with the locally generated signal to produce the reference signal. The reference signal is then given by

$$r(t) = R \sin(\omega_1 t + \zeta(t)) \qquad (11)$$

where R is the amplitude. Thus, the reference signal is an amplitude scaled replica of the desired signal.

Any interference signal without the proper pseudonoise code has its waveform drastically changed by the reference loop. When the coded local oscillator signal is mixed with the interference, the interference spectrum is spread by the code bandwidth. The bandpass filter, therefore, changes the interference component out of the mixer. As a result, the interference at the array output is uncorrelated with the reference signal.

In the biphase system, the timing of the pseudonoise code is acquired and tracked at receiver by a delay lock loop shown in Figure 4. To acquire the code timing, the code generator at the receiver is run faster than the received signal's code. This code slewing is continued until the sum channel voltage in the delay lock loop exceeds the acquisition threshold (indicating the two codes are aligned). The sweep voltage is then switched off as shown in Figure 4.

With this so-called sliding correlation method, the code generated at the receiver is correlated with the received signal for as many as all possible timing offsets. Thus, the acquisition time is proportional to the code length, and the code length must be short for reasonable acquisition times.

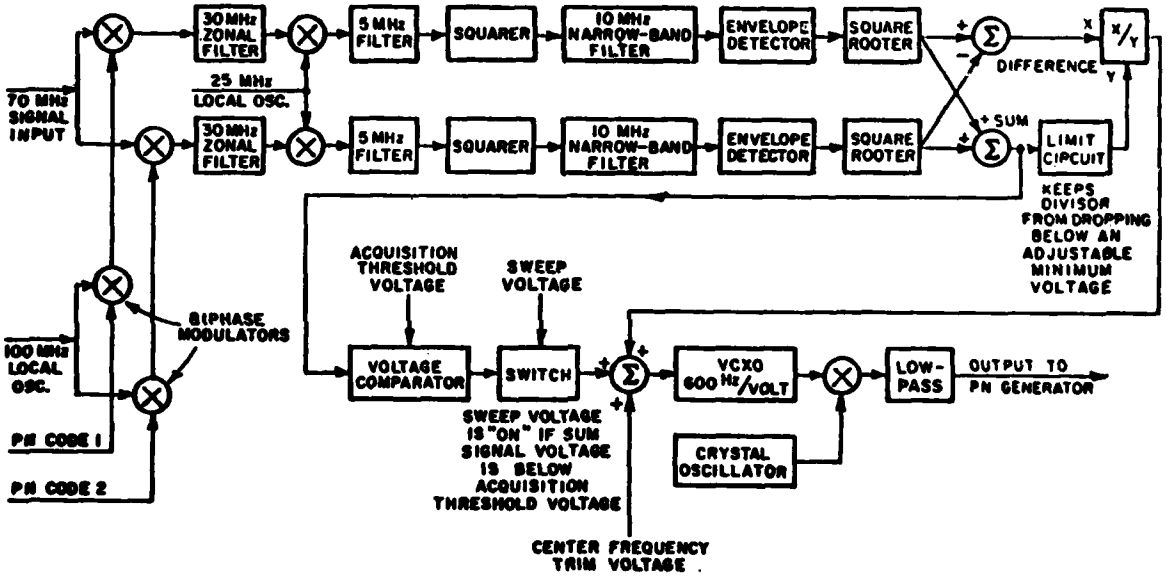

Figure 4.--Block diagram of the delay lock loop described in [4].

Short codes, however, may not have adequate security for many applications. The short code repeats often during transmission of the signal and, therefore, the code can easily be determined and used by a jammer. When the code modulates the jamming signal, the receiver is unable to distinguish the jamming signal from the desired signal. To overcome this problem, codes with very long periods are required.

For security and rapid acquisition, the signal must contain both a long and a short code. One method of combining the two codes is four-phase modulation. The next section discusses four-phase modulation with two codes.

C. Four-Phase Modulation Techniques

For security and rapid acquisition in a spread spectrum communication system with an adaptive array, the signal must contain both a long and a short code. This section considers how the two codes can be combined into a four-phase modulated signal. Both coherent and differential phase shift keyed modulated methods will be considered.

Two codes can modulate a four-phase or quadriphase shift keyed signal in two basic ways. Although these two modulation techniques could be described by one equation, the generation of reference signals (see Section D) is much clearer if two equations are used. Let the i-th code symbols for the two binary code streams be denoted by a_i and b_i (equal to 0 or 1). Then, for one modulation technique, the four-phase signal is

$$s(t) = \sin(\omega_1 t + \alpha(t) + \beta(t)) \tag{12}$$

where for coherent encoding

$$\left.\begin{aligned} \alpha(t) &= \gamma_m \pi \\ \beta(t) &= \delta_m \pi/2 \end{aligned}\right\} \quad (m-1)\,\Delta \leq t < m\Delta \tag{13, 14}$$

and for differential encoding

$$\left.\begin{aligned} \alpha(t) &= \alpha_m = \alpha_{m-1} + \gamma_m \pi \\ \beta(t) &= \beta_m = \beta_{m-1} + \delta_m \pi/2 \end{aligned}\right\} \quad (m-1)\,\Delta \leq t < m\Delta \tag{15, 16}$$

where

$$\gamma_m = f_1(a_m, b_m) = 0 \text{ or } 1, \tag{17}$$

and

$$\delta_m = f_2(a_m, b_m) = 0 \text{ or } 1. \tag{18}$$

The $f_1(\cdot)$ and $f_2(\cdot)$ are two arbitrary functions.

For the other modulation technique, the four-phase signal is

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \theta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \phi(t)) \tag{19}$$

where for coherent encoding

$$\left.\begin{aligned} \theta(t) &= \gamma_m \pi \qquad (20) \\ \phi(t) &= \delta_m \pi \qquad (21) \end{aligned}\right\} \quad (m-1)\,\Delta \leq t < m\Delta$$

and for differential encoding

$$\left.\begin{aligned} \theta(t) = \theta_m &= \theta_{m-1} + \gamma_m \pi \qquad (22) \\ \phi(t) = \phi_m &= \phi_{m-1} + \delta_m \pi \qquad (23) \end{aligned}\right\} \quad (m-1)\,\Delta \leq t < m\Delta\ .$$

The factor of $1/\sqrt{2}$ has been used in Equation (19) so that the signal power is the same as in Equation (12).

The functions $f_1(\cdot)$ and $f_2(\cdot)$ will now be considered to determine the number of different four-phase signals which combine two codes. These two functions can be combined into one function f, given by

$$(\gamma_m, \delta_m) = f(a_m, b_m). \tag{24}$$

For the signal, s(t), to contain the same information as the two code symbol streams, the function f must be one-to-one. There are four combinations of two code symbols. Therefore, there are 4! possible mappings between the four permutations of (a_m, b_m) and the four permutations of (γ_m, δ_m), or 24 one-to-one functions. As an example, five of these functions are given by

$$\gamma_m = a_m \tag{25a}$$

$$\delta_m = b_m, \tag{25b}$$

$$\gamma_m = a_m \tag{26a}$$

$$\delta_m = a_m \oplus b_m, \tag{26b}$$

$$\gamma_m = b_m \tag{27a}$$

$$\delta_m = a_m, \tag{27b}$$

$$\gamma_m = \bar{a}_m \tag{28a}$$

$$\delta_m = b_m, \tag{28b}$$

and

$$\gamma_m = a_m \oplus b_m \tag{29a}$$

$$\delta_m = a_m, \tag{29b}$$

where $\oplus$ represents the exclusive-or operation and the overbar denotes the inverse of the code symbol.

Most of the twenty four functions need not be considered for two reasons. First, the inverting of a symbol stream changes the code, but not the modulation method. For each of the twenty four functions, there are three others (in the set of twenty four) that can be obtained by inverting either one or both code symbol streams.

For this reason, only six functions need be considered. The functions given in Equations (25) and (28) provide an example of the inverting of a symbol stream. Second, the designation of the two symbol streams as a_j or b_j is arbitrary. For each of the remaining six functions, there is one other (in the set of six) that can be obtained by interchanging the a_j and b_j code symbols. For this reason, only three functions need be considered. The functions given in Equations (25) and (27) provide an example of this interchanging of symbols. Three functions which represent all twenty four functions are given by Equations (25), (26) and (29). Because the function given by Equation (29) can be obtained from that of Equation (26) by interchanging γ_m and δ_m, the former function will not be considered in determining different four-phase signals. Thus, the two functions or mappings to be considered are given by Equations (25) and (26).

With the above two mappings used with each of the two modulation techniques (given by Equations (12) and (19)) four different four-phase signals can be obtained. These are given by

$$s(t) = \sin(\omega_1 t + \alpha(t) + \beta(t)), \tag{30}$$

$$s(t) = \sin(\omega_1 t + \alpha(t) + \alpha(t)/2 + \beta(t)) , \tag{31}$$

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t+\theta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t+\phi(t)) , \tag{32}$$

and

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t+\theta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t+\theta(t)+\phi(t)) \tag{33}$$

where for coherent encoding

$$\left.\begin{aligned} \alpha(t) &= a_m\pi \qquad (34)\\ \beta(t) &= b_m\pi/2 \qquad (35)\end{aligned}\right\} \quad (m-1)\,\Delta \le t < m\Delta$$

or

$$\left.\begin{aligned} \theta(t) &= a_m\pi \qquad (36)\\ \phi(t) &= b_m\pi \qquad (37)\end{aligned}\right\} \quad (m-1)\,\Delta \le t < m\Delta$$

and for differential encoding

$$\left.\begin{aligned} \alpha(t) &= \alpha_m = \alpha_{m-1} + a_m\pi \\ \beta(t) &= \beta_m = \beta_{m-1} + b_m\pi/2 \end{aligned}\right\} (m-1)\,\Delta \le t < m\Delta \qquad (38),\ (39)$$

or

$$\left.\begin{aligned} \theta(t) &= \theta_m = \theta_{m-1} + a_m\pi \\ \phi(t) &= \phi_m = \phi_{m-1} + b_m\pi \end{aligned}\right\} (m-1)\,\Delta \le t < m\Delta\ . \qquad (40),\ (41)$$

Therefore, because either of two encoding methods (coherent or differential) may be used with each of the four signals, there are eight different ways to generate a four-phase signal from two codes.

D. Reference Signal Generation

To use a four-phase signal with an LMS adaptive array, a reference signal must be generated from the signal. This section discusses reference signal generation for each of the signals given in Equations (30) through (41). For each signal, the locally generated signals will be determined that can be used to generate reference signals when either one or both codes are synchronized at the receiver.

With a four-phase signal the same type of reference signal generation loop may be used as with the biphase signal (see Figure 3). Reference signal generation with this loop is described below for each of the different four-phase signals.

For s(t) as given in Equation (30), if only the first code stream is synchronized, a reference signal can be generated as follows. The locally generated signal, $s_\ell(t)$, in this case, is

$$s_\ell(t) = \sin(\omega_2 t + \alpha(t) + \psi). \qquad (42)$$

The product of $s_\ell(t)$ and s(t) is given by

$$s_\ell(t) \cdot s(t) = \frac{1}{2}\cos((\omega_1-\omega_2)t + \beta(t) - \psi) + s_n(t), \qquad (43)$$

where $s_n(t)$ contains the products not of interest. If $\beta(t)$ has been derived from b_m through coherent encoding (Equation (35)) then $\beta(t)$ is either 0 or $\pi/2$ and the product may be expressed as

$$s_\ell(t)\, s(t) = \frac{1}{2\sqrt{2}} \cos((\omega_1-\omega_2)t + \pi/4 - \psi) + \frac{1}{2\sqrt{2}} \sin((\omega_1-\omega_2)t + \pi/4 + \pi b_m - \psi) + s_n(t) \qquad (44)$$

for $(m-1)\,\Delta \leq t \leq m\Delta$. Therefore, a cw component is present in the mixer output. Because of this cw component, a reference signal correlated with the received signal can be generated as shown below. The output of the bandpass filter* in the reference loop will mainly consist of the component given by the first term in Equation (44). All other signal components will be drastically altered. The reference signal, $r(t)$, as given in Figure 2 is then

$$r(t) = F_{HP}\left\{s_\ell(t)\, \frac{1}{2\sqrt{2}} \cos((\omega_1-\omega_2)t + \pi/4 - \psi))\right\} \qquad (45)$$

where $F_{HP}\{\cdot\}$ is the output of the high-pass filter or

$$r(t) = \frac{1}{4\sqrt{2}} \sin(\omega_1 t + \alpha(t) + \pi/4). \qquad (46)$$

(Note that R in this case is $1/(4\sqrt{2})$.)

This reference signal can be shown to be correlated with $s(t)$ as follows. The signal, $s(t)$, as given in Equation (30) for coherent encoding, can be expressed as

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \alpha(t) + \pi/4) + \sin(\beta(t) - \pi/4) \cdot \cos(\omega_1 t + \alpha(t) + \pi/4). \qquad (47)$$

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*Because data is not modulating the four-phase signal, the filter bandwidth can be very small.

The correlation of s(t) and r(t) is then given by

$$R_{sr} = \frac{E\,[s(t)\,r(t)]}{\sqrt{E[s^2(t)\,r^2(t)]}} = \frac{1}{2}\ , \tag{48}$$

where E[·] denotes expected value. Thus, the reference signal is partially correlated with the desired signal. The effect of partial correlation on array performance is discussed in Chapter IV.

For s(t) as given in Equation (30) with differential encoding (Equation (39)), $\beta(t)$ may take on any of the four phase values. Thus, the product of $s_\ell(t)$ (as given in Equation (42)) and s(t) as given in Equation (43) does not contain any cw component. Therefore, in this case no reference signal can be generated with only the one code synchronized at the receiver.

For s(t) as given in Equation (30), if only the second code symbol stream is synchronized, $s_\ell(t)$ is

$$s_\ell(t) = \sin(\omega_2 t + \beta(t) + \psi). \tag{49}$$

The product of $s_\ell(t)$ and s(t) is given by

$$s_\ell(t)\ s(t) = \frac{1}{2}\cos((\omega_1-\omega_2)t + \alpha(t) - \psi) + s_n(t). \tag{50}$$

For both coherent and differential encoding there is no cw component in the product term and, therefore, $s_\ell(t)$ as given in Equation (49) cannot be used to generate a reference signal.

For s(t) as given in Equation (30), if both code symbol streams are synchronized, $s_\ell(t)$ is

$$s_\ell(t) = \sin(\omega_2 t + \alpha(t) + \beta(t) + \psi). \tag{51}$$

The product of $s_\ell(t)$ and s(t) is given by

$$s_\ell(t)\ s(t) = \frac{1}{2}\cos((\omega_1-\omega_2)t - \psi) + s_n(t). \tag{52}$$

Thus, $s_\ell(t)$ can be used to generate a reference signal. It can easily be shown that the correlation of s(t) and the reference signal is one.

For s(t) as given in Equation (31) the same results as presented above apply with $\alpha(t)$ replaced by $\alpha(t) + \alpha(t)/2$. This is shown in Table 1.

For s(t) as given in Equation (32) if only the first code symbol stream is synchronized, $s_\ell(t)$ is

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi). \tag{53}$$

The product of $s_\ell(t)$ and s(t) is given by

$$s_\ell(t)\, s(t) = \frac{1}{4} \cos((\omega_1-\omega_2)t - \psi) + s_n(t). \tag{54}$$

Thus, $s_\ell(t)$ can be used to generate a reference signal. It can easily be shown that the correlation of s(t) and the reference signal is one half. A similar result is obtained if only the second code symbol stream is synchronized. If both symbol streams are synchronized $s_\ell(t)$ is

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) + \frac{1}{\sqrt{2}} \cos(\omega_2 t + \phi(t)). \tag{55}$$

The product of $s_\ell(t)$ and s(t) is given by

$$s_\ell(t)\, s(t) = \frac{1}{2} \cos((\omega_1-\omega_2 t - \psi) + s_n(t). \tag{56}$$

Thus, $s_\ell(t)$ can be used to generate a reference signal. It can easily be shown that the correlation of s(t) and the reference signal is one.

For s(t) as given in Equation (33) if only the first code symbol stream is synchronized, $s_\ell(t)$ is

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi). \tag{57}$$

The product of $s_\ell(t)$ and s(t) is given by

$$s_\ell(t)\, s(t) = \frac{1}{4} \cos((\omega_1-\omega_2)t - \psi) + s_n(t), \tag{58}$$

Thus, $s_\ell(t)$ can be used to generate a reference signal. It can easily be shown that the correlation of $s(t)$ and the reference signal is one half. If only the second symbol stream is synchronized, then it can be shown that no reference signal can be generated. If both symbol streams are synchronized, then there are two possible locally generated signals. One signal is given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \phi(t) + \theta(t) + \psi). \tag{59}$$

The product of $s_\ell(t)$ and $s(t)$ is given by

$$s_\ell(t)\, s(t) = \frac{1}{4} \sin((\omega_1-\omega_2)t - \psi) + s_n(t). \tag{60}$$

Thus, $s_\ell(t)$ can be used to generate a reference signal whose correlation with $s(t)$ can be shown to be one half. Another locally generated signal is

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) + \frac{1}{\sqrt{2}} \cos(\omega_2 t + \phi(t) + \theta(t) + \psi). \tag{61}$$

The product of $s_\ell(t)$ and $s(t)$ is given by

$$s_\ell(t)\, s(t) = \frac{1}{2} \cos((\omega_1-\omega_2)t - \psi) + s_n(t). \tag{62}$$

Thus, $s_\ell(t)$ can be used to generate a reference signal whose correlation with $s(t)$ can be shown to be one.

The results of this section are summarized in Table 1. Thus, in this chapter eight possible ways to modulate a four-phase signal with two codes have been shown, and several ways to generate reference signals for these four-phase signals have been determined.

CHAPTER III

DATA MODULATION METHODS

A. Introduction

In Chapter II four-phase modulation techniques were discussed which involved two codes. In this chapter the addition of data to these four-phase signals is considered. Several methods for adding data to the signals will be described. For each method the resulting four-phase signals will be examined to determine if each of the locally generated signals listed in Table 1 still generates a reference signal.

For a reference signal to be generated it is necessary for the product of the locally generated signal and the received signal to contain a component whose bandwidth is much narrower than the received signal itself. Thus, there will be a processing gain for the desired signal in the reference loop of Figure 3. Specifically, some type of spread spectrum signal is required as in the biphase system. That is, the data rate must be less than (in general, an integer multiple less than) the code modulation rate.

There are several ways to add data to the four-phase signal which result in some type of spread spectrum signal. The three methods considered in this chapter are 1) mixing a data bit stream with one code, 2) mixing two data bit streams with the two codes and 3) mixing one data bit stream to both codes (i.e., the same data bits are mixed with each code).

In Chapter II the code symbols were encoded either coherently or differentially because the detection of the code symbols was not required. However, the data bits must be detected. If the signal is to be rapidly acquired by the receiver and the data detected immediately, then differential encoding (with differential detection) of the data is required. Therefore, only differential encoding of the data is considered in this chapter.

The three data modulation methods are described below. For each method the various four-phase signals are analyzed to determine if the locally generated signals listed in Table 1 can be used. Results are summarized in Table 2.

Table 2

Locally Generated Signals for Several Data Modulation Techniques

Four-Phase Signal With Two Codes Only	Code Symbol Stream To Which Data is Added	Locally Generated Signal Which Generates Reference Signal
$\sin(\omega_1 t+\alpha(t)+\beta(t))$ [$\beta(t)=b_i\pi/2$ only (coherent encoding)]	a_i b_i a_i+b_i a_i+b_i (equal data)	$\sin(\omega_2 t+\alpha(t)+\psi)$ $\sin(\omega_2 t+\alpha(t)+\beta(t)+\psi)$
$\sin(\omega_1 t+\alpha(t)+\beta(t))$	a_i b_i a_i+b_i a_i+b_i (equal data)	$\sin(\omega_2 t+\alpha(t)+\beta(t)+\psi)$
$\sin(\omega_1 t+\alpha(t)+\alpha(t)/2+\beta(t)$ [$\beta(t)=b_i\pi/2$ only (coherent encoding]	a_i b_i	$\sin(\omega_2 t+\alpha(t)+\alpha(t)/2+\beta(t)+\psi)$
$\sin(\omega_1 t+\alpha(t)+\alpha(t)/2+\beta(t)$	a_i b_i	$\sin(\omega_2 t+\alpha(t)+\alpha(t)/2+\beta(t)+\psi)$
$\frac{1}{\sqrt{2}}\sin(\omega_1 t+\theta(t))$ $+\frac{1}{\sqrt{2}}\cos(\omega_1 t+\phi(t))$	a_i b_i a_i+b_i	$\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)$ $\frac{1}{\sqrt{2}}\sin(\omega_2 t+\phi(t)+\psi)$
	a_i+b_i	$\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)$ $\frac{1}{\sqrt{2}}\sin(\omega_2 t+\phi(t)+\psi)$ $\left[\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)\right.$ $\left.+\frac{1}{\sqrt{2}}\cos(\omega_2 t+\phi(t)+\psi)\right]$

Table 2 (Continued)

$\frac{1}{\sqrt{2}}\sin(\omega_1 t+\theta(t))$ $+\frac{1}{\sqrt{2}}\cos(\omega_1 t+\theta(t)+\phi(t))$	a_1	$\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)$ $\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\phi(t)+\psi)$ $\left[\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)\right.$ $\left.+\frac{1}{\sqrt{2}}\cos(\omega_2 t+\theta(t)+\phi(t)+\psi)\right]$
	b_1 a_1+b_1 a_1+b_1 (equal data)	$\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\psi)$ $\frac{1}{\sqrt{2}}\sin(\omega_2 t+\theta(t)+\phi(t)+\psi)$

B. Data Mixed With One Code

In this section data modulation is considered where the data bits are added to one code symbol stream only. First to be considered is the addition of data bits to the a_i code symbols, followed by the b_i code symbols.

For case No. 1, Table 1, when data is added to the a_i code symbols, the resulting signal may be expressed as

$$s(t) = \sin(\omega_1 t + \zeta(t) + \beta(t)), \tag{63}$$

where

$$\zeta(t) = \alpha(t) + \gamma(t) \tag{64}$$

where

$$\gamma(t) = \gamma_i = \gamma_{i-1} + \pi d_{1i} \tag{65}$$

for $(i-1)T_b \leq t < iT_b$, where d_{1i} is the i-th data symbol in the first (and in this case, only) data symbol stream, T_b is the bit interval and γ_0 is equal to 0. It should be noted that the spreading ratio, k, is given by

$$k = T_b/\Delta \quad . \tag{66}$$

From Table 1 one possible locally generated signal is given by

$$s_\ell(t) = \sin(\omega_2 t + \alpha(t) + \psi). \tag{67}$$

The resulting product of $s_\ell(t)$ and $s(t)$ is given by

$$s_\ell(t)\, s(t) = \frac{1}{2\sqrt{2}} \cos\left((\omega_1-\omega_2)t + \gamma(t) + \pi/4 - \psi\right) + s_n(t). \tag{68}$$

Because the first term in the above equation has a bandwidth on the order of the data modulation rate, a reference signal can be generated using the locally generated signal given in Equation (67).

From Table 1 another possible locally generated signal is given by

$$s_\ell(t) = \sin(\omega_2 t + \alpha(t) + \beta(t) + \psi). \tag{69}$$

The resulting product of $s_\ell(t)$ and $s(t)$ is given by

$$s_\ell(t)\, s(t) = \frac{1}{2}\cos((\omega_1-\omega_2)t + \gamma(t) + \psi) + s_n(t). \tag{70}$$

Thus, a reference signal can be generated using $s_\ell(t)$ as given in Equation (69).

For case No. 2, Table 1, with data added to the a_i code symbols, the locally generated signal given for this case can easily be shown to generate a reference signal.

For cases No. 3 and 4, Table 1, with data added to the a_i code symbols, the resulting signal may be expressed as

$$s(t) = \sin(\omega_1 t + \zeta(t) + \zeta(t)/2 + \beta(t)) \tag{71}$$

where $\zeta(t)$ is given in Equations (64) and (65). For cases No. 3 and 4 it can easily be shown by the same method presented for cases No. 1 and 2 that reference signals can be generated using the locally generated signals listed in Table 1.

For case No. 5, with data added to the a_i code stream, the resulting signal may be expressed as

$$s(t) = \frac{1}{\sqrt{2}}\sin(\omega_1 t + \zeta(t)) + \frac{1}{\sqrt{2}}\cos(\omega_1 t + \phi(t)) \tag{72}$$

where

$$\zeta(t) = \theta(t) + \gamma(t) \tag{73}$$

and $\gamma(t)$ is given in Equation (65). For the locally generated signals given by

$$s_\ell(t) = \frac{1}{\sqrt{2}}\sin(\omega_2 t + \theta(t) + \psi) \tag{74}$$

and

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \phi(t) + \psi) \tag{75}$$

it can easily be shown that a reference signal can be generated. If the locally generated signal is given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) + \frac{1}{\sqrt{2}} \cos(\omega_2 t + \phi(t) + \psi) \tag{76}$$

then the product of $s_\ell(t)$ and $s(t)$ as given in Equation (72) is given by

$$s_\ell(t)\, s(t) = \frac{1}{4} \cos((\omega_1-\omega_2)t + \gamma(t) - \psi) + \frac{1}{4} \cos((\omega_1-\omega_2)t - \psi) + s_n(t). \tag{77}$$

Equation (77) may be expressed as

$$s_\ell(t)\, s(t) = \frac{1}{2} \cos((\omega_1-\omega_2)t - \psi) + s_n(t) \tag{78}$$

for $\gamma(t) = 0$,

and

$$s_\ell(t)\, s(t) = s_n(t) \tag{79}$$

for $\gamma(t) = \pi$.

From Equation (65), it should be noted that $\gamma(t)$ may only take on values of 0 or π. Thus, the output of the bandpass filter and hardlimiter shown in Figure 3 will be a cw signal randomly turned on and off at the data rate. The pulsed signal results in a pulsed reference signal which is correlated with the desired signal only half the time. Thus, the locally generated signal given by Equation (76) cannot be used to generate a reference signal for use by the adaptive array.

For case No. 6, with data added to the a_i code symbol stream, the resulting signal is given by

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \zeta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \zeta(t) + \phi(t)). \tag{80}$$

For the signal given by Equation (80) it can easily be shown that the locally generated signal listed in Table 1 will generate reference signals.

When data is added to the b_i code symbol stream only, the resulting signals for the first four cases in Table 1 may be expressed as

$$s(t) = \sin(\omega_1 t + \alpha(t) + \xi(t)) \tag{81}$$

for cases No. 1 and 2, and

$$s(t) = \sin(\omega_1 t + \alpha(t) + \alpha(t)/2 + \xi(t)) \tag{82}$$

for cases No. 3 and 4, where

$$\xi(t) = \beta(t) + \delta(t) \tag{83}$$

where

$$\delta(t) = \delta_i = \delta_{i-1} + \pi/2\ d_{2i} \tag{84}$$

for $(i-1)\ T_b \leq t < iT_b$, where d_{2i} is the i-th data symbol in the second (and in this case only) data symbol stream and δ_0 is equal to 0. For each of these cases the locally generated signals listed in Table 1 can be shown to generate reference signals.

With data added to the b_i code symbol stream, the resulting signals for the last two cases of Table 1 are given by

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \theta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \nu(t)) \tag{85}$$

for case No. 5, and

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \theta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \theta(t) + \nu(t)) \quad (86)$$

for case No. 6, where

$$\nu(t) = \phi(t) + \eta(t) \quad (87)$$

where

$$\eta(t) = \eta_i = \eta_{i-1} + \pi d_{2i} \quad (88)$$

for $(i-1)\ T_b \leq t < iT_b$ and η_0 is equal to 0.

For the signal given by Equation (85) the same reference signal generation results apply as for the case where data is added only to the a_i code symbol stream. That is, the locally generated signals given by Equations (74) and (75) but not Equation (76) can be used to generate a reference signal.

For the signal given by Equation (86), the locally generated signals given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) \quad (89)$$

and

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \phi(t) + \psi) \quad (90)$$

can be shown to generate reference signals. If the locally generated signal is given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) + \frac{1}{\sqrt{2}} \cos(\omega_2 t + \theta(t) + \phi(t) + \psi) \quad (91)$$

then the product of $s_\ell(t)$ and $s(t)$ as given in Equation (86) is given by

$$s_\ell(t)\, s(t) = \frac{1}{4}\cos((\omega_1-\omega_2)t - \psi)$$

$$+ \frac{1}{4}\cos((\omega_1-\omega_2)t + \eta(t) - \psi)$$

$$+ s_n(t). \qquad (92)$$

Equation (92) may be expressed as

$$s_\ell(t)\, s(t) = \frac{1}{2}\cos((\omega_1-\omega_2)t - \psi) + s_n(t) \qquad (93)$$

for $\eta(t) = 0$,

and

$$s_\ell(t)\, s(t) = s_n(t) \qquad (94)$$

for $\eta(t) = \pi$.

Therefore, as before, $s_\ell(t)$ as given in Equation (91) cannot be used to generate a reference signal.

Thus, when data is added to the a_i code symbol stream, all but one of the locally generated signals listed in Table 1 can be used to generate a reference signal. When data is added to the b_i code stream, all but two of the locally generated signals may be used.

C. Data Mixed With Both Codes

In this section data modulation is considered where two data bit streams, d_{1i} and d_{2i}, are mixed with the two codes. The resulting four-phase signals are first listed and the generation of reference signals for each case investigated.

With data added to both code symbol streams, the resulting four-phase signals for each case in Table 1 are given by

$$s(t) = \sin(\omega_1 t + \zeta(t) + \xi(t)) \qquad (95)$$

for cases No. 1 and 2,

$$s(t) = \sin(\omega_1 t + \zeta(t) + \zeta(t)/2 + \xi(t)) \tag{96}$$

for cases No. 3 and 4,

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \zeta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \nu(t)) \tag{97}$$

for case No. 5, and

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \zeta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \zeta(t) + \nu(t)) \tag{98}$$

for case No. 6, where $\zeta(t)$, $\xi(t)$, and $\nu(t)$ are given by Equations (64), (83), and (87), respectively.

For the signals given by Equations (95) and (96), it can easily be shown that the locally generated signals listed in Table 1 for cases No. 1 through 4 will generate reference signals. However, for the signal given by Equation (96) it can be seen that it is impossible to determine the data values when d_{1i} is equal to d_{2i}. Therefore, the signal given by Equation (96) cannot be used to transmit two data streams.

For the signals given by Equations (97) and (98) the locally generated signal given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) \tag{99}$$

can be shown to generate a reference signal. Also, for the signal given by Equation (97) the locally generated signal given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \phi(t) + \psi) \tag{100}$$

can be shown to generate a reference signal. Furthermore, for the signal given by Equation (98), the locally generated signal given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \theta(t) + \phi(t) + \psi) \tag{101}$$

can be shown to generate a reference signal. The remaining locally generated signals will now be examined in detail. For s(t) as given

in Equation (97) and $s_\ell(t)$ given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) + \frac{1}{\sqrt{2}} \cos(\omega_2 t + \phi(t) + \psi) \tag{102}$$

the product of the two signals is given by

$$\begin{aligned} s_\ell(t)\, s(t) = {} & \frac{1}{4} \cos((\omega_1-\omega_2)t + \gamma(t) - \psi) \\ & + \frac{1}{4} \cos((\omega_1-\omega_2)\, t + \eta(t) - \psi) \\ & + s_n(t) \quad . \end{aligned} \tag{103}$$

It can be seen that Equation (103) may be expressed as

$$s_\ell(t)\, s(t) = \frac{1}{2} \cos((\omega_1-\omega_2)t + \gamma(t) - \psi) + s_n(t) \tag{104}$$

for $\gamma(t) = \eta(t)$

and

$$s_\ell(t)\, s(t) = s_n(t) \tag{105}$$

for $\gamma(t) = \eta(t) + \pi$.

From Equations (65) and (88), it should be noted that the two relationships between $\gamma(t)$ and $\eta(t)$ given above are the only ones possible. Thus, the output of the bandpass filter and hardlimiter is a cw signal randomly turned on and off at the data rate. The pulsed signal results in a pulsed reference signal which is correlated with the desired signal only half the time. Thus, the locally generated signal given by Equation (102) cannot be used to generate a reference signal for use by the adaptive array.

For the signal given by Equation (98) and $s_\ell(t)$ given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) + \frac{1}{\sqrt{2}} \cos(\omega_2 t + \theta(t) + \phi(t) + \psi), \tag{106}$$

results similar to those presented above are obtained. Thus, the locally generated signal given by Equation (106) cannot be used to generate a reference signal for use by the adaptive array.

Thus, when two data symbol streams are added to both code symbol streams, all but two of the locally generated signals listed in Table 1 can be used to generate reference signals.

D. Like Data Mixed With Both Codes

In this section data modulation is considered where the same data bit streams are mixed with the two codes. Thus, the resulting four-phase signals are given by Equations (95) through (98) with

$$d_{1i} = d_{2i}. \tag{107}$$

Reference signal generation for the individual cases is discussed below.

For s(t) as given in Equation (95) the locally generated signals from Table 1 for cases No. 1 and 2 can be shown to generate reference signals.

For s(t) as given in Equation (96) it can be seen that, since d_{1i} is equal to d_{2i}, there is no net phase shift in the signal due to data. Therefore, data modulation of this type cannot be used with this signal.

For s(t) as given in Equation (97) with d_{1i} equal to d_{2i} it can be shown that the locally generated signals listed in Table 1 can be used to generate reference signals.

For s(t) as given in Equation (98) with d_{1i} equal to d_{2i} it can be shown that the locally generated signals given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) \tag{108}$$

and

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \phi(t) + \psi) \tag{109}$$

can be used to generate reference signals. With the locally generated signal given by

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi)$$

$$+ \frac{1}{\sqrt{2}} \cos(\omega_2 t + \theta(t) + \phi(t) + \psi), \qquad (110)$$

the product of $s_\ell(t)$ and $s(t)$ as given in Equation (98) is given by

$$s_\ell(t)\, s(t) = \frac{1}{4} \cos((\omega_1-\omega_2)t + \gamma(t) - \psi)$$

$$+ \frac{1}{4} \cos((\omega_1-\omega_2)t - \psi) + s_n(t). \qquad (111)$$

Equation (111) may be expressed as

$$s_\ell(t)\, s(t) = \frac{1}{2} \cos((\omega_1-\omega_2)t - \psi) + s_n(t) \qquad (112)$$

for $\gamma(t) = 0$,

and

$$s_\ell(t)\, s(t) = s_n(t) \qquad (113)$$

for $\gamma(t) = \pi$.

Thus, the locally generated signal given by Equation (110) cannot be used to generate a reference signal.

Thus, when the same data bit stream is mixed with the two codes all but one of the locally generated signals listed in Table 1 can be used to generate reference signals. A summary of the results of this chapter is presented in Table 2.

CHAPTER IV

LMS ADAPTIVE ANTENNA PERFORMANCE WITH A PARTIALLY CORRELATED REFERENCE SIGNAL

A. Introduction

In Chapters II and III some of the reference signals considered were only partially correlated to the received signal. In this chapter the effect that a partially correlated reference signal has on the adaptive antenna performance is studied and compared to the performance where the reference signal is fully correlated with the received signal.

As seen in Table 1 the correlation of the reference signal and the received signal is either 1 (fully correlated case) or 1/2 (partially correlated case). These two cases are analyzed and compared below. The parameters of interest include the steady state element weights, the array output signal-to-noise ratio, and the error signal in the array. The first parameters considered are the steady state element weights for an N element antenna array with desired signal and noise present at the receiver. The resulting signal-to-noise ratio for both types of reference signals is then determined. Finally, the error signal for one loop of the adpative array is examined in detail.

B. The Steady State Element Weights

In this section the steady state adaptive array element weights are compared for the partially and fully correlated reference signals. A block diagram of an N element LMS array is shown in Figure 5. The signal received by the ith element, $y_i(t)$, is split with a quadrature hybrid into an inphase signal, $x_{I_i}(t)$, and a quadrature signal, $x_{Q_i}(t)$. These signals are then multiplied by controllable weight w_{I_i} or w_{Q_i}. The weighted signals are summed to form the array output, $s_o(t)$. The array output is subtracted from the reference signal to form the error signal, $e(t)$. The element weights are generated from the error signal and the $x_{I_i}(t)$ and $x_{Q_i}(t)$ signals.

The four-phase signals to be considered in this chapter is given by

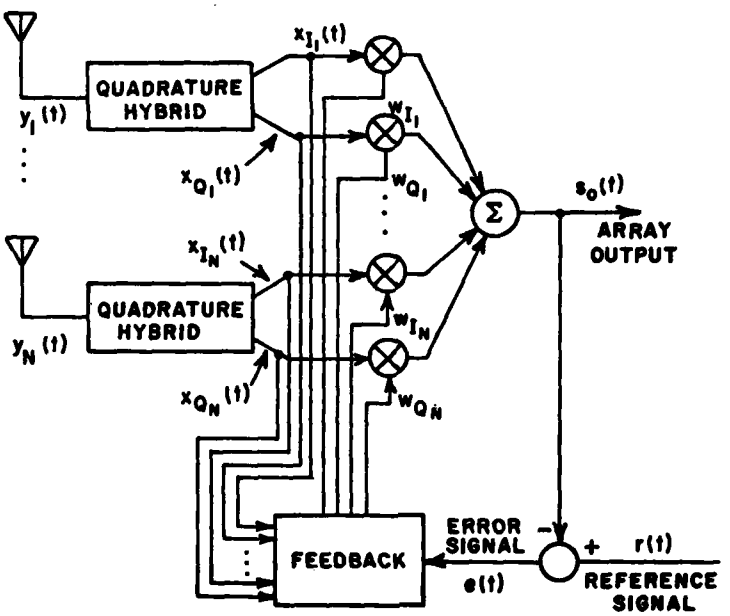


Figure 5. The LMS adaptive array.

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \theta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \phi(t)) \quad . \tag{114}$$

The results of this chapter will be the same for the other four-phase signals as well. The signal received by the ith element may be expressed as

$$y_i(t) = \frac{A_d}{\sqrt{2}} \sin(\omega_1 t + \theta(t) + \kappa_i) + \frac{A_d}{\sqrt{2}} \cos(\omega_1 t + \phi(t) + \kappa_i) + n_i(t) \quad , \tag{115}$$

where $A_d^2/2$ is the power of the received signal, κ_i is the phase difference in the signal between the first and the ith element, and $n_i(t)$ is the noise received by the ith element. The reference signal for the fully correlated signal case, $r_1(t)$, may be given by

$$r_1(t) = \frac{R}{\sqrt{2}} \sin(\omega_1 t + \theta(t)) + \frac{R}{\sqrt{2}} \cos(\omega_1 t + \phi(t)) \qquad (116)$$

where $R^2/2$ is the power of the reference signal. The reference signal for the partially correlated case, $r_2(t)$, may be given by

$$r_2(t) = R \sin(\omega_2 t + \theta(t)) \quad . \qquad (117)$$

For the received signal given by Equation (115), the inphase signal out the quadrature hybrid is given by

$$x_{I_i}(t) = \frac{A_d}{\sqrt{2}} \sin(\omega_1 t + \theta(t) + \kappa_i) + \frac{A_d}{\sqrt{2}} \cos(\omega_1 t + \phi(t) + \kappa_i) + n_{I_i}(t) \quad , \qquad (118)$$

where $n_{I_i}(t)$ is the inphase component of the noise. Similarly, the quadrature signal out of the quadrature hybrid is given by

$$x_{Q_i}(t) = \frac{A_d}{\sqrt{2}} \sin(\omega_1 t + \theta(t) + \kappa_i + \pi/2) + \frac{A_d}{\sqrt{2}} \cos(\omega_1 t + \phi(t) + \kappa_i + \pi/2) + n_{Q_i} \quad , \qquad (119)$$

where $n_{Q_i}(t)$ is the quadrature component of the noise.

For the N element array, let the element weight vector be given by

$$W_r = \begin{pmatrix} w_{I_1} \\ w_{Q_1} \\ \vdots \\ w_{I_N} \\ w_{Q_N} \end{pmatrix} \qquad (120)$$

and the signal vector, X_r, be given by

$$X_r = \begin{pmatrix} x_{I_1} \\ x_{Q_1} \\ \vdots \\ x_{I_N} \\ x_{Q_N} \end{pmatrix} \tag{121}$$

The signal covariance matrix, Φ_r, is defined by

$$\Phi_r \triangleq E[X_r X_r^T] \tag{122}$$

where $E[\cdot]$ denotes expected value and X_r^T denotes the transpose of X_r. The reference correlation vector S_r is defined by

$$S_r = E[X_r r(t)] \quad . \tag{123}$$

For the LMS algorithm [1] it can be shown that the steady state element weights are given by

$$W_r = \Phi_r^{-1} S_r \tag{124}$$

(where Φ_r^{-1} denotes the inverse of Φ_r) when Φ_r is nonsingular (this will always be true when noise is present at the receiver). A comparison will now be made between the fully and partially correlated cases. For the fully correlated case, the element weight vector is given by

$$W_r = \Phi_r^{-1} E[X_r r_1(t)] \quad . \tag{125}$$

After substituting Equations (116), (118) and (119) into the above equation, the weight vector is given by

$$W_r = \Phi_r^{-1} \begin{pmatrix} \frac{A_d R}{2\sqrt{2}} \cos(0) \\ \frac{A_d r}{2\sqrt{2}} \cos\left(\frac{\pi}{2}\right) \\ \vdots \\ \frac{A_d R}{2\sqrt{2}} \cos(\kappa_N) \\ \frac{A_d R}{2\sqrt{2}} \cos\left(\kappa_N + \frac{\pi}{2}\right) \end{pmatrix} \tag{126}$$

or

$$W_r = \Phi_r^{-1} \frac{A_d R}{2\sqrt{2}} \begin{pmatrix} 1 \\ 0 \\ \vdots \\ \cos(\kappa_N) \\ \cos\left(\kappa_N + \frac{\pi}{2}\right) \end{pmatrix} \tag{127}$$

For the partially correlated case, the element weight vector is given by

$$W_r = \Phi_r^{-1} E[X_r r_2(t)] \quad . \tag{128}$$

After substituting Equations (117) through (119) in the above equation, the weight vector is given by

$$W_r = \Phi_r^{-1} \frac{A_d R}{4} \begin{pmatrix} 1 \\ 0 \\ \vdots \\ \cos(\kappa_N) \\ \cos\left(\kappa_N + \frac{\pi}{2}\right) \end{pmatrix} \quad . \tag{129}$$

Therefore, the element weights are less by a factor of $\sqrt{2}$ in the partially correlated case as compared to the fully correlated case. The reduction in weights results in a three decibel reduction in signal power at the output of the array for the same reference signal level. There is a similar reduction in noise and interfering power levels,

though, and the array output signal-to-noise ratio will, therefore, be the same for both correlation cases.

It should be noted that in an actual implementation of the LMS algorithm the decreased signal level for the partially correlated case may effect the array performance. Any noise generated in the circuitry itself will degrade the array performance more in the partially correlated case. Furthermore, in the partially correlated case the component of the signal from which the reference signal is derived contains only half the total signal power. This component, therefore, is six decibels lower in the partially correlated case. Thus, the generation of the reference signal may also be affected.

C. The Error Signal

The previous analysis considered the steady state performance of the array, but ignored the weight jitter that might be caused by changes in the error signal. In this section, the error signal is studied for both the partially and fully correlated cases. To simplify the discussion the error signal is determined for a single loop in an adaptive array without noise present. Results can be extended to an N element array with noise at the receiver.

From Equations (127) and (129) it can be seen that for a one loop adaptive array, the steady state weight, w_1, is given by

$$w_1 = R/A_d \tag{130}$$

for the fully correlated case, and

$$w_1 = R/\sqrt{2}A_d \tag{131}$$

for the partially correlated case. The signals involved in both these cases are shown in a one loop implementation of the LMS adaptive array in Figures 6 and 7. As seen in Figures 6 and 7 the error signal is zero for the fully correlated case. However, for the partially correlated case, the error signal is given by

$$e(t) = \frac{R}{2}\sin(\omega_1 t + \theta(t)) - \frac{R}{2}\cos(\omega_1 t + \phi(t)) \quad . \tag{132}$$

Thus, the error signal has the same power as the array output signals. In this case the product of e(t) and s(t) is given by

$$z(t) = e(t)s(t) \tag{133}$$

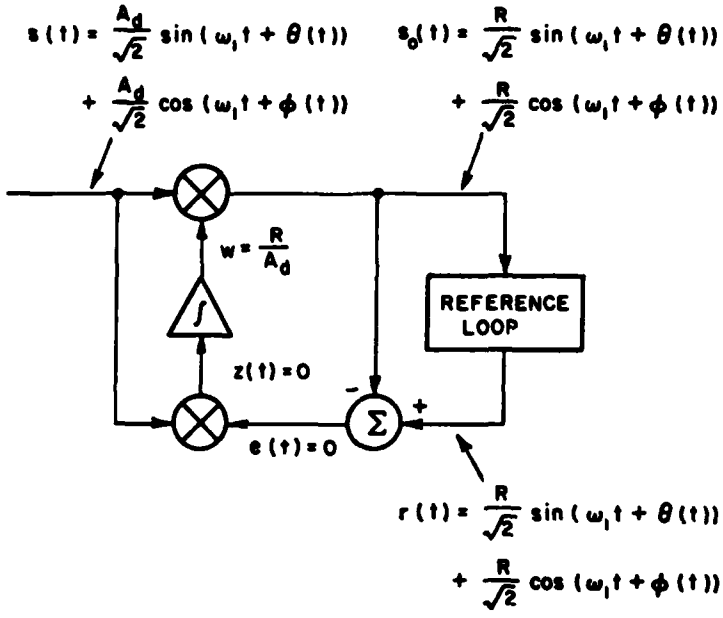


Figure 6. Single loop adaptive array in steady state with a fully correlated reference signal.

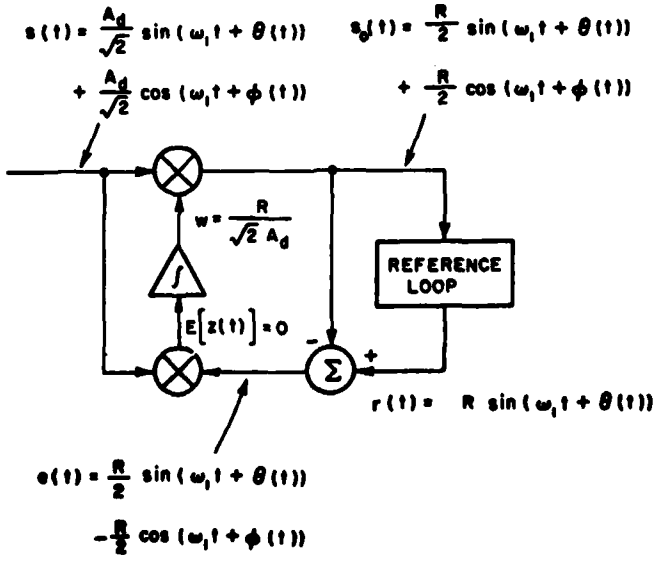


Figure 7. Single loop adaptive array in steady state with a partially correlated reference signal.

or, using Equations (132) and (114),

$$z(t) = \left[\frac{R}{2}\sin(\omega_1 t + \theta(t)) - \frac{R}{2}\cos(\omega_1 t + \phi(t))\right] \cdot \left[\frac{R}{2}\sin(\omega_1 t + \theta(t)) + \frac{R}{2}\cos(\omega_1 t + \phi(t))\right] \quad . \tag{134}$$

Equation (134) can be reduced to give

$$z(t) = \frac{RA_d}{\sqrt{2}}\cos(2\omega_1 t) \quad . \tag{135}$$

As shown above, $z(t)$ consists of a sinusoidal waveform at twice the carrier frequency of the received signals. Because this frequency would typically be outside the response range of the integrator in the loop, the variation in $z(t)$ would not cause any weight jitter. However, in a hardware implementation of the LMS algorithm with non-ideal components, the additional error signal in the partially correlated case could cause some weight jitter.

In this chapter it has been shown that, theoretically, the use of a partially correlated reference signal in an LMS adaptive array will not change the output signal-to-noise ratio or weight jitter as compared with the use of a fully correlated reference signal. In an actual hardware implementation of the array, however, the decreased signal level and increased error signal in the partially correlated case may degrade the array's performance.

CHAPTER V

USE OF FOUR-PHASE SIGNALS IN A JAMMER ENVIRONMENT

A. Introduction

In this chapter a four-phase communication system with an adaptive array at the receiver is developed. As discussed in the Introduction, the four-phase system was developed to overcome some of the shortcomings of a previous biphase system [4]. The four-phase system must still allow for rapid acquisition of the signal at the receiver and suppression of conventional (e.g., noise and cw) jamming as in the biphase system.

The shortcomings of the biphase system are discussed first. The results of Chapters II and III are used to determine which modulation techniques can be employed in overcoming these shortcomings. As in any technique where the reference signal for the array is generated from the array output, signal acquisition is the most difficult part of the problem in designing the system. Several methods for signal acquisition are discussed and one method is chosen for the design of a system. Finally, the design of the entire system is briefly discussed and the operation of the system is described.

B. Modulation Technique

Noise and interference with a greater power than the signal itself may be present at the receiver during acquisition. Thus, in the biphase system, the code timing is acquired at the receiver by the sliding correlation method, whereby, for all possible code timing offsets, the code generated at receiver is correlated with the received signal to determine the correct code timing. With an adaptive array the code generated at the receiver is also used to produce the locally generated signal for the reference loop. Therefore, when the receiver's code timing is correct the adaptive array will increase the signal-to-noise ratio out of the array. This method for acquiring the code timing works quite well but does have a shortcoming. The number of code timing offsets is equal to the code length, and, thus, the code must have a short length, and repeat numerous times during the acquisition period. It is, therefore, not difficult for a jammer to determine the short code and generate its own biphase signal. Since the adaptive array has no way to distinguish the jammer's signal from the desired signal, the array may acquire the jammer's signal and null the desired signal.

A very long length code is, therefore, required for greater communication security; preferably, a code which doesn't repeat over a long period of time.

As shown in Chapter II, four-phase modulation offers a method to combine a short code for rapid acquisition with a long code for communication security. The short code will be used to generate the reference signal only during acquisition. If the long code can be quickly acquired after acquisition of the short code (as discussed in Section C), then the long code can be used to generate the reference signal to provide communication security for the system. Because four-phase modulation is used, it is more difficult for a jammer to determine that a short code is present in the signal and what the short code symbols are. But even if the short code is determined, the receiver can distinguish between a jammer with only the short code and the desired signal because the jammer would not contain a long code. Thus, the system can be made secure against this type of jamming.

Thus, for the four-phase system to overcome the short code shortcoming of the biphase system, two possible reference signals must exist for the four-phase signal. One reference signal is generated knowing only the short code timing and the other by also knowing the long code timing. From Table 1, it can be seen that the four-phase signals in cases 1, 3, 5, and 6 have at least two reference signals (i.e., two different locally generated signals). Furthermore, for the system to remain secure after long code acquisition, the reference signal generated from the long code must be uncorrelated with a biphase signal containing only the short code. Only the signals in cases 5 and 6 can be used to meet this condition. The four-phase signals and locally generated signals that can be used to provide security against a jammer with a biphase signal containing the short code, are, therefore, given by

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \theta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \phi(t)) \qquad (136)$$

with

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) \qquad (137)$$

and

$$s_\ell(t) = \frac{1}{\sqrt{2}} \cos(\omega_2 t + \phi(t) + \psi), \qquad (138)$$

and

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \theta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \phi(t) + \theta(t)) \quad (139)$$

with

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \theta(t) + \psi) \quad (140)$$

and

$$s_\ell(t) = \frac{1}{\sqrt{2}} \sin(\omega_2 t + \phi(t) + \theta(t) + \psi). \quad (141)$$

It should be noted that either differential or coherent encoding of the codes can be used.

The method of data modulation for the four-phase signal will now be examined as a way to overcome the second shortcoming of the biphase system, the vulnerability to a repeat jammer with remodulation. With a biphase signal data is added to the coded signal by additional 180 degree phase shifts in the signal. Therefore, the signal from a jammer which repeats the desired signal and adds 180 degree phase shifts cannot be distinguished from the desired signal. As before, the array may acquire the jammer's signal and null the desired signal. To overcome this problem, the four-phase data modulation technique must not produce additional 180 degree phase transitions. The modulation possiblities from Table 2 are s(t) as given in Equation (136) with data added to either the a_i or b_i code symbol stream and s(t) as given in Equation (139) with data added to the b_i code symbol stream. For these four-phase signals, biphase remodulation produces changes in the data and data on the previously unchanged code symbol stream. Because the component of the signal which contained only the code symbols will now contain data (i.e., it is now a spread spectrum signal), the remodulated signal can easily be distinguished from the desired signal.

With data added to only one code, the phase shift due to a "1" data bit is either plus or minus 90 degrees. The actual phase shift depends on both codes. If a phase shift of plus or minus ninety degrees is added to the four-phase signal, it is as likely to produce an apparent data bit on the code stream without data as it is to change the data. Therefore, a repeat jammer with remodulation involving random phase shifts can not effectively jam the system. The repeat jammer is required to have a detailed knowledge of the signal structure and the codes involved.

Therefore, if the four-phase signal is given by Equation (136) with data added to the a_j or b_j code symbol stream, or Equation (139) with data added to the b_j code symbol streams, a system can be designed to overcome the shortcomings of the biphase system. The design of the system is described in Section D. The long code acquisition will be determined first, though, in Section C.

C. Long Code Acquisition

As stated previously, signal acquisition is the most difficult aspect of the four-phase communication system. Acquisition of the signal by the receiver requires the acquisition of both the short and long code timing. The short code timing can be acquired by the sliding correlation method as in the biphase system. In this section the acquisition of the long code timing is discussed.

It is desirable to have the long code acquisition time less than the short code acquisition time, so that the total acquisition time for the four-phase system is not significantly greater than that for the biphase system. Rapid acquisition of the long code can be obtained after the short code acquisition because of two factors. First, after acquisition of the short code, any jamming signals will be nulled by the array and the output signal-to-noise ratio will be greater than that at the input. Also, the symbol transition timing for the long code is already known since the short and long code symbols have the same transition timing. The possible methods for determining long code symbol timing will now be discussed and one method will be chosen for use in a system.

One method for determining the long code timing involves a long code which contains several shorter codes as described in [10] and[11]. The sliding correlation method could be used to determine the code timing of these shorter codes and, thus, the entire long code, very quickly. However, the system would now be vulnerable to jamming by signals using shorter codes and, therefore, some of the security of the system would be lost.

Long codes can also be generated from an n-stage feedback shift register. With the proper feedback, codes of up to length 2^n-1 (i.e., pseudorandom) can be generated from the n-stage shift register. Thus, very long codes can be generated from relatively short length shift registers. To determine the code timing for a code generated from an n-stage shift register, it is only necessary to determine the n symbols in the shift register at a given time.

One method that the receiver can use to determine the n symbols involves transmitting the n symbols as data on the short code during acquisition. The n symbols could easily be detected at the receiver and loaded into the shift register. Since the probability of a data error at the receiver is usually very small, these n symbols would

have a high probability of being detected and loaded into the shift register correctly. The disadvantage of this method, however, is that the transmitter must first send the n symbols and then the data. Since the transmitter does not know when the signal has been acquired, it may stop sending the n symbols before they have been detected by the receiver. In this case the entire transmission would be lost by the receiver.

Another method that the receiver can use to determine the n symbols involves the detection of the code symbols on the signal. The n consecutively detected code symbols will be the current contents of the shift register if the only feedback in the shift register is to the first stage. This feedback requirement is not very restrictive because most codes are generated with feedback only to the first stage. This acquisition method is called the Rapid Acquisition by Sequential Estimation (RASE) method and is described in [12]. A block diagram is shown in Figure 8 of the circuitry needed for implementation of this technique. For this technique, the code symbols on the received signal are demodulated and loaded into the feedback shift register. This shift register has the same length and feedback connections as that used to generate the code at the transmitter. When the shift register is fully loaded the feedback is connected by the load and track logic. If the code bits have been detected correctly, the output of the shift register is synchronized with the code on the received signal. To verify synchronization, the correlation between the received signal and the generated code is determined by the load and track logic. If the correlation value does not exceed a given threshold, the above process is repeated (i.e., the shift register is reloaded) until synchronization is obtained. Using this method synchronization for a 2^n-1 bit pseudo-noise code can be obtained after detection of as few as n code symbols. Even with a large amount of noise present with the received signal, although many loadings of the shift register may be required before the signal is acquired, the average time required for acquisition is still much less than for the sliding correlation method.

For use with the four-phase signal the RASE method must be slightly modified. First, for rapid acquisition, the code symbols must be differentially encoded so that they can be differentially detected at the receiver. Thus, a differential detector will be used to determine the phase shifts in the received signals. Also, since the phase shifts in the signal correspond to the short code, data, and the long code symbols, detection logic must be used to determine the long code symbols from the phase shifts.

A block diagram of the RASE method is shown in Figure 9 for the acquisition of the long code timing. As shown in this figure the array output containing the desired four-phase signal with noise is differentially detected using the symbol transition timing from

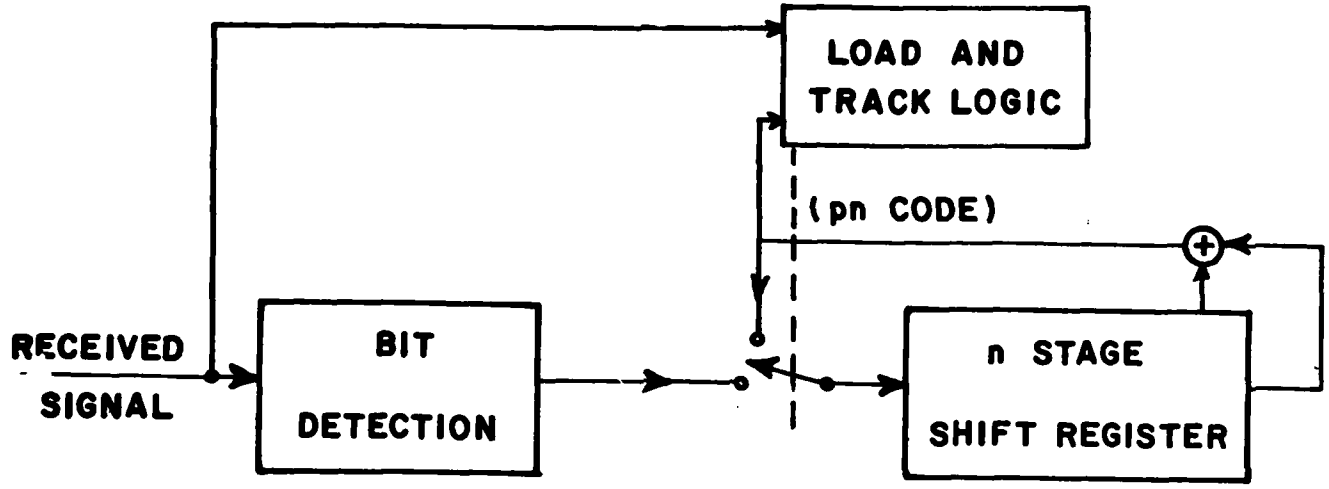


Figure 8.--Rapid Acquisition by Sequential Estimation block diagram.

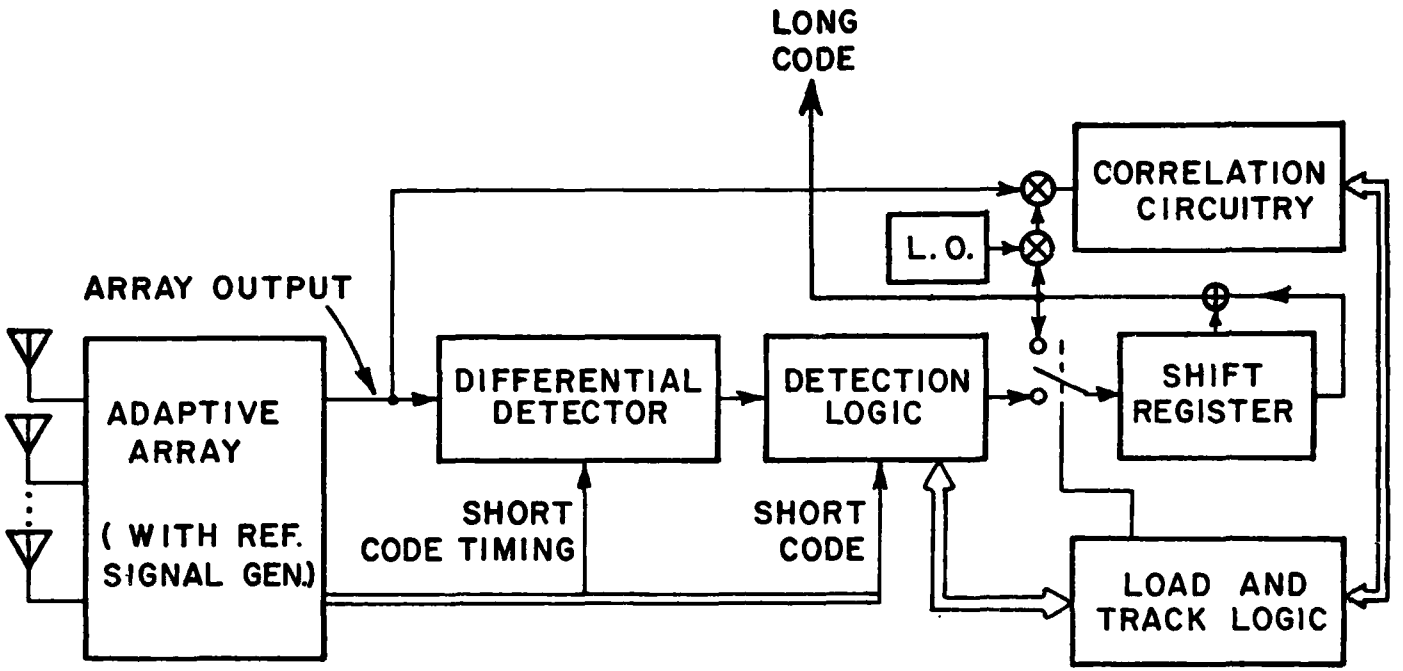


Figure 9.--RASE with an adaptive array for four-phase modulation.

the tracking of the short code. Information about the phase shifts present at each bit is then passed to the detection logic. Since the short code bits are known, the detection logic can determine the long code bits and in some cases also determine if errors have been made by the differential detector. If no errors are detected, the long code bits are loaded into the shift register. The shift register is then connected in the feedback mode and the output of the shift register correlated with the array output to verify code timing. If the correlation of the two signals after a given time exceeds a threshold value, the output of the shift register is used to generate the reference signal for the array. Otherwise, the shift register is reloaded and the process repeated until code synchronization is obtained.

If the long code acquisition time with the RASE method is too long, there are methods to decrease the acquisition time, although increased circuit complexity is required. The Recursive-aided RASE method can be used as described in [13]. Also, if the initial loadings of the short and long code shift registers in the transmitter are known at the receiver, then the long code timing can be seen to be just the short code timing plus some multiple of the short code length. It is, therefore only necessary to determine this multiple to acquire the long code timing. Thus, the long code acquisition time may be reduced by a factor of the short code length, although very complex circuitry may be required with this method. The above two techniques were not used in the four-phase system because the long code acquisition time as determined in Chapter VIII was not too long.

A four-phase modulation technique will now be chosen from those given at the end of Section B. As stated above, the long code must be differentially encoded so that the code symbols may be differentially detected. Also, the long code acquisition time using the RASE technique can be shown to be much less if data is not added to the long code. Thus, if the a_j code symbol stream is arbitrarily chosen as the short code symbol stream and b_j as the long code symbol stream, then the only four-phase modulation technique that can be used is given by

$$s(t) = \frac{1}{\sqrt{2}} \sin(\omega_1 t + \zeta(t)) + \frac{1}{\sqrt{2}} \cos(\omega_1 t + \phi(t)) \qquad (142)$$

where

$$\zeta(t) = \theta(t) + \gamma(t) \qquad (143)$$

where

$$\theta(t) = \theta_m = \theta_{m-1} + \pi a_m \tag{144}$$

for $(m-1)\,\Delta \leq t < m\Delta$,

and

$$\gamma(t) = \gamma_i = \gamma_{i-1} + \pi d_i \tag{145}$$

for $(i-1)\,T_b \leq t < iT_b$

and

$$\phi(t) = \phi_m = \phi_{m-1} + \pi b_m \tag{146}$$

for $(m-1)\,\Delta \leq t < m\Delta$.

The a_m, b_m, and d_i are the m-th short code symbol, m-th long code symbol, and the i-th data symbol, respectively.

D. System Description

The entire four-phase communication system as developed in the preceding sections will now be described. First to be discussed is the acquisition procedure. A block diagram of the entire system is then described and the areas of study in the next chapters are mentioned.

In summary, the signal acquisition procedure is as follows:

1) The short code timing is acquired using the sliding correlation method.

2) The short code is used to generate a reference signal in the array to null jammers and increase signal-to-noise ratio.

3) The long code timing is quickly acquired using the RASE method.

4) The long code is immediately used to generate the reference signal to provide system security.

To provide protection against smart jammers (i.e., jammers using only the short code or repeat jammers with remodulation), if the long code timing is not acquired in a short period of time (step 3), the short code timing is changed and steps 1 through 4 are repeated.

A block diagram of the entire four-phase communication system is shown in Figure 10. The four-phase signal is transmitted and received by the adaptive array. From the array output the short code timing is determined and then tracked by the delay lock loop as in the biphase system. Long code timing is acquired by the long code acquisition circuitry. The control logic controls the acquisition procedure steps, including which codes are used in the reference loop.

There are several areas of study for this system which are covered in greater detail in the next several chapters. These areas include the short code acquisition (Chapter VI), the tracking of the short code by the delay lock loop (Chapter VII), and the long code acquisition (Chapter VIII). Also, the structure of the long code required for a secure system (Chapter IX) and the effect of smart jamming (Chapter X) are discussed.

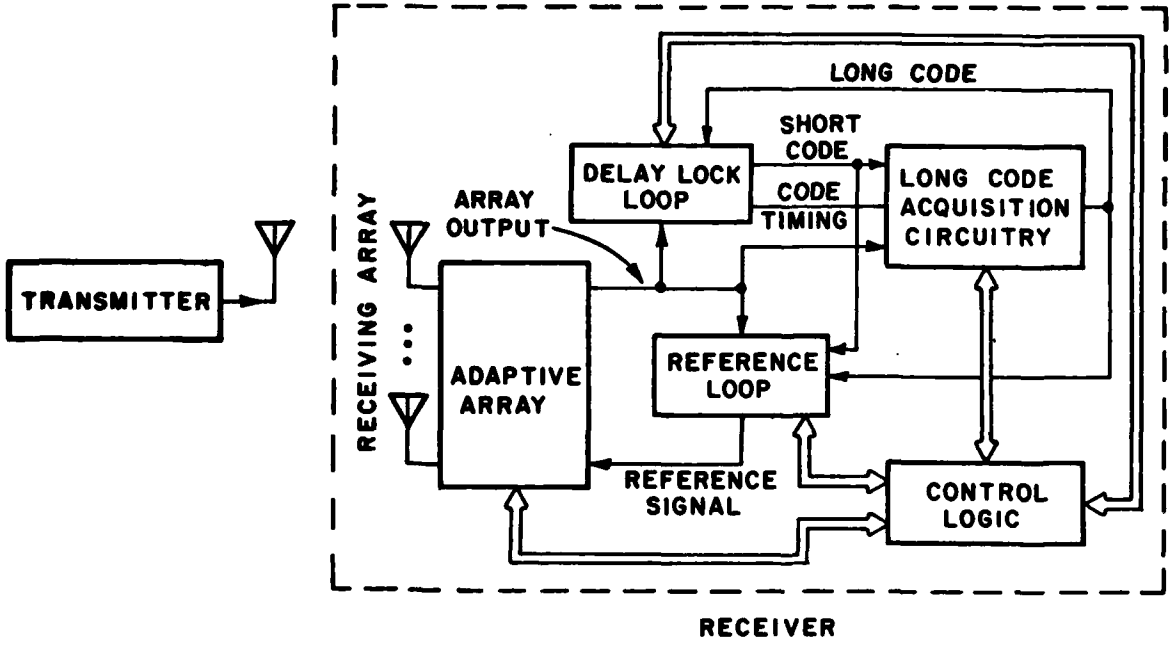


Figure 10.--Block diagram of the four-phase communication system.

CHAPTER VI

SHORT CODE ACQUISITION

A. Introduction

The first step in the acquisition of the four-phase signal by the receiver is the acquisition of the short code timing. In this chapter short code acquisition is considered for the sliding correlation method using a delay lock loop. Although the acquisition method was also used in the biphase system, the acquisition method was not analyzed in detail. Results presented in this chapter are applicable to both the four-phase and biphase systems.

The purpose of this chapter is to study the acquistion process and determine the equations involved so that the results can be used in the design of the four-phase system. In Section B a general discussion of the sliding correlation method is presented. The maximum code length for acquisition in a given time in determined and related parameter discussed. In Section C the acquisition without noise is studied. The time response of the delay lock loop is determined during the acquisition period. In Section D the acquisition with noise is considered. Equations are derived which determine the probability of acquisition with noise. Filter bandwidths and threshold levels are determined for optimum performance of the sliding correlation method for given operating conditions.

B. Maximum Code Length and Sweep Rate

The first step in the acquisition of the signal by the receiver is the determination of the proper timing of the short code. Proper code timing is then maintained by a delay lock loop. The discussion in this section concerns the performance and the parameters involved in the acquisition of the short code by the sliding correlation method.

Noise and interference with a greater power than the signal itself may be present at the receiver during acquisition. Because of this, the best method for determining the short code timing must involve a checking, for all possible code timing offsets, of the correlation of the received signal with a locally (or receiver) generated signal containing the short code. The timing offset which produces the greatest correlation is then used by the delay lock loop to track the short code.

To reduce the magnitude of false correlation peaks, the correlation should be made over an entire code period (the time it takes before the code repeats itself), Thus, the code rate, acquisition time, τ_{acq}, and code length (number of bits in the code before it repeats), N, may be related by the equation

$$\text{Code rate} = N \cdot N \cdot \frac{1}{\tau_{acq}} \quad . \tag{147}$$

The above equation assumes that once an estimate (within 1 chip on code bit interval) of the timing offset has been made, the time required to reduce the timing accuracy to within the steady state error of the delay lock loop (final transient time) is negligible. Although this is not always the case, as will be seen later, this is a useful approximation at this point.

For a given code rate and acquisition time, the maximum code length is, from Equation (147), given by

$$N \leq \sqrt{\tau_{acq} \cdot \text{code rate}} \quad . \tag{148}$$

The code length can be longer than this value only if correlation is made over less than an entire code period. The code structure would have to be examined in much greater detail in this case.

Because the short pseudonoise code is usually generated from a linear feedback shift register, the code length used in a system may be given by

$$N' = 2^n - 1 \quad , \tag{149}$$

where n is the number of stages in the shift register.

Thus, N' will, in general be less than N.

The sequential checking of all timing offsets may be done either in a digital or analog form. In the digital method [14, pp. 588-592] the locally generated signal is at the same code rate as the received signal. The output of the correlation circuitry is sampled at a certain time, compared to a threshold value, and, if below this value, the timing offset of the locally generated code is incremented by a fixed amount (usually 0.5 or 1 chip). The process is repeated until the correct timing offset is found.

In the analog or sliding correlation method, the receiver generated signal is at a slightly different code rate from the received signal. The output of the correlation circuitry is continuously compared to a threshold value. When the threshold is exceeded the code rate of the locally generated signal is changed to that of the received signal. Although the acquisition probabilities of both methods are very similar, the analog system can switch to delay lock loop tracking closer to the correct timing offset. This reduces the final transient time of the delay lock loop in achieving steady state performance. Thus, the analog method will be considered in this section.

For the analog system the code rate difference between the received signal and the locally generated signal (sweep rate) is given by

$$\text{Sweep rate} = \frac{\text{Code rate}}{N} \quad . \tag{150}$$

As stated before the acutal code length employed in a system, N', is usually less than N. The sweep rate used may then be given by

$$\text{Sweep rate} = \frac{\text{Code rate}}{N'} \quad , \tag{151}$$

which is greater than or equal to the sweep rate of Equation (150). Thus, the acquisition time may be slightly less than the τ_{acq} in Equation (148), to keep the total short code acquisition time below τ_{acq} even when considering the effect of the final transient time.

Thus, in this section the maximum code length for acquisition in a given time was determined to be given by Equation (148) and the sweep rate for the chosen code length was determined to be given by Equation (151).

C. Acquisition Without Noise

In this section the acquisition is studied of the short code by the sliding correlation method using a delay lock loop. A block diagram of the delay lock loop using envelope correlation is shown in Figure 11. As seen in this figure, the received signal is split into two channels. In one channel the signal is mixed with the code advanced by half a chip (code symbol interval) and in the other channel with the code delayed by a half a chip. When the code timing at the receiver is the same as the received signal's code timing, the received signal is despread by the mixing process. The output of the mixers is then passed through a bandpass filter and an envelope detector is used to determine the output signal level. The outputs of the two envelope detectors are then subtracted and passed through the loop filter, F(p).

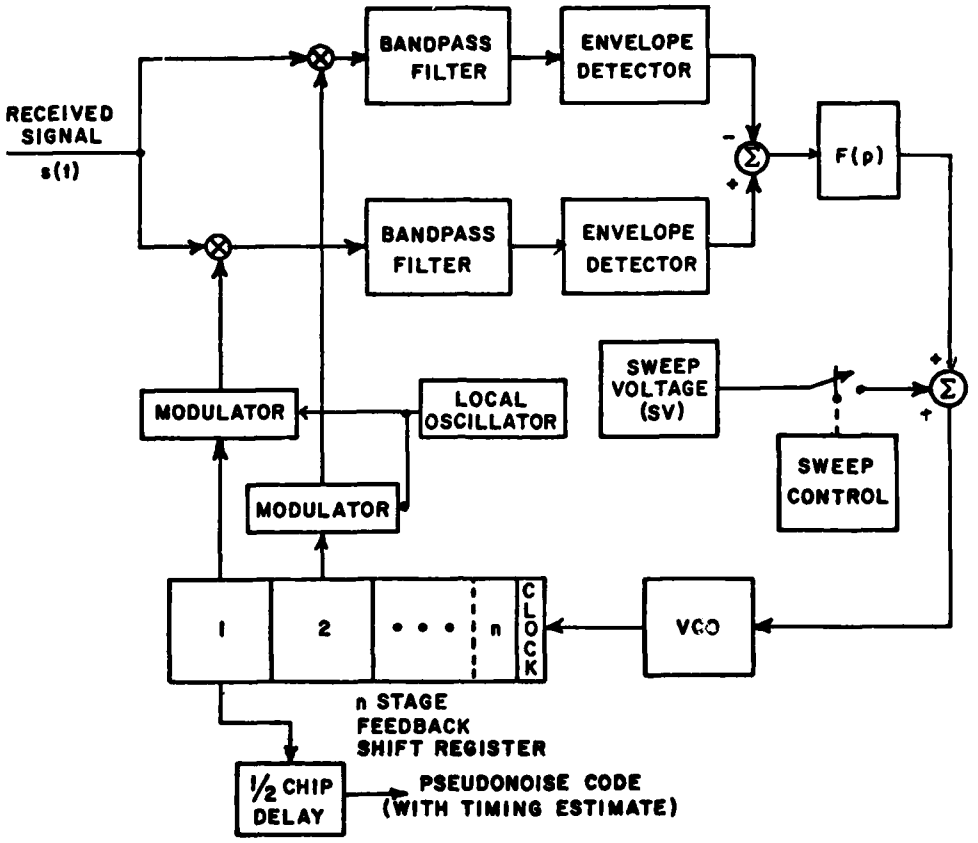


Figure 11. The delay lock loop with envelope correlation.

A sweep voltage, SV, is added to the output of the loop filter during acquisition. When the sweep control circuitry determines that the timing error is within the lock range of the loop, the sweep voltage is turned off. The voltage out of the summer is used to control the frequency of voltage controlled oscillator (VCO) which is used to clock the feedback shift register.

The sliding correlation method studied in this chapter is similar to that described in [14] for the biphase system. The delay lock loop described in [14] is shown in Figure 12. The major difference in the delay lock loops of Figures 11 and 12 is the lack of a squarer and square rooter to remove data on the signal in Figure 11. Because the loop bandwidth of the delay lock loop will, in general, be much less than the data bandwidth, the use of the squarer and the square rooter was found to be unnecessary. Furthermore, the removal of these non-linear elements makes possible an exact analysis of the delay lock loop.

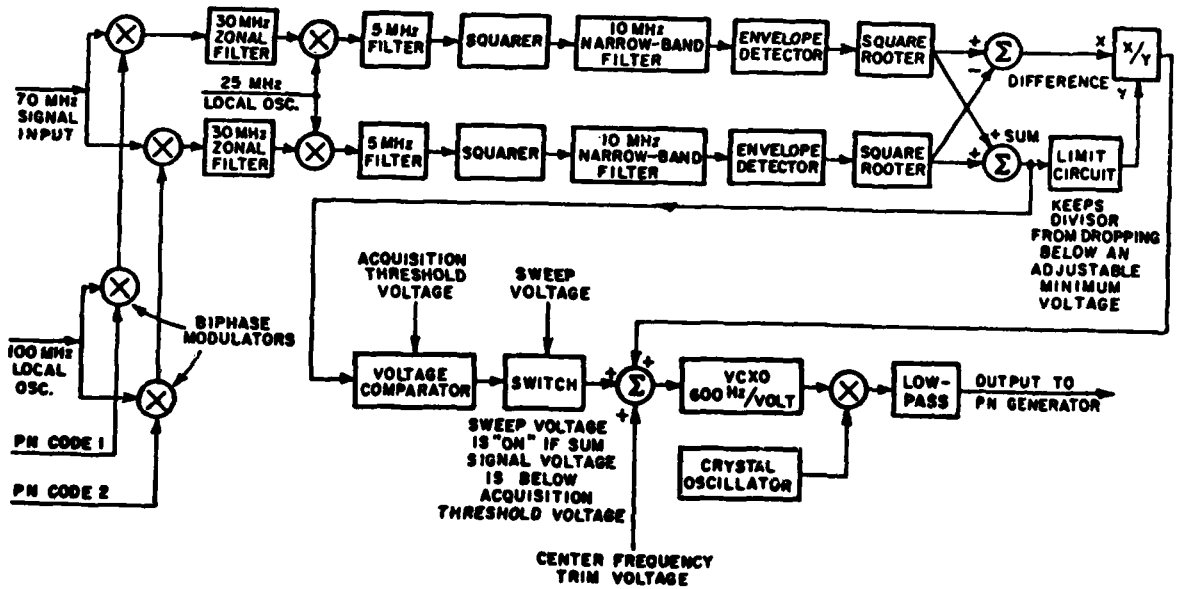


Figure 12. Block diagram of the delay lock loop described in [14].

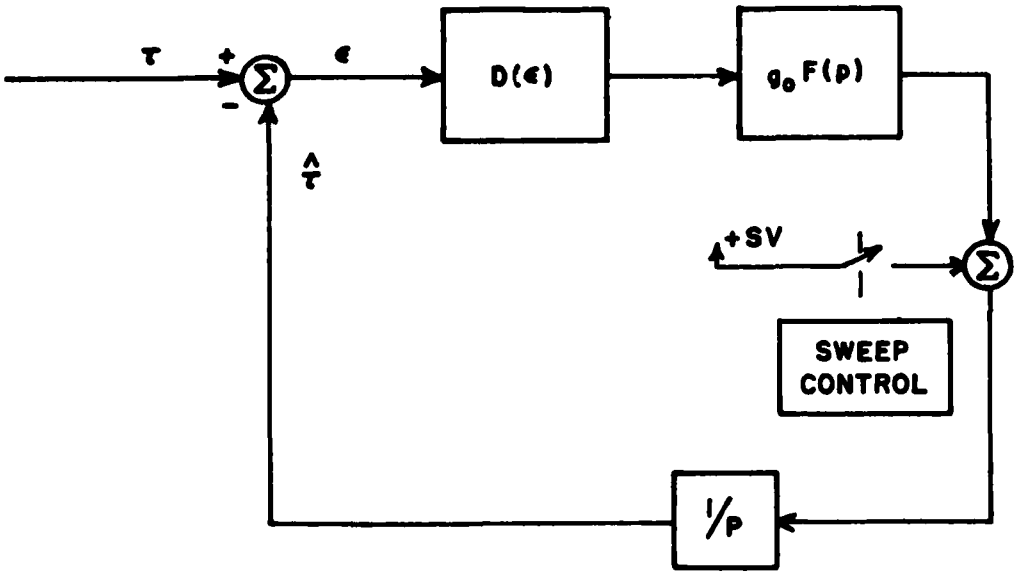
The analysis of the code timing acquisition has been done previously for the delay lock loop with square law detection (see, for example, [6]). However, in this chapter the delay lock loop is considered with linear envelope detection and with the use of the sum channel to determine when to stop the slewing of the code during acquisition. Linear envelope detection is used because it is better suited for use with the sum channel as discussed later.

To analyze the delay lock loop, this loop may be modelled as shown in Figure 13 [6, p. 577]. The equation describing the loop is given by

$$\hat{\tau} = [D(\epsilon)g_0F(p) + SV]\frac{1}{p} \tag{152}$$

where

$$\hat{\tau} = \tau - \epsilon \quad . \tag{153}$$



$\hat{\tau}$ - code timing estimate
τ - received signal timing
ϵ - timing error
$D(\epsilon)$ - loop discrimination characteristic
p - d/dt
g_0 - loop gain

Figure 13. Mathematical model of the delay lock loop of Figure 11.

After rearranging terms, the equation is given by

$$SV + D(\varepsilon)g_o F(p) = p(\tau - \varepsilon) \quad . \tag{154}$$

To normalize the parameters with respect to time, let

$$x \triangleq \frac{\varepsilon}{\Delta} \quad , \tag{155}$$

$$y \triangleq \frac{\tau}{\Delta} \quad , \tag{156}$$

$$s \triangleq \frac{p}{\rho_o} \quad , \tag{157}$$

and

$$g \triangleq \frac{g_o}{\rho_o} \quad , \tag{158}$$

where

Δ is the chip interval, and

ρ_o is the loop-filter frequency constant.

If the discriminator characteristic, D(x), is normalized, such that

$$D'(0) = 1.0 \quad , \tag{159}$$

where $D'(x) \triangleq dD(x)/dx$ then g is the normalized gain. Equation (154) may be rewritten as

$$SV + D(x)gF(s) = s(y - x) \quad . \tag{160}$$

For the loop filter whose transfer function is given by

$$F(s) = \frac{1 + \sqrt{2}\, s}{1 + gs} \quad , \tag{161a}$$

where

$$g >>> 1 \quad , \tag{161b}$$

the closed loop transfer functions of the loop "has been shown to be optimum for ramp inputs of delay in the presence of white noise in that it minimizes the total squared transient error plus the mean-squared error caused by interfering noise" [6, p. 545]. Hence, this filter will be analyzed in the loop.

Equation (160) may then be rewritten as

$$SV + D(x)\left[\frac{1 + \sqrt{2}\, s}{\frac{1}{g} + s}\right] = s(y - x) \quad , \tag{162}$$

and

$$\ddot{x} = -\left[D(x) + \sqrt{2}\, D'(x)\dot{x} + \dot{x}/g - \dot{y}/g - \ddot{y} + \frac{SV}{g} + S\dot{V}\right] \tag{163}$$

where

$$\dot{x} = \frac{dx}{dt} \quad . \tag{164}$$

If we assume the received signal's code timing is not changing with time, i.e.,

$$\ddot{y} = \dot{y} = 0 \quad , \tag{165}$$

then Equation (163) may be put in the form given by

$$\frac{d\dot{x}}{dx} = -\frac{[D(x) + \sqrt{2}\, D'(x)\dot{x} + \dot{x}/g + SV/g + S\dot{V}]}{\dot{x}} \tag{166}$$

In the delay lock loop of Figure 11, the envelope detector may use either linear or square law detection. For large signal-to-noise ratios, both types of detectors have about the same output signal-to-noise ratios. Because the signal-to-noise ratio in the envelope detector is basically the same as that for data detection, the signal-to-noise ratio will usually be large. Also, the discriminate characteristics of the loop, D(x), will be the same for both types of detectors when the timing error is within one-half of a chip. However, the linear envelope detector gives a more suitable output for use by the

quisition (sweep control) circuitry, as shown later. Thus, the delay
ck loop with linear envelope detection will be analyzed.

With linear envelope detection, the expression for the discrimi-
tion characteristic is given by

$$D(x) = \begin{cases} -0.5\ (1.5 + x) & -1.5 \leq x \leq -0.5 \\ x & |x| < 0.5 \\ 0.5\ (1.5 - x) & 0.5 \leq x \leq 1.5 \\ 0 & \text{elsewhere} \end{cases} \qquad (167)$$

i

$$D'(x) = \begin{cases} -0.5 & 0.5 \leq |x| \leq 1.5 \\ 1 & |x| < 0.5 \\ 0 & \text{elsewhere} \end{cases} \qquad (168)$$

From Equation (166), using Equations (167) and (168), a phase
ane plot of the acquisition trajectory of the loop may be determined.
wever, in Equation (166), when the sweep voltage is turned off, $S\dot{V}$
comes infinite as does $d\dot{x}/dx$. This discontinuity may be taken into
count by examining Figure 13, which shows that when the sweep voltage
removed the value of $\dot{x}$ ($\dot{\varepsilon}$), changes immediately by $S\dot{V}$. Because of
s fact, SV need not be considered in Equation (166).

Computer analysis to determine the phase plane plot can be made
using the approximations given by

$$\dot{x}_{n+1} = \dot{x}_n + \gamma_n\, \delta x_n \qquad (169)$$

$$x_{n+1} = x_n + \delta x_n \qquad (170)$$

re

$$\gamma_n = \left.\frac{d\dot{x}}{dx}\right|_{\substack{x=x_n \\ \dot{x}=\dot{x}_n}} \qquad (171)$$

and δx_n, chosen to minimize the number of steps while maintaining accuracy, is given by (as suggested in [6, p. 579])

$$\delta x_n = \frac{0.02}{1+|\gamma_n|} \operatorname{sgn}(\dot{x}_n) \quad . \tag{172}$$

To obtain a time response for the system, computer analysis can be made using the approximation

$$t_{n+1} = t_n + \frac{\delta x_n}{1+|\gamma_n|} \frac{1}{\dot{x}_n} \quad . \tag{173}$$

Using the above method, consider first the case where the sweep control circuitry is not employed, i.e., the sweep voltage is always applied. Figures 14 and 15 show the acquisition trajectories and time response of the loop with infinite loop gain (meeting the requirement of Equation (161)). When the loop gain is reduced to a practical value of 10, Figures 16 and 17 demonstrate that the response of the loop is basically unchanged.* Thus, a loop gain of 10 will be assumed in this analysis.

Figure 16 shows that the maximum normalized sweep speed, $\dot{x}_n$, for which the loop still locks is approximately given by

$$\dot{x}_s = 1 \quad , \tag{174}$$

which corresponds to a sweep speed of ρ_0 chips per second. For $\dot{x}_s$ equal to one, the time required to reach steady state is, from Figure 17, about $8/\rho_0$ seconds, i.e., the final transient time is the same as the time needed to search 8 timing offsets.

Now, in general, ρ_0 would be chosen to be fairly small to reduce the jitter in tracking the pseudonoise code by the delay lock loop (see Chapter VII). The magnitude of the jitter is especially important in the short-long code acquisition scheme under consideration because increased jitter causes increased long code acquisition time (see Chapter VIII). Also with noise present in the system the sweep rate may be set considerably less than ρ_0 to ensure acquisition.

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* A steady state error in the loop exists in this case which may be calculated and eliminated in the timing estimate used by the receiver.

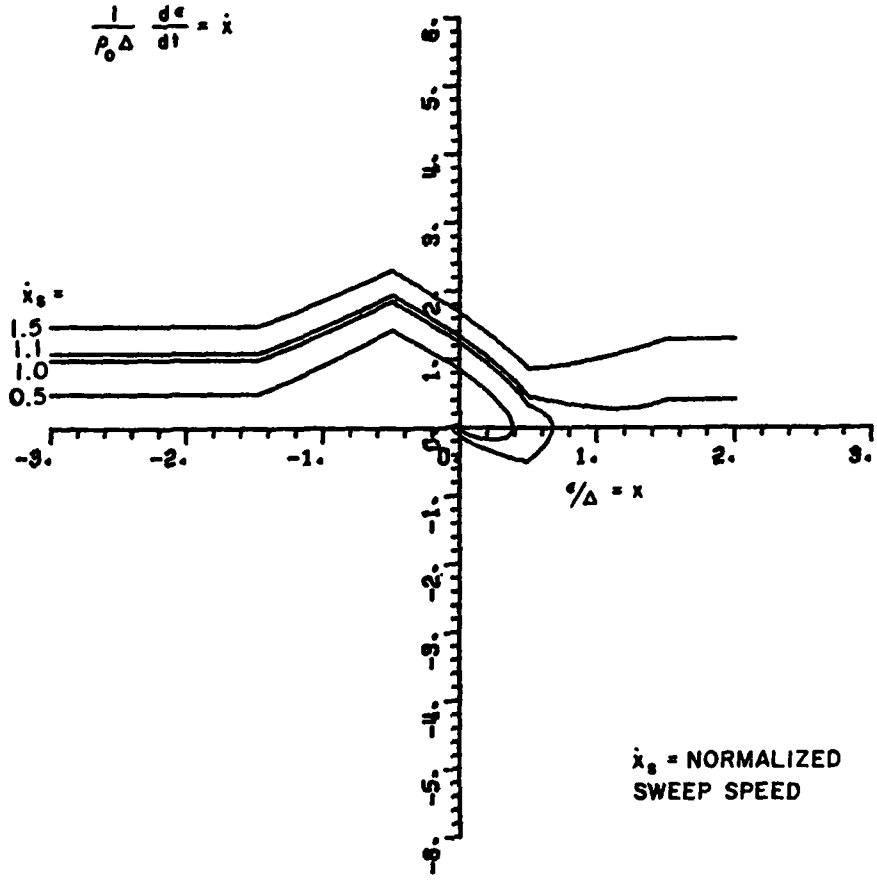

Figure 14. Acquisition trajectory of the delay lock loop with linear envelope detection (infinite loop gain), for various sweep speeds.

Thus, to acquire the short code in the required time without a large steady state code jitter, a much higher sweep speed than ρ_0 is usually required. Circuitry is needed which switches off the sweep voltage based on the decision that the timing error is such that the loop will lock without the sweep voltage. For the loop to lock the acquisition trajectory must be in a given region of the phase plane after the sweep voltage is removed. This region is shown in Figure 18. Figures 19 through 22 show the effect of switching off the sweep voltage at various times, i.e., timing offsets. In these cases the sweep speed is set equal to $4\rho_0$. However, similar results are obtained for much higher sweep speeds. Thus, the location of the acquisition trajectory immediately after the sweep voltage is removed can be plotted (Figure 23), and the final transient time versus switching time can also be determined (Figure 24), for all positive sweep speeds.

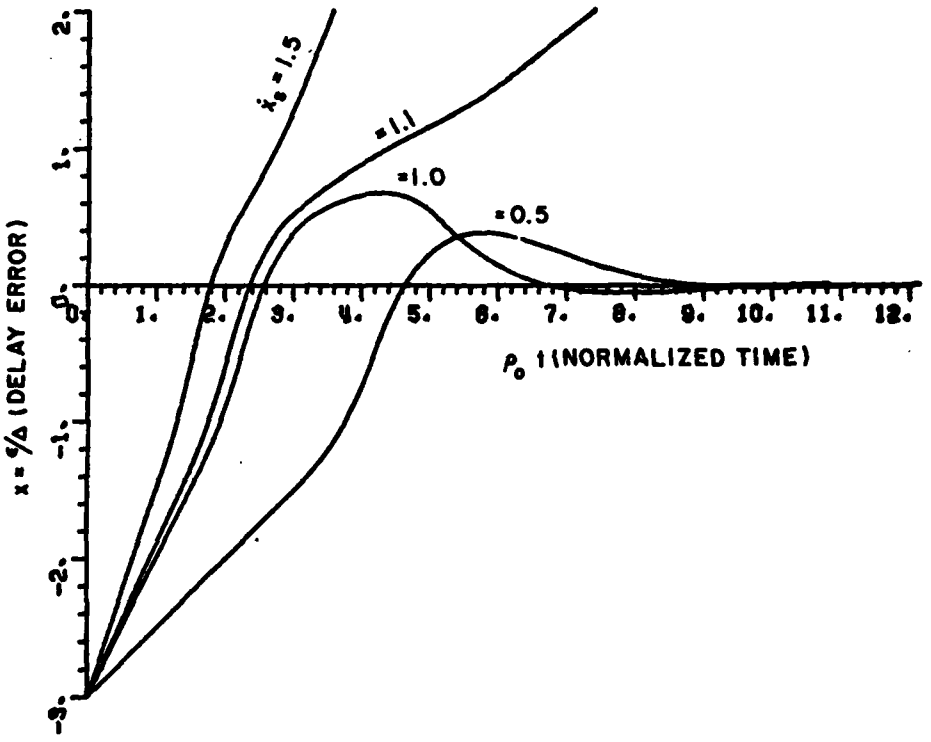

Figure 15. Time response of the delay lock loop with linear envelope detection (infinite loop gain), for various sweep speeds.

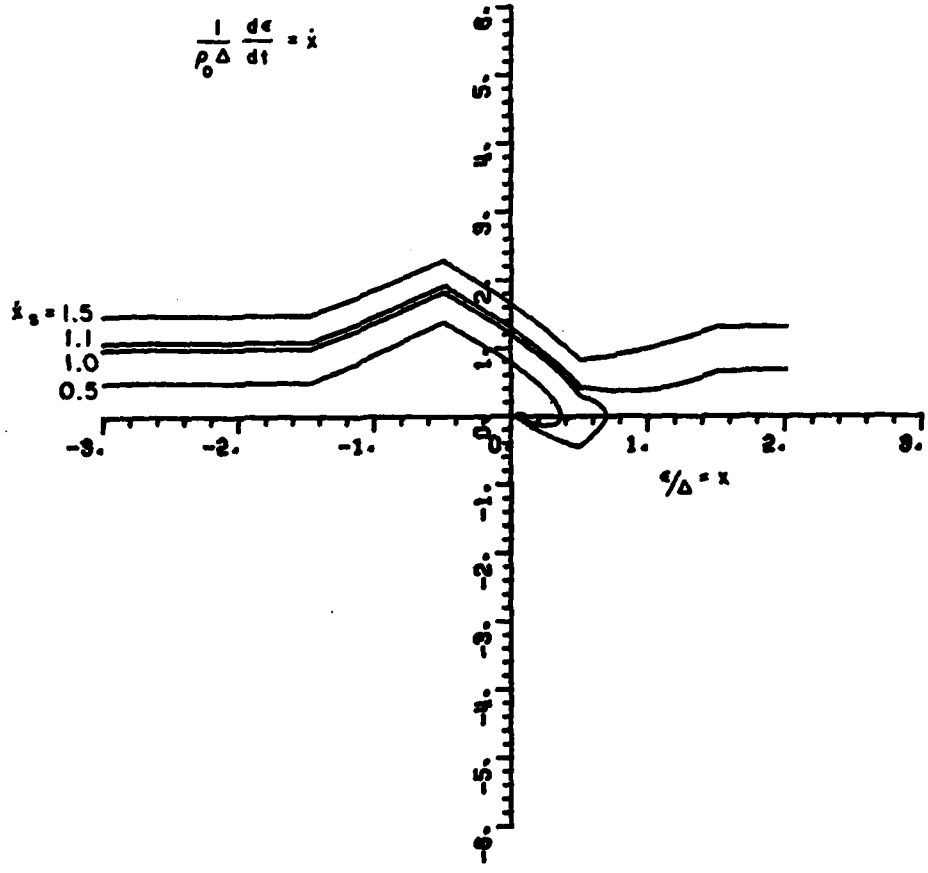

Figure 16. Acquisition trajectory of the delay lock loop with linear envelope detection (normalized loop gain of 10), for various sweep speeds.

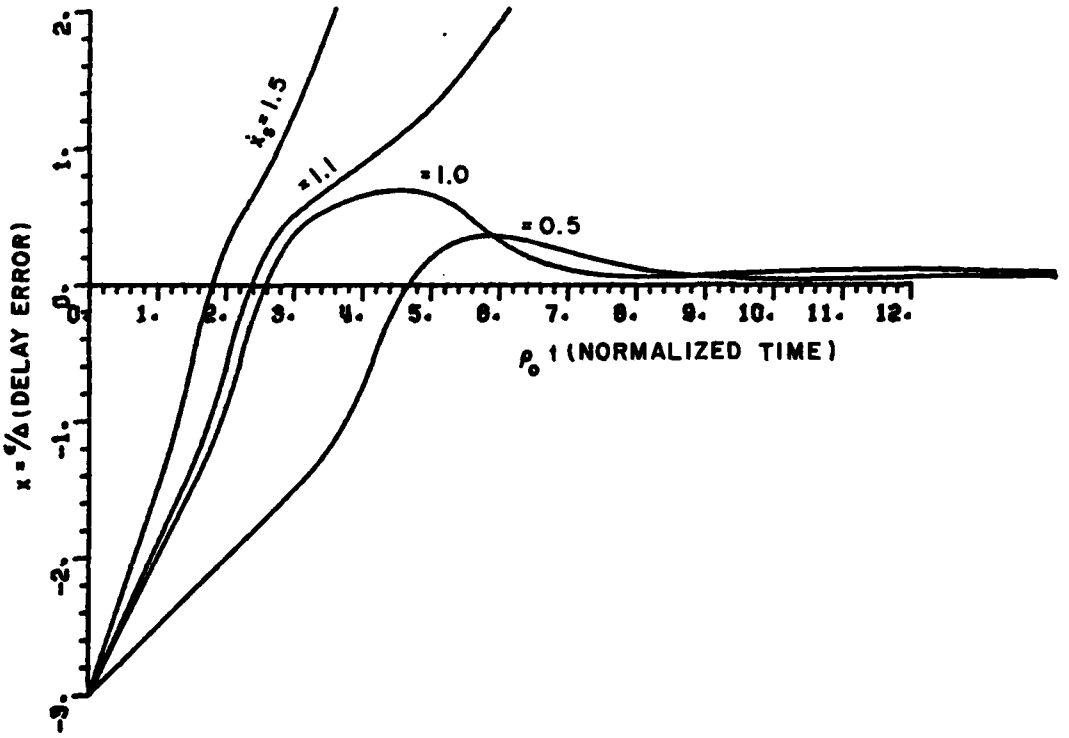

Figure 17. Time response of the delay lock loop with linear envelope detection (normalized loop gain of 10), for various sweep speeds.

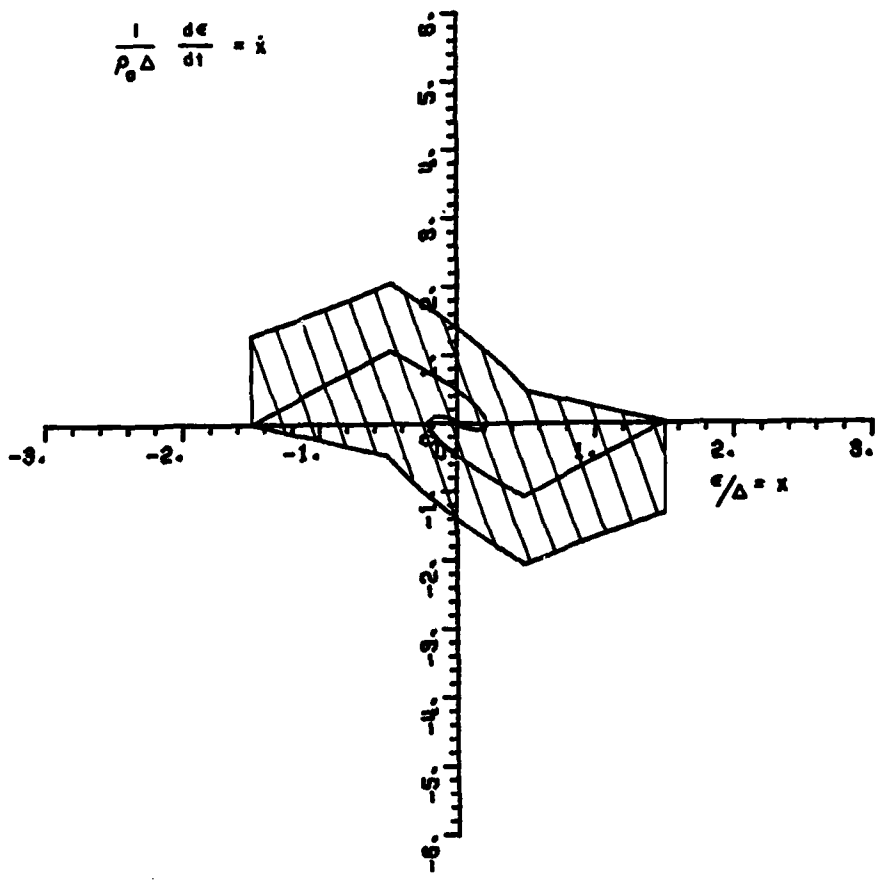

Figure 18. Capture region for delay lock loop with linear envelope detection (normalized loop gain of 10), with sweep voltage off.

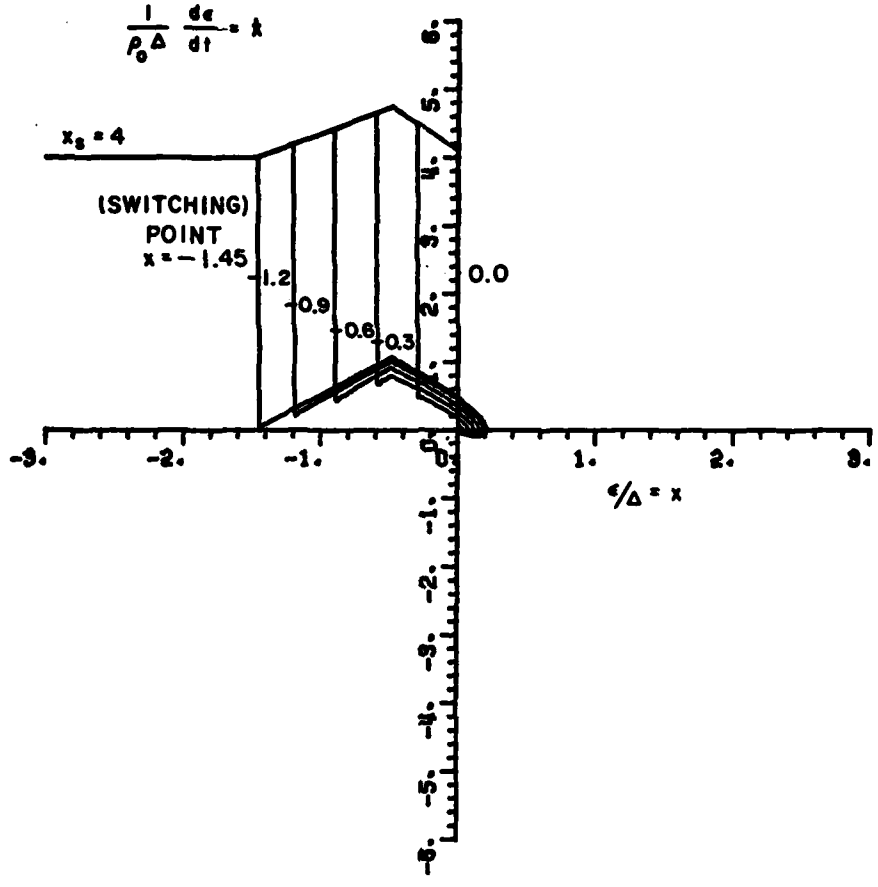

Figure 19. Acquisition trajectory of the delay lock loop with linear envelope detection (normalized loop gain of 10), for various sweep voltage switching times.

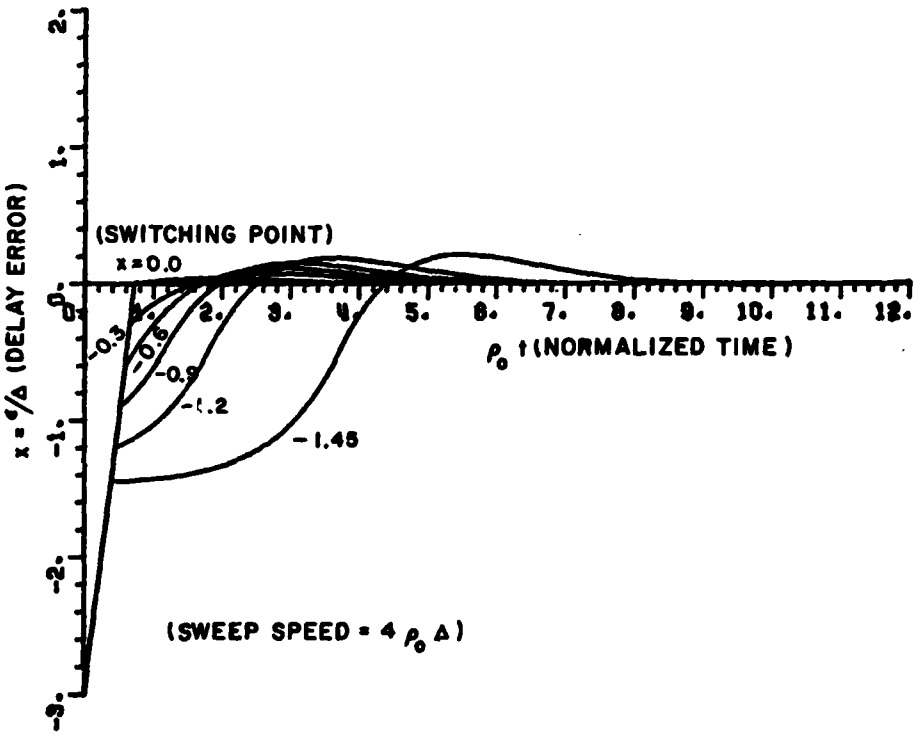

Figure 20. Time response of the delay lock loop with linear envelope detection (normalized loop gain of 10), for various sweep voltage switching times.

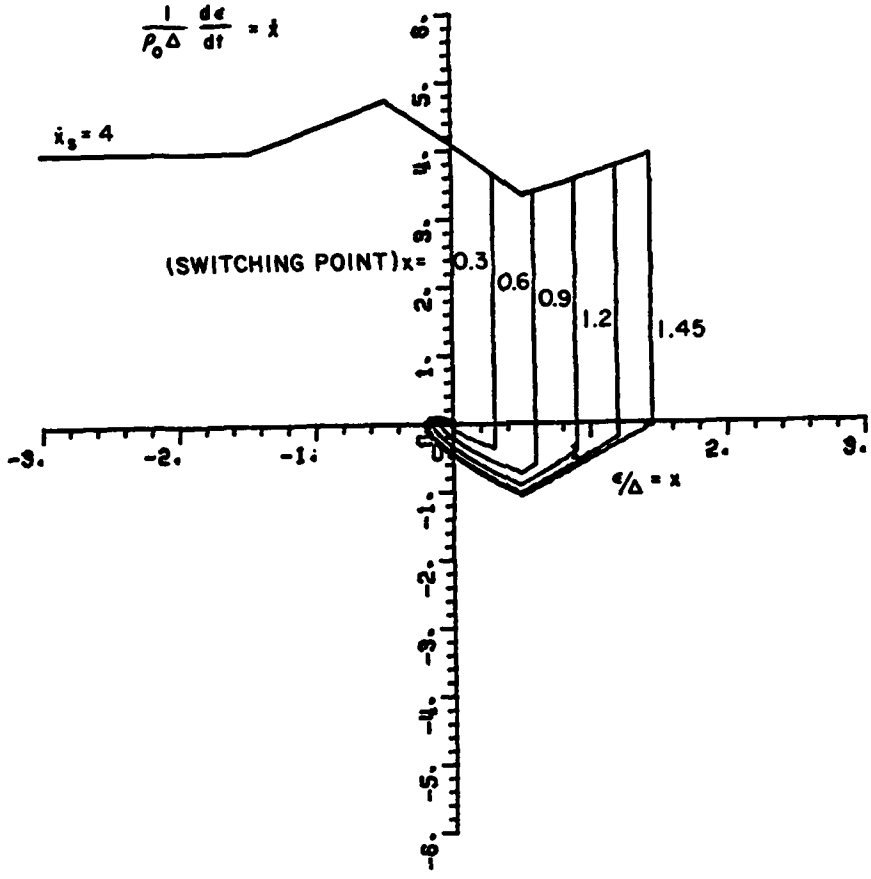

Figure 21. Acquisition trajectory of the delay lock loop with linear envelope detection (normalized loop gain of 10), for various sweep voltage switching times.

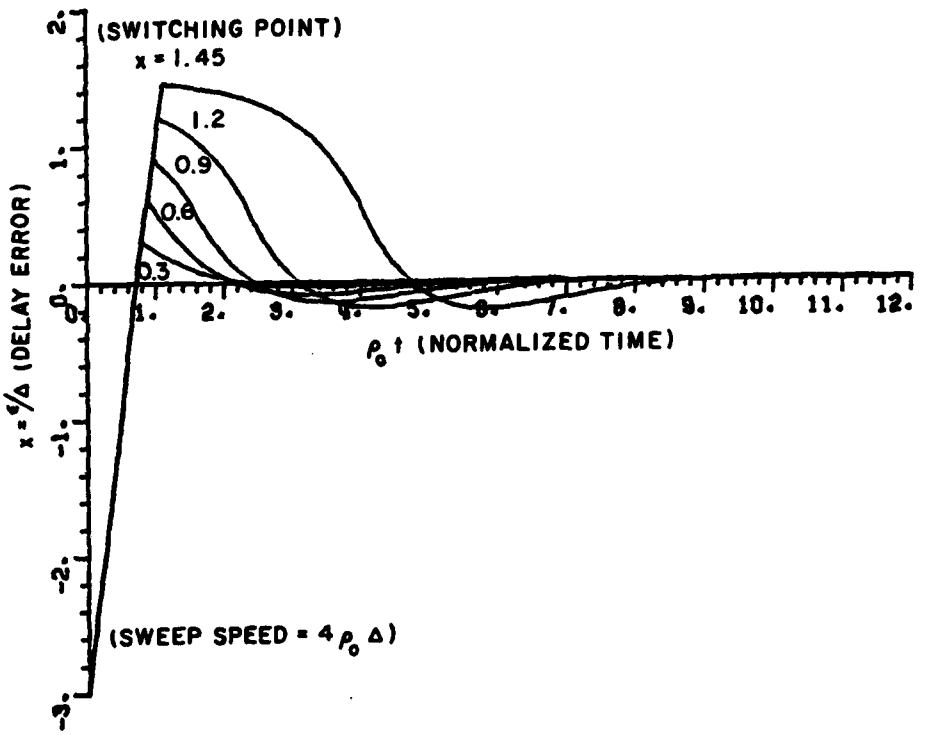

Figure 22. Time response of the delay lock loop with linear envelope detection (normalized loop gain of 10) for various sweep voltage switching times.

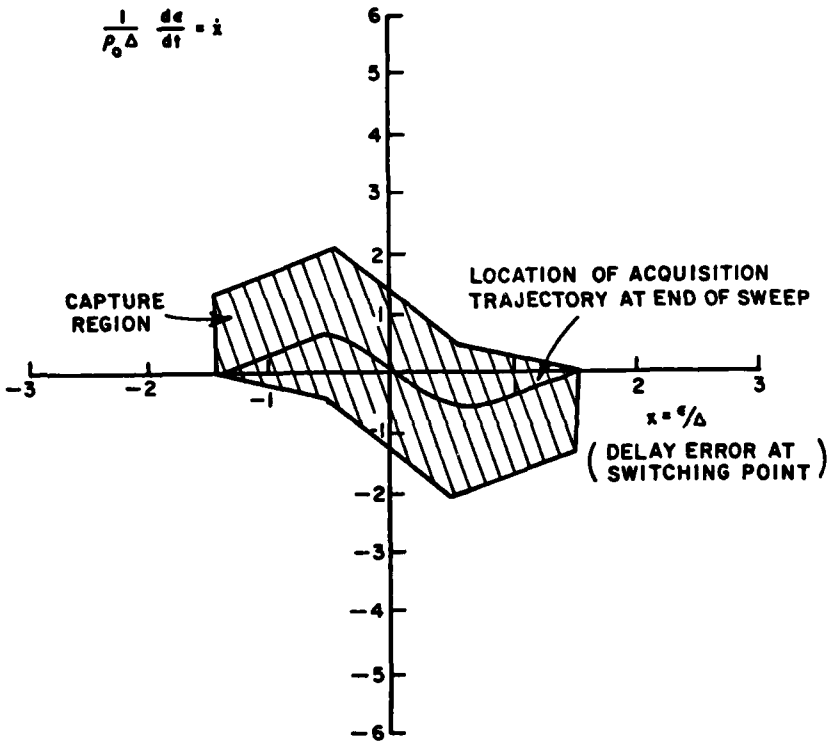

Figure 23. Location in the phase plane of the acquisition trajectory immediately after sweep voltage is switched off for the delay lock loop with linear envelope detection (normalized loop gain of 10).

In Figure 23 it can be noted that as the switching time approaches $\epsilon=0$, the location of the trajectory at the end of the sweep becomes closer to the center of the capture range. Thus, when the incoming signal is corrupted by noise, the chance of the noise causing the trajectory to jump outside the capture range is reduced as the switching time approaches ϵ equal to 0.

Note in Figure 24 that the final transient time is given in terms of ρ_0, the loop filter frequency constant. Because the sweep speed may be much greater than ρ_0 chips per second, the final transient time can become a large portion of the acquisition time. Thus, it is important to have the switching time as near as possible to the time where the final transient time is minimum. In Figure 24 the final transient time is given as the time required after the sweep voltage is switched off for the delay error to become less than and stay within 0.01Δ. The value of 0.01Δ was chosen as it should be (see Chapter VII) less than the standard deviation of the jitter in the loop while tracking the code.

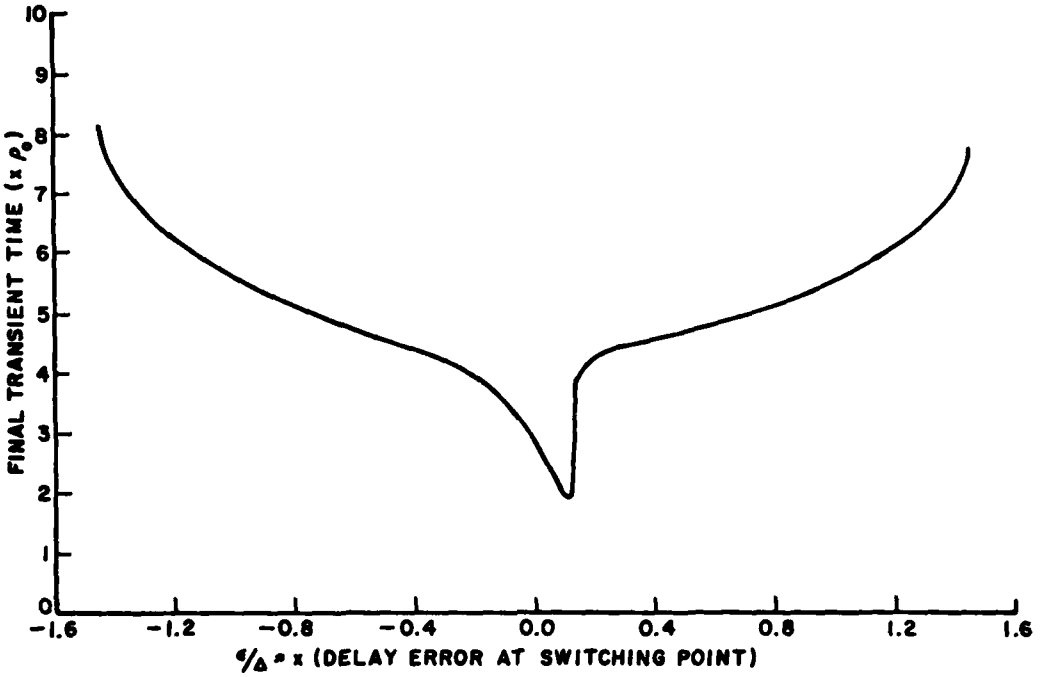

Figure 24. The final transient time versus the delay error when the sweep voltage is switched off, for the delay lock loop with linear envelope detection (normalized loop gain of 10).

The reason for the discontinuity in the curve of Figure 24 when x is approximately 0.1 is as follows. When the sweep voltage is switched off at a delay error greater than 0.1Δ, an additional oscillation in the response is required before the oscillations stay below 0.01Δ. Hence, at this point the final transient time is greatly increased.

If calculations are made with the final error of 0.01Δ decreased, the delay error at the discontinuity (minimum final transient time) approaches zero. If the final error is increased, so is the delay error at the discontinuity, although only slightly for most practical values of final error (up to about 0.05Δ).

Thus, in this section the acquisition trajectory and time response of the delay lock loop with linear envelope detection were determined. It was seen that if the sweep rate is greater than the loop filter frequency constant, a sweep voltage which is turned off after acquisition must be used in the delay lock loop. Without noise the sweep voltage

must be turned off when the timing offset magnitude is less than one and a half chips for acquisition. To ensure acquisition with noise and to keep the final transient time a minimum, the sweep voltage should be turned off when the timing offset is about one tenth of a chip.

D. Acquisition With Noise

In Section C, in examining the lockup of the delay lock loop without noise present, it was determined that the loop should lock, even in the presence of noise, if the sweep voltage is switched off near enough to the time when the timing error is zero. To be analyzed in this part, is the circuitry needed to determine when the sweep should be turned off. Also, after the delay lock loop is tracking the code timing, this circuitry must determine when the loop has lost lock and, therefore, the sweep voltage switched back on. Also, to be determined is the probability of acquisition with noise.

Clearly, the sweep control must utilize some function of the autocorrelation function of the pseudonoise code. One such function could be just the correlation of the incoming signal with a locally generated pseudonoise code at the timing estimate. When the voltage out of the correlation processor exceeded a certain value, the sweep would be switched off. A single correlation, however, only gives a positive correlation value over a plus or minus one chip timing offset interval. The loop can achieve lock and track the signal within a plus or minus one and a half chip error. Hence, the signal used by the sweep control circuits to determine whether the system can lockup, and, after acquisition, whether the loop is still tracking properly, should have a positive value over this range. Such a signal can be generated by taking the sum of the outputs of the envelope detectors in the delay lock loop of Figure 11. This sum channel, with linear envelope detection, has an output, $D_S(x)$, given by

$$D_S(x) = \begin{cases} x + 1.5 & ; \quad -1.5 \leq x < -0.5 \\ 1.0 & ; \quad |x| \leq 0.5 \\ 1.5 - x & ; \quad 0.5 < x \leq 1.5 \\ 0 & ; \quad \text{elsewhere} \end{cases} \quad . \qquad (175)$$

Note that $D_S(x)$ is constant over a range of x from minus one half to plus one half. If envelope detectors with square law detection had been employed in the delay lock loop, the sum channel output, $D_S(x)$, would be lower at x equal to zero than at plus or minus one-half. This is undesirable as the output of the sum channel would decrease near the value of delay error where switching is desired. Devices performing the square root operation on the output of the detectors would be required to generate the output function of Equation (175) in this case.

this complicates both the design and the analysis of the delay lock op, linear envelope detectors have been considered.

The use of the output of two channels for determining proper code ckup, as compared to the use of the output of a single correlation annel, results in more noise in the output for a given signal-to- ise ratio. However, the wider range in delay error for which $D_S(x)$ positive results in better performance with noise present during quisition, as will be seen later.

The delay lock loop with the sum channel used by the sweep con- ol circuitry is shown in Figure 25. The sum of the output of the near envelope detectors is passed through a low pass filter to im- ove performance by reducing the noise. The filter to be examined a single pole (RC) filter whose transfer function given by

$$F_s(s) = \frac{1}{1+s} \tag{176}$$

ere

$$s = p/p_1 \tag{177}$$

ere p_1 is the sum channel filter frequency constant, 1/RC.

The sweep control circuitry compares the output of the filter to given threshold voltage. When this threshold is exceeded the sweep ltage is switched off so that the loop can track the code timing. en the loop is tracking, the output of the filter is compared to the reshold value. If the output voltage falls below the threshold, loss lock is assumed, and the sweep voltage is switched on so that the quisition process may be repeated.

The analysis of the delay lock loop during acquisition (consider- the sweep control) involves several parameters. In general, the le rate, data rate (which determines the spreading ratio), sweep ed, and range in input signal-to-noise ratio are system parameters ch will have been determined earlier. The value of the acquisition eshold and the bandwidth of the sum channel filter must then be ermined based on the performance criteria of the probability of miss l false alarm. The probability of miss is the probability of the ep voltage not being switched off when the delay error is within the ture range of the delay lock loop. The probability of false alarm is probability of the sweep voltage being switched off when the delay or is outside the capture range. In the following analysis the ationship of these parameters is examined and optimum values are ermined.

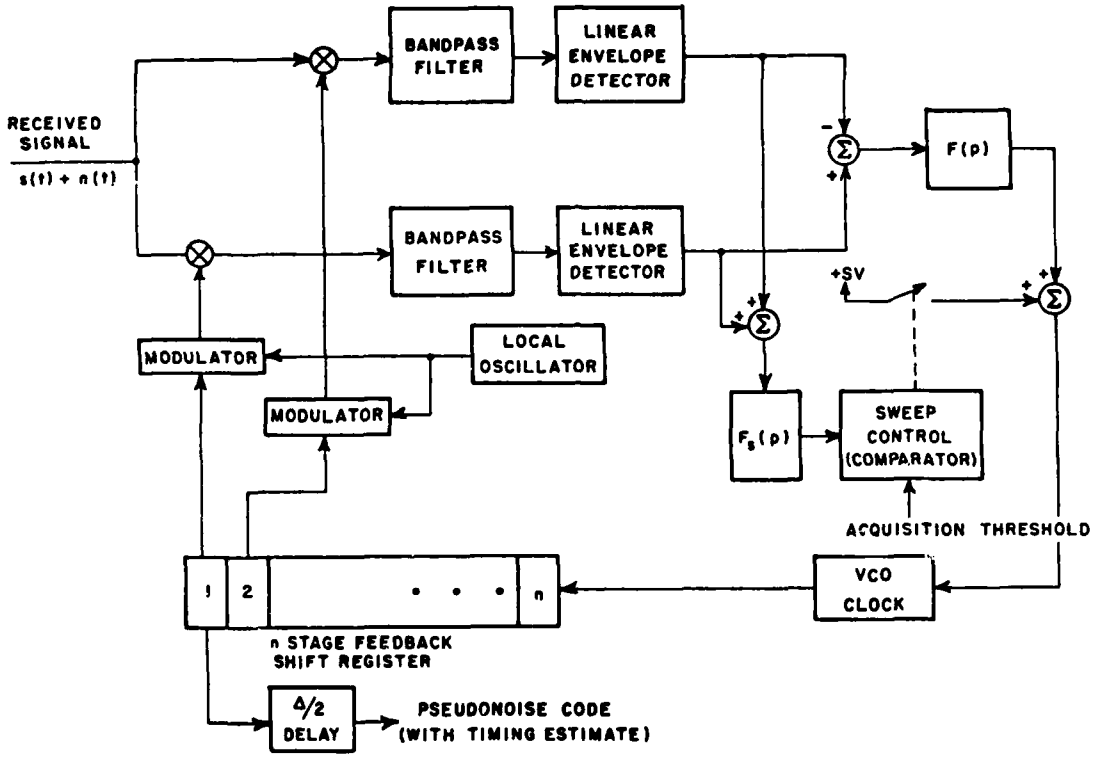

Figure 25. The delay lock loop with linear envelope detection and sweep control utilizing the sum channel voltage.

First to be examined is the output of the sum channel before filtering without noise present. In Equation (174) this output is given as a function of x, the timing offset. To analyze the output after filtering this output must be given as a function of time. As seen in Figure 21, the change in time offset with respect to time, $\dot{x}$, varies with timing offset, even if the loop does not lock, because the difference channel output (D(x)) is present in the loop at all times. If this channel were removed during the sweep portion of the acquisition, the sweep rate would be constant and the output of the sum channel as a function of time would be given by

$$D_s(t) = \begin{cases} (t-t_o)\dot{x}_s + 1.5 & -\frac{1.5}{\dot{x}_s} \le (t-t_o) < \frac{-0.5}{\dot{x}_s} \\ 1.0 & |t-t_o| < \frac{0.5}{\dot{x}_s} \\ 1.5-(t-t_o)\dot{x}_s & \frac{0.5}{\dot{x}_s} < (t-t_o) \le \frac{1.5}{\dot{x}_s} \\ 0 & \text{elsewhere} \end{cases} , \quad (178)$$

where t_o is the time when x is equal to minus one and one-half.

However, if the difference channel output was removed, the location of the acquisition trajectory at the end of the sweep (see Figure 23) would always be along the x axis. This is not as close to the center of the capture region of the loop, and, thus, the probability of not acquiring the signal with noise present would be increased. Also, since $\dot{x}$ is zero at the end of the sweep, the final transient time is increased. Therefore, the system was designed so that the difference channel output is always present in the loop, and, therefore, its effect on the sum channel output must be considered.

With the difference channel output in the loop, the output of the sum channel as a function of time can be computed by combining the results of Section C with Equation (175). In Figure 26 the output of the sum channel is shown for various normalized sweep speeds, $\dot{x}_s$. Note that the time has been normalized to the sweep speed so that a comparison to Equation (178) can be made. From Figure 26 it is seen that as the sweep rate is increased, the output of the sum channel approaches that of Equation (178). Since in most systems,

$$\dot{x}_s > 10 \quad , \tag{179}$$

the output of the sum channel will be assumed to be given by Equation (178) in this analysis.

Next to be examined is the sum channel output before filtering with noise present. The noise considered consists of both received thermal noise and the self noise generated in the loop. This self noise is due to timing error and other undesired signal components. The noise is assumed to be white Gaussian noise with single sided power spectral density of N_o.

The signal power out of the bandpass filter in each delay lock loop channel is dependent on the timing offset between the received signal and the coded signal with which it is mixed in that channel, P_{s_i}, where i is one for the top or delayed channel in Figure 25 and two for the bottom or advanced channel, is given by

$$P_{S_1}(x) = \begin{cases} P_S(x+0.5)^2 & -0.5 \leq x \leq 0.5 \\ P_S(1.5-x)^2 & 0.5 < x \leq 1.5 \\ 0 & \text{elsewhere} \end{cases} \tag{180}$$

and

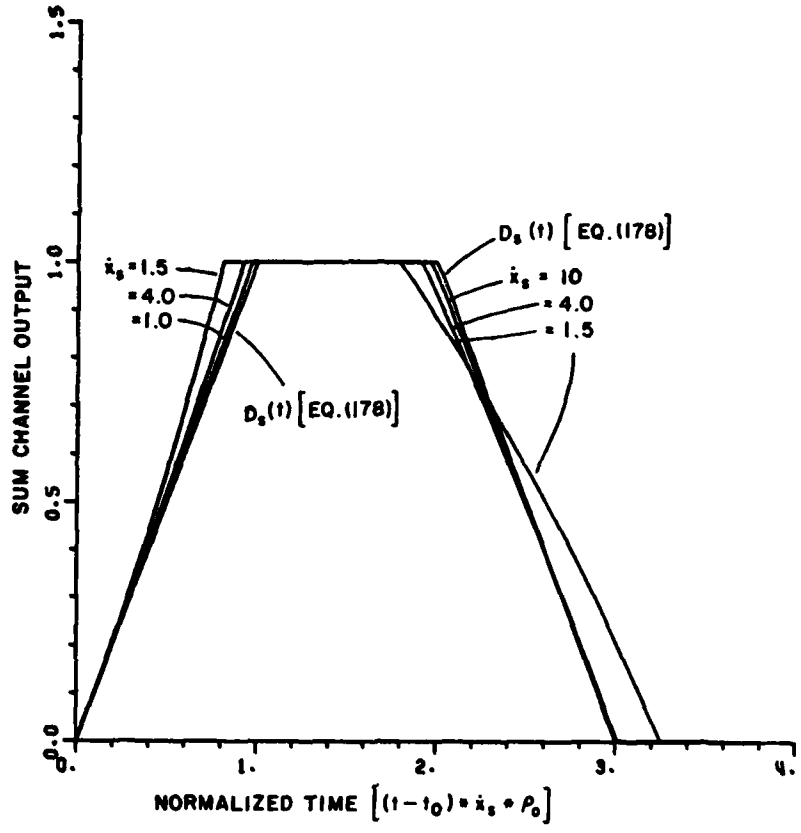

Figure 26. Sum channel output before filtering for the delay lock loop with linear envelope detection (normalized loop gain of 10) versus time for various sweep speeds.

$$P_{S_2}(x) = \begin{cases} P_S(x+1.5)^2 & -1.5 \leq x \leq -0.5 \\ P_S(0.5-x)^2 & -0.5 < x \leq 0.5 \\ 0 & \text{elsewhere} \end{cases} \qquad (181)$$

where P_S is the power in the signal out of the filter when there is no timing error in the channel.

Note that with a four-phase signal P_S is only half of the power into the filter with no timing error because the long code biphase portion of the signal, when mixed with the short coded signal, does not pass through the filter.

As shown before, if Equation (179) is true, $p_{s_i}(t)$ may be obtained by using the relation given by

$$x = (t-t_o)\dot{x}_s \tag{182}$$

in Equations (180) and (181).

When the signal plus noise is passed through the bandpass filter of bandwidth B_{IF}, with no timing offset in the channel, the signal-to-noise ratio out of the filter is given by

$$S/N\Big|_{IF} = \frac{P_S}{N_o B_{IF}/2} \quad . \tag{183}$$

The signal-to-noise ratio in the ith channel for any timing offset is then given by

$$S/N\Big|_i = S/N\Big|_{IF} \frac{P_{s_i}}{P_S} \quad . \tag{184}$$

The output of the linear envelope detector is described by its mean and power spectral density. To determine the mean value of the output, first consider the linear rectifier, described by

$$V_{out} = \begin{cases} 0 & V_{in} \leq 0 \\ \\ V_{in} & V_{in} > 0 \end{cases} , \tag{185}$$

where V_{in} is the input voltage and V_{out} is the output voltage. From [16] the expected value of the output voltage is given by

$$E\{V_{out}\} = \left(\frac{N_o B_{IF}/2}{2\pi}\right)^{1/2} {}_1F_1\left(-\frac{1}{2};\ 1;\ -\frac{S}{N}\Big|_i\right) \quad . \tag{186}$$

where ${}_1F_1(\cdot)$ is the confluent hypergeometric series given by

$${}_1F_1(c;d;z) = \sum_{j=0}^{\infty} \frac{(c)_j}{(d)_j} \frac{z^j}{j!} \tag{187}$$

where

$$(a)_j = \begin{cases} a(a+1) \cdots (a+j-1) & j \geq 1 \\ 1 & j = 0 \end{cases} \quad . \tag{188}$$

For the linear envelope detector described by

$$V_{out} = \begin{cases} -V_{in} & V_{in} \leq 0 \\ V_{in} & V_{in} > 0 \end{cases} \quad , \tag{189}$$

the expected value of the output can easily be shown to be twice that of Equation (186), or

$$E\{V_{out}\} = 2\left(\frac{N_o B_{IF}/2}{2\pi}\right)^{1/2} {}_1F_1\left(-\frac{1}{2};\ 1;\ -\frac{S}{N}\Big|_i\right) \quad . \tag{190}$$

For the linear rectifier, the power spectral density as a function of frequency, f, of the output is given by [16]

$$W_c(f) = \begin{cases} 2h_{11}^2 N_o/2 + h_{02}^2 B_{IF}(N_o/2)^2 \frac{1}{4}(2-f/(B_{IF}/2)) & \\ \qquad \text{for } 0 < f \leq B_{IF}/2 & \\ h_{02}^2 B_{IF}(N_o/2)^2 \frac{1}{4}(2-f/(B_{IF}/2)) & \\ \qquad \text{for } B_{IF}/2 < f \leq B_{IF} & \\ 0 \qquad \text{elsewhere} & \end{cases} \tag{191}$$

where

$$h_{11} = \frac{1}{2}\left(\frac{S/N|_i}{\pi}\right)^{1/2} {}_1F_1\left(\frac{1}{2};\ 2;\ -\frac{S}{N}\Big|_i\right) \tag{192}$$

and

$$h_{02} = (2\pi N_o B_{IF}/2)^{-1/2} {}_1F_1\left(\frac{1}{2};\ 1;\ -\frac{S}{N}\Big|_i\right) \quad . \tag{193}$$

For the linear envelope detector [17],

$$h'_{11} = 2h_{11} \tag{194}$$

and

$$h'_{02} = 2h_{02} \quad , \tag{195}$$

and the power spectral density may be easily determined.

Equations (190) and (191) give values based on a constant $S/N|_i$. However, P_{S_i} and, thus, $S/N|_i$ vary with time during acquisition. From Equation (151) the sweep rate can be expressed in the form given by

$$\text{Sweep rate} = \frac{k}{N'} \cdot \text{data rate} \quad , \tag{196}$$

where k is the spreading ratio. In most spread spectrum systems, the spreading ratio is much smaller than the code length, i.e.,

$$k/N' << 1 \quad . \tag{197}$$

When Equation (197) holds

$$B_{IF} \doteq \text{data rate} >> \text{Sweep rate}, \tag{198}$$

and the mean and power spectral density equations are valid at a given time even though their values are changing with time.

Equation (190) may now be written in the form

$$(E[V_{out}],t) = 2\left(\frac{1}{2\pi \left.\frac{S}{N}\right|_{IF}}\right)^{1/2} {}_1F_1\left(-\frac{1}{2}; 1; -\left.\frac{S}{N}\right|_{IF} \frac{P_{s_i}(t)}{P_S}\right)\sqrt{P_S} \tag{199}$$

where $P_{s_i}(t)$ is given by Equations (180) and (181) with Equation (182). Thus, the mean of the output of the filter for one channel is given by

$$\mu_i(t) = F^{-1}\{F\{(E[V_{out}],t|_{fixed})\} \cdot F_s(j\omega)\} \tag{200}$$

where $F\{\cdot\}$ is the Fourier transform, $F^{-1}\{\cdot\}$ is the inverse Fourier transform, and $F_s(j\omega)$ is the sum channel filter transfer function of Equation (184) with $j\omega$ substituted for p. Because the sum channel is

linear, the output of the filter can be considered as the sum of the outputs for each channel. The mean value of the output of the filter is then given by

$$\mu(t) = \mu_1(t) + \mu_2(t) \quad . \tag{201}$$

The bandwidth of the sum channel filter, B_n, is given by

$$B_n = \frac{1}{2\pi} \int_0^\infty |F_s(j\omega)|^2 \, d\omega \quad , \tag{202}$$

or

$$B_n = \frac{1}{2\pi} \int_0^\infty \frac{1}{1+\omega RC)^2} \, d\omega \quad , \tag{203}$$

or

$$B_n = \frac{1}{4RC} \quad . \tag{204}$$

Because B_n is usually on the order of the sweep rate, from Equation (198) it can be assumed that

$$B_n << B_{IF} \quad . \tag{205}$$

Therefore, the power spectral density of the output of the filter for one channel can be approximated by

$$W_c(f) = \begin{cases} 8h_{11}^2(N_o/2) + 4h_{02}^2 B_{IF}(N_o/2)^2 \cdot \frac{1}{2} \\ \qquad\qquad \text{for } 0 < f < B_n \\ 0 \qquad\qquad \text{elsewhere} \end{cases} \quad . \tag{206}$$

The probability density function of the voltage out of the envelope detector is Rician. However, with the assumption of Equation (205) the filter output can be considered to have a Gaussian density. The variance of the filter output for one channel is then given by

$$\sigma_i^2 = \int_0^\infty W_c(f)df \quad , \tag{207}$$

or from Equation (206)

$$\sigma_i^2 = [8\, h_{11}^2 (N_o/2) + 2\, h_{02}^2\, B_{IF} (N_o/2)^2]\, B_n \quad . \tag{208}$$

As the variance is a function of time, this may be rewritten as

$$\sigma_i^2(t) = \frac{B_n}{B_{IF}\pi} \left[2\, \frac{P_{s_i}(t)}{P_S}\, {}_2F_1\left(\frac{1}{2};\, 2;\, -\frac{S}{N}\Big|_{IF}\, \frac{P_{s_i}(t)}{P_S}\right) + \frac{1}{\frac{S}{N}\Big|_{IF}}\, {}_2F_1\left(\frac{1}{2};\, 1;\, -\frac{S}{N}\Big|_{IF}\, \frac{P_{s_i}(t)}{P_S}\right) \right] P_S \quad . \tag{209}$$

Because the noise in each channel can be assumed to be independent, the variance of the output of the sum filter is given by

$$\sigma^2(t) = \sigma_1^2(t) + \sigma_2^2(t) \quad . \tag{210}$$

With the mean and variance of the filter output, $z(t)$, known, the probability of false alarm and miss for a given acquisition threshold, z_{acq}, can be determined. The probability of false alarm is given by

$$P_{fa} = P_r(z(t) \geq z_{acq} / P_{S_1}(t) = P_{S_2}(t) = 0) \tag{211}$$

or

$$P_{fa} = \int_{z_{acq}}^\infty \frac{1}{\sqrt{2\pi}\sigma}\, e^{-\frac{(z-\mu)^2}{2\sigma^2}}\, dz \tag{212}$$

$$= \frac{1}{2} \cdot \frac{2}{\sqrt{\pi}} \int_{\left(\frac{z_{acq}-\mu}{\sqrt{2}\,\sigma}\right)}^\infty e^{-z^2}\, dz \tag{213}$$

or, using the complementary error function,

$$P_{fa} = \frac{1}{2} \operatorname{erfc}\left(\frac{z_{acq}-\mu}{\sqrt{2}\sigma}\right) \tag{214}$$

where (with $P_{s_i}(t) = 0$ in Equations (201) and (210))

$$\mu = 4\left(2\pi \left.\frac{S}{N}\right|_{IF}\right)^{-1/2} \sqrt{P_S} \tag{215}$$

and

$$\sigma = \sqrt{\frac{2\,B_n}{\pi\, B_{IF}\left(S/N\big|_{IF}\right)}}\ \sqrt{P_S} \quad . \tag{216}$$

The probability of miss, which is a function of timing offset (or time as related by Equation (182)) is then given by

$$P_{miss}(t) = P_r(z(t) < z_{acq} / P_{s_1}(t) \neq 0 \text{ or } P_{s_2}(t) \neq 0) \tag{217}$$

or

$$P_{miss}(t) = \int_{-\infty}^{z_{acq}} \frac{1}{\sqrt{2\pi}\sigma(t)}\, e^{-\frac{(z-\mu(t))^2}{2\sigma^2(t)}}\, dz \tag{218}$$

or

$$P_{miss}(t) = \frac{1}{2} \operatorname{erfc}\left(\frac{2\mu(t)-z_{acq}}{\sqrt{2}\,\sigma(t)}\right) \tag{219}$$

where $\mu(t)$ and $\sigma(t)$ are given in Equations (201) and (210), respectively.

Equations (214) and (219) can be solved by using numerical analysis on a computer. The following approximations from asymptotic expansions were used in solving these equations.

For the confluent hypergeometric series with $x > 7$ (from [18])

$${}_1F_1\left(-\frac{1}{2};\ 1;\ -x\right) \doteq 2\sqrt{\frac{x}{\pi}}\left[1 + \frac{1}{4x} + \frac{1}{64x^2}\right] \quad , \tag{220}$$

$$,F_1\left(\frac{1}{2};\ 2;-x\right) \doteq \frac{2}{\sqrt{\pi x}}\left[1 - \frac{1}{4x}\right] \quad , \tag{221}$$

and

$$,F_1\left(\frac{1}{2};\ 1;-x\right) = \frac{1}{\sqrt{\pi x}}\left[1 + \frac{1}{4x}\right] \quad . \tag{222}$$

For the complementary error function (from [18])

$$\text{erfc}(x) \doteq \begin{cases} \dfrac{e^{-x^2}}{\sqrt{\pi}x}\left(1 + \sum\limits_{i=1}^{\ell} \dfrac{\prod\limits_{j=1}^{i}(2j-1)}{(2x^2)^i}(-1)^i\right) & x>2 \\ 1 - \dfrac{2}{\sqrt{\pi}} \sum\limits_{i=1}^{\ell} \dfrac{x^{(2i-1)}(-1)^{i-1}}{(2i-1)\prod\limits_{j=2}^{i}(j-1)} & 0<x<2 \\ 2 - \text{erfc}(-x) & x<0 \end{cases} \quad , \tag{223}$$

where ℓ is chosen so to terminate the series when the terms begin to increase in absolute value.

To determine the acquisition threshold for a given P_{fa} or P_{miss} the method of bisection [19] was used to find the inverse of the complementary error function.

The results of the computer analysis can be examined now. However, an interpretation of the meaning of the various parameters involved will be made first.

Note that since $\sqrt{P_S}$ is a common factor to both the mean and variance, results obtained will be independent of P_S and depend only on the signal-to-noise ratio, as expected.

P_{fa}, as given in Equation (214), is, as stated before, the probability that z(t) will exceed z_{acq} when the delay error is outside plus or minus 1.5Δ at any given time. Because z(t) is passed through a filter of time constant, τ_c, given by

$$\tau_c = RC \quad , \tag{224}$$

the P_{fa} for a given period of time during acquisition is approximately given by

$$P_{fa}(t_1 \leq t \leq t_2) \doteq P_{fa}(\text{from Equation (214)}) \cdot \frac{(t_2-t_1)}{\tau_c} \quad . \quad (225)$$

If a false alarm occurs, it should take a period of time approximately equal to the time constant before z(t) falls below Z_{acq} causing the sweep voltage to be switched on again. Thus, the expected value of the proportional increase in acquisition time for a given P_{fa} is approximately the P_{fa} given in Equation (214).

P_{miss}, on the other hand, varies with timing offset and will take on different values over the range of timing error from minus 1.5Δ to plus 1.5Δ. However, if it assumed that

$$B_n > f_s \quad , \quad (226)$$

then P_{miss} for each sweep past the correct timing offset is simply the maximum value of P_{miss} over the range of timing error.

At this point the optimum value of the sum channel filter bandwidth, B_n, (as related to f_s) can be determined using computer analysis. Optimum value in this case means that value for which the probability density functions of the sum channel output amplitude with and without signal present have the greatest separation. In other words, it is the value of B_n that, for a given value of P_{miss}, yields minimum P_{fa} and vice versa (if P_{miss} and P_{fa} are less than 0.5). Analysis has shown that the optimum value of B_n is given by

$$B_n\Big|_{opt} \doteq 0.53\, f_s \quad , \quad (227)$$

and that the maximum value of P_{miss} occurs at the time when the timing offset is 0.1Δ, or

$$P_{miss}\Big|_{max} = P_{miss}\Big|_{\varepsilon=0.1\Delta} \quad . \quad (228)$$

These values are independent of other parameters involved (such as $S/N|_{IF}$) to the accuracy shown here. Note that Equation (227) verifies that the assumption of Equation (226) is true. Also, Equation (228) means that if the sweep voltage is switched off during the time when code acquisition can occur, it will be switched off at or before a timing error of 0.1Δ as desired from Section C.

The parameters of interest left to examine are B_{IF}, f_s, and $S/N|_{IF}$. From Equations (196) and (198),

$$\frac{B_{IF}}{f_s} \doteq (\text{data rate}) \cdot \frac{N'}{\text{code rate}} \tag{229}$$

or

$$\frac{B_{IF}}{f_s} \doteq \frac{N'}{k} \tag{230}$$

where k is the spreading ratio. Therefore, the results (P_{fa}, P_{miss}, and z_{acq}) to be presented will be given as functions of N'/k and $S/N|_{IF}$.

In Figure 27 a comparison has been made of the performance of a digital acquisition method described in [6,pp. 588-592] and the analog method described in this section. Since the two methods are completely different, a comparison can only be made based on similar acquisition times and data rates (not on similar B_n's and f_s's). Figure 27 shows that approximately 3.5 dB higher $S/N|_{IF}$ is required by the analog method to obtain the same P_{miss} for a given P_{fa}. Part of this difference may be due to the use of the sum of two channels (and, thus, twice the noise level) for the analog method as compared to one channel in the digital case. However, not enough information is provided in [6] to be able to verify their results.

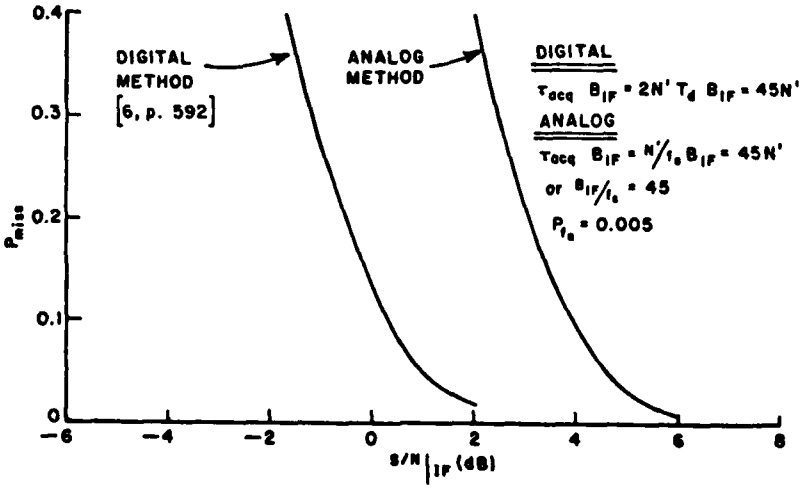

Figure 27. Comparison of the performance of a digital acquisition method [6,Fig. 18-34] and the analog method of Chapter VI, for a given P_{fa} and $\tau_{acq}B_{IF}$.

The results presented in [6,p. 592] are given for a low P_{fa} and a rather high P_{miss}, which is of interest in a radar problem. In the application discussed in this paper, the opposite is true. As shown before, a fairly high P_{fa} (say 0.1) only increases the acquisition time by the same proportion (10% in this case). Hence, a rather high P_{fa} can be tolerated. A miss causes the acquisition time to double, however. In a jammer environment, this additional delay may be enough to cause the adaptive array not to be able to acquire the desired signal at all. Thus, P_{miss} must be kept very low (actual values would be based on the required reliability of the system).

In Figure 28 the P_{fa} is plotted versus $S/N|_{IF}$ for a given P_{miss} with several values of N'/k. These curves can be used to determine the performance of a given system. Since Z_{acq} varies in these curves, the acquisition threshold, as given in Figure 29, for the worst case can be used in a system to assure performance better than or equal to that of the worst case.

Thus, in this section the use of the sum channel voltage in determining when to turn off the sweep voltage has been described. Equations were derived and results plotted for the probability of acquisition with given threshold levels versus signal-to-noise ratio in the delay lock loop for given short code lengths and spreading ratios.

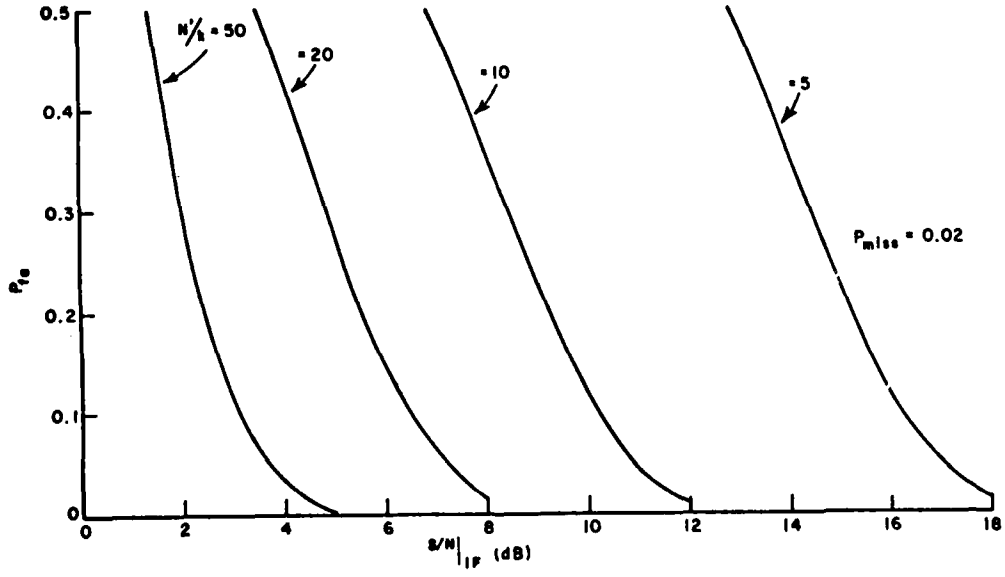

Figure 28. The probability of false alarm versus $S/N|_{IF}$ for several values of N'/k, for acquisition of the delay lock loop of Figure 25.

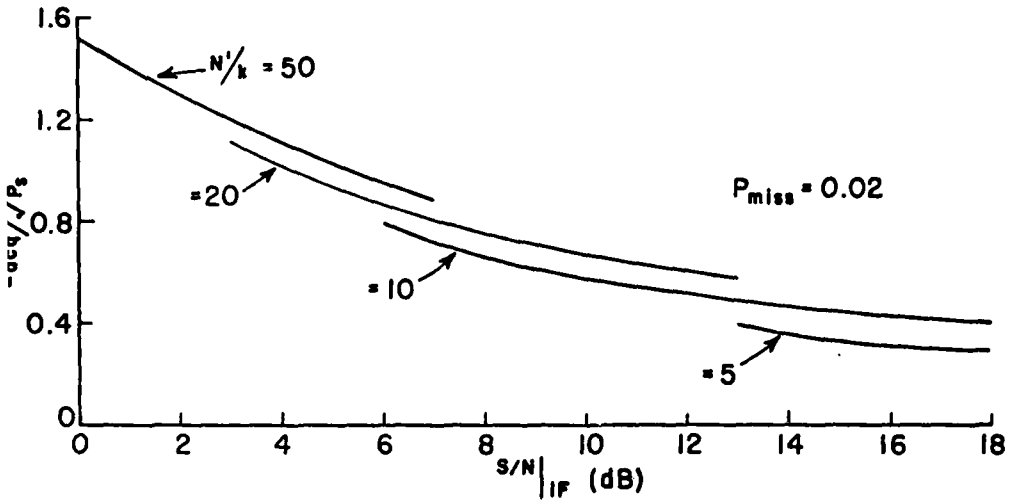

Figure 29. Normalized acquisition threshold versus $S/N|_{IF}$ for several values of N'/k corresponding to Figure 28.

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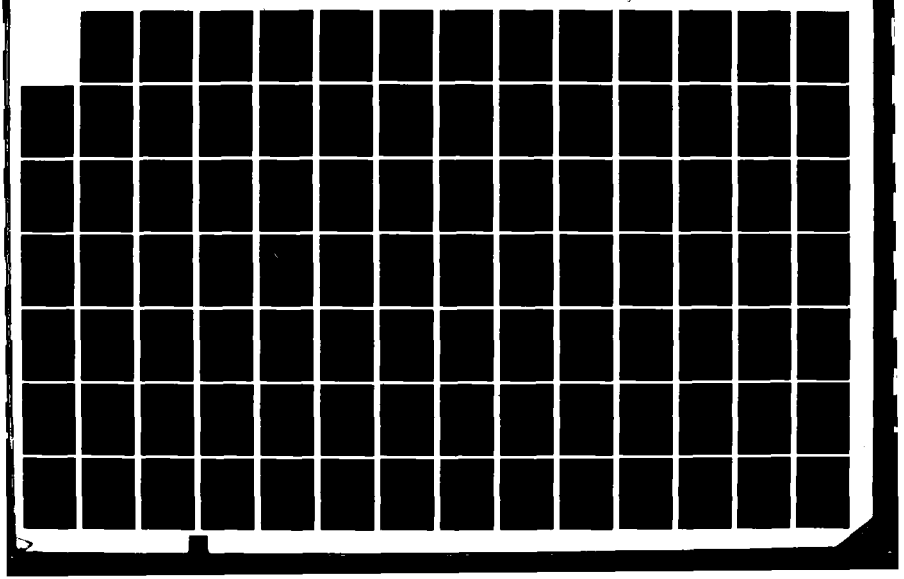
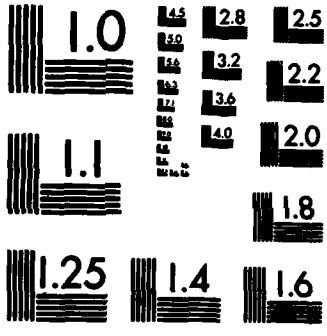




CHAPTER VII

TRACKING OF THE CODES BY THE DELAY LOCK LOOP

A. Introduction

After acquisition of the short code timing, the delay lock loop tracks the short code timing during the acquisition of the long code timing. After acquisition of the long code timing, the delay lock loop then tracks the long code timing. Because the short code timing is used in the long code acquisition process as discussed in Chapter V, any tracking error of the short code will affect the long code acquisition time (see Chapter VIII). The tracking error of the delay lock loop is discussed in this chapter.

In the delay lock loop, noise is generated by the signals in the loop even if noise is not present with the received signal. This generated noise is called self noise and is examined in Section B. In Section B the self noise in each channel (advanced and delayed code channels) is determined. The self noise out of the sum filter is calculated and the effect is discussed of this noise on the short code acquisition procedure. The self noise out of the difference (loop) filter is then determined and the effect is discussed of this noise on the tracking error of the delay lock loop.

In Section C the tracking jitter of the delay lock loop with noise present on the received signal is discussed. Results are obtained on what effect noise and loop bandwidth have on the tracking jitter.

B. Self Noise

In order to determine the tracking performance of the delay lock loop, the self noise in the loop must first be examined. Self noise is defined as the signal components, other than the desired, which are generated when the coded biphase signal generated in the delay lock loop is mixed with the received four-phase signal (see Figure 25). In this section the power spectral density of the self noise in each channel of the delay lock loop is first determined. The cross-correlation of the self noise between the channels is then examined. The self noise out of the sum and difference filters is then calculated and expressions are

derived relating the signal-to-noise ratio in each channel to the received signal-to-noise ratio.

In the analysis of this section the presence of data on the four-phase signal has not been considered. Although data modulation will be present with one code on the signal in the four-phase system, it will not be significantly affected by the narrow bandpass filter in each channel. It can be shown that with the bandwidth of the bandpass filter on the order of the data modulation rate, the desired component output of this filter will be reduced by only twenty percent when data modulation is present. Data modulation has, therefore, not been considered as being present with either code on the four-phase signal, so that the self noise equations in this section are valid for the delay lock loop tracking of either the long or the short code timing.

The four-phase signal without data is given by Equation (19), or

$$s_r(t) = \sqrt{P_r}\sin(\omega_1 t + \theta(t)) + \sqrt{P_r}\cos(\omega_1 t + \phi(t)) \quad . \qquad (231)$$

where P_r is the power in the received signal.

The biphase signal that is mixed with the four-phase signal in one channel of the delay lock loop is given by

$$S_b(t) = \sqrt{2P_b}\sin(\omega_2(t+\varepsilon) + \theta(t+\varepsilon) + \psi) \qquad (232)$$

where P_b is the biphase signal power and ε is the timing error between the biphase and the received four-phase signal in one channel. The output of the mixer is then given by

$$S_{out}(t) = S_r(t)S_b(t) \qquad (233)$$

or, considering only the lower frequency components,

$$S_{out}(t) = \sqrt{2P_s}\,[\cos(\omega_1 t - \omega_2(t+\varepsilon) - \theta(t+\varepsilon) + \theta(t) - \psi)$$

$$- \sin(\omega_1 t - \omega_2(t+\varepsilon) - \theta(t+\varepsilon) + \phi(t) - \psi)] \quad , \qquad (234)$$

where $2P_s$ is the signal power in one channel of the delay lock loop. Equation (234) may be expressed as

$$S_{out}(t) = \sqrt{2P_s}\,[\cos((\omega_1 - \omega_2)t - \omega_2\varepsilon - \psi) \cdot \cos(\theta(t) - \theta(t-\varepsilon))$$

$$- \sin((\omega_1 - \omega_2)t - \omega_2\varepsilon - \psi) \cdot \cos(\phi(t) - \theta(t+\varepsilon))] \quad . \tag{235}$$

Note that if $\varepsilon=0$, the desired signal component is $\sqrt{2P_s}\cos((\omega_1-\omega_2)t - \psi)$, a CW signal.

To determine the power spectral density of the self noise in each channel from Equation (235) it is first necessary to consider the power spectral density of each of the baseband self noise components, $\cos(\theta(t) -\theta(t-\varepsilon))$ and $\cos(\phi(t)-\theta(t+\varepsilon))$. These two components are the results of the mixing of the coded biphase signal generated by the delay lock loop with the biphase component of the four-phase signal with the same code as that being tracked and with the biphase component of the four-phase signal with the different code, respectively. Since two different codes are involved, the two signal components of Equation (235) are not only orthogonal, but they are also uncorrelated. Thus, the power spectral density of $S_{out}(t)$ may be considered as the sum of the power spectral density of each orthogonal signal.

First to be examined is the baseband signal formed by the mixing of the biphase signals with different codes, $\cos(\phi(t)-\theta(t+\varepsilon))$. Because there is no desired signal component in this signal, the entire signal is self noise. The baseband signal, $\cos(\phi(t)-\theta(t+\varepsilon))$ is a pseudorandom sequence of 1's and 0's whose symbol duration is alternately $|\varepsilon_1|$ and $\Delta-|\varepsilon_1|$, where

$$\varepsilon_1 \triangleq \varepsilon - m\Delta \quad , \quad m = 0, \pm 1, \cdots \tag{236a}$$

and

$$|\varepsilon_1| \leq \Delta/2 \quad . \tag{236b}$$

The pseudorandom sequence has a length on the order of the product of the lengths of the long and short codes, and, hence, is very long. It can, therefore, be assumed that the sequence has infinite length (i.e., it is a truly random sequence) with a negligible effect on the results. The autocorrelation function of this sequence can be calculated to be given by

$$R(\tau) = \begin{cases} 1 - 2\frac{|\tau|}{\Delta} & |\tau| < |\varepsilon| \\ 1 - \left(\frac{|\varepsilon|+|\tau|}{\Delta}\right) & |\varepsilon| \leq |\tau| \leq \Delta-|\varepsilon| \\ 0 & \text{elsewhere} \end{cases} . \quad (237)$$

The autocorrelation function may be rewritten as

$$R(\tau) = R_1(\tau) + R_2(\tau) \quad (238)$$

where

$$R_1(\tau) = \begin{cases} \left(\frac{|\varepsilon|-|\tau|}{\Delta}\right) & |\tau| < |\varepsilon| \\ 0 & \text{elsewhere} \end{cases} \quad (239)$$

and

$$R_2(\tau) = \begin{cases} 1 - \frac{|\varepsilon|+|\tau|}{\Delta} & |\tau| < \Delta-|\varepsilon| \\ 0 & \text{elsewhere} \end{cases} . \quad (240)$$

The Fourier transform of $R_1(\tau)$ and $R_2(\tau)$ is given by

$$F\{R_1(\tau)\} = \frac{|\varepsilon|}{\Delta}^2 \text{sinc}^2(\pi f|\varepsilon|) \quad (241)$$

and

$$F\{R_2(\tau)\} = \frac{(\Delta-|\varepsilon|)^2}{\Delta} \text{sinc}^2(\pi f(\Delta-|\varepsilon|)) . \quad (242)$$

Therefore, the Fourier transform of $R(\tau)$, the power spectral density of the baseband signal, is given by

$$G_1(f) = \frac{(\Delta-|\varepsilon|)^2}{\Delta} \text{sinc}^2(\pi f(\Delta-|\varepsilon|)) + \frac{|\varepsilon|^2}{\Delta} \text{sinc}^2(\pi f|\varepsilon|) . \quad (243)$$

The power spectral density of the self noise component from the product of the two differently coded biphase signals in one channel is, therefore, given by

$$G_{sn_1} = \frac{P_s}{2} G_1(f-f_0) + \frac{P_s}{2} G_1(f+f_0) \qquad (244)$$

where

$$f_0 = (\omega_1 - \omega_2)/2\pi \quad . \qquad (245)$$

The other baseband signal to be examined is the signal formed by the mixing of the biphase signals with the same codes, $\cos(\theta(t)-\theta(t+\varepsilon))$. Three possible ranges for ε may be considered for this signal,

$$|\varepsilon| < \Delta/2 \quad , \qquad (246)$$

$$\frac{\Delta}{2} \leq |\varepsilon| < \Delta \quad , \qquad (247)$$

and

$$|\varepsilon| \geq \Delta \quad . \qquad (248)$$

With $|\varepsilon|<\Delta/2$, the baseband signal has a value of +1, except for -1 pulses of width $|\varepsilon|$ which occur with a probability of about one-half at every chip interval. When the long code is involved, the occurrence of these pulses may be assumed to be completely random, with a negligible effect on the results. In this case, the autocorrelation function is given by

$$R(\tau) = \begin{cases} 1 - \dfrac{2|\tau|}{\Delta} & |\tau| < |\varepsilon| \\ 1 - \dfrac{|\varepsilon|+|\tau-m\Delta|}{\Delta} & m\Delta-|\varepsilon| \leq \tau < m\Delta+|\varepsilon| \\ & \text{for } m=\pm1,\pm2, \cdots \\ 1 - \dfrac{2|\varepsilon|}{\Delta} & \text{elsewhere} \end{cases} \quad . \qquad (249)$$

The autocorrelation function may be rewritten as

$$R(\tau) = R_1(\tau) + R_2(\tau) + R_3(\tau) \tag{250}$$

where

$$R_1(\tau) = 1 - \frac{2|\varepsilon|}{\Delta} \qquad \text{for all } \tau \quad , \tag{251}$$

$$R_2(\tau) = \begin{cases} \dfrac{|\varepsilon| - |\tau|}{\Delta} & |\tau| < |\varepsilon| \\ 0 & \text{elsewhere} \end{cases} \tag{252}$$

and

$$R_3(\tau) = \begin{cases} \dfrac{|\varepsilon| - |\tau - m\Delta|}{\Delta} & m\Delta - |\varepsilon| \le \tau < m\Delta + |\varepsilon| \text{ for } m = 0, \pm 1, \pm 2, \cdots \\ 0 & \text{elsewhere} \end{cases} , \tag{253}$$

The Fourier transform of $R_1(\tau)$ and $R_2(\tau)$ is given by

$$F\{R_1(\tau)\} = \left(1 - \frac{2|\varepsilon|}{\Delta}\right) \delta(f) \tag{254}$$

and

$$F\{R_2(\tau)\} = \frac{|\varepsilon|^2}{\Delta} \operatorname{sinc}^2(\pi f |\varepsilon|) \quad . \tag{255}$$

Since $R_3(\tau)$ is a periodic function, its Fourier transform is given by

$$F\{R_3(\tau)\} = \sum_{n=-\infty}^{\infty} c_n \, \delta\left(f - \frac{n}{\Delta}\right) \tag{256}$$

where c_n is the nth component in the Fourier series of $R_3(\tau)$. Thus,

$$c_n = \frac{1}{\Delta} \int_{-|\varepsilon|}^{|\varepsilon|} \left(\frac{|\varepsilon| - |\tau|}{\Delta}\right) e^{-jn\frac{2\pi}{\Delta}t} \, dt \quad , \tag{257}$$

and

$$F\{R_3(\tau)\} = \frac{|\varepsilon|^2}{\Delta} \sum_{n=-\infty}^{\infty} \text{sinc}^2(\pi f|\varepsilon|)\, \delta(f-n/\Delta) \quad . \tag{258}$$

Therefore, the power spectral density of the baseband signal is given by

$$G(f) = \left(1 - \frac{2|\varepsilon|}{\Delta}\right) \delta(f) + \frac{|\varepsilon|^2}{\Delta} \text{sinc}^2(\pi f|\varepsilon|) + \left(\frac{|\varepsilon|}{\Delta}\right)^2 \sum_{n=-\infty}^{\infty} \text{sinc}^2(\pi f|\varepsilon|)\, \delta(f-n/\Delta) \quad . \tag{259}$$

The desired signal component is the $\delta(f)$ term, given by

$$\left(1 - \frac{2|\varepsilon|}{\Delta}\right) + \left(\frac{|\varepsilon|}{\Delta}\right)^2 = \left(1 - \frac{|\varepsilon|}{\Delta}\right)^2 \quad . \tag{260}$$

Thus, the dc component is just $1 - \frac{|\varepsilon|}{\Delta}$, as expected.

The baseband self noise power spectral density is, therefore, given by

$$G_2(f) = \frac{|\varepsilon|^2}{\Delta} \text{sinc}^2(\pi f|\varepsilon|) + \left(\frac{|\varepsilon|}{\Delta}\right)^2 \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \text{sinc}^2(\pi f|\varepsilon|)\, \delta(f-n/\Delta) \quad . \tag{261}$$

The power spectral density of the self noise component from the product of the two identically coded biphase signals in one channel is (for $|\varepsilon| < \Delta/2$) given by

$$G_{sn_2} = \frac{P_s}{2} G_2(f-f_0) + \frac{P_s}{2} G_2(f+f_0) \quad , \tag{262}$$

where f_0 is given in Equation (245).

When the short code is involved in the calculation of the power spectral density of the baseband self noise component with the same codes, the fact that the pseudorandom sequence has finite length must b considered. In this case, the -1 pulses in the baseband signal are pseudorandom with a period corresponding to the code length, N.

If the short code is a pseudonoise code with its well defined autocorrelation function, the self noise power spectral density may easily be determined. In this case, it can be shown that the autocorrelation function of the baseband component is given by

$$R(\tau) = \begin{cases} 1 - 2\left(\frac{N+1}{N}\right)\frac{|\tau - \ell N\Delta|}{\Delta} & , \quad \ell N\Delta - |\varepsilon| < \tau < \ell N\Delta + |\varepsilon| \\ & \quad \text{for } \ell = 0, \pm 1, \pm 2, \cdots \\ 1 - \left(\frac{N+1}{N}\right)\left(\frac{|\varepsilon| - |\tau - m\Delta|}{\Delta}\right) & m\Delta - |\varepsilon| < \tau < m\Delta + |\varepsilon| \\ & \quad m = \pm 1, \pm 2, \cdots \\ & \quad m \neq \ell N \\ 1 - 2\left(\frac{N+1}{N}\right)\frac{|\varepsilon|}{\Delta} & \text{elsewhere} \end{cases} \tag{263}$$

This may be rewritten as

$$R(\tau) = R_1(\tau) + R_2(\tau) + R_3(\tau) \tag{264}$$

where

$$R_1(\tau) = 1 - 2\left(\frac{N+1}{N}\right)\frac{|\varepsilon|}{\Delta} \qquad \text{for all } \tau \quad , \tag{265}$$

$$R_2(\tau) = \begin{cases} \left(\frac{N+1}{N}\right)\frac{|\varepsilon| - |\tau - \ell N\Delta|}{\Delta} & \ell N\Delta - |\varepsilon| < \tau < \ell N\Delta + |\varepsilon| \\ & \quad \ell = 0, \pm 1, \pm 2, \cdots \\ 0 & \text{elsewhere} \end{cases} \tag{266}$$

and

$$R_3(\tau) = \begin{cases} \left(\frac{N+1}{N}\right)\frac{|\varepsilon| - |\tau - m\Delta|}{\Delta} & m\Delta - |\varepsilon| < \tau < m\Delta + |\varepsilon| \\ & \quad m = 0, \pm 1, \pm 2, \cdots \ . \\ 0 & \text{elsewhere} \end{cases} \tag{267}$$

The Fourier transform of these components is given by

$$F\{R_1(\tau)\} = \left(1 - 2\left(\frac{N+1}{N}\right)\frac{|\varepsilon|}{\Delta}\right)\delta(f) \quad , \tag{268}$$

$$F\{R_2(\tau)\} = \left(\frac{N+1}{N^2}\right)\left(\frac{|\varepsilon|}{\Delta}\right)^2 \sum_{n=-\infty}^{\infty} \mathrm{sinc}^2(\pi f|\varepsilon|)\,\delta\left(f - \frac{n}{N\Delta}\right) \quad , \tag{269}$$

and

$$F\{R_3(\tau)\} = \left(\frac{N+1}{N}\right)\left(\frac{|\varepsilon|}{\Delta}\right)^2 \sum_{n=-\infty}^{\infty} \mathrm{sinc}^2(\pi f|\varepsilon|)\,\delta\left(f - \frac{n}{\Delta}\right) \quad . \tag{270}$$

Therefore, the power spectral density of the baseband signal is given by

$$\begin{aligned} G(f) = {} & \left(1 - 2\left(\frac{N+1}{N}\right)\frac{|\varepsilon|}{\Delta}\right)\delta(f) \\ & + \left(\frac{N+1}{N^2}\right)\left(\frac{|\varepsilon|}{\Delta}\right)^2 \sum_{n=-\infty}^{\infty} \mathrm{sinc}^2(\pi f|\varepsilon|)\,\delta\left(f - \frac{n}{N\Delta}\right) \\ & + \left(\frac{N+1}{N}\right)\left(\frac{|\varepsilon|}{\Delta}\right)^2 \sum_{n=-\infty}^{\infty} \mathrm{sinc}^2(\pi f|\varepsilon|)\,\delta\left(f - \frac{n}{\Delta}\right) \quad . \end{aligned} \tag{271}$$

The desired component is the $\delta(f)$ term, given by

$$\begin{aligned} & \left(1 - 2\left(\frac{N+1}{N}\right)\frac{|\varepsilon|}{\Delta}\right) + \left(\frac{N+1}{N^2}\right)\left(\frac{|\varepsilon|}{\Delta}\right)^2 + \left(\frac{N+1}{N}\right)\left(\frac{|\varepsilon|}{\Delta}\right)^2 \\ & = \left(1 - \left(\frac{N+1}{N}\right)\frac{|\varepsilon|}{\Delta}\right)^2 \quad . \end{aligned} \tag{272}$$

The self noise baseband power spectral density is, therefore, given by

$$\begin{aligned} G_3(f) = {} & \left(\frac{N+1}{N^2\Delta}\right)\frac{|\varepsilon|}{\Delta}^2 \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \mathrm{sinc}^2(\pi f|\varepsilon|)\,\delta\left(f - \frac{n}{N\Delta}\right) \\ & + \left(\frac{N+1}{N}\right)\left(\frac{|\varepsilon|}{\Delta}\right)^2 \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \mathrm{sinc}^2(\pi f|\varepsilon|)\,\delta\left(f - \frac{n}{\Delta}\right) \quad . \end{aligned} \tag{273}$$

In comparing this result with Equation (261), note that the continuous spectrum has become a line spectrum. As N approaches infinity Equation (273) will, of course, approach Equation (261). Because in most cases N will be on the order of 100 or greater, the difference between using Equations (261) and (273) in any analysis will be negligible. Thus, the self noise power density spectrum of Equation (261) and the assumption of a truly random code will be employed in the remainder of this section.

With $\Delta/2 \leq |\varepsilon| < \Delta$, the baseband signal again has a value of +1, except for -1 pulses of width $|\varepsilon|$ which occur with a probability of about one-half at every chip interval. In this case, with the assumption of a random code, the autocorrelation function is given by

$$R(\tau) = \begin{cases} 1 - \dfrac{2|\tau|}{\Delta} & |\tau| < \Delta - |\varepsilon| \\ \dfrac{|\varepsilon| - |\tau|}{\Delta} & |\varepsilon| \leq |\tau| < \Delta - |\varepsilon| \\ 1 - \dfrac{|\varepsilon| + |\tau - m\Delta|}{\Delta} & (m-1)\Delta + |\varepsilon| \leq |\tau| < (m+1)\Delta - |\varepsilon| \\ & \text{for } m = \pm 1, \pm 2, \cdots \\ 0 & \text{elsewhere} \end{cases} . \quad (274)$$

The autocorrelation function may be rewritten as

$$R(\tau) = R_1(\tau) + R_2(\tau) \quad (275)$$

where

$$R_1(\tau) = \begin{cases} \dfrac{|\varepsilon| - |\tau|}{\Delta} & |\tau| < |\varepsilon| \\ 0 & \text{elsewhere} \end{cases} \quad (276)$$

and

$$R_2(\tau) = \begin{cases} 1 - \dfrac{|\varepsilon| + |\tau - m\Delta|}{\Delta} & (m-1)\Delta \leq |\tau| < (m+1)\Delta - |\varepsilon| \\ & \text{for } m = 0, \pm 1, \pm 2, \cdots \\ 0 & \text{elsewhere} \end{cases} . \quad (277)$$

The Fourier transform of these components is given by

$$F\{R_1(\tau)\} = \frac{|\varepsilon|^2}{\Delta} \operatorname{sinc}^2(\pi f|\varepsilon|) \tag{278}$$

and

$$F\{R_2(\tau)\} = \left(\frac{\Delta-|\varepsilon|}{\Delta}\right)^2 \sum_{n=-\infty}^{\infty} \operatorname{sinc}^2(\pi f(\Delta-|\varepsilon|))\ \delta\left(f - \frac{n}{\Delta}\right) \quad . \tag{279}$$

Therefore, the power spectral density of the baseband signal is given by

$$G(f) = \frac{|\varepsilon|^2}{\Delta} \operatorname{sinc}^2(\pi f|\varepsilon|)$$

$$+ \left(\frac{\Delta-|\varepsilon|}{\Delta}\right)^2 \sum_{n=-\infty}^{\infty} \operatorname{sinc}^2(\pi f(\Delta-|\varepsilon|))\ \delta\left(f - \frac{n}{\Delta}\right) \quad . \tag{280}$$

The desired signal component is the $\delta(f)$ term, $(\Delta-|\varepsilon|/\Delta)^2$, and, thus, the baseband power spectral density of the self noise is given by

$$G_4(f) = \frac{|\varepsilon|^2}{\Delta} \operatorname{sinc}^2(\pi f|\varepsilon|)$$

$$+ \left(\frac{\Delta-|\varepsilon|}{\Delta}\right)^2 \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \operatorname{sinc}^2(\pi f(\Delta-|\varepsilon|))\ \delta\left(f - \frac{n}{\Delta}\right) \quad . \tag{281}$$

The power spectral density of the self noise from the product of the two identically coded biphase signals is (for $\Delta/2 \leq |\varepsilon| < \Delta$)

$$G_{sn_4}(f) = \frac{P_s}{2} G_4(f-f_o) + \frac{P_s}{2} G_4(f+f_o) \quad . \tag{282}$$

When $|\varepsilon| \geq \Delta$, the baseband signal will have the same characteristics as in the case where the two mixed biphase signals have different codes. Thus, the power spectral density of the baseband self noise component from the product of two identically coded biphase signals with $|\varepsilon| \geq \Delta$ is given by Equation (244). The results obtained in this section so far are summarized in Table 3. From these results it can be seen that the self noise generated by the mixing of two different

Table 3

Power Spectral Densities for the Self Noise Components in Each Delay Lock Loop Channel

Type of Component	Power Spectral Density
Self noise component produced from the product of the bi-phase coded signal in the delay lock loop and the four-phase signal component with a different code	$G_{s_{n_1}}(f) = \frac{P_s}{2} G_1(f-f_o) + \frac{P_s}{2} G_1(f+f_o)$ where $G_1(f) = \frac{(\Delta-\lvert\varepsilon_1\rvert)^2}{\Delta} \operatorname{sinc}^2(\pi f(\Delta-\lvert\varepsilon_1\rvert)) + \frac{\lvert\varepsilon_1\rvert^2}{\Delta} \operatorname{sinc}^2(\pi f\lvert\varepsilon_1\rvert)$ where $\varepsilon_1=\varepsilon-m\Delta$, $m=0,\pm1,\cdots$ and $\lvert\varepsilon_1\rvert\leq\Delta/2$
Self noise component produced from the product of the bi-phase coded signal in the delay lock loop and the four-phase signal component with the same code	$G_{s_{n_2}}(f) = \frac{P_s}{2} G_2(f-f_o) + \frac{P_s}{2} G_2(f+f_o)$ where $G_2(f) = \frac{\lvert\varepsilon\rvert^2}{\Delta} \operatorname{sinc}^2(\pi f\lvert\varepsilon\rvert) + \left(\frac{\lvert\varepsilon\rvert}{\Delta}\right)^2 \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \operatorname{sinc}^2(\pi f\lvert\varepsilon\rvert)\, \delta\left(f-\frac{n}{\Delta}\right)$ for $\lvert\varepsilon\rvert\leq\Delta/2$ $G_2(f) = \frac{\lvert\varepsilon\rvert^2}{\Delta} \operatorname{sinc}^2(\pi f\lvert\varepsilon\rvert) + \left(\frac{\Delta-\lvert\varepsilon\rvert}{\Delta}\right)^2 \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \operatorname{sinc}^2(\pi f(\Delta-\lvert\varepsilon\rvert)) \cdot \delta\left(f-\frac{n}{\Delta}\right)$ for $\Delta/2<\lvert\varepsilon\rvert\leq\Delta$ $G_2(f) = \frac{(\Delta-\lvert\varepsilon_1\rvert)^2}{\Delta} \operatorname{sinc}^2(\pi f(\Delta-\lvert\varepsilon_1\rvert)) + \frac{\lvert\varepsilon_1\rvert^2}{\Delta} \operatorname{sinc}^2(\pi f\lvert\varepsilon_1\rvert)$ for $\lvert\varepsilon\rvert>\Delta$ where $\varepsilon_1=\varepsilon-m\Delta$, $m=\pm1,\pm2,\cdots$ and $\lvert\varepsilon_1\rvert\leq\Delta/2$

codes has a power spectral density whose bandwidth and amplitude changes with timing error. The self noise power remains constant (equal to P_S), however, and, therefore, as the magnitude of the power spectral density increases, the bandwidth decreases, and vice versa. The self noise generated by the mixing of the two identically coded signals has a power density spectrum whose magnitude increases and bandwidth decreases with increasing timing error for $|\varepsilon|<\Delta$. The power in the self noise increases with timing error in this case, from 0 to P_S for $|\varepsilon|$ equal to Δ.

In the delay lock loop, the self noise passes through a narrow bandpass filter (see Figure 25). Now, the self noise spectrum has a bandwidth greater than or equal to the code rate (see Table 3). On the other hand, the narrow bandpass filter has a bandwidth on the order of the data rate. For a large spreading ratio, that is,

$$k >> 1 \quad , \tag{283}$$

the self noise output of the narrow bandpass filter can be assumed to have a flat power spectral density with a bandwidth equal to the bandwidth of the narrow bandpass filter and a Gaussian probability density function of the amplitude [15]. The magnitude of the power spectral density out of the filter is given by the magnitude of the self noise power spectral density at f_o, $G(f_o)$. The power out of the narrow bandpass filter is then given by

$$P_{SN} = (G(f_o) + G(-f_o)) \frac{\Delta}{k} \quad . \tag{284}$$

Thus, the self noise power out of the narrow bandpass filter for the short code-long code product is given by (from Table 3)

$$P_{SN_1}(|\varepsilon_1|) = \left[\left(\frac{\Delta-|\varepsilon_1|}{\Delta}\right)^2 + \left(\frac{|\varepsilon_1|}{\Delta}\right)^2\right] \frac{P_S}{k} \tag{285}$$

or

$$P_{SN_1}(|\varepsilon_1|) = \left[1 - 2\frac{|\varepsilon_1|}{\Delta} + 2\left(\frac{|\varepsilon_1|}{\Delta}\right)^2\right] \frac{P_S}{k} \quad \text{for } |\varepsilon_1| \leq \Delta/2 \quad . \tag{286}$$

For the product of the two identically coded signals, the self noise power out of the narrow bandpass filter is given by (from Table 3)

$$P_{SN_2}(|\varepsilon|) = \begin{cases} \left(\frac{|\varepsilon|}{\Delta}\right)^2 \frac{P_S}{k} & |\varepsilon| \le \Delta \\ \left[1 - 2\frac{|\varepsilon_1|}{\Delta} + 2\left(\frac{|\varepsilon_1|}{\Delta}\right)^2\right]\frac{P_S}{k} & \text{for } |\varepsilon| > \Delta \end{cases} \quad (287)$$

where $|\varepsilon_1| = |\varepsilon| - m\Delta$, m an integer greater than 0, and $|\varepsilon_1| \le \Delta/2$.

Since the output power spectral density is flat and the output has a Gaussian probability density function, the output is the same as if white Gaussian noise was present at the input to the filter. Thus, an $S/N|_{IF}$ can be determined based on k, $|\varepsilon|$, and the received signal-to-noise ratio $S/N|_{RF}$. As this $S/N|_{IF}$ is based on $|\varepsilon|$, which may vary with time, the $S/N|_{IF}$ may also vary with time. The effect on the $S/N|_{IF}$ of the self noise present during acquisition and during tracking will now be examined.

During acquisition, ε is continuously changing and will take on a wide range of values. For $|\varepsilon| > \Delta$, in one channel of the delay lock loop, the power of the self noise is given by

$$P_{SN} = P_{SN_1}(|\varepsilon_1|) + P_{SN_2}(|\varepsilon_1|) \quad (288)$$

or, from Equations (286) and (287)

$$P_{SN} = 2\left[1 - 2\frac{|\varepsilon_1|}{\Delta} + 2\left(\frac{|\varepsilon_1|}{\Delta}\right)^2\right]\frac{P_S}{k} \quad (289)$$

where $|\varepsilon_1| = |\varepsilon| - m\Delta$, $m = \pm 1, \pm 2, \cdots$ and $|\varepsilon_1| \le \Delta/2$. Thus, P_{SN} will vary from $2P_S/k$ to P_S/k during acquisition. Since analysis with a varying noise power is difficult, the worse case value of $2P_S/k$ will be assumed in the remaining analysis. For this assumption, $S/N|_{IF}$ is given by

$$S/N|_{IF} = \frac{k}{\frac{1}{S/N|_{RF}} + \frac{2P_s}{P_s}} \quad (290)$$

or

$$S/N|_{IF} = \frac{k}{\frac{1}{S/N|_{RF}} + 2} \quad (291)$$

Thus, $S/N|_{IF}$ is upper bounded by k/2. The $S/N|_{IF}$ given above can be used with the acquisition analysis of Chapter VI.

When the delay lock loop is tracking the signal, the average value of $|\epsilon|$ is 0.5Δ in each channel. For proper operation of the long code acquisition circuitry (see Chapter VIII), the tracking jitter is usually small (less than 0.1Δ). Thus, the self noise power during tracking is approximately given by

$$P_{SN} = P_{SN_1}(0.5\Delta) + P_{SN_2}(0.5\Delta) \tag{292}$$

or from Equations (286) and (287)

$$P_{SN} = [1 - 2(.5) + 2(.5)^2]\frac{P_s}{k} + (.5)^2\frac{P_s}{k} \tag{293}$$

or

$$P_{SN} = 0.75\ P_s/k \quad . \tag{294}$$

Therefore, the $S/N|_{IF}$ is given by

$$S/N|_{IF} = \frac{k}{\frac{1}{S/N|_{RF}} + \frac{3}{4}} \quad . \tag{295}$$

The $S/N|_{IF}$ as given in Equation (295) is the correct value for each channel. However, in the analysis of tracking jitter a different $S/N|_{IF}$ will be used for the reasons explained below. In the delay lock loop, the outputs of the envelope detector in each channel are subtracted to generate the signal used in the code tracking. Therefore, any correlation between the noise in each channel will effect the tracking performance of the loop. Indeed, the self noise in each channel is correlated. The correlation of the baseband components of the self noise can be shown (see [6, pp. 538-543], for a similar analysis) to be given by

$$R_{12}(\tau) = \begin{cases} \frac{\tau}{\Delta} & 0 \le \tau < \frac{\Delta}{2} \\ (\Delta-\tau)/\Delta & \frac{\Delta}{2} \le \tau < \Delta \\ 0 & \text{elsewhere} \end{cases} \quad . \tag{296}$$

for $|\varepsilon| = 0.5\Delta$.

The power spectral density of the correlated baseband noise is then given by

$$G_{12}(f) = \frac{1}{4\Delta} \operatorname{sinc}^2(\pi f \tfrac{\Delta}{2}) \cos(2\pi f \tfrac{\Delta}{2}) \quad . \tag{297}$$

The power spectral density of the correlated noise is then given by

$$G(f) = \frac{P_s}{2} G_{12}(f-f_o) + \frac{P_s}{2} G_{12}(f-f_o) \quad . \tag{298}$$

As in the analysis before, since a narrow bandpass filter is used in each channel of the delay lock loop, the power of the correlated self noise out of the filter can be approximated by

$$P_{SN} = P_s/(4k) \quad . \tag{299}$$

The power given above is the self noise power in each channel that is cancelled when the envelope detector outputs are subtracted. Therefore, this noise power need not be considered when calculating the tracking jitter. The $S/N|_{IF}$ to be used in computing tracking jitter is, then, given by

$$S/N\Big|_{IF} = \frac{k}{\frac{1}{S/N\Big|_{RF}} + \frac{1}{2}} \tag{300}$$

Equations (291) and (300) may be compared to the $S/N|_{IF}$ when the delay lock loop is acquiring and tracking a biphase signal. Using the same method as for the four-phase signal, it can be shown for the biphase signal that during acquisition,

$$S/N\Big|_{IF} = \frac{1}{\frac{1}{S/N\Big|_{RF}} + 1} \tag{301}$$

and during tracking

$$S/N\Big|_{IF} = k\, S/N\Big|_{RF} \quad . \tag{302}$$

Thus, during tracking of the biphase signal the self noise in the delay lock loop will have a negligible effect on the $S/N|_{IF}$. However, as the $S/N|_{RF}$ decreases, the $S/N|_{IF}$ difference between the biphase and the four-phase signals in the delay lock loop will become smaller.

C. Tracking Jitter

The tracking jitter of the delay lock loop with linear envelope detection with noise present on the received signal will now be examined. To be considered first is the variance of the noise out of the loop filter. Next, the discriminator characteristic is examined when noise is present on the received signal. The tracking jitter is then determined and plotted. Finally, a comparison is made between the tracking jitter of the delay lock loop with linear envelope detection and with square law detection.

First to be considered is the variance of the noise at the output of the loop filter. Since it is desired that the tracking jitter be kept small, it can be assumed that

$$B_\ell << B_{IF} \tag{303}$$

where B_ℓ is the loop filter bandwidth. Thus, following the analysis of Chapter VI, the variance of the output of the loop filter for the ith delay lock loop channel can be approximated by (see Equation (208))

$$\sigma_i^2 = [8\, h_{11}^2 (N_o/2) + 2\, h_{02}^2\, B_{IF} (N_o/2)^2] B_\ell \tag{304}$$

where h_{11} and h_{02} are given in Equations (192) and (193). From these equations the variance can be rewritten as

$$\sigma_i^2 = \frac{B_\ell}{B_{IF}\pi} \left[2 \frac{P_{S_i}}{P_S} \, {}_2F_1\left(\frac{1}{2}; 2; -\frac{S}{N}\Big|_{IF} \frac{P_{S_i}}{P_S}\right) + \frac{1}{S/N|_{IF}} \, {}_2F_1\left(\frac{1}{2}; 1; -\frac{S}{N}\Big|_{IF} \frac{P_{S_i}}{P_S}\right) \right] P_S \quad . \tag{305}$$

Thus, the variance is dependent on P_{S_i}, the predetection signal power in the ith delay lock loop channel. From Equations (180) and (181), the predetection signal power can be seen to be a function of the timing error, ε, that is,

$$P_{S_1}(\epsilon) = \begin{cases} P_S(\epsilon/\Delta+0.5)^2 & -0.5\Delta \leq \epsilon \leq 0.5\Delta \\ P_S(1.5-\epsilon/\Delta)^2 & 0.5\Delta < \epsilon \leq 1.5\Delta \\ 0 & \text{elsewhere} \end{cases} \quad (306)$$

and

$$P_{S_2}(\epsilon) = \begin{cases} P_S(\epsilon/\Delta+1.5)^2 & -1.5\Delta \leq \epsilon \leq -0.5\Delta \\ P_S(0.5-\epsilon/\Delta)^2 & -0.5\Delta < \epsilon \leq 0.5\Delta \\ 0 & \text{elsewhere} \end{cases} . \quad (307)$$

Thus, the variance is dependent on the timing error in each channel. However, if it is assumed that the tracking jitter, σ_ϵ, is small compared to the chip duration, that is,

$$\sigma_\epsilon << \Delta \quad , \quad (308)$$

then, as discussed in Chapter VI, the timing error in each channel will have a magnitude of about $\Delta/2$. The predetection signal power in each of the delay lock loop channels can then be approximated by

$$P_{S_i}(\Delta/2) = 0.25P_S \quad . \quad (309)$$

The variance of the noise in the ith delay lock loop channel, normalized to the received signal power, P_S, is then given by

$$\frac{\sigma_i^2}{P_S} = \frac{B_\ell}{B_{IF}} \left[0.5 \, {}_1F_1^2\left(\frac{1}{2};2; -0.25\, S/N\Big|_{IF}\right) + \frac{1}{S/N\Big|_{IF}} \, {}_1F_1^2\left(\frac{1}{2};1; -0.25\, S/N\Big|_{IF}\right) \right] \quad . \quad (310)$$

Because the noise in each channel is assumed to be independent, the variance of the output of the loop filter is given by

$$\sigma_n^2 = 2\sigma_i^2 \quad . \quad (311)$$

The effect that this variance has on the tracking jitter is dependent on the discriminator characteristic, which will now be considered. The normalized discriminator characteristic for the delay lock loop with linear envelope detection without noise present at the input is given in Equation (167). With noise and without normalizing, this characteristic is given by

$$D(\varepsilon) = E\{V_{out}/\varepsilon\}_1 - E\{V_{out}/\varepsilon\}_2 \quad , \tag{312}$$

where $E\{V_{out}/\varepsilon\}_1$ and $E\{V_{out}/\varepsilon\}_2$ are the expected values of the linear envelope detector outputs for the advanced and delayed channels (1 and 2) of the delay lock loop, respectively, for a given ε. From equation (190) the expected value of the output for the ith channel is given by

$$E\{V_{out}/\varepsilon\}_i = 2\left\{\frac{(N_o/2)B_{IF}}{2\pi}\right\}^{1/2} {}_2F_1\left(-\frac{1}{2};\ 1;\ -S/N\big|_i\right) \tag{313}$$

or

$$\frac{E\{V_{out}/\varepsilon\}_i}{\sqrt{P_S}} = 2\left(\frac{1}{2\pi S/N\big|_{IF}}\right)^{1/2} {}_2F_1\left(-\frac{1}{2};\ 1;\ -S/N\big|_{IF}\ \frac{P_{S_i}(\varepsilon)}{P_S}\right) \tag{314}$$

where P_{S_i} is given in Equations (306) and (307) for i equal to 1 and 2, respectively. From Equation (314), Equation (312) can be expressed as

$$D(\varepsilon) = 2\left(\frac{1}{2\pi S/N\big|_{IF}}\right)^{1/2} \left\{ {}_2F_1\left(-\frac{1}{2};\ 1;\ -S/N\big|_{IF}\ \frac{P_{S_1}(\varepsilon)}{P_S}\right) - {}_2F_1\left(-\frac{1}{2};\ 1;\ -S/N\big|_{IF}\ \frac{P_{S_2}(\varepsilon)}{P_S}\right)\right\} \sqrt{P_S} \quad . \tag{315}$$

Thus, unlike the delay lock loop with square law detection [6, pp. 545-567], the discriminator characteristic for linear envelope detection is dependent on the signal-to-noise ratio. This is shown in Figure 30, where the discriminator characteristic given by Equation (315) is plotted for various values of $S/N|_{IF}$. It can be noted that without noise ($S/N|_{IF} = \infty$) the maximum output voltage is $2\sqrt{2P_S}/\pi$ ($=0.9003\sqrt{P_S}$), which is the output of a linear envelope detector with a sinusoidal input of magnitude $\sqrt{2P_S}$.

The timing jitter will now be determined from the noise variance and the discriminator characteristic. It can be seen that

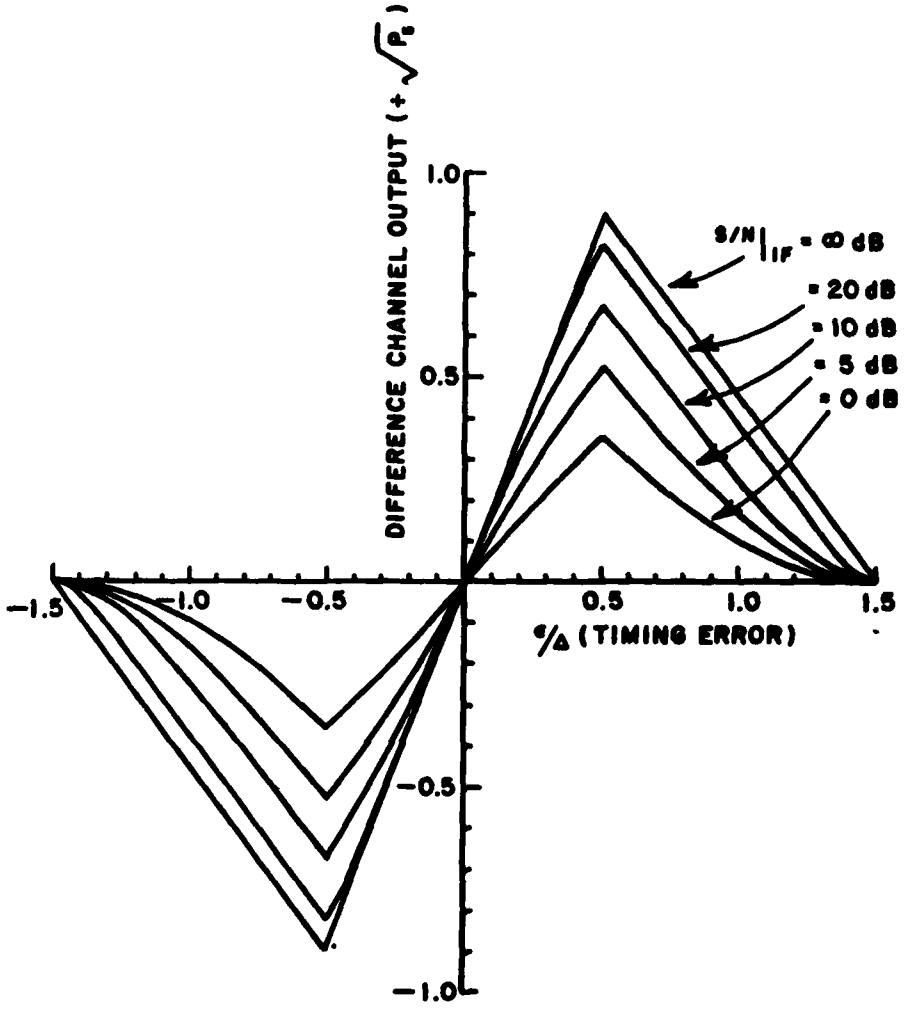


Figure 30. The discriminator characteristic for the delay lock loop with linear envelope detection for several values of $S/N|_{IF}$.

$$\frac{\partial \epsilon}{\partial V_{out}} = \frac{1}{D'(\epsilon)} \tag{316}$$

where V_{out} is the voltage out the loop filter and $D'(\epsilon)$ is the derivative of the discriminator characteristic with respect to ϵ. Thus, the standard deviation of the timing error (timing jitter) may be given by

$$\sigma_\epsilon = \frac{\sigma_n}{D'(\epsilon)} \quad . \tag{317}$$

As can be seen in Figure 30, the discriminator slope, $D'(\epsilon)$, is not constant for ϵ between $-\Delta/2$ and $\Delta/2$ when noise is present on the input. However, if again it is assumed that the tracking jitter is small, as in Equation (308), then the $D'(\epsilon)$ in Equation (316) is nearly constant and can be approximated by

$$D'(\epsilon) = D(0.1\Delta)/(0.1\Delta) \tag{318}$$

or, from Equation (315),

$$\frac{D'(\epsilon)\Delta}{\sqrt{P_S}} = 20\left(\frac{1}{2\pi S/N\big|_{IF}}\right)^{1/2} \left\{ {}_1F_1\left(-\frac{1}{2};\ 1;\ -0.36\ S/N\big|_{IF}\right) - {}_1F_1\left(-\frac{1}{2};\ 1;\ -0.16\ S/N\big|_{IF}\right)\right\} \quad . \tag{319}$$

The closed loop bandwidth, B_ℓ, of the delay lock loop will now be determined. With the loop filter as given by Equation (161), the closed loop transfer function (see [6, pp. 544-545]) has the form

$$H(p/\rho_0) = \frac{1+\sqrt{2}\ p/\rho_0}{1+\sqrt{2}p/\rho_0+(p/\rho_0)^2} \quad . \tag{320}$$

The noise bandwidth of the loop is then given by

$$B_\ell = \frac{1}{2\pi}\int_0^\infty \left|H\left(\frac{j\omega}{\rho_0}\right)\right|^2 d\omega \quad . \tag{321}$$

From Equation (320), the noise bandwidth can be evaluated to be

$$B_\ell = 0.53\ \rho_0 \quad . \tag{322}$$

Therefore, from Equations (310), (311), (317), (319) and (322), the normalized timing jitter is given by

$$\frac{\sigma_\epsilon}{\Delta} = \left(\frac{0.53\rho_0}{B_{IF}}\right)^{1/2}\left[\frac{2}{\pi}\left\{0.5\ {}_2F_1\left(\frac{1}{2};\ 2;\ -0.25\ S/N\big|_{IF}\right) + \frac{1}{S/N\big|_{IF}}\ {}_2F_1\left(\frac{1}{2};\ 1;\ -0.25\ S/N\big|_{IF}\right)\right\}\right]^{1/2}$$

$$\cdot\left[20\left(\frac{1}{2\pi S/N\big|_{IF}}\right)^{1/2}\left\{{}_1F_1\left(-\frac{1}{2};\ 1;\ -0.36\ S/N\big|_{IF}\right) - {}_1F_1\left(-\frac{1}{2};\ 1;\ -0.16\ S/N\big|_{IF}\right)\right\}\right]^{-1} . \quad (323)$$

The parameters of interest in the short code tracking are $S/N|_{IF}$, ρ_0/B_{IF}, and σ_ϵ/Δ. σ_ϵ/Δ is plotted versus $S/N|_{IF}$ for various values of ρ_0/B_{IF} in Figure 31. It should be noted from Equation (323) that the timing jitter is proportional to $\sqrt{\rho_0/B_{IF}}$. In general, ρ_0 is desired to be as large as possible (for a given σ_ϵ/Δ) so that the final acquisition time (see Chapter VI) is as small as possible. Thus, in a typical design problem (see Chapter XI) the $S/N|_{IF}$ and the maximum desired σ_ϵ/Δ (determined in Chapter VIII) will be known and a value for ρ_0 must be determined. In Figure 32, the required ρ_0/B_{IF} is shown versus $S/N|_{IF}$ for various values of σ_ϵ/Δ for use in such a problem.

A comparison can now be made between the tracking jitter for the delay lock loop with linear envelope detection and square law detection. From [6], Equation (18-99), the tracking jitter for the delay lock loop with square law detection, expressed in the notation of this report, is given by

$$\frac{\sigma_\epsilon}{\Delta} = \left(\frac{0.53\rho_0}{B_{IF}}\right)^{1/2}\left(\frac{1}{2S/N\big|_{IF}} + \frac{1}{(S/N\big|_{IF})^2}\right)^{1/2} . \quad (324)$$

Equations (323) and (324) are plotted in Figure 33, where the tracking jitter of the two delay lock loops is plotted versus $S/N|_{IF}$ for ρ_0/B_{IF} equal to 0.1. As can be seen in this figure, the tracking jitter of the delay lock loop is about the same for both types of detectors. Only for large timing jitter is there significant difference in the jitter of the two delay lock loops. However, for large timing jitter, the assumption of Equation (308) is no longer valid, and, therefore, the equation for the linear envelope detector may not be accurate. Since $\sqrt{\rho_0/B_{IF}}$ is a factor in the tracking jitter equation for both types of detectors, the performance of the two types will be nearly

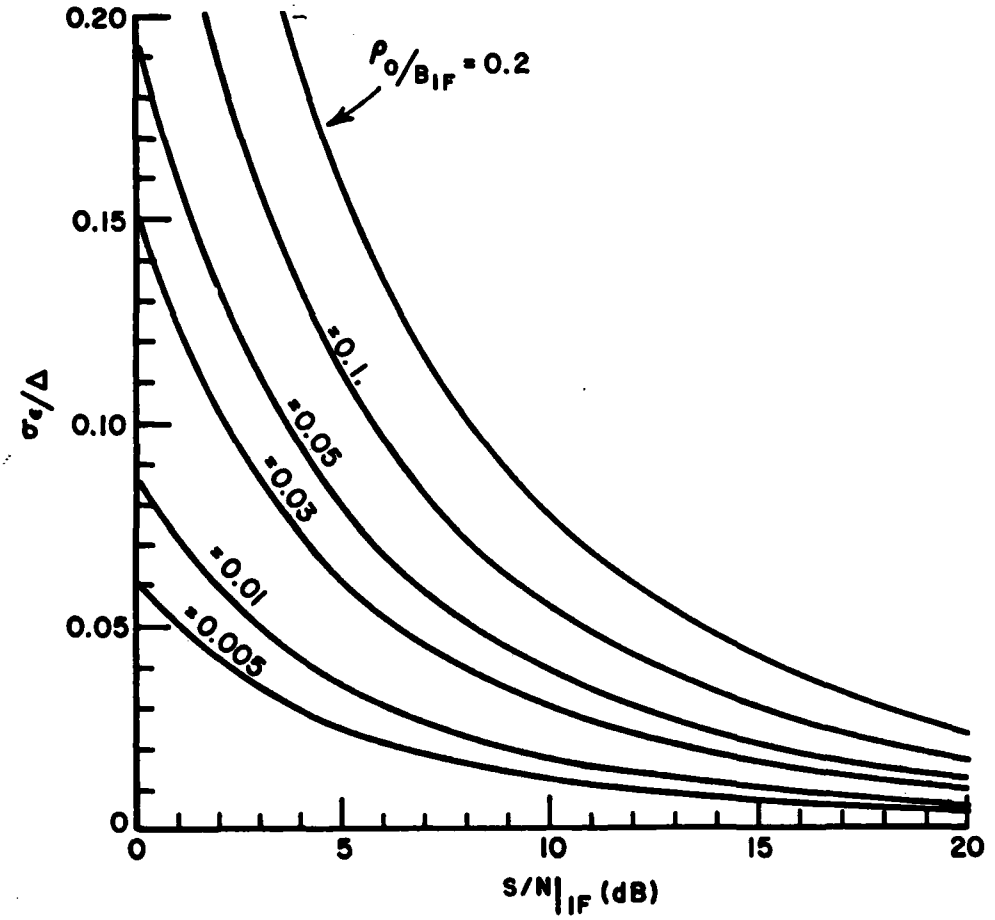


Figure 31. Normalized code timing jitter σ_ϵ/Δ, versus $S/N|_{IF}$ for various values of ρ_0/B_{IF}, for the delay lock loop with linear envelope detection.

identical for all values of ρ_0/B_{IF}. Thus, the use of linear envelope detection in the delay lock loop, so that the sum channel can be easily implemented (see Chapter VI), does not significantly change the tracking jitter that would be obtained with square law detection.

Thus, in this chapter the effect the self noise has on the signal-to-noise ratio in the delay lock loop has been determined. The signal-to-noise ratio was calculated for the delay lock loop during acquisition (Equation (291)) and during tracking (Equation (300)). The self noise was shown to set an upper limit on the signal-to-noise ratio. The tracking jitter for the delay lock loop was calculated and it given by Equation (323). The tracking jitter for the delay lock loop with

linear envelope detection was shown to be close to the tracking jitter with square law detection.

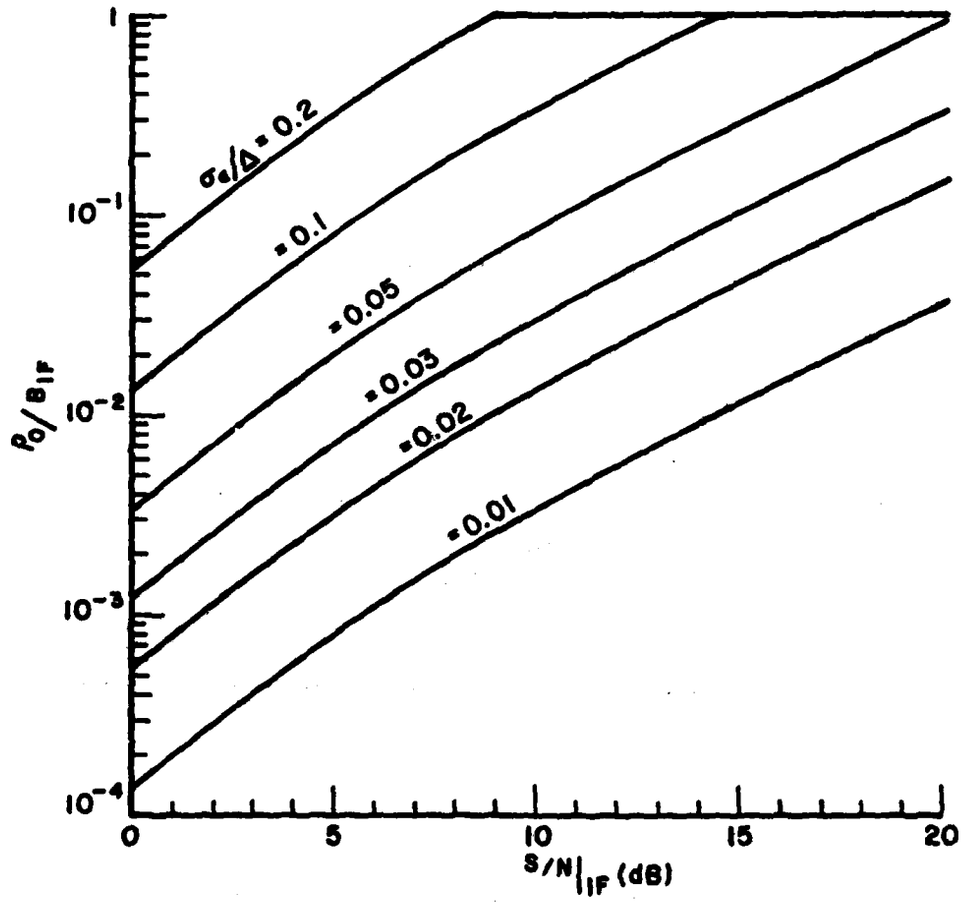


Figure 32. ρ_0/B_{IF} versus $S/N|_{IF}$ for various values of σ_ϵ/Δ for the delay lock loop with linear envelope detection.

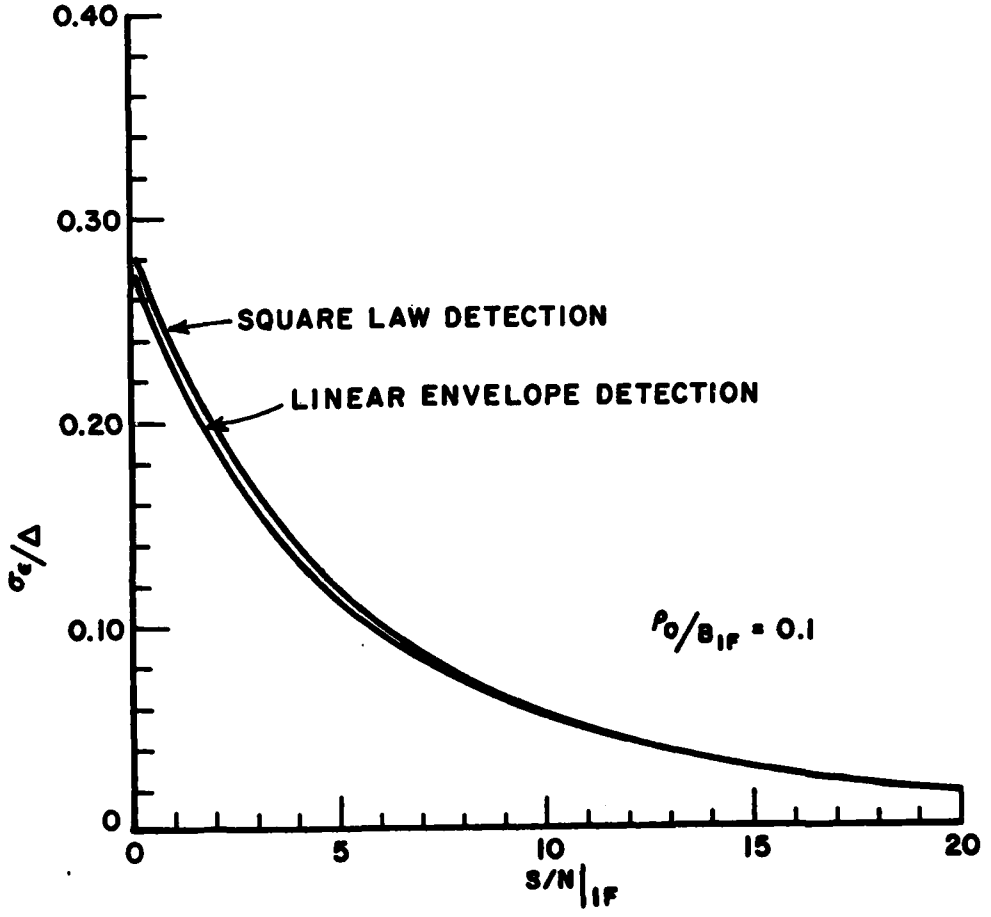


Figure 33. Comparison of the tracking jitter, σ_ϵ/Δ, versus $S/N|_{IF}$ for the delay lock loop with square law and linear envelope detection.

CHAPTER VIII

LONG CODE ACQUISITION

A. Introduction

In this chapter the long code acquisition procedure as described briefly in Chapter V is described and analyzed in detail. This chapter is divided into several sections. In the remainder of the first section the acquisition procedure is briefly described. The performance of the differential detector is the main factor in determining the performance of the acquisition procedure. In Section B the average bit error probability is calculated for ideal differential detection with noise, and the dependence of adjacent bit errors is studied. Also analyzed in Section B is the performance of the differential detector with timing jitter. In Section C an approximate model for the acquisition system is analyzed. Although this model only roughly approximates the actual acquisition system, equations can be derived which aid in understanding the performance of the actual system. The actual detection scheme is described in Section D. A model for this detection system is developed in Section E, and acquisition performance results are presented from a computer simulation using this model.

After the short code timing has been acquired, the long code timing is acquired by the receiver by the method to be described below. To obtain long code synchronization a method other than the sliding correlation method can be used because the interference and noise has been reduced in the array output at this point. Since the long code symbol transition timing is known from the delay lock loop tracking of the short code, it is only necessary to determine what the code symbols are during each symbol interval. Under these conditions a technique may be used which is known as Rapid Acquisition by Sequential Estimation[12] to acquire the timing of the long code. This method is described in detail in the next several paragraphs. Immediately after the long code timing has been acquired, the long code will then be used to generate the reference signal for the array.

In Figure 34 a block diagram of the Rapid Acquisition by Sequential Estimation (RASE) system is shown. For this technique, the code bits on the received signal are demodulated and loaded into feedback shift register. This shift register has the same length and feedback connections as that used to generate the code at the transmitter. When the shift register is fully loaded, the feedback is connected, and, if

the code bits have been demodulated correctly, the output of the shift register is synchronized with the code on the received signal. To verify synchronization, the correlation between the received signal and the generated code is determined. If the correlation value does not exceed a given threshold, the above process is repeated (i.e., the shift register is reloaded until synchronization is obtained. Using this method synchronization for a 2^n-1 bit pseudonoise code can be obtained after detection of as few as n bits. Even with a large amount of noise present with the received signal, although many loadings of the shift register will be required before the signal is acquired, the average time required for acquisition is still much less than for the sliding correlator method.

In Figure 34 the shift register is shown with two feedback taps, connected through an exclusive-or gate to the first stage of the shift register. However, more than two taps or even nonlinear logic could also be used in the feedback, if desired, to increase code security. The only requirement for this technique is that the only feedback connection must be to the first stage of the shift register.

RASE

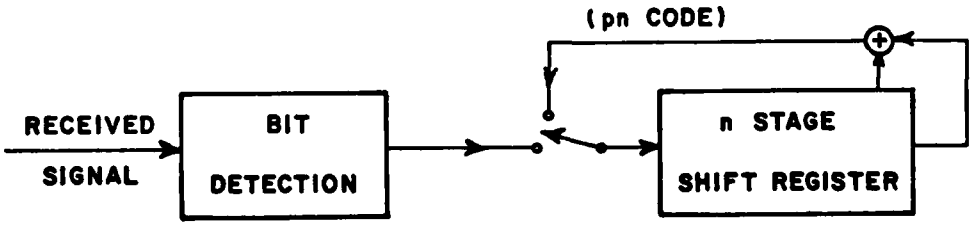


Figure 34. Rapid Acquisition by Sequential Estimation block diagram.

A block diagram of the RASE method is shown in Figure 35 for the acquisition of the long code timing. As shown in this figure the array output containing the desired signal with noise is differentially detected using the symbol transition timing information from the tracking of the short code. Information about the phase shifts present at each bit is then passed to the detection logic. Since the short code bits are known, the detection logic can determine the long code bits and in some cases also determine if errors have been made by the differential detector. If no errors are detected, the long code bits are loaded into the shift register. The shift register is then connected in the feedback mode and the output of the shift register correlated with the array output to verify code timing. If the correlation of the two signals after a given time exceeds a threshold value, the output of the

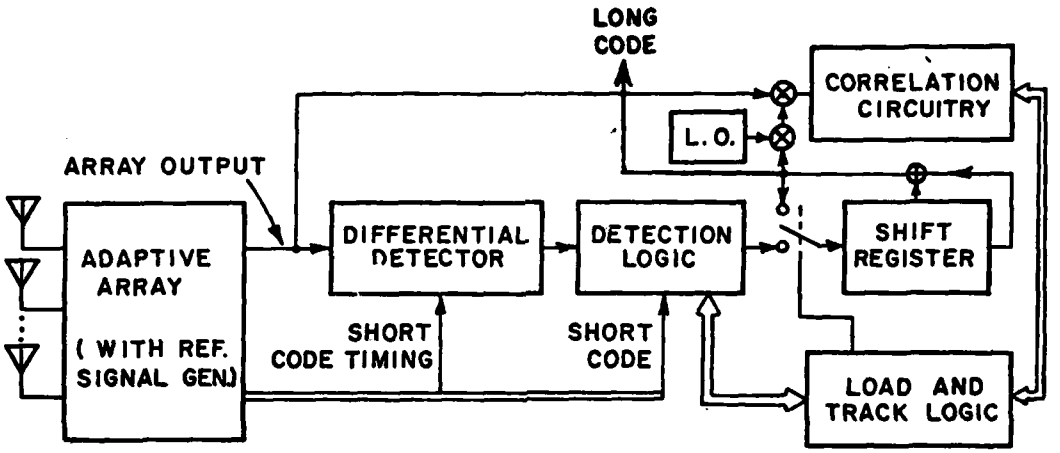


Figure 35. RASE with an adaptive array for four-phase modulated signal.

shift register is used to generate the reference signal for the array. Otherwise, the shift register is reloaded and the process repeated until code synchronization is obtained.

B. Differential Detector Performance

The acquisition procedure described in Section A uses a differential detector to determine the bits to be loaded into the shift register. Thus, the error probability of the differential detector is the main factor in determining the lockup time for the short code. In the first portion of this section the average bit error probability is computed for ideal four-phase differential detection with noise. As in any differential detector the probability of error for a given bit is dependent on whether an error occurs in detecting the previous bit. This dependency of errors is examined next. Finally, the bit error probability is computed for differential detection with timing jitter. From this timing jitter analysis the effect on differential detector performance can be studied for the bandwidth of the filters in the delay lock loop (see Chapter VI).

First to be considered is the average bit error probability for ideal four-phase differential detection with noise. In Figure 36 a block diagram is shown of the differential detector. At the differential detector input, the input signal, $z(t)$, is given by

$$z(t) = s(t) + n(t) \tag{325}$$

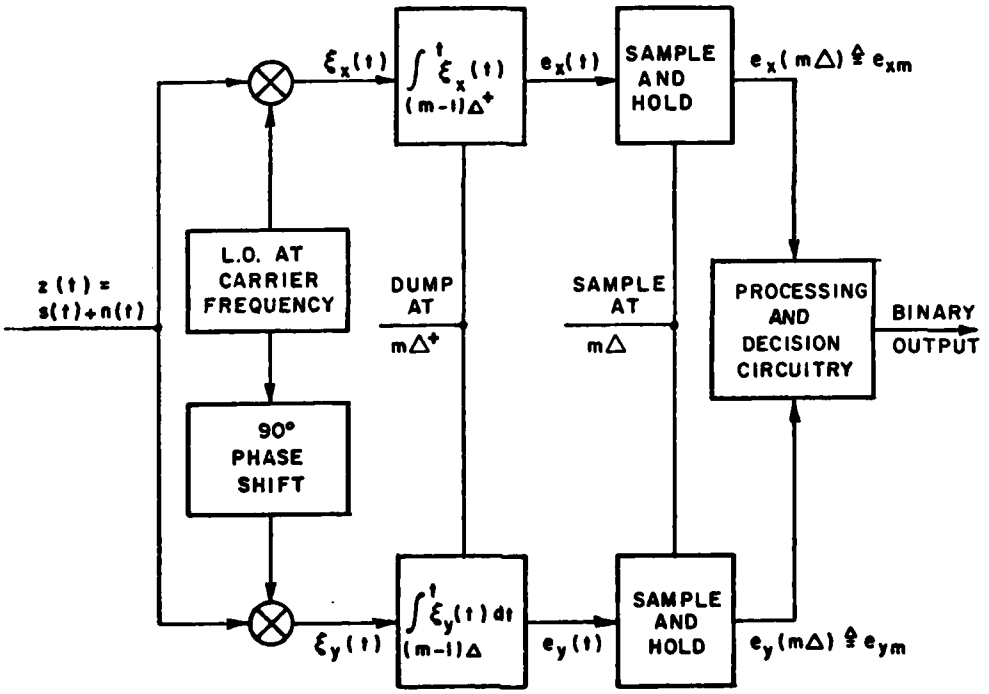


Figure 36. The differential detector.

where s(t) is the four-phase signal and n(t) is noise which is assumed to be white Gaussian noise with single sided power spectral density N_0. As seen in Figure 36, z(t) is split into orthogonal components and integrated over each chip (code symbol interval), Δ. The mth chip signal vector is, therefore, given by

$$\bar{z}_m = e_{xm}\,\bar{a}_x + e_{ym}\,\bar{a}_y \tag{326}$$

where $\bar{a}_x$ and $\bar{a}_y$ are unit vectors defining a rectangular coordinate frame.

For four-phase differential detection, in the decision circuitry the magnitude of the angle between $\bar{z}_{m-1}$ and $\bar{z}_m$, defined in the interval $[0,2\pi]$ is compared with the decision angles to determine the two received code symbols. The decision boundaries are shown in Figure 37 for ideal four-phase differential detection with equiprobable "0"'s and "1"'s in the presence of white Gaussian noise.

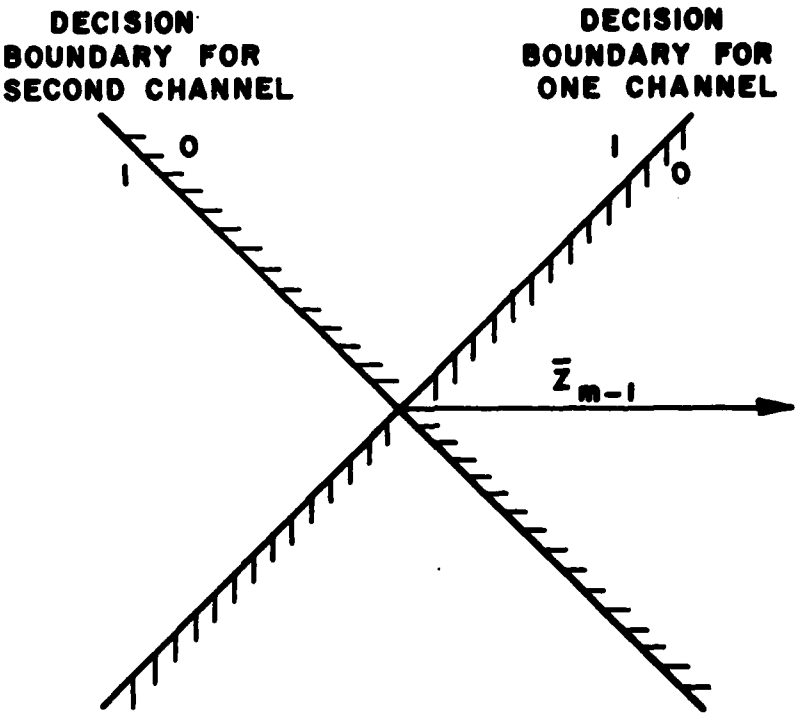


Figure 37. Decision boundaries for the mth code symbols for four-phase differential detection.

The receiver rule may be derived from Figure 37 as follows. Let θ be the angular difference between two consecutive signal vectors, that is,

$$\theta = \tan^{-1}\left(\frac{e_{ym}}{e_{xm}}\right) - \tan^{-1}\left(\frac{e_{y(m-1)}}{e_{x(m-1)}}\right) \quad . \tag{327}$$

Then the receiver rule for one channel is given by

$$\cos\theta \geq \sin\theta \qquad \text{"0" transmitted} \tag{328}$$

and

$$\cos\theta < \sin\theta \qquad \text{"1" transmitted} \quad . \tag{329}$$

Equation (328) can also be considered as meaning that the dot product of the two consecutive signal vectors is greater than or equal to the magnitude of the vectors' cross product. That is,

$$\bar{z}_{m-1} \cdot \bar{z}_m \geq (\bar{z}_{m-1} \times \bar{z}_m) \cdot \bar{a}_z \tag{330}$$

where $\bar{a}_z$ is a unit vector perpendicular to $\bar{a}_x$ and $\bar{a}_y$. Equations (326) and (330) may be combined to give the inequality

$$e_{x(m-1)}e_{xm} + e_{y(m-1)}e_{ym} \geq e_{x(m-1)}e_{ym} - e_{y(m-1)}e_{xm}. \tag{331}$$

Thus, for one channel the receiver rule may be given by

$$e_{x(m-1)}e_{xm} + e_{y(m-1)}e_{ym} - e_{x(m-1)}e_{ym} + e_{y(m-1)}e_{xm} \geq 0 \quad \text{"0" transmitted} \tag{332}$$

and

$$e_{x(m-1)}e_{xm} + e_{y(m-1)}e_{ym} - e_{x(m-1)}e_{ym} + e_{y(m-1)}e_{xm} < 0 \quad \text{"1" transmitted.} \tag{333}$$

Similarly, for the second channel, the receiver rule can be derived to be given by

$$(\bar{z}_{m-1} \times \bar{z}_m) \cdot \bar{a}_z + \bar{z}_{m-1} \cdot \bar{z}_m \geq 0 \tag{334}$$

or

$$e_{x(m-1)}e_{ym} - e_{y(m-1)}e_{xm} + e_{x(m-1)}e_{xm} + e_{y(m-1)}e_{ym} \geq 0 \quad \text{"0" transmitted,} \tag{335}$$

and

$$e_{x(m-1)}e_{ym} - e_{y(m-1)}e_{xm} + e_{x(m-1)}e_{xm} + e_{y(m-1)}e_{ym} < 0 \quad \text{"1" transmitted .} \tag{336}$$

Equations (332) through (336) are in the form that they can be easily implemented in the processing and decision circuitry of the differential detector.

From Figure 37 it can be seen that the decision boundary for a given channel with four-phase differential detection is the decision boundary for biphase differential detection rotated 45 degrees. Thus, ideal differential detection of one channel of a four-phase signal has the same average bit error probability as differential detection of a

biphase signal with a 45 degree error in signal vector angle. The bit error probability for biphase differential detection with signal vector angle error has been determined in [20]. From [20], Equation (74), the bit error probability with a 45 degree angular error, and, thus, the error probability for one channel in a four-phase signal is given by

$$P_{E_1} = \frac{1}{\pi}\int_0^{\pi/2} \exp\frac{E_\Delta/N_0}{2\cos^2\theta+\sin^2\theta}\, d\theta$$

$$+ \frac{1}{\pi}\sqrt{\frac{E_\Delta}{2N_0}}\int_{-\pi/2}^{\pi/2}\int_{\sqrt{2E_\Delta/N_0}\cos(x+\pi/4)}^{\sqrt{E_\Delta/N_0}\cos x}\exp(-u^2/2)du$$

$$\cdot \exp[-E_\Delta/N_0(\sin^2 x)]\cos x\, dx \quad , \tag{337}$$

where E_Δ is the signal energy per chip interval. It should be noted that E_Δ is twice the energy per code symbol because the signal energy is divided between the two code symbols in each chip interval.

Evaluation of Equation (337) was done with the computer program used in [20]. Results are plotted in Figure 38. There are several other equations which can be used to compute the probability of error in a single channel with four-phase differential detection, including [21], Equations (54) and (55) which is derived in [22]. These equations give results similar to those of Figure 38.

The probability of at least one error in detecting both channels will now be considered. If the error probability for each of the two channels was independent of the other channel, then the probability of at least one error in each chip interval would be given by

$$P_{E_2} = 2P_{E_1} - P_{E_1}^2 \quad . \tag{338}$$

With differential detection, the error probabilities are not independent, however, although Equation (338) gives results within 3 percent of the actual value for E_Δ/N_0 between 1 and 4. The actual value of the probability of at least one error in a given chip interval is given by ([21], Equation (71), derived in [22])

$$P_{E_3} = \int_{\pi/4}^{\pi}\frac{1}{\pi}\int_0^{\pi/2}\sin x\,[1 + (E_\Delta/N_0)(1 + \cos y \sin x)]$$

$$\cdot \exp(-(E_\Delta/N_0)(1 - \cos y \sin x))\, dx\, dy \quad . \tag{339}$$

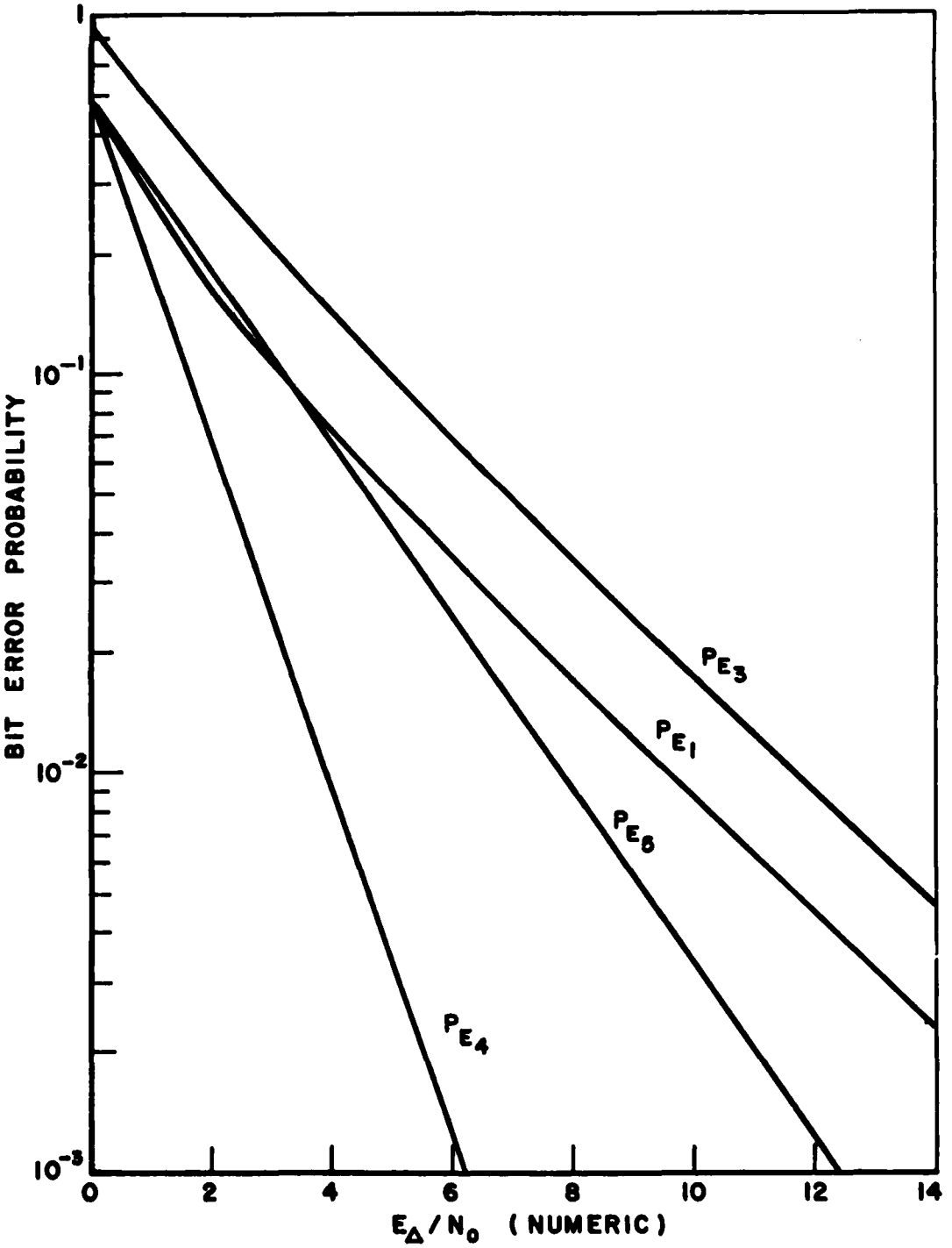


Figure 38. Average bit error probability versus E_Δ/N_0 for differential detection.

Evaluation of Equation (339) was performed numerically using Simpson's 1/3 rule with 100 points for each integral. Results are plotted in Figure 38. It should be noted that these results agree with the tabulated values of [23]. Two other curves are plotted in Figure 38. These include the bit error probability for biphase differential detection, which is given by

$$P_{E_4} = \frac{1}{2} \exp[-E_\Delta/N_0] \quad . \tag{340}$$

For comparison purposes, the curve given by

$$P_{E_5} = \frac{1}{2} \exp[-E_\Delta/2N_0] \tag{341}$$

is also plotted.

As seen in Figure 38, the probability of error in one channel is less than 1/2 $\exp[E_\Delta/2N_0]$ for E_Δ/N_0 between 0 and 4. Thus, for a given energy per code symbol (rather than energy per chip) to noise density ratio four-phase differential detection has a lower bit error probability than biphase differential detection for small E_Δ/N_0. As shown in Section E, this range of E_Δ/N_0 values is the region of interest in the long code acquisition method.

In differential detection the phase difference between two consecutive signal vectors is used to determine the code symbols. Thus, the error probability for a given chip interval is dependent upon whether there were errors during the previous chip interval. Because of this error dependence the probability of loading n bits without errors into the shift register during the long code acquisition will be different than just the nth power of the average bit error probability. This error dependence will now be examined.

For biphase differential detection the dependence of error probabilities has been studied in [24]. With biphase differential detection there are four combinations of errors (or conditional error probability cases) to consider: (1) two errors, (2) no errors, (3) an error followed by no error, and (4) no error followed by an error. For four-phase differential detection the number of cases is increased to 16. That is, there are four possible error combinations in one chip interval (conditions) and four possible error combinations in the next chip interval (resulting errors).

To calculate the conditional error probabilities it is first necessary to consider the probability density function of the phase error due to noise of the ith chip interval signal vector in the

differential detector, ψ_i. For white, Gaussian noise this probability density function is given by [25]

$$p(\psi/(E_\Delta/N_o)) = \frac{1}{2\pi}\exp\left[-\frac{E_\Delta}{N_o}\right] + \frac{1}{\sqrt{2\pi}}\exp\left[-\frac{E_\Delta}{N_o}\sin^2\psi\right] \cdot \sqrt{\frac{2E_\Delta}{N_o}}\cos\psi\left[\frac{1}{2} + Q(\psi, E_\Delta/N_o)\right] \quad (342)$$

where

$$Q(\psi, E_\Delta/N_o) = \frac{1}{\sqrt{2\pi}}\int_0^{\sqrt{2E_\Delta/N_o}\cos\psi}\exp[-u^2/2]\,du \quad . \quad (343)$$

As an example to show how the error probabilties may be calculated, the case will be considered of two consecutive errors in one channel and none in the other. Let $\underline{e}_{i_\ell}$ denote an error in the ℓth code symbol of the ith chip interval and $\bar{e}_{i_\ell}$ denote no error. Then the probability of an error in one channel given an error in the same channel in the previous chip interval, with no errors in the other channel is given by

$$P_r(e_{i_1}\bar{e}_{i_2}/e_{(i-1)_1}\bar{e}_{(i-1)_2}) = \frac{P_r(e_{i_1}\bar{e}_{i_2}e_{(i-1)_1}\bar{e}_{(i-1)_2})}{P_r(e_{(i-1)_1}\bar{e}_{(i-1)_2})} \quad . \quad (344)$$

The denominator in Equation (344) may be seen from the decision boundaries shown in Figure 37 to be given by

$$P_r(e_{(i-1)_1}\bar{e}_{(i-1)_2}) = P_r\left(\frac{\pi}{4} < \psi_{(i-1)} - \psi_{(i-2)} \leq \frac{3\pi}{4}\right) \quad (345)$$

or

$$P_r(e_{(i-1)_1}\bar{e}_{(i-1)_2}) = P_r\left(\frac{\pi}{4} + \psi_{(i-2)} < \psi_{(i-1)} \leq \frac{3\pi}{4} + \psi_{(i-2)}\right) \quad . \quad (346)$$

From Equation (342), the above equation may be written as

$$P_r(e_{(i-1)_1}\bar{e}_{(i-1)_2}) = \int_{-\pi}^{\pi}\int_{\pi/4+\psi_{(i-2)}}^{3\pi/4+\psi_{(i-2)}} p(\psi_{(i-1)}/(E_\Delta/N_o))$$

$$\cdot\, p(\psi_{(i-2)}/(E_\Delta/N_o))d\psi_{(i-2)}d\psi_{(i-1)} \qquad (347)$$

The numerator of the right-hand side of Equation (344) may be seen from Figure 37 to be given by

$$P_r(e_{i_1}\bar{e}_{i_2}e_{(i-1)}\bar{e}_{(i-1)_2})$$

$$= P_r\left(\frac{\pi}{4} \le \psi_{(i-1)} - \psi_{(i-2)} < \frac{3\pi}{4}\,,\; -\frac{3\pi}{4} \le \psi_i - \psi_{(i-1)} < -\frac{\pi}{4}\right) \qquad (348)$$

or

$$P_r(e_{i_1}\bar{e}_{i_2}e_{(i-1)_1}\bar{e}_{(i-1)_2})$$

$$= P_r\Big(\frac{\pi}{4} + \psi_{(i-2)} \le \psi_{(i-1)} < \frac{3\pi}{4} + \psi_{(i-1)},$$

$$\frac{-3\pi}{4} + \psi_{(i-1)} \le \psi_i < \frac{-\pi}{4} + \psi_{(i-1)}\Big) \qquad (349)$$

and, thus, from Equation (342)

$$P_r(e_{i_1}\bar{e}_{i_2}e_{(i-1)_1}\bar{e}_{(i-1)_2}) = \int_{-\pi}^{\pi}\int_{\pi/4+\psi_{(i-2)}}^{3\pi/4+\psi_{(i-2)}}\int_{-3\pi/4+\psi_{(i-1)}}^{-\pi/4+\psi_{(i-1)}}$$

$$p(\psi_i/(E_\Delta/N_o))p(\psi_{(i-1)}/(E_\Delta/N_o))$$

$$p(\psi_{(i-2)}/(E_\Delta/N_o))\; d\psi_i d\psi_{(i-1)}d\psi_{(i-2)} \cdot \qquad (350)$$

Evaluation of Equations (347) and (350) was done numerically using Simpson's 1/3 rule with 24 points for each integral. $P_r(e_{i_1}\ \bar{e}_{i_2}/e_{(i-1)_1}\ \bar{e}_{(i-1)_2})$ was then calculated from Equation (344).

Using the method described above the conditional error probabilities were determined for all cases. In Table 4 the limits on the integrals in Equation (350) are shown for all cases. The conditional error probabilities are plotted in Figures 39 through 41. As can be seen from these figures the conditional error probabilities vary widely about the average from case to case. Thus, the conditional error probabilities must be taken into account when analyzing the long code acquisition time.

The next topic to be considered is the effect that bit timing error has on the differential detector bit error probability. As discussed in Chapters VI and VII, the bandwidth of the delay lock loop filter and the signal-to-noise ratio determine the jitter in the code timing. The bandwidth of this filter is usually desired to be as large as possible to increase the short code acquisition probability. Thus, the timing jitter will usually be made as large as is possible without seriously affecting the performance of the differential detector.

In the following analysis the effect is studied of bit timing jitter on the average bit error probability for a single channel in a four-phase signal. Although analysis could also be performed for the effect of timing jitter on the conditional error probabilities and the average probability of an error in at least one channel, this would require an extremely large number of cases to be studied and make the job of determining the filter bandwidth very complex. Thus, only this one case has been considered.

To determine the effect of timing jitter on the differential detector, the effect of timing jitter on the signal vectors will be considered first. Referring to Figure 36, with a timing error, ε, the outputs of the sample-and-holds in the differential detector are given by

$$e_x(m\Delta+\varepsilon) = \int_{(m-1)\Delta+\varepsilon}^{m\Delta+\varepsilon} \xi_x(t)dt \qquad (351)$$

and

$$e_x(m\Delta+\varepsilon) = \int_{(m-1)\Delta+\varepsilon}^{m\Delta+\varepsilon} \xi_y(t)dt \quad . \qquad (352)$$

Table 4

Integral Limits for Equation (339) for All Conditional Error Probability Cases

Conditional Error Probability	Limits for Integral Over			
	$\psi_{(i-1)}$		ψ_i	
	Lower $(+\psi_{(i-2)})$	Upper $(+\psi_{(i-2)})$	Lower $(+\psi_{(i-1)})$	Upper $(+\psi_{(i-1)})$
$P_r(e_{i_1} e_{i_2} / e_{(i-1)_1} e_{(i-1)_2})$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$
$P_r(e_{i_1} e_{i_2} / \bar{e}_{(i-1)_1} e_{(i-1)_2})$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$
$P_r(e_{i_1} e_{i_2} / e_{(i-1)_1} \bar{e}_{(i-1)_2})$	$-\frac{3\pi}{4}$	$-\frac{\pi}{4}$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$
$P_r(e_{i_1} e_{i_2} / \bar{e}_{(i-1)_1} \bar{e}_{(i-1)_2})$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$
$P_r(\bar{e}_{i_1} e_{i_2} / e_{(i-1)_1} e_{(i-1)_2})$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$	$-\frac{3\pi}{4}$	$-\frac{\pi}{4}$
$P_r(\bar{e}_{i_1} e_{i_2} / e_{(i-1)_1} \bar{e}_{(i-1)_2})$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$	$-\frac{3\pi}{4}$	$-\frac{\pi}{4}$
$P_r(\bar{e}_{i_1} e_{i_2} / \bar{e}_{(i-1)_1} e_{(i-1)_2})$	$-\frac{3\pi}{4}$	$-\frac{\pi}{4}$	$-\frac{3\pi}{4}$	$-\frac{\pi}{4}$
$P_r(\bar{e}_{i_1} e_{i_2} / \bar{e}_{(i-1)_1} \bar{e}_{(i-1)_2})$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$	$-\frac{3\pi}{4}$	$-\frac{\pi}{4}$
$P_r(e_{i_1} \bar{e}_{i_2} / e_{(i-1)_1} e_{(i-1)_2})$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$
$P_r(e_{i_1} \bar{e}_{i_2} / e_{(i-1)_1} \bar{e}_{(i-1)_2})$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$
$P_r(e_{i_1} \bar{e}_{i_2} / \bar{e}_{(i-1)_1} e_{(i-1)_2})$	$-\frac{3\pi}{4}$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$
$P_r(e_{i_1} \bar{e}_{i_2} / \bar{e}_{(i-1)_1} \bar{e}_{(i-1)_2})$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$
$P_r(\bar{e}_{i_1} \bar{e}_{i_2} / e_{(i-1)_1} e_{(i-1)_2})$	$-\frac{\pi}{4}$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$
$P_r(\bar{e}_{i_1} \bar{e}_{i_2} / e_{(i-1)_1} \bar{e}_{(i-1)_2})$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$
$P_r(\bar{e}_{i_1} \bar{e}_{i_2} / \bar{e}_{(i-1)_1} e_{(i-1)_2})$	$-\frac{3\pi}{4}$	$-\frac{\pi}{4}$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$
$P_r(\bar{e}_{i_1} \bar{e}_{i_2} / \bar{e}_{(i-1)_1} \bar{e}_{(i-1)_2})$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$

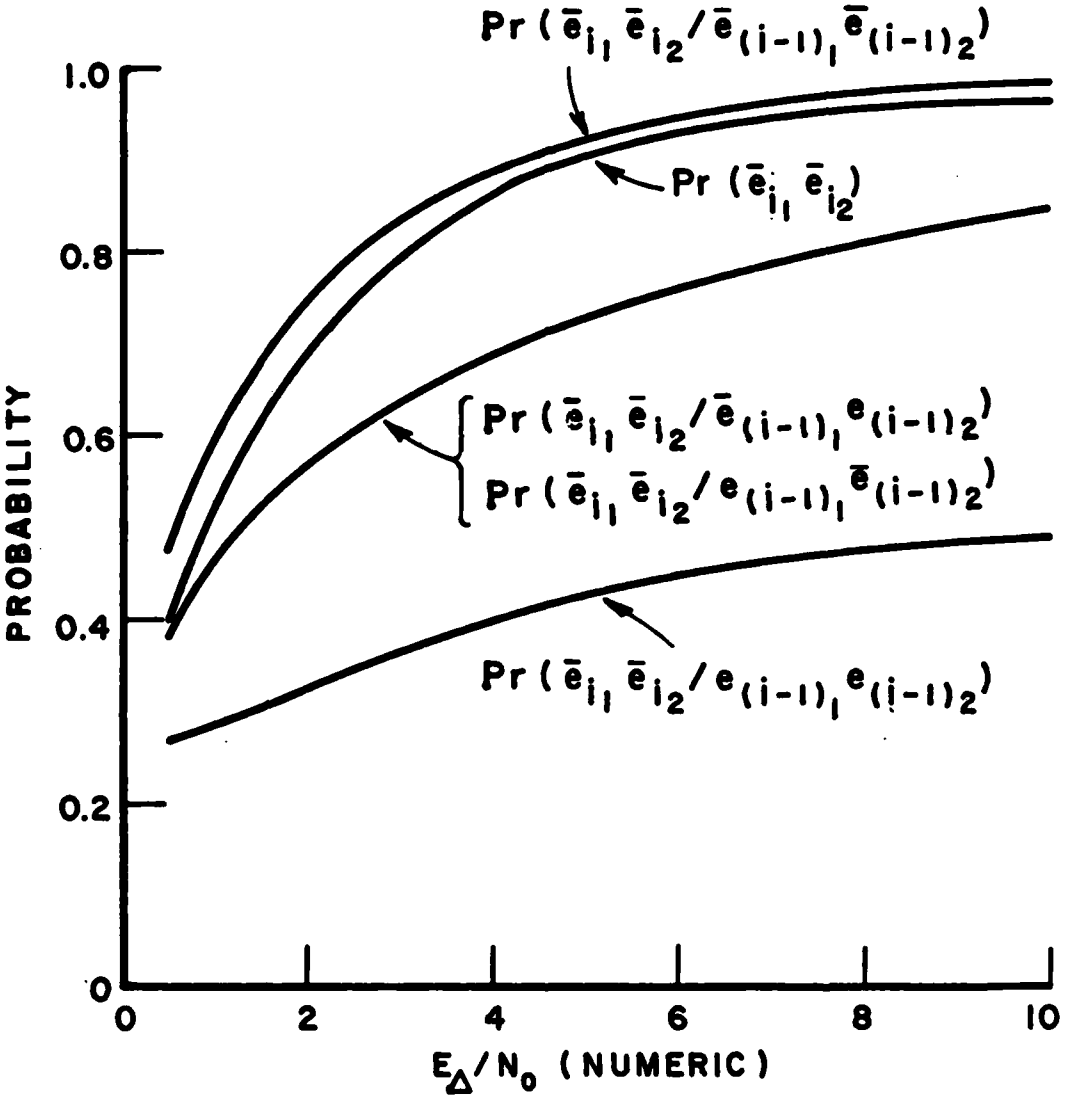


Figure 39. Conditional error probabilities for no errors versus E_Δ/N_0.

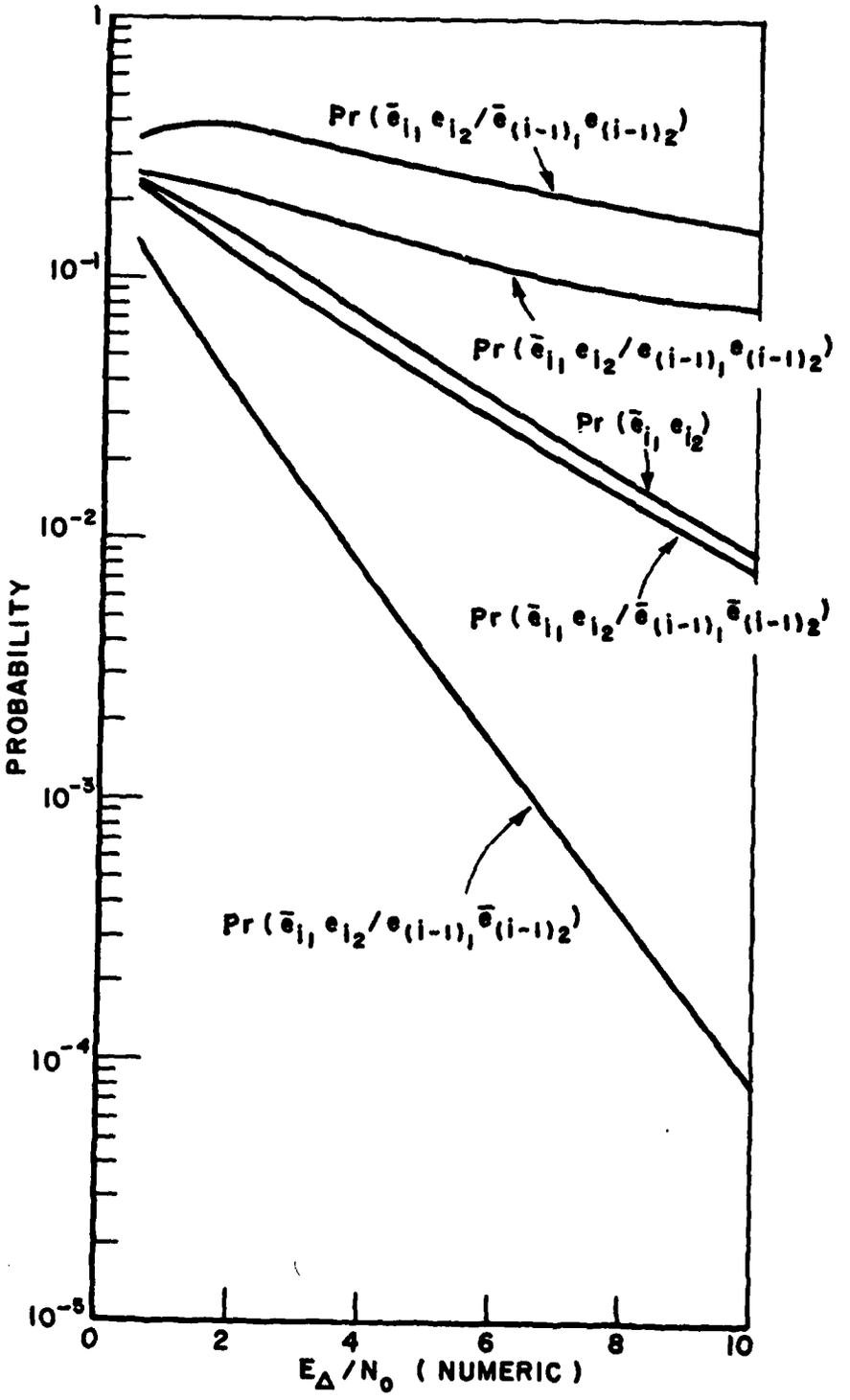


Figure 40. Conditional error probabilities for a single error versus E_Δ/N_0.

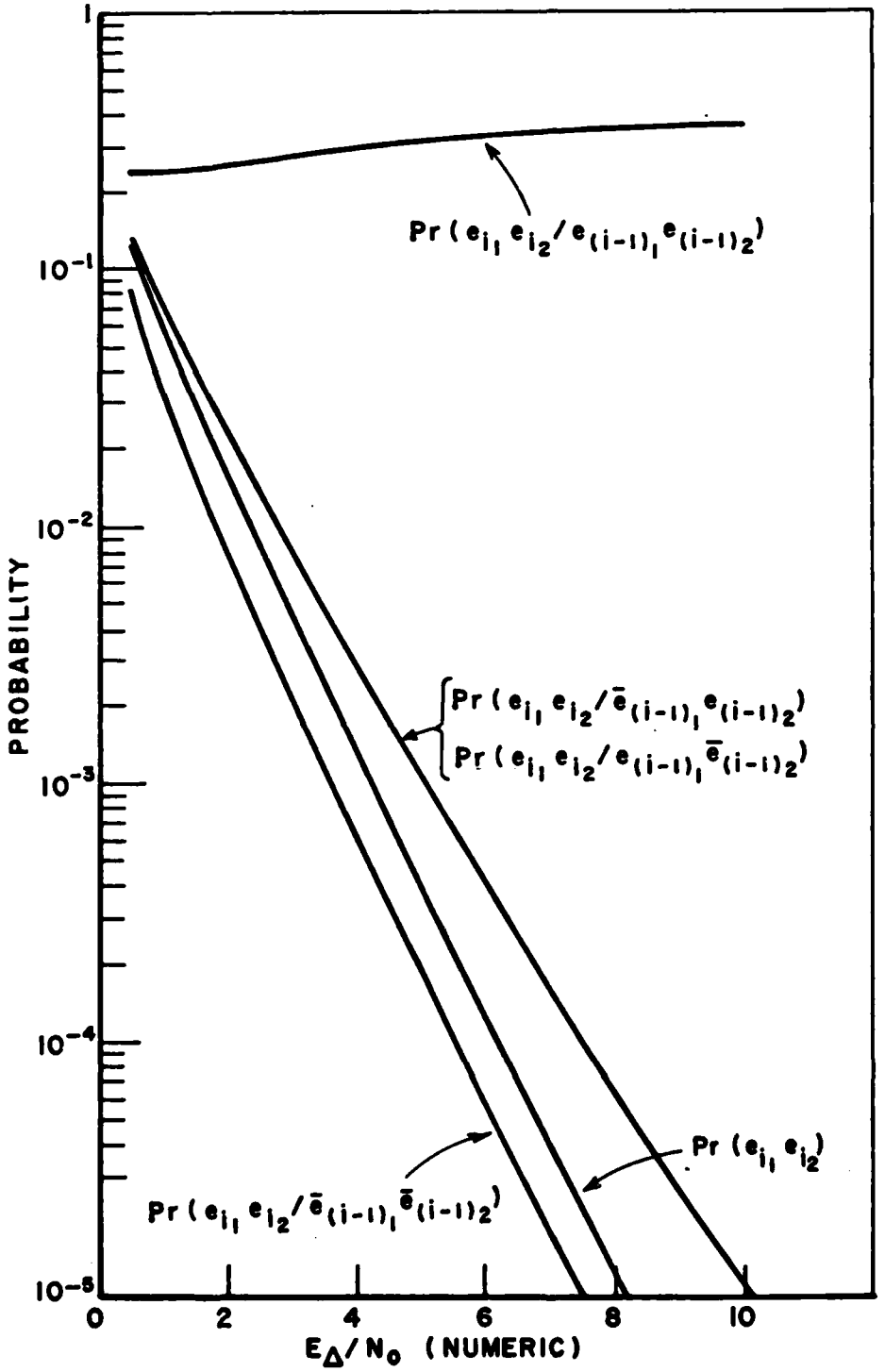


Figure 41. Conditional error probabilities for two errors versus E_Δ/N_0.

The parameters of interest for the signal vectors are the magnitude of two consecutive signal vectors L_1 and L_2, and the error in the angle between them due to timing error, $\Delta\theta$. With timing error there are 16 cases to consider. The signal vector magnitudes and angular error for these cases are listed in Table 5.

The average probability of error with timing error may be calculated by averaging the probability of error for each of the 16 cases. The probability of error for the ith case with a given timing error is given by (from [20])

$$K(L_1, L_2\ \Delta\phi_\varepsilon/\varepsilon, \text{ case i}) =$$

$$\frac{1}{\pi}\int_0^{\pi/2} \exp\left[-\frac{L_1^2L_2^2\cos^2\Delta\phi_\varepsilon\ /N_0}{L_1^2\cos^2\theta+L_2^2\cos^2\Delta\phi_\varepsilon\sin^2\theta}\right] d\theta$$

$$+\frac{L_1}{\pi\sqrt{2N_0}}\int_{-\pi/2}^{\pi/2}\left\{\int_{L_2\sqrt{2/N_0}\cos(x+\Delta\phi_\varepsilon)}^{L_2\sqrt{2/N_0}\cos x\cos\Delta\phi_\varepsilon} \exp[-u^2/2]du\right\}$$

$$\cdot \exp\left[-\frac{L_1^2\sin^2 x}{N_0}\right]\cos x\ dx \quad , \tag{353}$$

where

$$\Delta\phi_\varepsilon = \Delta\theta + \pi/4 \tag{354}$$

and L_1, L_2, $\Delta\theta$ are given in Table 5. As discussed previously $\pi/4$ has been added to $\Delta\theta$ in Equation (354) to make the equation in [20] for bi-phase differential detection correspond to that for four-phase differential detection.

As stated before (see Chapter VI), the timing error, ε, is assumed to have a Guassian distribution, which may be given by

$$p(\varepsilon) = \frac{1}{\sqrt{2\pi}\sigma_\varepsilon}\exp\left[-\frac{\varepsilon^2}{2\sigma_\varepsilon^2}\right] \tag{355}$$

where σ_ε is the standard deviation of the timing jitter. Thus, the probability of error for a given case is given by

Table 5

Signal Vector Magnitudes and Angular Error with Timing Error for All Cases

Case	Signal vector magnitude*		Angular error
	L_1	L_2	$\Delta\theta$
1	1	1	0
2	1	$(1-\varepsilon)^2+\varepsilon^2$	$\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
3	1	$1-2\varepsilon$	0
4	1	$(1-\varepsilon)^2+\varepsilon^2$	$-\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
5	$(1-\varepsilon)^2+\varepsilon^2$	1	$-2\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
6	$(1-\varepsilon)^2+\varepsilon^2$	$(1-\varepsilon)^2+\varepsilon^2$	$-\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
7	$(1-\varepsilon)^2+\varepsilon^2$	$1-2\varepsilon$	0
8	$(1-\varepsilon)^2+\varepsilon^2$	$(1-\varepsilon)^2+\varepsilon^2$	$-\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
9	$1-2\varepsilon$	1	0
10	$1-2\varepsilon$	$(1-\varepsilon)^2+\varepsilon^2$	$-\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
11	$1-2\varepsilon$	$1-2\varepsilon$	0
12	$1-2\varepsilon$	$(1-\varepsilon)^2+\varepsilon^2$	$\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
13	$(1-\varepsilon)^2+\varepsilon^2$	1	$2\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
14	$(1-\varepsilon)^2+\varepsilon^2$	$(1-\varepsilon)^2+\varepsilon^2$	$\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$
15	$(1-\varepsilon)^2+\varepsilon^2$	$1-2\varepsilon$	0
16	$(1-\varepsilon)^2+\varepsilon^2$	$(1-\varepsilon)^2+\varepsilon^2$	$\tan^{-1}\frac{\varepsilon}{1-\varepsilon}$

*Normalized to 1 without timing error.

$$P_E(\text{case i}) = \int_\varepsilon K(L_1, L_2, \Delta\phi_\varepsilon/\varepsilon, \text{ case i}) p(\varepsilon) d\varepsilon \ . \qquad (356)$$

The average probability of error for all cases is then given by

$$P_E = \frac{1}{16} \sum_{i=1}^{16} \int_\varepsilon K(L_1, L_2, \Delta\phi_\varepsilon/\varepsilon, \text{ case i}) \cdot p(\varepsilon) d\varepsilon \ . \qquad (357)$$

Equation (357) has been analyzed using numerical techniques. Simpson's one-third rule was employed in evaluating all integrals. The number of points for each integral was 4 for u (Equation (353)), 40 for x (Equation (353)), 30 for θ (Equation (353)), and 150 for ε (Equation (355)). The results of the computer analysis are shown in Figure 42, where the average probability of error in a single channel is plotted versus E_Δ/N_0 for various values of timing jitter. Figure 42 can be used to determine the increase in E_Δ/N_0 required with timing jitter to obtain a given error performance. Thus, the effect of different delay lock loop filter bandwidths can be determined on the differential detector performance. A design example using this information is presented in Chapter XI.

C. Analysis of an Approximate Long Code Acquisition Model

In this section a simplified model of the long code acquisition scheme is analyzed. For this model several assumptions are made for the acquisition system so that the system can be studied theoretically. Although these assumptions are not true for the actual system, with these assumptions equations can be derived which give a rough idea of the actual system performance. The parameters being studied in this section are the long code acquisition time and the probability of long code timing acquisition in a given time as a function of E_Δ/N_0 and long code shift register length.

The following assumptions for the long code acquisition system model have been made in this section. It must be stressed that these assumptions are not true for the actual system and will only be used in this section. The assumptions are:

(a) The long code can be differentially detected by itself (without the short code plus data).

(b) The bit error probability for each code symbol is independent of other symbols.

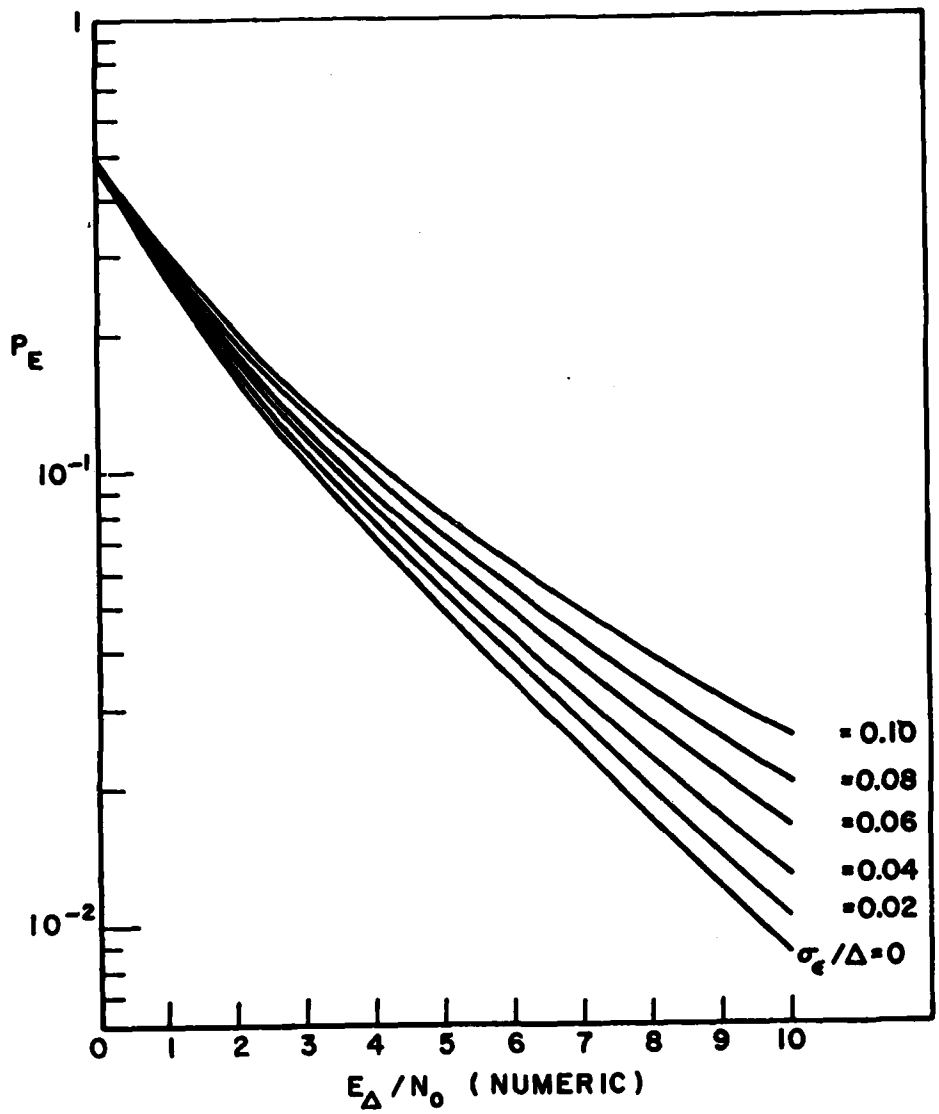


Figure 42. The average probability of a symbol error in four-phase differential detection versus E_Δ/N_0 for various values of timing jitter.

(c) The bit error probability is given by

$$P_E = \frac{1}{2} \exp[-E_\Delta/2N_0] \quad . \tag{358}$$

Although in the actual system the long code cannot be differentially detected by itself, assumption (a) is still fairly reasonable since when detecting the four-phase signal, the short code is already known. Assumption (b) was shown to be wrong in Section B. However, this assumption allows for the derivation of equations in this part which are still reasonably accurate. The approximation to the average bit error probability in assumption (c) was discussed in Section B, and shown in Figure 38 to be fairly accurate over a range of E_Δ/N_0 values from 1 to 4, which is the range considered in this part.

This simplified model will now be analyzed to determine the average long code acquisition time and the probability of acquisition in a given time. As described in Section A the long code acquisition scheme involves the loading of a shift register with the detected code symbols followed by the correlation of the output of the shift register with the received signal. With the assumptions described previously, the probability of fully loading an n stage shift register with error free code symbols is given by

$$P_n = (1-P_E)^n \quad , \tag{359}$$

where P_E is given in Equation (358). The trials of fully loading the shift register are independent Bernoulli trials. Thus, the number of trials required for an error free loading (i.e., for acquisition) has a geometrical distribution. The probability of success of the xth trial is then given by

$$P_r(x=X) = P_n(1-P_n)^{X-1} \quad , \tag{360}$$

and the average number of trials required is the reciprocal of P_n.

For each loading of the shift register, the output of the shift register is correlated with the received signal for a period of time which will be referred to as the correlation time. The correlation time is discussed in Chapter IX. As stated in this section, the correlation time, T_{corr}, will, in general, be some given multiple, M, of the number of stages in the shift register for a given system, i.e.,

$$T_{corr} = Mn\ \Delta \quad . \tag{361}$$

Thus, the average acquisition time is given by

$$T_{acq} = \frac{Mn\ \Delta}{(1-P_E)^n} \tag{362}$$

For the sliding correlation method of acquisition (used for the short code), the average acquisition time is given by (see Chapter VI)

$$T_{acq} = 2^{n-1} T_{corr} \quad . \tag{363}$$

Thus, for P_E equal to one-half (random guessing of the code timing) the average lockup time for this model is twice that for the sliding correlation method. However, as P_E decreases, the lockup time with this model will become much less.

Equations (362) and (358) can be combined to obtain the average acquisition time, which is given by

$$T_{acq} = M \frac{n \Delta}{(1 - \frac{1}{2} \exp[-E_\Delta/2N_0])^n} \quad . \tag{364}$$

Equation (364) is plotted in Figure 43, where the required E_Δ/N_0 is plotted versus n for several values of average acquisition time. As can be seen in this figure very long codes can be used with rapid acquisition if E_Δ/N_0 is greater than 3. It should be noted that this is the usual operating limit of a biphase communication system with an adaptive array (see Section E for further details).

The probability of acquisition in a given time will now be examined. In the analysis for Figure 43 the average lockup time rather than the maximum lockup time was considered. For the short code acquisition the acquisition time has a uniform probability density with the maximum acquisition time equal to twice the average. However, for the long code, the acquisition time has a geometrical distribution as shown in Equation (360). Thus, the probability of more than X trials being required to achieve lockup can easily be shown to be given by

$$P_r(x>X) = (1-P_n)^X \quad . \tag{365}$$

Therefore, there is no maximum lockup time and a probability of acquisition, P_{acq}, within a specified number of trials must be considered. From Equation (365) the probability of acquisition in X trials is given by

$$P_{acq} = 1 - (1-P_n)^X \quad . \tag{366}$$

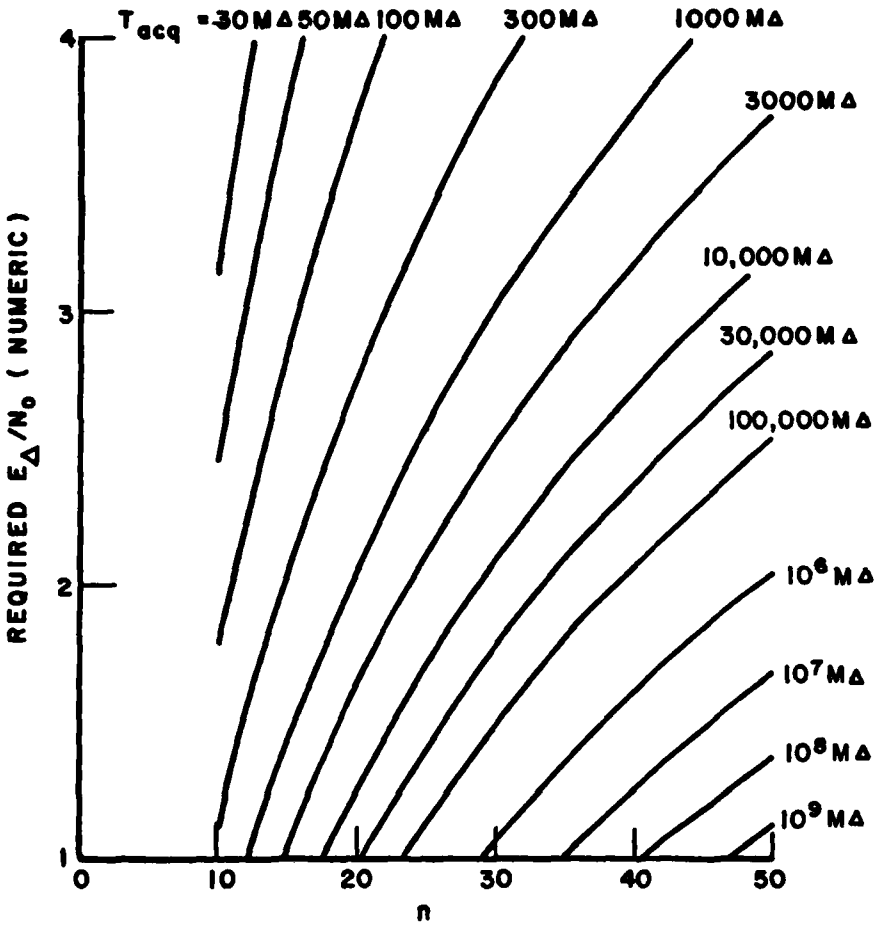


Figure 43. Required E_Δ/N_0 versus shift register length for various values of long code average acquisition time for the approximate system model.

In general, the probability of acquisition for a given trial, P_n, will be a very small number, and, thus, an approximation to Equation (366) can be made. It can be shown that for

$$\frac{1}{P_n} > 10 \quad , \tag{367}$$

$$(1-P_n)^{1/P_n} \approx e^{-1}\left(1 - \frac{P_n}{2}\right) \tag{368}$$

with less than a 0.2 percent error. Since, in general,

$$\frac{1}{P_n} >> 10 \quad , \tag{369}$$

the probability of acquisition can be approximated by

$$P_{acq} \triangleq 1 - e^{-y} \tag{370}$$

where

$$y = X P_n \quad , \tag{371}$$

i.e., y is the multiple of the average number of trials required for a given acquisition probability. Equation (370) may be rewritten as

$$y \triangleq -2.3 \log(1-P_{acq}) \quad . \tag{372}$$

Equation (372) is plotted in Figure 44. It can be seen that the probability of acquisition in the average acquisition time is about 63 percent. This equation can be used with Figure 43 by noting that the time required to acquire the long code timing with a given probability is y times T_{acq} as given in Figure 43. A design example is presented in Chapter XI.

D. The Long Code Symbol Detection Scheme

In this section the long code symbol detection scheme is described. The reason a detection scheme must be developed is that in differentially detecting the four-phase signal (i.e., determining the two symbols corresponding to the phase shift (see Figure 37 for the decision boundaries)) the long code symbols, the short code symbols, and the data bits are detected together, and only the long code symbols are desired. To determine how to separate the long code symbols the modulation method will be examined first. An ambiguity problem exists in detecting a signal with this type of modulation, and this problem is discussed next. A way to get around this problem is then discussed, and a detection scheme is described. The detecting of errors using this scheme is considered next. Finally, the detection logic is shown.

The four-phase signal under consideration in this dissertation can be expressed as (from Chapter V, Equation (142)).

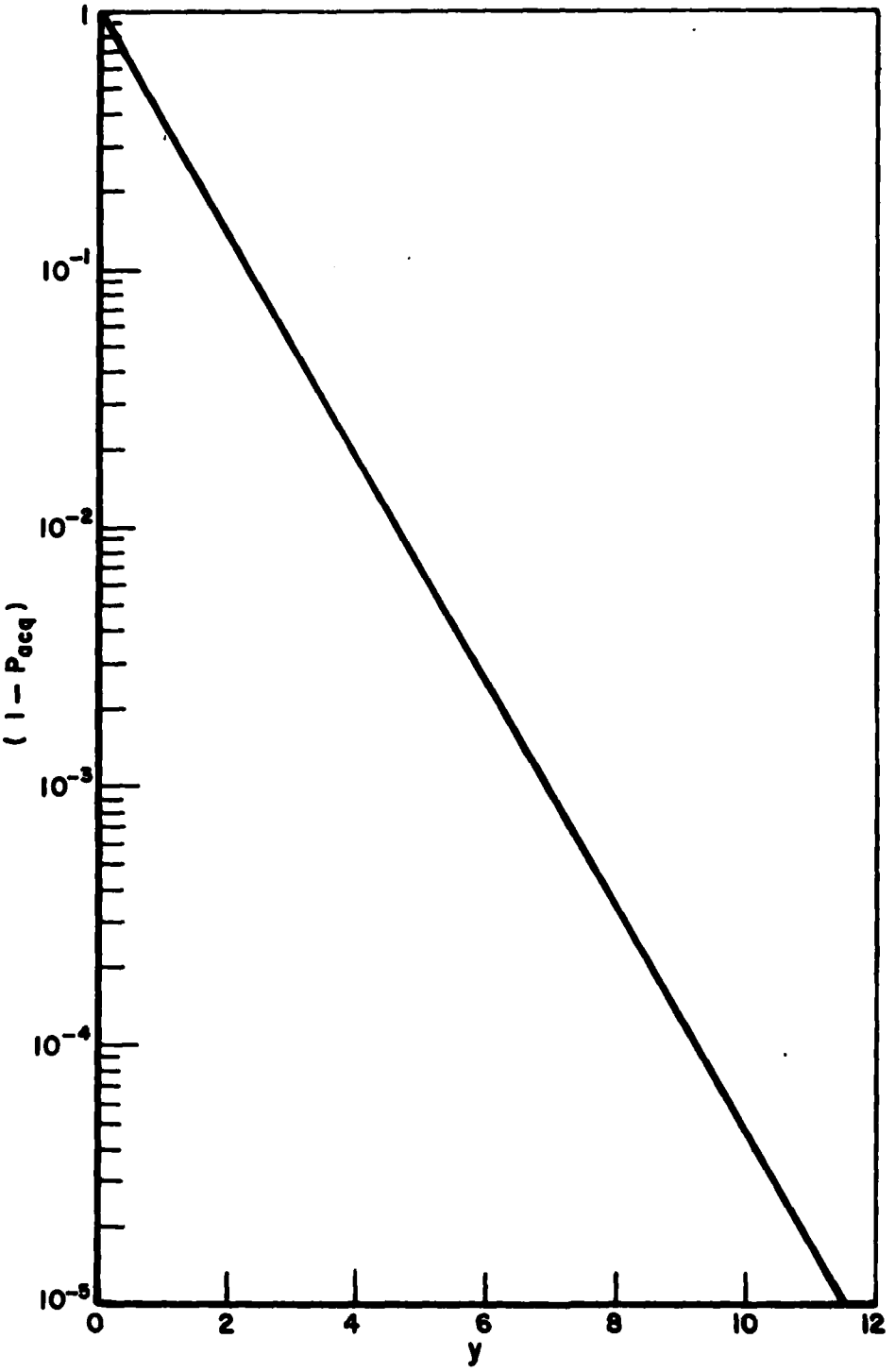


Figure 44. The probability of not acquiring the long code versus the multiple of the average acquisition time for the approximate system model.

$$s(t) = \sin(\omega t+\zeta(t)) + \cos(\omega t+\phi(t)) \qquad (373)$$

where ω is the carrier frequency,

$$\zeta(t) = \zeta_m = \zeta_{m-1} + \eta_m\pi$$
$$\phi(t) = \phi_m = \phi_{m-1} + b_m\pi \qquad (m-1)\Delta \leq t < m\Delta$$

ζ_m is the constant phase angle added to the short code signal component during the mth chip interval,

ϕ_m is the constant phase angle added to the long code signal component during the mth chip interval,

η_m is the mth symbol of a stream of ones and zeros derived from the short code plus data, and

b_m is the mth symbol of a stream of ones and zeros derived from the long code.

The phase shifts in this signal due to the two codes plus data may be determined from Equation (373) and are shown in Table 6. As shown in Table 6 from the phase shifts alone, two symbol streams can be determined but it is impossible to determine which symbol stream contains the long code symbols. Specifically, when a plus or minus ninety degree phase shift occurs it is impossible to determine the long code symbol unless either the short code plus data symbol or the previous phase is known. These two parameters are considered below.

Considering the previous phase first, it can be seen in Table 6 that there are four possible previous phases. These may be grouped into two states, state A, consisting of plus and minus ninety degrees, and state B, consisting of zero and one hundred eighty degrees. Examination of Table 6 shows that it is only necessary to know the previous state to determine the long code symbol from the phase shift. From each phase shift the previous state for determining the next symbol can be calculated. Thus, once the previous state is known, all subsequent long code symbols can be determined. However, there is a fifty percent chance of error in choosing the initial previous state at random.

Considering the short code plus data symbols next, it should be noted that the short code is already known. Thus, the short code plus data symbols are known except for every kth symbol, where k is the spreading ratio. However, which symbol contains data is also not known. To use only the short code symbols to determine the long code symbols would lead to a probability of an error of one-half every k symbols. For n much greater than k, the probability of an error in fully loading

Table 6

The Phase Shifts Caused By the Long and Short Code Symbols Plus Data for the Four-Phase Modulation Scheme

Symbol		Previous Phase (degrees)	Phase Shift (degrees)
Short Code Plus Data η_m	Long Code b_m		
0	0	0	0
0	0	90	0
0	0	180	0
0	0	- 90	0
0	1	0	- 90
0	1	90	+ 90
0	1	180	- 90
0	1	- 90	+ 90
1	0	0	+ 90
1	0	90	- 90
1	0	180	+ 90
1	0	- 90	- 90
1	1	0	180
1	1	90	180
1	1	180	180
1	1	- 90	180

the shift register (even with error free differential detection) can become quite large. Thus, other methods must be examined.

To reduce the chance of error in the long code detection scheme, after examining several schemes, a scheme was chosen which used a combination of the previous state and short code symbols. In this scheme the short code is used to determine the long code symbols until a plus or minus ninety degree phase transition occurs. At this point the

phase shift plus the short code symbol is used to determine the previous state from Table 6. The probability of error in determining the previous state is then the probability of a "1" data bit occurring with this short code symbol, which is given by

$$P_E = \frac{1}{2k} \quad . \tag{374}$$

Thus, for large spreading ratios this probability is small. With the previous state determined, both the long code and short code plus data symbols can be determined from the phase shifts. Also, since the short code symbols are known, the data bits may also be determined. This detection scheme is shown in Table 7.

Since the data bits can be determined using this scheme, some errors in the differential detector can be detected. That is, since a "1" data bit may occur only every kth code symbol in the transmitted signal, if "1" data bits are detected at other than every kth symbol an error is known to have occurred. Unfortunately, from the detection scheme it is impossible to determine which symbol is in error. However, if an error is detected, the shift register loading can be stopped, the register cleared, and shift register loading resumed. This method saves both the time required to complete loading of the shift register and the correlation time for the cases where an erroneous loading of the shift register may occur.

Because of several factors including the dependence of symbol errors as described in Section B, it is extremely difficult to determine theoretically the performance of this detection scheme with the differential detector. Therefore, this detection scheme has been modelled in Section E, and a computer simulation has been made of the long code acquisition procedure for white, Gaussian noise present on the received signal. However, some understanding of this detection scheme's error detecting capability can be obtained by briefly examining Table 7. For example, the case can be considered where the previous state has been determined and there are no data bits present for several consecutive short code symbols. As can be seen in Table 7, if the phase shift determined by the differential detector is in error by 180 degrees, then a "1" data bit will be determined, and this will signal an error. If the detected phase shift is in error by plus or minus ninety degrees, then an error in the next code symbol's previous state will be made. As seen in Table 7, if there is an error in the previous state and the next phase shifts are determined correctly, then with a plus or minus ninety degree phase shift it will be determined that a "1" data bit has been received (note that no data bits have been assumed present), and an error will be detected. Thus, for this case, most errors in the differential detector will be detected. Although only one special case was considered here, it will be shown in Section E that this detection scheme does indeed detect most of the differential detection errors.

Table 7
The Detection Scheme

1) Initially (Unknown previous state)

Phase Shift* (degrees)	Short Code Symbol	Next Previous State	Long Code Symbol	"1" Data Bit
0	0	Unknown	0	No
0	1	Unknown	0	Yes
+ 90	0	B	1	No
+ 90	1	A	0	No
180	0	Unknown	1	Yes
180	1	Unknown	1	No
- 90	0	A	1	No
- 90	1	B	0	No

*The phase shift is determined by the differential detector. From Figure 37, +90 degrees corresponds to a "01" output from the differential detector, -90 degrees is a "10", 180 degrees is a "11", and 0 degrees is a "00".

2) Previous State A

Phase Shift (degrees)	Short Code Symbol	Next Previous State	Long Code Symbol	"1" Data Bit
0	0	A	0	No
0	1	A	0	Yes
+ 90	0	B	1	No
+ 90	1	B	1	Yes
180	0	A	1	Yes
180	1	A	1	No
- 90	0	B	0	Yes
- 90	1	B	0	No

Table 7 (Cont.)

3) Previous State B

Phase Shift (degree)	Short Code Symbol	Next Previous State	Long Code Symbol	"1" Data Bit
0	0	B	0	No
0	1	B	0	Yes
+ 90	0	A	0	Yes
+ 90	1	A	0	No
180	0	B	1	Yes
180	1	B	1	No
- 90	0	A	1	No
- 90	1	A	1	Yes

A block diagram of the circuitry necessary for implementation of this detection scheme is shown in Figure 45. The logic for the PROM shown in this figure is provided in Table 8.

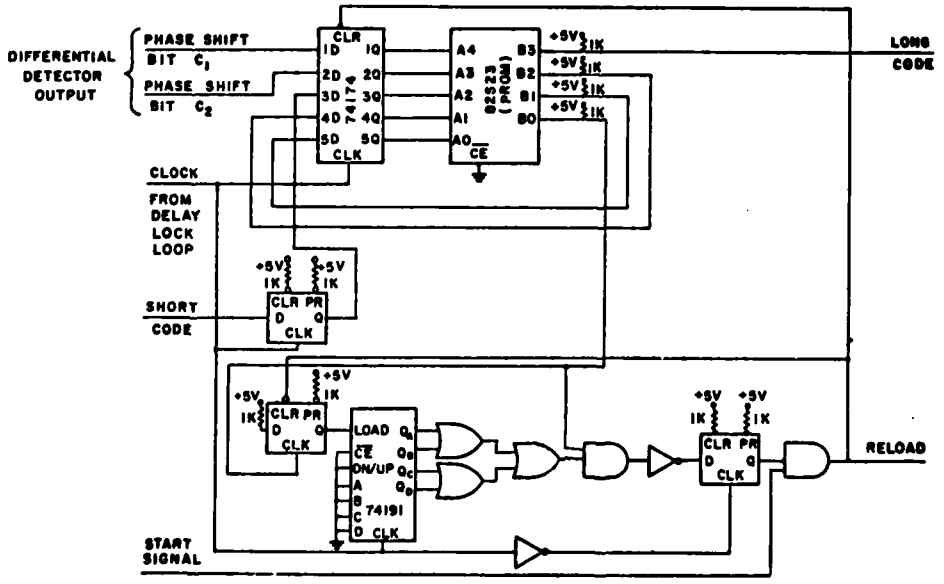


Figure 45. Block diagram of the circuitry for implementation of the detection scheme of Table 7 with k=16.

Table 8

PROM Logic for Figure 45

Input				Output		
Differential Detector Outputs		Short Code Symbol	Previous State*	Long Code Symbol	Next Previous State*	Data Bit
0	0	0	0 0	0	0 0	0
0	1	0	0 0	1	0 1	0
1	0	0	0 0	1	1 0	0
1	1	0	0 0	1	0 0	1
0	0	1	0 0	0	0 0	1
0	1	1	0 0	0	1 0	0
1	0	1	0 0	0	0 1	0
1	1	1	0 0	1	0 0	0
0	0	0	1 0	0	1 0	0
0	1	0	1 0	1	0 1	0
1	0	0	1 0	0	0 1	1
1	1	0	1 0	1	1 0	1
0	0	1	1 0	0	1 0	1
0	1	1	1 0	1	0 1	1
1	0	1	1 0	0	0 1	0
1	1	1	1 0	1	1 0	0
0	0	0	0 1	0	0 1	0
0	1	0	0 1	0	1 0	1
1	0	0	0 1	1	1 0	0
1	1	0	0 1	1	0 1	1
0	0	1	0 1	0	0 1	1
0	1	1	0 1	0	1 0	0
1	0	1	0 1	1	1 0	1
1	1	1	0 1	1	0 1	0

* Previous state 0 0 is unknown previous state.
Previous state 1 0 is previous State A.
Previous state 0 1 is previous State B.

E. Simulation of the Long Code Acquisition Method

In this section the simulation of the long code acquisition method is discussed and the results of this simulation are presented. The simulation method is used for the analysis of the acquisition method because the dependence of symbol errors in the differential detector (Section B) and the complexity of the detection logic (Section D) make a theoretical analysis extremely difficult. First to be described in this section is the method by which the noise at the receiver is simulated. Next the model of the acquisition method used in the simulation is described. Finally, the results of a large number of computer runs using this model are shown and discussed.

The performance measure of interest in this part is the average lockup time as a function of E_Δ/N_0 and the number of stages in the shift register used to generate the long code. The effect of the spreading ratio and correlation time is also considered. The performance of the acquisition procedure is determined by the average lockup time for a large number of computer simulations of the acquisition procedure where the signal and noise input to the receiver is generated at random. To simulate the generation of a signal with noise and the detection method for this signal, the following steps are performed on the computer.

Step 1 is the simulation of the transmitter. First, two code symbol streams are generated by the computer. Each symbol is generated at random with equally probable 1's and 0's. One symbol stream is labelled the short code, and the other stream is labelled the long code, i.e., it contains the b_i's (as defined in Equation (373)).

Second, data bits are generated at random with equally probable 1's and 0's. These are added to every kth short code symbol to generate the η_i's (as defined in Equation (373)). Which one of the first k short code symbols is to have the first data bit added to it is determined at random with each of the k symbols equally probable.

Third, the b_i and η_i symbol streams are converted to differential phase shifts by the modulation method shown in Table 6, simulating the actual modulation method. The initial previous state is chosen at random with States A and B equally probable.

Step 2 is the simulation of the noise added to the signal at the differential detector. The parameter of interest in this model is the angular error in the phase of the chip interval signal vectors due to noise in the differential detector. As discussed in Section B, the probability density function for this phase error for a given E_Δ/N_0 is given by

$$p(\psi/(E_\Delta/N_o)) = \frac{1}{2\pi} \exp\left[-\frac{E_\Delta}{N_o}\right]$$

$$+ \frac{1}{\sqrt{2\pi}} \exp\left[-\frac{E_\Delta}{N_o}\sin^2\psi\right]\sqrt{\frac{2E_\Delta}{N_o}}\cos\psi\left[\frac{1}{2} + Q(\psi,E_\Delta/N_o)\right] \tag{342}$$

where

$$Q(\psi,E_\Delta/N_o) = \frac{1}{\sqrt{2\pi}} \int_0^{\sqrt{2E_\Delta/N_o}\cos\psi} \exp[-u^2/2]\, du \quad . \tag{343}$$

This probability density function is plotted in Figure 46 for E_Δ/N_o between 1 and 4. The probability distribution function for this phase error is then given by

$$P(\psi/(E_\Delta/N_o)) = \int_{-\pi}^{\psi} p(X/(E_\Delta/N_o))\, dX \quad . \tag{375}$$

This function is plotted in Figure 47 again for E_Δ/N_o between 1 and 4.

For the simulation it is desired to generate phase errors for each signal vector at random, with the phase error having a probability density function given by Equation (342). To do this, a subroutine is used that generates a random number between 0 and 1 with a uniform distribution. With this number the value of ψ is determined for which the probability distribution function as given in Equation (375) is equal to the generated number. By this method the values of ψ which are generated will have the probability density function of Equation (342).

The only difficulty in the above procedure is that the generation of the values of ψ for a given $P(\psi/(E_\Delta/N_o))$ requires the inverse of Equation (375) to be determined. To accomplish this Equation (375) is first evaluated for several values of ψ with a given value of E_Δ/N_o. The inverse function of ψ versus $P(\psi/(E_\Delta/N_o))$ is then approximated by a low order polynomial using the least squares method. A three piece, fourth order polynomial approximation determined using 24 points per piece was found to provide a good approximation to the inverse function. The polynomial coefficients are then easily used to compute ψ from the value of $P(\psi/(E_\Delta/N_o))$. This approximation process needs only to be done once for a simulation with a given value of E_Δ/N_o. Using the above method a phase error is then determined for each signal vector.

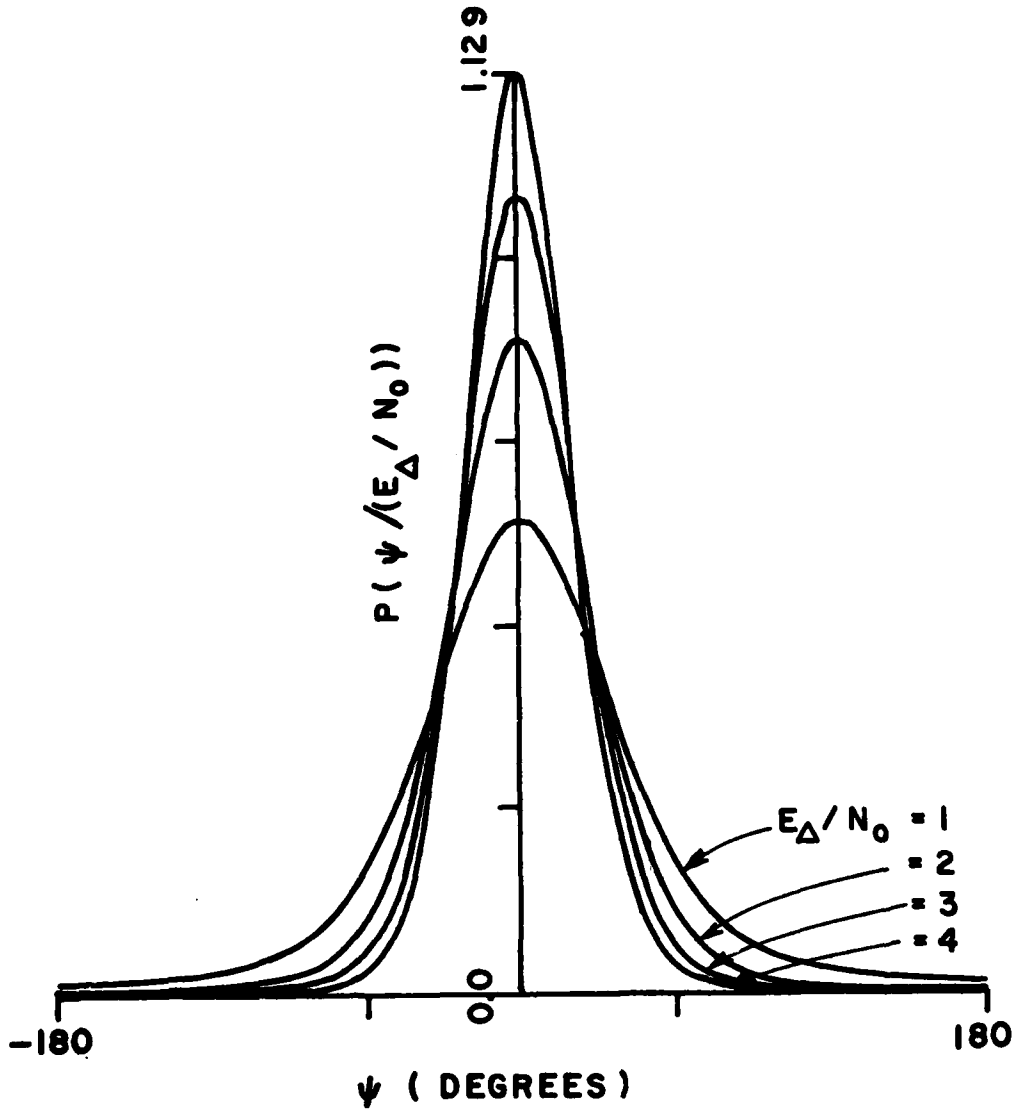


Figure 46. The probability density function of the signal vector phase error for several values of E_Δ/N_0.

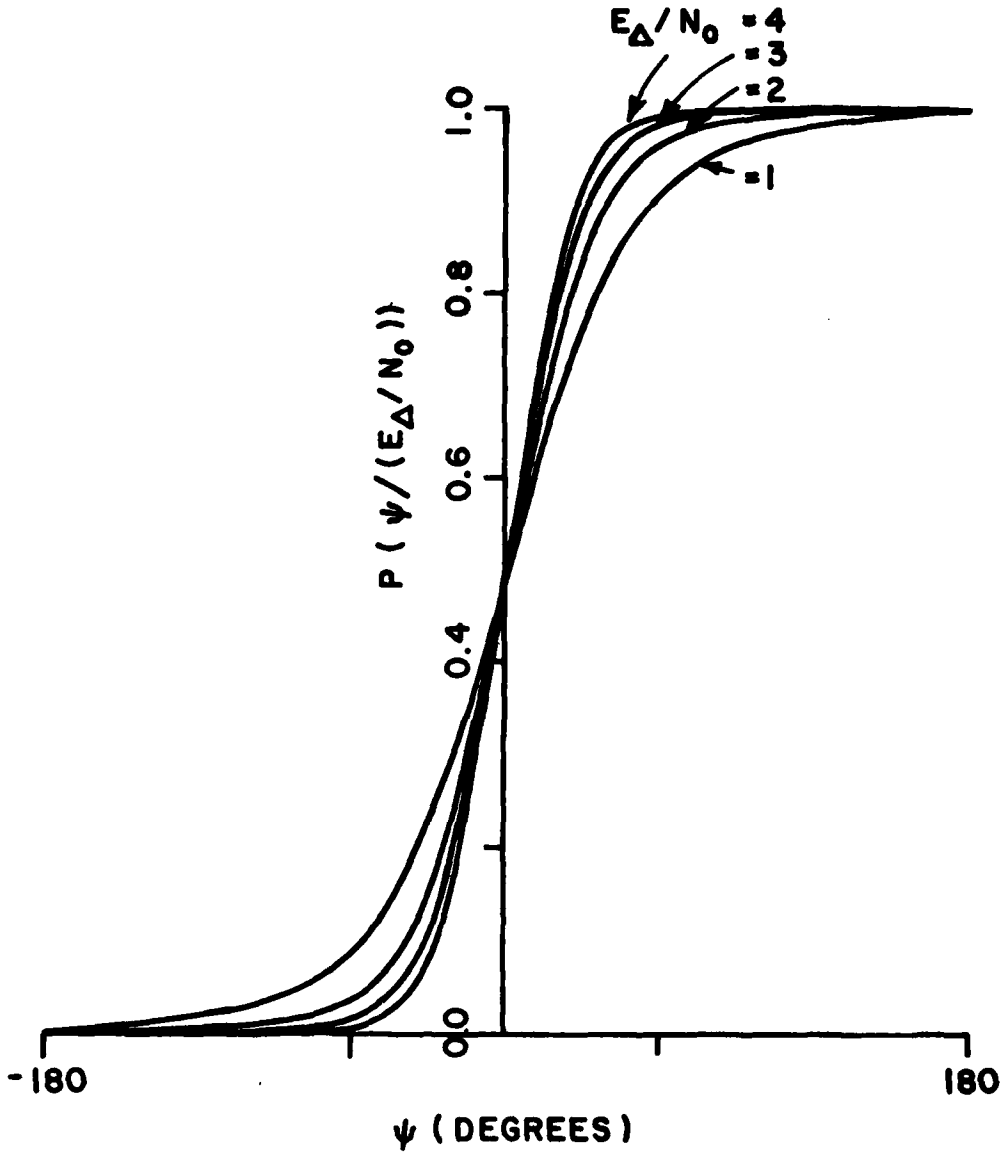


Figure 47. The probability distribution function of the signal vector phase error for several values of E_Δ/N_0.

Step 3 is the simulation of the differential detector. First, from the phase error for each chip interval signal vector, the differential phase shift error per chip interval is determined. Second, this differential phase shift error is compared to the decision boundaries shown in Figure 37 to determine the error, if any, that would be made by the differential detector. Third, this error is added to the differential phase shift due to the signal. The symbols corresponding to the differential phase shifts are now ready for processing by the detection scheme. It can be seen that by the above method the expected values of the conditional symbol error rates in the differential detector are the same as those given in Section B.

Step 4 is the simulation of the detection scheme. First, from the symbols corresponding to the differential phase shifts, the long code symbols and the "1" data bits are determined by the method shown in Table 8. Second, errors in the detection process are detected as described in Section D by determining if the "1" data bits only occur at intervals of k symbols, where k is the spreading ratio. Third, if an error is detected, the detection scheme is halted, and the number of symbols detected is recorded. It should be noted that if no errors were detected in n long code symbols, where n is the number of stages in the feedback shift register, then in the actual acquisition procedure a correlation would be made between the shift register output and the received signal. To simulate this in the model, if no errors are detected in n long code symbols, a correlation trial is recorded. Then the n detected long code symbols are compared with the transmitted symbols. If no errors in the detected symbols are found, then a completion of acquisition is recorded.

To determine the average lockup the above steps are repeated for a very large number of code symbols. The number of symbols detected, N_{SD}, is determined along with the number of correlation trials, N_{CT}, and the number of successful acquisitions, N_{SA}. The average lockup time is then given by

$$T_{acq} = \frac{N_{SD}+N_{CT}\cdot T_{corr}}{N_{SA}} \quad \text{(in chip intervals)} \qquad (376)$$

where T_{corr} is the correlation time.

The results of the computer simulation are presented in Figure 48, which shows the required E_Δ/N_0 versus shift register length for a given average long code lockup time. From Figure 48 it can be seen that for E_Δ/N_0 between 3 and 4 numeric, synchronization can be obtained in 30,000 chip intervals or less for codes generated from 40 to 50 stage shift registers. Thus, very long codes can be used if the minimum E_Δ/N_0 is at least 5 to 6 dB. This restriction on E_Δ/N_0 values does not decrease the range of the adaptive array, however, because other factors also places the minimum E_Δ/N_0 value in this range. One factor is

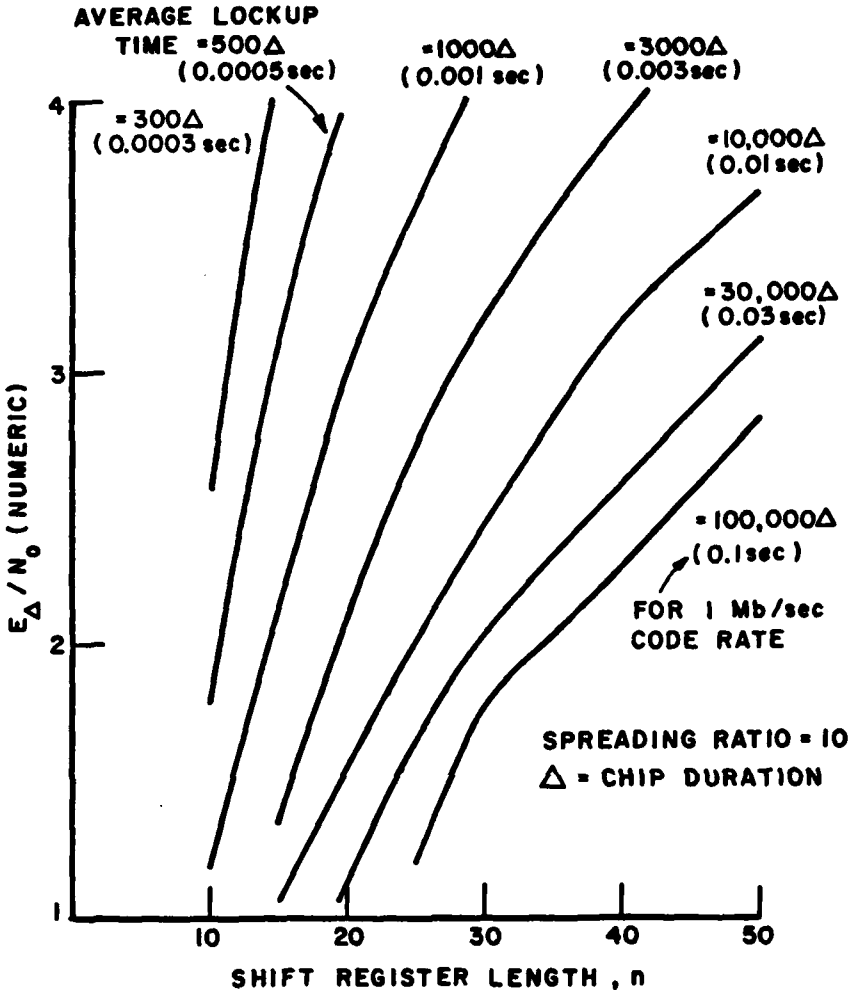


Figure 48. Required E_Δ/N_0 versus shift register length for given average lockup time, with a correlation time of $10n\Delta$.

the required energy per data bit to noise density ratio, which must be at least 13 (numeric) for a bit error probability with ideal differential detection on the order of 10^{-6} (see Section B). Since data is present only on one of the two orthogonal biphase signals, with a spreading ratio of 10, the required E_Δ/N_0 is about 2.6. Since timing jitter, frequency offset, and other factors may degrade the differential detector performance in an actual system, an even higher E_Δ/N_0 may be required to get the same bit error probability. Thus, from Figure 48 it can be seen that using the acquisition procedure, the timing for very long codes can be quickly acquired without any sacrifice in array performance.

In Figure 48 the spreading ratio was equal to 10. Computer simulation has shown that these results do not vary significantly with spreading ratio for the spreading ratio in the range from 5 to 20. Thus, the results of Figure 48 can be used in most cases.

Also in Figure 48 the correlation time was equal to 10n chip intervals. The effect on the acquisition time of the correlation time is examined below. In Equation (376) it can be seen that the effect of the correlation time is dependent on ratio of the number of symbols detected to the number of correlation trials. For the range of parameters in Figure 48, the simulation has shown that this ratio has an average of about 10n for all cases, but varies by as much as a factor of 5 for individual cases. The effect of varying the correlation time is illustrated in Figures 49 through 51. For these figures, with the correlation time given by

$$T_{corr} = Mn\Delta \quad , \tag{361}$$

M is varied from 5 to 40. It can be seen that for E_Δ/N_0 between 3 and 4, and n about 40, increasing M from 5 to 40 increases the average lockup time only a small amount.

The results of this section can be compared to the results of Section C for the approximate model. In comparing Figure 43 to the figures in this part, it can be seen that the simulation shows that the lockup time is, in general, several times faster than that predicted with the approximate model. However, the results of Section C can still be used to obtain a rough idea of the acquisition performance.

In this simulation study the probability of acquisition in a given time was not considered. Such an analysis would require many times more simulation runs and, thus, be very time consuming. Therefore, the results of Section C will be used to approximate the probability of acquisition in a given time (see Chapter XI).

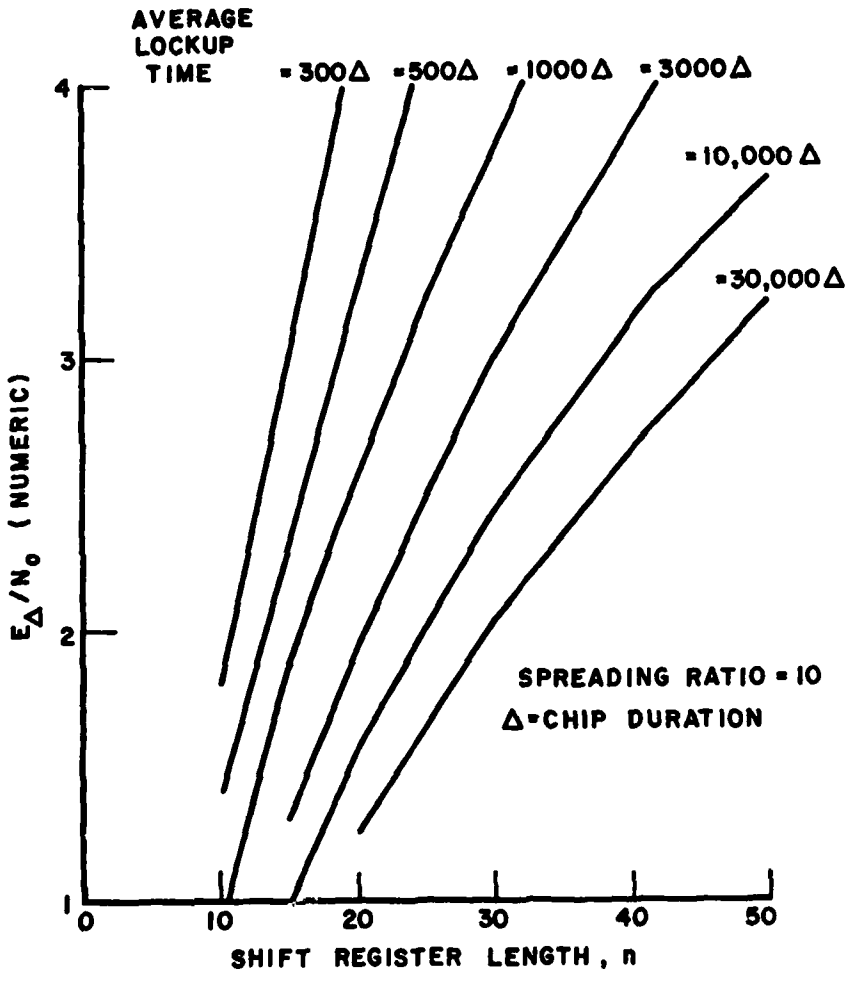


Figure 49. Required E_Δ/N_0 versus shift register length for given average lockup times, with a correlation time of $5n\Delta$.

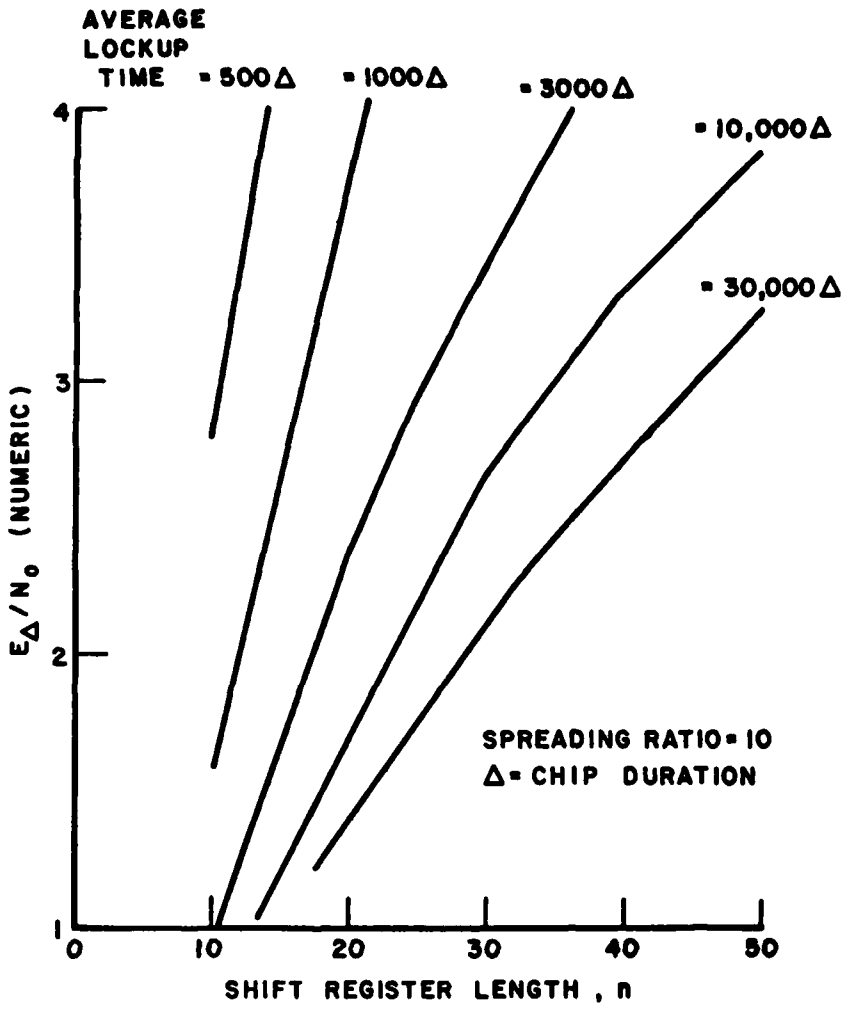


Figure 50. Required E_Δ/N_0 versus shift register length for given average lockup times, with a correlation time of $20n\Delta$.

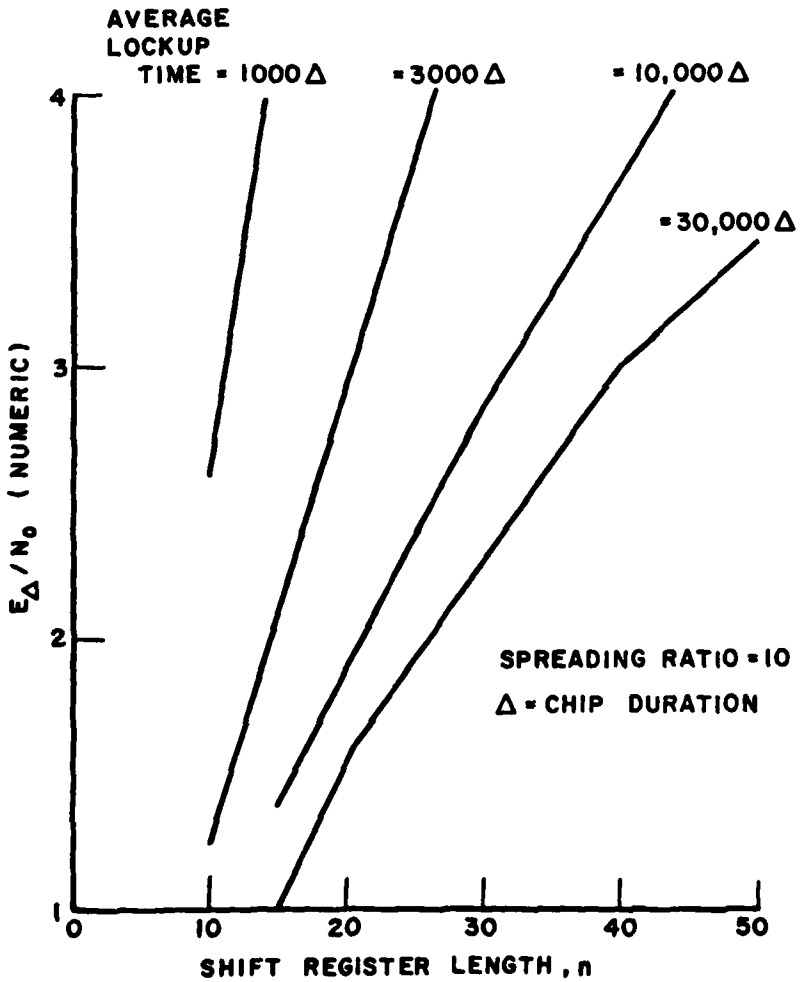


Figure 51. Required E_Δ/N_0 versus shift register length for given average lockup times, with a correlation time of 40nΔ.

CHAPTER IX

THE LONG CODE

A. Introduction

In this chapter the long code in the four-phase communication system is examined. The properties which the long code must have to make the system more secure against effective smart jamming while allowing for rapid timing acquisition using the method described in Chapter VIII are considered here. As will be shown, the security of the system is dependent on the length of the long code and the method by which the code is generated. Also, to assure rapid acquisition the code must have certain correlation properties. First to be analyzed is the necessary length of the code. Next, a problem associated with the security of linearly generated codes is examined. The advantage of nonlinear codes is then considered. Finally, the correlation properties of codes are discussed.

B. Code Length

One advantage of using a long code to generate the reference signal in an adaptive array is that, if the code period is long enough, a repeat jammer, even with a variable transmission delay, may not be effective. The reason for this is as follows. First, if the repeat jammer remodulates and retransmits the four phase desired signal, then the code and the signal will be changed in such a way that the adaptive array will treat the repeat jammer's signal as interference (see Chapter X). Therefore, consider the case where the jammer retransmits the desired signal, unchanged, at a later time. First assume the time delay between the desired and repeated signal is greater than one chip interval (a reasonable assumption, see Chapter X). If the delay is less than the long code acquisition time and the receiver considers the repeated signal as the desired signal, then this received signal can be effectively used by the system. If the delay is greater than the long code acquisition time, then the array will treat the repeated signal as interference so long as the delay is different from a multiple of the long code period. Thus, the code must be sufficiently long so that a repeat jammer could never retransmit a signal with the same code timing as the desired signal.

Such a code could have a period of one year, and the code could be changed once a year so that it never repeats. For example, on a one megabit per second communication link, the code length would need to be about 3×10^{13}. Thus, if a maximal length feedback shift register were used to generate the code, it would have to be 45 stages long ($2^{45}-1 \cong 3 \times 10^{13}$). Much shorter codes could actually be used because the probability of a repeat jammer determining that a very long code is repeating is small. Thus, the required communication security may even be achieved with a billion symbol code (generated by a thirty stage shift register).

C. Code Structure

Next consider the topic of code structure or how the code is generated. If the code is long enough so that the repeat jammer is ineffective, then to be effective, the smart jammer must be able to generate a signal with the same long code as the desired signal and with the same timing at the receiver. It can then use this signal to jam the system. This, however, requires the smart jammer to be able to accomplish a great deal. First, it must be able to separate the long code symbols and the short code with data symbols in the desired signal. This may be possible because the two signals containing these symbols are orthogonal. Second, the jammer must know that a long and a short code are involved in the system and that a knowledge of the long code and its timing will aid in effective jamming. Third, the jammer must be able to determine which is the long code. But most important, the jammer must be able to determine the long code and its timing.

If the code is very long, the ability of the jammer to determine the code and its timing depends on the code structure. That is, the jammer must be able to determine the code and its timing from a short sequence of code bits. Although for a very long code this may seem to be very difficult, this is exactly what the adaptive array receiver is doing to acquire the long code timing (see Chapter VIII). The advantage the receiver has over the smart jammer in determining the properly timed code is a knowledge of the number of stages in the shift register and the feedback connections. The smart jammer, on the other hand, may be in a position to detect the code symbols with a very low bit error rate, while the receiver may have to operate with a much higher bit error rate (such as in satellite communication systems). Thus, the code must be generated in such a way that without any knowledge of the feedback shift register the jammer cannot determine the code and its timing, even with the correct code symbols. However, the code must also be generated in such a way that the receiver can acquire the code timing in the required time.

With respect to the above criteria, consider codes generated from linear feedback shift registers. At the receiver the time to acquire

long code timing is based in part upon the number of shift register stages (see Chapter VIII). Thus, the number of stages will be limited to some maximum value. The receiver is only required to determine correctly a sequence of bits equal in number to the shift register length to obtain code timing. The jammer, on the other hand, must determine the code and its timing without a knowledge of the shift register length or feedback connections. One method the jammer can use is to check each one of several shift register lengths to see if linear feedback connections exist which generate the code. The method to do this is described below as taken from [26].

The equation for a linear feedback shift register of length n may be given by

$$s(i+1) = A\, s(i) \tag{377}$$

where s(i) is an n dimension column vector containing the bits in the shift register at time i, and A is an n x n matrix for the shift register. If,

$$x(1) = [s(1)\ s(2)\ \cdots\ s(n)] \quad , \tag{378}$$

and

$$x(2) = [s(2)\ s(3)\ \cdots\ s(n+1)] \tag{379}$$

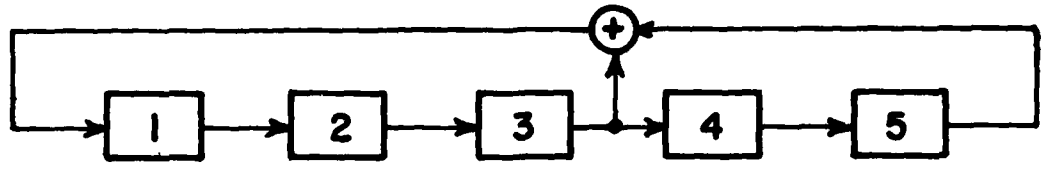
then

$$A = x(2)\,[x(1)]^{-1} \quad \text{modulo 2} \quad , \tag{380}$$

if $X(1)^{-1}$ exists.

It is noted in [26] that x(1) is nonsingular for any maximal length shift register sequence. For a linear feedback shift register with feedback connections only to the first stage (as required for long code acquisition, see Chapter VIII), the location of 1's in the first row of A gives the location of the feedback connections. This is illustrated in Figure 52. Thus, only 2n code symbols need to be used in determining the code.

The jammer would, therefore, determine an A matrix for values of n starting at a small number and increasing until an A matrix was



$$A = \begin{pmatrix} 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{pmatrix}$$

Figure 52. A five stage linear feedback shift register and its corresponding A matrix.

found which led to a code which matched the long code. Because the value of n used in the system is limited (from Chapter VIII, a value of n greater than 50 would be impractical in most systems), the number of trials the jammer would have to make is not excessive. The time consuming part of the process is computing, for each n, $[x(1)]^{-1}$ in Equation (380), for which at most on the order of n^3 computer operations are required. The total number of operations required in the jammer's search for the type of linear feedback shift register used by the system for various values of n is shown in Table 9. Note that even with a microprocessor with an instruction time of 1 μsec, the jammer could determine the length of the long code's linear feedback shift register and its feedback connections in a short amount of time. The jammer is then only required to detect n code symbols to generate a code with the proper timing to defeat the system.

The use of nonlinear logic in the feedback shift register can drastically decrease the probability of the determination of the code by the smart jammer. With nonlinear feedback logic (that is, logic that uses other than just exclusive-or operations) the procedure described before cannot be used to determine the taps from just 2n code symbols. However, the output of a feedback shift register with nonlinear logic can always be generated from a shift register with

Table 9

Number of Computer Operations Required for a Smart Jammer to Determine the Length and Linear Feedback Connections of the Shift Register Used to Generate the Long Code for Various Values of Shift Register Length

Shift register length used in generating long code (n)	Number of computer operations required in search for determining correct A matrix $\left(\sum_{i=1}^{n} i^3\right)$
5	225
10	3025
15	14,400
20	44,100
25	105,625
30	216,225
35	396,900
40	672,400
45	1,071,225
50	1,625,625

linear feedback. Up to a 2^n-1 length linear feedback shift register may be required, though. The Berlekamp-Massey algorithm [27,28] can be used to find the minimum length linear feedback shift register which generates a given nonlinearly generated code. Thus, although the method discussed before for determining the code length and feedback taps for linearly generated codes could be used by the jammer, the proper use of nonlinear logic can make this process far too time consuming. Hence, a very secure code can be generated with a shift register with a small number of stages (usually less than 50). The number of computer operations required for the jammer to determine a code which, although generated by nonlinear feedback logic in an n stage shift register, requires an m stage shift register with linear feedback to generate it, is given by (using the same analysis as in Table 9, with [18])

$$\sum_{i=1}^{m} (i^3) = \frac{m^2(m+1)^2}{4} \quad . \tag{381}$$

For example, if m is equal to 20,000 a bank of 1000 microprocessors with an instruction time of 1 μsec would take about 1 year to determine the code. Such a value of m could theoretically be achieved using nonlinear logic with shift registers of a length of only 16 or greater. Thus, the possibility exists for generating very secure codes with a small number of shift register stages.

For the long code acquisition method to work, the nonlinear code must be generated with a shift register whose only feedback is to the first stage. Nonlinear codes of this type are described in [29]. An example of this type of code is given below. The nonlinear code considered is given by

$$a_k = a_{k-31} \oplus a_{k-6} \oplus a_{k-21} \oplus (a_{k-8} \odot a_{k-6})$$

$$\oplus (a_{k-8} \odot a_{k-21}) \oplus (a_{k-6} \odot a_{k-21}) \quad , \tag{382}$$

where a_k is the kth code symbol, $\oplus$ represents an exclusive-or operation and $\odot$ represents the and operation. The 31 stage shift register and the nonlinear feedback logic to generate this code are shown in Figure 53. From [29, p. 159], it is seen that this code has length 2,146,670,359 (when the shift register is initially loaded with 1's). This is very close to the maximum length code that can be generated from a 31 stage shift register which is $2^{31} - 1$ or 2,147,483,647. Thus, very long nonlinear codes can be easily generated from short length shift registers. However, although many different nonlinear codes are described in [29], it may require considerable effort to find other nonlinear codes which are both very long and generated from a short length shift register.

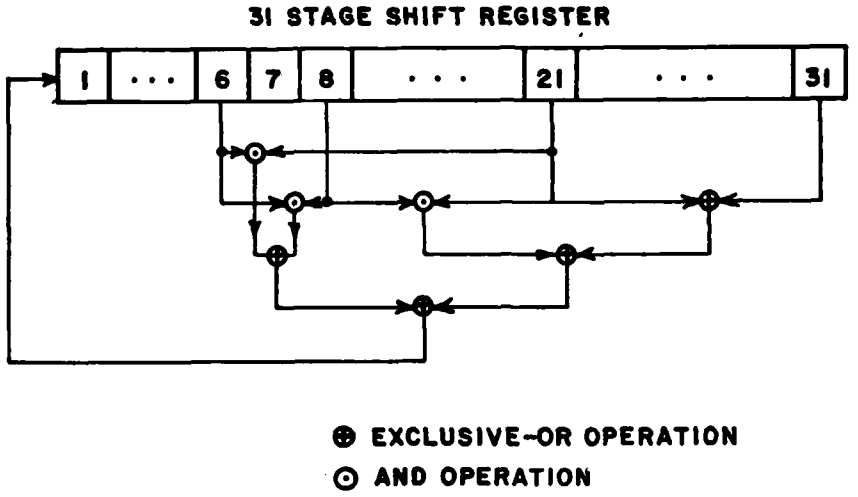


Figure 53. The feedback shift register needed to generate the nonlinear code given by Equation (382).

D. Code Properties

The next topic to be considered is the properties that the long code must have to assure rapid acquisition of the code timing using the method described in Chapter VIII. Since very long codes are used in the system, the correlation in the acquisition procedure can only be made over a short segment or subsequence of the code. Thus, there may be a high degree of correlation between the received signal and the code generated at the receiver when the code timing is in error. This will increase the probability of acquiring the wrong code timing and, therefore, increase the acquisition time. The long code must, therefore, be designed to have as small as a subsequence cross-correlation as possible.

Designing feedback shift registers which generate codes with low subsequence cross-correlation is extremely difficult. In general, numerous codes would be examined and the code with the lowest subsequence cross-correlation chosen for use in the system. In [6], [30], [31], and [32] this problem is examined and codes are found by trial and error which have low subsequence cross-correlation. To analyze the subsequence cross-correlation for a given code (that is, to determine its probability density function) it is necessary to find the cross-correlation for all possible cases. However, for linear codes, as shown in [32], it is only necessary to determine the probability density function of the number of 1's for the consecutive M_n code symbols to determine the

subsequence cross-correlation probability density function. Here, M_n is the correlation time in code symbols. This probability density function can be used to choose the correlation time so that with a given correlation threshold value the probability of acquiring the wrong code timing and the probability of missing the correct code timing is acceptable. This problem is further considered in [32]. It should be noted that the probability density function of the subsequence cross-correlation is different for each value of correlation time which complicates the choosing of a correlation time. Also for nonlinear codes such an analysis is quite involved.

The long code used in the system should, therefore, have a very long period, have good subsequence correlation properties, and be generated with nonlinear feedback logic with a short length shift register which requires a very long length shift register with linear feedback logic to generate the same code. It is very difficult, though, to design the shift register with feedback logic to generate such a code. References [6] and [26] through [32] give some insight into how codes may be analyzed for the desired properties, but no insight is given to how to easily find the codes with these properties. Thus, unfortunately, a very long and exhaustive study of numerous codes would be necessary to find even a few codes with good properties. This has not been done in this paper, but such a study could be made later if it was needed.

If only codes generated with linear feedback logic are considered, very long codes with good subsequence correlation properties can be found without too much difficulty (see reference [27]). These codes still provide some protection against smart jammers and they (in particular, pseudonoise codes) are considered in the experimental setup in Chapter XI.

CHAPTER X

JAMMER EFFECTS

A. Introduction

In this chapter the effect that various types of jamming would have on the four-phase communication system with an adaptive array is considered. The discussion expands upon that presented in Chapter V. Smart jamming techniques are emphasized. Two different times are considered when jamming may occur. These are the time during the acquisition of the signal by the adaptive array and the time after acquisition. The types of jammers to be considered are conventional jammers (i.e., tone and noise jammers), repeat jammers with and without remodulation, and jammers using only the short code. The effect of these jammers is described below.

B. Conventional Jammers and Repeat Jammers Without Remodulation

The first type of jamming to be considered is conventional jamming. As shown in Chapter IV, the performance of the adaptive array during and after acquisition is not significantly different for the four-phase system as compared to the biphase system (not considering smart jammers). The only difference for the four-phase system is a three decibel reduction in the weight values and a constant error signal in the feedback circuitry. This, however, will have a negligible effect on the array performance with conventional jamming. Thus, it can be seen that the four-phase system will have the same capability to defeat conventional jamming as the biphase system.

The next jammer type to be considered is the repeat jammer without remodulation. During acquisition the adaptive array is as likely to acquire a repeat jammer signal as to acquire the desired signal. However, since the repeated signal is not remodulated, the adaptive array can use the repeated signal in place of the desired signal.

After acquisition of the desired signal, with the long code being used to generate reference signal, a repeat jammer will be treated as conventional interference unless the long code timing of the repeated signal is the same as that of the desired signals. That is, to be

effective,the repeated signal must be delayed by a multiple of the long code period. As discussed in Chapter IX, such a delay would be extremel difficult to achieve or even impossible if the long code never repeats. Thus, a repeat jammer without remodulation will not effect the system.

C. Repeat Jammers With Remodulation

A repeat jammer with remodulation will now be considered. Since the system uses four-phase differential phase shift keying, the type of remodulation to be studied is that which adds additional phase shifts to the signal. The intent of the jammer is then to change the data while allowing the repeated signal to still be acquired and tracked by the adaptive array.

In a biphase communication system remodulation of the signal by adding 180° phase shifts at a rate equal to or less than the desired signal data rate results in a signal which can still be acquired by the adaptive array, although the data is changed. Thus, effective jamming can be achieved in biphase systems with this method. However, if the remodulation rate is much greater than the desired signal data rate, then the repeated signal would be greatly attenuated by the band-pass filters in the delay lock loop and the reference loop. Therefore, the repeated signal would not be acquired by the adaptive array for high remodulation rates. Thus, the jammer must be able to approximately determine the data rate. For the biphase system, since the short code repeats frequently, it is easy for the jammer to examine the signal and determine the rate at which the code bits are changed; i.e., to determing the data rate.

For the four-phase communication system the remodulation by the jammer could consist of the addition of 180, 90, or -90 degree phase shifts to the desired signal. With such a scheme, the remodulation will appear on the short code as additional data bits. Since the short code on the four-phase signal is acquired in the same manner as the code on the biphase signal, the short code timing on a repeated signal may also be acquired by the adaptive array if the remodulation rate is equal to or less than the data rate of the desired signal. However, for the four-phase signal it is much more difficult for the jammer to determine the data rate because the desired signal contains two codes. Thus, a jammer may only be able to guess at the data rate with the chance of choosing the rate too high.

It should be noted that the repeated signal and the desired sigaanl are equally likely to have their short codes acquired by the adaptive array. Whichever signal does not have its short code timing acquired is then nulled by the adaptive array. If the remodulated repeated signal short code timing is acquired, then erroneous data wil be received. Thus, the desired signal would be effectively jammed in

a biphase system. However, in the four-phase system the long code timing must still be acquired, and this is unlikely to occur for the repeated signal with remodulation as explained below.

If the long code has been changed or is not present on the received signal, long code timing may not be acquired in a short time. To be discussed now is what happens if the long code timing is not obtained in a given time (chosen by the system designer). That time is the time for which the long code timing would be acquired with a given probability if the unchanged long code was present on the received signal (see Section VIII-C). This probability would normally be high, say 99.9%. Therefore, if the long code timing is not obtained in this time it would be assumed at the receiver that the received signal does not contain the unchanged long code and, therefore, is not the desired signal.

As discussed in Chapter V, the adaptive array will then begin to null the signal for which long code synchronization was not achieved and try to acquire another signal containing the short code. To accomplish this, the slew voltage is turned on in the delay lock loop (which is tracking the short code timing) and the short code timing is, therefore, changed from that of the previously acquired signal. The slew voltage is held on long enough to change the short code timing at least two code symbols, and then the short code timing acquisition procedure is started. This ensures that the delay lock loop will not lockup on the short code of the same signal until it has examined all other possible short code timings (i.e., has tried to find all other signals containing the short code). Thus, the adaptive array will continuously search for a signal with the short code plus an unchanged long code, which is, presumably, the desired signal.

Several methods of remodulation will now be discussed to determine if it is possible to change the data without changing the long code. First to be considered is biphase modulation. As can be seen from Table 6, if an additional 180° phase shift is added to the signal both the long code symbol, b_m, and the short code plus data symbol, η_m, are changed. Since the long code symbols are changed it is unlikely that the long code shift register will be loaded properly and long code synchronization obtained in the required time. Therefore, as discussed before, the adaptive array would null the repeated signal with biphase remodulation and search for the desired signal.

Another type of remodulation to be considered involves the use of plus or minus 90° phase shifts. As can be seen in Table 6, if a "1" bit changes the short code plus data symbol, η_m, an additional plus or minus 90° phase shift occurs. Therefore, the only way to change the data but not the long code is to add plus or minus 90° phase shifts to the signal. However, both the long code symbol and the previous phase or state determine whether a "1" data bit will cause a plus or minus 90° phase shift. Thus, unless the jammer is very sophisticated and

understands the type of system being used, it must guess at whether a plus or minus 90° phase shift should be added. If the wrong phase shift is used, though, as can be seen in Table 6, the long code symbol will be changed. That is, a plus or minus 90° additional phase shift is as likely to change only the data as it is to change the long code symbol. Thus, even with plus or minus 90° remodulation, it is unlikely that the long code shift register will be loaded properly and long code synchronization obtained in the required time. Therefore, as discussed before, the adaptive array will null the repeated signal with plus or minus 90° remodulation and search for the desired signal.

As discussed in considering the repeat jammer with remodulation, it is unlikely that long code synchronization could be obtained in the required time. It is possible for synchronization to occur, however, if the remodulation does not occur during the interval in which the long code symbols are being detected. It should be noted that the jammer has no way of determining when the long code symbols are being detected and, thus, would only be lucky if there were no remodulation during this period.

Although it is unlikely for the long code synchronization to be obtained for the remodulated signal, what would happen if synchronization did occur will now be examined. Once synchronization is obtained, the long code is used to generate the reference signal, as discussed in Chapter V. Since data (or changed long code symbols) are not present on the long code for the desired signal, the bandwidth of the filter in the reference loop is on the order of the frequency uncertainty of the received signal. Therefore, the filter bandwidth is much less than the data bandwidth. If the jammer remodulates the desired signal, then the bandwidth of this signal after mixing with the long code will be wider than the bandwidth of the filter. Thus, the signal will become distorted by the reference loop filter. The generated reference signal will, therefore, become uncorrelated with the received signal, resulting in the nulling of this signal by the adaptive array. Long code timing will then be lost by the delay lock loop. As stated in Chapter V, when the long code is no longer synchronized at the receiver, the entire signal acquisition procedure is started again. Therefore, even in the unlikely event that the long code synchronization is obtained for a repeated signal with remodulation, the adaptive array would not be able to maintain synchronization and would search for the desired signal.

After acquisition of the desired signal by the adaptive array, the repeat jammer with remodulation, like the repeat jammer without remodulation discussed before, will have no effect on the system. Therefore, repeat jammers with remodulation may increase the acquisition time, but they cannot prevent the acquisition of the four-phase signal.

Another type of jammer is one that uses only the short code on a biphase signal. It should be noted that it may be difficult for a jammer to determine the short code since the modulation scheme of the desired signal uses both the short code and the long code. If the short code was determined, however, a jammer could generate a biphase signal with this code to jam this system. This jamming signal would then be as likely to be acquired by the adaptive array as the desired signal. As before, though, since the long code would not be present on this signal, a short period after the acquisition of this signal, the adaptive array would null this signal and begin searching for the desired signal. Thus, this type of jamming would not be effective.

After acquisition of the desired signal, since the adaptive array uses the long code to generate the reference signal, a jamming signal containing only the short code will be treated the same as conventional jamming. Thus, a jammer using the short code on a biphase signal would not be effective after acquisition.

In conclusion, conventional jamming will have the same effect on the four-phase system as it had on the biphase system, i.e., it will be sufficiently reduced in most cases. Most important, though, is the fact that repeat jamming with remodulation cannot jam the four-phase system like it could in the biphase system. It may in some instances increase the acquisition time, however.

CHAPTER XI

AN EXPERIMENTAL SYSTEM

A. Introduction

In this chapter an experimental system is described and experimental results are discussed to verify the feasibility of the four-phase communication system with an adaptive array. In Section B design parameters for the system are determined using the results from Chapters VI through IX. In Section C block diagrams and circuit schematics are developed for the system. Finally, in Section D experimental results are shown and discussed.

B. Design Parameters

In this section the design parameters are determined for an experimental four-phase communication system with an adaptive array. The system developed uses an adaptive array that was previously built for use in a biphase communication system [33]. Thus, some of the design parameters have already been set for the four-phase system, and these parameters are discussed first in this part. Next, several performance requirements, such as the maximum signal acquisition time, are chosen arbitrarily for the system. These parameters are the performance specifications that would typically be determined by the system application. The remaining design parameters are then determined from the above parameters using the results of Chapters VI through IX. Finally, the design parameters determined in this section are shown in Table 10.

The experimental system developed uses an adaptive array which was built previously for use in a biphase communication system. This adaptive array is described in [33]. A delay lock loop, long code acquisition circuitry, and control logic were added to this adaptive array to modify it for use in the four-phase system. However, the filters used in this array were not changed. Because these filters were designed for use with certain code and data rates, these rates were kept the same for the four-phase system. The code rate was, therefore, 175.2×10^3 code symbols per second. With a spreading ratio of 16, the data rate is then 10.95×10^3 data symbols per second. These values have been found to be satisfactory for the four-phase system.

The analysis of Chapters VI through IX shows that there are numerous tradeoffs involved among the design parameters. This greatly complicates the design problem for an arbitrary system. In a typical design problem, however, many of these design parameters would be set by the performance requirements of the system, allowing for the straightforward calculation of the remaining parameters. Therefore, for this experimental system, several performance requirements were set arbitrarily or for convenience to illustrate a typical design analysis.

One such performance requirement is the maximum total lockup time for the signal at the adaptive array. This is the maximum length of time required for the entire four-phase signal acquisition procedure with a given probability of acquisition (usually high) assuming no smart jamming. (The possible effect of smart jamming on the acquisition time is discussed in Chapter X.) In general, this time is desired to be less than one second so that the communication delay due to the acquisition procedure is not noticeable in many applications. Therefore, the maximum total lockup time was chosen to be 0.55 seconds, which was found to be a convenient value. The maximum short code lockup time was then chosen to be 0.4 seconds of the total lockup time with the probability of short code timing acquisition in this time chosen arbitrarily to be 98%. The maximum long code lockup time is, therefore, 0.15 seconds. The probability of long code timing acquisition in this time was set arbitrarily to 99%.

Another parameter which was chosen for convenience is the long code correlation time, which is discussed in Chapter IX. As discussed in this chapter, this parameter would usually be determined after an analysis of the subsequence crosscorrelation of a given code. However, such an analysis is complicated and is not related to the feasibility of the four-phase system. Therefore, this analysis was not performed. In [32], the correlation time considered is approximately twenty times the long code shift register length, n, in code symbol intervals. With this correlation time it was found in [32] that the code had reasonable subsequence correlation properties. Thus, the correlation time for the experimental system was chosen to be $20n\Delta$.

A parameter related to the correlation time is the threshold for the correlation circuitry in the long code acquisition procedure (see Chapter IX). In a typical design problem, this value would also be determined from an analysis of the subsequence crosscorrelation of the long code and the required probability of obtaining the wrong long code timing or missing the correct timing during acquisition. Again, such an analysis is complicated and is not related to the feasibility of the four-phase system. Therefore, the correlation threshold value calculated in [32, p. 41], has been used in this system, $0.66\sqrt{P_S}$.

The final parameter which was chosen rather arbitrarily is the required energy per chip interval to single sided noise density ratio, E_Δ/N_0. This parameter is the lowest value of E_Δ/N_0 for which the adaptive array will acquire the four-phase signal within the required maximum total lockup time. This parameter would normally be determined by the noise environment in which the system is to operate. For the experimental system, an E_Δ/N_0 value of 4 (6 dB) was found to be necessary for acquisition of very long codes in the required time with the given code rate. Since the code rate in this system is much less than that for many communication systems, a lower required E_Δ/N_0 may be possible in many applications. It should be noted from the analyses of previous sections that when the system is operating with an E_Δ/N_0 greater than that required, the probability of acquiring the short and long code timing in the given maximum times will be higher than that specified.

From the above parameters the remaining parameters will now be determined using the results of Chapters VI through IX. In the analysis to follow all numbers (except for the code and data rate and timing jitter) have been rounded to three significant figures.

The first parameter to be considered is the average long code acquisition time. For a 99% probability of acquisition the ratio of the maximum to average long code lockup time is given from Equation (372).

$$y = -2.3 \log(1 - P_{acq}) = 4.6 \tag{383}$$

The average lockup time is, therefore, given by

$$T_{acq} = 175.2 \times 10^3 \text{ code symbols per second} \times \frac{0.15 \text{ second}}{4.6}$$

$$= 5710\Delta \ . \tag{384}$$

The long code shift register length will now be determined. From Figure 50, it can be seen that for a required E_Δ/N_0 equal to 4 with the above average lockup time, about a 40 stage shift register can be used to generate the long code. However, for the calculations for Figure 50 it was assumed that there was no timing jitter at the receiver. With timing jitter the probability of error in the differential detector during the long code acquisition procedure will increase and, therefore, so will the average long code acquisition time. Thus, the long code shift register should be less than 40 stages in length to compensate for timing jitter. The long code was, therefore, chosen to be generated from a 34 stage shift register. From [34, p. 492], the feedback taps to generate a pseudonoise code were chosen to be at stages 1, 2, 27, and 34. The length of the long code is then given by

$$2^{34} - 1 = 1.72 \times 10^{10} \text{ code symbols} \quad , \tag{385}$$

and the code period is given by

$$\text{Long code period} = \frac{1.72 \times 10^{10} \text{ code symbols}}{175.2 \times 10^{3} \text{ code symbols/second}}$$

$$= 9.96 \times 10^{4} \text{ sec (27.7 hours)} \tag{386}$$

The timing jitter that is acceptable during the long code acquisition procedure will now be considered. From Figure 50 it can be seen that for a long code shift register with 34 stages, the average acquisition time is 2700Δ, or about half the average acquisition time for a long code shift register length of 40. Therefore, the acceptable timing jitter is that which causes the average lockup time to double. From Section C of Chapter VIII, for an approximate model of the acquisition procedure, the average long code lockup time is given by Equation (364),

$$T_{acq} = \frac{Mn \quad \Delta}{(1 - \frac{1}{2} \exp(-E_{\Delta}/2N_0))^{n}} \quad . \tag{387}$$

This equation uses the approximation for the symbol error probability, P_E, given by Equation (358),

$$P_E = \frac{1}{2} \exp(-E_{\Delta}/2N_0) \quad . \tag{388}$$

The exact expression for the symbol error probability is plotted in Figure 42 for various values of timing jitter. With no timing jitter and E_{Δ}/N_0 equal to 4, P_E is seen from Figure 42 (as calculated from Equation (357) to be 0.0716. Thus, for the experimental system, the average long code acquisition time, as determined from an approximate model of the long code acquisition procedure, is given by

$$T_{acq} = \frac{20 \times 34 \quad \Delta}{(1 - 0.0716)^{34}} = 8500\Delta \quad . \tag{389}$$

Although this is about three times the actual average long code lockup time, the approximate model can still be used to determine the acceptable timing jitter. As stated before, the acceptable timing jitter is that which causes the acquisition time to double. Thus, for the approximate model, the average acquisition time with timing jitter is given by

$$T_{acq} = 17000\Delta = \frac{20 \times 34}{(1 - P_E)^{34}}\Delta \qquad (390)$$

where P_E is the symbol error probability with timing jitter. The value of P_E is then given by

$$P_E = 1 - \left(\frac{20 \times 34}{17000}\right)^{1/34} = 0.0903 \quad . \qquad (391)$$

As seen in Figure 42 (as calculated from Equation (357)), this is the value of P_E for a timing jitter of approximately 0.06Δ, with E_Δ/N_0 equal to 4. Because the above analysis is not exact, a timing jitter of 0.04Δ was chosen for the system design to help insure acquisition in the specified time.

The optimum loop filter frequency constant, ρ_0, can now be calculated. The first parameter that must be considered to determine ρ_0 is the $S/N|_{IF}$, which is computed as follows. With E_Δ/N_0 equal to 4, the energy per code symbol-to-noise density ratio is equal to 2. Thus, if the bandwidth of the filters through which the received signal is first passed is approximately equal to the code rate, the received signal power in one channel-to-noise ratio, $S/N|_{RF}$, is given by

$$S/N|_{RF} = \frac{1}{2} \cdot E_\Delta/N_0 = 2 \quad . \qquad (392)$$

Thus, from Equation (300), with a spreading ratio of 16, $S/N|_{IF}$ is given by

$$S/N|_{IF} = \frac{k}{\frac{1}{S/N|_{RF}} + \frac{1}{2}} = \frac{16}{\frac{1}{2} + \frac{1}{2}} = 16 \quad (12.0 \text{ dB}) \quad . \qquad (393)$$

As seen in Figure 32 (as calculated from Equation (323)), with $S/N|_{IF}$ as given above and a timing jitter of 0.04Δ, the optimum ρ_0/B_{IF} is equal to 0.0916.

In general the bandwidth of the filters in each channel of the delay lock loop, B_{IF}, will be on the order of the data bandwidth. Thus, for the experimental system, B_{IF} should be about 10.95 kHz. However, since 15 kHz bandwidth filters were readily available, they were used in the delay lock loop. Therefore, the loop filter frequency constant is given by

$$\rho_0 = 0.0916 B_{IF} = 0.0916 \times 15 \text{ kHz} = 1.37 \text{ kHz} \quad . \qquad (394)$$

The next parameter to be considered is the short code length. With the maximum short code acquisition time equal to 0.4 seconds and a code rate of 175.2×10^3 code symbols per second, the maximum length of the short code is given by Equation (148),

$$N \leq \sqrt{\tau_{acq} \cdot \text{code rate}} = \sqrt{.4 \times 175.2 \times 10^3} = 265 \quad . \tag{395}$$

Thus, for a pseudonoise code generated from a linear feedback register, the maximum short code length is given by

$$N' = 2^8 - 1 = 255 \quad . \tag{396}$$

Thus, an eight stage shift register will be used to generate the short code. From [34, p. 476], the feedback tops were chosen to be at stages 1, 6, 7, and 8.

For a length 255 short code, the maximum acquisition time is given by

$$\tau_{acq} = \frac{(N')^2}{\text{code rate}} = \frac{255^2}{175.2 \times 10^3} = 0.371 \text{ seconds} \tag{397}$$

Therefore, the final transient time (as discussed in Chapter VI) must be less than 0.029 seconds for the maximum total short code acquisition time to be less than 0.4 seconds. From Figure 24, the final transient time is seen to vary from $8/\rho_0$ to $2/\rho_0$ or, for ρ_0 equal to 1.37 kHz, from 0.00582 seconds to 0.00146 seconds. Thus, as required, the maximum total short code acquisition time is less than 0.4 seconds.

The sweep rate will now be determined. From Equation (151), the sweep rate for the experimental system is given by

$$f_s = \frac{\text{code rate}}{N'} = \frac{175.2 \times 10^3 \text{ code symbols per second}}{255 \text{ code symbols}}$$

$$= 687 \text{ Hz} \quad . \tag{398}$$

The optimum bandwidth of the sum channel filter is then given by Equation (227),

$$B_n|_{opt} = 0.53 \, f_s = 0.53 \times 687 \text{ Hz} = 364 \text{ Hz} \quad . \tag{399}$$

The probability of acquiring the wrong code timing during the short code acquisition procedure and the acquisition threshold for the delay lock loop will now be considered. For the experimental system N'/k is given by

$$\frac{N'}{k} = \frac{255}{16} = 15.9 \quad . \tag{400}$$

During acquisition the $S/N|_{IF}$ is given by (see Equation (291))

$$S/N|_{IF} = \frac{k}{\frac{1}{S/N|_{RF}} + 2} \quad . \tag{401}$$

However, because the delay lock loop is coupled to the adaptive array, the $S/N|_{RF}$ will change during acquisition. Initially during acquisition, the array rejects the desired signal and, therefore, the $S/N|_{RF}$ will be very small. When the code timing offset becomes less than half a chip, the array pulls the desired signal out of the noise and increases $S/N|_{RF}$. For the experimental system with a minimum E_Δ/N_o equal to 4, $S/N|_{RF}$ will increase to 2 when acquisition occurs. With $S/N|_{RF}$ equal to 2,

$$S/N|_{IF} = \frac{16}{\frac{1}{2} + 2} = 6.4 \quad (8.1 \text{ dB}) \quad . \tag{402}$$

From Equation (214), Chapter VI, (and as seen in Figure 28) with $S/N|_{IF}$ equal 6.4, the probability of false alarm during acquisition, P_{fa}, can be calculated. For a probability of miss equal to 0.02, P_{fa} is equal to .0573 with the acquisition threshold equal to .718 $\sqrt{P_S}$. It should be noted that with this value of P_{fa}, the maximum short code acquisition time will be increased by only about 5.73% (as compared to the case where P_{fa} is equal to 0). Therefore, the maximum short code acquisition time will remain below 0.4 seconds. The calculation of P_{fa} from Equation (214), Chapter VI, does not consider that an array is coupled to the delay lock loop. Because of the array, in the experimental system, P_{fa} will be less than 0.0573. Therefore, the maximum short code acquisition time will remain below 0.4 seconds.

Finally, the average total lockup time for the system will now be determined. For the short code acquisition, the average acquisition time is just half the maximum time or 0.2 seconds. For the long code, as given in Equation (383), the average acquisition time is 1/4.6 times the maximum time of 0.15 seconds. Therefore, the average total lockup time is 0.233 seconds.

The parameters determined in this section are listed in Table 10. These parameters are used in Section C in the design of the experimental system.

Table 10

Design Parameters for an Experimental Four-Phase System

Parameter	Value
Code rate	175.2×10^3 code symbols/second
Spreading ratio	16
Data rate	10.95×10^3 data symbols/second
Maximum total lockup time	0.55 seconds
Maximum short code lockup time	0.4 seconds
Maximum long code lockup time	0.15 seconds
Probability of acquiring short code in maximum time	98%
Probability of acquiring long code in maximum time	99%
Long code correlation time	$20n\Delta$ (680Δ)
Long code correlation threshold	$0.66\sqrt{P_S}$
Minimum E_Δ/N_0	4 (6 dB)

Table 10 (Continued)

Average long code lockup time	5710Δ (0.0326 seconds)
Long code:	
(a) Length	1.72×10^{10} code symbols
(b) Shift register length	34 stages
(c) Shift register feedback taps	stages 1, 2, 27, 34
(d) Period	27.7 hours
Timing jitter during tracking of the short code	0.04Δ
$S/N\|_{IF}$ during acquisition	6.4 (8.1 dB)
$S/N\|_{IF}$ during tracking	16.0 (12.0 dB)
Loop filter frequency constant	1.37 kHz
Short code:	
(a) Length	255 code symbols
(b) Shift register length	8 stages
(c) Shift register feedback taps	stages 1, 6, 7, 8
(d) Period	1.46 milliseconds
Delay lock loop sweep rate	687 Hz
Sum channel filter bandwidth	364 Hz
Probability of acquiring wrong short code timing in the delay lock loop	5.73%
Acquisition threshold for sum channel in the delay lock loop	$0.718\sqrt{P_S}$
Average total lockup time	0.233 seconds

C. Circuit Design

In this section the circuitry for the four-phase system is described. A block diagram of the four-phase system to be described is shown in Figure 54. As seen in this figure the four-phase system consists of a transmitter and a receiver. The receiver has been divided into five subsystems, the adaptive array, the reference loop, the delay lock loop, the long code acquisition circuitry, and the control logic. In this section a block diagram and circuit schematic are developed for the transmitter and each receiver subsystem. The design parameters of Section B are used in the design of the system.

The first subsystem to be described is the transmitter. As given in Table 10, the transmitter design parameters include a code rate of 175.2×10^3 code symbols per second, a spreading ratio of 16, and a data rate of 10.95×10^3 data symbols per second. Also, as seen in Table 10, the short code is generated from an eight stage linear feedback shift register with feedback taps at stages 1, 6, 7, and 8, and the long code is generated from a 34 stage linear feedback shift register with feedback taps at stages 1, 2, 27, and 34.

A block diagram of the transmitter is shown in Figure 55. As seen in this figure a long code and a short code mixed with pseudorandom data symbols generated at a rate corresponding to the spreading ratio are generated first. Using two delay flip-flops these symbols are then converted to the symbols corresponding to the phase of the four-phase differential phase shift keyed signal. These symbols are then used to control the output phase of a quadriphase modulator. The output of this quadriphase modulator is then the four-phase signal given by Equation (142), with a carrier frequency of 70 MHz. A very stable external 70 MHz frequency source was used for the carrier frequency input to the transmitter.

A circuit schematic corresponding to the block diagram of the transmitter is shown in Figure 56. Several switches have been added to this circuit for use in the testing of the system as described in Section D.

The next subsystem to be considered is the channel simulator. The purpose of the simulator is to generate the signals to be processed by the receiver in such a way as to simulate the signal that would be received if antenna elements were employed. By using a channel simulator the system can be tested without the need for antenna elements and RF components. A block diagram of the channel simulator is shown in Figure 57.

As shown in this figure, the transmitted signal (which is at 70 MHz) is divided four ways because the adaptive array in the experimental system is designed for use with four antenna elements. Interference

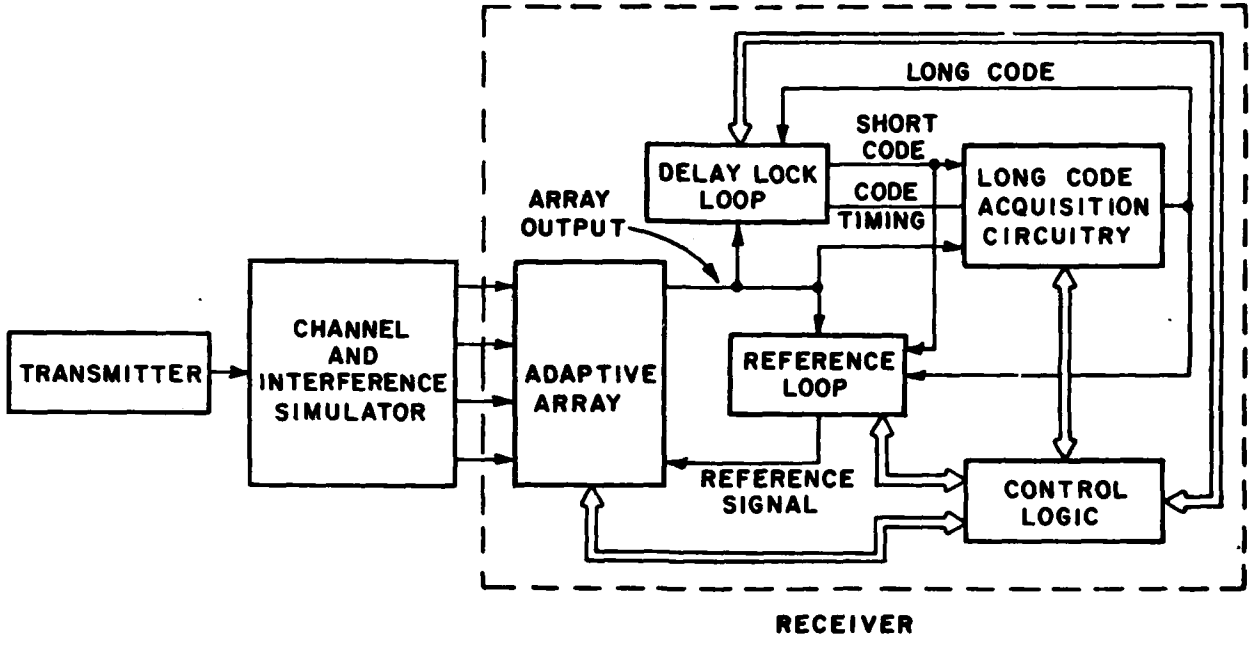


Figure 54. Block diagram of the experimental four-phase communication system with an adaptive array at the receiver.

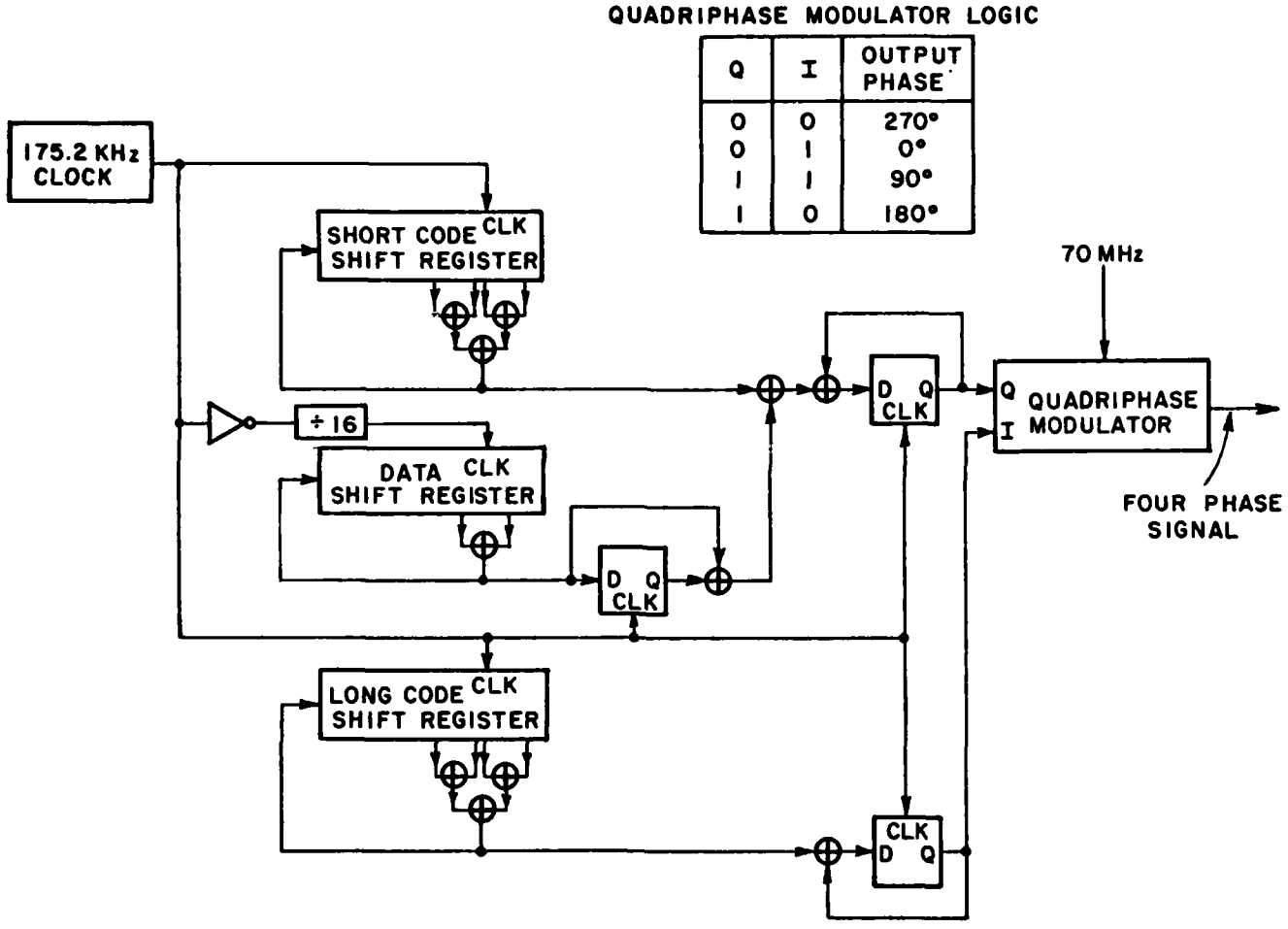


Figure 55. Block diagram of the transmitter.

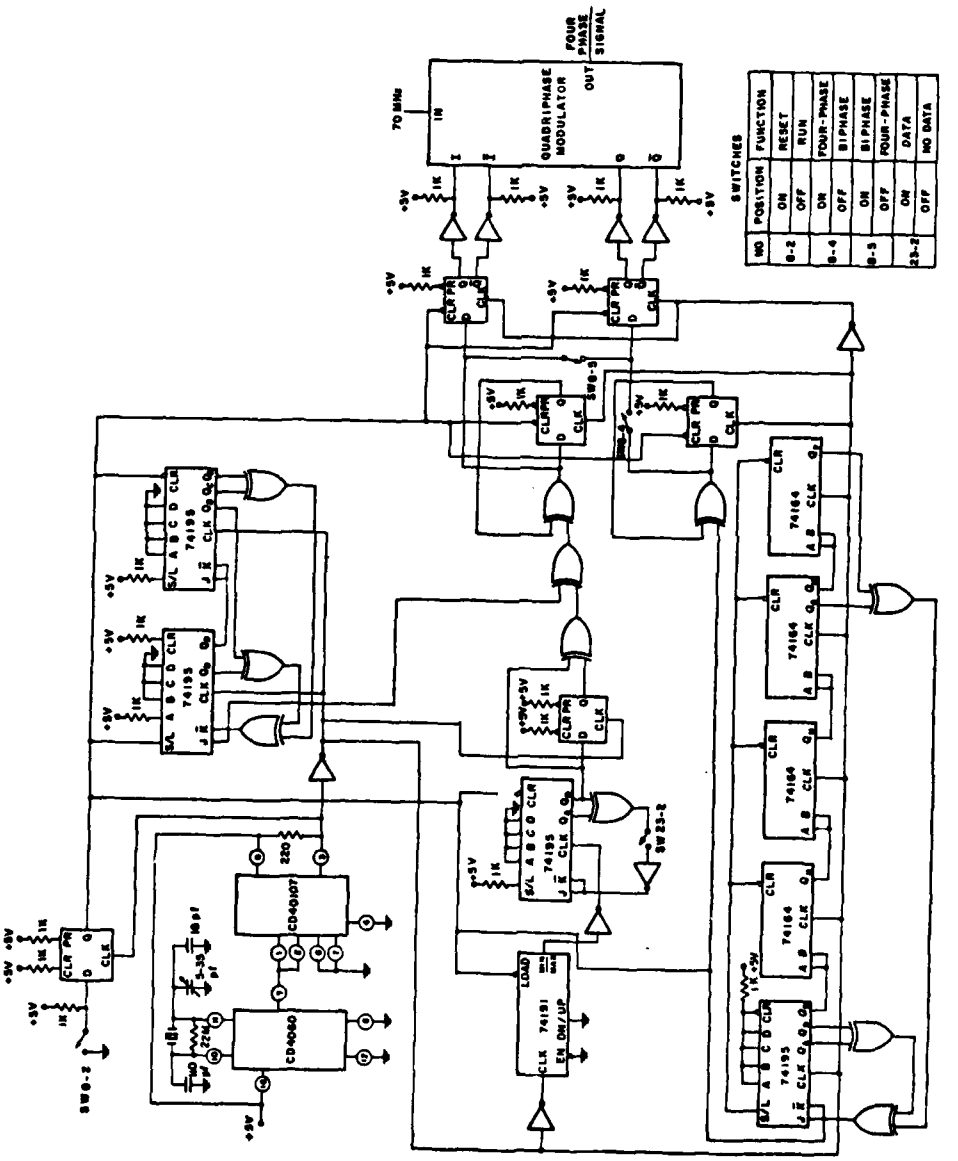


Figure 56. Circuit schematic of the transmitter.

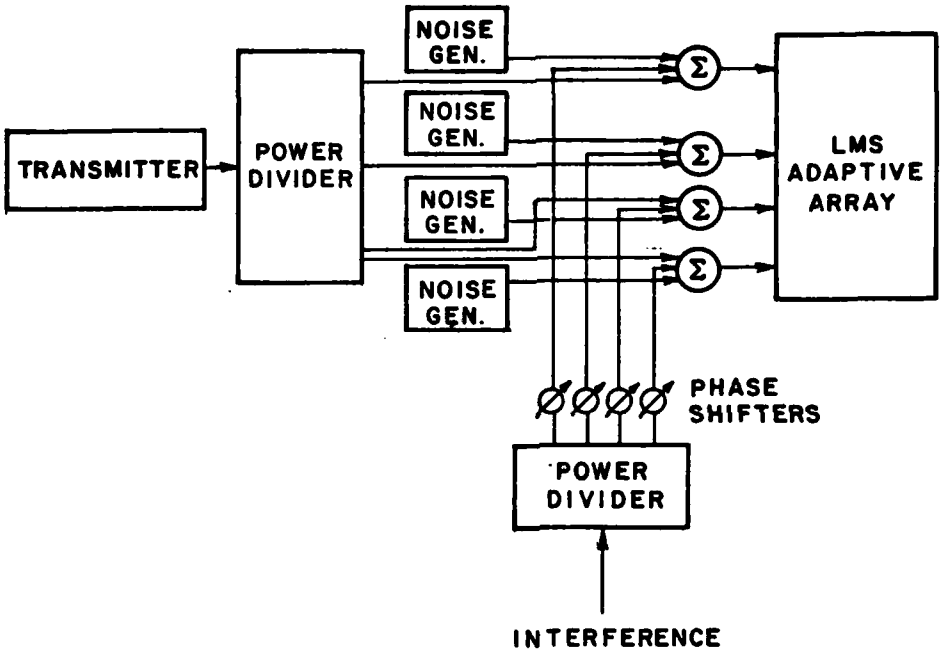


Figure 57. Block diagram of the channel simulator.

is also divided four ways and each of the four interference signals is passed through phase shifters. By adjusting the phase shift of each signal, the simulated angle of arrival of the interference on the adaptive array can be changed. Since the desired signal is not phase shifted, it is always incident on the receiving array at broadside in the simulation. Independent sources add noise to each of the four signals to simulate the received noise on each antenna element. Thus, the channel simulator simulates a communication channel with a four element receiving antenna array, with the desired signal arriving at broadside and interference arriving at any angle.

The next subsystem to be considered is the adaptive array, i.e., the circuitry for implementation of the LMS algorithm. As stated before, the adaptive array employed in the system was built previously for use in a biphase system and is described in [33]. The code rate, spreading ratio, and data rate used in the experimental system were kept the same as those used in the biphase system to minimize changes in this adaptive array. However, this array was designed for use in a biphase system where code synchronization was obtained at the transmitter rather than at the receiver with the adaptive array (with the transmitter and receiver as used in this paper), which is opposite of the four-phase experimental system. Thus, some modifications to this array were required.

A functional diagram of the LMS algorithm implementation is shown in Figure 58 (Figure 11, [33]). To the left of the dashed line in this figure is the circuitry which is contained in each of four weight boxes, one for each antenna element. To the right of the dashed line is the circuitry in which the outputs of the four weight boxes were combined and an error signal for each weight box was generated. As seen in Figure 58, this circuitry requires inputs of the received signal from each antenna element (through an IF amplifier), the reference signal from the reference loop, and four control signals. These control signals are the HRF/LRF, weight reset, integrate/hold and error on/off TTL inputs. The function of these control signals and their use in the four-phase system are described below.

The HRF/LRF TTL input is used to control the gain of the amplifier shown in Figure 58, based on whether the high rate format or low rate format of the array is used. The code rate and spreading ratio for the four-phase system is the low rate format as described in [33]. Thus, for the four-phase system, the HRF/LRF TTL input was set low using a switch on the front panel of the array.

The weight reset TTL input is used to reset the integrators (the weight values) to some fixed value. This fixed value was set at 1 for the in-phase weight in one weight box and zero for all other weights so that the antenna pattern is fixed at the pattern for one element. For signal acquisition, the weights are first reset by applying a high

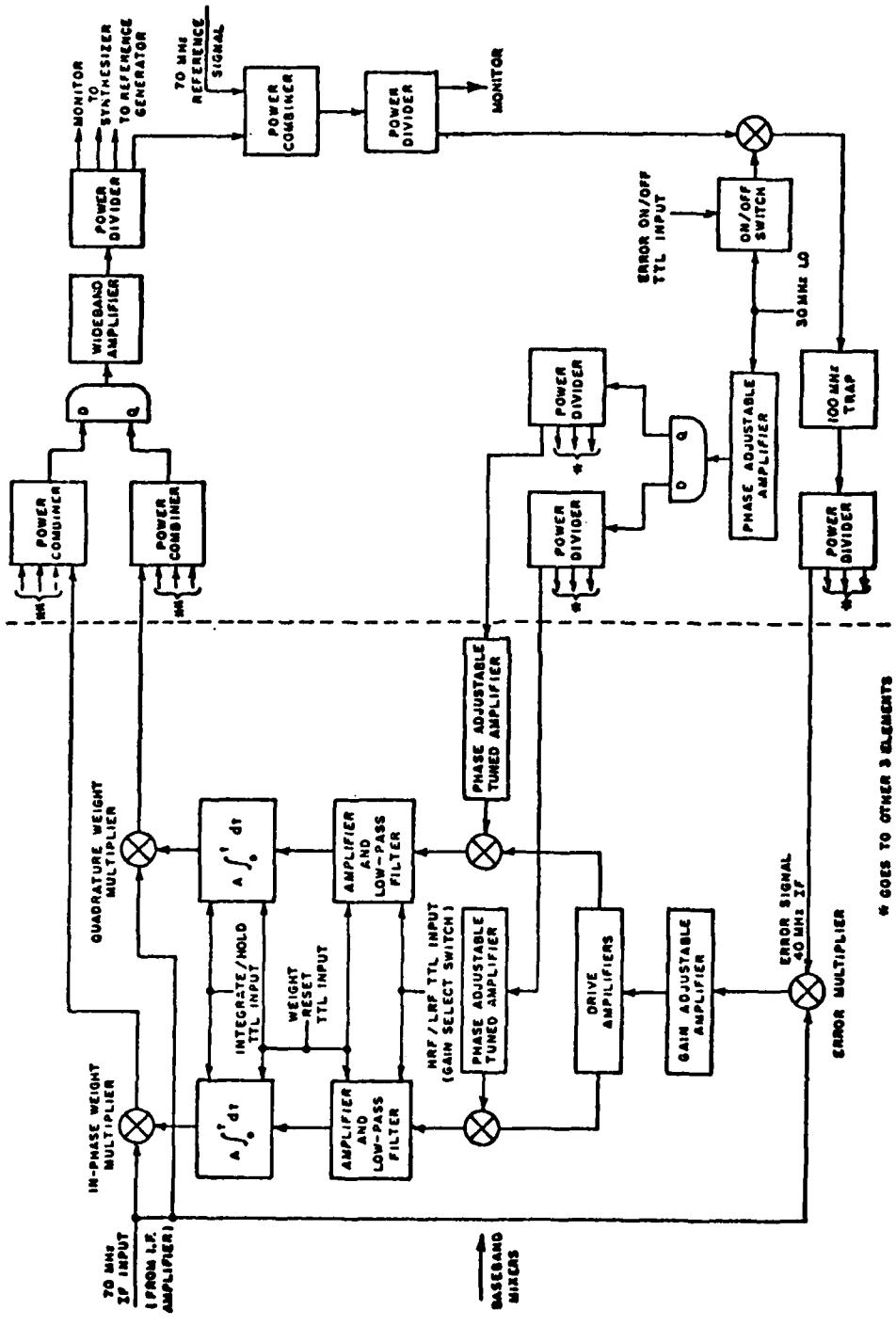


Figure 58. Functional diagram of the LMS algorithm implementation.

voltage to the weight reset TTL input, and then with a low voltage at the input the adaptive process is begun. Thus, in the four-phase system the weight reset TTL input was generated by the control logic which controls when signal acquisition is to begin. The control logic is described later in this section.

The integrate/hold TTL input is used to hold the value of the integrator output (the weight value) or to allow integration (adaption) to occur. The error on/off TTL input is used to turn the error signal on and off. These signals are dependent on the weight reset TTL input signal. That is, when the weight reset TTL input signal is high, the values of the integrator outputs are held and the error signal is turned off. When the weight reset TTL input is low, integration (adaption) occurs and the error signal is on. Thus, the integrate/hold TTL input signal and the error on/off TTL input signal are the complement of the weight reset TTL input signal.

The next subsystem of the receiver to be considered is the reference loop, which generates the reference signal for the adaptive array. A block diagram of the reference loop is shown in Figure 59, and is described below.

The locally generated code shown in the figure is either the long or the short code, depending on which code the delay lock loop is tracking. The code modulates a local oscillator signal, and the modulated signal is then mixed with the array output signal. The resultant signal contains a despread component of the desired signal when the locally generated code is synchronized with the code in the received signal. The resultant signal is then passed through a bandpass filter whose output consists mainly of the despread component of the desired signal. The signal is then hardlimited so that the reference signal has constant amplitude. Finally, the hardlimited signal is mixed with the locally generated code to generate the array reference signal. The array reference signal will consist primarily of the desired signal component when the locally generated code is properly synchronized.

The reference loop used in the experimental system was built previously and is described in [33]. As discussed before, the system described in [33] was designed for use in a biphase system where code synchronization was obtained at the transmitter rather than at the receiver with the adaptive array (with the transmitter and receiver as used in this paper). Therefore, the reference loop was modified for use in the four-phase system. The code used in the reference loop was generated in the delay lock loop rather than in the reference loop itself as in [33]. The circuitry in the reference loop was not changed, though. Thus, as described in [33], the bandwidth of the bandpass filter was 28 kHz.

The next subsystem to be considered is the delay lock loop. The purpose of the delay lock loop is to acquire and track the short code

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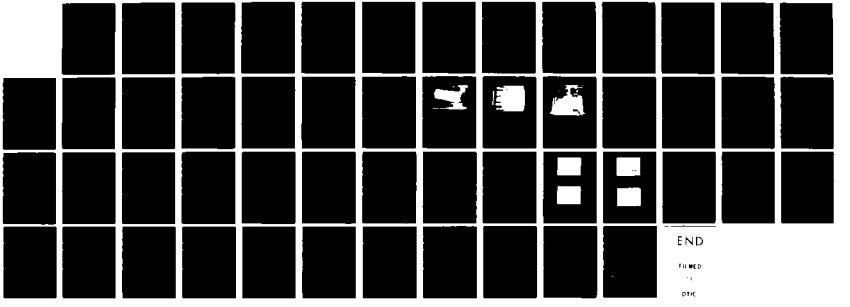
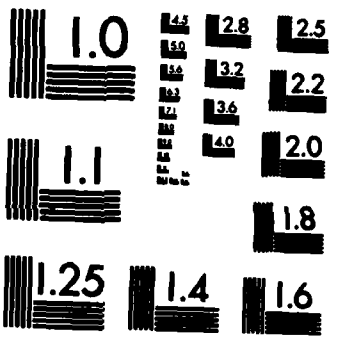




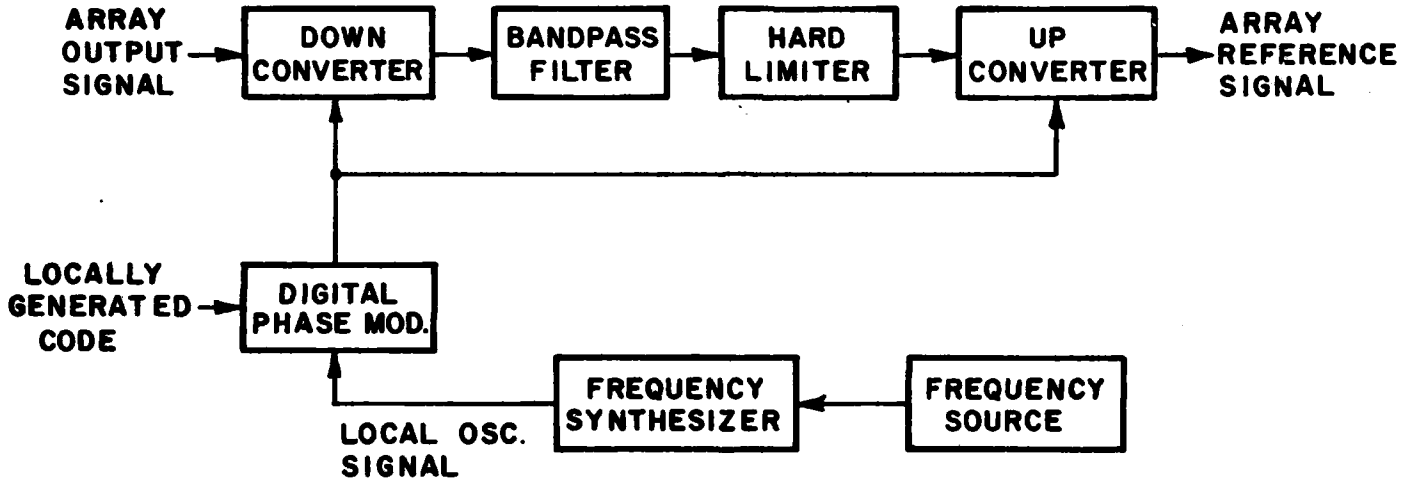


Figure 59. Block diagram of the reference loop.

timing and to track the long code timing. A block diagram of the delay lock loop designed for the experimental system is shown in Figure 60. A detailed analysis of this subsystem is contained in Chapters VI and VII.

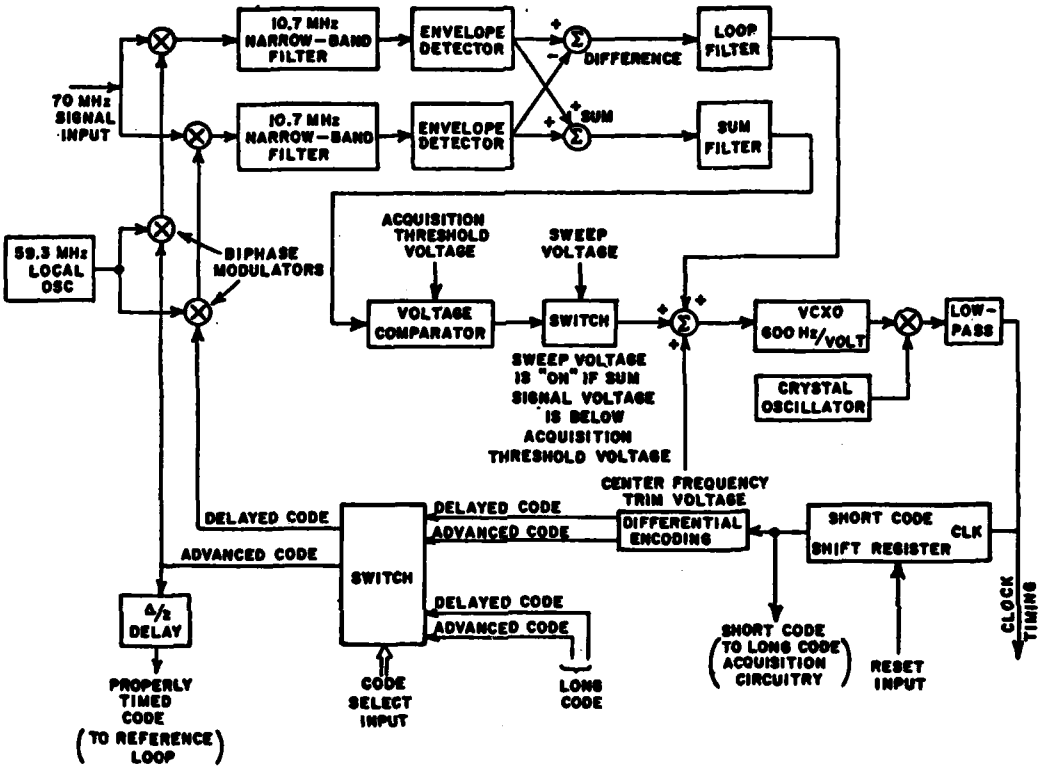


Figure 60. Block diagram of the delay lock loop.

The inputs to the delay lock loop are the array output signal, the half chip advanced and delayed long code, the code select input, and the reset input. With these signals the delay lock loop generates the clock timing for the received signal's code, the short code for use in the long code acquisition circuitry and the properly timed code for use in the reference loop.

A major portion of the delay lock loop used in the experimental system was built previously, and is described in [36]. The circuitry was extensively modified, including the removal of squarer and square rooter devices. These devices were found not to be necessary as discussed in Chapters VI and VII. Circuit schematics for the delay lock loop are presented in Figures 61 through 64. The function of these circuits and the parameters from Section B used in their design are discussed below.

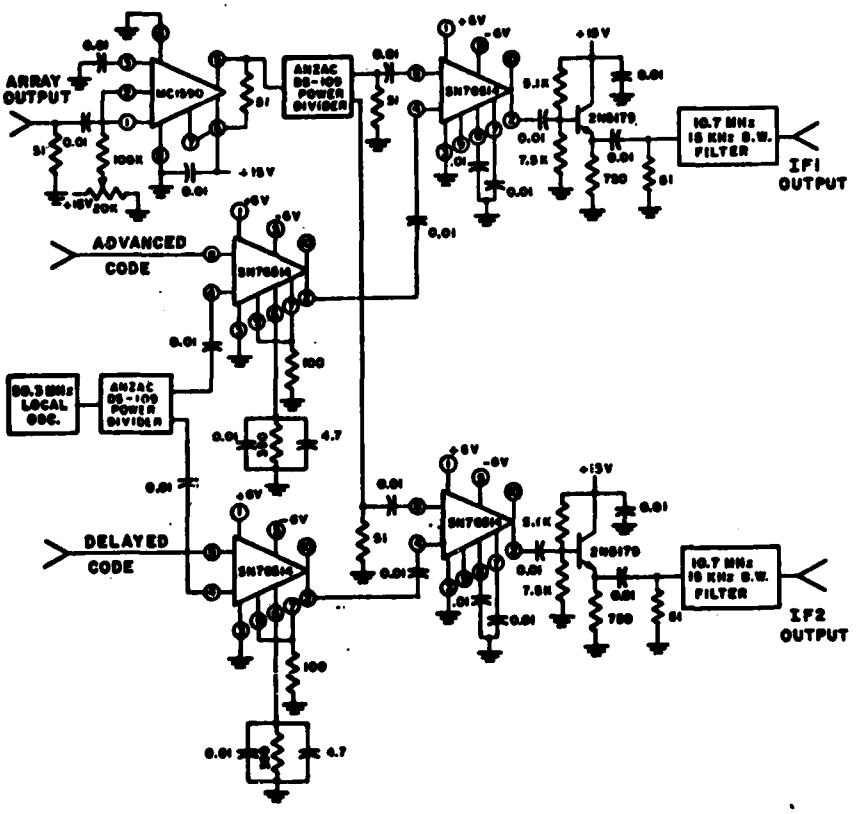


Figure 61. Circuit schematic of the modulators and mixers in the delay lock loop.

As shown in Figure 61, the array output is amplified and split into two channels. The half chip advanced and delayed codes modulate 59.3 MHz signals, and these modulated signals are mixed with the array output. The resultant signal in each channel will contain the despread component of the desired signal when the locally generated code is synchronized with the received signal's code. Thus, the resultant signal in each channel is passed through a narrowband, 10.7 MHz center frequency filter to remove most of the unwanted signals. As discussed in Section B, the data rate is 10.95 kbits per second. The filter bandwidth, therefore, should be on the order of 10.95 kHz. Two filters with 15 kHz bandwidths were employed because they were available.

The circuitry used for envelope detection of the two filtered signals is shown in Figure 62. It should be noted that the circuitry is somewhat different in each envelope detector. These differences were present in the original delay lock loop described in [36] and were left unchanged in the four-phase system. In each channel the signal is first amplified. The signal is then hardlimited and mixed with the nonhardlimited signal. Thus, the output of the mixer contains a signal proportional to the envelope of the filtered signal plus

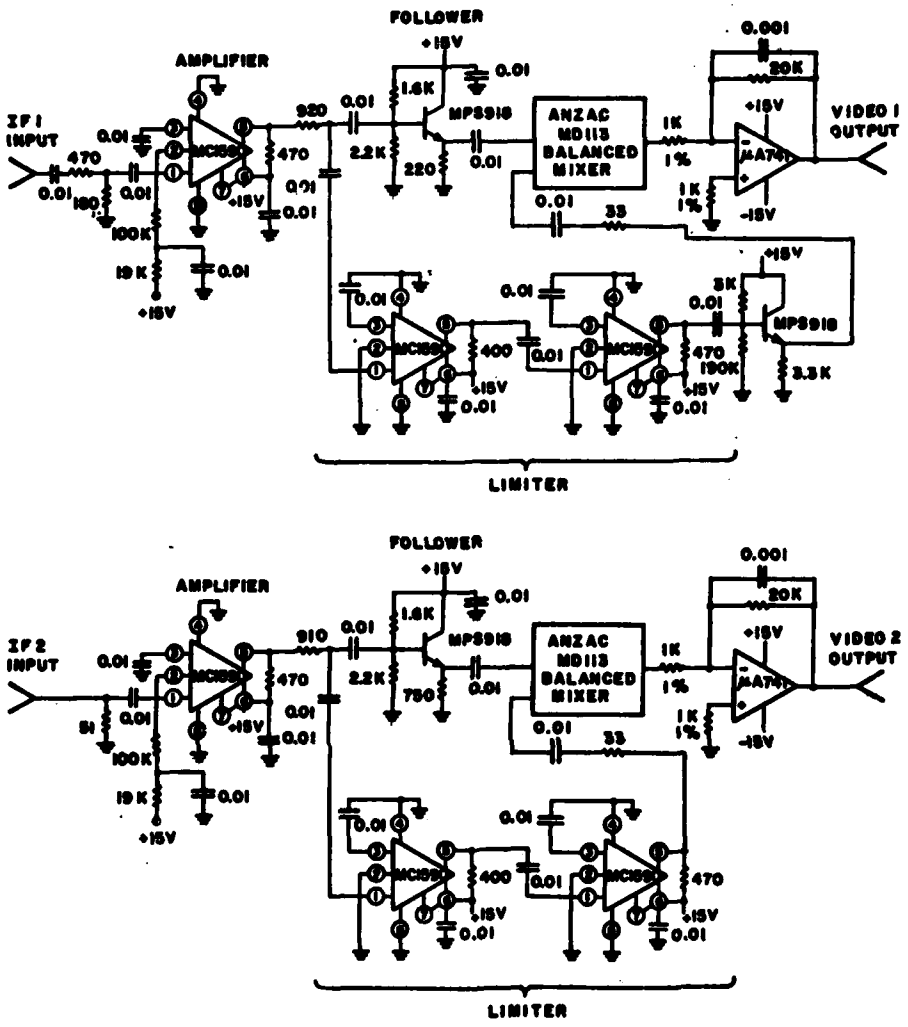


Figure 62. Circuit schematic of the envelope detector in the delay lock loop.

components around 21.4 MHz. The double frequency components are removed by a lowpass active filter containing a μA741 operational amplifier. The cutoff frequency of this filter was chosen to be much higher than that of the sum and the loop filters. Thus, the low pass filter will have a negligible effect on the delay lock loop performance. As seen in Figure 62, a 20 kΩ resistor and a 0.001 μf capacitor are used. Therefore, the cutoff frequency is given by

$$f = \frac{1}{2\pi RC} \tag{403}$$

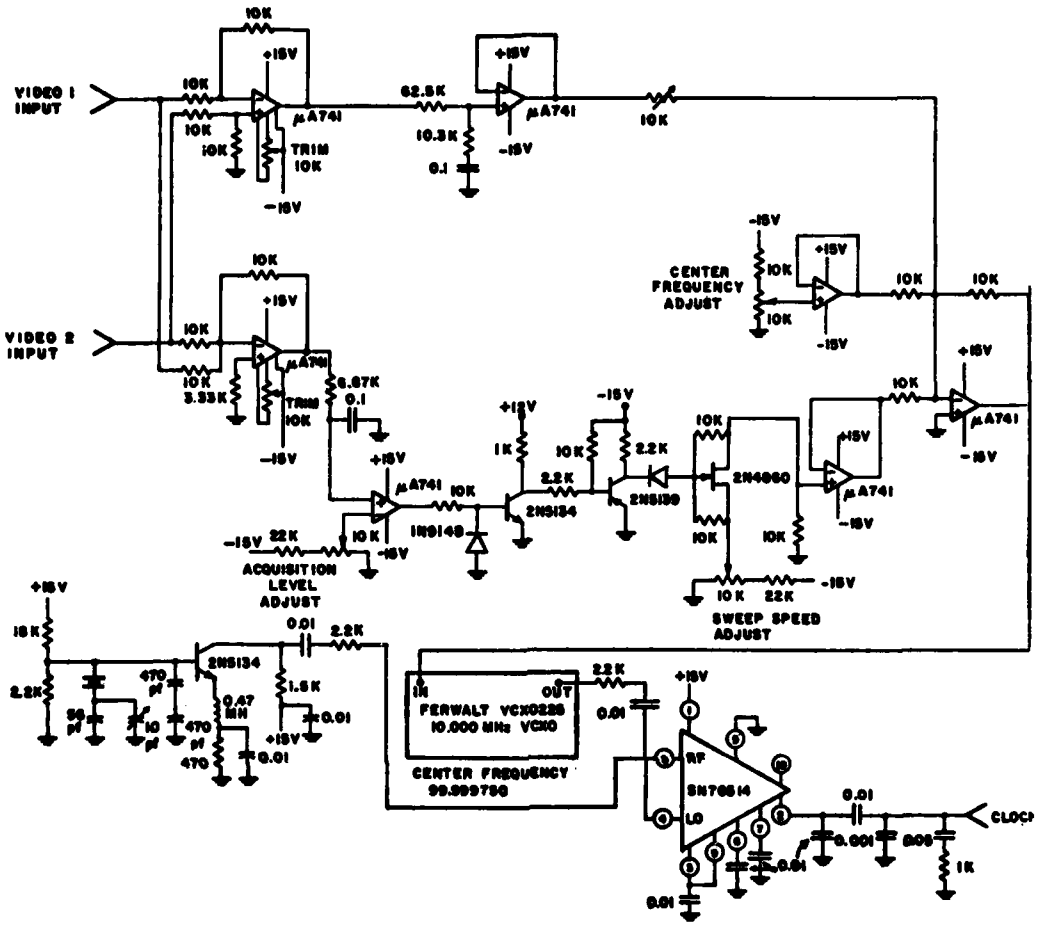


Figure 63. Circuit schematic of the sum and difference channels in the delay lock loop.

$$= \frac{1}{2\pi \times 20 \times 10^{3} \times 0.001 \times 10^{-6}} \qquad (404)$$

or,

$$f \approx 7.96 \text{ kHz} \quad . \qquad (405)$$

In Figure 63, a schematic is shown of the circuitry used to generate the clock from the outputs of the envelope detectors. As shown in this figure, the difference and the sum voltages are determined for the outputs of the detectors. The difference voltage out of the operational amplifier shown at the top of the schematic is passed through the loop

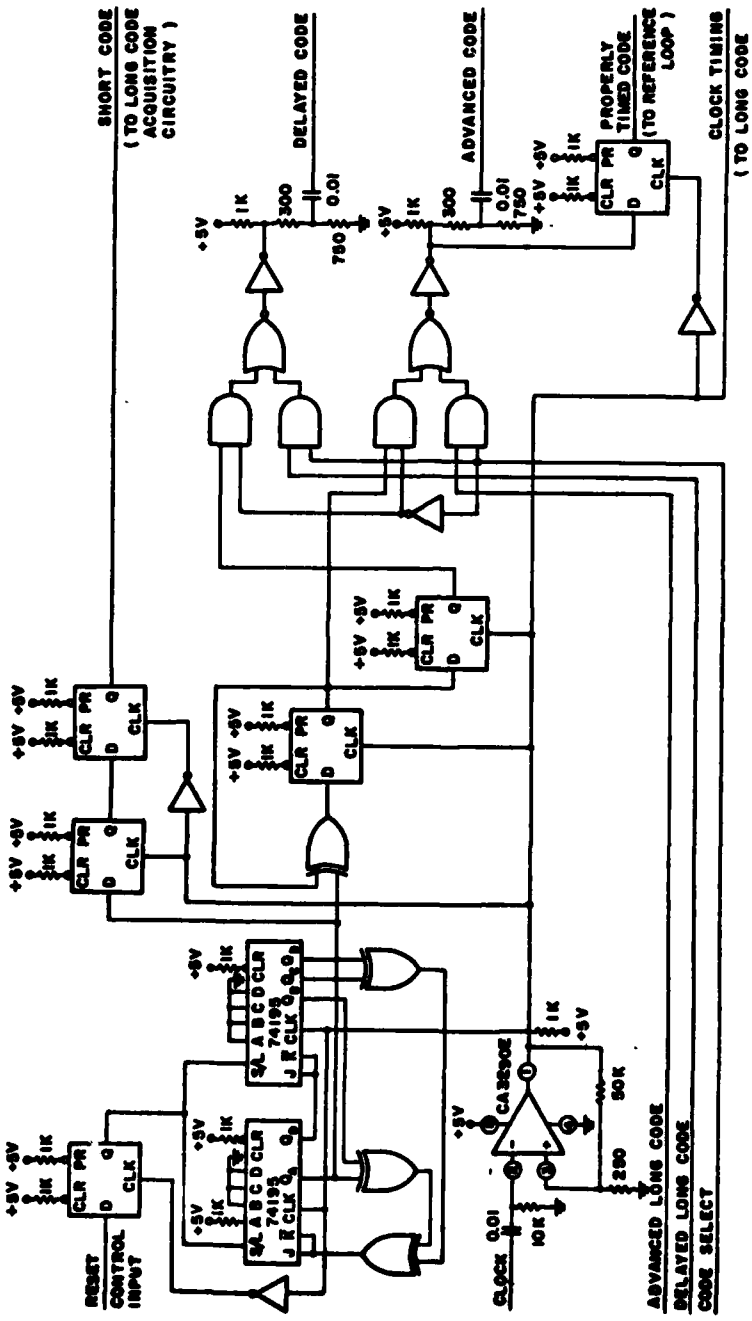


Figure 64. Circuit schematic of the short code shift register and code select logic.

filter. As determined in Section B, the loop filter frequency constant is 1.37 kHz. The values of the resistors and capacitor in the loop filter were determined from the equations given in [6, page 545].

For the sum channel, a filter of bandwidth 364 Hz was determined in Section B. With an RC lowpass filter, the bandwidth is given by

$$B_n = \frac{1}{4RC} = 364 \text{ Hz} \quad . \tag{406}$$

Let,

$$C = 0.1 \ \mu f \quad , \tag{407}$$

then

$$R = \frac{1}{4 \times 0.1 \times 10^{-6} \times 364} \approx 6.87 \ k\Omega \tag{408}$$

The above values were used in the circuitry shown in Figure 63.

The voltage out of the sum channel filter is compared to the acquisition threshold voltage using an operational amplifier. As given in Section B, this voltage was adjusted to $0.718\sqrt{P_S}$ in the circuit. The output of the voltage comparing operational amplifier turns the sweep voltage on and off by the use of a series of transistors. The sweep voltage was set so that the voltage caused a 687 Hz increase in the frequency of the voltage controlled crystal oscillator (VCXO) as specified in Section B. Furthermore, the center frequency adjust voltage was set so that the clock frequency was 175.2 kHz (the code rate) when the sweep voltage was off.

Using an operational amplifier, the difference channel voltage, center frequency adjust voltage and the sweep speed adjust voltage are summed. The combined voltage is used to control the output frequency of a VCXO. The output of this VCXO is mixed with a constant frequency source. The frequency of this source is such that the difference in frequency between the source and the center frequency of the VCXO is 175.2 kHz. Therefore, after low pass filtering the clock output is a sinusoidal waveform with frequency near 175.2 kHz.

In Figure 64 the circuit schematic for the short code shift register and the code select logic is shown. As seen in this figure the sinusoidal clock waveform is converted to a TTL signal by using a CA3290 voltage comparator. This TTL signal is used to clock the short code shift register. As given in Section B, an eight stage shift

register was used with feedback taps at stages 1, 6, 7, and 8. A reset signal is used to initialize the shift register to contain a "1" in stage 1 and "0" in the other stages.

The short code symbols are differentially encoded so that a "1" causes a change in the output symbol stream and a "0" does not cause a change. The differential encoding is accomplished with an exclusive-or gate and a D flip-flop. The output symbol stream is the advanced code. The symbol stream is delayed one clock period to generate the delayed code.

The code select input is used by the control select logic to control whether the short code or the long code differentially encoded symbols are to be used in the delay lock loop. The chosen symbols are converted from TTL level signals to plus-and-minus one volt signals using the circuitry shown. The plus-and-minus one volt signals are used to modulate the 59.3 MHz signal as shown in Figure 61. The advanced code symbols are delayed half a clock period to generate the properly timed code used in the reference loop.

As shown at the top of Figure 64, the short code symbols are delayed one and one-half clock periods for use by the long code acquisition circuitry. By delaying the code this amount the short code symbols are synchronized with the properly timed code symbols sent to the reference loop.

The next subsystem to be considered is the long code acquisition circuitry. The purpose of the subsystem is to acquire the timing of the long code. A block diagram of the long code acquisition circuitry is shown in Figure 65. A detailed analysis of the subsystem is contained in Chapter VIII.

The inputs to the long code acquisition circuitry are the array output, short code timing, and the short code symbols. With these inputs the circuitry generates the properly timed long code.

In Figure 66 a block diagram of the differential detector is shown. As seen in this figure, the array output is divided into two channels. The array output is mixed with a 70 MHz signal in one channel and with the 70 MHz signal phase shifted ninety degrees in the other channel. The resultant signals are the baseband components of the array output. $e_x(t)$ is the baseband component of the array output in phase with the 70 MHz signal and $e_y(t)$ is the inquadrature baseband component. The baseband components are integrated over each code symbol and the outputs of the integrators are sampled and held. The control logic for the integrators and sample-and-holds is shown in Figure 67 and described below. The integrate and sample-and-hold circuitry is shown in Figure 68 and also described below. The outputs of the integrate and sample-and-hold circuitry are then inphase and inquadrature signal vectors corresponding to the m and m-1 code symbols. With these signal vectors,

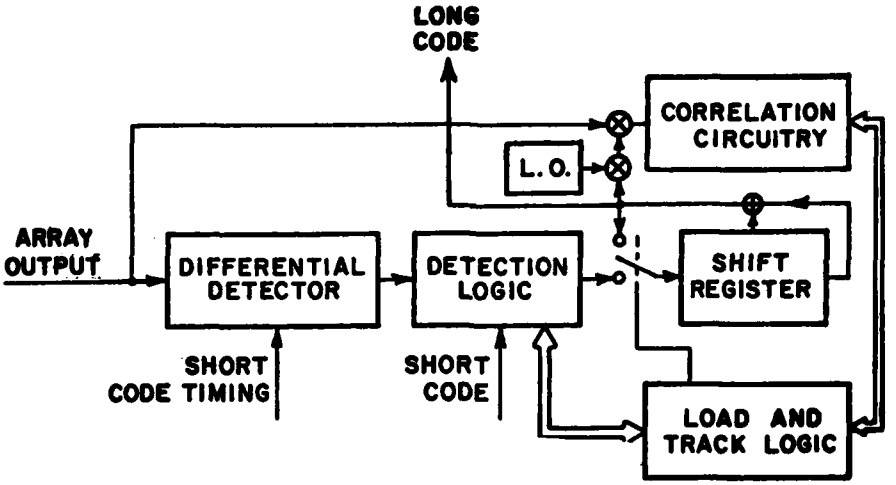


Figure 65. Block diagram of the long code acquisition circuitry.

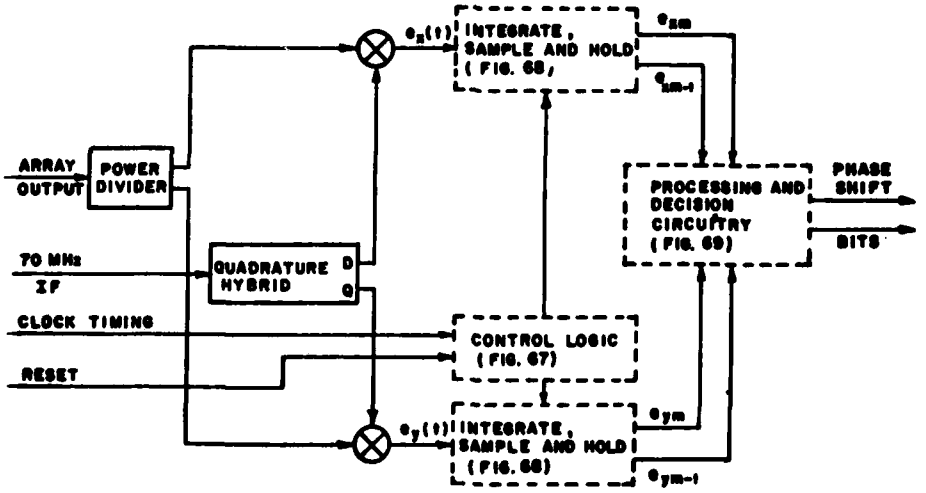


Figure 66. Block diagram of the differential detector.

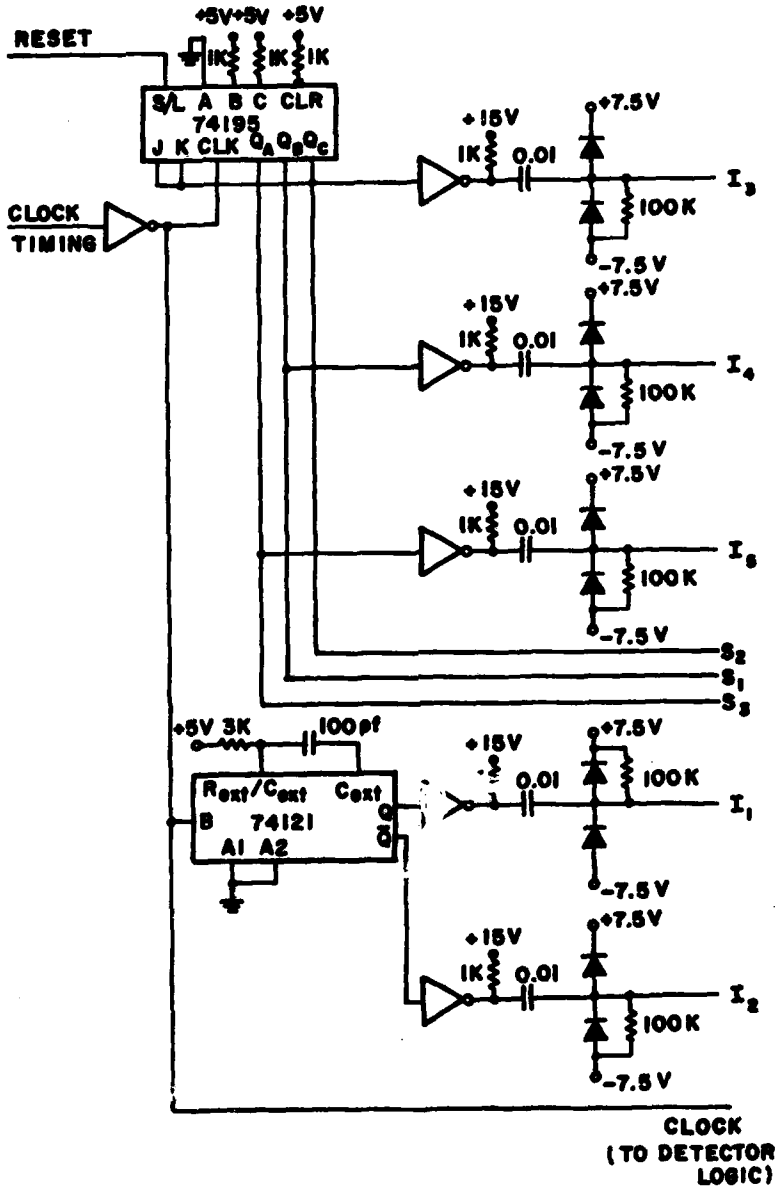


Figure 67. Circuit schematic of the differential detector control logic.

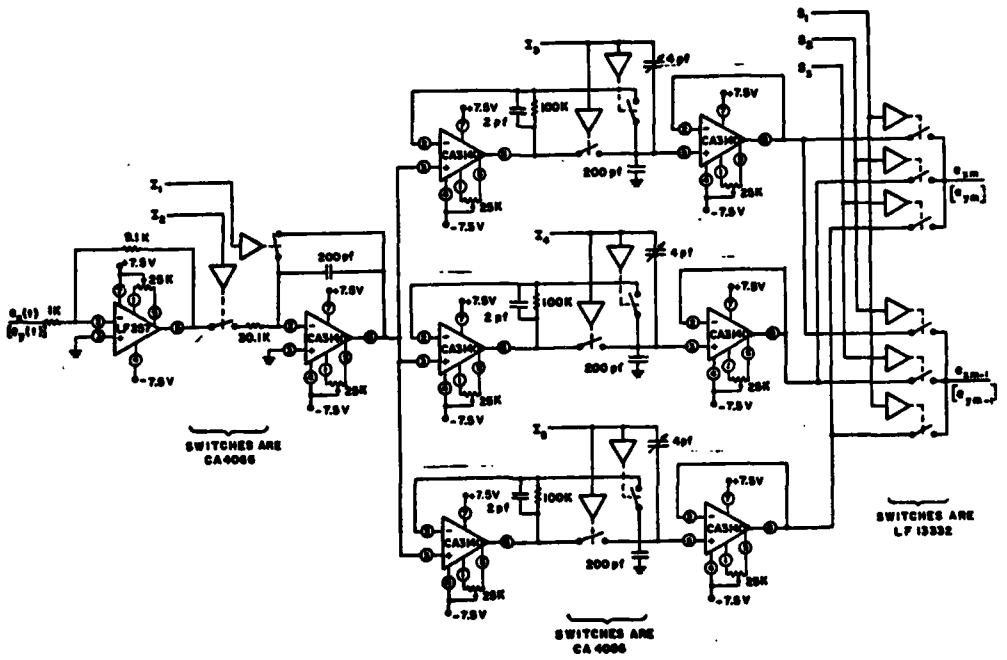


Figure 68. Circuit schematic of the integrate and sample-and-hold circuitry for the $e_x(t)$ [$e_y(t)$] channel.

the processing and decision circuitry shown in Figure 69 determines the phase shift between each code symbol interval. Two phase shift bits are necessary to represent the four possible phase shifts. The processing and decision circuitry is discussed below.

The control logic for the differential detector is shown in Figure 67. This logic generates the signals which control the switches on the integrators and sample-and-holds, and gate the output of these devices. The control signals are generated with a shift register and with a monostable multivibrator (74121). Several of the control signals are converted from TTL level signals to plus-and-minus 7.5 volt signals required by the switching circuitry. Conversion is accomplished with the inverter, diodes, resistors and capacitor shown for each control signal. The control signals for the integrators are labelled I_1 and I_2. Control signal I_1 is high for the integration and low during the dumping of the integrator output at the end of each code symbol interval. Control signal I_2 is the complement of I_1. These control signals are generated by the monostable vibrator shown at the bottom of Figure 67. The device is clocked by the code timing and with a 3 kΩ resistor and 100 pf capacitor generates a 200 nanosecond pulse each clock period. Thus, the integrator will integrate for all but 200 nanoseconds of each

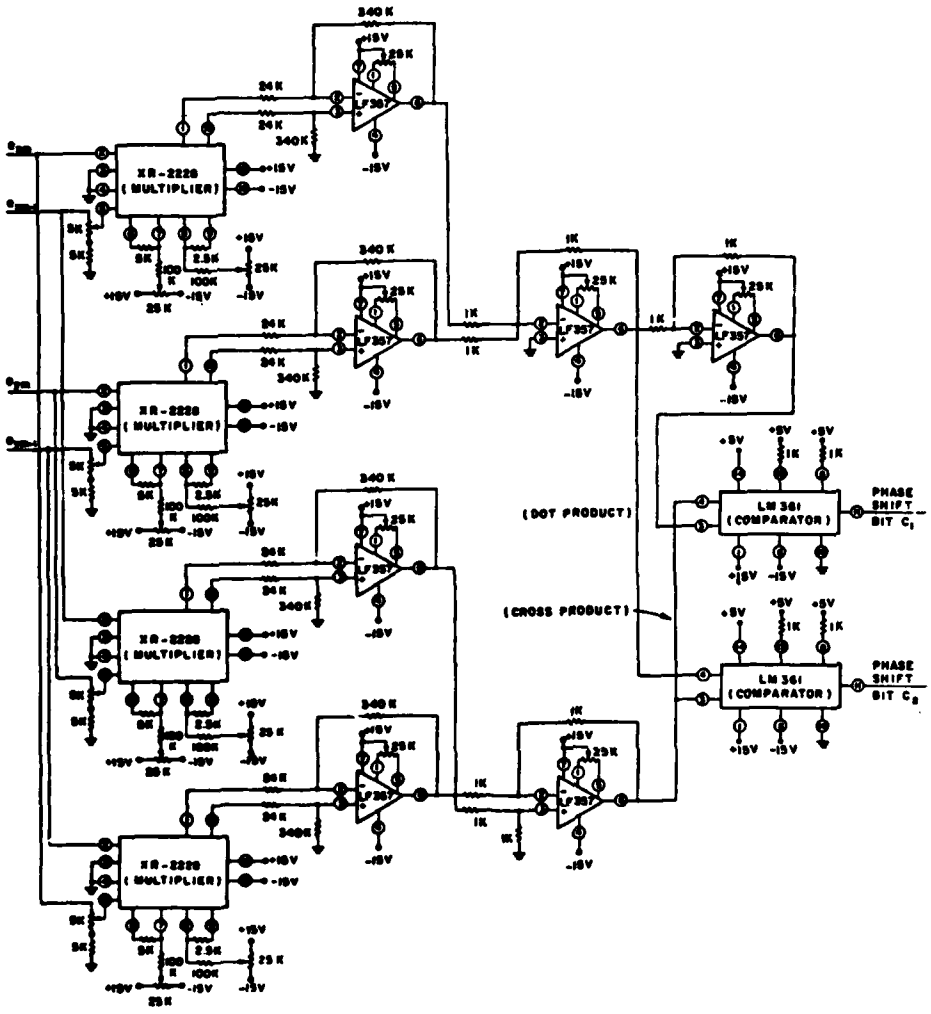


Figure 69. Circuit schematic of the processing and decision circuitry.

chip or about 5.51 microseconds. Thus, about 3.5 percent of the signal is not integrated because of the integrator dump time. This loss was not considered in the analysis of the long code acquisition time. However, the effect of this loss is small compared to the effect of the timing jitter which has a standard deviation of 4 percent of a chip.

The sample-and-hold control signals are labelled I_3, I_4, and I_5. When these signals are high, the sample-and-holds track the output of the integrators. When the signals are switched low, the sample-and-holds hold the integrator output value at the switching time. Both the m and the m-1 chip signal vector components must be available at all times

for the processing and decision circuitry as shown in Figure 66. Therefore, three sample-and-holds are required for each integrator. At any time one sample-and-hold is tracking the integrator output. Another sample-and-hold is holding the integrator output value at the end of the previous (mth) chip. This value is the signal vector component for the mth chip. A third sample-and-hold is holding the integrator output value at the end of the m-1 chip. Therefore, each sample-and-hold tracks the integrator output for one chip and holds the integrator output at the end of the chip for two chips. The sample-and-hold control signal is high for one chip and low for two chips. The chip during which the control signal is high will be different for each sample-and-hold. These signals are generated in the three state shift register shown at the top of Figure 67. With a reset signal the shift register is loaded with 011. These bits are cycled through the shift register clocked by the code timing. The output of each stage of the shift register is inverted and converted to plus-and-minus 7.5 volt signals to generate the proper control signals for the sample-and-hold.

The signals labelled S_2, S_1, and S_3 gate the outputs of the sample-and-holds as shown in Figure 68. By the gating and combining of the sample-and-hold outputs, the m and m-1 chip signal vector components are output by the differential detector. The control signals S_1, S_2, and S_3 are similar to the I_3, I_4, and I_5 control signals except that they are TTL level signals as required by the LF13332 switches. Thus, the output of the three stage shift register is used without any conversions.

A circuit schematic for the integrate and sample-and-hold devices is shown in Figure 68. There is one of these circuits for each of the two channels in the differential detector. As seen in Figure 68, the baseband component is amplified by a gain of 9.1. The signal is integrated over each chip and the value of the integrator output at the end of the chip is held by one of three sample-and-holds. Finally, the outputs of the sample-and-holds are gated and combined to generate one signal containing the mth chip signal vector components and another signal containing the m-1 chip signal vector components. It should be noted that the latter signal is a one chip delayed version of the former signal.

A circuit schematic of the processing circuitry is shown in Figure 69. In the processing circuitry the signal vector components are multiplied and combined to generate the dot product and the magnitude of the cross product for the adjacent signal vectors. Two comparators are used to decide which of four possible phase shifts has occurred. The receiver rule used by comparators is given by Equations (332), (333), (335) and (336). Two symbol streams corresponding to the phase shift at each chip are generated.

A circuit schematic of the detection logic is shown in Figure 70. The circuitry for the detection logic was developed in Section VIII-D. In the detection logic the phase shift bits, the short code symbols,

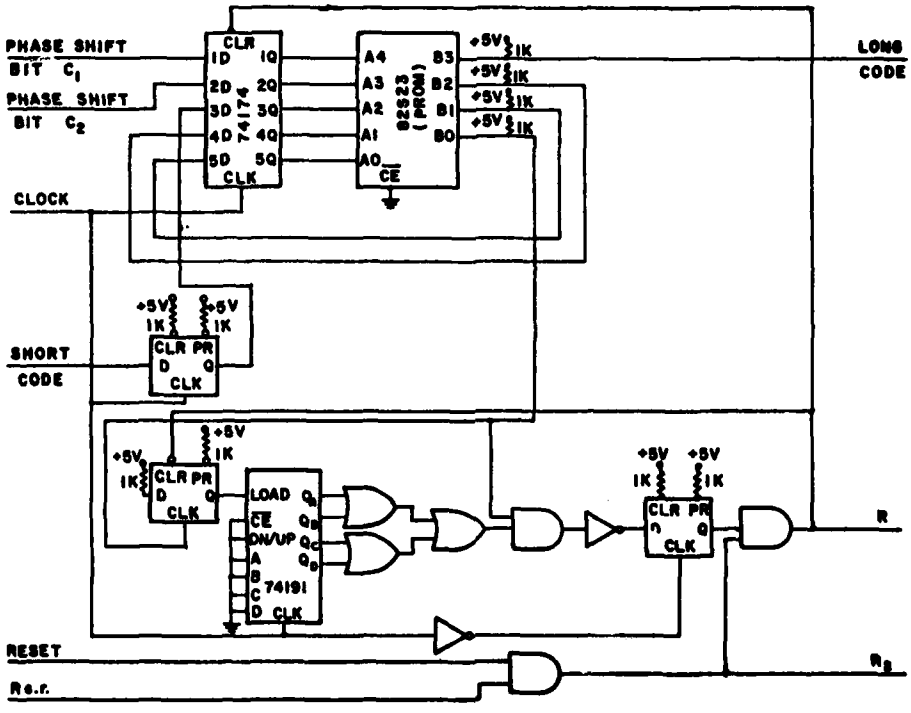


Figure 70. Circuit schematic of the detection logic.

and the previous phase state symbols (B2 and B1) are used to determine the long code symbols, the next previous state symbols, and the data. The short code symbols are delayed one clock period because the phase shift symbols are delayed the same amount because of the processing time in the differential detector. As discussed in Section VIII-D, circuitry is employed to detect errors in the detection process by sending a pulse whenever data bits are other than a multiple of 16 code symbols apart. This pulse is transmitted on the signal labelled R, which resets the detection logic. It should be noted that a system reset pulse or a reset pulse from the load and track logic ($R_{s.r.}$) also resets the detection logic. Reset signal R_2 transmits either of the last two types or resets.

In Figure 71 a circuit schematic is shown for the shift register and part of the load and track logic. With this logic the shift register is loaded with the long code bits, the shift register is switched into the feedback mode, and the long code symbols are generated for use by the correlation processor. A thirty-four stage shift register is used with the same feedback connections as the long code shift register in the transmitter. The input to the shift register is controlled by logic. The logic determines whether the long code symbols from the detection logic are fed into the shift register or whether the symbols from the shift register feedback logic are fed into the

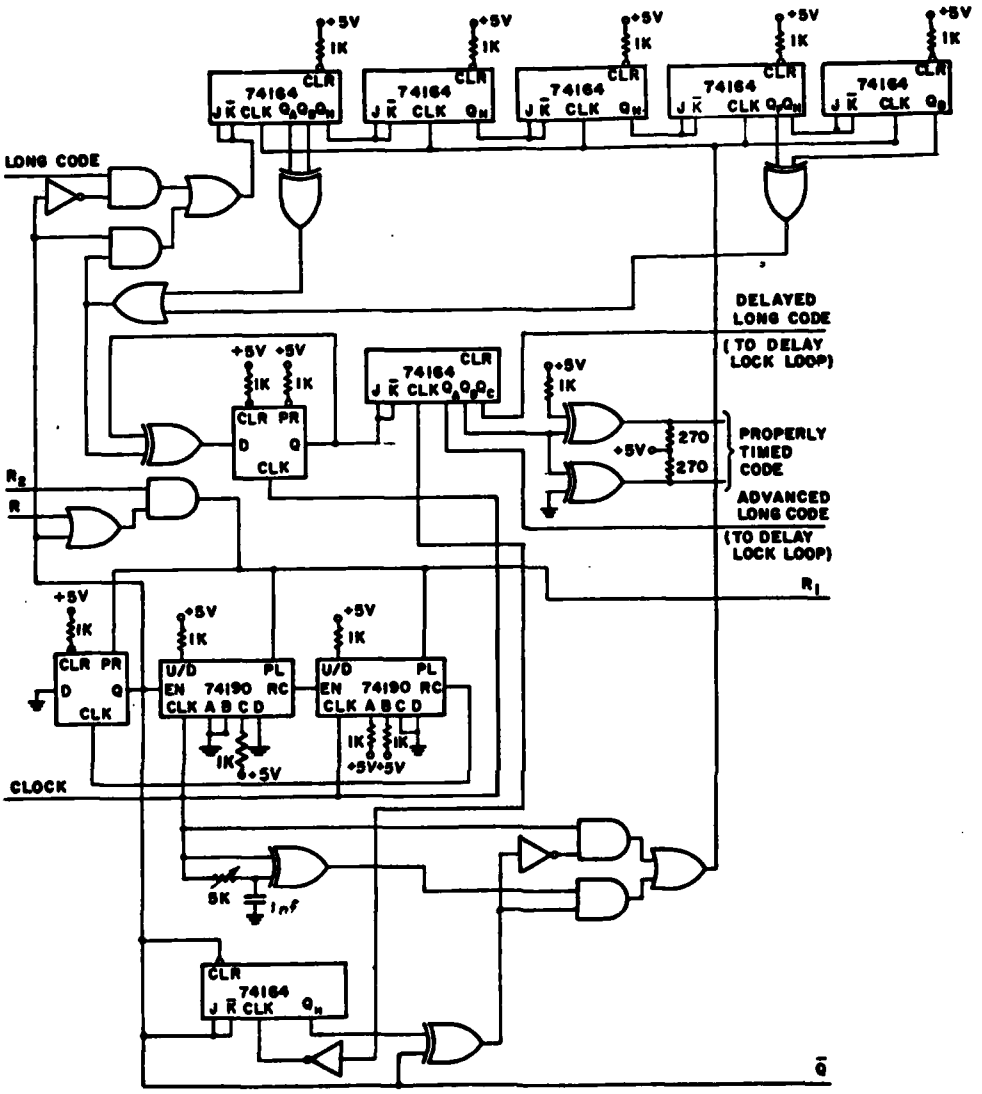


Figure 71. Circuit schematic of the long code shift register and part of the load and track logic.

shift register. The signal controlling which symbols are loaded into the register is labelled $\overline{Q}$ and is the output of a D flip-flop as shown in Figure 71. This signal is initially set low by the reset signal R_2. When $\overline{Q}$ is low the long code bits from the detection logic are loaded into the shift register and the counters (74190's) are enabled. These counters are initially loaded with thirty-four and count down to zero causing $\overline{Q}$ to go high. When $\overline{Q}$ goes high the shift register is switched into the feedback mode. Thus, the switching occurs when all thirty-four

stages of the shift register have been loaded with the detected long code symbols. If $\overline{Q}$ is low, i.e., the shift register is being loaded, then if R goes low, signalling a detection error, the counter is reset. Thus, the shift register is reloaded when a detection error occurs, which is as desired. After $\overline{Q}$ goes high, i.e., the shift register is loaded, as seen in the schematic, R will no longer reload the shift register.

The output symbols of the long code shift register are differentially encoded using an exclusive-or gate and a D flip-flop. The half chip delayed, half chip advanced, and properly timed codes are generated using a shift register (74164, in the middle of Figure 71) clocked at twice the clock rates of the code. This clock is generated using the exclusive-or gate with an RC lowpass filter on one input. The clock signal from the delay lock loop is delayed with this lowpass filter so that the output of the exclusive-or gate consists of pulses occurring on both the positive and negative going edges of the clock. Thus, this clock is at twice the frequency of the clock from the delay lock loop.

The complement of the properly timed code is generated along with the properly timed code using exclusive-or gates with pullup resistors. These resistors enable the signals to drive the mixers in the correlation processor.

The long code symbol detection process takes two clock periods to be completed. Thus, the long code that is generated after the shift register is loaded with the correctly detected long code symbols is delayed by two chips from the received signal's code. The long code shift register must be advanced two additional steps before the long code is properly timed. The shift register and logic gates shown at the bottom of Figure 71 accomplish this. The doubled clock (instead of the clock from the delay lock loop) is used to clock the long code shift register for two code clock periods immediately after the shift register is loaded. Thus, two additional clock pulses are added to the clock signal, and the output long code is synchronized with the received long code when the long code symbols are correctly detected.

In Figure 72 a circuit schematic of the correlation processor is shown. The synchronization of the locally generated long code with the received code is checked with this circuitry. As seen in this figure the properly timed code from the long code shift register modulates an amplified 59.3 MHz signal. The 59.3 MHz signal is obtained from the same local oscillator used to generate the 59.3 MHz signal in the delay lock loop. The modulated signal is amplified and mixed with the array output. If the locally generated long code is synchronized with the received code, the long code component of the desired signal is despread. A 10.7 MHz sinusoidal component is then present in the mixer output along with other signal components. A narrow band 10.7 MHz filter is used to obtain the sinusoidal component while

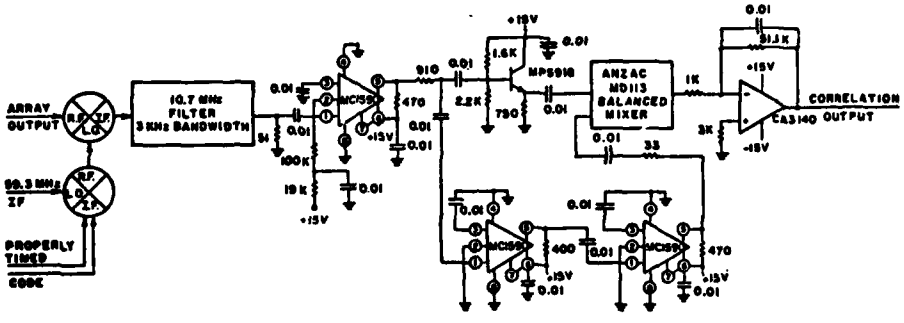


Figure 72. Circuit schematic of the correlation processor.

attenuating all other components. The bandwidth of this filter is dependent on the frequency uncertainty of the received desired signal and on the response time of the correlation processor.

The experimental system was designed to allow for a frequency uncertainty of up to 1 kHz. The correlation time for the checking of a loading of the long code shift register is 680 chips as specified in Section B or 3.91 milliseconds. Thus, the dominating factor in determining the filter bandwidth is the frequency uncertainty. A filter with a bandwidth of three kHz was chosen from the filters available that met the frequency uncertainty requirement.

The output of the filter is then envelope detected using the same circuitry as that used in the delay lock loop. The filter output is hardlimited, mixed with the nonhardlimited signal and lowpass filtered to generate a correlation output proportional to the despread component of the desired signal. The lowpass filter is an active RC filter with a time constant on the order of the correlation time.

In Figure 73 a circuit schematic of the remaining part of the load and track logic and the control logic is shown. Both these subsystems are shown in the same figure because they use the same signals. The control logic determines which code is to be used as a reference in the receiver and resets the system if it is determined that a smart jammer's signal is being tracked by the system. The portion of the load and track logic shown determines if the locally generated long code is correctly synchronized and reloads the long code shift register if it is not synchronized.

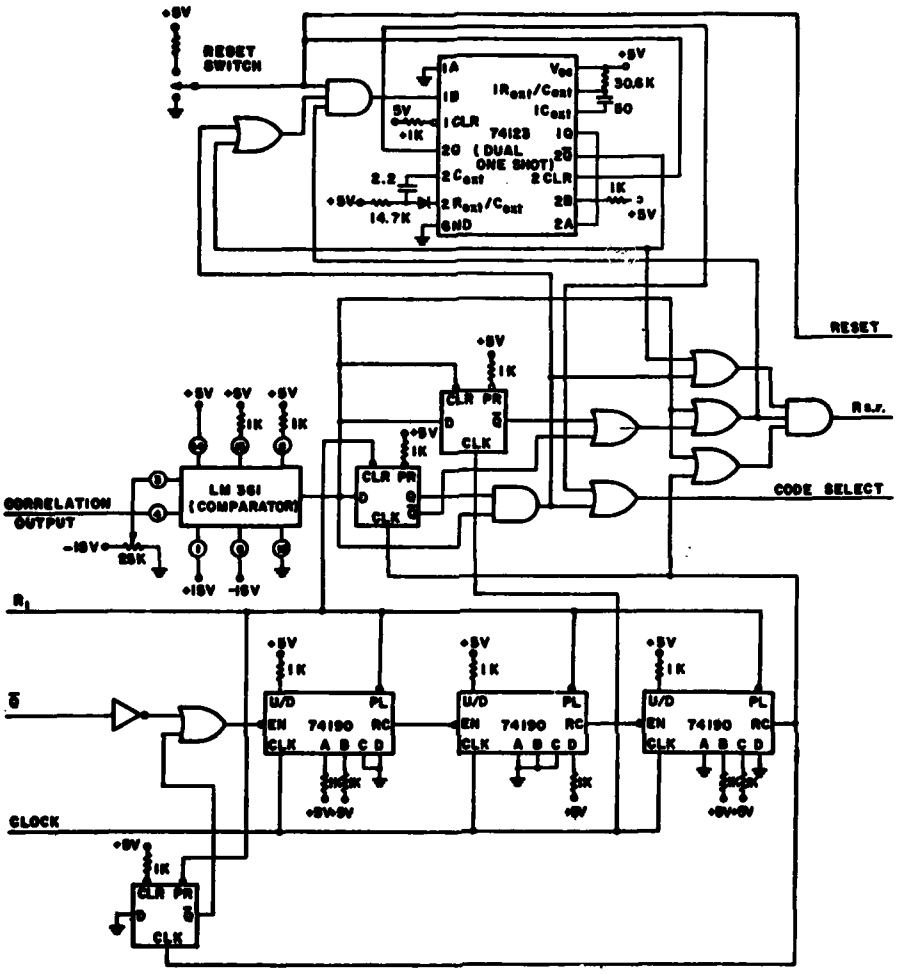


Figure 73. Circuit schematic of part of the load and track logic and the control logic.

As shown in Figure 73 the correlation output is compared to the acquisition threshold voltage. This voltage was set to 0.66 times the maximum possible correlation output voltage when noise is not present. The maximum voltage is that voltage which is present when the locally generated long code is synchronized with the received code. The output of the comparator is sampled at the end of the correlation period. A counter is used to determine the end of the correlation period. This counter is enabled by the $\overline{Q}$ signal which goes high when the long code shift register is loaded. It is initially loaded with 683 and counts down to zero when the comparator output is sampled. The counter is set to 683 because three clock periods are allowed for the long code shift register to be advanced two clock periods in addition to the 680

clock periods for the correlation time specified in Section B. A reset signal, R_1, is used to initially load the counter.

If the correlation output is greater than the acquisition threshold at the end of the correlation time, the comparator output is high. Thus, the code select output is set high which causes the delay lock loop to track the long code rather than the short code. Also, the long code is then used by the reference loop to generate the reference signal. If the comparator output is low at the end of the correlation time, the shift register reset signal $R_{s.r.}$ goes low for one clock pulse. As discussed previously, a low $R_{s.r.}$ signal causes the long code shift register to be reloaded and, therefore, the correlation processing is repeated. With a low comparator output, the code select line is always low. Therefore, if long code synchronization is lost, the delay lock loop switches to the tracking of the short code timing. In general, if the long code timing is lost, so is the short code timing and the acquisition procedure is restarted.

The dual one shot shown in Figure 73 is used to provide smart jammer protection. The circuitry is designed so that if the comparator output is not high after 0.55 seconds, then the code select line is set high. With the code select line high, the delay lock loop attempts to track the long code timing. Since this timing is wrong, slewing of the code timing will occur. The code select line is held high long enough to advance the short code timing offset by several chips. Then the code select line is set low. The process is repeated every 0.55 seconds, if necessary. The above procedure provides smart jammer protection for the following reason (as explained in Chapter X). If the adaptive array has acquired a smart jammer's signal as the desired signal, then the short code timing will be tracked by the delay lock loop. However, long code timing will not be acquired within 0.55 seconds, the maximum allowable acquisition time. The delay lock loop is then slewed until another signal (hopefully, the desired signal) with the short code is acquired by the array. With this method, the smart jammer's signal will be acquired again by the array only if the desired signal is not present.

Figures 74 through 76 show part of the hardware used in the experimental system. Figure 74 shows the transmitter whose schematic is shown in Figure 56. The logic and the quadriphase modulator are labelled in the figure. Figure 75 shows the delay lock loop whose block diagram is shown in Figure 60. The individual components of the delay lock loop are labelled and correspond roughly to the schematics of Figures 61 through 64. Figure 76 shows the long code acquistion circuitry whose block diagram is shown in Figure 65 and the control logic. The components of the long code acquisition circuitry in the block diagram are labelled in the figure. The control logic circuitry is also labelled. The schematics for the circuitry in this figure are shown in Figures 66 through 73.

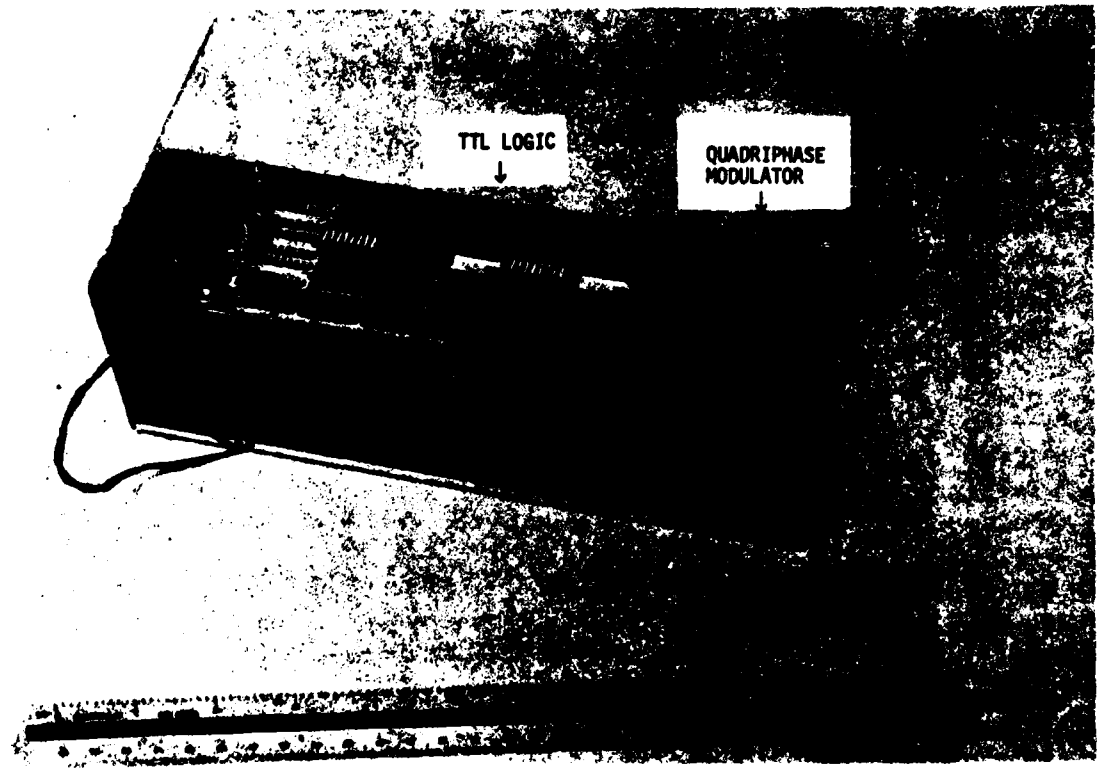


Figure 74. The transmitter hardware for the schematic of Figure 56.

D. Experimental Results

This section describes the experimental results obtained with the four-phase communication system described in Section C. The results are used to verify the analysis of Chapters VI, VII and VIII. The results are also used to demonstrate the rapid acquisition and conventional and smart jamming protection of the four-phase system. All experimental results are compared to the results obtained with the biphase system.

The major analytical results of Chapters VI, VII and VIII are verified by testing one parameter in each chapter versus the signal-to-noise ratio at the receiver. From Chapter VI, the probability of false alarm during short code acquisition is examined. From Chapter VII, the tracking jitter of the delay lock loop is studied. Finally, from Chapter VIII, the long code acquisition time is examined.

The four-phase system capabilities are tested with three experiments. To demonstrate rapid acquisition, the total acquisition time versus signal-to-noise ratio is determined. To demonstrate conventional jamming protection, the effect of a CW jammer is studied. Finally, to demonstrate smart jammer protection, the effect is studied of a repeat jammer with remodulation and a biphase jammer with the short code.

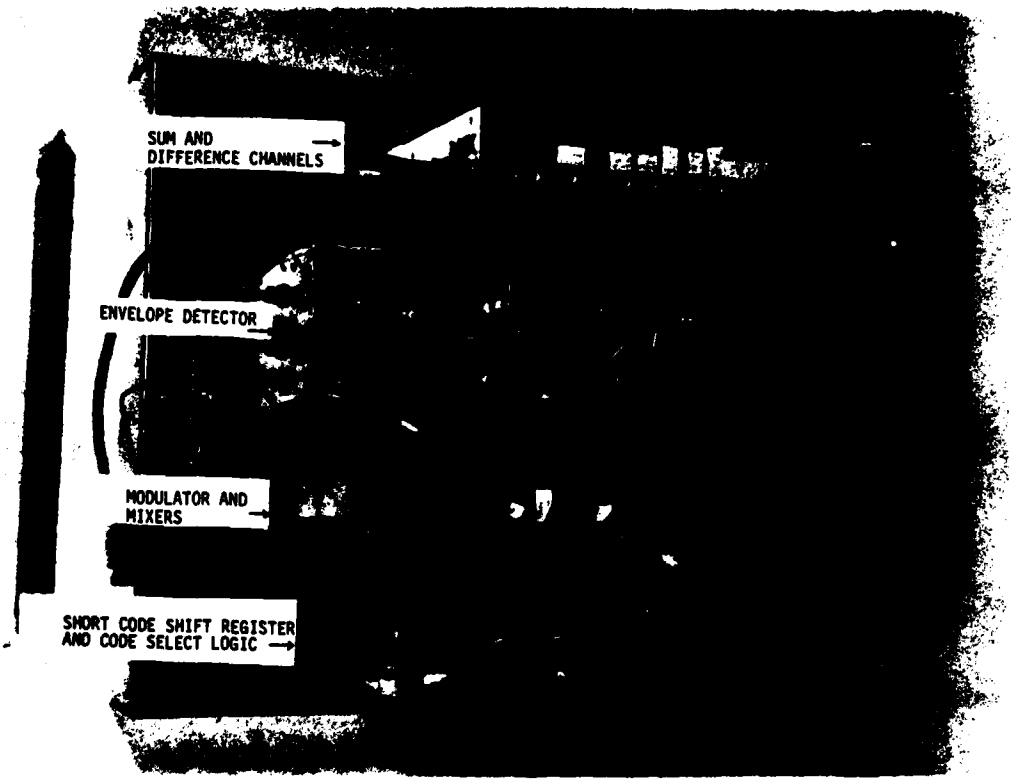


Figure 75. The delay lock loop hardware for the block diagram of Figure 60.

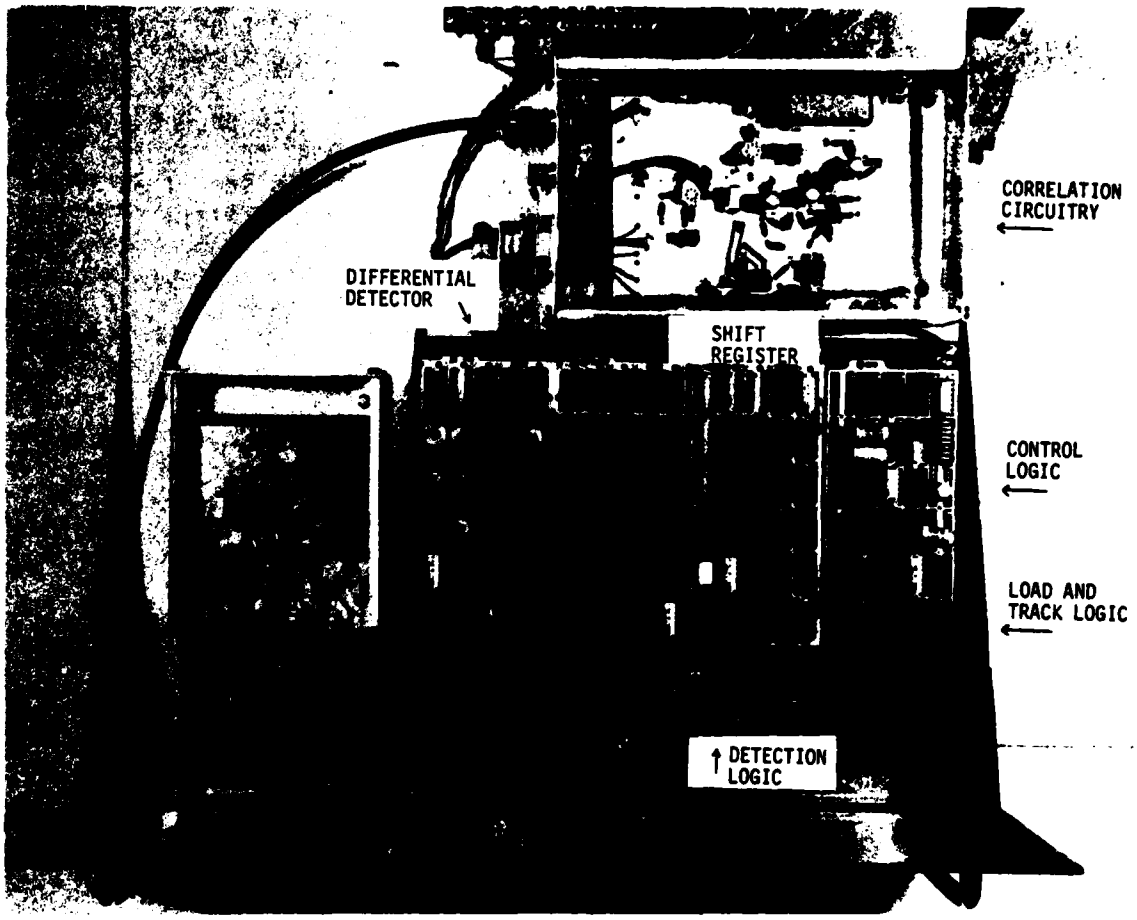


Figure 76. The long code acquisition hardware for the block diagram of Figure 65 and the control logic hardware.

The probability of false alarm is the probability that the sum channel output exceeds the acquisition threshold during acquisition. This probability is measured when the code timing offset in the delay lock loop is outside the capture range of the loop. The probabilty of false alarm is analyzed in detail in Chapter VI. From the results of this chapter as illustrated in Figures 28 and 29, it is seen that the probability of false alarm depends on N'/k, P_{miss}, and $S/N|_{IF}$. For the experimental system from Table 10,

$$N'/k = \frac{255}{16} \approx 15.9 \tag{409}$$

and

$$P_{miss} = 0.02 \quad . \tag{410}$$

From Chapter VII, the $S/N|_{IF}$ can be determined as a function of the received signal-to-noise ratio, $S/N|_{RF}$. For a four-phase signal, from Equation (291),

$$S/N|_{IF} = \frac{16}{\frac{1}{S/N|_{RF}} + 2} \quad . \tag{411}$$

For the biphase signal, from Equation (301),

$$S/N|_{IF} = \frac{16}{\frac{1}{S/N|_{RF}} + 1} \quad . \tag{412}$$

The probability of false alarm and the corresponding acquistion threshold can be calculated from Equation (214). Figure 80 shows the theoretical probability of false alarm versus $S/N|_{RF}$ as obtained with the above equations. The setup for the experimental tests is described below.

Figure 77 shows the experimental setup used to measure the probability of false alarm. The signal, either four-phase or biphase, is generated by the transmitter shown in Figure 56. The signal is then mixed with noise. The noise level can be varied to change the signal-to-noise ratio into the delay lock loop. A block diagram of the delay lock loop is shown in Figure 60.

The delay lock loop was modified for the experiment as shown in Figure 78. The input to the VCXO was disconnected and a constant

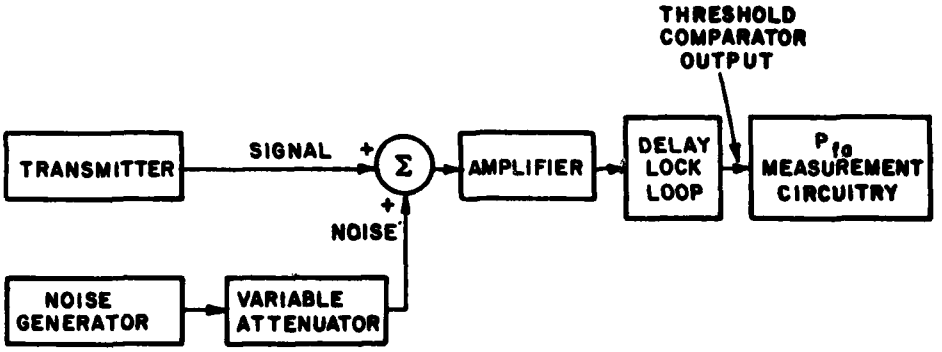


Figure 77. Experimental setup for probability of false alarm measurement.

voltage applied to the VCXO. Thus, the sweep speeds can be kept constant (at 687 Hz from Table 10) during acquisition and the signal is not acquired. The probability of false alarm can now be measured by monitoring the output of the threshold comparator. The comparator compares the sum voltage to the acquisition level.

Figure 79 shows the circuitry used to convert the threshold comparator output to the probability of false alarm value. This circuitry counts the number of times the threshold comparator output goes high during a given interval. The interval is one hundred times the sum channel filter time constant (approximately .27 seconds). Thus, the count at the end of this interval corresponds to one hundred times the false alarm rate in that interval. As shown in Figure 79, the threshold comparator output is converted to a TTL level signal with a LM361. The output of the LM361 clocks a counter. The counter is enabled during a pulse out of the 74121. This pulse is approximately .27 seconds long.

The output of the counter at the end of pulse is recorded as the false alarm percentage during the interval. By taking a large number of false alarm percentage readings, an average false alarm percentage can be determined. A confidence interval for the actual false alarm probability can also be determined (see [37]).

The results of the experimental data collected by the above method are shown in Figure 80. The probability of false alarm is plotted versus the signal-to-noise ratio for P_{miss} equal to 0.02. Both theoretical and experimental results are shown for the four-phase and biphase signals.

The experimental results vary somewhat from the theoretical results. This can be attributed to the difficulty in obtaining precise

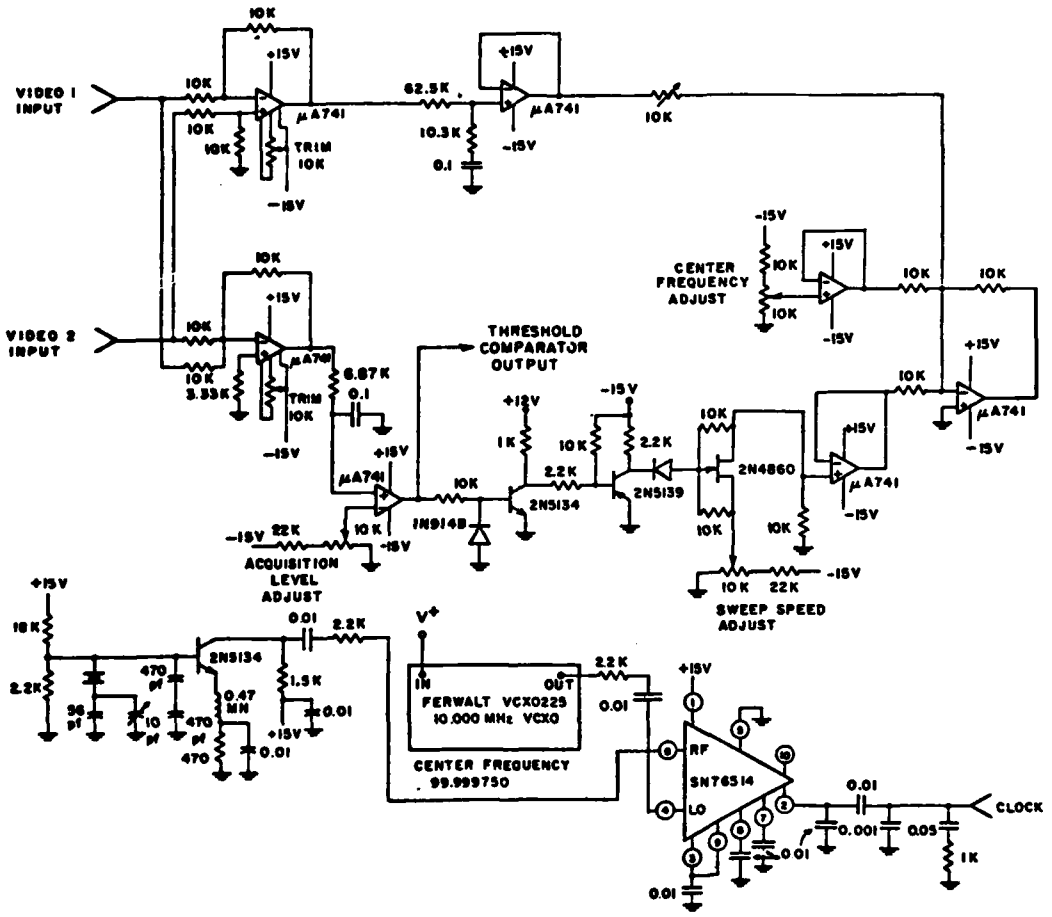
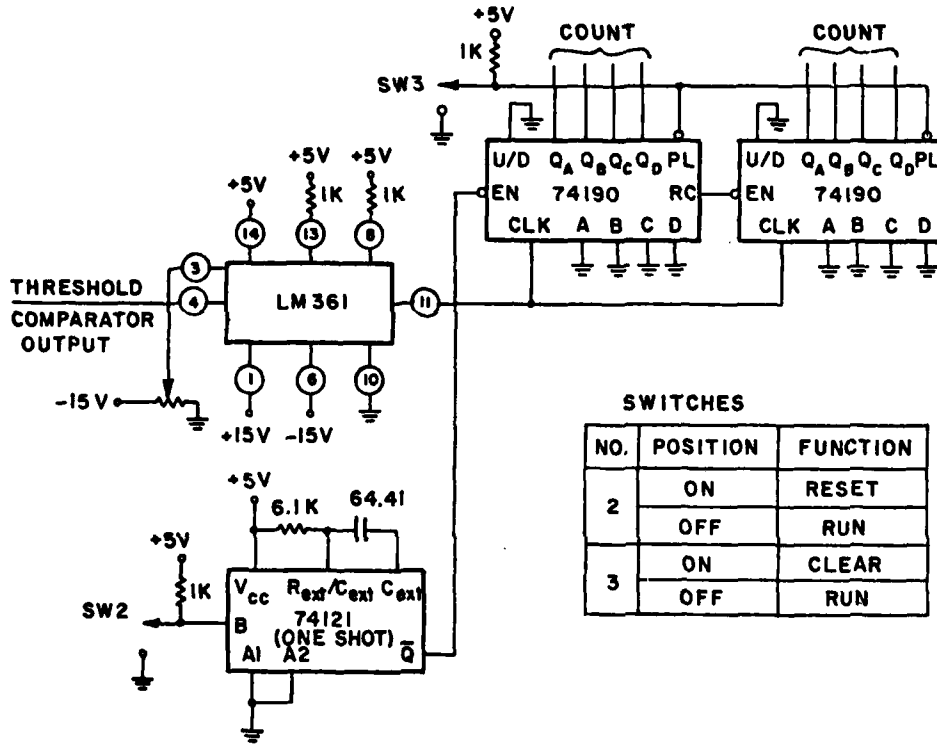


Figure 78. Portion of the delay lock loop modified for experimental testing of the probability of false alarm (original version shown in Figure 63).



NO.	POSITION	FUNCTION
2	ON	RESET
	OFF	RUN
3	ON	CLEAR
	OFF	RUN

Figure 79. Schematic of the circuitry that measures probability of false alarm.

experimental results with both low and high signal-to-noise ratios. For low signal-to-noise ratios the sum channel voltage can be shown to have a large mean as compared to its standard deviation. Therefore, relatively small changes in the acquisition threshold or signal level can produce large changes in the probability of false alarm. Small errors in the experimental system, therefore, can produce a large error in the experimental results.

For higher signal-to-noise ratios, the noise in the delay lock loop is primarily self noise. As discussed in Chapter VII, the level of the self noise constantly varies during acquisition and a worse case value was chosen for theoretical calculations. Therefore, the average self noise level and the actual probability of false alarm will be somewhat less than that predicted theoretically for high received signal-to-noise ratios. This is shown in Figure 80. The experimental results are, therefore, in agreement with theoretical results when the above inaccuracies are considered.

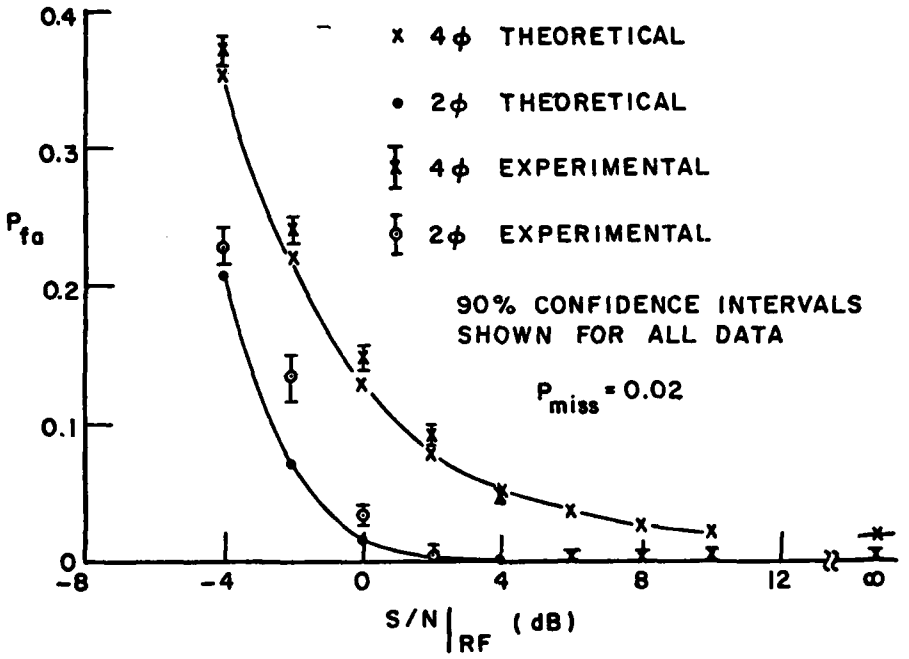


Figure 80. Probability of false alarm versus received signal-to-noise ratio; comparison of theoretical and experimental results for both biphase and four-phase signals.

Timing jitter is the standard deviation of the code tracking error in the delay lock loop. Timing jitter is analyzed in detail in Chapter VII. From the results of this chapter as illustrated in Figure 31, it is seen that timing jitter depends on ρ_0/B_{IF} and $S/N|_{IF}$. For the experimental system from Table 10,

$$\rho_0/B_{IF} = 0.0916 \quad . \tag{413}$$

Also from Chapter VII, the $S/N|_{IF}$ after acquisition can be determined as a function of the received signal-to-noise ratio, $S/N|_{RF}$. For a four-phase signal, from Equation (300) with k equal to 16,

$$S/N|_{IF} = \frac{16}{\frac{1}{S/N|_{RF}} + \frac{1}{2}} \quad . \tag{414}$$

For the biphase signal, from Equation (302) with k equal to 16,

$$S/N|_{IF} = 16(S/N|_{RF}) \quad . \qquad (415)$$

The timing jitter can be calculated from Equation (323). Figure 83 shows the timing jitter versus $S/N|_{RF}$ obtained with the above equations. The setup for the experimental tests is described below.

Figure 81 shows the experimental setup used to measure the timing jitter. The setup is similar to that used in the measurement of the probability of false alarm.

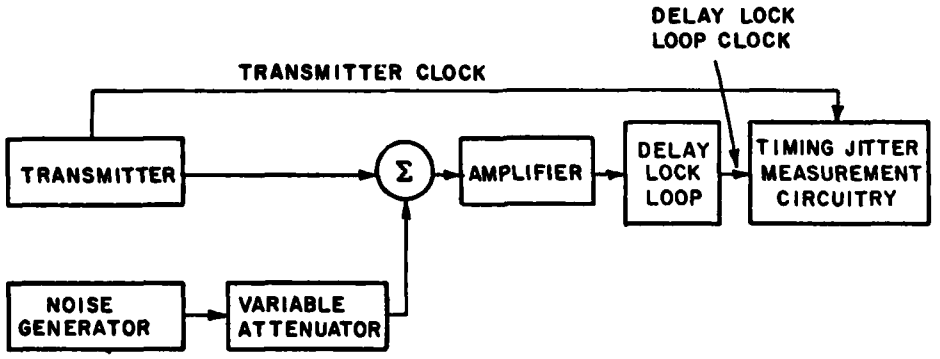


Figure 81. Experimental setup for timing jitter measurement.

Figure 82 shows the circuitry used to measure the timing jitter. A phase comparator produces a voltage (positive or negative) proportional to the timing error between the transmitter and delay lock loop clocks. The voltage is amplified and displayed on a digital storage oscilloscope. With the oscilloscope, the voltage and, therefore, the timing error at a given instant can be determined. With repeated measurements, an ensemble average and standard deviation can be determined. Also, a confidence interval for the actual timing jitter can be calculated (see [37]).

The experimental results obtained by the above method are shown in Figure 83. The timing jitter is plotted versus received signal-to-noise ratio. Both theoretical and experimental results are shown for the four-phase and biphase signals.

The experimental results vary somewhat from the theoretical results. The variation may have been caused by changes in the loop gain during the experiments. The timing jitter varies greatly with small changes in loop gain. Therefore, any drifts in amplifier gain in the delay lock loop could have caused a difference in experimental and theoretical results. On the whole, though, experimental results show good agreement with theoretical results.

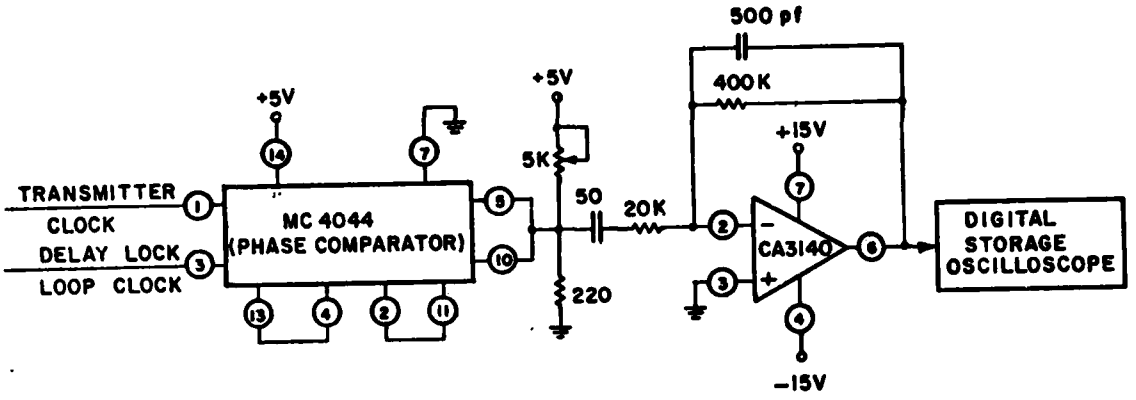


Figure 82. Schematic of the timing jitter measurement circuitry.

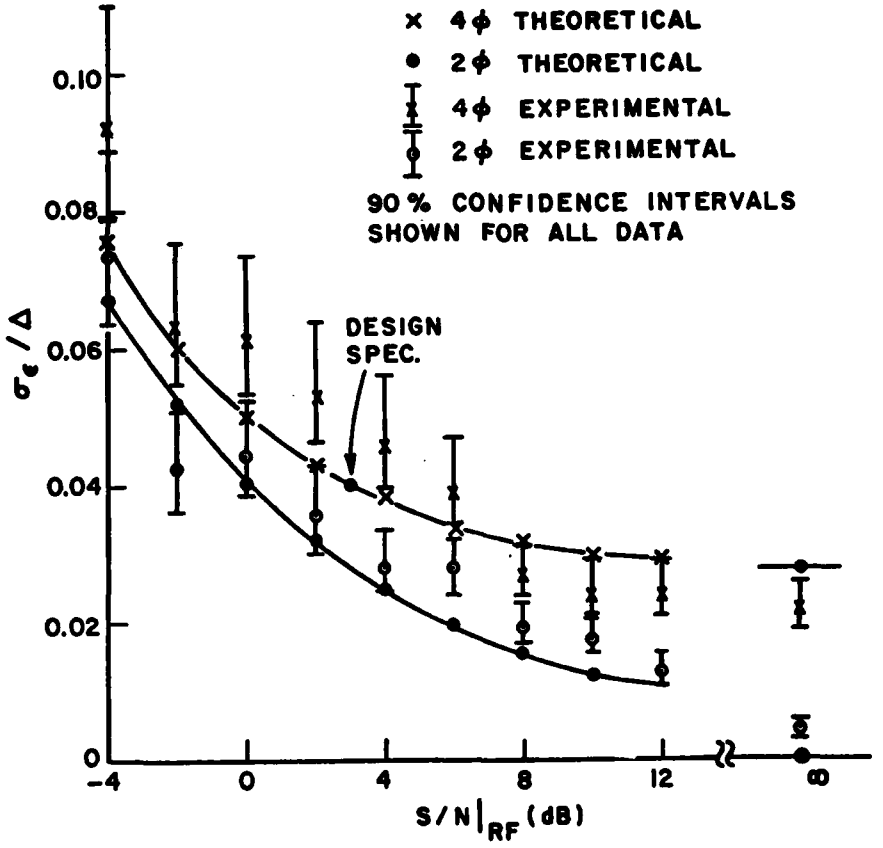


Figure 83. Delay lock loop normalized timing jitter, $\sigma_\varepsilon/\Delta$; versus received signal-to-noise ratio, $S/N|_{RF}$; comparison of theoretical and experimental results.

The average long code acquisition time is the average time required for the long code to be acquired after the short code timing has been acquired. The long code acquisition is analyzed in detail in Chapter VIII. Both computer simulation and approximations were used to analyze the long code acquisition times because an exact analysis was too complex. From the results of Chapter VIII, it is seen that the long code acquisition time depends on the long code shift register length, the correlation time, the spreading ratio, and the energy per chip to noise density ratio. For the experimental system, from Table 10, the long code shift register length is 34, the correlation time is 680 chips, and the spreading ratio is 16.

Figure 84 shows the computer simulation, approximate theoretical and experimental results. The average long code acquisition time is plotted versus E_Δ/N_0.

The computer simulation results were obtained using the computer program described in Section VIII-E. The simulation does not consider timing error with the delay lock loop tracking the short code. As shown in Table 10, the tracking jitter may be as much as 0.04Δ. The jitter will increase the average long code acquisition time and, therefore, the simulation results underestimate the average acquisition time.

For the approximate model, the average long code acquisition time for the experimental system is given by (from Equation (362))

$$T_{acq} = \frac{680\ \Delta}{(1-P_E)^{34}} \quad , \tag{416}$$

where P_E is the probability of error in detecting a long code symbol. Tracking jitter can be taken into account by calculating the probability of error with the tracking jitter value given in Figure 83. The probability of error with tracking jitter is given by Equation (357). The approximate theoretical long code acquisition time calculated from the above equations is plotted in Figure 84.

Because of the approximations made in the approximate model, the theoretical results overestimate the actual acquisition time rather than underestimate it as with the simulation. Therefore, the simulation and approximate theoretical results can be considered as lower and upper bounds, respectively, of the actual long code acquisition time.

Figure 85 shows the experimental setup used to measure the long code acquisition time. The signal is combined with noise and amplified. The amplified signal is used by the long code acquisition circuitry and the delay lock loop. The delay lock loop tracks the short code timing and short code symbols used by the long code acquisition circuitry.

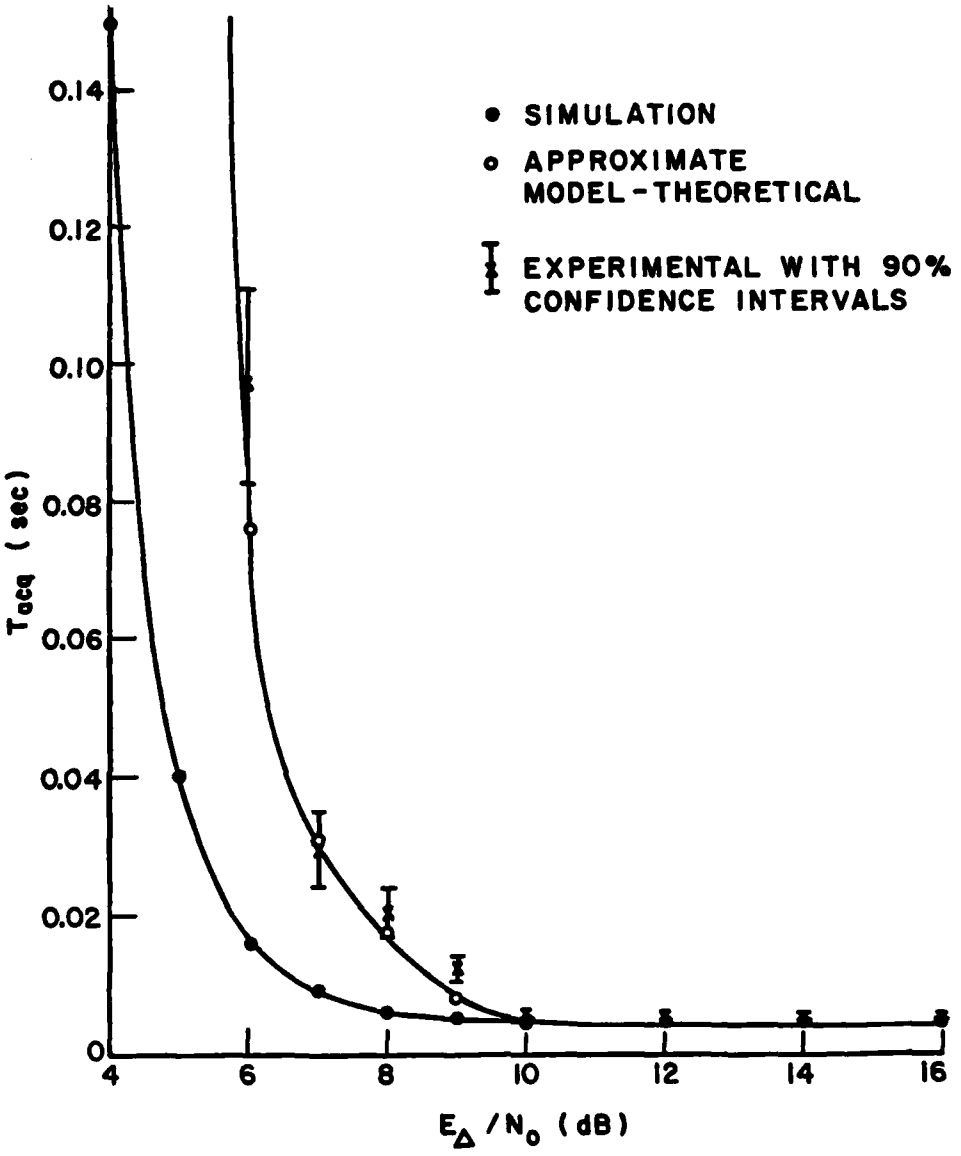


Figure 84. Long code acquisition time, T_{acq}, versus energy per chip to noise density ratio E_Δ/N_0; comparison of simulation, approximate theoretical, and experimental results.

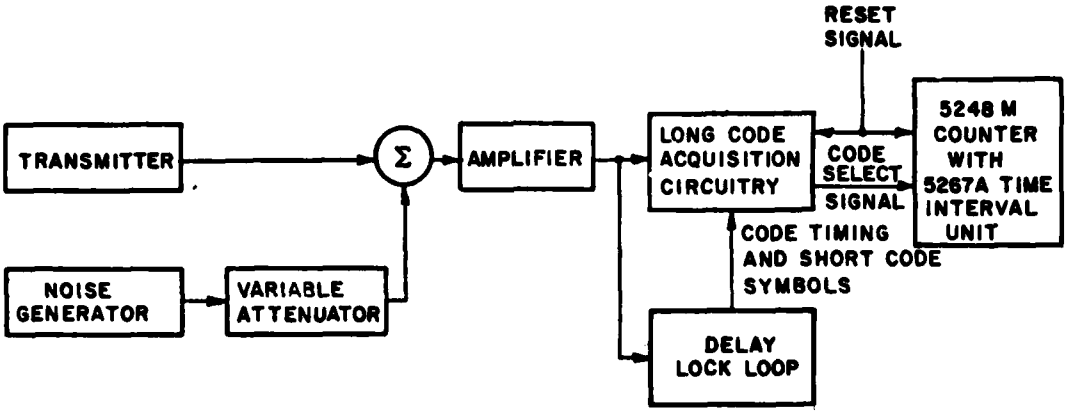


Figure 85. Experimental setup for long code acquisition time measurement.

The test procedure is as follows. While the delay lock loop continuously tracks the short code, a reset signal starts the long code acquisition process. In the long code acquisition circuitry, the code select line (see Figure 73) goes high when the long code is acquired. A time interval counter measures the interval between the reset signal and the high transition in the code select line. The time interval, i.e., the long code acquisition time, is displayed on the counter and recorded. The above process is repeated (up to 50 times) to determine an average long code acquisition time and a confidence interval for the actual average acquisition time.

As shown in Figure 84, the experimental results obtained with the above method are close to the upper bound of the predicted acquistion time. Thus, the experimental results show that the required E_Δ/N_0 for a given T_{acq} is as much as one decibel greater than predicted. Because of the amount of circuitry involved in the long code acquisition process, a one decibel degradation is not considered excessive. The degradation may be due to at least two factors. First, the integrators in the differential detectors have a finite dump time. Because of the dump time, the signal energy detected per chip is decreased. The dump time was not considered in the simulation or theoretical results. Second, there are offsets in the operational amplifiers and multipliers. These offsets were minimized but are still present in the system and will effect the acquisition performance. The experimental results are, therefore, in agreement with simulation and approximate theoretical results.

To demonstrate the rapid acquisition of the four-phase system, the average total acquisition time was examined. The predicted and experimental results are discussed below.

The predicted average total acquisition time is the expected average short code plus long code acquisition time. The predicted short code acquisition time is approximately 0.2 seconds (see Table 10). It is independent of the received energy per chip to noise density ratio. The expected average long code acquisition time is given by the experimental results of Figure 84. Because a four element adaptive array is used in the experimental system, the array output energy per chip to noise density ratio was assumed to be six decibels greater than that received, $E_\Delta/N_0|_{IN}$. The array output E_Δ/N_0 was used in determining the expected long code acquisition time from Figure 84. The predicted average total acquisition time is plotted versus $E_\Delta/N_0|_{IN}$ in Figure 86.

The total acquisition time for the experimental system of Figure 54 was measured by a method similar to that used to measure long code acquisition time. Specifically, a time interval counter measured the interval between the system reset signal and the high transition of the code select line. Fifty acquisition time measurements were taken per $E_\Delta/N_0|_{IN}$ value to determine an average total acquisition time and a confidence interval for the actual average. The experimental results are shown in Figure 86. Because of the smart jammer protection circuitry, a high transition in the code select line occurs if the long code has not been acquired in 0.55 seconds. Therefore, the probability of not acquiring the code in the required time, P_{na}, was determined and is shown in Figure 86.

The experimental results show a slightly greater average total acquisition time than that predicted for low $E_\Delta/N_0|_{IN}$ (0 to 3 dB). This increase can be attributed to the degradation in array performance with low input signal-to-noise ratios. When $E_\Delta/N_0|_{IN}$ is 0 dB, the array input S/N is almost -20 dB because the bandwidth of the noise is much greater than the signal bandwidth into the array. With such a low S/N, the array weights are controlled more by the noise than by the signal. Thus, the output S/N may be less than optimum, i.e., less than 6 dB greater than the input S/N. The long code acquisition time will be increased because of the lower output S/N (E_Δ/N_0). The total acquisition time is, therefore, also increased.

Because of the degradations discussed previously, the average total acquisition time for the experimental system with E_Δ/N_0 equal to 0 dB is about fifty percent greater than that specified in the design. Figure 86 shows the design specification in relation to the experimental results. The experimental results, however, still show rapid acquisition for the system.

To demonstrate the conventional jamming protection of the four-phase system, experimental tests were performed with a CW jammer. The results of these tests are discussed below. First, the suppression of a CW jammer by the array with a biphase desired signal is compared to the suppression with a four-phase desired signal. The maximum jammer to signal power ratio, J/S, at the array input is then shown for

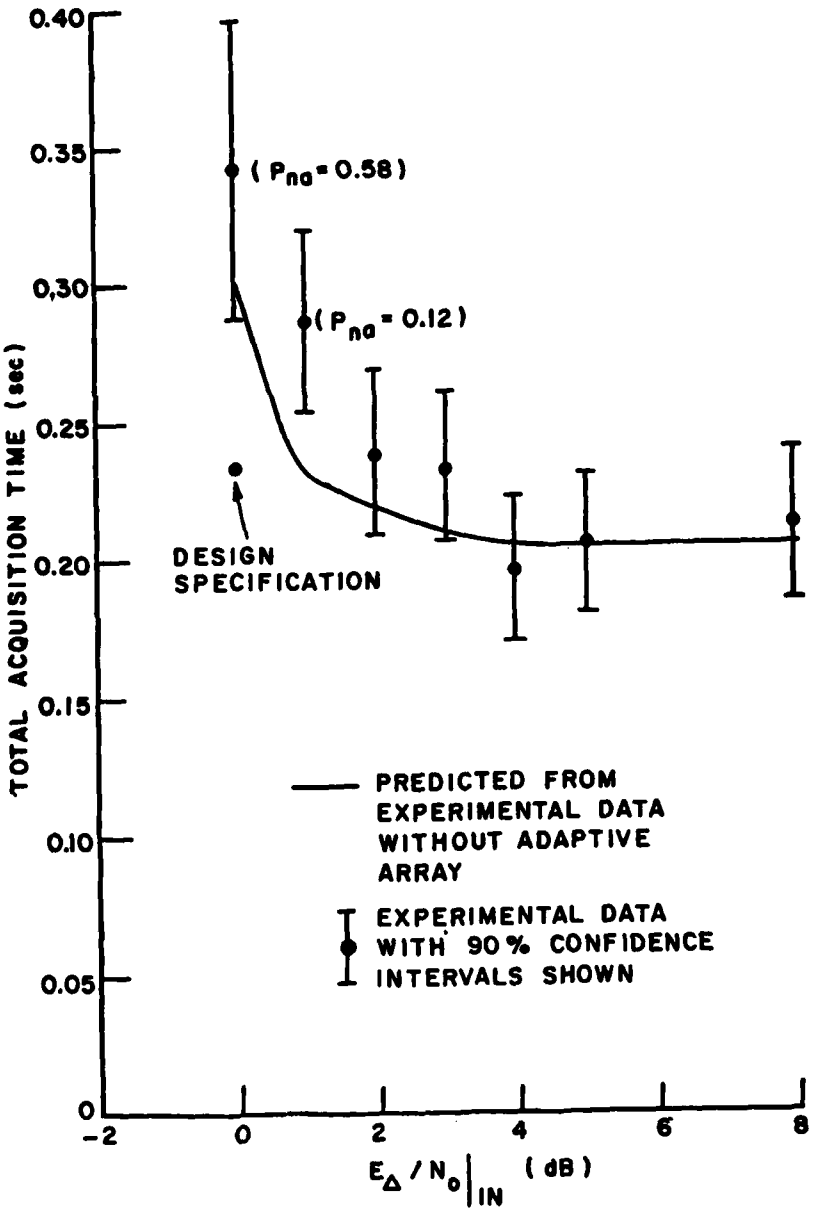


Figure 86. Total acquisition time versus received E_Δ/N_0; comparison of predicted and experimental results.

acquisition of the signal at the receiver. Next, the reason for this maximum J/S is discussed. Finally, the difference in maximum J/S is discussed for the biphase and four-phase desired signals.

The array used in the experimental system was shown to give the best performance when

$$E_{\Delta}/N_0|_{IN} \geq 8 \text{ dB} \quad . \tag{417}$$

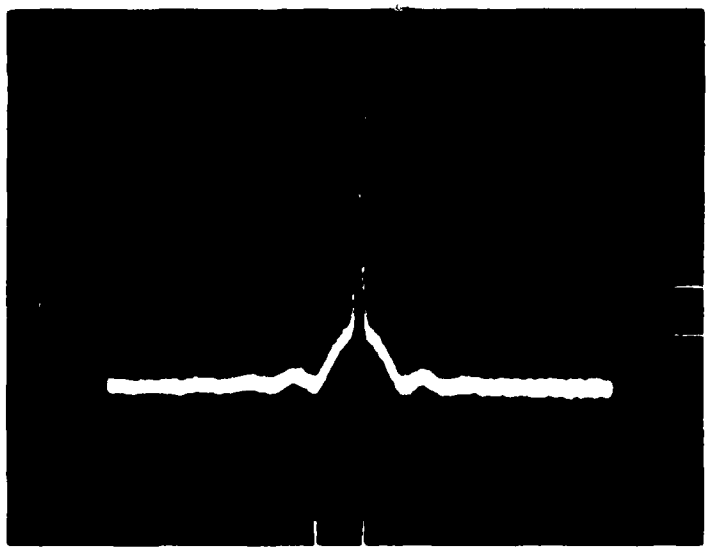
In this case, the array output signal level is independent of the received signal-to-noise ratio. Furthermore, the received CW jammer level does not effect the long code acquisition time in the four-phase system. However, when the received jammer-to-desired signal power ratio, J/S, is high enough, the short code, and, thus, the signal is not acquired.

The suppression of a CW jammer by the array is shown in Figures 87 through 90. In these figures the array input and output power density spectrum is shown with the desired signal and CW interference. The J/S is 20 dB at the array input. Figures 87 and 88 are for a biphase desired signal, and Figures 89 and 90 are for a four-phase desired signal. These figures show a desired signal-to-jammer power ratio improvement of about 30 dB for both types of desired signal. Thus, the CW suppression by the array is the same for a four-phase and a biphase desired signal.

The maximum J/S at the array input for which acquisition can occur is 23 dB for the biphase system and 20 dB for the four-phase system. This maximum value is dependent on the system parameters as described below.

The maximum J/S is dependent on the code modulation frequency and the acquisition time for the system. This is because the rate of response of the weights is proprotional to the signal strength in the LMS adaptive array. For the strongest interfering signal, the weights must respond slower than 0.2 times the code modulation frequency [38]. Otherwise, the weights will begin to modulate the interference to look like the reference signal. When this occurs during acquisition, the modulated interference is present in the array output, and the delay lock loop tracks the code timing on this signal. The desired signal is, therefore, never acquired.

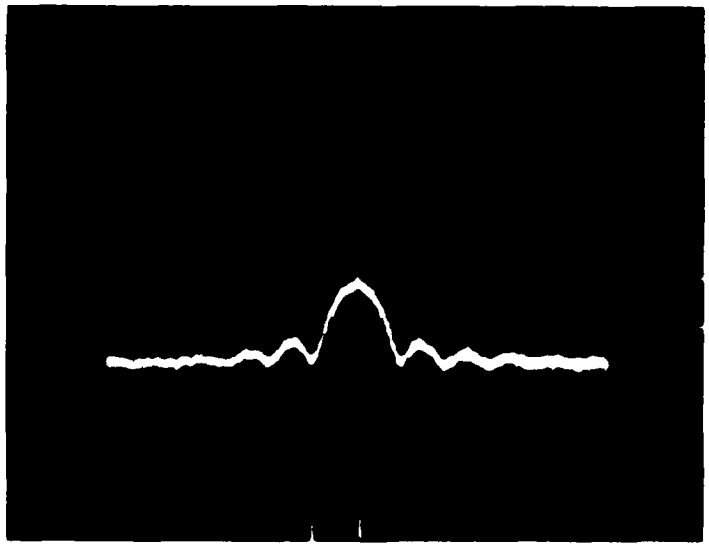
For the weakest desired signal, the weights must respond faster than the inverse of the sum channel filter bandwidth in the delay lock loop. Otherwise, the desired signal will not be pulled out of the noise and the acquisition threshold exceeded in the delay lock loop during acquisition.



10 dB/div

200 kHz/div

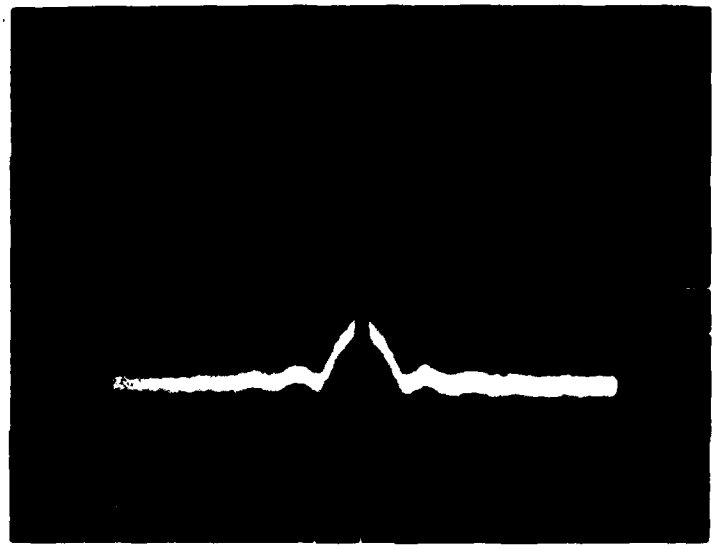
Figure 87. Received power density spectrum with biphase desired signal and CW jammer at 70 MHz; $E_\Delta/N_O|_{IN}$ equal to 8 dB, J/S equal to 20 dB.



10 dB/div

200 kHz/div

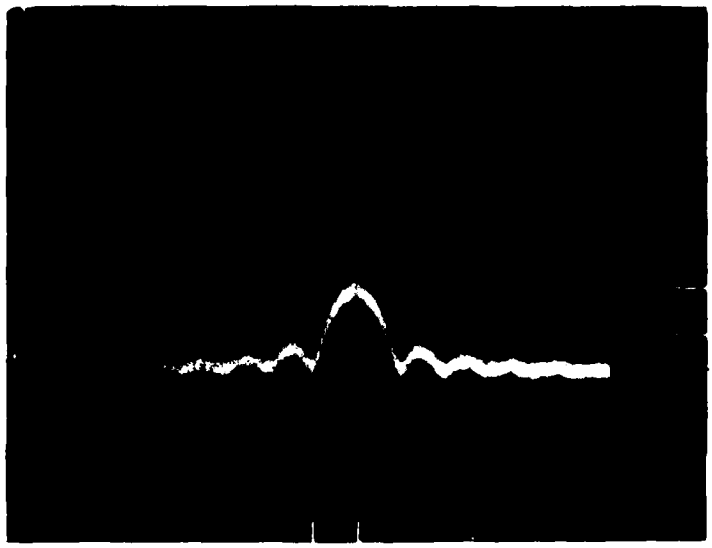
Figure 88. Array output power density spectrum with input of Figure 87.



10 dB/div

200 kHz/div

Figure 89. Received power density spectrum with four-phase desired signal and CW jammer at 70 MHz; $E_\Delta/N_o|_{IN}$ equal to 8 dB. J/S equal to 20 dB.



10 dB/div

200 kHz/div

Figure 90. Array output power density spectrum with input of Figure 89.

By adjusting the loop gain in the adaptive array, a maximum J/S can be obtained equal to the ratio of the parameters given above. For the experimental system, the code modulation frequency is 175.2 kHz and the sum channel filter bandwidth is 364 Hz. The maximum J/S is, therefore, given by

$$J/S\Big|_{max} = \frac{0.2 \times 175.2 \times 10^3}{364} \approx 96 \quad (20 \text{ dB}) \quad . \tag{418}$$

The theoretical analysis of the maximum J/S is only approximate, however. As shown by the experimental results, a maximum J/S of 23 dB was obtained with the biphase system.

A much higher maximum J/S can be obtained by changing the system parameters. In particular, increasing the code modulation frequency would increase the maximum J/S. That is, the main reason for only a 23 dB maximum J/S in the experimental system is that the code modulation frequency is low. In systems with code modulation frequencies in the MHz range, a maximum J/S of 30 dB or more can be obtained.

As shown before the maximum J/S is 3 dB less for the four-phase system as compared to the biphase system. The reason is that for the same desired signal level, the component containing the short code is 3 dB less in the four-phase system. It is the timing for this short code that must be acquired first by the delay lock loop. As shown before, the array suppresses the CW jammer the same amount in the biphase and four-phase systems. Thus, although the maximum J/S is 3 dB higher in the biphase system, the jammer to short code component power ratio is the same for both systems when acquisition cannot occur.

Experimental results, therefore, show the CW interference protection of the four-phase system. The CW suppression was seen to be the same (about 30 dB) for both the biphase and the four-phase systems. The maximum J/S for acquisition was shown to be 20 dB for the four-phase system. This limit was seen to be due to system parameters, e.g., with a higher code modulation frequency, a higher maximum J/S could be attained.

To demonstrate smart jamming protection, the four-phase system was tested with a biphase jammer with the short code and a repeat jammer with biphase remodulation. These are the two jammer types that can jam the biphase system. The experimental system was tested by measuring the total acquisition time with smart jamming. The generation of the smart jammer and the experimental results are discussed below.

Figure 91 shows a schematic of the circuitry that generates the smart jammers. The circuitry generates either a biphase jamming signal with the short code or a jamming signal identical to that for a repeat

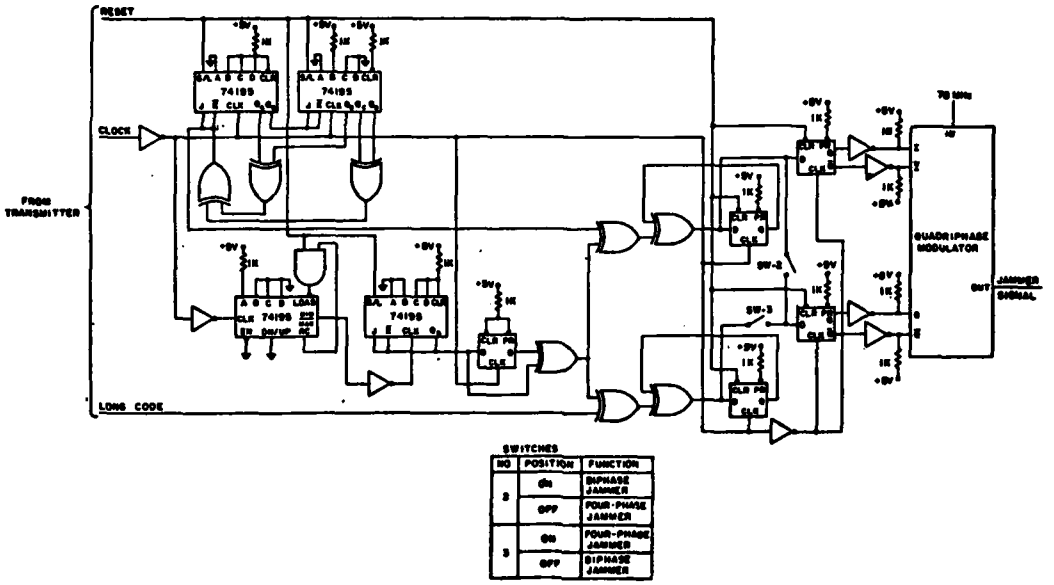


Figure 91. Circuit schematic of the smart jammer.

jammer with biphase remodulation. These signals are used in the channel simulator of Figure 57. The generation of the biphase and repeat jamming signals is described below.

The biphase smart jammer with the short code is generated as follows. The clock from the transmitter clocks the short code shift register. The reset signal from the transmitter sets the initial loading of this shift register. The initial loading of the shift register is different from that of the shift register in the transmitter. Thus, the code timing of the smart jammer is different from that of the transmitter so that the array can null one signal during short code acquisition. The timing offset was set arbitrarily to 178 code symbols with jammer's code a delayed version of desired signal's code. The short code is mixed with data such that the resulting signal has a spreading ratio of 14. The choice of 14 was arbitrary, and the use of data modulation simply illustrates what a smart jammer might do. The data modulation has little effect on the experimental results with a biphase jammer. The short code plus data then biphase modulates a 70 MHz signal when the switches are in the correct position. The resulting biphase smart jammer is used in the channel simulator where a phase shift of sixty degrees in the signal was set between the array elements.

The repeat jammer with biphase remodulation is generated as fol-
ws. The short code plus data are generated in the same way as for
e biphase jammer. In this case, the different short code timing
the smart jammer and the desired signal simulates the delay (about
illisecond for the experimental system) in the repeated signal.
e long code from the transmitter is mixed with the same data as the
ort code. Thus, both the short and long codes are mixed with data
ulating biphase remodulation by the jammer. The codes plus data
en modulate a 70 MHz signal to generate the repeat jammer with bi-
se remodulation. The repeat jammer signal is used in the channel
ulator in the same manner as the biphase signal.

Experimental results were obtained for the total acquisition
ne for the desired signal with smart jamming. The total acquisition
ne was determined by measuring the time interval between the system
set signal and a high transition in the long code correlation com-
ator output (see Figure 73). This output goes high when the long
de timing has been acquired. Fifty time measurements were taken
determine an average total acquisition time and a confidence interval
the actual acquisition time.

Figure 92 shows the experimental results obtained with a biphase
mmer with the short code. The total acquisition time is plotted
sus the jammer to desired signal power ratio. The experimental
sults are shown along with a curve that approximates the results.

The results can be explained as follows. For J/S less than
dB, the receiver cannot acquire the short code timing of the smart
mmer. Therefore, the smart jammer does not effect the acquisition
ne. The acquisition time for this case is about 0.2 seconds and
in agreement with the total acquisition time experimental results
scussed previously. When J/S is greater than -4 dB, the receiver
first acquire the short code timing of either the smart jammer
the desired signal. The acquisition time for this case is calcu-
ted theoretically below.

For the experimental system, the acquisition time with smart
mming can be calculated by considering several factors. First,
ing acquisition the code at the receiver is run faster than the code
the incoming signal. Second, the initial offset between the re-
iver's code and the desired signal's code (and, also, the jammer's
de) is random and has a uniform distribution between 0 and 255 code
mbols. Third, the timing offset between the desired and jamming
gnal's codes is 178 code symbols or about two thirds of the code
ngth. Finally, $E_s/N_0/_{IN}$ is large enough (14 dB) that the long code
quisition time is negligible compared to the total acquisition time.

With the above conditions, the acquisition time can be calculated
follows. The probability of acquiring the desired signal's short

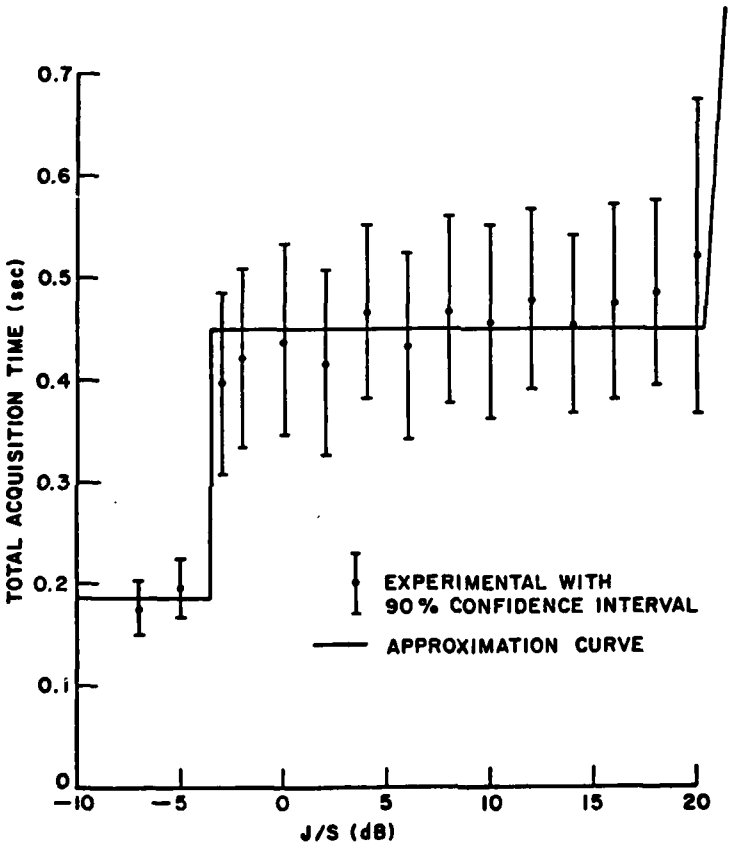


Figure 92. Total acquisition time versus jammer-to-signal power ratio for biphase jammer with short code.

code first can be seen to be two thirds. The maximum time to acquire the desired signal's code first is two-thirds of the maximum short code acquisition time (0.4 seconds from Table 10) or approximately 0.267 seconds. Therefore, the average acquisition time when the desired signal's short code is acquired first, can be seen to be approximately 0.133 seconds. The probability of acquiring the smart jammer's code first is one third. When the short code is acquired the system searches for the long code timing. Since the long code is not present on the jamming signal, 0.55 seconds later the receiver slews the short code timing to find the next signal with the short code. This signal is the desired signal. The slewing time is two thirds of the maximum short code acquisition time or approximately 0.267 seconds. Therefore, the acquisition time when the jammer's short code is acquired first is approximately 0.817 seconds. The average acquisition time with the smart jammer can now be calculated from the probability of acquiring each signal first and the average acquisition time when each signal is acquired first. Thus, the average acquisition time in seconds is

$$0.36 \triangleq 2/3(0.133) + 1/3(0.817) \quad . \tag{419}$$

The above value is only an approximation and is seen to be somewhat less than the experimental results shown in Figure 92.

When J/S is greater than 20 dB, as shown in Figure 92, the desired signal is no longer acquired. This maximum J/S for acquisition is the same as that for a CW jammer at 70 MHz. Therefore, a biphase jammer with the short code is no more effective in preventing acquisition than a CW jammer. As with the CW jammer, the maximum J/S for acquisition depends on the system parameters and would increase with code modulation frequency.

Figure 93 shows the experimental results obtained with a repeat jammer with remodulation. The total acquisition time is plotted versus the jammer to desired signal power ratio. The experimental results are shown along with a curve that approximates the results.

The experimental results are similar to those obtained with a biphase jammer and can be discussed in the same way. For J/S less than -1 dB, the smart jammer's short code is not acquired by the receiver. Therefore, the jammer has no effect on the acquisition time. When the smart jammer effects the acquisition time, the J/S is three decibels greater than with the biphase jammer. This is because with the four-phase jamming signal, the signal component with the short code contains only half the total signal power. Thus, the four-phase jammer must be three decibels stronger than the biphase jammer to obtain the same power in the signal component used in the short code acquisition.

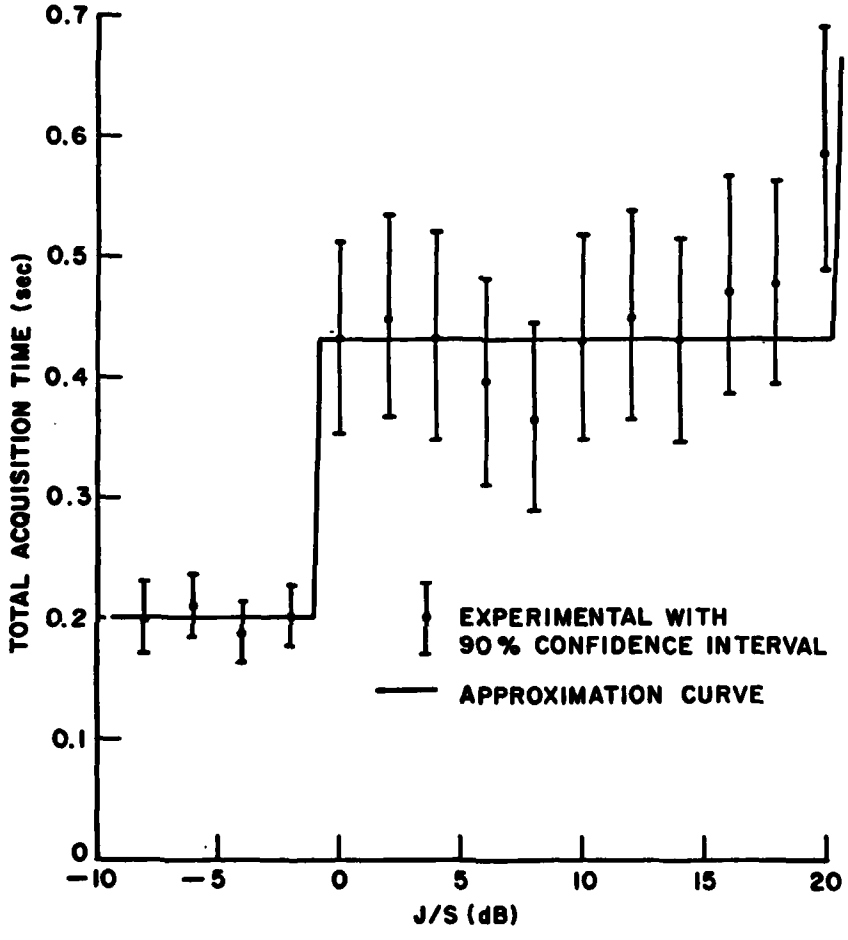


Figure 93. Total acquisition time versus jammer-to-signal power ratio for repeat jammer with biphase remodulation.

For J/S greater than -1 dB, the jammer signal can be acquired by the receiver and, therefore, will effect the acquisition time. The theoretical average acquisition time in this case is the same as that with the biphase jammer. The measured average acquisition time as shown in Figure 93 is approximately the same as that obtained with the biphase jammer.

As with the biphase jammer, when J/S is greater than 20 dB, the desired signal cannot be acquired in the experimental system. As before, the maximum J/S for acquisition will depend on the system parameters.

In summary, experimental results have verified theoretical results and shown the rapid acquisition and jammer protection of the four-phase system. Experimental results were in agreement with theoretical calculations of the probability of false alarm during acquisition, code tracking jitter, and long code acquisition time. Experimental results showed the rapid acquisition of the four-phase signal with noise. The conventional jammer protection of the four-phase system was shown to be only slightly less than that of the biphase system. Finally, experimental results with the four-phase system demonstrated that although a smart jammer may slightly increase the acquisition time, it is no more effective in preventing acquisition than a CW jammer.

CHAPTER XII

SUMMARY AND CONCLUSIONS

The purpose of this research was to develop a four-phase communication system for use with an adaptive array. This system was developed to improve upon a previously developed biphase system. The four-phase system was analyzed both theoretically and experimentally. The analytical and experimental results demonstrate the rapid acquisition and jammer protection of the four-phase system.

The four-phase system was developed by first examining the previous biphase system and then studying the four-phase modulation techniques which overcome the biphase system's shortcomings. The biphase system was shown to have two shortcomings: 1) short codes must be used for reasonable acquisition times, but short codes may not have adequate security for many applications, and 2) the biphase system is vulnerable to repeat jammers with biphase remodulation. To overcome the first shortcoming, a long and a short code were shown to be required on the signal. Several modulation techniques were presented which combined two codes. Because these signals were to be used with an adaptive array, reference signal generation techniques were described. To overcome the second shortcoming, a data modulation method other than biphase was shown to be required. Several data modulation techniques were presented and reference signal generation methods for these techniques were discussed. A particular type of four-phase signal was shown to be able to overcome the biphase system shortcomings. A communication system was developed for this system. The four-phase signal consists of two orthogonal biphase signals. One signal contains a short code for rapid acquisition. The other contains a long code to be used for protection against smart jammers. The reference signal generation technique uses the same reference signal generation loop as in the biphase system, but a biphase reference signal partially correlated with the received signal is generated. The signal acquisition technique involves a multi-step process. The short code timing is first acquired by the sliding correlation method. With the short code used in reference signal generation, the long code timing is rapidly acquired by the Rapid Acquisition by Sequential Estimation method. The long code is then used in reference signal generation.

To assure rapid acquisition of the signal at the receiver, the acquisition procedure was analyzed in detail. The acquisition of the short code timing by the sliding correlation method was studied first. The acquisition trajectory of the delay lock loop was shown without noise present with the signal. Equations were derived that describe

the acquisition process with noise in terms of the delay lock loop parameters. The tracking jitter of the delay lock loop was then analyzed. Equations were developed which determine the tracking jitter in terms of the delay lock loop parameters. Next, the long code acquisition process was analyzed. Differential detection of the four-phase signal in the acquisition process was discussed in detail. An appropriate model for the acquisition process was analyzed. Computer simulation results for the actual process were discussed. It was shown that very long codes (those that repeat once a year or less) can be acquired rapidly even with low received signal-to-noise ratios.

To assure that the long code can provide security in the system, long code structure was studied. Nonlinear codes were shown to be more secure than linear codes, but even linear codes were seen to provide reasonable security.

The effect was then discussed of various jamming techniques on the acquisition procedure. It was shown that conventional jamming, repeat jamming with remodulation, and biphase jamming with the short code could not jam the system.

An experimental four-phase system was then described, and experimental results discussed. The system provided an example of how the analytical results of this study can be used to develop a system to meet specific requirements. Circuit schematics showed how the acquisition procedure can be implemented. Experimental results verified analytical results. The experimental results also demonstrated the rapid acquisition (about 0.2 seconds) and conventional jamming protection (a maximum received jammer-to-signal ratio of 20 dB) of the system. The conventional jamming protection was shown to be close to that of the biphase system and could be increased with code frequencies greater than the 175.2 kHz used. Finally, it was shown that although a smart jammer may slightly increase the acquisition time, it is no more effective in preventing acquisition than a CW jammer. Thus, the four-phase system is not vulnerable to the same type of jamming techniques as the biphase system.

It is concluded that the four-phase communication system presented here provides both conventional and smart jamming protection with rapid acquisition of the signal at the receiver. The analytical and experimental results presented in this study can be used in designing such systems.

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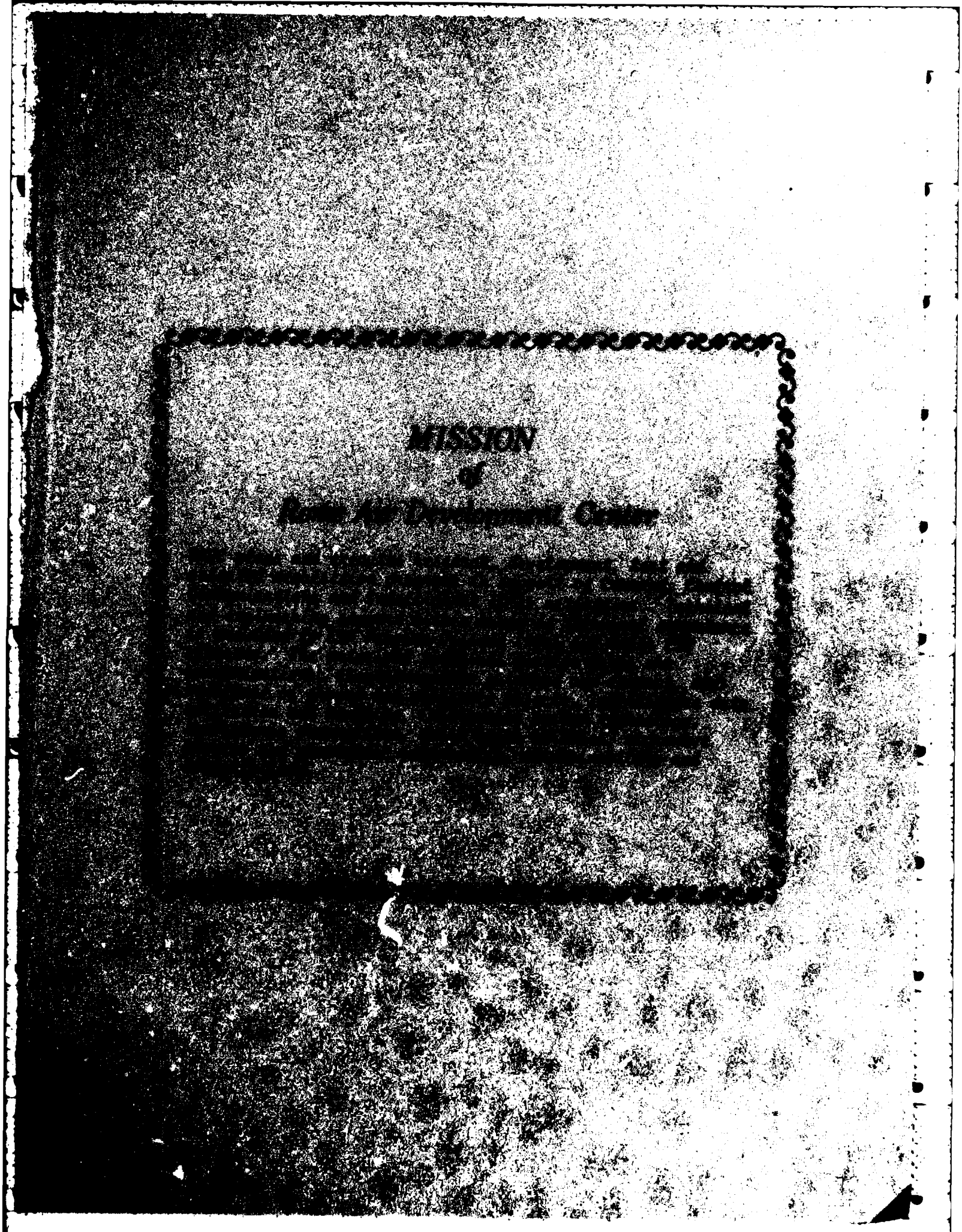
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