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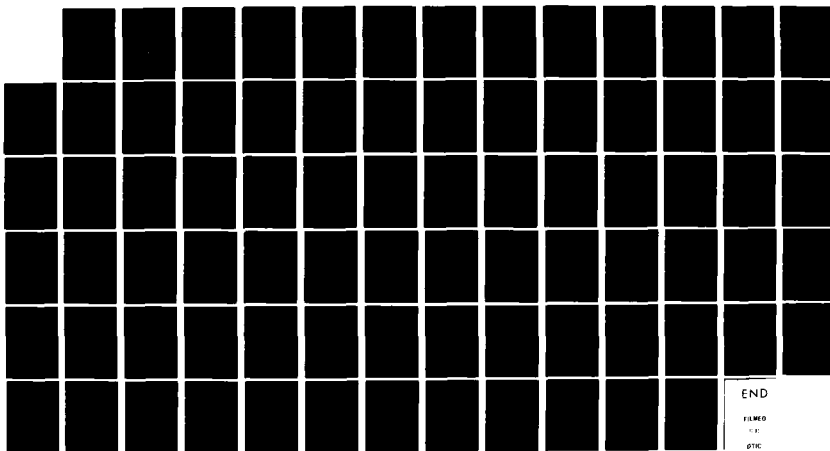
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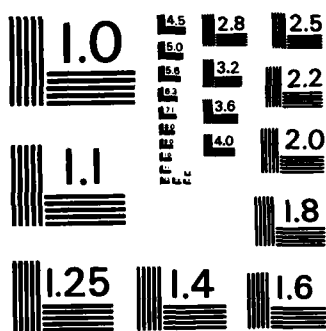
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Wideband Monolithic Microwave Amplifier Study

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The detailed study of factors limiting the performance of microwave monolithic distributed amplifiers utilizing GaAs FETS is continued. New expressions for gain, attenuation constant, phase constant and optimum numbers of devices are given. A sensitivity analysis is carried out and a computer program to analyze amplifier performance and aid in design is presented. The report concludes with a practical design for an 8-device amplifier from 2 to 20 GHz having a gain of 4.75 dB at 20 GHz.		

ECE-82-10

October 1982

Wideband Monolithic Microwave Amplifier Study

J. B. Beyer, R. C. Becker, J. E. Nordman,
S. N. Prasad and G. Hohenwarter



A

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I. FREQUENCY RESPONSE

1.1. Introduction

This report summarizes our efforts during the period 31 July 1981 to 30 June 1982 which was the second year of a three year program to study the design of distributed monolithic GaAs FET amplifiers in the 10 - 20 GHz region. We have continued our study of the limitations of transmission line attenuation begun during the first year. The attenuation caused by the line loading imposed by device parasitic resistances was found to be a fundamental limitation to gain and frequency response and must be carefully considered in the design of practical amplifiers.

1.2 Gain of the Distributed Amplifier

The distributed amplifier may be modeled as shown in Figure 1.1. The blocks characterized by the propagation constant γ represent lumped sections of transmission line. The details of the sections will be dealt with in section 1.3.

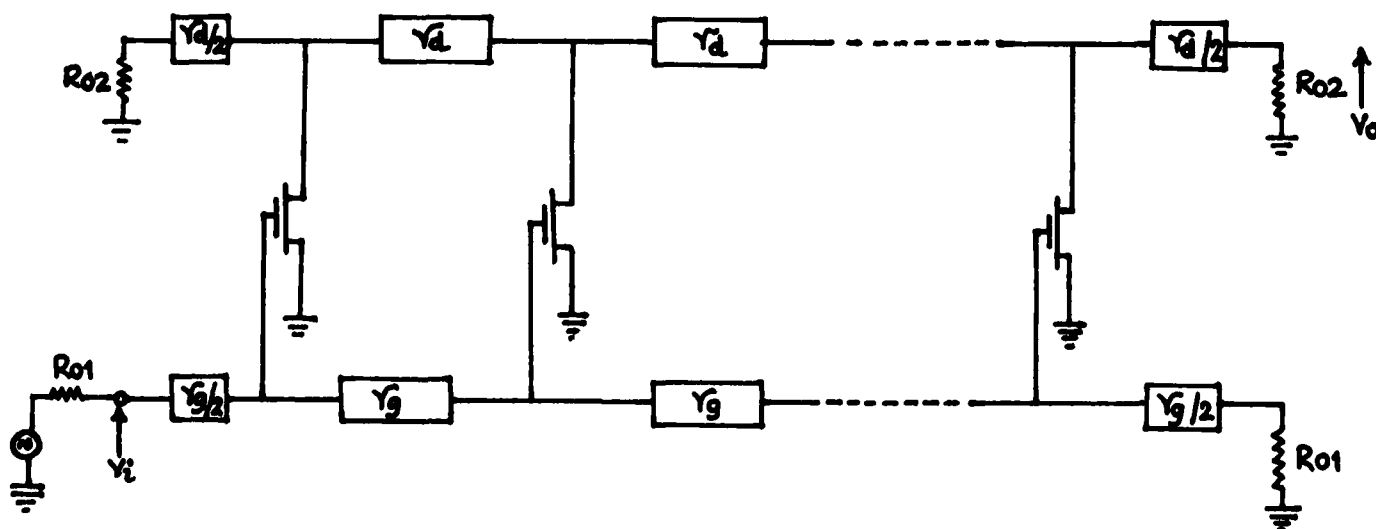


Fig. 1.1. Schematic of distributed amplifier.

where

γ_g = propagation constant on the gate line = $\alpha_g + j\beta_g$

γ_d = propagation constant on the drain line = $\alpha_d + j\beta_d$

α_g = attenuation constant per section on the gate line (nepers/section)

α_d = attenuation constant per section on the drain line (nepers/section)

β_g = phase shift per section on the gate line

β_d = phase shift per section on the drain line

Considering that in the microwave range the FET input circuits can be modeled by a series RC network, one may follow each signal path through the amplifier and find the total current delivered to R_{02} by summing the contributions of each active element.

The output voltage V_0 can be written as

$$V_0 = \frac{g_m R_{02} V_i}{2(1+j\omega C_g R_g)} \sum_{k=1}^n e^{-\frac{(2k-1)}{2} \gamma_g} e^{-\frac{(2n-2k+1)}{2} \gamma_d} \quad (1)$$

where

g_m - Device transconductance (mS)

C_g - Gate to source capacitance

R_g - Total resistance between gate and source terminals

R_{02} - Impedance of the drain line

From Equation (1) the expression for the voltage gain can be derived as

$$A = \frac{g_m}{2} \frac{R_{02}}{[1+(\omega/\omega_H)^2]^{1/2}} e^{-n/2(\gamma_g+\gamma_d)} \frac{\sinh[\frac{n}{2}(\gamma_g-\gamma_d)]}{\sinh[\frac{1}{2}(\gamma_g-\gamma_d)]} \quad (2)$$

where $\omega_H = \frac{1}{R_g C_g}$, gate circuit cutoff frequency.

Assuming $\beta_g = \beta_d$, a required condition, the following expressions for the magnitude of the voltage gain can be derived,

$$|A| = \frac{g_m R_{02}}{2[1+(\frac{\omega}{\omega_H})^2]^{1/2}} \frac{\sinh \frac{n}{2}(\alpha_d-\alpha_g)}{\sinh \frac{1}{2}(\alpha_d-\alpha_g)} e^{-n/2(\alpha_g+\alpha_d)} \quad (3)$$

Requiring $d(A)/dn = 0$ yields the optimum number of devices for maximum gain at a given frequency. This results in

$$n_{\text{opt}} = \frac{1}{\alpha_d - \alpha_g} \ln \left| \frac{\alpha_d}{\alpha_g} \right| \quad (4)$$

Figure 1.2 shows a plot of the gain of the distributed amplifier using 150 μm gate width device. The gain computed analytically is in good agreement with the data obtained from computer simulation (see section 4 for OPNODE CAD program).

1.3 Attenuation in Gate and Drain Lines

It is evident from section 1.2 that attenuation in the input and output transmission lines is of primary importance in the design and performance of microwave distributed amplifiers. It will now be dealt with in detail.

The gate and drain lines are actually lumped element transmission lines. They can be modeled as 'constant-k' low pass filters. The filter sections could be either in T-configuration or π -configuration. A gate line T-section shown in Fig. 1.3 is considered for analysis.

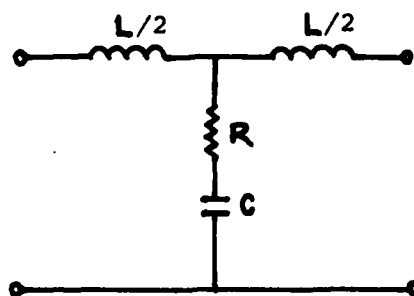


Fig. 1.3. Gate line T-section.

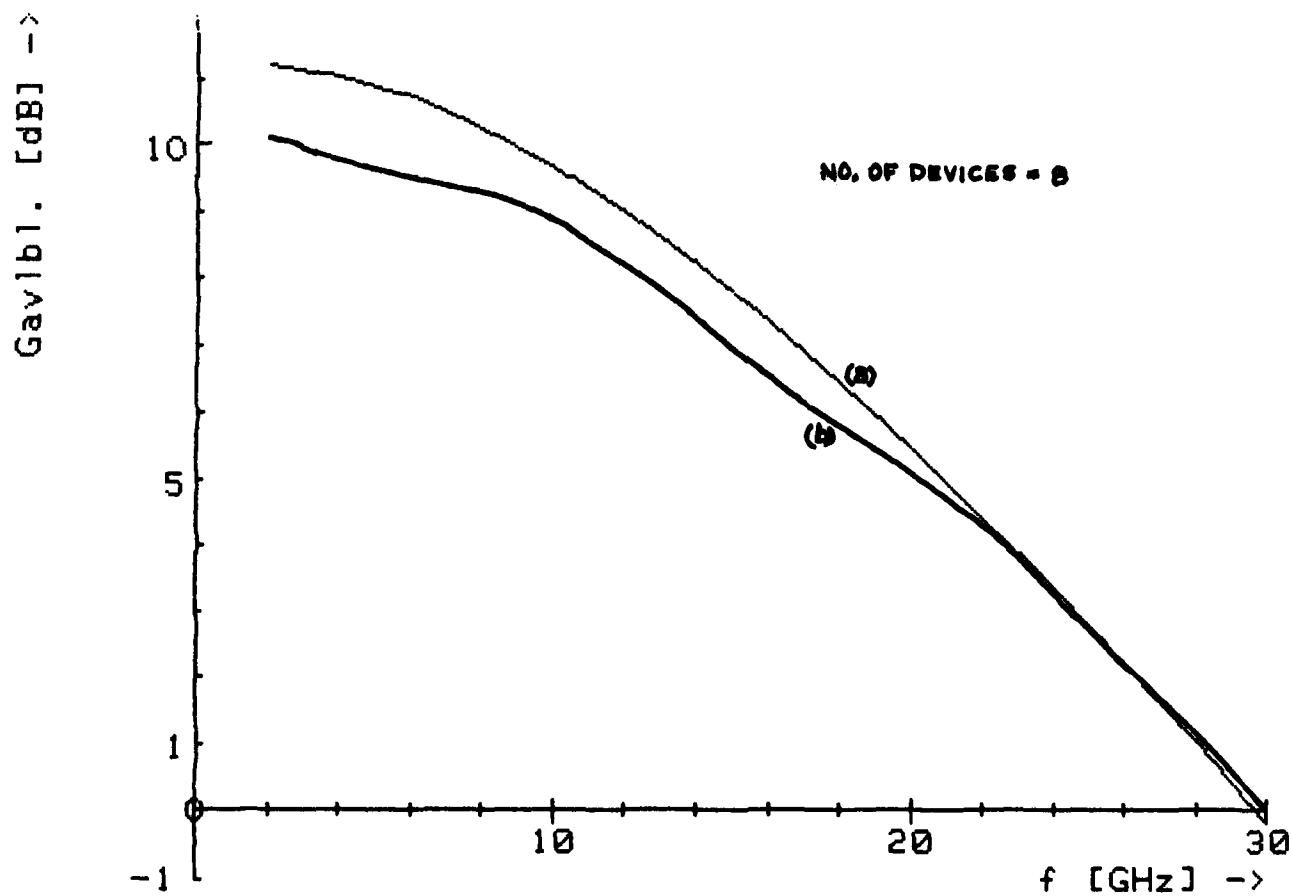


Fig. 1.2. Gain of Distributed Amplifier Using 150 μ Device

- (a) Analytical
- (b) Computer Simulation

Here the R and C in the shunt element are the resistance and capacitance seen between gate and source terminals in the usual microwave model of a GaAs FET.

In the analysis of the gate line T-section shown in Fig. 1.3 we assume that the loss per section is small. The transfer constant γ for a T-section is given by¹

$$\cosh \gamma = 1 + \frac{Z_1}{2Z_2} \quad (5)$$

where $\gamma = \alpha + j\beta$.

α = attenuation constant

β = phase constant.

$$Z_1 = j\omega L$$

$$Z_2 = R + \frac{1}{j\omega C}$$

Starting from equation (5) it can be shown that

$$\alpha_g \approx \frac{\omega^2 / \omega_H \omega_C}{\sqrt{1 + (\omega / \omega_H)^2 - (\omega / \omega_C)^2}} \text{ nepers} \quad (6)$$

where $\omega_H = \frac{1}{RC}$ and $\omega_C = \frac{2}{\sqrt{LC}}$. Equation (6) is valid for $\alpha \leq .4$ nepers/section. ω_H is the device input RC network cutoff frequency and ω_C is the lumped element transmission line cut off frequency. Thus we find that the attenuation per section of a T-network modeled gate line is a critical function of the cutoff frequencies ω_H and ω_C . Also, equation (6) indicates that gate line attenuation is highly frequency sensitive.

¹Zobel, O. T., BSTJ, 3, 567 (1923).

A similar analysis could be carried out for a drainline modeled as a T-section low pass filter. A section of the lumped element drainline is shown in Fig. 1.4. Here the R and C of the shunt element are the resistance and capacitance seen between the drain and source terminals in the microwave transistor model.

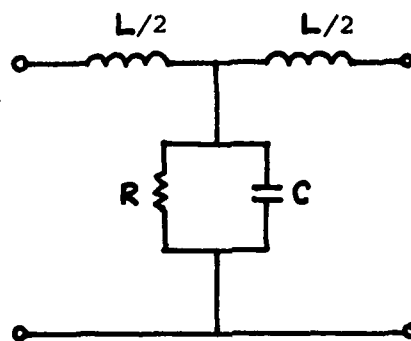


Fig. 1.4. Drain line T-section.

It can be easily shown that for this network

$$\alpha_d \approx \frac{\sqrt{\frac{L}{C}}}{2R \sqrt{1 - \left(\frac{\omega}{\omega_C}\right)^2}} \text{ nepers} \quad (7)$$

(valid for $\alpha \leq .4$ nepers/section)

For frequencies well below ω_C , Eq. (7) reduces to the equation for attenuation on a distributed line which will be developed shortly. Furthermore, it should also be noted that within that frequency range the attenuation is essentially invariant.

Now, let us look at the equations for attenuation of gate and drain lines modeled as uniform distributed transmission lines. The gate line can be modeled as a distributed transmission line as shown in Fig. 1.5.

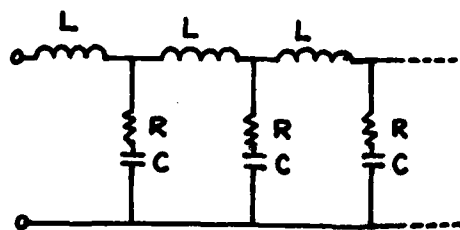


Fig. 1.5. Distributed gate line.

It can be shown that

$$\alpha_g = (1 + \omega^2 R^2 C^2)^{-1/4} \omega \sqrt{LC} \sqrt{\frac{\sqrt{1 + \omega^2 C^2 R^2} - 1}{2\sqrt{1 + \omega^2 C^2 R^2}}} \text{ nepers} \quad (8)$$

when $\omega RC \ll 1$, equation (8) reduces to,

$$\alpha_g \approx \frac{\omega^2 RC \sqrt{LC}}{2} = \frac{\omega^2 C^2 R Z_0}{2} \quad (9)$$

where $Z_0 = \sqrt{\frac{L}{C}}$, is the characteristic impedance of the gateline. It is interesting to note that equation (6) for a lumped line reduces to equation (9) for $\omega \ll \omega_H, \omega_C$.

Similarly if the drainline is modeled as a uniform distributed transmissionline as shown in Fig. 1.6, we obtain the following equation for the line attenuation.

$$\alpha_d = \omega \sqrt{LC} \left[1 + \left(\frac{G}{\omega C} \right)^2 \right]^{1/4} \sqrt{\frac{1 - 1/[1 + (\frac{G}{\omega C})^2]^{1/2}}{2}} \quad (10)$$

where $G = 1/R$

When $G/\omega C \ll 1$, equation (10) reduces to

$$\alpha_d \approx \frac{G}{2} \sqrt{\frac{L}{C}}$$

$$= \frac{GZ_0}{2} \quad (11)$$

where Z_0 is the characteristic impedance of the drainline.

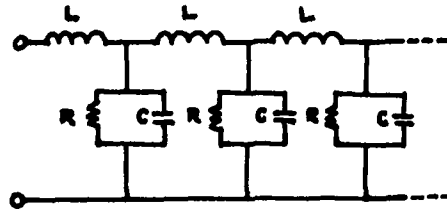


Fig. 1.6. Distributed drain line.

A close look at equations (6), (7), (9) and (11) shows that the gate line attenuation is more frequency sensitive than the drainline attenuation.

Figure 1.7 shows a plot of the gateline attenuation vs frequency and Figure 1.8 shows the drainline attenuation vs. frequency. There is good agreement between the numbers computed from equations (6), (7) and the data from computer simulation.

1.4 Equations for β /unequal β s

In the classical lossless distributed amplifier the input and output transmission line cutoff frequencies are made equal by choosing $L_1 C_1 = L_2 C_2$. This then yields equal phase constants which insures that the signal currents of each active device will add in the output line in the proper phase for maximum gain and no phase distortion. When losses are considered, however, not only is frequency dependent attenuation introduced as has been discussed, but unequal phase constants on the input and output lines also result. For the constant- k transmission line, the general expression

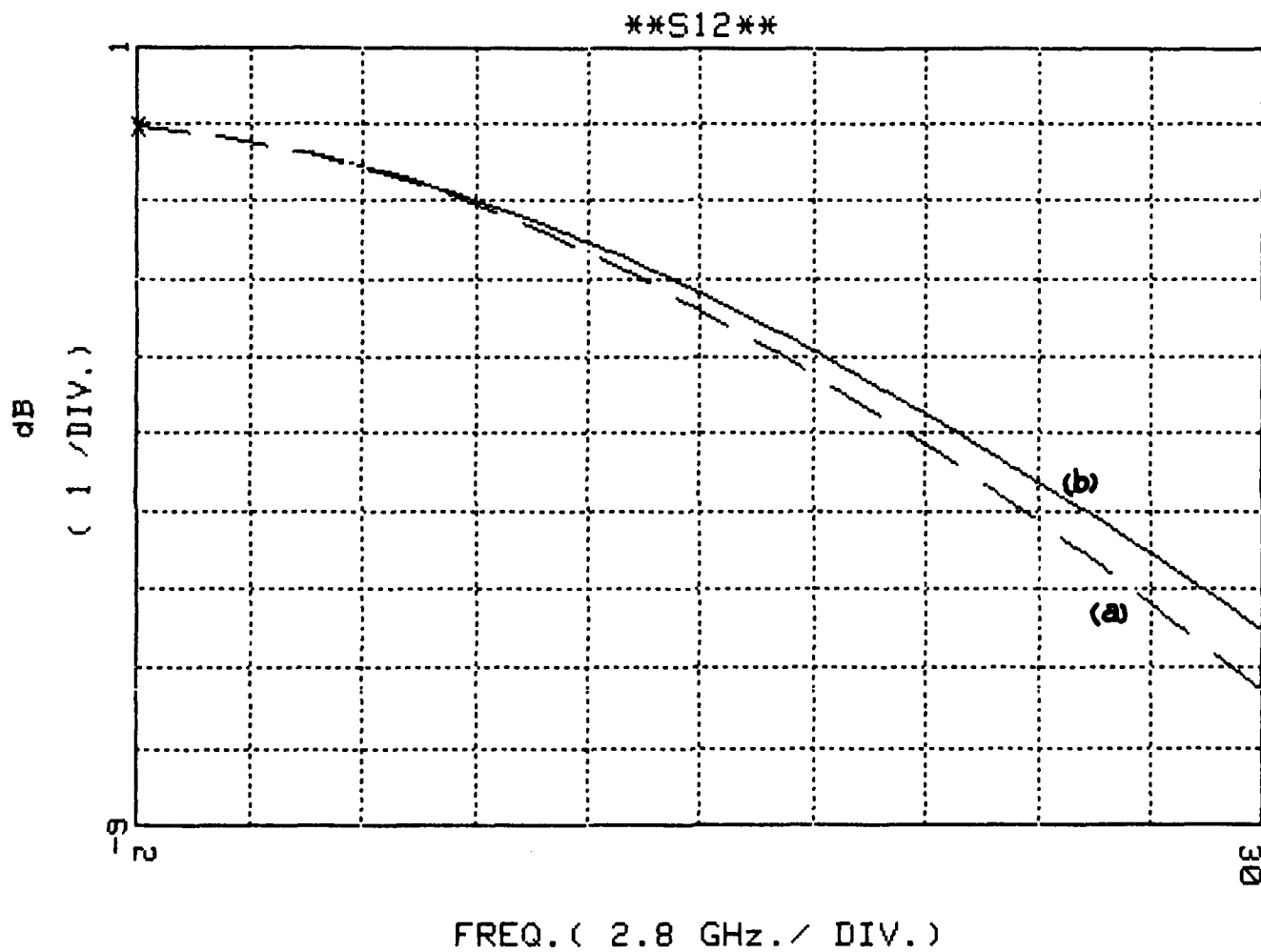


Fig. 1.7. Constant-k gate line attenuation for 3 sections using a 150 μm device and a 20 Ω gate line.

- a) Theoretical prediction
- b) CAD prediction

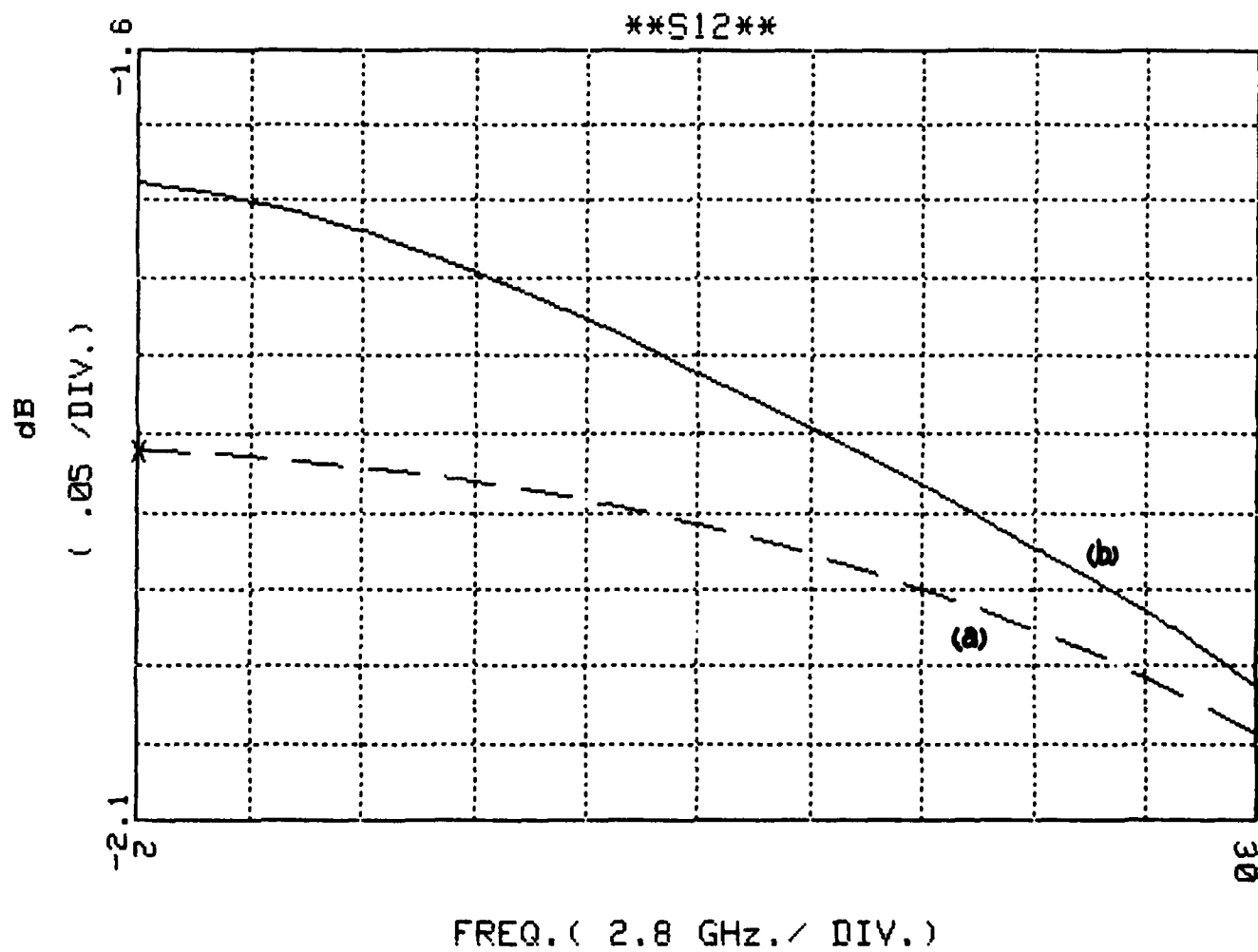


Fig. 1.8. Constant-k drain line attenuation for 3 sections, using a 150 μm device and a 100 Ω drain line.

- a) Theoretical prediction
- b) CAD prediction

$$\cosh\alpha \cos\beta + j\sinh\alpha \sin\beta = 1 + \frac{Z_1}{2Z_2} \quad (12)$$

must be solved for α and β where Z_1 is the series impedance element and Z_2 is the shunt impedance element of the transmission line section. For $\alpha \lesssim 0.4$, $\cosh\alpha \approx 1$, and (12) reduces to

$$\cos\beta \approx \operatorname{Re} \left[1 + \frac{Z_1}{2Z_2} \right] \quad (13)$$

When the appropriate impedances are inserted for Z_1 and Z_2 , we find

$$\beta_g \approx \cos^{-1} \left[1 - \frac{2\omega^2/\omega_{C1}^2}{1 + \omega^2/\omega_H^2} \right] \quad \text{where } \omega_H = \frac{1}{R_g C_g} \quad (14)$$

for the gate line, and

$$\beta_d \approx \cos^{-1} \left[1 - 2\omega^2/\omega_{C2}^2 \right] \quad (15)$$

for the drain line

These equations are in good agreement with computer models of the transmission lines. (Ref: Figs. 1.9, 1.10) It is important to note the factor of $(1 + \omega^2/\omega_H^2)$ in the expression for β_g . The presence of this factor gives β_g a slightly positive curvature while β_d has a slightly negative curvature; The result is a phase velocity mismatch between gate and drain lines at high frequencies despite the identical cutoff frequencies. For operation below $\frac{1}{2} f_c$, the approximation

$$\beta = \omega\sqrt{LC} \quad (16)$$

is adequate.

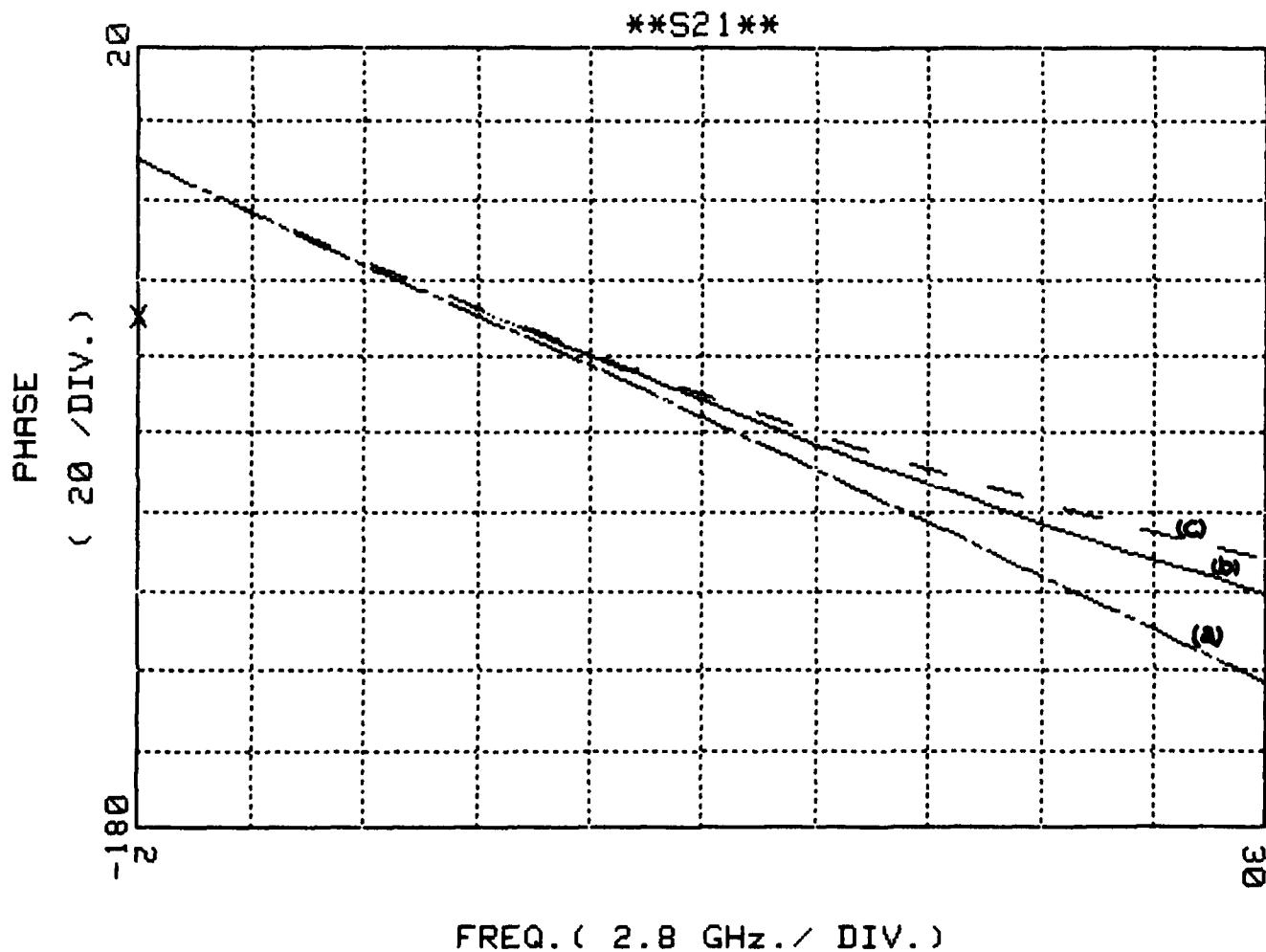


Fig. 1.9. Constant-k gate transmission line phase characteristics for 3 sections using a 150 μm device with 20 Ω characteristic impedance and a 72 GHz cutoff.

- a) Linear approximation: $\beta = \omega \sqrt{L_g C_g}$
- b) CAD prediction
- c) Theoretical prediction

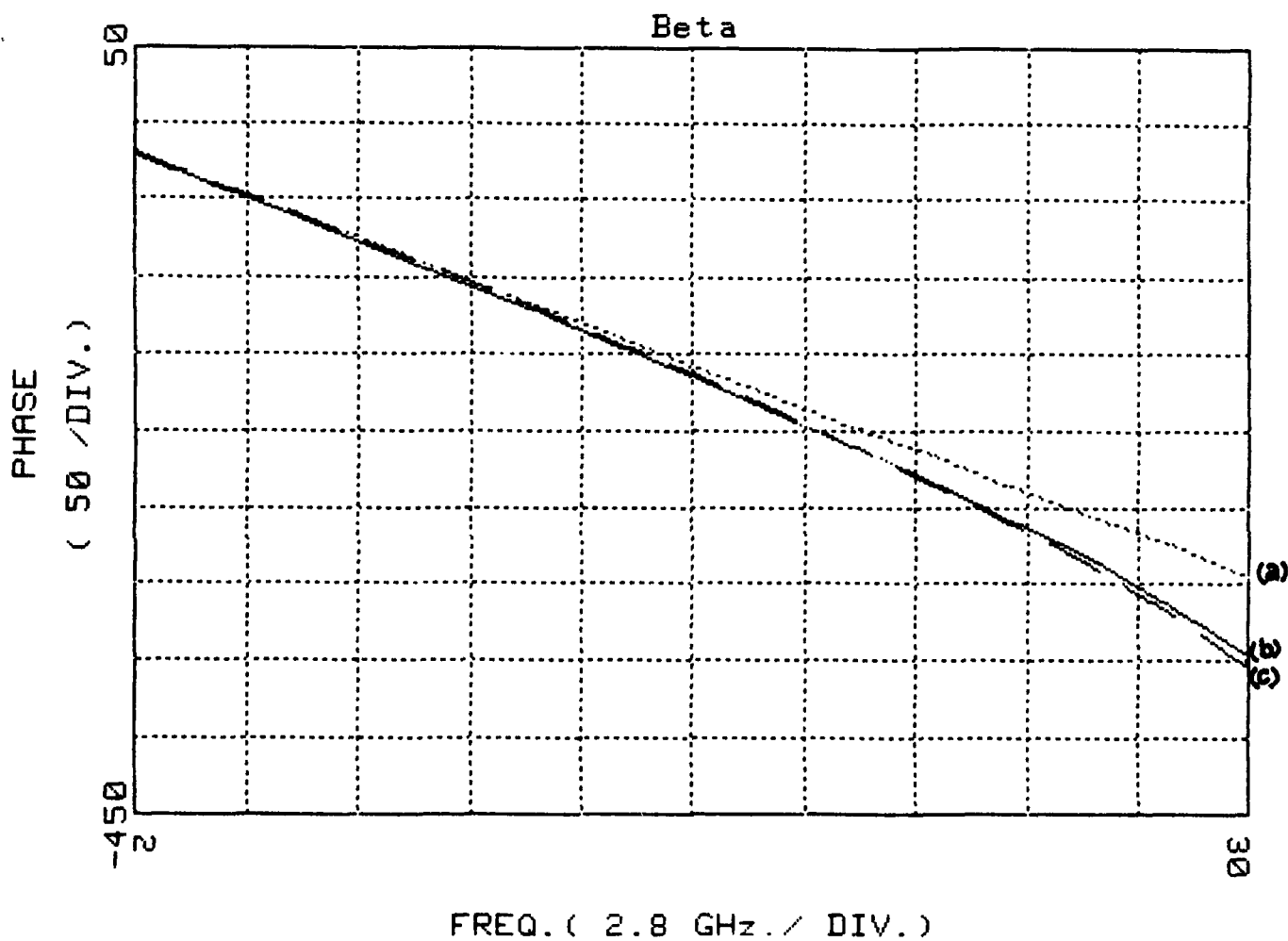


Fig. 1.10. Constant-k drain transmission line phase characteristics for 3 sections using a 300 μm device with 100 Ω characteristic impedance and a 37 GHz cutoff.

- a) Linear approximation: $\beta = \omega \sqrt{L_d C_d}$
- b) CAD prediction
- c) Theoretical prediction

1.5 M-Derived Filter Sections

In the previous discussion, only the constant-k type of transmission line was considered. Use of only this type of line restricts the ratio of gate line impedance to drain line impedance through the required approximate matching of cutoff frequencies for both lines. Previously, considerable emphasis was placed on modifying frequency response by using m-derived line sections [2] [3]. Here, we explore impedance modification.

Starting from the fundamental equations for cutoff frequency and impedance

$$f_C = \frac{1}{\pi\sqrt{LC}} \quad R_0 = \sqrt{\frac{L}{C}} \quad (17)$$

the requisite L and C for a particular R_0 and f_C may be found as

$$L = \frac{R_0}{\pi f_C} \quad C = \frac{1}{\pi f_C R_0} \quad (18)$$

Obviously, C bears no relation to C_d , which is ultimately the value we wish to use. Clearly, the required pad capacitance could be added, but an important advantage of using m-derived filters would be sacrificed.

If one defines the factor

$$m = \frac{C_g}{C} \quad \text{or} \quad m = \frac{C_d}{C} \quad (19)$$

and restricting $m \leq 1$, it can be seen from Fig. 1.11 that the series inductance of the m-derived line section is smaller than that of the constant-k line section by a factor of m.

²Bassett, H. G., Kelly, L. C., Proc. IEE, Vol. 101, Pt. III, pp. 5-14 (1954).

³Sarma, O. G., Proc. IEE, Vol. 102B, pp. 689-697 (1955).

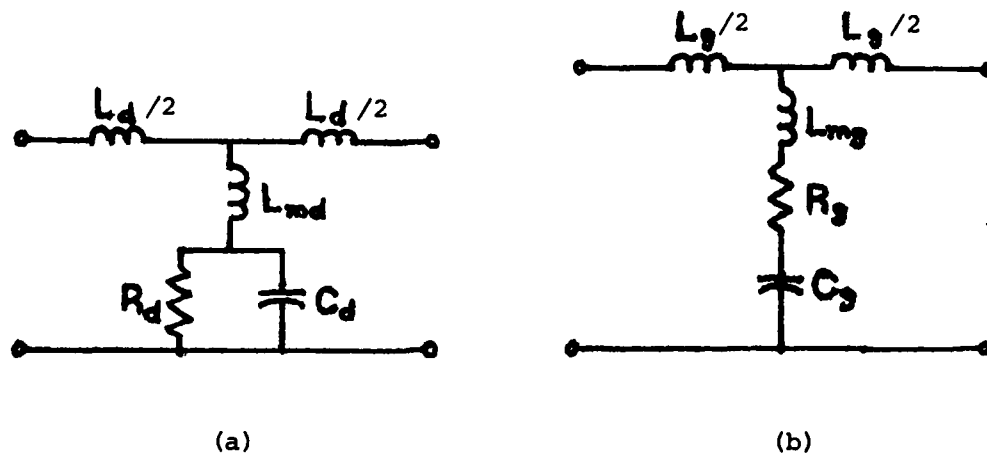


Fig. 1.11. T-section m-derived transmission line. (a) for drain line; b) for gate line.

The significance of the reduction of series inductance becomes apparent when the synthesis of the inductors from microstrip is considered.

It can be easily shown that the inductance of an electrically short microstrip transmission line is

$$L_s = \frac{Z_0 d}{v_p} \quad (20)$$

where L_s is the equivalent inductance, d is the line length, and v_p is the phase velocity of the line. If the length $d \leq \lambda/7$, the error is $< 15\%$. For a particular substrate, given the required current handling capacity of these elements, the lower boundary on the width of the microstrip is established. The required inductance determines the length, d , and the error criterion sets the useful upper frequency limit of the inductor. Use of m-derived transmission line sections offers the possibility of reducing L_s , and hence, increasing the useful upper frequency limit of the synthesized line.

When using m-derived transmission lines, one must not assume that β for the m-derived line behaves the same as for the constant-k line. Instead,

$$\beta_d \approx \cos^{-1} \left\{ 1 + \frac{\frac{2\omega^2}{\omega_{p2}^2} \left[\frac{4\omega^2}{\omega_{d2}^2 \omega_{T2}^2} + \frac{4}{\omega_{T2}^2} - \frac{1}{\omega_{d2}^2} \right]}{\frac{8\omega^2}{\omega_{T2}^2} \left[\frac{2\omega^2}{\omega_{d2}^2 \omega_{T2}^2} + \frac{2}{\omega_{T2}^2} - \frac{1}{\omega_{d2}^2} \right] + \frac{1}{\omega_{d2}^2}} \right\} \quad (21)$$

$$\omega_{T2} = \frac{2}{\sqrt{L_{md} C_d}}$$

$$\omega_{p2} = \frac{2}{\sqrt{L_d C_d}}$$

$$\omega_{d2} = \frac{1}{R_d C_d}$$

and

$$\beta_g \approx \cos^{-1} \left[1 - \frac{\omega^2 L_g C_g - \omega^4 L_{mg} L_g C_g^2}{2[(1 - \omega^2 L_{mg} C_g)^2 + \omega^2 R_g^2 C_g^2]} \right] \quad (22)$$

where β_d is the drain line phase constant and β_g is the gate line phase constant. The obvious lack of similarity to Eqs. 14 and 15 for the constant-k line should be sufficient to indicate the need for careful consideration of phase velocity when the line is used near its cutoff frequency. Below $f_c/2$, the phase constants may be approximated as

$$\beta_g \approx \sqrt{L_g C_g} \quad (23)$$

$$\beta_d \approx \sqrt{L_d C_d}$$

with modest accuracy.

As can be seen in Figs. 1.12 and 1.13, the Eqs. 21 and 22 are in good agreement with the values obtained by computer simulation. Eq. 21 was plotted for a line of $f_c = 25$ GHz, and deviates above f_c . Eq. 22 was plotted for an $f_c = 72$ GHz. It is particularly interesting to note that the phase constants of the constant-k gate and drain lines from which the m-derived filters were developed are given by

$$\beta_g = \frac{\omega}{m} \sqrt{L_g C_g} \quad \beta_d = \frac{\omega}{m} \sqrt{L_d C_d} \quad (24)$$

and are not good approximations to the resulting m-derived filters.

Attenuation of the m-derived gate and drain lines is given by

$$\alpha_g = \frac{\frac{\omega R_g C_g}{\omega^2 L_{mg} C_g - 1}}{\left[\frac{4(1 - \omega^2 L_{mg} C_g)^2 + \omega^2 R_g^2 C_g^2}{\omega^2 L_g C_g + \omega^4 L_{mg}^2 L_g C_g^2} - 1 \right]^{1/2}} \quad (25)$$

$$\alpha_d = \frac{\frac{\omega/\omega_d}{4\omega^2/\omega_{T2}^2 - \omega^2/\omega_d^2 + 4\omega^4/\omega_d^2 \omega_{T2}^2}}{\left[\frac{\omega_{pd}^2 [(1 - 4\omega^2/\omega_{T2}^2)^2/\omega_d^2 + 16\omega^2/\omega_{T2}^4]}{\omega^2/\omega_d^2 - 4\omega^2/\omega_{T2}^2 - 4\omega^4/\omega_d^2 \omega_{T2}^2} - 1 \right]^{1/2}} \quad (26)$$

Eqs. 25 and 26 are plotted in figs. 1.14 and 1.15. In general, the m-derived transmission lines display slightly higher attenuation than a constant-k line of the same cutoff frequency and slightly higher impedance. Thus, the m-derived line appears to be doubly deficient.

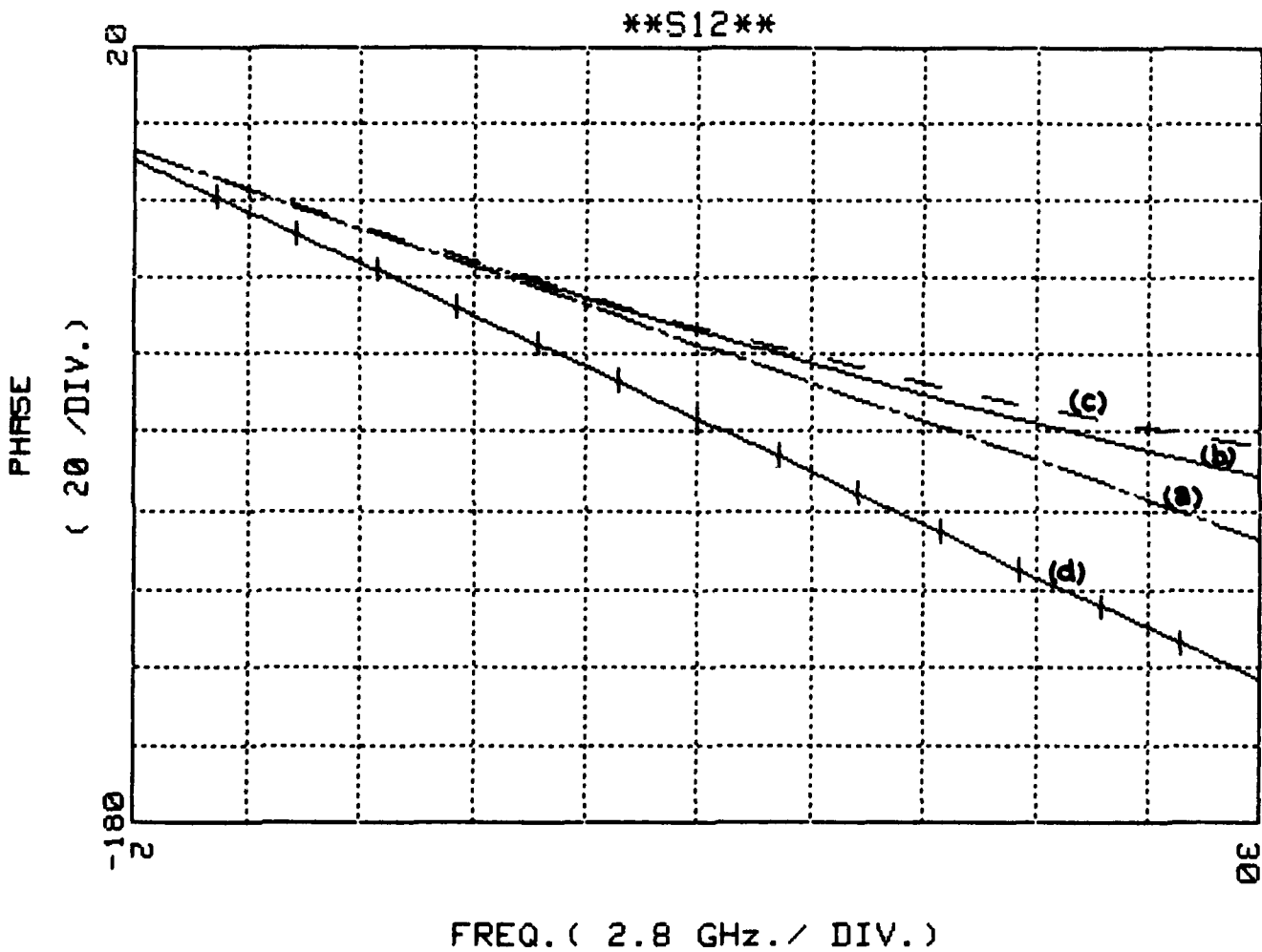


Fig. 1.12. M-derived gate transmission line phase characteristics for 3-sections using a 150 μm device with 15 Ω characteristic impedance ($m = 0.748$) and a 72 GHz cutoff.

- a) Linear approximation: $\beta = \omega \sqrt{L_g C_g}$
- b) CAD prediction
- c) Theoretical prediction
- d) Constant-k linear approximation: $\beta = \omega \sqrt{L_g C_g} / m$

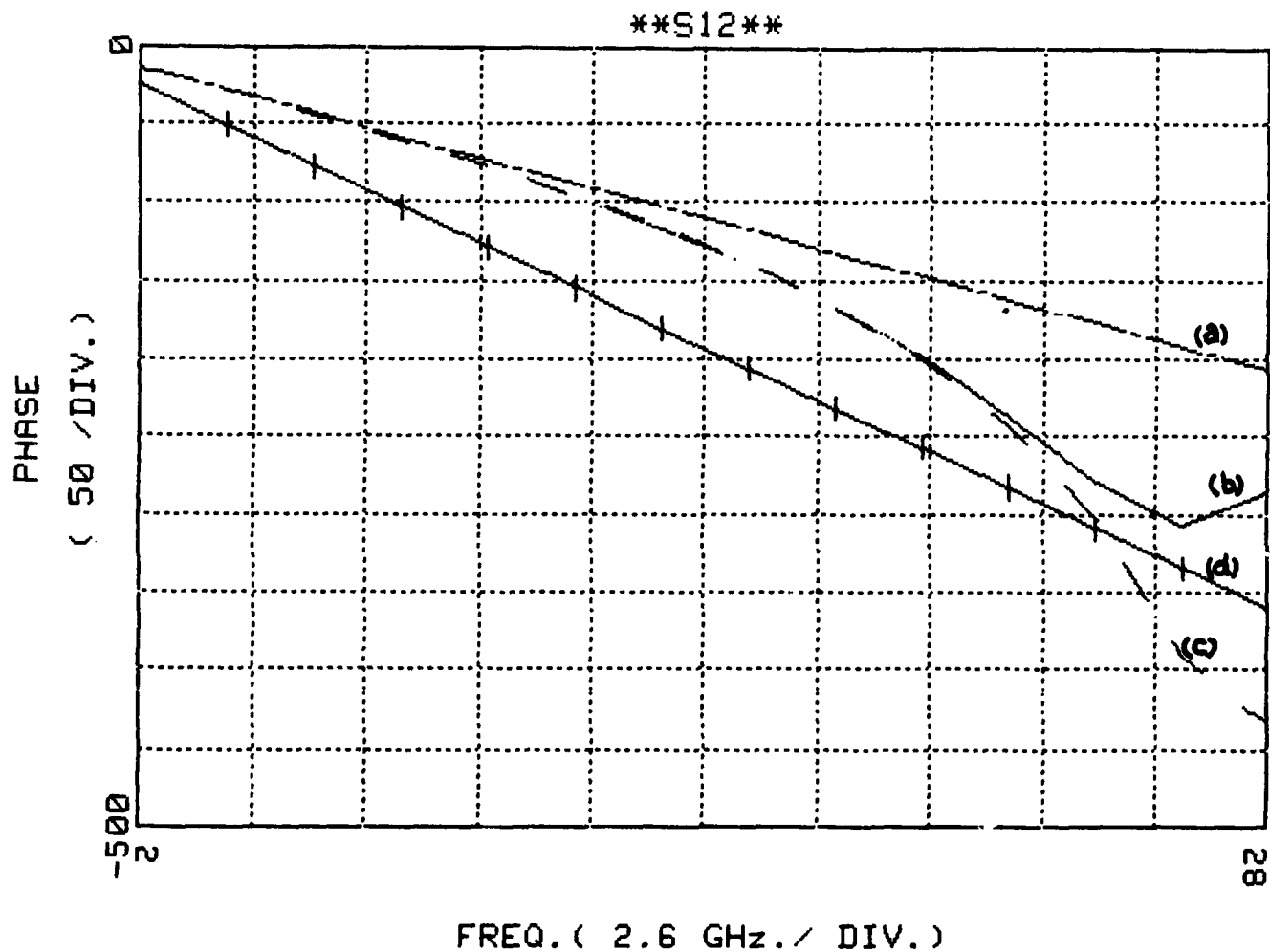


Fig. 1.13. M-derived drain transmission line phase characteristics for 3 sections of line using a 300 μm device with 80 Ω characteristic impedance ($m = 0.572$), and 25 GHz cutoff.

- a) Linear approximation: $\beta = \omega \sqrt{L_d C_d}$
- b) CAD prediction
- c) Theoretical prediction
- d) Constant-k linear approximation: $\beta = \omega \sqrt{L_d C_d} / m$

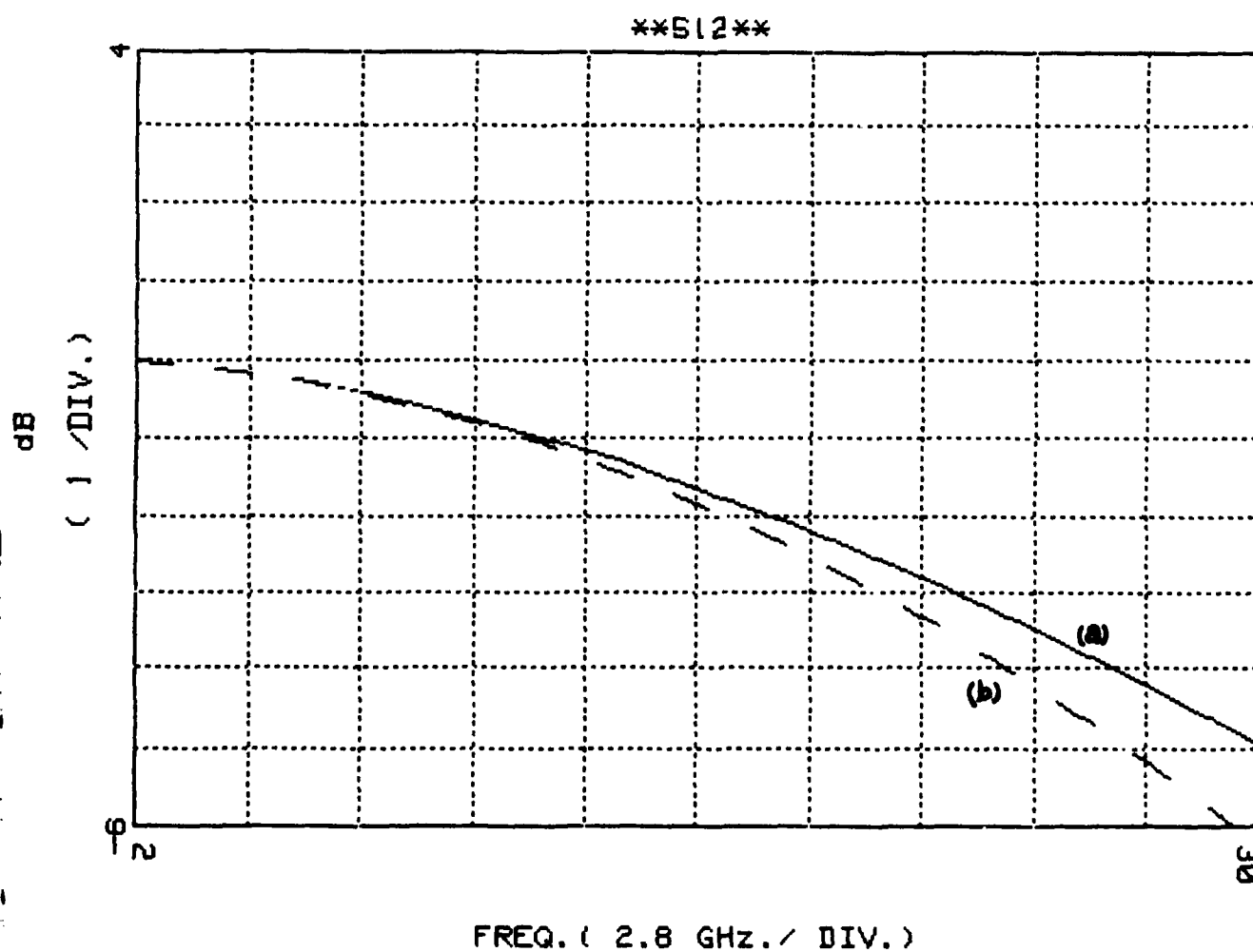


Fig. 1.14. M-derived gate transmission line attenuation for 3 sections using a 150 μm device with 15 Ω characteristic impedance ($m = 0.798$) and a 72 GHz cutoff.

- a) CAD prediction
- b) Theoretical prediction

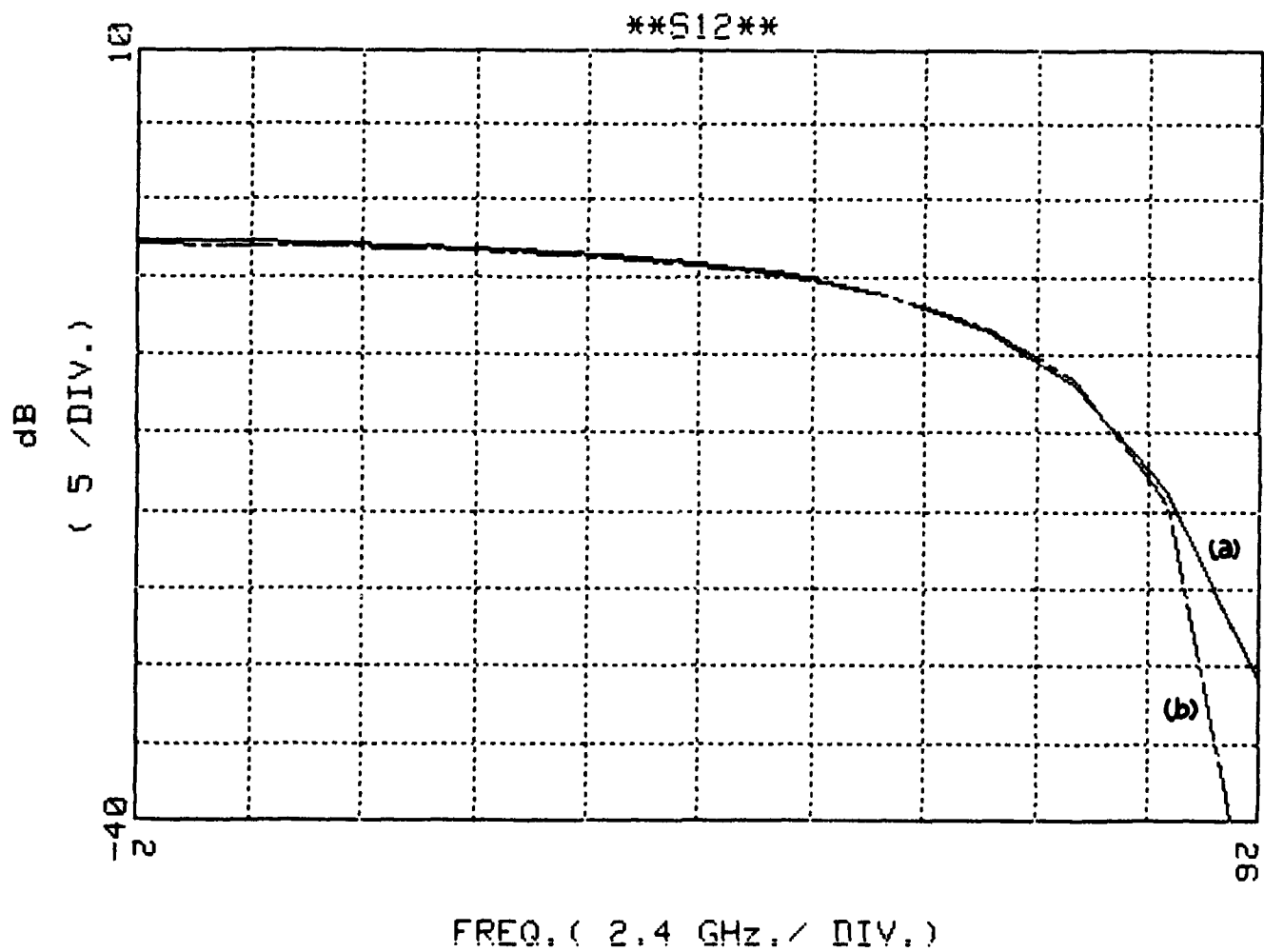


Fig. 1.15. M-derived transmission line attenuation for 3 sections using a 300 μm device with 80 Ω characteristic impedance ($m = 0.572$) and a 25 GHz cutoff.

- a) CAD prediction
- b) Theoretical prediction

II. Gain-Bandwidth Considerations

2.1 Classical Approach

If the active devices in a distributed amplifier are considered lossless and can be modeled simply with a current generator and input and output capacitances one can easily show that Eq. 3 (Section 1.2) reduces to

$$A = \frac{n g_m R_{02}}{2} \quad (26)$$

With the frequency in this case limited only by the line cutoff frequency, a gain-bandwidth product can be formed from (26) yielding

$$A f_c = \frac{n g_m}{2 \pi C_g} \left(\frac{C_g}{C_d} \right) \quad (27)$$

This allows operation considerably higher in frequency than the maximum one would calculate from the device above. This frequency, which results from the condition $MAG = 1$, is usually given as

$$\omega_{MAX} = \frac{g_m}{2 C_g} \sqrt{\frac{R_d}{R_g}} = \frac{\omega_T}{2} \sqrt{\frac{R_d}{R_g}} \quad (28)$$

for an FET. This, of course, is one of the advantages of the classical distributed amplifier resulting from the fact that individual device current contributions are summed in the load and hence individual transistor gain need not be greater than one.

However, in considering real MESFET devices for such an amplifier it is necessary to realize that device speed limitations and unavoidable parasitic elements must be added to the simple equivalent circuit. Transit time effects give an upper frequency for use of the circuit model and begin to cause distortions at frequencies of the order of

$$\omega_{\text{transit}} = \frac{1}{\tau} = \frac{g_m}{C_{\text{intrinsic}}} \quad (29)$$

This of course is an upper limit for any amplifier configuration. When the resistance R_g in series with the gate capacitor and R_d in shunt with the drain current generator are included we can form a more realistic gain bandwidth product by multiplying Eq. 3 directly by the line cutoff frequency

$$Af_C = \frac{f_T}{(1 + (\omega/\omega_H)^2)^{1/2}} \frac{C_g}{C_d} \frac{\sinh n/2 (\alpha_g - \alpha_d)}{\sinh \frac{1}{2} (\alpha_g - \alpha_d)} e^{-\frac{n}{2} (\alpha_g + \alpha_d)} \quad (30)$$

where $f_T = \frac{g_m}{2\pi C_g}$; $\omega_H = \frac{1}{R_g C_g}$.

Equation 30 shows the factor of increase over f_T possible and illustrates the importance of line attenuation as well as the gate circuit cutoff frequency. Table 2.1 shows some values from Eq. 30 calculated at 20 GHz using a typical 300 μ transistor (TI 78B1-55Ic, $f_H = 34$ GHz). From Eq. 4, n_{opt} for this amplifier is 3.14.

n	1	2	3	4	5	6
Af_C/f_T	2.15	4.6	5.08	4.84	4.48	3.87

Table 2.1

It should be pointed out that because of the frequency dependence of α_g and α_d , Eq. 30 may yield gain fall off well below ω_H . Hence this gain-bandwidth differs from the classical one in that the gain is not flat out to the vicinity of ω_c .

2.2 Gain Bounds

The drain resistance considered by itself imposes a limitation on the voltage level on the output line and hence on the gain. This can easily be seen by considering one section, say the p -th, of the output line. The current generator which delivers a power of $V_p I_{\text{gen}}$ must supply a power greater than that demanded by the parasitic drain resistor, V_p^2/R_d , if the output line voltage is to continue to grow at the $(p+1)$ -th device. Hence

$$V_{\text{out}} g_m V_{\text{in}} > V_{\text{out}}^2/R_d \quad (31)$$

or

$$A_V = \frac{V_{\text{out}}}{V_{\text{in}}} \leq g_m R_d \quad (32)$$

Thus, regardless of the number of stages the maximum voltage gain must be limited to the value $g_m R_d$.

Equations 26 and 32 then give us bounds for the gain as a function of the number of devices. One would expect our true response in a practical case to approach these bounds asymptotically at best as shown in Fig. 2.1.

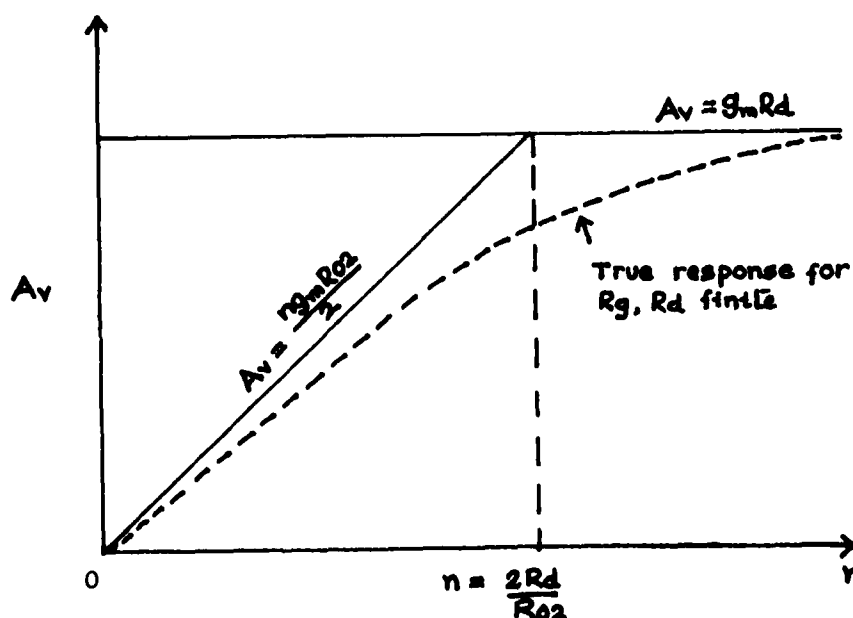


Figure 2.1

The effect of the resistance R_g is more complicated. First of all it causes a frequency dependent decay in the voltage $V_{i(n)}$ at each position in the input line. In addition, the voltage $v_{g(n)}$ which drives the output current generator is now a frequency dependent fraction of the voltage on the input line. Specifically

$$|v_{g(n)}| = \frac{|V_{i(n)}|}{\sqrt{1 + \omega^2 / \omega_H^2}}$$

$$\text{where } \omega_H = \frac{1}{R_g C_g}$$

$$V_{i(n)} = V_{i(0)} e^{-\alpha_g n},$$

and α_g is given by Eq. (6).

The effect of this on the gain curve is to further decrease the gain at high frequencies such that a maximum occurs at some n as was shown in Eq. 4. This maximum decreases in magnitude as well as in n value as frequency increases (as shown in Fig. 2.2.)

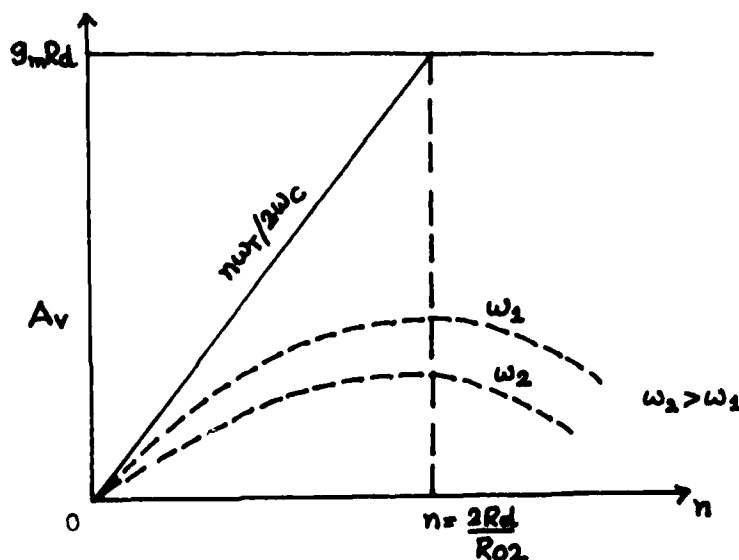


Figure 2.2

2.3 Figure of Merit

In comparing gain and bandwidth for distributed and cascade amplifiers made with the same devices one notes the following:

- 1) At mid-band one assumes all of the generator voltage driving a cascade amplifier appears across C_g . As such the stage gain becomes

$$A_C = g_m \frac{R_d}{2} \sqrt{\frac{R_{02}}{R_D}} \quad (33)$$

If the distributed amplifier also drives the same load, namely R_{02} , one sees from (32) that

$$A_D = 2 \sqrt{\frac{R_d}{R_{02}}} A_C \quad (34)$$

- 2) the high frequency cutoff for voltage gain for a stage of a cascade amplifier is ω_H . This frequency also dictates the high frequency performance of the distributed amplifier but in a more complicated way. Because of the effect of input line attenuation one can expect a voltage gain decrease for frequencies somewhat below ω_H .

Note that in a typical FET, ω_H is larger than $\omega_{\max}$. This implies that the voltage gain remains constant beyond $\omega_{\max}$ but that the device has no power gain beyond this frequency. This, of course, points out the importance of the unity current gain frequency ω_T in dictating the high frequency performance.

- 3) Power gain can be achieved with a single stage amplifier up to a frequency

$$\omega_{\max} = \frac{\omega_T}{2} \sqrt{\frac{R_d}{R_g}}$$

as long as $\omega_{\max} < \omega_{\text{transit}}$

- (4) Power gain can be achieved for a lossless distributed amplifier up to frequencies beyond the cutoff of the transmission lines if $\omega_c < \omega_{\text{transit}}$.
- (5) Broad band uniform gain for a lossless distributed amplifier, however, is limited by

$$\omega_c = \frac{2}{\sqrt{LC}}$$

- (6) Power gain for a lossy distributed amplifier with a series $R_g C_g$ input is limited at least by

$$\omega_H \approx \frac{1}{R_g C_g}.$$

In fact, because V_g decreases along the line more rapidly as frequency rises, the optimum n also decreases with frequency. Therefore, for a given n , there are two sources for output decline and one would expect the frequency limits to be less than ω_H with a value probably decreasing with increasing n .

It is evident from the foregoing that a suitable figure of merit for judging distributed amplifier performance is not a simple matter to define. We attempt now to find the MAG for a distributed amplifier so as to determine analytically from it the maximum frequency of operation.

From Eq. (1) (section 1.2) one can write for the output power

$$P_{\text{out}} = |v_0^2|/R_{02}$$

$$= \frac{g_m^2 V_i^2 R_{02}}{4(1+(\omega/\omega_H)^2)} \left[\frac{\sinh \frac{n}{2} (\alpha_d - \alpha_g)}{\sinh \frac{1}{2} (\alpha_d - \alpha_g)} e^{-\frac{n}{2} (\alpha_g + \alpha_d)} \right]^2 \quad (35)$$

The input impedance of the gate line can be written as

$$Z_{in} = \sqrt{\frac{L_g}{C_g}} (1+j \omega/\omega_H)^{1/2} \left(1 - \frac{(\omega/\omega_c)^2}{4(1+j \omega/\omega_H)} \right)$$

$$\approx R_{01} (1+j \omega/\omega_H)^{1/2} \quad \text{for } \omega \ll \omega_c \quad (36)$$

Equation 36 allows the calculation of the input power, and the resultant power gain using (35) becomes

$$MAG = \frac{g_m^2 R_{02} R_{01}}{4(1 + (\omega/\omega_H)^2)^{3/4} (1 + (\omega/2\omega_H)^2)^{1/2}} \left[\frac{\sinh \frac{n}{2} (\alpha_d - \alpha_g)}{\sinh \frac{1}{2} (\alpha_d - \alpha_g)} e^{-\frac{n}{2} (\alpha_g + \alpha_d)} \right]^2 \quad (37)$$

Equation 37 is implicitly frequency dependent through α_g and α_d , and hence finding the frequency at which $MAG = 1$ is a formidable task.

Because of such problems a computer program has been developed to study the distributed amplifier performance as a function of its many design variables. The program will be described in a later section of this report but this section will conclude with some of the results of the use of this program.

Figure 2.3 shows the gain and n_{opt} as a function of ω_H with the line inductance as a running parameter.

The drainline inductance is chosen such that both lines have the same cutoff frequencies. With changes in the inductance, not only the cutoff frequency changes, but so does the characteristic impedance.

From Fig. 2.3 it is obvious that with an increasing time constant in the gate, which increases gateline loss, the available gain and the optimum number of devices for maximum gain at 20 GHz both decrease. Furthermore, the optimum number of devices decreases for increasing gate and drainline impedance. This is probably due to increasing loss per section for constant R_g and C_g with increasing L_g .

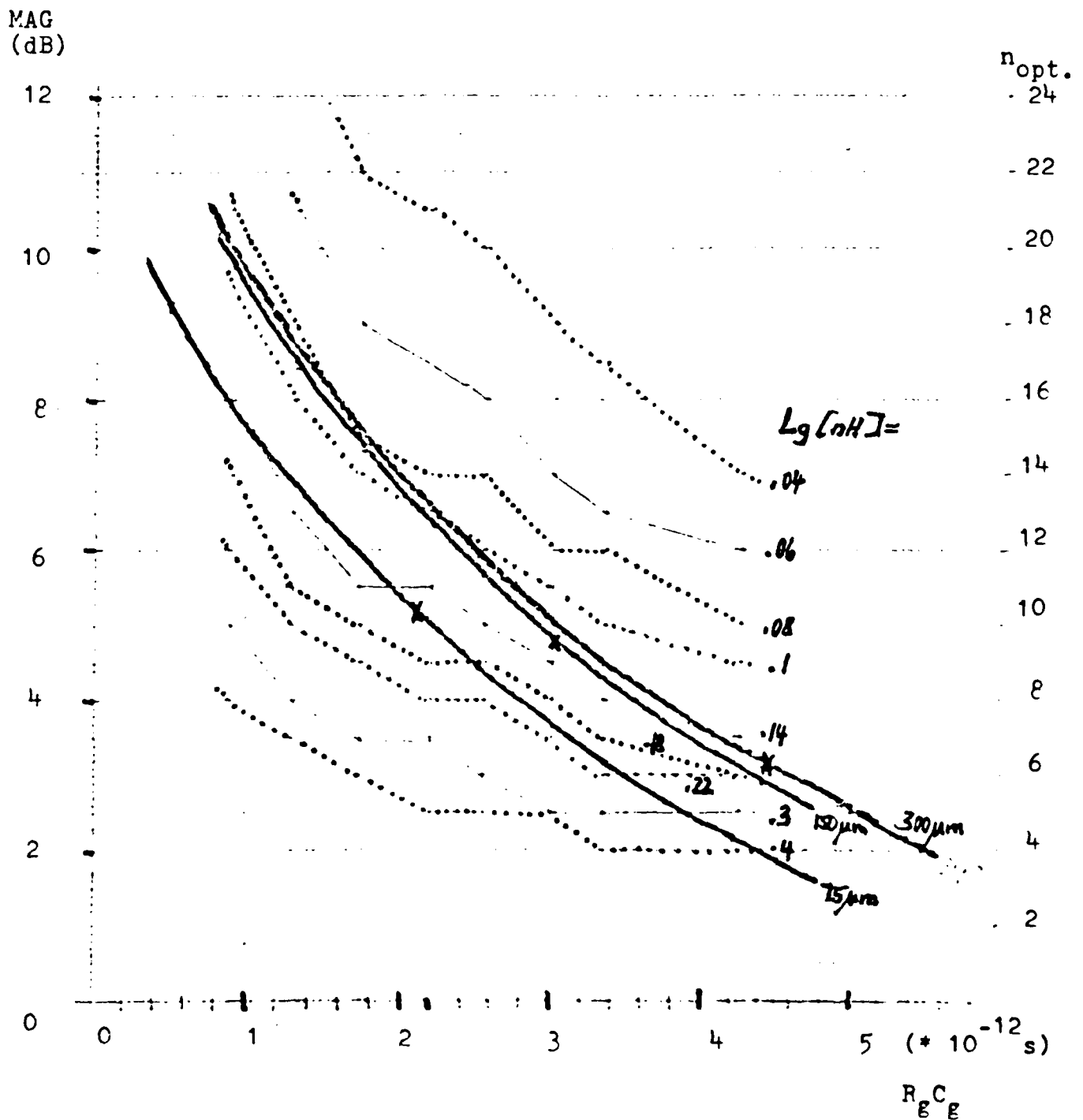


Fig. 2.3. Maximum available gain vs. $R_g C_g$ (bold lines) and optimum number of devices vs. $R_g C_g$ (150 μm devices).

It may be interesting to note that, as long as the optimum number of devices is adjusted accordingly, the available gain of the distributed amplifier is almost entirely independent of gate and drainline impedance and cutoff frequency. This seems to amount to a fundamental limitation, which we are currently studying.

If the number of devices is fixed, however, the available gain does change with L_g . This is apparent from the plots in Fig. 2.4 which represents the response of an amplifier with 4 devices for various gateline inductors L_g . The transistor model used was that of the 300 μm device.

Fig. 2.4 also shows how the bandwidth decreases with increasing gate line impedance. Again this may be simply because of the changing attenuation vs. frequency for the gateline. At this point it could appear most advantageous to use low gateline impedances in order to obtain flat response up to high frequencies. Unfortunately, the available gain then drops due to the low drainline impedance dictated by the requirement for equal cutoff frequency of both lines.

The dependence of the 3 dB bandwidth of a distributed amplifier on the gate time-constant is given in Fig. 2.5. As expected the 3 dB bandwidth decreases with increasing R-C product.

No further emphasis is placed on bandwidth or gain-bandwidth-product at this point; Instead we attempt to define a 'figure of merit' for lossy distributed amplifiers which compares the frequencies of 0 dB power gain of a distributed amplifier and a single transistor stage with complex conjugate matching.

The circuit analysis program determines this figure of merit by evaluating the frequency response up to a frequency where $|S_{21}| = 1$. The corresponding 0 dB frequency for a single stage is computed from Eq. 28.

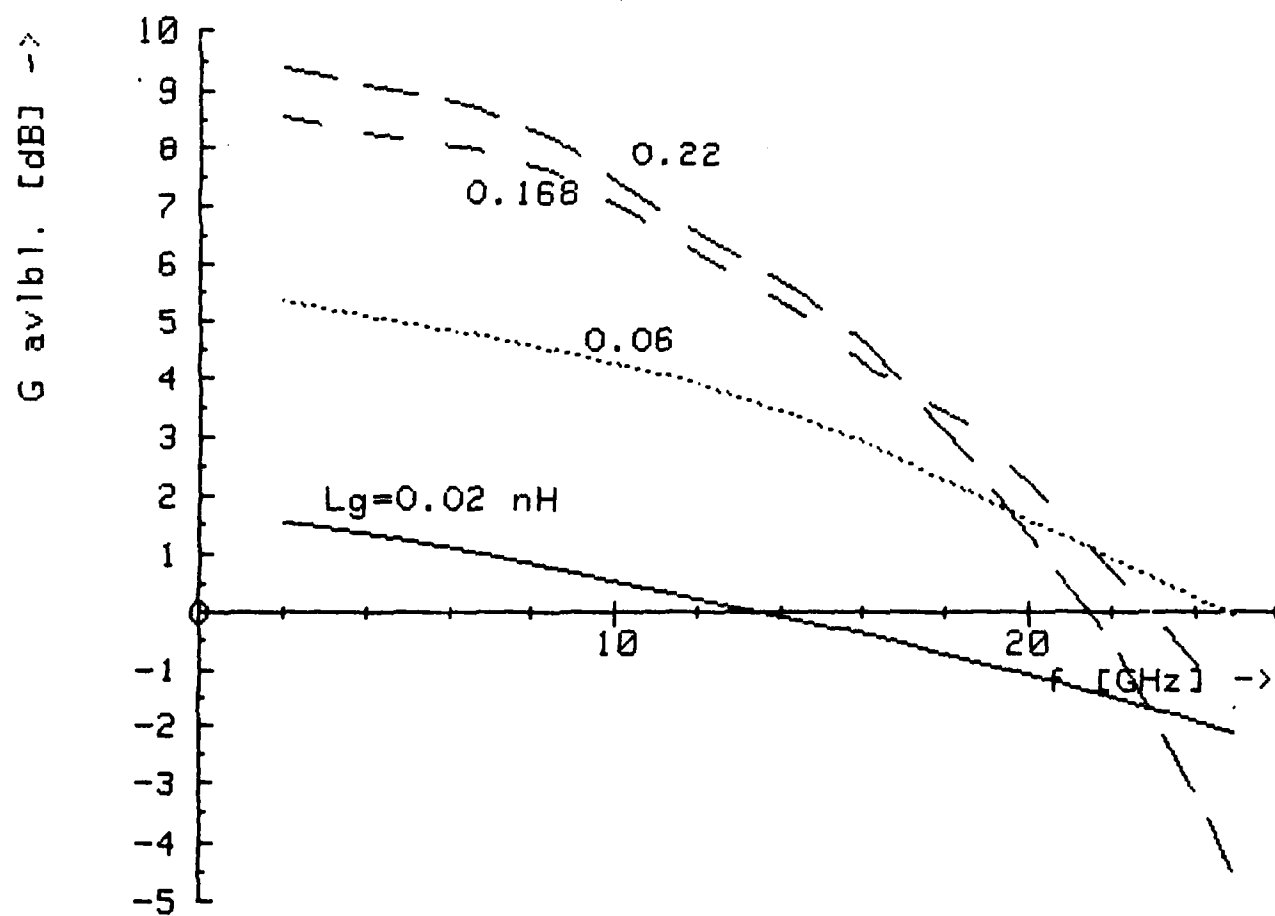


Fig. 2.4. G available [dB] vs. f [GHz].

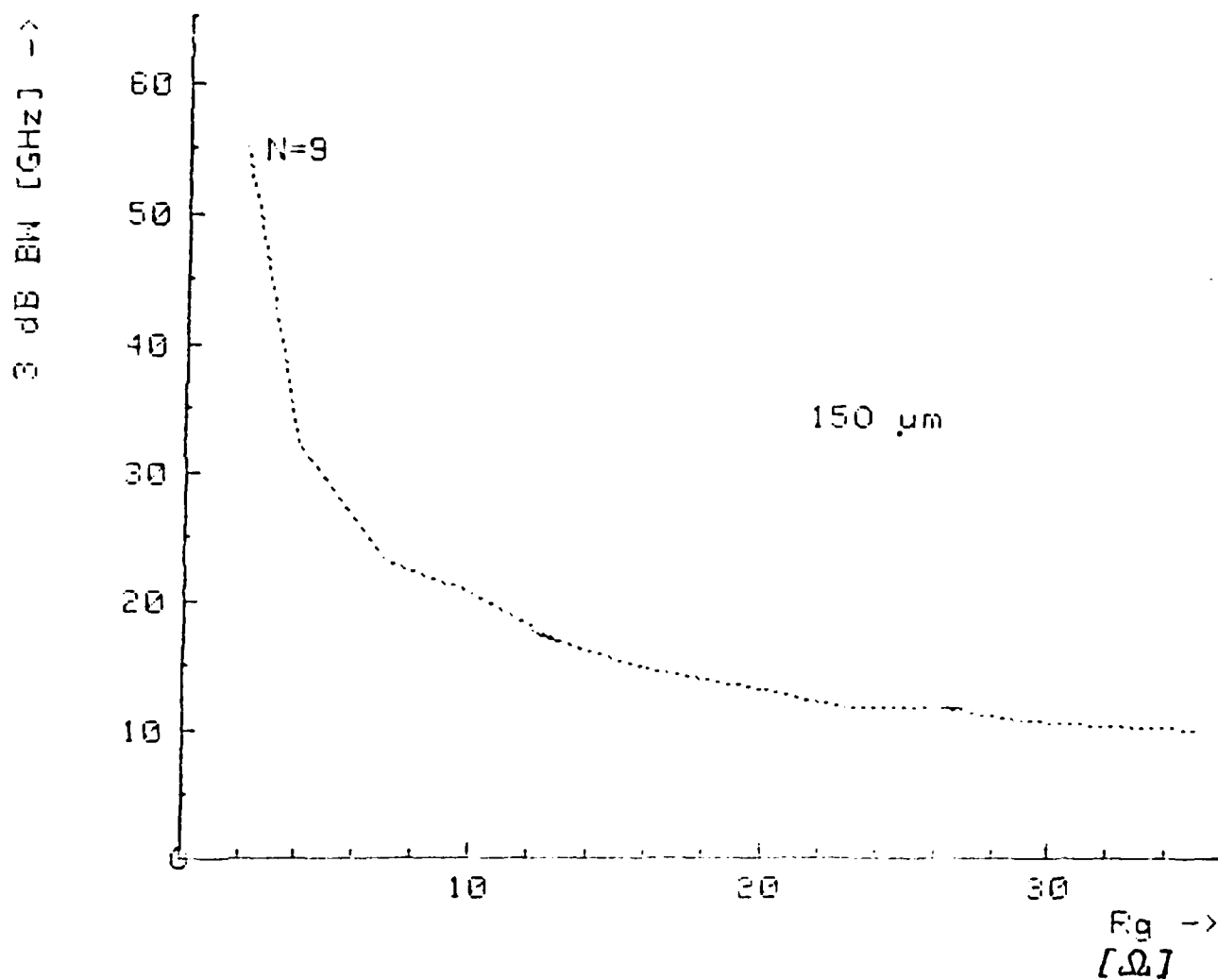


Fig. 2.5. 3 dB BW [GHz] vs. R_g .

The figure of merit is the ratio of the two 0 dB frequencies. Fig. 2.6 contains data on the figure of merit for two amplifiers with $150\text{ }\mu\text{m}$ transistors. One amplifier consists of 5 devices, the other one of 9 devices. Notable is the dropoff of the figure of merit toward lower R-C products. Also note the asymptotic behavior which seems to indicate that the maximum figure of merit achievable is approx. 0.6. Even drastically different values of the transistor parameters did not yield larger figures of merit as yet.

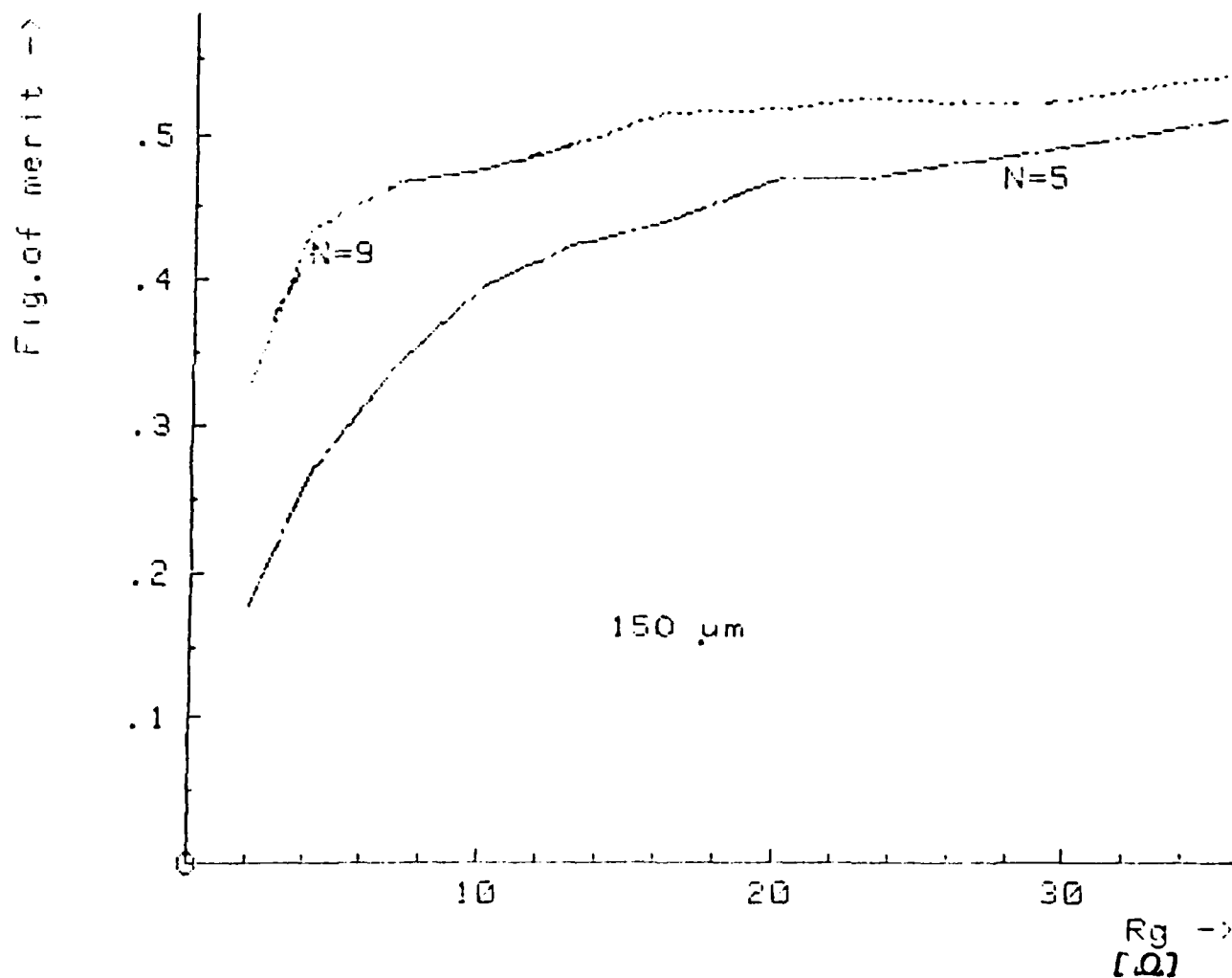


Fig. 2.6. Fig. of merit vs. R_g .

III. Sensitivity

As is evident from the last section, there are many parameters that affect distributed amplifier performance. Due to the limited possibilities for post fabrication modification of monolithic circuitry, it is important to consider the sensitivity of any circuit to its component values. Of equal importance is the ability of a sensitivity analysis to highlight those components or device parameters most directly affecting performance.

Standard analytical techniques may be applied to the gain equation,

$$A = \frac{g_m}{2} \sqrt{|z_{01}| |z_{02}|} \left[\frac{e^{-n\gamma_d} - e^{-n\gamma_g}}{\sinh(\frac{1}{2}(\gamma_g - \gamma_d))} \right] \quad (38)$$

which is an intermediate form of Eq. (2) with γ_g and γ_d defined for the type of synthetic transmission lines in use. Here, we will use constant-k transmission lines, and γ_g and γ_d are the same as previously defined.

For the case of $\beta_g \approx \beta_d$, it can be shown that

$$S_A^{R_g} \approx \alpha_g \left(\frac{n e^{-n\alpha_g}}{e^{-n\alpha_d} - e^{-n\alpha_g}} - \frac{\cosh[1/2(\alpha_g - \alpha_d)]}{2 \sinh[1/2(\alpha_g - \alpha_d)]} \right) \left(1 - \frac{\omega^2/\omega_H^2}{1 + \omega^2/\omega_H^2 - \omega^2/\omega_{cg}^2} \right) - \frac{\omega^2/\omega_H^2}{1 + \omega^2/\omega_H^2} \quad (39)$$

$$S_A^{R_{ds}} \approx \alpha_d \left(\frac{n e^{-n\alpha_d}}{e^{-n\alpha_d} - e^{-n\alpha_g}} - \frac{1}{2} \frac{\cosh[1/2(\alpha_g - \alpha_d)]}{\sinh[1/2(\alpha_g - \alpha_d)]} \right) \quad (40)$$

where $S_A^{R_g}$ and $S_A^{R_d}$ are the sensitivity with respect to R_g and R_d of the amplifier gain, ω_{cg} is the gate line cutoff radian frequency, and $\omega_H = (R_g C_{gs})^{-1}$.

To calculate sensitivities for gate and drain line components, it is necessary to use the complete expression for gain in order to include the effect of phase velocity mismatch between gate and drain transmission lines. The equations

$$S_A^L = \frac{1}{4} + \left(\frac{n e^{-n\gamma_g}}{e^{-n\gamma_d} - e^{-n\gamma_g}} - \frac{\cosh[1/2(\gamma_g - \gamma_d)]}{2 \sinh[1/2(\gamma_g - \gamma_d)]} \right) \left(\alpha_g \left\{ 1 - \frac{1}{2} \left(\frac{1 + \omega^2/\omega_H^2 - 2\omega^2/\omega_{cg}^2}{1 + \omega^2/\omega_H^2 - \omega^2/\omega_{cg}^2} \right) \right\} + j \frac{1}{(1 + \omega^2/\omega_H^2 - \omega^2/\omega_{cg}^2)^{1/2}} \right) \quad (41)$$

$$S_A^C = -\frac{\omega^2/\omega_H^2}{1 + \omega^2/\omega_H^2} - \frac{1}{4} + \left(\frac{n e^{-n\gamma_g}}{e^{-n\gamma_d} - e^{-n\gamma_g}} - \frac{1}{2} \frac{\cosh[1/2(\gamma_g - \gamma_d)]}{\sinh[1/2(\gamma_g - \gamma_d)]} \right) \cdot \left(\alpha_g \left\{ 2 - \frac{1}{2} \left(\frac{1 + 3\omega^2/\omega_H^2 - 2\omega^2/\omega_{cg}^2}{1 + \omega^2/\omega_H^2 - \omega^2/\omega_{cg}^2} \right) \right\} + j \frac{\left[\omega/\omega_{cl} - \frac{2\omega^3/\omega_{cg} \omega_H^2}{1 + \omega^2/\omega_H^2} \right]}{(1 + \omega^2/\omega_H^2 - \omega^2/\omega_{cg}^2)^{1/2}} \right) \quad (42)$$

$$S_A^L = \frac{1}{4} + \left(\frac{1}{2} \frac{\cosh[1/2(\gamma_g - \gamma_d)]}{\sinh[1/2(\gamma_g - \gamma_d)]} - \frac{n e^{-n\gamma_d}}{e^{-n\gamma_d} - e^{-n\gamma_g}} \right) \left(\frac{\alpha_d/2}{1 - \omega^2/\omega_{cd}^2} + j \frac{\omega/\omega_{cd}}{(1 - \omega^2/\omega_{cd}^2)^{1/2}} \right) \quad (43)$$

$$S_A^C = -\frac{1}{4} + \left(\frac{\cosh[1/2(\gamma_g - \gamma_d)]}{2 \sinh[1/2(\gamma_g - \gamma_d)]} - \frac{n e^{-n\gamma_d}}{e^{-n\gamma_d} - e^{-n\gamma_g}} \right) \left(\alpha_d \left(\frac{2\omega^2/\omega_{cd}^2 - 1}{1 - \omega^2/\omega_{cd}^2} \right) + j \frac{\omega/\omega_{cd}}{(1 - \omega^2/\omega_{cd}^2)^{1/2}} \right) \quad (44)$$

where

$S_A^{L_g}$ = sensitivity w.r.t. L_g (gate line inductor)

$S_A^{C_g}$ = sensitivity w.r.t. C_g (MESFET gate capacitance)

$S_A^{L_d}$ = sensitivity w.r.t. L_d (drain line inductor)

$S_A^{C_d}$ = sensitivity w.r.t. C_d (MESFET drain-source capacitance)

ω_{cd} = drainline cutoff radian frequency.

Computer studies of these equations were carried out for a group of amplifiers with gate and drain line impedances in the vicinity of 20 Ω and 100 Ω , respectively. The results are tabulated in Table 3.1 for a 300 μm device and in Table 3.2 for a 150 μm device. For example, for a 6 device amplifier these studies indicate that the sensitivity of the amplifiers to R_g ranged from a low of -0.01 at 2 GHz to -0.87 at 20 GHz for a 150 μm device. This is indicative of the significant effect of R_g on high frequency performance. This may be contrasted to the sensitivity to R_d for the same amplifier which ranged from 0.19 at 2 GHz to only 0.23 at 20 GHz. Clearly R_d is not as significant as R_g to high frequency performance.

Further studies of Eqs. (41) thru (44) indicate that, for the same group of amplifiers, overall sensitivity to L_g ranged from 0.1 to 0.3. For small amplifiers (2 to 4 transistors), $S_A^{L_g}$ decreased in magnitude with frequency. For larger amplifiers, $S_A^{L_g}$ dips and then begins to increase with frequency, indicating that the phase mismatch error becomes more significant in long amplifiers. This is not unexpected, as the phase velocity is a much stronger function of L_g than is the attenuation.

Sensitivity to C_g typically ranged from -0.25 to -1.5, decreasing monotonically with increasing frequency. This indicates that the size of C_g has a significant effect on high frequency gain. Sensitivity to C_d ranged from +0.1 to -0.5 for the group. The change in sign is again due to the small change in α_d with C_d

Distributed amplifier sensitivity analysis

Rg(ohms)	Rd(ohms)	Cg(pF)	Cd(pF)	Lg(nH)	Ld(nH)	N	
11	380	.440	.091	.168	.910	4	
f(GHz)	Sens(Rg)	Sens(Rd)	Sens(L2)	Sens(C2)	Sens(L1)	Sens(C1)	
2.000	-.014	.243	.128	-.009	.252	-.264	
4.000	-.058	.245	.124	-.009	.248	-.305	
6.000	-.128	.250	.118	-.012	.239	-.372	
8.000	-.224	.256	.107	-.016	.226	-.460	
10.000	-.344	.265	.092	-.023	.209	-.567	
12.000	-.484	.276	.069	-.036	.189	-.686	
14.000	-.641	.290	.038	-.057	.167	-.814	
16.000	-.813	.307	-.006	-.090	.143	-.946	
18.000	-.995	.327	-.065	-.138	.119	-1.076	
20.000	-1.185	.352	-.147	-.210	.095	-1.200	
22.000	-1.379	.383	-.260	-.317	.073	-1.314	
24.000	-1.576	.421	-.419	-.481	.057	-1.412	*
26.000	-1.775	.471	-.655	-.744	.053	-1.490	*
28.000	-1.975	.539	-1.036	-1.214	.072	-1.536	*
30.000	-2.180	.641	-1.762	-2.222	.140	-1.532	*

Rg(ohms)	Rd(ohms)	Cg(pF)	Cd(pF)	Lg(nH)	Ld(nH)	N	
11	380	.440	.091	.168	.910	6	
f(GHz)	Sens(Rg)	Sens(Rd)	Sens(L2)	Sens(C2)	Sens(L1)	Sens(C1)	
2.000	-.018	.346	.075	.095	.257	-.270	
4.000	-.073	.352	.069	.094	.256	-.327	
6.000	-.163	.360	.056	.091	.249	-.419	
8.000	-.284	.373	.036	.084	.238	-.539	
10.000	-.433	.390	.006	.071	.226	-.681	
12.000	-.605	.411	-.039	.046	.215	-.835	
14.000	-.795	.437	-.103	.006	.207	-.995	
16.000	-.998	.469	-.191	-.057	.204	-1.150	
18.000	-1.208	.507	-.313	-.152	.209	-1.293	
20.000	-1.421	.553	-.479	-.290	.225	-1.414	
22.000	-1.631	.609	-.705	-.492	.258	-1.502	
24.000	-1.836	.678	-1.017	-.789	.315	-1.540	*
26.000	-2.037	.765	-1.460	-1.251	.407	-1.507	*
28.000	-2.236	.883	-2.135	-2.049	.544	-1.370	*
30.000	-2.443	1.055	-3.343	-3.751	.711	-1.101	*

* Indicates approximations used in the calculations have exceeded their error boundaries, and the values are therefore suspect.

Table 3.1
300 μ m Gate Width

Rg(ohms)	Rd(ohms)	Cg(pF)	Cd(pF)	Lg(nH)	Ld(nH)	N	
20	700	.221	.046	.088	.426	4	
f(GHz)	Sens(Rg)	Sens(Rd)	Sens(L2)	Sens(C2)	Sens(L1)	Sens(C1)	
2.000	-.009	.132	.184	-.118	.248	-.258	
4.000	-.037	.133	.183	-.117	.244	-.281	
6.000	-.082	.134	.182	-.117	.238	-.318	
8.000	-.144	.135	.181	-.117	.229	-.369	
10.000	-.220	.137	.179	-.117	.220	-.430	
12.000	-.309	.139	.176	-.118	.209	-.499	
14.000	-.408	.141	.172	-.119	.198	-.574	
16.000	-.516	.144	.167	-.121	.187	-.654	
18.000	-.631	.147	.160	-.125	.176	-.735	
20.000	-.750	.150	.151	-.130	.165	-.816	
22.000	-.871	.153	.140	-.138	.155	-.896	
24.000	-.993	.157	.127	-.147	.145	-.974	
26.000	-1.115	.162	.111	-.159	.135	-1.048	
28.000	-1.235	.166	.091	-.173	.127	-1.118	
30.000	-1.353	.171	.069	-.191	.119	-1.184	

Rg(ohms)	Rd(ohms)	Cg(pF)	Cd(pF)	Lg(nH)	Ld(nH)	N	
20	700	.221	.046	.088	.426	6	
f(GHz)	Sens(Rg)	Sens(Rd)	Sens(L2)	Sens(C2)	Sens(L1)	Sens(C1)	
2.000	-.011	.194	.153	-.056	.248	-.260	
4.000	-.044	.195	.152	-.056	.242	-.291	
6.000	-.097	.197	.151	-.055	.233	-.340	
8.000	-.170	.199	.148	-.054	.222	-.406	
10.000	-.259	.203	.144	-.054	.211	-.485	
12.000	-.363	.207	.138	-.055	.201	-.573	
14.000	-.480	.212	.129	-.057	.191	-.668	
16.000	-.605	.217	.118	-.062	.183	-.767	
18.000	-.737	.223	.103	-.070	.178	-.866	
20.000	-.873	.230	.084	-.081	.174	-.963	
22.000	-1.010	.237	.060	-.096	.174	-1.056	
24.000	-1.147	.245	.032	-.115	.175	-1.144	
26.000	-1.283	.253	-.003	-.140	.180	-1.225	
28.000	-1.414	.262	-.044	-.170	.187	-1.300	
30.000	-1.541	.272	-.091	-.206	.196	-1.367	

Rg(ohms)	Rd(ohms)	Cg(pF)	Cd(pF)	Lg(nH)	Ld(nH)	N	
20	700	.221	.046	.088	.426	8	
f(GHz)	Sens(Rg)	Sens(Rd)	Sens(L2)	Sens(C2)	Sens(L1)	Sens(C1)	
2.000	-.013	.252	.124	.002	.247	-.263	
4.000	-.051	.254	.122	.003	.239	-.301	
6.000	.113	.257	.120	.005	.228	-.363	
8.000	-.196	.262	.115	.006	.217	-.444	
10.000	-.299	.267	.109	.007	.207	-.540	
12.000	-.419	.274	.099	.006	.199	-.648	
14.000	-.551	.282	.084	.002	.195	-.761	
16.000	-.692	.291	.065	-.006	.197	-.876	
18.000	-.840	.301	.039	-.019	.203	-.989	
20.000	-.990	.313	.006	-.037	.216	-1.097	
22.000	-1.140	.325	-.034	-.062	.234	-1.197	
24.000	-1.287	.338	-.084	-.095	.257	-1.288	
26.000	-1.430	.352	-.142	-.135	.284	-1.369	
28.000	-1.567	.366	-.209	-.183	.315	-1.438	
30.000	-1.697	.382	-.285	-.238	.350	-1.493	

Table 3.2

150 μ m Gate Width

being overshadowed by the effect of C_d on the phase velocity matching on the drain line and the gate line. A positive sign indicates improving phase velocity match; a negative sign indicates decreasing phase velocity matching. For L_d , sensitivity ranged from 0.16 to -0.48, and decreased monotonically with increasing frequency. Regarding sign changes, $S_A^{L_d}$ displays the same characteristics as C_d .

By far, the largest sensitivities occur in the gate $R_g C_g$ network. The large negative values of $S_A^{R_g}$ and $S_A^{C_g}$ suggest that these two parameters are suitable candidates for device design improvements. The strongly negative values of $S_A^{C_g}$ are the result of increasing the MESFET input time constant with increasing C_g . This results in rapidly rising attenuation on the gate line. The same is true for increasing R_g . The significance of the $R_g C_g$ product has already appeared in earlier sections and will be further explored in the remainder of this report.

IV. Computer Aided Design

4.1 A Program for Distributed AMPlifier OPTimization (DAMPOP)

Using the HP circuit analysis program "OPNODE/1000 REV 3.0 3/26/82" a routine has been developed which is capable of analyzing and optimizing distributed amplifiers as well as cascaded configurations. The circuit is built up by repeated looping through the description of a single cell while changing node numbers in the cell accordingly. The maximum number of devices in a given amplifier topology depends on the circuit's complexity, i.e. the number of nodes per section.

For transistor equivalent circuits used by us this number is 25. This is sufficient since gate line loss and common sense limits the number of cells per amplifier to approximately a dozen.

The program is capable of the following:

- 1) Determination of S-parameters for distributed and cascaded amplifiers.
Matching and bias networks can be included.
- 2) Optimization of the number of cells, N , with intent to maximize the gain at some predetermined frequency.
- 3) Optimization of the number of cells for maximum 3 dB-bandwidth of the amplifier.
- 4) Optimization of the number of cells for maximum gain-bandwidth-product.
- 5) Optimization of the number of cells with respect to a function defined by the user.
- 6) Optimization of the number of cells to achieve maximum "figure of merit" as defined by the 0-dB-gain-frequency of the distributed amplifier divided by the same frequency for a single tuned stage, $(f_{0 \text{ dB distr. amp.}})/(f_{\text{max. single device}})$.
- 7) Determination of maximum gain, 3 dB bandwidth, gain-bandwidth-product, 0 dB frequency and figure of merit of a given amplifier.
- 8) Determination of the maximum available gain by correction of S_{21} for reflections occurring at the in- and output.

Figures 4.1 and 4.2 show the equivalent circuits of individual cells as used for various amplifier topologies. Data resulting from the use of this program on the HP-1000 computer system has already appeared in earlier sections of this report. Further studies using this program will be presented here followed by some conclusions resulting from their application.

4.2 The Effect of Mismatched Gate- and Drainline Terminations on Performance

Smooth gain vs. frequency responses in distributed amplifiers are achieved by terminating gate- and drain lines by their respective characteristic impedances. By allowing for some ripple, however, it may be possible to increase the high-end gain of a distributed amplifier. This will be illustrated by the results of computer simulations for a distributed amplifier comprised of 4 TI 300 μm gate-width transistors. Fig. 4.3 shows the equivalent circuit for the complete amplifier; bias networks and decoupling capacitors are not included in the calculations.

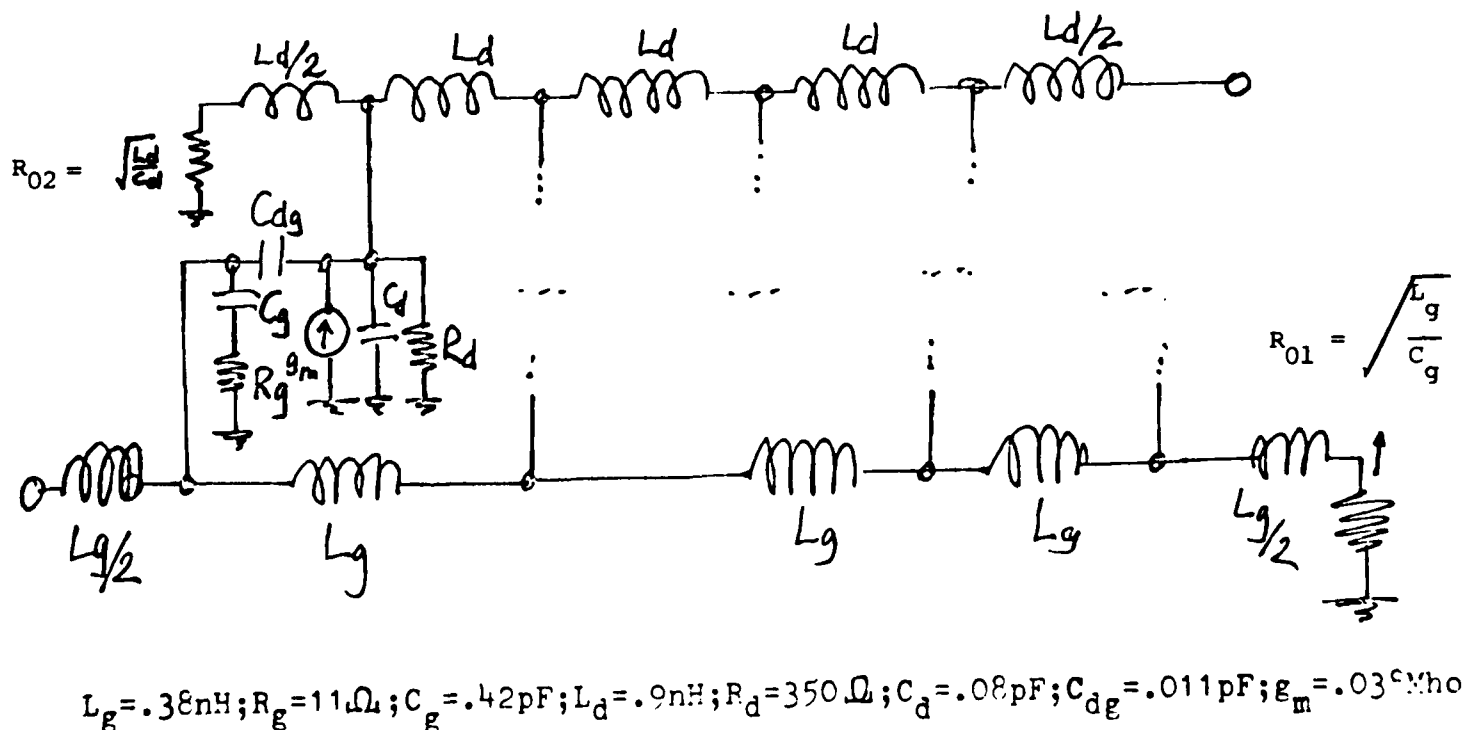


Figure 4.3

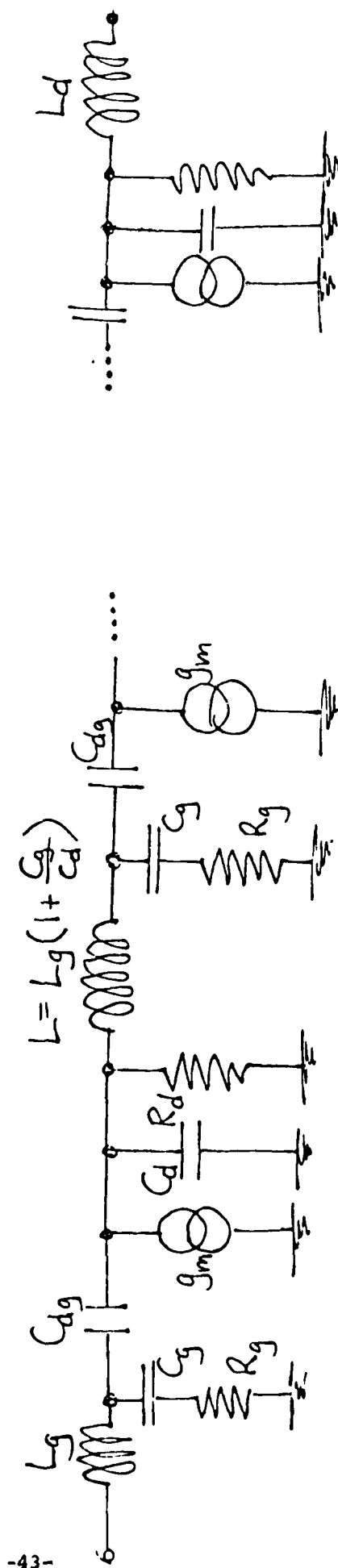
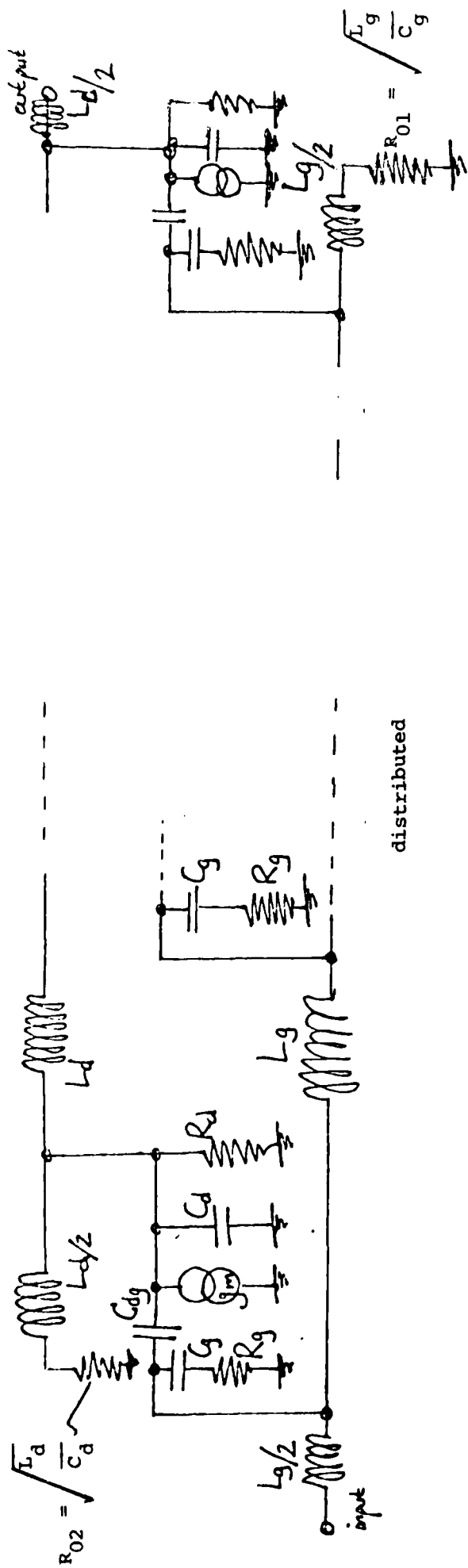
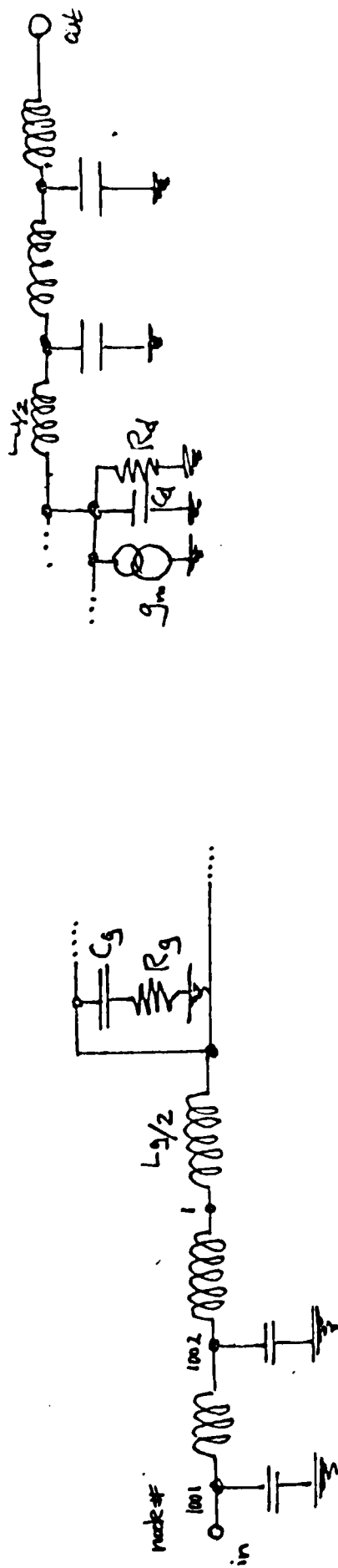


Fig. 4.1.



distributed, matched

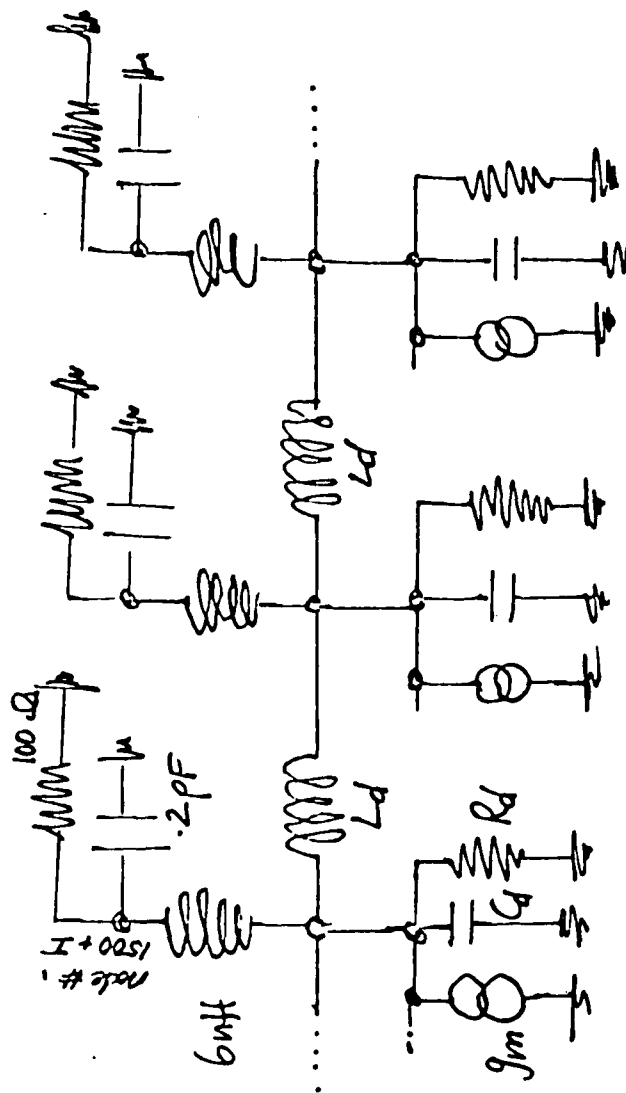


Fig. 4.2. Distributed, Matched, Biased

For the given element values the characteristic impedance of the gateline is $Z_g = 30 \Omega$ and of the drainline is $Z_d = 100 \Omega$. By definition the gain will be $|S_{21}|$.

Terminating the gate- and drainline into their appropriate impedances results in a maximum gain of 9 dB at 2 GHz and 1.2 dB at 20 GHz. The gain for source and load impedances of 50Ω is 8.6 dB at 2 GHz and -0.06 dB at 20 GHz. Figs. 4.4 - 4.6 show S_{21} , S_{11} and S_{22} for the latter case, respectively.

If now the gateline termination is changed while the drainline termination Z_d remains unaltered the gain of the amplifier at 20 GHz into 50Ω will change as plotted in Fig. 4.7. Decreasing the impedance Z_g causes the 20 GHz gain to increase. Fig. 4.8 then indicates that for a gateline termination of $Z_g = \text{const.} = 0.1 \Omega$ (for all practical purposes 0) a further gain increase can be achieved by increasing the value of Z_d . Maximum gain is reached for $Z_d \rightarrow \infty$.

The only other elements left at our disposition without seriously affecting the construction of the individual cells are the half-sections of gate- and drainline at the in- and output of the amplifier. Table 4.1 contains the results of a change of $L_g/2$ at the end of the gateline, i.e. at its "termination":

$L_g/2$ (nH)	$S_{21} _{20 \text{ GHz}}$ [dB]	
.05	1.3	$Z_g = 0$
.1	1.4	$Z_d \rightarrow \infty$
.15	1.4	
.19	1.4	
.3	1.3	

Table 4.1

f1 marker freq up
 f2 change scale
 f3 plot hardcopy
 f4 exit plot
 f5 marker freq down

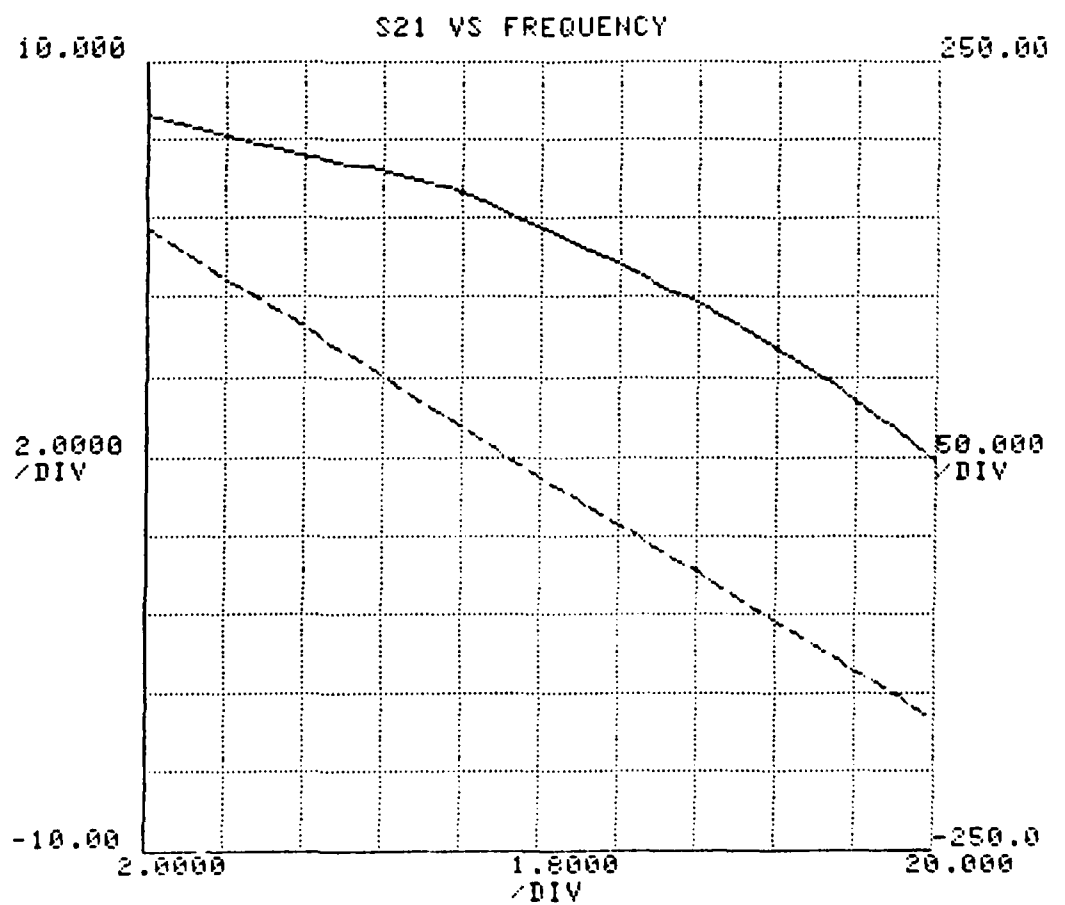


Figure 4.4

f1 marker freq up
 f2 change scale
 f3 plot hardcopy
 f4 exit plot
 f5 marker freq down

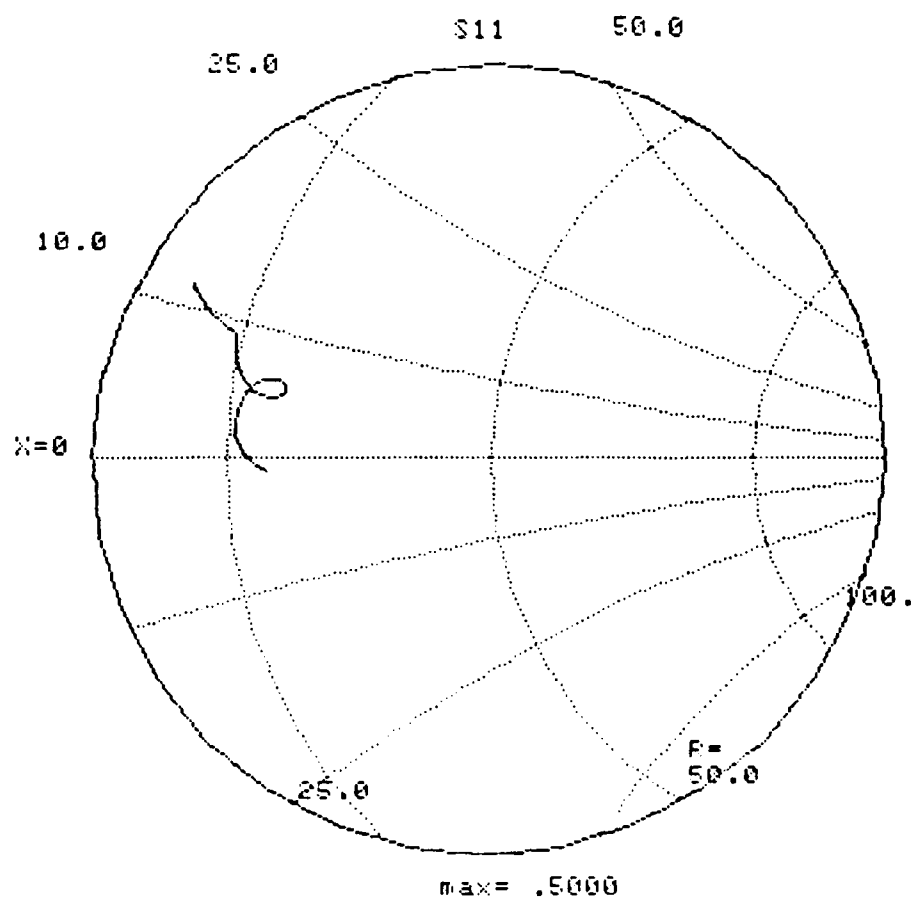


Figure 4.5

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 f2 change scale
 f3 plot hardcopy
 f4 exit plot
 f5 marker freq down

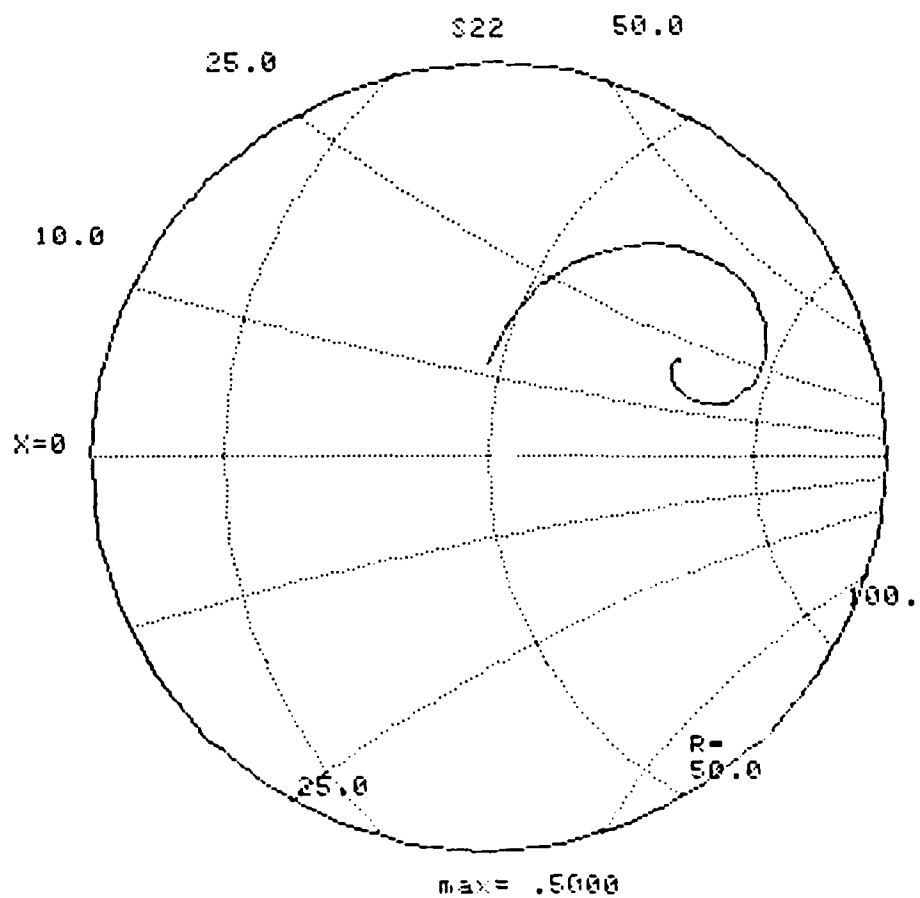


Figure 4.6

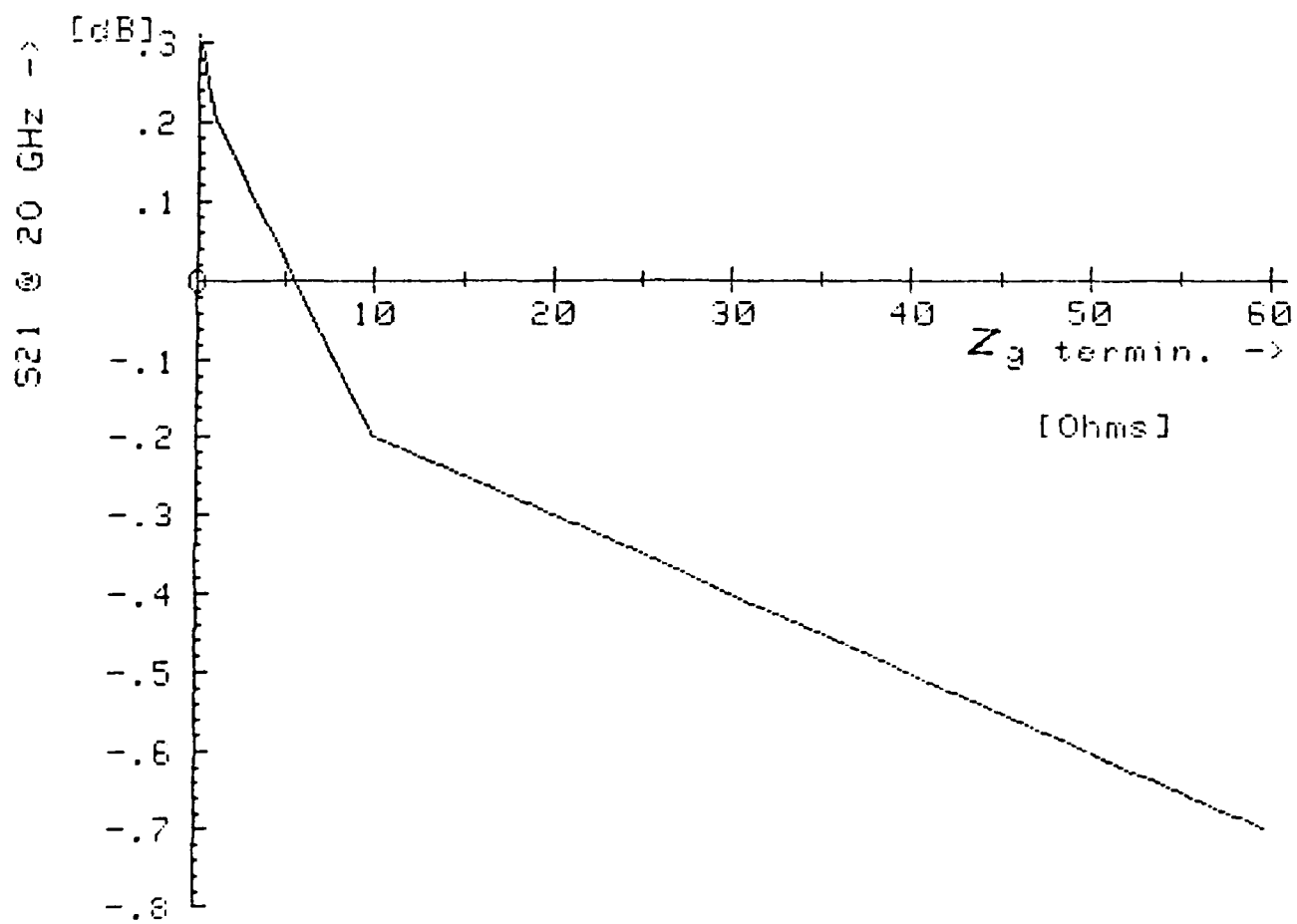


Figure 4.7

521 @ 20 GHz [dB] →

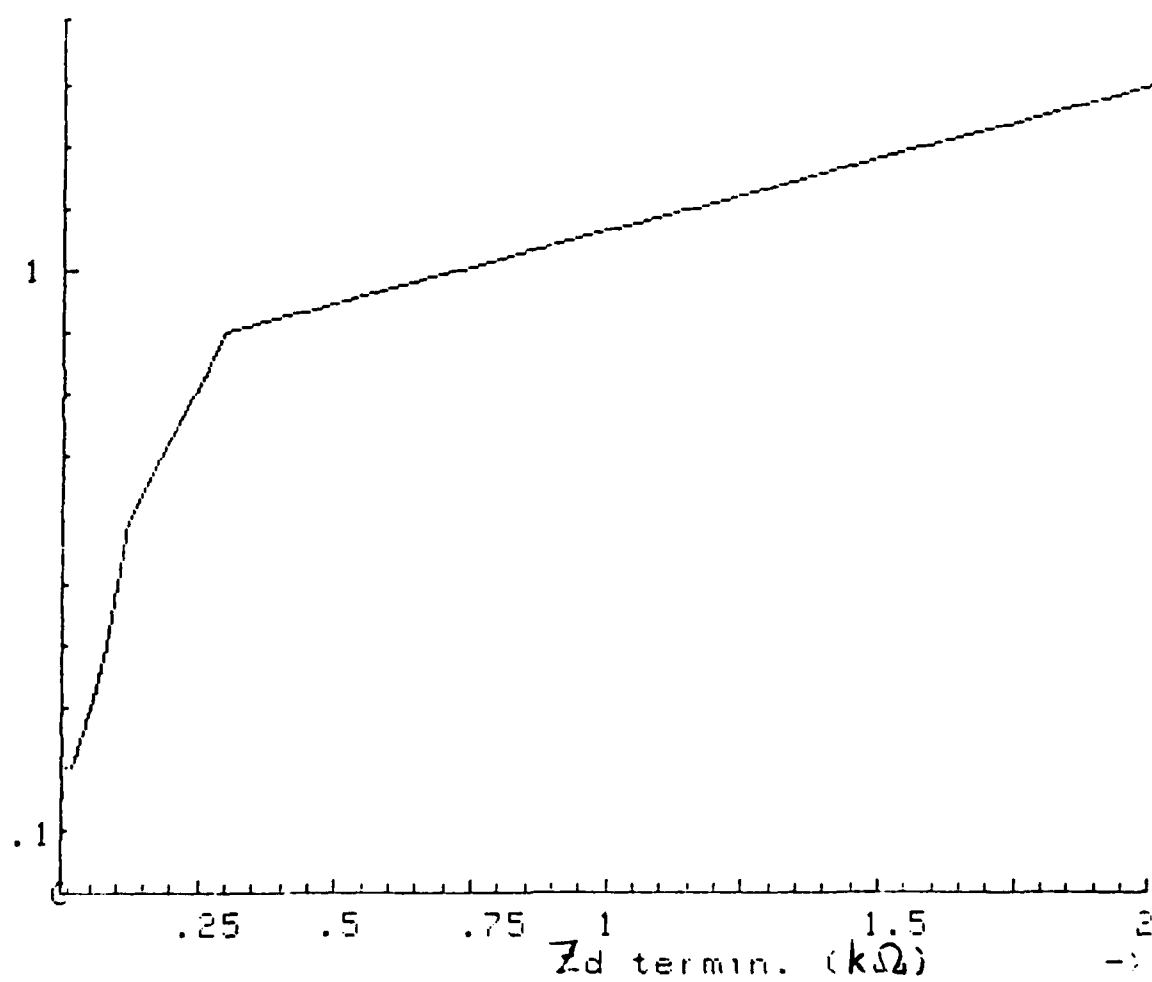


Figure 4.8

Choosing the optimum value above and varying the inductor at the input to the gate line results in gain changes according to Table 4.2:

$L_g/2$ [nH]	$S_{21} _{20 \text{ GHz}}$ [dB]	$L_g/2$ at termination
.01	1.5	= 0.15 nH
.07	1.6	$Z_g = 0$
.1	1.6	$Z_d \rightarrow \infty$
.19	1.4	

Table 4.2

Finally, the last step is to optimize the output section $L_d/2$. In doing so the gain can be further increased as shown in Table 4.3:

$L_d/2$ [nH]	$S_{21} _{20 \text{ GHz}}$ [dB]	$L_g/2$ input = 0.1 nH
.1	1.7	$L_g/2$ termin. = 0.15 nH
.2	1.8	$Z_g = 0$
.25	1.8	$Z_d \rightarrow \infty$
.3	1.8	
.45	1.6	

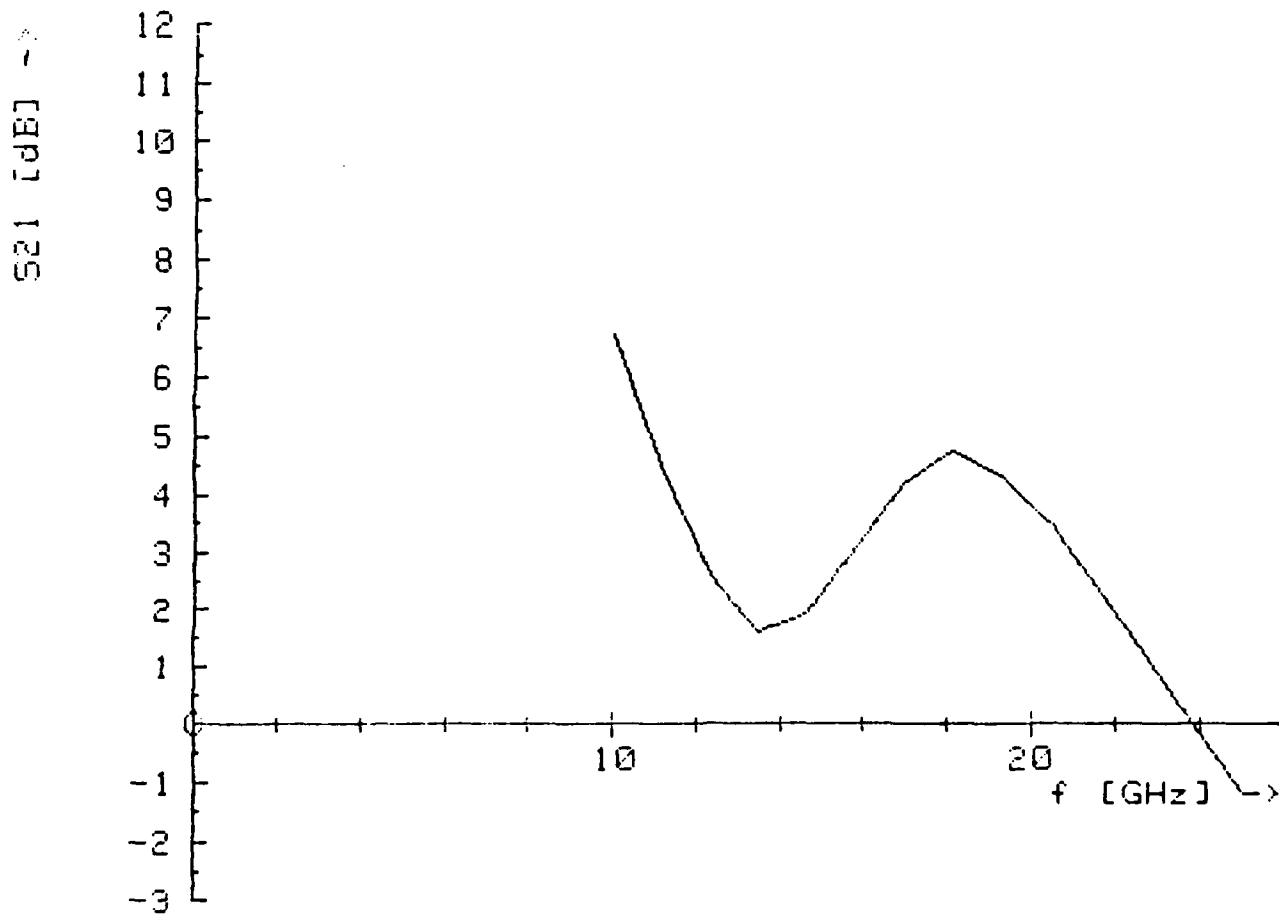
Table 4.3

The gain vs. frequency response of this amplifier ($L_d/2 = 0.25$ nH) is given in Fig. 4.9. It should be noted that the increase in gain toward lower frequencies could easily be compensated by appropriate in- and output matching networks. The overall improvement in gain at 20 GHz is ≈ 2.8 dB. The gain variations amount to 3 dB from 11 to 22 GHz which can be considered tolerable in light of the gain improvement at the high end of the frequency range.

Variation of the individual inductances in gate- and drainline can provide even higher gain yet, however the concept of a distributed amplifier utilizing uniform transmission lines begins to lose validity.

It can be concluded that the gain of the distributed amplifier under consideration can be improved at high frequencies by manipulating gate- and drainline terminations and line sections. Gain flatness will worsen, however. Compensation for increased low frequency gain will be necessary.

The active device available to us with its S-parameters yields a gain of 1.2 dB at 20 GHz when used in the unmodified distributed amplifier configuration. The gain figure increases according to our simulations to about 4 dB at 20 GHz into 50Ω if gate and drainline terminations are replaced by a short and an open, respectively, with inductor values at in- and output adjusted appropriately.



S_{21} [dB] vs. f [GHz]

Figure 4.9

4.3 Studies on Distributed Amplifiers Using Different Gatewidth Devices and Concluding Remarks

Studies were carried out in order to examine the effect of line impedance on available gain and also the frequency response of amplifiers using different gate width devices.

The effect of varying the gate and drainline impedances on the available gain at the highest frequency of interest (20 GHz) is depicted in Fig. 4.10 for a 150 μm gate width device. It is evident that when drain line impedance is high (in comparison to 50 Ω) the effect of changes in gate and drainline impedances on available gain is small. Further, the figure indicates that for high gain, a low gate line impedance and a high drain line impedance is necessary. The lower the gate line impedance the higher the cutoff frequency of the lines. The amplifier was designed on the basis of equal cutoff frequencies for the gate and drain lines.

Table 4.4 gives the optimum number of devices for different gate and drain line impedances. It may be noted that the optimum number of devices decreases with increase in impedance. This can be expected because with an increase in line impedance the attenuation would go up, thereby allowing fewer devices for maximum gain at a given frequency.

Table 4.4

$R_{01} \backslash R_{02}$	20 Ω	30 Ω	40 Ω	50 Ω
50	12	9	7	5
60	10	8	6	5
70	10	7	5	4
80	9	7	5	4
90	9	6	5	4
100	9	6	5	4

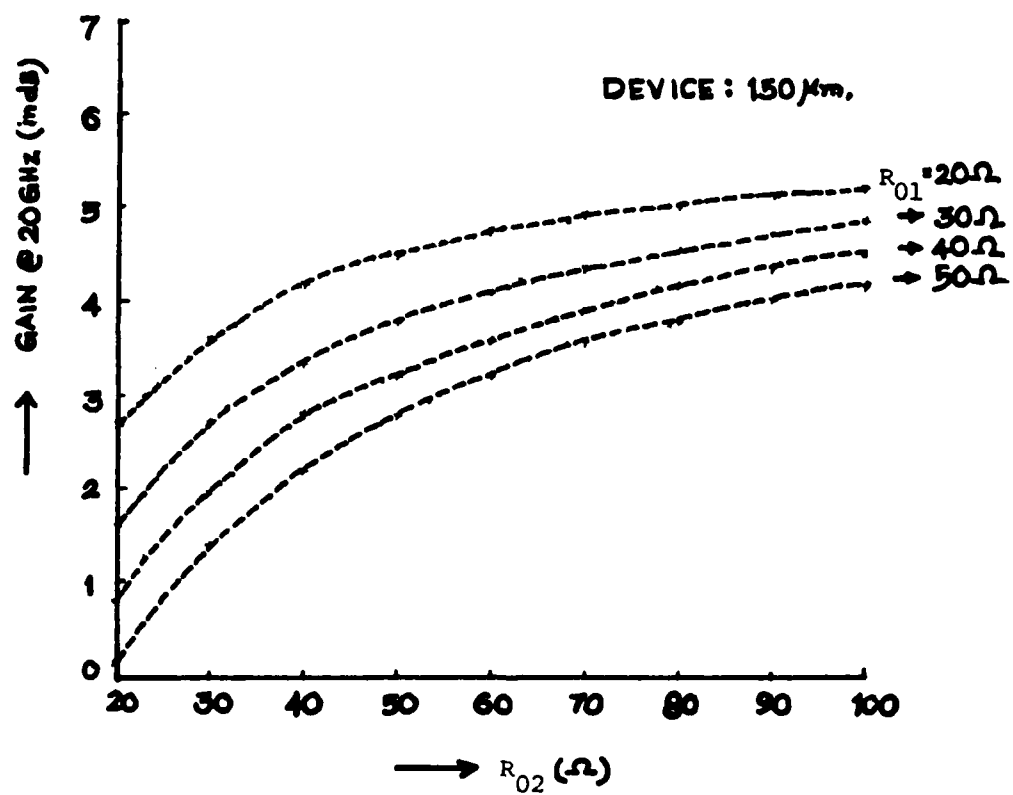


Fig. 4.10. Gain vs. R_{02} for optimum number of devices with R_{01} as a parameter.

Numerical experiments were conducted in order to compare the frequency response of distributed amplifiers using devices with different gate widths. In order to make this comparative study the gate and drain line impedances were kept unchanged. Three devices with gate widths 300 μm , 150 μm and 75 μm were considered for the study. Due to the nonavailability of exact data on 75 μm device its parameters were obtained by scaling the TI 300 μm gate width device. Therefore the performance curves presented here should not be considered as exact. However they are helpful in judging the general trend.

The device parameters used in the study are given in Table 4.5.

Table 4.5

Gate width (μm)	<u>300</u>	<u>150</u>	<u>75</u>
g_m (mS)	38	27	20
C_g (pF)	0.42	0.2205	0.116
R_g (Ω)	11.1	20	36
R_d (Ω)	350	700	1400
C_d (pF)	0.08	0.04	0.02
C_{dg} (pF)	0.011	0.007	0.0045

Fig. 4.11 shows the frequency response for optimum number of devices. It can be seen that there is an increase in gain at 20 GHz as the device size is reduced. The optimum number of devices increases. This is due to the decrease in line attenuation. Gate line attenuation is a function of ω_H and ω_C . Even though the increase in ω_H is small the increase in ω_C is considerable enough to reduce attenuation with the reduction in device size. Also, the drain line attenuation reduces due to the increase in R_d with device size reduction.

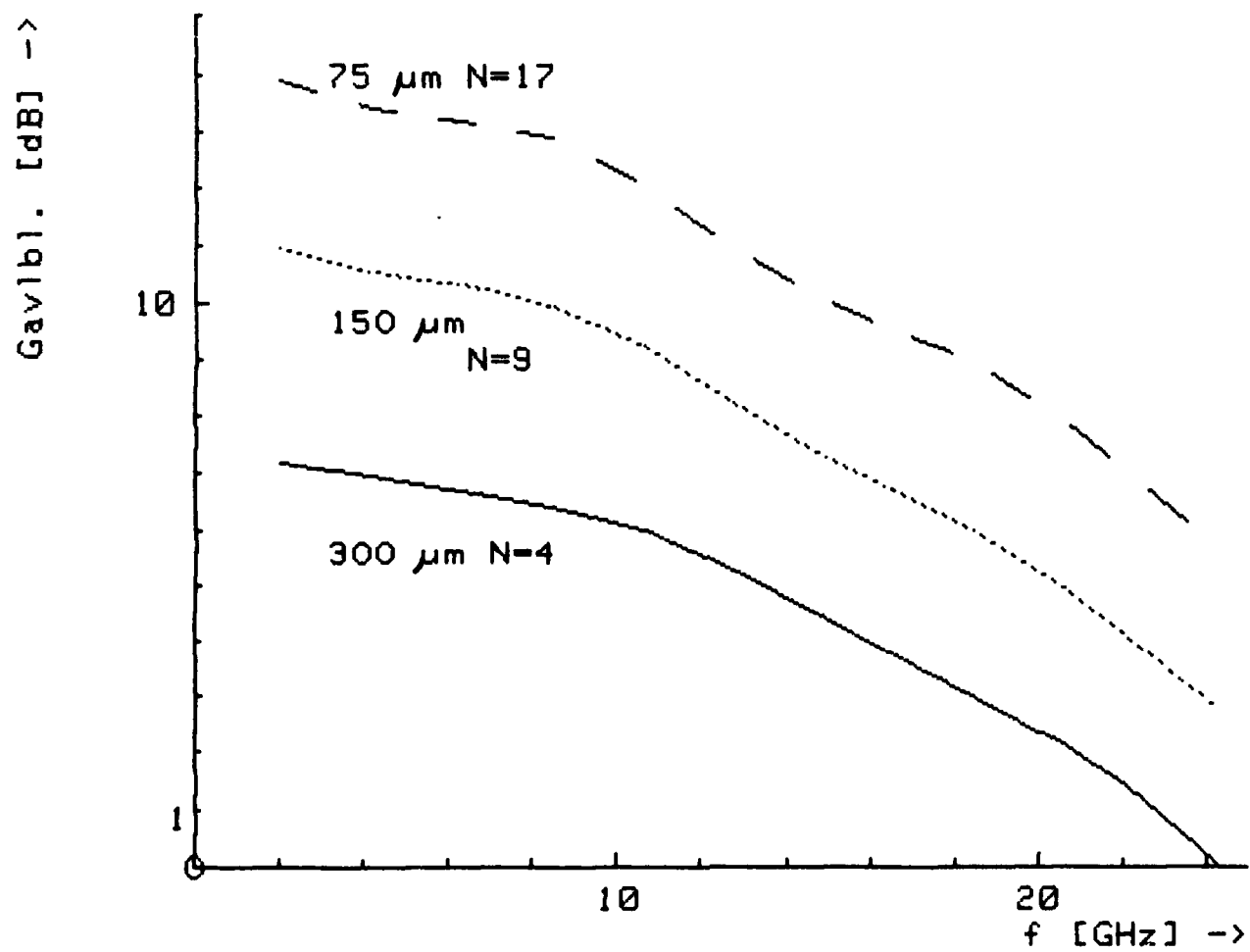


Fig. 4.11. Frequency response of distributed amplifiers using different gate width devices.

Thus, even though g_m decreases with the reduction in device gate width the gain increases due to the reduction in line attenuation.

Also, it may be observed that the g_m to C_g ratio which is the gain bandwidth product of the device increases with reduced gate width (according to data supplied to us by TI). Therefore it may be expected that the available gain from a distributed amplifier would increase with decrease in device size.

However, since lumped inductors are used to build gate and drain lines, the size of the device cannot be reduced indefinitely because of practical difficulties in realizing appropriate inductors. The above arguments will be examined in-depth after we receive the exact device data from TI. However, at present, it can be concluded that a device having gate width less than 300 μm is required to obtain higher gain from a distributed amplifier at 20 GHz.

V. DESIGN OF A PROTOTYPE AMPLIFIER

The design and layout of a distributed amplifier is presented in this section.

5.1 Choice of the Device:

As indicated in the previous section, the TI 150 μm gate width device gives higher gain at 20 GHz than TI 300 μm gate width device. Hence the 150 μm device has been used here for the design. The parameters of the device are given below.

g_m :	27 mS
R_g :	20 Ω
C_g :	.2205 pF
R_d :	700 Ω
C_d :	0.04 pF
C_{dg} :	0.007 pF

The above 150 μm device can be fabricated by TI while the 75 μm device of previous section is scaled and does not represent an actual device.

5.2 Number of Devices and Line Impedances:

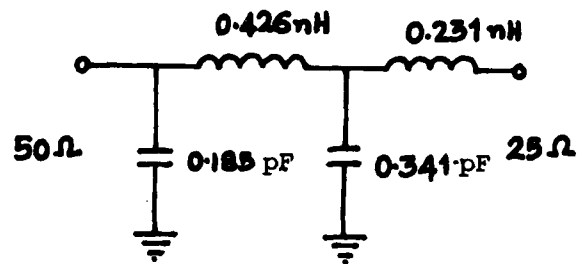
The gain at the highest frequency of interest and the optimum number of devices vary with the choice of line impedances as discussed in the previous section.

As seen in Section 4, low gate line impedance (with respect to $50\ \Omega$) and high drain line impedance (with respect to $50\ \Omega$) results in higher gain. A low gate line impedance implies a low value of gate line inductor and high drain line impedance implies a high value of drain line lumped inductor. These inductors can be realized as short lengths of microstrip lines. The dimensions of gate line inductor in comparison to device geometry and the maximum allowable length of drain line inductor at the highest frequency of operation place limits on the choice of inductors and hence the line impedances. In the present design, a gate line impedance of 25 ohms and a drain line impedance of 75 ohms have been chosen. The number of devices chosen is 8 which gives maximum gain at 20 GHz.

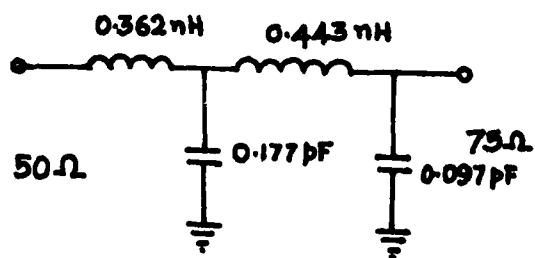
5.3 Design of Input and Output Matching Networks:

When the gate line and drain line impedances are different from the standard measurement system impedance of $50\ \Omega$, impedance transformers on the input and output ports of the amplifier are necessary. Also, they are desirable for cascading amplifier stages. A simple design of these transformers is possible by the use of the Chebyshev impedance-transforming networks of low-pass filter form.¹ These networks can be designed for a given bandwidth and a specified passband ripple. The lumped elements (inductors and capacitors) could be realized in microstrip form. The input and output transformers designed are shown in Fig. 5.2(a) and Fig. 5.2(b). The pass band ripple is 0.053 dB and 0.018 dB respectively, in a bandwidth of 12 GHz (9 - 21 GHz).

¹G. L. Matthaei, "Tables of Chebyshev Impedance - Transforming Networks of Low Pass Filter Forms," Proc. IEEE, pp. 939-963, Aug. 1964.



(a) Input transformer



(b) Output transformer

Figure 5.2

5.4 Biasing Network

The drain and gate biasing networks are standard low pass filters. The design incorporates a resistor as shown in Fig. 5.3 to dissipate the power at frequencies below the cutoff frequency of the filter.

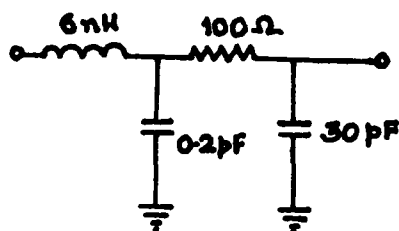


Fig. 5.3. Biasing network

5.5 Design of Lumped Elements

The gate and drain line inductors as well as the elements of the impedance transformers can be realized as lumped elements in microstrip form as already mentioned. A lumped inductor can be realized by a short length of high impedance microstrip and a lumped capacitor by a short length of wide microstrip as shown in Fig. 5.4 (a) and (b) respectively.

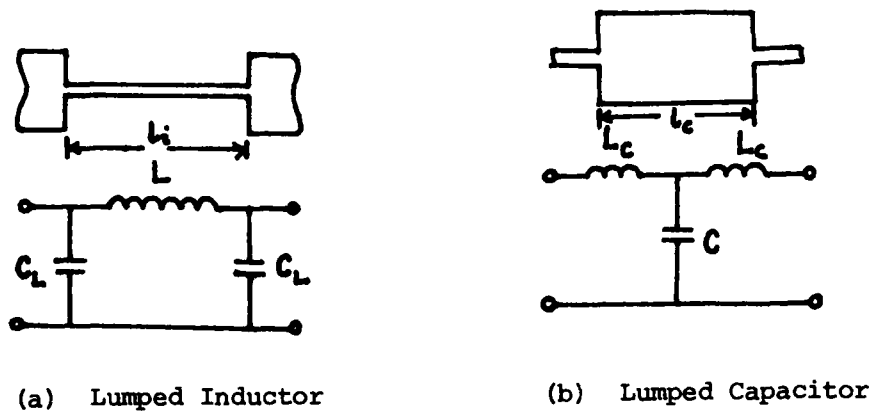


Fig. (5.4)

The length of the inductor is given by²

$$l_i \approx \frac{f \lambda_g L}{Z} \quad (45)$$

where f is the frequency and λ_g is the wavelength in microstrip. The end-capacitances, C_L are given by

$$C_L = \frac{l_i}{2fZ\lambda_g} \quad (46)$$

The length of the lumped capacitor is given by,

$$l_c \approx f \lambda_g ZC \quad (47)$$

and the end-inductances are given by

$$L_C \approx \frac{l_c Z}{2f\lambda_g} \quad (48)$$

The lengths of the lumped elements are required to be less than $\lambda_g/7$ as discussed in Section 1.5. Further the transverse dimension of the lumped capacitor should be less than $\lambda_g/2$ to prevent any radiation.

²T. C. Edwards, "Foundations for Microstrip Circuit Design," John Wiley & Sons, N.Y., 1981, p. 212.

It can be seen from equations (45) and (47) that for a given value of the lumped element, at a particular frequency the length of the element is a function of the line impedance. The choice of the line impedance fixes the width of the strip for a given substrate thickness. The width of the microstrip must be such that the current density in the strip cross section does not exceed the recommended maximum value ($\approx 10^5$ A/cm² for Au on GaAs).

5.6 General Remarks

1. The substrate thickness in the present design was restricted to 6 mils from the point of view of the problems in fabrication of vias for grounding purposes.
2. The conductor loss (which is of the order of 1.3 dB/cm @ 20 GHz in a 100 Ω microstripline on a semi-insulating 6 mils thick GaAs substrate ($\epsilon_r = 12.9$)) in microstriplines is negligibly small compared to the gate and drainline attenuations caused by the parasitic resistances of the device.
3. The end capacitances in lumped inductors and end inductances in lumped capacitors must be taken into account in the design. One can take advantage of the end capacitances in drain line inductors to increase the drain line shunt capacity. The reactive elements due to steps and bends in microstrips also need to be considered in the design.
4. For large capacitance values MIM (Si_3N_4) capacitors will be used.
5. The resistive terminations to be used are either MESA or metal type depending on the resistance value.

Fig. 5.4 shows the amplifier circuit topology. The layout of a distributed amplifier designed using TI 150 μm GaAs MESFET is depicted in Figures 5.5(a) - 5.5(d). The performance of the amplifier simulated on the computer is shown in Figures 5.6(a) - 5(c).

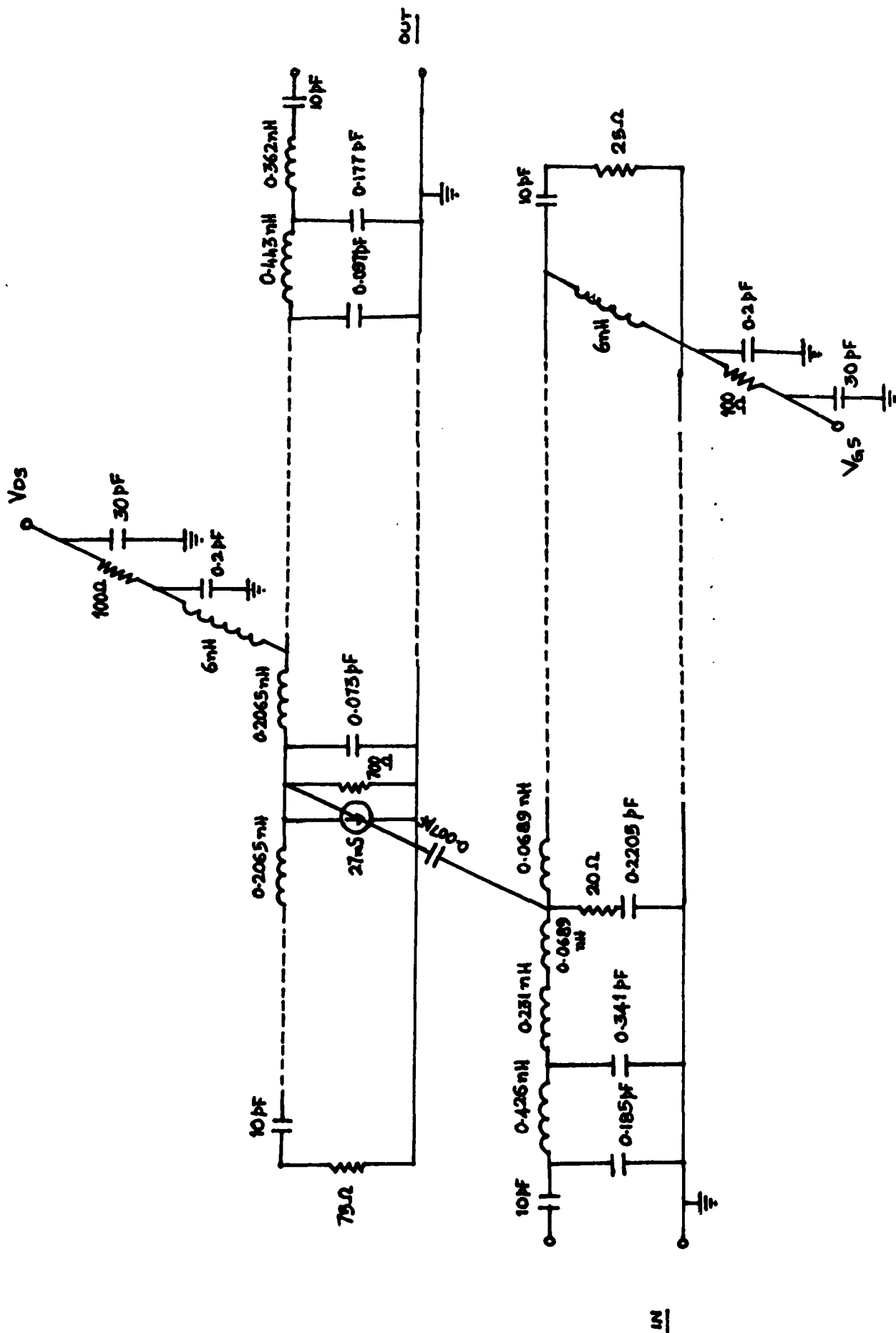


Fig. 5.4. The distributed amplifier circuit topology.

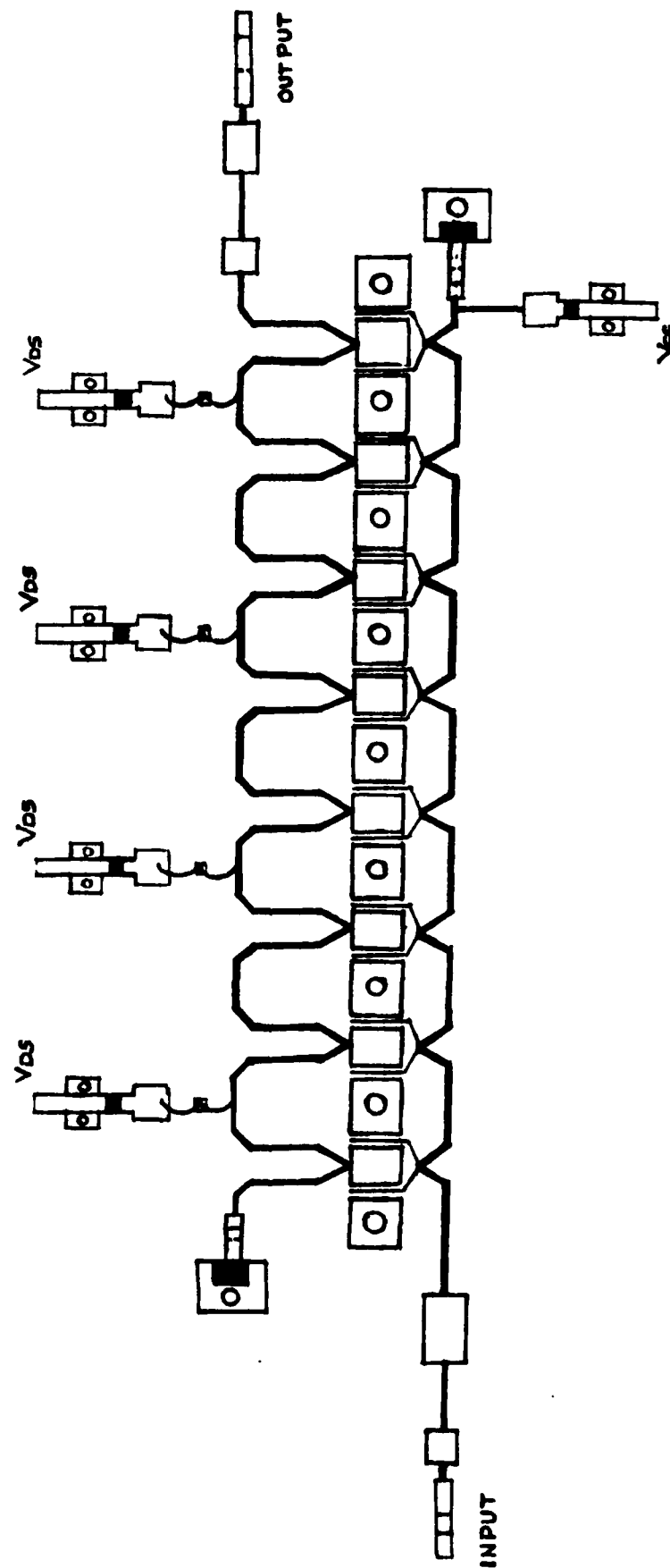
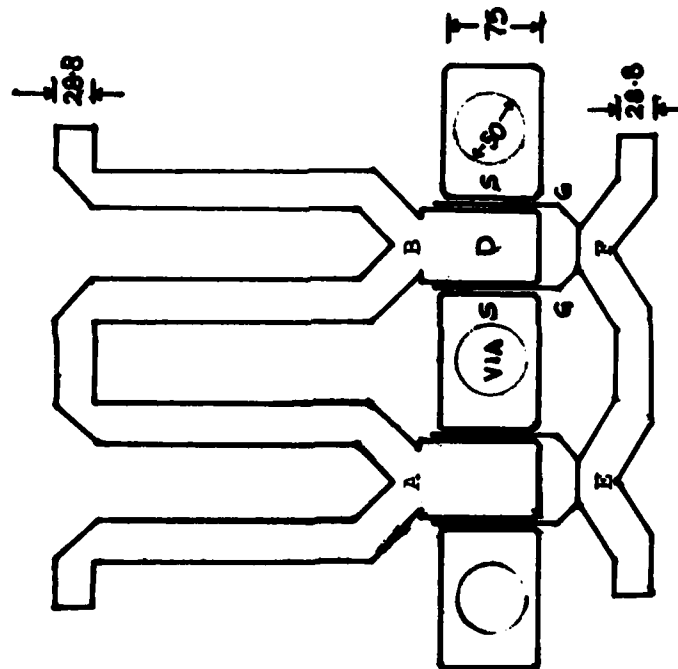


Fig. 5.5(a). Layout of the amplifier (not to scale).



Length of gate line inductor (E-F): 185 μm
 Length of drain line inductor (A-B): 554 μm

Fig. 5.5(b). A Section of the Distributed Amplifier
 (all dimensions in μm .)

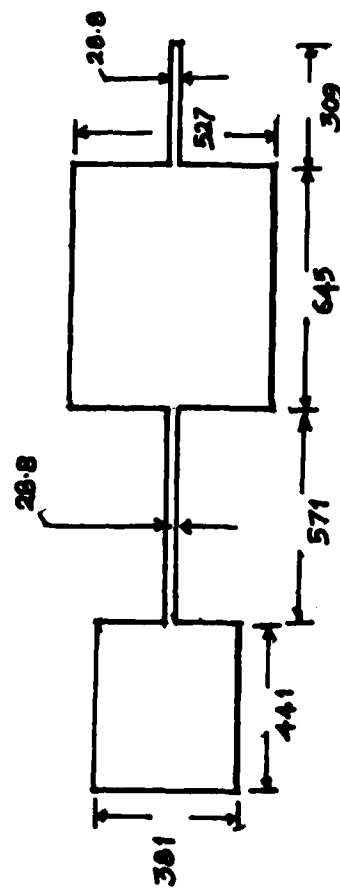


Fig. 5.5(c). Input matching network (all dimensions are in μm .)

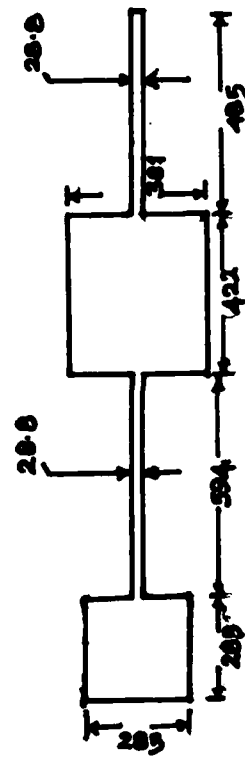


Fig. 5.5(d). Output matching network (all dimension in μm .)

f1 marker freq up
 f2 change scale
 f3 plot hardcopy
 f4 exit plot
 f5 marker freq down

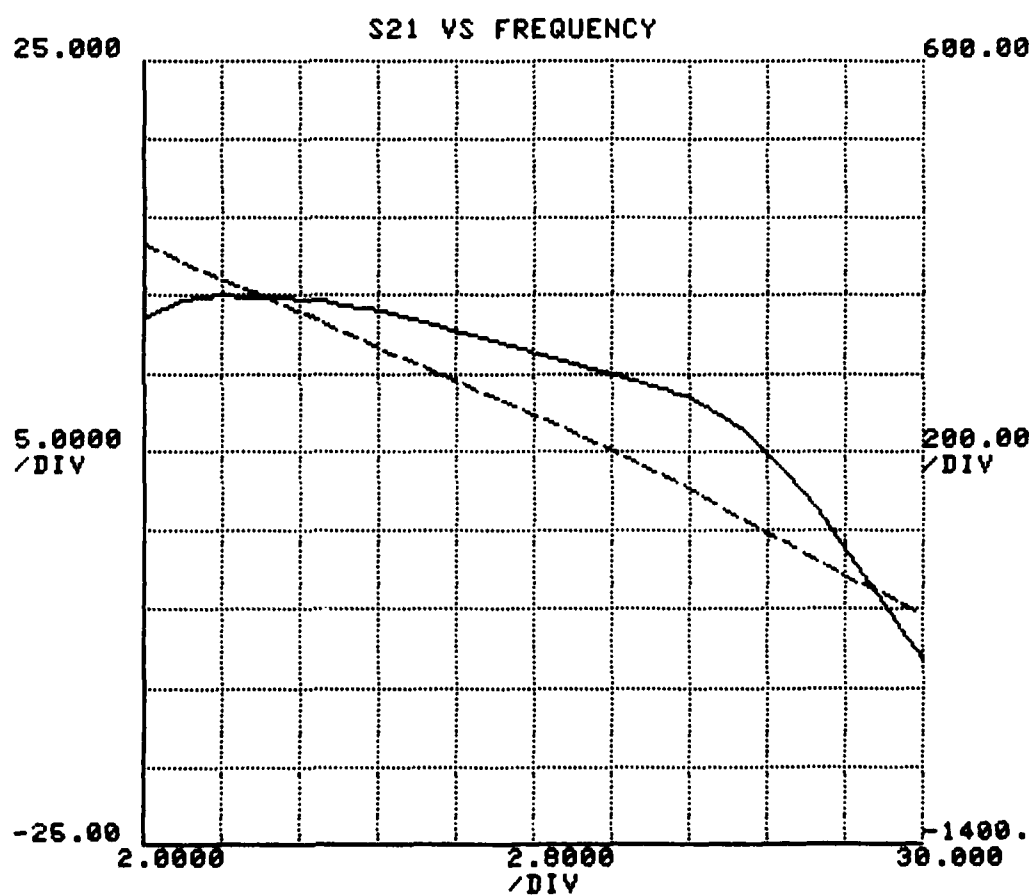


Fig. 5.6 (a). The distributed amplifier gain vs. frequency.

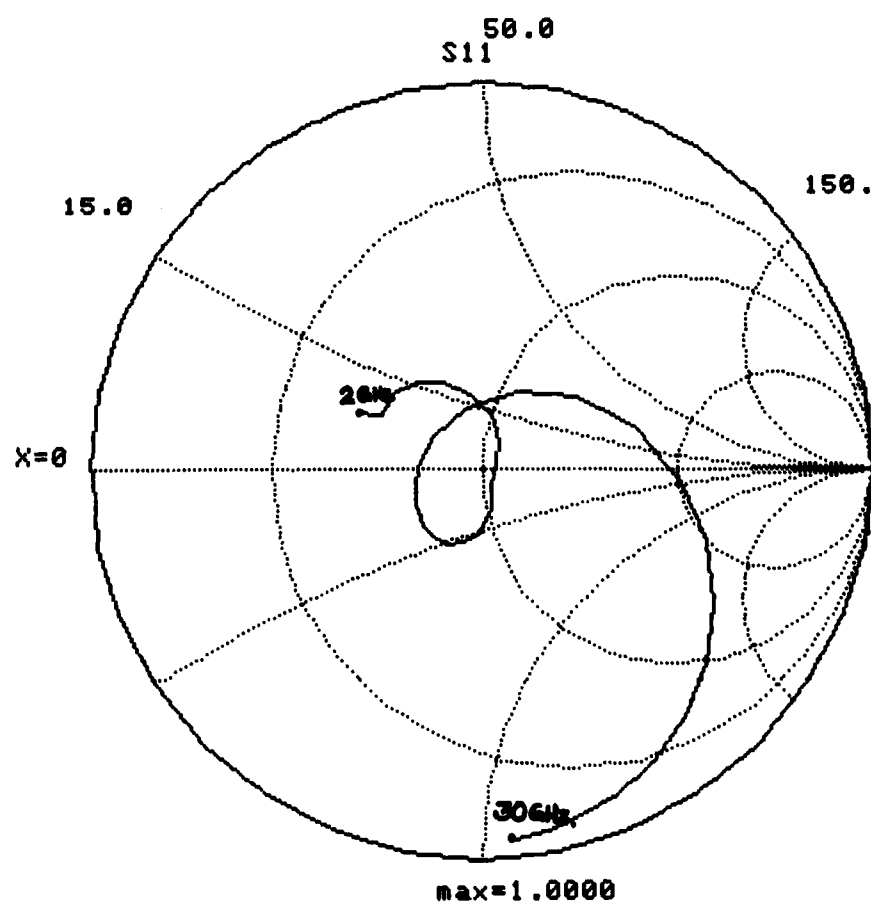


Fig. 5.6 (b). S_{11} of the amplifier.

f1 marker freq up
 f2 change scale
 f3 plot hardcopy
 f4 exit plot
 f5 marker freq down

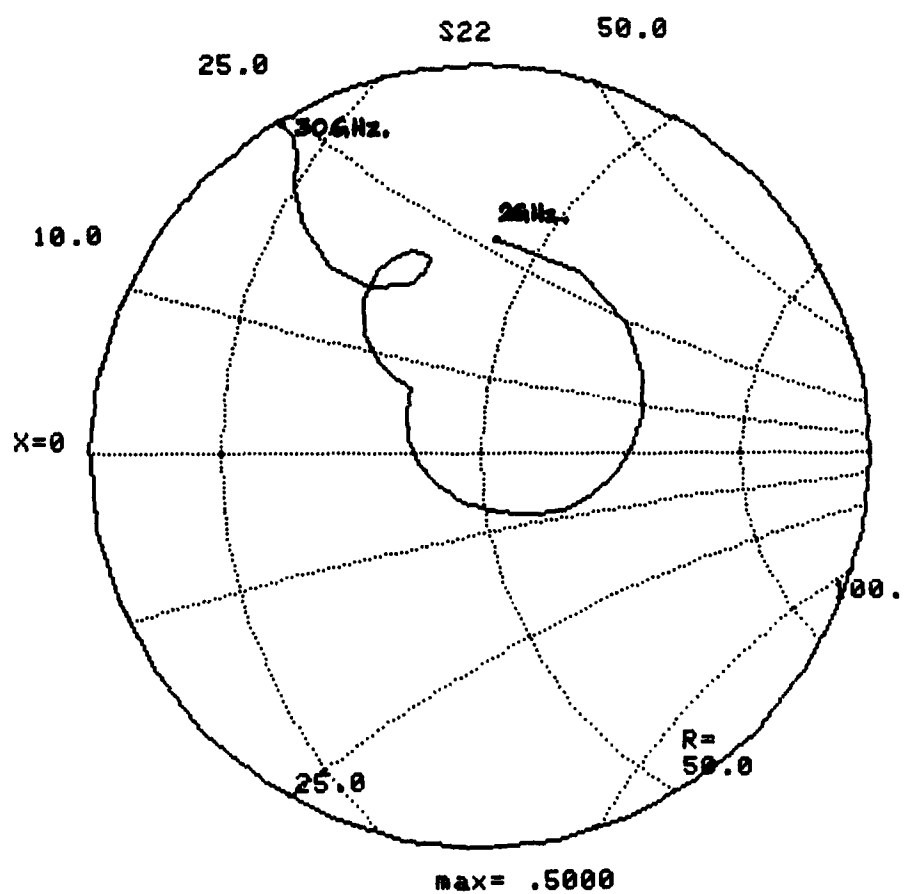


Fig. 5.6(c). S_{22} of the amplifier.

SUMMARY, CONCLUSION AND PRESENT EFFORTS

Theoretical analysis of a distributed amplifier has been carried out resulting in closed form expressions for gain, optimum number of devices, line attenuations and phase constants. A computer program has been developed to simulate a distributed amplifier on the HP 1000 computer. With this program, computer aided design of the amplifier can be carried out.

The classical definition of gain-bandwidth product was examined in the context of the distributed amplifier and found to be unsatisfactory for the purpose. We are continuing to consider this question and work is underway to determine a suitable figure of merit for a distributed amplifier. Extensive sensitivity studies of the gain with respect to various circuit parameters were carried out.

Both the analytical and computer aided studies have revealed the importance of $\omega_H(1/R_g C_g)$, the gate circuit cutoff frequency in controlling the attenuation in the gate line and hence the amplifier gain performance at high frequencies. The sensitivity analysis of the amplifier has also indicated that the parameters R_g and C_g of the device are the critical parameters severely affecting the gain of the amplifier. Therefore it can be said that a reduction in $R_g C_g$ -product of the device is necessary for its use in a wideband distributed amplifier.

Computer studies have resulted in evaluating the effects of line impedance and terminations on the gain and general performance of the amplifier.

From the scaled data for devices it has been shown that in order to increase the gain at 20 GHz one has to use devices smaller than 300 μm . Accordingly an amplifier has been designed using TI 150 μm device. The performance of the amplifier was simulated on the computer. The layout and computer performance of the amplifier are given in the report. The amplifier has a gain of 4.75 dB at 20 GHz.

At present we are awaiting more data on devices from TI in order to send the design for fabrication at TI. We will continue theoretical studies on gain bandwidth product, figure of merit and sensitivity of the amplifier. In addition we are continuing a detailed study of the comparison of the distributed amplifier with the conventional cascade amplifier.

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