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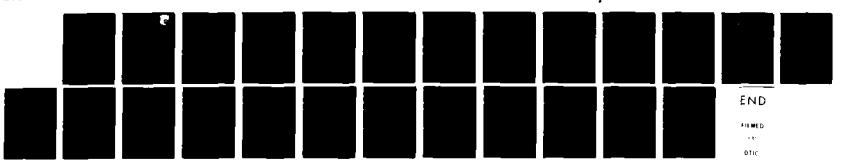

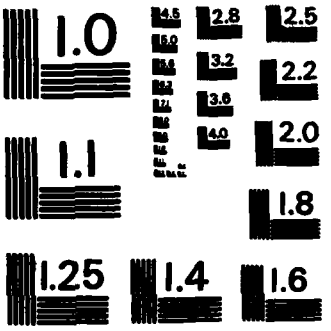

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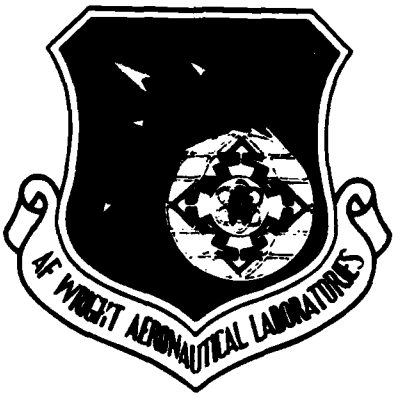

ADVANCED AVIONIC SYSTEMS FOR MULTIMISSION APPLICATIONS

Boeing Military Airplane Company
Seattle, Washington 98124

October 1982

Final Report for Period July 1980 - June 1981

Approved for public release, distribution unlimited.

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This technical report has been reviewed and is approved for publication.

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This technical report summarizes the update of the Single Processor Synchronous Executive (SPSE) to MIL-STD-1553B, MIL-STD-1750, and MIL-STD-1589B. This update was conducted as a follow-on to the original SPSE task performed for the AASMMA program.

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FOREWORD

VOLUME III

This final technical report for the Advanced Avionic Systems for Multi-Mission Applications (AASMMA) was prepared by The Boeing Military Airplane Co. (BMAC), Seattle, Washington. The final report consist of three separately bound volumes which covers the work performed under contract F33615-77-C-1252 during the period of January 1978 to June 1981.

The program was performed in two phases for the Air Force Wright Aeronautical Laboratories, Wright-Patterson AFB, Ohio 45433. The first phase covered three tasks which addressed (1) Distributed Avionics Information System Design, (2) Avionic Cost Analysis Methods & Models, and (3) Embedded Microcomputer Standardization Concepts. These tasks were conducted for AFWAL/AAAA. The contract monitor was Mr Gary Wambold, the program manager was Mr Donald E Dewey, and the principal investigators were Dr Leroy A Smith and Mr Al Crossgrove. Volume I of this report describes this phase.

The second phase of the program Volumes II and III covered tasks which addressed (1) the Development & Evaluation of Advanced Digital Avionics System Architectures and (2) the Development of a Single Processor Synchronous Executive (SPSE) derived from the Digital Avionics Information System (DAIS) Executive. These tasks were conducted for AFWAL/AAAS and the AFWAL contract manager was Mr Claude M Fletcher, Jr, the Boeing program manager was Dr Leroy A Smith, and the principal investigator was Mr Stephen W Behnen.

The other significant contributers to this effort included:

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1.1 Scope

This technical report summarizes the update of the Single Processor Synchronous Executive (SPSE) to MIL-STD-1553B, MIL-STD-1750, and MIL-STD-1589B. This update was conducted as a follow-on to the original SPSE task performed for the AASMMA program. The SPSE update effort began in July 1980 and was completed in May 1981.

The update of the Single Processor Synchronous Executive was accomplished in three phases. Phase 1 was the update to MIL-STD-1553B and is described in detail in section 3.1. Phase 2 was the update to MIL-STD-1750 and is described in section 3.2. Section 3.3 describes phase 3 of the update effort, the conversion to MIL-STD-1589B.

The successful completion of each phase was verified by a laboratory demonstration of the SPSE capabilities. In section 4.0 the performance of the converted SPSE is described along with the demonstration results.

1.2 Background

The Single Processor Synchronous Executive was originally derived from the DAIS executive released in September 1979. The objective of the original SPSE was to develop a version of the DAIS executive that was a least one-third smaller and required less processing time. The result of the SPSE effort was an executive designed to support a single processor architecture where the normal bus traffic is totally synchronous. The original SPSE, which was delivered in April 1980, was coded in J73/I HOL, controlled bus traffic on a MIL-STD-1553A data bus, and executed in a AN/AYK-15 processor. The DAIS executive-to-applications interface, as well as all other DAIS standards, were maintained in the SPSE. The delivered size of the original SPSE was 5564 words and it ran 35 to 40% faster than the DAIS executive.

During the time that the SPSE was being developed, the military standards on which it was based were being updated. The DAIS executive was scheduled for

conversion to the latest standards and an AASMMA follow-on task was defined to provide a similar conversion of the SPSE. This report summarizes the conversion of the SPSE to these latest standards.

1.3 Program Objective

The primary objective of the SPSE conversion was to update the SPSE to the new military standards and to maintain the original SPSE objectives:

- o support synchronous bus communications
- o maintain the DAIS executive-to-application interface
- o strive for minimum memory requirements
- o support the avionic system load for an AMST or modern tactical fighter aircraft
- o use the DAIS support software such as LINKS, ALAP, PALEFAC and the PALEFAC preprocessor.

A secondary objective of the SPSE conversion was to keep the SPSE concurrent with the latest enhancements to the DAIS executive.

2.0 Program Summary

Work on the SPSE conversion began in July 1980 with the conversion to MIL-STD-1553B and continued through April 1981 when the conversion to MIL-STD-1589B was complete. The software delivery of the fully converted executive was on 24 April 1981.

2.1 Approach

The SPSE conversion occurred in three distinct steps as shown in the SPSE conversion schedule, Figure 2-1. The first update was a 1553B, AN/AYK-15, J73/I version. The second update was a 1553B, AN/AYK-15A, J73/I version. The third update was to 1553B, AN/AYK-15A, J73. For each update to the SPSE, the following steps occurred:

1) New documentation was produced. This included an updated System Control Procedures, Part I Specification and Part II Specification.

2) An Interim Program Design Review (IPDR) was held to review the changes made for the update.

3) The executive was coded, compiled and linked.

4) The executive was integrated into a laboratory environment and thoroughly debugged and tested.

5) A demonstration was held as specified in the SPSE Test Plan/Procedures.

Each update to the SPSE began by examining the DAIS executive documentation for that version and identifying the update related changes that occurred and the enhancements that were made. Each change was examined for applicability and incorporated into the SPSE documentation and code if it met the objectives of the SPSE conversion program.

The original SPSE conversion schedule called for the documentation of all three updates to be completed by 1 September 1980. Because of delays in receipt of the DAIS executive documentation, update and delivery of the SPSE J73 documentation did not occur until February 1981. Also because of this delay, and the delay in the receipt of the GFE AN/AYK-15A, the third IPDR and 1750 demonstration was delayed until March 1981.

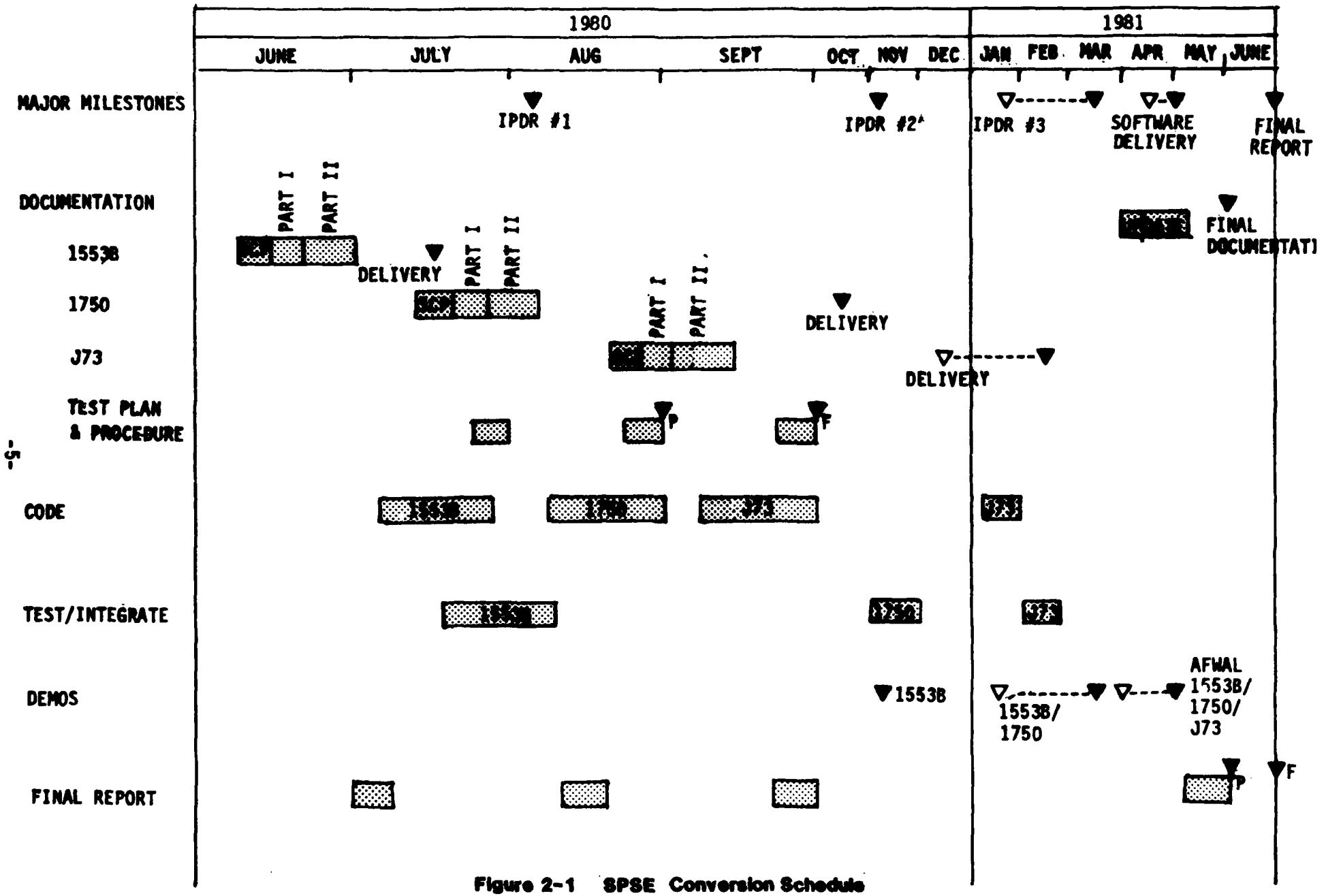

Figure 2-1 SPSE Conversion Schedule

2.2 Documentation Produced

A number of documents were generated in support of the SPSE conversion. Each update to the SPSE required a new System Control Procedures, Part I and Part II specification which superseded the document for the previous version. The complete list of documents is provided in Table 2-1.

Table 2-1 SPSE DOCUMENTATION

1553B UPDATE

SPSE System Control Procedures
Computer Program Design Specification for the SPSE, Part I
Computer Program Product Specification for SPSE, Volume I: Local Executive
Computer Program Product Specification for SPSE, Volume II: Master Executive
IPDR #1 Agenda
IPDR #1 Presentation Material
IPDR #1 Minutes
SPSE Functional Test Report, Group I, Part I
SPSE Source Code

1750 UPDATE

SPSE System Control Procedures
Computer Program Design Specification for the SPSE, Part I
Computer Program Product Specification for SPSE, Volume I: Local Executive
Computer Program Product Specification for SPSE, Volume II: Master Executive
IPDR #2 Agenda
IPDR #2 Presentation Material
IPDR #2 Minutes
SPSE Functional Test Report, Group I, Part 2
SPSE Source Code

Table 2-1 SPSE DOCUMENTATION (Cont.)

J73 UPDATE

SPSE System Control Procedures
Computer Program Design Specification for the SPSE, Part I
Computer Program Product Specification for SPSE, Volume I: Local Executive
Computer Program Product Specification for SPSE, Volume II: Master Executive
IPDR #3 Agenda
IPDR #3 Presentation Material
IPDR #3 Minutes
SPSE Functional Test Report, Group II
SPSE Source Code

OTHER DOCUMENTS

SPSE Test Plan and Procedures
Technical Report

2.3 Support Tools

In addition to the SUBSORT and INGEUNS support tools described in the AASMMA Final Report (1 May 1980), one additional support tool was created to aid the program development.

The Original Nested Test Organizer (TONTO) is a modified version of the NROFF text processor available under the UNIX operating system. All versions of the System Control Procedures were combined into a single nested text file and all versions of the Part I Specifications were combined into a second nested text file. This format allows fast and easy comparison of the many updates and variations in the different versions. The TONTO program can be commanded to extract from a nested text file any single version of the SCP or Part I Specification. The TONTO program is the text processing equivalent of the INGEUNS program which can extract from the universal source files the code for a single version of the SPSE.

3.0 DETAILED PROGRAM DESCRIPTION

3.1 MIL-STD-1553B CONVERSION

The first phase of the SPSE update effort was to change the multiplex data bus protocol from MIL-STD-1553A to MIL-STD-1553B. The major differences between 1553A and 1553B which affected the SPSE are listed below.

- o MODE CODES: 1553B explicitly defines the meaning and implementation of all mode codes while 1553A allows the user to define the mode commands.

- o STATUS WORD: 1553B defines the use of each bit in the status word while 1553A defines only the MESSAGE ERROR and TERMINAL FAIL bits. 1553A provided nine bits that were available for the user to define.

3.1.1 Directly Related Changes

Because the update to 1553B is a change in the multiplex data bus protocol, only the master executive, which is responsible for bus control and bus error processing, is affected. There were no changes to the local executive or to the local executive data base as a result of the update to 1553B.

Several changes were made to the PALEFAC tables used by the master executive. The bus commands in P$MCPLIST, the minor cycle bus list, changed to reflect the new Synchronize with Data Word mode code. Likewise, the bus commands in P$IDLE, the idle polling list, changed to reflect the new Transmit Status mode code. These two PALEFAC changes did not require any changes to the master executive code. In P$TDB, the terminal data base, the data items relating to the interface modules in a remote terminal were deleted. As a result, the code changed in the bus error processing routine M$ERCON that referenced the terminal data base.

In addition to the PALEFAC data base changes, there were changes in the master executive data base. In both the run queue and the input queue the type RT'CHNL'ERR was deleted. The master executive code that referenced this data was also deleted.

One other 1553B related change to the master executive was in the code that set the BCIU's Processor Control Register (PCR). Bit 14 of the PCR is the BUSY/CONTINUE bit. In 1553A, a 1 in this bit position signified the busy state. The 1553B BCIU interpreted a 1 in this bit to signify CONTINUE.

3.1.2 Enhancements

Not all of the changes made to the 1553B version of the SPSE were directly related to the change in bus protocol. During the conversion of the DAIS executive to 1553B, several performance enhancements were incorporated into the code. These enhancements, which were included in the SPSE 1553B update, are listed below.

1) W$RNQ'MDR was deleted from the run queue entry format. This entry had been used to store the mode data register each time the bus was halted in case the current bus list would be suspended.

2) A new input queue type was added: BCIU'FAULT. This entry type is entered into the input queue whenever an invalid bus status word is detected.

3) The name of the routine M$EATINPQ was changed to M$CLRINPQ. There was no change in the actual code of the routine.

3.2 MIL-STD-1750 CONVERSION

The second update to the SPSE was a change in target machines. The original SPSE and the 1553B update to the SPSE both executed in an AN/AYK-15 processor. The 1750 update to the SPSE enabled it to execute in an AN/AYK-15A processor, a MIL-STD-1750 machine. The SPSE, then, was impacted by both MIL-STD-1750 and the AN/AYK-15A design specification.

3.2.1 Directly Related Changes

The update to MIL-STD-1750 required that a new J73/I compiler be used. Most of the executive HOL code did not change and a single recompilation was all that was necessary to convert the executive to MIL-STD-1750. The executive code that did change was in the hardware interface routines and in the application task interface routines as described below.

1) Interrupt processing was changed to reflect the change in the interrupt structure between the AN/AYK-15 and the AN/AYK-15A. The number and types of machine interrupts changed and the number of BCI interrupts dropped from 6 levels to 2 levels.

2) The processor/DMA sequence changed. The new processor/BCI interface includes a lockout flag that is set before DMA and cleared afterwards. The executive READ and WRITE service routines now test this flag before proceeding with the read or write operation.

3) The subroutine linkage mechanism changed. The AN/AYK-15A processor performs subroutine linkage through a stack. A system stack has been defined for use by the executive and privileged mode application tasks. In addition, plus each normal mode application task has its own stack area.

4) The executive routines that were written in assembly language were recoded in the 1750 assembly language.

5) The executive service routines for the 1750 version were written in assembly language to facilitate switching the stack pointer (R15) from the application stack to the system stack when an executive service is requested.

3.2.2 Enhancements

As in the 1553B update, several enhancements that were made during the DAIS 1750 update were included in the SPSE 1750 update. These enhancements are listed below.

1) The input and run queue type BCIU'FAULT was deleted.

2) The interface routines to Timer B were deleted.

3) Starting and stopping the bus was simplified.

4) The handling for machine related interrupts was transferred to the local executive.

3.3 MIL-STD-1589B CONVERSION

The third and final update to the SPSE was the conversion from MIL-STD-1589 (J73/I) to MIL-STD-1589B (J73) high order language. Each routine of the executive that was written in J73/I was rewritten in J73. The assembly language routines were not affected by this update. The major differences between J73/I and J73 that affected the SPSE are listed below.

1) The START and TERM directives were added to each module.

2) [ ] were changed to ( ).

3) SWITCH statements became CASE statements.

4) Status lists became status types.

5) Rigorous type checking was added.

6) Embedded procedures were repositioned.

3.3.1 Directly Related Changes

The most obvious result of the change to J73 is that all high order language code was changed to the new syntax. Other directly related changes in the executive were:

- some status lists were changed to defines
- many of the data tables and items were changed to a data type more descriptive of their function
- the defines and declarations for the real-time statements were changed

3.3.2 Enhancements

In addition to the changes directly related to the update to J73, several enhancements were incorporated into the executive. These enhancements were first included in the J73 DAIS executive and were added to the J73 SPSE after they were evaluated and, in some cases, modified.

1) The two stacks used by application tasks, A$XXXX and J$XXXX, were consolidated into a single stack, J$XXXX. This change resulted in deletion of the privileged comsub area and V$TOS and in changes to Task Table 8.

2) In order to protect the minor cycle data, interrupts were disabled at the beginning of X$MCSETUP and enabled again after the test of the minor cycle number.

3) Starting the BCI was simplified by having M$STAR set the instruction address register (IAR) instead of requiring each routine that called M$STAR to set the IAR first.

4) Bus error processing was completely changed. The new bus error processing was organized into a more structured flow to improve the control flow and provide easier maintainance. Table 3-1 shows the routines that were deleted and the routines that now comprise the new bus error processing.

Table 3-1 BUS ERROR PROCESSING ROUTINES

ROUTINES DELETED	ROUTINES ADDED
M$ERCON	M$ERCON
M$CONMAN	M$CONMAN
M$FAILTERM	M$FAILTERM
M$TFAIL	M$TFAIL
M$CLRINPQ	M$TOGGLE'BUS
M$ERNQ	
M$PATH	
M$RETRY	
M$SETUP	
M$BUSEX	
M$MDCODE	
LOGFAULT	

4.0 DEMONSTRATION RESULTS

The SPSE was demonstrated after each conversion step. The 1553B demonstration was conducted at the Boeing DARTS facility on 17 November 1980. On 18 March 1981 the 1750 demonstration was also held in the Boeing DARTS facility. The SPSE J73 demonstration was held in the AFWAL facilities at WPAFB on 29 April 1981.

The 1553B and the 1750 demonstration consisted of monitoring the processing which occurred in a single load module while specially designed applications software (MAP) was requesting services of the SPSE. The J73 demonstration was in two parts with each part requiring a different load module. The first load module was the SPSE linked to the MAP software. The second was the SPSE linked to a modified version of the DAIS Validation and Verification (V&V) program. Each of the three SPSE demonstrations was a complete success and showed that the executive was working properly at each conversion level.

The Boeing and AFWAL demonstrations verified that the SPSE code satisfied the design requirements and the conversion objectives listed in section 1.3 of this report. All features of the SPSE described in the (1553B, AN/AYK-15A, J73) Part I and Part II specifications have been supplied in the delivered software.

The delivered size of the fully converted SPSE is 3648 words. This compares to 8486 words for the fully converted DAIS executive. Figure 4-1 shows the evolution of the executive size from the original SPSE to the J73 SPSE.

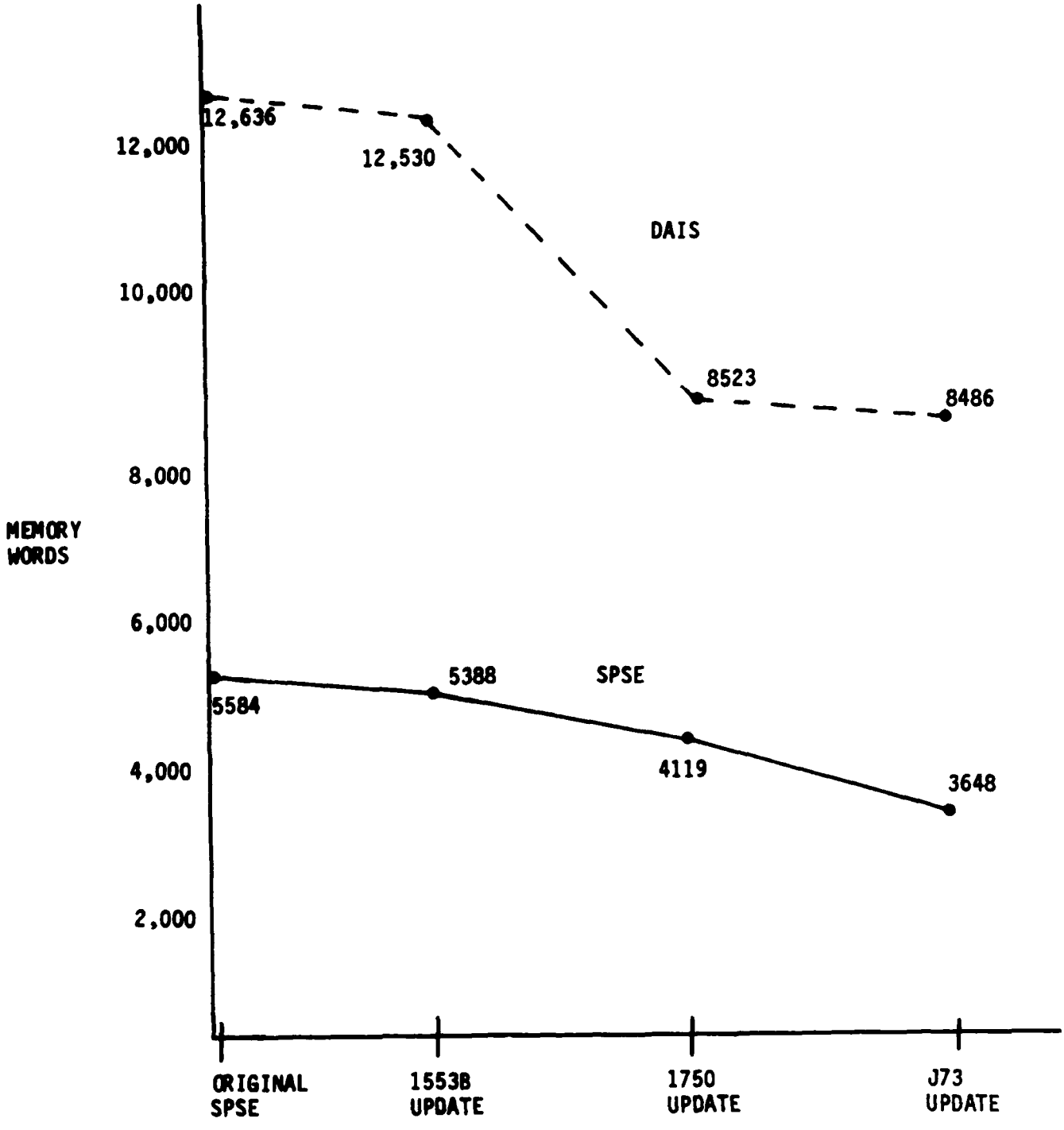

Figure 4-1 SPSE Memory Requirements