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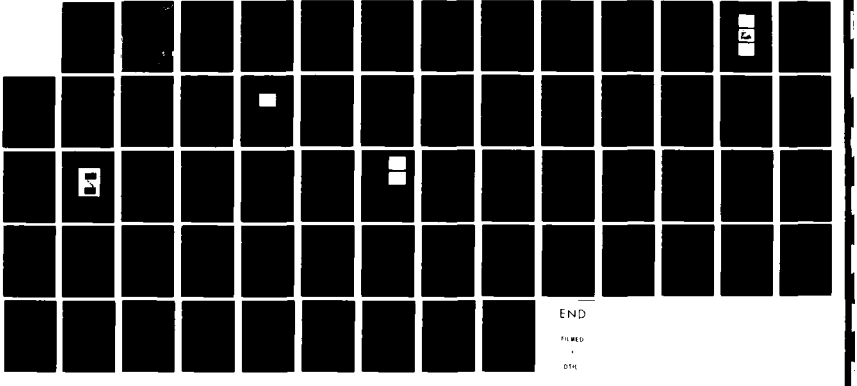

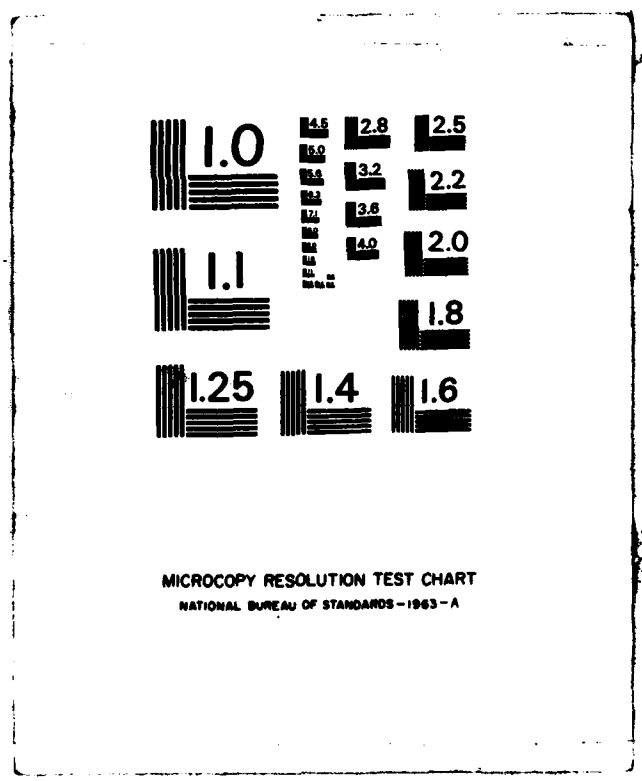
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S-I-S mm-WAVE MIXERS AND DETECTORS

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This program is part of an ongoing effort to fabricate all-refractory S-I-S devices for use as mm-wave detectors and mixers in the quantum regime, and operating in the temperature range of 8-10 K. There are four ongoing approaches to achieve this goal: (1) Development of high-quality NbN-barrier-Nb S-I-S junctions as an intermediate goal towards fabricating all-NbN junctions; (2) Actual development of all-NbN junctions using the results of (1) above as a guide; (3) Development of an in-house NbN deposition capability in order to speed the progress on (2) above; and (4) The use of existing all-Nb digital circuit fabrication capability to design

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and fabricate mm-wave mixers to operate at $T \lesssim 4.2$ K, thus gaining valuable experience that can be applied to the eventual design of all-NbN mixers.

Sputtered NbN-a:Si-Nb Josephson tunnel junctions fabricated using SRC's SNAP process (Selective Niobium Anodization Process) have been developed to yield $I_C R_N = 1.5$ mV, $V_m = 25$ mV and $V_g = 3.8$ mV at $J_o \sim 10 - 1000$ A/cm^2, where I_C is the critical current, R_N is the normal resistance, V_m is the subgap leakage parameter, V_g is the sum of gaps voltage, and J_o is the critical current density. The improvements required to yield these parameters are: (1) A low power (20W), long (1 hr) sputter etch of the NbN surface prior to barrier deposition and (2) The use of an a:Si/a:SiH/a:Si composite barrier. These improvements are sufficient to make these devices interesting for use as S-I-S mm-wave detectors operating in the 100 GHz range.

All-NbN devices using the plain a:Si barrier have been developed to the point where they exhibit S-I-S tunnelling characteristics, albeit of only fair quality. Processing of these devices requires the use of a thermal oxidation variant of SNAP. Due to the delays encountered in transporting all-NbN samples from SRC to NRL for NbN deposition, SRC is developing an in-house NbN sputtering capability. The best results to date are $T_C = 15.1$ K for a NbC_xN_y film deposited at ambient temperature as a gas mixture consisting of $Ar:N_2:CH_4$ in the ratio of 62:5:2 and at a total pressure of 10 mTorr and a power of 500 W. This is approaching the quality required for S-I-S device fabrication.

Fourteen types of mm-wave mixer chips have been designed in collaboration with the Goddard Institute for Space Studies using the existing all-Nb digital circuit fabrication process. Masks were fabricated, and a trial fabrication proved the integrity of the process. The viability of the proposed mounting scheme has been experimentally ascertained.

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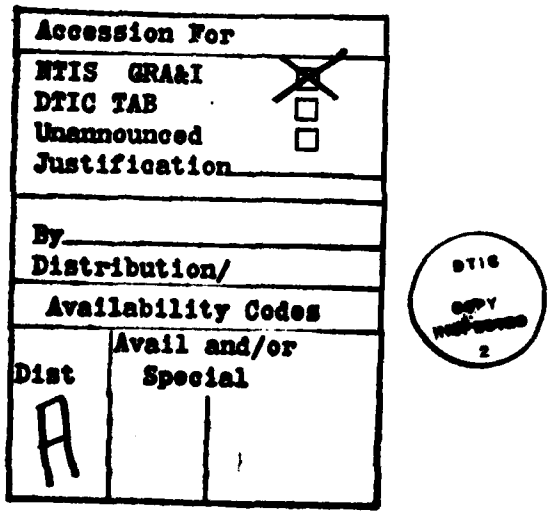

LIST OF ILLUSTRATIONS

SECTION 1

INTRODUCTION

The work described in this report was done under NRL Contract No. N00014-81-C-2525. The objective of this effort is to develop a technology for the fabrication of refractory superconducting tunnel junctions which can operate efficiently in the photon-assisted tunneling mode at temperatures of 8 - 10K as either mixers of detectors of mm-wave radiation. The work described in this report is ongoing work. Previous work was done under NRL Contract No. N00173-80-0159, and reported in September 1981.[1]

That previous work explored the use of polysilicon, amorphous sputtered silicon (a-Si), and low temperature chemical vapor deposited germanium (CVD Ge) as barriers for NbN-barrier-Nb tunnel junctions. Use was also made of the selective niobium anodization process[2] to pattern the junctions. The amorphous sputtered silicon resulted in the best tunneling junctions with a value of $I_c R_N$ = 1 mV, V_m = 15 mV, V_g = 3.4 mV, and $J_o \simeq 10 - 100$ A/cm^2; where I_c is the critical current, R_N is the normal resistance, V_m is the subgap leakage parameter, V_g is the sum of gaps voltage, and J_o is the critical current density.

Devices made using arsenic (n type) doped CVD Ge barriers were promising, but results were not nearly as good as the a-Si barriers. It was discovered, however, that the NbN films used in the n-Ge work were of poor quality, and that better NbN base electrode films could result in superior devices.[3]

Boron doped (p type) CVD Ge barriers yielded fairly good super-Schottky devices for barrier thicknesses > 10 nm. Thinner barriers yielded Josephson junctions, but not of the desired S-I-S character required for mm-wave work. This approach was abandoned. Nonetheless, the work was judged to be of sufficient interest and merit to justify publication.

Hence some time was taken for additional study of these devices, resulting in a draft of a paper to be submitted to the Journal of Applied Physics. This manuscript is included in Appendix B of this report in its present form, and is currently undergoing revision before submission.

During the previous contract some preliminary work was done on fabricating NbN-barrier-NbN devices. It was found that anodization did not work well for device isolation, so thermal oxidation was tried using SiO_2 as an oxidation mask. At the time it was tentatively concluded that the thermal oxidation technique was successful,[1] and subsequent work has verified the efficacy of this process (see Section 3). No all-NbN S-I-S devices resulted from the early work, although some encouraging non S-I-S Josephson junctions were constructed.

Another very important result of the early work was the discovery that the quality of the NbN base electrode had a profound influence on the device results obtained. The transition temperature T_c, X-ray diffraction, and reflectivity measurements were subsequently made on all NbN base electrode films supplied by NRL. It was found that reflectivity > 80% at 850 nm, and T_c > 14K generally were required to produce good devices.

The above work on a-Si barriers and NbN quality was written up and submitted to Applied Physics Letters where it was published in April 1982.[3] It is also included in Appendix A of this report. In addition, this work was presented as a poster paper[4] at the March 1982 Meeting of the American Physical Society in Dallas, Texas, as was the aforementioned p-type Ge superSchottky junction work.[5]

The work described in this report is a continuation of the work described above, with the additional goal of ultimately incorporating suitable refractory S-I-S devices into mm-wave detectors and mixers operating in the quantum mode and at temperatures as high as 8 - 10 K. To attain this goal, work has proceeded along four major avenues: Further refinement of NbN-aSi-Nb devices, development of NbN-aSi-NbN devices,

development of in-house capability of sputtering high quality NbN films, and design and fabrication of S-I-S mm-wave mixers using existing all-Nb SNAP technology. Thus, this report will be divided into those four areas, followed by a conclusion section, which will include directions in which this work is presently proceeding. It is understood that all device fabrication is done using the selective niobium anodization process (SNAP) which has been fully publicized.[2] Additional details of SNAP specific for NbN device fabrication will be discussed where appropriate.

SECTION 2

NIOBIUM NITRIDE/NIOBIUM DEVICES

Even though the ultimate goal of this work is the development of all-niobium nitride devices, the fabrication of niobium nitride/niobium devices is an important and useful subgoal. This is especially true since SRC's program in Josephson Digital Devices and Circuits has resulted in outstanding results in fabricating Nb-aSi-Nb devices. Nb-aSi-Nb devices with V_m = 25 mV and uniformity of σ = 5% for 4 μm x 4 μm junction arrays have been achieved.[6,7] Many of these results feed directly into the niobium nitride program. Thus most of our work with NbN uses the a-Si barrier and SNAP to isolate the junctions. The difference in processing NbN devices is the use of thinner barriers to achieve the same current density.

Since the only niobium nitride used in this work which has produced good device results is deposited at NRL by E.J. Cukauskas and shipped to SRC, several days or more can elapse between the niobium nitride deposition and the barrier/counterelectrode deposition. Thus a standard procedure was developed to clean the niobium nitride prior to the barrier deposition. This consists of a 2 minute, 500 W sputter etch in the Perkin Elmer 24008SA system immediately before the barrier is deposited, but after the presputter of the Si target. This removes roughly 100 Å of NbN which should suffice to eliminate any oxide or surface contamination layers. This procedure is capable of producing a-Si barrier devices with, at best, V_m = 23 mV, I_cR = 1.2 mV and V_g = 3.5 mV. Although these are impressive results, the fact that I_cR and V_g are both lower than the theoretical expectation is in congruence with the theory for an S-I-N-S junction.[8] The presence of the typical knee structure just above V_g is also suggestive of a normal metal layer.[4,9,10] The fact that all-Nb

junctions using a nominally identical barrier yield I_cR = 1.7 mV and V_g = 2.8 (almost the expected value for Nb) indicates that the barrier and upper interface between the a-Si and Nb is probably not the problem. Thus we inferred that the sputter etch of the NbN results in sufficient damage and Ar implantation to convert the surface to something approximating a normal metal. An experiment using N_2 as the sputter etch gas in an attempt to preserve the NbN stoichiometry resulted in devices that looked more like S-I-N junctions than S-I-S. A sputter etch in argon at 20 watts for a full hour was then employed. The resultant devices had I_cR = 1.8 mV and V_g = 3.8 mV. This is a significant improvement, and indicates the importance of surface treatments to optimize S-I-S junction quality.

An important improvement in device quality that was discovered in the digital devices and circuits program is the use of a hydrogenated Si (a-Si:H) layer in the *middle* of the barrier. If the entire barrier is hydrogenated all-Nb devices are of greatly reduced quality. Presumably this is due to "poisoning" of the Nb adjacent to the barrier by the hydrogen. By sputtering unhydrogenated Si, followed by a-Si:H and then a final unhydrogenated Si it is possible to improve the quality of the barrier without poisoning the electrodes. The resultant devices using this composite barrier had a significant increase in V_m and I_cR. This result carries directly over to NbN/Nb junction fabrication. The use of the a-Si/a-Si:H/a-Si composite barrier resulted in improved V_m (to 25 mV) and a significant increase in I_cR, to 1.5 mV from 1.2 mV for nominally identical samples fabricated both with and without the composite barrier.

These results are summarized in Fig. 1(a,b,c). Fig. 1(a) is a very good standard device with the high power sputter etch and a-Si barrier. Fig. 1(b) shows the effect of using the composite barrier with subgap leakage reduced considerably. The effect of the low power sputter etch is

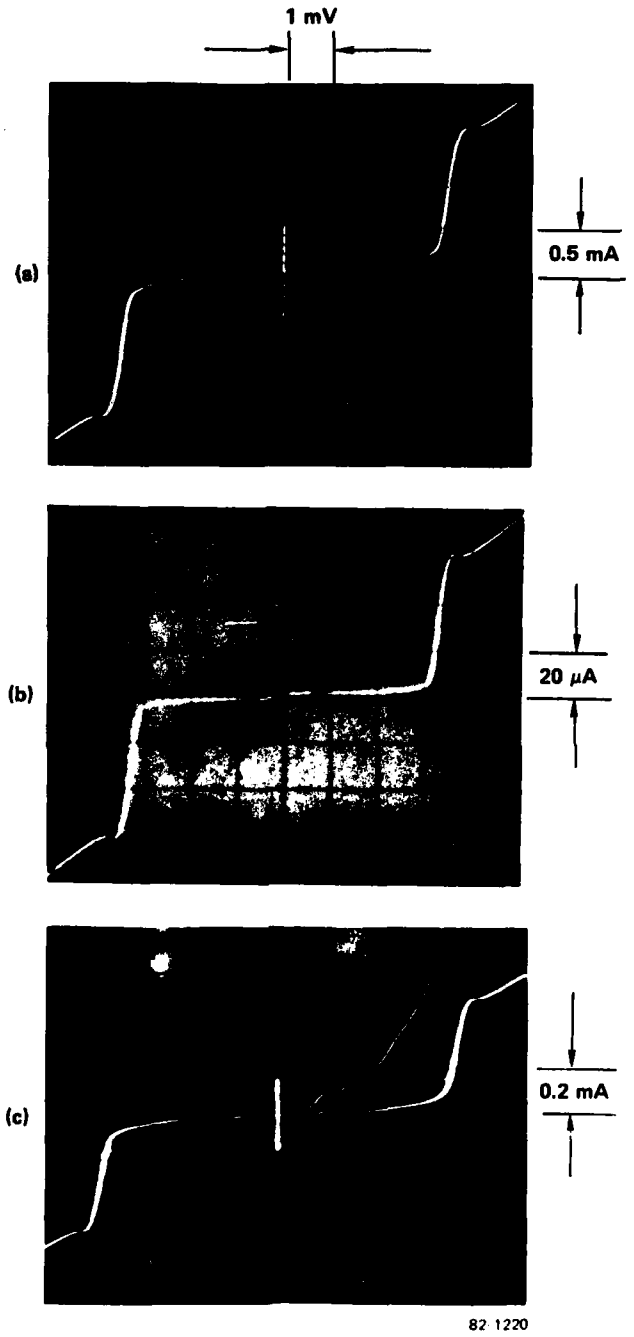

FIG. 1 I-V characteristics for NbN/αSi/Nb devices illustrating the effect of two major process improvements: (a) a baseline junction using the standard process; (b) the use of the composite barrier results in significantly lower subgap leakage current; and (c) the use of the low power sputter etch results in increased I_cR and V_g.

evident in c, with a gap voltage of 3.8 mV. Both of these improvements have not yet been incorporated together, but since they individually address different problems the net result should be further improvement in device quality. The fact that the knee structure above V_g is observed on all these devices indicates that the interface between metal and barrier is still less than ideal. Further improvement is also desirable in ΔV_g, the voltage spread in the rise of current at the gap. For S-I-S mm-wave applications the "corner" where the current rise at V_g occurs should be as sharp as possible.[12] Our best NbN/Nb devices should show some quantum effects at ~ 100 GHz ($\Delta V_g < hf/e$), but for operation at lower frequencies the above mentioned improvements will be required.

NbN/Nb junctions require a barrier about 2/3 the thickness of nominally identical Nb/Nb junctions in order to yield the same critical current density. This has been attributed to increased barrier height at the NbN/a-Si interface. In order to quantify the barrier height we have determined junction current density as a function of barrier thickness. This is plotted in Fig. 2. Since the critical current is sometimes difficult to measure accurately due to noise and flux trapping problems, we have measured the conductance at 5 mV for each junction on the wafer. This is plotted as a function of r^2, the square of the distance from the center of the silicon barrier deposition. It has been determined from optical experiments[13] that the barrier thickness, t, is given by

$$t = 4.7 \times 10^{-7} - 2.4 \times 10^{-9} r^2,$$

with units in cm. From the plot it can be seen that the conductance is exponential in thickness, as expected for a tunnel junction. Using the expression[13]

$$J = \frac{3.16 \times 10^{10}}{t} \sqrt{\phi} \exp\left(-1.025\ t\sqrt{\phi}\right)$$

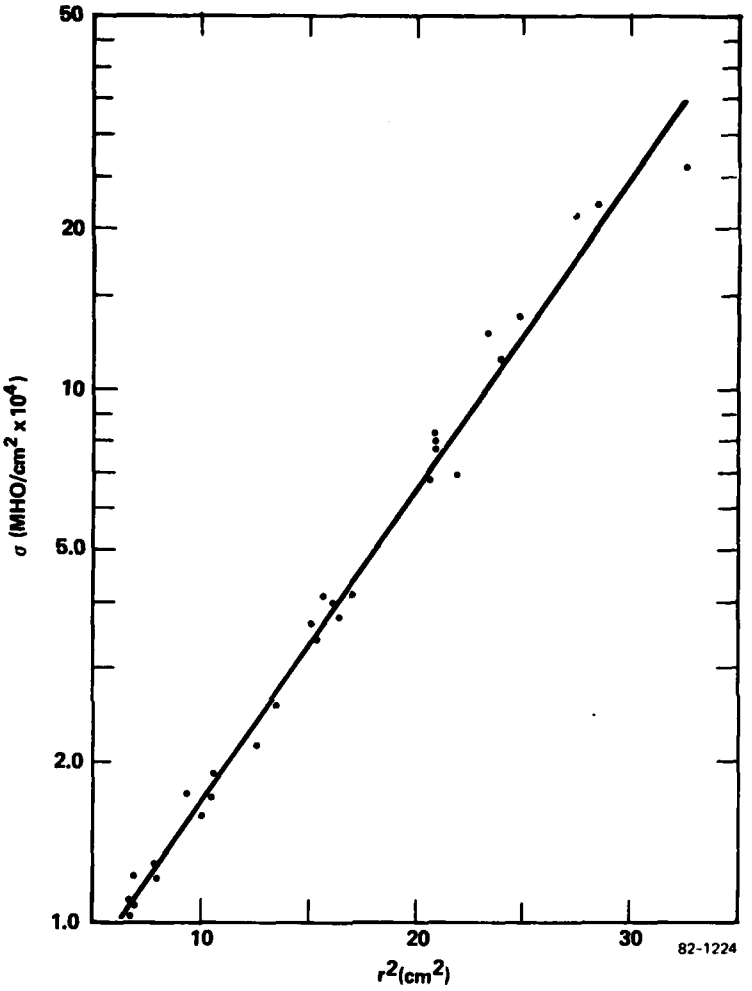

FIG. 2 The junction conductance per unit area (in mhos/cm^{2}x 10^4) as a function of the square of the distance from the center of the αSi barrier deposition. The linear dependence confirms tunneling as the transport mechanism and yields an average barrier height of ϕ = 0.28 mV.

we find that $\phi = 0.28$ V, where t is expressed in Å. This can be compared to $\phi = 0.08$ V for a Nb/a-Si/Nb junction.

It should be mentioned that due to the profound influence of NbN quality on junction characteristics, all incoming NbN films are routinely subjected to reflectivity measurements and X-ray diffraction. The reflectivity at $\lambda = 850$ mm is perhaps the best indicator of suitability for device fabrication. Films with reflectivity, $R > 80\%$ yield good devices, although the very best devices occur for $R \gtrsim 85\%$. It is not yet clear what the cause of this relationship is. Certainly high reflectivity films could simply be smoother, but *very* low reflectivity is clearly associated with poor stoichiometry, as evidenced by the appearance of Nb_2N or other phases in the X-ray diffraction results. Thus loss of reflectivity could signal slight changes in stoichiometry in the film. This problem is certainly worthy of further study.

SECTION 3

ALL-NIOBIUM NITRIDE DEVICES

A major problem with extending the work done on NbN/Nb devices to all-NbN is that NbN cannot be anodized cleanly past ~ 5 volts. Anodization to higher voltages results in a gradual roughening of the surface accompanied by an increasing haziness in the interference colors. Experiments have been done using different anodization rates, temperatures and solutions with no significant improvement. As an alternative, thermal oxidation has been developed as an isolation process. A 30 minute oxidation at 400°C in dry O_2 is sufficient to convert 40 nm of NbN to 120 nm of $NbNO_x$. The oxidation slows once the a-Si layer is reached. This is consistent with our optical result that the a-Si barrier forms only 0.3 nm of oxide upon exposure to air.[14] Most samples oxidized using this procedure form smooth oxide surfaces that are comparable to the Nb_2O_5 formed by anodizing niobium. The use of thermal oxidation requires an SiO_2 mask instead of the photoresist mask commonly used for Nb SNAP devices. Resolution of small devices (to 2 μm) using the SiO_2 mask is not a problem. The effect of the 400°C temperature upon the a-Si (or composite) barrier and/or the NbN/a-Si interface is not known at this time.

The first reasonably successful wafer completed using this process was run 1/15/82A. The films used were NN 205/NN 217 for the lower/upper electrodes, respectively. The barrier was formed by a 40 second deposition of a-Si. NN 217 was deposited at full heater power and 1500 W rf power at NRL. The resultant junctions were of high current density, ~ 5000 A/cm^2, with fully modulable Josephson current. They had a small amount of hysteresis and sometimes some gap structure was visible at ~ 3.0 mV. The device character was not, however, the desired S-I-S. The fact that the critical current of these devices scaled with area, and was fully modulable indicate that the thermal oxidation process is capable of successfully isolating

Josephson junctions without inducing nonuniformities or significant edge effects.

Two recent wafers, 6/18/82I and J, were completed using 45 second a-Si barriers and NN 241 as a counterelectrode. The base electrodes were NN 205 and NN 223 respectively. NN 223 is not a very good sample, with reflectivity at λ = 850 nm of R = 75%. The resultant devices are all shorts. NN 205 has R = 89%. The resultant devices have a definite S-I-S character, with fully modulable supercurrent, although the supercurrent density is rather high, $\gtrsim$ 2000 A/cm^2, and V_g = 2.6 mV (see Fig. 3). The yield of good devices was only fair, mostly due to shorts through the thermal oxide. This problem is being resolved by a revision to the contact niobium mask that reduces the size of the contact pads, thus decreasing the probability of encountering a defect.

The upper electrode, NN 241, is a film deposited at ambient temperature, and is actually a niobium carbonitride, NbC_xN_y (discussed in the next section). These results represent the best all-NbN devices produced to date. The fact that they are S-I-S is very important, since tunnel junctions are well understood, and easily compared.

A more recent attempt, using NN 226/NN 272 and a 43 second a-Si barrier yielded shorts. NN 226 has R = 75% at λ = 850 nm, so it can be surmised that the NbN quality was insufficient to yield good devices.

Since these all-NbN devices are contacted by a Nb film, it is not possible to get good device measurements at T > 9K. Such measurements would be desirable in order to fully evaluate the devices, and the technological importance of these devices lies at T $\lesssim$ 10K. New masks have been designed and ordered that will allow the use of an SiO_2 insulator layer under a NbN contact layer. The SiO_2 is required as an etch stop for plasma etching of NbN (it is not required for the presently used wet etch of Nb). In addition, the SiO_2 will help eliminate any shorting through the

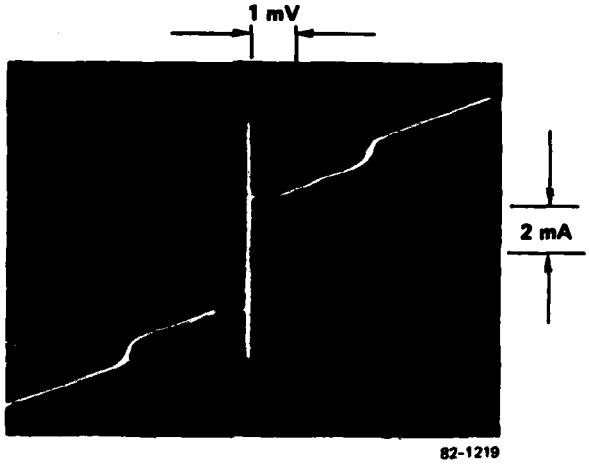

FIG. 3 The I-V characteristic for a NbN/αSi/NbN junction fabricated using the thermal oxidation variant of SNAP.

thermal oxide. An important result that may be gleaned from using NbN as the contact layer will be from high temperature annealing experiments. If the NbN/a-Si/NbN junctions are stable under annealing to T > 400°C it can be reasonably inferred that the thermal oxidation step has little or no effect on junction characteristics. If the junctions are unstable, another barrier may be required.

SECTION 4

NIOBIUM NITRIDE MATERIAL

During the course of this project the niobium nitride material has been sputtered at NRL by E. Cukauskas onto 2" diameter wafers supplied by SRC. Except for occasional equipment failures, this material has been quite good, and has permitted excellent progress to be made in this work. However, continuing device work is focusing more on all-NbN structures, and it has become apparent that the time required to fabricate devices is too long, with three round trips required for all-NbN devices fabricated using NbN wiring. In addition wafers are subject to loss, breakage, contamination and aging effects in the mail. Thus, for continued progress an in-house source of NbN films is mandatory. In May, 1982, an existing UHV system was reconfigured to produce high-quality NbN films. Before relating our results using this system, E. Cukauskas's results will be summarized, since our work builds upon his experience base.

The NbN films produced at NRL for the earlier portion of this work (roughly through May 1982) were deposited onto heated (~ 600°C) substrates. These films have been fully characterized using T_c, X-ray diffraction and auger spectroscopy.[15,16] In addition, SRC has characterized these films in terms of their optical reflectivity, vis-a-vis the device quality.[3] In May 1982 Cucauskas's UHV system developed a water leak with the substrate heater turned on. Due to this occurrence he discovered that good films could be made with ambient temperature deposition as long as sufficient methane was added to the sputtering gas mixture. Using this approach, he has produced films of NbC_xN_y with T_c as high as 15.8K. During the period when he was determining the optimum sputtering parameters for these films SRC assisted by providing X-ray diffraction and reflectivity measurements. This work will be published soon.[17] Of interest to our contract work is the reflectivity of these films. This is shown in Fig. 4 for a number of

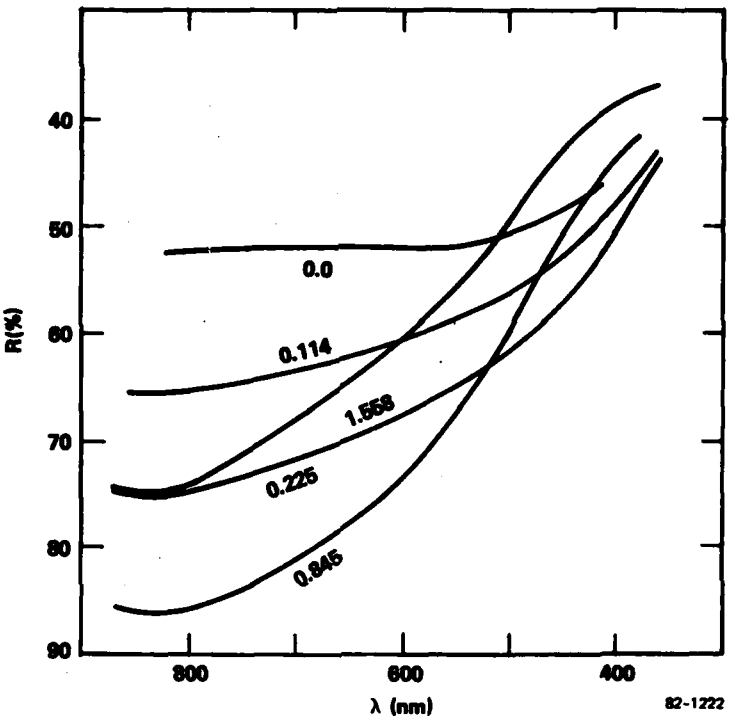

FIG. 4 The reflectivity of various NbC_xN_y films as a function of wavelength. The maximum reflectivity corresponds to the highest T_c and generally the best device results.

films of varying carbon content. There is a strong correlation between high reflectivity and T_c, with one of the highest T_c films, 15.85 K having R = 88%. It is not yet definite that high R corresponds to good device quality for NbC_xN_y, as it certainly does for NbN (high substrate temperature). However, as discussed in Section 3, device 1/15/82A with NN 241 (ambient) counterelectrode resulted in the best all-NbN devices to date, and for NN 241 R = 83%. Note that counterelectrode films, such as NN 241 are typically about 300 Å thick, and typically do not produce quite as high reflectivity as the 3000 Å films that are usually deposited.

With the above results in mind, it was decided to try to emulate Cukauskas's ambient temperature results with our system. This system (Fig. 5) is a totally dry pumped system consisting of a carbon vane mechanical pump coupled with two LN_2 sorption pumps for roughing purposes. The 18-inch stainless steel bell jar has ten 25 liter/sec ion pumps and one 8-inch cryopump for its main pumping complement, and typically achieves a base pressure of 5×10^{-8} torr. An rf diode sputtering head is fitted with a single 8-inch niobium target and the substrates are placed on a "J" arm table with a 600°C heating capability. This capability has not been significantly exercised due to Cukauskas's impressive ambient temperature results. System monitoring is accomplished with a wide range ionization gauge, capacitance manometer, and a differentially pumped residual gas analyzer.

Several runs have been completed in this system. After some initial teething pains several good films have been produced. These results are summarized in Table 1. It is encouraging that the reflectivity data on our films, as shown in Fig. 6, also tracks the T_c and carbon content. This is qualitatively similar to Cukauskas's results shown in Fig. 4.

The X-ray results on Cukauskas's films typically have a ratio of 111:200 peak heights that is >> 1 for low carbon films, << 1 for optimal films and ~ 1 for high carbon films. Our films typically have a very strong 111 orientation, both with and without a small 200 peak. There is no systematic

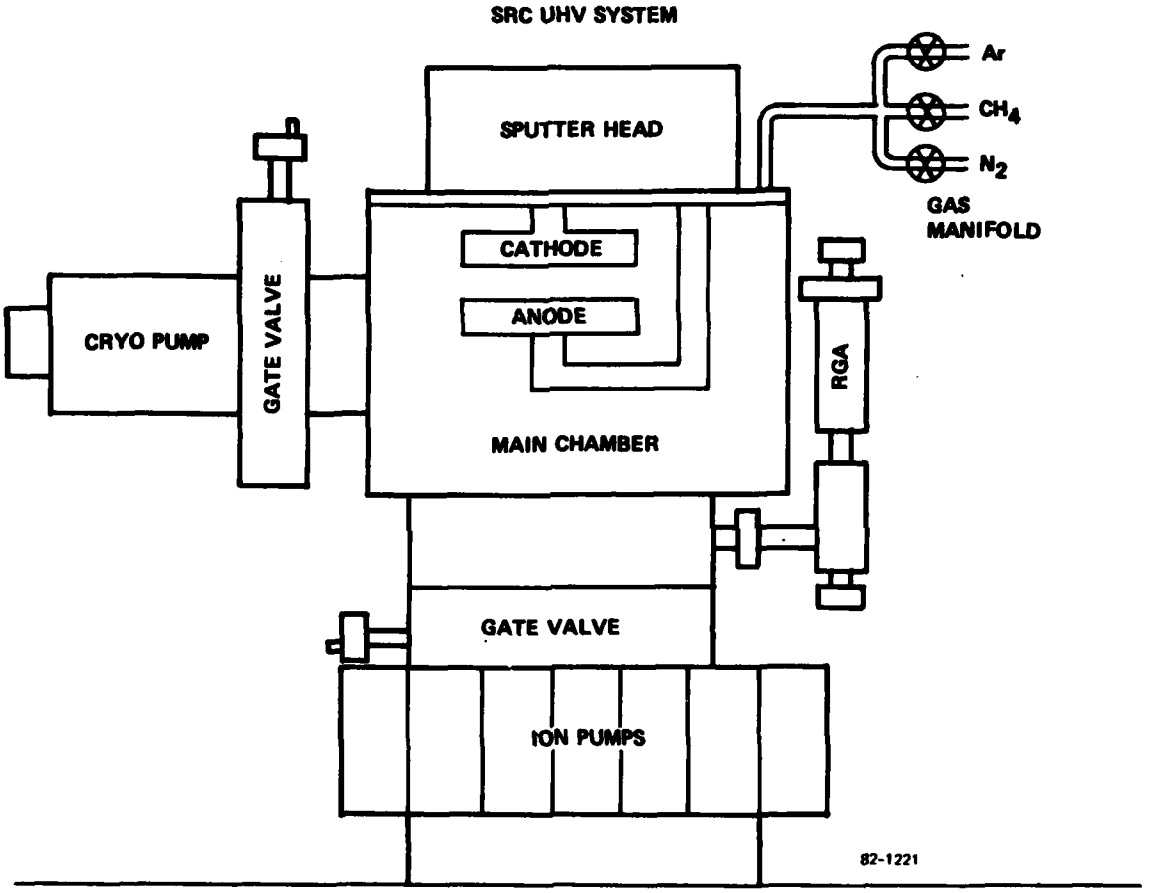

FIG. 5 A schematic drawing of the SRC UHV system used to produce NbC_xN_y films. The highest T_c films produced to date are 15.1 K.

TABLE I

Essential data on recent SRC NbC_xN_y films
The $CH_4 + N_2$ pressure is maintained at 1.0 μ for these runs and the total gas pressure is 10.0 μ. The 200 peak in parenthesis indicates it is much smaller than the 111 peak. Sputtering power is 500 W in an RF diode configuration.

NbN RUN	CH_4/N_2 RATIO	T_c(K)	X-RAY PEAKS	R(%) AT 800 nm
6	0	10.1	111	51
10	.1	13.9	111 & (200)	63
7	.2	14.6	111	64
8	.4	15.1	111 & (200)	70
11	.6	14.4	111 & (200)	76
9	.8	14.6	111 & (200)	71

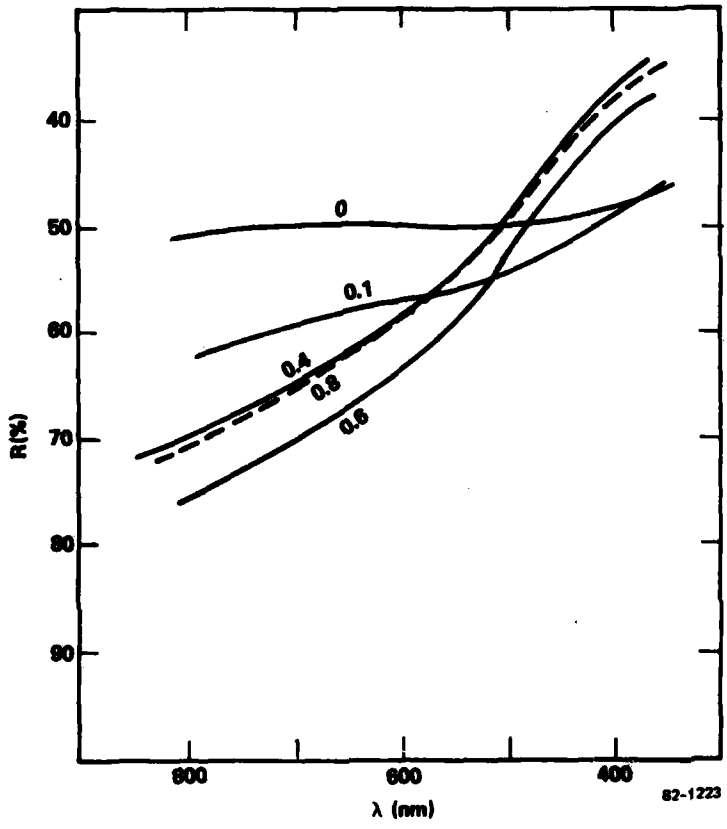

FIG. 6 The reflectivity of a series of SRC NbC_xN_y films of varying carbon content. The results are qualitatively the same as NRL's, shown in Fig. 4.

variation with carbon content. The significance of these X-ray results is not known, but they are certainly useful in determining if pathological films have been produced. The fact that we do not observe any extraneous peaks is encouraging.

a-Si barrier devices were fabricated on our NbN #7 and #8. The #7 results were nontunneling Josephson junctions. #8 resulted in poor quality devices, but definitely S-I-S. It appears that again the reflectivity is a good indicator of device quality, since #7 has $R \tilde{=} 64\%$ and #8 has $R \tilde{=} 71\%$. (Recall that $R > 80\%$ is our general criterion for quality junctions.) Our more recent higher quality films have not yet been fabricated into devices.

Presently, several modifications are being made to the SRC system such as the addition of precision needle valve and flowmeter assemblies to allow more precise flow control of the gas ratios and more accurate reproduction of run flow conditions. Once the installation of this equipment is completed, attempts will be made to vary the gas ratios and partial pressures to obtain more optimum NbC_xN_y films with higher T_c and especially better reflectivity.

SECTION 5

S-I-S MIXER

Since the ultimate goal of this program is to develop S-I-S mm-wave mixers and detectors it is appropriate to initiate work on design and evaluation of mm-wave devices fabricated using SRC's SNAP technology. Given the developmental nature of the NbN/Nb and all-NbN devices, the best initial candidate for S-I-S mixers is the all-Nb device using the composite barrier. These devices have been demonstrated in digital circuits,[7] thus mixer fabrication requires only a new design using established design rules, and appropriate circuit and device parameters. The similarities between NbN and Nb are enough that essentially the same circuit fabrication can be carried over to NbN once device development has progressed sufficiently far to justify NbN mm-wave circuit fabrication.

Given the specialized nature of mm-wave design and evaluation, it was decided to collaborate with a group having expertise in this area, but perhaps lacking in fabrication facilities. This congruence of goals led us to initiate a collaborative effort with the Goddard Institute for Space Studies (GISS).

It was determined, due to its low dielectric constant and low loss, that quartz is the preferred substrate material for mm wave mixers. Two-inch diameter quartz wafers were obtained and processed into Nb SNAP devices, verifying that these substrates were suitable for SNAP device fabrication. GISS uses mixer chips of dimension 5 x 10 x 5 mil, bonding or soldering them to a larger chip containing the required choke structures. Thus, tests were conducted in which the 2" diameter quartz wafers were coated with Nb/Au and sawn into a 5 x 10 mil grid using a 5 mil deep sawcut (the wafers are 20 mil thick). The wafers were then backlapped at GISS to 5 mil, thus separating the individual chips. Soldering tests were conducted by GISS to determine an appropriate solder and find the limits of

resolderability. The above work has successfully determined the feasibility of the desired device mounting procedure.

Using SRC's measured values of capacitance and inductance, plus the various design rules and tolerances required for digital circuit fabrication, a set of S-I-S mixer designs were evolved in collaboration with GISS. Since there is some uncertainty, not only in the device parameter values, but also in the exact requirements for a good S-I-S mixer, a total of 14 different designs were finalized. These consist of 1, 2, 4 and 8 junction series arrays using junctions of various diameters. The bonding pads are tapered to minimize inductance without adding unduly to the parasitic capacitance. The resulting design is denoted the SR 8102. The SR 8102 also includes numerous devices and test structures to measure junction characteristics, capacitance, uniformity and contact resistance, among other parameters of importance.

The digitization and production of the SR 8102 took several months due to problems encountered in formatting and in actual mask production. A usable mask set was received in May 1982 and fabrication was initiated. The quartz wafer failed due to a very dirty surface. The dirt was only revealed by spinning on photoresist for the first patterning step, whereupon the dirt particles cause "wakes" to appear in the resist. The standard Si wafer cleaning process has subsequently been replaced by a more stringent scrubbing method for the quartz. Two other Si wafers being processed with the quartz wafer were completed. However, they encountered severe undercutting during the trilayer etch and the SiO_2 via etch due to poor humidity control in the photoresist room. The net result was that a significant percentage of devices are shorted. Temperature and humidity recorders have subsequently been placed in all processing areas to warn of potential problems. Figure 7 shows a SEM micrograph of a mixer device fabricated in the initial run. This shows the basic integrity of the process. Barring major equipment failure, it is expected that successful SR 8102 chips will be completed shortly.

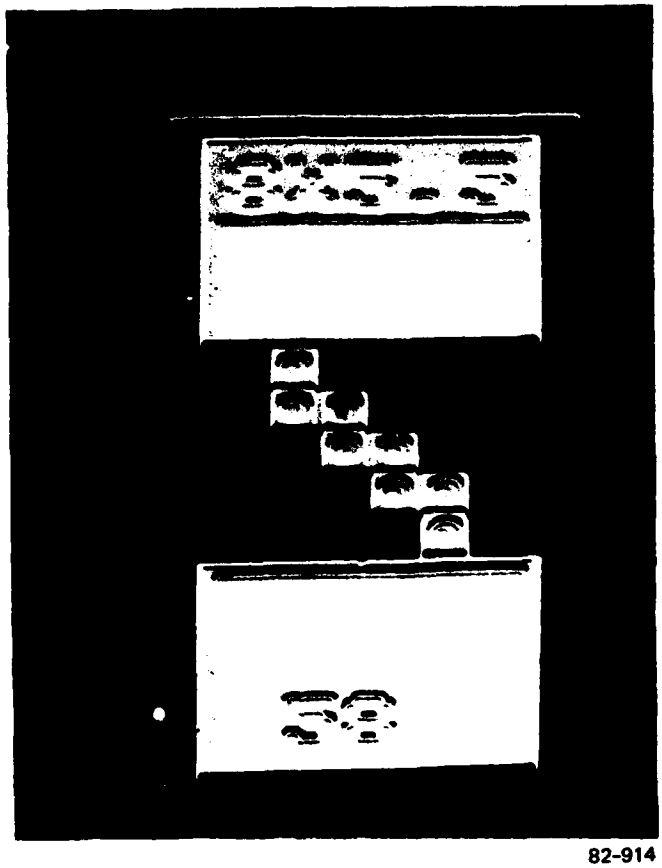

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FIG. 7 SEM micrograph of a four-junction S-I-S mm-wave detector array fabricated using SNAP. Junction diameter is 4 μm.

SECTION 6
CONCLUSIONS

The a-Si composite barrier yields excellent NbN/Nb junctions. It is expected that further refinement of these devices will shortly yield junctions of suitable quality for mm-wave applications in the quantum regime. This barrier is also the prime candidate for all-NbN junction fabrication. In this case, there are two important questions to answer: (1) The effect of depositing NbN as a counterelectrode and (2) the effect of the 400°C oxidation process used in SNAP. A collaborative experiment with NRL comparing the NRL mesa-etch process with the thermal oxidation SNAP should answer the latter question. The previously mentioned annealing experiments that will be undertaken also bear on this problem. Future fabrications using NbN deposition variations, such as rf and dc magnetron, different sputtering pressure, etc. will address the former question.

The CVD n-Ge barrier is a candidate for further exploration. Early experiments gave potentially promising results[1] given the fact that poor quality NbN films were used. Given that the CVD process takes place at 380°C, the thermal oxidation step at 400°C is not expected to be a problem. Modern low pressure CVD apparatus holds the promise for production of extremely uniform and well characterized barriers.

A major impediment to progress in making all-NbN junctions has been the time consumed by shipping wafers between SRC and NRL. The potential for contamination and breakage is also a problem. The promising results of SRC's new in-house NbN materials effort indicate that this problem may soon be resolved. Full material and device evaluation will be necessary before using SRC NbN as the major device constituent.

It is anticipated that all-Nb mm-wave mixer chips will be

delivered to GISS in the near future. Evaluation of these chips will determine the direction of this aspect of the program. Continuing progress being made at SRC on all-Nb junctions bodes well for the eventual success of the mm-wave mixers. NbN/Nb and all-NbN devices will be incorporated into mm-wave mixers as soon as the device characteristics are developed to sufficient quality.

SECTION 7

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APPENDIX A

Niobium nitride-niobium Josephson tunnel junctions with sputtered amorphous silicon barriers

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Niobium nitride-niobium Josephson tunnel junctions with sputtered amorphous silicon barriers (NbN-αSi-Nb) have been prepared using processing that is fully compatible with integrated circuit fabrication. These junctions are of suitable quality and uniformity for digital circuit and *S-I-S* detector applications. The junction quality depends critically upon the properties of the NbN surface, and seems to correlate well with the UV/visible reflectivity of this surface.

PACS numbers: 74.50. + r, 68.48. + f, 85.25. + k

The development of Josephson tunnel junctions which incorporate materials with transition temperatures $T_c > 10$ K is technologically important, because they can be cooled with small, closed-cycle refrigeration systems which are relatively compact, reliable, and economical. The possibility of using such coolers would greatly expedite the nonlaboratory use of Josephson devices and circuits in such applications as magnetometry, *A/D* conversion, digital signal processing, and high-frequency mixing and detection.

Previous work with these materials has, in most cases, employed a mechanically soft, low T_c material such as lead or lead alloy as a counterelectrode.[1-5] The only reported experiments in which *both* electrodes were refractory and high T_c are the work by Shinoki *et al.*[6] on NbN-SiO_x-NbN and that of Tarutani on V_3Ga-SiO_x-Mo_3Re_2.[7]

We report here work on tunnel junctions consisting of a NbN base electrode, a sputtered amorphous silicon barrier, and a Nb counterelectrode. The processing employed is fully compatible with integrated circuit fabrication. While the Nb counterelectrode $T_c \approx 9.2$ K does not quite qualify as a high T_c material, it is refractory and very rugged, and the devices made from such films are expected to be very reliable. Furthermore, the use of the sputtered amorphous silicon tunneling barrier and the Nb counterelectrode allows direct comparison with Nb-Si-Nb junctions which have very reproducible characteristics. Both the NbN/Nb and Nb/Nb structures are prepared by the selective niobium anodization process (SNAP).[8] In SNAP, the entire "trilayer" of superconductor-barrier-Nb is formed before any device patterning is performed. The inherent cleanliness of this process should minimize and, hopefully, eliminate accidental processing artifacts from influencing the comparison.

Devices are fabricated on 5-cm-diam silicon wafers cleaned by a standard semiconductor process followed by thermal oxidation. The niobium nitride base electrodes are deposited at the Naval Research Laboratory (NRL) onto heated substrates by reactive rf sputtering in an oil-free ultrahigh vacuum system.[9] The substrates and substrate holder are baked out at a temperature of 700 °C during a 15-min presputtering of the niobium target in an argon atmosphere. The sputtering gases of argon and nitrogen are mixed in an appendage mixing chamber and allowed to flow through a metering valve into the system which is pumped by a throttled cyropump. After an equilibrium flow is achieved, the substrates are rotated under the target and the deposition is carried out at a power density of 8 W/cm^2, corresponding to a deposition rate of approximately 10 nm/min. The films are deposited to a typical thickness of 150–300 nm and have

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transition temperatures ranging from 12 to 16 K. The dependence of the transition temperature, crystalline structure, and composition of the deposited film upon the sputtering parameters and system contamination have been previously reported.[10]

The silicon barrier and Nb counterelectrode depositions are done at Sperry Research Center (SRC), using the same techniques as previously described for all-Nb SNAP devices[8] with three exceptions. Since the NbN lower electrode and αSi barrier are deposited in different laboratories in different vacuum systems, oxides and other surface contamination will have accumulated on the surface during its exposure to the atmosphere. Therefore, a light *in situ* sputter etch is carried out prior to the αSi barrier deposition. This removes about 15 nm from the top of the NbN film. Another change from the previously described process is that the Si is sputtered in pure argon without any hydrogen in the sputtering gas. This modification had previously been incorporated into the fabrication procedure for all-Nb devices at SRC in order to simplify the process. Finally, the barriers are only about 2/3 of the thickness used for all-Nb devices to achieve similar current density.

The junctions are isolated using the selective niobium anodization process. This process has been previously described.[8] Briefly, anodization is used to convert the niobium counterelectrode completely into Nb_2O_5 everywhere except where it is desired to isolate a junction. A layer of Nb is then deposited and patterned to contact the counterelectrode. No problems have been encountered when using this process with a NbN lower electrode.

Device measurements were made in a *mu*-metal-shielded cryostat that inserts into the helium storage dewar. The temperature is measured with a calibrated Cryocal germanium thermometer to within 0.1 K.

The T_c of the NbN-base electrode is usually determined from a companion film deposited on a quartz control chip placed in the system alongside the silicon wafer. However, discrepancies between the T_c of the control chip and the T_c of the NbN film on the completed devices have sometimes been noted. This is being investigated to determine if there is any dependence of T_c or other film parameters on the substrate type. NbN films have been characterized by their reflectivity in the UV/visible region of the spectrum using a Beckman UV 5270 spectrophotometer and by x-ray diffraction. The x-ray diffraction data yield information about the structure of the entire NbN layer while the UV/visible reflectivity measurements probe only several nanometers below the surface of the film, which is comparable to the superconducting coherence length in NbN. Thus, the reflectivity measurements and the tunneling characteristics of the completed devices probe roughly the same depth into these films.

Figure 1 (a) displays an I-V curve for one of our best NbN-αSi-Nb devices, and in (b) an I-V curve for a Nb-αSi-Nb device of comparable critical current density. The barriers were not done in the same deposition, since this results in vastly different current densities, with the NbN devices having a current density roughly two orders of magnitude smaller. We tentatively attribute this to a higher Schottky-barrier height for the NbN-Si interface than for the Nb-Si interface.

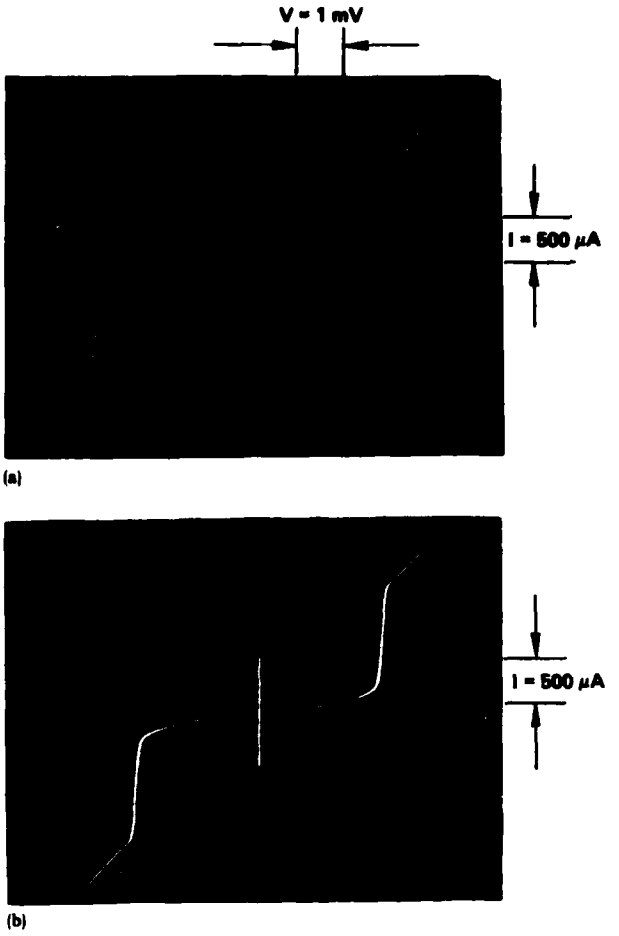

FIG. 1. (a) I-V curve for a NbN-αSi-Nb device at 4.2 K. The critical current density J_c is 500 A/cm^2. (b) A comparable Nb-αSi-Nb device with J_c = 250 A/cm^2.

Properties of these two junction types are shown in Table I. The quantity t is the barrier thickness required to produce junctions with current densities of ~ 100–1000 A/cm^2. V_g is the observed sum of the energy gaps at 4.2 K. The subgap resistance measured at 1.5 mV times the critical current is denoted by V_m and is a general indicator of the junction's suitability for digital applications. Higher values of V_m allow more current to be switched out of the junction into the load. I_cR is another common indicator of junction quality. The capacitance per unit area C/A determines the response time of the junction for both digital and mm-wave applications. The value of 0.04 pF/μm^2 is comparable to lead alloy junctions,[11] and at 1000 A/cm^2 yields an RC time of $\approx$5 ps. The NbN capacitance correlates well with the reduced barrier thickness of these junctions compared with the all-Nb junctions, for which the capacitance was measured from both Fiske and superconducting quantum interference device resonances. ΔV_g is a rough indication of the voltage width of the current rise at the gap voltage. A small ΔV_g is important for S-I-S mm-wave detection in the quantum limit, which requires $\Delta V_g < hf/e$, where h is Planck's constant, e is the electronic charge, and f is the mm-wave frequency. A ΔV_g value of 0.5 mV implies that quantum operation of these

TABLE I. A comparison of junction properties for NbN vs Nb lower electrode devices.

	t	V_g	V_m @ 1.5 mV	I_cR	C/A	ΔV_g
Nb	6–7 nm	2.8 mV	9–11 mV	1.3 mV	~0.025 pF/μm^2	0.15–0.20 mV
NbN	4–5 nm	<3.5 mV	15–22 mV	1–1.3 mV	~0.04 pF/μm^2	>0.5 mV

devices is achieved at frequencies greater than 120 GHz.

The dependence of the maximum Josephson current on magnetic field in the absence of stray trapped magnetic flux is the expected Fraunhofer diffraction pattern which indicates that the tunneling current is uniform across the junction. These junctions tend to trap flux more easily than all-Nb junctions of the same geometry. Our all-Nb devices can be cooled to liquid helium temperature and measured with little or no problem from flux trapping, while the NbN devices may have to be heated above T_c and cooled several times before a maximum value of critical current that modulates as $|(\sin x)/x|$ can be obtained. This problem may be attributable to the large London penetration depth in NbN, about 200 nm, which is comparable to the film thickness.[12] In the case of the Nb films, the penetration depth is only 80 nm which is considerably smaller than the film thicknesses used. Junctions made using a thicker NbN lower electrode are better in this regard, but still not as good as all-Nb junctions.

The all-Nb junctions fabricated at SRC are very reproducible. The NbN-based junctions are not yet as reproducible, and some runs have yielded junctions of much poorer quality than indicated in Table I. There appears to be a correlation between device quality and the crystallographic phases and/or surface condition of the lower electrode. UV/visible reflectivity measurements and x-ray diffraction measurements have been used to classify the NbN films used for the base electrode.

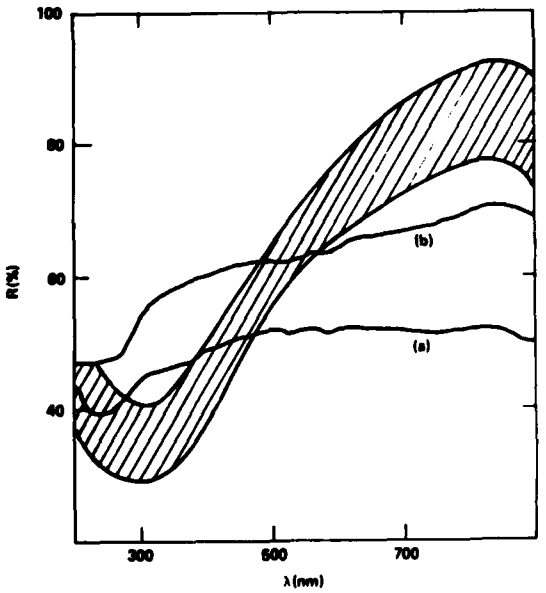

FIG. 2. Shaded region shows the reflectivity vs wavelength seen on NbN films that have yielded good tunnel junctions. The two solid curves, (a) and (b), show R vs λ for two films that exhibited non-NbN phases, and yielded poor quality devices.

Figure 2 displays the reflectivity measurements made on a number of NbN films which were the base electrodes for tunnel devices of varying quality. Films whose reflectivity data fell in the grey shaded area yielded devices of the quality indicated in Table I. Curve (a) is the data for a film that exhibited a broad (10–16 K) superconducting transition and evidence of Nb crystalline structure. The I-V curves of the completed devices were linear with no critical current. Curve (b) corresponds to a film with a Nb_2N phase and a 6-K transition temperature. Devices made from this film were nonhysteretic without any pronounced gap structure.

The x-ray diffraction data indicate that good tunnel junctions can be fabricated on films that exhibit NbN (111) and/or NbN (200) peaks, or on fine grain structure films which did not yield any crystalline peaks. Films that exhibit other phases besides NbN do not yield good junctions. Films that exhibit acceptable x-ray diffraction results do not always yield good tunnel junctions. If these films also show low reflectivity and low T_c ($\lesssim$ 15 K) then poor quality devices will be obtained. Work is proceeding in the hope of quantifying the relationship between junction quality and reflectivity, and in understanding the physics of these devices.

In conclusion, Nb-αSi-Nb tunnel junctions of quality suitable for digital and S-I-S detector applications have been fabricated using processing that is suitable for integrated circuit fabrication. Comparison of these devices with all-Nb devices made using the same barrier, counterelectrode, and processing procedures indicates that the NbN-αSi interface probably results in a higher tunneling barrier than Nb-αSi. It was also found that the crystallographic phase, reflectivity, and transition temperature are indicators of the quality of the junctions that can be fabricated from a given film. In particular, the reflectivity is the best indicator, and films whose reflectivity falls outside the shaded area in Fig. 2 invariably yield poorer quality junctions.

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APPENDIX B

NbN-p^+ Ge Super-Schottky Diodes

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SECTION 1
INTRODUCTION

A super-Schottky diode is formed by contacting a degenerately doped semiconductor with a superconductor. The low voltage electrical characteristics are identical to those of a superconductor-insulator-normal metal (S-I-N) tunnel junction, which reflects the quasiparticle density of states in the superconductor. The tunnel barrier I is the Schottky barrier, which is formed by a depletion layer induced on the surface of the semiconductor by the presence of the superconductor. At higher voltages and/or at higher temperatures, the electrical characteristics of the device should conform to those of a conventional Schottky barrier diode, in which the nonohmic behavior results from the voltage dependence of the barrier shape. Conventional Schottky diodes have been studied intensively [1] and their I-V characteristic in the direction of forward bias is described quite well at noncryogenic temperatures by the exponential form

$$I = I_s(T) \quad \exp(eV/kT) - 1 \quad , \qquad (1)$$

where $I_s(T)$ is a characteristic of the diode, e is the electronic charge, k is Boltzmann's constant, and T is the temperature. At noncryogenic temperatures and for voltages on the order of 0.1V or larger ($eV/kT \gg 1$) the exponential dominates and a plot of ℓn I vs. V yields a straight line. The case of super-Schottky tunneling is theoretically identical to the case of tunneling between a superconductor and a normal metal through an insulating barrier. The distinguishing feature in the case of a super-Schottky diode is that the layer corresponding to the normal metal is a degenerate semiconductor, and the insulating barrier is formed by the depletion layer induced in that semiconductor. Analysis of S-I-N devices and super-Schottky diodes at low temperatures yields the same functional dependence as in eqn. (1) [2].

Previous work on super-Schottky diodes includes Pb on p - GaAs [3].

Pb on p^+Si [4] and Nb on p-GaAs [5]. Much of this work was aimed at exploring these devices for use as mm-wave detectors. The limiting factor for microwave application of super-Schottkys has been the extra series impedance of the device due to spreading resistance in the semiconductor side of the diode. This resistance contributes to the RC time constant of the diode, thus limiting its high frequency response. The use of either arrays of diodes [6] or thin semiconductor layers [4] has been proposed to minimize this effect. In the work reported here, use was made of the thinnest possible semiconductor layers consistent with Schottky-type device characteristics. Superconductor-insulator-superconductor junctions with their even higher degree of nonlinearity, and operating in the quantum limited detection mode, may be preferable for high frequency mixing due to their greater sensitivity [7]. For applications where the sensitivity is not so important, the super-Schottky or S-I-N device may have an advantage due to the absence of Josephson currents which limit the operating bias range of the device and contribute to the noise.

The work reported here is an offshoot of an attempt to make NbN-Ge-Nb Josephson tunnel junctions using chemical vapor deposited (CVD) Ge or Si as tunneling barriers. Recently, evaporated Si on Nb_3Sn and V_3Si [8,9], and sputtered Si on Nb [10] have been used as tunnel barriers in Josephson junctions. NbN, (and presumably also the A15 compounds) because of its lower reactivity with Si than Nb, permits barrier formation of Si or Ge, by either glow-discharge deposition at substrate temperatures $\simeq$ 300°C [11,12] or by chemical vapor deposition (CVD) at substrate temperatures $\lesssim$ 700°C [13]. The glow-discharge production of Si results in amorphous barriers; the CVD deposition of Si or Ge onto NbN results in polycrystalline layers at temperatures well below those required to produce polycrystalline layers on SiO_2 substrates [14].

The use of crystalline rather than amorphous barriers poses both potential advantages and disadvantages compared to alternate fabrication techniques for both super-Schottky and Josephson devices. Compared to

amorphous barriers [8-12], crystalline barriers offer the potential for greater control of doping and greater understanding. Compared to bulk single crystal barriers, the CVD barriers offer lower series resistance; compared to membrane devices [4], the CVD barriers offer greater mechanical strength. On the other hand, the polycrystalline CVD barriers may be less uniform in thickness than both amorphous or single crystal membrane barriers because of finite crystallite size. While the poorer uniformity may be critical in Josephson devices, this may be of less consequence in super-Schottky devices, as long as the Schottky depletion width is everywhere less than the total CVD layer thickness. In such a case, the variable layer thickness may contribute only to a variable parasitic series resistance rather than to a variable tunnel impedance.

Our devices, with Ge p^+ barrier thicknesses in the range of 30-60 nm, showed good Schottky-like behavior and could be produced with fairly good reproducibility, uniformity and yield. It was found that for barriers thinner than ~ 30 nm the devices have Josephson coupling between the electrodes, but poor tunneling characteristics. For barriers in the 30-60 nm range, the Josephson coupling is suppressed, and the resulting devices appear to be NbN-Ge super-Schottky diodes, where the Ge-Nb contact has comparatively much lower resistance. Hence the structure is essentially that of an S-I-N-S tunnel junction with a thick N layer.

SECTION 2
FABRICATION

Fabrication of our super-Schottky devices is similar to the previously described fabrication of NbN-aSi-Nb Josephson devices [15] with the exception that the Ge barrier is deposited using low temperature CVD instead of sputtering, as in the case of the a-Si barrier.

The lower electrode is niobium nitride deposited at the Naval Research Laboratory NRL [10] at a rate of 0.2 - 0.3 nm/sec in an oil-free ultra-high vacuum system by reactive rf sputtering onto heated 5 cm diameter silicon wafers. The films are deposited to a thickness of 150 nm and have transition temperatures in the range from 15-16 K. The dependence of the transition temperature, composition and crystalline structure of the deposited film upon tne sputtering parameters and system contamination has been reported [17].

The Ge barrier and Nb counterelectrode were deposited at Sperry Research Center (SRC). Since the NbN lower electrode and the Ge barrier are deposited in different laboratories, various techniques were used to ensure a clean NbN surface prior to deposition of the Ge. Initially either a light sputter etch or a 20 sec. dip in buffered HF is performed immediately prior to inserting the wafers into the standard pressure, cool wall CVD reactor. The wafers are then heated to 600°C in an atmosphere of NH_3/Ar to effect further cleaning. This is followed by an Ar flush while the temperature is dropped to 380°C. Upon achieving a stable temperature germane and diborane gases are introduced and the barrier is grown at a rate of about 7-8 Å/sec. Varying the flow of diborane yields different doping densities.

The volume concentrations of germane and diborane were 8×10^{-3} and $1 - 2 \times 10^{-4}$, respectively in a carrier gas which was 1/3 Ar and 2/3 N_2.

Growth rates were observed to accelerate after about one minute even though flow rate and temperature were controlled. The barrier layers were observed to be highly specular reflecting. Thicker layers (~ 1000 Å - 2000 Å) which were used to study material properties had a slight hazy appearance, presumably because of increased grain size [18]. The growth rate of the germanium layers was slightly increased by the addition of diborane. Incidentally, introduction of phosphine to produce n-type layers results in substantially lower growth rates at degenerate doping levels; a similar observation on the growth rates of phosphorous-doped a-Si has been observed by Taniguichi, Osaka and Huose [19].

X-ray diffraction showed that the thicker layers were polycrystalline with a <111> preferred orientation. Room temperature resistivity of the p^+ Ge layers was ~ 10^{-3} Ω-cm. As shown in Fig. 1, the conductivity of the films initially increases in cooling below room temperature as would be expected for crystalline, but not amorphous, material. The films remain conducting at 4.2 K indicating degenerate doping. The resistivity of these heavily doped germanium layers is within a factor of three of that which one would expect for epitaxial single-crystal germanium of comparable doping under the assumption that boron atoms are introduced into the layer in proportion to the concentration of GeH_4 introduced into the reactor. Reflectivities of the layers were measured in the infrared. The plasma resonances were relatively washed-out compared to that of single crystal germanium. The wavelength of the observed minimum reflectivity corresponded to a boron doping density [20] in the range of $5 - 8 \times 10^{19}$ cm^{-3}, a value somewhat higher than inferred by conductivity measurements.

Following the barrier deposition the wafers are immediately placed in a Perkin-Elmer 2400 8SA sputtering system and a niobium counter-electrode ~ 30 nm thick is deposited using high rate magnetron sputtering. The resulting NbN-Ge-Nb "trilayer" is then patterned using the Selective Niobium Anodization Process (SNAP) [10]. This process consists of

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FIG. 1 The conductivity of a thick p^+ Ge film as a function of temperature.

completely anodizing through the Nb counterelectrode except where it is desired to isolate a junction. Junction areas are protected from anodization by a photoresist stencil. Anodization and resist stripping is followed by deposition and patterning of a niobium wiring layer about 300 nm thick.

SECTION 3

RESULTS

Three different super-Schottky wafers were processed and evaluated in the course of this work. The barrier characteristics for these three samples are summarized in Table I. The Ge thickness is determined by multiple beam interferometry except for sample 4/7/81 which is estimated from the nominal deposition rate and deposition time. X-ray diffraction and results on electrical conductivity as a function of temperature, both done using thicker but similar CVD Ge films, indicate that the material is polycrystalline. The doping is inferred [21] from the resistivity of nominally identical but thicker samples (~ 10 μm), fabricated in a separate deposition, by assuming that the doping level is the same as for a single crystal sample with the same resistivity. The depletion region of a Schottky barrier formed on a degenerately doped semiconductor at low enough temperatures, where the fermi function can be well approximated by a step function, can be considered to be formed of two portions: one of width W where total carrier exhaustion is obtained; and a second where some carriers can partially compensate the ionized acceptors, as shown in Fig. 2. The width W is given by

$$W = \left(\frac{2V_p}{qN\epsilon_s}\right)^{\frac{1}{2}} \left\{\left(\frac{6}{5}\right)^{\frac{1}{2}} - \left(\frac{6}{5} - 2\psi_B\right)^{\frac{1}{2}}\right\}, \qquad (2)$$

where V_p is the Fermi level penetration (potential far from the barrier), ϵ_s the dielectric constant of the semiconductor, N the acceptor density and ψ_B is the barrier height as shown in Fig. 2 [22]. Since the maximum barrier height ψ_B is presumably less than the semiconducting energy gap we take $\psi_B \tilde{\sim} 0.3$ eV for degenerately doped germanium at cryogenic temperatures [23] to obtain the maximum W, shown in Table I. The significance of these values of W is that they are significantly smaller than the

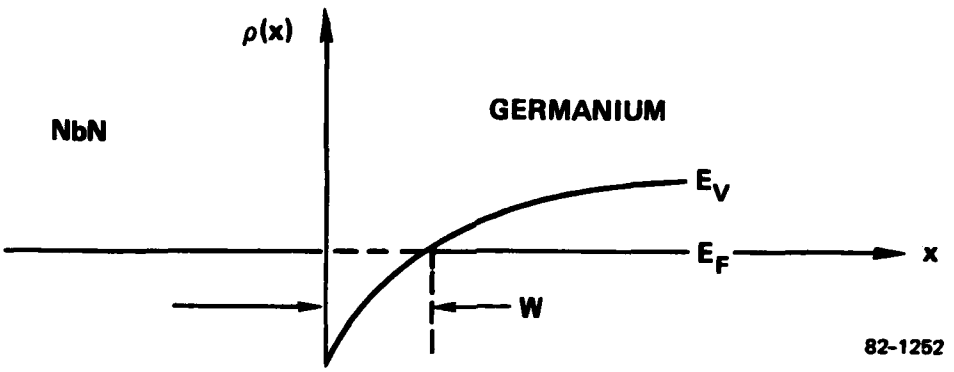

FIG. 2 The assumed band diagram for a NbN-p^+ Ge barrier.

TABLE I

SAMPLE DESIGNATION	NbN DESIGNATION	Ge THICKNESS	DOPING† DENSITY (cm^{-1})	W DEPLETION† WIDTH (nm)	PRECLEAN
4/7/81	156a	60 nm*	2×10^{19}	0.8	Sput Etch
5/4/81 A & B	156b	30 nm	2×10^{19}	0.8	A - HF Dip B - Sput Etch
5/6/81 A & B	158a	33 nm	7×10^{17}	4.0	A - Sput Etch B - HF Dip

* This number is estimated from the deposition rate and time.

† These numbers are inferred from the resistivity of thick samples made in a separate run.

barrier thickness. Thus quasiparticle tunneling between the Ge barrier and the NbN electrode might be expected to be the main conduction mechanism. The observed electrical characteristics of super-Schottky samples 5/6/81 A & B are not completely consistent with the significantly lower doping density inferred from the nominally identical thicker sample. The doping density and depletion width should thus be regarded as only a qualitative guide to the expected device structure and characteristics.

A typical I-V curve for the devices produced in Table I is shown in Figure 3(a), with the corresponding dV/dI vs. V curve shown in Fig. 3(b). The general character of these devices is always super-Schottky. Thinner Ge barrier devices with barrier thicknesses of ~ 20 nm and ~ 14 nm on NN 158 and NN 156 were also fabricated. These devices have large to moderate supercurrent density that modulates in approximately the $|(\sin x)/x|$ Frauenhofer diffraction pattern expected for a uniform Josephson tunnel junction. $I_c R_n$ products of < 0.15 mV are typical. These devices do not have the distinctive S-I-S quasiparticle tunneling characteristic, instead the I-V characteristic is typically nonhysteretic with only a slight hint of structure on the dV/dI curves at 3.0 - 3.5 mV.

The observed conductance per unit area at zero voltage ranges from 2×10^{-5} mhos/μm^2 to 2×10^{-4} mhos/μm^2 for the samples of Table I. The samples subjected to the HF dip prior to barrier deposition have slightly lower conductance than those sputter etched. The samples with the nominally lighter doping density have slightly lower conductance also. This is qualitatively consistent with a super-Schottky tunneling barrier. Note that the conductance does not depend strongly, if at all, on the Ge thickness, which is to be expected if the barrier width is a function of doping density.

The temperature dependence of these super-Schottky devices also indicates that the major contribution to their characteristic is due to tunneling between the Ge barrier and the NbN electrode. The dV/dI vs. V

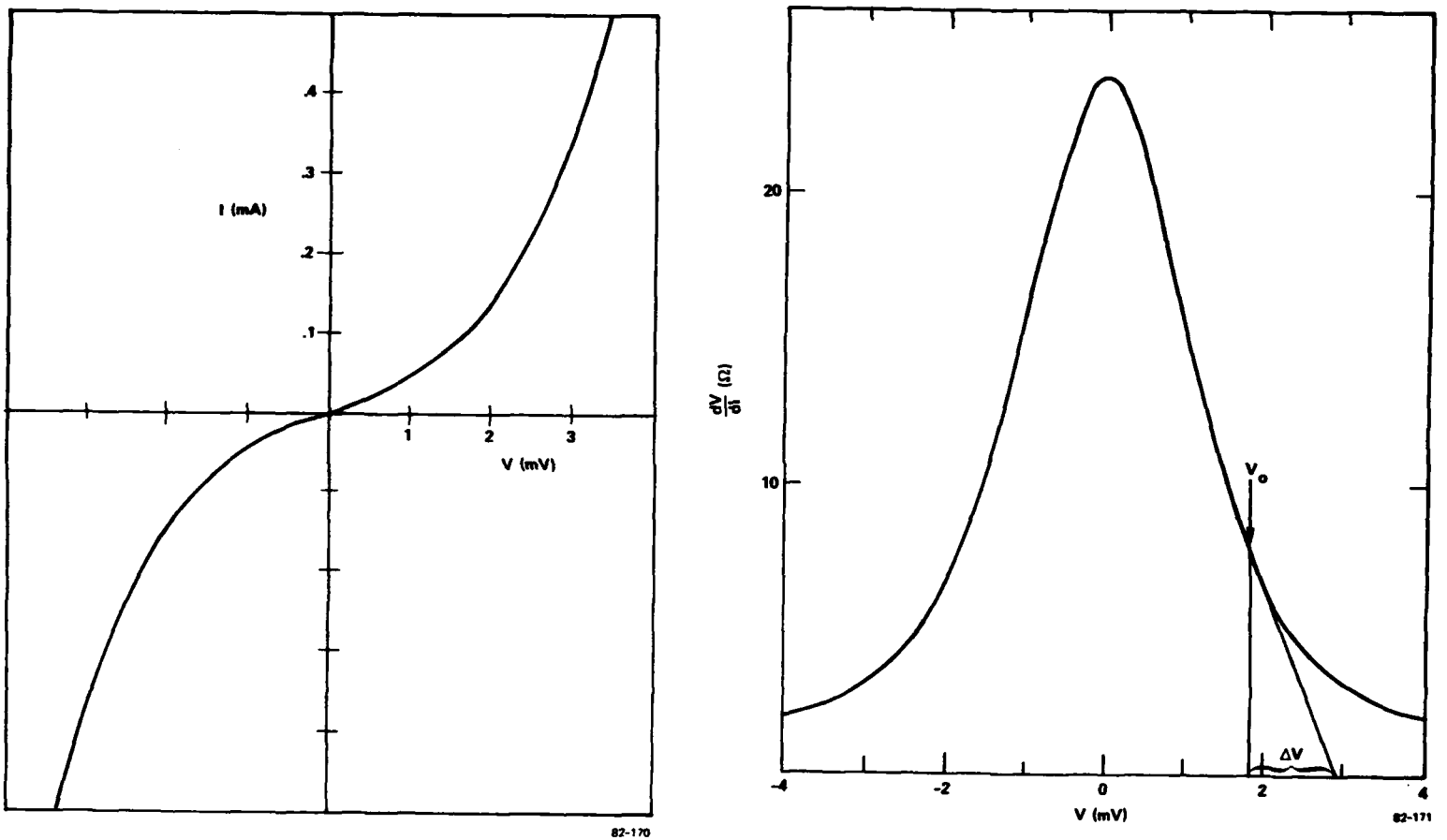

FIG. 3 (a) The I-V characteristic at 4.2 K for a typical NbN-Ge super-Schottky device of barrier thickness 60 nm. (b) dV/dI vs. V for the same device. The device area is 60 μ^2, resulting in a conductivity density of 7.2×10^{-4} mhos/μ^2 at zero voltage.

curves are qualitatively the same as T is varied from 4.2 K to 15 K, with a gradually decreasing curvature. As the Nb transition temperature is passed, a series resistance appears, but the overall shape of the curve remains the same.

Many of the devices with barriers ~ 30 nm thick have shoulders on the dV/dI vs. V curves, as shown in Fig. 4. The voltages and temperature dependence of this structure indicate that it corresponds to the energy gap in the niobium film. This is presumably caused by proximity effect coupling between the Nb and the Ge barrier. The tunneling density of states for such an N-S bilayer is expected to show structure not only at the induced gap of the N layer, but also at the energy gap of the S layer [24]. The magnitude and shape of this structure may depend on the detailed nature of the N-S interface, and it is surprising that we see a peak as large as shown in Fig. 4. This interpretation is consistent, however, with the observation that the devices made with the thicker, 60 nm, barriers never show this structure, and that the 30 nm barrier devices often show a small critical current ($\lesssim$ 10 μA) that is modulated by a magnetic field. This Josephson coupling appears as only a minor perturbation on the overall I-V characteristic, with an $I_c R_n$ product of only a few μV.

Concurrent work on NbN-aSi-Nb tunnel junctions [15] has indicated that their tunneling characteristics are very sensitive to the quality of the NbN film surface. In particular, for the films used in the Ge work there is comparison data on a-Si barrier devices made on NN 156 and NN 158 wafers (four 2" wafers were deposited at the same time during run NN 156 and three during run NN 158). NN 156 yielded tunnel junctions of reasonably high quality, with $I_c R_n$ ~ 1 mV and inferred gap for the NbN surface of 2.0 mV [15]. NN 158, however, yielded relatively poor tunnel junctions with a very low value for the NbN gap and $I_c R_n$ ~ 0.3 mV. This was attributed to the failure of the substrate heater at some unknown point during the NN 158 deposition. The Ge barrier devices fabricated

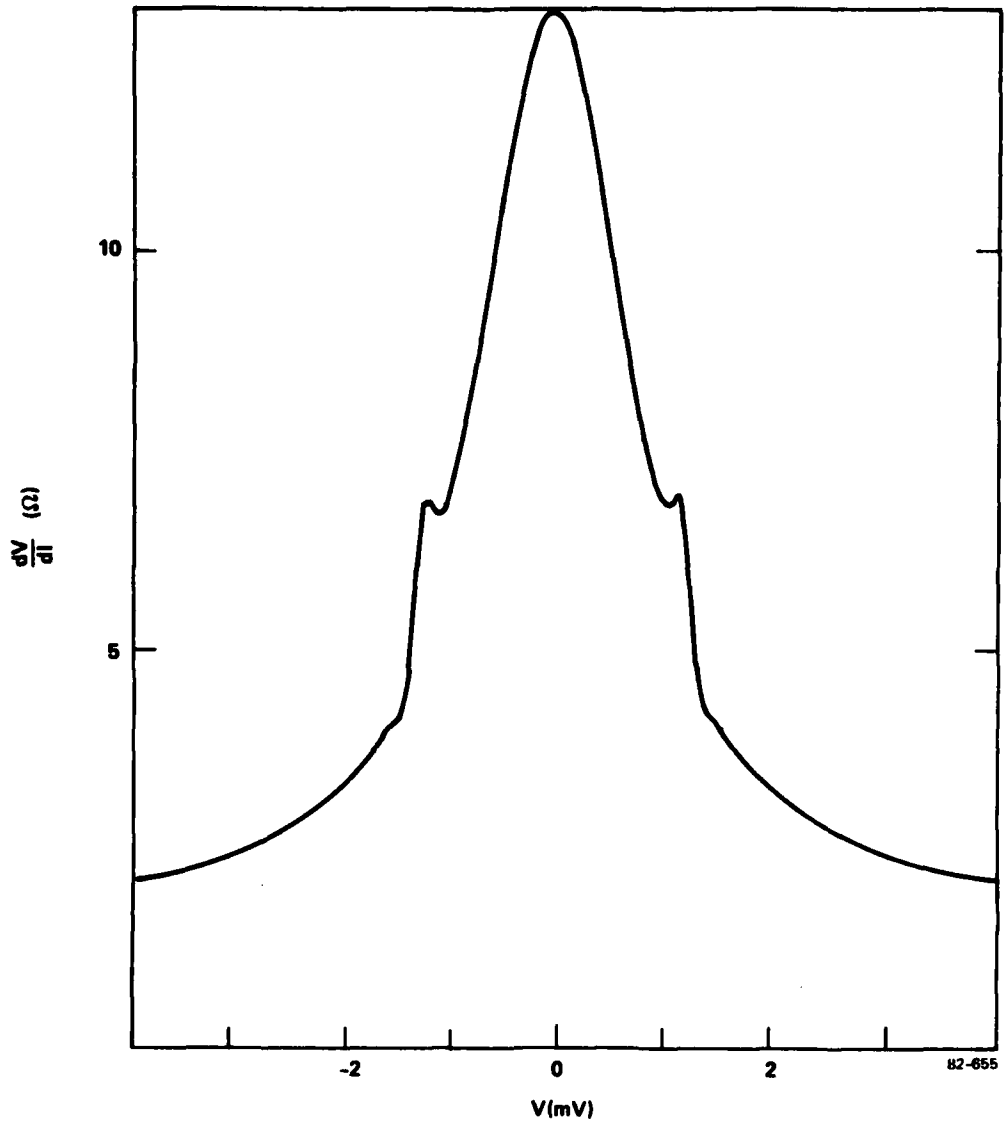

FIG. 4 The dV/dI vs. V characteristic at 4.2K for a device with a barrier ~ 30 nm thick.

on runs NN 156 and NN 158 are virtually indistinguishable. Since no systematic variation of NbN quality has been observed on multiple wafer depositions, either in the form of a variation in the energy gap or a variation of T_c, one concludes that the Ge barrier devices are less sensitive to the quality of the NbN surface than the a-Si devices. This is plausible, since the NbN/Ge super-Schottky barrier/interface is much further from ideal than the Si junctions. Whereas the a-Si tunnel junctions are qualitatively similar to the BCS S-I-S I-V curve, the Ge is a poor approximation of the BCS S-I-N characteristic.

The log-current vs. voltage curve up to 0.3 volts is shown in Fig. 5 for a typical super-Schottky diode. At ~ 0.3 volts, these devices blow out. The asymmetry in the two branches of the curve reflects the asymmetry in the Schottky barrier shape. Even though the highest voltages used, 0.3 volts, is more than 100 (kT/e), the current-vs-voltage characteristic has not become exponential, as it should in the case of a true Schottky barrier. The linear version of this I-V plot (not shown) indicates that the characteristic is linear up to about 40 mV. From the above results it appears that the band diagram illustrated in Fig. 6 is at least qualitatively appropriate for these devices.

The conclusion that NbN forms a much higher Schottky barrier with p^+ Ge than Nb is further reinforced by our observation that NbN also forms a higher barrier with sputtered Si barriers [15]† than does Nb. However, this conclusion must also be tempered by the caveat that these devices are far from ideal, and that the proposed diagram might also be applied to devices that could be different from those described here, depending on the exact values of the barrier heights, doping density, and the quality of the two interfaces.

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† Continuing work on NbN-aSi-Nb devices indicates an average barrier height of ~ 0.3 mV as opposed to 0.08 mV for similar Nb-aSi-Nb devices.

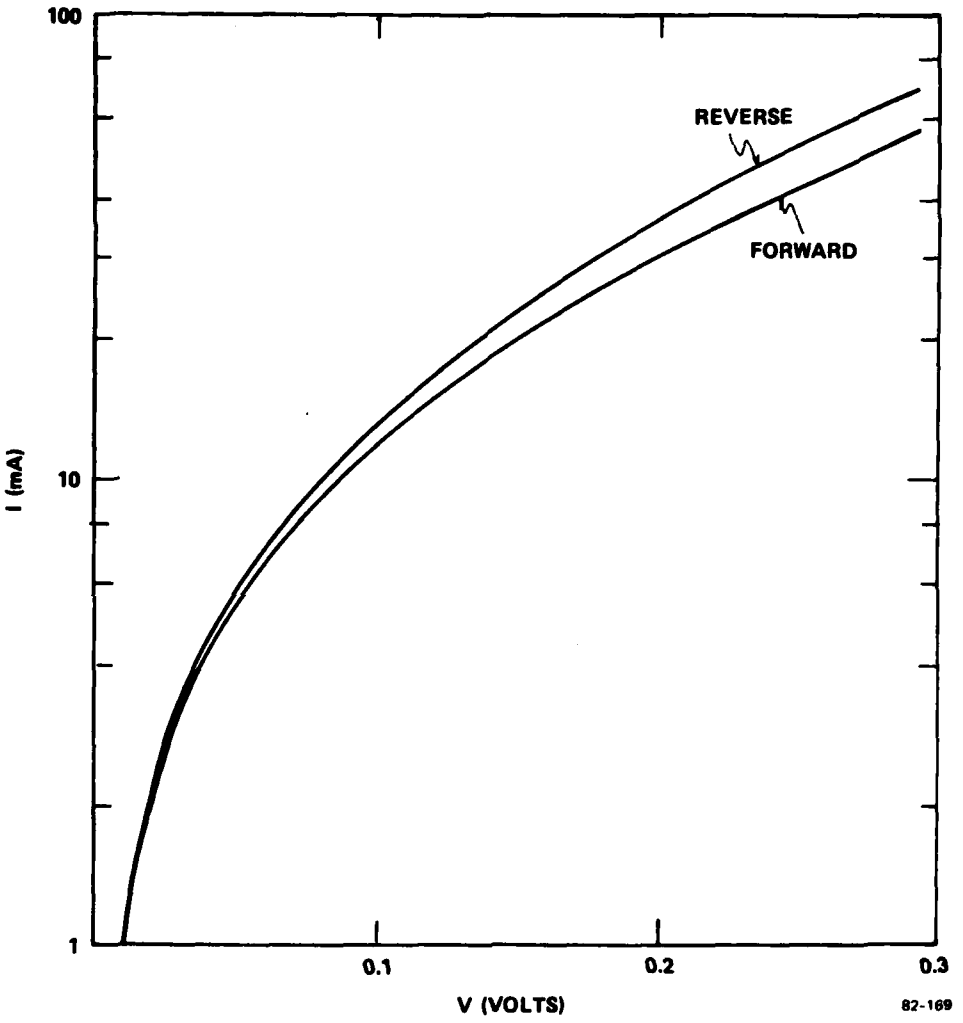

FIG. 5 A high voltage ℓn I-V curve for an ~ 60 nm barrier device at 4.2 K. The curve labeled forward is biased with the Nb electrode positive and the NbN electrode negative. The device blew out at ~ 0.3 volts.

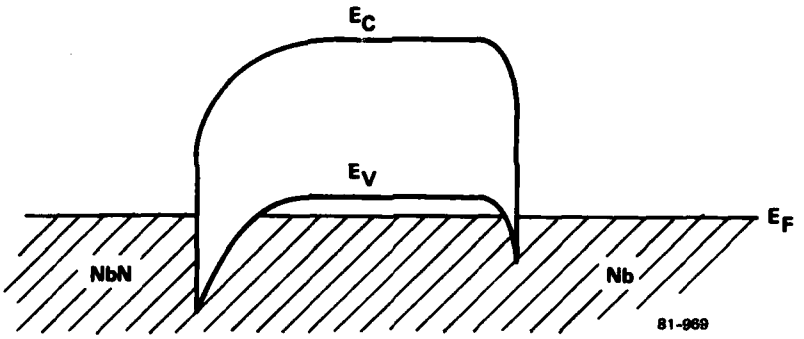

FIG. 6 Proposed band diagram for a NbN-p^+ Ge-Nb device.

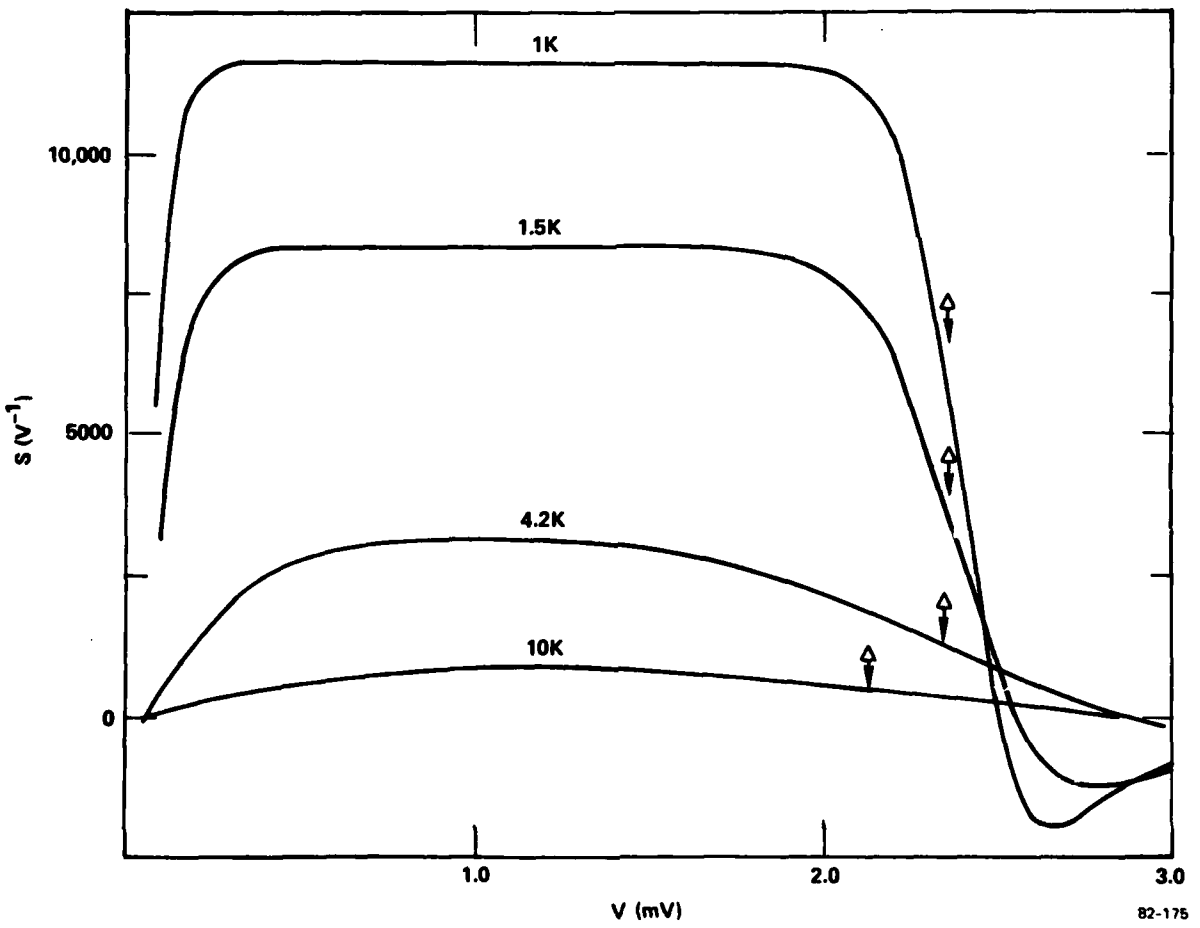

FIG. 7 S vs. V at 1.5, 4.2 and 10 K as calculated for a BCS S-I-N device with a T_c = 15.5 K superconducting electrode.

SECTION 4

THE NONLINEARITY PARAMETER

When employing Schottky and super-Schottky diodes as microwave detectors and mixers the figure of merit most often used is the nonlinearity parameter S, which is defined as

$$S \equiv \frac{\partial^2 I/\partial V^2}{\partial I/\partial V} \quad . \tag{3}$$

The higher the value of S, the better is the response of the device as a mixer or incoherent detector. For the functional form given by eqn. (1) it can be seen that S = e/kT. Thus as T is reduced, S can be expected to increase. However, the performance of conventional Schottky diodes saturates at relatively low values of S as T is lowered. This situation has been described by expressing the nonlinearity as $S = eV/k\ (T + T_o)$, where T_o is the "excessive temperature". T_o has been empirically determined to be 50K for GaAs [25]. Alternately, the nonlinearity has been expressed as $S = eV/\gamma kT$, where γ is a temperature dependent nonideality factor, which goes from 1 at room temperature to ~ 15 at 4.2 K for a GaAs Schottky barrier [26]. The net result is that S is limited to $\lesssim 300$ for conventional Schottky barrier diodes at low temperature. Thus the appeal of the super-Schottky in which values of S as high as several thousand at T ~ 1-2 K have been reported [3-5].

Since S is of major importance in the evaluation of these devices as microwave mixers, it is worth spending some time in determining the way in which S is to be measured and how it behaves. Fig. 3(b) shows a typical dV/dI vs. V curve and the construct used to determine S. It can be shown that at any voltage V_o, $S(V_o) = |1/\Delta V|$; ΔV is the distance between the intercepts of two lines with the voltage axis. The two lines are a vertical line through point V_o and the tangent to the dV/dI curve

at point V_o. This construct does not depend on the functional form of the I-V characteristic, it is completely general for S as defined above. From a plot of dV/dI vs. V it is thus relatively easy to generate a plot of S vs. V.

Equation (1) in the introduction is often applied to super-Schottky devices. This equation is appropriate for *both* Schottky diodes and for super-Schottky diodes, but only in the correct parameter ranges. For super-Schottky diodes this equation is valid for $kT \lesssim eV$, $eV \lesssim \Delta$, and $kT << \Delta$ [2]. In the limit that $e^{SV} >> 1$ it should be possible to determine S directly from the slope of the ℓn I vs. V plot. This condition does not hold for super-Schottky devices since $eV \lesssim \Delta$, implying that $e^{SV} \sim 1$. Thus S values determined using the slope of ℓn I vs. V [3-5] are typically higher than the true value.

The equation for the current vs. voltage characteristic of an S-I-N/super-Schottky device, using a BCS density of states, is

$$I(V) = \frac{1}{R_n e} \int_{\Delta}^{\infty} dE \, \frac{E}{\sqrt{E^2 - \Delta^2}} \left\{ f(E - V) - f(E + V) \right\}$$

where R_n is the normal resistance, Δ is the energy gap on the superconducting side of the device and $f(E) = (e^{\beta E} + 1)^{-1}$ is the Fermi function, with $\beta = 1/kT$. This equation can be integrated to generate theoretical I-V curves for S-I-N devices, or, more appropriately for our purposes, plots of S vs. V. These theoretical curves are shown in Fig. 7 for a S-I-N device with a NbN base electrode having $T_c = 15.5$ K, using the temperature dependent value of $\Delta(T)$. The flat portion of the 1.0 K and 1.5 K curves indicate the region where the approximation $S \sim e/kT$ is valid. At 10 K it can be seen that this is a poor approximation.

The actual S-V curves for two different Ge barrier devices at 4.2 K are shown in Fig. 8. The 60 nm barrier device more or less

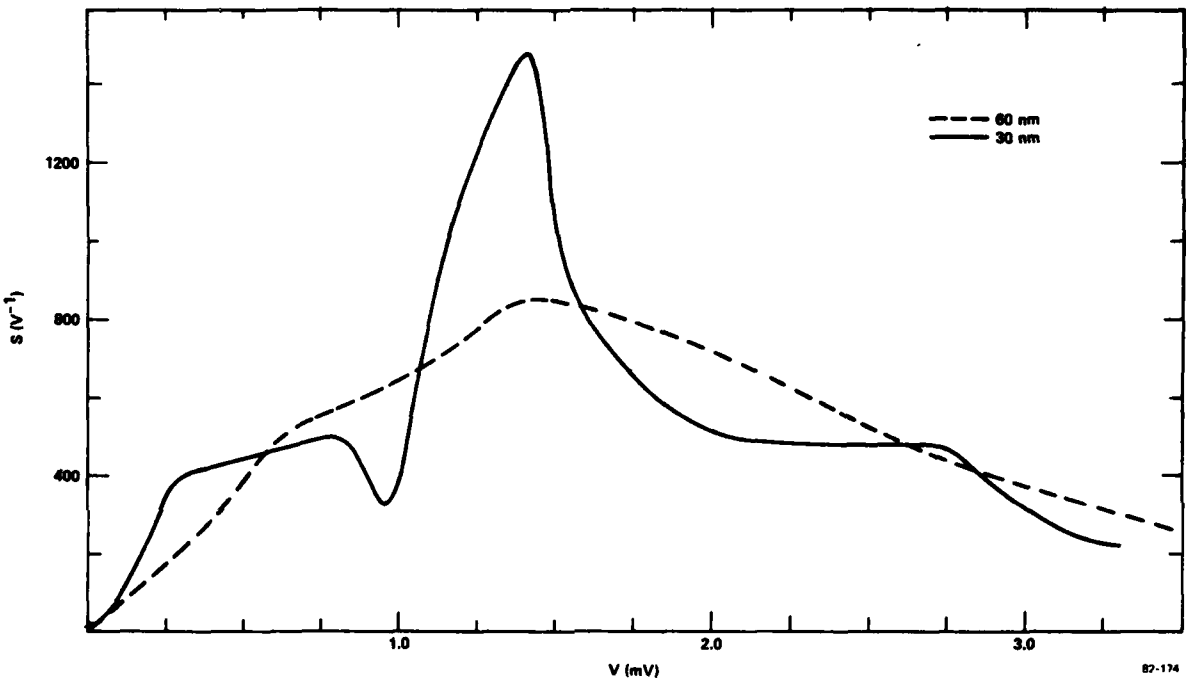

FIG. 8 (a) A plot of S vs. V generated from the dV/dI curve of Fig. 3(b). The temperature is 4.35 K. (b) The curve for a 30 nm barrier device.

approximates the theoretical curve, but with an S value that is consistently less than the ideal BCS value. The zero crossing of S is not observed in any of our devices (this corresponds to a minimum in dV/dI vs. V). The 30 nm barrier device has a large peak at ~ 1.4 mV, which corresponds to the shoulder seen in Fig. 4. This peak moves to lower voltage as the temperature is raised, and disappears at 9 K. As mentioned previously, this is consistent with the energy gap of the Nb electrode. In Fig. 4 these peaks are quite large, and their steepest portion yields an S value that is very high, but only over a very limited voltage range. The S vs. V curve for the particular 30 nm barrier device shown in Fig. 8 corresponds to a dV/dI vs. V curve in which the shoulders are barely evident.

The maximum value of S for a 60 nm barrier device is plotted as a function of temperature in Fig. 9. The decrease at 9 K is due to the series resistance of the Nb contact. For comparison, the functional form of the BCS value is indicated by the solid line, normalized to the experimental value at 4.2 K. Theoretically, S = 11,600/T, indicating that these devices are far from ideal. Even at 10 K a weak nonlinearity exists in our Ge devices which is far below the theoretical value.

In summary, we have fabricated devices using CVD p^+ Ge as the barrier material with a NbN lower electrode and a Nb upper electrode. The electrical characteristics of these devices is consistent with tunneling through a Schottky barrier between the p^+ Ge and the NbN, with the Nb electrode functioning primarily as an "ohmic" contact. It appears that although the Ge forms a fairly uniform barrier, the barrier/interface quality is relatively poor. The nonlinearity of these devices, combined with low series impedance on the semiconductor side of the device indicate that potential applications exist in the area of microwave sensors and mixers.

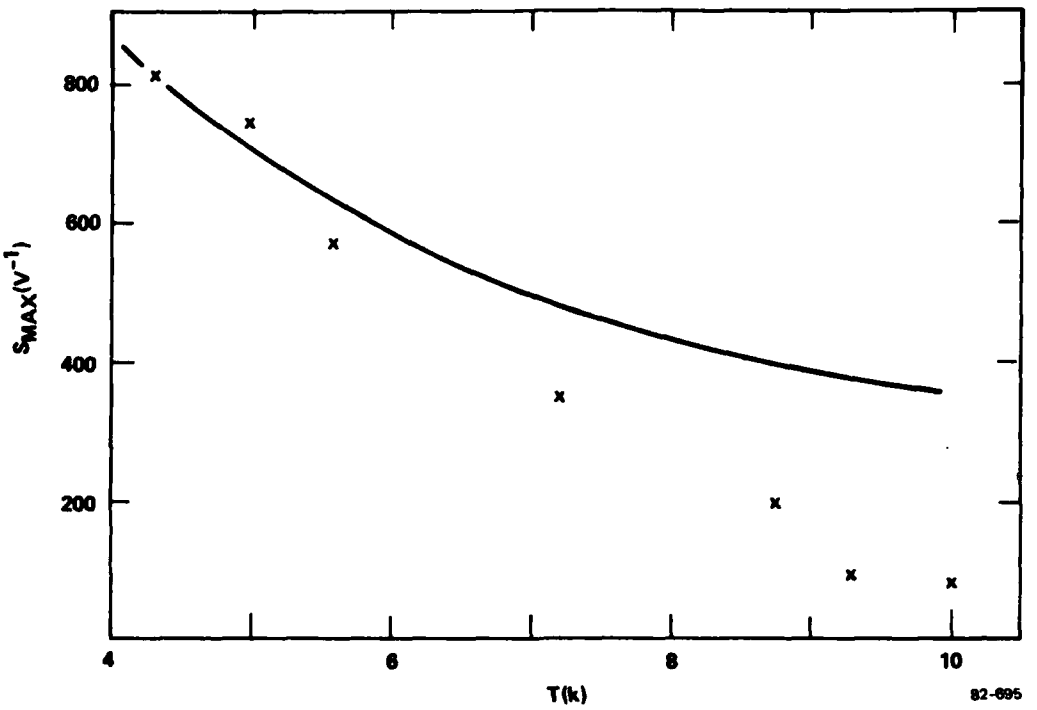

FIG. 9 The maximum value of S (seen at ~ 1.5 mV) for a 60 nm barrier device as a function of temperature. The BCS functional dependence, normalized at 4.2°K to the experimental point, is indicated by the solid line.

SECTION 5

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