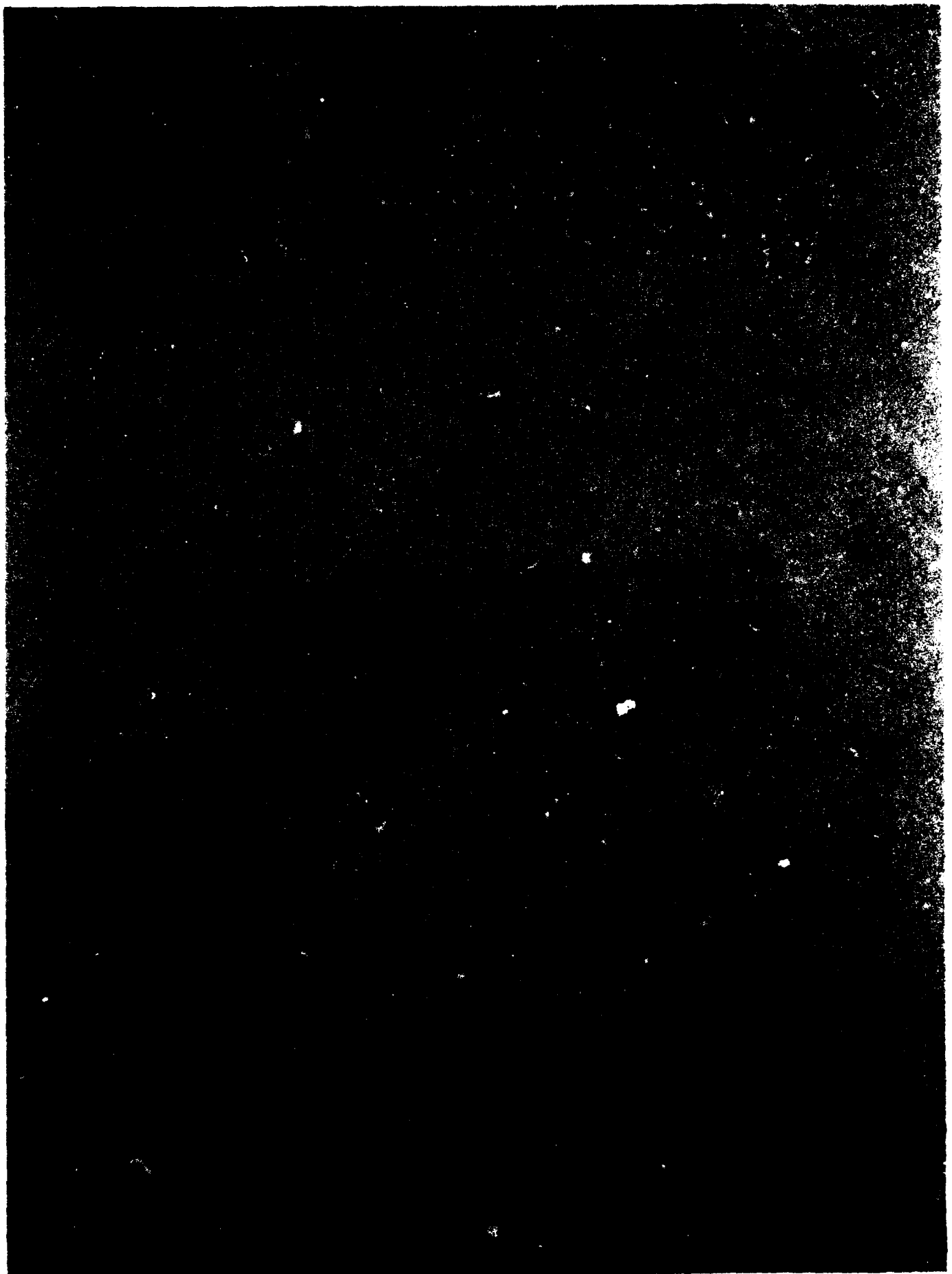


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## 1. INTRODUCTION

This report describes theoretical and experimental work performed in connection with the development of a new kind of electronic computer memory. The memory is based on a hybrid combination of semiconductor and ferroelectric ceramic elements which uses an anomalous photovoltaic effect<sup>1-4</sup> found in the ferroelectric ceramics. This memory is a variation on the conventional static or dynamic semiconductor memories in common use. Conventional devices are volatile memories which lose their information content when power to the devices is interrupted. Devices based on the new concept, however, are nonvolatile. In some respects they have memory characteristics similar to those of metal nitride oxide semiconductor (MNOS) and floating gate EAPROM (electrically alterable programmable read-only memory) devices. The new photovoltaic ferroelectric-semiconductor, however, can be expected to be superior to the presently available EAPROM devices. This new device will excel in programming time, in the number of possible read/write cycles, and in retention of the encoded memory states. Based on the work described in this report, the device is also expected to be superior in surviving environmental radiation.

The digital photovoltaic-ferroelectric-semiconductor memory cell concept has been described and demonstrated.<sup>5,6</sup> Within a semiconductor read/write cell there is incorporated an additional element which is a photovoltaic ferroelectric ceramic element. In operation, this element always retains, within its molecular structure, the last written bit in the memory state. The state characteristic is one of two directions of remanent polarization. This polarization is encoded by a write pulse with an addressing transistor at the same time that a sense transistor is encoded with a gate charge. The same addressing transistor places a volatile charge (positive or negative) on the gate of the sense transistor gate and encodes the ferroelectric element, switching the remanent polarization if the memory state is to be changed. The encoded ferroelectric elements are then used at any time to place a charge on the gates of the sense transistor, even after the original gate charge has leaked off. To charge the sense transistor gates and to maintain a charge requires that the encoded ferroelectric elements be illuminated.

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<sup>1</sup>p. S. Brody, *Solid State Comm.* 12 (1973), 673.

<sup>2</sup>p. S. Brody, *J. Solid State Chemistry* 12 (1975), 673.

<sup>3</sup>For a recent review, see R. Von Baltz, *Bulk Photovoltaic Effect in Ferro- and Piezoelectric Materials, Ferroelectrics*, 35 (1981), 131.

<sup>4</sup>p. S. Brody, *Ferroelectrics* 38 (1981), 939.

<sup>5</sup>p. S. Brody, *Appl. Phys. Lett.* 38 (February 1981), 673.

<sup>6</sup>p. S. Brody, *Investigation of Photovoltaic Ferroelectric Semiconductor Nonvolatile Memory*, Harry Diamond Laboratories HDL-TR-1948 (March 1981).

The charging is the result of the anomalous high-voltage photovoltaic ferroelectric ceramics. An open circuited photovoltaic ferroelectric ceramic element, when illuminated, will charge to a characteristic positive or negative voltage. The polarity of the charge depends on the direction of the electrically switchable remanent polarization. The magnitude of the voltage is proportional to the remanent polarization up to its maximum level. A capacitance placed across the element so as to shunt it will also be charged to that same saturation voltage level.

The characteristics of the switching are such that a two-state nonvolatile random access memory (RAM) is possible, operating with microsecond-duration write and erase pulses. In this report there are shown arrangements of cells and cell structures for such a device. Also discussed are approaches and problems in fabricating integrated devices.

New experimental work described in this report includes the performance of a test cell with respect to the various memory cell parameters. The test cell uses a sense transistor based on a junction field-effect transistor (JFET) rather than on the MOSFET device previously used.<sup>5,6</sup> There are also experiments in which the radiation hardness of the photovoltaic ferroelectric-semiconductor memory element was evaluated. These experiments indicate that the encoded polarization state and the photovoltaic mechanism are largely unaffected by both high total dose and dose rates of hard radiation.

## 2. JFET CELL AND TEST CIRCUIT

One arrangement has been described for a nonvolatile "sense transistor" cell element consisting of a ferroelectric element, two diodes, and a MOSFET.<sup>5,6</sup> Another functional equivalent using two JFET transistors and a photovoltaic ferroelectric element is shown schematically in figure 1. This new arrangement reduces by one the number of semiconductor components and also has advantages with respect to radiation hardness, since the more radiation-sensitive MOSFET has been eliminated as the sense transistor.

The functioning of this circuit is essentially the same as that of the MOSFET cell.<sup>5,6</sup> A positive voltage applied to the ferroelectric

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<sup>5</sup>P. S. Brody, *Appl. Phys. Lett.* 38 (February 1981), 673.

<sup>6</sup>P. S. Brody, *Investigation of Photovoltaic Ferroelectric Semiconductor Nonvolatile Memory*, Harry Diamond Laboratories HDL-TR-1948 (March 1981).

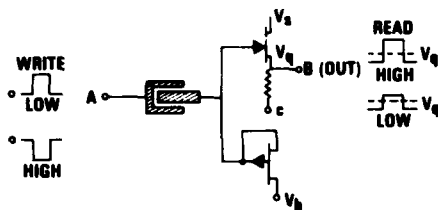


Figure 1. Arrangement using JFET transistors which makes dynamic cell sense transistor nonvolatile (not complete cell--write/read accessing elements are not shown).

element (which functions as a coupling capacitor) results in an instantaneous positive voltage at the gates, which then decays to a smaller positive voltage,  $V_s$ , plus the small drop across the diode through the n-channel JFET input diode during the write pulse duration,  $t_o$ . At time  $t_o$  the input of the capacitive element returns to ground, resulting in an instantaneous negative voltage at the gate, which decays rapidly to the negative voltage,  $V_b$ , less the diode drop through the p-JFET-based diode. The gate of the n-channel JFET (the sense transistor) is then charged to this negative voltage, which decays slowly through the high gate-to-ground resistance. This is the negative volatile gate memory charge.

A positive pulse applied to the ferroelectric element results, in a similar manner, in a positive volatile gate memory charge. The volatile memory states of the n-channel JFET sense transistor are controlled by these gate charges. A negative charge on the n-channel JFET gate from a positive write pulse increases the drain source channel resistance of the sense JFET, reducing the value of the quiescent voltage  $V_q$ , at B. If the transistor is operating near cutoff, this voltage,  $V_q$ , is small. The read output is then a low-level signal, indicating one of the binomial memory states, for example, a 0. A negative write pulse removes any negative gate charge, causing the channel resistance to decrease and increasing the quiescent voltage  $V_q$  to its high-level value, now indicating a 1. These read voltages are accessed with a read-access transistor (not shown). A column-select signal on the gate of the read-access transistor connects the sense transistor source point to a row. The row is accessed for read with a row-select signal at the gate of a row-access transistor.

The write pulses are applied with a transistor analog switch (not shown). The arrangement must be able to provide both positive and negative voltage pulses. In the tests described this is done with VMOS transistors, but more ideally a single JFET switch could be used. In that case the column and row address is produced by connecting the transistor drain to the desired positive or negative voltage source (column select) while simultaneously clamping the initially negative-biased gate to the source (row select).

The analog switches not only write by charging gates, but also switch the ferroelectric elements within the cells. When illuminated,

these elements charge the gate input capacitance to either a positive or negative voltage. The polarity of these voltages is the same as that of the volatile charge. If these voltages are equal to or greater than the gate voltage levels set by  $V_s$  and  $V_b$ , then the sense transistor returns to, or remains in, the last memory state addressed after the volatile charge vanishes. This provides the nonvolatile memory characteristics of the devices.

The test circuit (fig. 2) used ferroelectric memory elements which were bifilar planar electrode structures on a PZT-5A substrate. The memory elements were produced using a computer-generated reticle and negative photoresist. The substrates were 2-in.-diam, 0.015-in.-thick wafers of polished PZT-5A. Test element arrays (12 elements in an array) were formed 30 at a time on a single wafer. The wafer was then cut apart with a diamond blade. Each chip consisted of a single array. These were mounted in 14-pin dual in-line packages (DIP's), the terminals of which were connected to finger planar electrodes. Between a finger and a U-shaped central common electrode is a U-shaped gap across which the switching voltage will appear. Figure 3 is a photo-

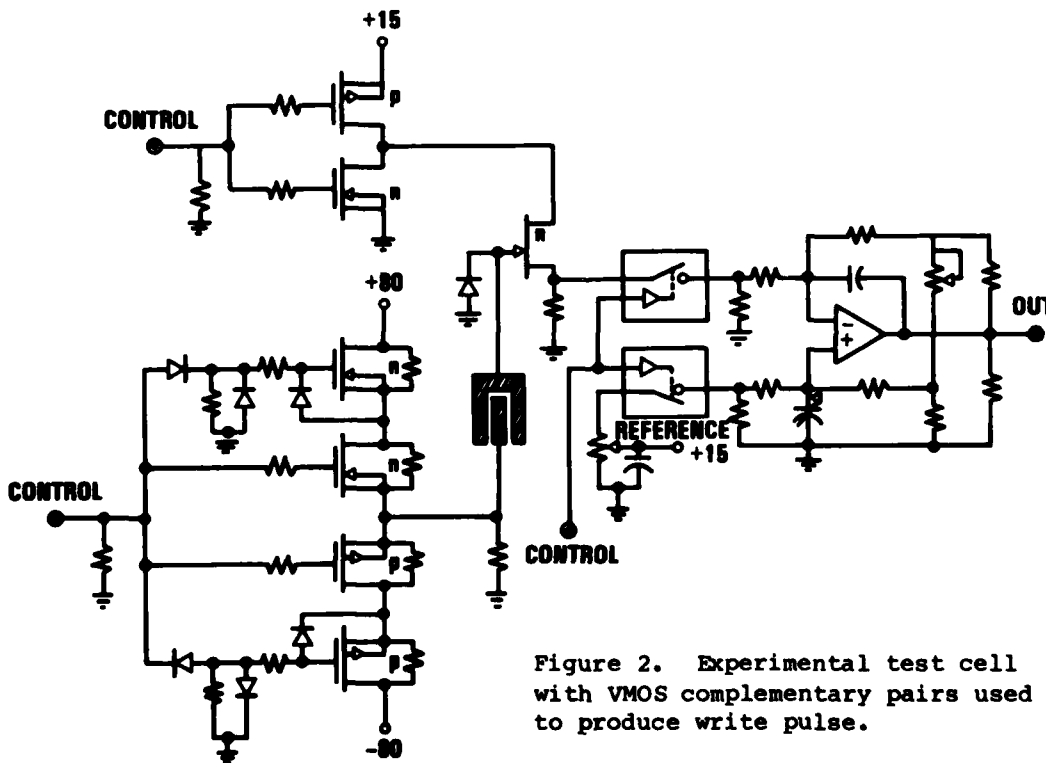


Figure 2. Experimental test cell with VMOS complementary pairs used to produce write pulse.

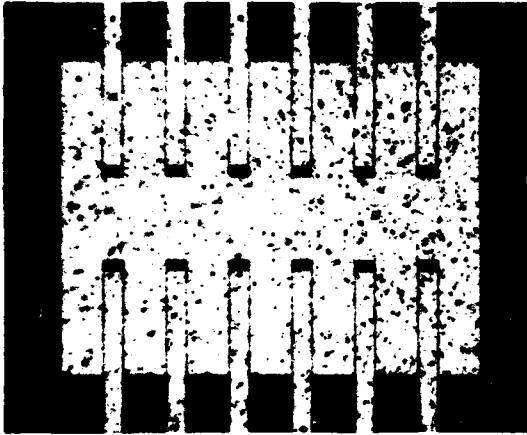


Figure 3. Photomicrograph of 12-element array. Metallization is Cr-Au.

micrograph of a 12-element array. The active regions that are the gaps are each  $5 \mu\text{m}$ . The memory regions thus formed are  $5000 \mu\text{m}^2$  exclusive of electrodes. The fabrication yield was moderate with an occasional finger electrode in an array shorted to the common electrode.

For test purposes, an individual element--or memory region--is switched by connecting the element to the JFET gate and diode input and driving the common electrode positive or negative with a write pulse. For test purposes, an individual cell consisted of a single-array element in the test circuit shown.

### 2.1 Dependence of Read Outputs on Pulse Duration

An experimental test cell was constructed based on this new arrangement. The test circuit, shown in figure 2, was used to measure the dependence of the nonvolatile memory read outputs on write pulse duration. Plotted in figure 4 is the change in voltage at the source resistor measured 10 min after an encoding which reverses the element's spontaneous remanent polarization. During the 10-min interval, the initial volatile gate sense transistor gate charge has decayed. The charge on the gate is now the result of the photovoltaic output from the memory element. Illumination was from a 4-W fluorescent tube (GE F4T5 BLB) placed about 1 cm from the test DIP, producing about  $1 \text{ mW}/\text{cm}^2$  of 370-nm centered radiation. The sense transistor circuit is a source follower. The change in output voltage is equal to the gate voltage change resulting from the photovoltaic charging, except for larger negative gate signals where the transistor cuts off. Figure 5 shows the dependence of the output voltage change on pulse voltage for a pulse duration of 300 ns. The effects of approaching saturation are seen, but saturation is not reached. The write voltages in these measurements were limited to  $\pm 80 \text{ V}$  by source gate breakdown in the V-groove MOS (VMOS) write circuits.

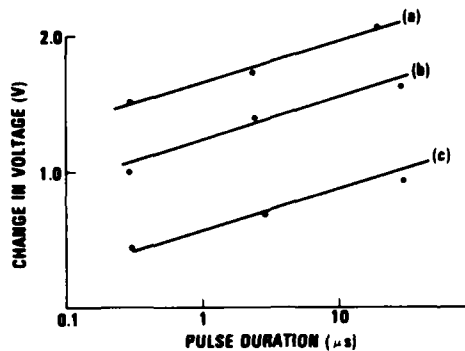
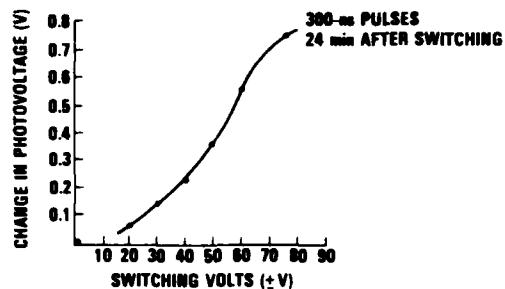


Figure 4. Quiescent voltage change as function of pulse duration for  $\pm 74$ ,  $\pm 45$ , and  $\pm 30$  V switching pulses using test circuit in figure 2 and DIP array element.

Figure 5. Dependence of gate photovoltage change on pulse magnitude.



## 2.2 Switching Characteristics

In a memory device it is preferable for the switching pulse to switch the ferroelectric polarization between two fully saturated states. Saturation will generally be difficult to achieve for low switching voltages and short pulse duration. The use of a double write pulse--a positive pulse followed by a negative pulse to produce the effect of a negative pulse (write high) and a negative pulse followed by a positive pulse to produce a single positive pulse (write low)--improves the situation for short duration write pulses. The double pulse system prevents the polarizations (and, therefore, the photoelectromotive forces--emf's) from walk-up and walk-down relative to a fixed level. The effectiveness of the double pulse method is a consequence of the hysteresis relation characteristic of polarity switching in the photovoltaic ferroelectric materials. Hysteresis relations between photovoltage and pulse number typical of the PZT-5A material are shown in figures 6 and 7. Note the softening of the loops for shorter duration pulses. In both cases, however, a reversing pulse is more effective in changing the element photovoltage than subsequent nonreversing pulses.

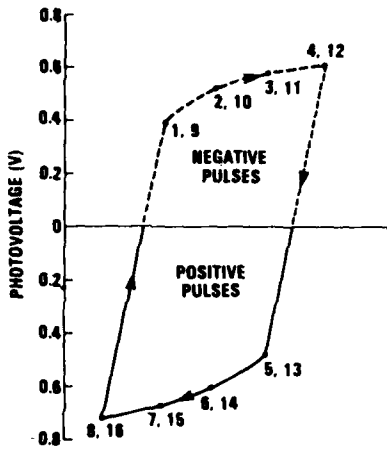
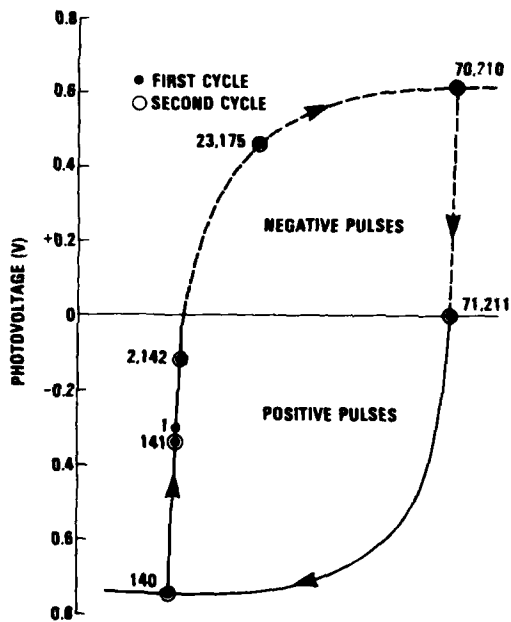


Figure 7. "Hysteresis" relation for 200-ns pulses.

Figure 6. "Hysteresis" relation between photovoltage and number of pulses for 11- $\mu$ s pulses.



In table 1 we see the results of experiments using asymmetric double pulses. Despite the varied sequences of read/write, the sense transistor output was always found to be in either a low voltage output (0.02 V) or a high voltage output (0.5 V) state. Two-state operation is clearly demonstrated. The tests also demonstrate at least  $10^7$  writes for arbitrarily varied sequences of high and low writes.

TABLE 1. EFFECT OF VARIED SEQUENCE OF WRITE-HIGH AND WRITE-LOW PULSES USING ASYMMETRIC POLARITY DOUBLE PULSE WRITES

Number of successive writes		Output after final write of series of successive writes (V)
1	Low	0.02
1	High	0.48
$2 \times 10^6$	Low	0.02
1	High	0.48
1	Low	0.02
1	High	0.50
$1 \times 10^6$	High	0.55
$2 \times 10^6$	High	0.58
1	Low	0.07
1	High	0.44
1	Low	0.05
$4 \times 10^6$	High	0.45
1	Low	0.02

Note: The experimental arrangement shown in figure 2 with a single memory element was used in these tests.

### 2.3 Retentivity of Stored Data

The decay of the photovoltage (which controls the memory state) with time is initially logarithmic and eventually levels off, supporting the expectation of indefinitely long memory retentivity.<sup>5</sup> Figure 8 shows memory retention results using the JFET test cell. A linear extrapolation of the plotted data shows the memory window closing in

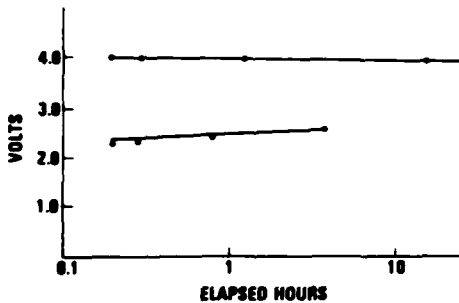


Figure 8. Memory photovoltage versus elapsed time for two memory states.

<sup>5</sup>p. S. Brody, *Appl. Phys. Lett.* 38 (February 1981), 673.

about 35 years. A linear extrapolation, however, is a worst possible assumption, since the logarithmic decay rate decreases with increasing time.

#### 2.4 Radiation Hardness

The effects of total  $\gamma$  radiation dose on memory retention, and on the functioning of the ferroelectric element as a photovoltaic charge generator, were examined. An encoded single element mounted in a DIP element was subjected to an incrementally increasing total  $\gamma$  dose. The element was then returned to the test circuit. As before, a 4-W fluorescent tube was used as the illumination source. The results shown in figure 9 are photovoltages remeasured about 30 min after removing a test array element from a  $^{60}\text{Co}$  source. For the higher total doses the initial photoelectromotive force was somewhat decreased from the initial value. The magnitude, however, increased with time over a period of several hours to the initial value. This temporary decrease is possibly due to a temporary darkening produced by the radiation. The darkening, however, vanished with time.

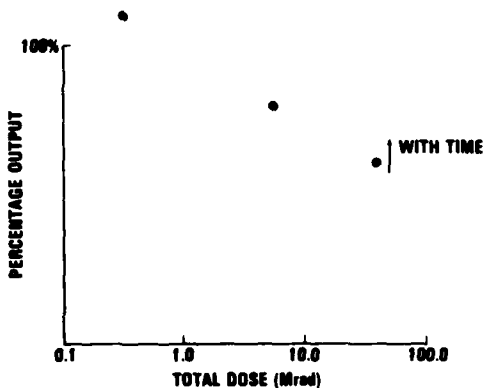


Figure 9. Results of total  $\gamma$  radiation dose on memory retention.

The effects of  $\dot{\gamma}$  were determined by exposing a similar test array which had been encoded to a flash x-ray dose of  $2 \times 10^{11}$  rads/s. The device was then returned to the test fixture and read out. There was no significant change in sense transistor output.

These experiments show an intrinsic radiation hardness of the memory elements. The photovoltaic ferroelectric element is, however, just one portion of a memory cell. The remaining components are semiconductor elements--in particular, a sense transistor, which must continue to function normally after irradiation. This transistor, in MNOS and floating gate devices, is by necessity a very high impedance

device. The isolation of the floating gate charge, or of the interfacial MNOS charges retained in traps, is necessary in these devices. There must be no leakage of stored charge over the life of the memory state. This means that the conductivity of the insulating material isolating the gate (floating gate) from the channel must be very low. Radiation, however, has the effect of increasing conductivity, which reduces memory lifetime, and also creating charged defects, which can overwhelm the effects of the stored memory charge. MNOS and floating gate devices tend therefore to be radiation sensitive. The photovoltaic ferroelectric-semiconductor arrangement, however, can use a lower impedance sense transistor--e.g., a JFET used in the test device (see fig. 1 and 2), because there is a generation mechanism available for placing charges on the transistor gate. The energy for the charge generation comes from illumination incident on the photovoltaic element. The gate can be charged at any time during the indefinitely long life of the polarization state. An isolated packet of charge need therefore not be retained over the life of the memory, and the insulation between gate and channel need therefore not be as high as in floating gate or MNOS types. This semiconductor structure used with the ferroelectric element in a memory cell can therefore be of a type that is lower in impedance and is more radiation resistant. The photovoltaic semiconductor memory has, in this respect, an important advantage over the MNOS and floating gate charge retention memories.

### 3. APPLICATIONS TO RAM NONVOLATILE MEMORY--CONTINUOUS ILLUMINATION

The cell described in section 2 can be used with a continuous source of energizing illumination as a high-speed nonvolatile electronic RAM. The RAM application is interesting because there is no presently available device that would appear to be competitive with respect to permanence and speed. The continuous illumination form of the RAM memory has the two following characteristics:

(1) The transistor states persist, as addressed, even after the volatile gate charges have decayed. No overhead circuitry is needed to refresh the gates. The device is thus a static memory (although the cell structure is basically of the dynamic type) in the sense that refresh is not required.

(2) It is nonvolatile in the sense that if all power including illumination is removed, the information within the matrix is not lost. Restoring power and illumination returns each transistor or output to its correct value.

### 3.1 Application to Electrically Programmable and Electrically Alterable Read-Only Memory

A relatively simple scheme involves electrically addressing ferroelectric elements in matrix fashion in a programming device. Once programmed, the device is used as a read-only memory (ROM), but can be reprogrammed electrically very rapidly. Continuous or periodic pulse illumination provides the gate charges. A continuous illumination source keeps the gates charged or charges them when the memory is to be read out. The rate at which the gates charge and the total fluence (total optical energy in joules) required to charge the gates depend on the intensity and wavelength of the illumination and the gate-to-ground or channel capacitance and leakage. The gate-to-ground capacitance depends not only on the sense transistor capacitance to ground but also on the way the ferroelectric element is structured and the electrode configured. A lower limit on energy required to charge a gate to a specified voltage and a lower limit on illumination flux can, however, be obtained. The result of these calculations points to high densities and low optical energy fluence requirements in integrated devices.

The special requirements for an illumination source are compensated for by beneficial attributes of indefinitely long memory, retentivity, fast write times, and good environmental characteristics.

### 3.2 Nonvolatile RAM Requiring Illumination Only to Restore Memory States

A continuous source of illumination is not required for RAM. Illumination need be used only to restore lost memory states. To do this, cells are arranged in a matrix with refresh circuitry to operate as a dynamic RAM. If it were just an ordinary dynamic RAM, the memory data would be lost if the operating power were lost, or if the refresh cycle were interrupted (for another reason). In the photovoltaic ferroelectric semiconductor devices, however, the information stored at the time of the interruption is retained in the switchable ferroelectric elements. To restore normal operation after cycle interruption, the ferroelectric elements are all simultaneously illuminated with a low-level uv flood source. Figure 10 shows schematically the interrupt and restoration. Once the gates are recharged, the transistors will be in the correct memory states. Normal refresh can begin again and the illumination source removed.

This scheme is of the dynamic type. Refresh circuitry is required. A memory of the static type--but similar in other respects--can also be designed. As is true in a volatile static memory, a more complex cell structure would be necessary.

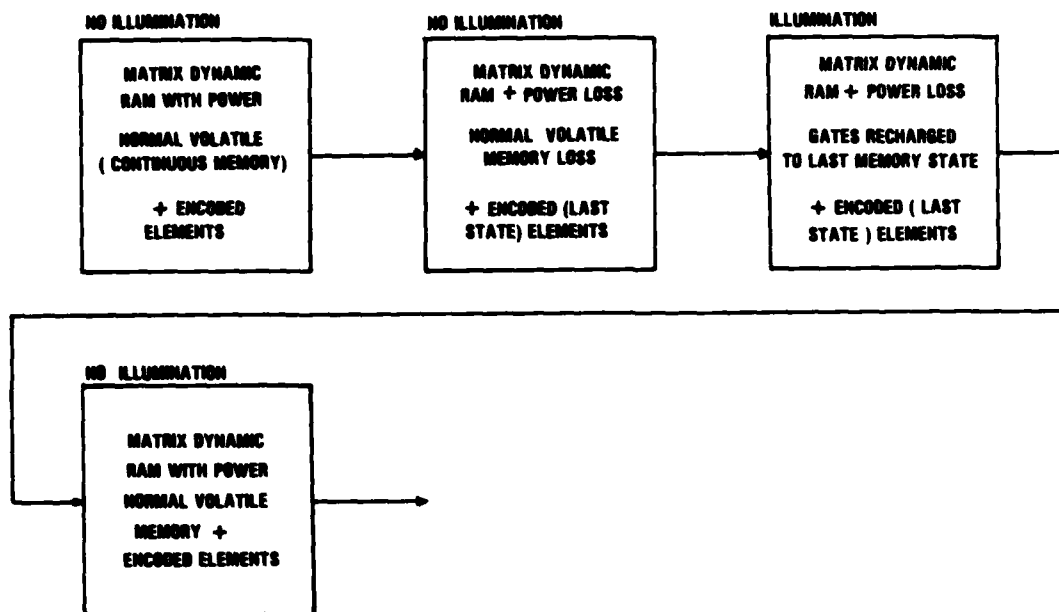


Figure 10 Scheme for nonvolatile photovoltaic ferroelectric-semiconductor RAM. To restore lost information, device is energized with low-level illumination flux.

#### 4. APPROACH TO INTEGRATED DEVICES

Fully integrated devices could be fabricated with photovoltaic ferroelectric film memory elements on a silicon substrate. Integrated into the substrate would be a write transistor, a read access transistor, and a sense transistor with the photovoltaic ferroelectric memory elements as islands on the substrate. There are numerous possible cell configurations and element electrode configurations. In one configuration ferroelectric memory elements are arranged with edge electrodes or with planar electrodes, with the remanent polarization and photocurrent flow perpendicular to the direction of an illumination flux. This is called a transverse configuration in accordance with photoconductivity nomenclature. In another configuration--a so-called longitudinal configuration--the flux and polarization are parallel and the illumination passes through transparent electrodes. The transverse configuration was used for the experimental devices described in this report and in previous publications, but it is not necessarily the preferred arrangement.

The technology required for producing polycrystalline and single crystal films with ferroelectric properties on silicon and oxide substrates has been previously reviewed.<sup>6</sup> A typical process utilizes rf sputtering and subsequent thermal annealing. The annealing process converts the sputtered material, which is in an amorphous or a microcrystalline state, to a polycrystalline material with 0.1  $\mu\text{m}$  or larger crystal grains.

For the configuration shown in figure 1, the switching and access transistors could be JFET or other MOS structures, or even bipolar devices. Either dielectric or junction isolation could be used for required isolations.

It is understood that in integrated devices switching voltages must be maintained within moderate limits. Voltages as high as those used in the experimental device require high voltage transistors, a capability which in the experimental devices is provided by the VMOS. It is felt, however, that element voltage requirements can be very considerably reduced--by reducing element size or by using ferroelectric materials with lower coercive fields. Even with the material used, P2T-5A switching voltages may be reduced to less than 10 V by increasing minimum write time to milliseconds (rather than microseconds).

In an integrated device, cell densities would be primarily controlled by the size of the semiconductor portion of the cells. The area requirements of the ferroelectric element islands would not be large. Based on known constants, one computes that a sense transistor with a 1-pF gate capacitance would be charged to its memory photovoltage in 1 s by a 5- by 100- $\mu\text{m}$  edge-configured P2T-5A structure, using an illumination flux of 0.3  $\text{mW}/\text{cm}^2$ . This is a density of  $2 \times 10^5$  elements per  $\text{cm}^2$  exclusive of requirements for spacing and connections.

## 5. CONCLUSIONS

The experimental analysis presented in this report supports the feasibility of moderate to high-density semiconductor EAPROM and RAM memory devices that use the photovoltaic effect in ferroelectric elements. The advantages over present devices exist in the potential for microsecond duration read/write cycle times, indefinitely long-time memory retentivity, and insensitivity of the intrinsic memory states to hard radiation. In addition, integrated devices can utilize JFET transistors which are less sensitive to hard radiation than the MOS structures used in floating gate devices.

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<sup>6</sup>P. S. Brody, *Investigation of Photovoltaic Ferroelectric Semiconductor Nonvolatile Memory*, Harry Diamond Laboratories HDL-TR-1948 (March 1981).

There appears to be a potential for high density devices. One particularly attractive embodiment of the photovoltaic ferroelectric semiconductor memory concept would be a high density device which would function normally as an ordinary high-speed RAM with refresh circuitry. If the refresh cycle is lost--for example, by power shutoff--the memory states could be restored by a low-level illumination of the memory chips for several seconds.

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