

AD-A123 648

CARRIER TRANSPORT STUDY IN SILICON DEVICES: ELECTRICAL  
AND OPTICAL STUDIE. (U) WESTINGHOUSE ELECTRIC CORP  
BALTIMORE MD J R SZEDON ET AL 30 OCT 82

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ARO-15824. 1-MS DAAG29-79-C-0026

F/G 28/3

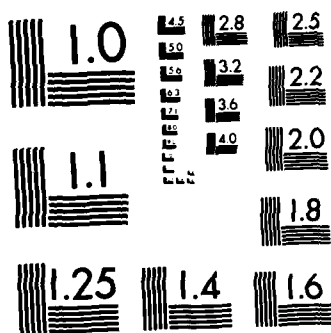
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|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|-----------------------------------------------------------------------|
| 1. REPORT NUMBER<br>15824.1-MS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 2. GOVT ACCESSION NO.<br><b>AD-A223648</b> | 3. RECIPIENT'S CATALOG NUMBER                                         |
| 4. TITLE (and Subtitle)<br>Carrier Transport Study in Silicon Devices:<br>Electrical and Optical Studies of Multi-Layer<br>Insulators for Memory Device Applications                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                            | 5. TYPE OF REPORT & PERIOD COVERED<br>Final:<br>20 Feb 79 - 30 Sep 82 |
| 7. AUTHOR(s)<br>J. R. Szedon<br>T. A. Temofonte<br>K. Vedam                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                            | 6. PERFORMING ORG. REPORT NUMBER                                      |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS<br>Westinghouse Electric Corporation<br>Baltimore, MD 21203                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                            | 8. CONTRACT OR GRANT NUMBER(s)<br>DAAG29 79 C 0026                    |
| 11. CONTROLLING OFFICE NAME AND ADDRESS<br>U. S. Army Research Office<br>Post Office Box 11711<br>Research Triangle Park, NC 27709                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                            | 10. PROGRAM ELEMENT, PROJECT, TASK<br>AREA & WORK UNIT NUMBERS        |
| 14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                            | 12. REPORT DATE<br>Oct 30, 82                                         |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                            | 13. NUMBER OF PAGES<br>94                                             |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                            | 15. SECURITY CLASS. (of this report)<br>Unclassified                  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                            | 15a. DECLASSIFICATION/DOWNGRADING<br>SCHEDULE                         |
| 16. DISTRIBUTION STATEMENT (of this Report)<br><br>Approved for public release; distribution unlimited.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                            |                                                                       |
| 17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)<br><br>NA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                            |                                                                       |
| 18. SUPPLEMENTARY NOTES<br>The view, opinions, and/or findings contained in this report are those of the<br>author(s) and should not be construed as an official Department of the Army<br>position, policy, or decision, unless so designated by other documentation.                                                                                                                                                                                                                                                                                                                                                                                      |                                            |                                                                       |
| 19. KEY WORDS (Continue on reverse side if necessary and identify by block number)<br><br>electrical properties      silicon dioxide<br>optical properties      silicon<br>insulators      thin films<br>memory devices      oxides                                                                                                                                                                                                                                                                                                                                                                                                                         |                                            |                                                                       |
| 20. ABSTRACT (Continue on reverse side if necessary and identify by block number)<br><br>We have studied the electrical and optical behavior of specimens from a 3x5<br>matrix, considering three deposition temperatures. In addition to a set of<br>unannealed specimens at each deposition temperature, four sets of annealed<br>samples were prepared at each temperature, for high and low temperature<br>treatments in hydrogen and in nitrogen. By excluding results for specimens<br>prepared at 750 Deg. C, except those receiving anneals at 1000 Deg. C in either<br>hydrogen or nitrogen, we found clear direct effects of annealing on all the |                                            |                                                                       |

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20. ABSTRACT CONTINUED

parameters of preliminary interest. The results of spectroscopic ellipsometry analysis indicate that the film structure of the specimen with the baseline silicon nitride is significantly different from the films deposited at higher temperature. It does not have an ellipsometrically detectable layer of silicon dioxide at the silicon surface. The stability of the memory states associated with the pulsed write and clear conditions correlated with the final density of fast surface states, except for anomalous behavior of the 750 Deg. C, unannealed specimen. Consideration of the ellipsometry results leads us to speculate that any thin oxide film which has an electronic influence in the baseline specimens must be substantially different from those associated with the preparation of nitride films at 850 Deg. C. From this base, we can define a clearer route to optimize and understand the behavior of MNOS structures in memory device applications.

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CARRIER TRANSPORT STUDY IN SILICON

ELECTRICAL AND OPTICAL STUDIES  
OF MULTI-LAYER INSULATORS FOR  
MEMORY DEVICE APPLICATIONS

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October 30, 1982

PROGRESS REPORT

(TWENTY COPIES REQUIRED)

1. ARO PROPOSAL NUMBER: 15824-MS
2. PERIOD COVERED BY REPORT: 10/1/81 to 9/30/82
3. TITLE OF PROPOSAL: Carrier Transport Study in Silicon Devices
4. CONTRACT OR GRANT NUMBER: DAAG29-79-C-0026
5. NAME OF INSTITUTION: Westinghouse Elec. Corp., Advanced Technology Laboratory
6. AUTHOR(S) OF REPORT: R. N. Ghoshtagore, J. R. Szedon and T. A. Temofonte
7. LIST OF MANUSCRIPTS SUBMITTED OR PUBLISHED UNDER ARO SPONSORSHIP DURING THIS PERIOD, INCLUDING JOURNAL REFERENCES:

None during this period

8. SCIENTIFIC PERSONNEL SUPPORTED BY THIS PROJECT AND DEGREES AWARDED DURING THIS REPORTING PERIOD:

Dr. J. R. Szedon, T. A. Temofonte and Dr. R. N. Ghoshtagore were partially supported by this contract during the period of report.

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SUBMITTED BY WESTINGHOUSE ELECTRIC CORPORATION.

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## ABSTRACT

We have studied the electrical and optical behavior of specimens from a 3x5 matrix, considering three deposition temperatures. In addition to a set of unannealed specimens at each deposition temperature, four sets of annealed samples were prepared at each temperature, for high and low temperature treatments in hydrogen and in nitrogen. By excluding results for specimens prepared at 750 Deg. C, except those receiving anneals at 1000 Deg. C in either hydrogen or nitrogen, we found clear direct effects of annealing on all the parameters of preliminary interest. The results of spectroscopic ellipsometry analysis indicate that the film structure of the specimen with the baseline silicon nitride is significantly different from the films deposited at higher temperature. It does not have an ellipsometrically detectable layer of silicon dioxide at the silicon surface. The stability of the memory states associated with the pulsed write and clear conditions correlated with the final density of fast surface states, except for anomalous behavior of the 750 Deg. C, unannealed specimen. Consideration of the ellipsometry results leads us to speculate that any thin oxide film which has an electronic influence in the baseline specimens must be substantially different from those associated with the preparation of nitride films at 850 Deg. C. From this base, we can define a clearer route to optimize and understand the behavior of MNOS structures in memory device applications.

## 1. INTRODUCTION

### 1.1 Objectives

The purpose of the work reported here has been to explore the prospects for optimizing the important memory parameter characteristics of MNOS devices with regard to preparation and annealing parameters which are compatible with a practical fabrication sequence. Furthermore, the extended purpose is to understand the effects of the processing and annealing parameter variations in terms of the physical and chemical nature of MNOS structures.

### 1.2 Approach

The approach we used was primarily empirical. A 3x5 matrix of deposition temperatures and annealing conditions for the silicon nitride was defined. We used a baseline processing sequence for MNOS memory chips to deposit a gate insulator at a temperature of 750 Deg. C. We also prepared samples at two higher deposition temperatures, 800 and 850 Deg. C. In addition to unannealed specimens of insulators, for which the maximum temperatures were those encountered during deposition, other samples - with insulators prepared at each of these temperatures - were heat-treated in hydrogen and in nitrogen at two temperatures higher than the deposition temperature in each case. The details of the annealing temperatures for the matrix are given in Table 1.

For each element in the deposition/annealing matrix, two different types of substrates were used. One type was the same as that

Table 1. Matrix of deposition and annealing conditions for silicon nitride film specimens used in this work.

| Deposition Temperature<br>in Deg. C | Ambient Gas<br>Annealing Temperature in Deg. C |                  |      |                  |      |
|-------------------------------------|------------------------------------------------|------------------|------|------------------|------|
|                                     | No anneal                                      | Hydrogen anneal  |      | Nitrogen anneal  |      |
|                                     |                                                | T1=800<br>T2=900 | 1000 | T1=800<br>T2=900 | 1000 |
|                                     |                                                | *                |      |                  |      |
| 750                                 | [13]                                           | [23]<br>@ T1     | [33] | [43]<br>@ T1     | [53] |
| 800                                 | [12]                                           | [22]<br>@ T2     | [32] | [42]<br>@ T2     | [52] |
| 850                                 | [11]                                           | [21]<br>@ T2     | [31] | [41]<br>@ T2     | [51] |

\*  
Brackets denote specimen designation.

used for memory circuit fabrication, having an epitaxially-grown n-type layer on a p-type substrate. The other type was similar except for having a boron-diffused grid at the surface of the epitaxial layer. The ungridded substrates were used, in part, for capacitors to permit a rapid survey of effects on the insulator charge density of the matrix variations. Other portions of the ungridded substrates were intended to be used for ellipsometric characterizations.

The gridded substrates were intended to provide for minority carrier injection in capacitors used to study the consequences of matrix variables on the dynamic properties of the MNOS structures. Zirinsky has noted that such gridded structures permit the simulation of minority carrier injection properties of FETs which are important in dynamic characterizations of memory behavior for pulses as short as one (1) microsecond. Since fabrication of the gridded capacitors is much simpler than preparation of memory FETs, those specimens should be freer of the influences of irrelevant processing effects which could be present with FETs. Since the integrity of the nitride films was not deliberately disturbed prior to annealing, e. g. by the opening of contact windows for FETs, the hydrogen annealing results in this study are expected to differ from those in which the lateral diffusion of (2) hydrogen from window openings was possible.

Specifically, our approach was to survey the insulator charge behavior in the ungridded capacitor samples in order to broadly characterize initial effects of the matrix variables on flat-band voltage. We also used the gridded capacitor specimens in a similar fashion to obtain more detailed information in the manner of

(1)  
Zirinsky. We examined deposition and annealing influences on the density of fast surface states ( using the difference in voltage between fixed capacitance values for the inversion and near flat-band portions of the C-V curves) and on the inferred threshold voltage for memory FETs (from the voltage at the minimum of the C-V curves). Switching behavior for static and pulse conditions were also established. On the basis of this information, gridded capacitor specimens from half of the matrix were characterized in terms of degradation due to repetitive switching.

Initially we had planned to use the multiple internal reflection (MIR) technique for infra-red spectroscopy to assess matrix influences on hydrogen and silicon bonds on selected specimens. (3) Logistically, it was not feasible to prepare MIR specimens for each of the matrix conditions. Furthermore, the intended collaborator for the MIR study could not guarantee his participation within the available time. As an alternative to the MIR technique, we elected to use spectroscopic ellipsometry (SE) to assess physical and (gross) chemical effects in MNOS structures which were variously prepared or annealed. With the SE method, no information on the details of chemical bonding is provided. The technique can sensitively indicate changes in properties associated with the optical behavior of multi-layered film structures. It has been applied to studies of MNOS specimens. (4) With SE evaluation, specimens are physically similar to those used for electrical studies. In addition, we were able to arrange for a collaborative effort on SE measurement of selected specimens.

## 2. EXPERIMENTAL PROCEDURE

### 2.1 Film preparation.

Table 1 in Section 1.2 gives the 3x5 matrix of film deposition and annealing conditions which were used for this work. All of the silicon nitride films were deposited using a low pressure, chemical vapor deposition (LPCVD) technique at 0.5 Torr. The final thickness of the nitride films was  $465 \pm 20$  Angstroms. Prior to the deposition, all substrates were etched for 60 s in a 1:100 solution of hydrofluoric acid in water, then they were loaded immediately into the LPCVD reactor.

Two kinds of 7.5 cm (3 ") diameter silicon substrates were used to prepare the specimens. Both kinds were p-type (20 to 40 ohm-cm) with an n-type epitaxial surface layer ( $13 \pm 1$  micrometer thick) of 3 to 6 ohm-cm resistivity. The n-type epitaxial layer on half the substrates was boron-diffused at 900 Deg. C to a depth of  $1.65 + 0.25$  micrometers in a mesh pattern to produce a p<sup>+</sup> grid having a sheet resistance of about 15 ohms/square. The grid lines were 5.6 micrometers wide with a center-to-center spacing of 75 micrometers, covering about 14.7% of the wafer surface.

The purpose of the grid was to provide an adequate supply of minority carriers at the surface of the n-type epitaxial layer under conditions of negative metal-to-silicon bias. For large values of such bias the carriers provide tunneling current from the silicon. During capacitance-voltage (C-V) characterization of the charge state of the

insulators, the minority carriers permit an inversion layer capacitance response of the semiconductor surface space-charge region which provides information in addition to that which can be obtained on ungridded capacitor samples. The primary use of the ungridded wafers was to provide film specimens for ellipsometric measurements.

After the silicon nitride films were prepared on the substrates, the lots scheduled for annealing in hydrogen or nitrogen received those treatments within the LPCVD reactor before being removed and exposed to the air. This was done to minimize any effects of residual water vapor during the annealing procedures.

## 2.2 Device Fabrication.

In the preparation of capacitor structures for electrical measurements, the processing steps were selected to correspond as closely as possible to those used in the production of MNOS memory circuits at the Westinghouse Advanced Technology Division. Photoresist was used to protect the silicon nitride on the wafer top surface while the back surface was plasma-etched to permit forming an ohmic back contact. After removal of the photoresist, layers of aluminum (1 micrometer thick) were thermally evaporated at 40 Angstroms/second onto both the front and back surfaces of the wafers which were held at 300 Deg. C. With the back aluminum protected, an array of circular capacitors was photolithographically delineated in the front layer of aluminum. Each module in the array consisted of three capacitors which were 0.0005, 0.0047, and  $0.019 \text{ cm}^2$  in area. After removal of the photoresist, the wafers were heated for 25 min in flowing nitrogen at 450 Deg. C to sinter the back aluminum contacts.

### 2.3 Electrical Measurement Details.

To characterize the memory behavior of the capacitors on this program, we used a Pulsed C-V Tester which was designed for earlier work (5) at Westinghouse. The system consists of a specially designed sequencer, a Boonton Model 72AD digital capacitance meter, a ramp voltage supply, a pulse voltage supply, and a double-pole double-throw coaxial relay with type BNC connectors. The relay connects the device under test either to the meter for measurement under ramped bias, which is provided through the meter, or to the pulse voltage supply. The relay and the timing of the ramp and the pulse supplies are controlled by the sequencer. Once initiated, the sequence proceeds automatically through a number of phases, whose status is indicated by LEDs.

In the first phase, DC bias of either -20 V (for writing into the device) or +20 V (for clearing) is presented to the device under test for a period of 10 sec. Next, the relay switches the device to the pulse supply. If no pulse is desired, as in the case of DC clear and DC write conditions, a pulse of zero amplitude for 100 microseconds is selected. If pulse clearing is desired, a pulse of +25 V amplitude and 100 microsecond duration is used. For pulse writing, the amplitude is -20 V and the duration is 100 ms. The sequencer activates the relay next, and the device is connected to the meter at 0 V for 1 s before the ramp bias voltage is applied for a 20 s interval during the measurement. The amplitude of the bias ramp is different depending on the write or clear state which is of interest. Specific values are given below in Section 3.3.2.

## 2.4 Spectroscopic Ellipsometry.

Six samples of variously deposited and annealed films of silicon nitride were supplied to Professor K. Vedam of the Materials Research Laboratory at the Pennsylvania State University. The specimens were those designated as 11, 31, 51, 13, 33, and 53 in Table 1 of Section 1.2. These films were deposited at either 750 or 850 Deg. C. For each deposition temperature, one sample had been annealed at 1000 Deg. C in nitrogen; another, in hydrogen at the same temperature; and a third had not been annealed. All six specimens were non-destructively measured using a spectroscopic ellipsometer with a rotating analyser. Three of the specimens were identified as being of special significance due to their memory behavior: the unannealed films deposited at 750 and 850 Deg. C and the film deposited at 850 Deg. C and annealed in hydrogen at 1000 Deg. C. The data for these three specimens was analyzed in the manner of Theeten et al.<sup>(6)</sup> A summary of the results is given in Section 3.4. More details appear in Appendix A.

### 3. RESULTS

#### 3.1 Initial Static Characterization

Preliminary characterizations of all matrix specimens were made in terms of high frequency (1MHz) capacitance-voltage (C-V) measurements of the gridded and ungridded wafers. Three circular dot capacitors with areas of 0.0005, 0.0047, and 0.019 cm<sup>2</sup> were used. For the ungridded specimens, the presence of the junction at the interface of the epitaxial layer and the substrate introduces a space charge capacitance in series with the MNOS capacitor. This capacitance can reduce the measured capacitance for accumulation conditions at the surface of the epi-layer below that expected for the MNOS insulator capacitance. With the capacitor sizes available to us, this effect was significant only for the medium and large dots. Consequently, we used the smallest capacitor for the C-V characterizations which are discussed below. An example of the C-V behavior for a small capacitor on an ungridded substrate with the unannealed, baseline silicon nitride film is shown in Fig. 1, at the left.

For the gridded wafers, similar consideration must be given to the effect of series capacitance due to the junction formed between the diffused grid and the epi-layer. In that case, the space-charge region capacitance of the grid is only about one tenth that of the insulator capacitance for the area above the grid. Under positive metal-silicon bias, the net capacitance presented by the grid area is limited to the

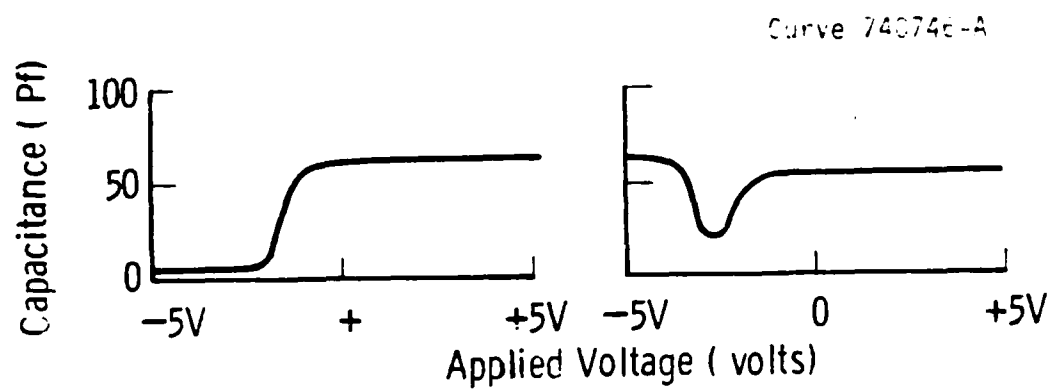


Figure 1. Examples of C-V behavior at 1 MHz for silicon nitride films deposited at 750 Deg. C on plain (left) and gridded (right) substrates.

(low) value arising from the grid/epi-layer junction. Thus, for bias which accumulates the surface of the n-type epi-layer, the MNOS capacitance over the grid - which accounts for 15% of the dot area - may not be measured. Under some conditions, the area supplying grid capacitance may extend beyond the area of the metal dot, and less than 15% subtraction can occur. For bias which inverts the surface of the n-type epi-layer, that inversion layer should be in good electrical contact with the accumulated surface of the grid area. In such a situation, the space-charge region of the grid is effectively shunted and the measured capacitance is that of the insulator for the full area of the metal dot. The consequences of these effects are illustrated at the right in Figure 1 for the unannealed, baseline silicon nitride specimen on a gridded substrate.

Effects of various deposition temperatures and annealing conditions on the flat-band voltage ( $V_{FB}$ ) values of the MNOS capacitors are given in Table 2. Note that the values of flat-band voltage generally become more positive with increasing deposition temperature and that the lowest absolute values were produced by annealing in hydrogen. The most negative values of flat-band voltage resulted from the baseline process (750 Deg. C deposition, no annealing); the most positive values, from the anneal in nitrogen at 900 Deg. C of the nitride deposited at 850 Deg. C.

For the gridded specimens, deposition and annealing variations affected the voltage,  $V_{min}$ , at which the minimum value of capacitance was measured and the width,  $\Delta V_{CFB}$ , of the C-V curve at the flat-band capacitance value. These results are shown in Tables 3 and 4.

Table 2. Effect on flat-band voltage values of the deposition and annealing conditions under which the nitride films were prepared.

| Deposition Temperature<br>in Deg. C | Ambient Gas<br>Annealing Temperature in Deg. C |                  |        |                  |        |
|-------------------------------------|------------------------------------------------|------------------|--------|------------------|--------|
|                                     | No anneal                                      | Hydrogen anneal  |        | Nitrogen anneal  |        |
|                                     |                                                | T1=800<br>T2=900 | 1000   | T1=800<br>T2=900 | 1000   |
|                                     |                                                | *                |        |                  |        |
| 750                                 | -1.6 V                                         | -1.3 V<br>(T1)   | -0.6 V | -0.9 V<br>(T1)   | +1.6   |
| 800                                 | -0.4 V                                         | -0.2 V<br>(T2)   | -0.7 V | +2.0 V<br>(T2)   | +1.9 V |
| 850                                 | +2.0 V                                         | -0.5 V<br>(T2)   | -0.3 V | +2.5 V<br>(T2)   | +1.4 V |

\*  
Value of flat-band voltage from C-V curve for ungridded capacitor specimen.

Table 3. Effect on the voltage at the minimum capacitance of the C-V curve of the deposition and annealing conditions under which the nitride films were prepared.

| Deposition Temperature<br>in Deg. C | Ambient Gas<br>Annealing Temperature in Deg. C |                  |        |                  |        |
|-------------------------------------|------------------------------------------------|------------------|--------|------------------|--------|
|                                     | No anneal                                      | Hydrogen anneal  |        | Nitrogen anneal  |        |
|                                     |                                                | T1=800<br>T2=900 | 1000   | T1=800<br>T2=900 | 1000   |
| 750                                 | -2.4 V                                         | -2.3 V<br>(T1)   | -1.5 V | -2.0 V<br>(T1)   | -0.5 V |
| 800                                 | -1.8 V                                         | -1.3 V<br>(T2)   | -1.6 V | -0.6 V<br>(T2)   | N. A.  |
| 850                                 | -0.7 V                                         | -1.4 V<br>(T2)   | -1.4 V | +0.2 V<br>(T2)   | +0.1 V |

\*  
Value of  $V_{\min}$ , the voltage at the capacitance  
minimum of the C-V curve for gridded capacitor  
specimens.

Table 4. Effect on the width of the C-V curve at the flat band capacitance value of the conditions under which the nitride films were prepared.

| Deposition Temperature<br>in Deg. C | Ambient Gas<br>Annealing Temperature in Deg. C |                  |        |                  |        |
|-------------------------------------|------------------------------------------------|------------------|--------|------------------|--------|
|                                     | No anneal                                      | Hydrogen anneal  |        | Nitrogen anneal  |        |
|                                     |                                                | T1=800<br>T2=900 | 1000   | T1=800<br>T2=900 | 1000   |
|                                     |                                                | *                |        |                  |        |
| 750                                 | 1.75 V                                         | 1.17 V<br>(T1)   | 2.06 V | 2.36 V<br>(T1)   | 5.75 V |
| 800                                 | 2.27 V                                         | 1.57 V<br>(T2)   | 1.18 V | 4.04 V<br>(T2)   | N. A.  |
| 850                                 | 5.21 V                                         | 1.57 V<br>(T2)   | 2.02 V | 4.20 V<br>(T2)   | 4.51 V |

\*  
Value of  $\Delta V_{CFB}$ , the width in voltage at the flat-band capacitance of the C-V curve for gridded capacitor specimens.

Physically, the value of  $V_{\min}$  corresponds to the threshold voltage of an FET incorporating the structure of the MNOS capacitor. The parameter  $\Delta V_{\text{CFB}}^{(1)}$  is a measure of the density of fast surface states at the silicon-insulator interface, assuming that variations of dopant impurity concentration and of surface potential are negligible over the area of the capacitor.

The foregoing observations regarding the changes in C-V behavior give some insight into the effect of deposition and annealing conditions on the gross behavior of insulator charge and of surface states. In the next section, we survey the effects of selected conditions on the memory-related properties of the MNOS structures.

### 3.2 Switching Characteristics

All static and pulsed switching characterizations were carried out on capacitors formed on the substrates with diffused grids. This insured an adequate supply of minority carriers for trap charging with negative polarity Write pulses. The apparatus used for the measurements is described briefly in Section 2.3.

Four types of bias conditions were used in the characterization. Each was followed by a 1 second interval with 0 V applied across the capacitor before the C-V behavior was measured for a single ramped bias lasting 20 seconds. These conditions, with the range of ramped bias for measurement, are defined in Table 5.

Figure 2 shows a set of C-V curves taken (and correspondingly labeled) after each of the conditions defined in Table 5 for a gridded capacitor using the baseline silicon nitride (750 Deg. C, no anneal). A typical set of curves is shown in Figure 3 for a specimen of the

Table 5. Definition of conditions for writing and clearing gridded capacitors during memory tests, and of the limits of the 20 s ramped voltage excursion used subsequently for the C-V measurement.

| Condition number. | Mnemonic label | Amplitude, duration; hold; pre-ramp amplitude, duration; ramp limits for 20 s sweep.                                      |
|-------------------|----------------|---------------------------------------------------------------------------------------------------------------------------|
| 1.                | DC Write       | -20 V, 10 s;<br>hold: 0 V, 1 s;<br>pre-ramp: 0 V, 1.5 s;<br>ramp: 0 to -14 V.                                             |
| 2.                | DC Clear       | +20 V, 10 s;<br>hold: 0 V, 1 s;<br>pre-ramp: +6 V, 1.5 s;<br>ramp: +6 to -14 V.                                           |
| 3.                | Pulse Clear    | DC Write (no measurement);<br>+25 V, 100 microseconds;<br>hold: 0 V, 1 s;<br>pre-ramp: +6 V, 1.5 s;<br>ramp: +6 to -14 V. |
| 4.                | Pulse Write    | DC Clear (no measurement);<br>-20 V, 100 milliseconds;<br>hold: 0 V, 1 s;<br>pre-ramp: 0 V, 1.5 s;<br>ramp: 0 to -14 V.   |

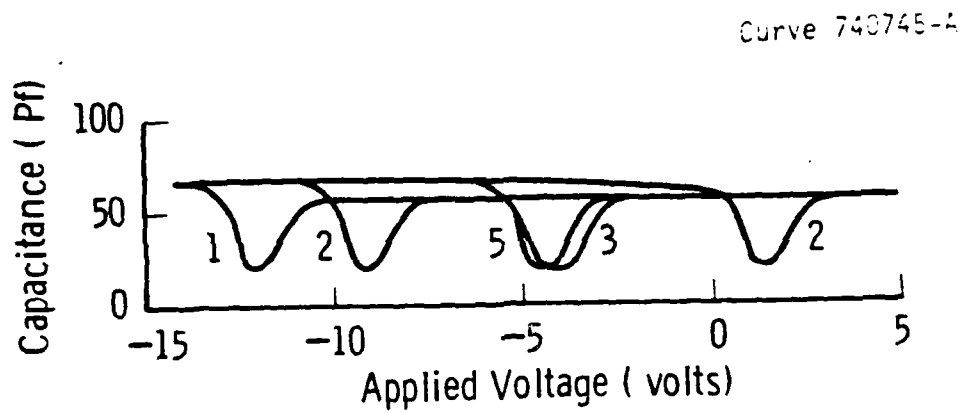


Figure 2. Typical C-V behavior for unannealed silicon nitride films deposited at 750 Deg. C for DC and pulsed Write and Clear conditions which are defined in Table 5.

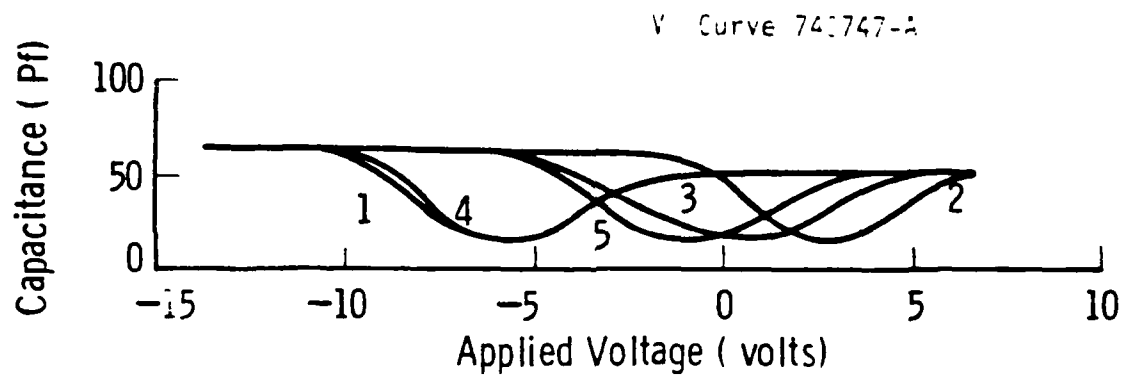


Figure 3. Examples of C-V behavior for a silicon nitride film deposited at 750 Deg. C and annealed at 1000 Deg. C in nitrogen. Labels indicate the switching conditions of Table 5.

baseline nitride which was subsequently annealed at 1000 Deg. C in nitrogen. Note that these curves are shifted to more positive voltages than those of Figure 2 for the unannealed specimen. The curves for the annealed nitride show broadening between the accumulation and inversion branches, indicating an increase in fast surface state density as a result of the anneal. This matter will be treated in more detail with regard to experiments with endurance during repetitive pulsing.

Complete sets of curves of the type shown in Figures 2 and 3 were obtained on 15 specimens from the original matrix of Table 1. (A gridded wafer was not available with a specimen of the nitride which had been deposited at 800 Deg. and annealed at 1000 Deg. C). Values of  $V_{min}$  for all four write/clear conditions of Table 5 are given in Figure 4.

There are a number of noteworthy aspects of the results shown in Figure 4. (1) The largest DC memory window (13 V) was obtained for the 750 Deg. C specimens (with and without the nitrogen anneal at 800 Deg. C) and for the unannealed films deposited at 800 Deg. C. (2) Specimens of films deposited at 750 Deg. C and annealed in nitrogen at 1000 Deg. C had the smallest DC memory window (8.6 V). (3) The widest pulsed memory window (6.9 V) was for the 850 Deg. C film which were annealed at 1000 Deg. C in nitrogen. (4) The smallest pulsed memory window was for the baseline specimens.

The survey just described suggests that some deposition and/or annealing conditions are more desirable than others as regards maximizing window sizes. However, a "best" choice cannot be made in the absence of information on the retention and endurance characteristics for the various specimens. The limited scope of the present program

Conditions, Sample No.

850°C Nitride, 11

H<sub>2</sub> { 900°C, 21

Anneal { 100°C, 31

N<sub>2</sub> { 900°C, 41

Anneal { 1000°C, 51

800°C Nitride, 12

H<sub>2</sub> { 900°C, 22

Anneal { 1000°C, 32

N<sub>2</sub> { 900°C, 42

Anneal { 1000°C, 52

750°C Nitride, 13

H<sub>2</sub> { 800°C, 23

Anneal { 1000°C, 33

N<sub>2</sub> { 800°C, 43

Anneal { 1000°C, 53

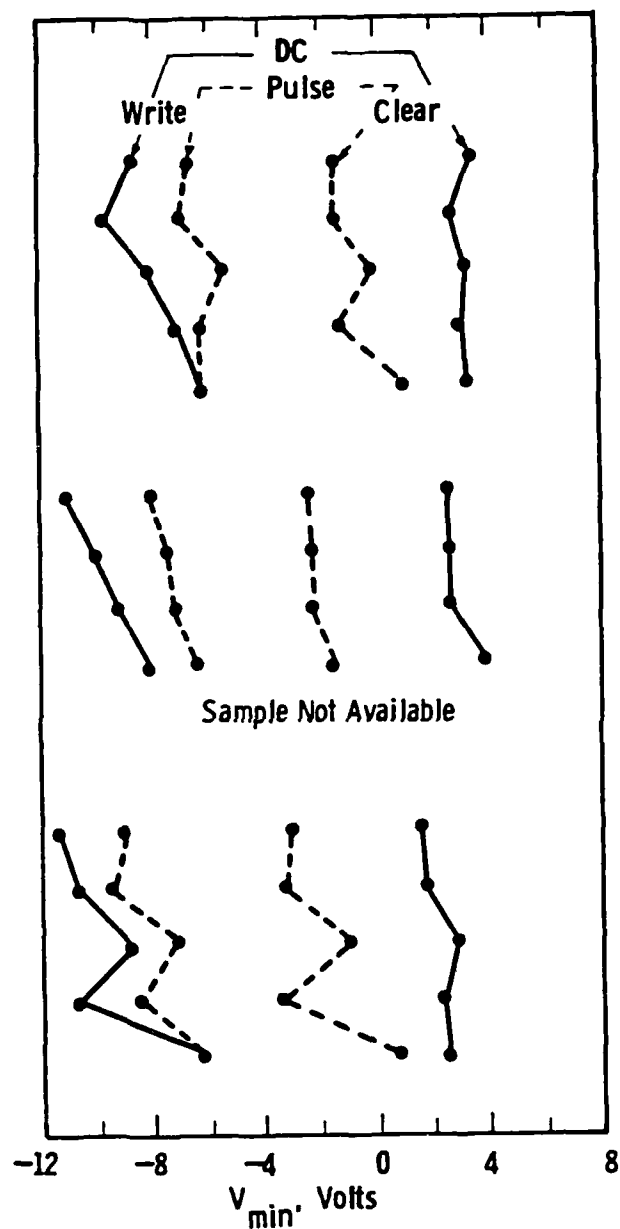


Figure 4. Comparisons of DC and pulsed memory states for all the nitride specimens from the processing matrix of Table 1.

forced us to restrict our attention to the endurance issue, since this will ultimately determine the practical application of a selected process. In the next section endurance results are presented.

### 3.3 Repetitively Cycled Pulsing.

#### 3.3.1 Initial Considerations

Repetitive pulse biasing was used to characterize the endurance of the various specimens. We were particularly interested in determining the sensitivity of the write/clear charge states and the DC and pulsed memory windows to the stress of such repetitive pulsing. Each sample was initially characterized using the four conditions defined in Table 5. Repetitive pulsing was then carried out for a fixed number of cycles and the samples were re-characterized. This procedure was continued until  $2 \times 10^6$  cycles were accumulated, in most cases. For selected samples, up to  $3 \times 10^7$  cycles were accumulated. The pulse frequency was 500 Hz and the pulses were 1 ms in width.

For the first measurements, the baseline samples (nitride deposited at 750 Deg., no subsequent anneal) were subjected to symmetric pulses of 25 V amplitude. After  $2 \times 10^6$  cycles the value of  $V_{\min}$  resulting from the pulse write condition was about 1 V more positive, the pulsed write/clear memory window was about 0.25 V larger, and the fast surface state density was about 30% larger than initially. Since we expected that some of the annealed specimens might exhibit smaller effects in these regards, we decided to accelerate the degradation effects by using asymmetric pulse heights of +20 and -38 V for clearing and writing, respectively.

Typical results for accelerated stressing of the baseline

specimens are given in Figures 5 and 6 in terms of the behavior of flat-band voltage and the voltage at minimum capacitance, respectively. From Figure 5, we note that the value of  $V_{FB}$  for pulse write conditions becomes 7.25 V more positive after  $2 \times 10^6$  cycles (in comparison to a 1 V positive change for the case of symmetric pulsing, described above). The pulsed memory window is virtually unchanged, while the DC memory window is reduced from a value of 15.5 V to 9.5 V.

By comparison, when  $V_{min}$  is used as the criterion, the pulse write state after stress is only 2.9 V more positive than before stress, since the net effect of surface states for the flat-band condition is stronger than for that at the onset of carrier inversion at the point of  $V_{min}$ . Also with the  $V_{min}$  criterion, the pulsed memory window is reduced slightly (by about 0.4 V), and the DC memory window is about 2.6 V smaller than before cycling. As we noted previously, the parameter  $V_{min}$  is more useful than the flat-band voltage value in characterizing the threshold voltage of memory transistors. For this reason, all remaining comparisons will be in terms of the parameter  $V_{min}$ .

### 3.3.2 Stability of Memory States.

The cycled asymmetric pulses described above were used to stress selected specimens for a total of  $2 \times 10^6$  cycles, except as noted below. Results for the endurance of the states established by DC write and DC clear are shown in Figure 7 for the cases of the films deposited at 750 and 850 Deg. C. This includes specimens which were given subsequent high temperature (1000 Deg. C) anneals in hydrogen and in nitrogen. Figure 8 presents comparable results in terms of the endurance of the states established by the pulsed write and pulsed clear

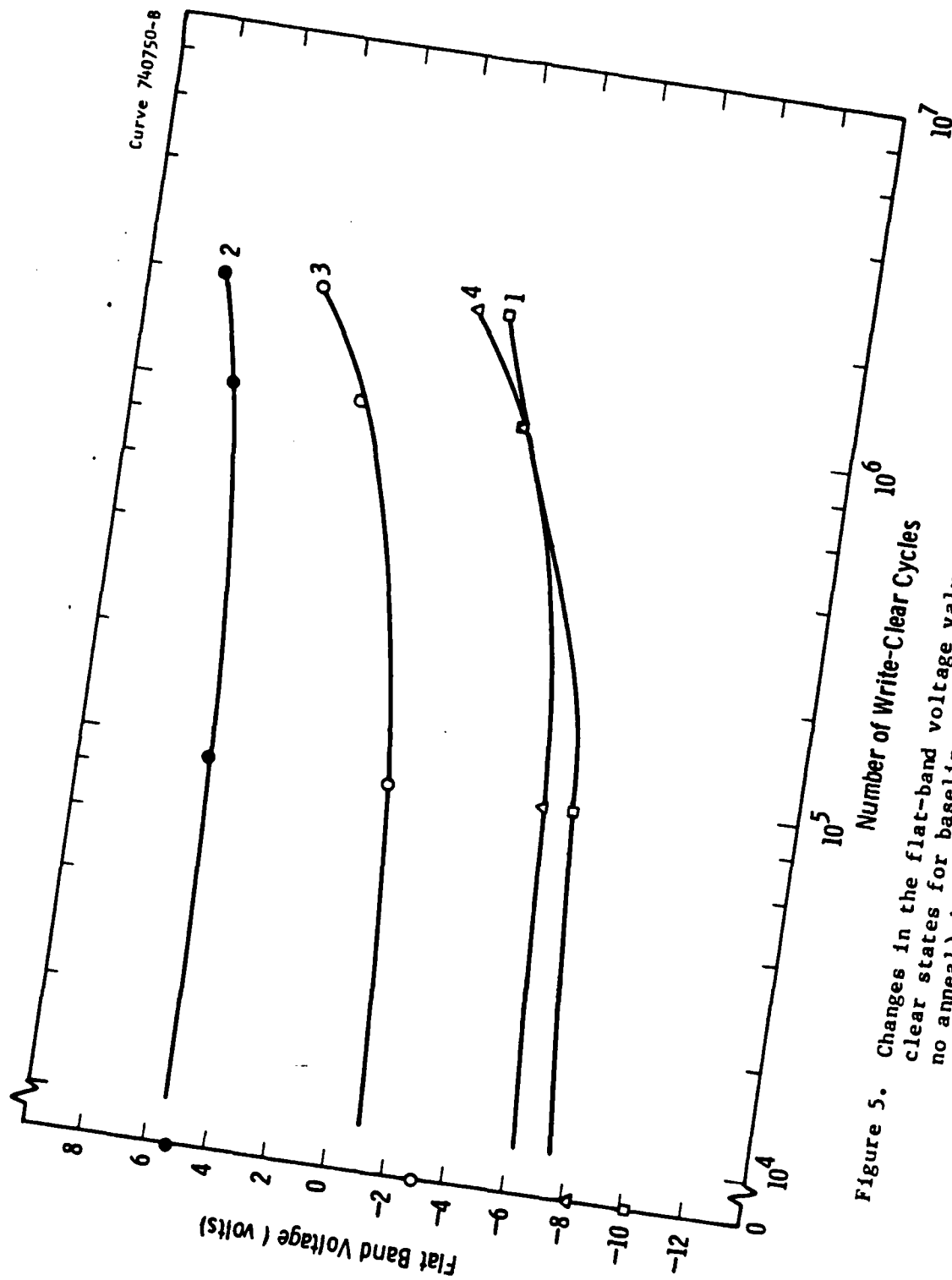


Figure 5. Changes in the flat-band voltage values of the DC write and clear states for baseline specimens (750 Deg. C deposition, no anneal) during the course of repetitive pulse cycling.

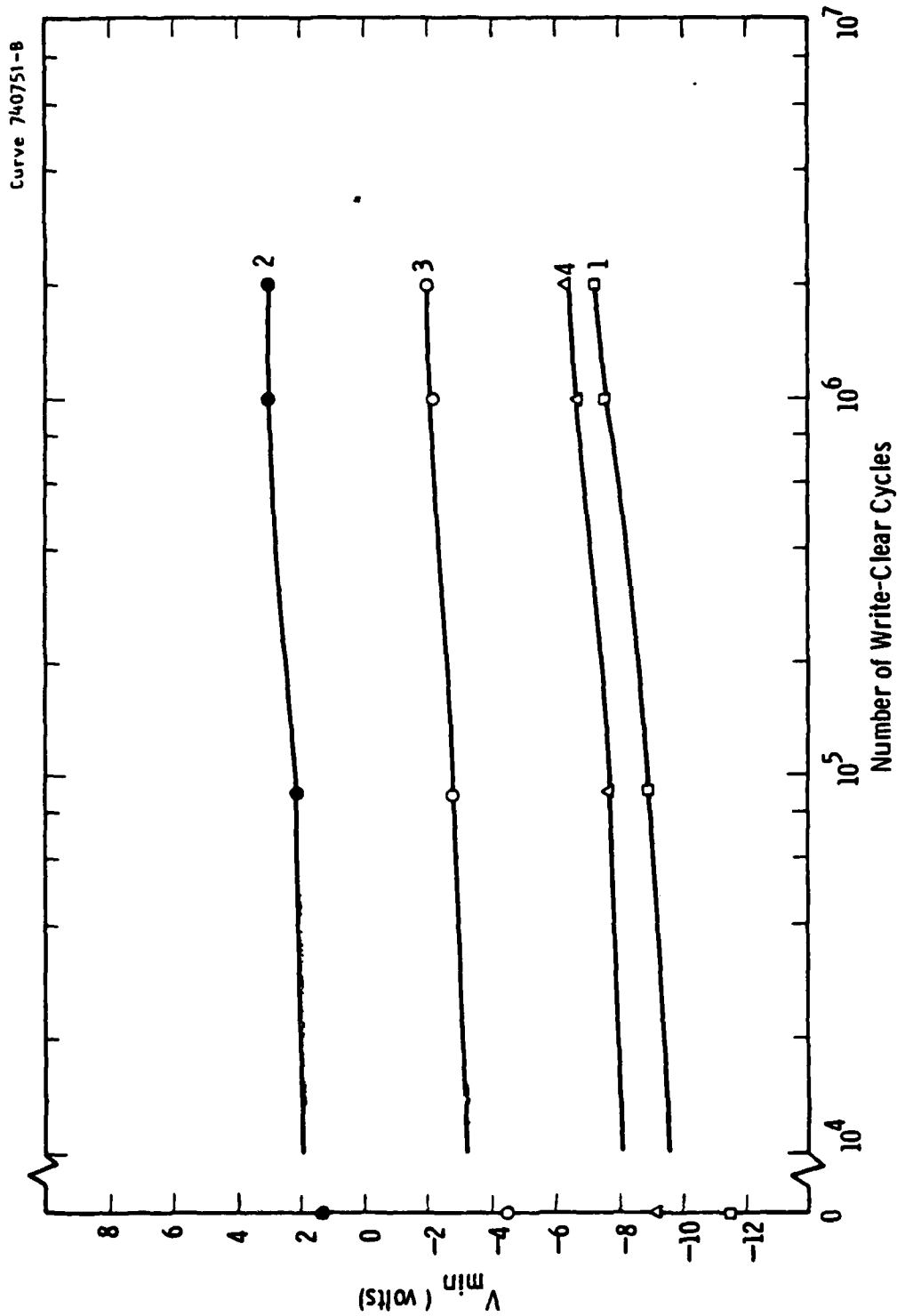


Figure 6. Changes in the voltage for minimum capacitance, corresponding to threshold voltage, for the DC write and clear states of baseline specimens during repetitive pulse cycling.

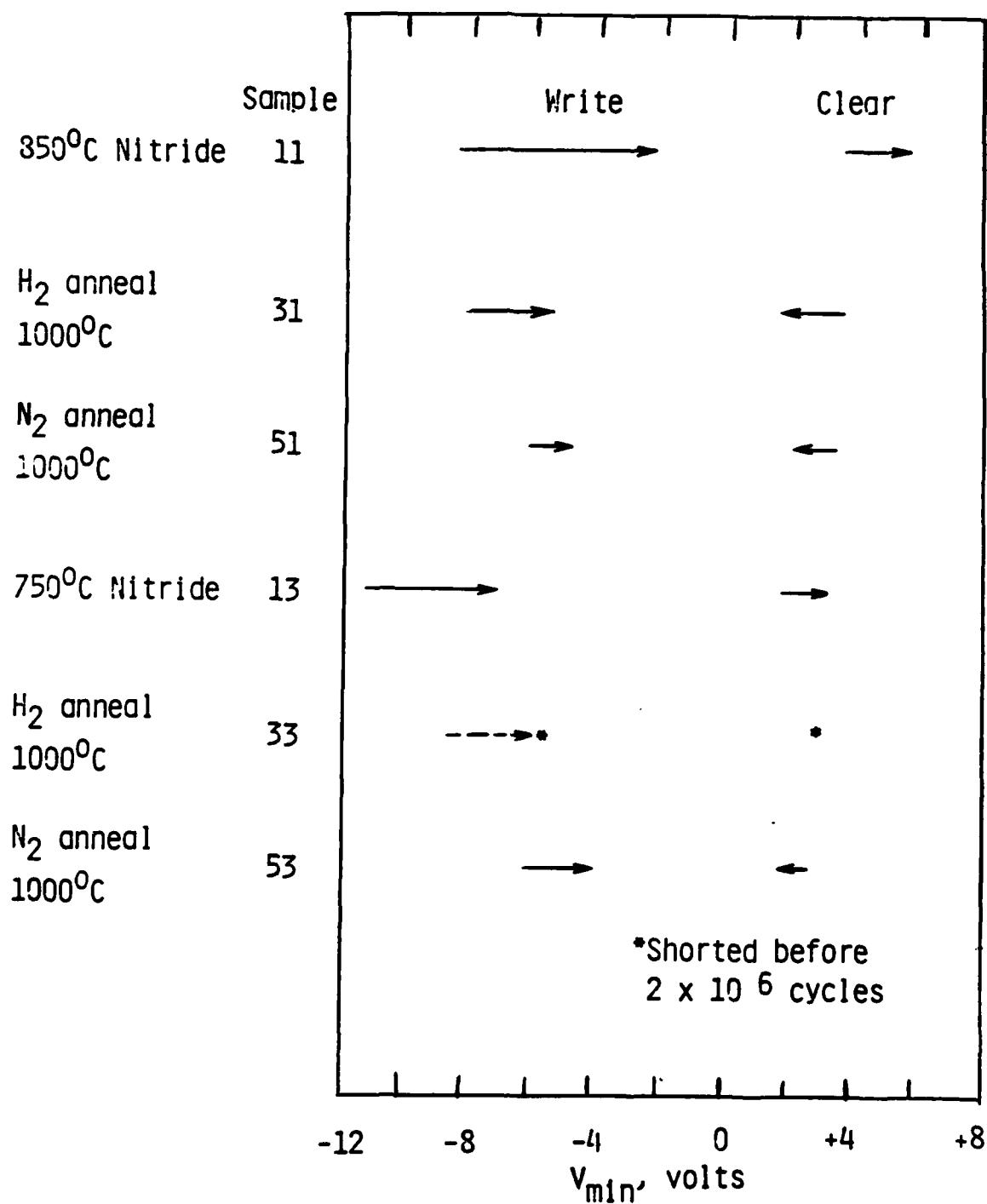


Figure 7. Comparison of the stability of the DC write and clear states for selected specimens subjected to 2 million pulsed cycles.

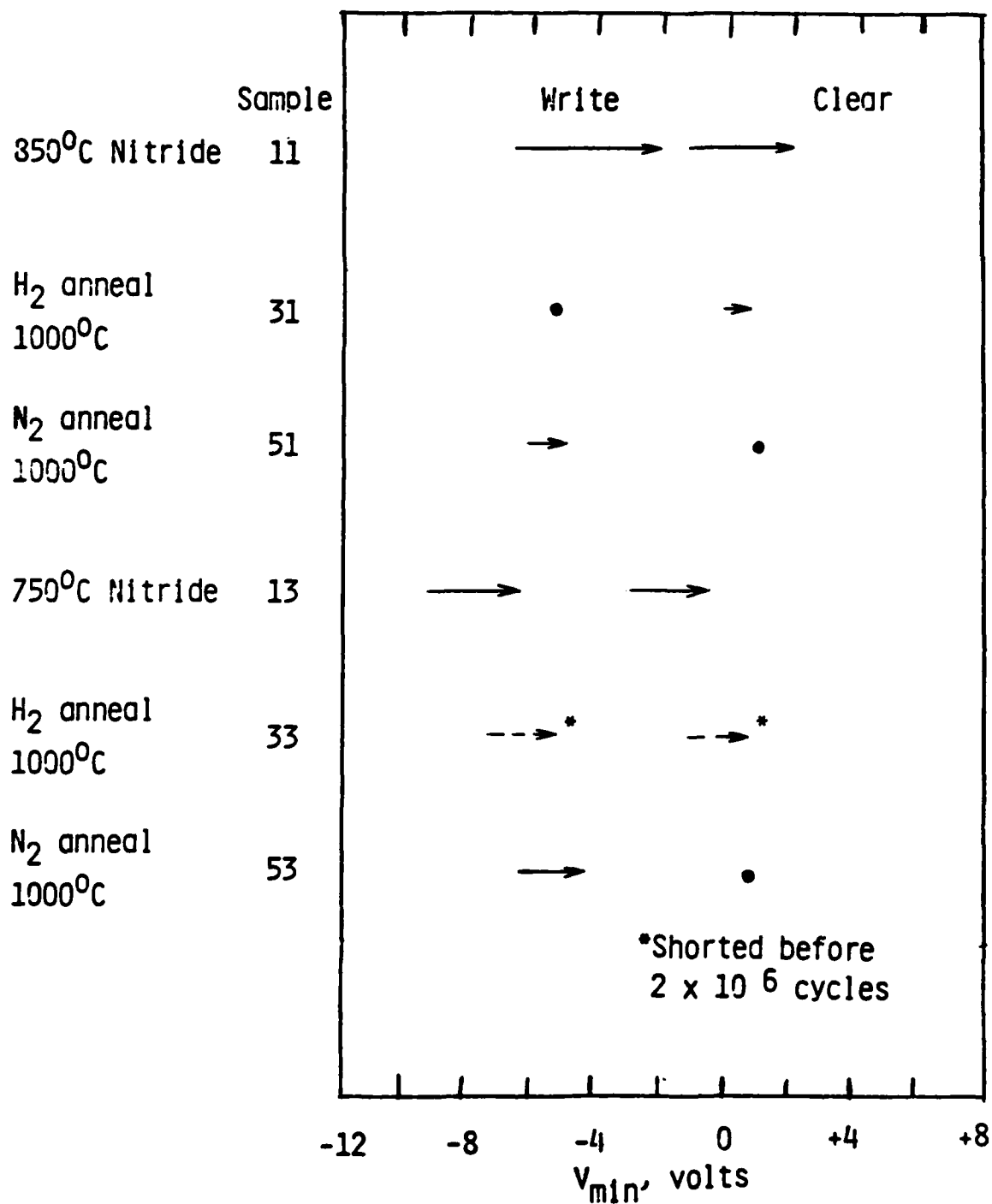


Figure 8. Relative stability of the pulsed write and clear states for selected specimens after 2 million pulsed cycles.

conditions of Table 5.

The following conclusions were drawn from the information in Figures 7 and 8:

(a) For unannealed films, endurance was better for those deposited at 750 Deg. C. In fact, the unannealed films prepared at 850 Deg. C exhibited the largest degradations in both the DC write state (+6.5 V) and in the pulsed write state (+5.0 V) of any films of the films considered.

(b) For the films annealed at 1000 Deg. C in hydrogen, those which were deposited at 750 Deg. C failed catastrophically between  $0.5 \times 10^6$  and  $2.0 \times 10^6$  cycles. On the other hand, those deposited at 850 Deg. C had more stable pulse write and pulse clear states than any other film which was tested. However, the DC write and clear states for these 850 Deg. C films showed shifts of +2.6 and -1.5 V, respectively, to cause a 4.1 V reduction in the DC window.

(c) Of the films annealed at 1000 Deg. C in nitrogen, those deposited at 850 Deg. C were more stable than those deposited at 750 Deg. C, except for the DC clear state. Note that the stability of the pulsed write and clear states for the 850 Deg. C films which were annealed in nitrogen was exceeded only by that for similarly deposited films which had been annealed in hydrogen.

(d) The change in the pulsed write state for the films deposited at 750 Deg. C and annealed at 1000 Deg. C was 1.6 times larger than that for the films deposited at 850 Deg. C and similarly annealed.

The smallest decrease in the pulsed memory window was 0.4 V, obtained for the case of the baseline specimen. By way of contrast,

the largest decrease was only 1.4 V, for the film deposited at 750 Deg. C and annealed at 1000 Deg. C in nitrogen. There was an increase (0.6 V) in the size of the pulsed memory window for the film deposited at 850 Deg. C and annealed in hydrogen at 1000 Deg. C.

In addition to producing changes in the voltages characteristic of the various memory states of the gridded capacitor specimens, repetitive pulse cycling produced changes in the density of fast surface states at the silicon/silicon dioxide interface of the MNOS structures. A summary of those changes is presented in the next section.

### 3.3.3 Effects on Fast Surface States.

In Section 3.1 we noted briefly some effects of various processing and annealing conditions on surface states. These effects were reflected in the width,  $\Delta V_{\text{CFB}}$ , between the accumulation and inversion branches of the C-V curve, measured at the flat-band capacitance value. Zirinsky, in Ref. 1, gives the relationship between the width and the density,  $N_{\text{ss}}$ , of fast surface states as:

$$\Delta V_{\text{CFB}} = \phi + q/C_{\text{ins}} (N_{\text{Si}} + N_{\text{ss}}).$$

In this expression,  $\phi$  is the band bending in the silicon at the accumulation condition of measurement,  $C_{\text{ins}}$  is the specific capacitance of the oxide and nitride layers, and  $N_{\text{Si}}$  is the areal density of minority carriers and ionized donors in the silicon. The terms  $\phi$  and  $q/C_{\text{ins}} N_{\text{Si}}$  have a combined value of about 0.8 to 1.0 V for the specimens considered. The value of  $\phi$  is approximately 0.5 V, being the amount of band-bending in the silicon for the condition of moderate inversion which corresponds to the space-charge capacitance value at flat-band.

The value for the second term is approximated from the theoretical curves presented in Sze (with the  $\phi$  term taken into account) for the doping concentration of interest, after scaling for the differences in specific capacitance values. (7)

If  $\phi$  and  $q/C_{ins Si}$  are small with respect to  $q/C_{ins ss}$ , then  $\Delta V_{CFB}$  will vary directly with  $N_{ss}$ .

In the present case, for a given sample only  $N_{ss}$  should be affected by the stress of repetitive pulsing. If we consider the change in  $\Delta V_{CFB}$  between final and initial conditions, which are respectively designated as 1 and 0, the increase in fast surface state density is then given by the expression:

$$\Delta N_{ss} = C_{ins} / q (\Delta V_{CFB,1} - \Delta V_{CFB,0}) = C_{ins} / q \Delta V.$$

Plots of  $\Delta V$  for various specimens during the course of stressing with repetitive pulses are given in Figures 9 and 10. From these data we draw several conclusions. The largest average increase in the density of fast surface states ( $7.9 \times 10^{12}$  states/cm<sup>2</sup>) due to stressing was for the baseline specimens. In contrast, films deposited at either 750 or 850 Deg. C, then annealed at 1000 Deg. C in nitrogen, exhibited slight reductions in surface state densities,  $5.6 \times 10^{11}$  and  $1.8 \times 10^{11}$  cm<sup>-2</sup>, respectively. For films annealed at high temperatures in hydrogen, increases of  $3 \times 10^{12}$  and  $1.4 \times 10^{12}$  cm<sup>-2</sup> were noted for the films deposited at 750 and 850 Deg. C, respectively. Unannealed films prepared at 850 Deg. C exhibited an average increase of about  $2.3 \times 10^{12}$  cm<sup>-2</sup>.

In short, for the films prepared at high temperature, the smallest increases in fast surface state densities due to repetitive pulsing up to  $2 \times 10^6$  cycles were associated with no annealing or

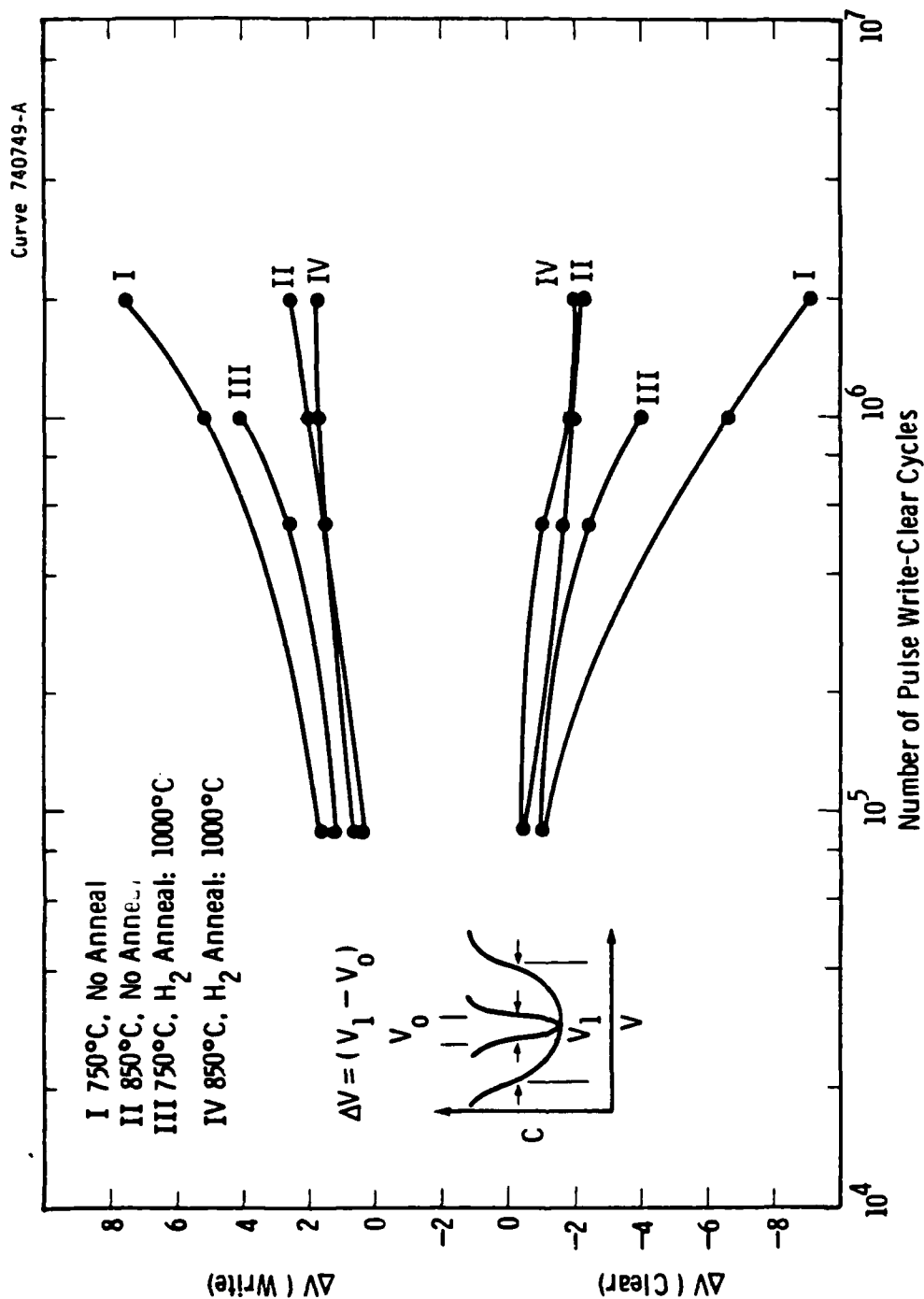


Figure 9. Change in surface state density (proportional to  $\Delta V$ ) due to pulsed cycling for specimens of as-deposited and hydrogen-annealed films which were prepared at 750 and 850 Deg. C.

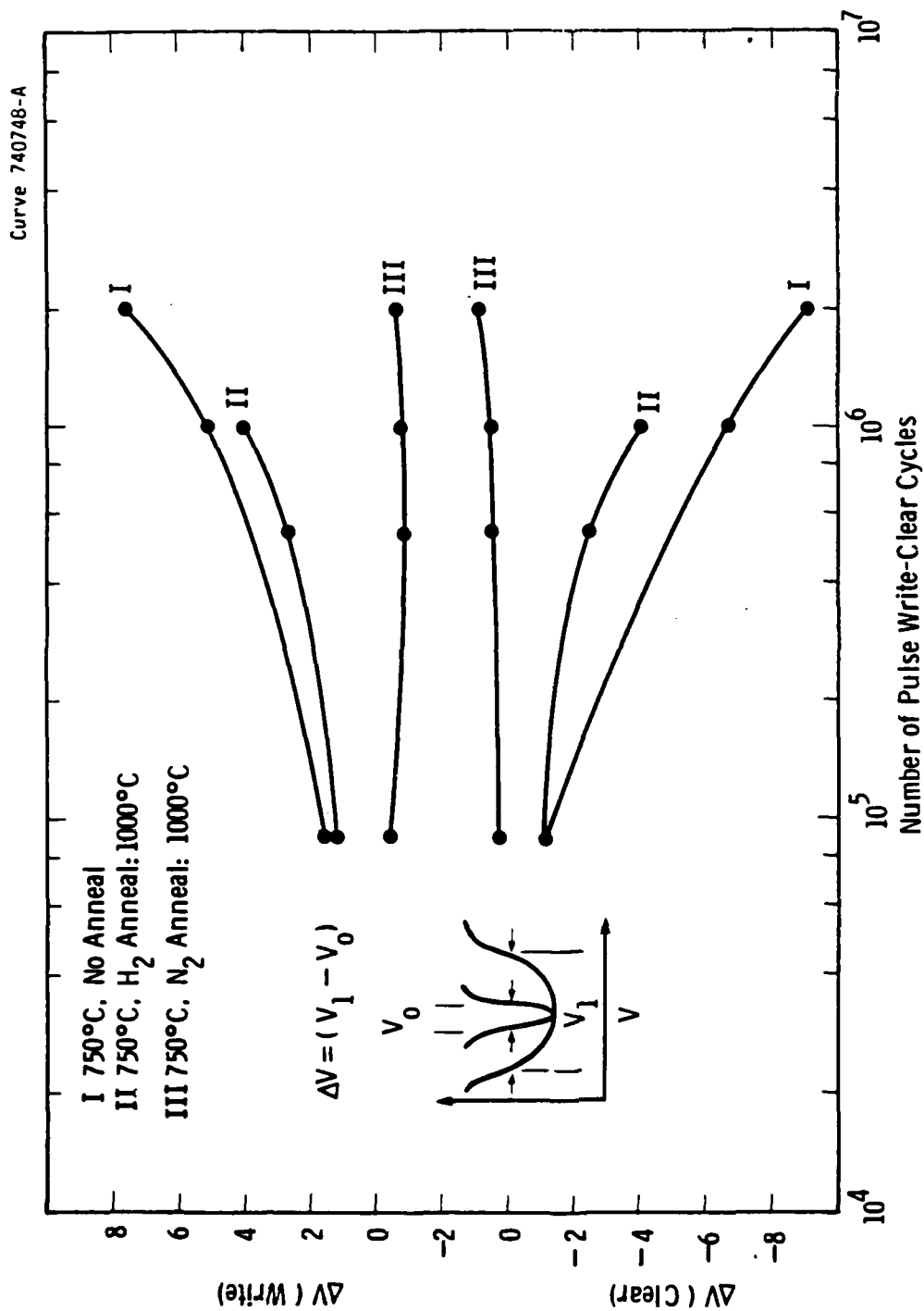


Figure 10. Cycled pulsing-induced changes in surface state density for baseline and annealed specimens of films prepared at 750 Deg. C.

annealing in hydrogen at 1000 Deg. C. This is illustrated in Figure 9. For the films annealed in nitrogen at 1000 Deg. C, there was little change in the value of  $N_{ss}$ , regardless of the temperature of preparation.

Finally, we examine the degree of correlation between final surface state density and the stability of the pulse write and the pulse clear states for various specimens over the course of  $2 \times 10^6$  cycles of pulsing. This is shown in Figure 11. Except for the case of the baseline specimen (#13, produced at 750 Deg. C and not annealed) there is very good correlation with regard to the pulse write state, as shown at the top of Figure 11. For the pulse clear state stability, sample 13 again appears to be distinct from the others. In addition, sample 53 (deposited at 750 Deg. C and annealed in nitrogen at 1000 Deg. C) does not follow the regression line for the remaining specimens. For the other specimens, there appears to be a reasonably linear relationship of the change in the voltage of the pulse write or the pulse clear states with the final value of fast surface state density.

Without ambiguity, consideration of the pulse write state stability shows specimen 31 (850 Deg. C deposition and 1000 Deg. C anneal in hydrogen) to be best in terms of our evaluation. By the same standard, specimen 11 (850 Deg. C deposition, no anneal) is the worst. Considering the pulse clear state, we conclude that specimens 31, 51 (like 31, but annealed at 1000 Deg. C in nitrogen), and 53 (like 13, but annealed at 1000 Deg. C in nitrogen), are similar in desirable behavior. Furthermore, for this state there seems to be a slightly weaker correlation between the change in voltage of the state due to repetitive

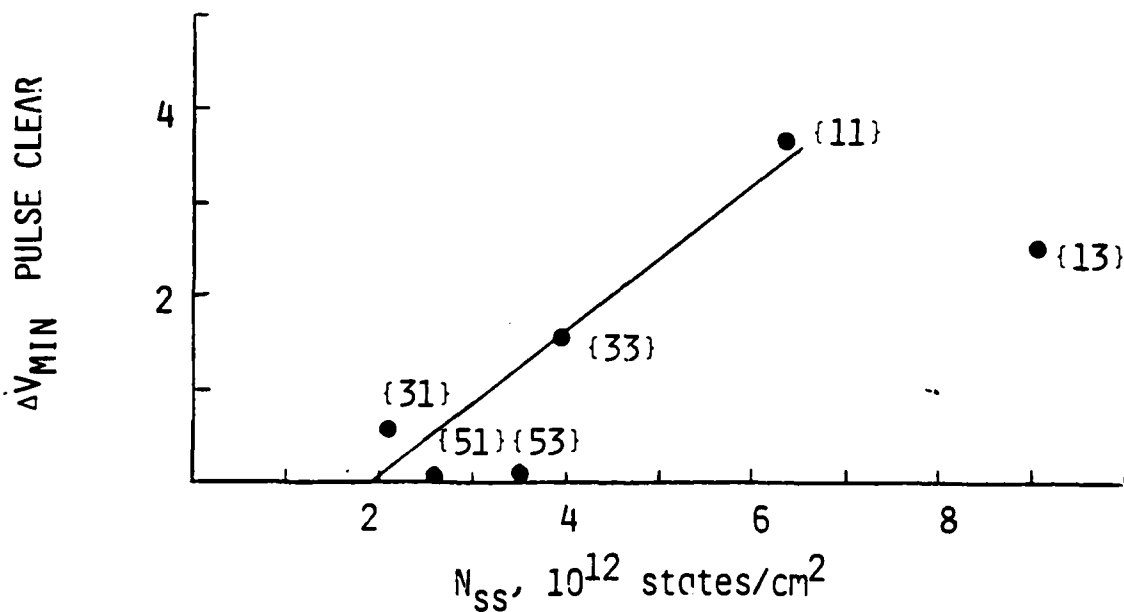
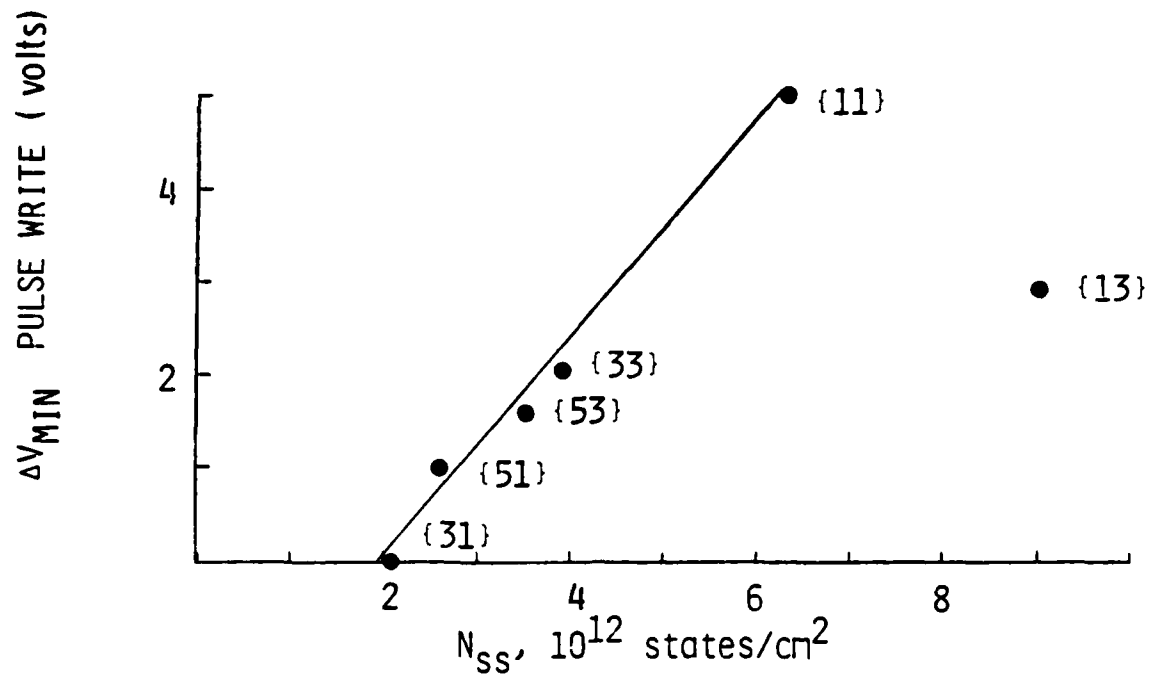


Figure 11. Correlation of pulsed memory state stability and the final density of fast surface states after extensive cycled pulsing.

pulsing and the final surface state density. We shall be considering some of these conclusions again in the next section with regard to the spectroscopic ellipsometry measurements.

### 3.4 Spectroscopic Ellipsometry

The analysis of the raw data obtained in the spectroscopic ellipsometry evaluations at Penn State was done for three specimens: SE#1, SE#2, and SE#5. These correspond to specimens 13, 11, and 31, respectively, in the matrix of Table 1. Specifically, the first in each series is the unannealed baseline specimen which was deposited at 750 Deg. C. The second in the series is the unannealed specimen of nitride which was deposited at 850 Deg. C. The last in the series was also deposited at 850 Deg. C, but it was annealed in hydrogen at 1000 Deg. C.

From the analysis, specimen SE#1 - the baseline sample - emerges as being distinct from the other two. By the least squares analysis, the optical data are best fit using a model of a single film, 495 Angstroms-thick, composed of a mixture of 90% silicon nitride and 10% silicon dioxide.

The data for the unannealed specimen prepared at 850 Deg. C are fit best by a three-layer model: 496 Angstroms of a mixed nitride/oxide (92% and 8%, respectively) on top of an optically absorbing layer (10 Angstroms thick) of amorphous silicon which lies atop another layer (19 Angstroms thick) composed of 58% silicon dioxide and 42% voids.

For the last specimen which was annealed in hydrogen at 1000 Deg. C after deposition at 850 Deg. C, the data are fit by a consistent model, in comparison with the unannealed specimen. The

thickness of the outermost layer was reduced slightly to 481 Angstroms, as was its silicon dioxide content (to 5%). The thickness of the amorphous silicon layer was only slightly modified. Finally there was an indicated reduction in the silicon dioxide content of the layer next to the silicon to 37%.

It is interesting that the unannealed baseline specimen gives no indication optically of a thin silicon dioxide layer, considering that such a layer is an intrinsic part of the electronic model for the MNOS memory device. We speculate that the optical results may be significant in future work to rationalize the poor correlation of memory state stability and final density of fast surface states which was noted in Section 3.3.3 with regard to Figure 11.

#### 4. SUMMARY

##### 4.1 General Observations.

The objectives of this program have been met. We have used as a baseline process the deposition of silicon nitride at 750 Deg. C in an LPCVD reactor. This process is used at the Westinghouse Advanced Technology Laboratories to produce MNOS structures for memory chips. We used a 3x5 matrix for which depositions were done at 700 Deg. C (the baseline condition) and at two higher temperatures (800 and 850 Deg. C). In addition to a set of unannealed specimens at each deposition temperature, four sets of annealed samples were prepared at each temperature, for high and low temperature treatments in hydrogen and in nitrogen. In addition to plain silicon wafers, substrates were also used which contained a boron-diffused grid pattern. The latter were used in order to permit the use of simple capacitor test structures while providing adequate supplies of minority carriers for injection during short pulse biasing and for inversion of the silicon surface at the capacitance measurement frequency of 1 MHz.

When viewed broadly, the initial electrical characterization results for the complete matrix of deposition and anneal conditions exhibited considerable variation. After excluding results for the specimens prepared at 750 Deg. C, except those receiving the anneals at 1000 Deg. C in either hydrogen or nitrogen, we found clear direct

effects of annealing on all the parameters of preliminary interest. These included the flat-band voltage, the voltage at the minimum capacitance point (corresponding to the threshold voltage of an FET), and the width of the C-V curve at flat-band (corresponding to the density of fast surface states).

Without further justification, the exclusion of the particular specimens would be very arbitrary. However, the results of analysis using spectroscopic ellipsometry indicate that the film structure of the specimen with the baseline silicon nitride is significantly different from the films deposited at higher temperature, specifically at 850 Deg. C. In particular, the specimen with the baseline nitride does not have an optically discernible layer of silicon dioxide at the silicon surface. This suggests that, from an electronic point of view, the interfacial charge characteristics affecting the flat-band voltage and the initial surface state density of the baseline specimen could differ considerably from those for the films deposited at higher temperatures. In these latter films, a distinct oxide layer was evident optically.

#### 4.2 Annealing Influences on Initial Electrical Behavior.

If the results for the 750 Deg. C specimens (as-deposited or annealed at 800 Deg. C) are excluded, then the effects of hydrogen annealing are straightforward. All flat-band voltage values are narrowed to the range: -0.2 to -0.7 V. The corresponding range for voltages at the minimum capacitance is also small: -1.3 to -1.6 V. There is little sensitivity of these parameters to either the deposition temperature of the film or the annealing temperature (900 or

1000 Deg. C) in hydrogen.

For the case of annealing in nitrogen, with the same exclusions as noted above, the results are similar. However, in the case of the flat-band voltage, the values are more positive for the low temperature anneals (+2.0 to +2.5 V) than for the high temperature ones (+1.4 to +1.9 V). The values for the voltage at the capacitance minimum show little sensitivity to the temperature of the anneal, ranging from -0.6 to +0.1 V.

With regard to initial surface state density, again observing the exclusion of the particular 750 Deg. C specimens noted earlier, low temperature annealing in hydrogen has the most beneficial effect. For the 900 Deg. C cases, densities are reduced to about  $0.6 \times 10^{12} \text{ cm}^{-2}$ . Results are more variable for the anneals at 1000 Deg. C, but the density values are still below  $1.1 \times 10^{12} \text{ cm}^{-2}$ .

In the case of annealing in nitrogen, the initial density values are higher than for the as-deposited or hydrogen-annealed cases. They range from  $1.4$  to  $3.2 \times 10^{12} \text{ cm}^{-2}$ . The higher temperature anneals result in even higher densities:  $3.5$  to  $4.8 \times 10^{12} \text{ cm}^{-2}$ .

#### 4.3 Electrical Stability For Pulse Cycling.

We evaluated the stability of selected memory states during the course of 2 million cycles of pulsed write and clear stress bias. We used a matrix reduced to a 2x3 size which treated only the extremes of deposition temperature (750 and 850 Deg. C) and the 1000 Deg. C anneals in hydrogen and nitrogen. The following comments and observations which deal primarily with the endurance issue of PEROS devices apply only to the specimens from the reduced matrix.

As we noted above, the results are complex if they are examined in extreme detail. More order is evident if we restrict our attention to changes in the memory states (as measured by the inferred threshold voltage from the voltage at the capacitance minimum) associated with the pulsed write and clear conditions. The stability of these memory states should relate to the density of fast surface states. There is no good correlation when the initial densities are considered. By treating the final values of density after 2 million pulse cycles, we find a strong correlation of final densities with the change in the voltages for the pulse write condition (established by hole injection from the silicon). There is slightly poorer correlation for changes in the pulse clear state. Some of the poorer correlation is the result of virtually no change in this state for the samples deposited at 750 and 850 Deg. C and annealed in nitrogen at 1000 Deg. C.

#### 4.4 Anomalous Behavior of the Baseline Specimen.

A major result from this treatment of the stability data was our recognition of the anomalous behavior of the 750 Deg. C, unannealed specimen. This specimen has the highest final density of surface states (50% more than the unannealed specimen deposited at 850 Deg. C). If the behavior of this specimen were to follow the regression line of the other samples, then a shift of 8.4 volts in the pulse write state would be expected. In fact, the change was only 3 V. Similarly for the pulse clear situation, the actual change was only 2.5 V, compared with a regression line projection of 5.5 V.

#### 4.5 Spectroscopic Ellipsometry.

As we noted earlier in this section, without an independent indication of a significant difference between the unannealed 750 Deg. C nitride and the others considered, it would be difficult to sustain our distinction between the memory behavior results for these specimens. That indication was provided by the spectroscopic ellipsometry analysis. Detailed treatment of the SE analysis results was limited to the baseline specimen and to specimens deposited at 850 Deg. C, of which one was unannealed and the other was annealed at 1000 Deg. C in hydrogen. The SE data for the latter two specimens is best fit by a multi-layer model in which a thin silicon dioxide layer (containing voids) adjoins the silicon substrate. No such layer is indicated in modeling the results for the film deposited at 750 Deg. C.

Consideration of the SE results leads us to speculate that any thin oxide film which has an electronic influence in the baseline specimens must be substantially different from those associated with the preparation of nitride films at 850 Deg. C. Such a possibility is consistent with the view that the oxide layer in the MNOS structure is affected by several influences. In the first place, there will be some growth of an oxide during the interval between final chemical etching and loading into the LPCVD reactor. Additional growth and/or modification of oxide can occur as the wafer is heated to the deposition temperature. Residual oxygen could be provided by the reactor environment. For nitride depositions at temperatures 100 Deg. C above the baseline case, this period of oxide growth or modification appears to be important.

This work has shown electrical and optical distinctions between the 750 Deg. C nitrides and those deposited at higher temperatures. From this base, we can define a clearer route to optimize and understand the behavior of MNOS structures in memory device applications. We enumerate some suggestions for such efforts in the next section.

## 5. RECOMMENDATIONS

Effort should be applied to separate effects of post-etching oxide growth and of oxide growth or modification during the heating of substrates to the nitride deposition temperature. This could be done by in-situ gas etching (e.g. with HCl) of the substrates prior to their exposure for controlled oxidation immediately before nitride deposition. Such a technique has been used at Westinghouse with good results to grow thin silicon dioxide films in an atmospheric pressure reactor.(8) These films were ellipsometrically measured to have thicknesses ranging from less than five to more than 20 Angstroms, depending on the temperature during a 2 min interval when oxygen was deliberately admitted into the argon ambient of the reactor.

The current work has established a means for making electrical and optical distinctions of the MNOS structure relevant to its memory performance. On this basis, similar evaluations should be made for specimens incorporating thin oxides prepared under controlled conditions. The electrical and optical properties of such specimens should be compared with those of the present work to identify important differences. Specifically, spectroscopic ellipsometry should be used to determine if a distinct oxide can be discerned optically for the case of the lowest nitride deposition temperatures of interest. We would expect that the separate preparation of the tunneling oxide should allow more flexibility in optimizing MNOS memory properties, particularly if

emphasis is put on very thin oxides. If results are promising, then a comprehensive study should be carried out using a matrix approach similar to that of the present work to identify the most useful conditions for optimizing selected memory parameters. This should include attention to the retention characteristics of the structures, a matter we were unable to address in the present work.

There could be considerable value to including ion implantation, perhaps with laser annealing, as special means for altering the density and composition of the outer portions of the insulator layers. Again, spectroscopic ellipsometry should be valuable as a means of making first order physical assessment of the effects of such treatments and promote correlations with electrical effects which such treatments may produce.

More detailed analysis of the chemical consequences of various techniques for oxide growth, nitride deposition and annealing conditions should be made with a sensitive technique, such a multiple internal reflection spectroscopy, after a reasonably small number of the most interesting types of specimens have been identified.

APPENDIX

REPORT OF WORK DONE ON THE ANALYSES OF SAMPLES  
SUBMITTED BY WESTINGHOUSE ELECTRIC CORPORATION.

By Professor K. Vedam

Materials Research Laboratory  
The Pennsylvania State University  
University Park, Pennsylvania

# REPORT OF WORK DONE ON THE ANALYSES OF SAMPLES SUBMITTED BY WESTINGHOUSE ELECTRIC CORPORATION

The six samples submitted by the Westinghouse Electric Corporation were non-destructively analysed with the help of the rotating analyser spectroscopic ellipsometer built in our laboratory. Figure 1 shows the schematic diagram of the instrument which is almost similar to the instrument built by Aspnes and Studna.<sup>1</sup> Figure 2 shows the typical reproducibility and precision of the data obtained on the two ellipsometric parameters  $\Delta$  and  $\psi$  and the consequent evaluated parameters such as the dielectric constant ( $\epsilon_1 - i \epsilon_2$ ) and the refractive index ( $n + ik$ ). Figures 3 and 4 show the data obtained with the above instrument on a bare silicon sample (again supplied by Westinghouse, along with the above mentioned six samples). It is seen that the values of  $\epsilon_1$  &  $\epsilon_2$  obtained agree very well with the values reported by Aspnes.<sup>2</sup> The maximum value of  $\epsilon_2$  at  $E_2$  position can of course be increased<sup>3</sup> considerably by proper in situ chemical etching, but no such attempts were made in this experiment.

Table I presents the values of  $\Delta$  and  $\psi$  for sample numbers 1, 2 and 5 in the region of photon energy 2.1 to 4.4 eV. These data have been analyzed following the procedure similar to Theeten et al.<sup>4</sup> in their study on  $\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$  structures. The results of such analyses are presented in Tables II-IV.

In brief, the analysis involves the computation of the ellipsometric parameters for assumed models representing the experimental sample and comparing such calculated parameters with the experimental values. Then the various assumed values in the models are varied in such a way, that the error function

$$F = \sum_{E_n} |\tan \psi(E_n)_{\text{calc}} - \tan \psi(E_n)_{\text{expt}}|^2 + \sum_{E_n} |\cos \Delta(E_n)_{\text{calc}} - \cos \Delta(E_n)_{\text{expt}}|^2$$

is minimized. In this expression  $\tan \psi(E_n)_{\text{calc}}$  corresponds to the calculated value of  $\tan \psi$  at the photon energy  $E_n$  and the other terms in the expression have similar meanings. For these computations we used the dielectric functions of Si,  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  given respectively by Aspnes and Theeten,<sup>5</sup> Malitson<sup>6</sup> and Philipp.<sup>7</sup>

Table II presents the data of the least squares analysis obtained on Sample No. 1. It is seen that the assumption of a single layer of  $\text{Si}_3\text{N}_4$  on the silicon substrate is not satisfactory. The only model that gives reasonable agreement (as evidenced by the minimum value obtained for mean square deviation) given in the last column of the table, is the one with the single film composed of a mixture of 90%  $\text{Si}_3\text{N}_4$  and 10%  $\text{SiO}_2$ , with thickness of 495Å. Adding additional parameters, such as voids, additional layers of different composition etc., does not improve the fit.

Table III presents similar results obtained on Sample No. 2, whose deposition temperature is 850°C, and the specimen was not subjected to any further treatment. Comparison of Tables II and III show the marked difference in the characteristics of samples 1 and 2. This is also evident from Figure 5, depicting the variation of the experimentally observed ellipsometric parameter  $\Delta$  as a function of the photon energy. In this case the model that best describes the sample No. 2 is one with the topmost layer of (92%  $\text{Si}_3\text{N}_4$  + 8%  $\text{SiO}_2$ ) of thickness 496Å, on top of an optically absorbing layer of amorphous silicon of 10Å thickness which itself is on top of another layer of (58%  $\text{SiO}_2$  + 42% void) of 19Å thickness. It must be emphasized that the numerical values as well as the exact description of the model should not be taken literally to be exact and as the "true" nature of the sample. It only means that the observed data can be best described by this model. It will be valuable to corroborate these results with depth profile study using techniques such as Auger Electron Spectroscopy, etc.

Table IV presents the results obtained on sample No. 5. It may be recalled that the preparation condition for this sample is similar to that of No. 2, except that it has been subjected to a further annealing treatment at 1000°C in Hydrogen atmosphere. The effect of this annealing treatment is brought out clearly in the experimentally determined ellipsometric parameter  $\Delta$  and this is shown in Figure 6. The results of the least squares analysis is shown in Table IV. Comparing the values given in this table with those in Table III, it is evident that the values of  $\sigma$  are all slightly larger, indicating that the true model may be more complicated than the ones used for sample No. 2. However, by comparing the final rows in Tables III and IV, it is seen that the effect of annealing under reducing conditions is (i) to reduce the thickness of the outermost layer from 496Å to 481Å, (ii) at the same time to reduce the percentage of  $\text{SiO}_2$  in the outermost layer from 8% to 5%, (iii) to reduce the effective thickness of the layer of

amorphous silicon from  $10\text{\AA}$  to  $9\text{\AA}$  and (iv) to reduce the fraction of  $\text{SiO}_2$  from 58% to 37% in the layer next to the silicon substrate.

It must be pointed out that the effect of hydrogenation of  $\text{Si}_3\text{N}_4$ ,  $\text{SiO}_2$  and Si and its effect on the effective band gap of the film has been completely ignored in the above analysis. Our own measurements not connected with the present study, lead us to believe that this may not really be valid. However, since our own conclusions in this field is still in the formative stage, definite statements in this regard cannot be made at this time.

The effect of annealing the sample at  $1000^\circ\text{C}$  will also reduce the amount of voids present in the sample or in other words one will expect some compaction of the film. This is evidenced by the reduction of film thickness of the outermost layer in sample No. 5 compared to that in sample No. 2.

If additional information on the history of the samples, and data such as Auger-spectroscopy-depth-profile are available the analysis can be continued further, hopefully with more benefit. However, it must be pointed out that, Theeten et al.<sup>4</sup> have demonstrated that analysis of  $\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$  structure is not a straight forward matter at the present state of our knowledge.

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TABLE I

| Wave-length<br>(nm) | Energy<br>ev | Sample No. 1 |        | Sample No. 2 |        | Sample No. 5 |        |
|---------------------|--------------|--------------|--------|--------------|--------|--------------|--------|
|                     |              | DELTA        | PSI    | DELTA        | PSI    | DELTA        | PSI    |
| 280                 | 4.430        | -71.692      | 36.825 | -64.399      | 36.011 | -67.751      | 36.211 |
| 282                 | 4.399        | -74.765      | 36.939 | -67.968      | 36.007 |              |        |
| 284                 | 4.368        | -77.838      | 37.086 | -71.234      | 36.165 |              |        |
| 286                 | 4.337        | -81.041      | 37.261 | -74.866      | 36.270 |              |        |
| 288                 | 4.307        | -83.938      | 37.404 | -78.143      | 36.329 |              |        |
| 290                 | 4.278        | -86.641      | 37.464 | -81.273      | 36.294 | -83.297      | 36.780 |
| 292                 | 4.248        | -88.782      | 37.466 | -83.701      | 36.213 |              |        |
| 294                 | 4.219        | 89.475       | 37.475 | -85.718      | 36.114 |              |        |
| 296                 | 4.191        | 87.875       | 37.511 | -87.532      | 36.049 |              |        |
| 298                 | 4.163        | 86.382       | 37.576 | -89.230      | 36.012 |              |        |
| 300                 | 4.135        | 84.899       | 37.696 | 89.074       | 36.037 | 87.183       | 36.684 |
| 302                 | 4.108        | 83.482       | 37.881 | 87.431       | 36.109 | 85.630       | 36.799 |
| 304                 | 4.081        | 82.087       | 38.136 | 85.865       | 36.256 | 84.154       | 36.984 |
| 306                 | 4.054        | 80.737       | 38.481 | 84.309       | 36.483 | 82.665       | 37.249 |
| 308                 | 4.028        | 79.554       | 38.861 | 82.938       | 36.739 | 81.389       | 37.551 |
| 310                 | 4.002        | 78.491       | 39.281 | 81.709       | 37.040 | 80.235       | 37.892 |
| 312                 | 3.976        | 77.616       | 39.683 | 80.693       | 37.341 | 79.260       | 38.231 |
| 314                 | 3.951        | 76.851       | 40.090 | 79.805       | 37.648 | 78.426       | 38.571 |
| 316                 | 3.926        | 76.108       | 40.533 | 78.941       | 37.986 | 77.621       | 38.949 |
| 318                 | 3.901        | 75.343       | 41.015 | 78.093       | 38.364 | 76.792       | 39.367 |
| 320                 | 3.876        | 74.570       | 41.569 | 77.202       | 38.807 | 75.966       | 39.855 |
| 322                 | 3.852        | 73.762       | 42.227 | 76.290       | 39.311 | 75.110       | 40.111 |
| 324                 | 3.829        | 72.957       | 42.976 | 75.378       | 39.892 | 73.312       | 41.812 |
| 326                 | 3.805        | 72.057       | 43.861 | 74.421       | 40.576 | 73.312       | 41.812 |
| 328                 | 3.782        | 71.252       | 44.743 | 73.715       | 41.160 | 72.481       | 42.568 |
| 330                 | 3.759        | 70.516       | 45.630 | 72.743       | 41.967 | 71.710       | 43.339 |
| 332                 | 3.736        | 69.826       | 46.503 | 72.075       | 42.638 | 71.009       | 44.071 |
| 334                 | 3.714        | 69.210       | 47.319 | 71.440       | 43.275 | 70.423       | 44.788 |
| 336                 | 3.692        | 68.566       | 48.209 | 70.821       | 43.962 | 69.800       | 45.544 |
| 338                 | 3.670        | 67.926       | 49.144 | 70.213       | 44.694 | 69.202       | 46.352 |
| 340                 | 3.648        | 67.227       | 50.201 | 69.578       | 45.535 | 68.545       | 47.274 |
| 342                 | 3.627        | 66.418       | 51.407 | 68.925       | 46.470 | 67.853       | 48.317 |
| 344                 | 3.606        | 65.571       | 52.770 | 68.243       | 47.563 | 67.138       | 49.492 |
| 346                 | 3.585        | 64.649       | 54.340 | 67.551       | 48.806 | 66.386       | 50.859 |
| 348                 | 3.565        | 63.814       | 55.926 | 66.933       | 50.074 | 65.719       | 52.241 |
| 350                 | 3.544        | 62.954       | 57.552 | 66.420       | 51.376 | 65.108       | 53.676 |

TABLE I (continued)

| Wave-length<br>(nm) | Energy<br>ev | Sample No. 1 |        | Sample No. 2 |        | Sample No. 3 |        |
|---------------------|--------------|--------------|--------|--------------|--------|--------------|--------|
|                     |              | DELTA        | PSI    | DELTA        | PSI    | DELTA        | PSI    |
| 352                 | 3.524        | 62.222       | 59.089 | 66.006       | 52.618 | 64.597       | 55.020 |
| 354                 | 3.504        | 61.510       | 60.594 | 66.118       | 53.589 | 64.173       | 56.356 |
| 356                 | 3.484        | 60.754       | 62.384 | 65.381       | 55.224 | 63.776       | 57.849 |
| 358                 | 3.465        | 59.844       | 64.205 | 65.087       | 56.844 | 63.322       | 59.610 |
| 360                 | 3.446        | 58.485       | 66.553 | 64.708       | 58.817 | 62.718       | 61.721 |
| 362                 | 3.427        | 56.072       | 69.347 | 64.018       | 61.219 | 61.623       | 64.300 |
| 364                 | 3.408        | 51.439       | 72.513 | 62.535       | 64.141 | 59.403       | 67.392 |
| 366                 | 3.389        | 42.288       | 75.685 | 59.274       | 67.590 | 54.629       | 70.907 |
| 368                 | 3.371        | 38.712       | 76.405 | 53.733       | 70.732 | 46.528       | 73.922 |
| 370                 | 3.353        | 18.176       | 78.054 | 44.978       | 73.345 | 34.607       | 76.022 |
| 372                 | 3.335        | 20.755       | 76.958 | 34.237       | 74.950 | 22.240       | 76.789 |
| 374                 | 3.317        | 27.825       | 75.118 | 23.342       | 75.496 | 15.387       | 76.368 |
| 376                 | 3.299        | 33.121       | 72.892 | 15.359       | 75.109 | 17.243       | 75.099 |
| 378                 | 3.282        | 36.792       | 70.493 | 13.597       | 73.939 | 22.393       | 73.252 |
| 380                 | 3.264        | 39.298       | 68.094 | 17.584       | 72.234 | 27.100       | 71.118 |
| 382                 | 3.247        | 41.034       | 65.680 | 21.840       | 70.235 | 30.819       | 68.818 |
| 384                 | 3.230        | 42.334       | 63.454 | 25.769       | 68.137 | 33.534       | 66.585 |
| 386                 | 3.214        | 43.462       | 61.284 | 29.033       | 65.944 | 35.837       | 64.326 |
| 388                 | 3.197        | 44.136       | 59.458 | 31.398       | 64.059 | 37.437       | 62.421 |
| 390                 | 3.181        | 44.771       | 57.879 | 33.271       | 62.374 | 38.738       | 60.742 |
| 392                 | 3.164        | 45.258       | 56.585 | 34.683       | 60.973 | 39.738       | 59.361 |
| 394                 | 3.148        | 45.699       | 55.482 | 35.810       | 59.766 | 40.556       | 58.167 |
| 396                 | 3.132        | 46.114       | 54.437 | 38.374       | 58.239 | 41.265       | 57.053 |
| 398                 | 3.117        | 46.499       | 53.438 | 37.815       | 57.498 | 41.959       | 55.971 |
| 400                 | 3.101        | 46.893       | 52.358 | 39.503       | 55.959 | 42.498       | 54.756 |
| 420                 | 2.953        | 50.635       | 44.648 | 45.979       | 47.255 | 47.843       | 46.377 |
| 440                 | 2.819        | 53.771       | 39.749 | 50.230       | 41.714 | 51.648       | 41.055 |
| 460                 | 2.697        | 56.560       | 36.263 | 53.596       | 37.826 | 54.779       | 37.303 |
| 480                 | 2.584        | 59.125       | 33.629 | 56.489       | 34.918 | 57.535       | 34.499 |
| 500                 | 2.481        | 61.497       | 31.513 | 59.090       | 32.625 | 60.037       | 32.266 |
| 520                 | 2.385        | 63.694       | 29.787 | 61.440       | 30.766 | 62.312       | 30.456 |
| 540                 | 2.297        | 65.761       | 28.319 | 63.608       | 29.303 | 64.434       | 28.926 |
| 560                 | 2.215        | 67.683       | 27.065 | 65.625       | 27.872 | 66.416       | 27.626 |
| 580                 | 2.139        | 69.531       | 25.958 | 67.539       | 26.706 | 68.303       | 26.481 |
| 600                 | 2.067        | 71.259       | 24.982 | 69.320       | 25.690 | 70.062       | 25.474 |

TABLE II

| No. of<br>parameters | Si <sub>3</sub> N <sub>4</sub> - on Si — film No. 1                                                                                             |                                                                                                                           | mean square<br>deviation<br>$\sigma$ |
|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
|                      | Model                                                                                                                                           | Best values<br>of parameters                                                                                              |                                      |
| 1                    | one-layer pure<br>Si <sub>3</sub> N <sub>4</sub>                                                                                                | $d = 471\text{\AA}$                                                                                                       | 0.274                                |
| 1                    | one-layer pure<br>Si <sub>3</sub> N <sub>4</sub> on 20 $\text{\AA}$<br>SiO <sub>2</sub>                                                         | $d = 460\text{\AA}$                                                                                                       | 0.256                                |
| 2                    | one layer<br>(Si <sub>3</sub> N <sub>4</sub> + SiO <sub>2</sub> )                                                                               | $d = 495\text{\AA}$<br>$x_{\text{SiO}_2} = 10\%$                                                                          | 0.110                                |
| 4                    | one layer<br>(Si <sub>3</sub> N <sub>4</sub> + SiO <sub>2</sub> )<br>on<br>one layer<br>(SiO <sub>2</sub> + voids)                              | $d = 485\text{\AA}$<br>$x_{\text{SiO}_2} = 10\%$<br>$d = 20\text{\AA}$<br>$x_{\text{SiO}_2} = 90\%$                       | 0.131                                |
| 6                    | one layer<br>(Si <sub>3</sub> N <sub>4</sub> + SiO <sub>2</sub> )<br>on<br>one layer<br>(a-Si)<br>on<br>one layer<br>(SiO <sub>2</sub> + voids) | $d = 485\text{\AA}$<br>$x_{\text{SiO}_2} = 10\%$<br>$d = 10\text{\AA}$<br>$d = 20\text{\AA}$<br>$x_{\text{SiO}_2} = 60\%$ | 0.232                                |

TABLE III

| No. of<br>parameters | <u>Si<sub>3</sub>N<sub>4</sub> - on Si — film No. 2</u>                                                                                       |                                                                                                                                     | mean square<br>deviation<br>$\sigma$ |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
|                      | Model                                                                                                                                         | Best Values<br>of parameters                                                                                                        |                                      |
| 1                    | one-layer pure<br>Si <sub>3</sub> N <sub>4</sub>                                                                                              | d = 485 $\text{\AA}$                                                                                                                | 0.287                                |
| -----                |                                                                                                                                               |                                                                                                                                     |                                      |
| 1                    | one-layer pure<br>Si <sub>3</sub> N <sub>4</sub><br>on<br>20 $\text{\AA}$ of SiO <sub>2</sub>                                                 | d = 474 $\text{\AA}$                                                                                                                | 0.275                                |
| -----                |                                                                                                                                               |                                                                                                                                     |                                      |
| 2                    | one-layer<br>[(Si <sub>3</sub> N <sub>4</sub> ) <sub>x</sub> +<br>(SiO <sub>2</sub> ) <sub>1-x</sub> ]                                        | d = 50 $\text{\AA}$<br>$x_{\text{SiO}_2} = 10\%$                                                                                    | 0.099                                |
| -----                |                                                                                                                                               |                                                                                                                                     |                                      |
| 4                    | one layer<br>(Si <sub>3</sub> N <sub>4</sub> + SiO <sub>2</sub> )<br>on<br>one layer<br>(SiO <sub>2</sub> + voids)                            | d = 498 $\text{\AA}$<br>$x_{\text{SiO}_2} = 10\%$<br><br>d = 20 $\text{\AA}$<br>$x_{\text{SiO}_2} = 90\%$                           | 0.097                                |
| -----                |                                                                                                                                               |                                                                                                                                     |                                      |
| 6                    | one layer<br>(Si <sub>3</sub> N <sub>4</sub> + SiO <sub>2</sub> )<br>on<br>one layer<br>a-Si<br>on<br>one-layer<br>(SiO <sub>2</sub> + voids) | d = 496 $\text{\AA}$<br>$x_{\text{SiO}_2} = 8\%$<br><br>d = 10 $\text{\AA}$<br><br>d = 19 $\text{\AA}$<br>$x_{\text{SiO}_2} = 58\%$ | 0.087                                |

TABLE IV

| No. of<br>parameters | Si <sub>3</sub> N <sub>4</sub> - on Si — film No. 5                                 |                                                                          | mean square<br>deviation<br>$\sigma$ |
|----------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------------------|
|                      | Model                                                                               | Best values<br>of parameters                                             |                                      |
| 1                    | one layer pure<br>Si <sub>3</sub> N <sub>4</sub>                                    | $d = 480\text{\AA}$                                                      | 0.338                                |
| 1                    | one layer pure<br>Si <sub>3</sub> N <sub>4</sub><br>on<br>17\AA of SiO <sub>2</sub> | $d = 471\text{\AA}$                                                      | 0.328                                |
| 2                    | one-layer<br>(Si <sub>3</sub> N <sub>4</sub> + SiO <sub>2</sub> )                   | $d = 508\text{\AA}$<br>$x_{\text{SiO}_2} = 12\%$                         | 0.106                                |
|                      | one-layer<br>(Si <sub>3</sub> N <sub>4</sub> + SiO <sub>2</sub> )<br>on             | $d = 481\text{\AA}$<br>$x_{\text{SiO}_2} = 5\%$                          | 0.103                                |
| 6                    | one-layer<br>a-Si<br>on<br>one-layer<br>(SiO <sub>2</sub> + voids)                  | $d = 9\text{\AA}$<br><br>$d = 18\text{\AA}$<br>$x_{\text{SiO}_2} = 37\%$ |                                      |

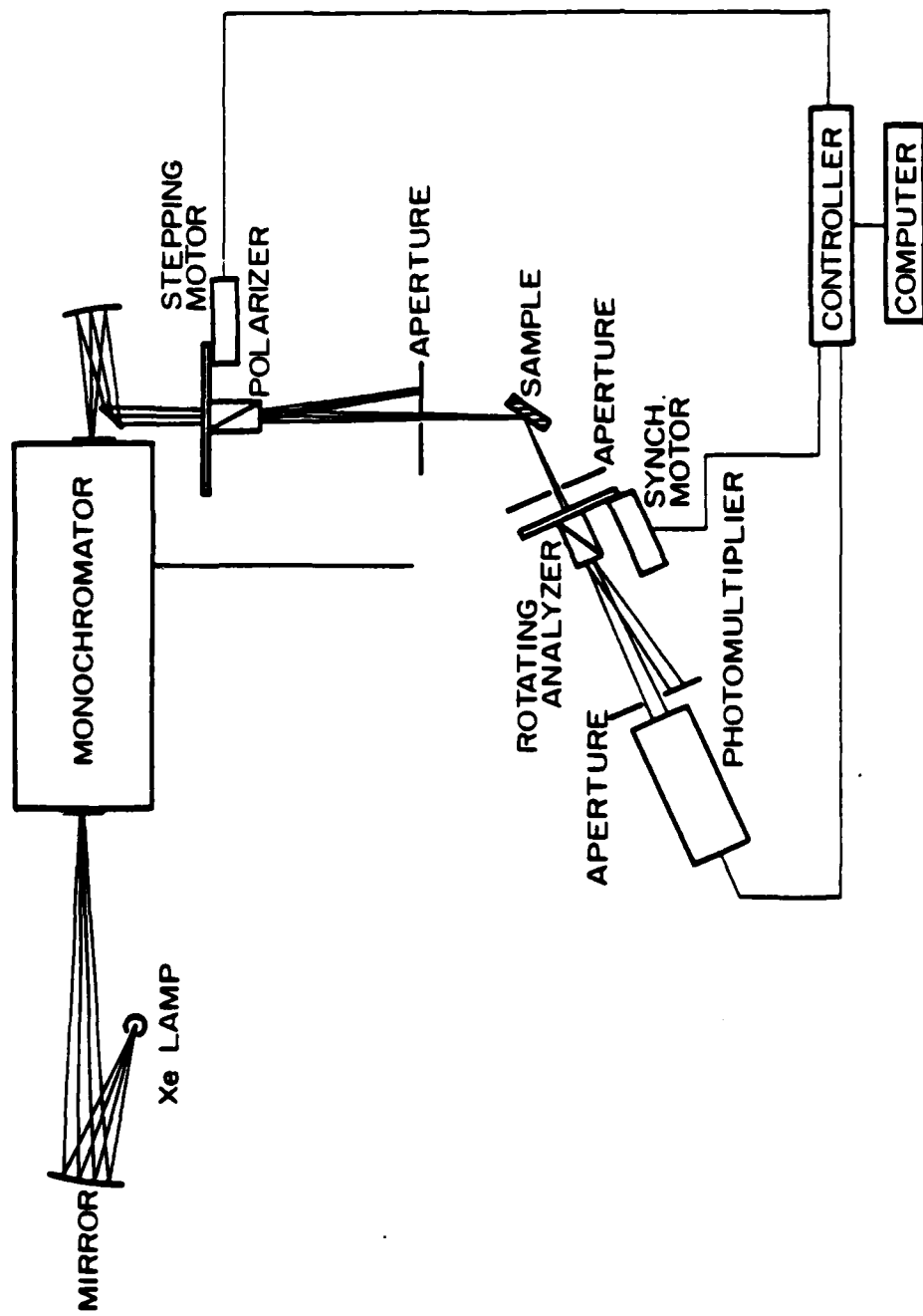


Figure 1. Schematic diagram of spectroscopic ellipsometer.

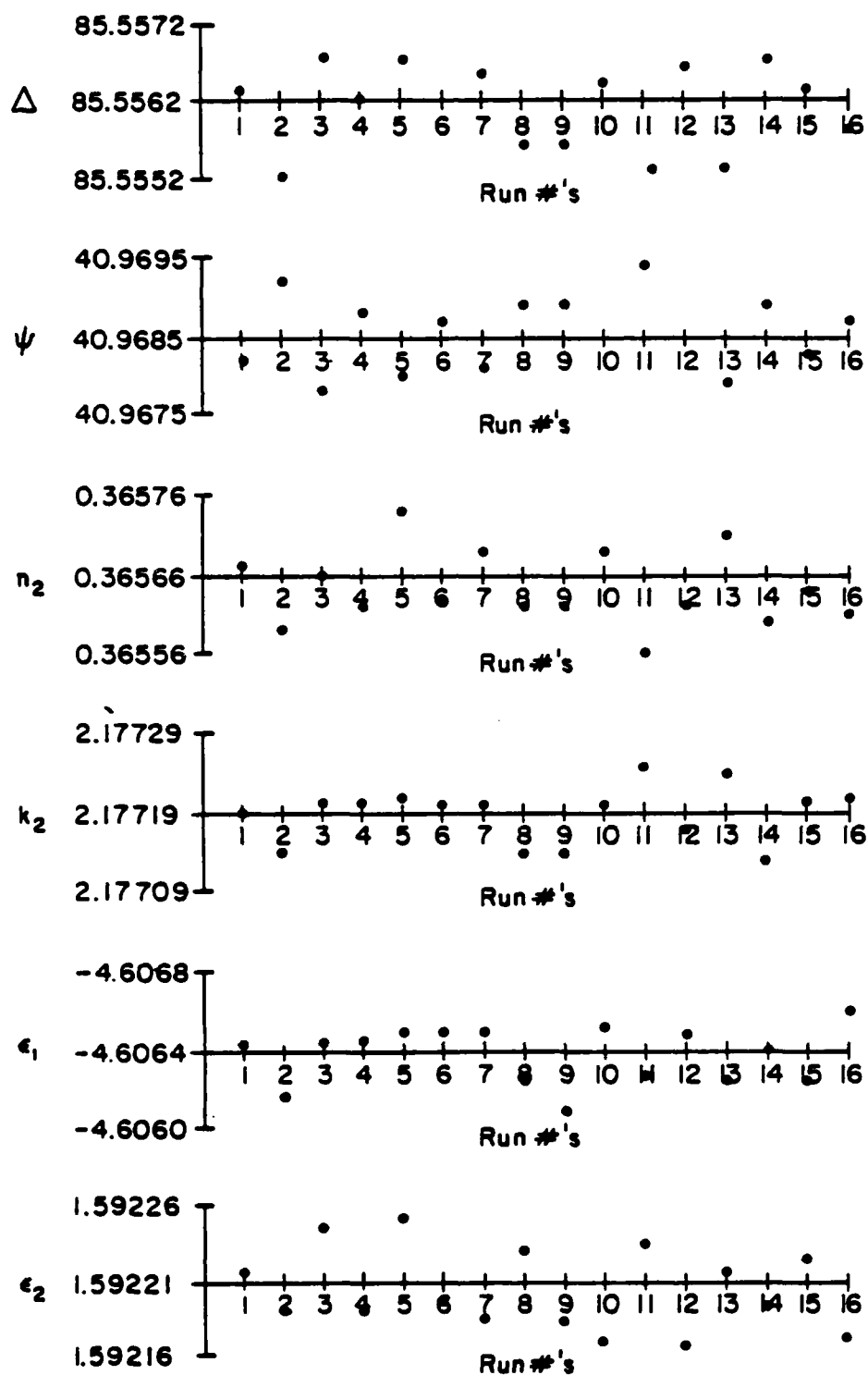


Figure 2. Reproducibility and scatter of the measured ellipsometric parameters  $\Delta$  and  $\psi$  for a gold film at  $\lambda$  546 nm. The corresponding variation in the computed values of  $n_2$ ,  $k_2$ ,  $\epsilon_1$  and  $\epsilon_2$  are also shown.

PLOT OF E1 VS ENERGY  
WEST. BARE SILICON SAMPLE

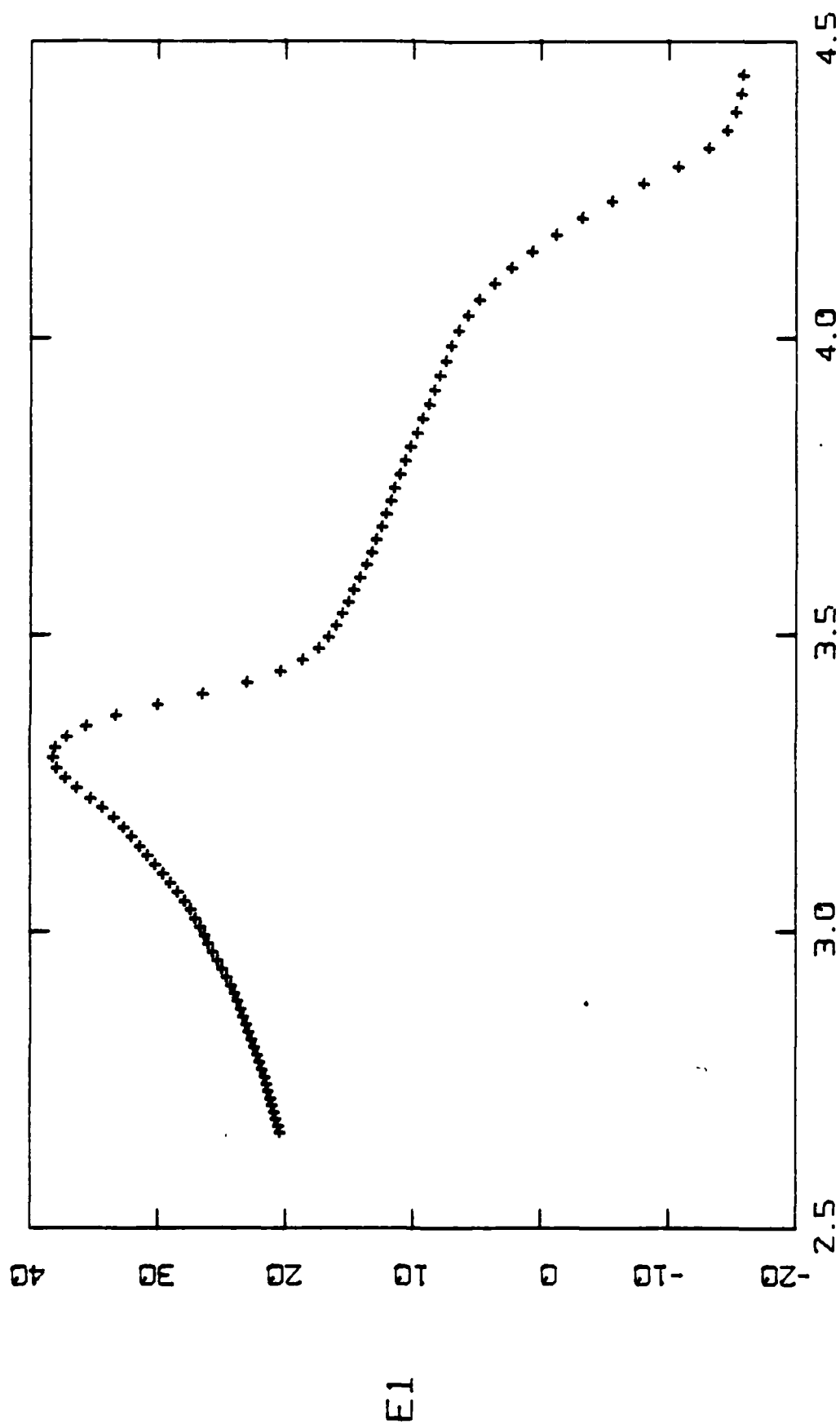


Figure 3

PLOT OF E2 VS ENERGY  
WEST. BARE SILICON SAMPLE

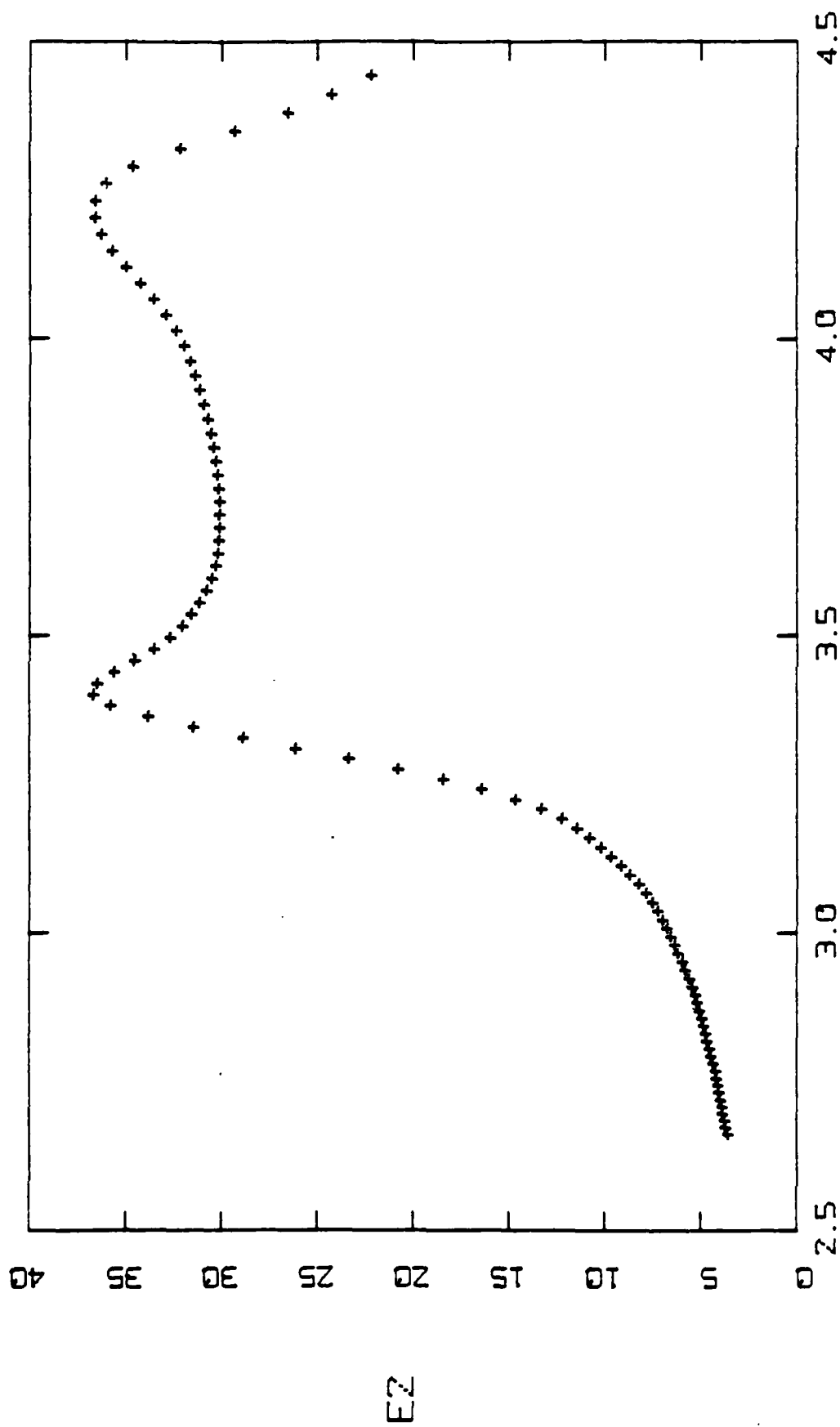
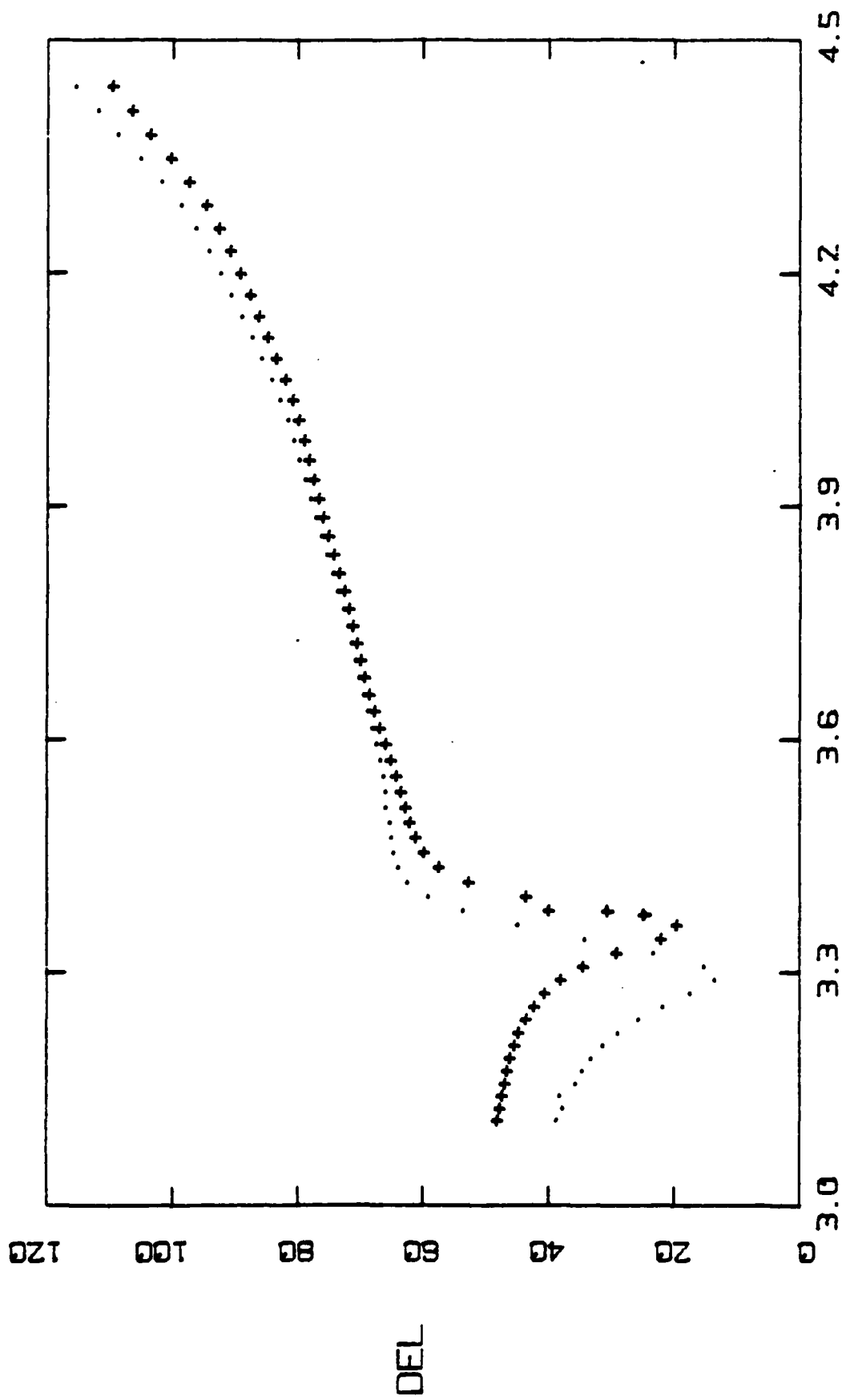


FIGURE 4

PLOT OF DELTA VS ENERGY  
SI-SI3N4 SAM #1(+) #2(.)



PHOTON ENERGY (EV)

FIGURE 5

PLOT OF DELTA VS ENERGY  
SI-SI3N4 SAM #5(+) #2(.)

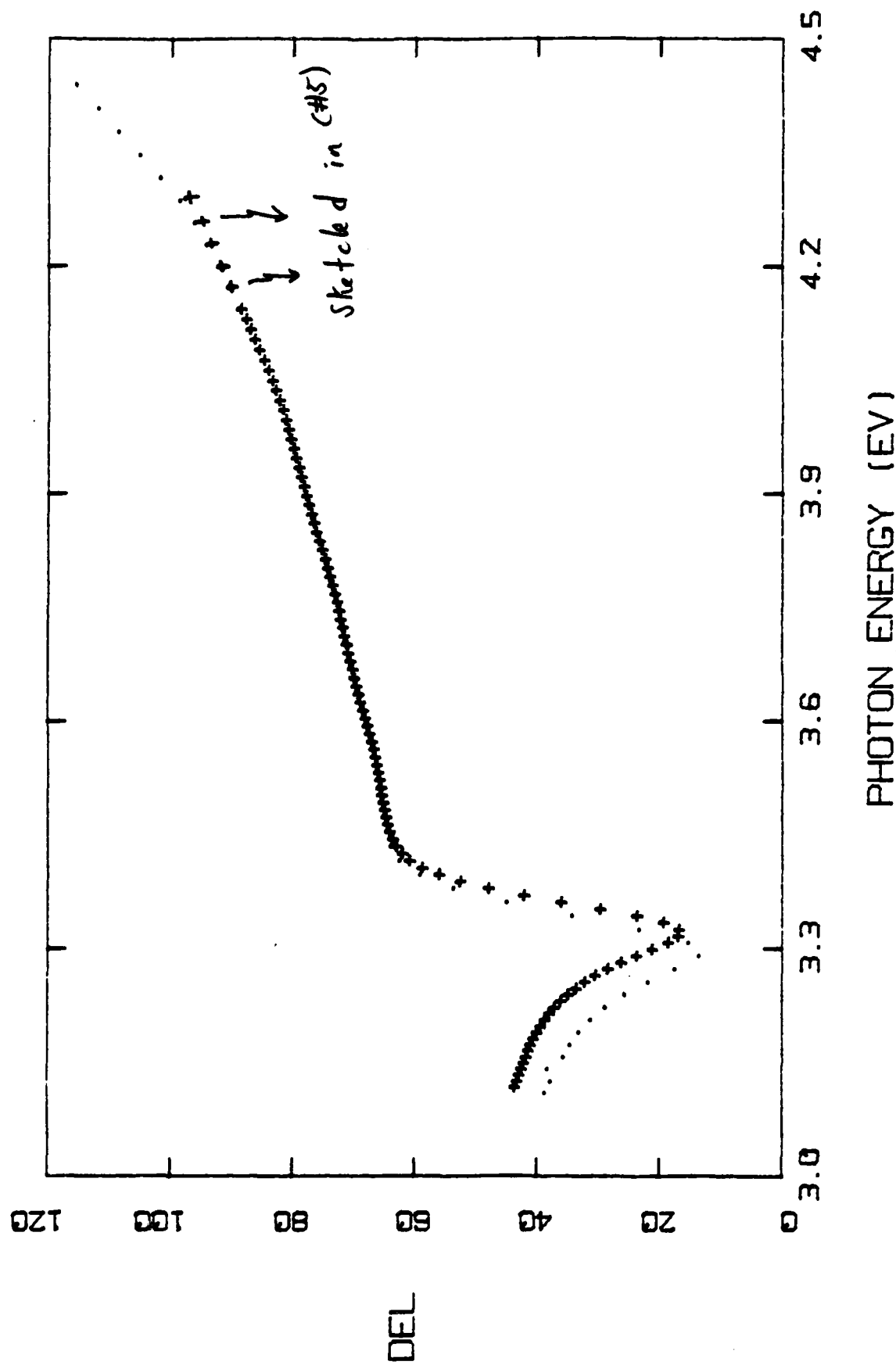


FIGURE 6

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