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Total Dose and Transient Radiation Testing of Two CMOS/SOS RAM's

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ABSTRACT

Total dose and transient radiation measurements were performed in situ on two complementary metal-oxide semiconductor/silicon on sapphire (CMOS/SOS) random-access memories (RAM's). Total-dose failure levels were determined using a ^{60}Co source. Upset levels were determined at both a flash x-ray facility and a linear accelerator. The two RAM's are configured as 256 × 4 and 1k × 1 and are equivalent to types 6551 and 6518, respectively.

Co 60 isotope

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This report summarizes the radiation test data on two complementary metal-oxide semiconductor/silicon on sapphire (CMOS/SOS) random-access memories (RAM's). The two types are CMOS/SOS versions of the 6551 and 6518 CMOS/bulk RAM's. These devices were manufactured by RCA and are to be used in a radiation-hardened Army communication system. Total-dose failure levels were determined using a ^{60}Co source. Upset levels were determined at both a flash x-ray facility and a linear accelerator (LINAC).

During the irradiation, the RAM under test was in its read mode with a checkerboard pattern stored in its memory. Figure 1 is a block diagram of the test setup. It is a hard-wired system; that is, the address, data, and comparison signals are generated by dedicated components in the interface chassis. This chassis consists of a clock and address generator; an erasable programmable read-only memory (EPROM), which provides checkerboard pattern data input to the RAM; and a comparator. The comparator circuit compares the data out of the RAM with the data stored in the EPROM. The output from the comparator provides a pass/fail signal, which is used to trigger the logic state analyzer (LSA). The LSA is set to trigger on a fail signal and to store the next 250 bytes of data, the maximum storage capability of the LSA. The data out of the RAM along with their addresses are stored and then printed out on a printer/terminal. For ^{60}Co tests, the device under test is irradiated until a fail signal occurs. For pulsed irradiation, the fail signal occurs during the pulse if the RAM is upset.

Five type 240A (6551) and two 239A (6518) RAM's were irradiated at the ^{60}Co source (a dose rate of 100 rad(Si)/s). One device, a type 240A, failed after only 1.93 krad(Si). This result is not included in the average failure data because we believe that this failure indication was noise-induced and was not due to the irradiation. Immediate checking after the source was lowered revealed that the device was operating normally again. This is in contrast to the other total-dose failures which typically took minutes to anneal. Table 1 shows the results for the remaining four type 240A devices. The average failure level was 33.5 krad(Si). Table 2 shows the results for the two type 239A devices. They failed at an average dose of 32.9 krad(Si). Failure is defined to occur when the first "non-compare" signal is detected by the LSA. Recovery for all devices occurred within one to two minutes after the irradiation was stopped. Recovery is defined to occur when the compare circuits detect no difference between the data stored in the EPROM and the RAM under test. Recovery always occurred without rewriting to the memory.

indicating that failure occurred in the peripheral circuits and the memory cells were not upset. For these tests, the power supply current I_{CC} was also recorded as a function of time and accumulated dose. The I_{CC} measured is the total current drawn by the device while in an active state. These data are also shown in tables 1 and 2. From these data, one can see a decrease in current for the first few seconds of irradiation. The decrease actually starts as the source emerges from its storage position. At this time, we do not understand this phenomenon.

Four type 240A RAM's were irradiated at our flash x-ray facility. The pulse width at half maximum was 20 ns and the charging voltage was 4.1 MV. One device had an upset of one bit in memory at 0.75×10^9 rad(Si)/s. When this device was subsequently exposed to 2.2×10^9 rad(Si)/s, no upset occurred. This leads us to believe tha the initial upset indication was spurious. One device showed address upset at 1×10^{11} rad(Si)/s but no memory loss. The last two devices showed no upset at dose rates as high as 1×10^{11} rad(Si)/s. None of the devices went into latchup.

An instability in the instrumentation for the 239A devices was discovered during the flash x-ray tests. We decided to abort these tests and spend the time correcting the problem in preparation for the LINAC tests.

Five of each type of device were irradiated at the Naval Research Laboratory LINAC. These devices were irradiated with a pulse width of 150 ns and a beam energy of 17 MeV. All upsets observed were changes in the stored RAM data. For the type 240A devices, one went to 3.3×10^{10} rad(Si)/s without upset. One other device upset at this dose rate. All devices upset above this dose rate and none below this dose rate, except for one device, which had an apparent upset at 1.4×10^9 rad(Si)/s. When this device as subsequently irradiated at dose rates up to 5×10^9 rad(Si)/s, no upset was observed. We believe the upset was related to the instrumentation. One device was irradiated to 4×10^{10} rad(Si)/s and showed a delayed upset 2 to 3 s after the pulse. We have previously observed delayed failures in microprocessors.[1]

For the 239A devices the lowest dose rate for upset was 2.5×10^{10} rad(Si)/s and the highest dose rate without upset was 4×10^{10} rad(Si)/s. All devices upset at dose rates of 5.8×10^{10} rad(Si)/s and higher. No latchup or permanent failure in any device was observed.

In the LINAC tests the I_{CC} current change was observed during the pulse using a Tektronix type CT-2 pulse transformer. The data showed that the RAM I_{CC} followed the radiation pulse, which indicates immediate recovery of the RAM even when there was a bit flip. Currents were observed to peak at approximately 300 mA for a dose rate of 5.8×10^{10} rad(Si)/s.

[1] *T. Pruitt et al, IEEE Trans. Nucl. Sci. NS-25, No. 6 (1978), 1205.*

TABLE 1. TOTAL-DOSE FAILURE LEVELS FOR RAM TYPE 240A (256 × 4)

Time (s)	5		8		21		48	
	I_{CC} (mA)	Accum. dose (krad(Si))	I_{CC} (mA)	Accum. dose (krad(Si)	I_{CC} (mA)	Accum. dose (krad(Si)	I_{CC} (mA)	Accum. dose (krad(Si)
0	0.151	0	0.142	0	0.152	0	0.298	0
10	0.136	1.08	0.133	1.04	0.136	1.08	0.282	1.12
20	0.132	2.16	0.132	2.09	0.132	2.16	0.274	2.24
30	0.130	3.24	0.132	3.13	0.131	3.25	0.273	3.36
40	0.130	4.32	0.133	4.18	0.133	4.33	0.276	4.48
50	0.128	5.40	0.132	5.22	0.136	5.41	0.279	5.60
60	0.130	6.48	0.133	6.26	0.140	6.49	0.283	6.71
120	0.242	12.96	0.210	12.53	0.299	12.98	0.505	13.43
180	1.500	19.44	1.287	18.79	1.755	19.48	2.280	20.14
240	4.806	25.92	4.450	25.06	5.491	25.97	6.890	26.86
300	10.511	32.40	10.147	31.32	12.193	32.46	Failed	33.0
						~~295 s~~	at 295 s	
310	11.588	33.48	11.228	32.36	12.950	33.54	-	-
320	13.229	34.56	12.016	33.41	Failed	33.0	-	-
	Failed at 323 s	34.88	Failed at 317 s	33.1	at 305 s	-	-	-

TABLE 2. TOTAL-DOSE FAILURE LEVELS FOR RAM TYPE 239A (1k × 1)

Time (s)	4		6	
	I_{CC} (mA)	Accum. dose (krad(Si))	I_{CC} (mA)	Accum. dose (krad(Si))
0	0.216	0	0.168	0
10	0.208	1.08	0.156	1.08
20	0.207	2.15	0.152	2.16
30	0.207	3.23	0.151	3.24
40	0.209	4.21	0.151	4.32
50	0.211	5.38	0.152	5.40
60	0.215	6.46	0.155	6.49
120	0.374	12.92	0.325	12.97
180	1.947	19.39	2.070	19.46
240	6.220	25.85	6.760	25.94
300	14.230	32.31	14.790	32.43
310	15.670	33.39	Failed	32.1
			at 279 s	-
	Failed at 313 s	33.7	-	-

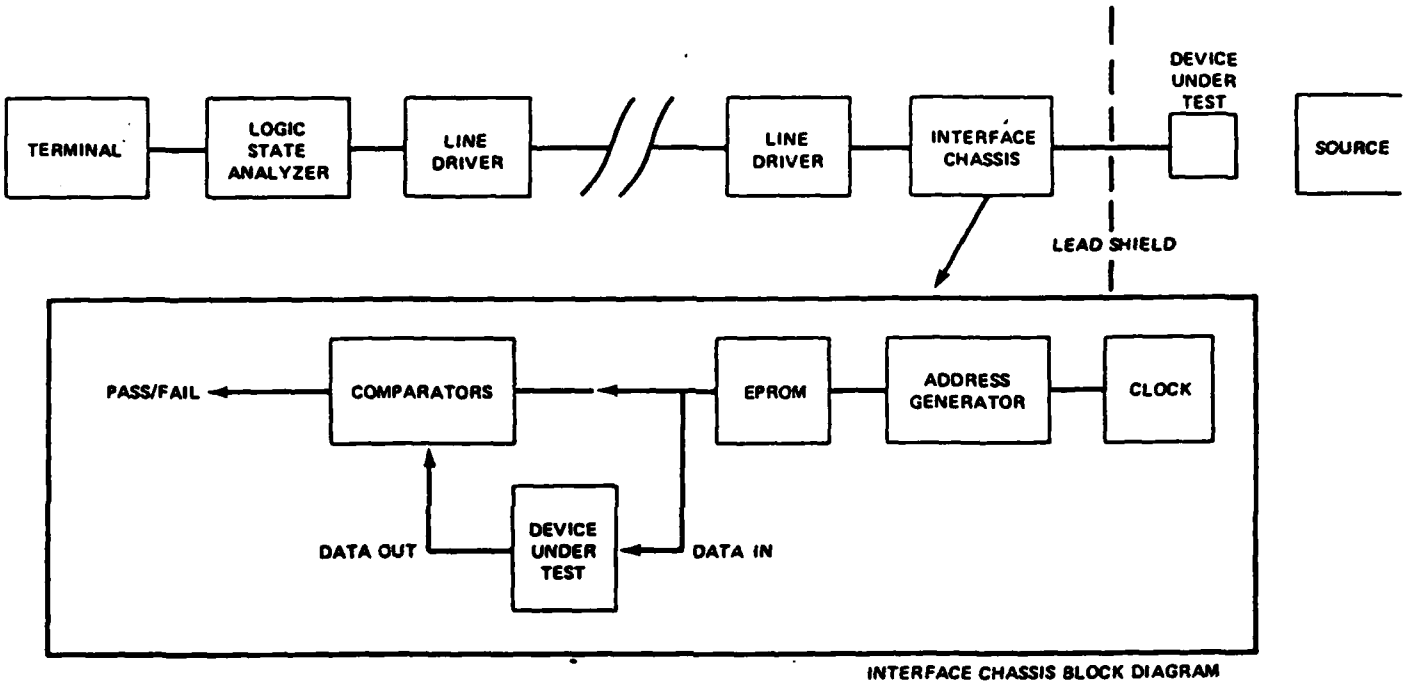

Figure 1. Static RAM Functional Block Diagram.