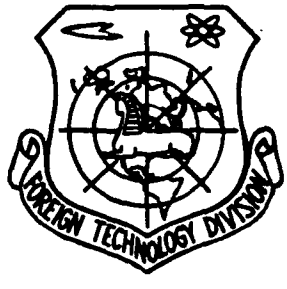
FTD-ID(RS)T-1691-82

FOREIGN TECHNOLOGY DIVISION

A FDM MASTER-GROUP SIGNAL ENCODING EQUIPMENT

by

Li Mingjiu, Jian Yushen



EDITED TRANSLATION

FTD-ID(RS)T-1691-82 10 February 1983

MICROFICHE NR: FTD-83-C-000131

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English pages: 20

Source: Tongxin Xuebao, Nr. 2, April 1981, pp. 26-35

Country of origin: China
Translated by: SCITRAN
F33657-81-D-0263
Requester: RCA

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ABSTRACT

This paper provides an introduction to the techniques used in newly developed carrier wave signal encoding equipment. This device converts a 300 channel 60-1300 kHz carrier wave signal to a 34368 kb/s digital signal which is transmitted over a third order group transmission system.

In this paper, on the basis of the noise requirements of the paper, we concentrated on the description of the level allocation and number of bits for encoding the encoder. We also discussed the selection of parameters, such as the sampling frequency and the output code pattern of the encoder. We also briefly introduced the composition of the device and the testing results.

The high speed sampling-hold circuit and the encoder are the major components of this equipment. Advanced circuit techniques are used in both cases. In the encoder, the ECL D-type flip-flop has been used as the comparator to greatly simplify installation and adjustment.

In this device, the sampling frequency is 2864 kHz, the encoding digit is 10 bits, and the noise indicator is -61.1 dBmop/cH. The actual testing results of various functions could all meet the requirements.

I. INTRODUCTION

Digital communication, due to its superior transmission characteristics and ease of matching with various signal sources, has become increasingly important day by day. Especially the rapid development in optical fiber communication has had a strong promotional effect on the development of digital communications. However, under the actual conditions in our country, simultaneously with the development of digital communication, we must also study the conversion problem between the simulation communication system and the digital communication system.

There are two mutual conversion methods between simulation and digital systems. One is the "sound frequency conversion" which does not require a conversion device. However, it is necessary to add modulation and demodulation devices which frequently cause the deterioration of the channel characteristics. The other one is to use a special conversion device which converts the master-group signal into the form suitable for the new transmission system. It is possible to establish the fact that no added deterioration of channel characteristics will occur. The second conversion method has many advantages; however, there are also many technical problems. This paper involves the problem of converting the carrier wave master-group signal into digital signals. Actually speaking, it is an introduction to the new equipment which converts the carrier wave master-group signal through 27
a simulation/digital conversion into a coded third order group rate digital signal. In this, the high speed, high accuracy encoding circuit is not only the basic technique to solve the conversion problem, but also an important technique necessary to study other wide band signal encoding processes. This device not only can be used in the conversion of the carrier wave 300 channel group into the coded third order group transmission system, but also can be used in the transmission of a small coaxial 300 channel group signal into the optical fiber communication system.

In a carrier wave group signal encoding device, the noise design is most important. This paper emphasizes the discussion of several

major problems, such as the sampling frequency level allocation, encoding digit, encoder output code pattern and frame structure. It also briefly introduces the actual composition of the equipment and the test results.

II. DISCUSSION OF SEVERAL MAJOR PROBLEMS

1. Sampling frequency

The standard conversion frequency spectrum of carrier wave master-group signals is (812-2044) kHz. The line frequency spectrum of a 300 channel small co-axial system is 60-1300 kHz. In order to improve flexibility, the equipment can accommodate both. If we directly sample with respect to the (812-2044) kHz frequency spectrum, then the sampling frequency should be greater than 4088 kHz and the frequency band utilization is too low. If we sample with respect to the (600-1300) kHz frequency band, then the sampling frequency only has to be greater than 2600 Hz and the frequency band utilization is better. Therefore, we used (60-1300) kHz as the sampled signal. When the input group signal is the standard conversion frequency spectrum, the frequency varying device is used to change it to the (60-1300) kHz band and then we conduct sampling. In addition, in the actual selection of sampling frequency, we must consider the following factors: (1) integer multiples of 8 kHz, (2) filter is easy to realize, (3) source of sampling frequency. For convenience, the sampling frequency here is directly obtained from the digital part of this device.

Summarizing the above factors, the sampling frequency of this equipment is obtained from the 12th branch frequency of the clock frequency 34368 kHz, which is 2864 kHz ($>2\times1300$ kHz). At this time, the excess amount of the frequency band is 264 kHz. The filter implementation will not be difficult.

2. The level allocation and quantitative noise of the encoder

In a carrier wave group signal encoding device, in order to

satisfy the noise indicator required by the carrier wave net, the most important problem is to accomplish the optimum design of noise. In order to sufficiently utilize the signal-to-noise characteristics determined by the number of bits of the encoding, we must carry out the optimum level allocation for the encoder by considering the overload noise which is determined by the amplitude distribution characteristics of the carrier wave signal. After the dynamic range of the signal is determined, the upper limit value of the level allocation is determined by the dc overload voltage of the decoder. Its lower limit value is determined by the quantitative noise and the error code noise.

(1) The nature of master-group signal and the allocation of the encoding level

The frequency branching multiple channel signal is formed by voice signal, bell signal and guiding frequency. Among them, the guiding frequency is a single frequency signal and its level is invariant with respect to time. The levels of the other two signals are constantly changing, depending on the voice load. Both theoretical analysis and actual testing showed that for a frequency branching multiple channel signal, when the channel number is large ($\geq$60 channels), its instantaneous amplitude probability density can be considered as according to normal distribution. Hence, carrier wave master group signals can adopt the normal distribution law. In fact, the frequency branching multiple channel signal also includes the bell signal. In our country, we use the 2100 Hz in-band ring form. This may cause the master group signal to slightly deviate from normal distribution; however, the effect would not be significant. When the average value is zero, a normal distribution can be expressed as

$$p(x)=\frac{1}{\sqrt{2\pi}\sigma}e^{-\frac{x^2}{2\sigma^2}} \qquad (1)$$

where σ is the effective value. The amplitude 4σ is defined as the "peak value" whose probability is 3.17×10^{-5}. Thus, the peak coefficient = peak value/effective value = 4, which is 12 dB. The actual testing results of the carrier wave signal showed that the peak coefficient was slightly different from that of the theoretical value based on normal distribution [1]. Usually, the average peak coefficient of 28

the carrier wave master group signal is 12.7 dB and its upper fluctuation deviation is 3σ which is 1 dB.

According to the recommendation of CCITT, the average power of the carrier wave master group signal is

$$S=-15+10\log 300=+9.8\ \text{dBm0}$$

The upper limit deviation of the average power level fluctuation is $3\sigma_1 = 0.5$ dB.

In addition, we should also consider the adjustment deviation of the signal level in a carrier wave system $\Delta S = \pm 0.5$ dB.

Summarizing the above mentioned results, we can see that the dc overload level L_0 of the encoder should be higher than the average power of the master group signal by

$$L=p_i+3\sigma_1+3\sigma_i+\Delta S=12.7+1+0.5+0.5=14.7\ \text{dB}$$

$$L_0=L+S=14.7+9.8=24.5\ \text{dBm0}.$$

This means that the allocation of the zero base level (0 dBm) should be placed 24.5 dB below the dc overload level of the encoder which is 21.5 dB below the sinusoidal overload level. The lower limit of the dynamic range of the carrier wave master group signal is the level of the guide and monitoring frequency signal. The level allocations of the encoder obtained based on these relations are shown in Figure 1.

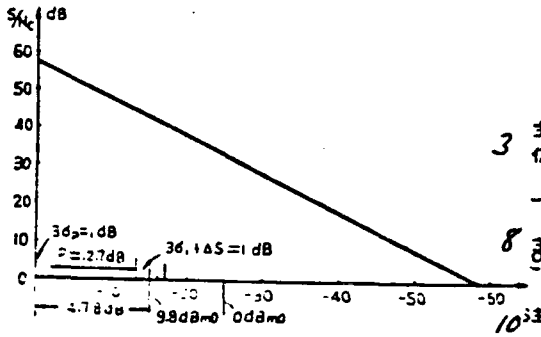

Figure 1. The level allocation of the encoder

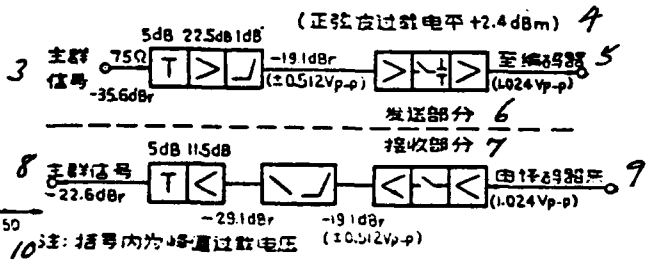

Figure 2. The level diagram of the transmitting and receiving parts

3--master group signal; 4--(sinusoidal wave overload level + 2.4 dBm); 5--to the encoder; 6--transmitting part; 7--receiving part; 8--master group signal; 9--from the decoder; 10--Note: The peak overload voltage is in the parenthesis.

Based on the above discussion, the level allocations at various points of the simulation part of the equipment are shown in Figure 2.

(2) The number of bits for encoding

The number of bits for encoding is determined by the noise power objective of the equipment.

The encoding noise power N_c produced in an encoder system is composed of the quantified noise N_q and the overload noise N_o. For linear encoding, when the signal is in normal distribution, the expression of encoding noise is

$$N_e = N_q + N_0 = \frac{2}{12}\left(\frac{2V}{2^n}\right)^2 \int_0^V \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{x^2}{2\sigma^2}} dx + 2\int_V^\infty (x-V)^2 \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{x^2}{2\sigma^2}} dx \quad (2)$$

where n is the number of bits for encoding and V is the peak overload voltage of the encoder. N_q is not related to the signal level, and its magnitude is determined by the quantified level. N_o is related to the ratio $\frac{V}{\sigma}$; when $\frac{V}{\sigma}$ is large, it is very small. It does not effect the total encoding noise. After $\frac{V}{\sigma}$ is decreased to a certain extent, N_o will increase rapidly and it will have a dominant affect in the total noise. If we carry out calculations using equation (2), we can plot the signal-noise-ratio characteristics as shown in Figure 3. From this figure, we can see that at a certain input level the S/N_c of the encoding system will have a maximum. If the input signal level exceeds this level, then S/N_c drops abruptly. By taking this level as the maximum allowable input level, then we can define the ratio between the encoder dc overload level and this level as the effective peak coefficient. This indicates that in order to obtain the largest S/N_c, we should adjust the average power level of the master group signal to the level required by the effective peak coefficient, which also means that the level allocation used in the previous section should be consistent with that here. However, because we cannot possibly accurately control the input level and also because carrier wave signal level varies significant with the load, therefore, there is no need to control it excessively with accuracy. From

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Figure 3, we can see that at 9 bits encoding the S/N_c obtained is the largest. We should adjust the signal level to -12.5 dB below the dc overload level. During encoding at 10 bits, the signal level should be at -13.1 dB. On the other hand, according to the discussion in the previous section, after considering the peak coefficient of the master group signal and various varying factors, the signal level should be placed at -14.7 dB below the dc overload level. At this time, it will not be possible to obtain the optimum S/N_c in theory. However, in a practical encoding system, we must consider various varying factors. Otherwise, once these variations emerge, the actually obtained S/N_c may be worse. Therefore, it can be assumed that the level allocation made in the previous section is adequate.

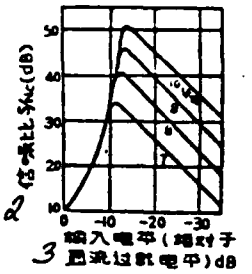

Figure 3. Theoretical value of S/N_c of a linear encoder (input signal is in normal distribution [3] 2--signal-to-noise ratio S/N_c(dB); 3--input level relative to dc overload level) dB

Using the S/N_c of allocated level of the encoder as the standard, let us convert the encoding and decoding noise powers to the zero relative level. Because the noise power can be considered to be concentrated in the half frequency band of the sampling frequency and is uniformly distributed, then after frequency band conversion and the addition of the constant weight of the voice signal 2.5 dB, the noise power of each frequency channel (bandwidth is 3.1 kHz) can be expressed as (when neglecting overload noise):

$$n_c \doteq N_s/\mathrm{CH} = 10\log\frac{1}{3\times 2^{2n}} + L_0 - 10\log\frac{\frac{1}{2}f_s}{W_s} - 2.5(\mathrm{dBmop/CH}) \qquad (3)$$

where n: number of bits for encoding

f_s: sampling frequency (kHz)

W_s: sound frequency channel bandwidth (kHz)

L_o: value of the standard level below the dc overload level (dB)

Using $f_s = 2864$ kHz, $W_s = 3.1$ kHz, $L_0 = 24.5$ dB to substitute into (3), and taking n = 9, we get

$$n_c = -63.7(\mathrm{dBmop/CH})(427\ \mathrm{pw/CH})$$

In the design of a master group encoding system, it is allowable that noise should be the noise target assigned to the shortest conversion section for this group signal in the carrier wave standard simulation circuit (line noise + frequency varying device noise). With regard to the master group signal, the assigned noise target for the most stringent conversion section is 883 pW/GH [3]. Hence, the allowable noise power of a master group signal encoding system should be 883 pW/GH (-60.5 dBmop/GH). This noise power should also be further distributed to the encoding terminal devices and the transmission line (including miscoding noise and trembling noise). In view of the present instrumental conditions, especially the difficulty in the realization of highly accurate decoding network, we can consider that the encoding terminal device can obtain a higher share, such as 783 pW. The remaining 100 pW is distributed along the transmission line. At this time, the noise power level of the encoding output terminal device should not exceed

$$n_c = -61.1(\text{dBmop/CH}) \quad (783\ \text{pw/GH})$$

According to the calculation of equation (3), we can find that when the imperfection of the encoder and the noise introduced by the PAM system are not considered, it is possible to satisfy the noise objective by using encoding at 9 bits. However, in an actual device, such imperfections and noise are always unavoidable. Therefore, in practice, we must use 10 bits for encoding.

3. The output code pattern of the encoder

In the output code patterns of the encoder, there are three typical code patterns which are the natural binary code, Grahm Code and the symmetric binary code. The gradual comparative coding system is more suitable to produce the natural binary code. The level encoder will output Grahm code. The symmetric binary code is more suited for the combination of full wave rectifying circuit and the gradual comparative encoder. The selection of the practical code pattern not only must consider the type of encoder, but also the noise caused by the transmission of erroneous codes.

The noise power caused by the transmission of erroneous codes is determined by the nature and probability of the erroneous code and the type of code. Furthermore, it may also be related to the magnitude of the input signal. Because there is not too much difference between the effect of the Grahm miscode and that of the natural binary code, we are only going to discuss the miscode noises of natural binary code and symmetric code in the following. In this discussion, we assume that: The dynamic range of the encoder is ±V, the average power of the signal is σ^2, miscoding is random and the probability is small, which is expressed by p_e.

(1) The natural binary code

The noise power caused by natural binary code is

$$N_e=\left\{V^2+\left(\frac{V}{2}\right)^2+\left(\frac{V}{4}\right)^2+\cdots\right\}\cdot p_e\doteq\frac{4}{3}V^2p_e \tag{4}$$

which is not related to the magnitude of the input signal. When the average power of the input signal is σ^2, the signal to noise ratio from equation (4) is

$$S/N_e=\frac{3}{4}\left(\frac{\sigma}{V}\right)^2\frac{1}{p_e} \tag{5}$$

In this design, $V/\sigma = 5.43$ (it is 14.7 dB when expressed by dB) therefore

$$S/N_e=-15.9-10\log p_e(\mathrm{dB}) \tag{6}$$

(2) The symmetric binary code

When using the symmetric binary code, the noise power due to miscoding is

$$N_e=\left[\int_{-V}^{V}(2x)^2p(x)dx+\left\{\left(\frac{V}{2}\right)^2+\left(\frac{V}{4}\right)^2+\cdots\right\}\right]\cdot p_e \tag{7}$$

When p(x) has a normal distribution and by neglecting the overloading of the encoder, we obtain the following from equation (7)

$$N_e=\left(4\sigma^2+\frac{1}{3}V^2\right)p_e \tag{8}$$

The noise power is related to the level of the input signal. The expression for the signal to noise ratio is

$$S/N_e = \frac{3}{12 + (V/\sigma)^2} \cdot \frac{1}{p_e} \quad (9)$$

Using $V/\sigma = 5.43$ in equation (9), we get

$$s/N_e = -11.4 - 10\log p_e \quad \text{(dB)} \quad (10)$$

Comparing equation (6) to (10), we can see that under identical miscoding rates, the signal to noise ratio of the symmetric code is higher than that of the natural binary code by 4.5 dB. Therefore, it is advantageous to use the symmetric binary code.

Let us assume the miscoding noise, similar to the quantified noise, is evenly distributed in the sampling frequency band. Then, based on equation (8) after frequency band conversion and introduction of the constant weight of 2.5 dB, the miscoding noise power of each 3.1 kHz wide sound frequency channel is

$$n_e = S + 10\log\left[\frac{12 + (V/\sigma)^2}{3}\right] + 10\log P_e - 10\log\frac{\frac{1}{2}f_s}{W_s} - 2.5(\text{dB mop/CH}) \quad (11)$$

Substituting $V/\sigma = 5.43$, $S = +9.8$ dB mo, $f_s = 2864$ kHz and $W_s = 3.1$ kHz into equation (11), we get

$$n_e = -8 + 10\log p_e \quad (12)$$

When the miscoding rate is $p_e = 10^{-7}$ (when the miscoding rate of reach relay is 10^{-9}, this corresponds to approximately 100 relay sections), we can obtain the following from equation (12)

$$n_e = -8 + 10\log 10^{-7} = -78(\text{dB mop/CH}) = 16(\text{PW/CH})$$

At this time, the noise caused by miscoding is very small. Therefore, the 100 PW line noise can be basically attributed to trembling. In addition, in order to facilitate the detection of miscoding and to prevent the appearance of a long series of "0" in the codes, we used an odd number check code. After 10 information bits, a monitoring bit is added. It is required that when even number of "1" appear in the information bits (including all "0"), the monitoring bit is "1", when an odd number of "1" exists, the monitoring bit is "0".

4. The frame structure

The selections of frame length and frame synchronistic code are related to synchronism. It was discussed in detail in the design. Here we will only briefly introduce the formation of the frame. As indicated in Figure 4, four groups of codes form a frame and each code group includes 12 bits. There are 48 bits in a frame. The 1-10 bits in each code group are used to transmit information. The 11th bit is the monitoring bit and the 12th bit is the frame synchronistic and duty bit. The frame synchronistic code pattern is 10 which occupies the 12th bit of the 1st and 3rd code groups respectively. The duty bit is used to transmit warning signals to the other end; it occupies the 12th bit of the 2nd and 4th groups. By using this arrangement and also by adding the odd number checking bit, the maximum number of continuous zeros in the codes will not exceed 21.

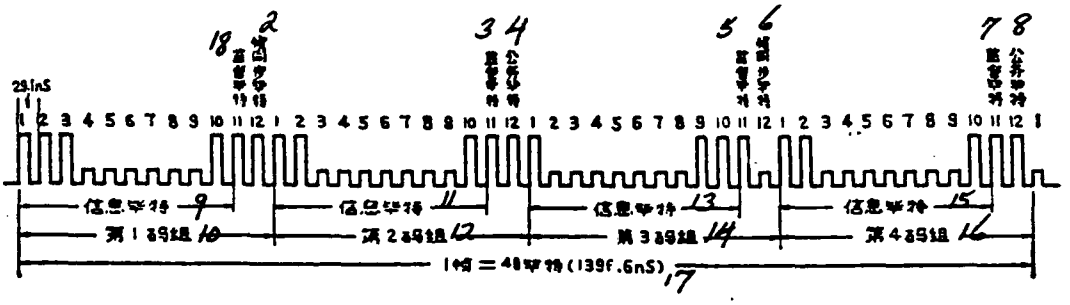

Figure 4. The frame structure
2--frame synchronistic bit; 3--monitoring bit; 4--duty bit; 5--monitoring bit; 6--frame synchronistic bit; 7--monitoring bit; 8--duty bit; 9--information bits; 10--the first code group; 11--information bits; 12--the second code group; 13--information bits; 14--the third code group; 15--information bits; 16--the fourth code group; 17--1 frame = 48 bits (1396.6nS); 18--monitoring bit

III. MAJOR PARAMETERS AND PERFORMANCE

1. Basic parameters of the carrier wave group signal

(1) signal frequency band (60-1300) kHz or (812-2044) kHz
(2) input/output impedance and reflective index, 75Ω, unbalanced <10%
(3) input level -35.6 dBr ±0.5 dB
(4) output level -22.6 dBr ±0.5 dB

2. The encoding part

(1) sampling frequency 2864 kHz
(2) quantified characteristics linear
(3) no. of bits for encoding 10 bits/sampling value
(4) encoder type gradual comparative type
(5) decoder type the current additive type formed by a trapezoidal decoding network
(6) code pattern symmetric binary code

3. The numerical part

(1) clock frequency 34 368 kHz ±20 ppm, on the transmission side; it is controlled by a crystal. On the receiving type, it is the ancillary type
(2) frame structure as shown in Figure 4
(3) frame synchronism the frame code is allocated discretely. It uses the bit by bit displacement format.
(4) transmission code speed 34368 kb/s
(5) transmission digital junction I. monopolar: zeroing code. output from ECL integrated circuit. Driving resistance of the double cable is 110Ω. II. Bipolar: according to CCITT regulations*
(6) receiving digital junction: I. zeroing code. Use an ECL linear receiver to receive the digital signal sent from the double cable. The line length is not greater than 30 meters. II. Bipolar: according to CCITT regulation

4. Major characteristics of the equipment

(1) frequency characteristics of net decay loss
The fluctuation in the (60-1000) kHz frequency band ≤±0.3 dB
The fluctuation in the (1000-1300) kHz frequency band ≤±0.5 dB
(2) the net loss level characteristics

Using the 0 dB mo testing level as the basis, in the range of ±21 dB mo to -10 dB mo, the net loss fluctuation is smaller than ±0.5 dB.

(3) noise characteristics

In the 3.1 kHz bandwidth sound frequency channel, the noise is not greater than -61.1 dB mop.

IV. THE COMPOSITION OF THE EQUIPMENT

The composition of the master group encoding equipment is shown in Figure 5. Now let us briefly introduce the working function of each component.

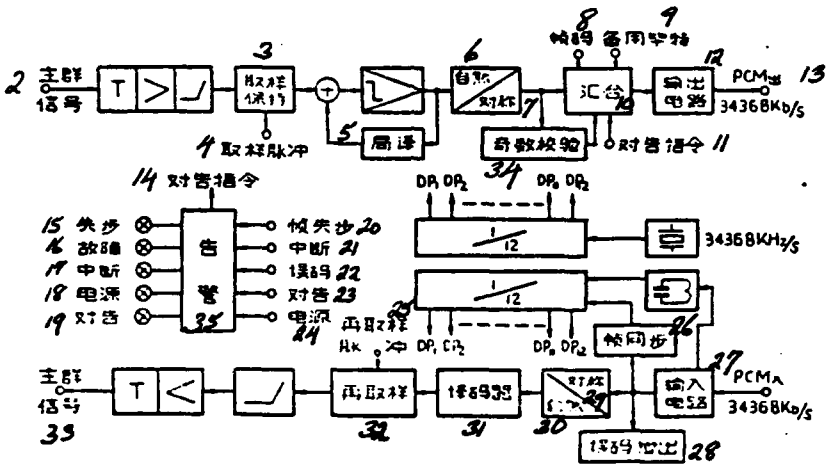

Figure 5. Composition of the master group encoding equipment 2--master group signal; 3--sample-hold; 4--sampling pulse; 5--partial decoding; 6--natural; 7--symmetric; 8--frame cools; 9--spare bit; 10--converging area; 11--responding command; 12--output circuit; 13--PCM output; 14--responding command; 15--skipping; 16--breakdown; 17--interruption; 18--power source; 19--responding; 20--frame skipping; 21--interruption; 22--miscoding; 23--responding; 24--power source; 25--resampling pulse; 26--frqme synchronism; 27--input circuit; 28--checking-out miscoding; 29--symmetric; 30--natural; 31--decoder; 32--resampling; 33--master group signal; 34--odd number checking; 35--alarm

1. Transmission amplifier

The input of the amplifier is the (60-1300) kHz 300 channel master group signal. The signal is sent to the sample hold circuit through the attenuator, amplifier and low pass filter. The function of the amplifier is to amplify the input signal to the required level. The attenuator has a 6 dB adjustable range in order to realize the

*bipolar junction has not been developed

optimal load adjustment of the encoder. The low pass filter has at least 40 dB attenuation with respect to frequencies above 1.5 MHz in order to avoid the occurrence of noise during the sampling process. 33

2. The sample-hold circuit

In the sample-hold circuit, the rate of 2864 kHz is used to sample the simulated signal and the signal level after sampling is maintained unchanged during the entire coding period in order to ensure the accuracy of encoding. Acting as a high speed sample-hold circuit, the voltage sampling, voltage maintenance and transistor constant current driving form is used. The principle of this circuit is shown in Figure 6. The sampling gate is a bridge gate formed by four Schockley diodes. This diode has the advantage of low forward resistance, large reverse resistance, combined capacitance and short storage time which is suitable for the requirements of a high speed, high accuracy sampling gate.

The 29.1 ns wide sampling pulse, after passing through the ECL integrated circuit, is added to the differential amplifier with a constant current source using a balanced form. It is added to the sampling gate from the emitter output device. By adding an emitter output device between the sampling gate and the pulse amplifier, it is possible to reduce the waveform distortion caused by the distribution capacitance to increase the balance of the driving pulse and to improve the resonance wave distortion. In addition, in order to improve the signed distortion noise ratio, the rising and falling times of the sampling pulse should be as short as possible.

The pre-amplifier is formed by a first order emitter output device in order to maintain low resistance output during charging of the capacitor.

The post-amplifier has an input impedance of >6 MΩ in order to satisfy the requirement that the falling part is 1/4000.

3. The encoder

The function of the encoder is to convert the PAM signal after sampling the 10 bits PGM signal. The encoder uses a simple circuit, high accuracy, one-by-one comparative encoding form. Its principle is shown diagrammatically in Figure 7.

1) The comparator

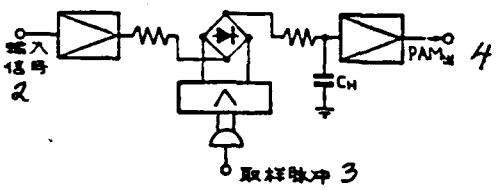

Figure 6. The sample-hold circuit
2--input signal; 3--sampling pulse; 4--PAM_{output}

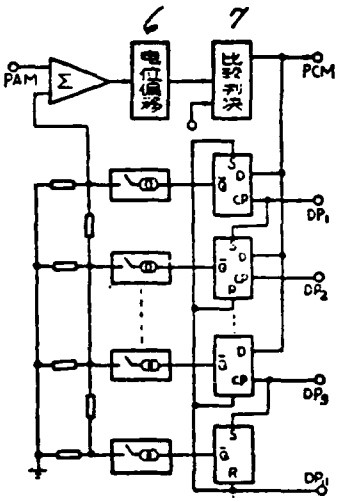

Figure 7. Principle of the encoder. 6--voltage shift; 7--comparative judgment

In a 10 bit encoder, when the maximum input signal is 1 V_{p-p}, the minimum quantified level is Δ = 1mV. If the indecisive range of the evaluated point is chosen to be $\Delta/3$, then the maximum resolution of the comparator is required to be 1/3 mV. When the clock frequency is 34368 kHz, the encoding circuit time delay should be smaller than 29.1 ns. In order to realize the high resolution, small time delay comparator, the ECL model D flip-flop is used to perform the comparative judgement and the ECL linear receiver is used as the voltage additive type of amplifier.

Testing results showed that the D type flip-flop had a maximum resolution of approximately 1 mV at the characteristic middle point of the transformation. If we further consider the variations of the

component parameters and electric power supply voltage, the D-type flip-flop resolution is 10 mV and the summation amplifier gain is 30 dB. The summation amplifier uses a bipolar line receiver in series; its center gain is 35 dB.

The comparator formed by a D-type flip-flop and line receiver is a small time delay, high resolution, simple adjustment, stable performance and easy to put together comparative judgement form.

2) The partial decoding logic circuit

This circuit uses the D input end and the R-S end of a first order flip-flop to simultaneously accomplish the feedback logic and memory functions to greatly simplify the composition of the circuit and to reduce the time delay of the return circuit.

3) Constant current source and switching circuit

The constant current source uses a single tube circuit as shown in Figure 8. In order to compensate for the temperature characteristics of V_{BE}, an error checking circuit formed by a high gain operational amplifier and standard transistors is used in the base bias power supply to ensure that in the given temperature range the relative error is less than 200 ppm between various constant current sources.

In order to allow the switching circuit to be directly driven by the logic circuit, its input conversion level should be the ECL logic level. In order to conveniently link the constant current source with the logic circuit, the switching circuit uses an unsaturated differential circuit.

4) The resistance network

In order to reduce the time delay of the resistance network, a trapezoidal composite thin film resistance network is used. In order to ensure the accuracy of encoding, the accuracy of resistance (relative value) is 200 ppm.

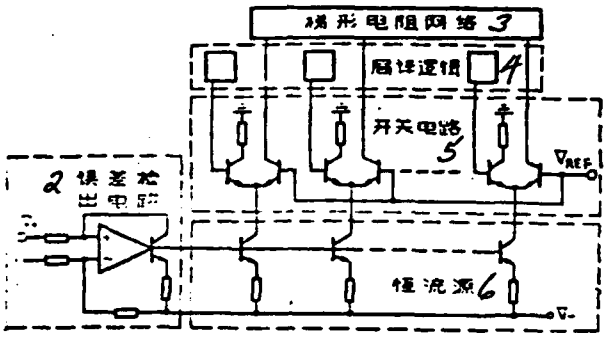

Figure 8. The constant current source and the switching circuit
2--error finding circuit; 3--trapezoidal resistance network; 4--partial decoding logic; 5--switching circuit; 6--constant current source

4. Code conversion and converging circuit

The output of a progressive comparative encoder is in natural binary code. First, use a natural/symmetric code converting circuit to convert it into symmetric binary code and then plug in the monitoring bit using the odd number checking encoding circuit to form the odd number checking code to be sent into the converging circuit. In the converging circuit, the information code, frame synchronistic code and opposite end alarm information are converged together according to the regulated time relation to form the 34368 kb/s code flow to be sent to the output junction circuit. The output junction circuit will convert the input digital signal into the form of the transmission system. When used in coordination with the optical cable transmission system, the output junction circuit uses the double wire form driven by the ECL integrated circuit. If the third order group PGM standard output form is needed, it is possible to use the exchange junction circuit disk method to obtain the bipolar standard output.

5. The receiving system

The digital signal transmitted from the digital transmission system is converted into the NRZ code form by the input junction circuit.

Using the exchange junction circuit disk method, it is possible to obtain the junction which matches the optical cable transmission system or a standard junction. The output NRZ code of the junction circuit is sent to the frame synchronism circuit, the symmetric code/natural code converting circuit and the miscoding monitoring circuit, respectively. The frame synchronism circuit picks out the frame synchronistic code from the digital signal to carry out comparison with the local frame synchronistic code. When inconsistency (i.e., a synchronism) exists, output displacement pulses are transmitted to cause the displacement of the frequency branching circuit in the receiving part to catch the frame synchronistic code sent from an external line until the frame synchronism between transmission and receiving is realized. In addition, there is an opposite end alarm receiving circuit in the frame synchronism circuit to receive the alarm information transmitted from the other end. The symmetric code/natural code converting circuit will first convert the input symmetric binary code into natural binary code and then transmit into the decoder. In the decoder, the input serial code is first converted into parallel code by a series to parallel converting circuit and then converted into the NRZ type of PAM signal by the decoding circuit. It is then sent to the sampling circuit after buffering amplification. In the time interval DP_2-DP_8 in the sampling circuit, let us sample the NRZ type PAM sample again to obtain the 50% vacant PAM signal. This PAM signal is demodulated by the low pass filter to obtain the simulated signal occupying the (60-1300) kHz frequency band. The frequency response distortion introduced by signal demodulation is compensated by the balancing device. Finally, through the use of an amplifier and an attenuator, the signal is adjusted to the regulated output level to be transmitted to the carrier wave commmunication equipment.

6. The timing circuit

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In the transmission part, the clock pulse is provided by the 34368 Hz crystal oscillator whose stability is ±20 ppm. Then, through 12 frequency branching circuits, the various control pulses required for the sampling, encoding and frame synchronism circuits are produced.

In the receiving part, the clock signal is obtained from the digital signal transmitted from an external line. When using ancillary bit synchronism, the clock extracting circuit extracts the clock information from the digital signal and then directly produces the clock pulses in the receiving part. Then, the various control pulses needed for the frame synchronism, decoding and resampling circuits are produced by the 12 frequency branching circuits.

7. Monitoring of miscoding and the alarm system

The miscoding monitoring circuit carries out checking with respect to the digital signal transmitted by the external line according to the odd number code formation rule to pick out the miscoding introduced during the transmission process. It obtains the erroneous pulse sequence and displays the number of miscodings on the miscoding counting circuit. When the miscoding rate is greater than 10^{-4}, an alarm signal is produced.

The alarm system includes features, such as missing step, breakdown*, code interruption, miscoding, and power failure, etc. When breakdown or code interruption happens, in addition to producing a corresponding warning on this end, it also sends opposite end alarm command to the transmission part of this end to allow the breakdown information to reach the other end through the duty bits.

V. CONCLUSIONS

An experimental machine was developed according to the design plan. The high speed, high accuracy sample-hold circuit and the encoding circuit are the highly complex components. Advanced circuit techniques are used for those circuits. The encoder reached the 10 bits static accuracy. All the high speed pulse circuits used are the ECL integrated circuits produced domestically.

*When the frame missing step exceeds 1 second, it is considered to be out of sequence.

(received October 1980)

The main characteristics of this equipment are its net attenuation frequency characteristics, net attenuation level characteristics and noise characteristics. The actual measured results are shown in Figures 9-10. They all satisfy the design requirements. However, the margin of the noise characteristics is not sufficient. In addition, it is more critical with large signals, which is yet to be improved upon by further study.

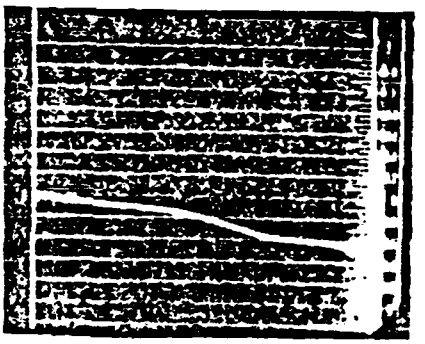

Figure 9. The net attenuation frequency characteristics

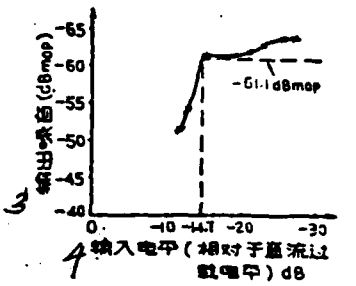

Figure 10. Noise characteristics
3--output noise (dB mop);
4--input level (relative to the dc overload level)

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