AD-A126 660 UNIVERSAL PIN ELECTRONICS(U) GIORDANO ASSOCIATES INC SPARTA NJ P C JACKSON 03 NOV 82 CECOM-81-0146-F DAAK80-81-C-0146

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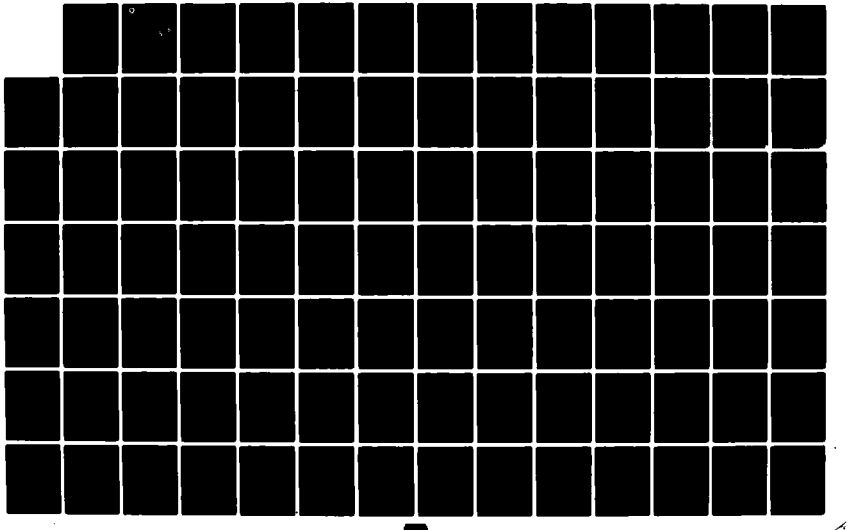

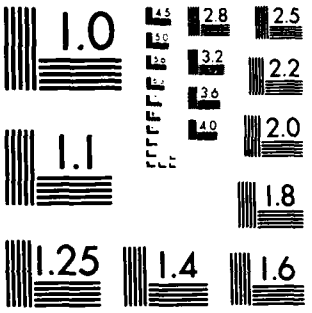

RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CECOM-81-0146-F

UNIVERSAL PIN ELECTRONICS

Philip C. Jackson

GIORDANO ASSOCIATES, INC.
21 White Deer Plaza
Sparta, NJ 07871

SEPTEMBER 1982

Final Report for Period Aug. 1981-Sep. 1982

DISTRIBUTION STATEMENT
Approved for public release;
distribution unlimited.

PREPARED FOR:
US Army Test, Measurement and Diagnostic
Technology Laboratory
Program Manager for TMDE

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U S ARMY COMMUNICATIONS—ELECTRONICS COMMAND
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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER CECOM-81-0146-F	2. GOVT ACCESSION NO. AD-A116660	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) UNIVERSAL PIN ELECTRONICS		5. TYPE OF REPORT & PERIOD COVERED FINAL AUG 81 - Sep 82
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) PHILIP C. JACKSON		8. CONTRACT OR GRANT NUMBER(s) DAAK80-81-C-0146
9. PERFORMING ORGANIZATION NAME AND ADDRESS Giordano Associates, Inc. 21 White Deer Plaza Sparta, NJ 07871		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62746A 1L162746A094 01, 012
11. CONTROLLING OFFICE NAME AND ADDRESS US Army Communications Electronics Command ATTN: DRCPM-TMDE-LT Fort Monmouth, NJ 07703		12. REPORT DATE September 1982
		13. NUMBER OF PAGES 122
14. MONITORING AGENCY NAME & ADDRESS(If different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

APPROVED FOR PUBLIC RELEASE: DISTRIBUTION UNLIMITED.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

PIN ELECTRONICS
AUTOMATIC TEST EQUIPMENT
BUILT IN TEST
DECOMPACTION

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The report describes a unique and advanced test system architecture which has the ability to put virtually an entire test system into a test head and is capable of operating at repetition rates of 100MHz and with test vectors of 250,000 bits deep. In addition, this new architecture has the potential to also provide extended analog capability with greatly improved reliability in a small physical package and at a reduced cost over conventional automatic test equipments. Block diagrams of the overall system, major subsystem and the single channel are presented and described. Specifications of the overall system and

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the single channel are also presented.

In addition to its use as an off-line ATE, this architecture can bring its inherent testing power directly to built-in-test (BIT) applications.

DAAK80-81-C-0146-II

UNIVERSAL PIN ELECTRONICS

Final Report

Contract DAAK80-81-C-0146

Prepared For

Test Technology Division

Test, Measurement, and Diagnostic Technology Laboratory

US Army Communications - Electronics Command

Fort Monmouth, NJ 07703

Prepared by

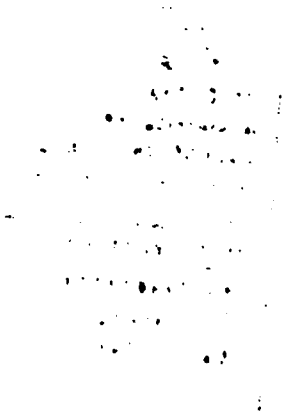
Philip C. Jackson

Giordano Associates Inc.

21 White Deer Plaza

Sparta, NJ 07871

November 3, 1982



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ABSTRACT

Most Automatic Test Equipment (ATE) currently available is large, costly, and complex in nature. It typically employs multiple chassis of stimulus and measurement instrumentation and elaborate switching systems. Most testers require the use of complex and costly interface devices as well. Analog testing and the various types of digital testing are accomplished by different tester subsystems. Even with the size, complexity and cost these testers are unable to accommodate the maximum repetition rates, array sizes, and throughput required to test today's LSI, VLSI and VHSIC components and the subsystems and systems utilizing these complex chips.

The Universal Pin Electronics (UPE) architecture represents the first significant breakthrough in testing technology in well over ten years. UPE has the potential to provide extensive analog and digital test capability with greatly improved reliability, in a much smaller physical package and at a reduced cost as compared to conventional ATE. Many stimulus and measurement instruments are no longer needed and the requirement for complex switching systems is eliminated. The same is true for most adapters or interface devices. Each pin electronics channel can be implemented via a small chip set or a single integrated module. This common set contributes to standardization within the tester and drastically affects overall size, weight, and cost.

UPE uses common tester electronics to create analog, parametric digital, and functional digital stimulus/measurement capability. The UPE architecture produces the following general advantages:

a) Reduced size

b) Reduced weight

c) Reduced cost

d) Increased reliability

For functional digital testing it results in breakthroughs in terms of:

a) Maximum test repetition rate

b) Maximum array size (vector depths)

c) Overall tester throughput

It also results in the following:

a) Reduction in the use of costly second generation instruments

b) Reduction in the use of costly ATE switching systems

c) Reduction in the size, complexity, and use of interface devices

In addition to its use as off-line ATE, Universal Pin Electronics can bring its inherent testing power directly into built-in test (BIT) applications. It is equally effective in dealing with both analog and digital circuitry since functional digital, analog, and parametric digital stimulus and measurement capability can be effected in each UPE channel. Other features pertinent to BIT include:

a) Increased test capability and reliability

b) Technological capability to accommodate the most

modern prime systems

c) Reduced size, weight, and cost

d) Equal effectiveness on analog and digital systems

e) Ability to filter false alarms to increase user confidence

f) reduction in off-line ATE Requirements

g) Maximized compatibility with off-line ATE

With this capability, UPE can accommodate the most stringent BIT requirements. At the same time, its extremely small size and modest weight allow such powerful capability to be utilized with little penalty to the prime system.

Universal Pin Electronics is a revolutionary concept. It has both ATE and BIT applications. The UPE architecture is structured to take advantage of the new technology continuously emerging from the semi-conductor industry. As new capabilities evolve, the UPE stimulus/measurement spectrum will expand accordingly. The report to follow delineates the UPE development program to date.

SECTION I

1.0 INTRODUCTION

The testing concept which led to pin electronics began with the explosion in the use of digital IC' some 10 to 20 years ago. The primary approach used to test the large digital circuit arrays which came upon the testing scene was to apply patterns of ones and zeros across all UUT input pins simultaneously while monitoring the subsequent response across all UUT output pins. In those early days, the testing community was content to perform this functional philosophy at rates governed by the I/O bus rate of the test system controller. The speed and density of the UUT logic circuitry at that time allowed good correlation between test results achieved at this low speed and actual performance in the real world at higher speeds.

With the boom in MSI and LSI, speed and density increased and tolerances plummeted. Many experts began to view testing at or near actual usage speeds as absolutely necessary for good correlation of test results. Thus, burst mode pin electronics was born. Early burst mode testers utilized a single, high speed semi-conductor memory element behind each driver/receiver. This freed the maximum test rate from the constraint of the I/O bus. Spurred on by rapidly falling chip prices, including memory elements, more elaborate architectures have evolved which allow tri-state control for real-time microprocessor bus testing, nested looping, real-time masking, etc.

In part, pin electronics derives its name because there is a distinct channel of test electronics devoted to each UUT pin. This is unlike some other architectures which utilize racks of

instruments which are switched across the UUT interface. Another reason revolves around physical placement which has become critical as testing speeds have increased. Lead lengths between the pin electronics driver/receiver and the UUT pins are held to an absolute minimum. Highly imaginative physical packaging schemes have been utilized to achieve this end. The approaches vary depending on the physical nature of the UUT (e.g. component testers usually package in a carousel arrangement, board testers in a rectangular alignment). Thus, the placement of the tester's drivers and receivers immediately adjacent to the UUT pins provides another reason for the name "pin electronics".

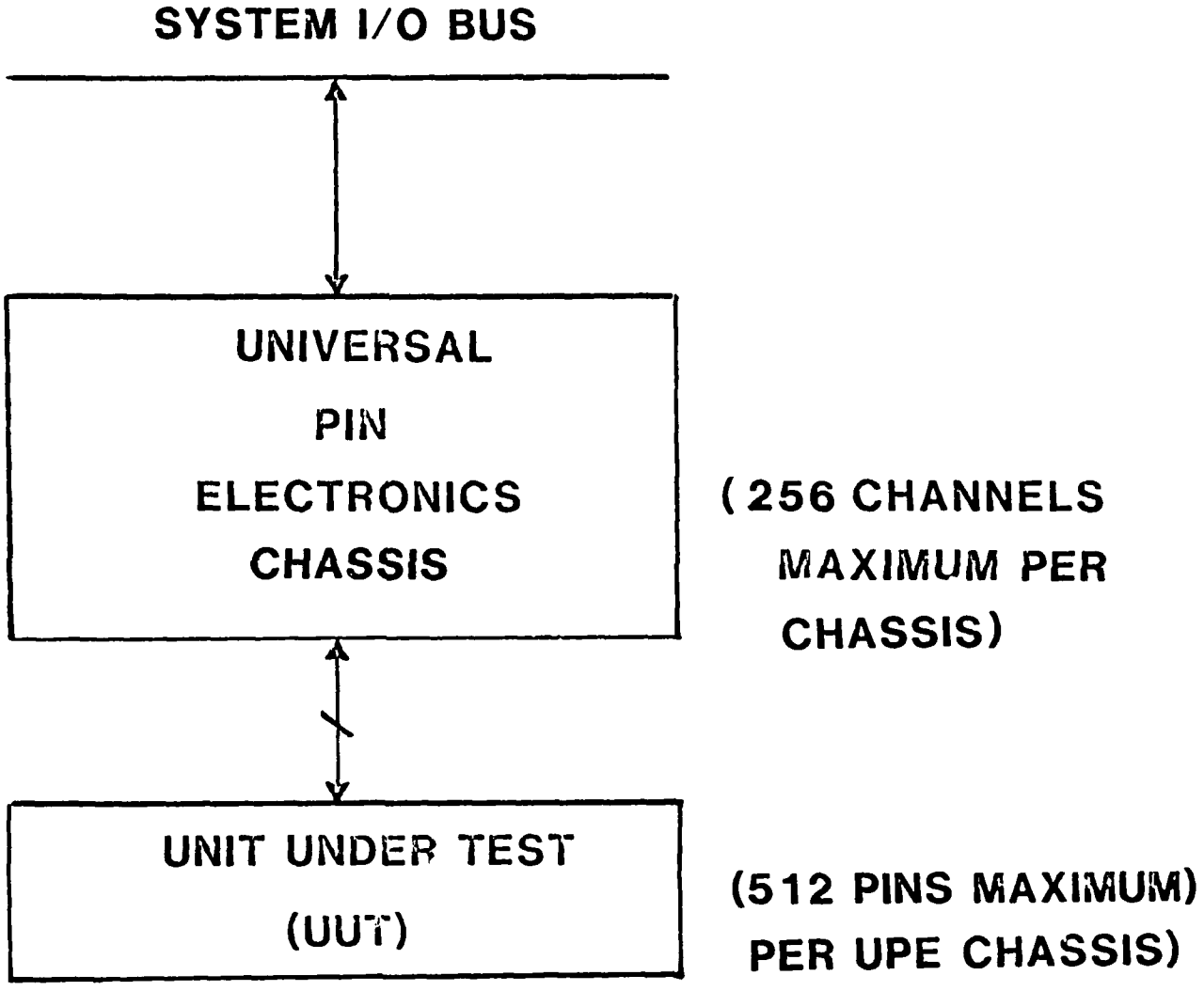
Today the stage is set for a dramatic increase in the use of pin electronics. Current semi-conductor technology provides the means to expand its scope far beyond functional digital testing. Advances in hybrid packaging, microprocessors, A/D and D/A techniques, memory technology, etc. make it highly likely that the role of pin electronics can be expanded to provide broad analog test capability and digital capabilities beyond just functional testing (e.g. parametric digital testing). The UUT stimulus spectrum of pin electronics can by expanded to encompass complex waveforms normally generated by instruments such as pulse generators, waveform generators, etc. In a like manner, the pin electronics measurement spectrum can be expanded to make measurements such as those normally requiring a digital voltmeter, timer-counter, waveform analyzer, etc. With the exception of high power and very high frequency applications, an almost universal testing architecture is possible.

With this architecture, Universal Pin Electronics (UPE) has

the potential to provide extensive analog and digital test capability with greatly improved reliability, in a much smaller physical package and at a reduced cost as compared to conventional ATE. A basic interface diagram is given in Figure 1-1 and shows the need for complex switching systems is eliminated. The same is true for most adapters or interface devices. The ability to put an entire test system into the size of a conventional test head realizes the shortest possible lead lengths and thus, the optimal signal integrity. Each pin electronics channel can be implemented via a small chip set or a single integrated module. This common set contributes to standardization within the tester and drastically affects overall size and weight. When yield figures improve as is traditional in the semiconductor industry, costs are expected to be dramatically reduced.

The objective of the current program was to develop a pin electronics architecture (hardware and software) capable of broad analog, digital and hybrid test capabilities on a minimum set of chips per channel. The goal was and is to realize affordable, reliable and compact test capability. Block diagrams of the overall analog, digital and hybrid pin electronics system plus detailed block diagrams of major subsystems have been generated. A functional description of each block in every diagram is provided including information as to the interrelationship between all blocks.

Detailed specifications on the overall system and each of the major subsystems have been generated. All pertinent parameters are specified including driver accuracy, source/sink current, slew-rates, output impedance, voltage range and



UPE SYSTEM INTERFACE DIAGRAM

FIGURE 1-1

resolution, etc. Also specified are receiver accuracy, response time, input impedance, voltage range and resolution, etc. Included are the optimal number of clocks plus clock duration, resolution, accuracy and the number of delays plus delay duration, resolution, accuracy, etc.

In addition, detailed electrical specifications delineate parameters such as skew times, tri-state switching, maximum shunt capacitance, etc. Other pertinent factors are described including automatic calibration, self-monitoring, clock synchronization, universal pin programmability, etc. An extensive component investigation was conducted so that the latest state-of-the-art component specifications are denoted for use in each major subsystem.

The program has attempted to optimize all of the more basic operating parameters such as maximum frequency, accuracy, etc. More subtle architecture innovations have also been pursued. For example, most current pin electronics operate at the programmed frequency only until the local memory capacity has been exhausted. At this point testing is momentarily halted while all appropriate local memory is refreshed from the mainframe. The program has investigated techniques which allow the local memory elements to effectively compact data so that these undesirable pauses are eliminated.

Section 2 provides a functional description, block diagrams and specifications of the overall UPE system. Section 3 contains a functional description, block diagram, and subsystem specification for the I/O interface. Sections 4 through 14 provide the same information items for the local memory, D/A conversion and

logic level generator, decoder/frequency multiplier, optional decompaction module, functional digital subsystem, driver/receiver, clocks/delays/APG, A/D converters, control software, calibration subsystem, and optional fault isolation subsystem. Section 15 is devoted to conclusions drawn from the effort, while section 16 makes pertinent recommendations.

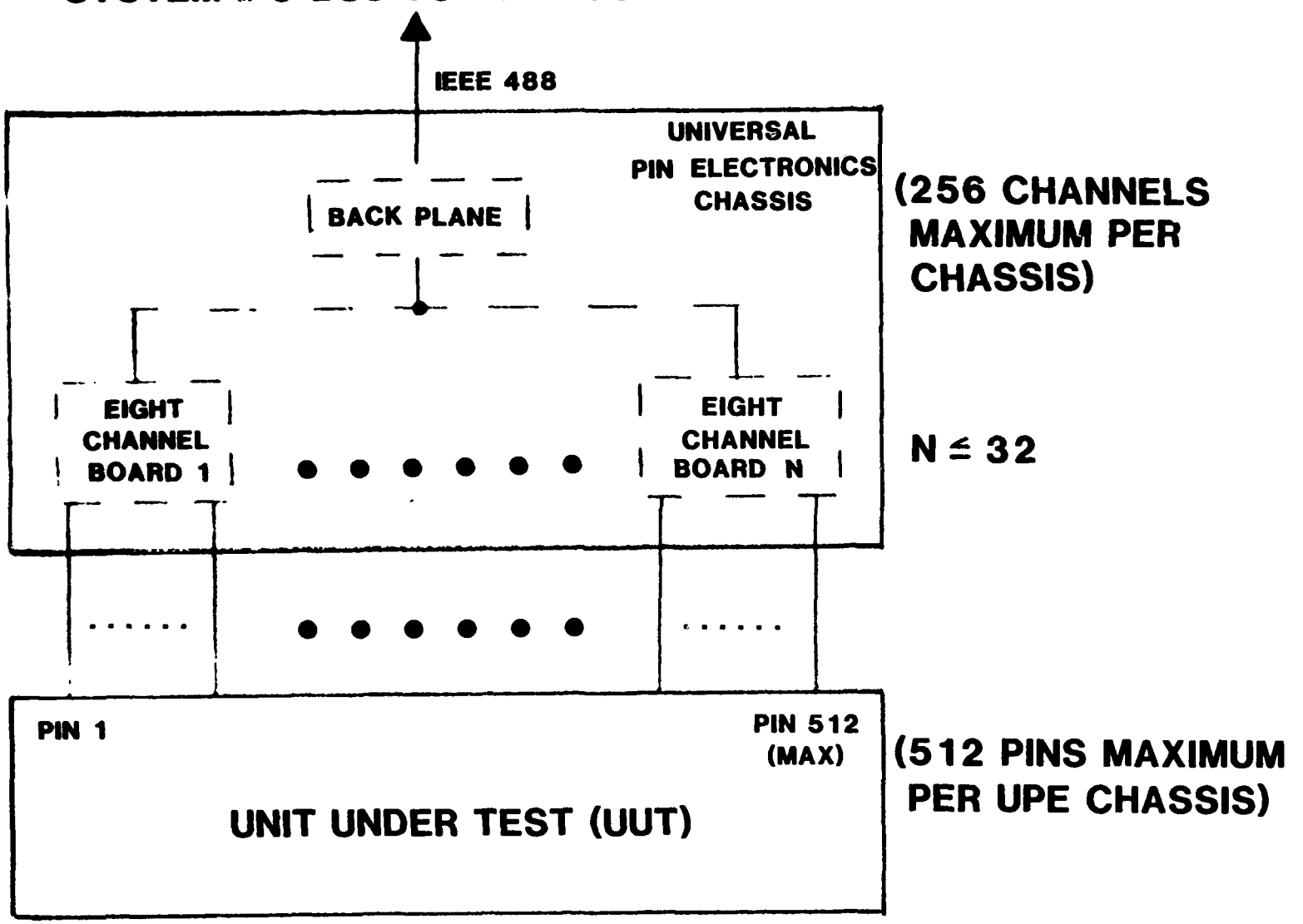
SECTION II

2.0 OVERALL SYSTEM

2.1 FUNCTIONAL DESCRIPTION

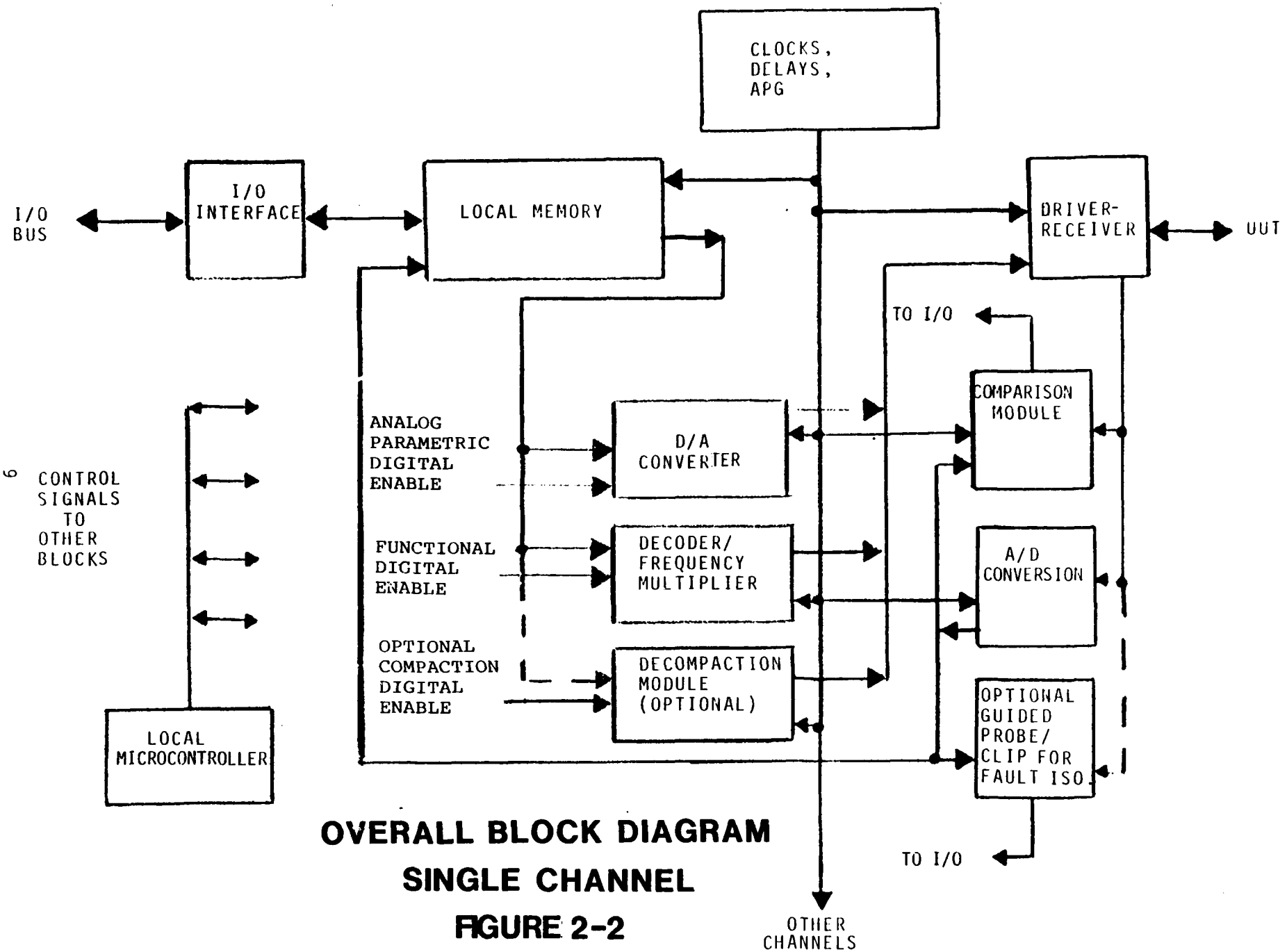
Figure 2-1 provides a UPE system interface diagram. The major elements in each UPE chassis are a backplane containing a backplane microcontroller, clocks, delays, algorithmic pattern generator, etc. and up to 32 eight channel boards of test electronics. A local microcontroller is assigned to each eight channel board. Up to 256 channels are available in each UPE chassis which provides for up to 512 UUT pins. Multiple chassis may be synchronized for larger UUT pin count requirements. Each chassis or group of chassis is linked to a main controller via the standard IEEE-488 bus. Since each UPE channel has a total test capability in terms of functional digital, parametric (time-domain) digital and analog stimulus/measurement, this report will center on the description of a single channel and revert where appropriate to eight channel board or chassis-wide explanations.

Figure 2-2 provides an overall block diagram of each UPE channel. The major elements are an I/O interface, a local memory, D/A converter and logic level generator, decoder/frequency multiplier, an optional decompaction module, functional digital subsystem, driver/receiver, clocks/delays and algorithmic pattern generator module, A/D conversion module, and an optional guided probe/clip for fault isolation. The driver/receiver is actually part of the functional digital subsystem but is of sufficient importance to warrant its own section. The local microcontroller and I/O interface perform



DETAILED UPE SYSTEM INTERFACE DIAGRAM

FIGURE 2-1



OVERALL BLOCK DIAGRAM

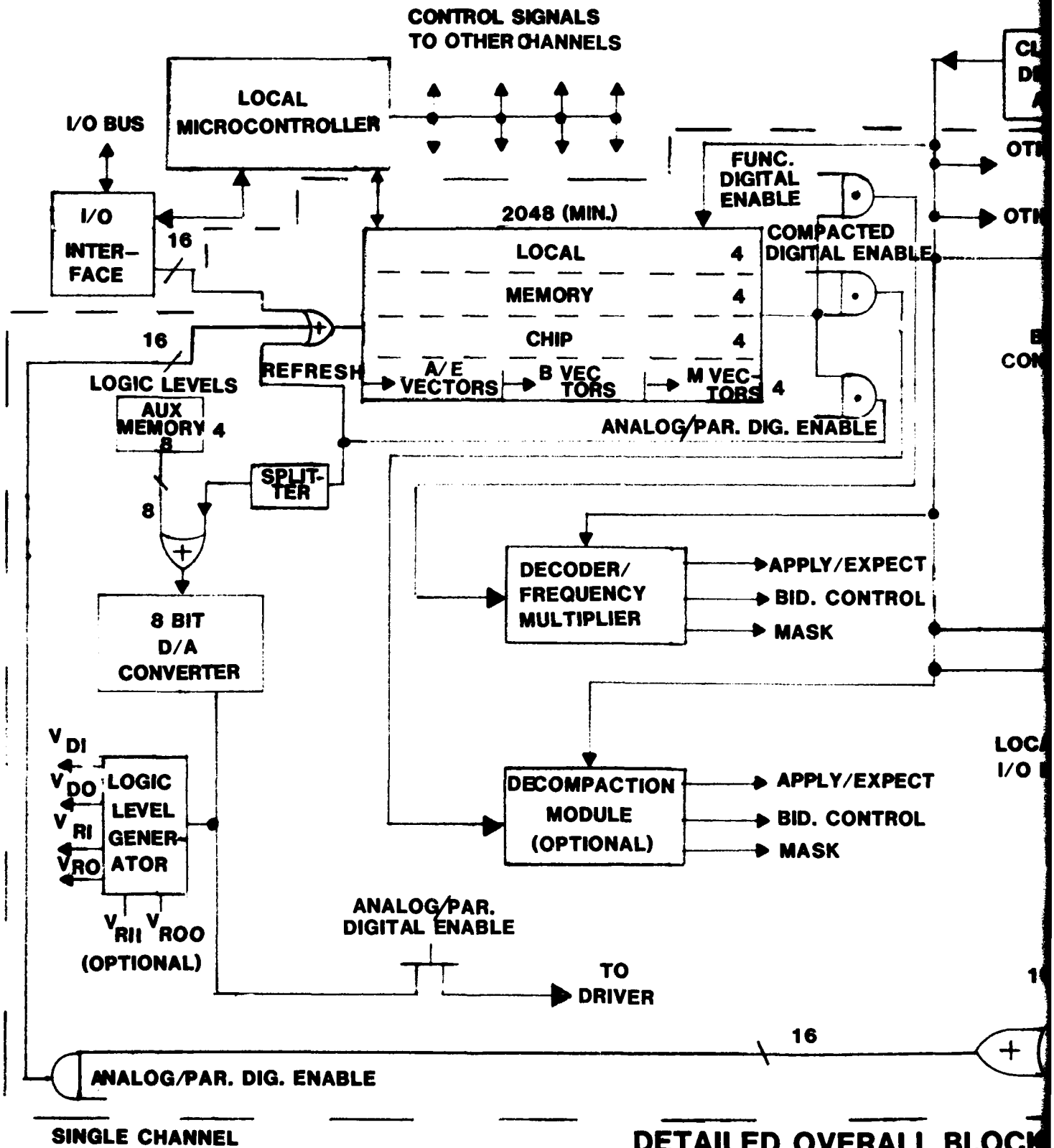
SINGLE CHANNEL

FIGURE 2-2

board-wide functions and the clock/delays system-wide functions.

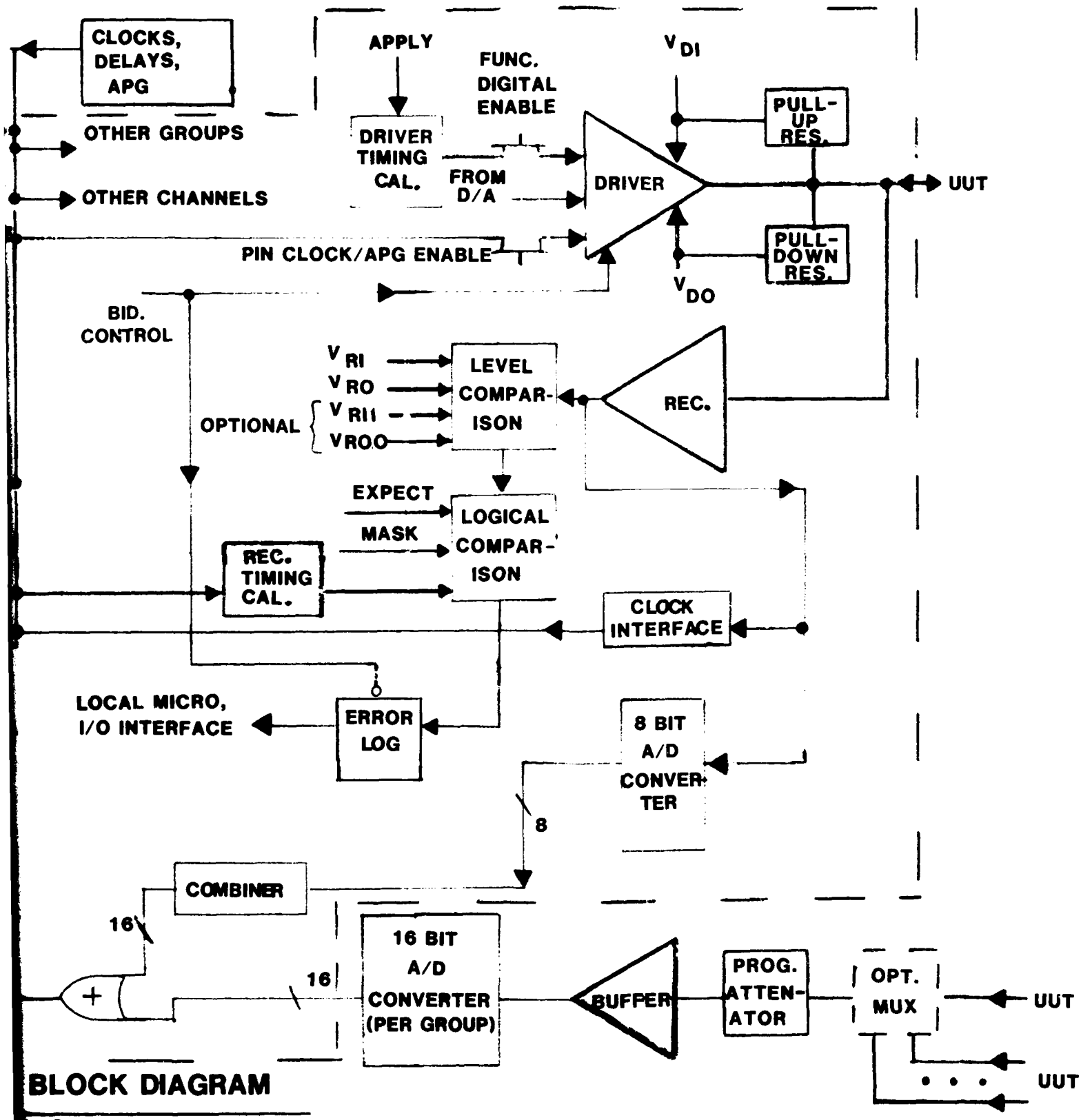
Each of the major channel elements is discussed in detail in sections to follow. Figure 2-3 provides a more detailed block diagram of a channel in the overall system. Since each pin electronics channel has such broad test capability, an attempt will be made to describe its operation by an individual description of each of the stimulus and measurement capabilities.

Before a test is initiated, each channel is defined as to whether it is to implement an analog stimulus, an analog measurement, a functional digital stimulus, a functional digital measurement, a parametric digital stimulus, or a parametric digital measurement. Analog stimuli and parametric digital stimuli operate in much the same fashion. Referring to Fig. 2-4, the local memory of each channel is 16 bits wide by 2K bits deep. At a memory read rate of 30 MHz, 16 data bits are available every 33 ns. The 16 data bits are strobed in a "ping-pong" fashion into two registers via a splitter circuit. Eight bits of data are extracted at a time from each of the two 16 bit registers. Each 8 bit segment is used as an input to the channel's 8 bit D/A converter. The output from the D/A converter to the channel driver provides either a parametric digital waveform or an analog waveform depending upon the software algorithm utilized by the local microcontroller. With a 30 MHz memory, 16 bits of data can be accessed every 33 ns, or in an equivalent fashion 8 bits of data every 16.7 ns. Thus, an effective 8 bits of data is realized at a 60 MHz rate. Analog and parametric digital waveforms up to 20MHz are attainable although distortion is considerably less at frequencies up to 5MHz. Refer to section 5 for additional



DETAILED OVERALL BLOCK

FIGURE 2-3



BLOCK DIAGRAM

-3

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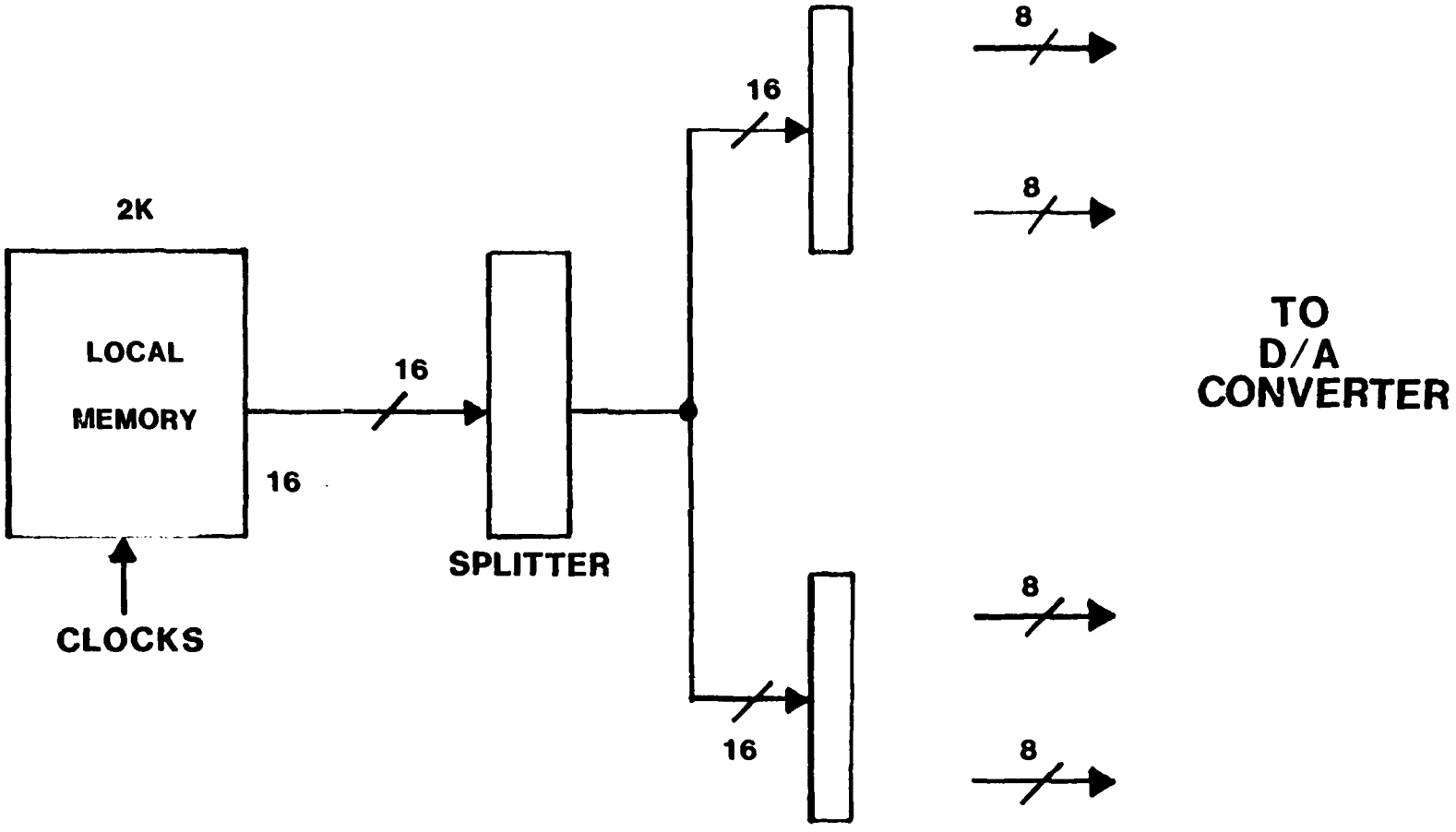


ANALOG AND PARAMETRIC DIGITAL STIMULI

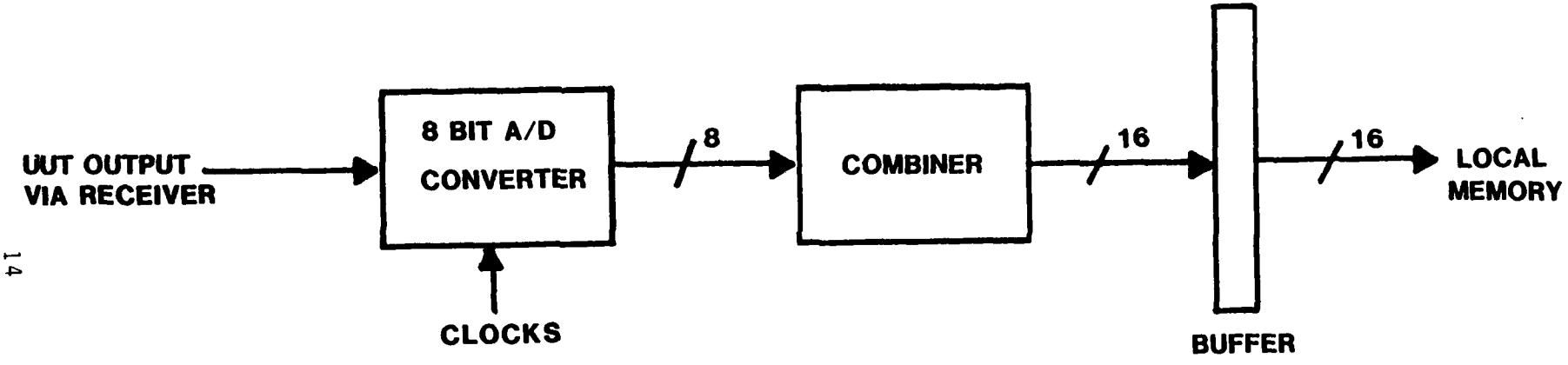
FIGURE 2-4

detail.

Analog measurement and parametric digital measurement capability is effected in much the same manner. Output signals coming back from the unit under test (UUT) are buffered by the pin electronics receiver and sent to the 8 bit A/D converter in each channel (refer to Fig. 2-5). The output of the 8 bit A/D converter is entered into a combiner where two 8 bit segments are joined into one 16 bit word. This information is strobed into a buffer so as to synchronize timing with regard to the A/D converter and local memory. The information from the buffer is then stored in local memory. Since the local memory is 2K by 16, the equivalent of 4,000 words of 8 bit storage is realized. With an 8 bit, 60 MHz A/D converter, 16 bits are available every 33 ns. Thus, the channel writes to memory at a 30 MHz rate. This is compatible with the 30 MHz rate chosen for the local memory. Using this ping-pong approach whereby two 8 bit segments from the A/D are combined into a single 16 bit word, the channel can use a much slower memory than would ordinarily be required.

A 16 bit A/D converter can be utilized for selective, high-resolution measurements. One can be implemented on each 8 channel UPE board. One or more local memory on the board is also utilized for this A/D converter. Since the 16 bit A/D is a slower device (i.e. 50 KHz) it is able to write directly to the 30 MHz memory.

This measurement architecture eliminates many problems associated with triggering. It is common to lose part or all of a signal due to the setting of a trigger level. Here conversion is continuous and the "snapshot" is taken only when the desired



ANALOG AND PARAMETRIC DIGITAL MEASUREMENT

FIGURE 2-5

waveform is centered in the memory.

The last two cases are the functional digital stimulus and the functional digital measurement. The descriptions to follow detail the most exhaustive test requirement in this category which deals with a real-time, bidirectional UUT pin. Here the tester must supply UUT inputs (apply data), evaluate UUT outputs (expect data), control the output impedance of the driver (bi-directional data), and cull out don't care situations (mask data). Detailed sections to follow also delineate the less demanding test situations which deal with input only or output only type UUT pins.

Two modes of data storage are employed, basic and compacted. The basic format utilizes absolute data and each 16 bit word which is read from memory is as follows:

a) Bits 1, 2, and 3 represent the applied/expected bit, the bidirectional bit, and the mask bit necessary for functional testing.

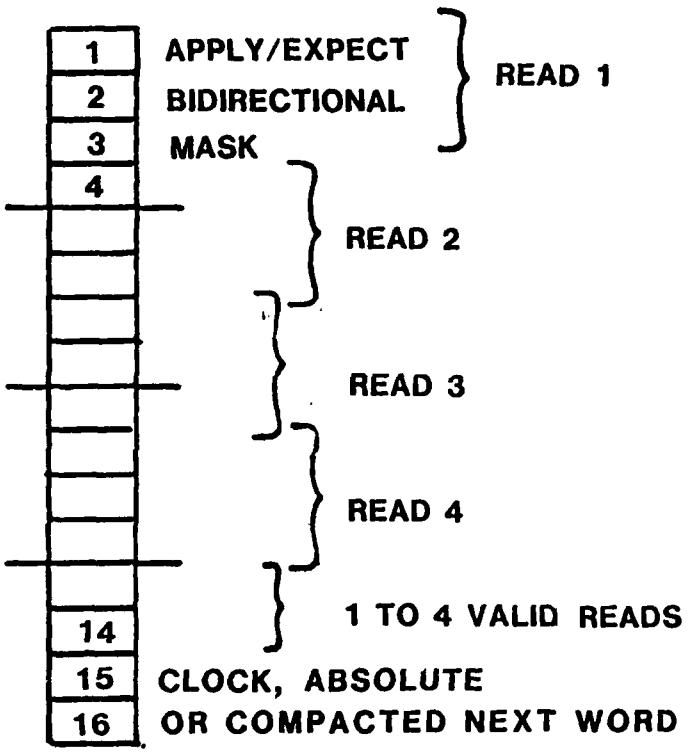
b) Bits 4, 5, and 6 a second 3 bit vector,

c) Bits 7, 8, and 9 a third vector, and

d) Bits 10, 11, and 12 are the fourth such vector of this type.

Bits 13 and 14 define whether a single read, two reads, three reads, or four reads in the word are valid. Bits 15 and 16 define whether or not there is a clock definition in the next word, whether or not the next word is in an absolute format, or whether it is in one of the two compacted forms (refer to Figure 2-6).

Prior to the initiation of testing, several words are accessed from memory. This essentially allows the structure to



BASIC WORD FORMAT
(BUS TYPE UUT PIN)

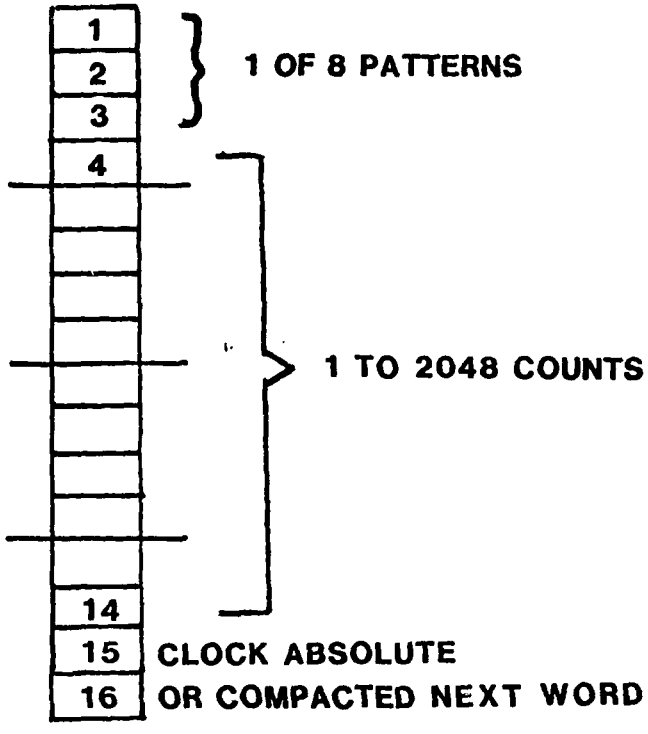
FIGURE 2-6

assume a look-ahead type architecture. This is equivalent to performing the decoding function of these words ahead of time in order to maintain maximum operating frequency.

In the absolute form, the first 12 bits of the 16 bit basic word read from memory define four vectors of three bits each. The three bits are the combined apply/expect bit, the bidirectional bit, and the mask bit. Thus, for each memory access four vectors in absolute form are defined. Since the memory repetition rate is 30 MHz, the channel is effectively providing a factor of four multiplication so that rates of up to 120 MHz are possible. This is in excess of the 100 MHz rate which is set as the maximum operating frequency of the pin electronics.

In the compacted mode, coded or compacted data is utilized. For example, the first 3 bits of the 16 bit memory word might define eight patterns of compacted data (refer to Figure 2-7). The first such pattern might be all ones, the second might be all zeros, the third might be alternate ones and zeros starting with ones, the fourth mignt be alternate zeros and ones starting with zero, and so forth. Bits 4 through 14 define the maximum count for the pattern defined by the first 3 bits. Since there are 11 bits involved it is possible to define patterns up to 2048 counts. Finally the last two bits define whether or not the next word is in one of two compacted forms, whether the intent is to revert back to the basic (absolute) format, or whether a clock format is to be selected. A second compacted word format is utilized in order to optimize the entire process.

If the word is defined as being a clock/delay/APG word, the first three bits define 1 of 7 clocks or the algorithmic pattern



COMPACTED WORD FORMAT 1

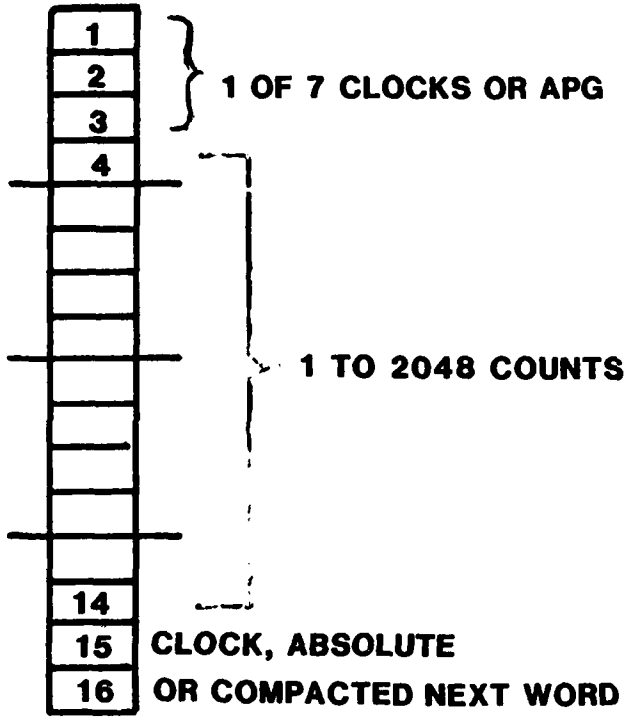
FIGURE 2-7

generator (APG). Fig. 2-8 shows how the next 11 bits allow a "pin clock" condition to be set up whereby a clock may be applied to the UUT directly through the driver for any count up to 2048. Any one of the 7 clocks may be selected under program control and applied to any channel (pin) or any number of channels.

The algorithmic pattern generation (APG) sequence is set up prior to test. Walking ones will be the first standard set in the sequence, walking zeros the second, checkerboard the third, and so on. When the APG code is read from the clock/delay/APG word, APG sequence number one is initiated. It proceeds on its own, finishes, and upon finishing generates an interrupt to return control to the next word. In other words, the APG sequence is fixed prior to test. All APG sequences proceed in the order predetermined before the start of the test. Also, each APG bit is hard-wired to a particular pin electronics channel. The interconnect between the pin electronics and the UUT determines to what pins it is applied.

It is possible to switch in real time from absolute to clocks/delays/APG, and to compacted form and back in any combination. When you enter the compacted form, pin clocks and APGs are no longer valid. When you emerge from compacted form they are legal again.

As mentioned, the local memory is 16 wide by 2K deep. This memory is filled with the apply/expect vectors, the bidirectional vectors, and the mask vectors. When in the compacted mode, the mask vectors and bidirectional vectors, since they are very predictable patterns, are compressed in a very efficient manner. Therefore, most of the local memory can be devoted to the

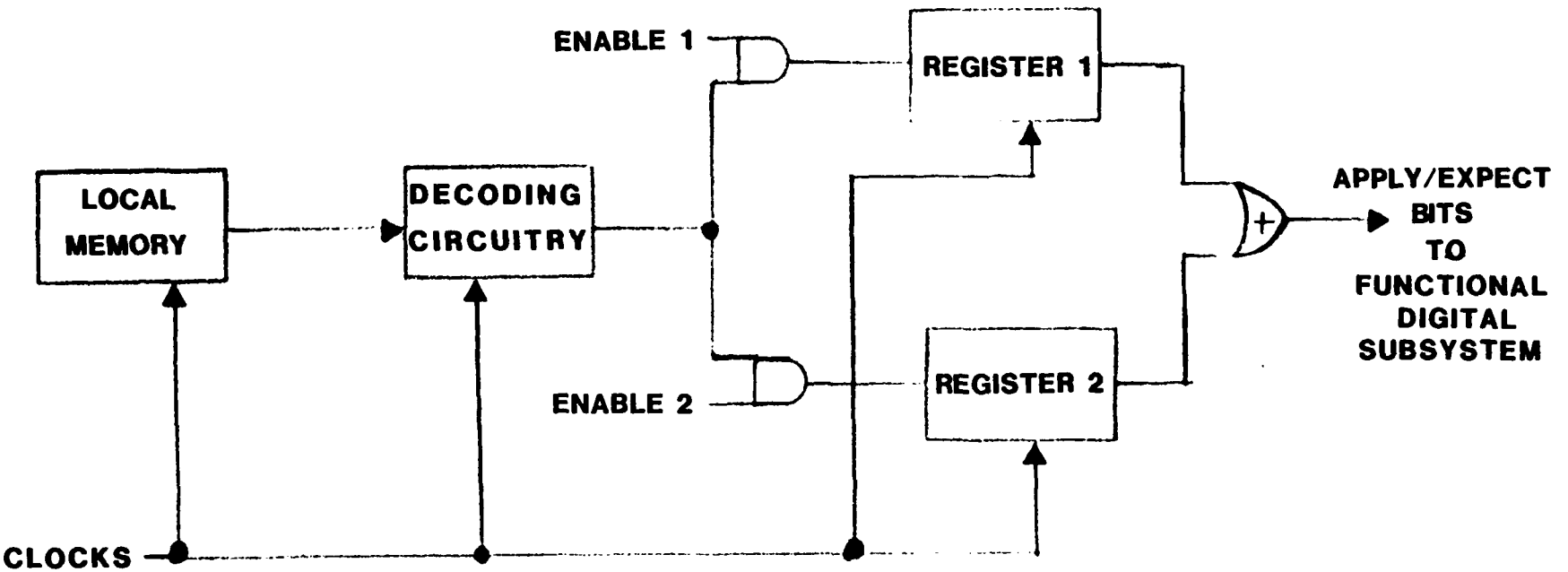


CLOCK/DELAY/APG FORMAT

FIGURE 2-8

apply/expect vectors which are more random in nature. When the data is extracted from the local memory in compacted form, it is directed to the decompaction module. The decompaction module takes the compacted data, decompacts it, and alternately strobes it into two registers (refer to Fig. 2-9). Two registers are devoted to the apply/expect pattern, two to the bidirectional pattern, and two to the mask pattern. Consider the apply/expect bit for the purposes of example. When the compacted data is decoded into absolute form by the decompaction module, it is strobed into one of the two apply/expect registers. The second word in the sequence from memory is strobed into the second such register. As soon as the first register empties as its absolute data is strobed to the UUT, it generates an interrupt telling the decompaction module to take another word from memory, decompact it, and refill the register. All of this is possible from a timing standpoint because the second apply/expect register is being utilized during this period of time. In a similar fashion the bidirectional and mask codes are decompacted. Of course, since they are much more predictable in nature, the compaction is much more efficient and the need to refresh them is less urgent. Priority interrupts define the apply/expect level as the highest, the bidirectional next highest, and the mask level as lowest. This priority is utilized because of the relative efficiency of compaction of these three different pieces of information.

The decompaction module is also an important factor in terms of increasing the maximum repetition rate. Most tester repetition rates are directly coupled to the access time of the local memory. The UPE architecture utilizes a 30 MHz local memory, 16



DECOMPACTION FLOW
APPLY/EXPECT BITS

FIGURE 2-9

bits wide by 2,048 bits deep. Each access of the memory provides 16 bits which are decoded by the decompaction module. At a 30 MHz rate, every 33 ns sixteen bits are available. At an average compaction ratio of 30 to 1, 480 bits of information are decoded every memory access cycle. The maximum repetition rate of the universal pin electronics is 100 MHz. At 100 MHz, 3 bits are required every 10 ns (the apply/expect bit, the bidirectional bit, and the mask bit). With the decompaction module, every 10 ns approximately 145 bits are available. Thus, if it is desired to operate at the maximum repetition rate of 100 MHz, a 48 to 1 factor of safety is provided. The factor of safety is even larger if the UUT pin does not require all 3 bits (bus type). However, worst case dictates 3 bits must be accessed from the same memory, the apply/expect, the bidirectional and the mask bits. Since the compaction is so efficient for the latter two bits (they are much less random) a factor of more than 30 to 1 is likely. Therefore memory will have to be accessed much less frequently. At an average compaction factor of 30 to 1, over 960,000 bits can be compacted into a 2K by 16 memory. If the assumption is made that the apply/expect, bidirectional, and mask take up equal amounts, over 300,000 bits of information are possible. A more realistic case would have the apply/expect equivalent depth of over 500,000 vectors since the bidirectional and mask bits are so predictable and therefore so compactible.

It is evident the decompaction module has a positive effect on the repetition rate of the pin electronics and on the compaction of vectors. A 32K memory can house on an average of 960,000 bits of information so that the UPE is able to run at the

programmed frequency for virtually unlimited periods of time. The same technique also helps free the maximum repetition rate from the access time of the memory which is the normal case in today's digital testers. In essence, the memory speed is multiplied by an average of 30 times insofar as test rates are concerned. Even though memory is accessed at 16 bits every 33 ns, the 16 bits represent a much larger amount of data. After being decompacted this data allows the driver and receiver of the pin electronics to operate at rates far in excess of 30 MHz because of the fact that so much additional data is available before memory must be accessed for the next cycle.

Another advantage gained by the use of the decompaction module is the dramatic increase in overall test throughput. A significant amount of time is normally taken just to transfer the large amounts of array or vector data from the test system bulk storage medium (e.g. disk) to the pin electronics via the system I/O. This time is much larger than the actual test time in many cases. The use of the decompaction module will decrease this transfer time drastically since the data is expressed in coded form.

It must be emphasized that the capabilities described in this document may be visualized as being the maximum test capability to be implemented. In any specific instance a subset of the described capability might be much more appropriate. For example, consider a hypothetical 200 pin tester. Based on a thorough workload analysis, it might be desirable to implement perhaps only 30 universal channels, 150 functional digital channels, and 20 analog/parametric digital only channels. Connections

between the universal pin electronics and the UUT would be effected via a passive interface to direct specific capabilities in an appropriate manner.

As a matter of practicality, specific subsets of the described capability might be the most practical implementation for a given test situation. The various advantages described herein would still be in effect and an easier design and build cycle might be realized. For example, the calibration capability might be eliminated in order to save time and dollars. Thus, the full capabilities and features described herein should be looked upon as being an ultimate design.

Despite the broad capability of the UPE, there will be test situations where specialized stimulus or measurement capability might be required. As the testing envelope encompassed by the UPE progresses over the years the requirement for external equipment will decrease but initially some external capability will likely be required in certain test situations.

2.2 OVERALL SYSTEM SPECIFICATION

General

Maximum Functional Digital Repetition Frequency	100 MHz
Maximum Parametric Digital Stimulus/Measurement Rate	20 MHz
Maximum Analog Stimulus/Measurement Rate	20 MHz
Maximum Pin Count Per Chassis	256 channels, 512 UUT pins
Driver Output Ranges	+-10 V, + - 1 V
Receiver Input Ranges	+-10 V, + - 1 V
Driver Output Resistance	1 OHM or 50 OHMs

Receiver Input Resistance	1 MEGOHM MIN.
Receiver Input Capacitance	10 pF MAX.
Crosstalk Between Pins	60 dB MIN.
Receiver Input Voltage Protection	+-20 V
Driver Source/Sink Current	+-50 ma
Functional Digital	
Maximum Driver/Receiver Skew	+-1 ns
Driver Slew Rate	1 v/ns
Minimum Vector Depth (standard)	20 K (8K tri-state)
Minimum Vector Depth (compacted)	250 K
Minimum Driver Tristate Impedance	100 K OHMs
Simultaneous Logic Families	Unlimited
Driver Output Range	+ - 10 V
Driver Accuracy	1%
Driver Resolution	80 mV
Driver Overshoot	10% no load
Receiver Input Range	+ - 10 V
Receiver Accuracy	1%
Receiver Resolution	80 mV
Receiver Input Levels (standard)	2
Receiver Input Levels (optional)	4
Pull-up Load Resistor	One per channel
Pull-down Load Resistor	One per channel
Number of Clock/delays	7
Number of Clock/delay Edges	14
Clock/delay Range	1 Hz to 100 MHz
Clock/delay Strobe Resolution	0.5 ns
Clock Modes	Asynchronous, synchronous to

	other clocks &/or to UUT, or external
Algorithmic Patterns	Walking one, Walking zero, checkerboard, inverted checkerboard
Analog/Parametric Digital	
Time Resolution	1 part in 4096 Max.
Sampling Rate	60 MHz Max.
Waveform Stimulus Types	Sine, square, pulse train, triangle, ramp
Stimulus Ranges	+-10 V, + - 1 V
Stimulus Accuracy	1%
Stimulus Resolution	80 mV, 8 mV
Waveform Measurement Parameters	Risetime, falltime, pulse-width, dc voltage, peak voltage, RMS voltage, frequency, period, delay, phase shift, events
Measurement Range	+ - 10V, + - 1 V per channel (+ - 50V, + - 100V, + - 200V per group, 16 bit resolution)
Measurement Accuracy	1%
Measurement Resolution	80 mV, 10V range; 8 mV, 1 V range (16 bit resolution on higher ranges)

Note

UPE architecture puts complete test cpability into every channel. Therefore, with the exception of clock/delay/APG and

high resolution data, all specifications apply to each UPE channel.

Environmental

The unit shall meet the environmental requirements of MIL-T-28800, Class 4 equipment, Style F except as modified below.

Temperature Range

Operating

The operating temperature range shall be 10 degrees C to 50 degrees C.

Nonoperating

The non-operating temperature range shall be -40 degrees C to 70 degrees C.

Relative Humidity

Operating

The operating relative humidity profile shall be:

a. from 3% to 95% (+5 -0), with no condensation, to 27 degrees C
b. from 8% to 74% at 35 degrees C
c. from 3% to 25% at 45 degrees C
d. from 3% to 20% at 50 degrees C
e. from 3% to 10% at 60 degrees C

Non Operating

The non-operating relative humidity profile shall be:

a. 100% with condensation, to 24 degrees C to
b. 75% at 35 degrees C decreasing to
c. 30% at 50 degrees C decreasing to
d. 10% at 75 degrees C

Units may be conditioned, prior to normal operation, by

removal of excess moisture and a drying out period after being subjected to conditions of condensation.

Altitude

Operating to 15,000 feet, non-operating to 40,000 feet.

Vibration

Operating, not applicable. Non-operating vibration shall be in accordance with MIL-STD-810, method 514.2, Equipment Category G, Procedure X, as follows: 2G at 5Hz and increasing to 5G at 12Hz, decreasing to 2G at 50Hz and remaining at 2G to 200Hz.

Shock

The non-operating shock requirements shall be half-sine 30g shock pulse in accordance with MIL-STD-810, Method 516.2, Procedure I, Figure 516.2-2.

Fungus-Inert Materials

Fungus-inert materials shall be used in accordance with MIL-STD-454, Requirement 4.

SECTION III

3. I/O INTERFACE

3.1 FUNCTIONAL DESCRIPTION

The I/O Interface is used to make the UPE compatible with the IEEE-488 bus which is the link to the main controller. Under control of the backplane microcontroller, this interface effects data flow between the UPE (boards and backplane) and the main controller. Any buffering necessary to eliminate local timing problems is provided in this subsystem.

Referring to the block diagram of Figure 3-1, the signal conditioner provides the electrical and mechanical compatibility with the IEEE bus. The buffer provides any temporary storage necessary to synchronize data flow between the UPE and the main controller. Timing problems are thus avoided.

Examples of data directed to the UPE local memory include:

a) Absolute data (apply, expect, bidirectional control, mask) for functional digital testing

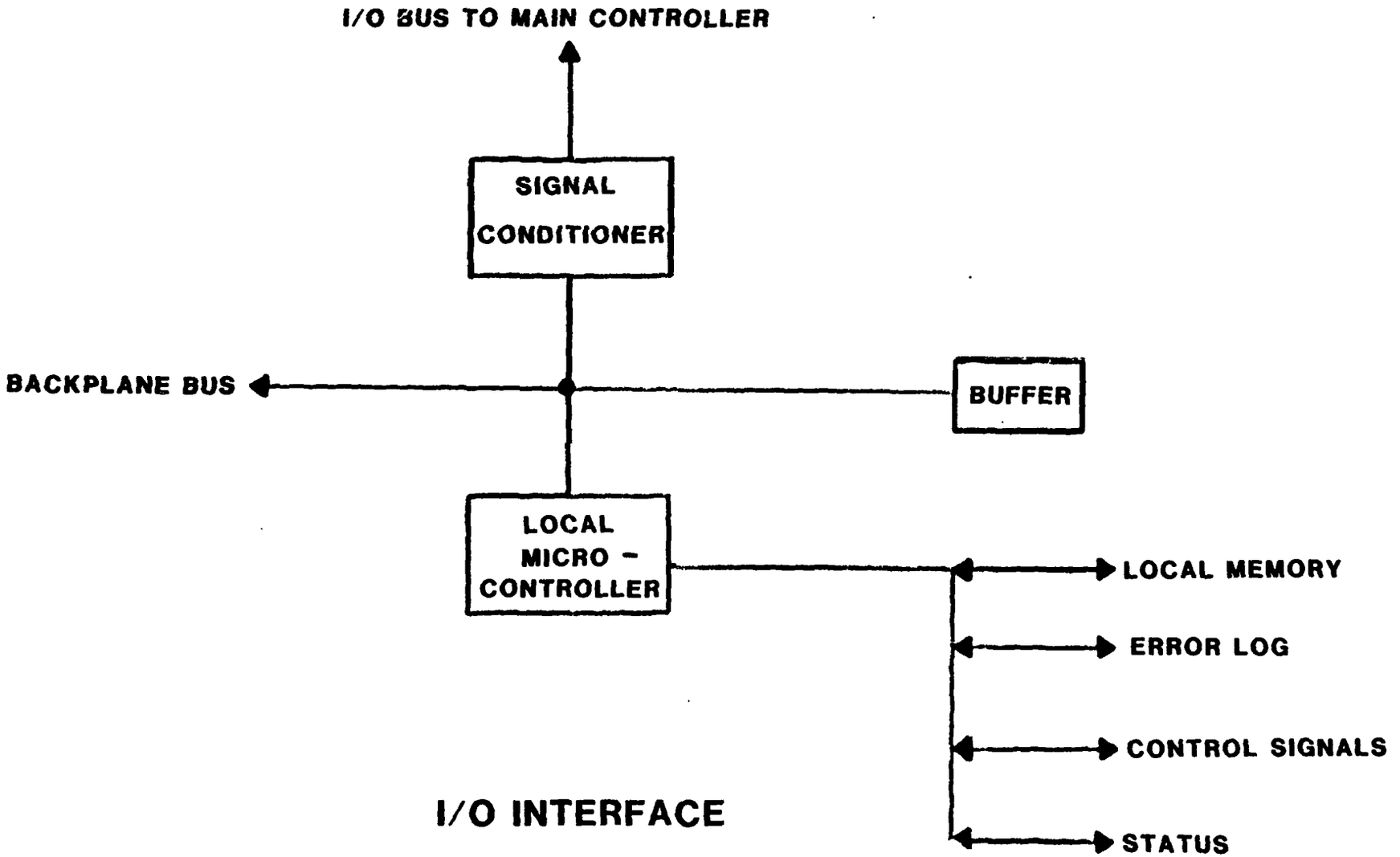
b) Compacted data for functional digital testing

c) Descriptions of analog and parametric digital stimuli to be generated by the local microcontroller from basic algorithms stored in ROM (significant preliminary analysis and setup is performed by the backplane microcontroller; refer to Section 12 for more detail)

d) Clock/delay/APG set-up data

Examples of data output from the UPE include:

a) Results of partial analog and parametric digital signal



I/O INTERFACE

FIGURE 3-1

analysis performed by the local microcontroller via analysis algorithms stored in ROM; final analysis is effected in the backplane.

b) Functional digital test results from the error log

c) Guided probe or fault signature diagnostic data from the error log

d) Results of APG testing

e) Status data (e.g. self-test, on-line confidence, etc.)

Due to the large amount of data transmitted across the IEEE interface to the universal pin electronics, the time it takes to transmit and receive data across the interface directly affects the throughput of a given UUT test. While the IEEE bus can theoretically support a data rate of 1 megabyte per second, a practical limit of 500 kilobytes per second more realistically represents the capabilities of the main controller to interact with the DMA bus of the UPE backplane microcontroller via the controller interface.

A sample analysis may place the transfer time in proper perspective. The digital array data is transmitted via the IEEE bus in block form. The overhead time to set up the pins to their proper mode, to set up the clocks, D/As, etc. are ignored in this analysis since the required number of bytes to set up the pin modes is a relatively small amount. For this sample analysis, a typical UUT will be defined as having 232 pins. For the UUT 80 pins are defined as inputs, 120 pins are defined as outputs and 32 as bus pins. A test pattern depth of 8K will be used as the vector size in the analysis.

The UUT requires 4 pattern arrays to run the test. These are

a driver array which is sized at 80 lines by 8K bits, a sensor array which is sized at 120 lines by 8K bits, a mask array which is sized at 120 lines by 8K bits, and a bus array sized at 32 lines by 8K bits by 3 (apply/expect, bi-directional, and mask). Since the error log information is processed in the UPE circuitry, error log data size is very small and will be ignored.

For the byte oriented IEEE interface the driver array is sized at 80 kilobytes, the receive and mask array at 120 kilobytes each, and the tri-state at 96 kilobytes. The total data to be transmitted is calculated to be 416 kilobytes. At a data rate of 500 kB per second, the time for transmission of the data across the IEEE is calculated to be approximately 0.8 seconds.

It is seen that the total time to transmit data for a 232 pin UUT with 8K pattern depth is less than 1 second. This is an acceptable transmission time which insures a respectable throughput in the test. If, however, the pattern depth approaches 50 kB to 250 kB, transmission time in the 5 to 30 second range would be seen unless the data compaction technique is used. The technique of data compaction assures that the total transmission time across conventional IEEE bus technology can be kept less than 1 second even for very large digital test patterns.

3.2 I/O INTERFACE SPECIFICATION

System Interface	Compatible with IEEE std. 488-1978 (488 compatible cable to be included)
Transfer Rate	0 to 500K bytes per second
Bus Address	Program Controllable
Power Supply Voltage	See Note 1

Internal Interface	See Note 1
Operating Temperature Range	See Note 2
Maximum Power Dissipation	See Note 2

Note 1

Power Supply voltage and internal interface levels, fan-out capability, etc. must be consistent with overall system design

Note 2

Operating temperature range and maximum power dissipation must be such that the overall environmental specification of Section 2 is achieved.

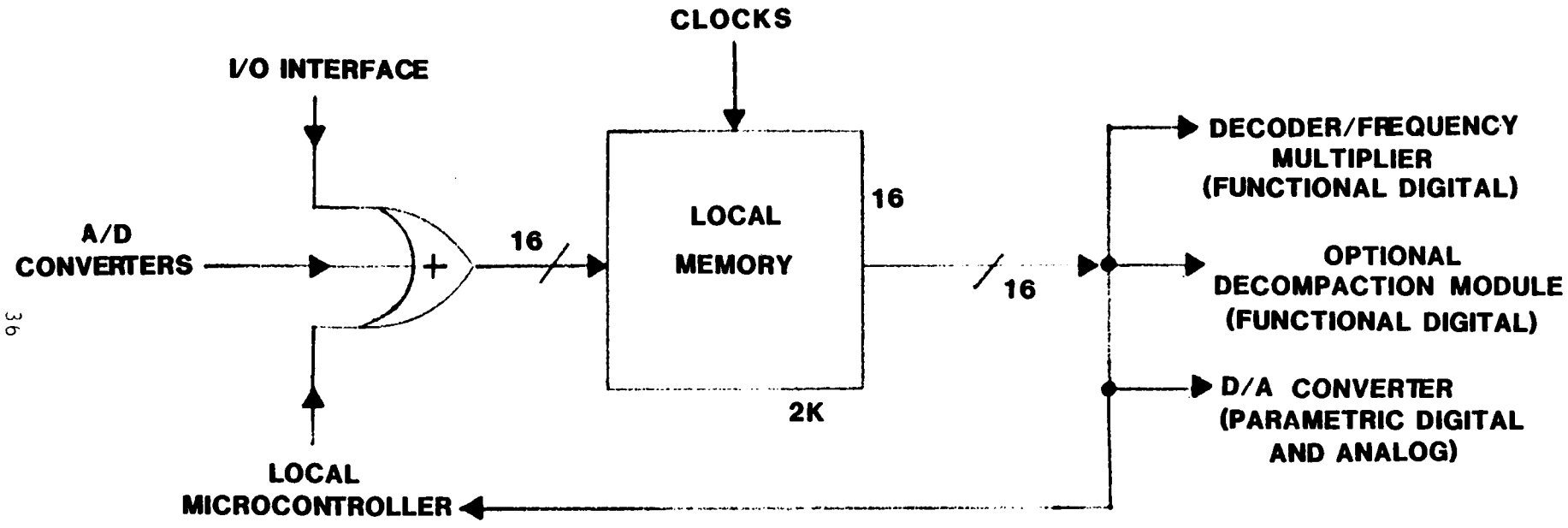
SECTION IV

4.0 LOCAL MEMORY

4.1 FUNCTIONAL DESCRIPTION

The local memory in each pin electronics channel is used for a number of different purposes. When the channel is in the basic functional digital testing mode, the memory is filled prior to testing with the absolute data for functional testing including as a maximum the apply/expect bit, the bidirectional bit, and the mask bit. Its data also describes the use of clocks in the pin clock mode and controls application of the algorithmic pattern generator (refer to Section 10). If the optional decompaction module is utilized for functional digital testing the memory stores coded or compacted data for use in this mode. In the analog and parametric digital stimulus modes, it contains the patterns that will be directed to the D/A converter which will convert them to actual waveforms for application to the UUT. In the analog and parametric digital measurement modes, the local memory will be filled during testing with digitized equivalents of outputs from the UUT. These digital equivalents will then be sent to the UPE microcontrollers which will analyze them and extract the parameters called for by the test program.

The local memory is depicted in the block diagram of Figure 4-1. Data can be entered directly from the main controller via the I/O interface (e.g. absolute data for functional digital testing), from the 8 or 16 bit A/D converter (e.g. digitized UUT output data), or from the local microcontroller (e.g. digitized analog stimulus). The output of the memory is directed to the



LOCAL MEMORY
FIGURE 4-1

decoder/frequency multiplier (absolute functional digital data), the decompaction module (compacted functional digital data), the D/A converter (analog or parametric digital stimulus), or the local microcontroller.

The proposed size for the local memory is 2K bits by 16. The proposed access time is 30 MHz. Current memory technology should easily allow 32K bits total at a 30 MHz rate. This is not stressing the state of the art in any manner. Even normal digital test subsystems use up to 20K bits per pin at present. Today's single memory chips easily exceed 64K bits. Therefore the design is well within reason from the standpoint of the current state of memory technology and even with regard to the amount of memory normally used by a 1982 style digital test system.

4.2 LOCAL MEMORY SPECIFICATION

Organization	
Words	2 K minimum
Bits per word	16
Maximum Access Time	33 ns
Maximum Write Cycle Time	33 ns
Parity	Not required
Power Supply Voltage	Note 1
I/O Levels	"
Mode	"
Technology	"
Operating Temperature Range	"
Operating Power Dissipation	"
Physical Dimensions	"

Note 1

Input/output (I/O) levels should be compatible with other elements in the channel. This and many other important memory characteristics cannot be determined in an optimal fashion until detailed design work is initiated. The mode selected (dynamic, static) and actual technology are best determined during the design phase ther parameters such as operating temperature range, .i..g power dissipation, and physical dimensions are also best selected during this phase. They should be optimized so as to meet the overall environmental and operating requirements for the pin electronics. For example, the actual design configuration will have a profound effect on the memory operating temperature range. The memory has to coexist with other tightly packaged heat producing components so that the entire UPE channel will be operable within its required temperture envelope. When a channel is not in use, the local memory should be placed in a deselect state so as to minimize power dissipation.

SECTION V

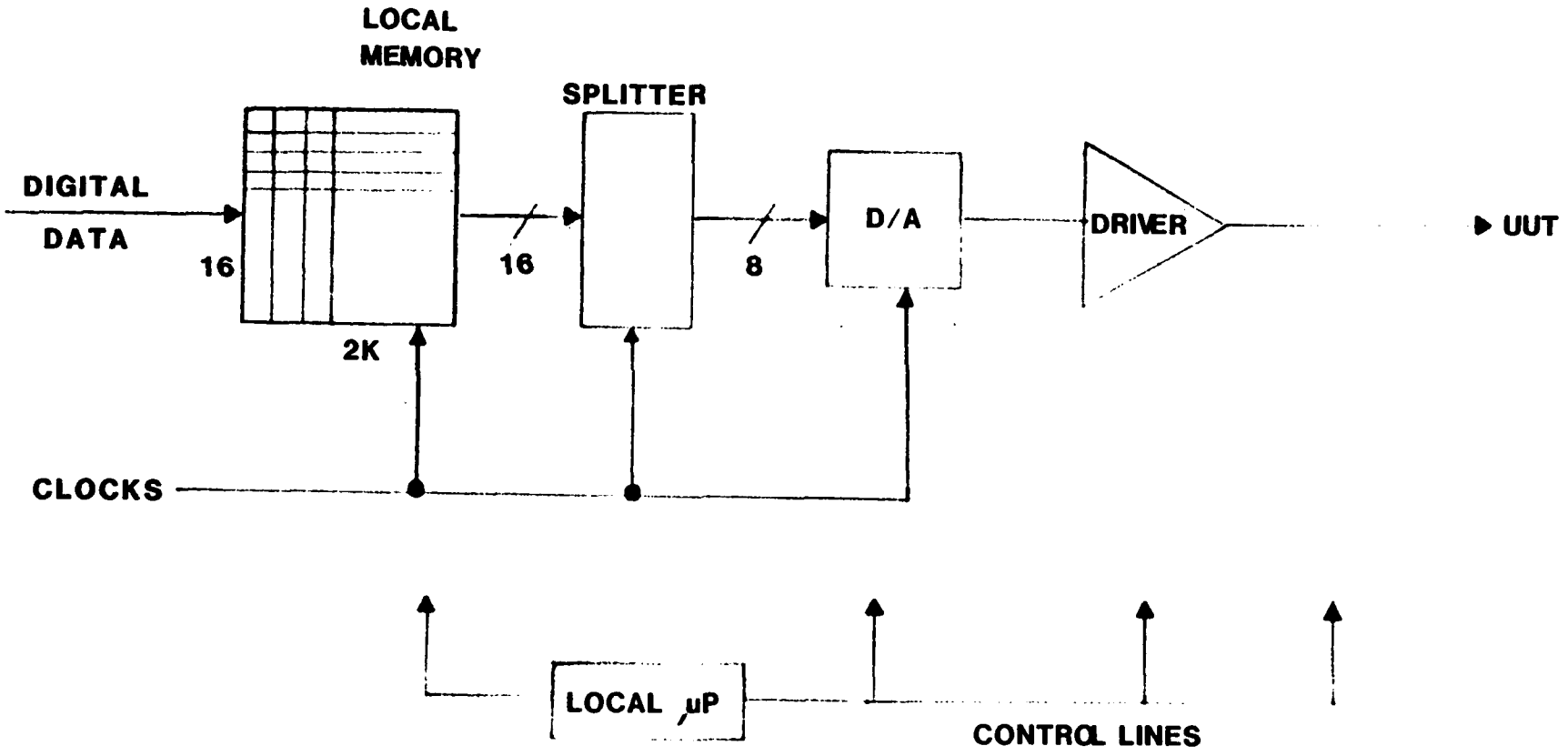
5.0 D/A CONVERTER AND LOGIC LEVEL GENERATOR

5.1 FUNCTIONAL DESCRIPTION

Each universal pin electronics channel has the inherent capability to generate virtually any analog or parametric digital stimulus, whether it be periodic or aperiodic. The reason for this is that the digital equivalent of these signals is stored in local memory in virtually any sequence. A standard pattern such as a sine wave, a square wave, etc., is generated by the backplane and local microcontrollers from algorithms stored in board and backplane ROM. Relatively simple algorithms are used to generate the patterns which are then stored in the local memory. Assume the test program calls for the application to the UUT of a 10 volt peak to peak, 5 KHz sine wave. The program is analyzed and the request generated by the main controller. The response is effected by the backplane and local microcontrollers in the pin electronics. The digital equivalent of that analog waveform is generated and entered into local memory.

In its initial configuration, the universal pin electronics will have the ability to generate sine waves, square waves, triangle waves, ramps, or random pulse trains of ones and zeros. In the future more complex algorithms can be developed to generate additional waveform types.

As can be seen from the analog, parametric digital signal flow diagram of Fig. 5-1, digital information is transferred under control of the microcontroller to the local memory. There are 8 channels per UPE board and one microcontroller per board.



ANALOG, PARAMETRIC DIGITAL SIGNAL FLOW
FIGURE 5-1

The digital equivalents of complete waveforms are stored. A 16 bit word is read from memory and divided into two 8 bit words in the splitter. This technique effectively multiplies the frequency of the signal. The actual waveform is then generated by the 8 bit D/A converter. The output from the D/A is directed to the driver for application to the UUT.

Factors such as the D/A converter sampling rate, the programmed clock frequency and the number of 6 bit digital vectors utilized all are important factors in generating the analog or parametric digital waveform. The more samples utilized the higher quality the waveform but the waveform frequency upper limit is constrained by the clock frequency. A more accurate picture of the clock frequency constraint is attained by considering the rate at which the local memory may be sampled as the governing factor. The UPE architecture is structured to allow higher frequency waveforms to be generated as technology improvements advance the state of the art in D/A converters and local memory elements. For high quality, lower frequency waveforms, selective high resolution D/A converters may be considered for use. Two ranges are used at present but additional ranges might be considered for selective stimuli generation over a wider voltage range.

The use of appropriate filters is implied in the D/A converter block. Especially as higher frequency waveforms are generated filters must be utilized to improve waveform quality (i.e. reduce distortion) as the number of digital vectors is reduced. The sample size and filter selection are automatically accomplished by the local microcontroller. The upper effective clock

frequency is 60 MHz since two 8 bit words can be accessed at the maximum 30 MHz local memory rate. Without even the necessity for filters the waveform distortion should be in the 1% range up to approximately 500 KHz. By the appropriate filter and sample size selection a distortion of 1% should be attainable up to approximately 5 MHz. At 20 MHz even the best filters should not allow a distortion too much better than 10 to 12%. As mentioned, however, technology advancements in memory and D/A elements will allow improvements to be easily incorporated into the UPE architecture.

The logic level generator is an important part of this subsystem. Today many test systems have fixed I/O levels for functional digital testing. Yet units under test with multiple logic families such as ECL, TTL, MOS, etc. are increasingly common. Without the ability to provide programmable levels, in many cases the tester is not able to conduct an adequate test on the UUT. Even in those testers which do have programmable logic levels, many are restricted to one family or perhaps two families of different UUT logic as a maximum.

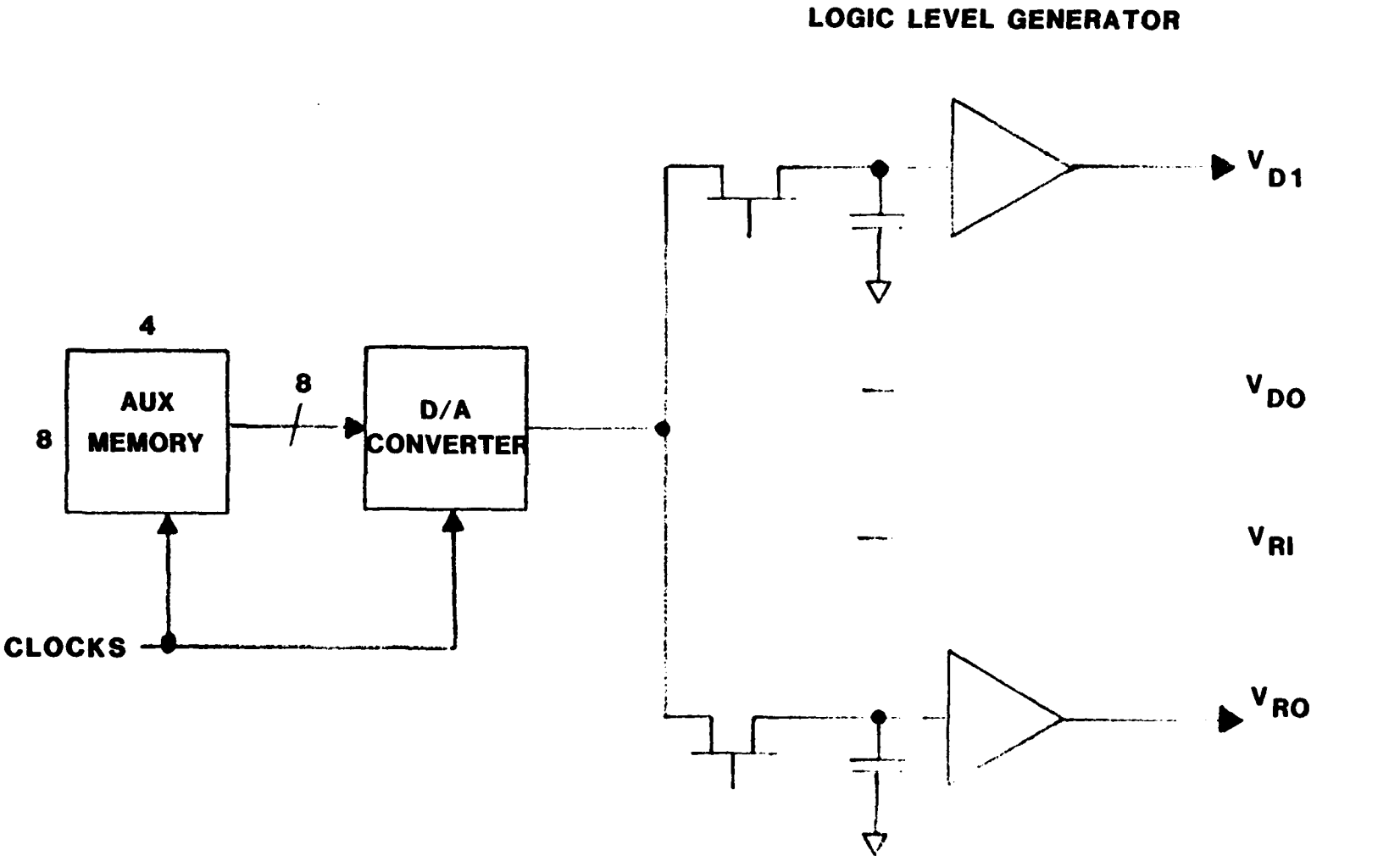
A typical approach in today's testers is to program large programmable power supplies for each of the different levels that are desired and switch these voltages to the various channels via some sort of a switching system. Because large programmable power supplies and significant switching is utilized, the approach is generally expensive and often unreliable.

The universal pin electronics channel provides an answer in a much more reliable and yet extremely effective approach. There is already a D/A converter in every channel of UPE. A small amount of additional memory is utilized (refer to the logic level

generator block diagram of Fig. 5-2). The auxiliary memory is a 4 by 8 configuration. Words of 8 bits are strobed out of the memory into the D/A converter. The D/A converter is not being used for parametric digital or analog testing when the UPE channel is performing functional digital testing. Therefore, it is available for this purpose. The 8 bits are converted by the D/A converter into a voltage level and strobed via a multiplexer into a buffer amplifier. Sufficient buffers are utilized in order to provide the logic levels necessary for functional digital test. Four levels are provided as a minimum: the logic one level for the driver (VD1), the logic zero level for the driver (VD0), the logic one level for the receiver (VR1), and the logic zero level for the receiver (VR0). As an option, two additional levels could be provided if so desired so as to place a window of two levels around the receiver logic one and a window of two levels aroung the receive logic zero. These two additional levels would be referred to as VR11 and VR00.

The subsystem's multiplexer switches the low output impedance D/A into each buffer in turn. The capacitor is rapidly charged. When the mux reverts to its high impedance state the capacitor discharges slowly because both the mux and the buffer are high impedance. The accuracy of the levels is determined in part by the cycle time of the multiplexer. The buffer must hold the level to a sufficient degree until refreshed on the subsequent cycle.

With the described approach universal programmability is realized on every pin. Therefore, the UPE can effectively test UUT with various families of logic and also do worse case testing



UNIVERSAL LOGIC LEVEL GENERATOR
FIGURE 5-2

by varying logic levels throughout their tolerance band. The amount of circuitry necessary in each channel to accomplish this universality is very small. All that is needed is the small 4 by 8 memory and the buffer amplifiers and multiplex switching that is shown in the logic level generator block diagram. The circuitry that is used is all solid state and is therefore extremely reliable.

5.2 D/A CONVERTER AND LOGIC LEVEL GENERATOR SPECIFICATION

D/A Converter

Input Format	8 bits
Input Levels	Note 1
Output Voltage Range	Note 2
Output Current	Note 2
Output Voltage Accuracy	Note 2
Maximum Settling Time	16.67 ns
Maximum Power Dissipation	Note 3
Operating Temperature Range	Note 3
Power Supply	Note 1

Logic Level Generator

Input Format	Four 8 bit words (VD1, VD0, VR1, VR0)
Optional Input Format	Above plus 2 additional 8 bit words (VR11, VR00)
Output Format	Analog voltage +-10 V for each of VD1, VD0, VR1, VR0
Optional Output Format	Above plus analog voltage +-10 V for each of VR11 and VR00
Output Voltage Accuracy	Note 2
Output Voltage Resolution	80 mV

Multiplexer Sampling Rate	Commensurate with output voltage requirement

Note 1

Input levels and power supply voltage(s) should be compatible with the overall system design.

Note 2

Output voltage ranges, accuracy, and current should be such that the system specification of Section 2.2 is met.

Note 3

Maximum power dissipation and operating temperature range must be chosen so that when the overall design is complete the UPE meets the environmental specification of Section 2.2.

SECTION VI

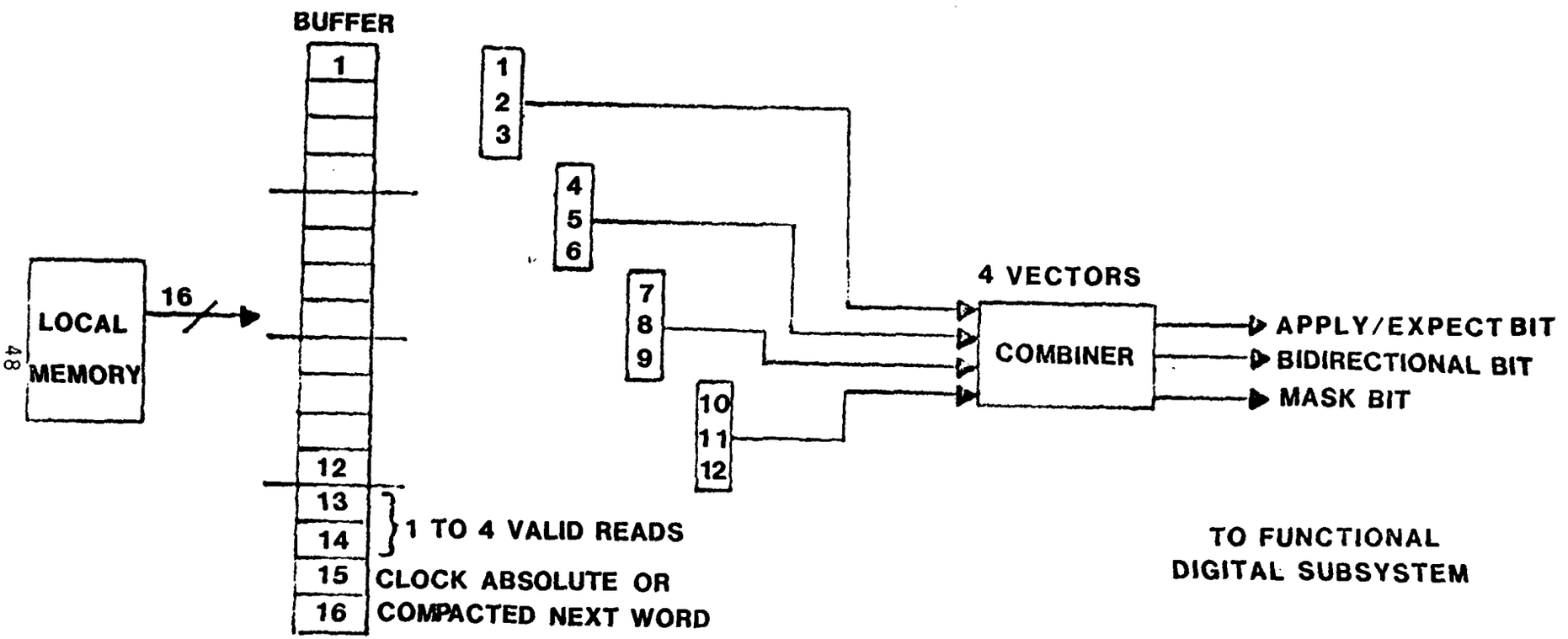
6.0 DECODER/FREQUENCY MULTIPLIER

6.1 FUNCTIONAL DESCRIPTION

The decoder/frequency multiplier subsystem is depicted in Figure 6-1. The 16 bit word is strobed from local memory into a buffer register. Consider the case where the particular channel must supply apply/expect bits, bidirectional bits, and mask bits to the UUT pin. In this case the first 12 bits stored in the buffer represent four 3 bit vectors. These four vectors are grouped together in a combiner unit. Thus, in the combiner are four vectors, each containing an apply/expect bit, a bidirectional bit, and a mask bit. These vectors are then applied to the functional digital subsystem.

One word is received from the local memory every 33 ns. Since four apply/expect, bidirectional, and mask vectors can be extracted from each 16 bit word, a frequency multiplication of four is achieved. Thus, the maximum repetition rate is multiplied by four. In this configuration the maximum vector depth without reloading from the main controller is 2,000 times 4 or a total of 8,000.

Bits 13 and 14 define whether or not one, two, three, or four words are to be extracted from the first 12 bits of the 16 bit word. Bits 15 and 16 define whether or not the next word from memory is absolute data, a clock word, or one of the two compacted words. Thus, if only two valid words are contained in the buffer, bits 13 and 14 will cause a skip to the next word where additional absolute data, a clock or compacted word will be



DECODER/FREQUENCY MULTIPLIER

FIGURE 6-1

found. With the effective frequency multiplication of four times, the local memory's 30 MHz rate is more than sufficient to meet the universal pin electronics repetition rate of 100 MHz.

The previous paragraph describes the worst case where a UUT pin requires the apply/expect, bidirectional, and mask bits. There are many cases where all three bits are not necessary for a given channel. Consider the case where only the apply or expected bit is required. In this situation, the first 10 bits of the word strobed from local memory into the buffer will all contain either applied or expected bits. When the combiner strobes this information to the driver or receiver, all 10 bits will be utilized as either applied or expected data. This will be predetermined prior to test, via an automatic software analysis of the test program. If the 10 bit apply/expect word format is utilized, even greater storage is realized. Ten bits times 2K words deep dictates 20K bits of storage per channel. The frequency multiplication factor of safety is even greater, since 10 bits are accessed from memory at a 30 MHz rate and 100 MHz is still the maximum operating channel rate. Refer to Section 6.2 for the specification of the output formats.

In conclusion, the decoder/frequency multiplier is used only where absolute data is being utilized. It is valid to switch from absolute data to compacted form or to the clock/delay/APG form in any combination. Refer to Section 7 for discussion on the optional decompaction module, and to Section 10 for discussion of the clocks/delays/APG.

6.2 DECODER/FREQUENCY MULTIPLIER SPECIFICATION

Input Word — 16 bits from Local Memory

Output Format

	TRISTATE OUTPUT	INPUT OR OUTPUT	INPUT AND OUTPUT
BIT 1	A/E	AorE	A
2	B	"	E
3	M	"	M*
4	A/E	"	A
5	B	"	E
6	M	"	M*
7	A/E	"	A
8	B	"	E
9	M	"	M*
10	A/E	"	A
11	B	VR	E
12	M	VR	M*
13	VR	VR	VR
14	VR	VR	VR
15	*1	*1	*1
16	*1	*1	*1

VR: Valid Reads
* Optional
*1 Clock, absolute or compacted next word

Maximum Input Rate	30 MHz
Maximum Output Rate	100 MHz
Logic Levels	System Compatible

SECTION VII

7.0 DECOMPACTION MODULE

7.1 FUNCTIONAL DESCRIPTION

Most of today's ATE digital subsystems are a maximum of 4,096 bits deep per channel. Most have a single memory element per channel (apply or expect pattern) although some of the more modern have two. Many of today's test programs run up to 30,000 vectors in order to achieve reasonable fault coverage. Estimates for the near term range up to 250,000 vectors, especially when the impact of VLSI and VHSIC is considered. Thus, real-time testing is impossible since large time gaps are required to refill local memory from the main frame. In short, at the present time valid testing results are in jeopardy and the problem is rapidly becoming worse.

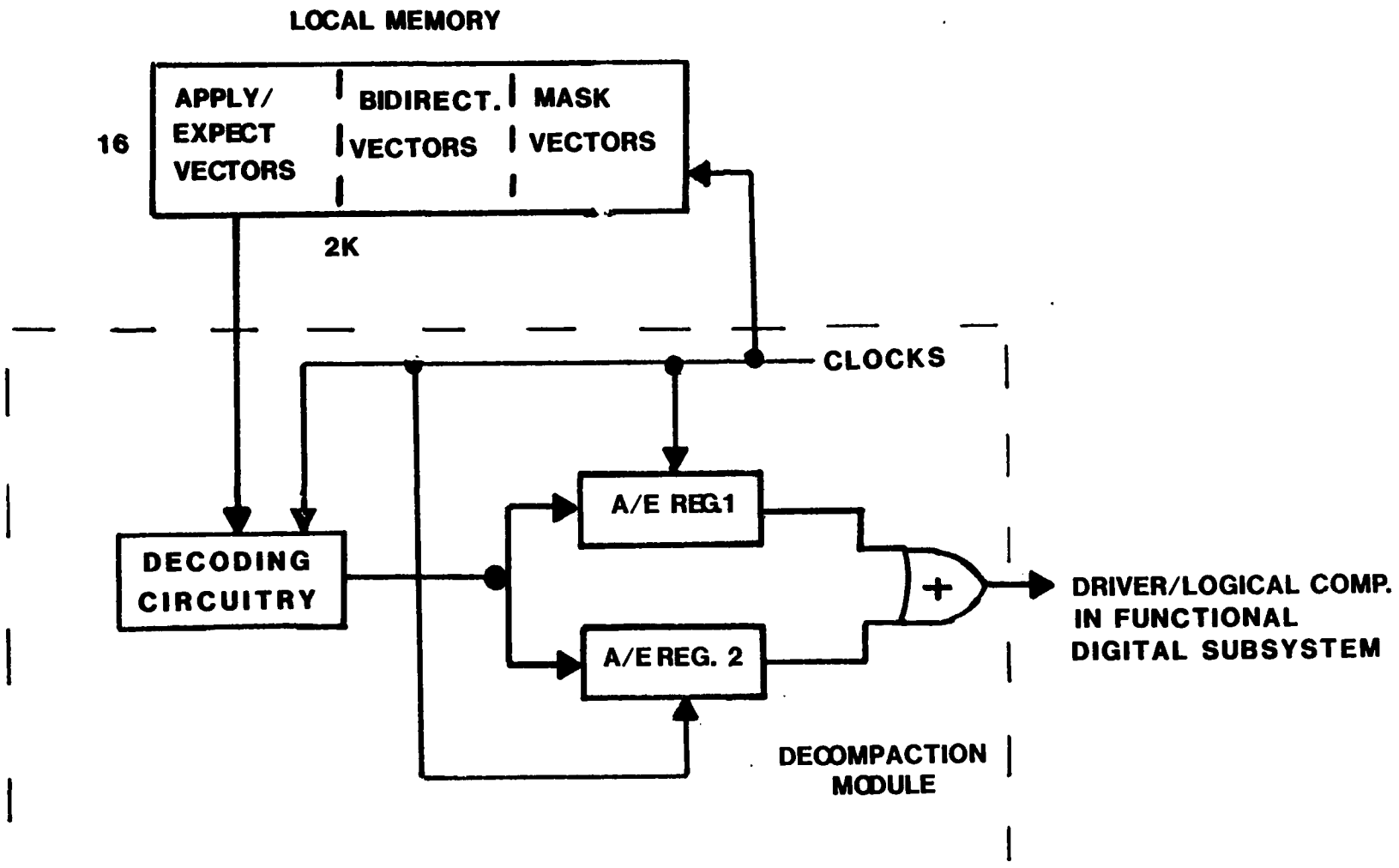
The simple solution of merely inserting local memory with depths to 250,000 bits per channel is prohibitively expensive. For real-time bidirectional driver control and real-time masking of receivers, a realistic requirement for today's typical bus-type LSI populated UUT, two additional memory elements are required per channel. This greatly amplifies the problem since a simplistic architecture would require 750,000 bits of memory per channel.

Another design constraint which tends to limit maximum test rates is the access time of the local memory utilized. Today's testers peak at 20 MHz where 100 MHz is vitally needed for valid test results. Tester architecture ties repetition rate directly to memory access time. A technologically innovative approach is

necessary to effectively increase array storage and increase repetition rates.

The decompaction module solves both problems. It is based upon the fact that at each point in time there are relatively few level changes on the pins across the UUT interface. There is a high probability that a pin will not change states for sequences of 8, 16 or more test steps. Also, there is a high probability that specific sequences of ones and zeros will exist for many bit times. Software algorithms are used to compact arrays by an average factor of 30/1. This compacted data is stored in local memory prior to testing. In real-time as the test progresses, the compacted data is read from memory and entered into the decompaction module. This module decompacts the data in real-time into absolute form for test purposes. As can be seen from the block diagram of Figure 7-1, the absolute output of the module is entered in a ping-pong fashion into two registers so that one may be refreshed as the other is utilized to supply the required pattern. Since 11 bits are assigned to the depth of the compacted word, each register should be 2 raised to the eleventh power or 2048 bits deep. Data to be applied to the UUT, data expected back from an operational UUT plus real-time bidirectional control and real-time masking data can all be so converted.

This approach allows a large amount of data to be stored in a small amount of memory (average of 30/1 compression). This same technique also frees the tester repetition rate from the memory access time. In essence, the memory speed is multiplied by an average of 30 times in so far as test rates are concerned.



DECOMPACTION FLOW, APPLY/EXPECT BIT

FIGURE 7-1

For example, compacted data from a 30 MHz memory could provide sufficient data to allow a tester to operate at repetition rates far in excess of 100 MHz. At an average compaction ratio of 30 to 1 an equivalent 480 bits are available every 33 ns (bit to ns ratio of 14.5 to 1). At a 100 MHz maximum repetition rate, 3 bits maximum (apply/expect, bidirectional, mask) are required every 10 ns (ratio of 0.3). Thus, the timing factor of safety generated by the decompaction module is approximately 48 to 1.

Two code formats will be utilized. The first was described in Section 2-1. The second must be fine-tuned but will be used for directed real-time branching so as to cycle single and multiple nested loops. The use of two different formats will optimize the overall coding technique.

Since it is legal to switch between the basic, clock, and compacted formats in real-time, the worst case timing situation must be accommodated. This occurs in the tri-state condition when the local memory stores the apply/expect, bidirectional, and mask data. To make sure the data is available for all 3 bits when entering the compacted phase, a software pre-scan extracts the first compacted word for each of the 3 types. Each word is decompacted and entered into its appropriate Register 1 prior to test. Before leaving the compacted mode during testing, the register not supplying the final data of the current sequence is filled with the initial data of the next compacted sequence. In this fashion timing problems are avoided. The rearrangement of the arrays is accomplished during the test program preparation process by the operating system which compacts the absolute data.

Using the wide memory store and a 30 MHz access time, the

minimum instantaneous compaction ratio is eliminated as a potential problem area. Since a maximum of 3 bits are required every 10 ns in the worst case, an equivalent 10 bits are required every memory cycle time of 33 ns. Since 12 bits are available the maximum repetition rate is achievable even with an absolutely incompressible data segment! If all 3 bits are not necessary (i.e. bus type UUT pin) an even greater factor of safety is present.

The use of a wide memory word and/or use of the decompaction module provide another advantage in that the UPE channel is essentially divided into higher speed and lower speed sections. A speed dichotomy is effected between the inputs and outputs of these modules. The higher speed circuitry is restricted to areas such as the driver/receiver, clock, compare, etc. whereas much of the UPE design can be much lower speed (e.g. I/O interface, level generation, local memory, local micro-controller, etc.).

Still another advantage gained by the use of the decompaction module is the dramatic increase in overall test throughput. A significant amount of time is normally used to transfer the large amounts of array or vector data from the test system bulk storage medium (e.g. disk) to the pin electronics via the system I/O. The bit width and the transfer time of the I/O bus are major constraining factors. The transfer time is much larger than the actual test time in many cases. The use of the decompaction module will decrease this transfer time drastically since the data is expressed in coded form. It is decoded in real-time as the test program progresses so overall time (transfer plus actual execution) is significantly reduced.

The decompaction module is a key to valid testing since it

allows a tester to store the large arrays required by today's complex LSI UUT. It is also a key to operation at the high frequencies required by this class of UUT. Finally, it can drastically reduce overall test time by minimizing the time to transfer array data from the system bulk storage medium.

7.2 DECOMPACTION MODULE SPECIFICATION

Input Format	1	Bits 1, 2, 3	One of eight patterns
		Bits 4 through 14	One to 2048 counts
		Bits 15 and 16	Basic, clock or compacted next word
Input Format	2	TBD	
Output Format		Alternating, serial 2048 bit maximum registers	
Input Frequency		30 MHz maximum	
Output Frequency		100 MHz maximum	
Power Supply Voltage		Note 1	
I/O Levels		Note 1	
Operating Temperature Range		Note 2	
Maximum Power Dissipation		Note 2	

Note 1

Power supply voltage and interface levels, fan-out capability, etc. must be consistent with overall system design

Note 2

Operating temperature range and maximum power dissipation must be such that the overall environmental specification of Section 2 is achieved.

SECTION VIII

8.0 FUNCTIONAL DIGITAL SUBSYSTEM

8.1 FUNCTIONAL DESCRIPTION

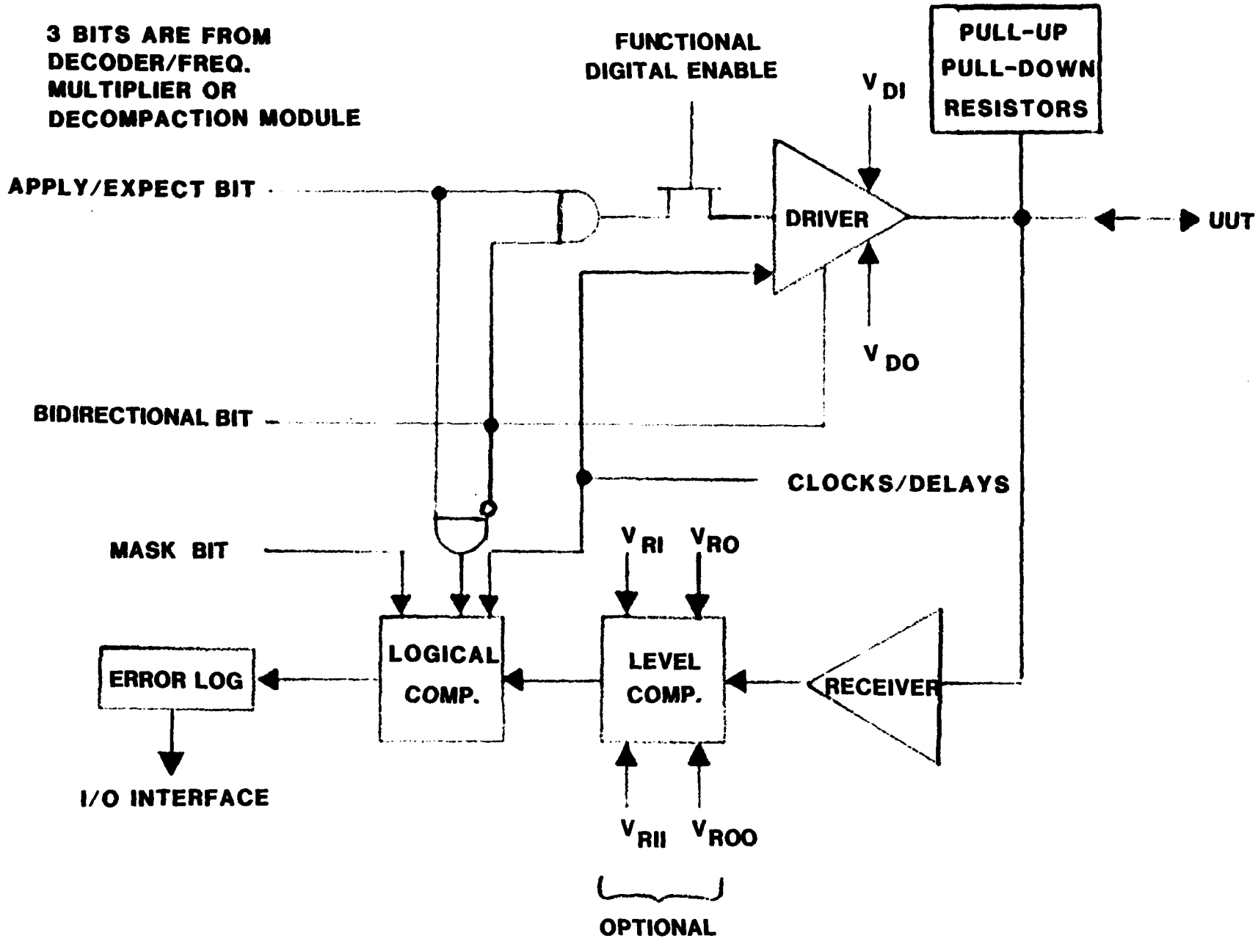
The functional digital subsystem consists basically of the driver/receiver and comparison circuitry as depicted in Figures 2-1 and 2-2. It supports testing of input only UUT pins, output only pins, or tristate bus pins. It can be utilized in GO/NOGO testing or in fault isolation testing of either the guided probe/clip or fault dictionary type. Referring to Figure 8-1, this subsystem receives up to three bits of data per clock cycle from:

a) the decoder/frequency multiplier if absolute data is used

b) the decompaction module if compacted data is used

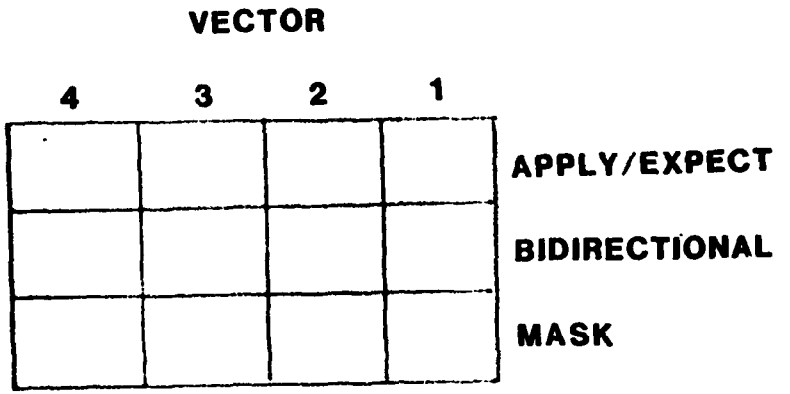
If the UUT pin is an input only, apply data is valid. If the pin is an output only, the expect data is valid. Both are coded on the same physical line. If the UUT pin is a tristate bus, apply/expect data is interspersed on the same line. In this case bidirectional data is utilized in order to control the output impedance of the driver. In many cases it is likely that mask bits will be necessary to screen out the "don't care" situations often encountered in testing. This is especially true during initialization procedures until the UUT can be sequenced to a predictable state. It is also becoming more common as bus structured UUT are used widely. Without such masking capability, indications of errors will be generated where it is desirable they be ignored.

Referring to Fig. 8-1, the Apply/Expect (A/E) line is used



FUNCTIONAL DIGITAL SUBSYSTEM

FIGURE 8-



FOUR-VECTOR COMBINER

FIGURE 8-2

to apply a stimulus bit to the UUT via the driver, to supply a bit to the logical comparator which represents the expected output from the UUT in that bit time, or both according to the bit time if bus type testing is being performed. The real-time bi-directional bit is used to control the driver output impedance. A high impedance or tri-state output can be programmed in real-time. Thus the driver can drive the bus or its low impedance can be removed from the bus in real-time so that the receiver may monitor the UUT. The mask bit is used to supply "don't care" overrides during those bit times when the UUT pin is not in a predictable state (e.g. during initialization).

A typical input stimulus bit stream to be applied to the UUT would flow from the A/E, be enabled via the digital enable line, pass through the driver and be programmed to the logic levels determined by VD1 and VD0, and be applied via the carefully controlled output impedance and slew-rate of the driver to the UUT.

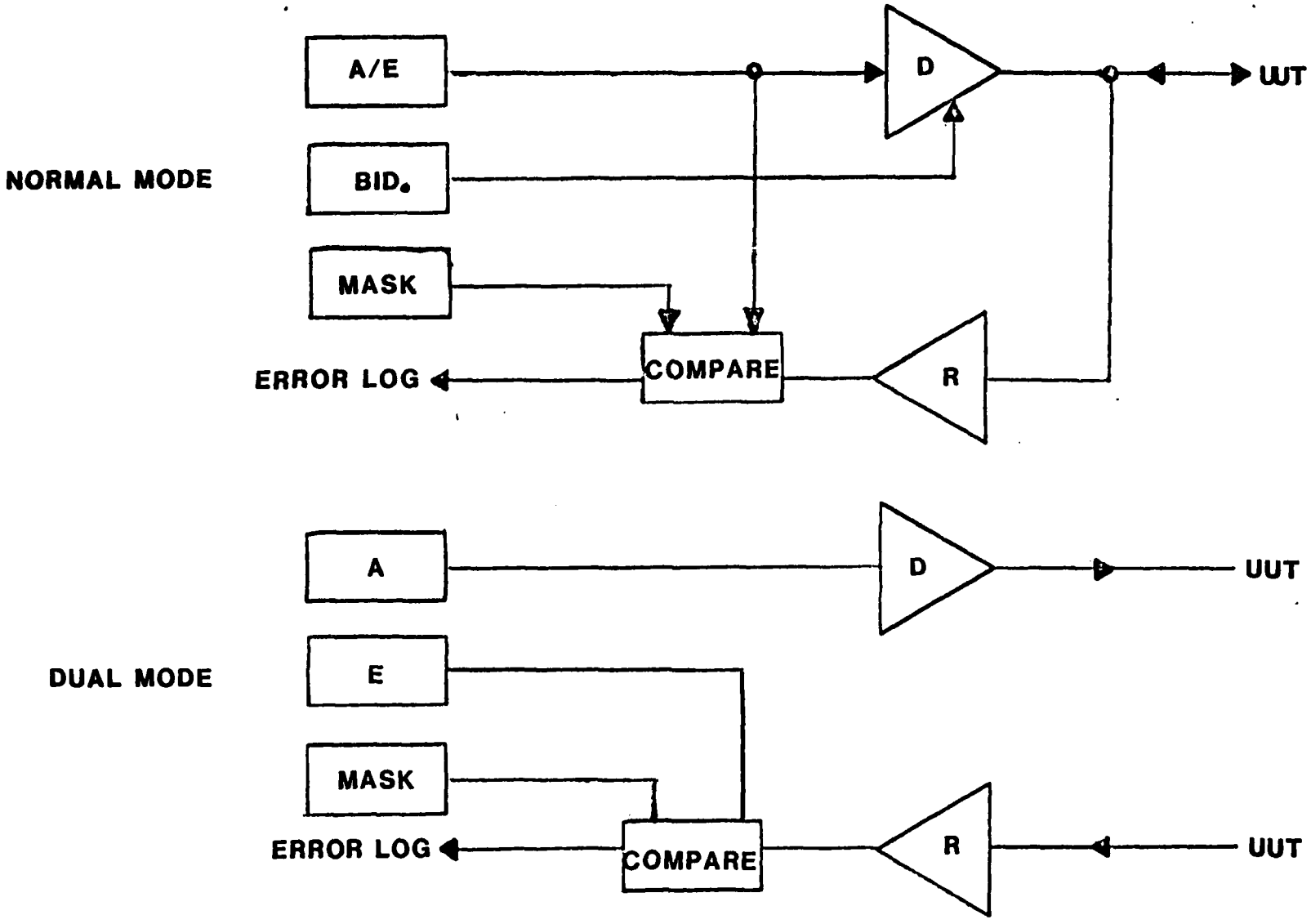
A typical output bit stream from the UUT would be buffered by the high input resistance, low input capacitance receiver, converted into a low impedance environment by the receiver, compared in the level comparator against VR1 and VR0(level mode) or VR1,VR11,VR0, and VR00(window mode) to ascertain whether an acceptable logic one or zero were present in a given bit time, compared against the expected bit as determined by the A/E input, and masked by the mask line as appropriate. The results of the comparison are entered into the error log.

In the case of a bus-type UUT pin, the apply/expect, bi-directional, and mask bits are all necessary. A basic word from memory extracts four 3 bit vectors and utilizes them as shown in

Fig. 8-2. If the UUT pin is an input only, 10 bits are strung together to form apply bits. If the pin is an output only, they are strung to provide 10 expect bits. If the pin is an output and the ability to mask is desired, the original format of Fig. 8-2 is employed with the exception that the 4 bidirectional bits are not utilized. All of this is determined prior to testing by a software analysis of the test program and the appropriate format so dictated.

A first-in first-out (FIFO) memory architecture is a good candidate for this application. In a FIFO the input and output data rate is basically uncoupled. It is not certain whether current commercially available FIFOs meet the frequency requirements. However, since the UPE will eventually be physically implemented in one or more special modules, a FIFO like architecture can be designed with appropriate speed characteristics.

It is a major goal of the UPE to provide as many pins of capability as is possible in as small a physical package as possible. In order to help achieve this goal, one channel of UPE can be used in a dual mode to provide both a functional digital input to the UUT and to monitor a functional digital UUT output. Referring to Fig. 8-3, the usual signal flow is depicted in the upper diagram. To utilize the channel in a dual mode, the flow in the lower diagram is used. An apply pattern can be directed to a UUT input pin and an expect/mask simultaneously to a UUT output pin. If pin clocks and APG are used in this mode a channel is used as an input or an output but not both. A software scan prior to test would identify any pins requiring a pin clock or APG capability and so rule their dual use as illegal. The use



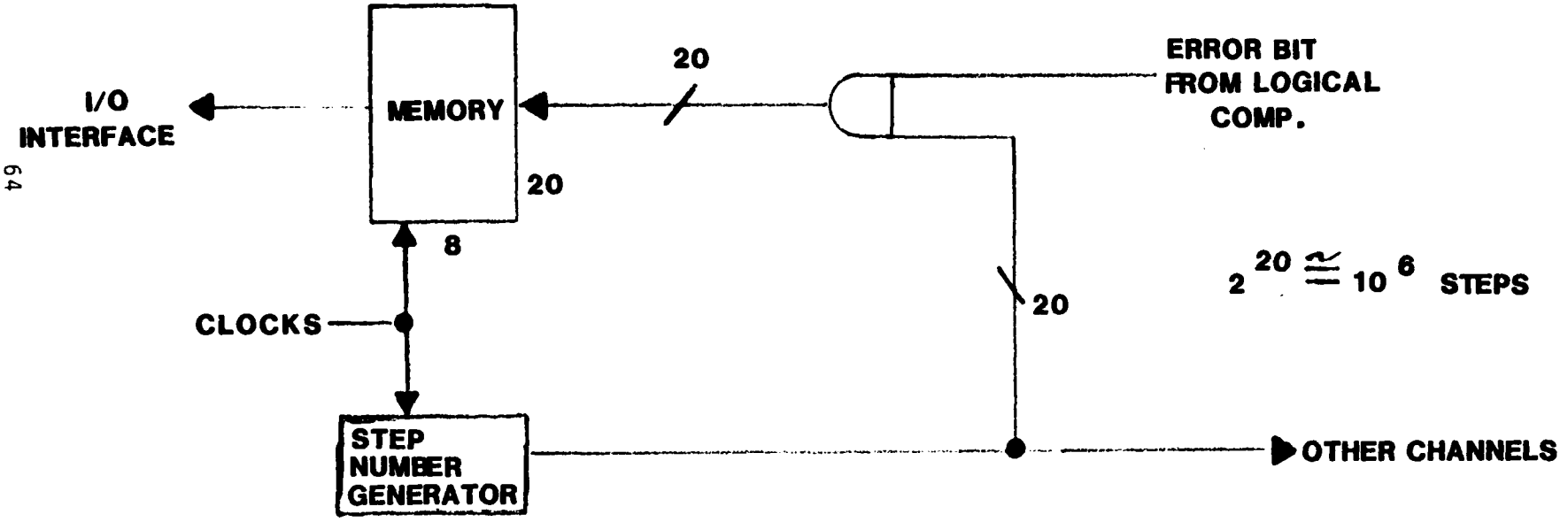
CHANNEL MODES

FIGURE 8-3

of compacted data is legal on channels utilized in the dual mode. The minimum instantaneous compaction should be scrutinized in advance by a software scan since the combination of apply, expect, and mask could be less compactible than an apply/expect, bidirectional, mask combination.

The two most powerful fault isolation techniques in current use are algorithms for fault signature table lookup and for error tracing using a guided probe. There are a number of fault signature lookup algorithms which allow the utilization of different data recording techniques. An investigation of these algorithms was made and it was determined that algorithms similar to those supported by LASAR (an ATPG software package) which describe failure signatures in terms of a unique set of pin and bit times for each failure were the most versatile and powerful currently available. Similarly, it was found that guided probe algorithms have been designed around several of the data recording techniques. An investigation of these algorithms yielded the conclusion that tracing the earliest error appeared to be most effective.

The error log is designed to store failures in a format which will optimize the presentation of this data for both the fault signature and guided probe modes of fault isolation. An 8 by 20 memory will be implemented in the error log of each channel (refer to Figure 8-4). Upon detecting a UUT failure, the step number of the test program will be stored in the error log memory. The first 8 failures will be identified by step number. This depth is deemed sufficient for detailed fault isolation and



ERROR LOG FORMAT

FIGURE 8-4

the use of a 20 bit word allows over 1 million vectors to be identified. Thus, the fault isolation software in the main controller receives the test step number for the first 8 failures on each pin. As noted this format is optimal for the fault signature and guided probe software packages.

The driver and receiver are the most important parts of the functional digital subsystem. They are so important, in fact, that they are discussed in detail in Section 9.

8.2 FUNCTIONAL DIGITAL SUBYSTEM SPECIFICATION

Maximum Functional Digital Repetition Frequency	100 MHz
Minimum Vector Depth (standard)	20K (8K tri-state)
Minimum Vector Depth (compacted)	250K
Simultaneous Logic Families	Unlimited
Crosstalk Betweeen Pins	60 dB MIN.
Driver Output Range	+-10 V
Driver Output Resistance	1 OHM MAX. (Short-Circuit Proof)
Driver Source/Sink Current	+-50 ma
Maximum Driver Skew	+-1 ns
Driver Slew Rate	1 v/ns
Minimum Driver Tristate Impedance	100 K OHMs
Driver Accuracy	1%
Driver Resolution	80 mV
Driver Overshoot	10% no load
Receiver Input Range	+-10 V
Receiver Input Voltage Protection	+-20 V
Receiver Input Resistance	1 MEGOHM MIN.

Receiver Input Capacitance	10 pF MAX.
Maximum Receiver Skew	+-1 ns
Receiver Accuracy	1%
Receiver Resolution	80 mV
Receiver Input Levels (standard)	2
Receiver Input Levels (optional)	4
Pull-up Load Resistor	One per channel
Pull-down Load Resistor	One per channel

SECTION IX

9.0 DRIVER/RECEIVER

9.1 FUNCTIONAL DESCRIPTION

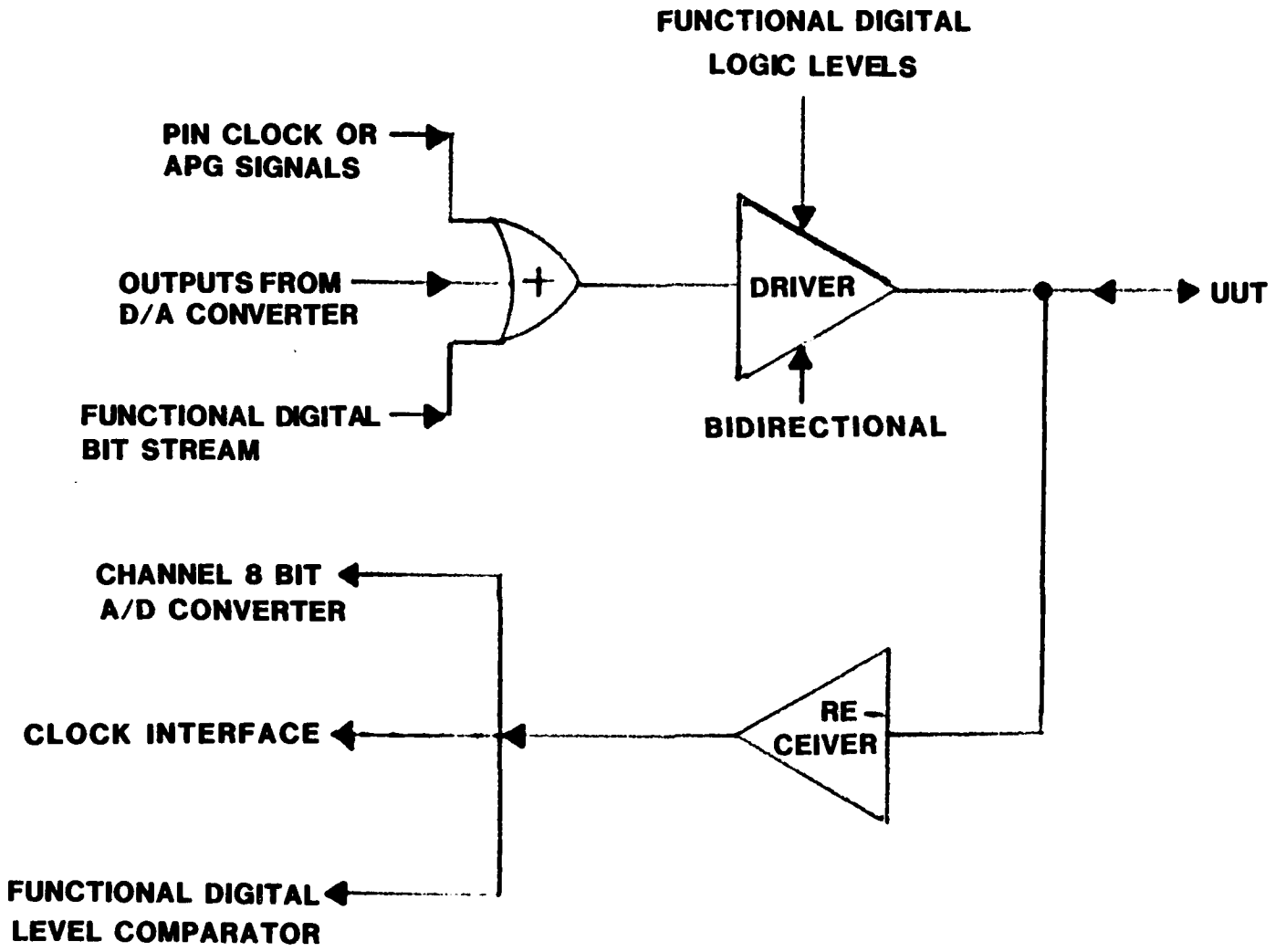
The universal pin electronics driver and receiver are two critical elements of the functional digital subsystem. They are of significant importance to warrant an entire section devoted solely to them. The driver is used to apply the functional digital, parametric digital, and analog signals to the unit under test. Its role is to ensure that the integrity of the waveform is preserved all the way to the UUT interface. The driver has a low output impedance which ensures the maximum accuracy despite the amount of current which flows between it and the UUT. In the analog and parametric digital cases, it must also ensure that the various waveforms generated out of the universal pin electronics D/A converter are maintained from an integrity standpoint all the way to the UUT. In the functional digital case, the slew rate of the driver must be carefully controlled so as to be compatible not only with the speed requirements of the UUT, but also to ensure that excessive overshoot and ringing do not occur because of the physical distance between the driver and the UUT. Slew rates which are selectable under local microprocessor control are a distinct possibility for optimizing performance. Also, in the functional digital case, the pin electronics driver must also be able to go to a tri-state or high impedance condition so as to be able to be compatible with the bus type testing which is so typical of today's microprocessor populated UUT.

The receiver is also extremely important. It should present

a high resistance, low capacitance to the UUT so that it has a minimum effect on the accuracy of the outputs from the UUT. It must not load the UUT from a resistance standpoint thereby affecting voltage accuracy nor must it provide excessive capacitive loading so as to change the phase or shape of the UUT waveform. The receiver buffers the signal from the UUT and converts it into a low impedance environment so that it can be processed within the confines of the universal pin electronics channel. It is basically a buffer and an impedance converter. Its slew rate, or ability to respond to the UUT is also of extreme importance. When a functional digital output is accommodated, the receiver directs the signal to the level comparator for checking against preprogrammed levels (VR1, VR0). In the analog and parametric digital modes it directs the signal to the 8 bit A/D converter for digitizing. It also routes clock outputs from the UUT for synchronizing with internal UPE clocks.

A flow diagram of the driver receiver subsystem is shown in Figure 9-1. Inputs to the driver can come from pin clock or algorithmic pattern generator signals, from D/A convertor outputs, or from the functional digital subsystem. Outputs from the latter source can be programmed to specific logic 1 and logic 0 levels as they pass through the driver and are applied to the UUT. Outputs coming back from the UUT are first buffered by the receiver. The receiver output can be directed to either the 8 bit A/D converter, to the level comparator in the functional digital subsystem, or to the clock interface.

In the case of the D/A converter inputs to the UUT, they pass through the driver on a one to one voltage basis. In other



DRIVER/RECEIVER
FIGURE 9-1

words, the waveform voltage is preserved as is. Range changing is effected in the D/A. Inputs from the functional digital, pin clock or APG are modified according to the logic level inputs dictated by the logic level generator subsystem.

Outputs from the UUT pass through the receiver on a one to one voltage basis in all cases. Range changing is effected in the A/D. Both the driver and the receiver effect an impedance conversion on all signals. The driver presents a carefully controlled one ohm or fifty ohm output to the UUT (the former for functional digital and the latter for parametric digital and analog) and the receiver presents a high resistance, low capacitance to the UUT.

As mentioned previously, there is a distinct possibility that the driver slew rate will be made a programmable function under control of the the local microcontroller. Individual slew rates would be selected in accordance with the type and frequency of the signal to be generated for application to a UUT pin. In each case the slew rate selected would be in consonance with the programmed voltage, frequency, etc. (e.g. faster slew rates would be used for the higher frequency, lower voltage range signals). The determination of whether or not to provide selectable slew rates will be made during the detailed design phase. The added complexity would be evaluated against the enhanced performance characteristics.

9.2 DRIVER/RECEIVER SPECIFICATION

Driver Input Signals	Pin Clock, APG, D/A Converter, Func. Digital Subsystem; programmed Logic Level signals
Driver Output Signal	To UUT
Receiver Input Signal	From UUT
Receiver Output Signals	Channel 8 bit A/D, Func. Digital Level Comparator, Clock Interface
Maximum Functional Digital Repetition Frequency	100 MHz
Maximum Parametric Digital Stimulus/Measurement Rate	20 MHz
Maximum Analog Stimulus/Measurement Rate	20 MHz
Driver Output Range (Functional Digital)	+-10 V
Driver Output Ranges (Analog/Parametric Digital)	+-10 V, +-1 V
Driver Output Resistance (Functional Digital)	1 OHM
Driver Output Resistance (Analog/Parametric Digital)	50 OHMs
Driver Source/Sink Current	+-50 ma
Driver Slew Rate	1 v/ns
Minimum Driver Tristate Impedance	100 K OHMs
Driver Accuracy	1%
Driver Overshoot	10% no load
Maximum Driver/Receiver Skew	+-1 ns
Receiver Input Range (Functional Digital)	+-10 V
Receiver Input Ranges (Analog/Parametric Digital)	+-10 V, +-1 V

Receiver Input Voltage Protection	+-20 V
Receiver Input Resistance	1 MEGOHM MIN.
Receiver Input Capacitance	10 pF MAX.
Receiver Accuracy	1%

SECTION X

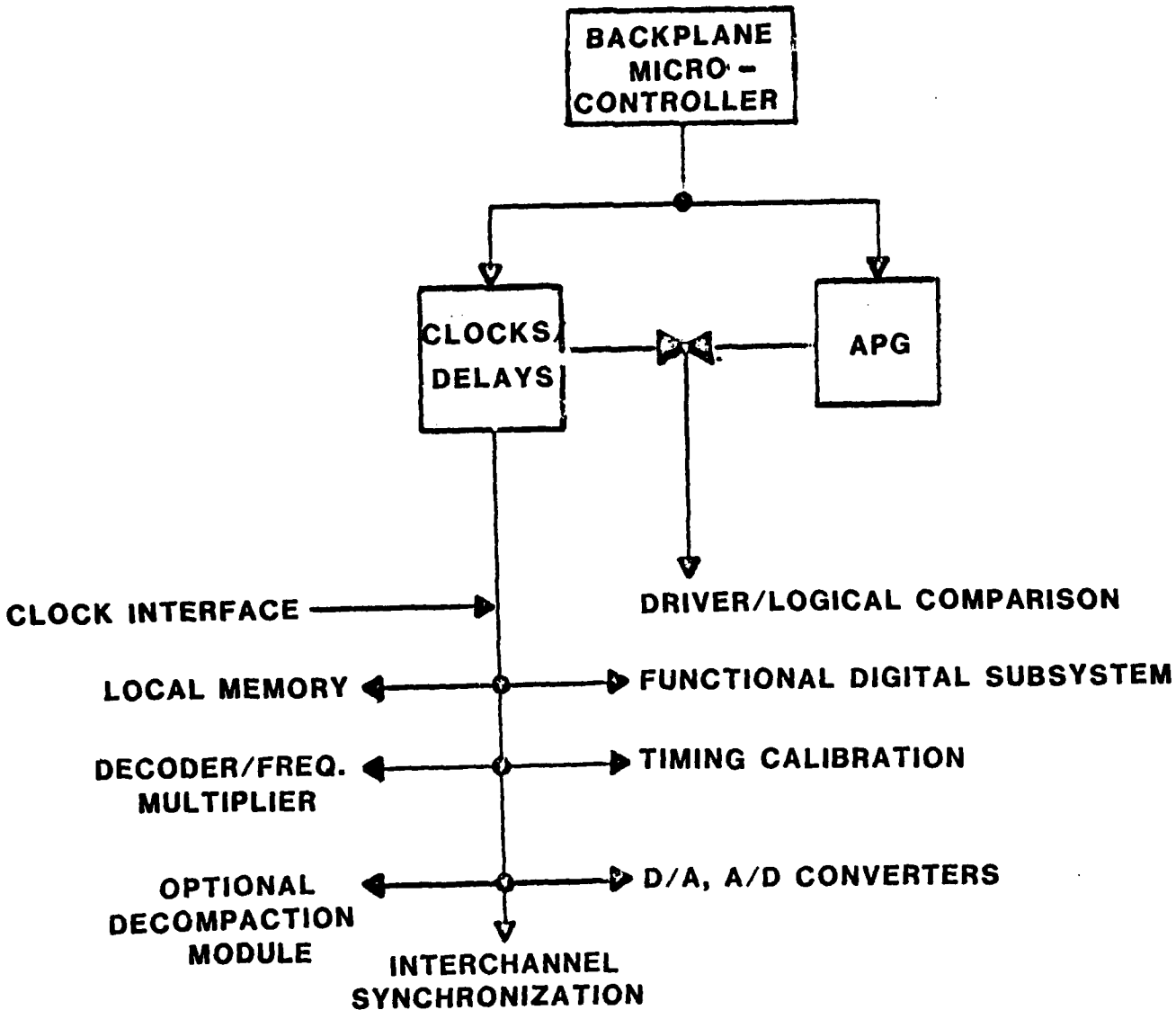
10.0 CLOCK/DELAYS/APG

10.1 FUNCTIONAL DESCRIPTION

The clock/delay and algorithmic pattern generator subsystem is the key timing module in the UPE. As can be seen from the block diagram of Fig. 10-1, the clock/delay is used to effect synchronization between virtually all subsystems in a channel and also to coordinate between channels when a UUT measurement so requires (e.g. skew between two output pulses, phase shift between two analog outputs, etc.).

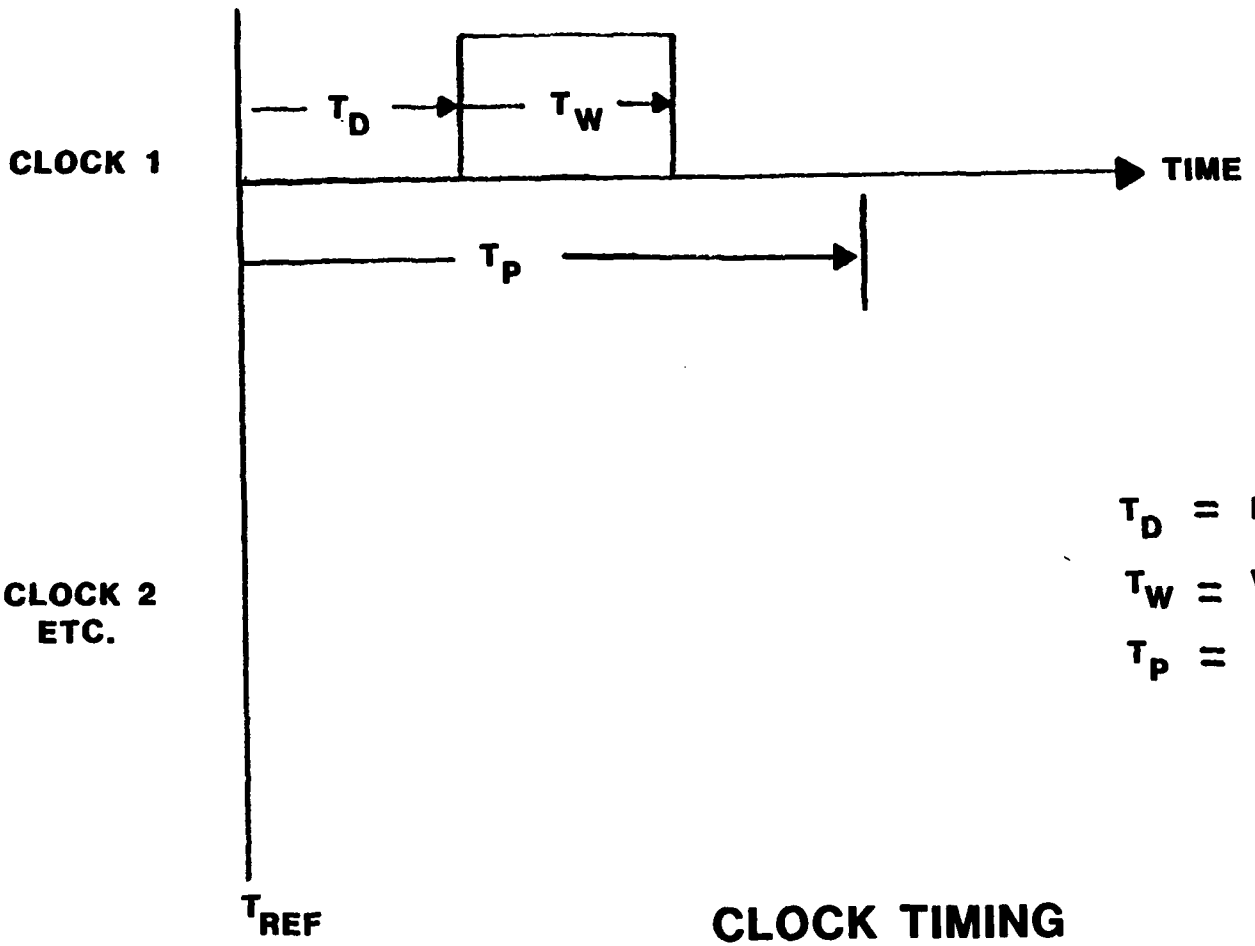
In functional digital testing, the clock(s) are programmed to specific frequencies, widths, etc. and are utilized to strobe test vectors to the UUT. Any of the seven clocks can control any one or more UPE channels. The clocks can be synchronized among themselves or with regard to any UUT clocks in any combination. The clocks are also used to program the delay between when a test vector is applied to the UUT and when the resultant UUT output vector(s) are compared in the functional digital subsystem logical comparison circuit. This programmed delay accounts for the UUT internal propagation delay. Again, any UPE delay can be directed to any pin or pins under program control. Virtually all of the other UPE subsystems are synchronized to the clocks/delays. Figure 10-2 shows how clock period (frequency), delay and width may be programmed and synchronized to a reference clock or clocks which may be internal or derived from the UUT.

Today many UUT contain multiple logic families. Many have dynamic, multiphase requirements. For this reason up to seven



CLOCKS/DELAYS/APG

FIGURE 10-1



T_D = DELAY TIME

T_W = WIDTH TIME

T_P = PERIOD

CLOCK TIMING
FIGURE 10-2

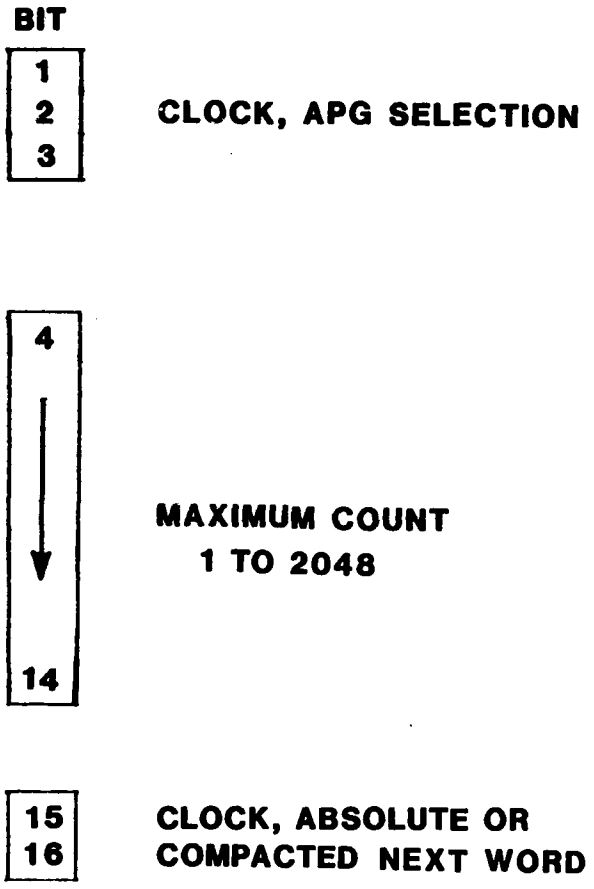
clock/delays may be selected under program control. Each may be assigned to any channel or combination of channels. Refer to the specification of Section 10.2 for exact details.

Delay lines already exist in the receiver portion so as to automatically effect calibration. These delays can also be utilized selectively for test purposes. Their fine resolution can be controlled by the local microprocessor as a delay vernier in addition to the already flexible clock/delay capability. In effect this increases the capability from seven clock strobes to an unlimited number in the fine resolution range where control is important. Since the calibrated table of values is stored locally, the microcontroller can restore the normal calibration values at the conclusion of the test program.

In the analog or parametric digital modes the clocks are used to strobe stimulus data to the UUT via the local memory, D/A, and driver. They also strobe this type of UUT output data via the receiver to the 8 bit channel or 16 bit group A/D converter and finally to local memory. Measurements between channels are also synchronized by the clocks.

Every effort is made to optimize the use of local memory. Thus a pin clock is also available. In this mode a clock may be selected and applied directly to the UUT via a driver or drivers. Fig. 10-3 shows how a burst of up to 2048 clock pulses may be generated by a single word from local memory.

Often ATE/UUT synchronization is effected by allowing one or more UUT clocks to control the test situation. In order to achieve the optimal flexibility in this regard, each UPE receiver will accept a clock output from the UUT and, under program



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PIN CLOCK WORD FORMAT

FIGURE 10-3

control, assign it to any one of the 7 clock control lines. A simple clock interface is utilized as a level controller. In this manner total flexibility is achieved between UPE and UUT clocks without the necessity of any special cabling or interface buffe ng between the two.

The APG section is also of extreme importance. Today most test systems on the market fall into the category of having their programs generated by software means. Simulators and ATG (automatic test generation) packages are common in the industry. Without the use of software packages to generate test programs, it would be extremely difficult to test functional digital UUT. In short, the required arrays or test patterns are derived on a software basis. This is because there is a unique test program for each different type of UUT. There is really no standard test program which can be utilized for these random logic type UUT.

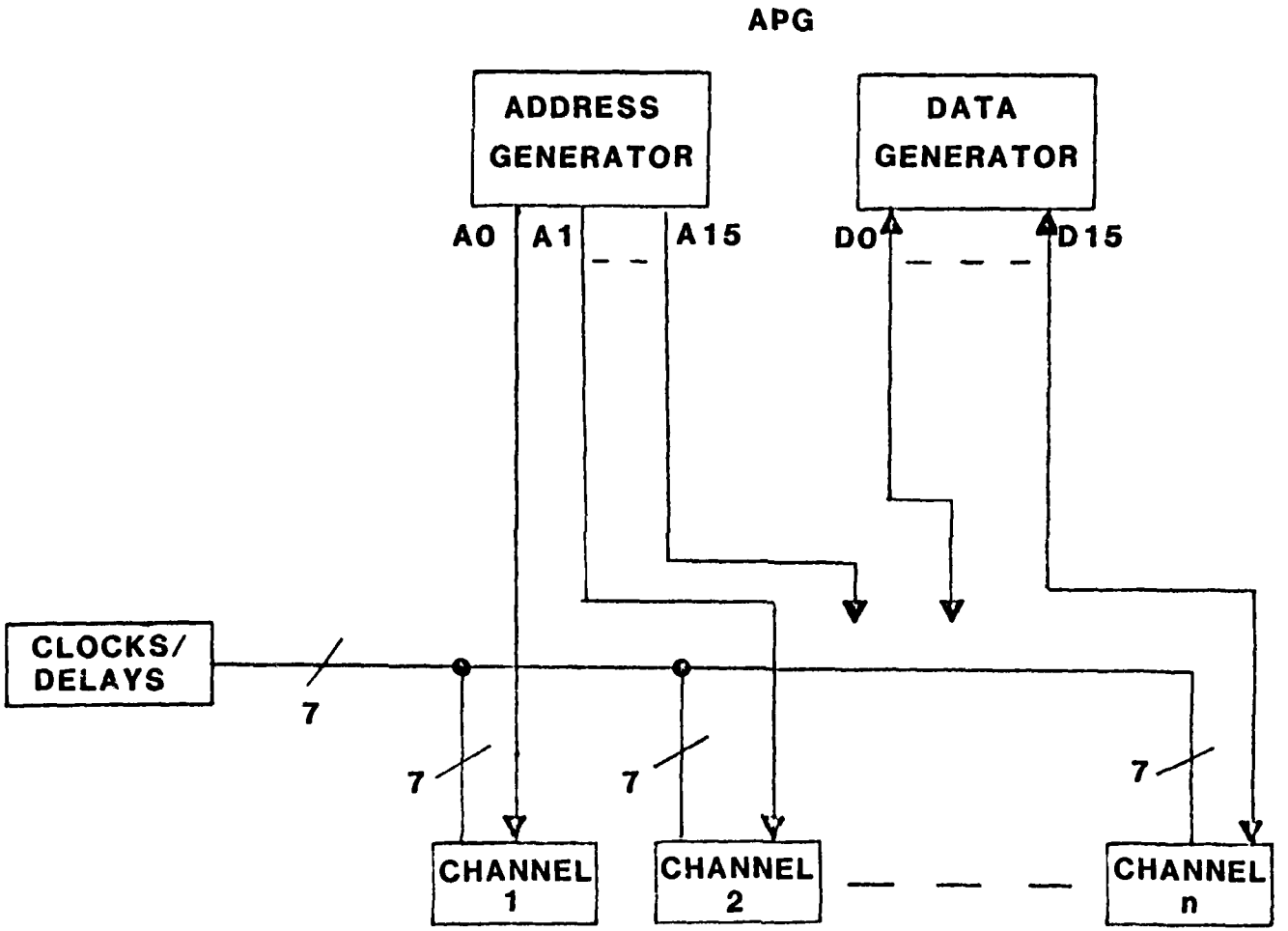
In the memory test industry, however, standard patterns are the norm. Memories are very predictable devices, regardless of whether one considers a large or small memory, a fast or slow memory, all are tested in much the same way. Words are written to the memory and then read back to determine whether or not the memory stored them correctly. In addition to looking for the word coming back in the correct fashion from the correct location, a check is made to ensure that there was not an inadvertent write to sections of the memory other than the intended area. Because of these reasons, the memory test industry has derived relatively standard test patterns. Some of the more common are walking ones, walking zeros, checkerboards, inverted checkerboards, and so on. Since these stimuli are standard, memory

testers usually generate them in hardware directly in the test head electronics. This eliminates the need for laborious software preparation of patterns. Since the patterns are generated locally in the test electronics they can also be applied at very rapid rates to the UUT. This is because they do not have to be transferred from a bulk storage medium such as a disk to the local electronics. They are generated right in the local electronics.

There is a real dichotomy between memory testers and so called random logic testers. The former have their stimuli and measurement derived in hardware, the latter must do it by lenghty software means. Since the vast majority of UUT are of the random type, the universal pin electronics will utilize patterns derived from the very best of today's simulators and automatic test generators. However, it is desirable to also have in the universal pin electronics local hardware generation of patterns in order to take advantage of the speed and lack of storage required when testing in this mode. UUT with both random logic and embedded memory are becoming much more common as memory chips become more and more dense. Thus, the UPE will have a so called algorithmic pattern generator which will be used to test memories. The use of the APG will allow the optimal use of local memory. In other words, it will not be necessary to store these repetitive standard patterns in the local memory. They will be generated algorithmically in hardware as required. Thus, the local memory is freed for random logic type patterns. The APG will be selectable under program control in the same manner as selecting a pin clock. The APG patterns will run in sequence on an interrupt

basis. The first sequence may be to apply walking ones to the UUT, the second to apply walking zeros, the third checkerboard, the fourth inverted checkerboard, and so forth. Expected patterns generated by the APG are compared against UUT outputs in the logical comparison circuitry. As soon as the sequence has been completed, the control will be handed back to the normal program on an interrupt basis. The clock/delays may be applied across all channels with complete flexibility (refer to Fig. 10-4). This flexibility is not necessary for the APG outputs. Each APG output will be assigned to a specific channel. Wiring between the UPE and the ATE will connect each APG line to the appropriate UUT pin.

The capability to generate patterns in hardware by the APG will be of substantial benefit to the UPE. As mentioned, many boards today contain not only random logic but memories. This is because the density of the memories has been increasing so rapidly that now it is not required to utilize an entire board full of memory to fulfill many system _ poses. In many cases a small portion of the board will suffice. Therefore, many boards contain a portion of memory and a portion of random logic. With the APG capability in the universal pin electronics, software derived arrays or patterns will be utilized to test parts of the board which house random logic and the APG will be used for the portions of the board which house memory. If all of the required memory patterns were generated by software means it would be a very inefficient use of local memory. Even if the optional decompaction module were present, it is much more efficient to generate memory patterns in hardware by the APG method.



CLOCK/DELAY, APG INTERCONNECT

FIGURE 10-4

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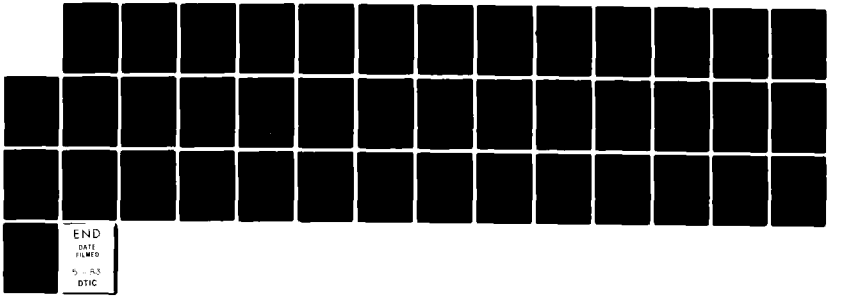

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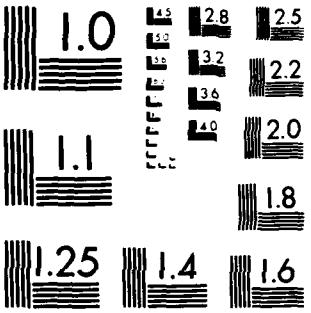


10.2 CLOCKS/DELAYS/APG SPECIFICATION

Number of clock/delays	7
Number of clock/delay edges	14
Clock/delay range	1 Hz to 100 MHz
Clock/delay strobe resolution	0.5 ns
Clock/delay jitter	0.5 ns
Clock Modes	Asynchronous, synchronous to other clocks &/or to UUT, or external
Algorithmic Patterns	Walking one, walking zero, checkerboard, inverted checkerboard
APG address width	8 standard, 16 optional
APG data width	8 standard, 16 optional
Power Supply Voltage	See Note 1
Internal Interface	See Note 1
Operating Temperature Range	See Note 2
Maximum power dissipation	See Note 2

Note 1

Power supply voltage and internal interface levels, fan-out, etc. must be consistent with overall system design

Note 2

Operating temperature range and maximum power dissipation must be such that the overall environmental specification of Section 2 is achieved

SECTION XI

11.0 A/D CONVERTERS

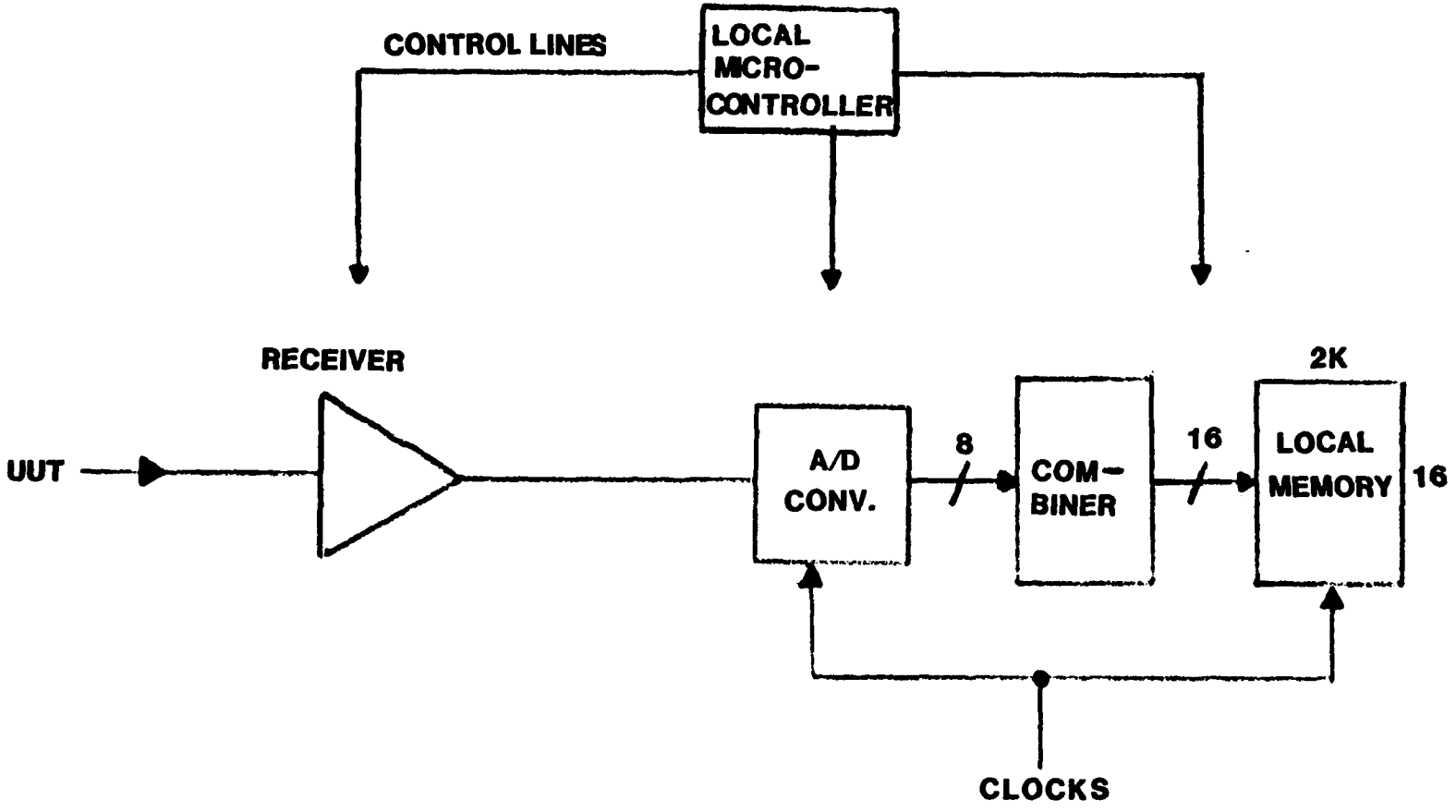
11.1 FUNCTIONAL DESCRIPTION

Referring to the analog, parametric digital signal flow diagram of Fig. 11-1, an output from the UUT enters the high resistance, low capacitance receiver whose low impedance output is routed to the 8 bit A/D converter. The output of the latter is directed to a combiner which buffers the data and combines two words in a 16 bit format for entry into the memory. The combiner is the key to using a 30 MHz memory and achieving a 60 MHz sampling capability.

Factors such as the A/D sampling rate, the programmed clock frequency, and the local memory access time all are factors in determining the maximum sampling rate of the UPE. Two 8 bit samples from the 8 bit A/D converter are combined and written into local memory. Since the local memory is 30 MHz maximum an effective 60 MHz sampling rate is achieved. This corresponds closely to the state of the art sampling rate of 8 bit A/D converters. As in the case of waveform generation, the use of filters is implicit in the A/D block. Such filters are totally under control of the local microcontroller.

The Nyquist criterion assumes that all frequencies present in the signal being measured are less than half the sampling frequency. Other criteria usually require the maximum frequency content to be one-third or less the sampling rate. Thus, the upper limit for waveforms to be evaluated is 20 MHz.

The UPE architecture is very flexible. IT is expected that



ANALOG, PARAMETRIC DIGITAL SIGNAL FLOW
FIGURE 11-1

A/D technology will continue to evolve in a rapid fashion. As this occurs such improved components may be easily utilized to extend this upper limit.

A significant feature of this architecture is its ability to capture an entire waveform and, under local microcontroller control, provide from the most elementary to the most exhausting analysis. For example, a UUT output pulse can be captured and complete data, such as rise time, fall time, width, etc. can be obtained locally from a single measurement. Multiple measurement instruments are not required. Both repetitive and one shot waveforms can be accommodated. After final analysis by the backplane microcontroller, only the final actual values of each parameter required by the test program need be sent back via the I/O bus to the main controller.

The generation of UUT stimuli from local memory and the recording of UUT outputs into local memory is controlled by the UPE clocks. UUT output measurements may be of the continuous type or they may be single-shot (e.g. a pulse). For continuous type signals the memory snapshot (the digital "grid" when the conversions are halted) may be taken on an enable bit such as a zero crossing or simply under program control. For single-shot outputs the snapshot may be effected via an external sync input from the UUT or from another UPE channel. When the sync signal occurs the next 4K conversions are captured.

The UPE channel is also capable of a self-trigger. Unlike the self-trigger process normally encountered, the initial part of the UUT waveform need not be lost depending on the setting of the voltage trigger level. The digital equivalent of an analog

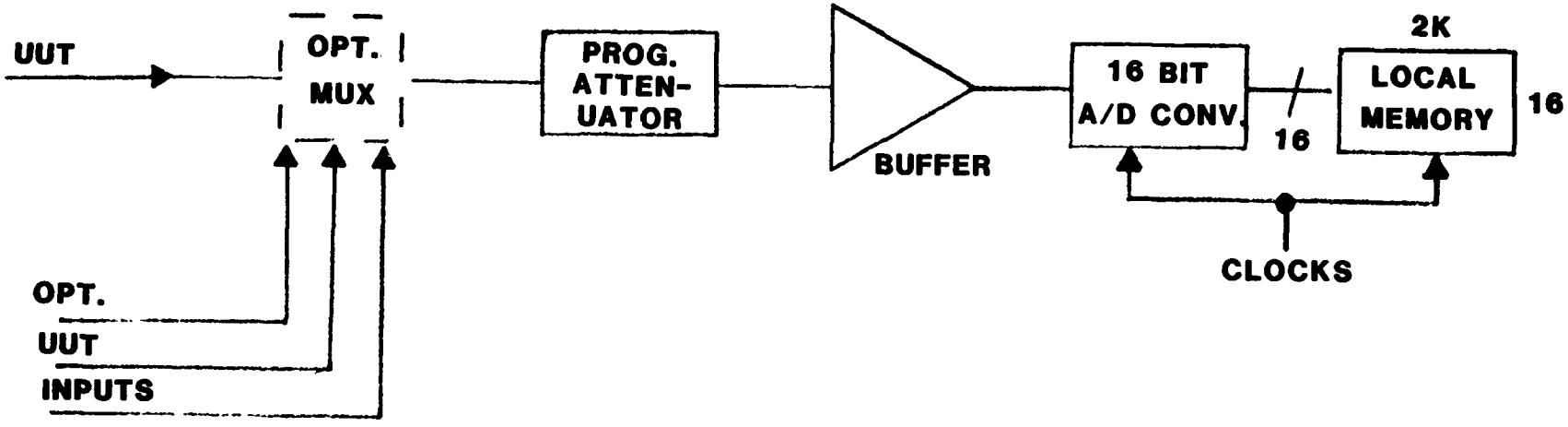
trigger level can be set in the combiner. Until that particular bit in the A/D ladder is enabled the signal is not considered valid. When the bit is enabled the next 3K conversions are captured together with the retention of the previous 1K. Thus the entire waveform is recorded without loss. This approach also prevents triggering on noise and thus not recording the actual output waveform. The 3K/1K split is somewhat arbitrary but probably representative of a reasonable division of post-trigger and pre-trigger data.

Since the local memory is 2k by 16, the equivalent of 4,096 words of 8 bit storage is realized. Using analysis algorithms contained in ROM, the local and backplane microcontrollers will extract any one or more of the following parameters:

Risetime
Falltime
Pulse Width
DC Voltage
Peak Voltage
RMS Voltage
Frequency
Period
Delay
Phase Shift
Events

In the future, additional algorithms can be added to extend this list.

Each UPE board of 8 channels may contain a 16 bit A/D for higher resolution measurements on a selective basis (Fig. 11-2).



16 BIT A/D CONVERTER SIGNAL FLOW
FIGURE 11-2

This type of UUT output is virtually never made at high speed or in real-time. Thus, the slower conversion time of this device is acceptable. Also, it is seldom if ever necessary to measure this type of output on multiple pins simultaneously. Therefore one 16 bit device per group of 8 channels is the maximum utilized.

An optional multiplexer may be utilized in those rare instances where multiple UUT outputs are such that a single 16 bit A/D per group is not sufficient. The optional multiplexer would allow 3 additional UUT inputs to be accommodated in a sequential fashion. UUT outputs of this type may often be of a higher voltage so that a programmable attenuator provides to +,- 10V, +,- 50V, +,- 100V, and +,- 200V ranges under program control.

Any one of the clocks may be programmed to synchronize the timing between analog or parametric digital channels. In essence the clock places a marker at a point or points on the digital equivalent of the UUT output waveform. In this fashion time related, multiple UUT output parameters may be measured. Examples are phase shift in the analog domain and pulse skew in the digital.

11.2 A/D CONVERTERS SPECIFICATION

	CHANNEL A/D	GROUP A/D
Input Voltage Ranges	+-10 V +-1 V	+-10V,+-50 V,+-100V,+-200V
Resolution (bits)	8	16
Max. Conversion Time	16.7 ns	20 us
Output Levels	Note 1	Note 1
Maximum Power Dissipation	Note 2	Note 2
Operating Temperature Range	Note 2	Note 2
Power Supply	Note 1	Note 1

Note 1

Output logic levels/fan-out capacity and power supply voltage(s) should be compatible with the overall system design.

Note 2

Maximum power dissipation and operating temperature range must be chosen so that when the overall design is complete the UPE meets the environmental specification of Section 2.3.

SECTION XII

12. CONTROL SOFTWARE

The UPE control software will be implemented on a microcontroller situated on each 8 channel board and on a single microcontroller located in the backplane (refer to Figures 12-1 and 12-2). In each case the microcontroller shall be an 8086 or equivalent. The exact support chip configuration (e.g. RAM, ROM, etc.) will be determined in the detailed design phase.

12.1 PROGRAM DEFINITION, 8 CHANNEL CONTROL PROGRAM

The purpose of the 8 channel control program is to accomplish tasks including the following:

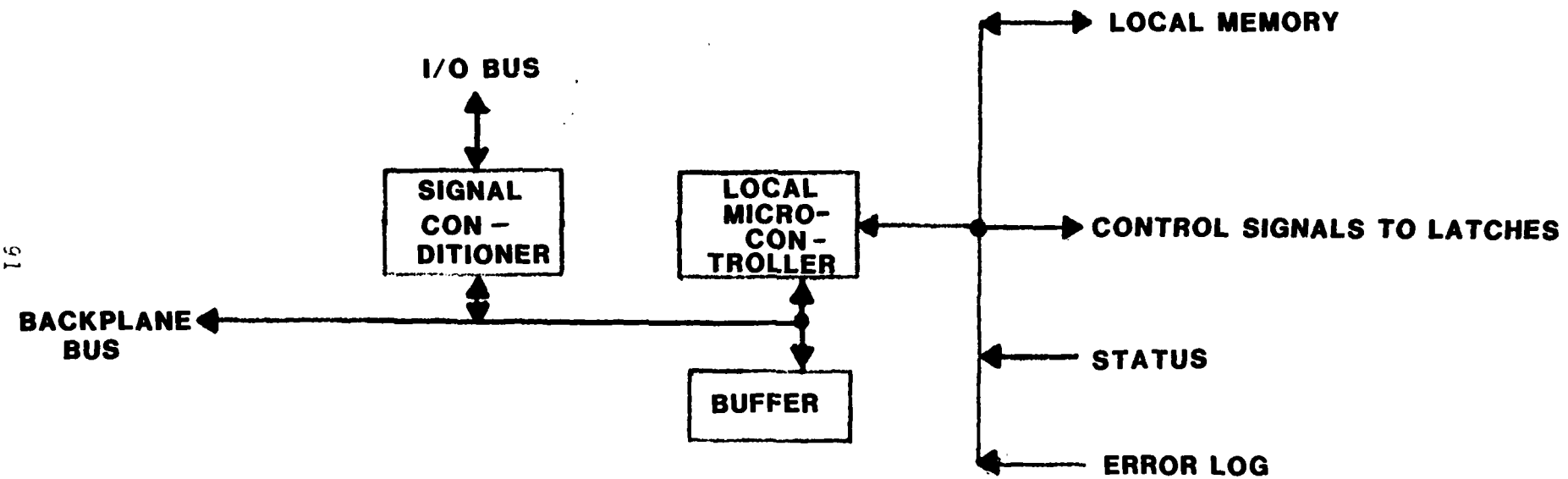
a) Accept commands and data from the interface to the backplane bus and setup the pin channels according to the command requirements

b) Compute and control delay offsets, voltage offsets, and filter offsets to meet calibration requirements

c) Prepare and transfer data between the pin electronics local memory and the backplane interface

This program is intended to be executed on a microprocessor incorporated on an 8 channel pin electronics board. It will be the only program executing on that microprocessor. This microprocessor will be referred to as the local microcontroller. It must interface with the various items on this board as described in the following paragraphs.

The local microcontroller software must control the interface hardware of the 8 channel pin electronics board, accept and



INTERFACE BLOCK DIAGRAM
LOCAL MICROCONTROLLER
FIGURE 12-1

process data input from these interfaces, and prepare and output through them. The hardware interfaces include:

a) Interface to backplane bus
b) Interface to channel function latches
c) Interface to reference voltage DACs
d) Interface to analog filter latches
e) Interface to pin channel local memory routing latches
f) Interface to functional digital error log

Each interface consists of a piece of hardware on the mic controller bus. Each interface has its own bus address, and c mand and control sequence.

The interface to backplane bus provides for a serial transfer of bytes of data both to and from the backplane microcontroller. It includes an interrupt mechanism for signaling that reset is to occur or that test operations are complete. The data is transferred according to a format which is to be determined.

The interface to channel function latches provides for the addressing of groups of latches and transferring data to those latches. The latches control the following functions:

a) Connection of drivers and/or receivers to UUT
b) Connection of digital or analog control to drive buffers
c) Selecting and routing clock, delay, APG signals
d) Routing data flow between local memory and other elements

The interface to reference voltage DACs provides for the

addressing of groups of latches and transferring data to those latches. The latches control the reference DACs which serve as reference values for digital drive and receive and for analog functions such as indicating voltage crossings to be utilized for frequency measurements.

The interface to analog filter latches provides for the addressing of groups of latches and transferring data to those latches. These latches select the extent of filtering accomplished during analog stimulus generation.

The interface to local memory routing latches provides for the addressing and transfer of data to groups of latches. These latches control the connection between the microcontroller and local memory of individual pin channels. These connections are required for loading and retrieving data.

12.2 DETAILED FUNCTIONAL REQUIREMENTS, 8 CHANNEL CONTROL PROGRAM

Requirements for the following three functions are provided below:

a) Setup pin channel functions

b) Calibrate delays, voltage, and filter values

c) Control data transfer with local pin channel memory

The setup pin channel functions program must accept commands and data from the interface to the backplane bus and setup the pin channel latches, the reference voltage DAC latches, and the analog filter latches according to the command requirements. It must also accept an interrupt from the backplane and disconnect all the pin channel drivers from the UUT interface. The input

shall be from the interface to the backplane bus. Data transferred on it consists of a pin channel address, a command, and data bytes appropriate to the command. Also provided through the interface to the backplane bus is an interrupt which signals that reset of all the pin channels is to be carried out. The program shall carry out any activities (handshaking) required to receive the data from the backplane. It shall interpret the commands and format data for transfer to the function latches. Where appropriate, it should make use of the offset and filter calibration operations described below. It shall carry out any activities required to set the appropriate latches. The output shall consist of data which sets the appropriate latches. In case of errors in data transfer, it shall also consist of a signal to the backplane of an error condition.

The calibrate delays, voltage, and filter values program must accept from the backplane parameters for delay offsets, voltage offsets, and filter offsets for calibrating pin channels. It must utilize this data in interpreting backplane setup commands for controlling the board. The inputs are from the interface to the backplane bus. Certain of the commands received through that interface include data describing the extent to which a pin channel is out of calibration with respect to time, voltage, or filtering. Other data contains the specific values to which the reference voltages and filter are to be set. This data is input to the offset calculation function. On receiving calibration data, the program must compute the actual values to be used based on the hardware characteristics of the 8 channel pin electronics board. For time offsets, the data is immediately sent to the

appropriate latches. For voltage and filter offset, this data is used in the computation of the actual data bytes to be sent to the latches. The output shall consist of data which sets the appropriate delay, DAC, or filter latches. In case of errors in data transfer, it shall also consist of a signal to the backplane of an error condition.

The control data transfer with local pin channel memory program must accept and process commands for transferring data between the local memory of a pin channel and the backplane. It must setup the proper connection between the local memory and itself. It must then effect the data transfer requested. In some cases, this transfer may require simple data processing to reduce the amount of data which must be transferred. There are three types of inputs from two interfaces. The first input is a command input. It is sent from the backplane and describes what data transfer is to be accomplished. The second data input is the data sent by the backplane to be entered into the local memory of a pin channel. The third data input is from the local memory or error log of a pin channel which is to be transferred to the backplane. There are two processing steps. The first step is the interpretation of the command to setup a link with the local memory of a particular pin channel. Since the local memory for a single pin channel can contain over 32,567 bits of data, the microcontroller cannot address all of them simultaneously. Thus it must set latches which connect it to one particular local memory. The second step depends on the command. If the command was to transfer data from the backplane to the local memory, then data is read through the interface to the backplane bus and

stored in the local memory. The data is used by the digital driver circuits the digital receiver circuits, or the DACs for analog driving. If the command was to return data from the local memory to the backplane, the microprocessor writes bytes from the local memory to the interface to the backplane bus. This data has been entered into local memory by the A/D converter or it is from the functional digital error log. The following simple data analyses are examples of what will be accomplished when required by the backplane command:

a) Find smallest or largest value of voltage read by receiver A/Ds
b) Find value read at a particular clock time by the receiver A/Ds
c) Find times when the read voltage values crossed a particular value in a particular direction.

There are three main types of output. The first type of output is data sent to the latches which connect or disconnect the microcontroller to a particular local memory. The second type of output is data which is entered into the local memory of a pin channel. The third type of output is data sent to the backplane from the local memory of a pin channel.

The 8 channel control program shall have an error recovery capability which alerts the backplane to the error, but will not monopolize the backplane bus in relating this message. The program shall be easily tailored to support pin electronic 8 channel boards of different capacities, voltage ranges, slew rates, etc. The program has complete and sole control of the microcontroller

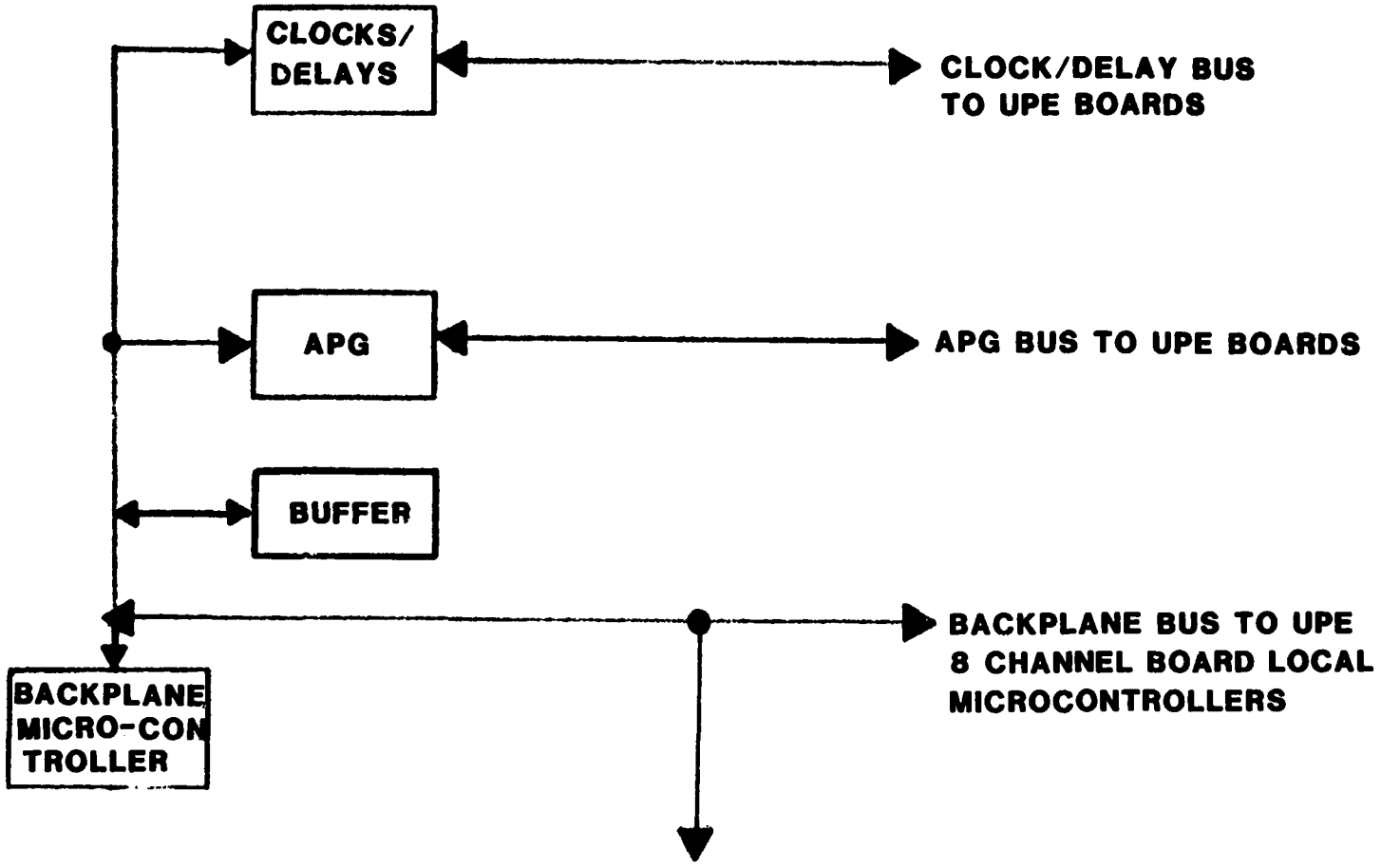
on a pin electronics 8 channel board. It implements only those commands which can be carried out on that particular board. These particular capabilities are inherent in the hardware including: the amount of local memory, the voltage range of the drivers and receivers, the slew rate of the drivers, and the granularity of choices in either voltage or filters. The normal range of possibilities for an 8 channel board capability shall be easily indicated to the computer program by changes to its parameters. These parameters shall include:

a) The existence of the functions associated with each channel function latch
b) The range and coding of the reference DACs
c) The range and coding of the analog filter
d) The size of local memory for a pin channel

12.3 PROGRAM DEFINITION, BACKPLANE CONTROL PROGRAM

The purpose of the backplane control program is to accomplish tasks including the following:

a) Accept input from the user or tester, error check the commands, and interpret them
b) Translate user or test station commands into a sequence of commands to the pin electronics 8 channel boards
c) Translate user or test station commands into latch bits which setup the pin electronics clocks and delay lines
d) Translate user or test station commands into data loaded on the pin electronics algorithmic pattern generator
e) Read data from the pin electronics 8 channel board, do



INTERFACE BLOCK DIAGRAM
BACKPLANE MICROCONTROLLER
FIGURE 12-2

appropriate analyses on the data and transmit results to the user or test station

This program is intended to be executed on a microprocessor incorporated in the pin electronics backplane device. It will be the only program executing on that microprocessor. It shall be referred to as the backplane microcontroller. It must interface with the various items on this board as described in the following subparagraphs. The backplane microprocessor software must control the interface hardware of the pin electronics backplane, accept and process data input from these interfaces, and prepare and output through them. The hardware interfaces include:

a) Interface to user or test station control bus
b) Backplane bus interface to the 8 channel boards
c) Interface to pin electronics clock and delay hardware
d) Interface to pin electronics algorithmic generator hardware

Each interface consists of a piece of hardware on the microcontroller bus. Each interface has its own bus address, and command and control sequence.

The interface bus to user or test station provides for the serial transfer of bytes of data both to and from the user or test station. It includes an interrupt mechanism for signaling test completion and pin electronics device error. The data is transferred according to a format which is to be determined.

The interface bus to 8 channel boards provides for the serial transfer of bytes of data both to and from the 8 channel boards. It includes an interrupt mechanism for signaling reset

and test operation complete. The data is transferred according to a format which is to be determined.

The interface to clock and delays latches provides for the addressing of groups of latches and transferring data to those latches. These latches control synchronization, repetition rate, delay, and burst count of pulses made available to the pin electronics 8 channel boards during test execution.

The interface to algorithmic pattern generator (APG) proviues for the addressing of memory and groups of latches and the transfer of data to them. These memories and latches control the operation of the pin electronics algorithmic pattern generator.

12.4 DETAILED FUNCTIONAL REQUIREMENTS, BACKPLANE CONTROL PROGRAM

Requirements for the following 4 functions are provided below:

a) Setup pin electronics 8 channel boards
b) Setup pin electronics clocks and delays
c) Setup pin electronics algorithmic generator
d) Prepare and return measurement data to user or test station

The setup pin electronics 8 channel boards program must accept commands and data from the interface to the user or test station, address the appropriate 8 channel boards, and format data to properly setup those boards for testing. It must recognize errors in the input commands and inform the user or test station of that error. The input shall be from the interface to the user or test station. Data transferred on it consists of commands, pin channel descriptions, and data for use in testing

on a pin channel. The program shall carry out any activities (handshaking) required to receive data from the user or test station. It shall interpret the commands, determine to which 8 channel board(s) it applies, and reformat the data for transmission to that (those) board(s). It shall carry out any activities required to transmit the data to the 8 channel board(s). The output shall consist of data transmitted to the 8 channel boards and error messages to the user or test station. The data transmitted to the 8 channel board consists of a pin channel address, commands, and data bytes appropriate to the commands. Error messages to the user shall include a short, human-readable message. Since overall test time is drastically influenced by setup procedures, the transfer and processing of data between the main controller and the UPE must be optimized.

One example of the efficiency which must be built into the backplane data distribution software concerns bus type UUT testing. Bidirectional control of an entire 8 or 16 busses is most often a common pattern. It is wasteful from a time standpoint to transfer this repetitive data 8 or 16 times. Instead it will be stored and transmitted via the I/O bus only once and the backplane microprocessor will distribute it to the appropriate 8 or 16 channels.

The setup pin electronics clocks and delays program must accept data from the user or test station and setup the pin electronic clocks and delays. It must also start clock execution, recognize completion of test execution, and where appropriate initiate preparation and transmittal of data to the user. The input shall be from the interface to the user or test station.

Data transferred through it shall consist of commands, identification of clock channels, and data bytes appropriate to the command. The program shall carry out any activities (handshaking) required to receive data from the user or test station. It shall interpret the commands, determine to which clock channel it applies, and reformat the data for setting up or activating the clock channel as appropriate. If the command requires, the program shall monitor the pin electronics clocks and either signal the user or test station or initiate preparation of the data for transmittal to the user. The output shall consist of data which sets the appropriate clock latches. In the case of errors in test execution, it shall also consist of messages transmitted to the user or test station.

The setup pin electronics algorithmic pattern generator program must accept data from the user or test station and setup the pin electronic algorithmic pattern generator. It must recognize errors in the input commands and inform the user or test station of that error. The input shall be from the interface to the user or test station. Data transferred through it shall consist of commands, algorithm configuration data, and pattern data. The program shall carry out any activities (handshaking) required to receive data from the user or test station. It shall interpret the commands, and reformat the data for transmission to the memory and latches of the algorithmic pattern generator. It shall carry out any activities required to transmit the data. The output shall consist of data transmitted to the algorithmic pattern generator memories and latches and of error messages to the user or test station. Error messages to the user shall

include a short, human-readable message.

The prepare and return measurement data program must accept data from the user or test station and based on embedded commands retrieve data from the 8 channel boards, prepare it for transmission to the user or test station, and transmit it. In some cases, this function must be automatically invoked at the end of test execution. There are two types of input. The first type of input shall be from the interface to the user or test station. Data transferred through it shall consist of commands, identification of clock channels, and data bytes appropriate to the command. The second type of input is from the pin electronics 8 channel boards. It consists of one or more of the following:

a) The test step times at which digital errors occurred (error log)
b) The digital bit stream read for specific test steps
c) The voltage values read on a pin at specific step times
d) The largest and/or smallest voltage value read on a pin channel
e) The step times at which the monitored voltage on a pin crossed a setup trip value

There are two processing steps. The first processing step is the interpretation and execution of that portion of the command which indicates on which 8 channel boards the data exists, and how it should be retrieved. During this step, individual 8 channel boards are addressed and appropriate data is read into the backplane microprocessor memory. The second processing step is the interpretation and execution of that portion of the user

or test station command which indicates the data processing of the test data and the format in which the results are to be returned to the user or test station. This step is completed when all the data requested by the user or test station is transmitted from the pin electronics.

The output shall consist of data transmitted to the 8 channel boards, data transmitted to the user or test station, and error messages sent to the user or test station. The data transmitted to the 8 channel board consists of a pin channel address, commands, and data bytes appropriate to retrieve data developed during a test. Data transmitted to the user shall be one of the following IEEE Std ATLAS types:

a) Rise-Time
b) Fall-Time
c) Pulse-Width
d) DC Voltage
e) Peak Voltage
f) RMS Voltage
g) Frequency
h) Period
i) Delay
j) Phase Shift
k) Events
l) Functional Digital Test Data

Error messages to the user shall include a short, human-readable message.

The backplane control program shall be easily tailored to

support the different numbers of pins and different capabilities of different pin electronics hardware configurations. The program has complete and sole control of the microprocessor on the pin electronics backplane. It must implement only those commands which can be carried out by the specific pin electronics device on which it resides. These particular capabilities are inherent in the hardware and include:

a) Number of pin channels

b) Depth of pin channel local memory

c) Digital and analog capabilities

d) Voltage and frequency range boundaries

e) Algorithmic pattern generator capabilities

The normal range of capabilities for a pin electronics channel shall be easily indicated to the program by changing values in a table describing each pin channel. The program shall be able to support a pin electronics device with its full complement of pin channels and its full functional capability.

SECTION XIII

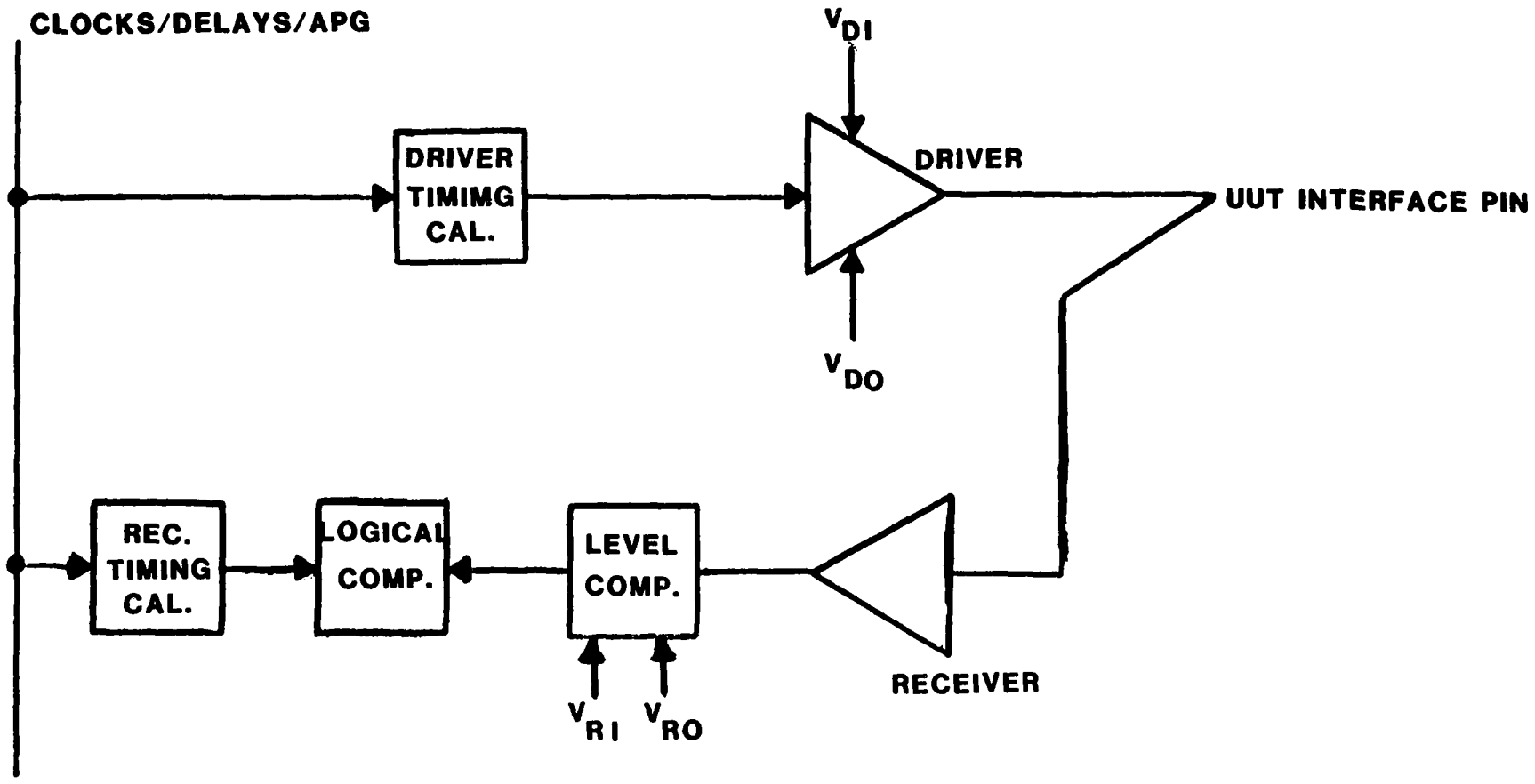
13. CALIBRATION SUBSYSTEM

13.1 Functional Description

Each channel of UPE is calibrated under program control by automatic deskewing networks to effect time calibration and automatic voltage networks to effect voltage calibration. As opposed to manual procedures, automatic calibration can be performed continually so that a high degree of confidence can be maintained with regard to the integrity of test results. Small adjustments can be made automatically as needed to insure accuracy. If by chance a channel drifts beyond the calibration range, an interrupt is generated to alert the test system operator.

The automatic calibration system is effected by the local microcontroller to ensure accuracy across all pins. Calibration is accomplished automatically with the same connection setup as is used for testing which eliminates operator error and possible handling damage during calibration (refer to Figure 13-1).

There is a variable delay circuit in both the UPE driver and receiver. For timing calibration purposes the test system contains a standard or reference receiver. The drivers are switched one at a time into this standard receiver via a path which includes the entire driver channel. Each driver is in turn programmed to generate a transition and the strobe time on the standard receiver is varied under program control to detect the transition. The strobe time is recorded for all driver channels by the UPE microcontroller. The absolute value of these delays is not the most important fact but the relative values are if skew



CALIBRATION SIGNAL FLOW

FIGURE 13-1

is to be eliminated. The microcontroller compares all values and adjusts out of spec channels until all are within tolerance. The procedure is then rerun to prove compliance.

After all UPE drivers are calibrated, they are utilized to calibrate their respective receivers. Each driver is connected to its receiver and programmed to effect a level transition. The strobe on each receiver is varied under program control to determine where in time the transition is detected. The microcontroller then scans a table into which all these values have been entered. Any channels out of tolerance are trimmed by their variable delays. Finally the entire procedure is rerun as a final check.

There is a 16 bit A/D converter for each block of channels which is used for highly accurate UUT measurements. This device is also utilized for automatic voltage calibration. Under program control, UPE driver levels are set to specific voltage values and switched in turn into the 16 bit A/D. The voltage values read by the A/D are compared by the microcontroller to the programmed values in all cases. Where the levels are found to be out of tolerance, a correction factor is logged in a memory location assigned to each level generator for each pin. Thereafter, whenever that generator is addressed under program control, the calibration factor is utilized to correct its output.

After the drivers have been voltage calibrated, they are utilized to calibrate their respective receivers. Each driver is connected to its respective receiver and is varied through a specific set of levels. The receiver reference levels are varied to determine their voltage compliance. Any connection factors

necessary are logged by the microcontroller into memory locations associated with that specific receiver.

13.2 CALIBRATION SPECIFICATION

The voltage calibration shall ensure the voltage accuracies stated in this document are achieved by automatic means and without the use of external equipment.

The timing calibration shall ensure the timing accuracies stated in this document are achieved by automatic means and without the use of external equipment.

13.3 SELF-TEST

Self-test provided in the universal pin electronics determines if the UPE chassis is operational. Self-test is provided at two levels. Specifically, a confidence test and a diagnostics test are provided. Both can be initiated via the main controller. Status information and results are read back via the I/O bus. The confidence test and diagnostic self-test perform similar test sequences in that both exercise the UPE to determine operational capability. The more general confidence test provides operational status. The diagnostic self-test takes operational status monitoring one step further in that it isolates a non-operational condition to a replaceable sub-assembly in the UPE chassis.

The confidence test and diagnostic self-test check the UPE in the following sequence. First, the backplane microcontroller and its associated circuitry are checked. If proper operation is attained at that level, the test sequences to the individual pin electronics assemblies starting with the local microcontrollers, clock circuitry, DAC circuitry, memory, driver/receiver

circuitry, etc. In this manner, a logical diagnostic approach assures fault isolation in the most efficient manner. It is expected that the confidence test can be run in less than 1 minute. An estimate of the duration of diagnostic self-test would be 1 to 10 minutes depending on the nature of the failure. In addition to self-test, the UPE chassis can be provided with on-line test capabilities which constantly monitor the readiness of the device and detect catastrophic failures. Operational readiness of power supplies, clock oscillators, temperature, and other critical elements can be continuously monitored. Interrupts to the main controller would flag any malfunctions.

SECTION XIV

14. FAULT ISOLATION SUBSYSTEM

14.1 FUNCTIONAL DESCRIPTION

There are two major approaches to fault isolation namely the guided probe/clip and the fault signature/fault dictionary. The guided probe works through interaction with the test system operator directing the placement of a special sensor (probe) on a given point on the UUT or a multi-point probe (clip) on a given IC. Data from the probed points are analyzed by the probe software to determine if a match exists with "good board" data obtained by a simulator or ATG package or learned from an actual UUT. The comparison determines if other points should be probed or if the source of the UUT's failure has been located. Once the failure has been located, the operator is informed as to its location in hard and/or soft copy.

Fault dictionaries are typically constructed as a result of a logic simulation run. For each simulated fault, a test step where the failure is first detected and the input/output pin states that differ from the "good machine" are stored in the dictionary file. Any failures detected during the actual circuit test cause the test system to search the dictionary for a match at the failed test step and matching failed output pins.

If the actual failure modes are restricted to simulated faults, this technique works well. However, the actual failure mode possibilities are too many to be practically considered or simulated; therefore, the possibility exists that a board fault will be encountered where no dictionary match exists. In

overcoming this problem, UPE software will supplment the dictionary look-up scheme with the guided-probe fault isolation technique. The guided-probe logic is invoked to further isolate the fault after the dictionary search has been exhausted. If the initial search narrows the fault to an internal ambiguity group, the probe can begin at this point thus saving the time to probe from the edge connector.

The guided probe requires two pieces of information to begin namely the circuit interconnect and IC reference data. The circuit interconnect is merely a list of all UUT components and a list of all interconnections between these components. The IC reference data consists of the logic values expected to occur at every node for each step in the test program. These two pieces of data are usually obtained via ATG based or interactive simulator based software. If these data bases are not available the following software will create them:

- Circuit processor. The programmer describes the IC's and components on his board as well as their interconnects in a convenient manner. The UPE circuit processor interprets this input and builds the necessary data base.

- UUT Learner. The operator is asked to probe all points on the circuit while the test program is run on a known good UUT. This data is catalogued to form the IC reference data.

The guided probe uses state of the art techniques to find, in an efficient and accurate manner a path from a faulty external pin through levels of IC's to the source of the failure. It correctly handles difficult situations such as wired nodes, large

bus nodes, and complex feedback loops.

The guided probe function is implemented by utilizing a normal channel of UPE, a physical probe and a cable to connect the probe to the UPE channel (Figure 14-1). The operator moves the probe to UUT nodal points as directed by the operating software and the nodal data is captured by the UPE channel. For the more efficient guided clip, multiple channels are used. The clip is placed over the IC on the UUT and 8, 16, 24, 40 or any appropriate number of points are monitored simultaneously. A cable carries the data back to a like number of channels of UPE. The electrical characteristics of the probe or clip and cable maintain signal integrity between the UUT and the UPE channel or channels.

In some instances simulators or ATG software are not utilized in the TPS preparation processs. In these cases the so-called "learn mode" must be utilized in order to capture the nodal data required by the guided probe/clip. In this process the GO/NOGO input vectors are applied to the UUT by the UPE and at the same time it records UUT outputs and internal nodal data. No logical comparison is made but rather the absolute data from the UUT output pins and nodes is captured by the UPE channel or channels. The data is grouped into 16 bit words, buffered, and written into the local UPE memory. When the memory is filled, the data is sent back to the main controller for utilization by the guided probe software.

Even at 100MHz rates the local memory is more than fast enough to record the data since the 16 bit wide data word effectively provides a considerable factor of safety. Only absolute

GUIDED PROBE/CLIP SIGNAL FLOW

FIGURE 14-1

data is recorded; no attempt will be made to compact in real-time. Thus, up to 32K bits can be recorded per pin in real-time before the local memory must unload back to the main controller.

14.2 FAULT ISOLATION SPECIFICATION

Maximum IC Pin Count	128
Maximum Board IC Count	1024
Maximum Test Program Step Count	1,000,000

In addition, the probe/clip shall have the following capabilities:

a) Single pin/IC clip optimization. Separate algorithms are enabled during single pin probe or clip use. During clip operation, the probe algorithm looks for the earliest failure present on the device which has just been probed. This allows it to jump over several levels of logic and quickly diagnose the failure. During single pin operation, however, it is more efficient to probe just those IC pins related to a particular failure, rather than the entire IC. Both the single pin probe and IC clip may be utilized during the probing of a given UUT.

b) Multi-level bus breakdown. LSI bus oriented logic often contains large bus nodes to which many devices may be attached. Classical probing techniques call for all inputs of an IC on the bus to be probed before going on to the next IC on the bus. This process would take a long time if done with a single point probe. The UPE probe allows for up to four levels of input pin priority designation. These levels are used to distinquish important pins (such as chip enables) from less important ones (data lines for example). The probe algorithm investigates all "most important"

pins on all IC's first before looking at pins at the next level. This allows it, for example, to probe all chip enable pins first for IC's attached to a bus node and to trace back on any errors found on those pins.

c) Infinite re-try. When probing, an operator may incorrectly place the probe, slip off the probe point, or disturb the board's normal operation. Through the use of the re-try feature this problem is eliminated.

d) Four state data reference. The IC reference data may have one of four values for each node and step: 0 (logical zero), 1 (logical one), D (tri-state disconnect), and U (an unknown masked value). The D state is invaluable in diagnosing problems on today's microprocessor busses. The U state is mandatory in handling flip-flops and other memory devices which are not initialized until some point in the test program; a U value keeps the probe software from incorrectly judging a good/bad condition.

e) No-probed nodes. Due to circuit operation and physical construction, various points on a UUT may not be probed without either affecting circuit performance or physically damaging the UUT. The programmer may specify any number of points in his circuit description to be "no-probed". The probe software, instead of asking the operator to probe such nodes, considers it "potentially" faulty. If no other source of failure is encountered, then the no-probed node is diagnosed as the source of the failure.

f) Reference verification. Reference data may originate from an off-line source such as an ATG. In any case, an important

step in UUT checkout is to verify the IC reference data against a known good UUT. The probe has a special mode which will direct the operator to probe every pin of every IC and verify the reference data for that pin.

g) Operator directed probing. As the ATE operator gains experience at testing a particular board type, he may be able to anticipate the source of the board's problem. The UPE software allows the operator to direct the probe to look at any point on a board; if that point is bad, the probe will continue tracking from it. If that point is good, then the probe software will go back to what it was previously doing. Through the use of this feature the operator provides "intuition" while the software provides the exhaustive input routine.

h) Programmer directed probing. The "intuition" developed by the operator in the last paragraph can be systematized by the board programmer in the form of "start" and "jump" points. "Start" points tell the probe where to begin probing if the test program fails in one way or another. This is analogous to the fault dictionary lookup guiding the initial probe placement, but more general in that the programmer may program any conjunction of events. "Jump" points are merely the programmer's equivalent of operator director probing; he merely indicates to the probe software that when it reaches point A, it should try points B, C, D, etc.

i) Data type mixing. The probe has the capability of dealing with two types of IC reference data. The four-state data mentioned earlier allows the probe to work with maximum accuracy. In particular, most feedback loops cannot be broken without it. In

cases where this data is not available or is too large, the UPE probe can work with less accurate data such as signatures based on CRC's (Cyclic Redundancy Check). If both types of data are present the probe uses the less accurate but faster data and switches to the fully accurate data when it encounters a feedback loop.

SECTION XV

15. CONCLUSIONS

In the early 1970s, the ATE industry saw the rapid emergence of exciting new hardware capability such as high speed digital word generator/receivers, flexible switching systems, etc. ATE software designers also produced significant new tools such as ATLAS compilers, simulators, guided probes, etc. Since that time little new technology has been developed to help the test community in its attempt to keep up with the ever upward thrust of the semiconductor industry. The UPE concept represents the first significant breakthrough in ATE technology in well over ten years.

The current effort has proven the feasibility of the universal pin electronics concept. Functional digital, analog, and parametric digital stimulus and measurement capability can be effected in a channel of test electronics. Other features identified during the program include:

a) Functional digital frequencies to 100MHz

b) Analog and parametric digital frequencies to 20 MHz

c) Vector depths in excess of 250,000

d) Individual voltage programmability of the logic levels on each input and output pin for functional digital testing

e) Real-time bidirectional control of drivers and real-time masking of receivers

f) Real-time selection of multiple clocks/delays

g) Real-time multiplexing of algorithmic pattern generators on each pin

h) Fault signature and guided probe/clip diagnostic capability

i) Self-contained voltage and timing calibration

j) Modular subsetting capability

This report is clearly intended to drive the state of the art. Although all capabilities described herein are believed technologically feasible at this date, various practical implementations might utilize only a partial subset of the described capabilities. As the state of the art in semiconductors advances, the flexible UPE structure will allow its test parameters to be moved forward accordingly.

The UPE concept has the promise of being able to radically alter the field of ATE which has been relatively stationary for almost 10 years. It has the potential for widespread use in both military and commercial applications. Its compact size yet extensive test capability make it usable in a wide variety of test situations (e.g. it is small enough to be used as a portable field tester and yet powerful enough to be used in intermediate and depot level applications). Eventually its cost should drop significantly as the yield on UPE chips/modules increases with expanded use.

The scope of the UPE has been drastically increased with the inclusion of built-in test applications in addition to ATE. Some of the reasons UPE appears to have such high potential for BIT include:

a) Increased test capability and reliability

b) Technological capability to accommodate the most modern

prime systems

c) Reduced, size, weight, and cost

d) Equal effectiveness on analog and digital systems

e) Ability to filter false alarms to increase user confidence

f) Reduction in off-line ATE requirements

g) Maximized compatibility with off-line ATE

UPE holds enormous potential for a truly cost-effective test implementation, whether as BIT or off-line ATE. In the ATE arena, its broad test capability will eliminate the need for much of the expensive stimulus/measurement instrumentation typical in today's testers. It will also eliminate much of the costly switching normally required. Interface devices will be drastically simplified. In the BIT application, its combined analog/digital test capability will greatly reduce the BIT circuitry normally utilized. Its small size and modest weight will also be extremely effective. Since it relies so heavily on LSI techniques for its implementation, UPE will be able to reap the downward cost curve with time and volume so typical of semiconductor devices.

SECTION XVI

16.0 RECOMMENDATIONS

Given the results of the study effort, as delineated in this report, it is appropriate to move UPE from the conceptual stage to the development stage. A phased development plan can allow the concept to be carefully monitored in this new phase. A multiple channel brassboard is recommended with at least two and preferably four channels. Partial clock/delay capability is also necessary. Appropriate operating software development should parallel the hardware effort. No attempt should be made at reducing the design to its final LSI and hybrid form until the brassboard proves the overall feasibility.

Although no specific high-order language has been specified for the UPE, it is likely that ATLAS will be the prime candidate. To this point care has been taken that nothing in the UPE development precludes the use of ATLAS. The evolution of the ATLAS language must be monitored carefully to maintain UPE compatibility.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