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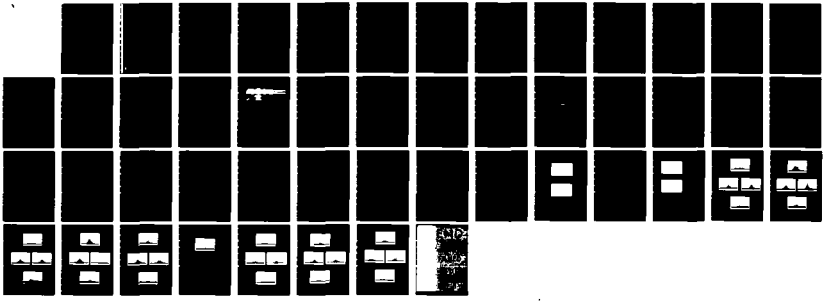

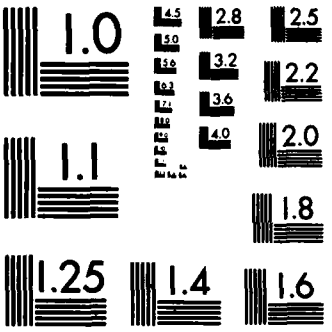

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FET FREQUENCY DISCRIMINATOR

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March 1982

FINAL REPORT
for the period 20 April 1977 to 31 December 1981

Naval Electronic Systems Command
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The FET Frequency Discriminator is an experimental microwave frequency discriminator developed for use in a specialized set-on VCO frequency memory system. Additional development and evaluation work has been done during this program to more fully determine the applicability of the FET frequency discriminator as a low-cost, expendable receiver front-end for both surveillance and ECM systems.

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Various methods for adjusting the frequency-to-voltage characteristic of the discriminator as well as the effects of detector characteristics and ambient temperature changes were evaluated. A number of discriminators for use in the 7- to 11-GHz and the 11- to 18-GHz bands were fabricated and tested. Interim breadboard and final packaged models were either delivered or installed in developmental frequency systems. The major limitations and deficiencies of the FET frequency discriminator that were reviewed during the program include the effects of temperature, input power level variations, nonlinearity, and component repeatability. Additional effort will be required to advance the developmental status of the FET frequency discriminator to the level necessary for inclusion in low-cost receiver systems, but the basic simplicity of the approach continues to show much promise.

PREFACE

This final report was prepared at RCA Laboratories, Princeton, New Jersey, under a modification to Contract No. N00039-76-C-0280. The report describes the work performed on various FET frequency discriminators for use in frequency memory systems for ECM applications. Various tasks for the program were worked on from May 1977 through December 1981 at the RCA Laboratories Microwave Technology Center under the direction of Dr. F. Sterzer. The project engineer was D. D. Mawhinney under the supervision of M. Nowogrodzki, Head of the Microwave Subsystems Group.

The author wishes to express his appreciation for the excellent technical assistance provided by H. Milgazo on the overall program and for the guidance from Mr. Nowogrodzki and technical advice in areas related to ECM functions and applications from H. Wolkstein. The assistance of A. Rosen and E. Mykietyn in areas related to fabrication and adjustment of the discriminators was especially valuable to the program.

The author also gratefully acknowledges the technical support and guidance, particularly in the areas of existing and future system requirements, provided by T. Timberlake of NESC which was of particular help to the program.

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SECTION I

INTRODUCTION

RCA Laboratories has been actively engaged in the development of VCO Frequency Memory Systems for use in electronic countermeasure (ECM) applications. The basic type of system which has been under development involves the use of a microwave discriminator to provide a frequency-dependent voltage to first open-loop tune the VCO and then to serve as a reference for correction of set-on and memory errors in a feedback loop. The microwave discriminator is an essential and critical component in the system.

During the course of this work, RCA Laboratories, under the sponsorship of the Naval Electronic Systems Command, developed a new type of wideband microwave frequency discriminator that is particularly well adapted to the function of providing the reference for a VCO frequency memory system. The simplicity of this new type of discriminator may eventually result in a small and low-cost device suitable as a high-speed receiver for expendable surveillance and countermeasures systems.

The discriminator consists of an FET amplifier stage and a diode detector with a minimal amount of associated circuitry to produce an analog voltage uniquely and - as an objective - linearly related to an input frequency. In its simplest form, the natural high-frequency roll-off characteristic of the GaAs FET provides a signal to the detector diode that diminishes in amplitude as the frequency increases. The ideal arrangement of an FET and a diode directly connected with no other circuitry cannot be realized because of the need for input and output connections, bias lines and chokes, and bypass and blocking capacitors, but the ideal can be closely approached with a very small circuit in which there are no lines long enough to cause the nonlinearities and ripples that are common in the transfer characteristics of interferometer-type discriminators. Furthermore, the leading and trailing edge errors due to the transit time differential of the two path lengths of the interferometer do not exist in the FET discriminator in which the rise and fall time limitations are a function only of the detector diode and the load capacitance. Another advantage of the FET frequency discriminator is the FET amplification factor which for the same given input signal produces a larger output signal from the detector than a passive interferometer does. The larger the discriminator output

voltage, the smaller is the amount of video amplification needed to tune the VCO and the faster it can be set on to the incoming frequency.

There are also disadvantages to the application of the FET frequency discriminator, and one of the tasks of this program was to study these and consider means to lessen the resulting consequences. Among these disadvantages are lack of device-to-device uniformity, nonlinearity, temperature sensitivity, and dependency upon input power level. The general objective of this program was to continue the development effort and to work toward improvement in the performance of the FET discriminator for low-cost expendable and frequency set-on and surveillance applications. Specifically, the program was to include effort on the following items:

(1) Development of improved frequency-to-voltage conversion linearity for the discriminator.

(2) Improvements in the integration techniques for supporting the FET amplifier and detector diodes on the same substrate.

(3) Optimized matching methods used between active and passive interconnected elements.

(4) Determination of temperature sensitivities and compensation techniques to enable operation in an airborne environment.

(5) Determination of early life linearity changes and voltage output stability to minimize aging effects.

(6) Implementation of cost reduction techniques wherever possible.

Since this program was a continuation of earlier effort involving the use of FET discriminators in VCO frequency memory systems and was performed concurrently with another contract amendment for a 7- to 11-GHz memory system, most of the FET discriminator evaluation involved system tests in this frequency range. The specific objective tasks of this program are listed in the following work statement for Item 0005 of the modified contract.

WORK STATEMENT
FET MICROWAVE DISCRIMINATOR

1. Review deficiencies inherent in the prototype FET discriminator delivered to NESC. Verify areas requiring improvement against specifications for front-end and/or expendable receiver applications.

2. Improve frequency-to-voltage conversion linearity. Optimize matching methods and integration techniques. Utilize computer-aided design techniques to optimize circuit topology to obtain conversion slope and response required.
3. Fabricate, evaluate, and deliver one (1) interim discriminator model.
4. Determine temperature and aging effects on the stability of the discriminator conversion characteristics. Implement temperature compensation controls.
5. Optimize multiple detector-to-circuit match. Determine optimum circuit biasing techniques.
6. Finalize integrated substrate and packaging design.
7. Build, test, and evaluate final discriminator models.
8. Deliver two (2) final models of the packaged discriminator.
9. Deliver bimonthly reports in the course of the program.
10. Deliver a final report at the completion of the program.

SECTION II

TECHNICAL DISCUSSION

A. DISCRIMINATOR FUNCTION AND REQUIREMENTS

The general function of any frequency discriminator is to convert an FM signal into an AM waveform suitable for further processing. In the case of typical FM communications signals, the absolute carrier frequency is not a part of the transmitted information, and the only constraint is that it is properly adjusted and stabilized for the specific communications channel or converted frequency being used. For applications such as identification and categorization of unknown incoming signals, the absolute frequency-to-voltage conversion characteristic of the frequency discriminator is significant and depending upon the specific system - may be the limiting factor in the accuracy of the system.

In an open-loop set-on VCO type of frequency memory system, such as the system shown by the block diagram of Fig. 1, the output of the frequency discriminator is used to electronically tune the VCO to the same frequency as the incoming signal. There probably will be video amplifiers to increase the voltage swing to the level required by the VCO to cover the required range, and linearizers may be necessary to match the frequency-to-voltage characteristics of the discriminator to the voltage-to-frequency tuning curve of the VCO. Since there is basically a direct connection from the input discriminator to the output VCO, the accuracy and stability of the frequency discriminator, as well as the VCO and other components, determine the overall input to output system error.

In the Locked-Open-Loop Voltage-Controlled Oscillator Frequency Memory System (LOL-VCO-FMS) approach, the impracticality of basing a system on the open loop accuracy and stability of the frequency discriminator, VCO, and other components has been recognized, and two major features have been added to improve the initial set-on and long-term memory errors. As shown by Fig. 2, the block diagram of the 8- to 10-GHz LOL-VCO-FMS which was delivered prior to this program, a sample of the incoming frequency is used to injection-lock the VCO to precisely the input frequency when the open-loop tuning drives the VCO close enough to this frequency to be within the locking range. Times as short

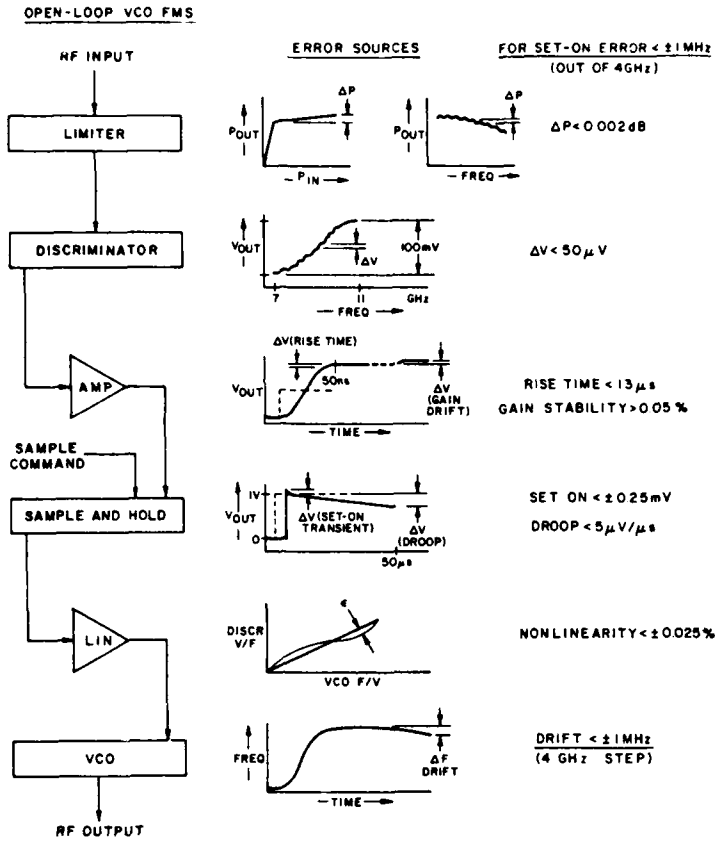


Figure 1. Open-loop set-on VCO-FMS and error sources.

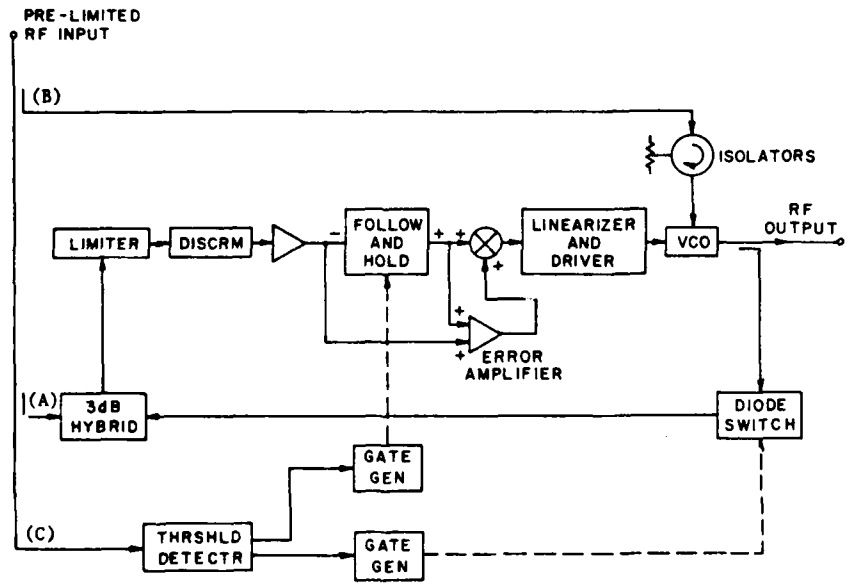


Figure 2. Modified LOL-VCO-FMS block diagram.

as 50 ns have been demonstrated as adequate to achieve this type of VCO set-on which became of little value in the frequency memory system that resulted after the system was modified from a dual-discriminator approach to the simplified arrangement of Fig. 2. The more significant new feature which differentiates the LOL-VCO-FMS from the basic open-loop set-on VCO frequency memory is the use of a feedback correction signal in which the discriminator provides a measure of the real-time VCO frequency for comparison of the discriminator output which was stored during the time the unknown input signal was present. In this arrangement, the long-term accuracy and stability requirements of the frequency discriminator are reduced because, ideally, the VCO is tuned by the feedback circuit to eliminate any open-loop error by equalizing the real-time discriminator output to the stored output from the same discriminator. As long as there is no change in the discriminator during the microsecond to millisecond intervals of interest, a residual error approaching zero is fully realizable.

Of course, some limitations do remain in obtaining this low input-to-output frequency error. Most important are the speed at which the error correction can take place and the amount of error that can be corrected. Both of these depend upon the gain and response of the feedback loop and upon the magnitude of the initial open-loop error of the system. The smaller the open-loop error, the less feedback gain will be required for a given final error and, in general, the faster the corrections will take place.

The effects of absolute accuracy (the initial maximum difference between input and output frequency at a specific delay time across the frequency band at the time the system is aligned and calibrated) and stability (the same error a period of time after the calibration) must be considered separately because the discriminator characteristics affect each differently. With ideal amplifiers and linearizers it should be possible to closely match any frequency discriminator characteristic to any VCO tuning curve, but response time requirements make it necessary to limit the overall gain and the number of linearizer breakpoints. Calculations have shown that if an open-loop time constant of 50 ns is assumed, a marginally adequate system response time could be obtainable with feedback gain as large as 50 (34 dB). For a ±1-MHz residual error from this one cause, the maximum open-loop error should not exceed ±50 MHz. The number of linearizer breakpoints is limited for practical reasons to about ten, and the linearizer design is constrained by selection of a circuit design and

components consistent with the 50-ns time constant. These constraints, in turn, make it essential that the discriminator have a smooth transfer characteristic without reversals, which would cause three different frequencies to produce the same output voltage, or sharp discontinuities, which would cause regions of very high open-loop gain and system instabilities. For a nominal open-loop gain of no more than ten, the voltage swing out of the frequency discriminator should be an the order of 0.5 to 1.0 V since the VCOs used in various systems will probably require from 5 to 10 V to cover the full frequency range. Finally, it has been demonstrated (see Appendix) that in a practical system requiring replacement of defective components such as a discriminator or a VCO, direct matching of frequency-voltage characteristics is difficult and both should have been initially adjusted against a normalized linear specification.

Stability requirements involve an understanding of the effect of changes once the initial calibrations or adjustments have been made and the system is exposed to operation for extended periods over a range of typical environmental conditions. In the direct open-loop set-on VCO frequency memory all changes due to drift or temperature translate directly into operating errors. In the LOL-VCO-FMS, the changes in discriminator or VCO characteristics are reduced by the feedback gain of the correction circuit so that the residual error is much smaller; however, the initial set-on error, before onset of the correction process, is directly affected. If an additional ±0.5-MHz error is allowed for the system after settling, an additional ±25-MHz drift error can be allowed for the discriminator and VCO for the same 34-dB feedback gain condition. The magnitude of this allowable error is such that temperature control of the discriminator and VCO is essential.

In summary, the requirements for the frequency discriminator for use in an LOC-VOC-FMS are:

Input Frequency Bandwidth:	2 to 4 GHz (approximately)
Output Signal for Full Band:	0.5 V minimum
Rise Time:	20 ns maximum
Linearity:	±50 MHz of straight line
Reversals:	None
Fine Grain Slope Variation:	Approx. 4:1 maximum
Variation with Temperature:	Voltage equivalent to ±25 MHz maximum

B. REVIEW OF FET FREQUENCY DISCRIMINATOR - OPERATION AND DEFICIENCIES

One of the specific tasks of the contract work statement requires a review of the inherent deficiencies of the prototype FET frequency discriminators and consideration of the degree of improvement required to permit such devices to be practical for the front-end of expendable receiver or ECM systems. In such systems, requirements for frequency identification and separation are added to the standard receiver functions of signal interception and detection. With the well-known interception probability limitations of swept YIG or superheterodyne receivers and the large size and high-cost penalties associated with present day channelized receivers, effort has been directed to the development and improvement of high-speed, wideband frequency discriminator devices capable of nanosecond response to short microwave pulses from interrogating search or tracking radars. As a result, the passive phase interferometer has been put to use as an instantaneous frequency measurement (IFM) subsystem in many types of receiver applications.

Generic long-short line IFM devices (as shown in Fig. 3) operate by splitting a preleveled rf signal into two unequal path lengths and then recombining and detecting the resulting phase-displaced signals to produce an analog voltage output which is a function of input frequency. Although advanced IFM interferometers have been designed recently using MIC techniques for reducing line length and minimizing fine grain structure due to interconnections and other error-producing nonlinearities, these devices still suffer from mismatches and imbalances in the dual-line circuit causing periodic ripples and discrete discontinuities in the band.

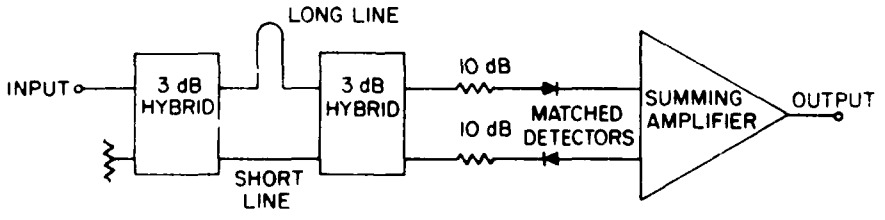


Figure 3. Long-line/short-line pulse Interferometer Frequency Discriminator.

For adequate frequency resolution, e.g., ±1 MHz in an overall frequency coverage of 4 GHz, the input rf power variations across the band must be restricted to a fraction of a dB, and the incidental power reflections and mismatches due to the passive components must be equally minimized. This requires that the components of the frequency discriminator for each of the differential path lengths, hybrids, and crystal detectors be selected and matched. Mismatches less than 1.05:1 are required to provide the frequency resolution and accuracy cited. Measurements have shown that the magnitude of the discontinuities and ripples obtained from a specially developed MIC dual-line interferometer - although a 3-1 improvement over the use of discrete components - still produces a nonlinear frequency error equivalent to ±50 MHz on the 7- to 11-GHz band. This error is excessive for many receiver applications.

In an earlier phase of this contract, RCA demonstrated a new approach for achieving frequency discrimination for IFM and receiver front-end applications on a device development program funded by NESC. This frequency discriminator used an active microwave field effect transistor (FET) in conjunction with a simple circuit topology arrangement and a detector diode to achieve a monotonic voltage output relatively proportional to rf frequency input. Figure 4 illustrates this active FET discriminator and compares it to a discrete component dual-line interferometer. This prototype discriminator was fabricated using an RCA GaAs MESFET chip that had the capability of providing 250-mW rf power output in X-band and, as shown by the network analyzer data of Table 1, with a typical gain capability of 6 dB at 7 GHz. With an input matching stub, it was simple to obtain a gain contour that monotonically decreased as a function of increasing frequency. This FET amplifier was flip-chip mounted on a ceramic substrate that also supported the rf input and output circuitry. A beam-lead Schottky diode, integrated on the same substrate, was used for output voltage detection. This diode, which was isolated from the FET drain circuit by a ceramic chip blocking capacitor, was forward biased at the proper operating point through an appropriate dropping resistor and rf choke arrangement.

The known or presumed deficiencies of this prototype FET frequency discriminator include sensitivity to input and environmental conditions as described below.

Figure 4. Comparison of the conventional interferometer discriminator and the FET discriminator.

TABLE 1. NETWORK ANALYZER DATA

FREQ	11		21		12		22	
7000.0	0.832	172	0.945	21	0.061	-9	0.526	-97
7500.0	0.848	151	0.983	3	0.068	-23	0.508	-121
8000.0	0.851	140	0.851	-13	0.063	-37	0.539	-149
8500.0	0.859	141	0.705	-24	0.054	-46	0.610	-167
9000.0	0.844	146	0.589	-29	0.048	-48	0.635	-173
9500.0	0.831	151	0.556	-34	0.047	-47	0.637	-175
10000.0	0.814	150	0.558	-37	0.053	-44	0.662	-170

FREQ	H21	S21	G1	G2	GMAX	U	K
7000.0	-0.5	-0.5	5.1	1.4	6.0	0.11	1.77
7500.0	1.8	-0.2	5.5	1.3	6.7	0.14	1.33
8000.0	3.8	-1.4	5.6	1.5	5.7	0.13	1.51
8500.0	5.1	-3.0	5.8	2.0	4.8	0.12	1.80
9000.0	4.7	-4.6	5.4	2.2	3.1	0.09	2.71
9500.0	4.4	-5.1	5.1	2.3	2.2	0.07	3.26
10000.0	4.6	-5.1	4.7	2.5	2.2	0.08	2.98

1. Input Power Level

Since this type of frequency discriminator is intended to provide a signal output proportional to frequency, the level of the input signal must be held absolutely constant. For the prototype design, there is no means of reducing this sensitivity by AGC, differential, or comparison techniques so that variations in input level are translated into frequency errors. For a 4-GHz bandwidth system, a ±0.1-dB input power variation from the calibrated norm would produce an apparent frequency error of ±46 MHz at midband with a maximum error of ±92 MHz at the high end of the band. Clearly, an input power limiter is required with a flatness on the order of ±0.01 dB to keep frequency errors from this cause below ±10 MHz. To lessen this sensitivity, a differential arrangement - preferably with logarithmic sensitivities - involving two discriminators should be considered. Another potential means of reducing but not eliminating this sensitivity is to use a sample of the input level to change the gain of the discriminator postamplifier as a precalibrated open-loop correction. Such a circuit would need a very fast response to track the discriminator rise and fall times.

2. Input Match and Discontinuities

The connection between the input limiter and the FET frequency discriminator is quite critical because of the high sensitivity of the FET frequency discriminator to power level variations. Since a connector VSWR of 1.1:1 would result in a mismatch loss of about 0.01 dB, a ±10-MHz frequency error would occur between a perfectly matched discriminator and limiter pair. With any mismatch in either or both, the frequency error will vary widely as the mismatches add or subtract with phase and frequency. The effect of long transmission lines will be to reduce the frequency difference between summing peaks and nulling valleys and the resulting discriminator voltage vs frequency characteristic will develop a substantial ripple - possibly violating the required voltage uniqueness required for any given input frequency. The only solution to this type of deficiency is to make sure the mismatches are below 1.05:1 and that all transmission and coupling line lengths are absolutely minimized.

3. Sensitivity to Environmental Variations

Since the FET and the detector diode are inherently susceptible to bias current variations with temperature, the dc output voltage must be expected to change with temperature. Operating the discriminator in a temperature-controlled environment will probably be a prerequisite to its use in a temperature-varying environment. Over a limited range, it may be possible to compensate the discriminator by varying the input bias conditions or the gain and offset of the postamplifier. This would be done on an individual basis and would require repeated temperature testing. Some form of built-in calibration using two or three known frequency sources is another possible means of correcting for discriminator sensitivity to temperature. The small size and minimal weight of the FET frequency discriminator structure should make it fairly immune to other environmental stresses such as shock and vibration.

C. DETECTOR DIODE

The function of the diode detector is to convert the rf signal into a dc voltage level. Since most of the frequency discrimination will be provided by the shaped gain of the FET amplifier, the frequency response of the detector should be nominally flat although a gradual decrease in sensitivity with increasing frequency would be acceptable. Most important is the need for an interconnection between the FET amplifier and the detector diode that is free of discontinuities and VSWR ripple producing transmission lines. Since a low reflection coefficient match would be difficult to obtain between the amplifier and detector over a wide band, as direct an interconnection as possible without transmission line matching elements is preferable. It is necessary, however, to block the drain voltage from the detector and to bring in a diode bias voltage for maximum sensitivity and for one means of electronic control of the discriminator characteristic. A schematic representation of the FET frequency discriminator is shown in Fig. 5.

To implement a method for optimizing the match of the detector diode to the FET amplifier, three different techniques have been evaluated. The first one was the typical chip tuning of the interconnecting line between the FET and the diode. The desirable short length of this line does not leave much room for positioning the small chip, but some effect can be observed and the shape of the discriminator characteristic can be varied slightly. This is not an adjustment technique that gives predictable results.

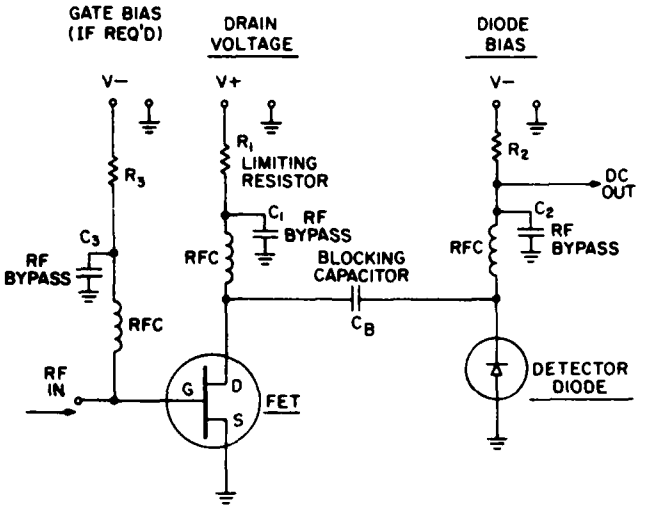


Figure 5. FET frequency discriminator schematic.

A somewhat better means of varying the detector characteristic is to adjust the diode bias voltage and the series current limiting resistor (R2). With either of these variables, the current through the diode can be adjusted to change the effective impedance of the diode to some degree. The size of the series resistor changes the output video impedance of the detector since it is effectively in parallel with the diode video impedance. The response time will be adversely affected if the time constant (R_2C_2) becomes too large. To keep the rise time of the detected pulse such that the pulse will be within 0.025% (1 MHz out of 4 GHz) of full value in 10 ns requires a time constant of 1.2 ns. For a bypass capacitance (C_2) of 25 pF, a total effective resistance of approximately 50-Ω maximum resistance is required without considering the effective capacitance of the diode itself. The typical effect of detector diode bias on the output of an FET discriminator is shown in Fig. 6.

The third technique considered for adjusting the diode characteristics was the use of a diode structure consisting of a large number of available diode elements in which the specific number used could be selected for optimum amplitude or linearity. To test this method, diode chips (a 7x7 matrix of diodes on a single chip) were ordered from NEC* (ND5K2C). Although the bonding

*Nippon Electric Co., Tokyo, Japan.

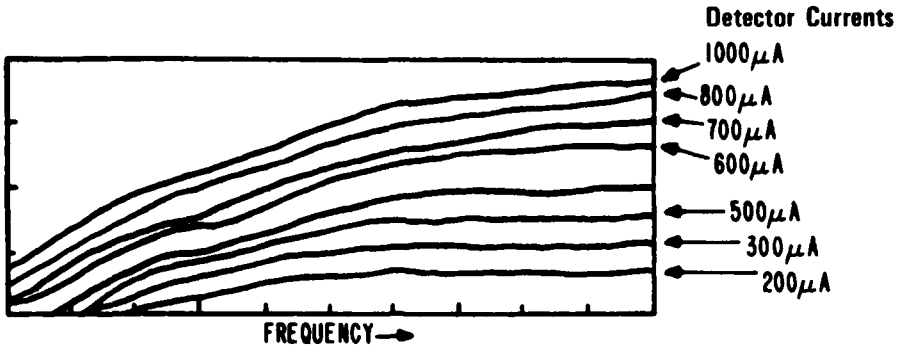


Figure 6. Effect of detector bias on FET discriminator output characteristic.

area of each diode is only 0.0005 in. diameter, it was possible to wire-bond to 5 of the approximately 49 diodes and to connect them in parallel to a metallized ceramic (5 mil thick/10 mil wide) substrate in order to measure the microwave frequency impedance for various numbers of diodes in parallel. The purpose was to measure how the detector impedance would vary with the number of diodes operating to determine if the detector array, with each diode separately biased and individually controllable, could function as a linearizer with diodes coming into conduction at different output levels from the FET stage.

Figure 7 shows the impedance plot obtained for three and two diodes connected in parallel and a single diode with current levels of approximately 130 μA each in a reasonably even division of current among the diodes. The real part of the impedance is quite low - less than 5 Ω - and the series bonding inductance and diode (and stray) capacitance resonate at approximately 5 GHz for the three diodes in parallel and 7.5 GHz for the single diode. It was not possible to discern the change in the real part of the impedance with the number of diodes because of the small load resistance level.

Figure 8 shows the variation of impedance of a single diode as a function of current (100 to 160 μA). There is a decided shift in the real part of the impedance in this case with little change in the reactance.

In the preceding tests, because of the physical structure of the diode array, it was necessary to bias all the chips in parallel and assume uniformity for the desired equal division of current. Since the results obtained did not allow for the accurate determination of the change in impedance, additional

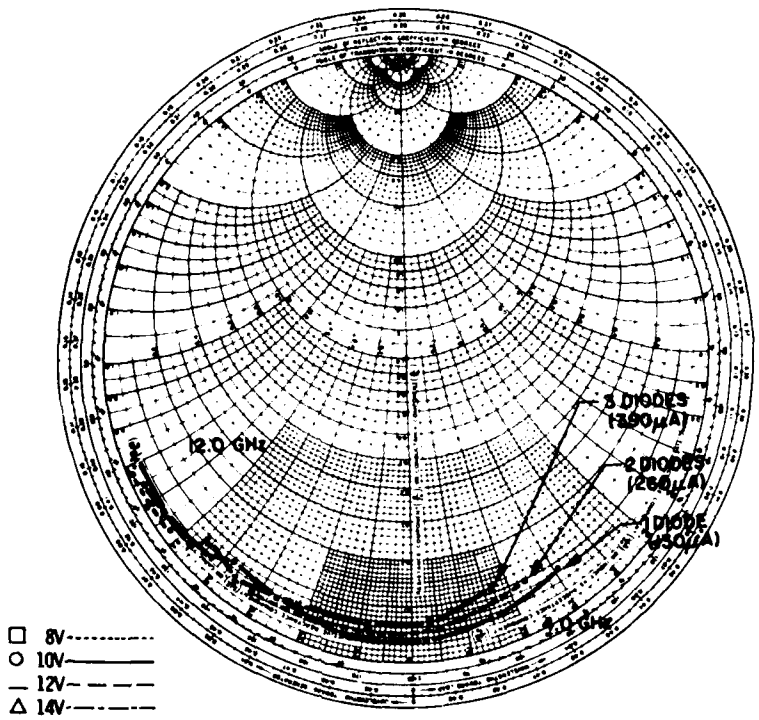


Figure 7. Impedance plot for three and two diodes in parallel and a single diode.

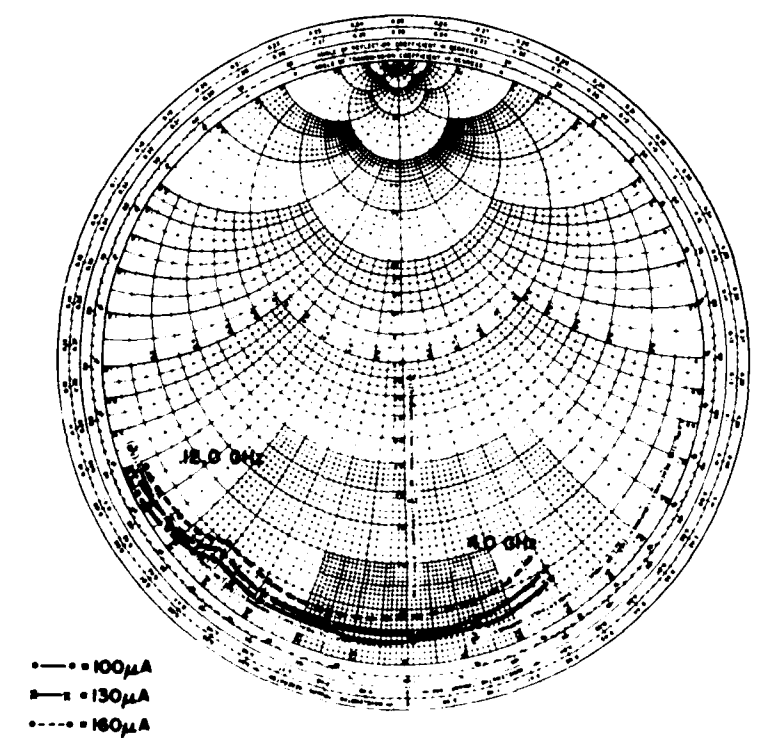


Figure 8. Impedance plot for a single diode as a function of current.

measurements were made with both the multiple diode array and a packaged device of the same type at various current levels. These impedance plots are shown in Figs. 9, 10, and 11; they are measurements of the following:

Fig. 9 - The multiple diode array with five diodes in parallel with the total current set to 78.5 μA and 540 μA.

Fig. 10 - The multiple diode array with four, three, and two diodes connected with the current adjusted so that each diode is biased at approximately 125 μA.

Fig. 11 - The packaged diode (one diode) operated at the same 125-μA bias level (approximately) and at 210 μA.

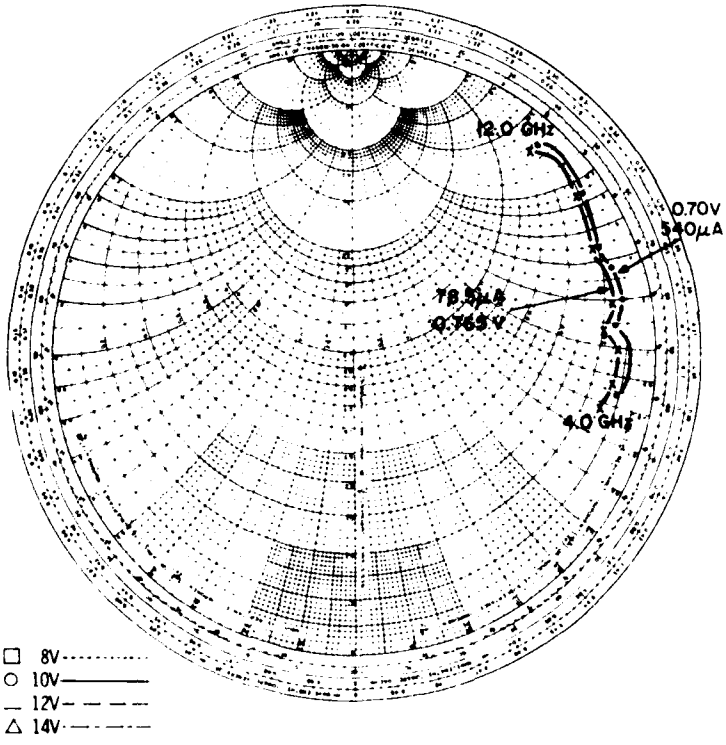


Figure 9. Impedance plot for five diodes in parallel.

A circuit was also fabricated to permit measurement of the HP 5082-0009 diode*, but we were unable to make adequate contact to this type of diode chip

*Hewlett-Packard, Palo Alto, CA.

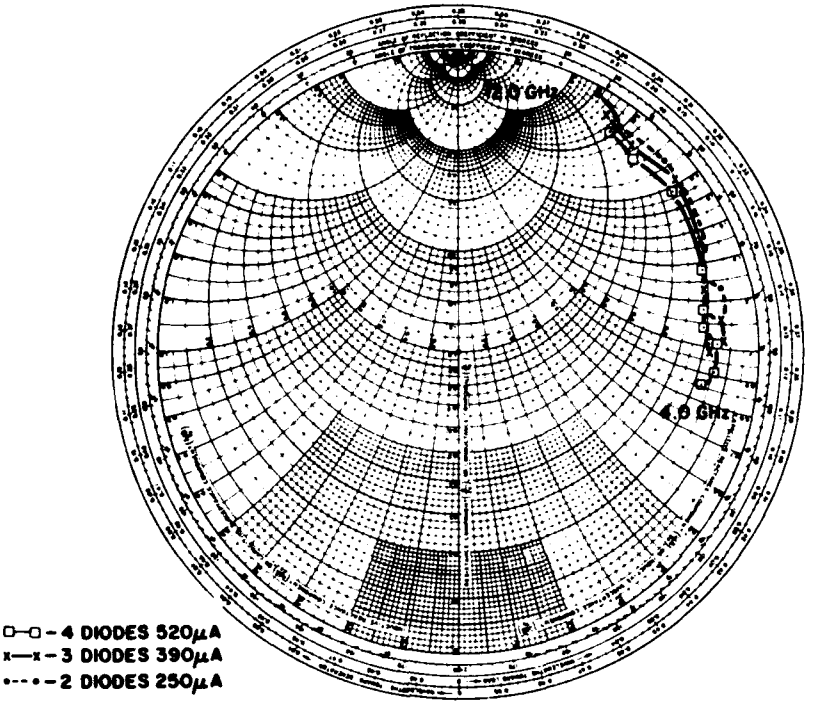


Figure 10. Impedance plots for four, three, and two diodes, each diode biased at ∿125 μA.

and measured an HP 5082-2217 (packaged) device instead. The results were comparable to those obtained with the NEC diodes. During the program, the circuits listed below were assembled and evaluated. As a general conclusion, the choice of detector had a relatively small effect upon the overall linearity.

(1) Discriminator circuit using a chip form of detector diode.

(2) Two discriminator circuits using packaged detector diodes (NEC) with a Johannson capacitor through the input 50-Ω line for tuning.

(3) Circuit to measure S-parameters of NEC detector diode in chip form.

(4) Circuit to measure S-parameters of NEC detector diode in packaged form.

(5) Circuit to measure S-parameters of HP diode in chip form.

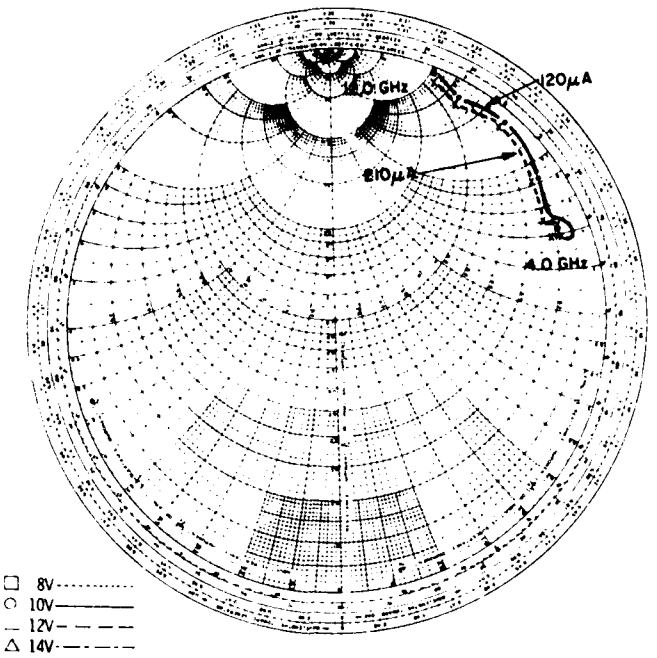


Figure 11. Impedance plot for one diode at 125 and 210 μA.

D. TEMPERATURE PERFORMANCE

The overall frequency discriminator essentially consists of the limiter, the FET device, and the detector diode. Since these are all semiconductor devices, it was to be expected that there would be significant offset changes with variations of temperature; however, the magnitude of the changes and the effect on the f/V transfer characteristic were not known.

One of the discriminators delivered during this program was tested at case temperatures of 28 and 70°C. The discriminator consisted of an RCA-fabricated 4-gate FET chip and a packaged NEC detector diode built on a ceramic substrate with suitable interconnection lines, blocking capacitors, and bias chokes. To eliminate the effect of the limiter, the discriminator was driven from a levelled sweep generator covering 7 to 11 GHz with an output of approximately -6 dBm. As may be seen from the plotted results (Fig. 12), at room temperature the f/V curve is reasonably uniform except for one major bump at 9.0 GHz. The output voltage swing is 0.37 V (-0.16 to -0.53 V) for a frequency swept from

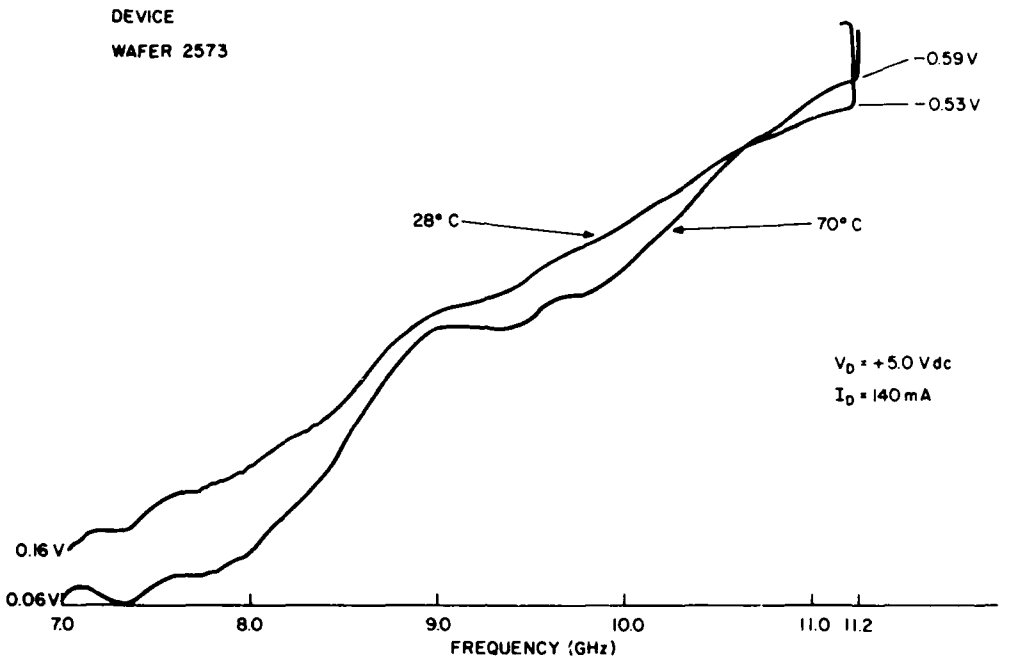


Figure 12. Temperature performance.

7.0 to 11.2 GHz. When the temperature was raised to 70°C, an increment of 42°C, the total swing changed to 0.53 V (-0.6 to -0.59 V). In addition, the shape of the curve changed in that the nonlinearities were accentuated.

From this test, it is obvious that any attempt at making absolute frequency readings from the discriminator would be unsuccessful unless the temperature was precisely controlled. The use of the discriminator in a system such as the feedback mode of the Locked-Open-Loop VCO Frequency Memory System, in which the discriminator voltage is used only to compare input and output frequencies, is practical because of the short memory time required during which time the temperature cannot significantly change. The overall calibration of the system and the ultimate accuracy require temperature stabilization of the limiter and discriminator - as well as of the VCO and any dc amplifiers in the tuning circuit or feedback loop.

E. INTERIM BREADBOARD MODEL

The interim breadboard model FET Frequency Discriminator delivered during this program consisted of an RCA 4-gate and an NEC-packaged detector diode

arranged on an alumina substrate. In addition to the voltage tuning provided by the FET gate and drain voltages and the detector diode bias current, ceramic chips were used to adjust the overall discriminator characteristic. The output voltage curve of the delivered model is shown in Fig. 13. An output voltage swing of almost 0.7 V was obtained with a frequency sweep from 7.0 to 11.2 GHz. The curve appears to be smooth and single-valued, but there are several bumps probably resulting from the levelled sweep oscillator input. A best-fit straight line drawn through this characteristic would show a maximum error of ±5% (±200 MHz out of 4 GHz). If a narrower bandwidth is considered, such as 9.2 to 11.0 GHz, a maximum linearity error of ±1.3% (±25 MHz out of 1.8 GHz) exists. There is no apparent fine grain error which would cause more than a ±10-MHz error.

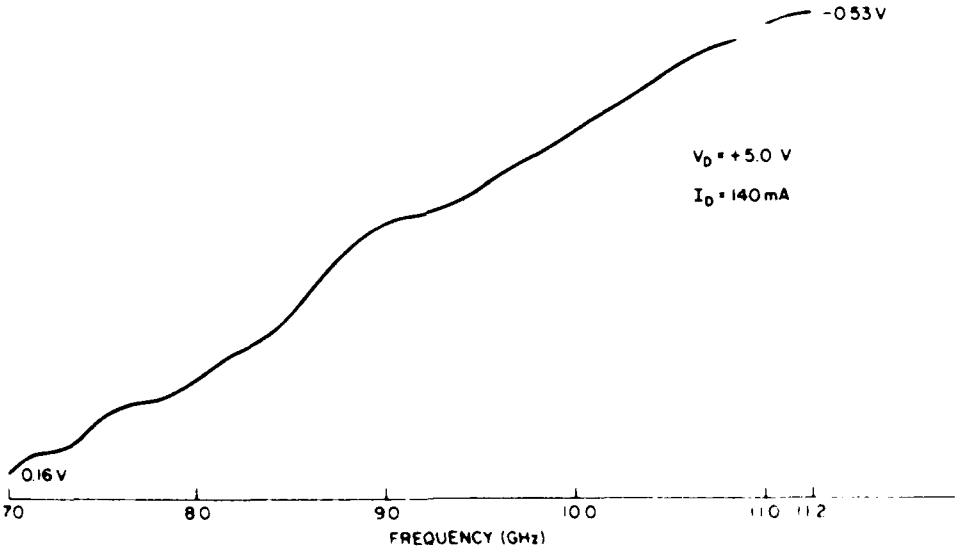


Figure 13. Output voltage vs input frequency of interim breadboard model.

The input level was approximately -6 dBm which is the level usually obtained from the TDA limiters. An isolator was provided with the delivered model so that reproducible results could be obtained when tested with a different generator, but a limiter was not included with this delivery.

E. 11- to 18-GHz FET FREQUENCY DISCRIMINATORS

In addition to the work done on 7- to 11-GHz FET frequency discriminators, some effort was applied to the fabrication and evaluation of discriminators for

use in a frequency memory system intended for operation over the full 11- to 18-GHz band. FETs specified to have usable gain over at least the lower half of the 11- to 18-GHz band were purchased from Dexcel and HP. The Dexcel chips tested poorly, but the HP devices worked reasonably well in the discriminator circuit. The same adjustment technique of varying the detector bias and drain supply voltages was used with the additional adjustment of gate bias. The f/V characteristic obtained with one of the HP devices is shown by the X-Y recorder plot of Fig. 14. The curve is exceptionally smooth and ripple-free and is single-valued throughout the 12.5- to 17.5-GHz range shown. An output voltage swing of only 100 mV was obtained, and the large slope variation would require the use of a linearizer with at least three breakpoints for reasonable f/V linearity.

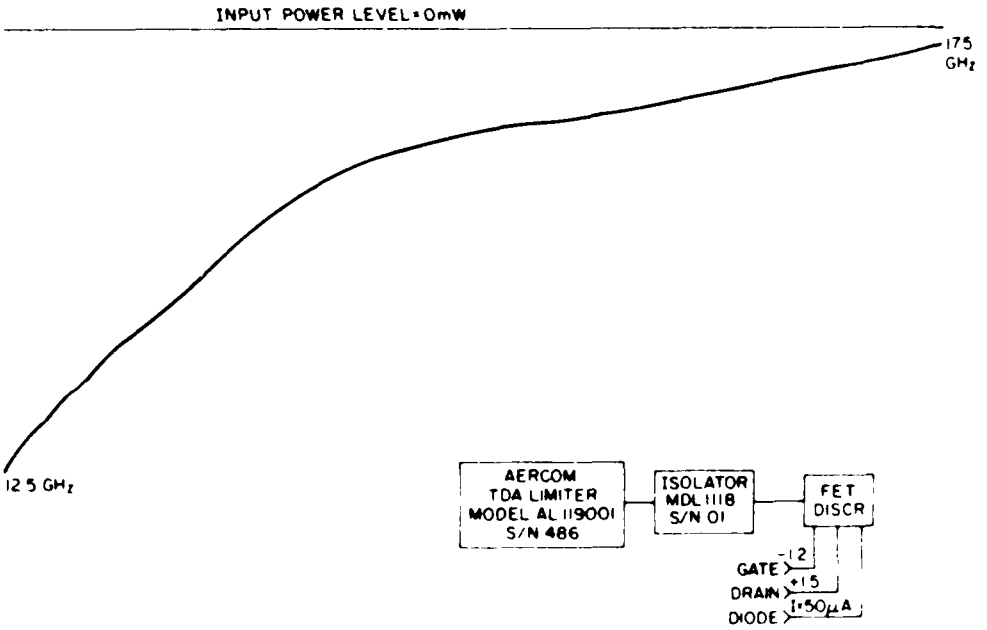


Figure 14. f/V characteristic of 11- to 18-GHz FET

A second 11- to 18-GHz frequency discriminator circuit was fabricated still using the HP FET and an NEC diode for the detector but with a longer input line to the FET gate to allow for some matching with a chip tuner. The basic schematic of this circuit is shown by Fig. 15.

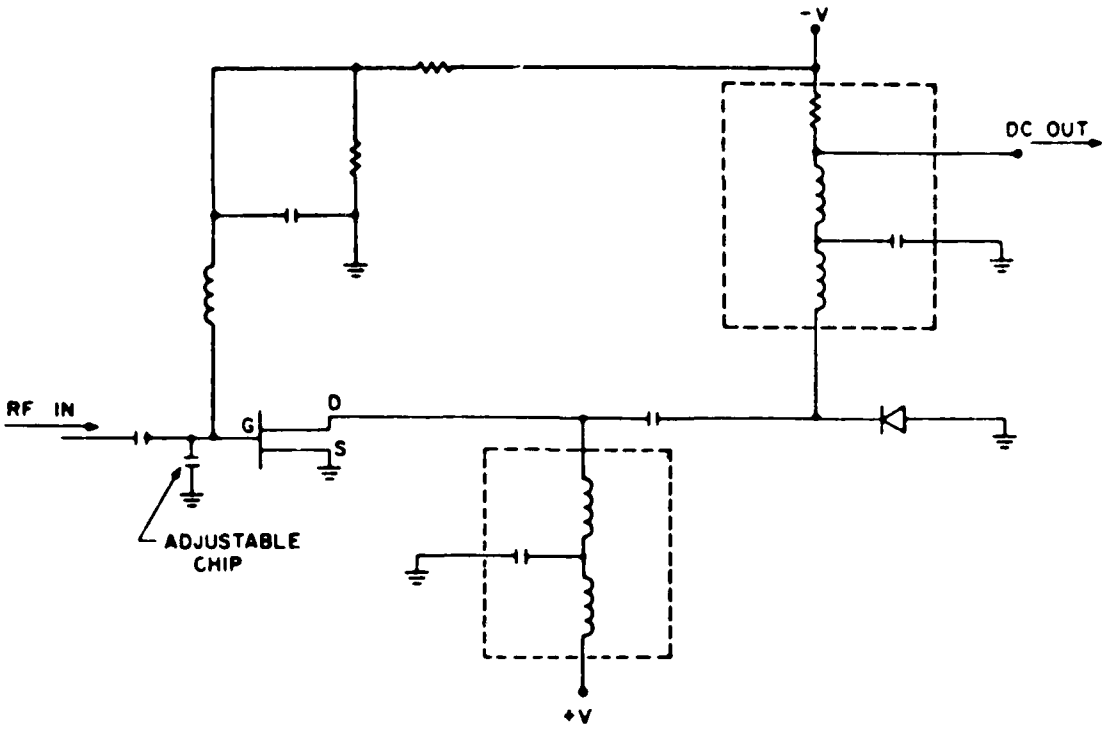


Figure 15. Schematic diagram of FET frequency discriminator output shaping circuit.

The 4-stage tunnel-diode amplifier type limiters were available for use in the discriminator assembly. The better of the two was selected, but the usable frequency range of the discriminator was substantially reduced by the nonuniformity of the output power vs frequency characteristic of the limiter. As shown in Fig. 16, the TDA limiter was tested alone and with two combinations of an additional isolator and adapters. The difference in the shape of the output curves among the three is relatively small, and the level difference can be accounted for by the attenuation of the isolator.

There is a variation of approximately 0.5 dB across the band that in itself would cause a frequency error (850 MHz out of the 2-GHz bandwidth) if there were no corrective capability afforded by tuning the FET discriminator. The rapid changes in the power output below 13 GHz and above 15.5 GHz limit the bandwidth of the discriminator substantially.

The overall discriminator output characteristic is shown by Fig. 17 with the input frequency range limited to 12.5 to 15 GHz over which the output

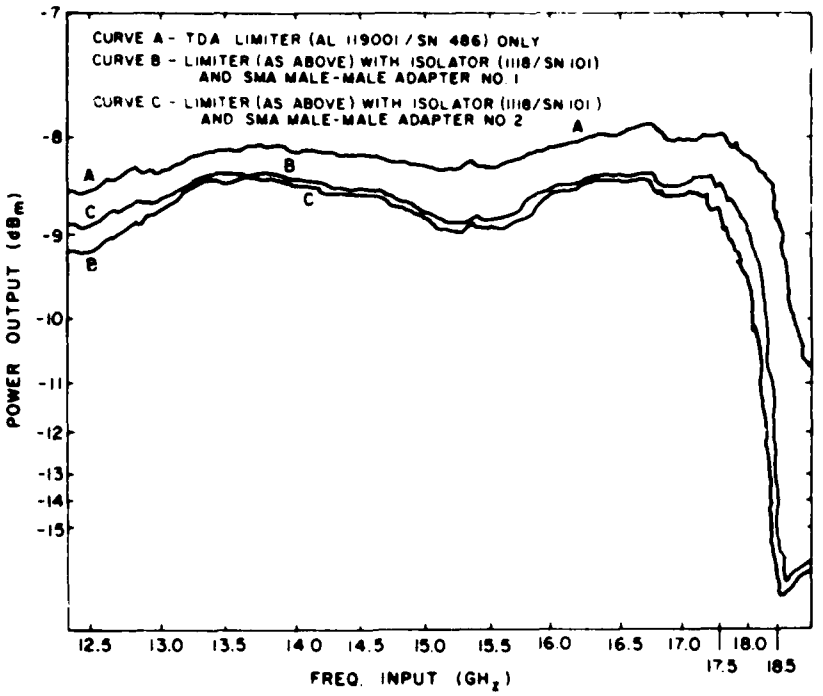


Figure 16. Limiter output test.

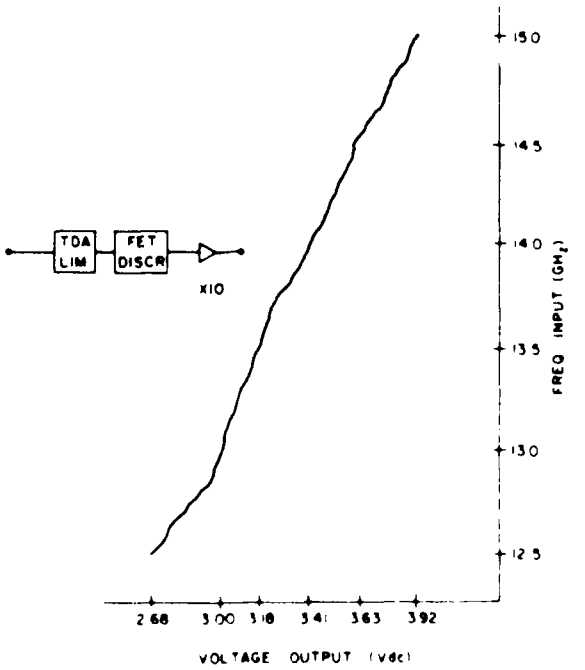


Figure 17. Frequency discriminator - low range.

characteristic is nominally linear and produces a total output voltage swing of 1.24 V. Over the extended frequency range of 12.5 to 17.5 GHz, as shown by Fig. 18, the output of the discriminator amplifier is 1.58 V but there is a significant departure from linear above 16 GHz.

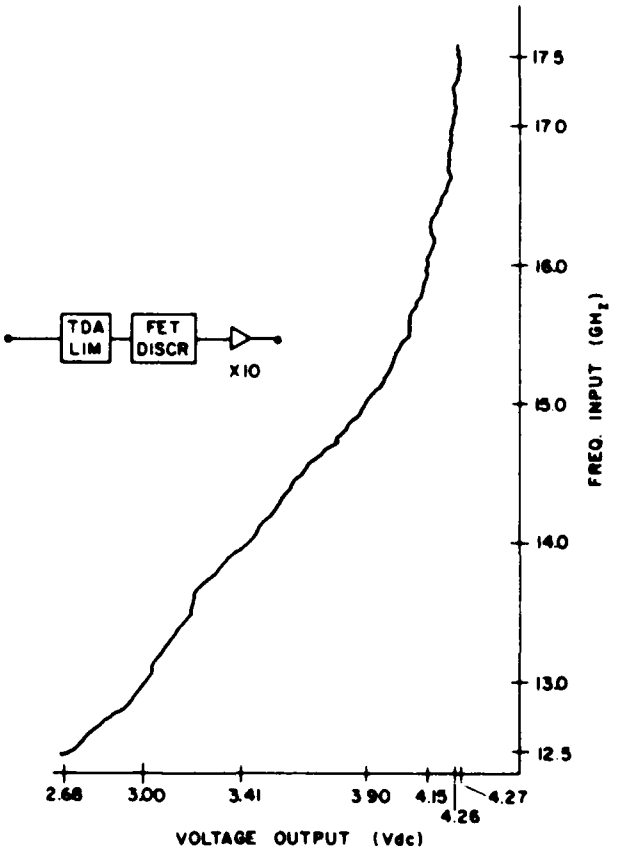


Figure 18. Frequency discriminator - high range.

This FET frequency discriminator was installed in a frequency memory system that was delivered as a part of the work on a program for a "Single Oscillator Wideband VCO" (Contract N00039-77-C-0271). The results obtained from the overall limiter-FET discriminator assembly were such as to limit the frequency coverage of the system to a bandwidth covering about 12.5 to 16 GHz. However, a relatively large voltage swing was obtained that required an amplification factor of only about 10 to tune the hyperabrupt varactor VCO over a comparable bandwidth. This was compatible with the set-on speed requirements of the system, and the linearity was adequate for direct tuning over the reduced bandwidth.

SECTION III

CONCLUSIONS AND RECOMMENDATIONS

The use of FET frequency discriminators as low-cost receiver front-ends in surveillance and ECM systems has considerable potential. The overall size and inherent simplicity are distinct advantages and the capability to operate over wide frequency ranges with fast response and reasonable accuracy has been shown. Remaining as the major obstacle to meeting the requirements of the low-cost receiver system applications is the need for an equally small and simple power limiter or an alternative.

All of the performance curves of the FET frequency discriminator evaluated during this program were degraded by the wideband fluctuations and fine-grain structure in the output power vs frequency characteristics of the TDA limiters used. At the start of the program, FET power limiters were not available as they now are. Further work using FET power limiters is warranted because these amplifiers do not require the large number of interstage isolators and circulators of negative resistance type amplifiers (TDA) and, therefore, should have much better fine-grain structure and flatter power output. Even more likely to produce the necessary size reduction and performance improvements would be an integrated FET amplifier/discriminator in which the frequency response of the last stage of the saturated amplifier including a detector would be properly shaped by tuning and bias adjustment. The total gain would, of course, depend upon the required input sensitivity.

Other techniques of reducing the dependency of the discriminator upon input power level and temperature need to be investigated further. Differential detector circuits, logarithmic amplification to permit ratio comparison, and circuits capable of operation equivalent to polar discriminators should be considered to reduce the power level dependency. Compensation and self-calibration techniques to diminish the effects of temperature variations on the accuracy of the FET frequency discriminator also need to be investigated.

APPENDIX

REPLACEMENT OF FET DISCRIMINATOR IN AN OPERATIONAL FREQUENCY MEMORY SYSTEM

The effect of replacing one FET discriminator with another set to cover the same band was evaluated during the repair of the original 8- to 10-GHz Locked-Open-Loop VCO Frequency Memory System. The FET discriminator, which had been installed in late 1976, was found to be inoperative as the system was being readied for some tests in early 1982. Evaluation of the problem showed that the unpackaged FET had degraded to the point where the output signal was only about one-third of the original amplitude.

The FET discriminator was removed and one of the discriminators delivered during this program was installed. When connected to the particular limiter of the system, the output frequency-to-voltage characteristic, which is shown by the photograph of Fig. A-1(a), was considerably more curved than that of the original FET discriminator for which the system had been optimized although the amplitude was more than sufficient. Readjustments of the detector diode bias and the FET drain voltage as well as some chip retuning of the input microstrip line resulted in a small improvement of the frequency-to-voltage characteristic as shown by the before and after double exposure photograph of Fig. A-1(b).

When the replacement FET discriminator was reinstalled in the 8- to 10-GHz frequency memory system, the resulting overall tracking accuracy between input and output frequencies was significantly poorer than originally measured. Even after the VCO linearizer was readjusted to provide somewhat better matching of the discriminator and VCO characteristics, a relatively large open-loop error remained. By reducing the usable bandwidth of the system to approximately a range of 8.0 to 9.7 GHz, the open-loop error was reduced to about 75 MHz - approximately double that obtained with the original discriminator. Our basic conclusion from this is that in order to consider the discriminator as a repairable component that can be removed and replaced, the discriminator assembly must be extended to include the limiter and an additional linearizer amplifier. The specification on the frequency-to-voltage conversion would have to be in terms of absolute linearity rather than matching a particular VCO which, in turn, would also be specified in terms of absolute linearity. The

discriminator assembly should also be contained within a separate temperature-controlled housing in order to better isolate its performance from external effects.

The results obtained from the repaired 8- to 10-GHz frequency memory system with the replacement FET discriminator are shown in sets of spectrum analyzer photographs in which a comparison of input and time-gated output frequencies is made at various times after the start of the short input pulse. The test equipment arrangement used for these measurements is shown by the block diagram of Fig. A-2. The microwave frequency input pulse is obtained by pulsing a high isolation PIN diode modulator to make a narrow rf input pulse from the cw output of a variable frequency X-band signal generator. The modulator, or its pulse driver, also produces a timing trigger for a variable delay pulse generator. The output pulse from this pulse generator is used to gate a PIN diode switch connected to the output of the frequency memory. Comparison of the input frequency represented by a narrow cw spectrum with the time-positionable, variable pulsewidth spectrum produced by the output PIN diode switch, provides a convenient picture of the error vs time performance of the frequency memory system.

The measurements were made at several input frequencies from 8.0 to 9.75 GHz and at three different delay times referenced to the start of the input pulse which was set to approximately 80 ns for all the tests. For the measurements at 300 ns and at 900 μs, photographs of the spectrum analyzer display were made only for the full noise-modulated condition. At 10 μs, photographs of the spectrum analyzer were taken with and without the FM noise modulation. The purpose of the noise modulation is to spread the output spectrum to cover the residual set-on and memory frequency errors. The width of the noise spectrum varies with frequency because of the nonlinearity of the VCO and discriminator characteristics.

To better describe the timing considerations of the measurements, reference is made to Figs. A-3(a) and (b). In both instances, the upper pulse is a detected sample of the PIN diode modulator generated input pulse that appears somewhat longer than the actual 80 ns to which it was set because of the response of the detector. The lower trace shows the drive pulse to the PIN diode switch which gates the output to the spectrum analyzer. The gate was set to a width of 200 ns for both conditions shown. In the first case the delay between the start of the input and the gate pulse was set to 300 ns so that the

spectrum analyzer display represents the frequency of the VCO in the 300- to 500-ns interval after the input pulse; in the second case the delay (only) was increased to change the sample time to 10 μs - equivalent to a false range of approximately +500 ft. No photographs were taken of the third test condition in which the delay was changed to 900 μs and, for improved visibility, the sample gate extended to 1.0 μs at a reduced PRF of 1000 pps to avoid overlap of the memory gate and pulse repetition interval.

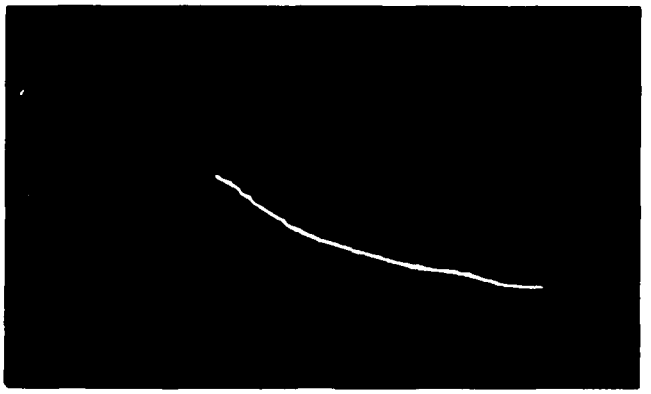
The input frequencies for the measurements and the respective series of photographs are as follows:

Figure	Input Frequency (GHz)
A-4	8.0
A-5	8.25
A-6	8.5
A-7	8.75
A-8 and A-9	9.0
A-10	9.25
A-11	9.5
A-12	9.75

For each set of spectrum analyzer photographs at a specific input frequency, the various test conditions were as follows:

Figure Letter	Test Condition	FM Noise
(a)	1	MAX
(b)	2	MAX
(c)	2	MIN
(d)	3	MAX

In general, this series of spectrum analyzer measurements shows that with the addition of some limited amount of FM noise modulation, the 8- to 10-GHz frequency memory system can store and retransmit a signal with a significant amount of energy in the presumed band of the interrogating radar although the replacement of the EEI discriminator resulted in a reduced accuracy for the system. The capabilities to work with a short input pulse, at least 50 ns or less, and to provide frequency storage for repetition rate type intervals, such as 1000 μs, are particularly impressive features of this basic system.



OUTPUT
VOLTAGE

APPROX.
0.5 V/DIV

(a) INITIAL

FREQUENCY
APPROX. 500 MHz/DIV

(b) AFTER ADDITION OF BIAS ADJUSTMENTS

Figure A-1. FET discrimination characteristics.

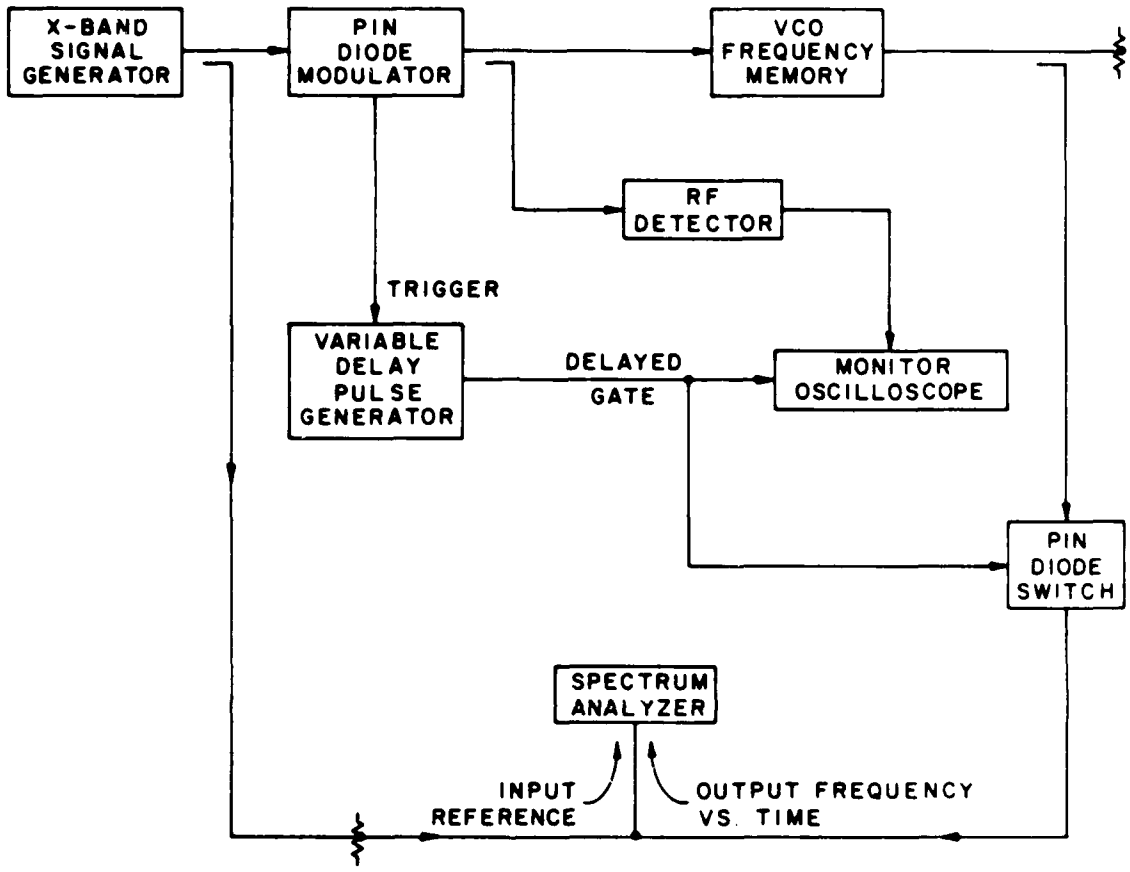
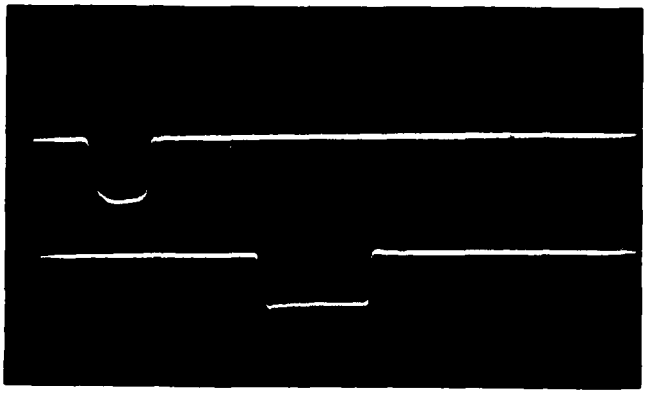


Figure A-2. Test equipment arrangement for frequency error vs time measurement.



— 100 ns/DIV ⟶

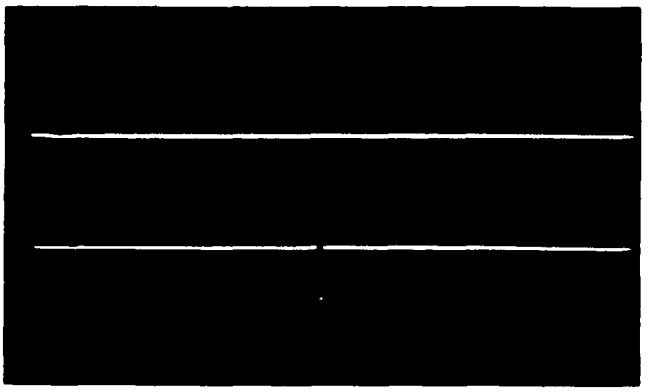
(a) TEST CONDITION #1

DETECTED rf INPUT PULSE APPROX. 80 ns WIDE

OUTPUT GATE FOR SPECTRUM ANALYZER 200 ns WIDE

300-ns DELAY FROM START OF INPUT PULSE

PRF = 5000 pps



— 2.0 μs/DIV ⟶

(b) TEST CONDITION #2

DETECTED rf INPUT PULSE APPROX. 80 ns WIDE

OUTPUT GATE FOR SPECTRUM ANALYZER 200 ns WIDE

10-μs DELAY FROM START OF INPUT PULSE

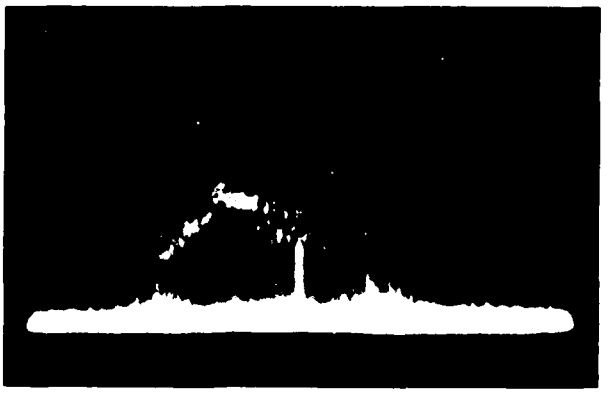
PRF = 5000 pps

TEST CONDITION #3 - NOT SHOWN

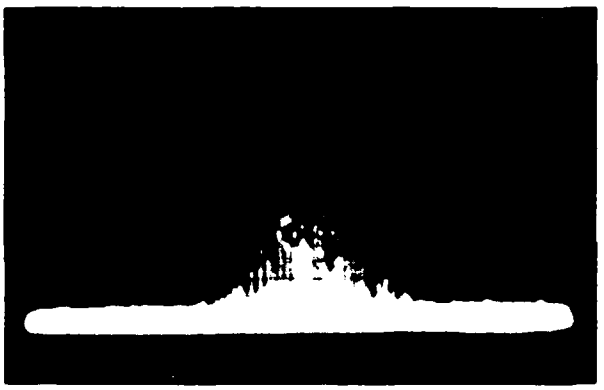
DETECTED rf INPUT PULSE APPROX. 80 ns WIDE
OUTPUT GATE WIDTH INCREASED TO 1.0 μs
OUTPUT GATE DELAYED BY 900 μs
PRF = 1000 pps

Figure A-3. Timing measurments.

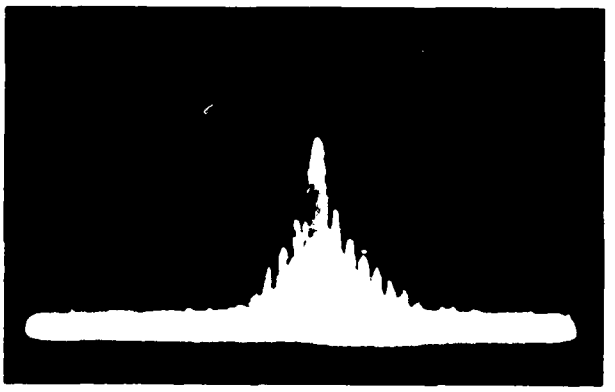
SPECTRUM ANALYZER 30 MHz/DIV



(a) OUTPUT GATE 200 ns WIDE
DELAYED BY 300 ns AFTER START OF
INPUT

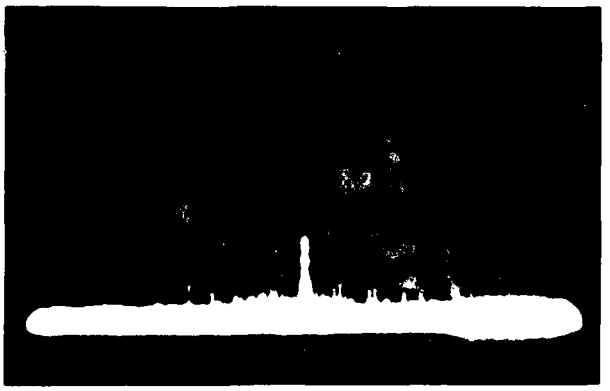


(b) WITH NOISE



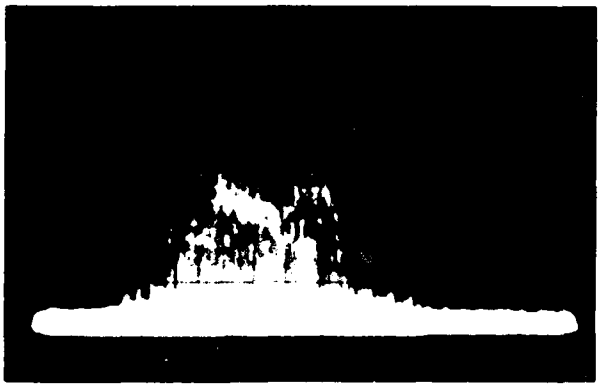
(c) WITHOUT NOISE

OUTPUT GATE DELAYED BY 10 μs

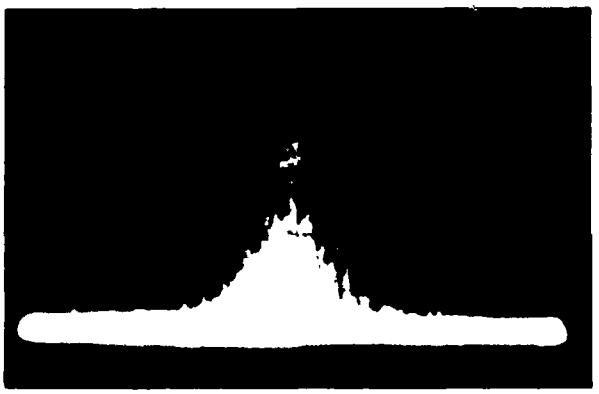


(d) OUTPUT GATE DELAYED BY 0.9 ms

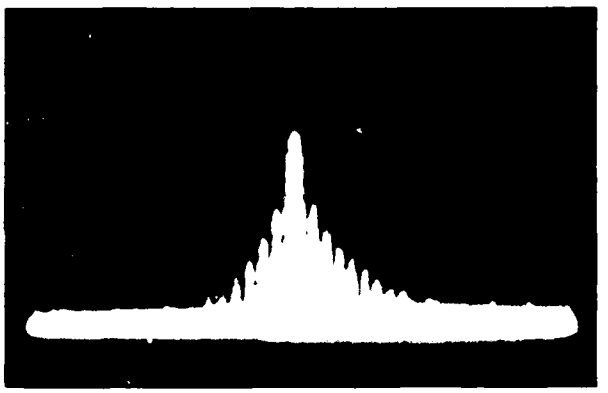
Figure A-4. Spectrum analyzer photographs - 8 GHz



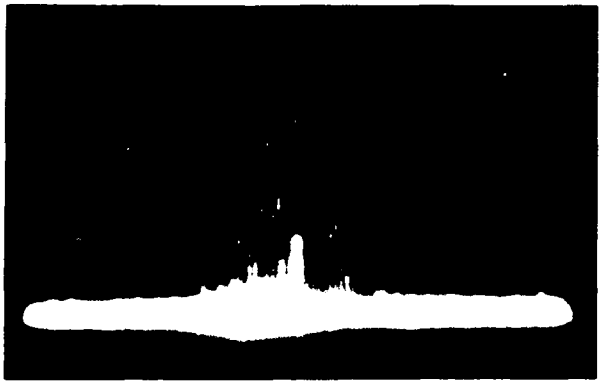
(a) 300 ns



(b) 10 μs



(c) 10 μs

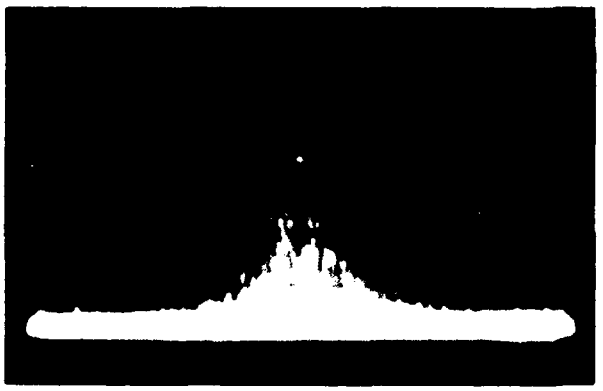


(d) 0.9 ms

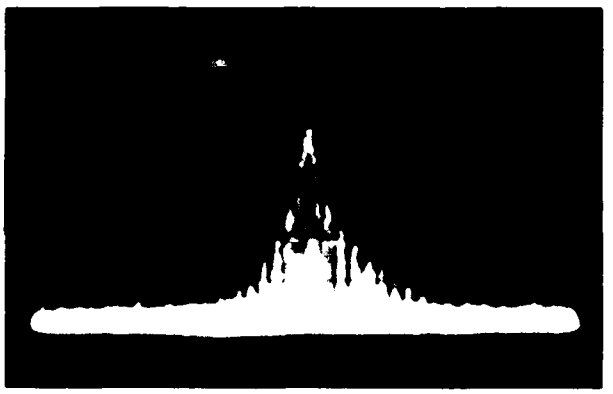
Figure A-5. Spectrum analyzer photographs - 5.5 GHz.

SPECTRUM ANALYZER 30 MHz/DIV

(a) OUTPUT GATE 200 ns WIDE
DELAYED BY 300 ns AFTER START OF
INPUT (~100 μs)

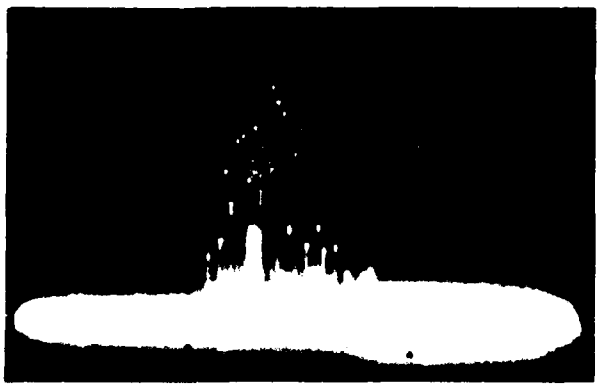


(b) WITH NOISE



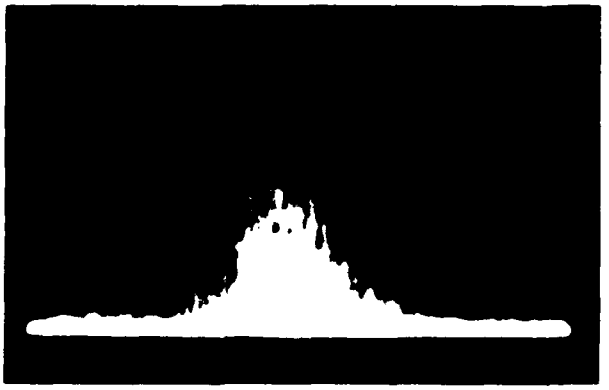
(c) WITHOUT NOISE

OUTPUT GATE 200 ns WIDE
DELAYED BY 10 μs

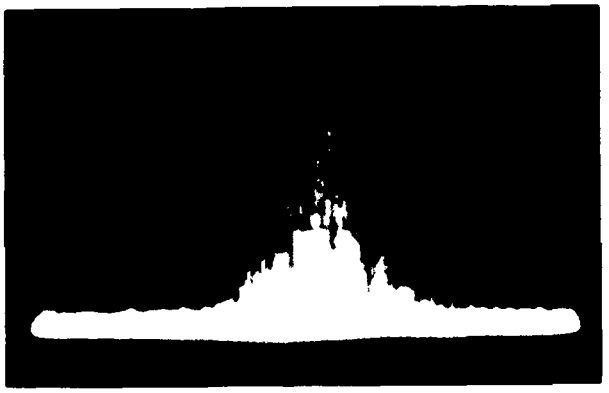


(d) OUTPUT GATE 1.0 μs WIDE
DELAYED BY 9.9 ms
PRF REDUCED TO 1 kHz

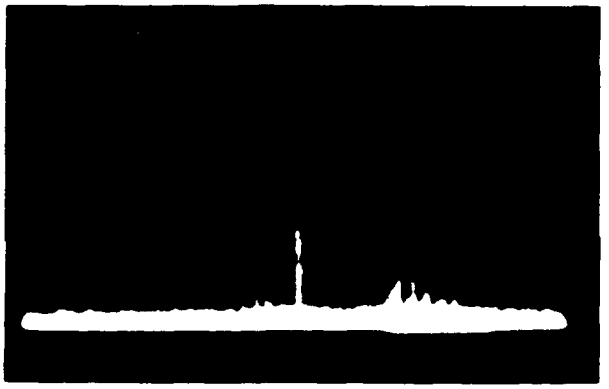
SPECTRUM ANALYZER 300 MHz/DIV



(a) OUTPUT GATE 200 ns
DELAYED BY 300 ns
PRF = 5 kHz

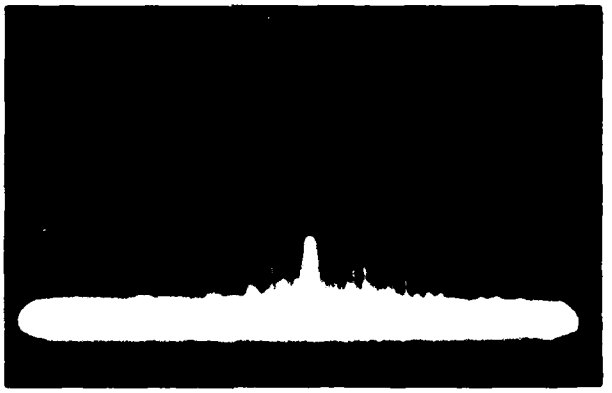


(b) WITH NOISE

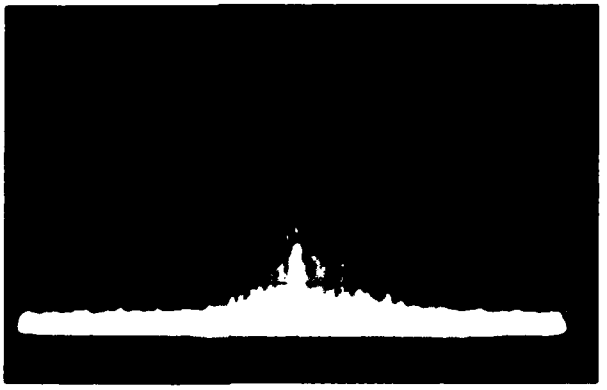


(c) WITHOUT NOISE

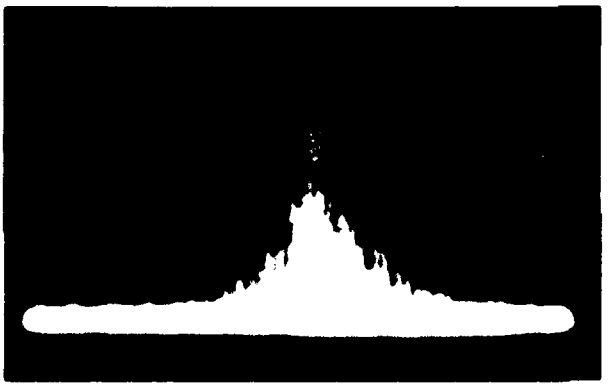
DELAYED BY 10 μs



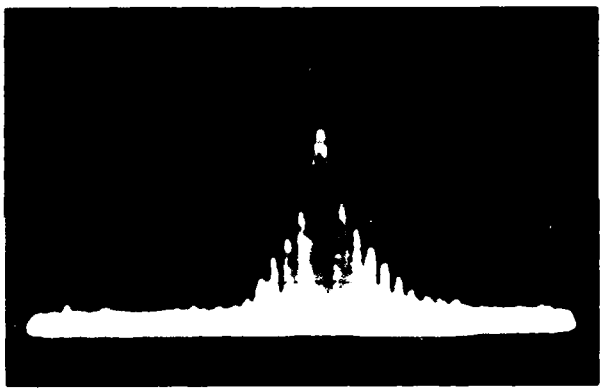
(d) OUTPUT GATE 1.0 μs WIDE
DELAYED BY 0.9 ms
PRF = 1 kHz



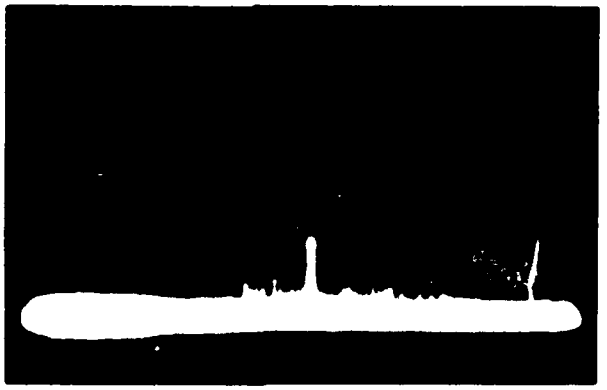
(a) 300 ns



(b) 10 μs



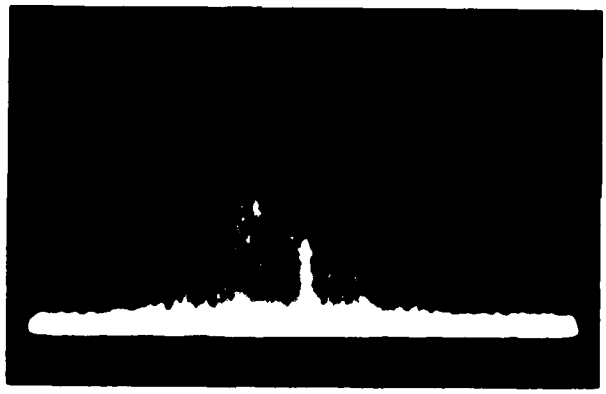
(c) 10 μs



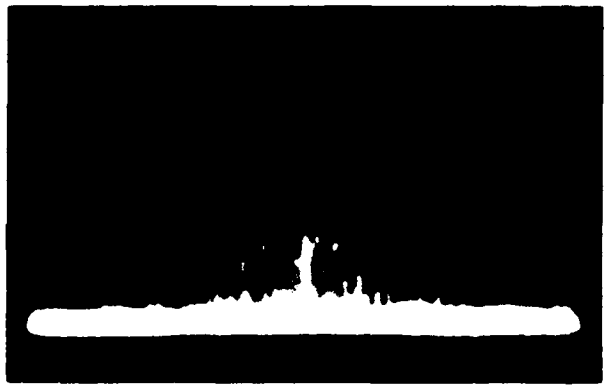
(d) 0.9 ms

CONDITION #3
WITHOUT NOISE

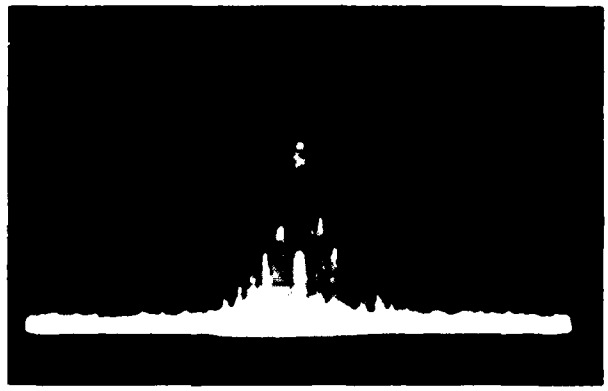
Figure A-9. Spectrum analyzer photographs - 9.0 GHz, condition #3 without noise.



(a) 300 ns



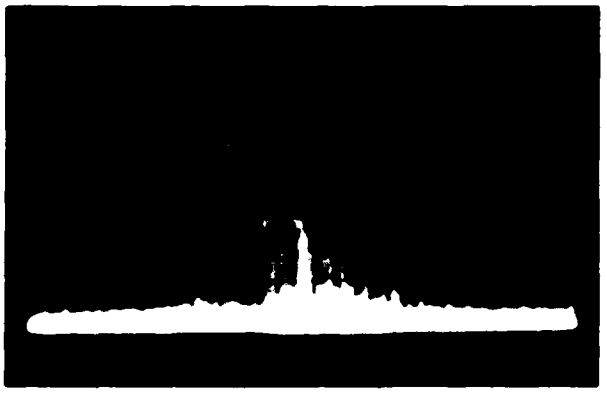
(b) 10 μs



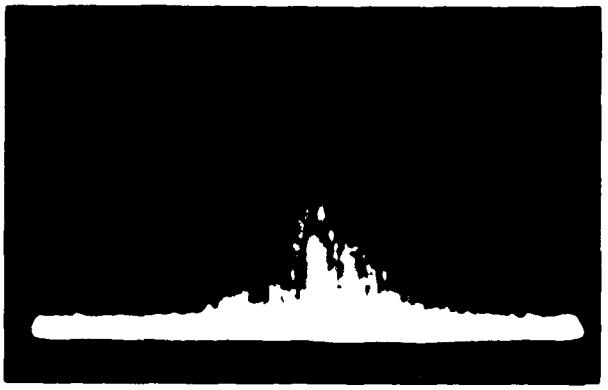
(c) 10 μs

(d) 0.9 ms

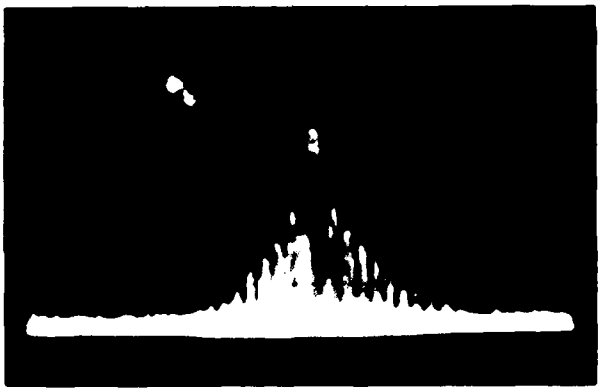
Figure X-10. Spectrum analyzer photographs - [illegible]



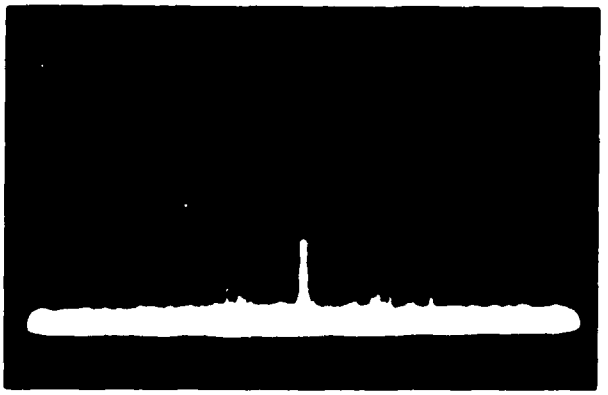
(a) 300 ns



(b) 10 μs

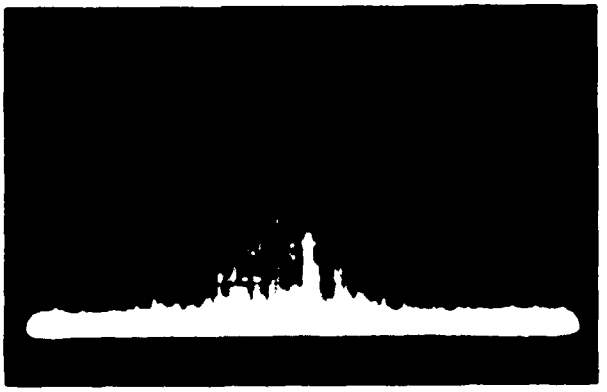


(c) 10 μs

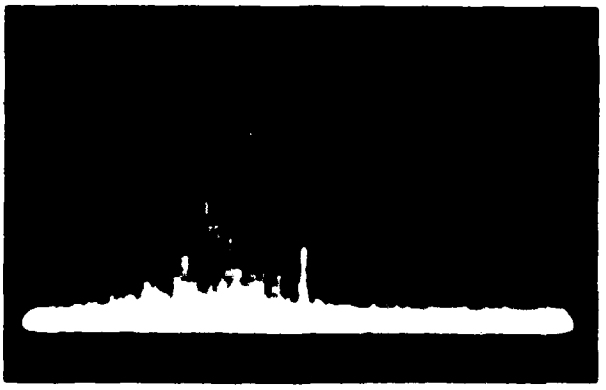


(d) 0.9 ms

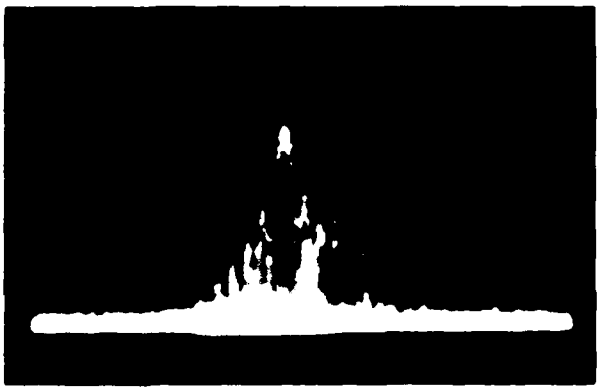
Figure A-11. Spectrum analyzer photographs



(a) 300 ns



(b) 10 μs



(c) 10 μs

(d) 0.9 ms

Figure A-12. Spectrum analyzer photographs [illegible]

END

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