INTEGRATED CIRCUITS LABORATORY

STANFORD ELECTRONICS LABORATORIES
DEPARTMENT OF ELECTRICAL ENGINEERING
STANFORD UNIVERSITY · STANFORD, CA 94305

TR-DXG501-82-1 ICL-17-79

COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUIT FABRICATION PROCESSES FOR VLSI DEVICES

prepared by

J.D. Plummer
R.W. Dutton
J.F. Gibbons
C.R. Helms
J.D. Meindl
W.A. Tiller
C.P. Ho
K.C. Saraswat
B.E. Deal

INTEGRATED CIRCUITS LABORATORY
STANFORD UNIVERSITY
Stanford, Ca. 94305

June 1983

Semi-Annual Report for Period 1 April 1982 · 30 September 1982

Prepared for:
ADVANCED RESEARCH PROJECTS AGENCY
1400 Wilson Boulevard
Arlington, Va. 22209

US Army Electronics Technology & Devices Laboratory

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: DELET - TR - 79 - 0257 - 4	2. GOVT ACCESSION NO.: AD-A130 105
	3. RECIPIENT'S CATALOG NUMBER:
4. TITLE (and Subtitle): Computer-Aided Design of Integrated Circuit Fabrication Processes for VLSI Devices (Computer-Aided Engineering of Semiconductor Integrated Circuits)	5. TYPE OF REPORT & PERIOD COVERED: Semi-Annual Report 1 April 1982-30 September 1982
	6. PERFORMING ORG. REPORT NUMBER: ~~2-DXG501~~
7. AUTHOR(s): A. Akinwande, G. Bronner, B. Cairns, L. Christel, W. Dibble, Jr., S. Dunham, R. Dutton, P. Fahey, J. Gibbons, M. Giles, C. Helms, C. Ho, E. Kutlu, L. Lie, H. Massoud, D. Modlin, J. Plummer,	8. CONTRACT OR GRANT NUMBER(s): MDA903-79-C-0257
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Stanford University, Integrated Circuits Laboratory, Stanford, California 94305	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS:
11. CONTROLLING OFFICE NAME AND ADDRESS: Defense Advanced Research Projects, 1400 Wilson Boulevard, Arlington, VA 22209	12. REPORT DATE: June 1983 / 13. NO. OF PAGES: 96
	15. SECURITY CLASS. (of this report): Unclassified
14. MONITORING AGENCY NAME & ADDRESS (if diff. from Controlling Office)	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from report)

18. SUPPLEMENTARY NOTES

This contract is awarded under Basic Agreement MDA903-79-C-0257, issued by Defense Supply Service-Washington. This research is sponsored by Defense Advanced Research Projects Agency (DARPA).

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Modeling Semiconductor Devices, Semiconductor Processing, Computer-Aided Device Design, Computer-Aided Process Design, Ion Implantation, Thermal Oxidation, Chemical Vapor Deposition, Device Simulation

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Efficient design of high performance VLSI processes requires accurate models for the physical processes used for fabrication. This is particularly true as device geometries shrink and fabrication technologies become inherently 2D. First order models for thermal oxidation, ion implantation, diffusion, chemical vapor deposition and other processes cannot accurately predict device structures from modern IC technologies.

over

DD FORM 1 JAN 73 1473

EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

19. KEY WORDS (Continued)

20 ABSTRACT (Continued)

The fundamental objective of this program is to develop accurate and physically correct models for these processes which are general enough to incorporate in a general purpose, user-oriented computer simulation tool - SUPREM. This program accepts process schedules as inputs and provides predicted device structures as outputs. It is meant to be capable of accurately simulating both bipolar and MOS VLSI structures. SUPREM is specifically designed to couple with device simulation tools so that it forms the cornerstone of a hierarchy of VLSI process, device, circuit and system design aids.

7 AUTHOR(s) (Continued)

K. Saraswat, F. C. Shone, M. Taubenblatt, Y. Thathachari, W. Tiller, E. Young.

TR DXG501-82-1 ICL 17-79

SEMI-ANNUAL REPORT

ON

COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUIT FABRICATION PROCESSES FOR VLSI DEVICES

APRIL 1, 1982 - SEPTEMBER 30, 1982

This work was supported by

a contract from the

DEFENSE ADVANCED RESEARCH

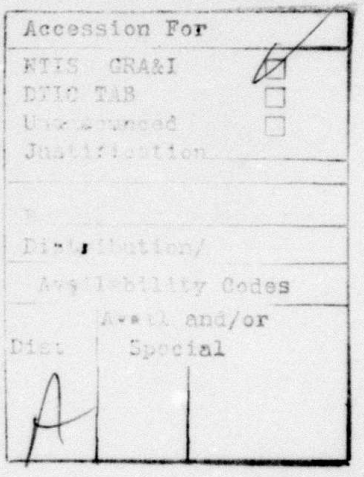
PROJECTS AGENCY

MDA903-79-C-0257

ARPA Order No. 3709

Approved for public release

Distribution unlimited



James D. Plummer

Stanford Electronics Laboratory

Stanford University Stanford, California

TABLE OF CONTENTS

COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUIT

FABRICATION PROCESSES FOR VLSI DEVICES

SUMMARY

The work described here builds upon an established program which over the past five years has resulted in the development of three generations of computer-aided process modeling programs - SUPREM I, II and III. The second generation version - SUPREM II - is currently in use at more than 150 industrial firms and university research groups and is generally regarded as the preminent tool of its type available today. A significant number of published papers from groups all over the world reference this computer program, and in fact, many papers include simulated results obtained from SUPREM. It has found widespread application in the design of state-of-the-art MOS and bipolar fabrication processes.

The principal highlight of the program during the present reporting period has been the release of SUPREM III. This is a completely new, greatly improved version of the program with substantially improved capabilities. SUPREM III can simulate structures with up to five material layers. Built in models for Si, SiO_2, Polysilicon and Si_3N_4 are included and other materials can easily be added with user defined parameters. A large number of new and/or improved physical models for oxidation, diffusion, epitaxy and ion

implantation are included in SUPREM III, these have, for the most part, come from experimental and theoretical work under this program over the past five years. These new models should greatly expand the range of applicability and the accuracy of the program.

At the present time approximately 25 copies of the new program have been licensed from the University by U. S. semiconductor manufacturers and defense contractors. We expect that over the lifetime of the program the distribution will eventually exceed that of SUPREM II. Initial feedback from industry users is beginning to come in to us, and it is clear already that the new program capabilities will make SUPREM III a much more valuable tool than its predecessors. We expect over the next two years to release updated versions of the program as new materials models become available. Much of the work which is aimed at this objective is described in the remainder of this report.

The specific goals of this research have been and continue to be the formulation of basic physical and mathematical models of integrated circuit fabrication processes which can accurately predict the structure of small geometry VLSI devices (and other arbitrary device structures) which will result from a given fabrication sequence, and to implement these models in a comprehensive process modeling computer program. Such a program, it was believed at the outset of this work, would significantly reduce costly and time consuming iterative, experimental approaches to developing or optimizing silicon technologies. This has, in fact, occurred. SUPREM III represents a major step along the path toward improved simulation tools.

It is clear that the historical trends in integrated circuit technology over the past two decades towards increased complexity and smaller active device dimensions will continue. Modern device structures employ lateral

device dimensions on the order of 2-3 μ and vertical dimensions well below 1 μm. There are no basic physical mechanisms which will prevent a reduction in each of these dimensions by an additional order of magnitude over the next two decades. Practically accomplishing this continued scaling, however, depends upon our ability to physically understand and quantitatively model the fabrication techniques which will be used in the construction of such devices.

For devices with relatively large geometries (>5 μ) and loose processing tolerances, relatively simple models suffice for prediction of vertical device structures resulting from a given fabrication sequence. As device dimensions shrink, however, it becomes essential to employ more robust process models and to consider the interaction both laterally and vertically of various processing steps, if accurate simulation of structures is to be obtained. This is important even with today's 2-3 μm device geometries; it will become essential for smaller devices.

Large geometry devices can be successfully modeled as one-dimensional structures. This is true for both process models and electrical models. Devices with lateral dimensions below a few microns, however, require two-dimensional models for accurate simulation. This need has stimulated a large body of work in recent years on two-dimensional electrical models of device current-voltage characteristics. One example of this type of work is the 2D program GEMINI, developed under this program. Work of this type has resulted in remarkable advances in our understanding of small geometry device physics.

Progress has not been as rapid, however, in two-dimensional process modeling. While some basic 2D process modeling programs have been developed at Stanford (SUPRA for example) and elsewhere, these programs do not

incorporate robust 2D kinetic models which can accurately predict doping profiles and device geometries under a wide range of conditions. This is a direct result of our need for improved physical models of oxidation, ion implantation, diffusion, and CVD. It is quite clear that these processes are not one dimensional. Recent experimental evidence has clearly indicated that oxidation or impurity diffusion in a localized region of a silicon substrate can substantially affect oxidation or diffusion rates in laterally or vertically adjacent regions of the substrate. There is no clear agreement at the present time on the basic physical mechanisms responsible for such results, although much has been learned in the past several years. It is clear, however, that we must quantitatively understand such phenomena if we are to accurately model small device structures.

A specific goal of this program is to understand and model these two-dimensional effects. We have made substantial progress in this regard in the past six months. It appears now that the basic physical phenomena underlying these interactions are the roles of points defects--silicon vacancies and interstitials--in impurity diffusion, thermal oxidation, and other processes. The generation and consumption of these point defects during high temperature fabrication steps appear to be the unifying physical effects which can explain many of the phenomena which have been regarded as anomalous to date. We have used such models to quantitatively understand a variety of process phenomena and have incorporated some of these models in SUPREM II. More such models are in SUPREM III. The unifying role of these mechanisms is a cornerstone of the work described in this progress report. We regard such models as absolutely essential to accurate modeling of two-dimensional effects in small devices.

Simply stated, the long-range objective of this research is the development of a 2D process modeling program which contains physically correct 2D kinetic models. Most of the effort under this program is aimed at experimental and theoretical work to uncover the basic physical mechanisms which govern 2D oxidation kinetics, 2D diffusion, etc. This is a major problem area with very difficult materials problems. It will become clear in the technical discussions later in this report that 2D process modeling involves much more than solving 1D equations in two dimensions. Basic physical laws and understanding are lacking at present. Effects such as lateral OED, oxidation under masking Si_3N_4 layers, lateral and vertical effects of high dopant concentrations on diffusion coefficients, and a host of other known experimental effects cannot be explained by a simple extrapolation of known 1D physical laws to 2D structures. This program is aimed at generating the physical understanding needed to develop 2D kinetic models.

An essential part of this is to develop models for bulk point defect (interstitial and vacancy) generation, recombination and diffusion, since it is clear that the local concentrations of these defects determine local diffusion coefficients, oxidation rates, etc. In fact, an alternative statement of the overall objective of this program would be to develop techniques for calculating local (i.e. time and position dependent) process parameters suitable for process simulation. Such process parameters will of necessity be geometry dependent which means that diffusion coefficients and oxidation rate constants, for example, will depend on the presence or absence of nearby heavily doped regions or oxidizing interfaces. This will imply a tight coupling between surface geometry and resulting impurity profiles in small devices.

In this context, the overall objectives of this program are:

(1) To develop accurate physical models for the basic technologies used in the fabrication of silicon integrated circuits--oxidation, ion implanatation, diffusion, and chemical vapor deposition (CVD).

(2) To develop accurate physical models for the interaction of these processes, for example, the enhancement of diffusion coefficients in an oxidizing ambient.

(3) To develop accurate physical models based upon silicon point defects for two-dimensional process phenomena in small geometry devi[illegible].

(4) To develop high resolution analytic tools for the experiment characterization of small device structures.

(5) To implement improved process models in updated versions of [illegible]EM III so that this program is capable of accurately simulating small devices and multi-layer structures.

(6) To aim toward a robust 2D process modeling program (SUPREM IV) which would combine outputs from this program with numerical techniques developed under other support.

(7) To disseminate the results to the semiconductor and defense industries.

The remainder of this report describes the specific research activities during the six month period covered by this report. Each of the subsequent sections includes a discussion of the problems under investigation, the results to date and plans for the future. The unifying themes of all of the work to be described are the development of new or improved models for SUPREM III and the investigation of 2D materials phenomena required to develop SUPREM IV.

1. OXIDATION AND POINT DEFECTS

S. DUNHAM, J. PLUMMER

The existence of interactions between silicon oxidation and the diffusion of impurities (OED and ORD) and growth/shrinkage of stacking faults (OISF) has been well established [1-12]. Both effects are attributed to the creation of interstitialcies at the oxidizing interface in order to relieve the stress created there [13-15]. Many of these studies have examined the relationship between oxidation rate $\frac{dX_o}{dt}$ and interstitialcy density resulting in fits to the equation:

$$C_I \propto \left(\frac{dX_o}{dt}\right)^n \qquad (1)$$

Unfortunately, the value of n must be calculated empirically and reported values have ranged from less than 0.3 [4] to more than 1.0 [12]. Our ongoing work then, is an attempt to physically account for the relationship between oxidation rate and point defect densities and thus to develop quantitative models for OED, ORD and other phenomena suitable for 2D process modeling in SUPREM IV.

It has been observed that in lightly-doped silicon, oxidation is more than 99% complete [16], so virtually all of the silicon interstitialcies created by oxidation must diffuse into the oxide where they react with incoming oxygen to complete the process. Therefore, the fluxes within the

oxide (Figure 1) determine the interstitialcy density at the interface. We can write the continuity equations for oxygen and silicon interstialcies as:

$$\frac{\partial C_o}{\partial t} = D_o \frac{\partial^2 C_o}{\partial x^2} - k_I C_I C_o \qquad (2)$$

$$\frac{\partial C_I}{\partial t} = D_I \frac{\partial^2 C_I}{\partial x^2} - k_I C_I C_o \qquad (3)$$

In steady state, as for relatively long oxidations, the time derivatives are zero so combining (2) and (3) and integrating twice we get:

$$C_o = \gamma C_I + a + bx \qquad (4)$$

where $\gamma = (D_I/D_O O)$.

Tracer experiments [17-19] have shown that oxidation takes place very close to the oxide-bulk interface so there is no flux of interstitials through the oxide. Therefore, we can conclude that:

$$\left(\frac{dC_I}{dx}\right)_{x = o} = 0 \qquad (5)$$

and $$C_I(o) = 0 \qquad (6)$$

By Henry's Law: $$C_o(0) = Kp_{O_2} \qquad (7)$$

so combining with (4) and (6):

$$a = Kp_{O_2} \qquad (8)$$

The rate of oxide growth is proportional to the flux of oxygen at the gas-oxide interface:

$$D_o \left(\frac{dC_o}{dx}\right)_{x=o} = -\frac{1}{\Omega}\frac{dX_o}{dt} \qquad (9)$$

where X_o is oxide thickness and Ω is the molecular volume of SiO_2. Combining this with (4) and (5):

$$b = -(D_o\Omega)^{-1}\left(\frac{dX_o}{dt}\right) \qquad (10)$$

We can now rewrite equation (4) as:

$$C_o = \gamma C_I + Kp_{O_2} - (D_o\Omega)^{-1}\left(\frac{dX_o}{dt}\right)X \qquad (11)$$

For conditions where the partial pressure dependence of the oxidation rate is linear (wet or high temperature dry), at the interface the rate of oxidation, which is equal to the oxygen flux, is proportional to the density of oxygen:

$$D_o \left(\frac{dC_o}{dx}\right)_{x=x_o} = k_o C_o X_o \qquad (12)$$

Due to volume constraints, a certain percentage (α) of interface reactions must result in point defect interactions. Ho and Plummer's results [20,21] show that vacancy mechanisms are negligible in intrinsin silicon so:

$$D_I \left(\frac{dC_I}{dx}\right)_{x=x_o} = -\alpha D_o \left(\frac{dC_o}{dx}\right)_{x=x_o} \qquad (13)$$

Substituting the derivative of (11) and rearranging:

$$\left(\frac{dC_I}{dx}\right)_{x = x_o} = \frac{\alpha}{1+\alpha} \; (\delta D_o \Omega)^{-1} \left(\frac{dX_o}{dt}\right) \qquad (14)$$

Combining this result with (12) and the experimental support for the Deal-Grove model [22] that says:

$$X_o = \frac{B}{2}\left(\frac{dX_0}{dt}\right) - \frac{A}{2} \qquad (15)$$

then solving for the density of interstitialcies at the oxide-bulk interface we get:

$$C_I \; (X_o) = K_1 \frac{dx_o}{dt} + K_2 \qquad (16)$$

$$K_1 = \frac{1}{\delta\Omega} \; \left[\frac{1}{k_o(1+\alpha)} - \frac{A}{2D_0}\right] \qquad (17)$$

$$K_2 = \frac{1}{\delta} \; \left[\frac{B}{2D_o} - Kp_{o_2}\right] \qquad (18)$$

We can see that depending on the magnitudes of K_1 and K_2, which will change with temperature and partial pressure, any power law relationship relating C_I and dx_o/dt between 0 and 1 can be approximated.

Looking first at stacking fault growth:

$$L = \int_o^t (K_I C_I - K_V C_V - K_R) \, dt \qquad (19)$$

Assuming steady-state recombination of point defects, then $C_V = (C_V^* \, C_I^*) \Big/ C_I$, so using (16) and looking only at parabolic oxidations where $\frac{dL}{dt} = \left(\frac{B}{2t}\right)^{1/2}$,

we can integrate to get:

$$L = \left(K_I K_1 B^{1/2}\right) t^{1/2} + \left(K_2 - K_r - \frac{2K_V C_I^* C_V^*}{K_2}\right) t + \frac{K_1 B^{1/2}}{2K_2} \ln\left(1 + \frac{2K_2}{K_1 B^{1/2}} t^{1/2}\right) \quad (20)$$

Ignoring the final term which should be small since $C_I >> C_I^*$, this expression gives a stacking fault length time dependence of between 0.5 and 1.0 which fits well with reported dependences [3,7-11]. In fact, fits to $L = A_1 t^{1/2} + A_2 t$ are virtually indistinguishable from the accepted practice of fitting to $L = At^n$ (Figure 2). Since the constants A_1 and A_2 will change with oxidizing conditions, we can see how different apparent power relationships should result.

Most impurities diffuse via point defect mechanisms which in the most general case gives:

$$D_i = C_I D_I + C_V D_V \quad (21)$$

As for stacking faults, except for impurities that diffuse only with vacancies (ORD), the second term is usually negligible so calculating the time-averaged diffusion constant gives:

$$\langle D_i \rangle = D_I K_1 \left\langle \frac{dx_o}{dt} \right\rangle + D_I K_2 \quad (22)$$

which can apear as any power dependence between 0 and 1. Most experimental work has involved changing either temperature or partial pressure so no direct comparison with experiment has been done to this point.

In conclusion, this work gives a physical basis for the observed dependence of impurity diffusion and stacking fault growth/regrowth on oxidation conditions. There appears to be great potential in unifying the many seemingly contradictory results that have shown up in this area. Such a model would enable prediction of the effect of oxidation on the resulting bulk properties and perhaps point out how to most effectively make use of these interactions.

References

[1] D.A. Antoniadis, A.G. Gonzales, and R.W. Dutton, J. Electrochem. Soc., 27, 813 (1978).

[2] R. Francis and P.S. Dobson, J. Appl. Phys., 50(1), 280 (1979).

[3] S.M. Hu, J. Appl. Phys., 45, 1567 (1974).

[4] K. Taniguchi, K. Kurosawa, and M. Kashiwagi, J. Electrochem. Soc., 127, 2243 (1980).

[5] A.M. Lin, D.A. Antoniadis, and R.W. Dutton, J. Electrochem. Soc., 128, 1131 (1981).

[6] S. Mizuo and H. Higuchi, Jap. J. Appl. Phys., 20, 739 (1981)

[7] R.B. Fair, J. Electrochem.Soc., 128, 1360 (1981).

[8] S.P. Murarka, J. Appl. Phys., 48, 5020 (1977).

[9] A.M. Lin, R.W. Dutton, D.A. Antoniodis, and W.A. Tiller, J. Electrochem. Soc., 128, 1121 (1981).

[10] S.P. Murarka, Physical Review B, 16, 1849 (1977).

[11] S.M. Hu, J. Appl. Phys., 51, 3666 (1980).

[12] Y. Ishikawa, Y. Sakina, H. Tanaka, S. Matsumoto, and T. Numi, J. Electrochem. Soc., 129, 644 (1982).

[13] W.A. Tiller, J. Electrochem. Soc., 127, 619 (1980).

[14] W.A. Tiller, J. Electrochem. Soc., 127, 625 (1980).

[15] W.A. Tiller, J. Electrochem. Soc., 128, 689 (1981).

[16] B.E. Deal, J. Electrochem. Soc., 110, 527 (1963).

[17] M.M. Atalla, in Properties of Elemental and Compound Semiconductors, 1960, ed. by H. Gatos, Interscience, 163 (1960).

[18] J.R. Ligenza and W.G. Spitzer, J. Phys. Chem. Solids, 14, 131 (1960).

[19] P.J. Jorgensen, J. Chem. Phys., 37, 874, (1962).

[20] C.P. Ho and J.D. Plummer, J. Electrochem. Soc., 126, 1516 (1979).

[21] C.P. Ho and J.D. Plummer, J. Electrochem. Soc., 126, 1523 (1979).

[22] B.E. Deal and A.S. Grove, J. Appl. Phys., 36, 3770 (1965).

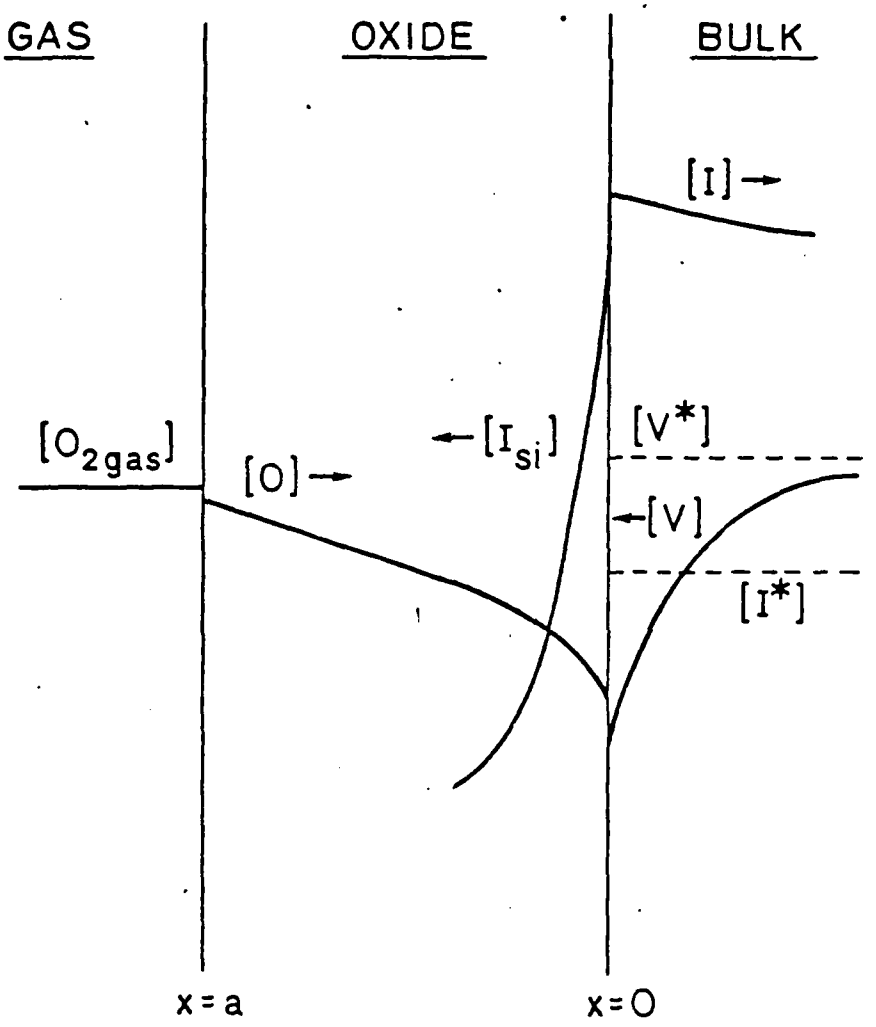


FIGURE 1: Densities and fluxes of reactants in oxidizing silicon.

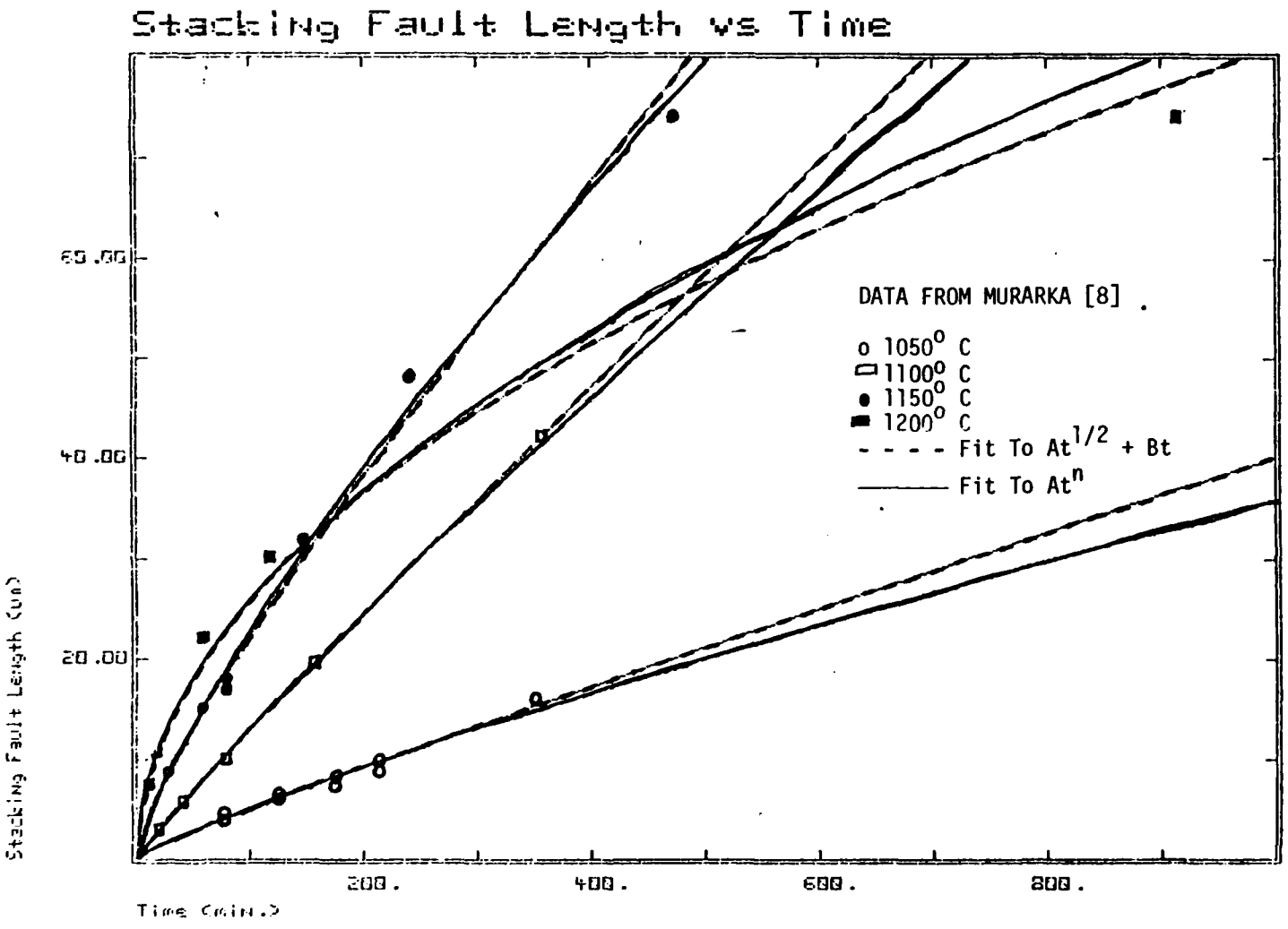


FIGURE 2: Comparison of modeling based upon equation 20 and experimental data.

2. THIN OXIDE GROWTH KINETICS IN DRY OXYGEN

H. MASSOUD, C. HO, J. PLUMMER

Very thin layers of thermal SiO_2 were grown in dry oxygen in the thickness range 0 - 500 A as described in earlier reports. These oxidations were carried out on single crystal silicon of different orientations (100), (111) and (110) , for different phosphorous substrate doping densities ($1 \times 10^{15}cm^{-3}$), ($2 \times 10^{20}cm^{-3}$) and ($3.2 \times 10^{20}cm^{-3}$) , in different oxygen partial pressures in argon (1 atm, 0.1 atm and 0.01 atm), in the temperature range 800°C to 1000°C. The growth was monitored by an in-situ automated high-temperature ellipsometer which is well-suited for data collection in the initial stages of oxidation where the growth rate is enhanced. The experimental work was done in cooperation with IBM.

The data were analyzed in the context of the Deal-Grove linear-parabolic model where the oxidation rate is expressed as:

$$\frac{dX_{ox}}{dt} = \frac{B}{2X_{ox}+A} \qquad (1)$$

where B and (B/A) are the parabolic and linear oxidation rate constants respectively. These rate constants describe the oxidation kinetics beyond the fast initial regime. The rate constants were obtained using the optimum X_i method. The oxidation rate enhancement in the thin regime can be expressed as an excess or as a ratio term:

$$\frac{dX_{ox}}{dt} = \frac{B}{2X_{ox}+A} + \Delta_e\left(X_{ox},t\right) \qquad (2)$$

or

$$\frac{dX_{ox}}{dt} = \frac{B}{2X_{ox}+A}\left[1 + \Delta_r(X_{ox},t)\right] \qquad (3)$$

where Δ_e and Δ_r are the excess or ratio enhancement terms which vanish with the onset of the linear parabolic kinetics. For all the orientations studied in 100% pure oxygen, it was found that these excess terms could be fitted to the following expressions:

$$\frac{dX_{ox}}{dt} = \frac{B}{2X_{ox}+A} + C_1 e^{-X_{ox}/L_1} + C_2 e^{-X_{ox}/L_2} \qquad (4)$$

or

$$\frac{dX_{ox}}{dt} = \frac{B}{2X_{ox}+A}\left(1 + K_1^* e^{-t/\tau_1} + K_2^* e^{-t/\tau_2}\right) \qquad (5)$$

The dependence of the oxidation excess enhancement term Δ_e on oxide-thickness is defined by two terms exponentially decaying with thickness. Both terms contribute to Δ_e up to ≈ 50Å, where the term (C_1,L_1) vanishes. From ≈ 50Å to to the onset of linear-parabolic kinetics (≈ 300Å), only the term (C_2,L_2) is responsible for the rate enhancement: L_1 is of the order of 7 - 17Å, and is a weak function of temperature. L_2 is of the order of 60 - 80Å, is temperature independent and is only a function of substrate orientation.

The oxidation rate enhancement studied as a ratio term was best fitted to an expression like that of equation (5). In this analysis K_1^* and K_2^* are orientation dependent constants that are temperature independent. This analysis is most consistent with the assumption that the concentration of oxygen species in the oxide during the initial stages of the oxidation is enhanced above what is inferred from permeation studies. The most frequently quoted values for the solubility of oxygen and water modules in SiO_2 are $5 \times 10^{16} cm^{-3}$ and $5 \times 10^{19} cm^{-3}$ respectively. This corresponds to an average spacing between the oxidant species of 270Å and 27Å for oxygen and steam respectively.

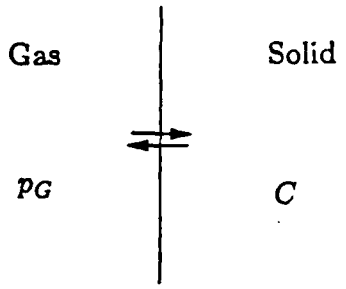
It is easily seen that the concept of an average bulk solubility is questionable in the case where the average spacing between the solute molecules is larger than the thickness of the film considered. This is illustrated in Figure 1. The same conclusion is arrived at when we consider the validity of application of Henry's Law to the kinetics of oxidation in the initial stages. Henry's Law assumes that the solubility C of a gas in equilibrium with a solid is related to the gas pressure p_G by the Henry's Law constant H:

$$C = Hp_G \tag{6}$$

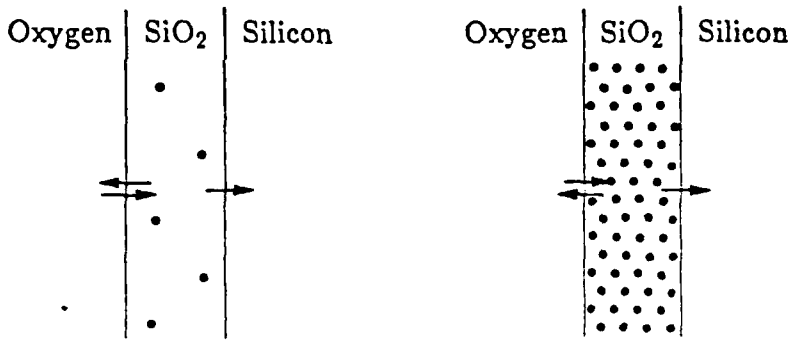
This assumes a semi-infinite solid. This assumption is needed to establish the equilibrium between the flux of gas molecules entering the solid and the flux of gas molecules leaving the solid. In equilibrium, these two fluxes are equal. In the case of a thin layer of SiO_2 (as shown in Figure 1), it is seen that in the case of dry oxygen, the flux of oxygen molecules consumed in the oxidation reaction at the Si-SiO_2 inteface may directly affect the equilibrium established at the outside surface of the SiO_2 layer. In the case of steam, the effects of the flux of water molecules consumed at the Si-SiO_2 interface are screened by the higher solubility of water in SiO_2. This is in agreement with the absence of a fast initial oxidation stage in the case of steam.

Analysis of the oxidation data at lower partial pressures of oxygen will help elucidate the importance of the role oxygen solubility plays in the non-steady state period present in the case of oxidation in dry oxygen. It may also suggest other physical mechanisms that play a role in fast initial oxidation as well.

HENRY'S LAW



$$C = Hp_G$$



Dry

$C^* = 5 \times 10^{16}$ cm^{-3}

O_2—O_2 spacing $\approx$ 270 Å

Wet

$C^* = 5 \times 10^{19}$ cm^{-3}

H_2O--H_2O spacing $\approx$ 27 Å

FIGURE 1: Physical arguments which may explain why O_2 solubility is higher than the equilibrium value during the initial oxidation stage (see text).

3. ATMOSPHERIC AND HIGH PRESSURE OXIDATION OF POLYCRYSTALLINE SILICON

B. CAIRNS, L. LIE

High pressure oxidation runs for polycrystalline silicon kinetic studies were not made during this time period because a problem of accurate temperature control developed in the high pressure oxidation system when it was converted from a 3-inch to 4-inch wafer capability for other internal Fairchild programs. A new tube and thermal control system which will correct this problem have been ordered and high pressure runs should resume in the late October to early December time frame.

3.1 Resistivity of Oxidized Polycrystalline Silicon

Measurements of polycrystalline silicon film resistivities following pyrogenic steam were completed. The phosphorous doped polycrystalline silicon fims were oxidized in 1, 5 and 10 atm pyrogenic H_2O at 750°, 800°, and 850°C. Results show that the resistivity is dependent on oxidation temperature and is fairly constant as the oxidation proceeds at a given temperature (Figures 1 and 2). As expected, the higher oxidation temperatures yielded lower film resistivities. In all cases, we did not oxidize more than 50% of the poly-Si films. Results reported by Saraswat of Stanford show a substantial increase in resistivity when more than 60% of the films are oxidized. The polycrystalline silicon films which did not receive a pre-oxidation anneal show a very rapid increase in the film resistivity for all temperatures and pressures to the values for the annealed films. This is not surprising for oxidation temperatures below the 950°C at which these films were doped. Reduced dopant solubility within the polycrystalline silicon grains after oxidation could be the main factor for this rapid increase in the resistivity. We could not

determine a time constant for the process, but it is complete in about 10 minutes. It was also noted that pressure effects appear negligible on the variation of film resistivities following oxidations up to 10 atm at these temperatures. The slight differences between 1 atm and 20 atm seen between Figures 1 and 2 are within the range of data scattering.

3.2 Atmospheric Oxidation of Polycrystalline Silicon

The oxidations of undoped polycrystalline silicon films in 1 atm pyrogenic steam at 750°, 800°, and 850°C have been completed. Half of the samples received a pre-oxidation anneal in nitrogen at the oxidation temperature. The plot of log oxide thickness versus log oxidation time is shown in Figure 3. For undoped polycrystalline silicon the differences observed in the oxidation rates between unannealed and pre-oxidation annealed samples are mostly within the accuracy of the oxide thickness measurements. This is not unexpected because x-ray diffraction analysis of the undoped polycrystalline silicon film as deposited by LPCVD at 615°C shows a predominant grain orientation of (110) and little changes are observed in the structure of polycrystalline silicon after annealing at temperatures up to 1000°C [1]. Analysis of the oxide growth data indicates that the oxidation kinetics of the film resembles that of (110) oriented single crystal siicon. The parabolic rate constant B was found to be slightly lower, by approximately 25%, than that of the (111) single crystal silicon; while the linear rate constant B/A was quite similar to that of the (111) single crystal silicon. These results are in agreement with available data comparing (111) and (110) lightly doped single crystal silicon oxidation kinetics [2,3]. The activation energies for B (38 kcal/mole) and B/A (35 kcal/mole) are the same, within the experimental accuracy, as for the B and B/A respectively, of the lightly doped

(111) single crystal silicon in this lower temperature range. The graphs of log B and log B/A versus reciprocal tempeature are shown in Figures 4 and 5, respectively.

The oxidation of doped and undoped polycrystalline silicon films in 1 atm dry O_2 ambient at 800°, 900°, and 1000°C have also been completed. Annealed and unannealed samples were included. All wafers were pulled in argon after each oxidation run. This completes the runs of the atmospheric part of the program. Analysis of the oxidation kinetics of these samples and comparison with respect to single crystal silicon oxidation in dry O_2 are underway.

3.3 Structural Evaluation

Several samples of doped polycrystalline silicon oxidized in pyrogenic steam at 1 atm and 10 atm have been submitted for cross-section TEM evaluation. Samples were chosen to evaluate the effects of pressure, temperature, and annealing on oxides of the same thickness range (2000-2500 A) as well as various thicknesses under constant temperature and pressure conditions.

References

[1] T.I. Kamins, M.M. Mandurah and K.C. Saraswat, J. Electrochem. Soc., 125, 927 (1978).

[2] Y. Kamigaki and Y. Itoh, J. Appl. Phys., 48, 2891 (1977).

[3] E.A. Irene, J. Electrochem. Soc., 121, 1613 (1974).

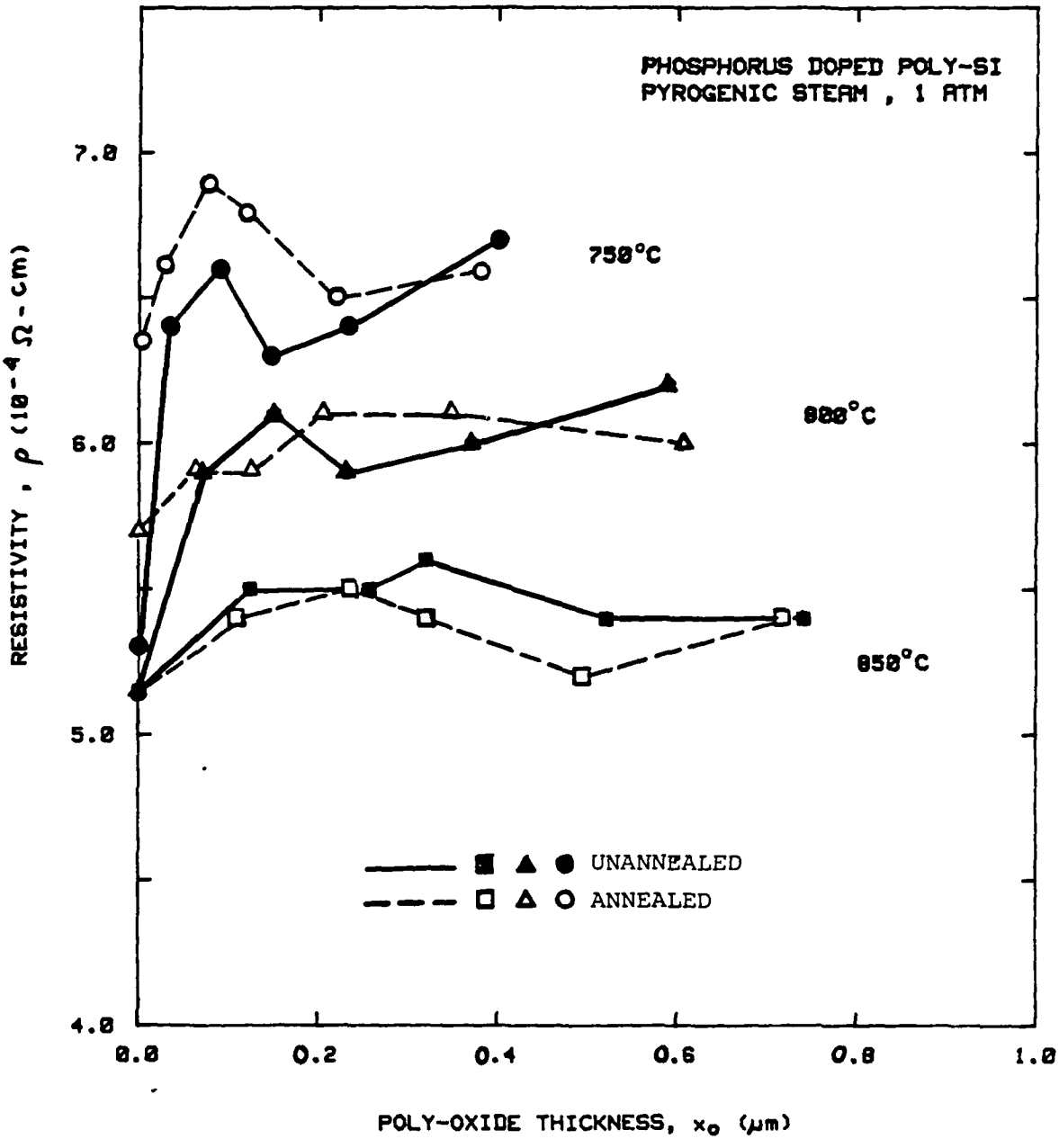


FIGURE 1: Residual poly-silicon film resistivity versus poly-silicon oxide thickness grown in 1 atm pyrogenic steam at 750°, 800°, and 850° C. Results for annealed and unannealed phosphorus doped poly-silicon film are shown.

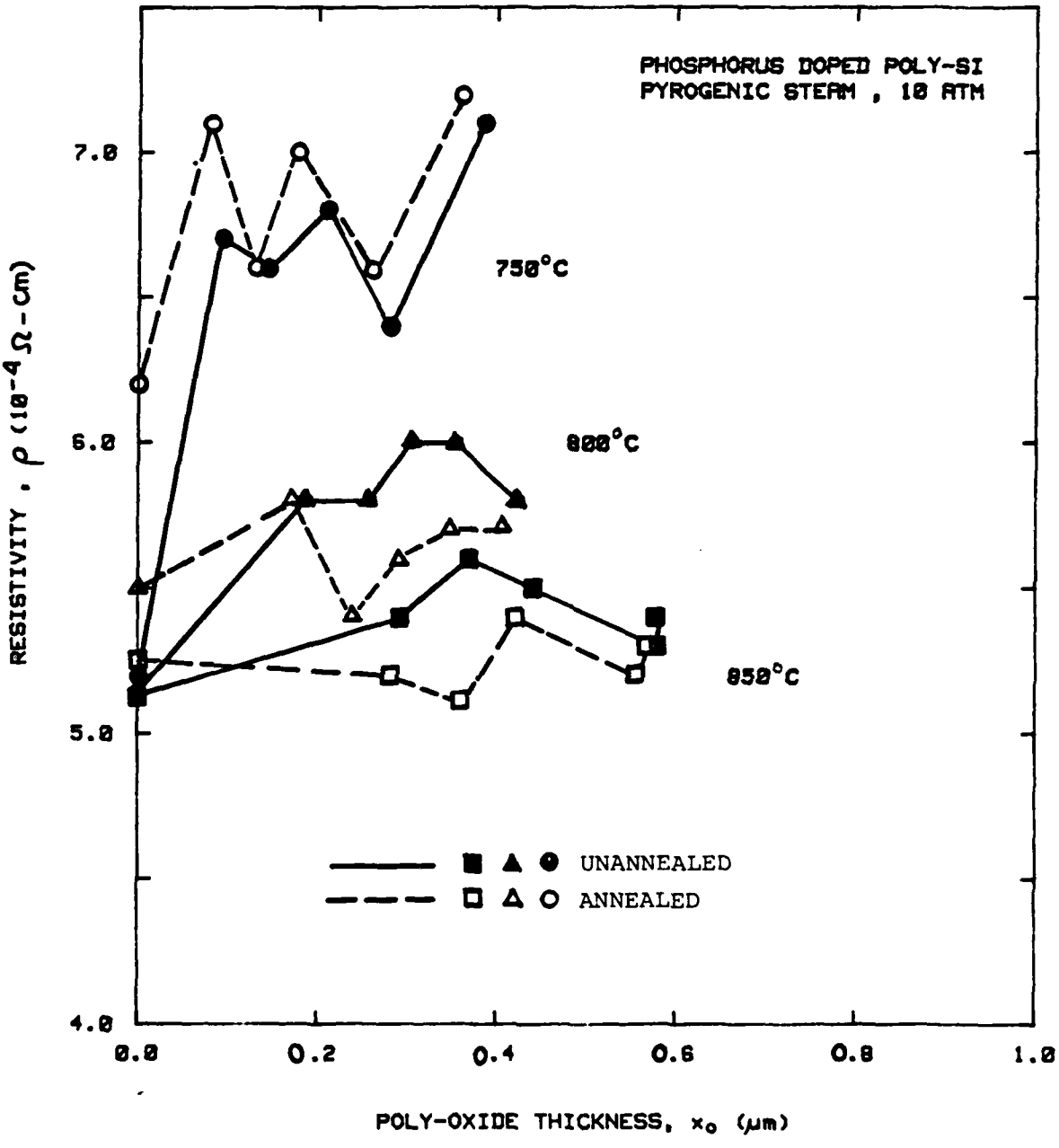


FIGURE 2: Residual poly-silicon film resistivity versus poly-silicon oxide thickness grown in 10 atm pyrogenic steam at 750°, 800°, and 850° C. Results for annealed and unannealed phosphorus doped poly-silicon film are shown.

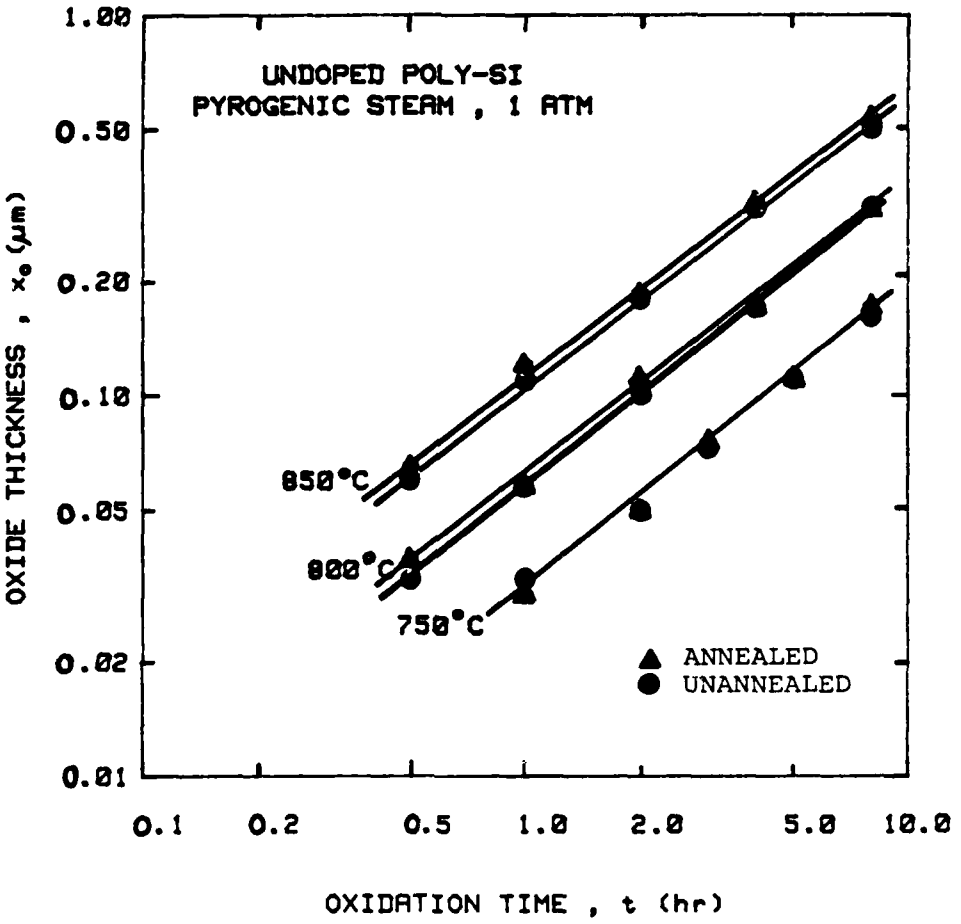


FIGURE 3: Oxide thickness versus oxidation time for annealed and unannealed undoped poly-silicon films oxidized in pyrogenic steam at 1 atm and 750^{o} - 850^{o} C.

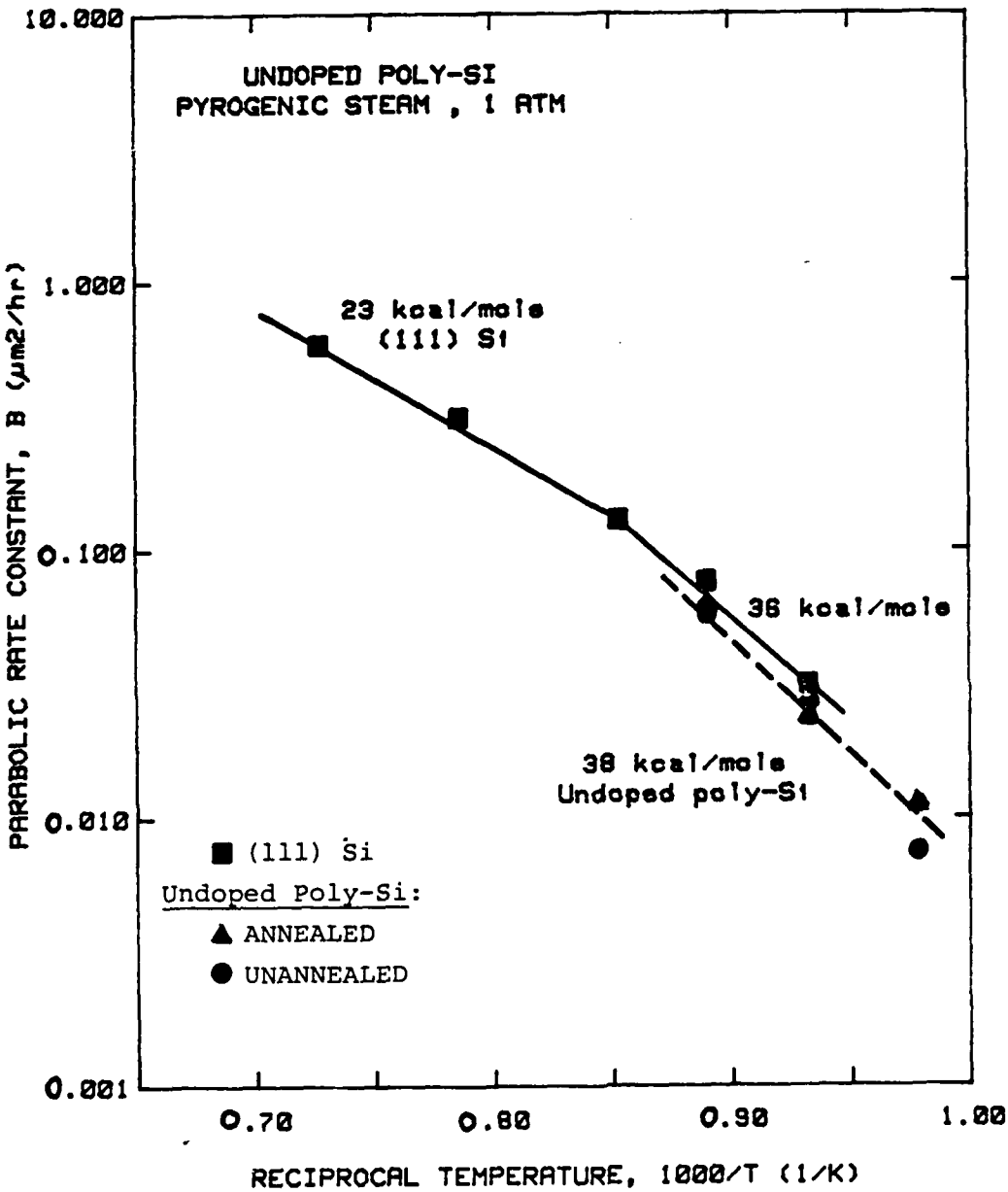


FIGURE 4: Parabolic rate constant B versus 1000/T for annealed and unannealed undoped poly-silicon films oxidized in pyrogenic H_2O at 1 atm and 750^0 - 850^0 C. Parabolic rate constants of (111) Si are shown for comparison.

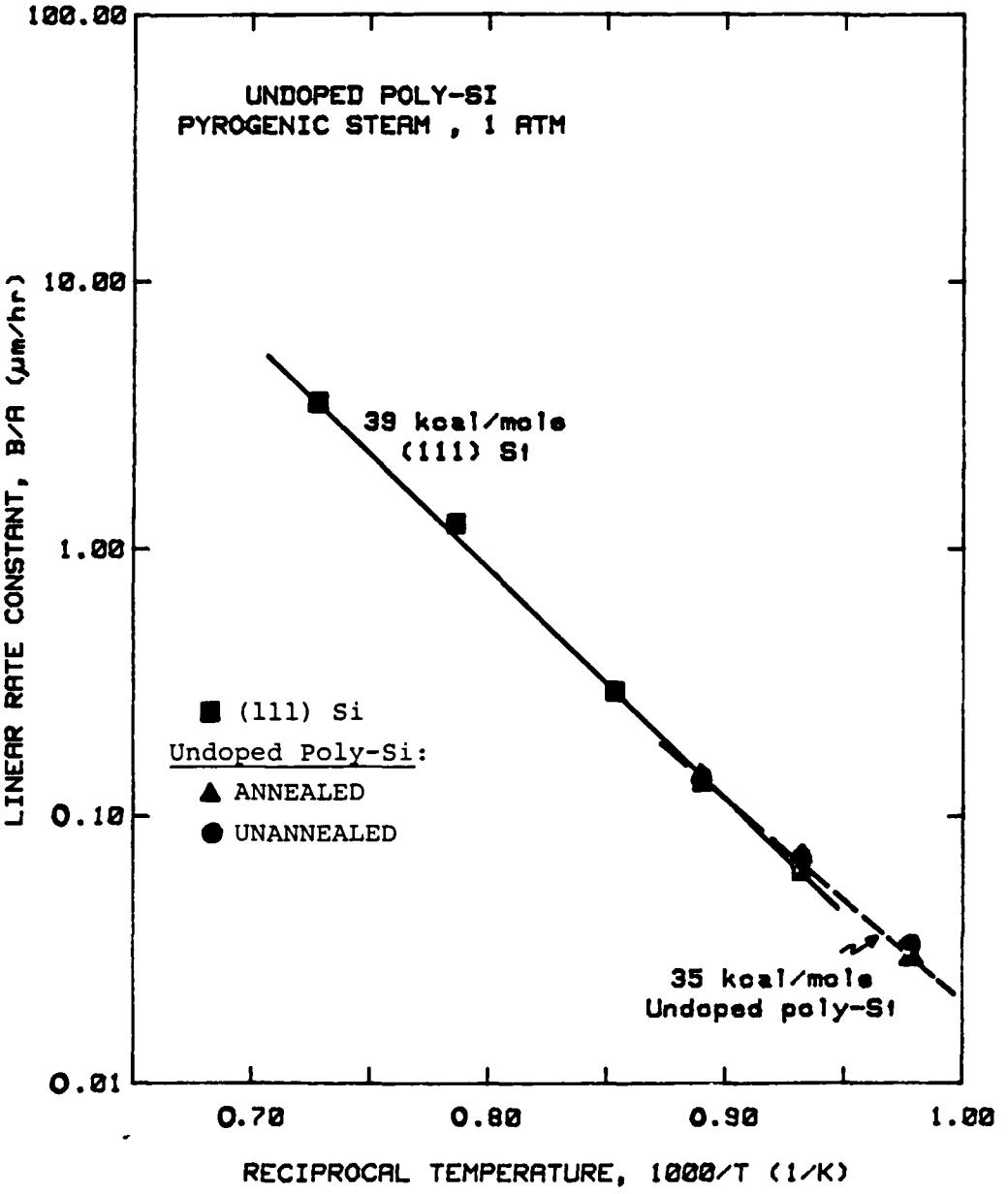


FIGURE 5: Linear rate constant B/A versus 1000/T for annealed and unannealed undoped poly-silicon films oxidized in pyrogenic H_2O at 1 atm and 750^0 - 850^0 C. Linear rate constants of (111) Si are shown for comparison.

4. OXIDATION ENHANCEMENT STUDIES

W. A. TILLER, Y. T. THATHACHARI, W. E. DIBBLE, JR.,
D. N. MODLIN and E. M. YOUNG

4.1 Field Enhancement

In the field-enhanced oxidation studies, the native oxide thickness, X_N is much less than the total oxide thickness, X_B, at t=700° C with a <100> substrate and I ≈ - 5μA. Thus, we decided to check to see if the experimental data satisfied a constant current-time product since this is what is expected theoretically; i.e.,

$$\overline{X_B} - X_N = \frac{It}{qN_o} \qquad (1)$$

where X_B is the average enhanced oxide thickness. The question is, does this also happen for the peak oxide thickness, i.e., do we have

$$X_B - X_N \alpha It \qquad (2)$$

In Figure 1, we see the superposed results of an I = - 5μA and t = 2.0 hr experiment with one at I = - 10μA and t = 1.0 hr. Although the profiles are quite similar, the - 10μA curve is wider at its base and has a lower peak height. Thus, although eq. 1 holds, eq. 2 does not hold exactly. This situation is readily explained. In the point to plane discharge, increasing I leads to enhanced natural repulsion betwen the ions so that the ion beam widens because the axial electric field is not increased in proportion to the increased space charge. Thus, the current density at the center of the beam must decrease because the integral of the total beam intensity is equal to the beam current.

The oxygen partial pressure dependence, P_{O_2}, was investigated with the negative ion beam at 700° C using an admixture of oxygen in argon. The values of X_B for t = 1 hr at I = - 10μA with 10%, 50%, 80%, and 100% O_2 in argon are given in Figure 2. We note that, as P_{O_2} is reduced by a factor of 10, X_B decreases by only ≈ 18%. The explanation for this result is thought to depend upon the electron attachment probability to O and O_2.

As P_{O_2} decreases, the concentration of unattached electrons entering the oxide increases. We expect that the concentration of free electrons, η, will be given by

$$\eta = K_1 \exp(-\varepsilon_1/kT) + K_2 \exp(-\varepsilon_2/kT) \qquad (3)$$

where K is a constant and ε is the binding energy of an electron to an O or O_2 (electron affinity). In eq. 3, K will decrease as P_{O_2} increases and will depend upon the relative population of O and O_2. If the concentration of O stays relatively constant even though the concentration of O_2 decreases, since $\varepsilon_O > \varepsilon_{O_2}$, one might expect X_B to be only slightly dependent upon P_{O_2}. Because of eq. 3, at higher T for a given t and I, we should expect X_B to fall off. This is observed experimentally.

In these studies, a series of baseline control experiments were conducted The Si wafer rested on a quartz plate at a distance of 0.5 cm below the platinum needle and no external potential was applied to the system. However, directly beneath the needle, the oxide growth was enhanced. This was later found to be due to (i) a small remnant positive polarization potential in the quartz plate and sapphire standoffs of the apparatus and (ii) to a lesser extent the presence of platinum in the system.

In Figure 3, two sets of control experiments at 900° C with Si <111> substrates with zero applied potential are shown. The first set, which were performed near the beginning of the experimental work, reveal an enhanced peak oxidation rate compared to that expected in a standard oxidation furnace. The second set, conducted some months later with no changes in the experimental apparatus, reveal an even greater enhanced peak oxidation rate compared to the first set. It was anticipated that these unwanted electrical effects were associated with (i) electrical polarization in the apparatus due to the flow of current I and (ii) work function differences between dissimilar materials; i.e., the equivalent voltage for the system, V_{eq}, is given by

$$V_{eq} = V_{pol} + V_{WF} \qquad (4)$$

We expect that $V_{pol} >> V_{WF}$ and that the difference between set 1 and set 2 of Figure 3 is due to changes in V_{pol}. The measured volume conductivity at 900°C is $\sigma_v \approx 10^{-9} ohm^{-1} cm^{-1}$ while the DC resistance for a fully polarized quartz plate in the apparatus is $\approx 1.4 \times 10^7$ ohms which leads to an IR drop of $\approx$ 70 volts across the quartz plate. Thus, if internal polarization completely cancels this voltage drop during a run, the remnant field left in the system system will be $\lesssim$ -70 volts.

Figure 4 shows three oxide thickness profiles for Si <iii> substrates at 900° C with t = 2 hrs. Experiment #63 was an open-circuit control while #119 and #131 had +50V and +100V, respectively, applied to the needle. As #63 was the first experiment performed, the oxidation enhancement is indicative of the remnant polarization present in the quartz plate at that time. Experiment

#119 was conducted shortly thereafter and, because the +50V is applied in series with V_{pol}, the resulting thickness profile is further enhanced. On the other hand, experiment #131 was performed after a number of experiments utilizing a beam current of I = +5μA. We see that, for an applied voltage of +100V, substantially less enhancement is obtained than that found in experiment #119. This is because V_{pol} changed both magnitude and sign because of the positive ion current forced through the sample and the quartz plate.

Assuming a linear relationship between the percentage peak enhancement and the resultant voltage on the needle, one can estimate the voltage due to remnant polarization. Experiments #63 and #119 show 37% and 62% enhancement, respectively, which would lead to a V_{pol} = +74V which agrees quite well with the estimate of 70 volts obtained earlier.

4.2 Photo Enhancement

The purpose of the present work was to examine the extent to which a true photonic or optically induced enhancement mechanism is at work in silicon versus enhancement caused by local excess heating of the surface at the laser beam spot. In our study, a Lexel argon-ion laser was used to generate a photon flux of selectable energy and adjustable intensity. In the continuous beam, only one wavelength of the five most powerful lasing wavelengths was used at a time; i.e., 2.4 eV, 2.5 eV, 2.54 eV, 2.6 eV or 2.7 eV. The beam was directed into a thermal oxidation furnace so as to hit the center surface of a vertical sample of silicon (see Figure 5) at a few degrees off of the normal to avoid multiple-reflection measurement errors of the beam spot power density. The silicon sample was otherwise exposed to typical thermal oxidation processing.

Typical oxidation conditions were two hours at 900° C in dry O_2 which resulted in control oxides of ≈ 450 A and ≈ 300 A for the <111> and <100> orientations, respectively. The peak oxidation enhancement, measured via ellipsometry, varied linearly with beam power density and was in the 3% to 30% range, as ilustrated in Figure 6. We note that the enhancement is greater for the <100> than for the <111> Si which is opposite to that expected for a purely thermal result.

Experiments were also carried out at low but constant beam power density while the photon flux was varied with the photon energy in the range 2.4 eV to 2.7 eV. At constant beam power P_o the photon flux F is directly proportional to the optical wavelength λ according to

$$F = \left(\frac{P_o}{hc}\right) \lambda \qquad (5)$$

where c is the speed of light and h is Planck's constant. Thus, at long wavelengths, more photons arrive at, and interact with, the active silicon surface than do so at shorter wavelengths. Figure 7 illustrates typical results for both <111> and <100> silicon and shows the percent oxidation enhancement to increase linearly with beam wavelength and thus with photon flux.

A variation of these two experiments was performed to conclusively demonstrate the nature of the photonic mechanism. Here, the power of the longer wavelength beam P_L was lowered to reduce F_L to the same value as that from a shorter wavelength beam operating at P_s; i.e., we require that

$$\frac{P_L}{P_s} = \frac{\lambda_s}{\lambda_L} \qquad (6)$$

If a photonic mechanism of oxidation enhancement is indeed operative, the amount of enhancement produced by both wavelengths should now be identical. The results shown in Figure 8 confirm this hypothesis.

A great deal of care must be exercised over the course of a typical 2 hour oxidation experiment both in measuring, and in maintaining constant, the power density of the laser beam. This is a prerequisite to observing the photonic effect with the precision of the experiments becoming more critical as the wavelength difference, $\Delta\lambda = \left| \lambda_i - \lambda_j \right|$, decreases. In addition, as the beam power density increases, more heating of the silicon surface is likely to occur, eventually washing out the photonic effect. Preliminary experiments show that, as the beam power density increases for fixed $\Delta\lambda$, this is indeed the case.

FIGURE 1: Oxide thickness vs position on wafer for 700° C oxidations.

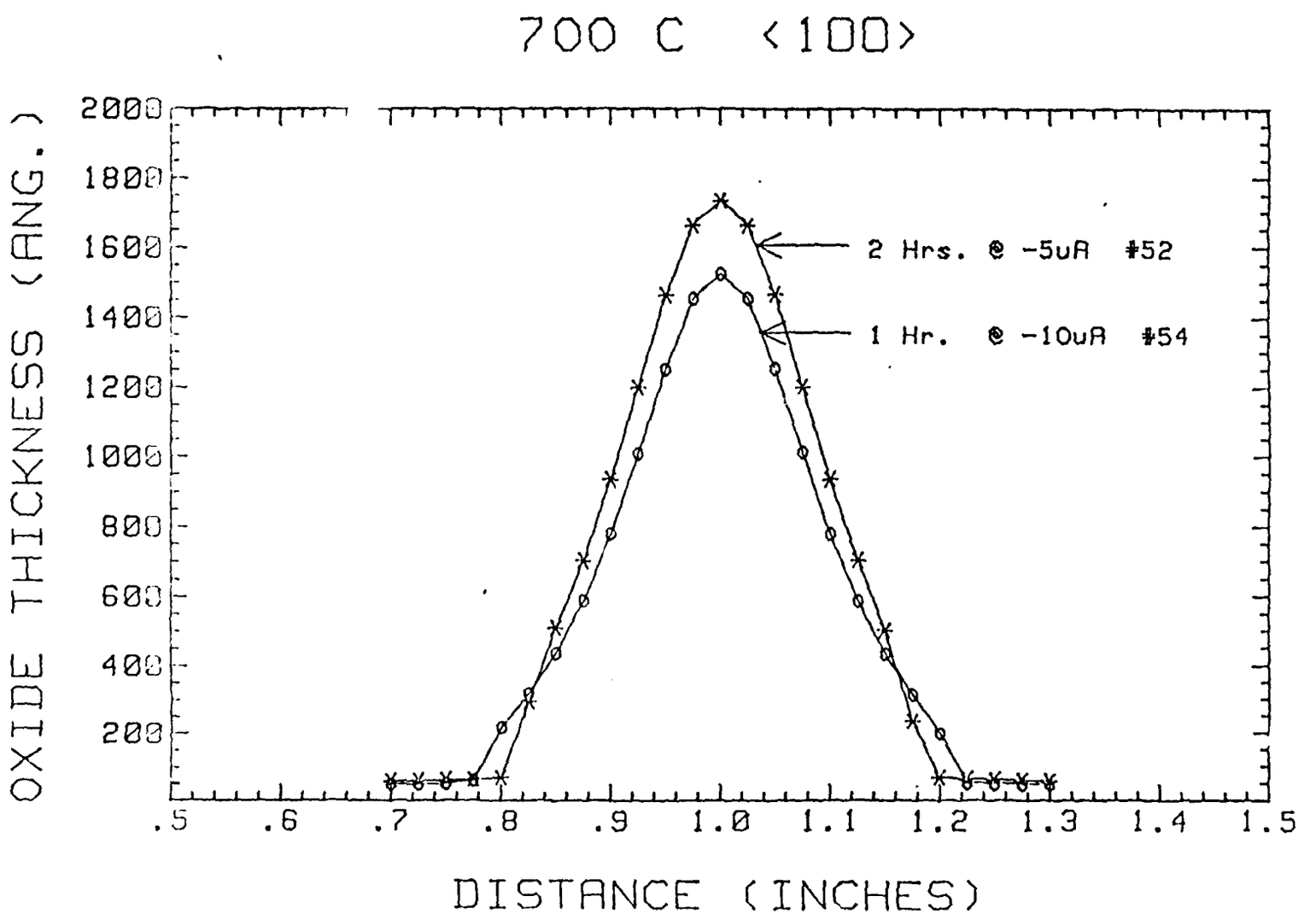
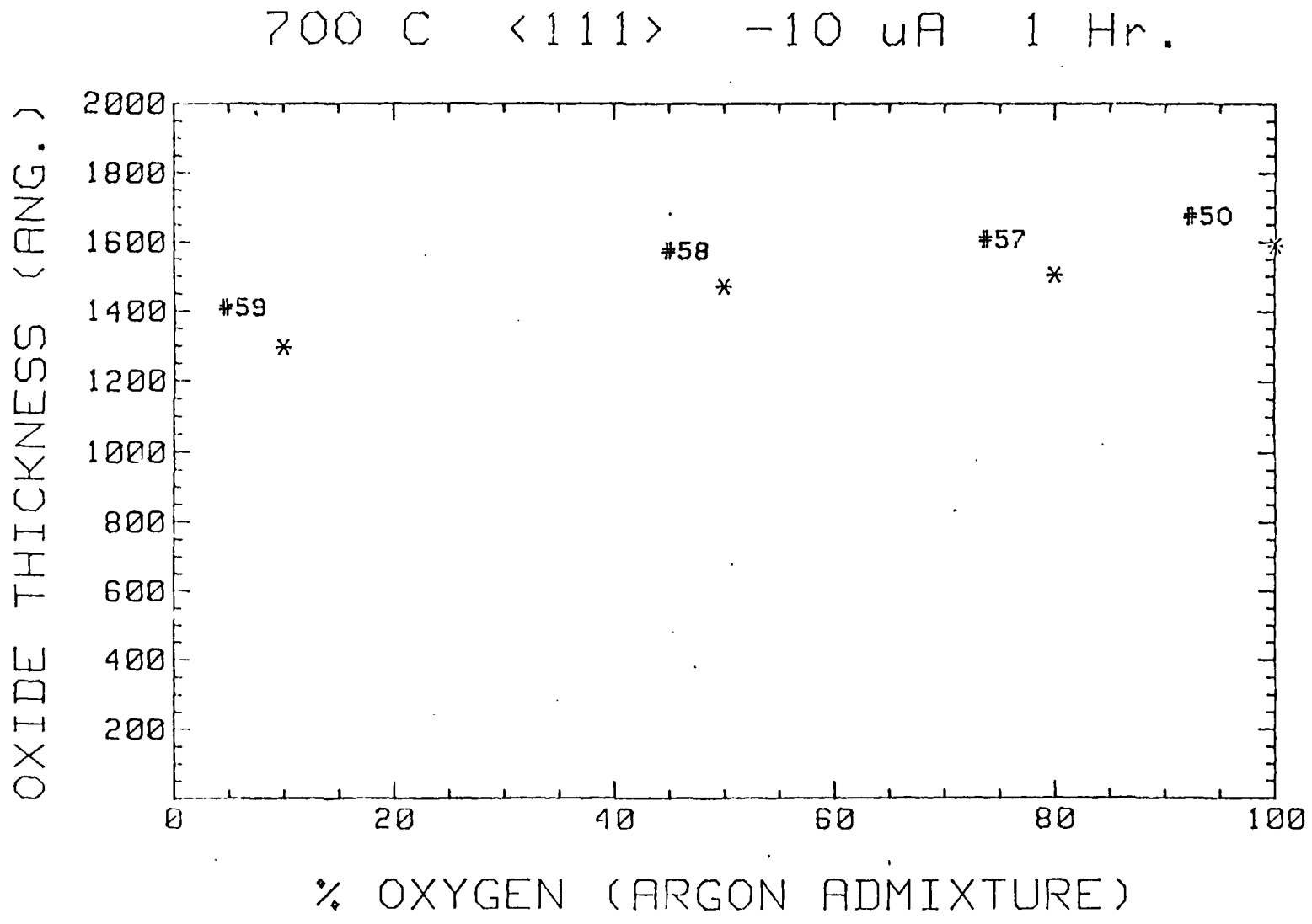


FIGURE 2: Dependence of oxide thickness on oxygen partial pressure for 700° C, 60' oxidations.



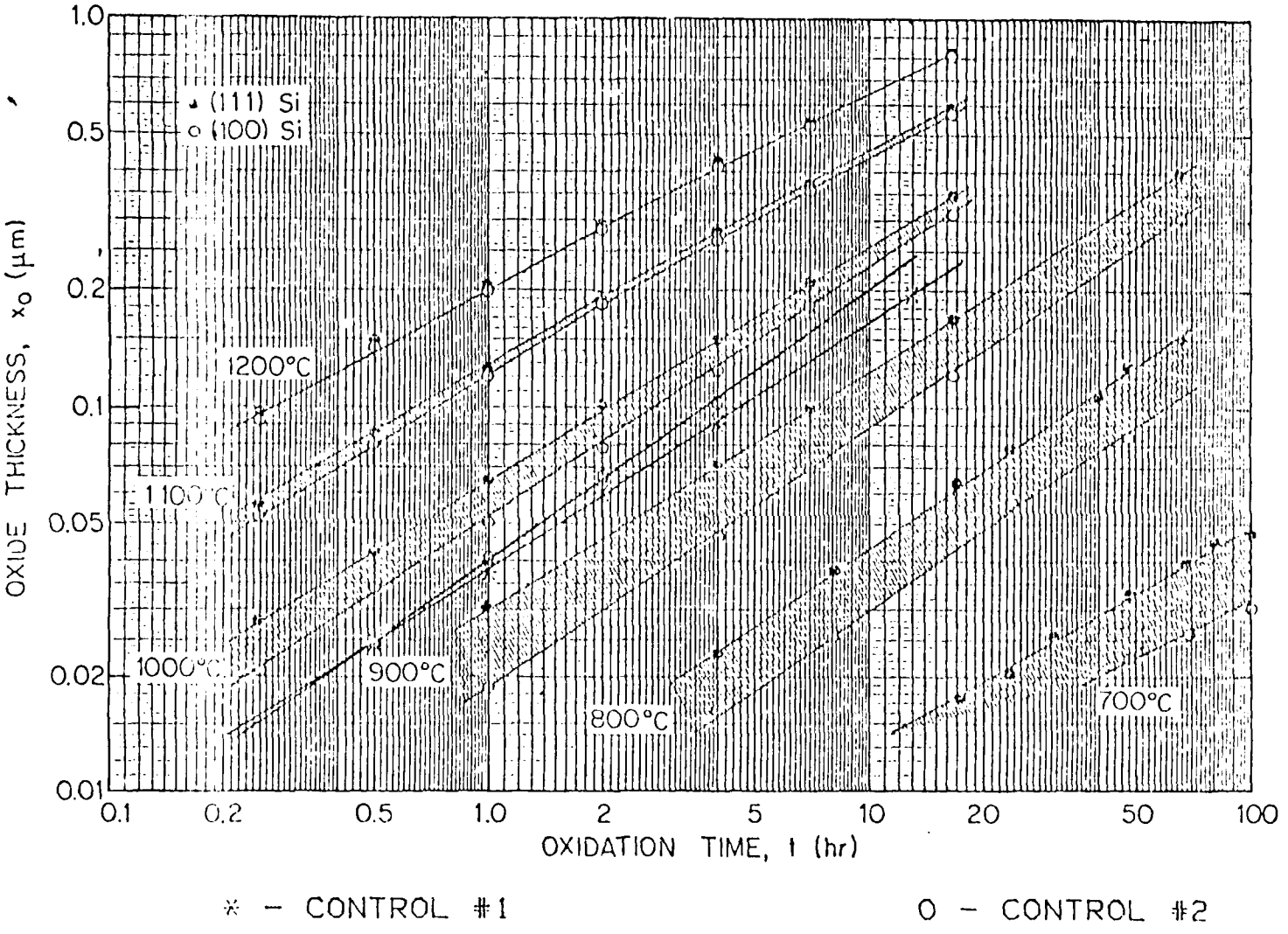


FIGURE 3: Relationship of enhanced oxidation kinetic results to "normal" oxidation data.

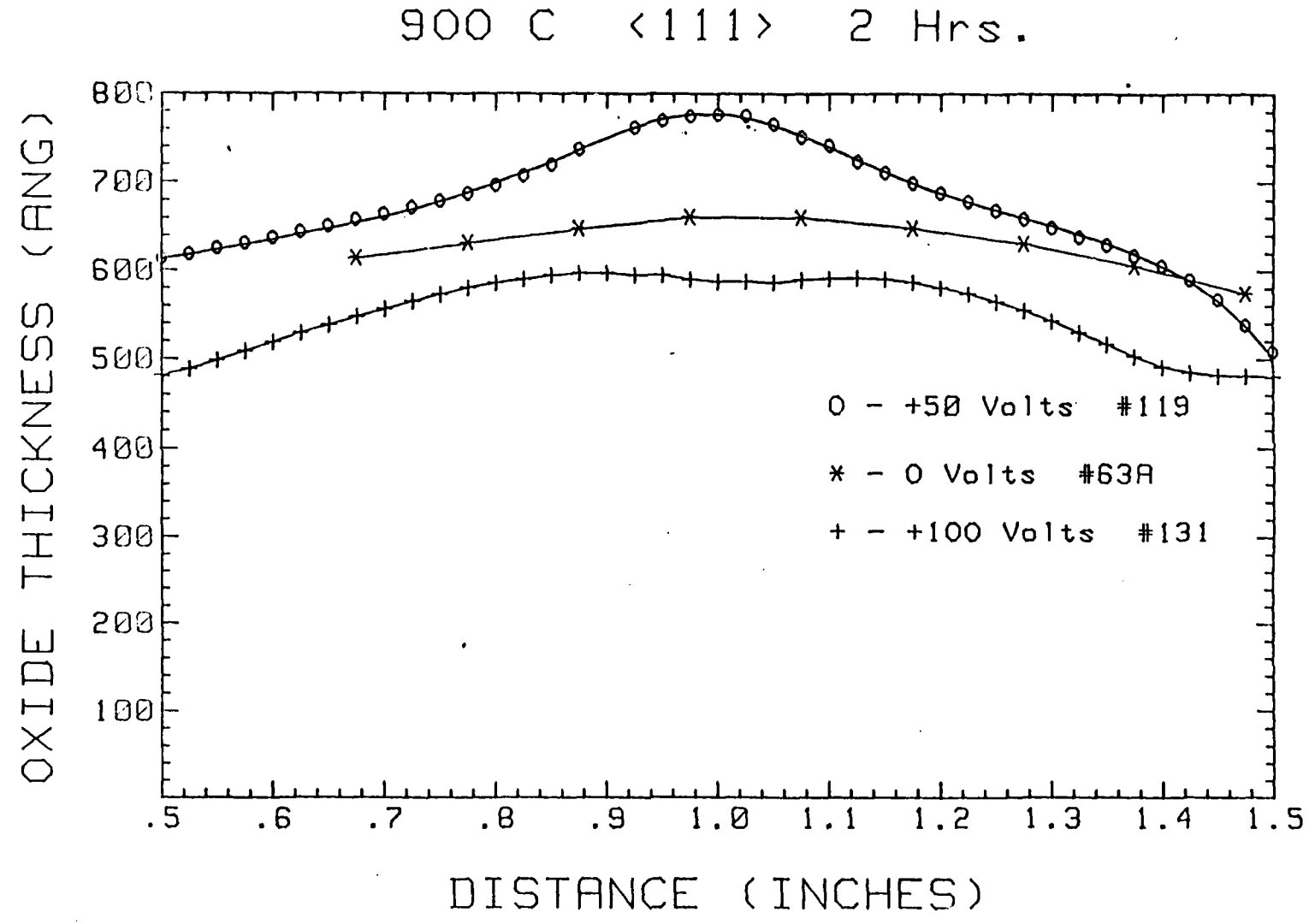


FIGURE 4: Oxide thickness profiles for 900° C, <111>, 2 hr oxidations.

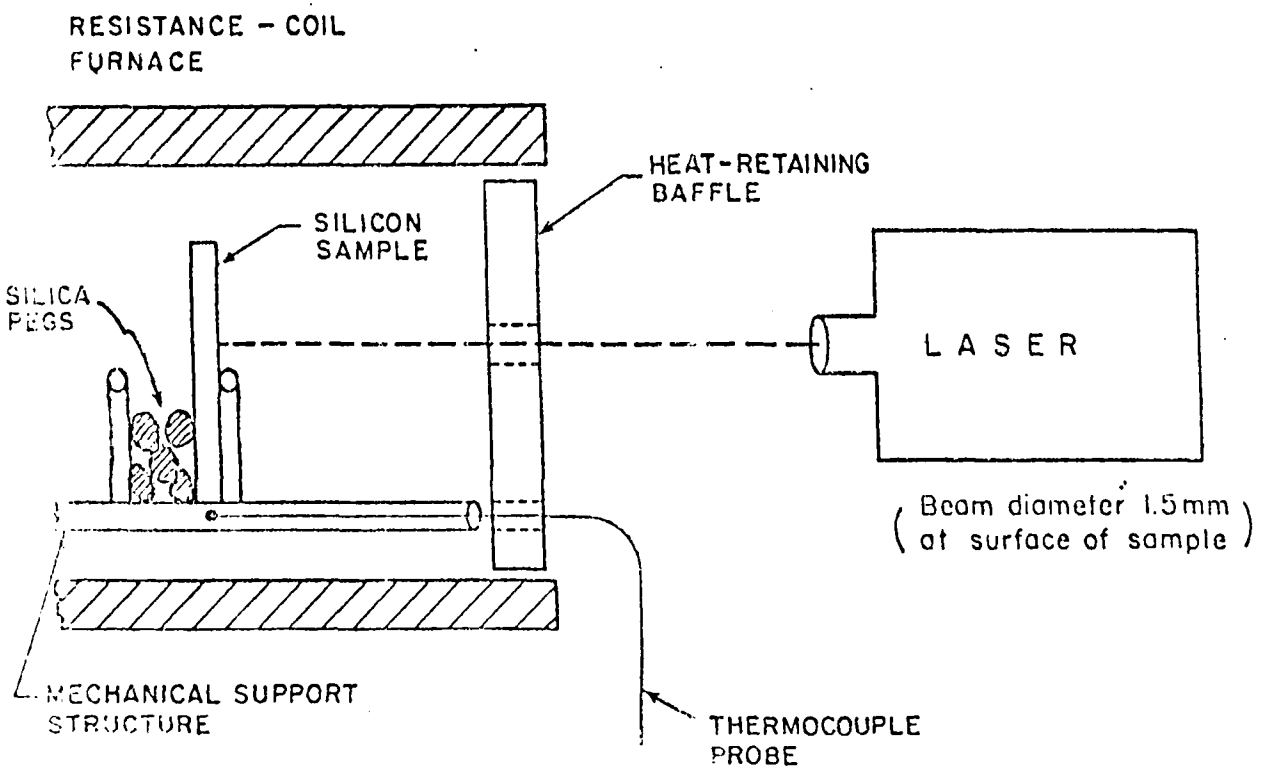


FIGURE 5: Experimental set-up for laser enhanced oxidation studies.

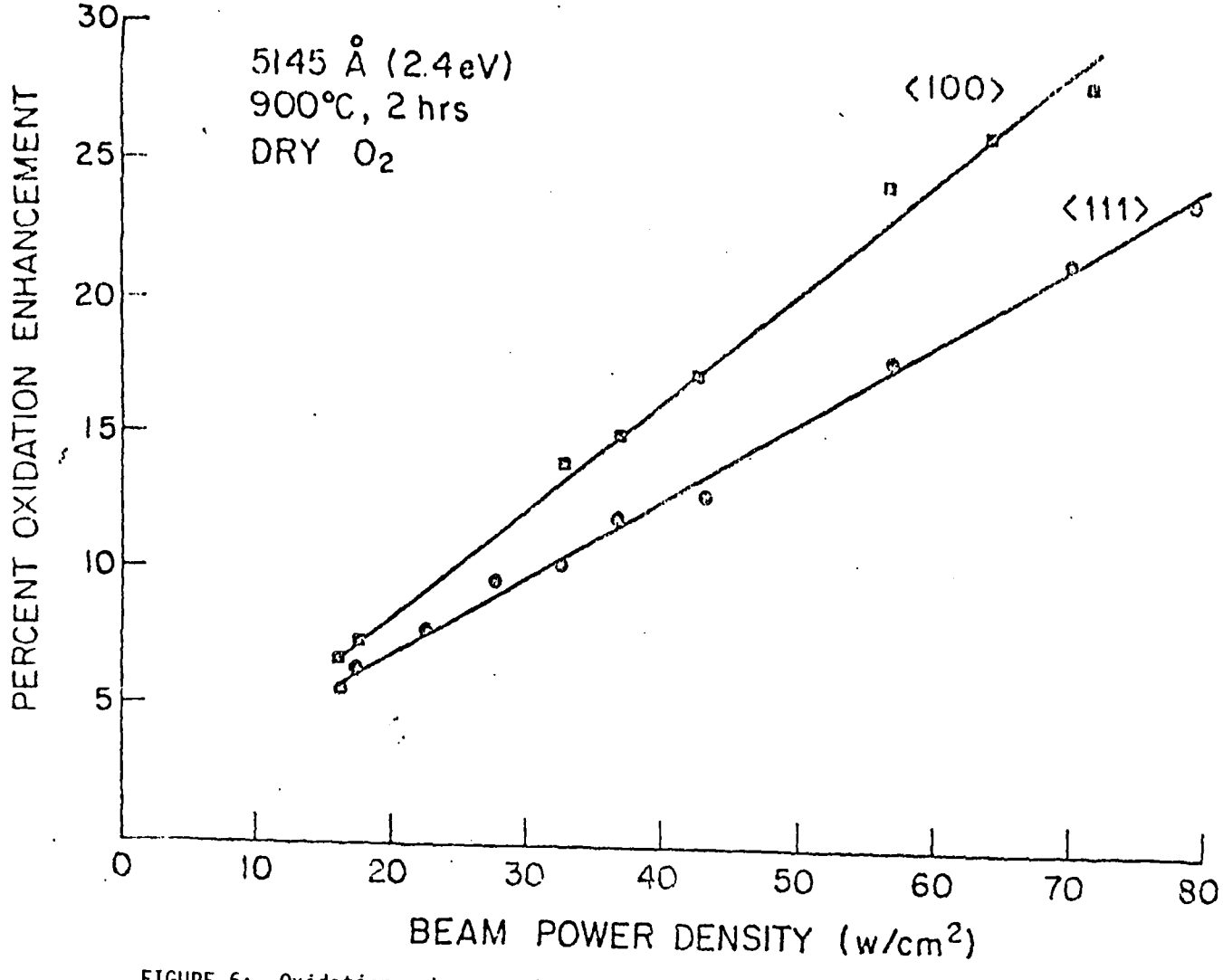


FIGURE 6· Oxidation enhancement verses laser beam power density at 900° C.

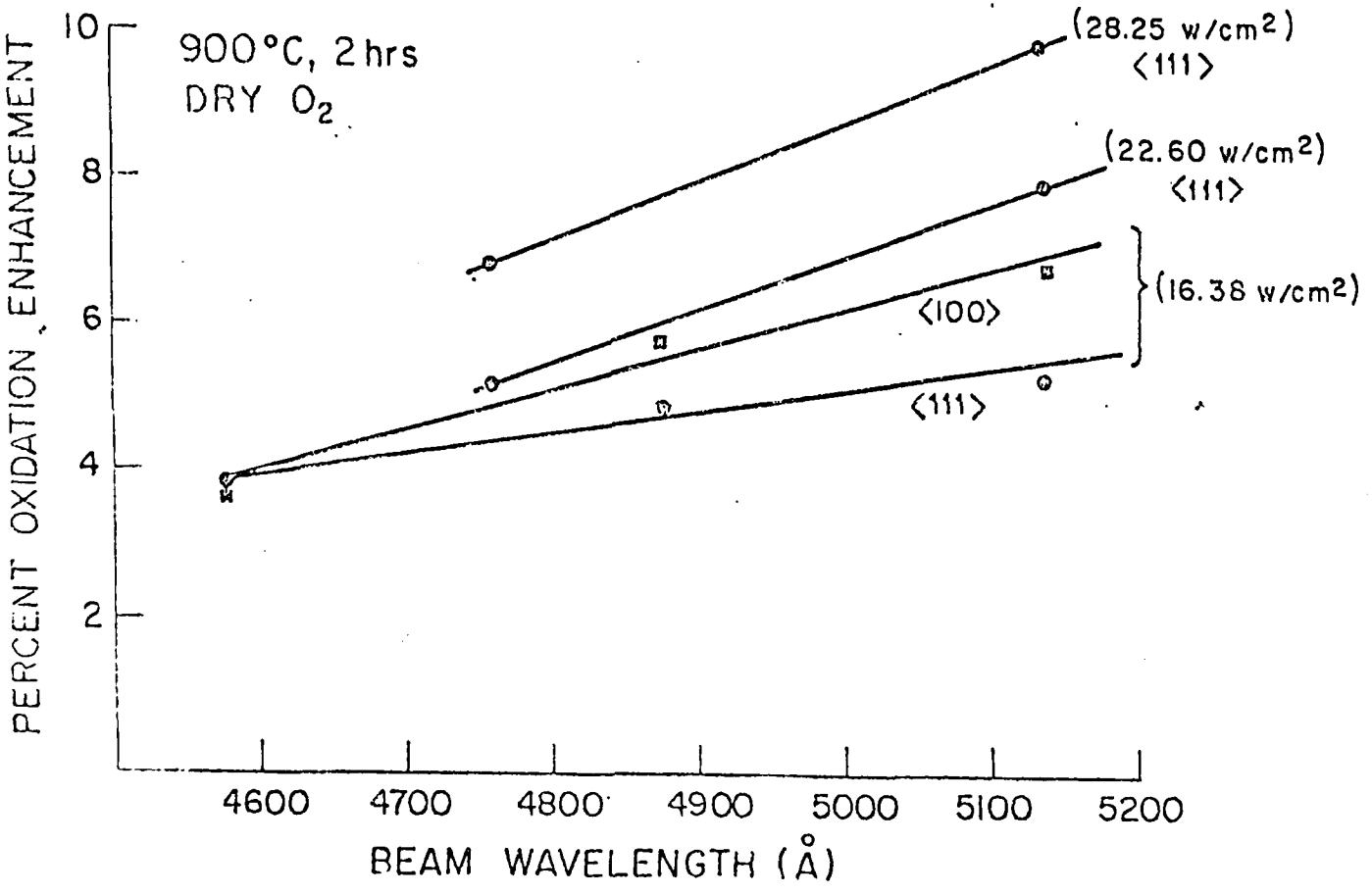


FIGURE 7: Oxidation enhancement verses laser beam wavelength at 900° C.

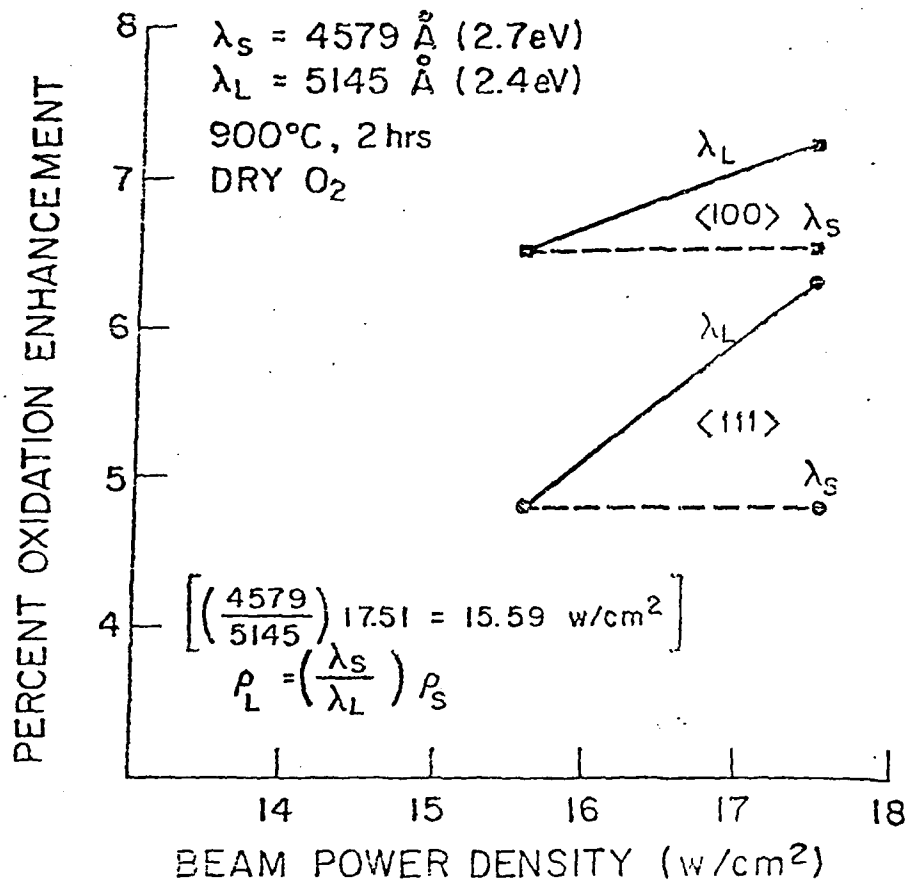


FIGURE 8: Oxidation enhancement verses laser beam power density for two laser wavelengths.

5. Si/SiO_2 INTERFACE CHARGES

A. AKINWANDE, C. HO, J. PLUMMER

In the last annual report, it was demonstrated: (a) as grown charges follow the Deal N_F triangle qualitatively but a careful examination of the results indicate a breakpoint at a temp of about 950° C. This led us to suggest that there may be a viscoelastic relaxation process occurring at the interface at the same time as charge generation during the oxidation process (Figure 1); (b) annealed charges appear not to show the temperature independence that the bottom part of the N_F triangle would suggest. There seems to be a break point at about 950° C also. This led us to suggest that the anneal process may be a viscoelastic decay process (Figure 2); (c) As confirmation of the fact that the annealed charges are not independent of temperature, thermal cycling experiments were carried out on (111) Si wafers oxidized in dry O_2 at 1000° C for 75 minutes. These wafers were later annealed in argon (< 2 ppm H_2O) and cycled between 900° C and 1100° C. The results did show that oxide charges do thermally cycle under the conditions given (Figure 3).

Since the above summarized experiments, numerous experiments have been carried out to answer some of the questions raised and attempts have also been made to develop theoretical tools to model the processes. The major accomplishments over the last few months are itemized below:

(1) A fast pull technique was developed to enable a quench of Si wafers from processing temperature to room temperature. This set up is shown in Figure 4. Quench durations of < 3 secs have generally been achieved.

(2) In the first set of experiments using the new experimental set-up, in oxides were grown at 1000° C in dry O_2 for 75 mins and were fast pulled (≈ 2 sec pull). They were subsequently annealed at various temperatures (800° C, 900° C and 1000° C) in argon which has < 1 ppm H_2O. The results are as shown in Figures 5, 6 and 7. From these results, the anneal process appears to be exponential with a time constant which decreases with temperature. The anneal process saturates to a final value which also decreases with temperature. Finally, this has led to a suggestion that the anneal kinetics may be described by:

$$N_f(t) = (N_f(o) - N_{fe}(T)) \exp\left(^{-t}/\tau(T)\right) + N_{fe}(T) \qquad (1)$$

where

$$\tau(T) = K \exp(Ea/kT) \qquad (2)$$

In order to explain this behavior, we favor a model which invokes a maxwellian viscoelastic relaxation process at the Si/SiO_2 interface. This process relieves the strain/stress at the interface. This implies that we must make an a priori assumption that strain/stress generated by the lack of free volume during the oxidation process is the origin of oxide charges. It must be reiterated though that this is just one of many possible models and careful further experimentation is required.

We have also investigated a situation in which the viscoelastic process is not maxwellian. This would result in a situation where the fictive "growth" temperature of the oxide is different from the anneal temperature [1]. It is expected under such circumstances that the anneal time constant would be a function of the processing

history of the Si/SiO_2 wafers. Preliminary experiments are being carried out to test this effect.

(3) The second set of recent experiments were to reproduce the thermal cycling of oxide charges under different anneal conditions (i.e., temperature). Oxides were grown on (111) and (100) Si Cz wafers at 1000° C in dry O_2 for 75 mins. They were subjected to 20 min pre heat in Argon prior to oxidation, 20 min 1% HCl/Ar etch + 20 min purge in Argon at 1000° C. The wafers were fast pulled from the oxidizing ambient (≈ 2 sec) and were subsequently given anneals in argon and cycled between 800° C and 1100° C. As the results shown in Figure 8 indicate, the charges do thermally cycle in argon on both orientations. It should be noted that the annealed charges at 800° C for (111) wafers are greater than the as grown values at 1000° C. This observation coupled with the fact that the charges reproduce under thermal cycling has led to the suggestion that there may be a reversible reaction going on at the interface between Si and SiO_2, that results in an equilibrium value of oxide charges for a particular temperature. Attempts have been made to formulate this problem mathematically and results thus far indicate chat more careful studies are required.

(4) The third set of new experiments were to study the as-grown charge kinetics. As we suggested earlier, it has been suggested in the literature [2] there may be a possibility that during an oxidation process, there is simultaneous generation and annihilation (anneal) of oxide charges at the Si/SiO_2 interface. The problem was formulated mathematically under the assumptions that: (a) there is a

distribution of oxide charges in the oxide with the highest value at the interface; (b) charges are generated as the interface moves past the point in question in the oxide; (c) charges are rather immobile; (d) charges at a point in the oxide anneal with an exponential decay starting from the time of generation, i.e., the time the interface moved past the point in question. The time constant would be what is expected from a viscoelastic relaxation

$$t = \frac{\eta(T)}{G} \qquad (3)$$

and, (e) a weighted sum of the charges is taken. The dependence this model would predict on oxide thickness is as shown in Figure 9. Preliminary experiments have been carried out and the results for (111) Si wafers are shown in Figure 10. It is our belief that by extension of the domain of the experiment, either by growing thicker oxides or growing oxides at higher temperature where T would be shorter, the peak predicted by the model would be observed. Experimentation is in progress.

(5) The fourth set of experiments were to investigate the as grown charges as a function of oxidation temperature at constant oxide thickness (600Å). As shown in Figure 11, we reproduce earlier results in which we observe a breakpoint at a temperature of about 950°C.

In order to conclude this report, it can be seen that many more questions have been raised than have been answered. We have thus set the following priorities:

(a) Repeat the thermal cycling experiments using both CZ and FZ Si wafers. This would eliminate any questions as to the effect of dissolved oxygen on Si on the Si/SiO_2 interface.

(b) Study the anneal kinetics from the point of view of a reversible process.

(c) Complete the study of the effect of thermal history (i.e., oxidation) on the anneal process.

(d) Determine if the anneal process which seems to be limited by a bond breaking/thermal mechanism can be aided by an external source of energy such as UV light at low temperature to shorten the decay time constant.

(e) Complete the experiments on the generation mechanisms.

References

[1] G. Hetherinton, K.H. Jack and J.C. Kennedy, "The Viscosity of Viterous Silica", Physics and Chemistry of Glasses, Vol 5, No. 5, p. 130, Oct. 1964.

[2] M. Hamasaki, "Generation Kinetics of Oxide Charges and Surface States During OXidation of Silicon"

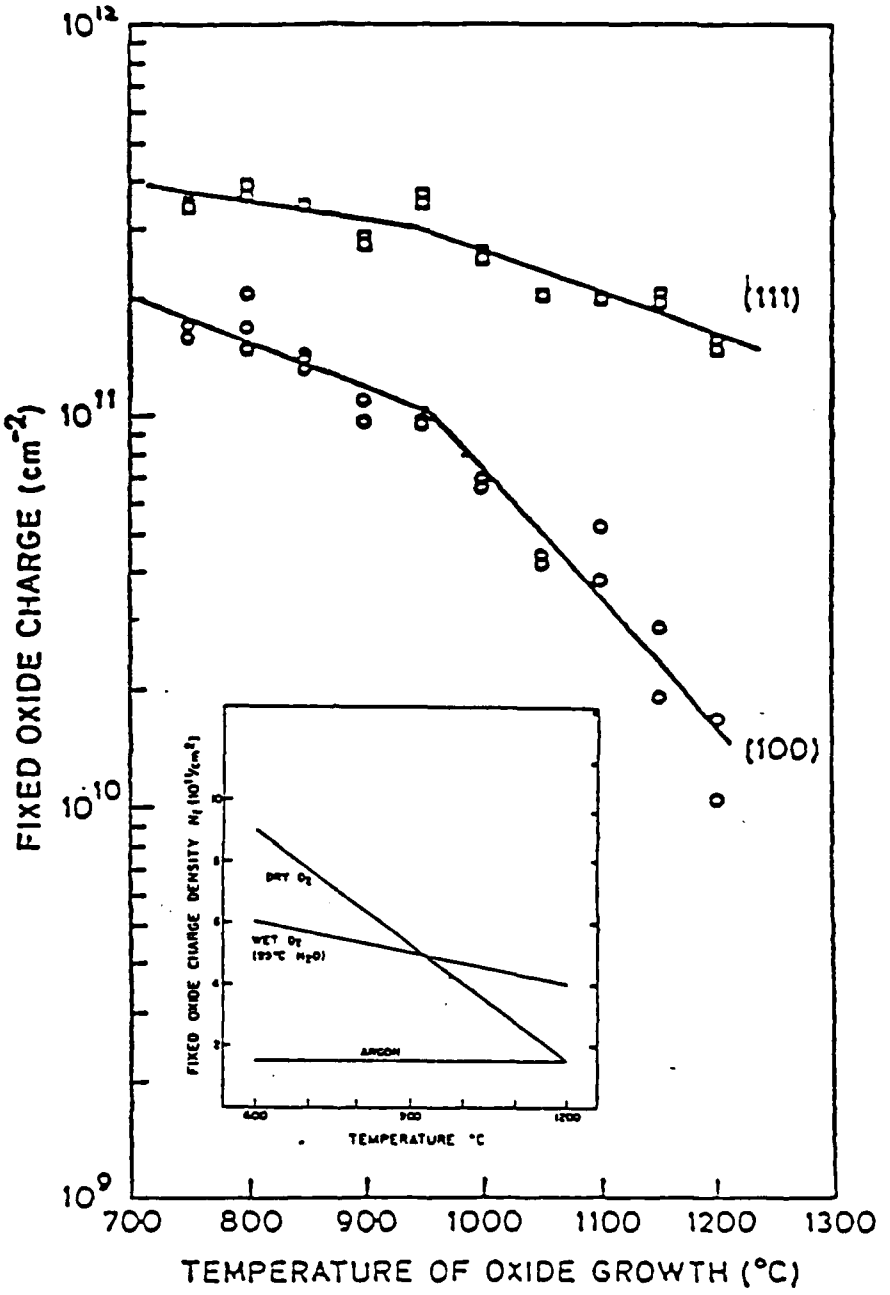


FIGURE 1: As-grown (fast pulled) fixed oxide charge density N_f vs. growth temperature for (111) and (100) wafers. While the general behavior expected from the N_f triangle is observed, a distinct break also occurs at $\sim 950^0$ C.

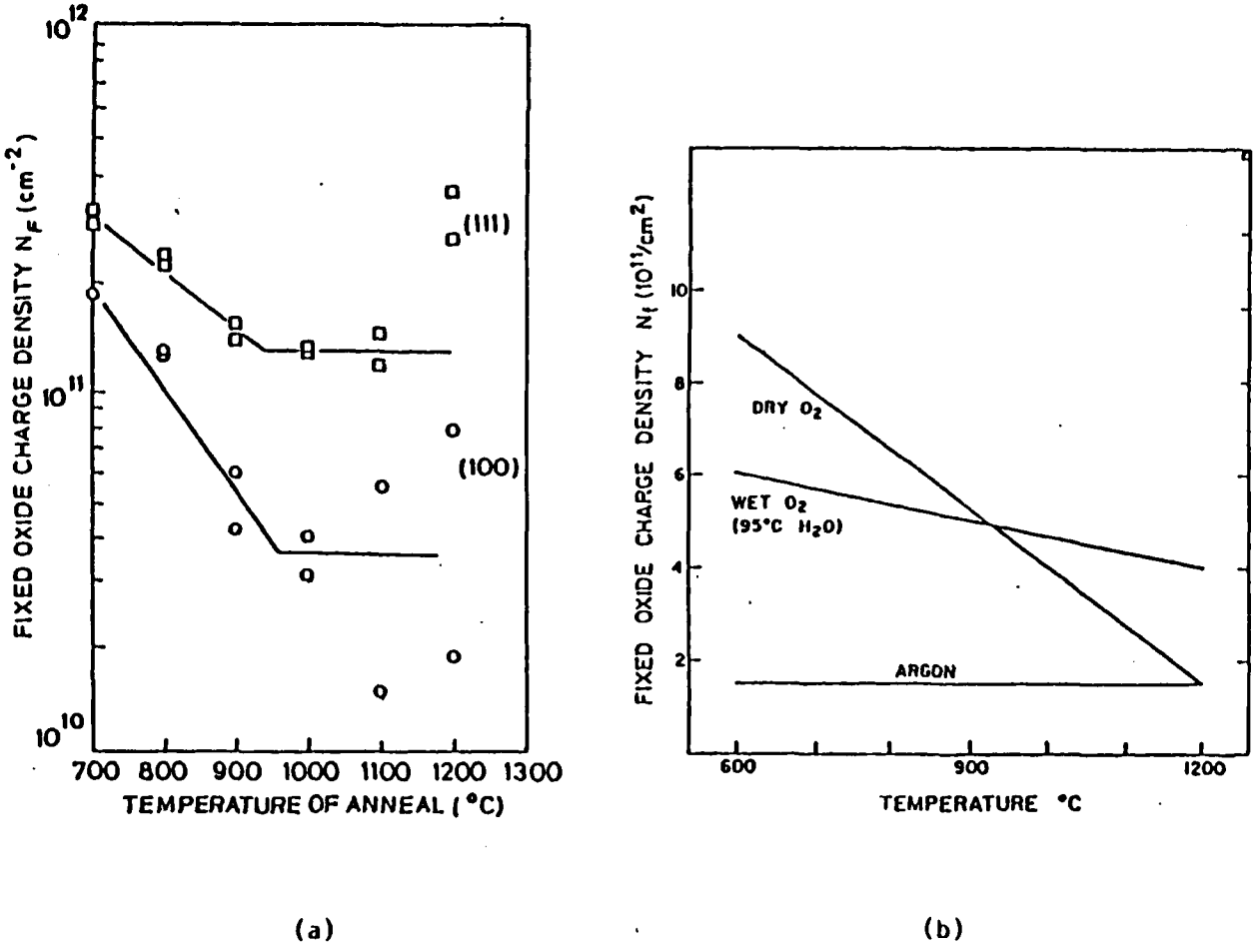


FIGURE 2: Fixed oxide charge density N_f vs. anneal temperature in argon for (111) and (100) wafers. (a) Expt. (b) N_f triangle. The times were adjusted at each temperature to reach an equilibrium value.

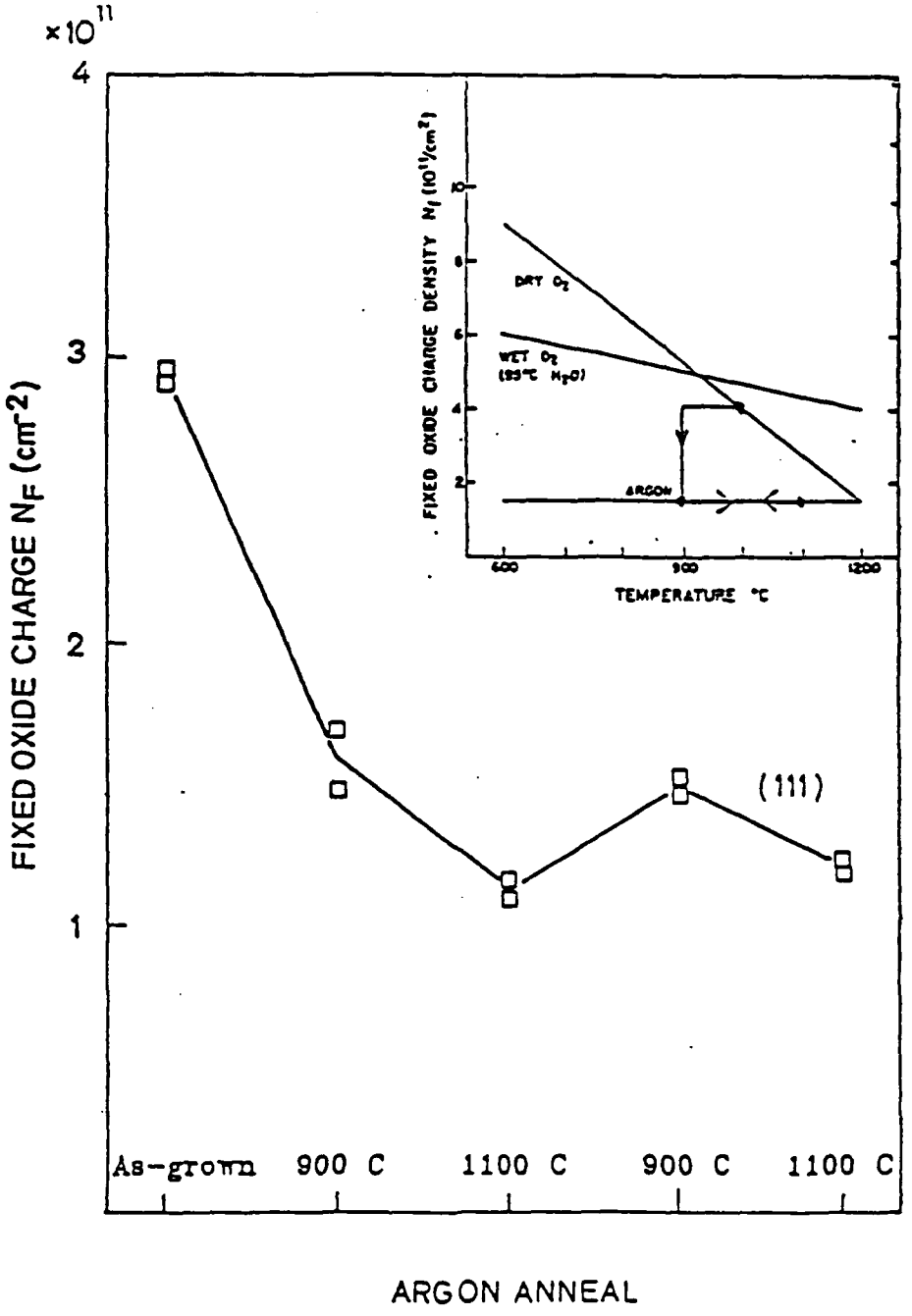


FIGURE 3: Fixed oxide charge density N_f vs. Argon anneal cycle for (111) wafers thermally cycled between 900^{o} C and 1100^{o} C in Ar. This illustrates that the bottom part of the N_f triangle is not flat.

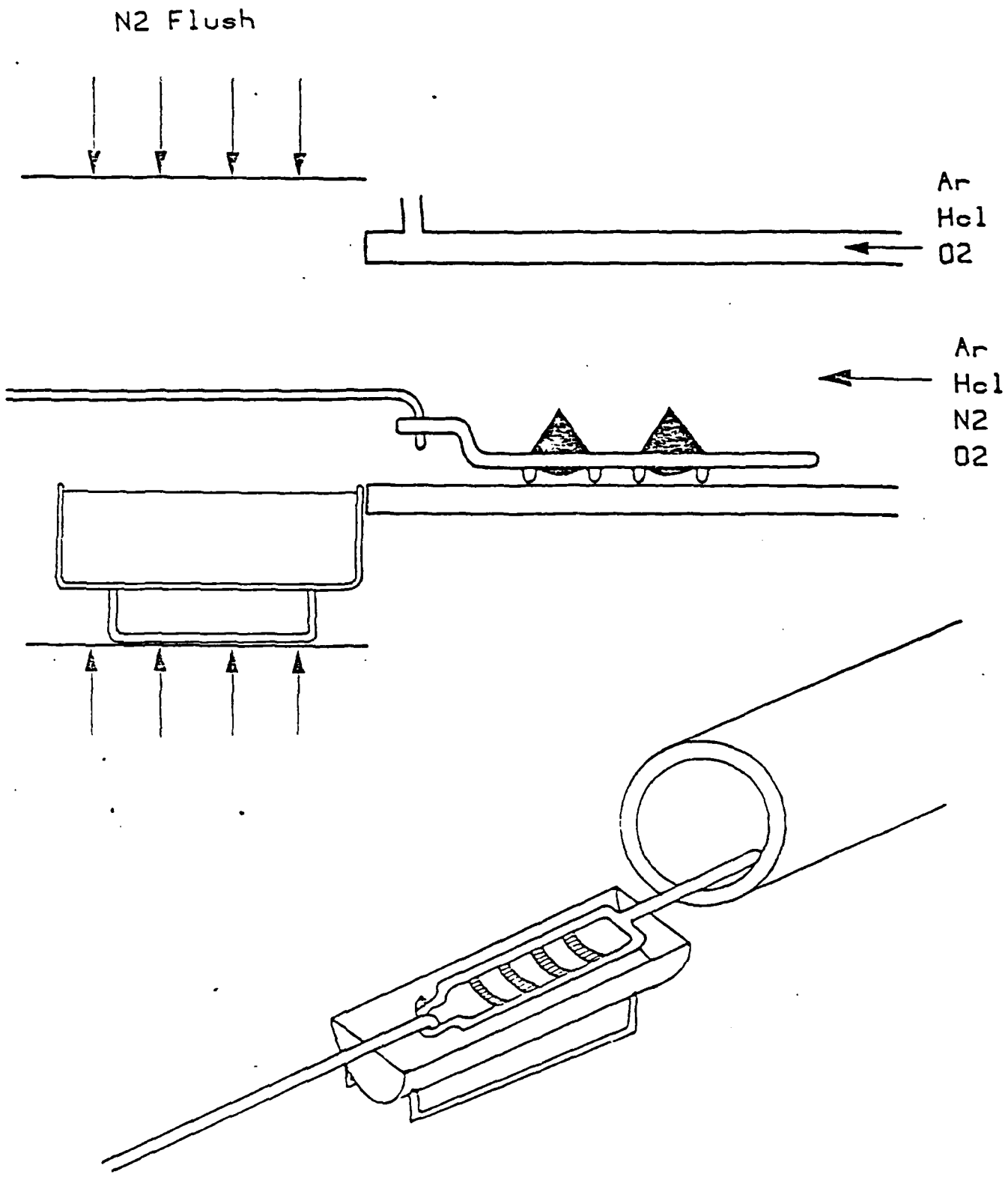


FIGURE 4: Schematic representation of fast pull apparatus designed to permit < 3 sec quench times from oxidation temperature to room temperature.

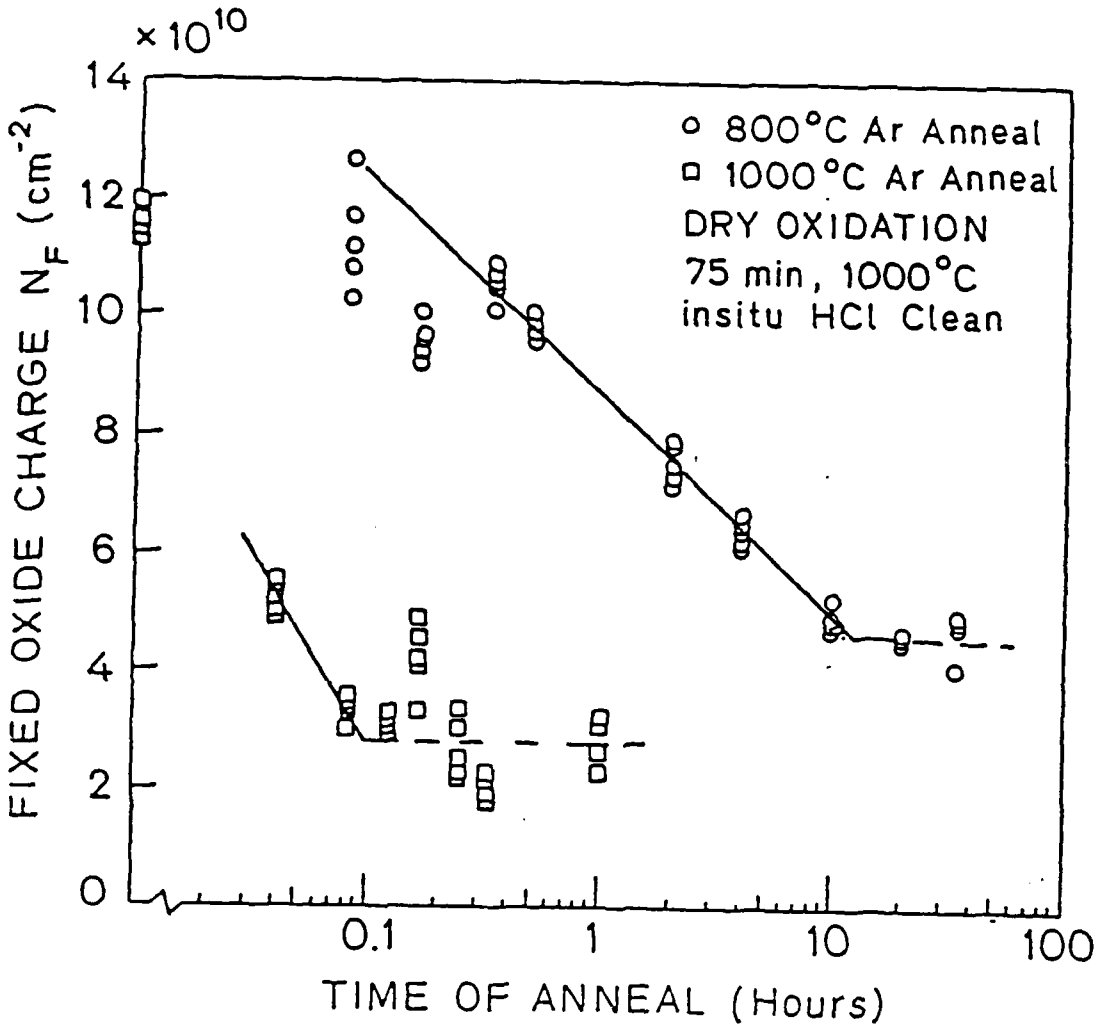


FIGURE 5: Example of anneal kinetics of oxide charges for (100) wafers in Argon at 800° C and 1000° C. Note that both decay time constants and the final annealed values are different at the two temperatures.

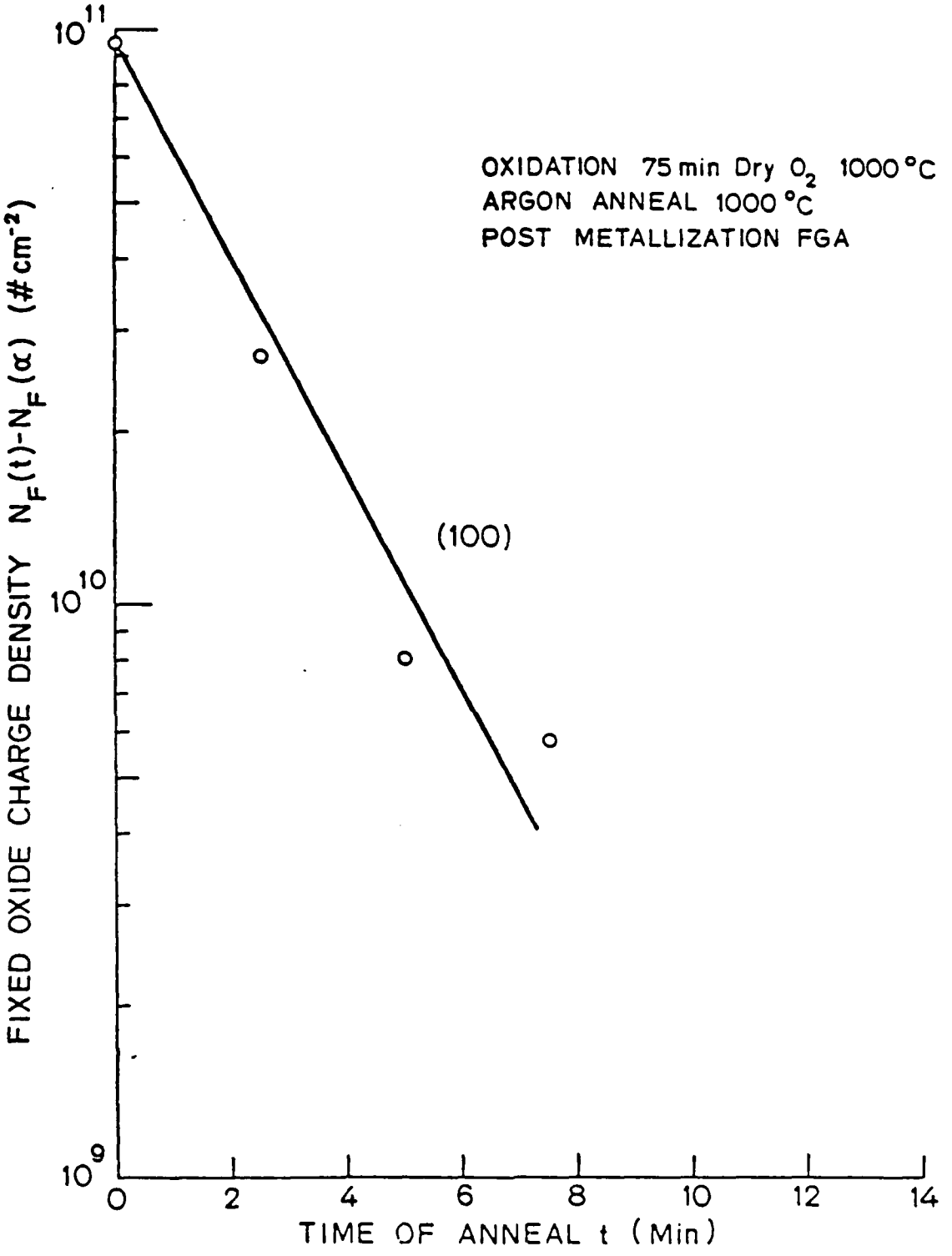


FIGURE 6: Anneal kinetics of N_f at 1000° C in Ar, for wafers oxidized at 1000° C in dry O_2.

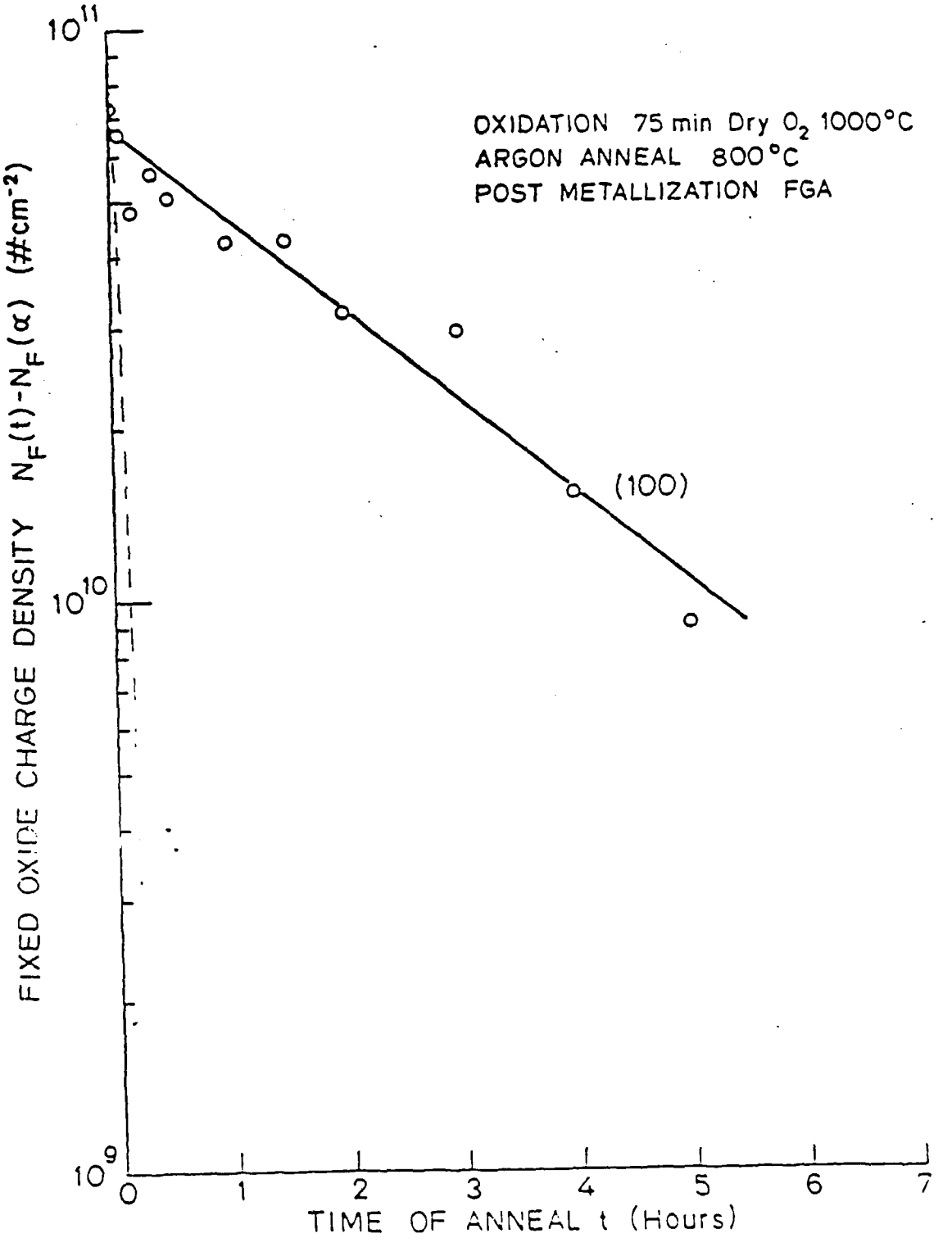


FIGURE 7: Anneal kinetics of N_f at 800° C in Ar, for wafers oxidized at 1000° C in dry O_2.

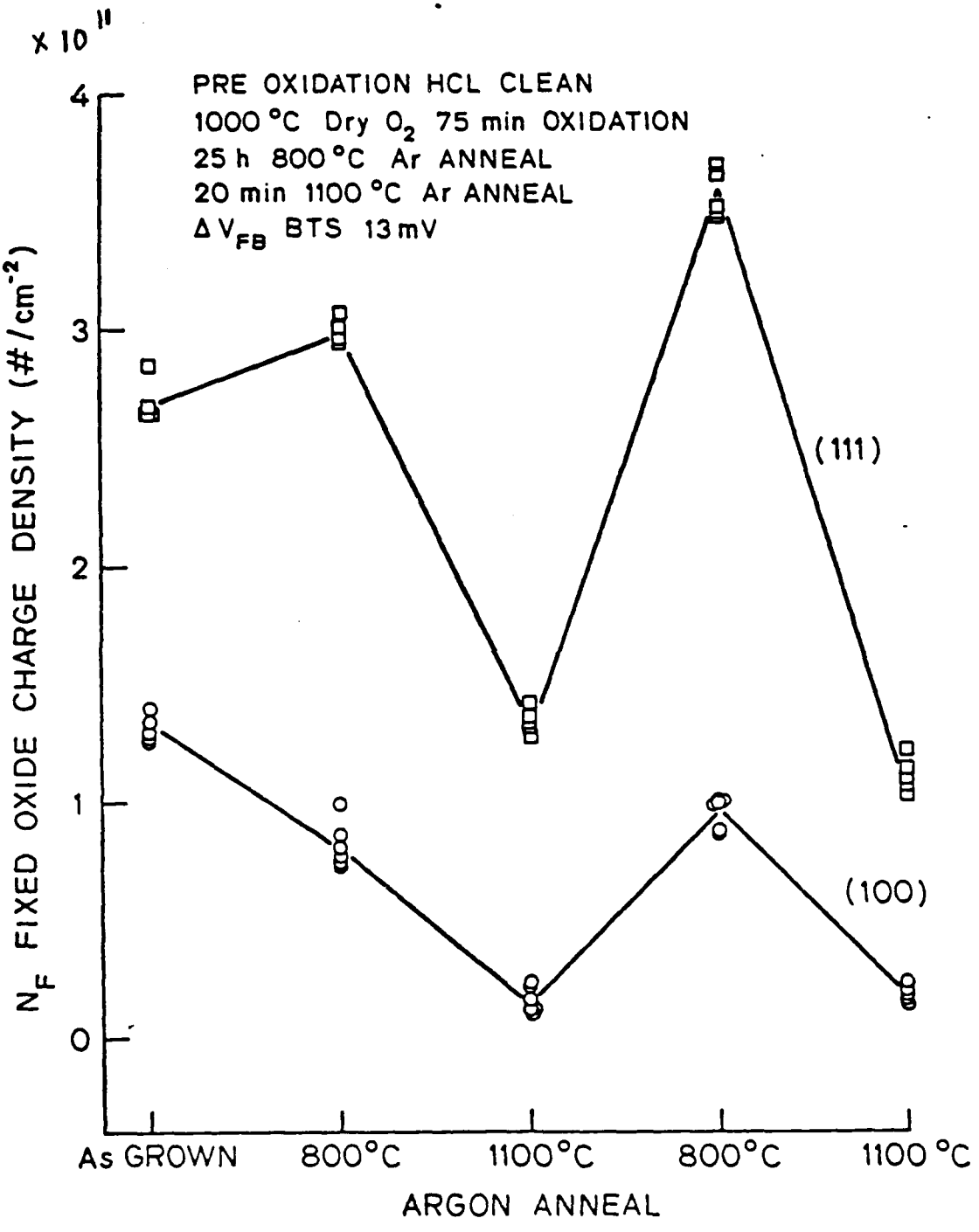


FIGURE 8: Thermal cycling of final Ar annealed value of N_f as the annealing temperature is charged from 800° C to 1100° C.

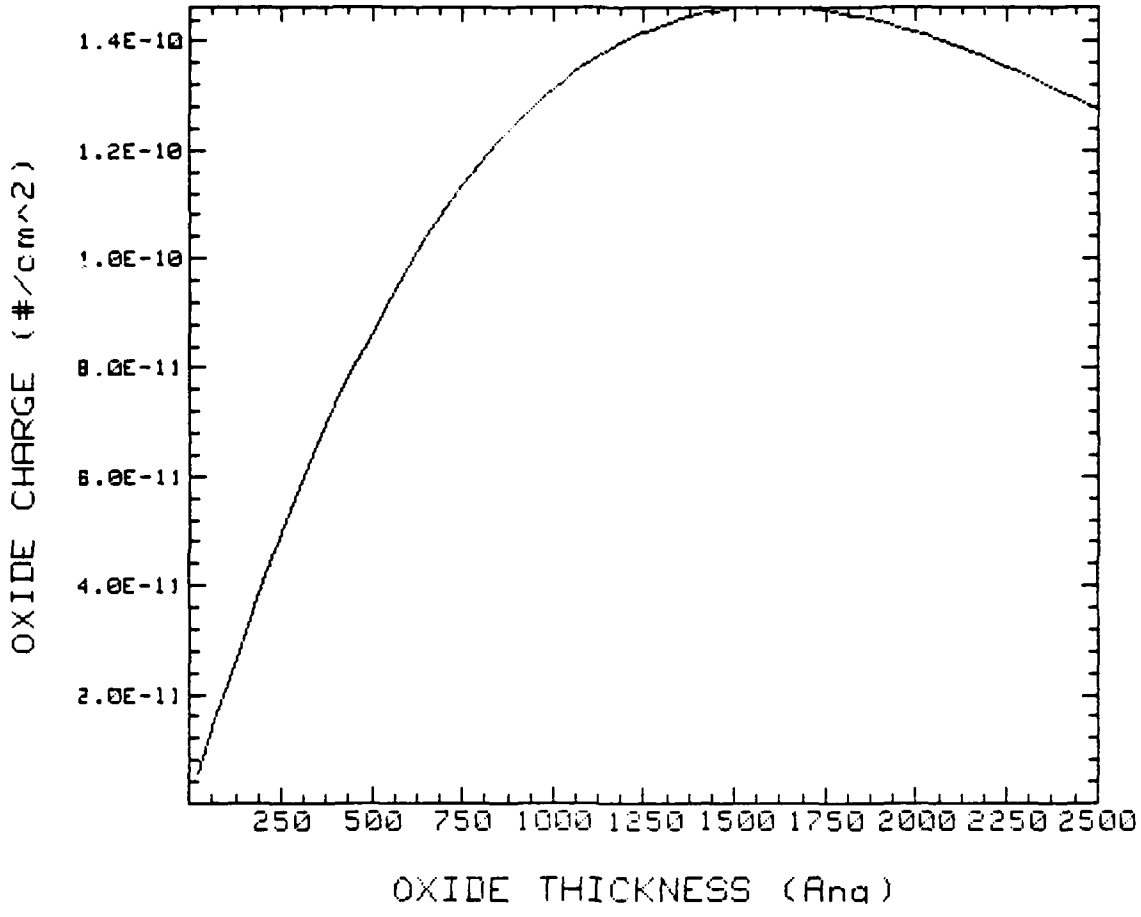


FIGURE 9: Predicted dependence of N_f on oxide thickness based upon the model described in the text, and a visco-elastic relaxation time of 4 hours.

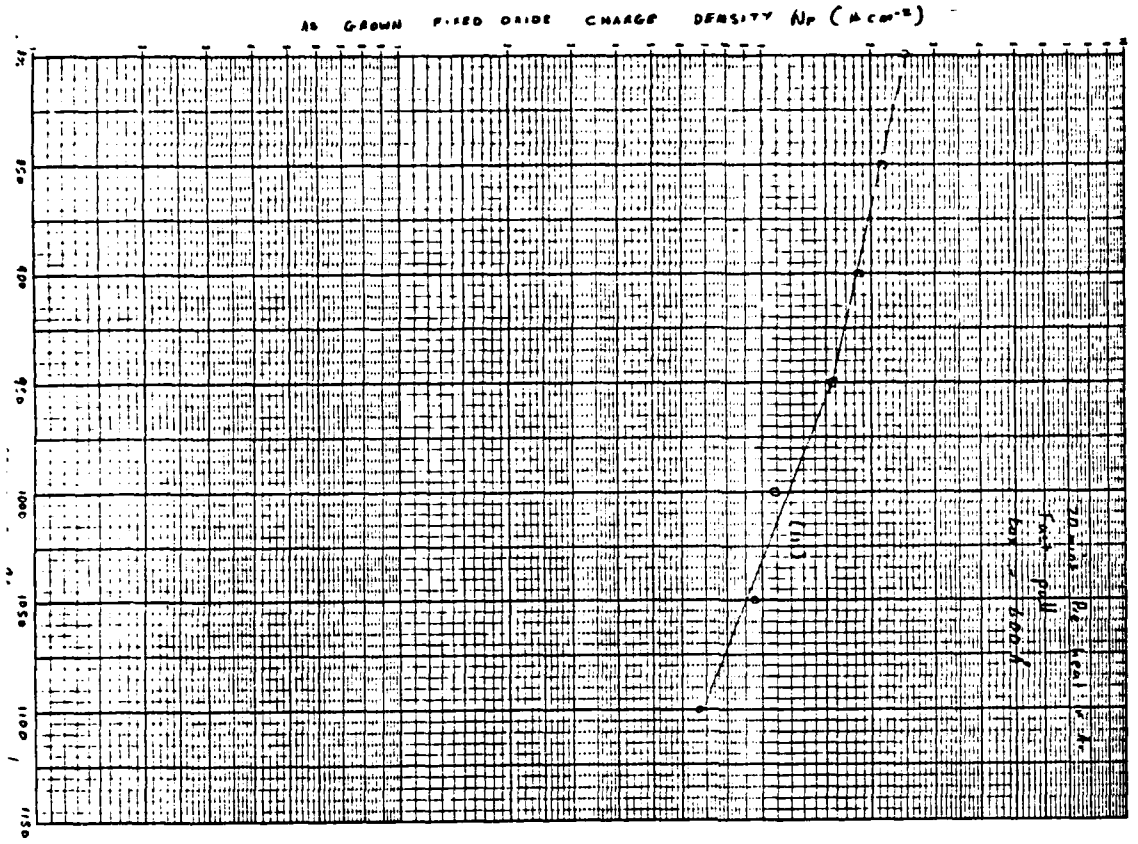


FIGURE 11: As grown N_f charge densities as a function of oxidation T for oxide grown to a similar thickness (600Å) at each T. Note the breakpoint at ~ 950° C.

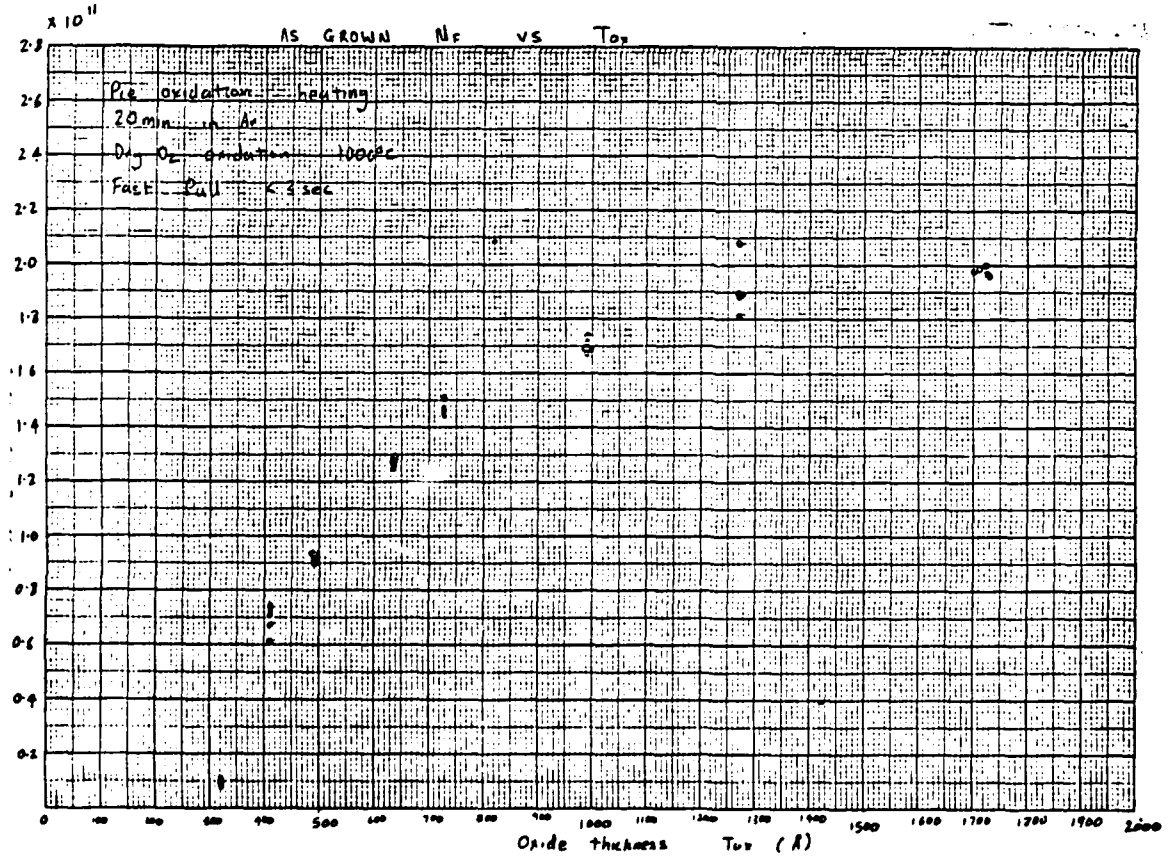


FIGURE 10: Experimental dependence of N_f oxide thickness for wafers oxidized at 1000° C in dry O_2.

6. MEASUREMENT AND CHARACTERIZATION OF THIN OXIDES ON POLYSILICON

E. KUTLU, K. SARASWAT, J. PLUMMER

Our first experiments on the oxidation of plysilicon showed that the oxidation kinetics of poly are different from the oxidation kinetics of single crystal silicon mostly during the linear regime [1]. It is, therefore, necessary to work with thin oxides in order to understand the oxidation kinetics, of polysilicon. Although several measurement techniques are available for the measurement of thin oxides on single crystal silicon, they are not generally useful for the measurement of thin oxides on poly.

The sensitivity of alpha step measurements to variations of the oxide thickness on the wafer makes the accuracy of the measurements questionable. The measurements give ± 20% thickness variations for oxides thinner than 1000 Å. Epplipsometry measurements would not be meaningful because of the multiple reflections coming from the multiple layer structure. The spectrophotometer technique would also fail, since short wavelengths, which are necessary for the measurement of thin films, would be absorbed by the silicon.

An alternative technique, which we are investigating, uses C-V measurements. When the oxide capaticance is known, oxide thickness can be obtained from the relationship

$$t_{ox} = \frac{\varepsilon_o K_{ox} A}{C_{ox}} \qquad (1)$$

where t_{ox} is the oxide thickness, ε_o is the permittivity of free space, K_{ox} is the dielectric constant of the oxide and C_{ox} is the oxide capacitance.

The capacitor structure prepared for these measurements is shown in Figure 1. In the following sections analyses of the different measurements on this structure will be discussed, and a set of experiments which are in progress will be described. Although the structure is distributed in nature, the equivalent circuit elements will be treated as lumped circuit elements.

6.1 Analysis of the Measurements

With the structure shown in Figure 1, three different measurements seem possible: substrate-ring shorted; substrate floating, and a 2-step measurement which will be described later.

1. Substrate-Ring Shorted

The structure, its lump equivalent and measured equivalent circuits are shown in Figures 2a, 2b, 2c respectively. In these figures: C_{ox} is the capacitance of the oxide layer on the silicon, C_s is the depletion or inversion layer capacitance of the substrate, R_{sp} the spreading resistance of the poly. R_s is the substrate resistance of the silicon and C_m and g_m are the measured equivalent capacitance and conductance of the system repectively.

As can be seen from Figure 2, the measured capacitance is in general different from the oxide capacitance C_{ox}, depending on the values of the parasitic elements. If some of those such as R_s, C_s and C_o are known, C_{ox} and R_{sp} can be found from C_m and g_m uniquely for the given structure. The resultant expressions are rather complicated, however, the dependence of C_m/C_{ox} on R_{sp}, t_o and R which is the radius of the dot are given in Figures 3-6. In these figures it is assumed that $R_s = 50\Omega$ and C_s is negligible.

As can be seen from Figure 3 and Figure 2b, there are two limiting cases corresponding to highly and lightly doped poly:

a) $$\lim_{R_{sp} \to 0} C_m = C_{ox} \qquad (2)$$

which means that for highly doped samples, the substrate parasitic elements t_o, R_s, C_s do not have an effect on the measurements.

b) $$\lim_{R_{sp} \to \infty} C_m = \frac{C'_{ox}}{1 + \omega^2 C_{ox}^2 R_s^2} \qquad (3)$$

where $$\frac{1}{C'_{ox}} = \frac{1}{C'_o} + \frac{1}{C_{ox}} \quad ; \quad \frac{1}{C'_o} = \frac{1}{C_o} + \frac{1}{C_s} \qquad (4)$$

which means that depending on the oxide thickness on the substrate, the measured capacitance will differ from the true oxide capacitance.

Neglecting the effect of the depletion capacitance i.e. $C'_o \simeq C_o$, three special thicknesses are distinguishable.

b1. $t_o = t_{ox}$

In this case, under the condition $\omega^2 C'^2_{ox} R_s^2 \ll 1$ $C_m = \frac{C_{ox}}{2}$

For two different thicknesses, this case is shown in Figure 5 and Figure 6.

b2. $t_o \gg t_{ox}$

which means $C_o \ll C_{ox}$. In this case, since C_o will dominate, we will measure C_o, rather than C_{ox}.

b3. $t_o << t_{ox}$

or $C_{ox} << C_o$. Since we will measure the oxide capacitance directly, this is the condition we have to consider when we want to measure thin oxides on lightly doped samples. The effect of t_o on the measured capacitance for lightly doped poly is shown in Figures 7-8.

Now, the question is, in the case of lightly doped poly, how thin can the oxide layer on the substrate be made in order to get the correct oxide thickness on poly? We cannot avoid having an oxide layer on the Si substrate, since this would totally change the polysilicon oxidation kinetics. Furthermore, if we make t_o thinner than 200A, then its thickness becomes comparable with that of the depletion layer and we can no longer neglect the depletion capacitance. Therefore, with this measurement technique, especially for the lightly and moderately doped poly, we cannot avoid the effects of parasitic elements on the measurement.

2. Floating Substrate

Another possible measurement which can be done between the ring and dot by letting the substrate float, seems to avoid the parasitic elements of the structure. The structure, and as a first approximation its equivalent circuit are shown in Figures 9a-9b respectively. Figure 9c illustrates the measured equivalent. As is seen from the figures the calculation of the oxide capacitance C_{ox}, requires a simple unique conversion from the measured capacitance C_m and the conductance g_m.

$$C_{ox} = C_m \left(1 + \frac{1}{K_1^2}\right) \; ; \; R_{sp} = \frac{1}{g_m(1 + K_1^2)} \qquad \text{where} \quad K_1^2 = \frac{\omega^2 C_m^2}{g_m^2} \qquad (5)$$

Although this technique looks simple, in the case of leakage from the poly to the substrate, the problems of the first technique would still exist here. Furthermore, since the whole structure is distributed, a first order lumped circuit approximation might not be adequate.

3. 2-Step Measurement

This technique utilizes a 2-step measurement, one between the gate and the substrate, and the other between the ring and the substrate. The advantage of this measurement is that it provides knowledge of the parasitics of the system. The second measurement will give directly the parasitics of the system, and by using this information in the first measurement, we will be able to extract the oxide capacitance. The measurement structures and their equivalent circuits are shown in Figures 10-11. In these figures: C_x is the total parasitic capacitance of the system, R_x is the total parasitic resistance of the system, R_c is the contact resistance between the Al and the poly, and C_{ox} is the oxide capacitance. C_{m1}, g_{m1} and C_{m2} are the measured equivalent capacitances and conductances of the 2-step measurement. From Figures 10-11, it can be shown that the above parameters can be calculated in terms of the measured capacitances and conductances as follows:

$$R_c = \frac{1}{g_{m2}(1 + K_2^2)} \quad ; \quad R_x = \frac{1}{g_{m1}(1 + K_1^2)} - R_c$$

$$C_x = C_{m2}\left(1 + \frac{1}{K_1^2}\right) \quad ; \quad C = \left[\frac{1}{C_{m2}}\left(\frac{K_2^2}{1 + K_2^2}\right) - \frac{1}{C_x}\right] \qquad (6)$$

$$\text{where:} \quad K_1^2 = \frac{\omega^2 C_{m1}^2}{g_{m1}^2} \quad ; \quad K_2^2 = \frac{\omega^2 C_{m2}^2}{g_{m2}^2} \qquad (7)$$

Experiments

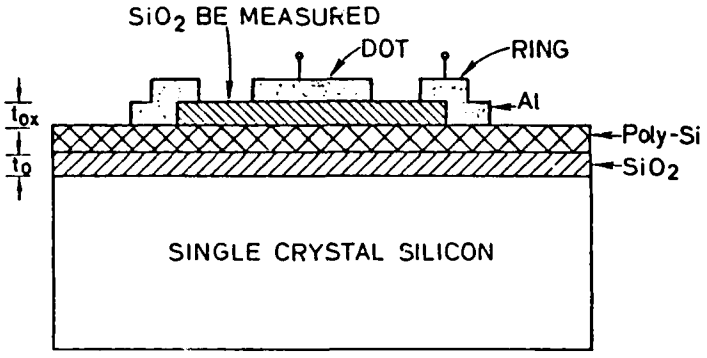
In order to verify the above analysis, the experiments should reflect the effects of the parasitic elements of the structure. So, the experiments should be done on both highly and lightly doped samples which have thin and thick oxide layers on the substrte. The substrate should be highly doped in order to reduce the ffect of R_S and C_S. The measurements should also be done for different thicknesses of oxide grown on the poly. Given the above considerations, the following samples were prepared.

1. Four 2", <111>, B doped wafers with 0.01 Ωcm resistivity were used as substrates.
2. Two of these wafers were oxidized in dry O_2 at 850°C for 15 min giving an average oxide thickness of 250Å. The other two wafers were oxidized in dry O_2 at 1100°C for 70 min giving an average oxide thickness of 1450Å.
3. Poly was deposited on all of the wafers with LPCVD. The average thickness was 0.5μm.
4. The halves of the first and second group of wafers were implanted with P with a dose of $10^{15}cm^{-2}$, whereas the other halves were implanted with a dose of $10^{16}cm^{-2}$.
5. All of the samples were annealed in Ar at 1000°C for 70 min, in order to allow the dopant to redistribute.
6. One-half wafer from each group with 10^{15} doping was oxidized at 850°C for 15 min. Both of these oxidation conditions should give 200Å average oxide thickness on the poly. The rest of the samples were oxidized in dry O_2 at

1100°C for 70 min. This last oxidation should give 1500Å average oxide thickness on the poly. Measurements are underway at the present time to characterize these samples. When all the measurements are completed, we would expect to see the following results.

1. With the floating substrate and the 2-step mesurements we would expect to measure the capacitance of the oxide on all of the samples, regardless of their preparation.
2. With the shorted substrate measurement, for highly doped samples we would expect to measure the correct oxide capacitance. However, for lightly doped samples, depending on the oxide thicknesses both on the substrate and on poly we should observe differences on the measured values.

The development of this technique for measuring thin oxides on polysilicon should allow us to characterize the growth kineties of SiO_2 on this film (and also on silicides and other thin films) and hence should provide better data and models for incorporation in SUPREM III.



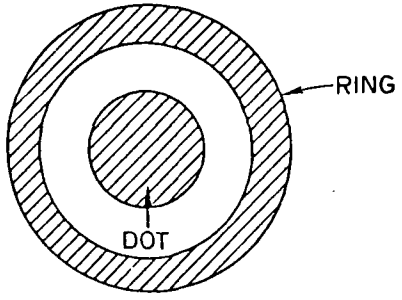


Fig. 1. The ring-dot structure for C-V measurements.

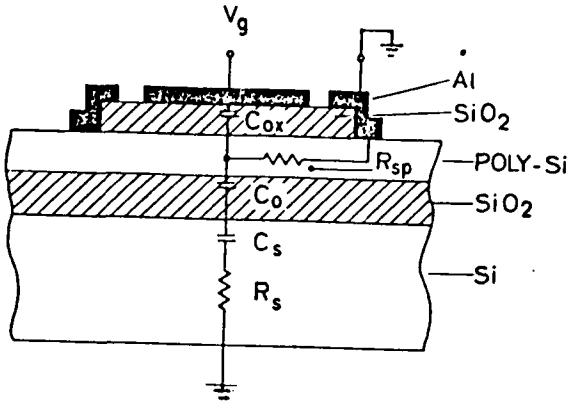
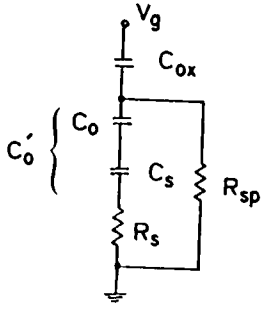
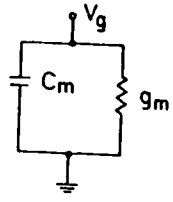


Fig.2.a. The structure for shorted substrate measurement



2.b. Lumped equivalent

≡



2.c. Measured equivalent

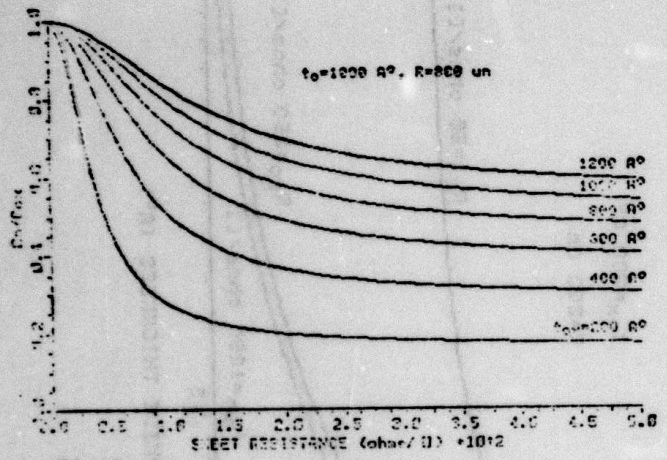


Fig.3

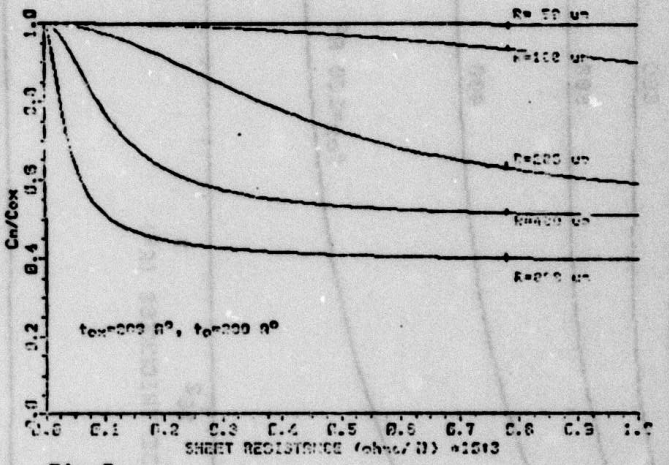


Fig.5

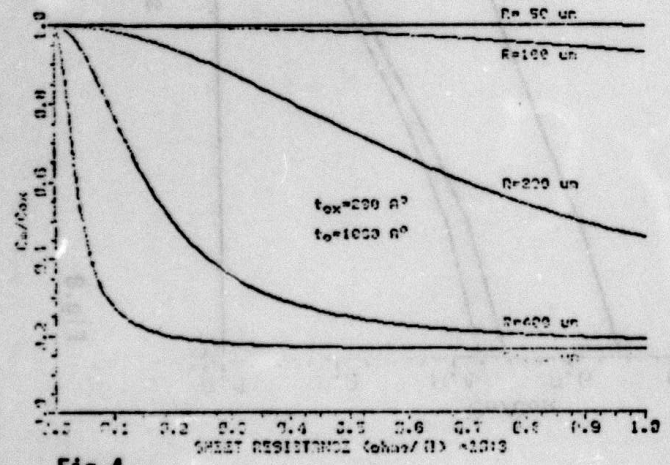


Fig.4

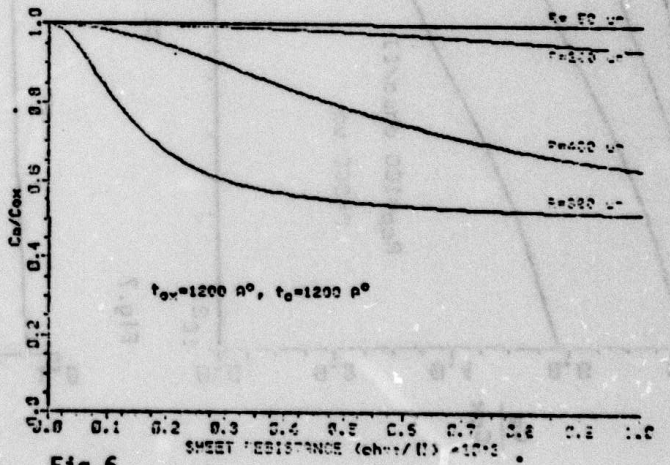


Fig.6

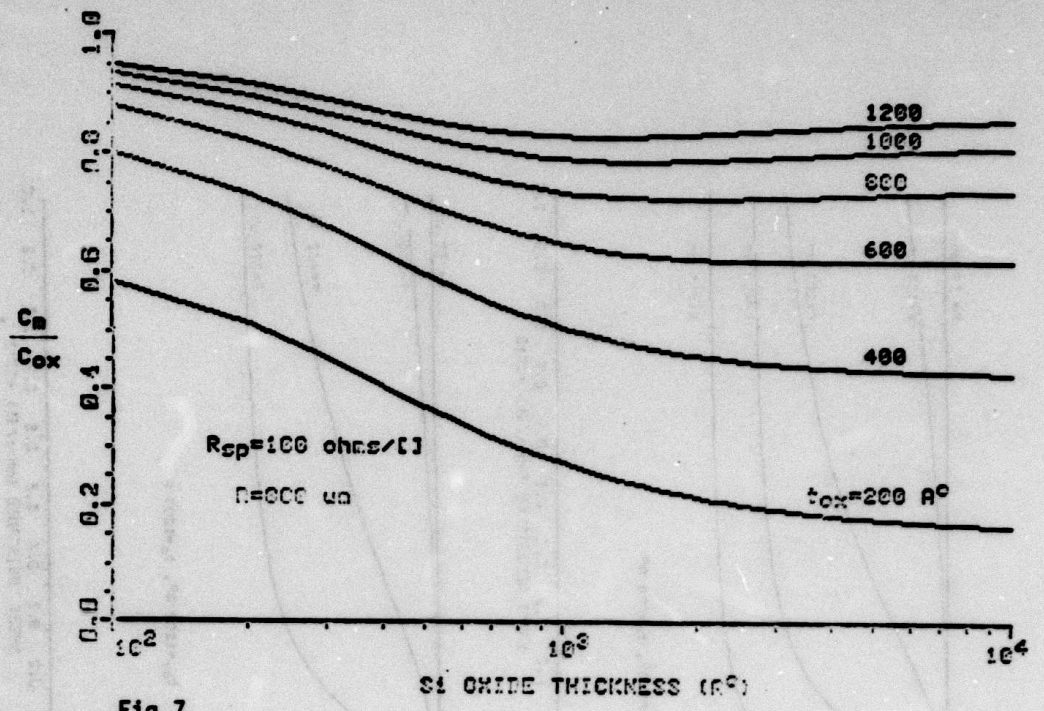

1.0
0.8
0.6
0.4
0.2
0.0
$\frac{C_m}{C_{ox}}$
1200
1000
800
600
400
R_{sp}=100 ohms/[]
R=800 um
t_{ox}=200 A°
10^2
10^3
10^4
SI OXIDE THICKNESS (A°)

Fig.7

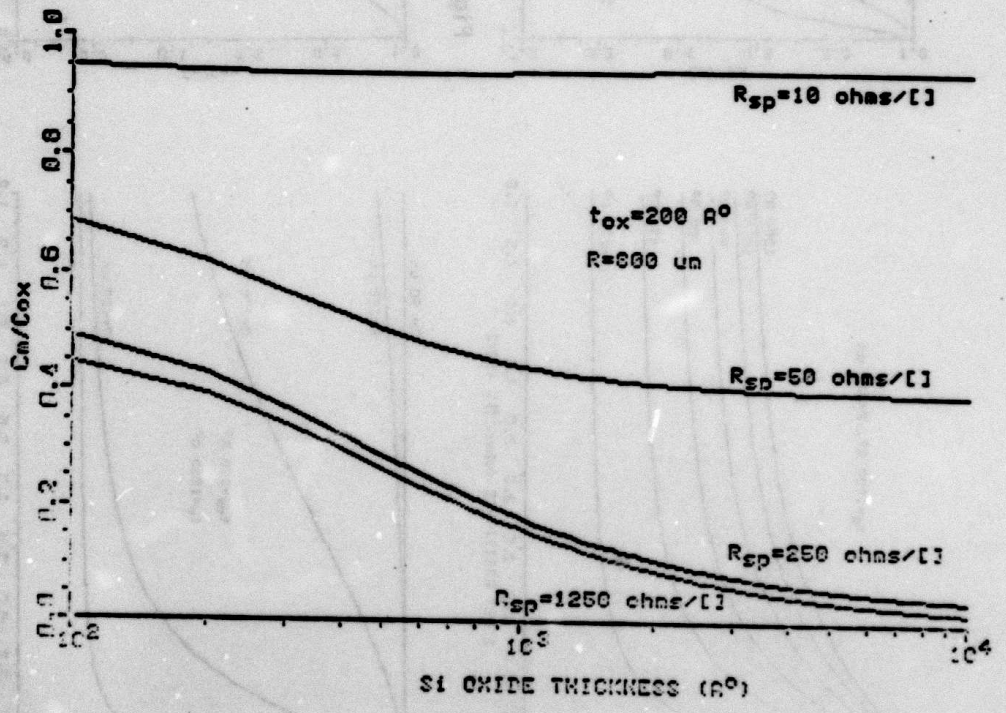

1.0
0.8
0.6
0.4
0.2
Cm/Cox
R_{sp}=10 ohms/[]
t_{ox}=200 A°
R=800 um
R_{sp}=50 ohms/[]
R_{sp}=250 ohms/[]
R_{sp}=1250 ohms/[]
10^2
10^3
10^4
SI OXIDE THICKNESS (A°)

Fig.8

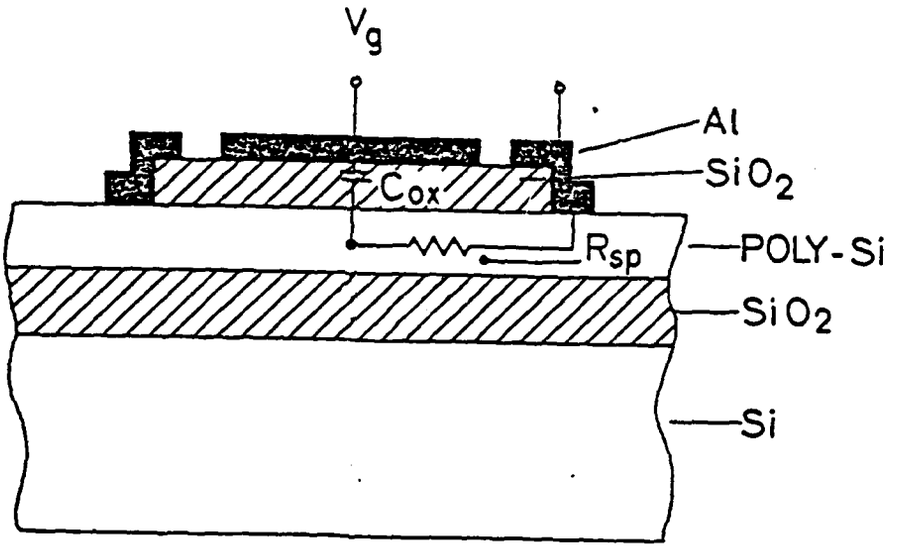
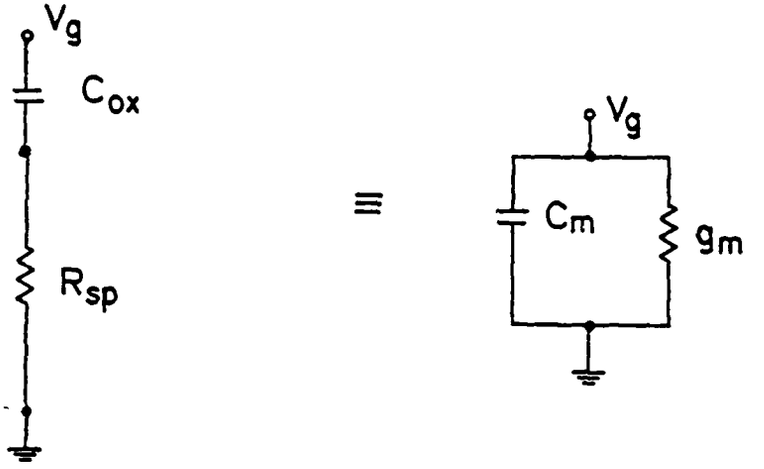


Fig.9.a. The structure for floating substrate measurement



9.b. Lumped Equivalent

9.c. Measured Equivalent

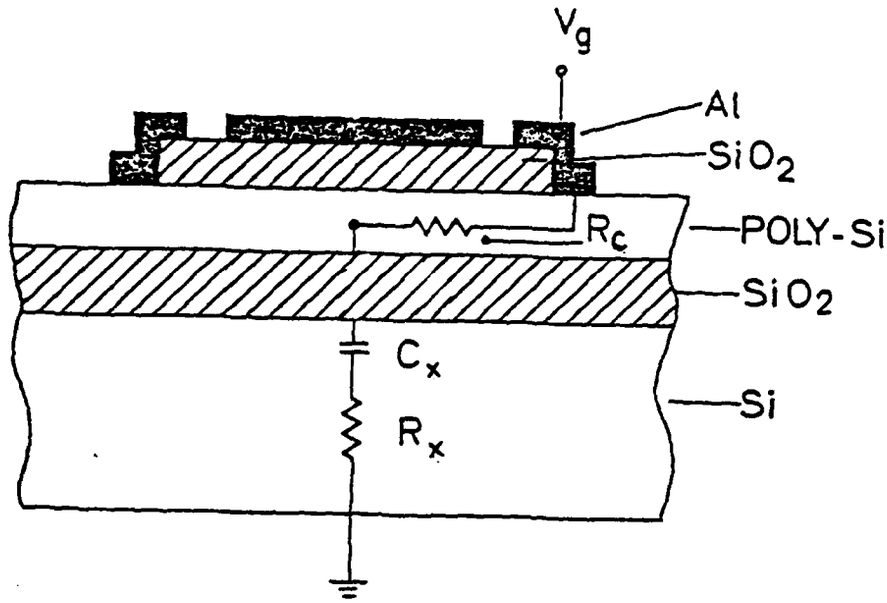
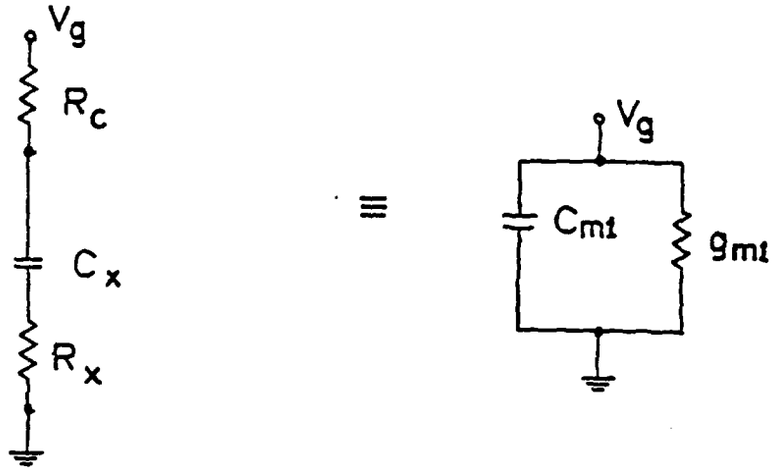


Fig.10.a. The structure for the first step measurement



10.b. Lumped equivalent

10.c. Measured equivalent

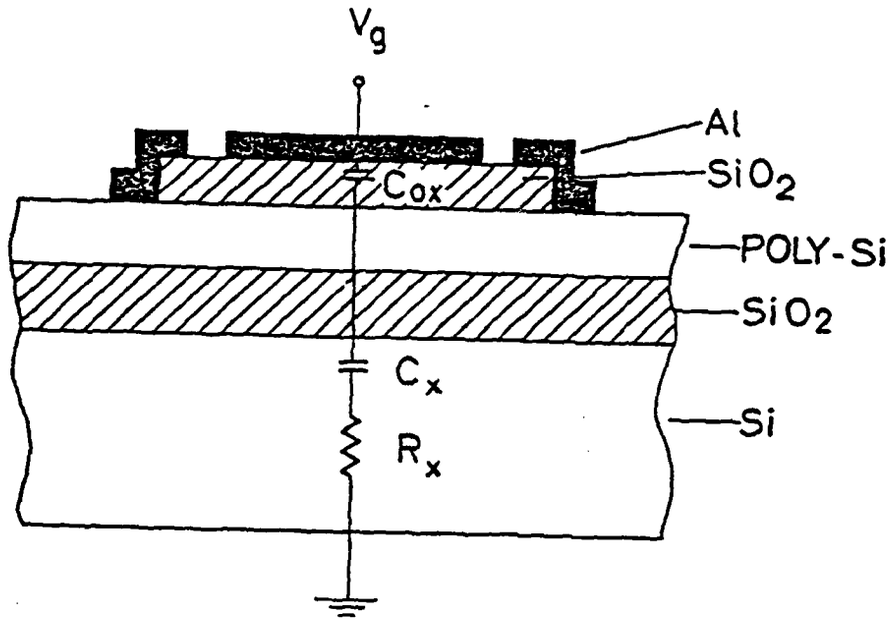
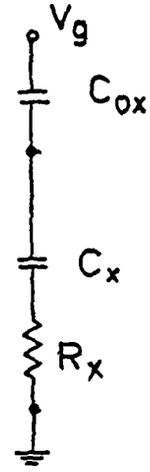
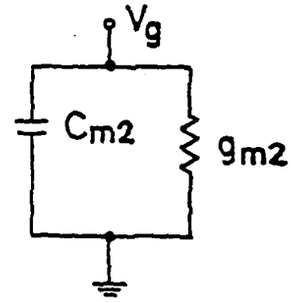


Fig.11.a.The structure for the second step measurement



11.b. Lumped equivalent

≡



11.c. Measured equivalent

7. ION IMPLANTATION AND RANGE STATISTICS

M. GILES, L. CHRISTEL, J. GIBBONS

During this period the main emphasis of our work has been the application of the Boltzmann transport equation to the calculation of ion implantation profiles for light ions and at low energies. As devices shrink to sub-micron dimensions the thickness of overlying films, such as oxides, must be correspondingly reduced. This will in time require implantation energies to be lowered. It is, therefore, necessary to develop methods of calculating implanted ion profiles at these low energies. Some time has also been spent in developing a very simple model of the diffusion of implanted ions based on a joined half-gaussian profile, suitable for hand calculation or as a rapid approximation in the early stages of process development.

7.1 Low Energy Light Ion Implantation

The Boltzmann transport equation approach [1] has been successfully applied to many ion implantation problems, predicting range and damage distributions, recoil distributions [2] and stoichiometric disturbances in compound semiconductors [3]. In this approach, numerical integration of the transport equation proceeds stepwise into the target. At each step the state is described by a matrix in which the value of an element corresponds to the number of ions with a certain energy E; moving at an angle Θ_j to the surface normal. During each step scattering redistributes ions in the energy-angle matrix. Ions which are scattered to angles greater than 90° are called backscattered and were previously considered stopped at the scattering point. However, when the incident ion is much lighter than the target atoms, a large fraction of the incident ions are backscattered. To follow the motion of these ions a multiple pass approach has been developed, where each pass follows the motion of ions backscattered during the previous pass.

In the present calculations, backscattered ions are removed from the matrix and their energy and angular distribution is stored for future use. At the end of the first pass, we then have a concentration profile as before, together with a set of matrices of backscattered ions for each step into the target. The second pass is made from inside the target towards the surface, which is the direction of motion of the previously backscattered ions. At the beginning of each step the stored backscatter distribution for the depth is added to the continuing distribution of ions still moving from the previous step. Ions backscattered during the step are again stored in preparation for a third pass, and so on until all of the ions have stopped.

The calculated profile for Boron implanted into Silicon at 15 keV is shown in Figure 1, where the target/ion mass ratio is 2.55. Here we observe that, even though 60% of the incident Boron ions are backscattered during the first pass, there is little change in the final profile. This is because most of the backscattered ions are moving almost perpendicular to the surface so are likely to be stopped or backscattered again with only a small change. Similar results are obtained with higher beam energies, leading to the conclusion that single pass Boltzmann or LSS [4] techniques will give satisfactory profile descriptions for these cases.

In two layer targets, different effects are observed depending on the relative masses of the target atoms in the two layers. When the layers are of similar mass, such as Silicon Dioxide on Silicon, there is no great change in profile except for some increase in recoil mixing at the interface. When the layers are of different mass, implanted ions tend to recoil from the heavier layer and accumulate in the lighter layer. This is illustrated by Figure 2, which shows the profiles for 15 keV Beryllium implanted into 300Å Silicon

Nitride on Gallium Arsenide. The dose retained in the GaAs is reduced from 88% to 75% of the incident beam, a very substantial reduction, and recoil mixing is increased.

7.2 Approximation of Implanted Profiles by Joined Half-Gaussians

It is well known that non-symmetrical impurity profiles are obtained when common ions such as Boron, Phosphorus and Arsenic are implanted into amorphous or randomly oriented Silicon. It has been shown [5,6] that Pearson distribution functions can provide an accurate fit for impurity distributions for implantation energies up to several hundred keV. Gibbons and Mylroie [7] showed that a distribution consisting of two half-Gaussian distributions joined at a modal projected range R_M could provide a satisfactory fit to impurity profiles obtained under typical implantation conditions.

We have chosen to construct joined half-Gaussian distributions which have the same mode, mean and standard deviation as the Pearson distribution for the implanted profile. The distributions can be constructed from the first three moments of the profile, which are available is tabular form for common ion/target combination [8].

In most processes ion implantation is followed by several high temperature steps during which the implanted distribution diffuses. The diffused distribution can also be approximated by a joined half-Gaussian with new values for R_M, σ_1, σ_2. Expressions have been derived for these parameters as a function of diffusivity and diffusion time. As an example, Figure 3 compares the joined half-Gaussian approximations with a numerical solution for the diffusion of a Pearson distribution, for 50 keV Boron in Silicon. It can be seen that the accuracy of the approximation improves with diffusion as both profiles tend towards a symmetric Gaussian. Considering the quality of

fit and the extreme simplicity with which Gaussian distributions can be constructed, it seems likely that the joined half-Gaussian approximation can provide satisfactory impurity profile estimations for first order analysis of experimental low energy implanted distributions and provide the means for calculating profile changes produced by diffusion.

References

[1] L.A. Christel, J. F. Gibbons and S. Mylroie, J. Appl. Phys. 51, 6176 (1980).

[2] L.A. Christel, J.F. Gibbons and S. Mylroie, Nucl. Inst. and Meth. 182,182 187 (1981).

[3] L.A. Christel, J.F. Gibbons, J. Appl. Phys. 52, 5050 (1981).

[4] J. LinshES, M AxhEDD ns H.E. Schiott, Matt. Fys. Medd. K. Dan. Vidensk. Selsk 33, 14 (1963).

[5] W.K. Hofkerr, D.P. Oosthoek, N.J. Koeman, H.A..M. DeGrefte, Rad. Effects 26, 223 (1975).

[6] A. Gat, J.F. Gibbons, T.J. Magee, J. Peng, V.R. Deline, P. Williams, C.A. Evans, Jr., Appl. Phys. Lett. 32, 5 (1978).

[7] J.F. Gibbons, S. Mylroie, Appl. Phys. Lett. 22, 11, 568 (1973).

[8] J.F. Gibbons, W.S. Johnson, S. Mylroie, "Projected Range Statistics in

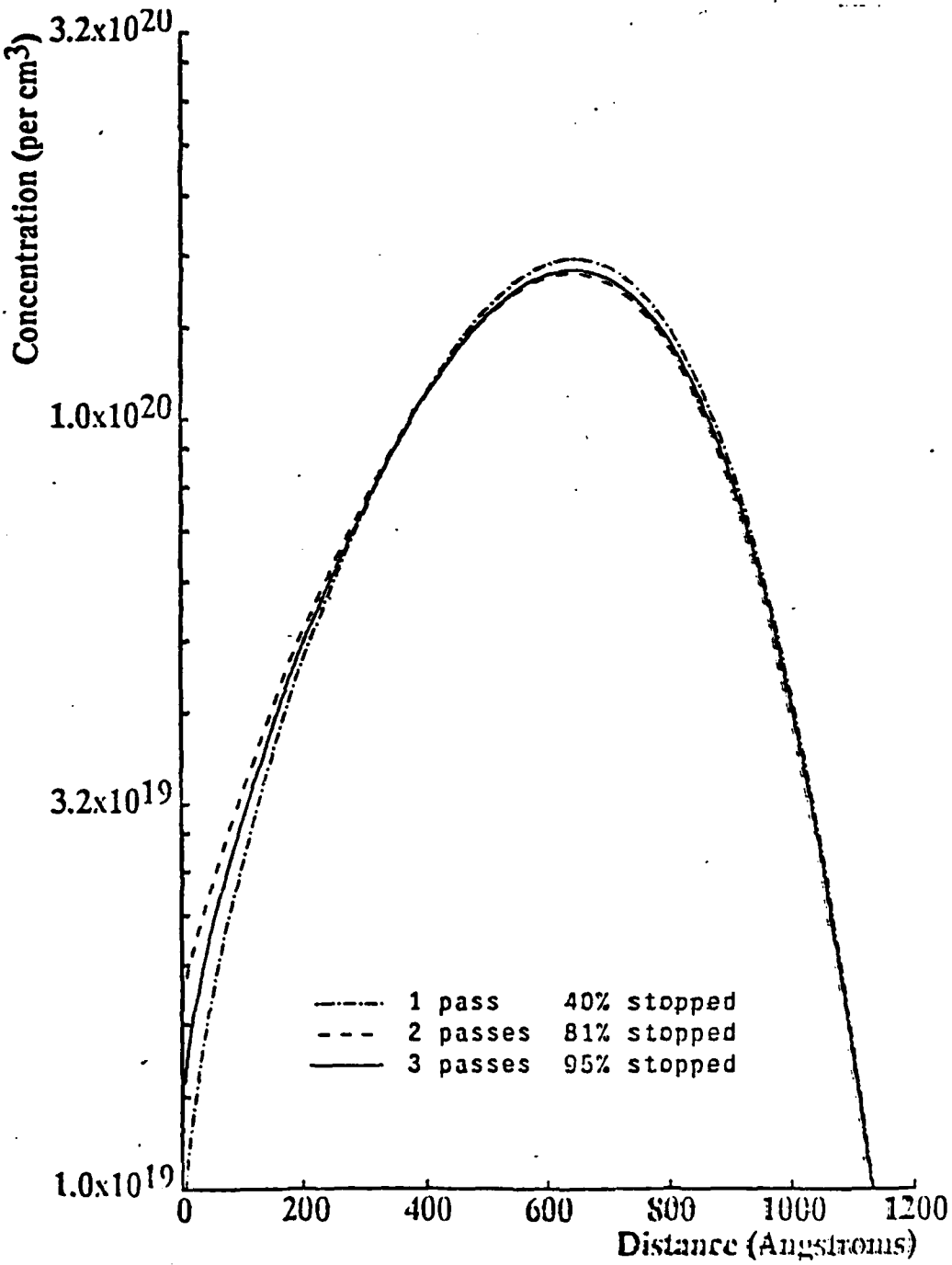


FIGURE 1: Implanted profile for 15 keV Boron into Silicon at a dose $10^{15}cm^{-2}$.

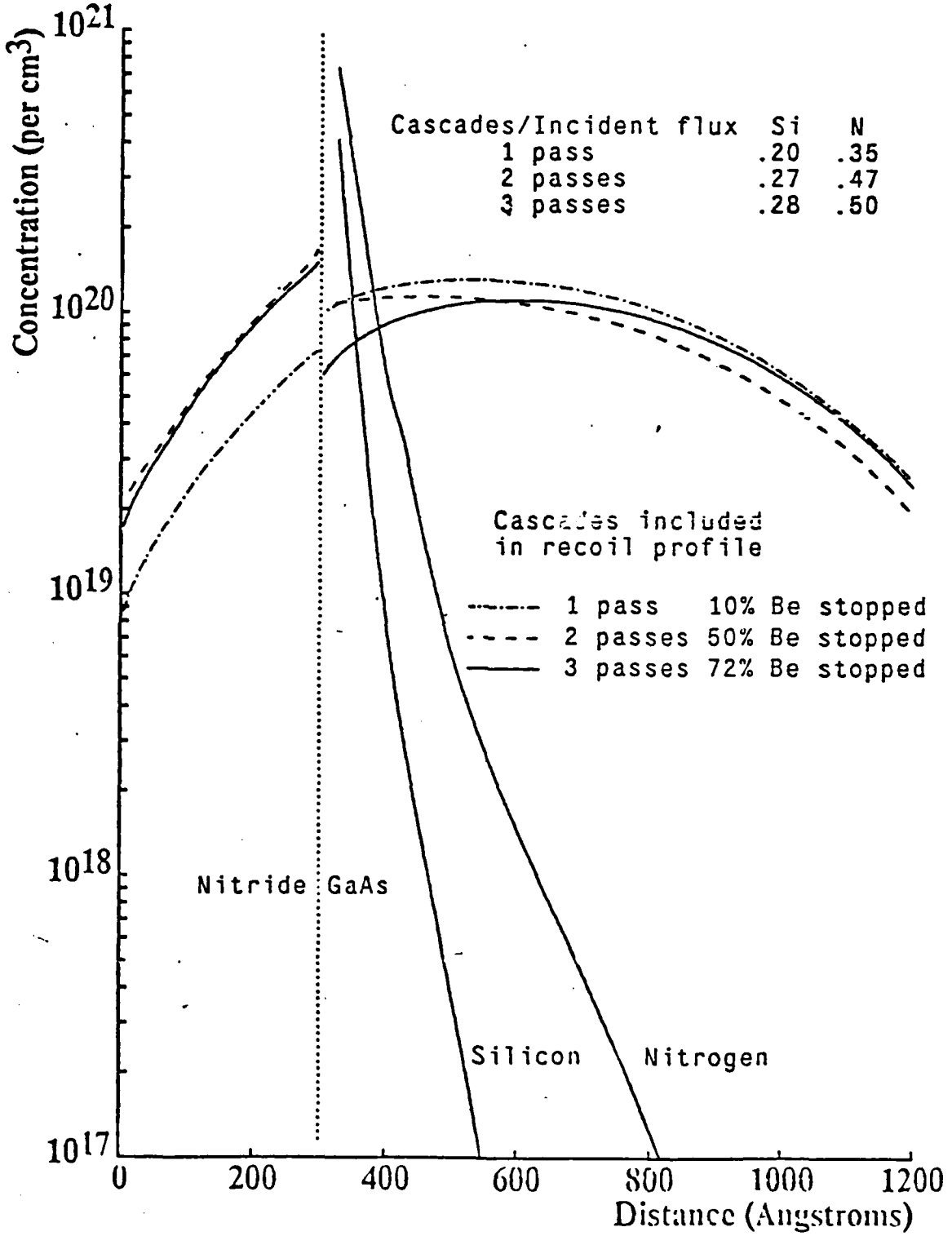


FIGURE 2: Implanted profile for 15 keV Beryllium into 300 Å of Silicon Nitride on Gallium Arsenide at a dose $10^{15}cm^2$, including recoil profiles of Silicon Nitrogen.

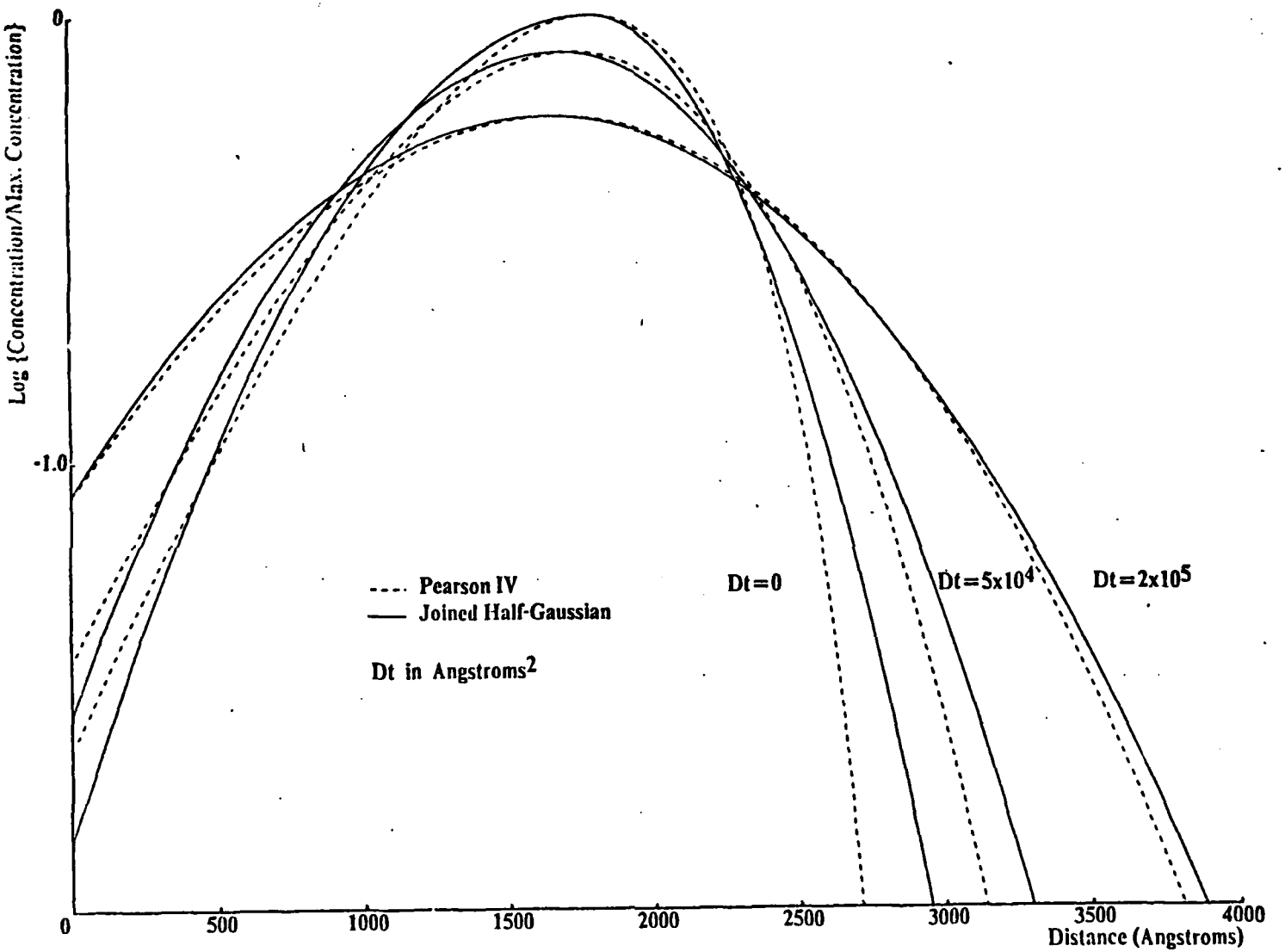


FIGURE 3: Comparison of Pearson IV with joined half-Gaussian distributions for diffusion of Boron implanted at 50 keV into Silicon.

8. SILICIDE/SILICON CONTACTS

F. C. SHONE, K. SARASWAT, J. PLUMMER

During the last few years ohmic contacts formed early in the process sequence to get denser device structure have become important. Such contacts are subjected to several high temperature steps after deposition. This modifies the requirements imposed on the materials being used to form the contacts. It has been observed that silicides of W, Mo, Ta, Ti are compatible with IC fabrication technology. They have fairly high conductivity, they can withstand all the chemicals encountered during fabrication processes, and thermal oxidation of their silicides can be accomplished in oxygen and steam to produce a passivating layer of SiO_2. Their contacts to shallow p-n junctions are reliable, and fine lines can be etched by plasma etching these materials. This indicates that the silicides of W, Mo, Ta, and Ti will be used as interconnection layers and ohmic contact materials in future VLSI devices. It is therefore of interest to model these parameters in SUPREM III.

Mochizuki et.al. annealed $MoSi_2$ contacts to heavily phosphorus doped N^+ diffusions and observed above 700° C the contact resistance increased rapidly. The problem was caused by dopant diffusion from the silicon to the silicide causing depletion of donor impurities at the silicon surface and hence resulting in increased contact resistance. To overcome this problem, they doped the silicide heavily with phosphorus prior to the anneal and found no increase in contact resistance took place even after annealing up to 1100° C. Obviously, in this case the loss of dopant did not take place and, therefore, the contact resistance remained stable.

The dopant concentration behavior in silicide layers depends on the type of dopant, annealing conditions, which films are present and the stoichiometry of

the silicide. The diffusivity of the dopants has been found to be more than three orders of magnitude higher than in single crystal silicon. This rapid diffusion and redistribution can explain observed changes in contact resistance during high temperature cycling. If these silicide are to be used as contact materials, the modeling of dopant diffusion in silicides and segregation and redistribution at the silicide/silicon interface are of extreme importance.

In experiments conducted in our laboratory, we have deposited WSi_2 thin films of about 2000 A thickness on silicon substrates and annealed then in N_2 for 30 minutes at 900° C to reduce the resistivity. After annealing, we heavily implanted the film with As^+ ions and then put CVD oxide on it as a cap. Finally, the wafers were placed in a furnace to diffuse the impurities into the silicon substrate.

We used RBS to measure the impurity redistributions in the silicide layer spreading resistance to measure the impurities profile in the silicon and AES to identify the interface segregation behavior. It was found that the As^+ dopant piled up at the interface and the dopant profile in silicon was similar to that found with doped polysilicon diffusion sources.

The initial experimental results show that the doped silicide acts as a diffusion source to form N^+ junctions and simultaneously forms an ohmic contact quite easily. Further study will emphazise the dopant segregation behavior and the mechanisms of dopant diffusion in the silicide and the silicon substrate to develop quantitative models suitable for SUPREM III implement.

9. GETTERING AND TRANSIENT PROCESS CHARACTERIZATION

G. BRONNER, C. HO, J. PLUMMER

The past work of this project has shown that tungsten silicide (WSi_2) can be used as a metal for contacting devices without degrading device performance. Wsi_2 can withstand high temperatures, one can anneal a finished device at high temperature (anywhere from 800° C to 1200° C), cool the device back to room temperature, and then measure how the anneal has affected the device characteristics. Thus by doing a series of anneals and device mesurements, a transient process can be characterized. This technique has been applied to the problem of backside damage gettering. Bipolar transistors were built. By looking at their low current behavior one can infer the level of metallic contamination in the device. Studying gettering with this technique raised a number of questions that we have been looking at over the past few months.

The first question we asked was whether we were really looking at metallic contamination when we examined the behavior of the base current in bipolar transistors. It is well known that metals can affect bipolar device characteristics; the issue was whether they were the only things that could be affecting the devices. Recently, it has been suggested that vacancies can affect device performance [1]. This seems reasonable on several levels. Vacancies are known to affect many processes in silicon. In SUPREM, diffusion and oxidation in heavily doped regions are explained via vacancy arguments. Additionally, vacancies are present in the right numbers. At 850° C the total number of vacancies in lightly doped silicon is $8.6 \times 10^{"}$ cm^{-3}. In doped regions these values are even higher. If these vacancy levels could be frozen in and if they were electrically active, they could swamp out any effects due to metallic contamination.

To test this idea, the following experiment was done. A wafer was oxidized at 1000° C to passivate the surface. It was then annealed at temperatures between 600° C and 1000° C. After each anneal the wafer was cooled as quickly as possible to room temperature. It then received a 1/2 hour anneal at 450° C in forming gas. Bulk lifetime was then measured by looking at the change in conductivity as a light was strobed on and off.

If frozen-in vacancies limit device performance, then lifetime should drop off with higher anneal temperature. A plot of lifetime vs. inverse temperature (t vs. 1/T) should give the activation energy of vacancy formation. The data is plotted in this form in Figure 1. We see that from 700° C to 1000° C the life-time is essentially constant. Only at the lowest anneal temperature, 600° C, is the lifetime somewhat higher. From this we conclude that frozen-in vacancies do not seem to directly affect device behavior. Thus, when we look at the low current operation of bipolar transistors we are likely seeing a phenomena caused by metallic contamination.

The reason for the rise in lifetime with the 600° C anneal is not clear, but it is possible to hypothesize an explanation. When metals are in solution in siicon, they can either be on or off lattice sites, i.e., they can be substitutional or interstitial. In general, interstitial diffusion is much faster than substitutional diffusion for these metals. Once equilibrium is reached, solubilities tend to be much higher for the substitutional forms of the metal. Only the substitutional metals are electrically active in silicon. Thus, when metals are first introduced into silicon, they are interstitial. These interstitial atoms diffuse quickly until equilibrium is established. They then would like to drop onto substitutional lattice sites. For that to happen the following reaction must take place:

$$M_{interstitial} + V \underset{k}{\rightleftarrows} M_{substitutional}, \qquad (1)$$

where M stands for a metal atom and V stands for a silicon vacancy. This reaction is a simplified one, but it does describe qualitatively what takes place. It has recently been suggested that instead of a substitutional metal atom one might have a vacancy-metal interstitital complex [2,3]. This effect, in addition to the various charge states of the atoms, is ignored.

For this reaction we can write the affinity product,

$$J = \frac{C_M sub}{C_M int\ C_V} \qquad (2)$$

where $C_M sub$ is the concentration of substitutional metal atoms, $C_M int$ is the concentration of interstitial metal atoms, and C_V is the concentration of vacancies. When J is less than the equilibrium constant k, the reaction is driven to the right, i.e., all the metal atoms assume substitutional sites. This is the situation at high temperatures when C_V is relatively high. As the temperature of the anneal decreases, C_V decreases and J increases. When J becomes greater than k, the reaction tends to reverse. Substitutional gold jumps off of the lattice to form a vacancy and an interstitial metal atom. Evidently, at 600° C the concentration of vacancies drops enough to cause this to happen. Thus, a fraction of the metal atoms become interstitial (and also electrically inactive) which we see as an increase in silicon lifetime.

With this background we feel that our experiments, with anneals in the range of 800° C to 1000° C, do indeed look at the metal concentrations in our devices. Therefore, we have fabricated a number of wafers with various test structures. These include different sized bipolar transistors, MOS capacitors, and various contact resistance structures. The bipolar transistors allow us to indirectly follow the levels of metallic contamination by looking at their low current operation. Different sized transistors let us separate the bulk effects, which we are interested in, from any surface effects. The MOS

capacitors, through pulsed lifetime tests, provide an independent measure of metallic contamination. The contact resistance structures look at the WsI_2/Si interface. From these, we will be able to see the amount of dopant segregation, and determine whether any changes in device characteristics are due to these effects. All of these devices have been built in float zone material to eliminate competition between the backside getters being studied and internal gettering due to oxygen precipitation.

Before following the time behavior of the backside getter, there are a few facts we were interested in establishing. The first of these had to do with how WSi_2 contacts affect device performance. All of our previous work has shown that silicide contacts do not degrade performance. There is the possibility that they could improve performance. A recent paper by Thompson and Tu [4] has shown that aluminum contacts on silicon can getter copper, silver, and gold. If WSi_2 acts in a similar fashion, we might have trouble following the behavior of a backside getter.

To see how much of a problem this might be, we have designed some control experiments to test the limits of our experimental procedure. The first of these looks at the behavior of a backside getter with and without WSi_2 contacts. A set of wafers consisting of the test structures outlined earlier is fabricated up to the metal deposition step. One wafer is taken, receives a backside getter, and then an 8 hour gettering anneal. Contacts are made to devices using Aluminum and the devices are characterized.

Another wafer receives a backside getter, but before receiving a getter anneal, its devices are contacted using WSi_2. It then is annealed for 8 hours, cooled to room temperature and its device characteristics are measured. This experiment will show how the WSi_2 affects the gettering process.

The other test we are conducting checks the premise that a number of short anneals have the same effect as one long aggregate. Towards that end an additional wafer is taken, it is given a backside getter, and it is then contacted with WSi_2. It is then annealed 8 separate times for 1 hour at a time. At the end of this series of anneals, the wafer's device characteristics are compared to the other two devices described above. This experiment essentially determines whether or not the gettering process can be treated as a linear system. If it can, then the device characteristics after 8 one hour anneals will be indistinguishable from one 8 hour anneal.

In summary, we have shown that our measurements of device characteristics do correlate with levels of metallic contamination. The device characteristics seem to be unaffected by vacancies in silicon, and because of that fact the device characteristics are relatively unaffected by such parameters as pull rate and cooling rate from high temperatue anneals. With that assurance, we went ahead and have fabricated a large number of wafers with various test structures.

Using these wafers a number of experiments have been started checking some of the underlying assumptions in our experimental procedure.

References

[1] J.G. Fossum and D.S. Lee, "A Physical Model for the Dependence of Carrier Lifetime on Doping Density in Nondegenerate Silicon", Solid State Elect. Vol. 25, No. 8, pp. 741-747, 1982.

[2] D.V. Lang, H.G. Grimmeiss, E. Meijer, and M. Jarss, "Complex Nature of Gold-Related Deep Levels in Silicon", Phys. Rev. B, Vol. 22, No. 7, pp. 3917-3934, 1980.

[3] J.A. Van Vechten and C.D. Thurmond, "Entrophy of Ionization and Temperature Variation of Ionization Levels of Defects in Semiconductors", Phys. Rev. B, Vol. 14, No. 8, pp. 3539-3550, 1976.

[4] R.D. Thompson and K.N. Tu", Low Temperature Gettering of Cu, Ag, Au across a wafer of Si by Al", Appl. Phys. Lett., 41(5), pp. 440-442, 1982.

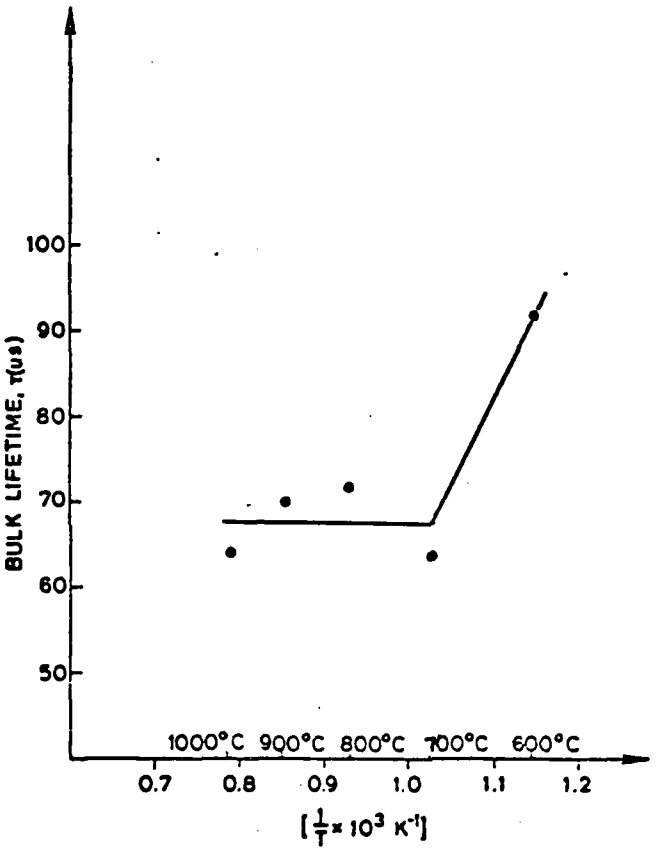


FIGURE 1: Bulk Lifetime, τ, measured after quenching sample from temperature T.

10. Si WAFER SURFACE PROPERTIES: SURFACE COMPOSITION AND THE EFFECT OF CLEANING PROCEDURE STUDIED BY ELLIPSOMETRY AND AUGER ELECTRON SPECTROSCOPY

M. TAUBENBLATT and C. HELMS

In this program, we have begun an investigation of the chemistry of wafer surfaces and the effect of various cleaning steps on the chemistry. One goal of this study is to compare ellipsometry measurements to electron spectroscopy to provide more quantitative measurements for thin oxides.

Although ellipsometry does not provide an actual identification of the species present on the surface, it does give information concerning the thickness and index of refraction of surface layers present (if the optical properties of the substrate are known). One difficulty with the technique is that the "effective substrate index" is a strong function of surface damage and adsorbed layers such as H_2O, OH, etc., so that care must be taken to assure the value of substrate index used is appropriate. The procedure normally followed in most laboratories is to fix the Si index at 3.85 - 0.02 i and using measured values of σ and ψ vary the layer thickness and index until the best fit to the ellipsometry equations is obtained. If the substrate index is correct, this leads to relatively good values for the layer thickness for thin layers but rather uncertain values for the layer index due to the insensitivity of σ and ψ to variations in the index. It is also important to note that ψ is relatively insensitive to thickness for thin layers, whereas σ is nearly linear; σ is therefore much more reliable for thickness determination. Also, σ and ψ change very little with the layer index for thin oxides so that determinations of the layer index from measurements of σ and ψ is very inaccurate. The importance of the substrate index can be seen if we look at a change in the imaginary part of the substrate index from -0.02 to -0.2; this gives a change in σ of $\approx 7°$.

A 7° error in σ, however, gives a 25 Å error in thickness (a large error, indeed, for thin oxides). Our approach is, therefore, to rely on values of a starting from a measurement of the substrate after removal from HF and then compare to the value obtained from the wafer with the native oxide present. Average values for σ averaged over a number of samples for the substrate after an HF dip are ≈ 176.4° and after an HF dip plus 3 hours are 175.9 (≈ 2 Å). As received were measured within 30 minutes of removal from the shipping container and give values of σ 173.8 (9 Å). The substrat value for σ of 176.4° corresponds to an imaginary part of the substrate index of -0.08 or, conversely, 7 Å of native oxide which, from our electron spectroscopy studies, can certainly be shown not to be present.

Unlike ellipsometry, Auger electron spectroscopy provides detailed information on the constituents present within 5-50 Å of the surface. In addition, information concerning the bonding of the surface atoms is also accessible. Measurements on wafers as received are, except for the oxides present, quite clean with the average carbon level observed being 0.10 monolayers in the surface region. The oxygen concentration is approximately 2 monolayers (5 Å).

In comparing the ellipsometry results to the Auger electron spectroscopy results, we see first that the layer thickness obtained from ellipsometry is larger (≈ a factor of two) than that obtained by AES. This discrepancy could be caused by a number of factors. First, due to the uncertainty in the effective substrate index, a large absolute error in the ellipsometry measurements might be expected. If the surface oxide is homogenous, the 10 Å + values of surface oxide thickness are definitely inconsistent with the AES results. It is possible, however, that the surface oxide is nonuniform so that there are substantial regions of thinner oxide present on the surface. This could account

for some of the discrepancy as ellipsometry and AES are effected much differently by inhomogenities.

In order to identify important effects in the cleaning procedures used commonly, we subjected the wafers to various cleaning steps and then followed the surface concentration with AES. A summary of the results are shown in Table I. Starting from the bottom, we note that the effect of a final HF dip yields what we believe to be the undesirable result that the surface ends up with a very high surface carbon concentration. If, however, the HF dip is followed (line 5) by an H_2O_2 treatment (note that all these treatments were for parameters of the so-called "RCA clean") without exposure to air quite low carbon concentrations were obtained. We feel that the HF dip removes a protective oxide layer, and when the wafer is then exposed to air carbon from CO, CO_2, hydrocarbons, etc., present can more easily deposit on the surface. The cleanest surface was obtained using the procedure shown through line 5; however, it may be more desirable to leave the surface with a thicker oxide but with a minimum carbon concentration (through line 4 which is the RCA clean minus the final HF dip).

TABLE I. EFFECT OF VARIOUS CLEANING PROCEDURES

	Procedure	Oxygen Concentration	Carbon Concentration
(1)	As received	2.8 ml	0.2 ml
(2)	$H_2SO_4:H_2O_2$ → DI water		
(3)	$NH_4OH:H_2O_2:H_2O$ (air)	2.3 ml	0.5 ml
	DI water		
(4)	$HCl:H_2O_2:H_2O$		
	DI water (air)	2.1 ml	0.1 ml
(5)	HFD_{1p} → DI water → H_2O_2 → DI water (air)	1.1 ml	0.2 ml
	Air		
	DI water (air)	0.4 ml	1.0 ml

11. STUDIES OF OXYGEN DIFFUSION THROUGH SiO_2

C. HELMS

In a recent paper Irene [1] has reported on measurements of the oxidant diffusion coefficient using a time lag method with in situ ellipsometry. For the temperature range investigated (600° C - 1000° C), a measurable lag time for an initial 1 μm thick oxide was observed only for the 1000° C sample. A value of $D = 2 \times 10^{-13}$ cm^2/sec was obtained which leads to a value of approximately 10^{21} cm^{-3} for the oxygen solubility. The value for D is somewhat higher than that obtained using exchange methods to measure diffusion coefficients [2-5] and considerably lower than that obtained by Norton [6] in his permeation experiment and definitely larger than the 10^{20} cm^{-3} maximum we have previously reported [7].

As pointed out by Revesz and Schaeffer [8], however, the comparison to the exchange experiments is meaningless in any case since the rate limiting step in that process is the exchange reaction not the diffusion process. We are then left with the large discrepancy of over 10^4 between Norton and Irene. The 10^{21} cm^{-3} solubility is also much larger than would be expected for inert gas molecules of roughtly the same size [8].

Recent results by Hamasaki [9] seem to shed some light on these discrepancies. Although much of Hamasaki's interpretation may be criticized, his experimental findings are difficult to refute. Namely, he finds that, when sequential oxidations are investigated, esepcially when a temperature change is involved, the initial growth rates for the sequential oxidation step depends strongly on the time-temperature history of the sample such that, for example, "when the temperature of the first oxidation is higher than that of the second oxidation, a faster growth rate in the initial state of the second oxidation

is found. An initial slower growth rate is also found when the temperature of the first oxidation is lower than that of the second oxidation" [9].

The findings of Irene and Hamasaki certainly indicate that the oxidation of silicon is a much more complicated process than we would like to think. It appears that thermal SiO_2 is not a static quantity, its properties depending on its temperature history and the pressure history of soluble molecules such as O_2, H_2O, CO, CO_2, etc., that may be present in the ambient. If this is the case, the diffusion coefficient would also be expected to be a function of time, pressure, and temperature, irrespective of any temperature dependence due to a single diffusion activation energy.

In Irene's case, the initial oxides were grown to an initial thickness of 1 μm at 1000° C. An "inert" anneal was then performed for about 20 hours. The temperature is then changed, equilibrated, and the ambient was switched to oxygen. The assumption was made that the transport properties are unaffected by either the anneal or the temperature change. Hamasaki's results certainly call the second assumption into question.

Even the "inert" anneal may not be so inert, since the structure of SiO_2 (Si-O-Si bond angle distribution, microvoid density, etc.) may well be affected even if the optical constants change little. In addition, there is a finite solubility of both Ar and N_2 in SiO_2 which could be responsible for blocking available sites for O_2 diffusion.

It would appear for most normal conditions where nonsequential oxidations are involved that, not only is the oxidant transport process in steady state, but the SiO_2 itself reaches a steady state condition. This would explain the agreement between Norton's values for diffusion coefficient [5], the expected solubility of O_2 [8], and the parabolic rate constant for oxidation [10].

References

[1] E.A. Irene, J. Electrochem. Soc. 129, 413, 1982.

[2] E.W. Sucov, J. Am. Cevam. Soc. 46, 14, 1963.

[3] R. Haul and G. Dumbgen, Z. Elektrochem. 66, 636, 1962.

[4] E.L. Williams, J. Am. Cevam. Soc. 48, 190, 1965.

[5] K. Muehlenbachs and H.A. Schaeffer, Am. Mineral. 15, 179, 1977.

[6] F.J. Norton, Nature 171, 701, 1961.

[7] J.W. Rouse, C.R. Helms, C.J. Han, Final Report for Period Ending 31 March 1982, p. 261.

[8] A.G. Revesz and H.A. Schaeffer, J. Electrochem. Soc. 129, 357, 1982.

[9] M. Hamasaki, Solid State Elec. 25, 479, 1982.

[10] B.E. Deal and A.S. Grove, J. Appl. Phys. 36, 3770, 1965.

12. PHOSPHORUS DIFFUSION IN SILICON

P. FAHEY, R. DUTTON

Of the four common dopants used in Si device processing, P, As, B and Sb, phosphorus exhibits by far the most complex diffusion behavior under typical process conditions. Consequently, it has proven the most difficult to model. Since the inception of SUPREM, phosphorus diffusion has been modeled using the theory of Fair and Tsai [1]. Unfortunately, model predictions do not correlate well with experimental results under all conditions, and the discrepancies prove worse under those conditions most important to modern process technology, i.e., low temperatures and shallow diffusions. In addition, since the time it was first introduced, a number of objections have been raised against the physical basis of the theory which indicate that the present model cannot be extended, even empirically, to handle important cases such as phosphorus diffusion in two-dimensions, phosphorus diffusion from polysilicon, and interaction of phosphorus with other impurities present during processing. Despite these shortcomings the Fair-Tsai model remains the only quantitative model of phosphorus diffusion yet developed.

In this last time period we have thoroughly reviewed the results of all pertinent experimental work concerning phosphorus diffusion and have scrutinized all previously proposed theories in order to develop a better model. The results of this effort have been encouraging and have produced a consistent picture of phosphorus diffusion in Silicon. At this juncture we are able to enumerate in detail the inadequacies of the present model and to outline an alternative model which is both theoretically sound and more consistent with experiment. The essence of our model is that: 1) phosphorus diffusion occurs

through a two-stream mechanism whereby phosphorus atoms can migrate as either a phosphorus-vacancy (PV) pair or as a phosphorus-interstitialcy (PI) pair; 2) the large fraction of electrically inactive phosphorus (≈ 2/3 total concentration) present under typical predeposition conditions is due to precipitation, and 3) phosphorus diffusion generates excess Si interstitials which can affect the diffusion of other impurities. This model differs markedly from the Fair-Tsai theory. We would like to first justify the above statements and contrast them with the equivalent stipulations of the Fair-Tsai model in order to elucidate the differences in predictive capabilities between our model and that of Fair and Tsai. We will then discuss the experimental work which is both in progress and under consideration to prove the correctness of our model.

We are led to point 1) above by considering that the kinked, two-zoned, profile of phosphorus diffusion is characteristic of a process where the species under consideration can exist in two states and diffuse by two different mechanisms. The kinked profile is a result of superposition of the two diffusive fluxes. For example, tellerium in germanium (which exists in the crystal in both substitutional and interstitial states) exhibits a diffusion profile very similar to that of phosphorus. The Fair-Tsai model proposes that phosphorus diffuses primarily as $P^+ V^=$ pairs. As the local Fermi level (which depends on the local P concentration) drops, the $P^+ V^=$ pairs dissociate, thereby generating excess vacancies which are responsible for formation of the kink. While this mechanism is not impossible, it is open to many questions and will be discussed shortly. Our conclusion 2) is based on the direct observation by Armigliato et.al. of precipitates [2] in concentrations high enough to account for the electrically inactive fractions. Fair and Tsai have proposed that this inactive fraction is due entirely to (electrically inactive) $P^+ V^=$ pairs. This hypothesis is shown here to be incorrect on fundamental grounds. Conditions of local charge neutrality dictate that:

$$n + [P^+V^=] + [V^-] + 2[V^=] = p + [P^+] + [P^+V^0] \quad (1)$$

while conservation of matter yields

$$[P]_{total} = [P^+] + [P^+V^0] + [P^+V^-] + [P^+V^=] \quad (2)$$

(here brackets denote concentrations and n and p are the electron and hole concentrations respectively). Combining these two equations we show that for the inactive concentration

$$[P]_{total} - n = 2[P^+V^=] + [P^+V^-] + 2[V^=] + [V^-] > 2[P^+V^=] \quad (3)$$

Thus, $P^+V^=$ pairs can account for at most one half of the inactive phosphorus. To estimate the absolute concentration of $P^+V^=$ pairs we write the formation reaction as

$$P^+ + V^= \rightleftharpoons P^+ V^= \quad (4)$$

Applying the law of mass action in a probabilistic sense the above reaction implies that in equilibrium

$$\Theta \frac{[P^+]}{[Si]} \frac{[V^=]}{[Si]} \exp(E_b/kT) = \frac{[P^+V^=]}{[Si]} \quad (5)$$

where Θ is a geometrical factor of order unity, [Si] is the concentration of silicon lattice sites ($= 5.5 \times 10^{22}$ cm^3), and E_b is the binding energy of the $P^+V^=$ pair. Using the commonly accepted vacancy energy level of $E^= = E_c$ - 0.11eV for the double negatively charged vacancy, and the highest experimentally observed value of n ($\approx 4 \times 10^{20}$ cm^{-3}), we obtain for 1000° C

$$\frac{[P^+V^=]}{[P^+]} = 3 \times 10^{10} \exp(E_b/kT) \quad (6)$$

For E_b as high as 1.0eV we obtain $[P^+V^=]/[P^+] \approx 5 \times 10^{-5}$ cm^{-3}. Under all realizable conditions then $[P^+V^=] << [P^+]$. In terms of absolute concentration $[P^+V^=]$ is probably in the range of 10^{13} to 10^{16} cm^{-3}

Our claim 3) that phosphorus diffusion generates excess interstitials is supported by the facts that, the diffusivityof a boron base is considerably enhanced (emitter dip effect), and surface stacking faults (which are extra planes of atoms), grow during the diffusion of phosphorus. It is generally acknowledged that these same effects occur during oxidation of the silicon surface due to the generation of excess interstititals. Our proposition is in direct opposition to the Fair-Tsai theory which proposes the generation of vacancies during diffusion (in this case one would expect enhanced shrinkage rather than growth of stacking faults). We also note that since the phosphorus precipitates observed by TEM experiments are of an interstitial nature, it is natural to expect the precipitation process itself to generate excess Si interstitials. This is in accord with experimental results of diffusion of phosphorus from polysilicon in which precipitation occurring primarily in the polysilicon is coincident with a reduction of the emitter dip effect. This type of effect is impossible to model with the Fair-Tsai theory.

To verify our model experimentally we have attempted to observe the behavior of antimony buried layers during the in-diffusion of phosphorus at the surface. This experiment is based on the following considerations. Due to its size, i.e., greater than Si, antimony is expected to have a relatively small interstitialcy component of diffusion and to effect movement primarily through a vacancy mechanism. Consistent with this idea is the experimental observation that when the silicon surface is oxidized antimony diffusion is not enhanced and in some cases it is actually retarded (it is postulated) due to annihilation of vacancies by the excess interstitials generated. It is clear then that antimony

should be enhanced during phosphorus diffusion if vacancies are generated, and should display no enhancement or possibly retardation if interstitials are generated. Preliminary results indicate that antimony diffusion is indeed retarded.

A number of additional experiments are presently being developed in an effort to further test the correctness, and quantify, our new model. It is hoped that antimony can be used under a variety of conditions as a marker layer to differentiate between vacancy and interstitialcy mechanisms of diffusion. Experiments to detect the phosphorus interstitialcy directly (e.g., by channeling) are in a preliminary state, and have thus far been restricted to feasibility studies.

References

[1] R.B. Fair, J.C. Isai, J. Electrochem. Soc. 124, 1107, 1977.

[2] A. Armigliato, D. Nobili, M. Serviodori, S. Solmi, J. Appl. Phys. 47, 5489, 1976.