AD-A130 410 THE AXIS TEST BOX HARDWARE REPORT(U) ROYAL SIGNALS AND RADAR ESTABLISHMENT MALVERN (ENGLAND) A L SIMCOCK APR 83 RSRE-MEMO-3584 DRIC-BR-88202 1/1

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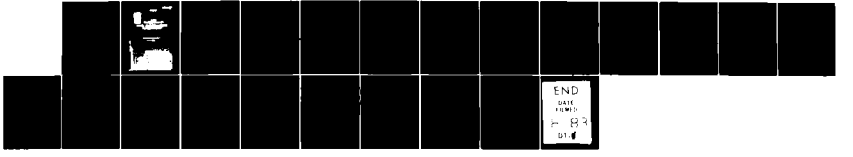

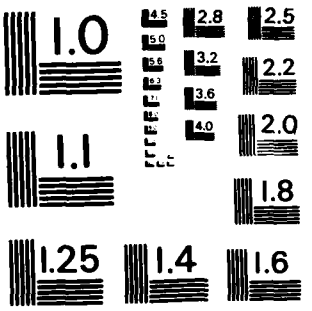

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ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 3584

Title: THE AXIS TEST BOX HARDWARE REPORT

Author: A L Simcock

Date: April 1983

SUMMARY

This Memorandum describes in detail the hardware which has been designed specifically to perform the functions required of the Axis Test Box. The interfaces to other, general purpose, circuits are also defined.

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LIST OF ABBREVIATIONS

AXIS	Automatic Exchange for the Investigation of Structured Software	
VDU	Visual Display Unit	
MMI	Man Machine Interface	
PPI	Programmable Peripheral Interface	
SUT	System Under Test	
CDU	Code Detector Unit	
TSU	Trunk Signalling Unit	
CPU	Central Processor Unit	
IDR	Input Data Register	
POPDAT	Peripheral Output Data	(See fig 2)
POPADD	" " Address	"
POPCOM	" " Command	"
POPSTA	" " Status	"
PIPDAT	" Input Data	"
PIPADD	" " Address	"
PIPCOM	" " Command	"
PIPSTA	" " Status	"

LIST OF REFERENCES

1)	AXIS Phase 1 (Volume 2) Unpublished MOD (PE) Report	Edited By P C Bottomley
2)	An Introduction to the AXIS Test Box	A L Simcock
3)	The AXIS Test Box Operating Guide	A L Simcock
4)	The AXIS Test Box Software Report	A L Simcock
5)	DISCUS hardware description and appendicies RSRE Memo 3483	H S Field-Richards
6)	Plessey Manual 652/SJ/01243 Section 2. Signalling Format	
7)	AXIS Test Box Input Buffer Card Circuit Diagram RSRO/010082/1	
8)	AXIS Test Box Output Buffer Card Circuit Diagram RSRO/010083/1	

1) INTRODUCTION

The AXIS Test BOX is a piece of equipment specifically designed to be used in the development and testing of elements for the T24 intra mural research project AXIS (ref 1).

This report is the final one of a series of four reports describing the AXIS Test Box. The first report (ref 2) is the Introduction to the AXIS Test Box and also acts as a guide to the supporting documentation etc. The second report (ref 3) is the Operating Guide and describes the User interaction with the Test Box and the facilities provided. The third report (ref 4) is the Software report and describes the software which provides the functions described in ref 3.

This report describes the hardware which has been specially designed to provide the Test Box functions. The individual circuit functions and their interactions are described. The logical operation of individual circuit blocks is described only when absolutely necessary.

2) The DISCUS Rack

The hardware of the AXIS Test Box is housed in a single 19 inch rack. The rack is designed to take standard double euro cards with indirect edge connectors. There are eight card positions in the rack, numbered 1 to 8 from left to right. Table 1 below indicates which card has been allocated to each card position. The backplane of the Test Box rack is an extension to the standard DISCUS backplane. The extra connections are listed in Table 2.

Rack Position	Card Description
1	External Interface To System Under Test
2	Output Buffer Card
3	Output Buffer PPI Card
4	Input Buffer Card
5	Input Buffer PPI Card
6	16K RAM
7	16K PROM
8	M6809 Microprocessor

Table 1 Position Of Cards In The Rack

Function	Connector Number	Card Position Number 1 2 3 4 5 6 7 8	Other Connections
AX +	BPLC C 5	----------	
AX -	C 6	----------	
DX +	C 7	----------	
DX -	C 8	----------	
TX +	C 9	----------	
TX -	C 10	----------	
AY +	C 11	----------	
AY -	C 12	----------	
DY +	C 13	----------	
DY -	C 14	----------	
TY +	C 15	----------	
TY -	C 16	----------	
op/ip	C 17	----------	
Start Tfr	C 18	----------	
CC Fail	C 19	----------	
AX TTL	C 20	----------	
Rx Trig	C 25	----------	
Tx Trig	C 26	----------	
up Clock	C 27	----------	8 BPUC A 31
GND	C 28	-	
Clock	C 29	----------	
Reset	C 30	----------	

Table 2 Extensions to DISCUS Backplane

NB. BPLC = Back Plane Lower Connector
BPUC = Back Plane Upper Connector
C 5 = 5th connector in row C
8 BPUC = Card 8 BPUC

3) The DISCUS Components

a) 16k RAM

The 16k RAM card holds 16k x 8 bits of Random Access, read write, Memory. This is used for the storage of program variables, message selection parameters and input messages. Approximately 6k bytes are used by the Test Box program.

b) 16k PROM

The 16k PROM card holds 16k x 8 bits of Programmable Read

Only Memory. The Test Box program and MMI messages occupy approximately 8k bytes of this memory.

c) PPI Card

Two Programmable Peripheral Interface (PPI) cards are used in the Test Box. Each card contains two PPI devices.

d) M 6809 Microprocessor

The M 6809 microprocessor card was designed to be DISCUS backplane compatible. The processor card also contains 'on-board' decoding for the Asynchronous Communications Interface Adaptor (ACIA) device which provides the interface to the VDU.
For a full description of the DISCUS components see ref 5.

4) The External Interface Card

The External Interface card contains no logic citcuits. Its primary function is to interface electrical signals on the backplane to convenient connection points on the card's front panel. The System Under Test (SUT) is controlled via the signals on six pairs of balanced lines. The function of these lines is listed for both input and output transfers in table 3 below, the X direction signals are then described in para 4.1 and the Y direction signals in para 4.2, ref 6 fully defines the interface. The external interface card connects these lines on the backplane (see table 2) to six pairs of 4mm banana sockets on the front panel. The SUT may then be connected to the Test Box via these banana sockets.

The interface also connects Transmit and Receive Trigger signals on the backplane to a switch on the front panel. The output from the switch is taken to a BNC socket also on the front panel thus allowing the User an oscilloscope trigger facility which may be used when investigating inputs to or outputs from the SUT, or when tracing the progress of messages within the SUT.

A second BNC socket is provided on the front panel so that an external clock source may be used, and a second switch used to select between external and internal clock sources.

NAME	DIRECTION	INPUT	OUTPUT
AX	CPU to SUT	Inactive	Control
DX	CPU to SUT	Input Grant	Data
TX	CPU to SUT	Timing	Timing
AY	SUT to CPU	Input Request	O/p ack
DY	SUT to CPU	Data	O/p ack
TY	SUT to CPU	Timing	O/p ack timing

Table 3 The Plessey Interface

4.1) The X Direction Signals

4.1.1) The ACTIVITY Signal

The ACTIVITY X signal is the primary control signal. A logic one on this wire indicates that an output transfer is in progress.

4.1.2) The DATA Signal

The DATA X wire has two functions, depenging on the state of the ACTIVITY X wire. A logic one on the ACTIVITY X indicates that the DATA X is being used to transfer data, ie. an output transfer. When the ACTIVITY X wire is at a logic zero DATA X is used as a control signal to indicate that an input transfer is in progress.

4.1.3) The TIMING Signal

The TIME X signal is in the quiescent state unless a transfer is in progress. When either an input or output transfer is in progress the TIME X signal governs the rate of data transfer.

4.2) The Y Direction Signals

4.2.1) The ACTIVITY Signal

The ACTIVITY Y signal has two uses. With a logic one on AX a, AY is used to indicate a response to an output transfer. When AX is at logic zero raising AY to logic one indicates a request for an input transfer. This request is then granted when DX is raised to a logic one.

4.2.2) The DATA Signal

The DATA Y signal has two uses: Firstly as the data path on an input transfer, and secondly as a response to an output transfer (in the same way as ACTIVITY Y).

4.2.3) The TIMING Signal

The TIME Y signal is in the quiescent state unless either an input transfer or the response to an output transfer is in progress.

5) The 'Two Card' System

Fig 1 illustrates the internal structure of the Test Box. The interface between the Test Box and the SUT is via the external interface card described in 4 above. The interface between the controlling microprocessor and the specially designed hardware is via the two PPI cards. One PPI card is used to interface to the Output Buffer card and the second PPI card

interfaces to the Input Buffer card. This means that two cards (a PPI card and a hardware card) are necessary to perform either outputs from or inputs to the microprocessor.

Each PPI card has two PPI devices. Each PPI device has three 8 bit ports A,B and C. Only ports A and B are used, leaving port C available for enhancements. The PPI devices are memory mapped, which means that each PPI port has a fixed address in the microprocessor memory area. Fig 2 indicates the PPI port addresses ,in Hexadecimal, and also defines the function of each used bit of each port. The letters down the left hand side in fig 2 (eg POPDAT) are the internal label names used in the program to identify each PPI port. The label name also gives an indication of the function of the port eg. POPDAT is the Peripheral OutPut DATa port. For a full description see ref 4.

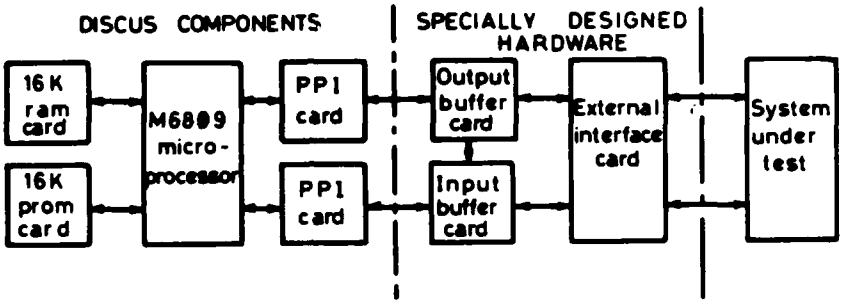

Fig 1 Test Box Internal Structure

6) Circuit Function Description - INPUT Buffer Card

Figure 3 is a representation of the functional circuit blocks of the Input Buffer card. The blocks correspond directly to the blocks outlined on the Input Buffer card circuit diagram (ref 7). The Input Buffer card handles inputs from the SUT to the Test Box at both control signal (AY etc) and message levels.

6.1) Input Interface

The input interface uses SN75107 devices to transform the Plessey interface (ref 6) balanced line format to the TTL logic levels used in the Test Box. The input signals received are ACTIVITY Y, DATA Y and TIMING Y (AY,DY and TY).

6.2) Check Code Verification

Ref 6 states that the three input transfer lines should

posess a certain timing relationship when an output transfer is taking place. AY and DY should be at logic one until the first four bits of the output message (the check code) have been received correctly by the SUT, they should then both be lowered to logic zero. If AY and DY have not assumed the correct level by the fourth clock pulse on TY the output check code is assumed to have failed. The 'check code OK/FAIL' flag (bit B1 of POPSTA) is then set to a logic one to indicate failure.
Although this circuit monitors the response to an output transfer it is correctly positioned on this card since it is the input signals AY,DY and TY which are being monitored.

6.3) Input Transfer Request

When the SUT has a message to send to the AXIS Test Box it signals so by raising the AY line. The AY line is also raised during output transfers as indicated in 6.2 above. AY going high will only be recognised as a valid request for input if AX is low at the same time. The 'input transfer request' flag (bit B1 of PIPSTA) is then raised. Since the interface conforms to a master slave organisation the SUT may request an input transfer but the transfer can only take place when the Test Box grants the request. Granting a request involves sending 48 clock pulses on the TX line and setting the DX line high for the duration of the this clock pulse train. 48 pulses are required for an input, replacing the 42 pulses necessary for an output, since the Test Box is replacing the S 250 CPU, and the S 250 uses the extra 6 pulses to insert its own Primary Switch Address value into the input message. When the Test Box has granted the request the Input Transfer Request circuit is reset ready to continue monitoring the AY and AX lines.

6.4) End of Input Transfer

The end of the input transfer is recognised by AY being lowered. Simultaneously AX must at logic zero. The end of input transfer circuit monitors the state of these two lines and sets the 'end of input transfer' flag (bit B2 of PIPSTA) when the above conditions are met.

6.5) Input Transfer Complete

If the setting of the 'end of input transfer' flag coincides with the 42nd clock pulse on TY then the 'ready to read' flag (bit B0 of PIPSTA) is also set.

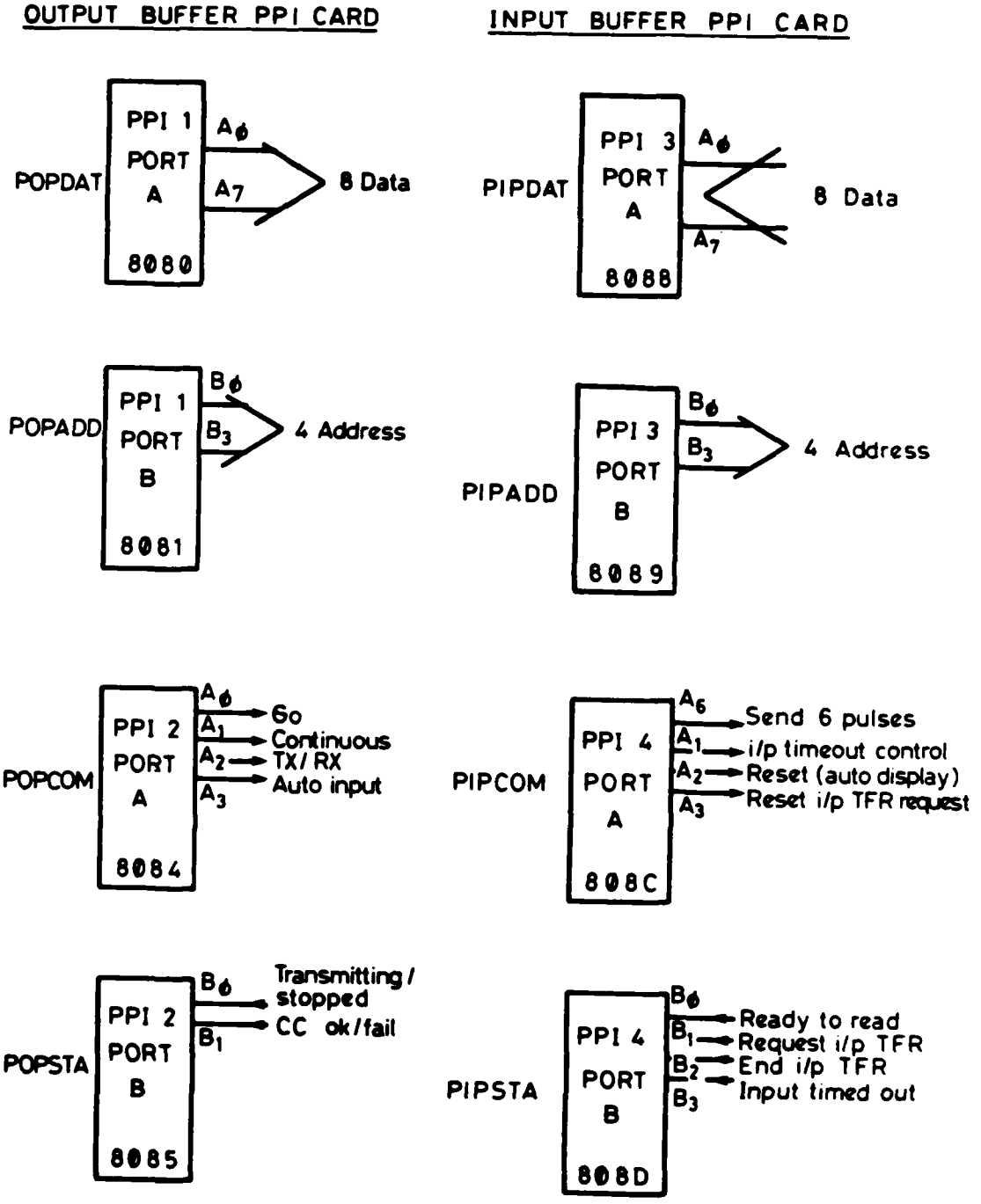

FIG 2. PPI PORT ADDRESSES AND BIT FUNCTIONS

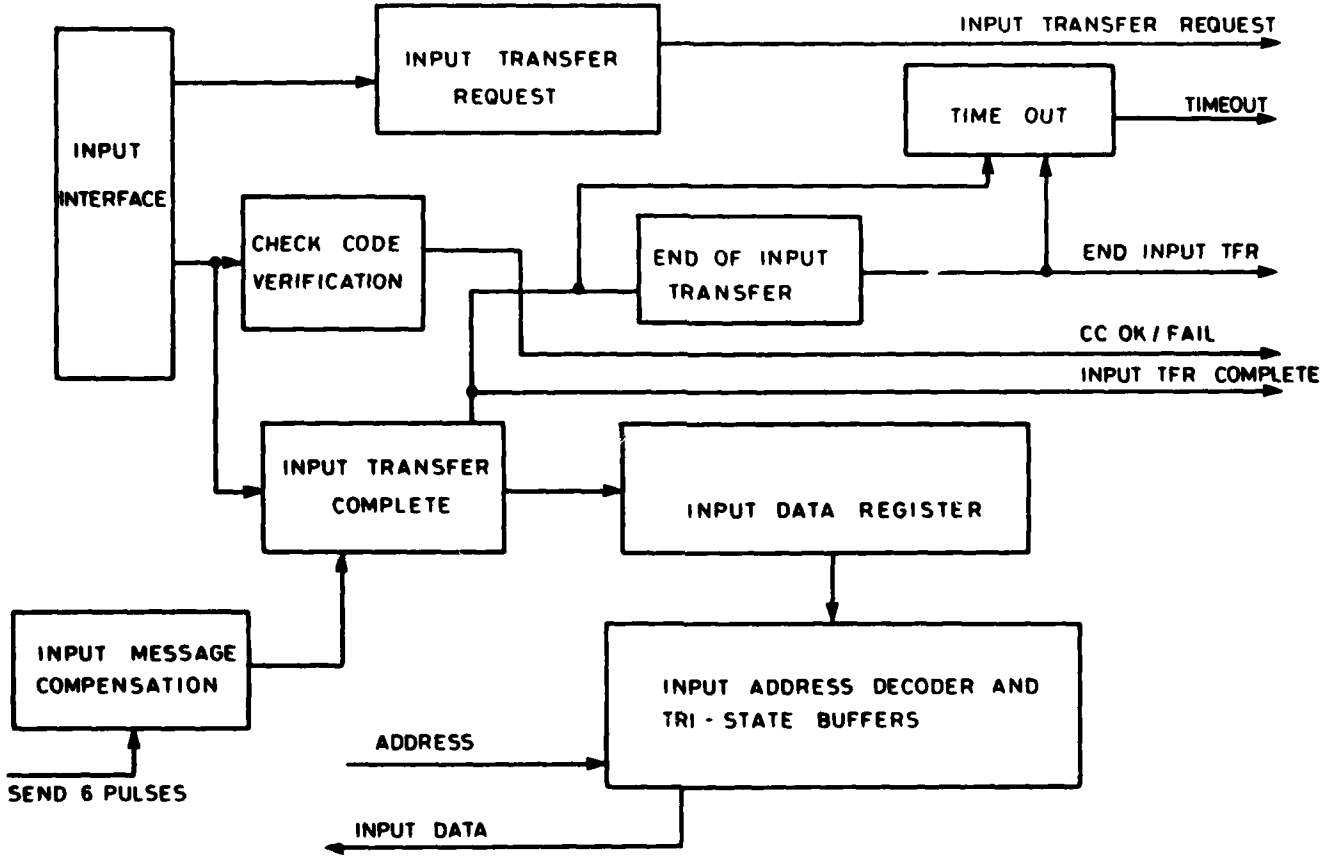

FIG. 3. BLOCK DIAGRAM INPUT BUFFER CARD

6.6) Input Message Compensation

Input transfers may have a GTU,Matrix Status or Matrix Connection register as the point of origin. GTU messages are always 42 bits in length Matrix messages are only 36 bits long. In order to standardise message bit positions it is necessary to insert six extra bits into Matrix input messages. The condition of these bits is unimportant so they are set to zero. Input messages from the Matrix will therefore be 42 bits in length, the last six bits being zeroes. This greatly simplifies the interpretation of input messages.
The input message compensation circuit is activated directly by the microprocessor if the 'end of input transfer' flag is set and the 'ready to read' flag is cleared. This circuit then injects six zeroes into the input data register for every message received from the Matrix Status or Matrix Connection registers. Six simulated clock pulses on TY also ensure that the input transfer request circuit (6.5 above) sets the 'ready to read' flag.

6.7) Input Data Register

The input data register is 42 bits in length, and is made up of five 8 bit registers and one 2 bit register. The compensated data from the DY line is loaded into this register in serial.

6.8) Input Address Decoder and Tri-State Buffers

The 42 bits of data in the input data register (IDR) have to be passed to the microprocessor as a six byte sequence via the single 8 bit port PIPDAT (Peripheral InPut DATa), which is port A of PPI 3 in fig 2. Six 8 bit tri-state buffers are provided. Table 4 below indicates which addresses have been allocated to each tri-state buffer on the input buffer card.
Each tri-state buffer can be loaded from its corresponding IDR register and all are connected to the PIPDAT 8 bit wide bus. Each buffer is enabled in sequence and the 42 bits of data read into the microprocessor memory. The enable input of each tri-state buffer is connected to a different output of a 4 line to 16 line decoder. The microprocessor outputs the address of each tri-state buffer via PIPADD (see fig 2) and the 4 line to 16 line decoder translates the address and enables the selected buffer.

Address in HEX	Register Selected
0	QUIESCENT STATE
1	IDR - Tri state 1
2	IDR - Tri state 2
3	IDR - Tri state 3
4	IDR - Tri state 4
5	IDR - Tri state 5
6	IDR - Tri state 6
7 to F	UNUSED

Table 4 Input Buffer Card Hardware Register Addresses

6.9) Time Out

After each output transfer an input transfer is expected in response. If there is a fault in the SUT the AXIS Test Box could get into a lockup situation looking for a response but not getting one. It would be possible to escape from this 'lock-up', but doing so would lose the sequence of input and output transfers, and would probably be very inconvenient. To prevent this happening a timeout circuit has been designed into the Test Box. This timeout is enabled after each output transfer and reset by the response input transfer. If an input response is not received within the timeout period the 'timeout' flag (bit B3 of PIPSTA) is set and the microprocessor can take appropriate action.

7) Circuit Function Description - OUTPUT Buffer Card

Figure 4 is a representation of the functional circuit blocks of the Output Buffer card. The blocks correspond directly to the blocks outlined on the Output Buffer circuit diagram (ref 8). The Output Buffer card handles outputs from the Test Box to the SUT at both control signal (AX etc) and message levels.

7.1) Output Interface

The output interface uses SN75110 devices to transform the the TTL logic levels used in the Test Box to the balanced line format required by the Plessey interface (ref 6). The output signals transmitted are ACTIVITY X, DATA X and TIMING X (AX,DX and TX).

7.2) Data Register A

Data register A is a 42 bit parallel in serial out

shift register, and is made up of six individual registers, five 8 bit registers and one 2 bit register. When data is clocked out of data register A it is not only sent to the output interface for transmission, it is also recirculated via the serial input of the data register B. Recirculating the data in this manner means that it is not necessary to reload the data registers after each output transfer.
The parallel data inputs of each component register of both the A and B data registers and the hardware counter are connected onto an 8 bit wide Data Bus (POPDAT in fig 2).
Fig 5 details Data Registers A and B and their interconnection with the data bus and the output address decoder (see para 7.4).

7.3) Data Register B

Data register B is a 42 bit shift register like data register A. Data clocked out in serial from this register is loaded into data register A in serial thus completing the recirculating loop.

Two data registers A and B are included to accomodate the option of transmitting two different output messages (see ref 3). Table 5 below indicates the initial contents of each data register, depending on the various menu options selected by the User (see ref 3).

Tx Option	Message Type	Register A	Register B
Single	A	Message A	Empty
Continuous	A	Message A	Message A
Multiple	A	Message A	Message A
Single	B	Message B	Empty
Continuous	B	Message B	Message B
Multiple	B	Message B	Message B
Single	T (both)	Message A	Message B
Continuous	T (both)	Message A	Message B
Multiple	T (both)	Message A	Message B

Table 5 Initial Data Register Contents

7.4) Output Address Decoder

The output address decoder is a 4 line to 16 line decoder. The 4 input lines represent addresses of each component register of the A and B data registers

and also the two registers which form the hardware counter. The information to be loaded into a particular register is placed on the Data Bus which joins all registers together, the address of the chosen register is then loaded onto the address inputs of the decoder via POPADD (see fig 2). The output line selected by the address input is then used to parallel load the data into the selected register. After each individual register is addressed output line zero (the quiescent state) is re-selected. Re-selecting the quiescent state has the effect of generating a pulse on the output line. This pulse is used to parallel load data into each component register as it is addressed. Table 6 below illustrates which hardware address has been assigned to each register on the output buffer card.

ADDRESS in HEX	Register Selected
0	QUIESCENT STATE
1	Register A - Shift register 1
2	Register A - Shift register 2
3	Register A - Shift register 3
4	Register A - Shift register 4
5	Register A - Shift register 5
6	Register A - Shift register 6
7	Register B - Shift register 1
8	Register B - Shift register 2
9	Register B - Shift register 3
A	Register B - Shift register 4
B	Register B - Shift register 5
C	Register B - Shift register 6
D	Hardware Counter - register 1
E	Hardware Counter - register 2
F	UNUSED

Table 6 Output Buffer Card Hardware Register Addresses

7.5) Hardware Output Counter

The hardware counter consists a 16 bit counter which is incremented every time an output takes place. The value of this counter is compared with the number of outputs required (this number having been stored in two 8 bit latches). The comparison is performed by four 4 bit magnitude comparators. When the two numbers are equal an equality pulse is generated.

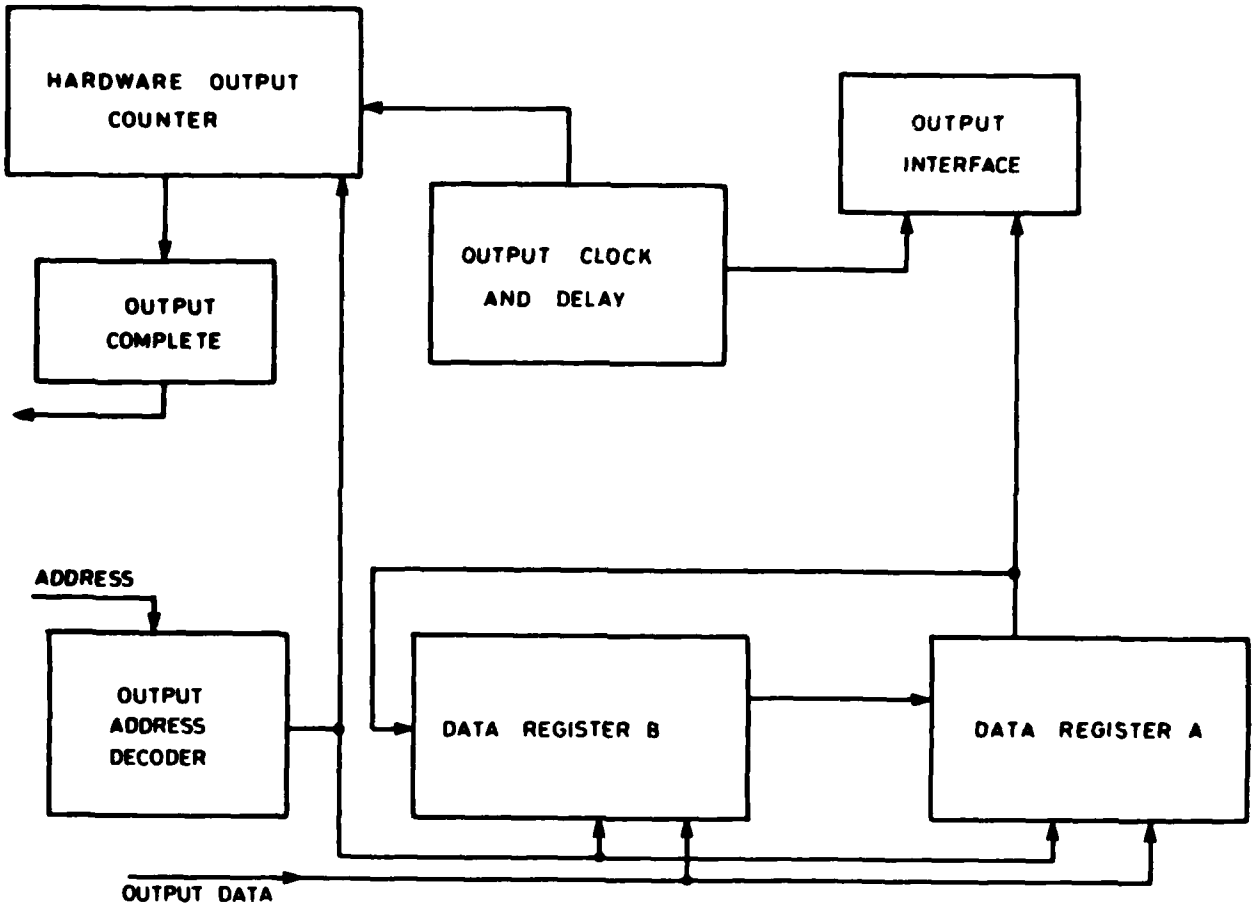

FIG. 4. BLOCK DIAGRAM OUTPUT BUFFER CARD

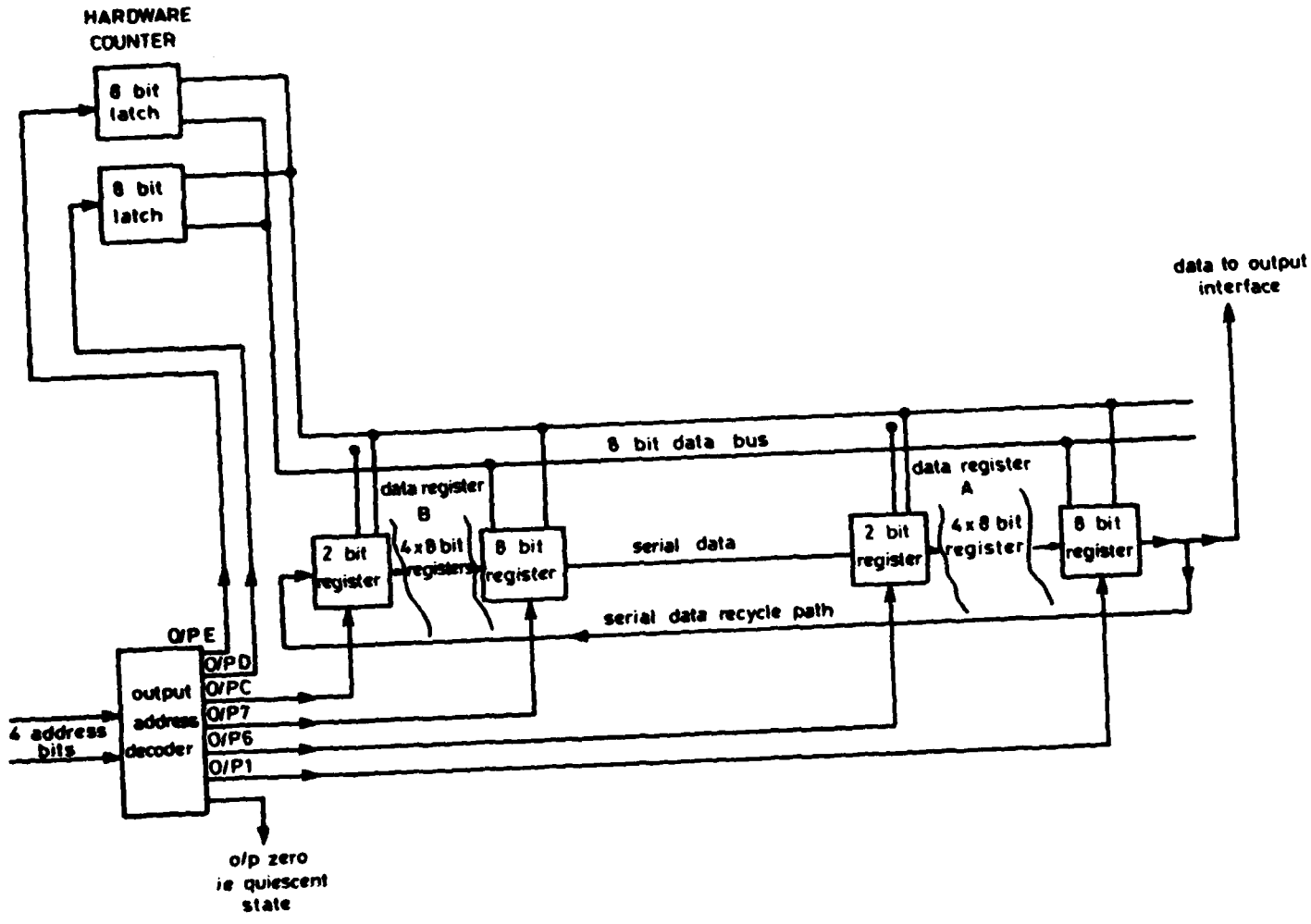

FIG.5. ADDRESS AND DATA BUS CONNECTIONS

If the User has selected Continuous outputs the number 1 is loaded into the data latches and the 'Continuous' command bit (see fig 2) is held at a logic one by the microprocessor which keeps the incrementing counter in reset mode, thus ensuring the two numbers can not equate and the equality pulse cannot be generated. In the case of Continuous outputs User intervention is required to instruct the microprocessor to stop outputs. This is achieved by removal of the counter reset, the next output transfer will then cause the equality pulse to be generated.

7.6) Output Complete

The equality pulse generated by the hardware counter is used by the output complete circuit to inhibit the clock and delay circuit thus stopping output transfers, and is also used to set bit B0 of POPSTA (see fig 2) to a logic one informing the microprocessor that the selected number of output transfers has been sent.
The GO (see para 7.7 below) pulse generated by the microprocessor to start the next sequence of output transfers is also used to reset the output complete and hardware counter circuits.

7.7) Output Clock And Delay

Each output transfer is 42 bits long. This is the reason that the Data registers are exactly 42 bits long and not a more uniform 40 or 48 bits. The output clock and delay circuit generates exactly 42 clock pulses for each output transfer and also generates a inter output delay of 256 clock cycles. A pulse called the GO pulse generated by the microprocessor on bit A0 of POPCOM (see fig 2). This GO pulse is used to start any output or input sequence, but since the microprocessor and the SUT will probably be operating with without a fixed frequency and/or it phase relationship, it must first be re-timed to ensure synchronisation. When the output or input sequence has been started the clock and delay circuit will continue to generate the clock for output transfers until the 'output complete' pulse described in 7.6 above causes output transfers to be stopped.
The output clock and delay circuit also has a role in input transfers. When a request for input transfer is granted the microprocessor instructs this circuit to generate 48 clock pulses to be transmitted on TX to enable the SUT to send its input transfer.
The clock and delay circuit also controls the interrelationship between the AX,DX and TX lines for both input and output transfers (see ref 6).

8) Special Circuit Features

The input and output buffer boards have been designed to be as simple and easy to maintain as possible. Only one circuit needs special description and that is the output clock and delay circuit. The output clock and delay uses a Motorola MC14557 1 to 64 bit variable length shift register to generate the 42 pulses for an output transfer, this same integrated circuit is also used to generate the 48 pulses necessary for an input transfer. This is possible because two of the length control inputs L2 (pin 1) and L4 (pin 15) are controlled by the microprocessor via bit A2 of POPCOM (see fig 2) thus programming the variable length shift register to suit either input or output transfers.

9) Conclusions

The AXIS Test Box has been in use for several months. Several minor changes and additions have been suggested by various users, all these changes have been incorporated by modifications to the Test Box software. The hardware design has remained stable throughout this period.

The existing hardware Input Buffer and Output Buffer cards which were made using backwiring techniques, will be replaced by printed circuit card versions. This will have two advantages;

a) When the hardware cards were made the only chip holders available were not of top quality. These suspect chip holders will be replaced by precision machined alternatives.

b) All the materials will be readily available when a second Test Box is required.

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7. Title

The Axis Test Box Hardware Report

7a. Title in Foreign Language (in the case of translations)

7b. Presented at (for conference papers) Title, place and date of conference

8. Author 1 Surname, initials	9(a) Author 2	9(b) Authors 3,4...	10. Date	pp. ref.
Simcock, A L				

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Abstract

This Memorandum describes in detail the hardware which has been designed specifically to perform the functions required of the Axis Test Box. The interfaces to other, general purpose, circuits are also defined.

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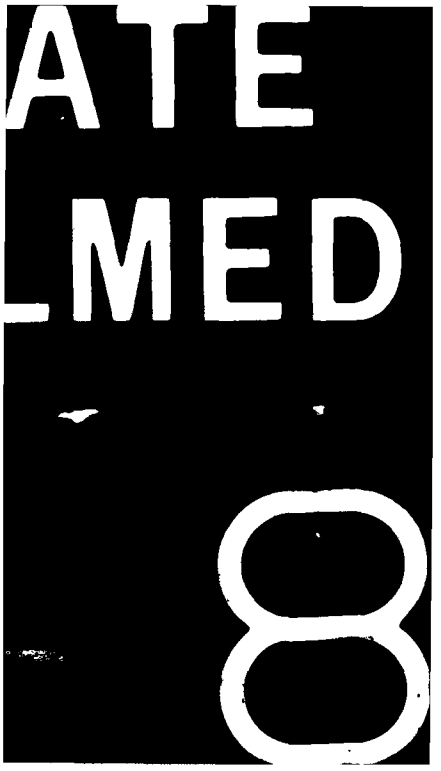
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