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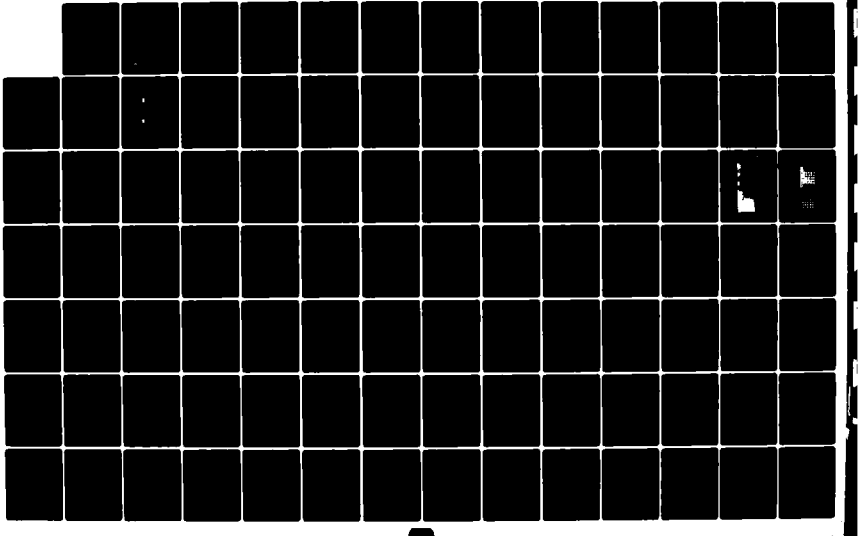

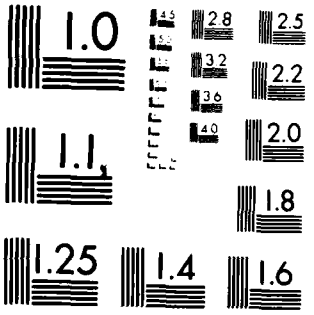

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THERMOELECTRICALLY COOLED FOCAL PLANE ARRAY MODULE

SEMI-ANNUAL TECHNICAL REPORT FINAL #1

28 September 1978 to 28 February 1979

W. E. Tennant

(805) 498-4545

Sponsored by:

Procurement and Production Directorate
Fort Belvoir, VA 22060

Rockwell International Science Center
1049 Camino Dos Rios
Thousand Oaks, California 91360

Rockwell International
Science Center

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PRINCIPAL INVESTIGATOR W. E. TENNANT

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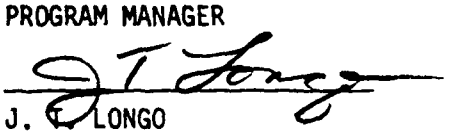

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This is the first semi-annual report of a project to develop a thermoelectrically cooled staring focal plane module. The approach is that of a backside-illuminated hybrid mosaic array coupled to a silicon CCD/MUX. The detector approach is based on a transparent substrate/heteroepitaxy technology, and the multiplexer incorporates background skimming, gain reduction, and frame transfer concepts.

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To permit long staring times it is necessary to have low leakage detectors. Planar detectors fabricated in InAsSb epilayers grown on GaSb substrates have exhibited leakage currents as low as 4×10^{-4} A/cm^2 at 195 K, about a factor of 2 from program goals. The corresponding R_oA is 42 Ω-cm^2. A basic understanding of the diode operation has been obtained. Surface passivation and doping control appear to be the key parameters.

To permit high density hybrid mosaic fabrication, techniques of indium column growth have been developed which will permit interconnects of sufficient height to meet final program goals.

Based on a thorough noise analysis, a test chip has been designed, and mask generation started. The circuits tested on this chip when incorporated into the final multiplexer should permit operation with the program D* goals even for staring times as long as 16 ms.

FOREWORD

The work reported in this document was performed at the Science Center, Rockwell International, Thousand Oaks, California, and at Electronics Research Center, Rockwell International, Anaheim, California. The work was supported by the U.S. Army Night Vision and Electro-Optical Laboratories, Fort Belvoir, Virginia under Contract Number DAAK70-78-C-0196. The monitoring engineers for NVEOL are R. E. Flannery and R. Balcerak.

The principal investigator was W. E. Tennant. D. H. Seib, J. P. Rode, G. M. Williams, and D. I. Cheung were project engineers. Additional support was given by R. A. Reidel, R., E. Eisel and F. A. Cox.

The program manager was A. M. Andrews.

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This is the first semi-annual report of a project to develop a thermoelectrically cooled staring focal plane module. The approach is that of a backside-illuminated hybrid mosaic array coupled to a silicon CCD/MUX. The detector approach is based on a transparent substrate/heteroepitaxy technology, and the multiplexer incorporates background skimming, gain reduction, and frame transfer concepts.

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1.0 REPORT SUMMARY

1.1 Program Objective

The program objective is to develop a high density, TE cooled, staring focal plane technology for use in applications such as hand-held viewers, guidance systems, and missile seekers. These objectives can best be met with photovoltaic detectors fabricated from backside-illuminated intrinsic semiconductors. These high density arrays must then be electrically and physically connected to a Si integrator/multiplexer.

1.2 General Approach

The program approach is to fabricate devices of increasing performance and complexity to culminate at the end of the program with the fabrication and testing of an operational, packaged, TE cooled, high density staring imager. This imager will be a backside-illuminated InAsSb mosaic coupled to a specially designed Si CCD-MUX which incorporates background skimming, gain reduction, and frame transfer features to handle large amounts of charge. This hybrid structure will be mounted for testing in a TE cooler package.

1.2.1 Plan

In order to create the requisite technology, three areas of investigation have been defined. These are: detector development, multiplexer development, and hybrid integration. In the area of detector development, several intermediate goals have been set and tied as closely as possible to specific research activities and deliverables. The program schedule (Appendix A) summarizes the plan and intermediate goals as conceived in the first two months modified slightly by the results of the first six months.

1.2.2 Specific Goals

Key goals for the detector portion of the program during the first six months were to attain >13 Ω-cm^2 R_0A products for over 90% of the diodes in an array, to obtain a quantum efficiency-fill factor product of greater than 50%, and to develop some understanding of the important parameters in improving the performance of small geometry devices.

For the multiplexer portion of the program, the specific goals included completion of the initial test chip design layout and analysis, completion of the 64 x 64 analysis, the start of test chip mask tape generation, and the start of test equipment design.

For the hybrid integration portion of the program, the specific goals were to design and fabricate test masks, to develop small geometry column growth on 5 x 5 arrays, and to fabricate hybrid structures from these arrays.

1.3 Accomplishments

The principal accomplishment of this six months was to fabricate diodes with R_0A products from 20 to over 40 Ω-cm^2. Because of their high material quality and low surface generation, these diodes exhibit a limited diffusion volume structure in which the volume which generates leakage current lies well within a recombination length of the junction. Because of this limited diffusion geometry, the leakage current of these devices is much lower (R_0A much higher) than would be expected from a simple narrow base diode model. Some insights have been gained from the analysis of these diodes which suggest ways of further improving diode performance and passivating the diodes. The successful passivation of these diodes would place the detector effort within a factor of two of the program goals.

Also in the detector area, the dislocation density-diode quality study has been completed resulting in a rejection criterion for InAsSb epitaxial layers. A melt bake study has been completed. Small geometry field plate devices have been fabricated using Au metal masking.

Accomplishments in the hybrid integration area have been the growth of In columns on 25, 50, 75, and 100 μm geometries and the fabrication of hybrid test structures from these devices. The small geometry hybrid work was made possible by the completion of test masks in mid-January.

Accomplishments in the multiplexer area have been to complete the noise analysis of the multiplexer. This analysis has included several approaches to input circuitry, gain reduction, and storage array operation and has incorporated 1/f noise calculations. The results show that the desired system D* is attainable with the full 16 ms integration time. Test chip

circuits implementing the most promising approaches have been designed and are nearly complete. Digitization of the masks is well underway.

2.0 TECHNICAL APPROACH

In order to obtain the highest possible performance from a TE cooled imager, the focal plane module approach incorporates several unique features. Figure 2.1 portrays the essential elements of the imager. Figure 2.2 shows the details of the hybrid structure. Light is incident through a mechanically strong, AR-coated, transparent substrate on diodes in the active layer. This configuration permits a very high percentage optically active area. Signal current is read out through indium column interconnects into a silicon CCD. Because of the need to handle large amounts of current without degradation in signal-to-noise, background skimming, gain reduction, and subframe transfer and storage are employed in the multiplexer to obtain on chip the potential of several milleseconds of integration time. To develop the necessary technology to build this imager, we are investigating new detector concepts, new hybrid fabrication techniques, and new multiplexer designs.

2.1 Detector Approach

2.1.1 R_oA Improvement

The baseline detector configuration is a planar, Be^+ ion implanted backside-illuminated array of photodiodes fabricated in a liquid phase epitaxial layer of $InAs_{0.9}Sb_{0.1}$ (λ_c = 4.4 μm @ 195 K) grown on a GaSb substrate. In Fig. 2.3, a schematic cross section of a detector is shown together with several parameters which are essential to the analysis of this structure. These parameters are the recombination length, minority carrier lifetime, minority carrier diffusivity, doping level, and thickness of semiconductor material on each side of the junction. Another key ingredient (not shown) is the surface (or heterojunction interface) recombination velocity which must be low unless the surface is isolated from the junction by a potential barrier. Several limiting cases can be obtained from the basic diode structure. The most important ones relating to our basic device design are shown in Fig. 2.4. The bulk limit occurs when the dimensions of the device are much greater than the recombination lengths. From the estimated parameter values shown in Table 2.1, it is clear that the current InAsSb arrays cannot

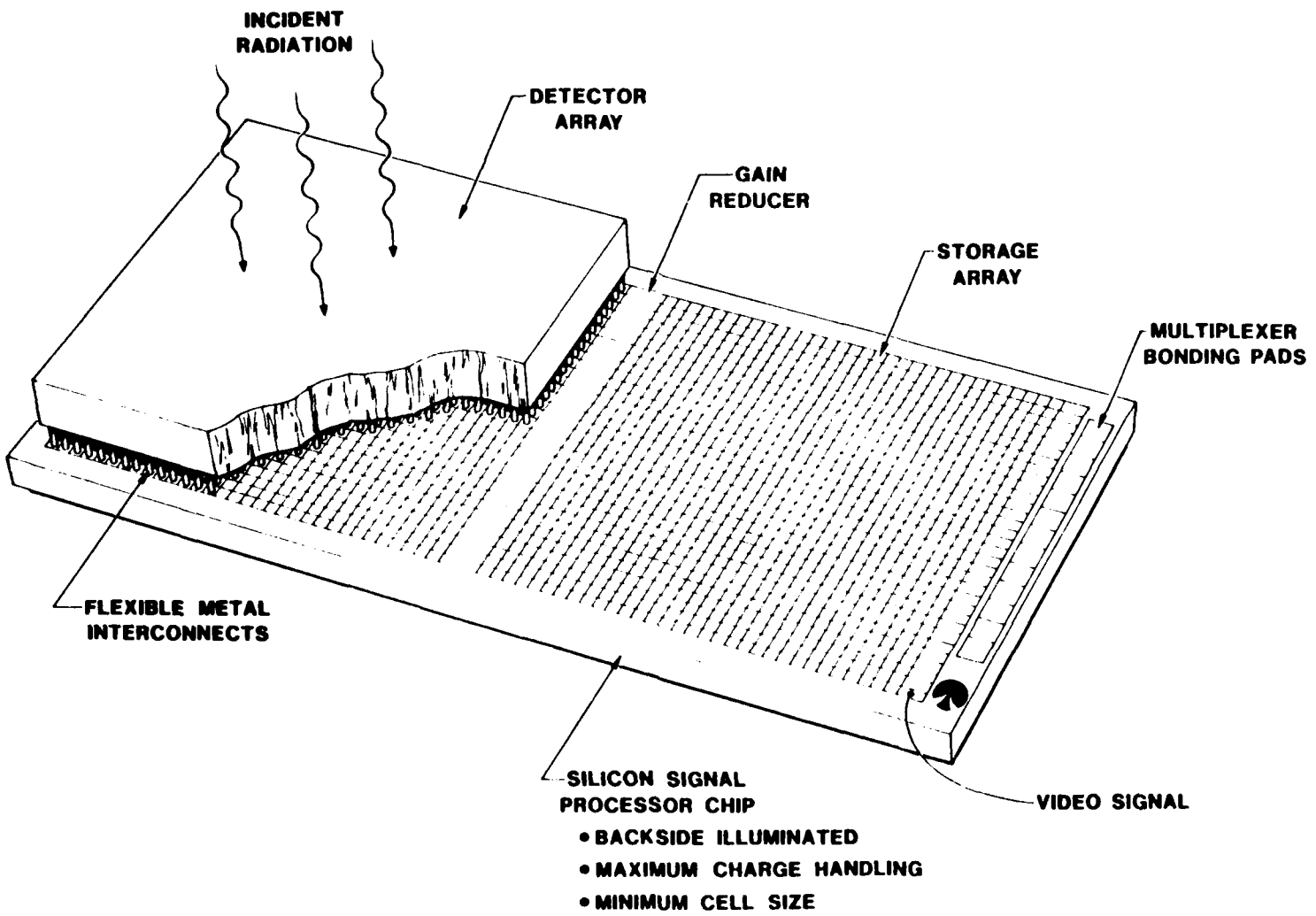

Fig. 2.1 IE STARE frame transfer concept.

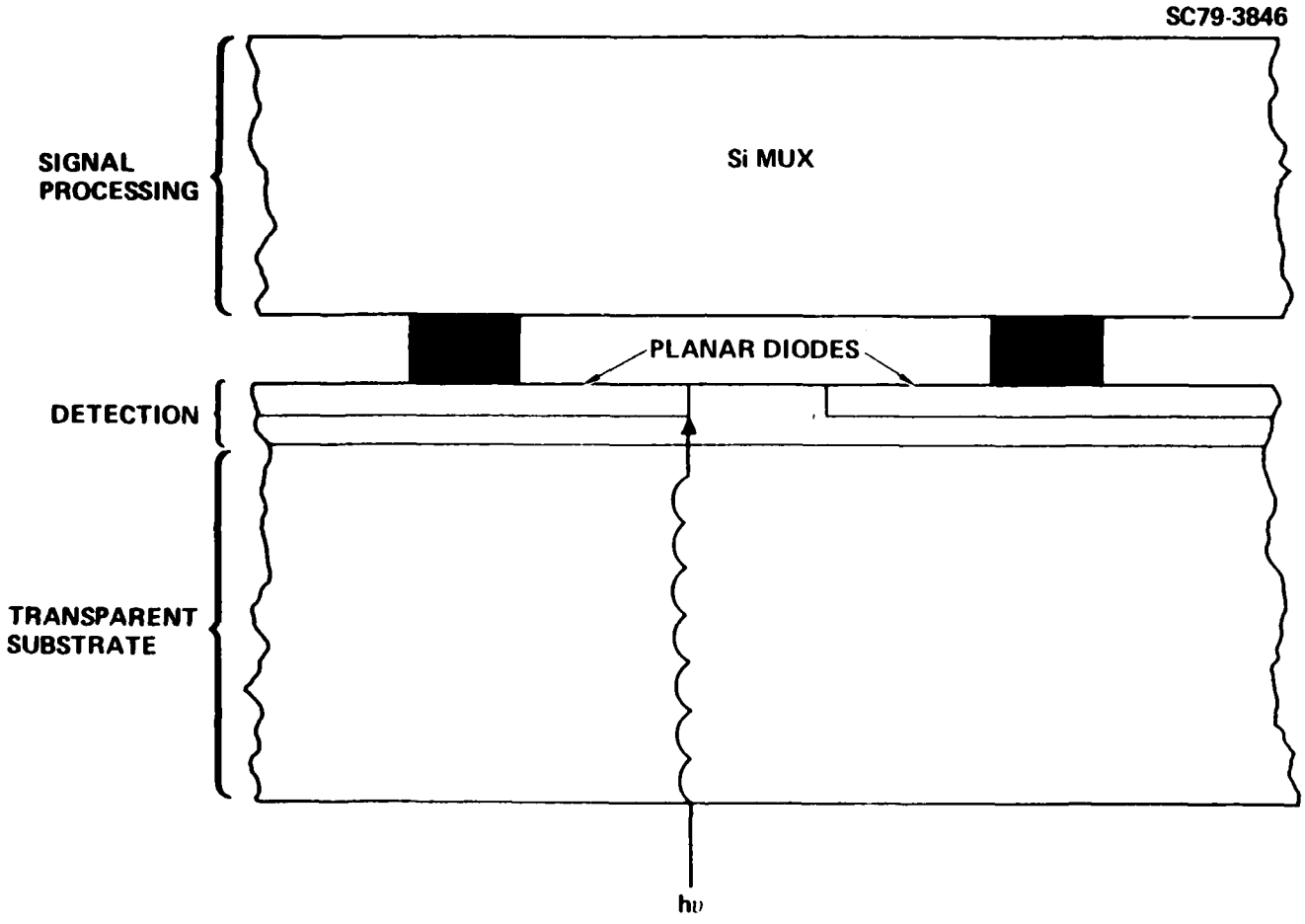

Fig. 2.2 Hybrid focal plane concept.

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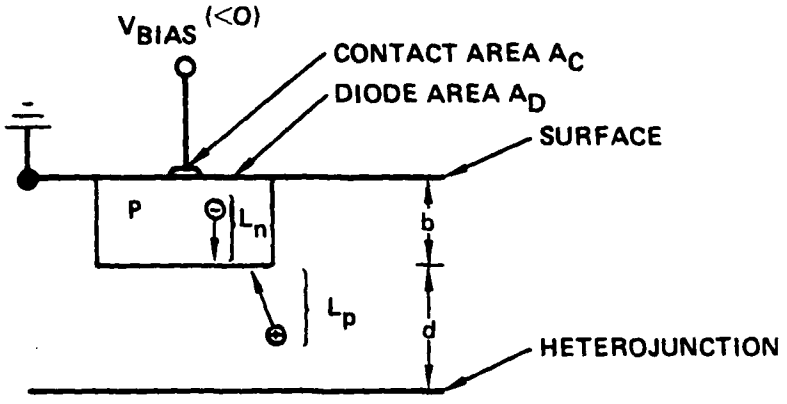

USEFUL RELATIONSHIPS & DEFINITIONS:

$L = \sqrt{D\tau} = \sqrt{\frac{\mu kT\tau}{q}}$ = CARRIER RECOMBINATION LENGTH

τ = MINORITY CARRIER LIFETIME

D = MINORITY CARRIER DIFFUSION CONSTANT

μ = MINORITY CARRIER MOBILITY

b = P-REGION DEPTH

d = n-REGION DEPTH

Fig. 2.3 Planar detector structure.

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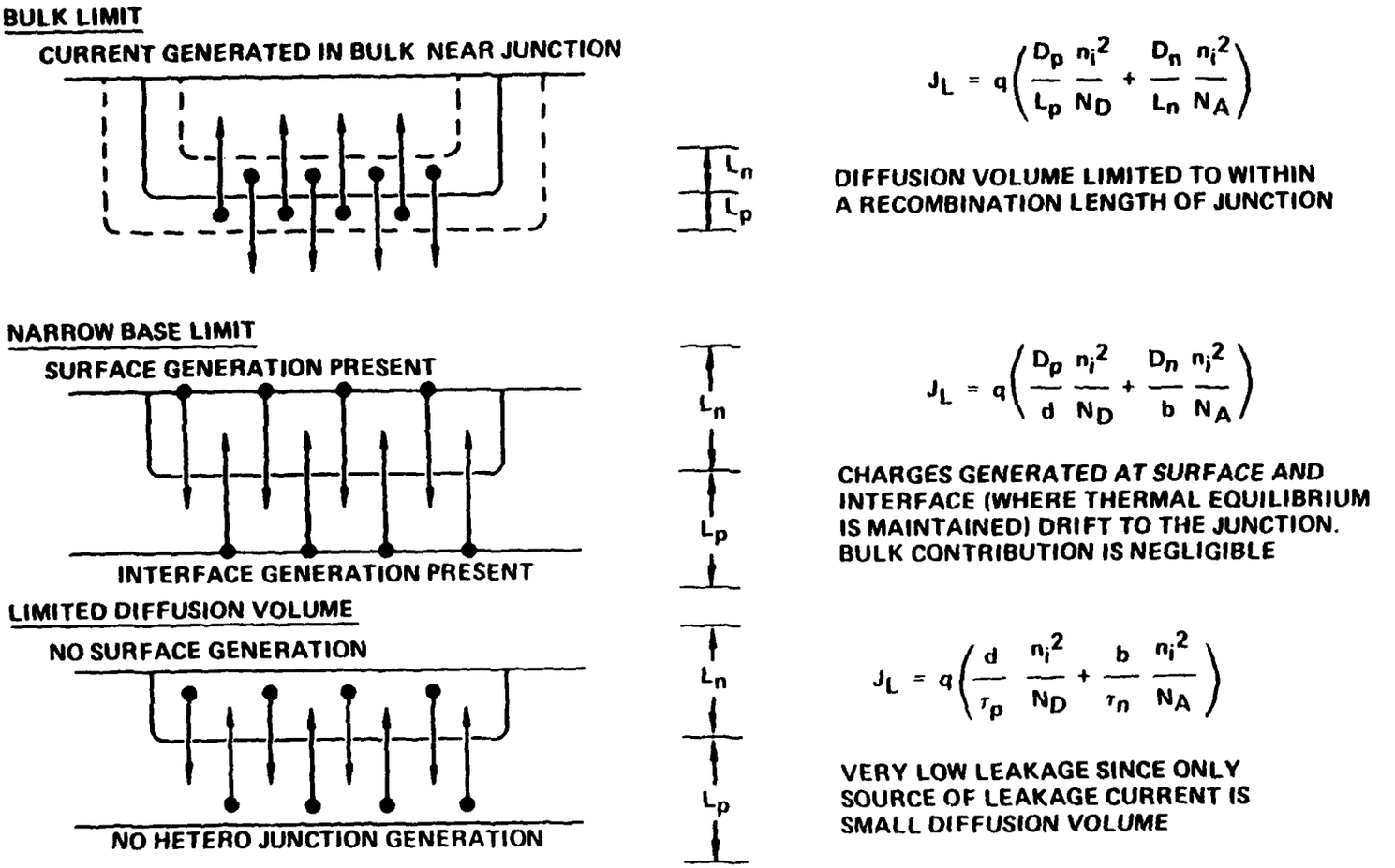


Fig. 2.4 Leakage current in various limits.

Table 2.1

Estimated InAsSb Material Parameters at 195K

Parameter	Values	Source
μ_n	6×10^4 cm^2/V-sec	Interpolation from InAs, InSb
D_n	10^3 cm^2/sec	From μ_n
τ_n	5×10^{-7} sec	From InSb @ 77 K
L_n calc.	220 μm	From D_n, τ_n
L_n meas.	24 μm	EBIC at 77 K
μ_p	390 cm^2/V-sec	Interpolation from InAs, InSb
D_p	6.54 cm^2/sec	From μ_p
τ_p	6×10^{-7}	Auger in InAs for 10^{16}/cm^3 = N_D
L_p calc.	20 μm	From D_p, τ_p
L_d meas.	5.5 μm	From EBIC at 77 K
N_A	10^{17}/cm^3	From SIMS
N_D	10^{16}/cm^3	From C-V of p-n junction
b	4 μm	Typical EBIC
d	2 μm	Typical EBIC

Narrow base limit

$$J_{L_n} = q \frac{D_n}{b} \frac{n_i^2}{N_A} = 205 \times 10^{-5} \text{ A/cm}^2$$

$$J_{L_p} = q \frac{D_p}{d} \frac{n_i^2}{N_D} = 27 \times 10^{-5} \text{ A/cm}^2$$

Limited diffusion volume limit

$$J_{L_n} = q \frac{b}{\tau} \frac{n_i^2}{N_A} = 6.6 \times 10^{-7} \text{ A/cm}^2$$

$$J_{L_p} = q \frac{d}{\tau} \frac{n_i^2}{N_D} = 2.7 \times 10^{-6} \text{A/cm}^2$$

be bulk limited in the electron contribution to the leakage current from the p-side of the junction. The recombination length for holes from the n-side, on the other hand, is sufficiently short that bulk generation may make some contribution. The most likely models to apply to the current devices, however, are the narrow base model and the limited diffusion volume model.

A narrow base diode will inevitably have higher leakage than a bulk limited diode with the same dopant concentration. This is simply because the high generation rate at the diode surface maintains the minority carrier equilibrium concentration (n_i^2/N_A or N_D) much closer to the junction than would be the case for a bulk limited diode. This limit of diode operation may still be useful, however, if the equilibrium minority carrier concentration can be reduced to a point in which the leakage current is within acceptable limits. This may be done by increasing the doping level N_A or N_D. Such an increase will eventually reduce the reombination length L_n or L_p. Therefore, raising the doping level will cease to help when the recombination length becomes less than the base width. It is also possible to decrease the diode leakage by increasing the base width. Thus, for the parameters shown on the table, doubling the base width and increasing the carrier concentration to $N_A > 10^{18}$ would lower the p-side leakage to $10^{-4}A/cm^2$, which is within the program goals. Leakage current from the n-side in this limit might be reduced by a factor of two by doubling the doping level of the n-layer, providing that the recombination length did not become unacceptably small.

The limited diffusion volume geometry has the greatest potential for diode performance. A limited diffusion volume diode can potentially have lower leakage than the bulk. The key requirements for operation in a limited diffusion mode are (a) surfaces and interfaces near the junction which block the passage of minority carriers, and (b) negligible generation rates at these surfaces. Epitaxial growth and implant diffusion techniques make the first requirement very straightforward. The second requirement involves the passivation of diode surfaces and interfaces. The problem is further complicated by the need to cover the top surface of the diode array to protect it from the surrounding environment (including subsequent processing and hybrid mating). At lower temperatures (77 K) SiO_2:N has successfully been used with a field plate to passivate the surface. At these temperatures, however, surface

generation over the diode area is insignificant because of the low equilibrium minority carrier concentration. The principal leakage mechanism at 77 K is perimeter leakage, which is satisfactorily controlled by the field plated SiO_2 structure. The ability of SiO_2:N to provide a satisfactory passivation at 195 K has not been fully explored and the initial results are mixed. To passivate the p-side of the junction, therefore, it is desirable to consider a variety of possible coating materials in addition to SiO_2 such as Al_2O_3 and As_2S_3 which have been used successfully on other III-V semiconductors. Another approach to passivating the surface is to epitaxially deposit a wide-bandgap III-V semiconductor over the surface creating a heterojunction where the surface used to be. Because of the low minority carrier concentration in such a layer, the leakage current would be quite low. Of course the requirement for a high quality heterojunction replaces that for a passive surface. Nevertheless, because of the similarities between overlayer and active layer, a low-generation heterojunction may be possible.

To obtain a limited diffusion structure on the n-side of the junction, again a low generation heterojunction is required. For an abrupt n-InAsSb n-GaSb interface, theory predicts a potential barrier to holes from the InAsSb crossing the heterojunction. This also implies a reduced generation rate at this heterojunction, because more energetic holes must be generated to overcome the barrier. In practice, however, the heterojunction may have a small amount of alloying which would cause a reduction in the barrier height and might contribute extra leakage. A limited diffusion volume is automatically obtained in the n-region surrounding the diode perimeter if the neighboring diodes are within a recombination length of the diode in question.

In addition to geometrical considerations, it is important to establish a baseline for material quality thereby insuring that there is no degradation in lifetime due to dislocations. It is also important to consider the as-grown material purity to attempt to reduce impurities which might cause generation in the material and thereby reduce lifetimes.

In the area of small geometry diode fabrication, some unique considerations must be made. The first is that if the diode lateral separation is on the order of the recombination length, the effective diode collection area should essentially equal the pixel area. Thus, in a p/n geometry, the

separation between p-regions should be <5 μm. Provided that a suitable implant mask can be found which will hold these tolerances and provided that the junction placement can be controlled to distances of order ±1 μm, obtaining a large fractional active area should be possible.

To obtain adequate mask tolerance control, Au metal masks will be used in preference to photoresist masks which, because of the thickness required to block the beam, tend not to hold tolerances well. Previous results from SIMS and EBIC have shown that typical junction depths of 4-5 μm are obtained under the currently used diode implant and annealing conditions. This accuracy is sufficient for these initial studies, but future experiments will treat this question in greater detail.

For large area mosaics the ability to hold tolerances over long distances also arises. For such geometries good wafer surface planarity is important. Therefore, the fabrication of diodes in polished epitaxial layers is important.

2.2 Hybrid Integration

The critical issues in the area of hybrid integration are: (1) the nucleation and growth of uniform In columns (2) the height to width ratio of the columns, (3) the height of columns required for a given thermal displacement upon cooling to avoid column breakage, (4) the mechanical strength of the In-In cold weld bond, 5) the avoidance of shorting between compressed columns, and 6) the alignment required for mating. These issues have been solved for 75-100 μm geometries on other programs. The aspects which are unique to 25-50 μm geometries lie principally in the areas of adequate column height, the avoidance of shorting, and alignment.

It has been shown on other programs that a total column height of 15-18 μm prior to mating is adequate for a hybrid of 3200 μm on a side when cooled from room temperature to 77 K. Because the differential thermal contraction is only about half as severe on cooling to 195 K, columns of 10 μm height should suffice for similar array sizes. The most satisfactory approach to obtaining the desired column height with a minimum of excess lateral growth (which increases the possibility of shorting) is to grow columns of half the

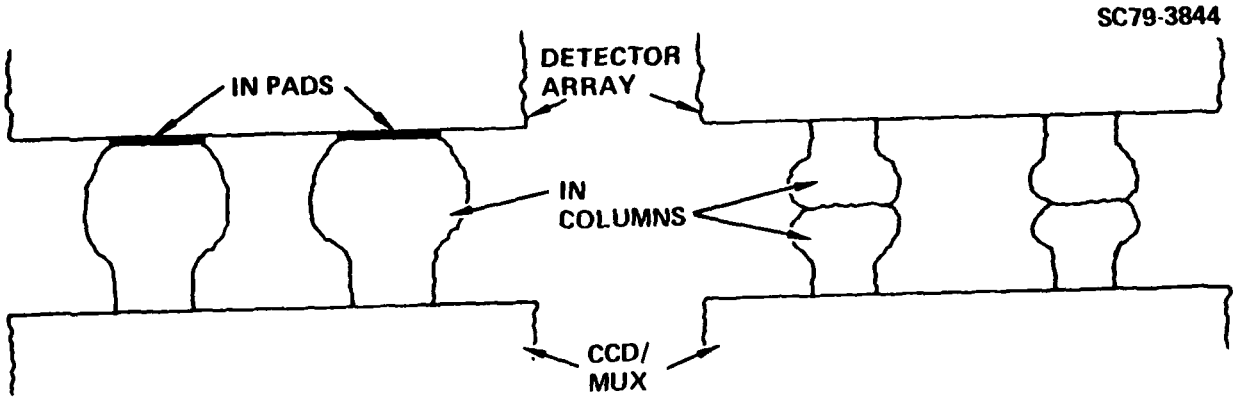
desired height on both surfaces to be mated (see Fig. 2.5). The columns are typically grown through holes defined in photoresist and thus the blooming which occurs when the column height exceeds the photoresist thickness is minimized in the two column approach. Furthermore because the columns can interpenetrate when compressed together, the oxide on the column surfaces is broken and the In-In cold weld formed is quite strong. By developing the two column approach with appropriate photoresist thickness, fabrication of small geometry hybrids is possible.

Alignment and mating of 75 and 100 μm arrays has been done routinely on current mating apparatus and initially no change is envisioned for 25 and 50 μm small array geometries, although some variation in temperature and pressure of mating should be explored to minimize column deformation for 25 μm devices.

The 26 element test array patterns are shown in Fig. 2.6. The 75 and 100 μm devices will be mated in a single hybrid structure as the 25 and 50 μm devices. Only two arrays from any hybrid structure will be bonded, however, because of the large number of test leads required. In addition to the twenty six diode leads each test array has a field plate and a ground connection. The test flow pattern for these arrays is given in Fig. 2.7.

2.3 Multiplexer Approach

The multiplexer chip for the thermoelectrically cooled focal plane module must accept charge from an area array of photodiodes and provide readout of these charge signals with minimum added noise or duty cycle reduction. One of the major problems which must be confronted in the multiplexer design is the need to handle a large amount of current (background photocurrent plus leakage current) with small unit cell sizes (2 mil x 2 mil). The nominal value for the detector leakage current at 195 K, which will be used in the following discussion, is 5 nA (corresponding to an R_0A of ~85). Assuming 3 nA of background generated current, an average of 8 nA of current must be accommodated at each detector site, given a direct injection input. This corresponds to 5×10^{10} holes/sec, or in a 16 msec frame, 8×10^8 holes/detector input. This greatly exceeds the possible charge storage capacity in a 2 mil cell; for 1000Å oxide, 15 V storage voltage, and ~20% of the cell



SINGLE COLUMN

- ADEQUATE COLUMN HEIGHT FOR 3-4 MIL GEOMETRIES UP TO 1/8 IN. CHIP SIZES
- COLUMNS TOO LARGE FOR FINE GEOMETRIES

DOUBLE COLUMN

- SAME OR GREATER COLUMN HEIGHT AS SINGLE COLUMN
- COLUMNS SMALL ENOUGH FOR 1-2 MIL GEOMETRIES
- HIGHER INTERCONNECT STRENGTH

Fig. 2.5 Indium column interconnect techniques.

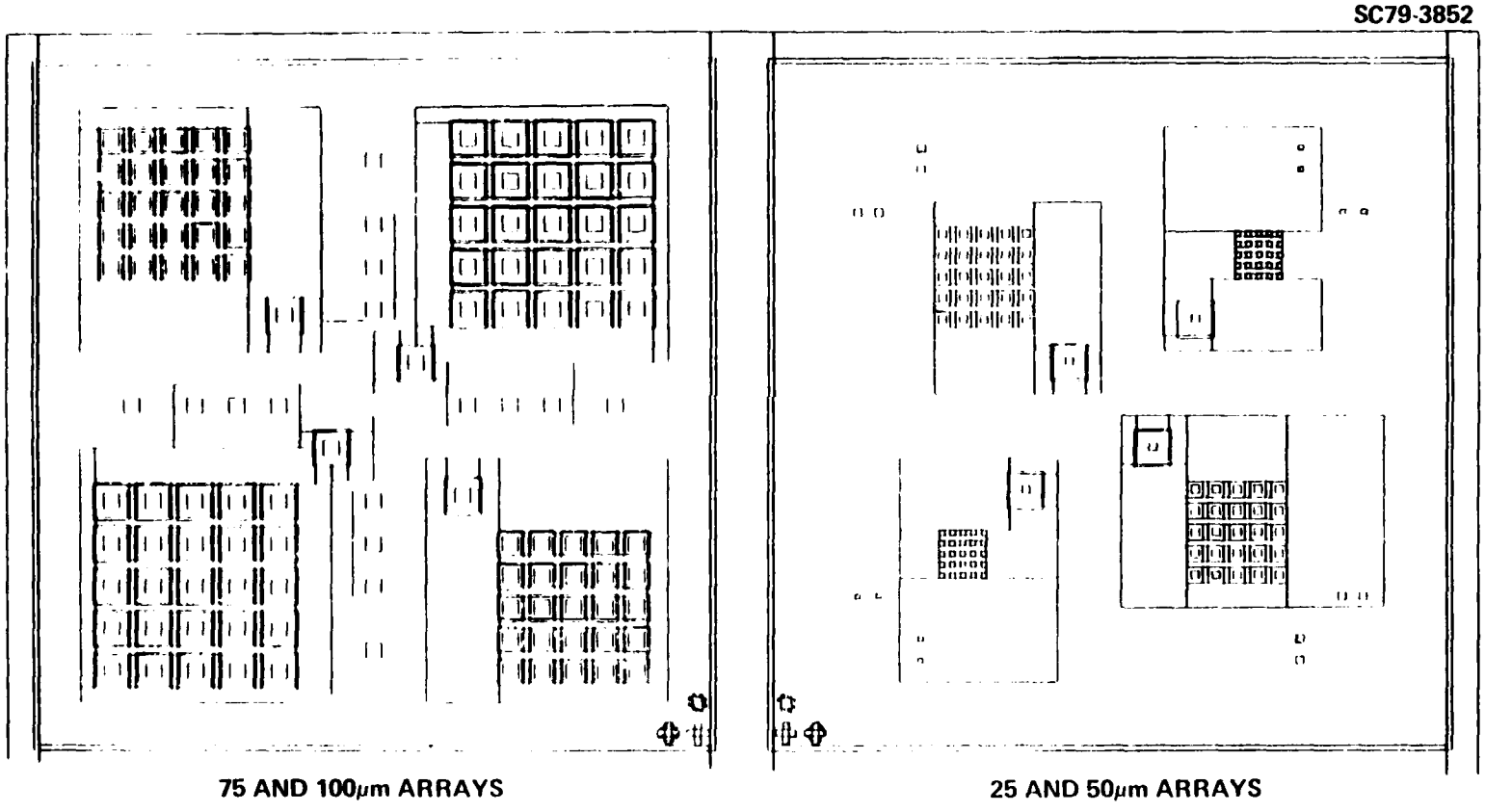


Fig. 2.6 TE STARE test array pattern.

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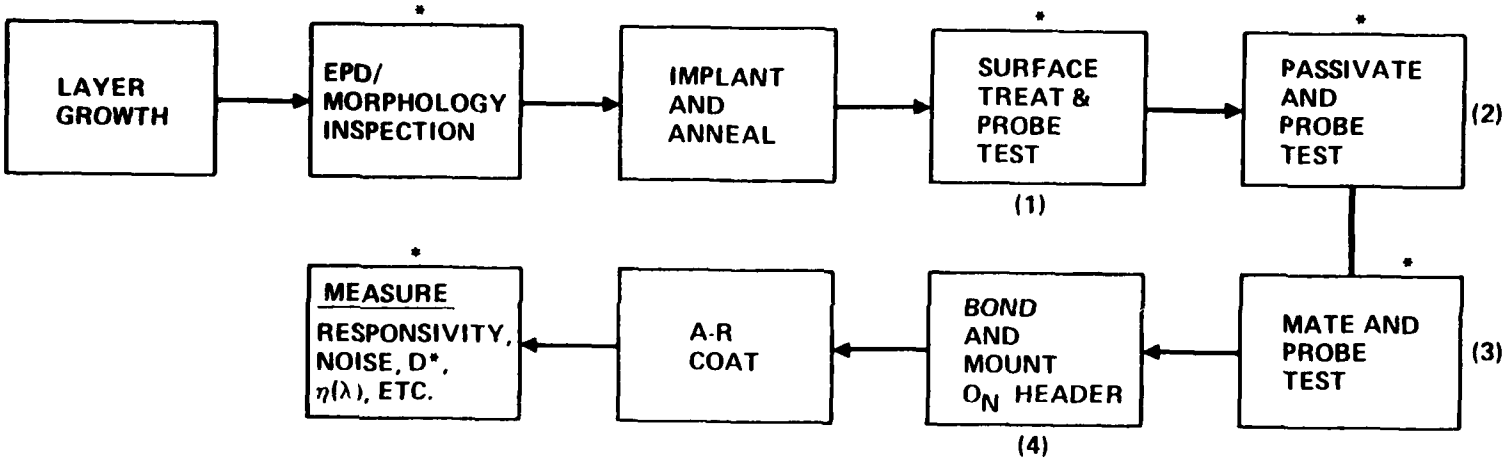

* INDICATES REJECTION CRITERIA APPLIED AT THIS POINT

(1) TO DETERMINE POTENTIAL LAYER QUALITY
(2) TO STUDY SURFACE PASSIVATION EFFECTIVENESS
(3) TO DETERMINE BEST ARRAYS FOR BONDING
(4) TWO ARRAYS CAN BE TESTED PER HEADER

Fig. 2.7 Fabrication and test flow pattern.

available for storage, this capacity is ~1.7 x 10^7 holes. This then implies a factor of 47 overload in the frame time.

The approach taken to accommodate this charge overload is as follows:

1. Divide the frame (stare time) into a number, N_{SF}, of subframes to limit the amount of charge which must be handled at any one time;

2. Use background skimming in each input cell to remove up to 80% of the unwanted background and leakage charge generated, in order to preserve charge capacity for signal charge and lengthen the integration time per subframe;

3. After each subframe, readout the charge from each column to a gain reducer which creates an attenuated charge replica of each subframe, with minimum added noise;

4. And finally, accumulate the N_{SF} attenuated subframe charges in a storage array and then readout the reconstituted frame.

A schematic drawing indicating this approach is shown in Fig. 2.8. In the focal plane array section, consisting of direct injection input FET, with skimmer, and charge transfer registers, the detector currents are integrated. These charge packets are then transferred to gain reducers (one per column of the focal plane section), where an attenuated (reduced in size by a constant scale factor) charge packet is generated sequentially for all pixels of a given column. These reduced charge packets are then introduced into the storage array, where all charge packets for a given pixel from the N_{SF} subframes are accumulated and stored in a location with one-to-one correspondence to the pixel position in the focal plane array section. After N_{SF} subframes, the accumulated charge for each pixel is read out to constitute the output data stream. Ideally, the readout of one frame should take place while accumulation of the next frame is occurring.

In this report, the multiplexer approach, as outlined above, is examined, both in terms of expected overall performance and requirements for the individual building blocks. In Section 3.3, an analysis of the signal-to-noise obtainable with the multiplexer approach is given. Guided by the results of this analysis, the building blocks are analyzed, design guidelines

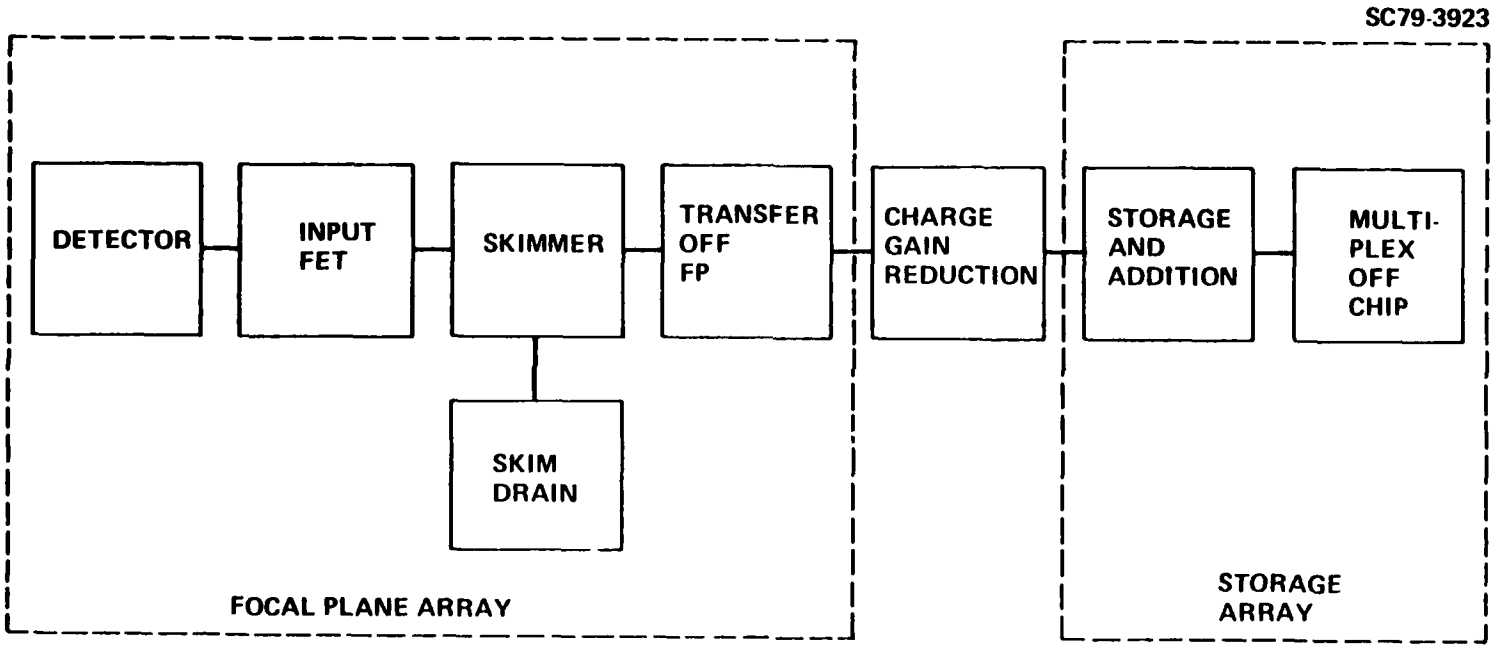

Fig. 2.8 Focal plane multiplexer module block diagram.

developed, and designs/layouts for inclusion on the test chip are presented. This section will also cover the overall test chip layout, the detector-CCD input circuits (focal plane array), gain reducer circuits and accumulate-and-storage arrays.

3.0 RESULTS

3.1 Detector Development

The most important results during this period center around the fabrication of very high R_0A $InAs_{0.9}Sb_{0.1}$ detectors. The behavior of the electrical properties of these detectors has shed considerable light on both the material properties of InAsSb and the proper analysis of the diffusion limited diode structure. In Fig. 3.1 are shown the current-voltage (I-V) characteristics of two diodes from layer 3-1020, one with nominally $(50\ \mu m)^2$ active area and the other with nominally $(100\ \mu m)^2$ active area. The leakage current at -100 mv reverse bias for the larger diode is 40 nA which translates to an "effective" R_0A value of 42 Ω-cm^2 by the simple formula:

$$R_0A = \frac{kT}{qI_L} A = \frac{1.68 \times 10^{-6}}{I_L(\text{Amps})} \ \Omega\text{-cm}^2$$

The smaller diode has essentially the same R_0A indicating that the leakage current varies with area as expected in the absence of dominant perimeter leakage mechanisms. The distribution of leakage currents at 100 mv reverse bias is shown for 26 contiguous 100 μm center detectors fabricated in a different InAsSb layer (3-1012) is shown in Fig. 3.2 The mean effective R_0A for these detectors is 27 $\pm$ 3 Ω-cm^2 showing that good uniformity as well as high R_0A product can be obtained.

We note here that we have defined an "effective" R_0A computationally from the leakage current in reverse bias. The R_0A measured at zero bias on any given diode will be higher by as much as 40%. For example, the zero bias R_0A measured on the diode in Fig. 3.1 is 59 Ω-cm^2. It is possible that this discrepancy is caused partially by perimeter leakage and partially by the finite series resistance of the very small probe contact on the diode surface. However, since the estimated R_0A is obtained from the region of the I-V curve in which the device actually will be operated and since it is a conservative figure, we use this as our evaluation standard. Even with this number we are within a factor of 2 of the program goal of R_0A = 85 Ω-cm^2.

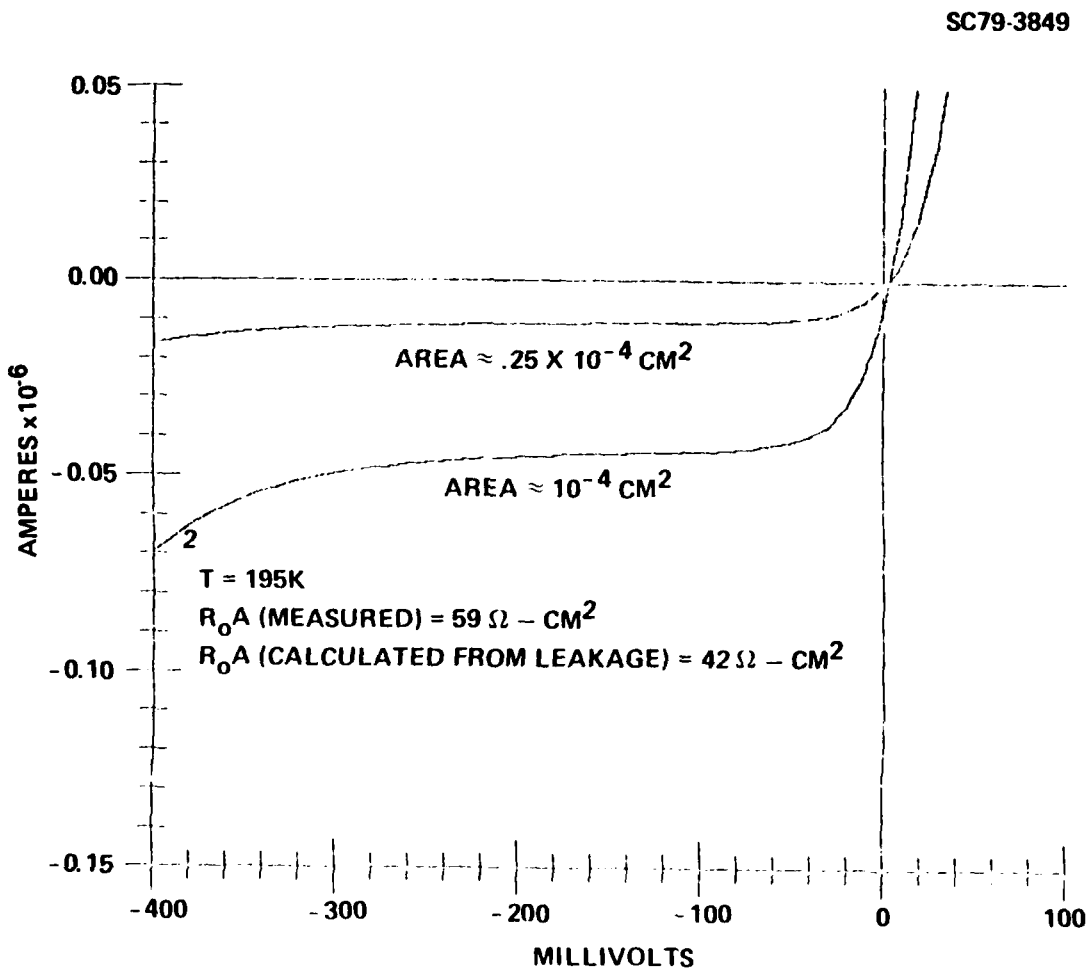

Fig. 3.1 Low leakage diode I-V characteristics.

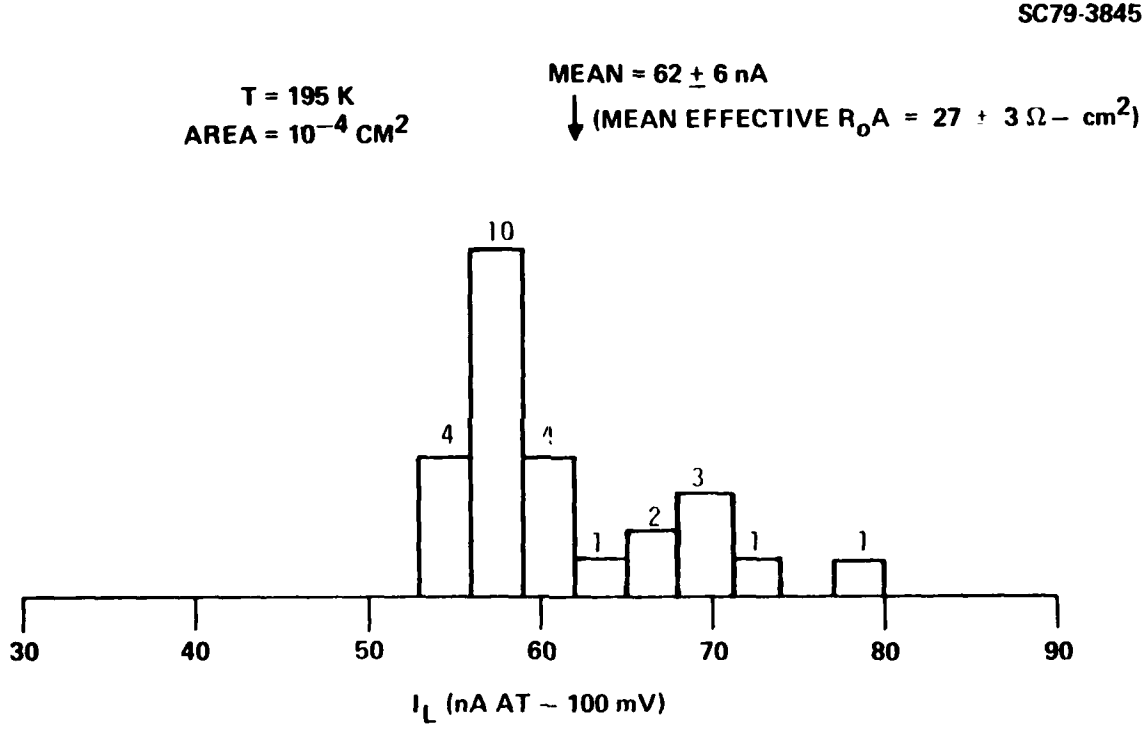

Fig. 3.2 Leakage current of 26 contiguous detectors.

These planar diodes were fabricated by Be^+ ion implantation in an $InAs_{0.9}Sb_{0.1}$ epitaxial layer ~13 μm thick grown by liquid phase epitaxy on a GaSb substrate. The implant dose was 5×10^{15} ions/cm^2 at 100 keV with the substrate held at room temperature. The implant mask used was 1000Å of SiO_2:N deposited at ~200°C by pyrolytic decomposition of SiH_4 and O_2 in the presence of NH_3. Over this was deposited a thin layer (~200Å) of Ti for adherence followed by a 4000Å layer of Au which served to block the incident ions. The Au and Ti were removed in the implanted region, but the SiO_2 was left to protect the semiconductor surface from contamination. After implant, the Au and Ti were removed using Technistrip gold etch and an HF-H_2O solution, respectively. The SiO_2 was left in place as an annealing cap for the Be atoms. The sample was annealed at 550°C for 1 hr. under flowing N_2. After annealing the SiO_2 was stripped in HF and the samples were etched a few minutes in a mixture of lactic, nitric, and hydrofluoric acids until probe measurements of 195 K gave the I-V characteristics like those shown above. This etching was for a longer period than that usually carried out for 77 K diodes and appeared to be necessary to obtain the low leakage currents shown.

During the course of the etching experiments on layer 3-1020 it was discovered that the surface etch did not produce effects that were linear with time. The layer was split in two parts (A and B) and both pieces etched for approximately the same length of time. Piece A showed a relatively low leakage current, 9×10^{-4} A/cm^2 (corresponding to an effective R_0A of 19 Ω-cm^2). This piece was set aside for field plate experiments. Piece B which showed a leakage current of 22×10^{-4} A/cm^2 (after sitting in air overnight) was etched further. No decrease in leakage was observed until 2 minutes and 15 seconds more etching had occurred. At this point, subsequent 30 sec-1 minute etches began to decrease the leakage to 3.8×10^{-4} A/cm^2 (effective R_0A = 44 Ω-cm^2). A further 30 second etch increased the leakage by 2 times but a longer etch (1 min) restored the low leakage value. The etching history of 3-1020 B is shown in Fig. 3.3. Three conclusions can be drawn from this unusual etching behavior: (1) the source of leakage current above the minimum observed is due to surface generation over the entire p-region surface; (2) a long surface etch passivates this surface thereby reducing generation by almost an order of magnitude; and (3) the etch, when applied repeatedly in short increments

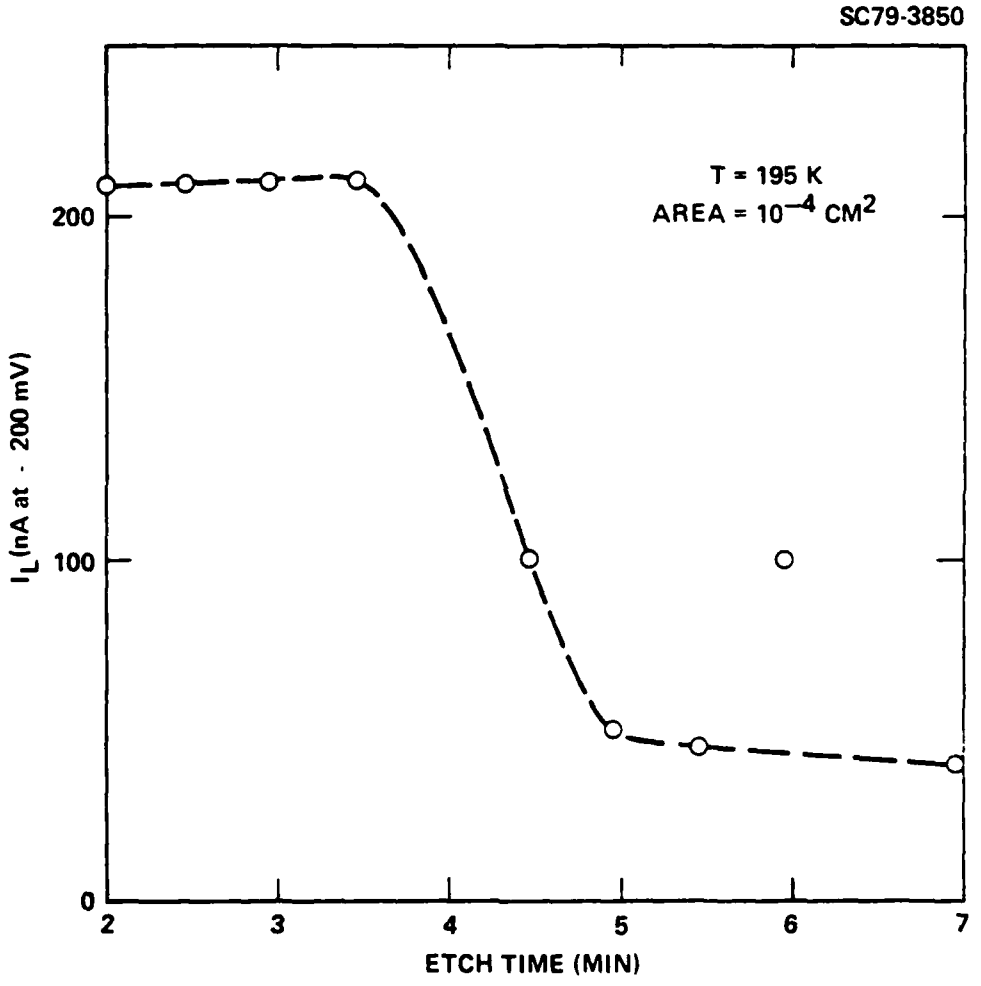

Fig. 3.3 Effects of surface etch on leakage current.

separated by probe tests, does not have the same effect as a long etch without interruption. In fact, if the etch is in some way improper, the surface generation may increase, as is shown by the increase at 6 minutes in Fig. 3.3. This last observation suggests the formation of a native oxide during the measurement cycle which partially inhibits the etching.

This sensitivity to surface etch suggests that these diodes prior to the etch are operating in the narrow base limit discussed above. The observed leakage currents correspond well to those estimated for a narrow base p-region. The decrease in leakage with increasing surface etch is attributable to the removal of implant damage and the establishment of a passive surface which moves the p-side of the sample toward a limited diffusion volume configuration. The levelling off of the leakage current at some minimum value results from the dominance of leakage from the substrate or from incomplete passivation of the p-surface. From the magnitude of the leakage current, the substrate also operates in the narrow base limit.

Having observed very low leakage diodes, the next step is to apply a protective coating. The first attempt has been to use the field plated/SiO_2:N structure developed for 77 K InAsSb. The results for layer 3-1020, shown in Fig. 3.4, indicate that the coated surface is a significant source of leakage current. The effective R_0A has decreased from 42 Ω-cm^2 to 4.4 Ω-cm^2, essentially returning the device to the narrow base diode configuration. The right hand panel of Fig. 3.4 shows the I-V characteristic of the diode after stripping the SiO_2 and field plates by ultrasonic cleaning in HF. Without any further etching the I-V characteristic has improved to equal the best value obtained on the layer. This indicates that although the SiO_2 coating caused high leakage, it did no permanent damage to the diodes. There is some reason to suspect that the particular deposition of SiO_2 made in this run was of poorer quality than that normally used in passivating InAsSb. For this deposition the optimal field plate bias was almost -70 V instead of the more typical -20 V. Moreover, this sample was given a 10 sec lactic, nitric, hydrofluoric etch just prior to deposition. From the evidence reported above (obtained after the deposition was made), an improper etch may degrade diode performance considerably. It is therefore possible that a proper SiO_2 deposition may still act as a good passivating coating.

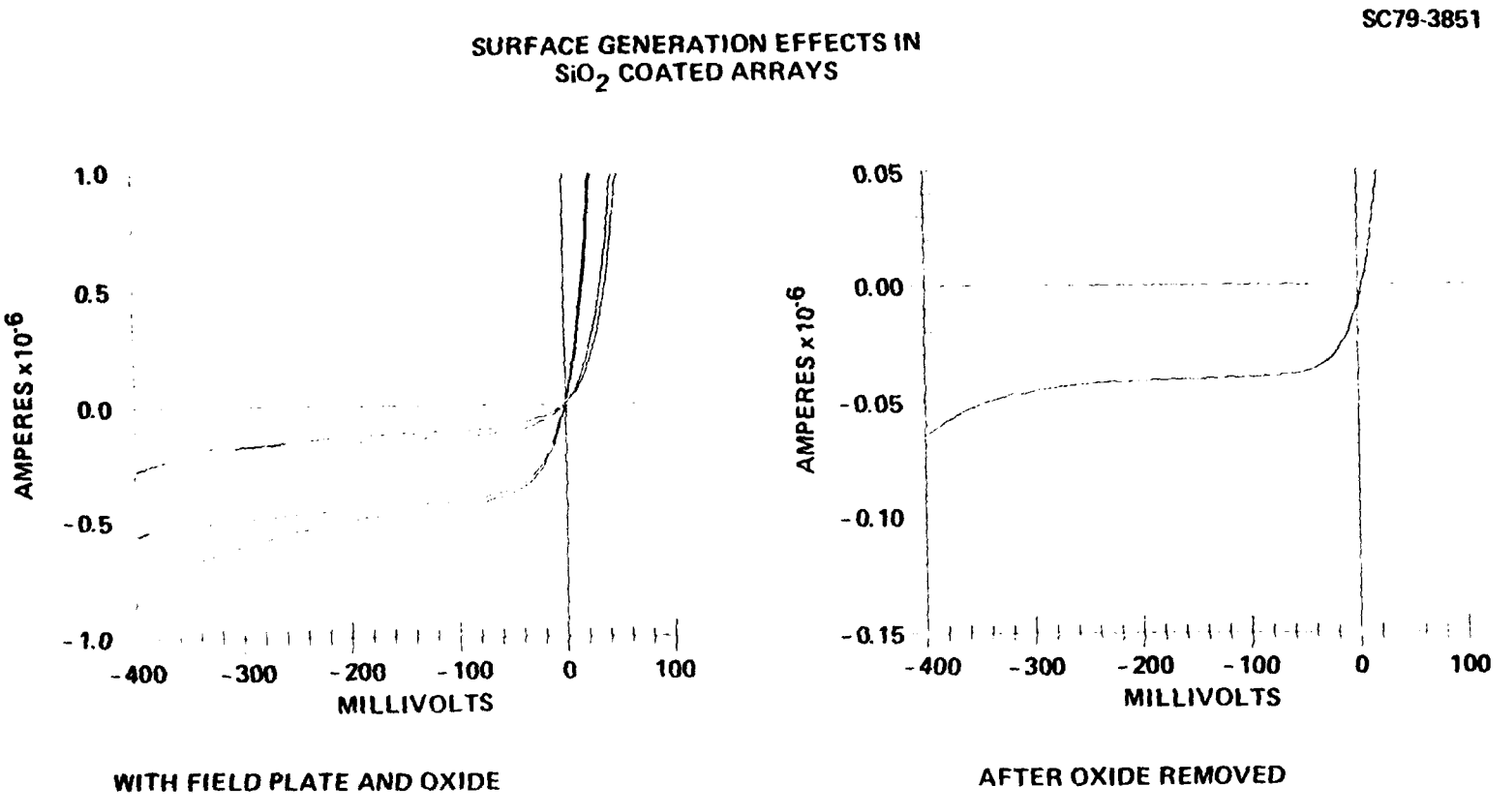

Fig. 3.4 Surface generation effects in SiO_2 coated arrays.

In order to establish a baseline for material quality, a study of the effect of dislocation density on leakage current was undertaken. Two different layers were studied: 3-1012 with an etch pit density of 2.4×10^4 cm^{-2} and 3-1013 with an etch pit density of 2.7×10^5 cm^{-2}. The dislocations of 26 diodes on 3-1012 and of 19 diodes on 3-1013 were counted and the reverse bias leakage current of each diode was measured after an optimal surface etch had been applied. The results are shown in Fig. 3.5. Clearly, the higher dislocation layer (3-1013) shows both higher leakage and a dependence of leakage upon dislocation count. The low dislocation layer (3-1012) shows no leakage dependence on dislocation density. One may therefore conclude that a layer with a dislocation density greater than a few $\times 10^4$ will not produce suitable diodes. It should be further noted that after etching the surface morphology of layer 3-1013 layer was generally poorer than that of layer 3-1012 and that the diodes on layer 3-1013 appeared to have a larger perimeter leakage component. One may also observe that the existence of a low leakage diode in layer 3-1012 with 16 dislocations suggests that the dislocations themselves do not necessarily cause higher leakage until one reaches a higher count (30-40/diode). However, the layer property which gives rise to dislocations also appears to give rise to higher leakage currents.

A preliminary study of the effects of melt baking prior to growth was conducted with the results being summarized in Table 3.1. No correlation was found between baking conditions and minimum leakage current. There is evidence from the table, however, that layers with rough surface morphology yield leakier diodes, and layers with higher substrate doping have less diode leakage.

Table 3.1

Melt Bake Study Summary

Layer	T(°C)	t(hr)	Dislocation Density(cm^{-2})	Breakdown Voltage	I(nA at -100 mV)	Surface Morphology
3-1016	620	24	2×10^4	1-2 V	102	Poor
3-1018	720	24	3×10^4	1-2 V	57	Good
3-1019	545	24	3×10^4	1-2 V	73	Good
3-1020	630	6	1×10^4	.5 V	38	Good

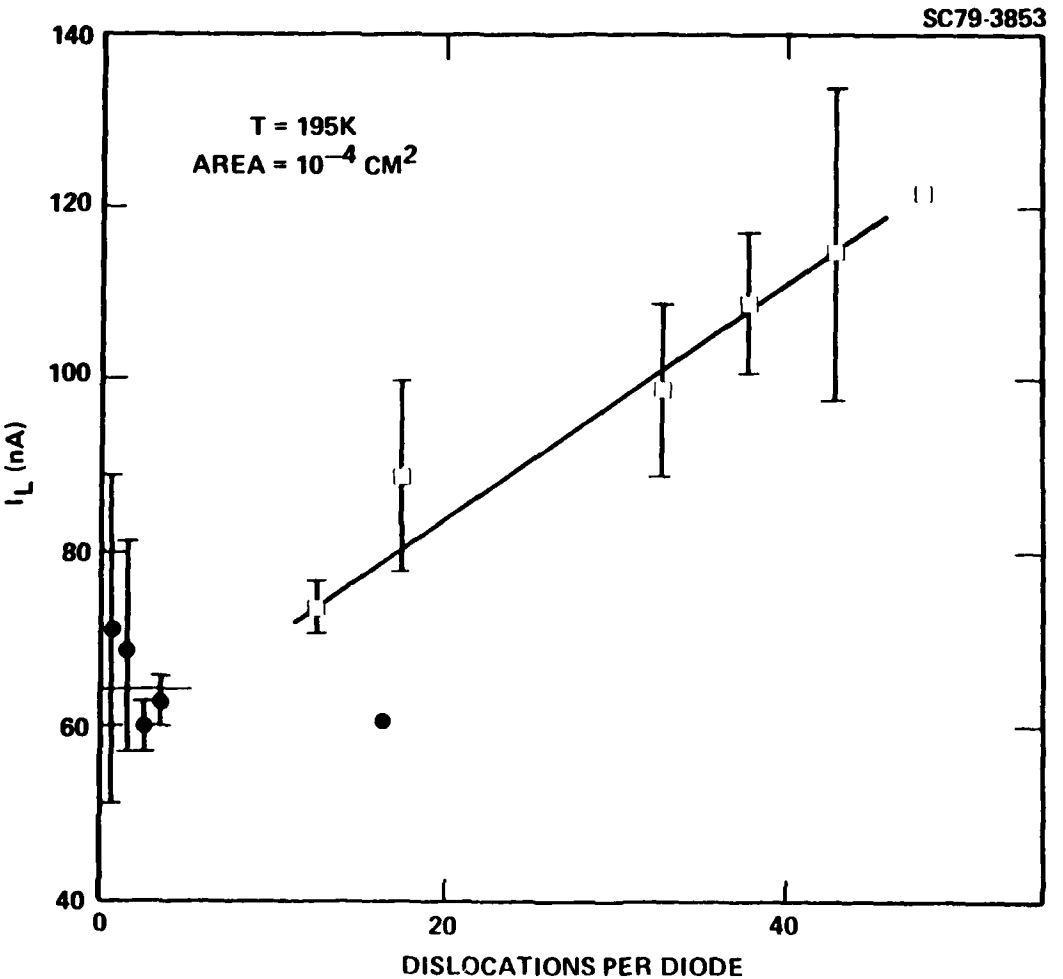

Fig. 3.5 Leakage current dependence on dislocation count.

The effectiveness of the Au metal masking in defining small geometry devices has been partially demonstrated by the variation of leakage current with nominal active area in Fig. 3.1. Problems have been found in focusing the mask aligner with sufficient accuracy to define 25 μm devices over large areas. This difficulty has been attributed to variations in layer thickness over large distances. Preliminary investigations of polishing layers after growth indicate that any diode degradation induced by polishing is removed by the surface etch. If further investigations bear this out, the focusing problems should be resolved.

3.2 Hybrid Integration

Successful fabrication of stripline structures for measuring 25, 50, 75, and 100 μm diodes in 5 x 5 hybrid array configurations has been accomplished with the use of a 4X projection mask aligner. Figure 3.6 shows the central array areas of these chips. Because of the differences between interconnect diameters required for the larger (75 and 100 μm) and smaller (25 and 50 μm) geometries, there are two separate test structures for the different size ranges. The stripline test chips are fabricated on a ~12 mil thick IR transparent Si wafer (resistivity >1 Ω-cm) which is covered on both sides with ~1700Å of SiO_2 for insulation and antireflection coating. On this are deposited metal striplines, the top layer being Au for bonding and the bottom Ti for adherence to the SiO_2. The smallest lines in the pattern are 5 μm wide. The Ti also forms a shorting plane to permit column growth on the striplines.

The standard column growth procedure has required some modification to obtain satisfactory column growth on the smallest geometries. In the standard procedure, a single 3 μm thick layer of photoresist is deposited over the test structure and holes are opened photolithographically to the striplines. The In columns are grown by electroplating and conform to the photoresist contour until they reach the top of the holes, at which point they begin to mushroom out. The lateral growth of columns above the photoresist appears to be enhanced by higher fields at the column edges. Figure 3.7 shows this effect clearly in columns grown on a 25 μm center test chip array through a 3 μm layer of photoresist. Although the columns have a total height of only ~3 μm above the photoresist they have grown laterally more than this in several

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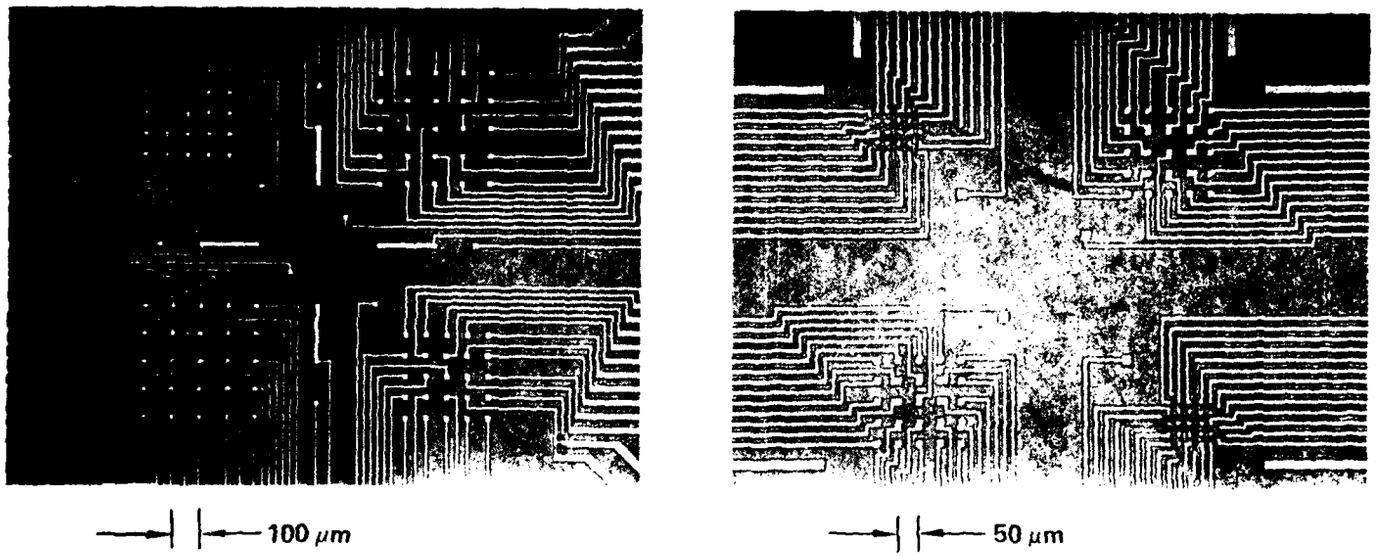

5 x 5 ARRAYS ON 75 AND 100 μm CENTERS

5 x 5 ARRAYS ON 25 AND 50 μm CENTERS

Fig. 3.6 TE STARE test chip.

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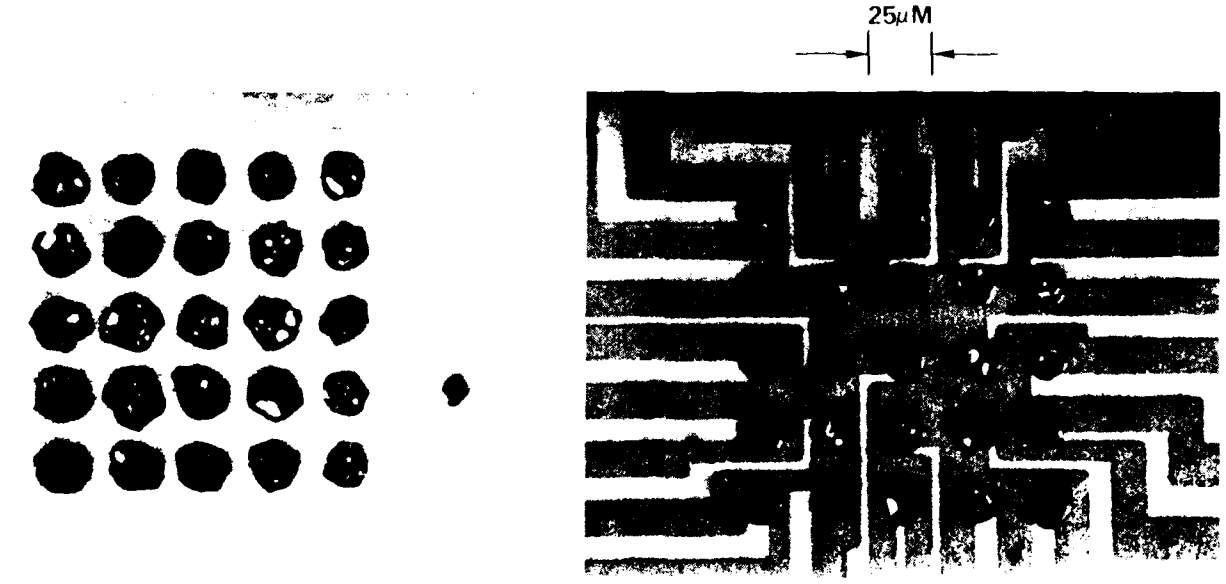

STANDARD METHOD
(1 LAYER PHOTO RESIST)

IMPROVED METHOD
(2 LAYERS PHOTO RESIST)

Fig. 3.7 Indium column growth on high density arrays.

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Science Center

places. A second layer of photoresist relieves this problem as is seen on the right hand panel of Fig. 3.7. The columns in this panel have been grown through a double layer of photoresist and thus have remained confined up to the necessary 6 μm height.

3.3 Multiplexer Results

3.3.1 Analysis of Signal-to-Noise Ratio of Thermoelectrically Cooled Staring Focal Plane Module

An analysis has been carried out to evaluate the signal-to-noise ratio which can be obtained with the focal plane concept described in the Approach Section (2.3). The intent of this analysis is to identify which portions of the focal plane contribute most significantly to the noise, to choose the optimum number of subframes, and to indicate design requirements for optimum performance. Accordingly, a worst case pixel (the one that would experience the most added noise due to the signal processing) has been traced through the focal plane; and the final signal-to-noise ratio has been compared to the ideal detector background plus leakage current limited signal-to-noise ratio for various numbers of subframes and values of other relevant focal plane parameters. The focal plane layout and other parameters postulated for this analysis are:

(1) 64 x 64 picture element focal plane array with 2 mil center-to-center dimensions;

(2) A direct injection with background skimming input circuit is used, with 0.80 skim ratio (= background charge removed ÷ mean background);

(3) Detector leakage plus background current = 8×10^{-9} amp;

(4) 16 msec total frame time;

(5) 1000Å oxide thickness (oxide capacitance = 3.45×10^{-8} f/cm^2), 15 V storage potential, and ~20% of the unit cell of the focal plane array available for charge storage;

(6) ± 10% variations in the total of detector leakage plus photocurrent, ± 5% skimming variations, and a 5°K ΔT variation to be accommodated.

Initially, in the analysis, the effects of 1/f noise from the detector and MOSFET input circuit are not included. This is done to simplify the analysis, for noise from subframe-to-subframe does not add in a RMS fashion if 1/f noise is included. That is, the correlation of low frequency noise from subframe-to-subframe must be taken into account prior to the inclusion of 1/f noise. Analysis is therefore initially performed neglecting 1/f noise; it will be included in an ad hoc manner at the end in Section 3.3.1.5.

With the above assumptions and qualifications, the various noise sources and operational parameters are now considered.

3.3.1.1 Focal Plane Array Section

Determination of Background Skim Ratio and Subframe Integration Time

Before proceeding with identification of important noise sources, the amount of leakage plus background charge which can be skimmed off, and the subframe integration time are determined. The base line detector-to-CCD interfacing circuit to be used is a direct injection with background skimming circuit. A schematic drawing of this input circuit is shown in Fig. 3.8. Charge from the photodiode flows through a p^+ diffusion on the multiplexer chip, under the input gate, to a receiving well. For background skimming, the receiving well consists of two separate wells: the storage and signal gates separated by a barrier, or meter gate. The storage gate first fills to a level dictated by the surface potential under the barrier; this constitutes the charge to be skimmed or removed (bottom of Fig. 3.8). Additional charge flows over the barrier into the signal well (which is actually also the CCD transport register). The amount which can be skimmed without removing signal charge is determined with the aid of Fig. 3.9). Let X be the mean background and leakage charge. From the assumption of ± 10% detector current variations and ± 5% skimmer variations, the worst case corresponds to a detector generating only 0.9X associated with a skimmer removing 5% more than average, or a total charge which can be removed without skimming signal charges of 0.85X (middle drawing of Fig. 3.9. It is therefore assumed that 0.8X can be removed for an extra margin of safety. Thus, the maximum skim fraction η_{SK}, defined as the ratio of the mean background removed to the mean background, is taken to be $\eta_{SK} = 0.8$.

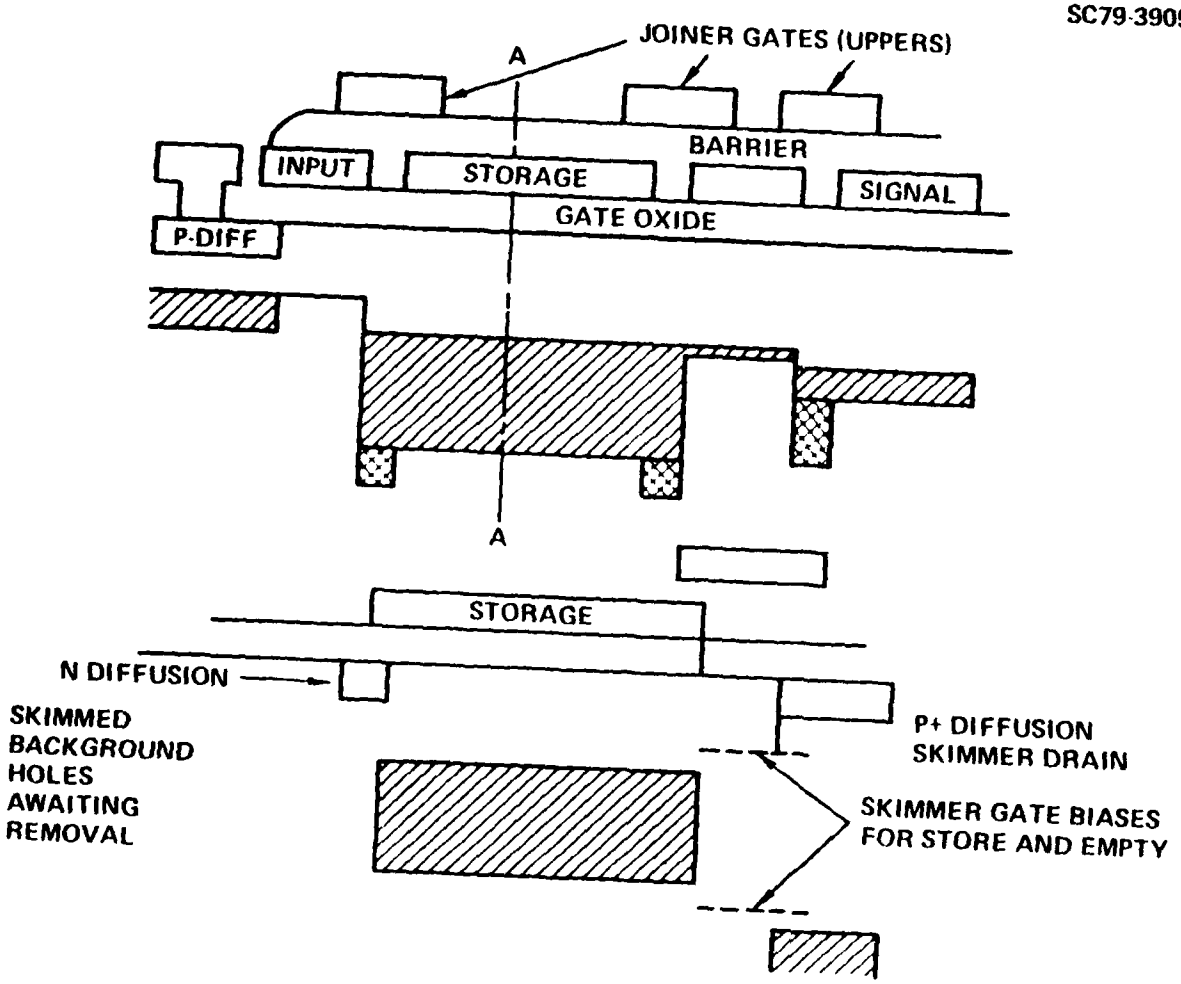

Fig. 3.8 Input circuit with skimmer for staring array.

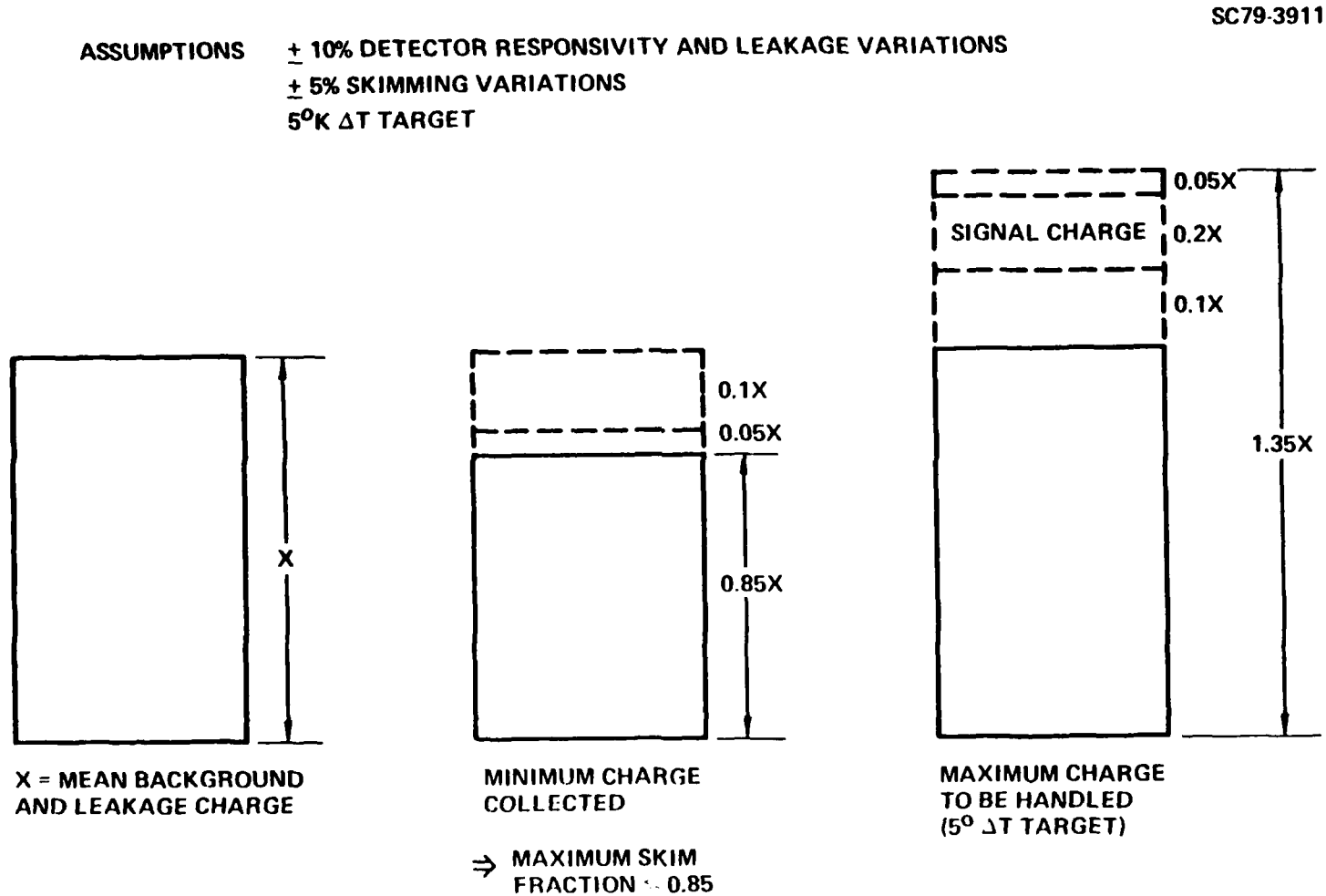

Fig. 3.9 Determination of maximum skimming fraction.

On the other hand, the maximum charge to be accommodated arises from a detector generating 1.1X with a skimmer removing 5% less than average (right drawing of Fig. 3.9. Also, a 5° ΔT at 4% contrast ratio per degree adds 0.2X, for a worst case of 1.35X. The amount of charge to be accommodated in the CCD transport register is therefore 1.35X - 0.8X = .55X.

The latter amount of charge to be handled in conjunction with the charge capacity in the CCD register dictated by the parameters of assumption (5) above determines the subframe integration time. The storage capacity is:

$$N_h = \frac{C_{ox} V A}{q} , \qquad (1)$$

where C_{ox} = oxide capacitnce
V = storage voltage
A = storage area.

With the parameters of assumption (5) above:

$$N_h = 1.68 \times 10^7 \text{ holes.} \qquad (2)$$

This must be greater than or equal to:

$$N_h = .55 \times t_i \times \frac{8 \times 10^{-9} \text{amps}}{1.6 \times 10^{-19} \text{ coul}} = 2.75 \times 10^{10} t_i , \qquad (3)$$

where t_i = integration time.

Equating Eqs. (2) and (3), $t_i \leq 610$ μsec. This implies a maximum number of subframes (with no dead time to read out the individual subframes) of

$$N_{SF}^{max} = \frac{16 \times 10^{-3}}{610 \times 10^{-6}} = 26 \text{ subframes.}$$

Actually, this maximum number cannot be realized because of the time required to read out the subframes from the focal plane array.

Detector Background and Leakage Shot Noise

The detector current gives shot noise equal to the square root of the total number of charges collected. Let N_B = total number of holes generated by detector current, I_B:

$$N_B = \frac{I_B t_i}{q}, \qquad (4)$$

where t_i = integration time and q = electron charge.

For $I_B = 8 \times 10^{-9}$A on the average, t_i = 610 μsec,

$$N_B = 3.05 \times 10^{17} \text{ holes/subframe}$$

Therefore, the shot noise = $\sigma_{shot} = \sqrt{N_B}$ = 5523 holes rms.

Input MOSFET Noise

The MOSFET channel noise current entering the first CCD well is given by:*

$$I_{MOS} = \frac{\frac{8}{3} kTg_m}{1+g_m R_D} \left[\frac{(1+j\omega C_D R_D)}{1 + \frac{j\omega C_D R_D}{1+g_m R_D}} \right]^{1/2} \text{ per HZ} \qquad (5)$$

where g_m = transconductance
C_D = detector + MOSFET input capacitnce
R_D = diode resistance
kT = Boltzmann's constant times temperature.

* R. Balcerak, P. W. Van Atta, J. T. Hall, and W. Grant, "Signal Processing Interface for 3-5 μm Intermediate Temperature Photovoltaic Detectors", in Proc. IRIS, Detector Specialty Meeting, San Diego, CA, 1976.

The noise begins to increase at f = 1/2 $R_D C_D$, which for $R_D = 7 \times 10^7$ Ω is 2.2 KHz and 22 KHz for C_D = 1 or 0.1 pf, respectively, the range expected for C_D. Since the subframe integration time is 610 μsec which implies an input bandwidth of ≈ 1.6 KHz, the noise spectrum is assumed constant over the band of interest and equal to:

$$I_{MOS} = \frac{8/3\ kTg_m}{1+g_m R_D}^{1/2} \tag{6}$$

Then

$$I_{MOS}^{Total^2} = \int_0^{1/(2\ t_{int})} I_{MOS}^2 \tag{7}$$

and

$$\sigma_{MOS} = \frac{I_{MOS}^{Total} \cdot t_{int}}{q} R = \frac{(8/3\ kTg_m)^{1/2}}{1+g_m R_D} \frac{\sqrt{t_{int}}}{q\sqrt{2}} \tag{8}$$

For $I = 8 \times 10^{-9}$A, $g_m = q/kT$ $I = 4.7 \times 10^{-7}$, and $g_m R_D = 32.9$, Eq. (5) yields:

$$\sigma_{MOS} = 187 \text{ holes rms.}$$

Background Skim Noise

The noise in the background skim process is modeled as KTC noise on the background storage gate and barrier gate has an area of ~10% of the array unit cell size, or a capacity of ~8 x 10^6 holes. Therefore, to accommodate 0.8X = 2.5×10^7 charges to be skimmed per subframe, four skims are required. KTC noise per skim is

$$\sigma'_{KTC} = \sqrt{2}\ \sqrt{KTC} = \sqrt{2}\ 342\ (C_{pf})^{1/2} \tag{9}$$

where the factor of $\sqrt{2}$ takes into account variation on both storage and barrier gates. For C = 0.9 pf (10% of cell area),

$$\sigma'_{KTC} = 145 \text{ holes rms} \quad (10)$$

and for four skims,

$$\sigma_{KTC} = 4\sqrt{145} = 290 \text{ holes rms.} \quad (11)$$

CCD Fast Surface State Noise

After charge integration and background skimming in the input circuit, the charge packets are introduced into a CCD register for transport to the gain reducer circuit. The CCD adds noise, the first source being fast surface state noise, given by (surface channel device assumed):

$$\sigma_{fss} = [0.7 \text{ KT } N_{ss} N_c A_c]^{1/2} \quad (12)$$

where N_{ss} = density of surface states
N_c = number of CCD cells
A_c = area of CCD cells.

For $N_{ss} = 10^{10}/cm^2\text{-eV}$, $N_c = 64$ (worst case element), $A_c = 1.04 \times 10^{-5}$ cm^2, this is:

$$\sigma_{fss} = 349 \text{ holes rms.} \quad (13)$$

Transfer Loss Noise

This noise source is given by

$$\sigma_{TL} = [2\varepsilon_c N_c \cdot N_h]^{1/2} \quad (14)$$

where ε_c = transfer inefficiency per cell
N_h = number of holes per charge packet.

Again, the worst case element has $N_c = 64$. For $N_h = (1-\eta_{SK})N_B = 6.1 \times 10^6$ (on the average) holes and $\varepsilon_c = 0.0005$,

$$\sigma_{TL} = 625 \text{ holes rms.}$$

Reset Noise

Assuming a fill-and-spill type gain reducer (Section 3.3.4), the charge is first detected with a reset floating diffusion output stage. The reset noise introduced is:

$$\sigma_{reset} = 342(C_{pf})^{1/2} \qquad (15)$$

where C_{pf} = detection node capacitance in pf. The node capacitance is determined by the maximum charge (Eq. 2) and the maximum voltage swing allowed. For a 5 V swing, $C_{pf} = .54$ pf and

$$\sigma_{reset} = 251 \text{ holes rms.}$$

Total Noise of Focal Plane Array

At this point, the noise up to the gain reducer is summarized.

σ_{shot} = Detector shot noise = 5523 holes rms.
σ_{MOS} = Input FET noise = 187 holes rms.
σ_{skim} = Skim noise = 290 holes rms.
$\sigma_{f_{ss}}$ = Fast interface state noise = 349 holes rms.
σ_{tL} = Transfer loss noise = 625 holes rms.
σ_{reset} = Reset noise = 251 holes rms.
TOTAL RMS NOISE = σ_T = 5586 holes rms.
= 1.01 x detector leakage + background shot noise

Thus, the noise to this point is ≈ 1.01 x the detector generated noise (in the absence of 1/f noise). The focal plane section therefore does not degrade the noise.

3.3.1.2 Gain Reducer Noise Contribution

At the gain reducer, assumed to be a reset floating diffusion amplifier followed by a fill-and-spill circuit, the noise, as well as the signal, are reduced by a gain factor 1/G (charge-out = 1/G times charge-in). The gain-reducer circuit also adds some additional noise. Therefore, the noise per packet after gain reduction is:

$$\sigma_{gr}^2 = \frac{\sigma_T^2}{G^2} + \sigma_{fs}^2 \qquad (16)$$

where σ_{fs} = the noise of the fill-and-spill circuit. $\sigma_{fs} = \sqrt{KTC} = 342(C_{pf})^{1/2}$ where C_{pf} = capacitance of the charge storage gate in pf. For a 12 μm x 12 μm gate with 1000Å oxide (Section 3.3.4), $C_{pf} = 5 \times 10^{-14}$ farads and σ_{fs} = 76 holes rms.

Equation (16) indicates the need to have a low noise gain reduction circuit for if this noise is large, or if G is large, the total noise can become dominated by σ_{fs}.

3.3.1.3 Storage Array Noise Contribution

After gain reduction, the reduced pixels are transported to storage sites in the storage array corresponding to their original location in the focal plane array, the contributions from all N_{sf} subframes of a given frame are accumulated, and finally the accumulated charge packets are read out. Noise will be added during the transport and input cycle for each subframe charge packet and during readout of the accumulated packets. The worst case element corresponds to the top row of the focal plane array and the column farthest from the storage array multiplexer output. During the transport and input cycles this pixel is subject to the most transfers, hence the most fast surface state and transfer loss noise. Also, during storage array readout, this pixel experiences the most multiplexer transfers.

Transport and Input Cycle Noise

During input, the reduced pixel has added to it fast surface state and transfer loss noise. The fast surface state noise will be given by

Eq. (12) with $N_{ss} = 10^{10}$ states/cm^2-eV, $N_c = 64$, and A_c = area of the input register CCD cell. $A_c = L{:}W$, where L = 51 μm and W = register width. Assuming that W = 4 μm, sufficient to accommodate the attenuated charge packets:

$$\sigma^i_{f_{ss}} = 155 \text{ holes rms.} \tag{17}$$

Since transfer noise is proportional to the square root of the number of carriers, for the input CCD to the storage register, this noise is $1/\sqrt{G}$ times the transfer noise in the focal plane array (Eq. 14) or

$$\sigma^i_{TL} = 625/\sqrt{G}. \tag{18}$$

Output Cycle Noise

During output, an accumulated packet also experiences fast surface state and transfer noise, and in addition reset noise at the output amplifier.

The fast surface state noise is again given by Eq. (12), with $A_c = N_{SF}/G$ times the CCD cell area of the focal plane array. (The cells in the storage array must accommodate the charges from N_{SF} subframes, each reduced by 1/G.) Therefore

$$\sigma^o_{f_{ss}} = 349 \sqrt{\frac{N_{SF}}{G}}. \tag{19}$$

This is the noise added to a pixel during readout; to refer it to the equivalent noise on a single subframe, it should be divided by N_{SF}, or:

$$\sigma^o_{f_{ss}}/\text{subframe} = \frac{349}{\sqrt{G}} \tag{20}$$

In much the same way, transfer loss noise will be given by Eq. (14) with N_h replaced by $(N_{SF}/G)N_h$. Referred to each subframe, this becomes:

$$\sigma^o_{TL}/\text{subframe} = \frac{625}{\sqrt{G}}. \tag{21}$$

Reset noise at the output amplifier is given by Eq. (15) with C_{pf} 0.5. Dividing by $\sqrt{N_{SF}}$ to refer to each subframe:

$$\sigma^{o}_{reset}/\text{subframe} = 251/\sqrt{N_{sf}}. \tag{22}$$

3.3.1.4 Total Input Referred Noise

An expression for the total noise per pixel per subframe, including all of the sources discussed can now be given. This is done by adding in quadrature all of the contributing noise sources as follows:

$$\sigma_T/\text{subframe} = \left[\left(\frac{5586}{G}\right)^2 + (76)^2 + (155)^2 + \left(\frac{625}{\sqrt{G}}\right)^2 + \left(\frac{349}{\sqrt{G}}\right)^2 + \left(\frac{625}{\sqrt{G}}\right)^2 + \left(\frac{251}{\sqrt{N_{SF}}}\right)^2\right]^{1/2} \tag{23}$$

Detector + Focal Plane | Gain Reducer | Storage Array Input | Storage Array Output

The total noise per pixel per frame is $\sqrt{N_{SF}}$ times Eq. (23), since N_{SF} subframes are accumulated to constitute a frame:

$$\sigma_T/\text{frame} = \sqrt{N_{SF}} \cdot \sigma_T/\text{subframe}. \tag{24}$$

Finally, Eq. (24) is multiplied by G in order to refer the total noise to the detector input CCD cell so that the signal-to-noise performance of the system as a whole can be compared to signal-to-noise of the detector itself over the frame time:

$$\sigma_T/\text{frame} = \text{noise per frame referred to input} = G\sqrt{N_{SF}}\,\sigma_T/\text{subframe} \tag{25}$$

In order to make a comparison between the detector noise limited performance and actual performance, an ideal system is now postulated. In this ideal system, a given pixel integrates for the entire frame time and the only noise source is detector background plus leakage induced noise. The signal-to-noise of this system is identified as (S/N) ideal. The performance of such an ideal system cannot, of course, be attained, due to loss of integration time to provide time to readout charge from the focal plane array and noise added by the system. It is however, desired to design the system to approach the ideal as closely as possible.

Two factors will determine the signal to noise ratio of the real system -- the number of subframes used (related to duty cycle) and the total noise -- given by Eq. (25). (S/N) ideal is given by

$$(S/N)_{ideal} = \frac{\left(\frac{I_s t_f}{q}\right)}{2.828 \times 10^4} \qquad (26)$$

where I_s = signal current, t_f = frame time, and 2.828×10^4 is the shot noise from the 8 nA detector current over the entire frame time. For the real system, using 610 μsec subframes,

$$S/N = \frac{N_{SF} \frac{t_f}{26} \frac{I_s}{q}}{\sigma_T'} = \frac{N_{SF}}{26} \cdot \frac{\frac{I_s t_f}{q}}{(NF)\ 2.828 \times 10^4} = \frac{N_{SF}}{26\ (NF)} \left(\frac{S}{N}\right)_{ideal} \qquad (27)$$

where NF is the "noise factor" which relates actual noise to detector noise over the entire frame time; i.e.,

$$\sigma_T' = (NF)\ 2.828 \times 10^4 \qquad (28)$$

Now, $(S/N) \div (S/N)_{ideal}$ can be obtained using Eqs. (23), (25) and (28) for different assumed values of N_{SF}, G, and other system parameters.

Such calculations are shown in Fig. 3.10 where $(S/N) \div (S/N)_{ideal}$ is shown vs N_{SF}. The curve labeled n=1 results from the assumption $1/G=1/N_{SF}$, in addition to the assumptions made in the preceding sections. The assumption ($n=1$, where $n = \frac{N_{SF}}{G}$) follows from assuming pixel storage capacity in the storage array and focal plane array are equal ($= N_{max}$). Then, after N_{SF} accumulations of N_{max}/G charges per subframe, $N_{SF} \cdot N_{max}/G = N_{max}$ or $N_{SF}/G = 1$. On Fig. 3.10, 1.0 on the vertical axis corresponds to the ideal system. Also indicated as a dashed line is the performance of a system with reduced integration time, but detector leakage + background noise limited; in this case the S/N varies as $\sqrt{t_{int}}$ or $\sqrt{N_{SF}}/26$ (for 26 610 μsec subframes maximum per frame). The curves are extended to 26 subframes, even though this would be unrealistic, since some time must be allowed for the focal plane to

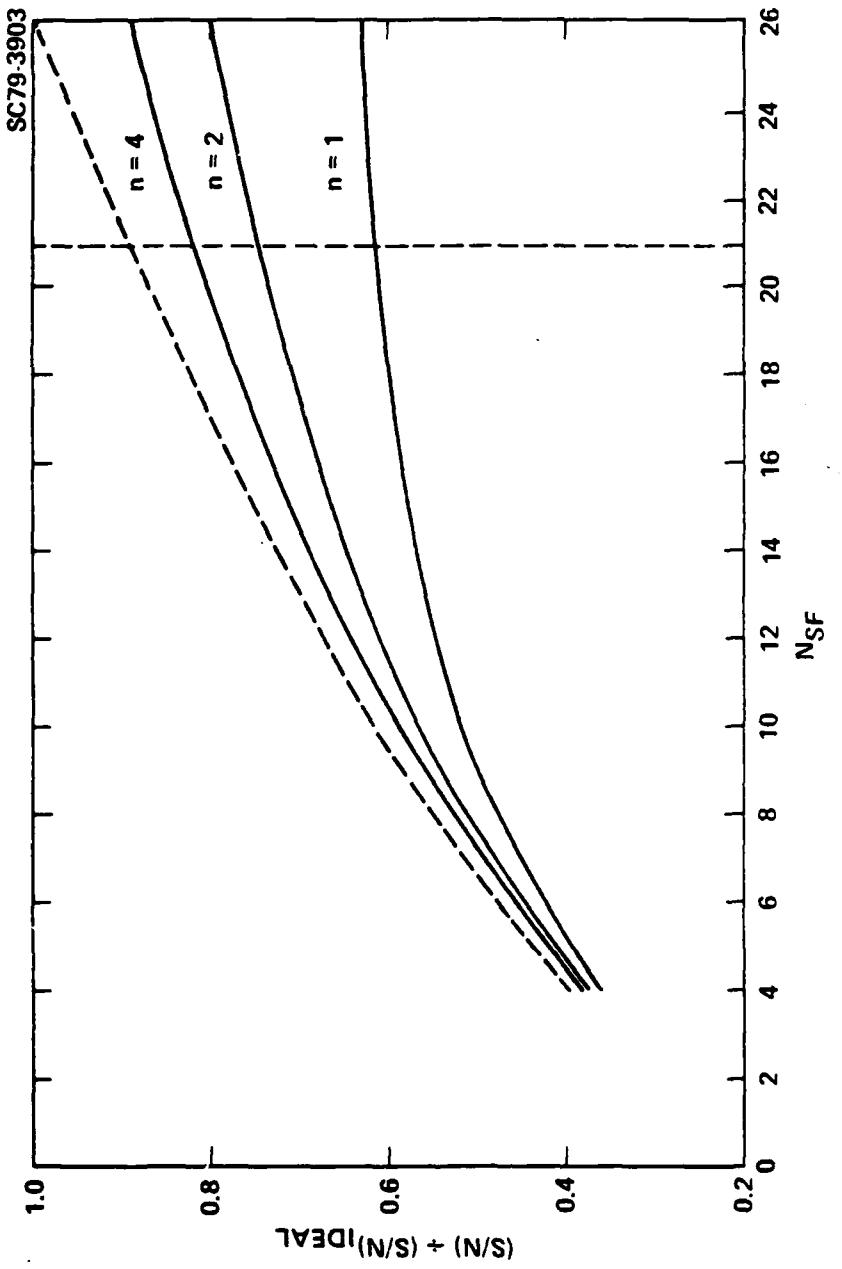

Fig. 3.10 System signal-to-noise ratio vs. N_{SF}.

be read out after each subframe. Assuming that readout can be done in 128 μsec (2 μsec per row) the maximum practical number of subframes would be:

$$\frac{16 \times 10^{-3} \text{ sec}}{(610 + 128) \times 10^{-6} \text{ sec}} = 21.$$

As indicated by curve n=1 of Fig. 3.10, the overall system does not attain ideal performance, even after adjustment for duty cycle reduction, because of the noise added by the signal processing components, particularly the accumulate-and-store array. At 21 subframes, the S/N is 0.62 of that for the ideal system. Actually, the performance increases very slowly with N_{SF} beyond ~16 subframes; it may therefore be advantageous to reduce the number of subframes and allow more time for subframe read out.

One approach to improving the system performance is to decrease the gain reduction factor, G, so that the storage array noise is not emphasized so much when total noise is referred back to the detector. This involves having a larger pixel storage area in the storage array than in the focal plane array; this may be practical in the design because in the storage array, area is not needed for the detector-to-CCD input circuit. The improvement possible is shown by curves 2 and 3 of Fig. 3.10. For these curves $1/G = 2/N_{SF}$ (n=2) and $1/G=4/N_{SF}$ (n=4). Significant improvement in performance results in these two cases, which might be realized by using fan-out, i.e, having larger cells in the accumulate-and-storage array than in the focal plane array. For curves n=2 and 3 of Fig. 3.10, .75 and .82 of ideal performance is realized at 21 subframes. The dependence on the number of subframes is somewhat stronger than for n=1.

Another method to improve overall performance is to reduce the noise introduced during input to the accumulate-and-store array (when the subframe charge packets and associated noise are small) by making the input register a buried channel device. Even though up to a factor of two specific capacity might be lost (compared to surface channel), the input channel width can be adjusted as necessary. Figure 3.11 shows the improvement obtained. It is assumed that the input channel has no surface state noise and the transfer loss noise is reduced by $\sqrt{10}$ (ε = .00005). Curves for $1/G = 1/N_{SF}$(n=1) and $1/G = 2/N_{SF}$ (n=2) are shown. 73% and 80% of ideal performance, respectively, are obtained.

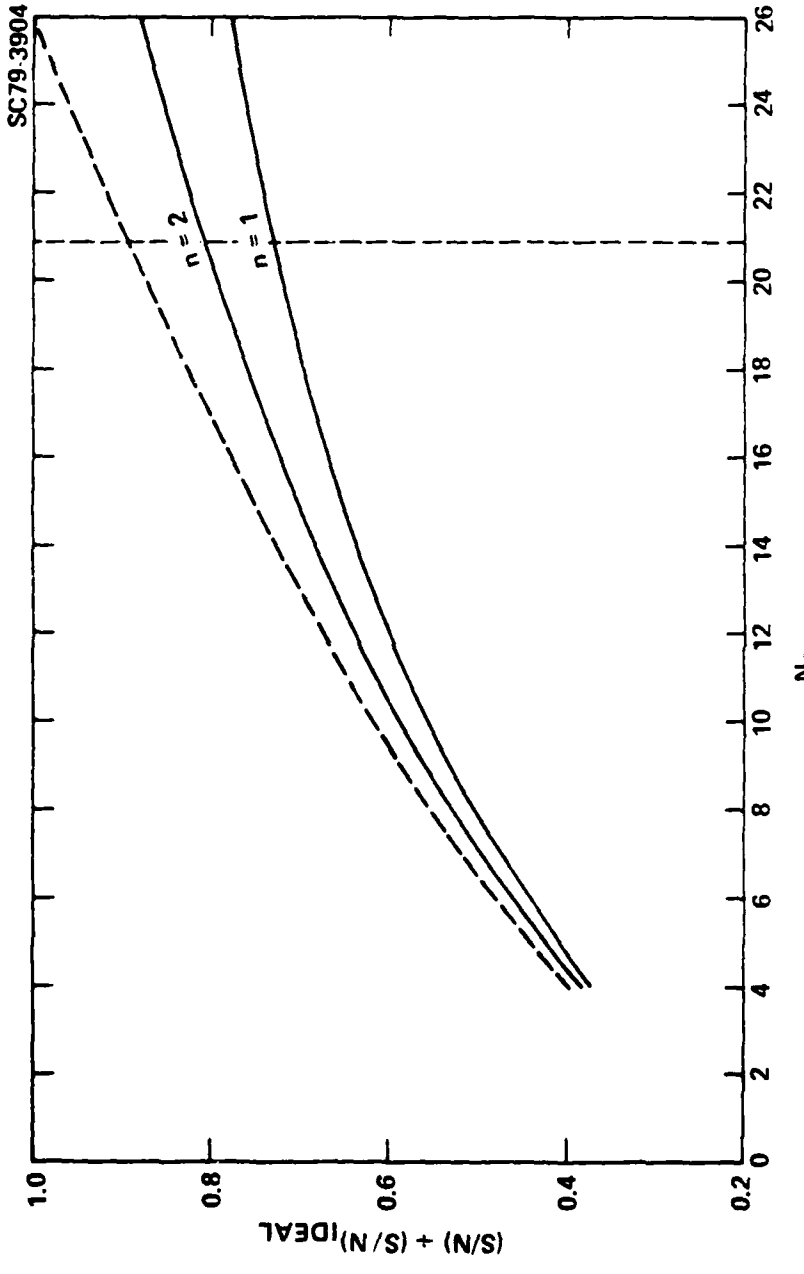

Fig. 3.11 System signal-to-noise ratio with buried channel input to accumulate-and-store array.

One of the assumptions of the analysis was that background charge skimming was utilized. The value of background skimming on overall system performance can now be indicated. If skimming is not used in the focal plane array the subframe integration time must be reduced so that the increased charge can be accommodated. Again, assuming a storage capacity of 1.68×10^7 and that, worst case, 1.3 times the mean detector and background charge must be accommodated, t_i = 258 μsec maximum. For 250 μsec subframes, the maximum number of subframes is 64 and the maximum practical number is 42. The shot noise on the detector current accumulated during 250 μsec is 3535 holes rms. All other noise sources remain approximately the same. Repeating the calculations, with a surface channel device and n=1, leads to the results shown in Fig. 3.12. Here the system performance is at best 30% of ideal, significantly worse than the system utilizing skimming. This results because with no skimming, the subframe integration time is not as long, hence the detector induced noise is reduced in comparison to fixed signal processor noise sources. Also, because of the increased charge to be handled, large gain reduction factors must be used, enhancing the effect of accumulate-and-store array noise when referred back to the input well.

Finally, the performance with a partitioner gain reducer is considered. The partitioner gain reducer (Section 3.3.4) is attractive because of layout simplicity, but it may possess full partition noise. If a charge packet, N, is partitioned into fractions 1/G and 1-1/G, a noise 1/G(1-1/G)N results. Substituting this expression for the fill-and-spill noise factor in Eq. (23) and repeating the calculations, all other parameters being the same, Fig. 3.13 results for n=1 and n=2. Comparison to Fig. 3.10 shows that the system with partition noise is inferior to the system with fill-and-spill gain reducer. However, it may be possible to operate a partitioner without partition noise. Accordingly, a partitioner gain reducer will be included on the test chip and evaluated.

3.3.1.5 1/f Noise Computation

1/f noise, predominantly from the input MOSFET, is present and can be significant in a staring system. To include the effects of 1/f noise in the foregoing analysis, note that Eq. (25) gives the detector shot noise plus

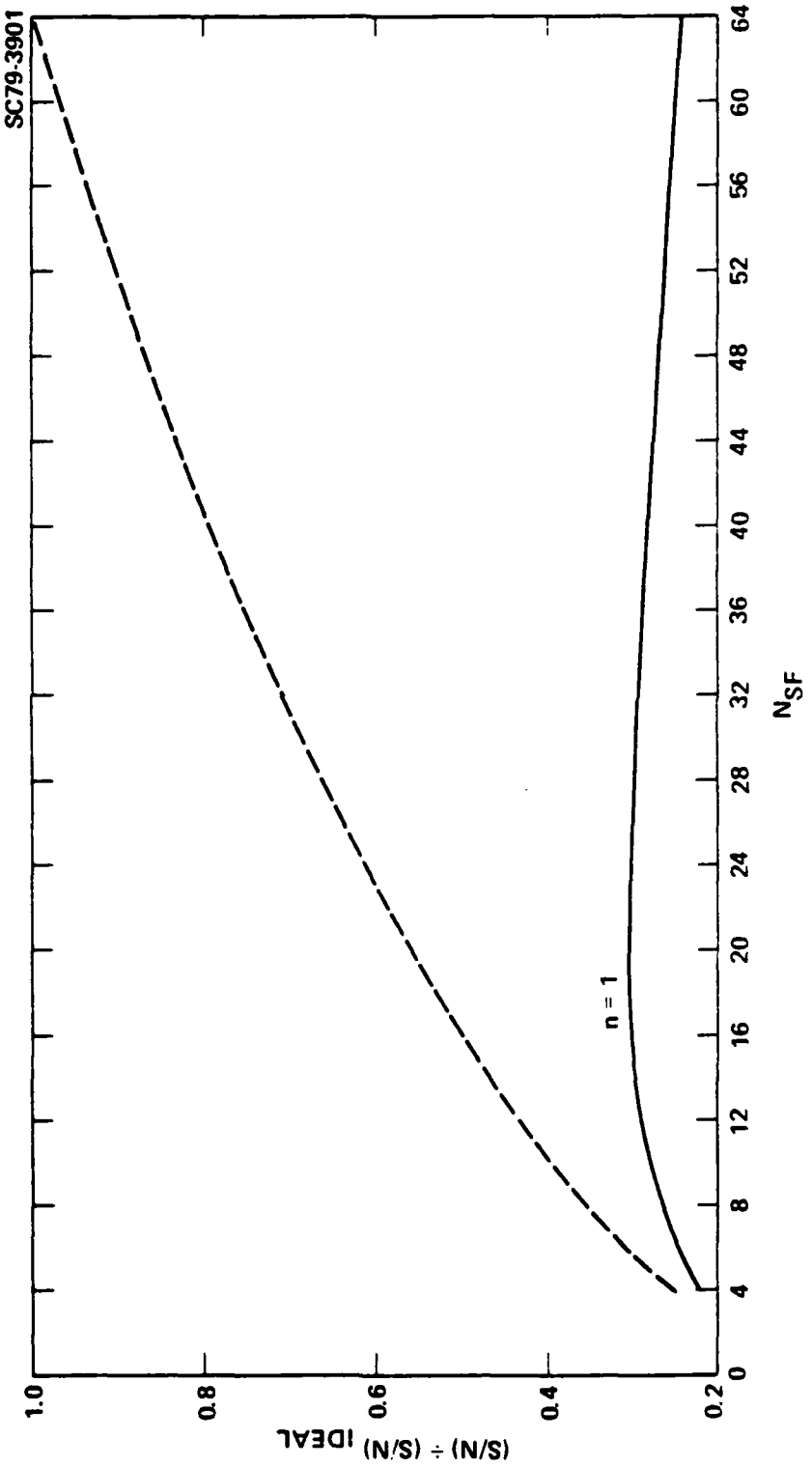

Fig. 3.12 System signal-to-noise ratio with no background skimming.

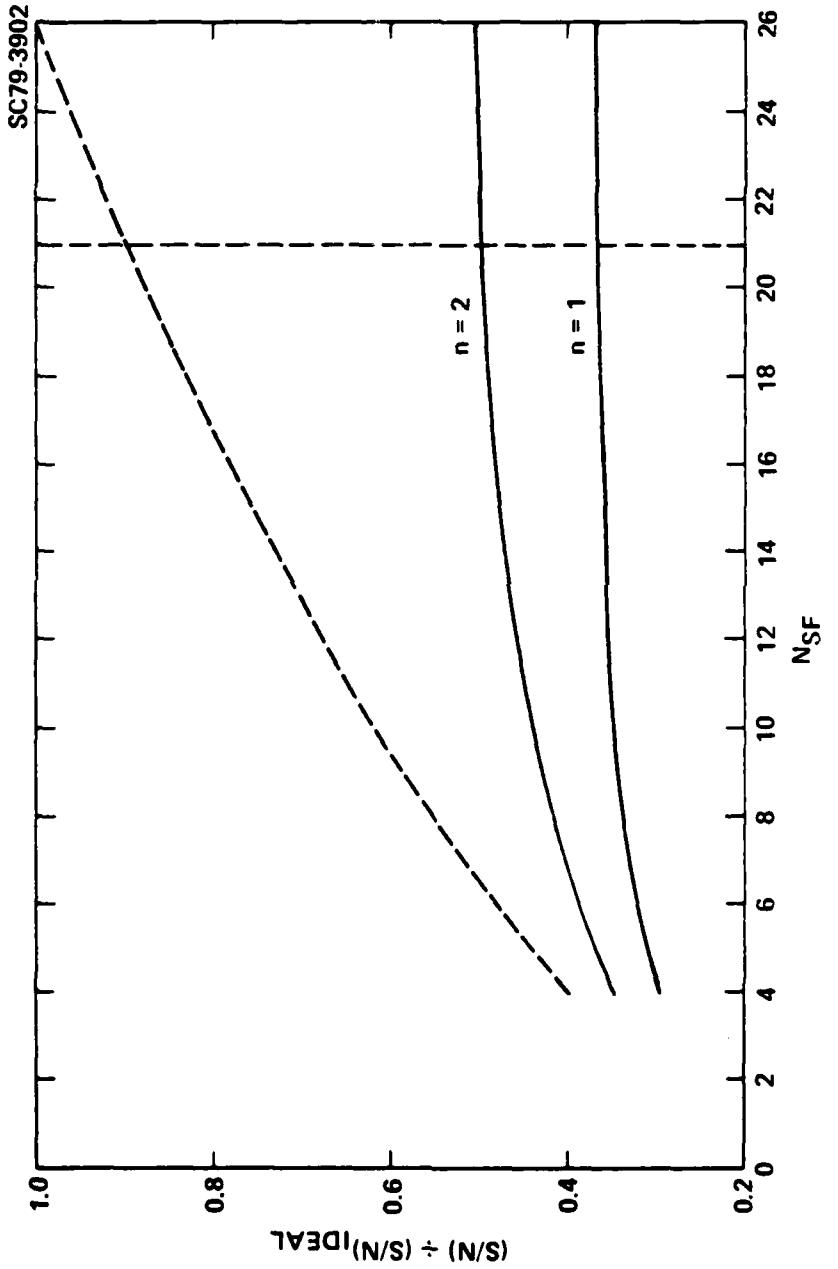

Fig. 3.13 System signal-to-noise ratio with partitioner gain reducer.

processor noise referred to in the input CCD well. The 1/f noise referred to this input well can then be added in quadrature to obtain the total noise.

Consider operation over a full frame time. The 1/f noise current of a MOSFET is given by

$$I_n^{1/f} = (8/3\ kT\ g_m)^{1/2} \left(\frac{f_n}{f}\right)^{1/2} \tag{29}$$

where f_n is the frequency where the 1/f noise equals the MOSFET channel thermal noise. Noise voltage is related to noise current by

$$V_n^{1/f} = \frac{I_n^{1/f}}{g_m} = \frac{(8/3\ kT)^{1/2}}{g_m^{1/2}} \left(\frac{f_n}{f}\right)^{1/2} \tag{30}$$

A good low noise MOSFET has $V_n^{1/f} = 10\ \mu V/\sqrt{Hz}$ at f=1 hz; from the parameters of Section 2.1.3 the MOSFET thermal channel noise is 5.8×10^{-14} amps/$\sqrt{Hz}$. Combining these two numbers yields $f_n = 6.6 \times 10^3$ Hz.

Now the total 1/f noise current over a frame time is

$$I_{n.T}^{1/f} = \int_{f_o}^{\sqrt{1/2t_f}} I_n^2 df = \left[(5.8 \times 10^{14})^2\ f_n\ I_n \frac{1/2t_f}{f_n} \right]^{1/2} \tag{31}$$

where f_o is the lowest frequency of interest. Evaluating this with t_f = 16 msec f_o = 0.1 Hz

$$I_{n,T}^{1/f} = 1.13 \times 10^{-11}\ A.$$

The 1/f noise change, referred to the input CCD well (suppressed by a factor of $1 + g_m R_D$) is:

$$\sigma^{1/f} = \frac{I_n^{1/f}\ t_f}{q(1+g_m R_D)} \tag{32}$$

For $R_oA = 85$, and operation with 100 mV reverse bias, which has been shown to be possible, $R_D = 1.5 \times 10^9\ \Omega$. Therefore, from Eq. (4), with $g_m = 4.7 \times 10^{-7}$ mhos

$$o^{1/f} = 1.54 \times 10^3 \text{ holes rms}$$

For conditions of the curve n=1 of Fig. 3.10, the total noise charge not including the 1/f noise component (N_{SF} = 26) is 4.46 x 10^4 holes rms. The total noise charge after adding the 1/f noise is also 4.46 x 10^4. Therefore, the 1/f noise under these conditions does not degrade the overall system performance.

Test MOSFETS of similar geometry to those utilized in the input circuits will be incorporated on the test chip so that the 1/f noise can actually be measured. Buried channel FET's will also be included and evaluated. However, operation with ~100 mV reverse bias on the detectors should guarantee that MOSFET 1/f noise will not be a problem.

3.3.2 Test Chip Design and Layout - General

To test and evaluate approaches for implementing the multiplexer concept, a test chip will be configured, laid out, processed and tested. This test chip will include:

1. Various approaches to the detector-to-CCD input circuit, with 51 x 51 μm cell size, in 5 x 5 arrays and/or linear arrays or single elements;

2. Approaches to gain reducer circuits, including fill-and-spill gain reducer and partitioner implementations;

3. Approaches to accumulate-and-store arrays, as 5 x 5 arrays with 51 μm x 51 μm cell size;

4. Two or more 5 x 10 arrays incorporating a 5 x 5 detector-CCD input array, gain reducers for each column and a 5 x 5 accumulate-and-store array with multiplexed output;

5. Multiplexer designs;

6. and miscellaneous test circuits, such as buried channel FET input structures, threshold voltage variation test structures, etc.

Figure 3-14 shows the tentative organization of the test chip, which is device number 30343, showing the locaiton of the various circuits. The

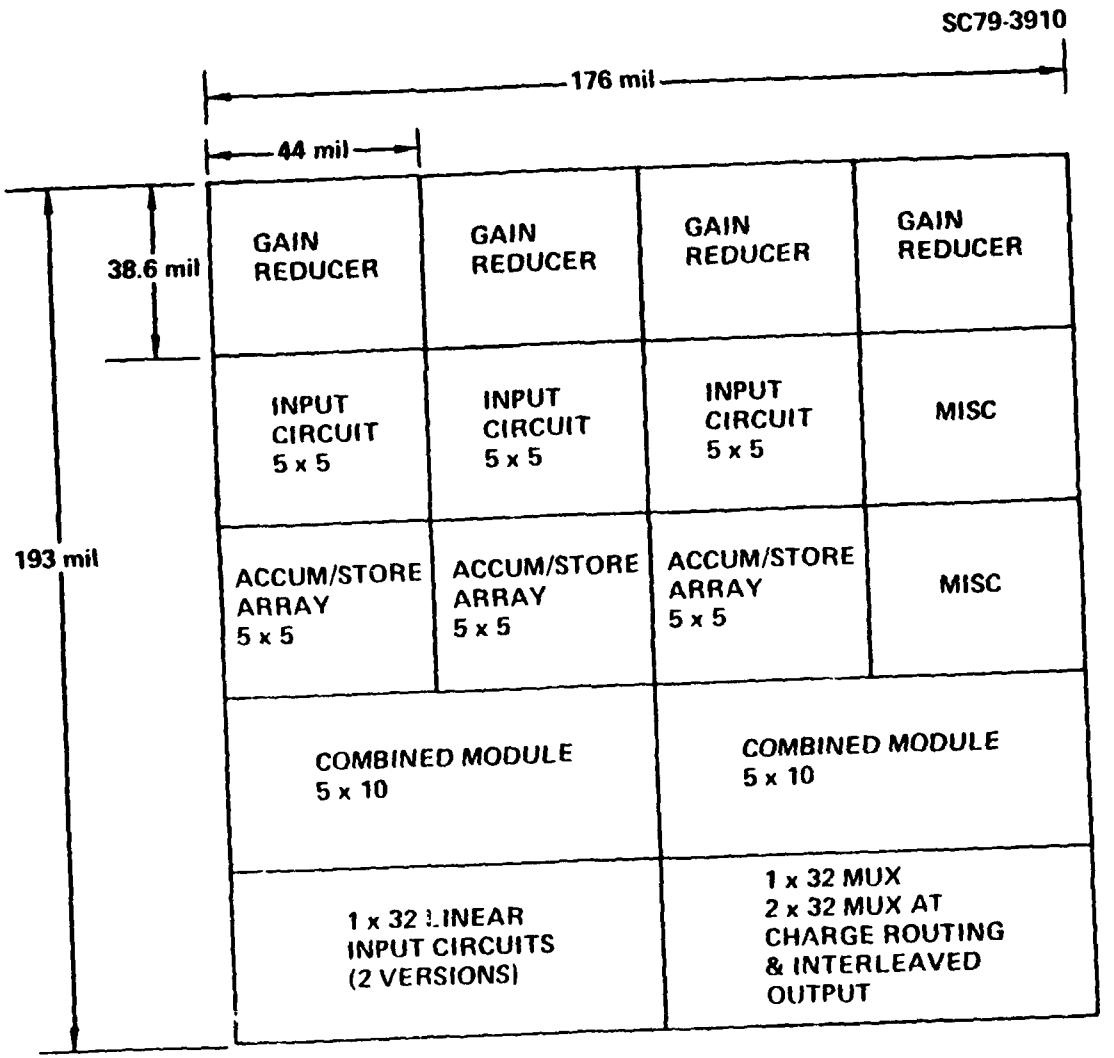

Fig. 3.14 Test chip overview - Device 30343.

test chip is being organized to have only two different output pad sets for ease of probing. These are an 8 x 7 pad set and a 16 x 7 pad set for larger devices (Fig. 3.15). Twelve of the smaller blocks and four of the larger can be accommodated on a test chip of approximately 200 mil^2, as indicated on Figure 3.14. The accumulate-and-store array layouts have 5 x 5 storage elements, 51 μm x 51 μm in size, and each is provided with three or five separate inputs and five separate outputs. The inputs are configured as fill-and-spill circuits identical to the fill-and-spill portion of the gain reducer test circuits. The input circuit arrays will be configured to have individual output charge sensing circuits (one for each of the five columns) very similar to the charge sensing circuit of the gain reducers. This combination will offer the possibility of evaluating the entire focal plane concept (input array plus gain reducer plus accumulate-and-store array) by wire bonding the outputs of an input array to the inputs of one of the accumulate-and-storage arrays. This option then provides another approach to evaluating the overall focal plane concept, in addition to the 5 x 10 combined modules.

The individual components to be incorporated on the test chip are described in the sections which follow.

3.3.3 Detector-to-CCD Input Circuits

In the focal plane array section of the multiplexer chip charge from the photodiode array is coupled to a CCD multiplexer structure and transferred out for further processing in subsequent portions of the multiplexer. For a design specification of 2 mil x 2 mil cells in the focal plane array section, direct injection is chosen as the preferred approach to the detector-CCD interface, because of its relative simplicity and advanced state of development. In addition, the analysis of Section 2.0 demonstrated the utility of background skimming in improving overall system performance. This approach-direct injection with background skimming -- has been utilized and demonstrated on other hybrid focal plane multiplexers, most recently the 32 x 32 Advanced Infrared Imaging Seeker (AI^2S) focal plane. The input circuit design for this device, which has 4 mil x 4 mil cell sizes, will be the basis for the designs for the present multiplexer. Basic operation of a direct-injection with background skimming circuit has been given in Section 3.3.1.1.

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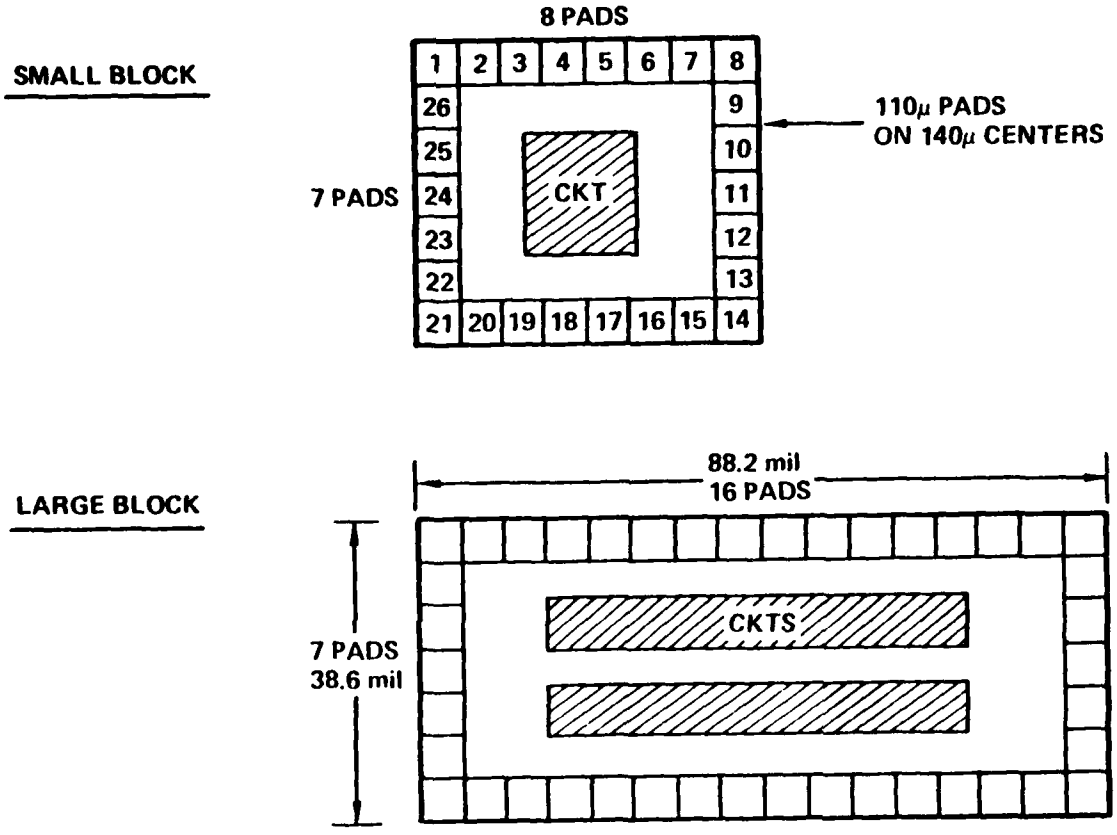


Fig. 3.15 Test chip (30343) pad layout detail.

3.3.3.1 Input Circuit Designs

The direct injection with background skimming (DIBS) circuit used in the 32 x 32 AI^2S chip is shown in schematic fashion in Fig. 3.16. In this design, all the critical gates - input (DIG), background storage (BS), and meter (MET) - are first level polysilicon gates for minimum threshold voltage variations or increased storage capacity. A common buffer gate (B1) bridges the gaps between these gates. The skim drain (SD) is implemented as a diffused bus line. Six leads (not including the input source (IS) and CCD phase electrodes) must be routed to each unit cell.

To adapt this design to a 2 mil x 2 mil unit cell, some modifications must be made. Three modifications which reduce the required number of bus leads and lend themselves to a more compact layout are shown in Fig. 3.17(a)-(c). Circuit (a), AI^2S adaption, retains first polysilicon DIG, BS, and MET gates, but the second level gates bridging the gaps of BS are connected to BS with polysilicon-polysilicon contacts. Also, a buffer gate is needed between MET and array phase 1 (A1) or phase 3 (A3). This gate can either be brought off-chip or connected to A1 (or A3) with a poly-poly contact. This circuit provides potentially the best background skimming uniformity and skimmed charge storage capacity. However, this comes at the expense of reduced CCD storage area, because of the large number of gates which must be defined. Also, obtaining sufficient space to make the B1-A1 contact is difficult.

Circuit (b) - second level meter gate - is the simplest adaptation, in that making the meter gate a second polysilicon gate leads to the need for fewer buffer gates. Five leads are needed for the input circuit, not including IS. Two each can be routed on the first and second polysilicon levels, and the skim drain interconnected by an aluminum bus. Because of the second level meter gate, analysis of background skimming shows that the skim nonuniformity may be worse that in circuit (a). Because of the first level BS gate, skimmed charge storage capacity is good.

A third variation is shown in circuit (c) - second level background storage gate. Here, the BS gate is second polysilicon and the MET gate is first polysilicon. This leads to the same number of gates and bus lines as circuit (b). Because MET is first polysilicon, skimming nonuniformity is

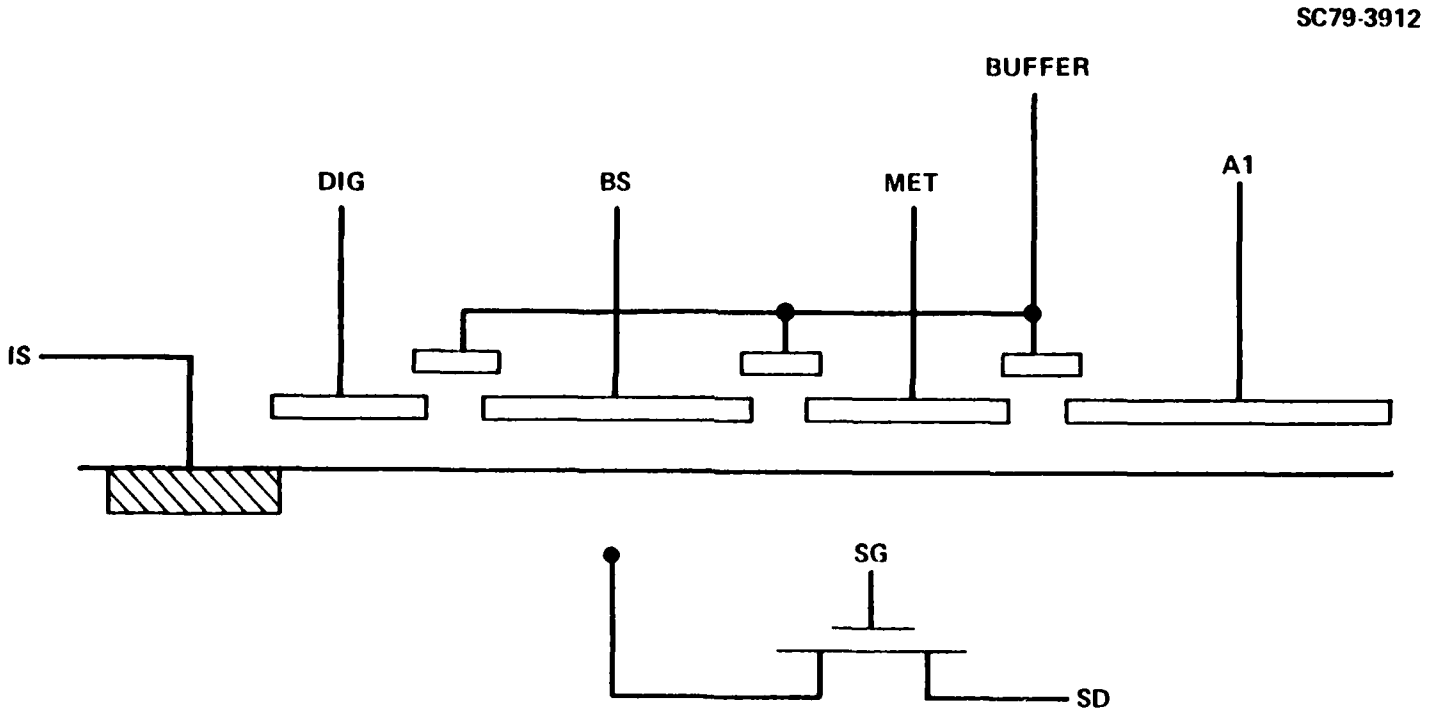


Fig. 3.16 Schematic of Al^2S direct injection with background skimming circuit.

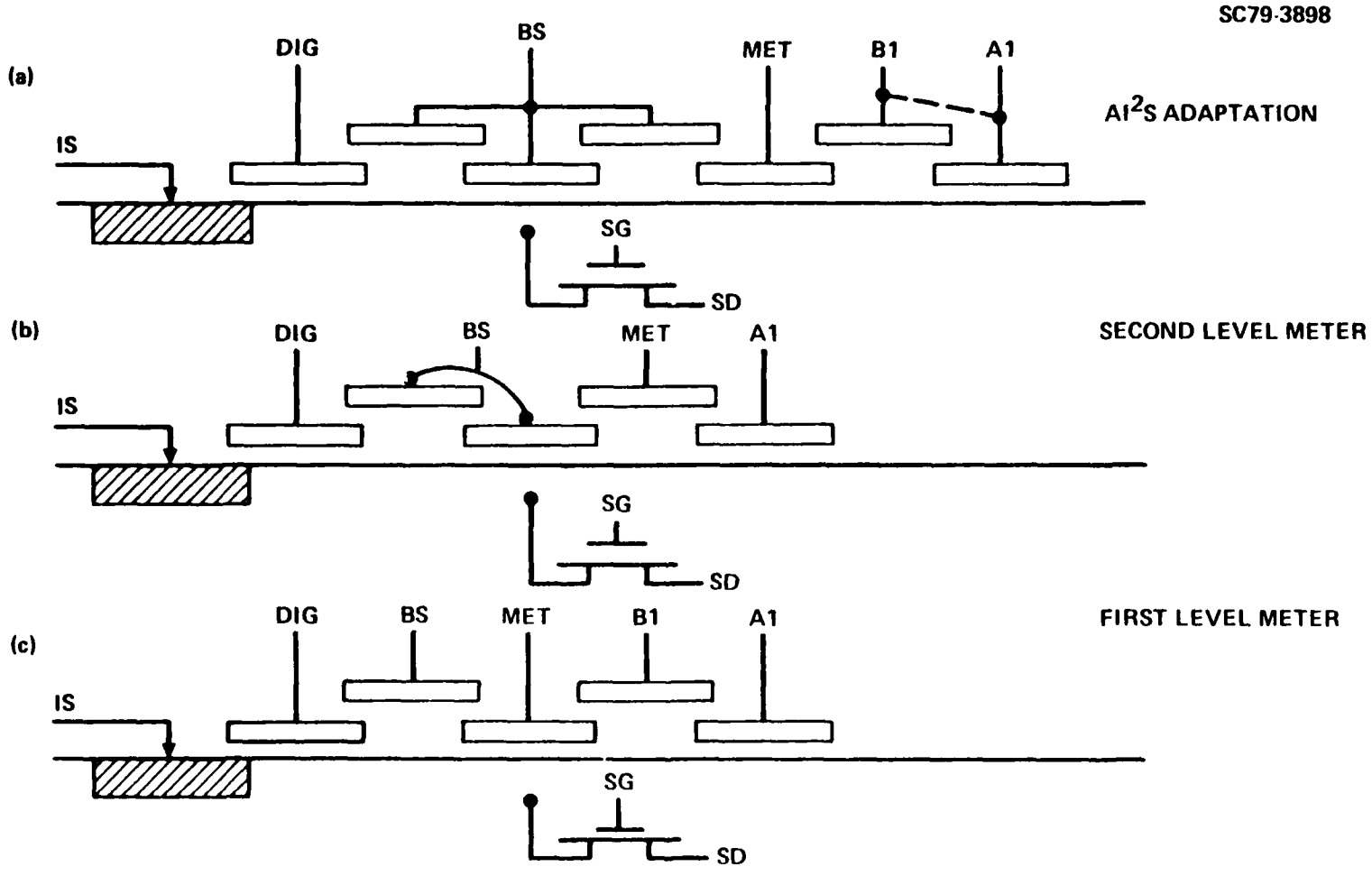


Fig. 3.17 Input circuit options.

minimized but skimmed background storage capacity is reduced. Other potential problems with this option involve obtaining sufficient area to make the B1-A1 polysilicon contact to avoid an extra lead, and the fact that the skim gate (SG) must be first polysilicon to interface with the second polysilicon BS gate.

Some of the properties of each of these three options are summarized in Table 3.2. The storage area, as a percentage of the 51 μm^2 cell, has been estimated from preliminary layouts. Circuit (b) is the most straightforward in terms of layout; accordingly, its design and layout are the furthest along at this time, as discussed in the next section.

3.3.3.2 Detailed Layout Considerations - Second Level Meter Gate Circuit

The present 32 x 32 AI^2S device is laid out as schematically shown in Fig. 3.18. One CCD electrode structure serves two channels, divided by a channel stop diffusion. A four-phase CCD is used for maximum charge handling capability. Detector charge flows through the input diode, into the background storage gate (charge to be skimmed) and CCD (charge to be retained). The skimmed charge is then removed to the skim drain, which is a diffused bus running between the diode input diffusions. In reducing the layout to 2 mil cells, a double channel CCD is retained, to reduce overhead area required for bus lines. However, use of a diffused p^+ bus for the skim drain connection is no longer practical without severely reducing the available CCD storage capacity. Using conventional n^+ channel stops with minimum 5 μm gap between p^+ and n^+ regions forces the input diffusions toward the CCD channel. This shift must be accommodated by reducing the CCD cell width, since lead routing area required is fixed. The p^+ skim drain will therefore be implemented using an isolated diffusion connected with an aluminum line. Furthermore, to reduce the number of diffusions required, the layout will be configured so that one skim drain diffusion serves four cells. This allows the background storage gate to be made larger. A schematic of the resulting layout, showing the diffusions and first polysilicon CCD gates is shown in Fig. 3.19. The basic building block for the array therefore consists of 4 input cells; this building block is repeated to make up the entire array. Because of the mirror symmetry both horizontally and vertically about the skim drain, and the fact

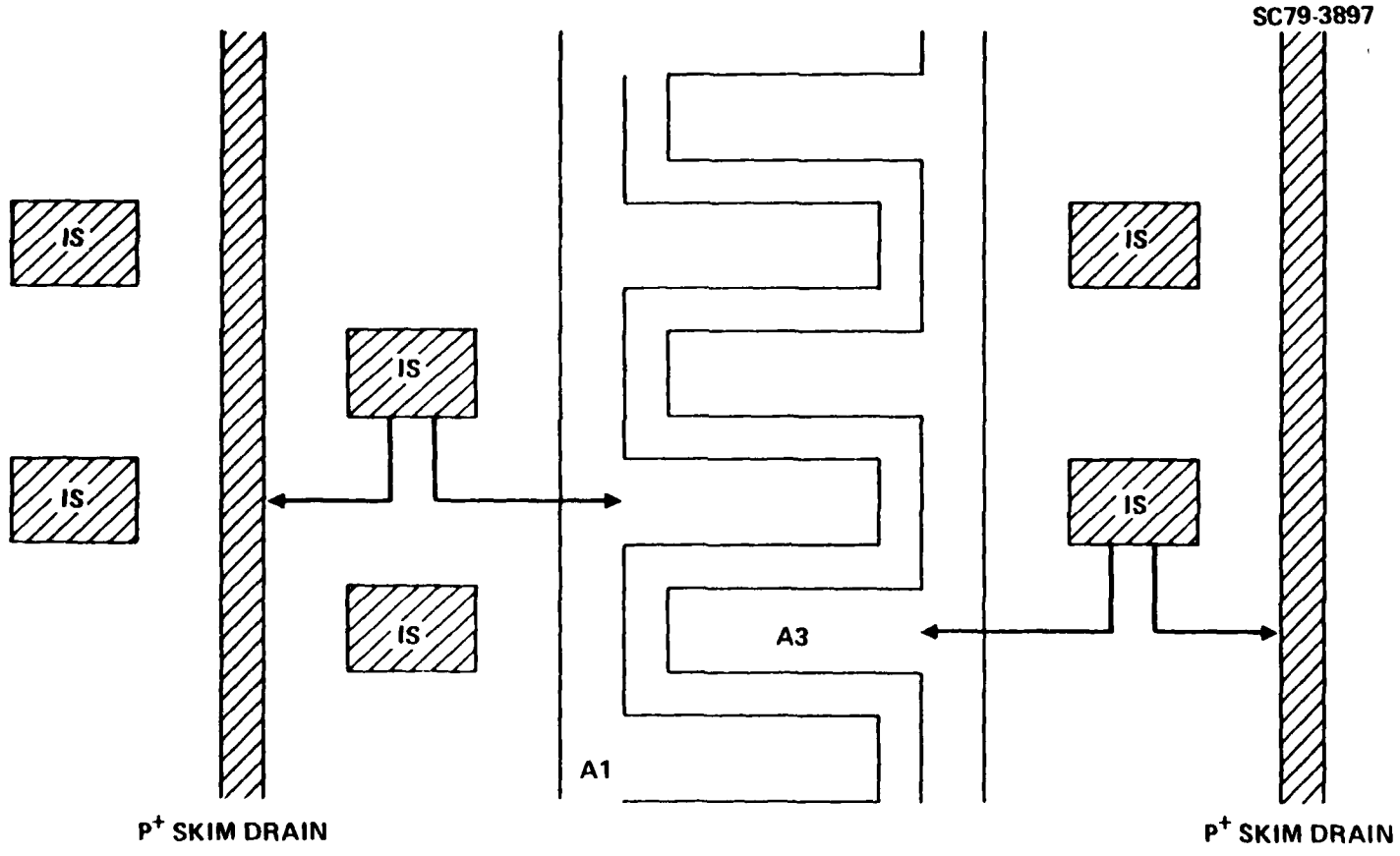


Fig. 3.18 Schematic layout of AI^2S circuit.

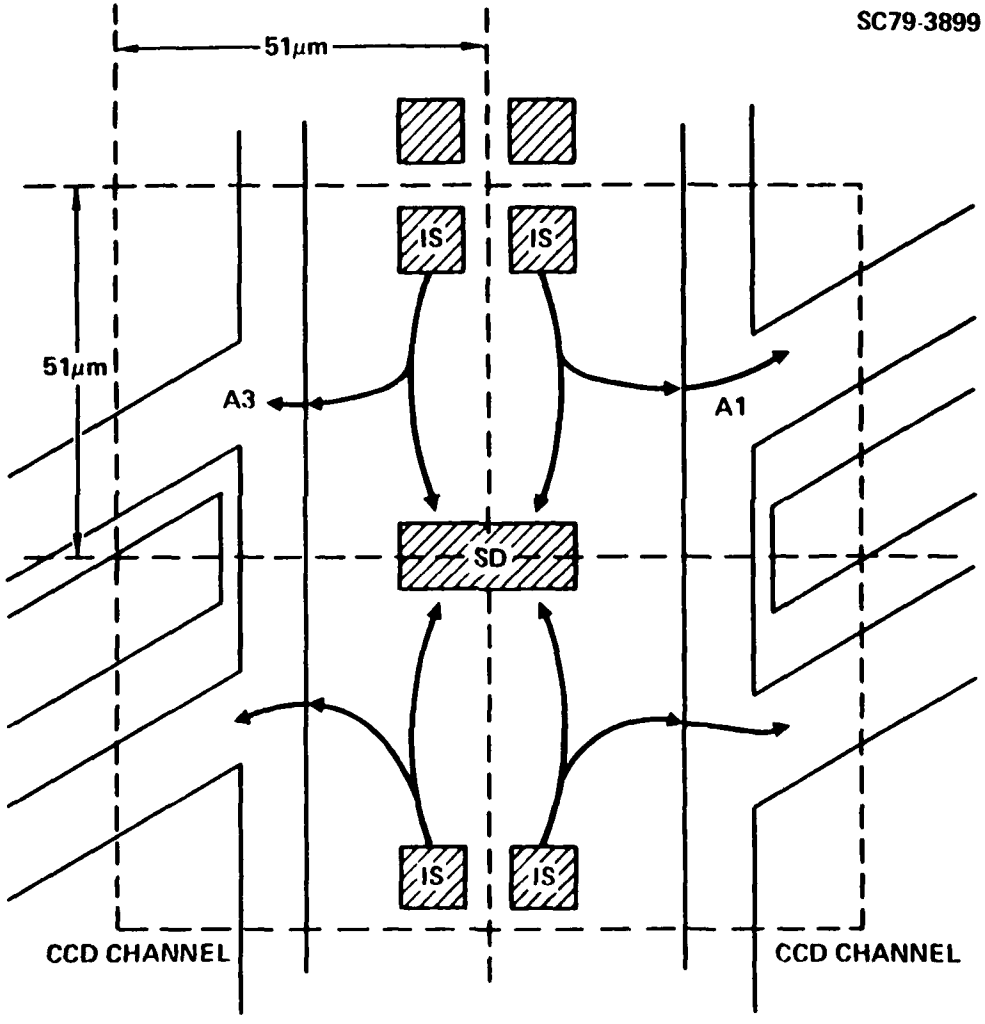


Fig. 3.19 Layout of 2 mil^2 input cell.

Table 3.2

Comparison of Input Circuit Options

Circuit	Lead Count(1)	Gate Count(1)	Storage Area Estimate(2)	Advantages & Disadvantages
(a) AI^2S Adaption	6	6	12.5%	First level storage and meter gates- best skim uniformity and BG store capacity. High Lead Count → Dense layout, low storage area
(b) 2nd Level Meter Gate	5	5	20%	Reduced lead count for layout simplicity (compared to (a)) Second Level MET → Good skim nonuniformity. Good background storage capacity
(c) 1st Level	5	5	20%	Reduced lead count compared to (a) First level MET → Good skim uniformity. Second Level Store → Poor BKG storage capacity. May be problems with SG and B1, i.e., SG is first level, min. area for making B1 p-p contact

(1) Input circuit only - not IS or array gates
(2) Percent of 51 μm^2 cell area

that charge enters the CCD from the right under the A1 CCD gates and from the left under the A3 gates, the gate fingers must be tilted as shown.

This approach to the input circuit layout has been computer coded and a computer plot showing the n^+, p^+, and first polysilicon gate levels is shown in Fig. 3.20. The CCD storage area is (1/2 CCD cell area) 561 μm^2 (21.5% of cell area) and the background storage gate area is 249 μm^2. Detector contact is made via an aluminum pad ~20 μm^2 on top and centered on each unit cell and contacting the input diffusion, IS.

3.3.3.3 Additional Input Circuit Layouts

Detailed layout and computer coding of other input circuit options is underway. The designs to be implemented include circuit (c) of Fig. 3.16 and a second version of circuit (b), using dielectric channel stops to possibly allow a diffused p^+ skim drain without detracting from CCD channel capacity.

3.3.4 Gain Reducer Circuits

In this section, the gain reducer concepts to be incorporated for test on the TECS test chip are introduced, discussed, and analyzed. Circuit schematics and layouts as they will be implemented on the test chip will be presented, and additional on-chip circuitry required for test and evaluation and test procedures will also be discussed.

After each subframe, the integrated charge is read out of the focal plane array by column CCD registers to a gain reducer circuit; one such circuit for each column. It is the purpose of the gain reducer circuit to produce an attenuated replica of the incoming charge packets with a minimum of additive noise. The attenuated charge packets are then accumulated in full frame of data is read out. The analysis of Section 3.3.1 indicates that gain reductions in the range 10-25 will be required, depending upon storage capacity which can be attained in the accumulate-and-storage array. In addition, the gain reducers must process each sample in 2-4 μsec so that system dead time can be reduced.

Two basic approaches for accomplishing the gain reducer function are proposed for inclusion on the test chip. These are: (1) the fill-and-spill

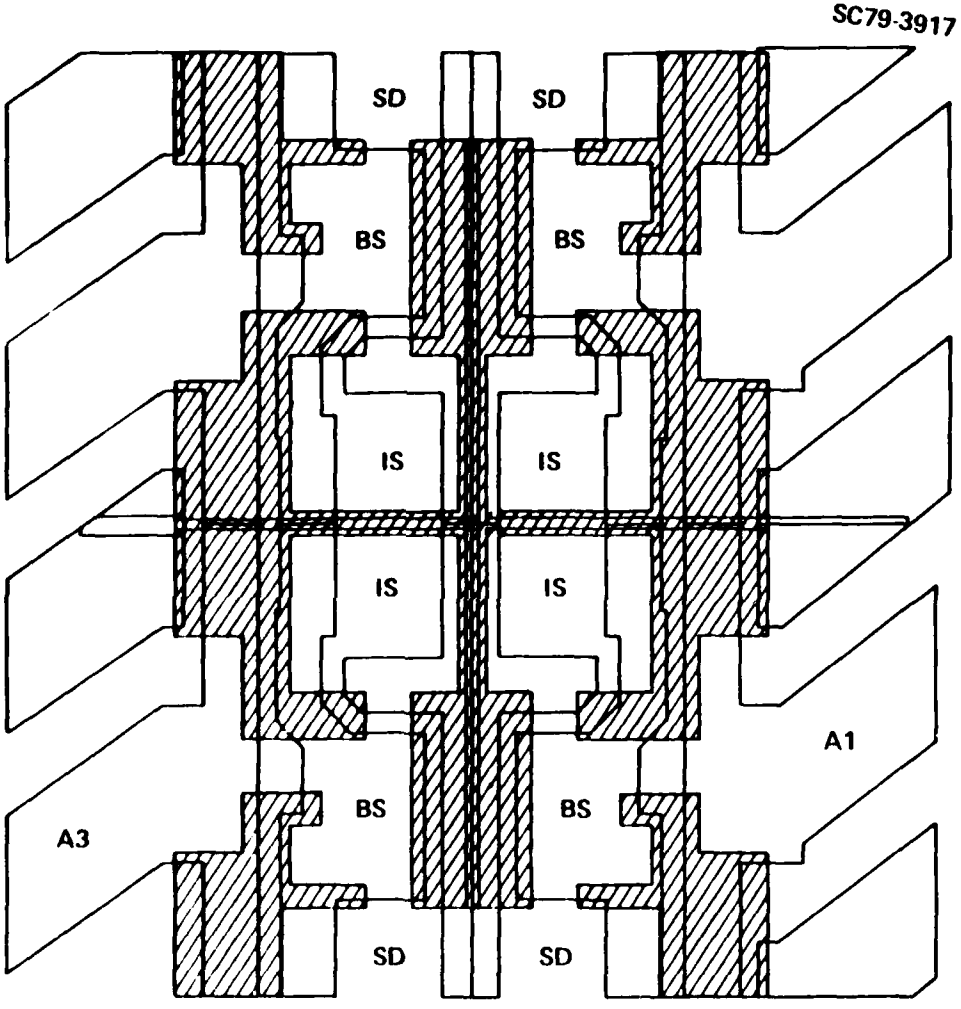


Fig. 3.20 Computer plot of four cell input circuit module.

gain reducer, in which incoming charge packets are converted to a voltage at a reset floating diffusion node, this voltage is applied to one of the gates of a fill-and-spill circuit and a new, attenuated, charge is generated; and (2) the partitioner gain reducer, in which a packet of charge is divided into two separate packets by raising a gate. These two approaches are described in detail, analyzed, and test circuit designs, layouts and test procedures are given in the sections which follow.

3.3.4.1 Fill-and-Spill Gain Reducer

A schematic of the fill-and-spill (FS) gain reducer is shown in Fig. 3.21. At the left, the charge packets are brought to a reset floating diffusion node, where the charge, Q_{in}, is converted to a voltage change:

$$\Delta V = \frac{Q_{in}}{C_N} \tag{33}$$

where C_N is the capacitance of the output node, the actual voltage on the node is $-V_R + \Delta V = -V_R + Q_{in}/C_N$, where $-V_R$ is the reset level of the floating diffusion. This voltage is also applied to the backflow gate of the fill-and-spill circuit. A source follower buffer may or may not be included between the sensing node and subsequent circuitry. Its utility would be in assuring equalization of node capacitance for different channels if different lead routing patterns were required between the focal plane and storage arrays (i.e., fan-out). In the following discussion, a buffer is not included. The fill-and-spill storage gate is connected to a fixed DC level. Assume this voltage is $-V_R$, then the difference voltage from the backflow to storage gates is $-V_R = Q_{in}/C_N - (-V_R) - Q_{in}/C_N$. Fill-and-spill action then generates an output charge, Q_{out},

$$Q_{out} = \frac{Q_{in}}{C_N} \cdot C_{ox} A_1 \tag{34}$$

where C_{ox} = the specific oxide capacitance under the storage gate and A_1 = active area of this gate.

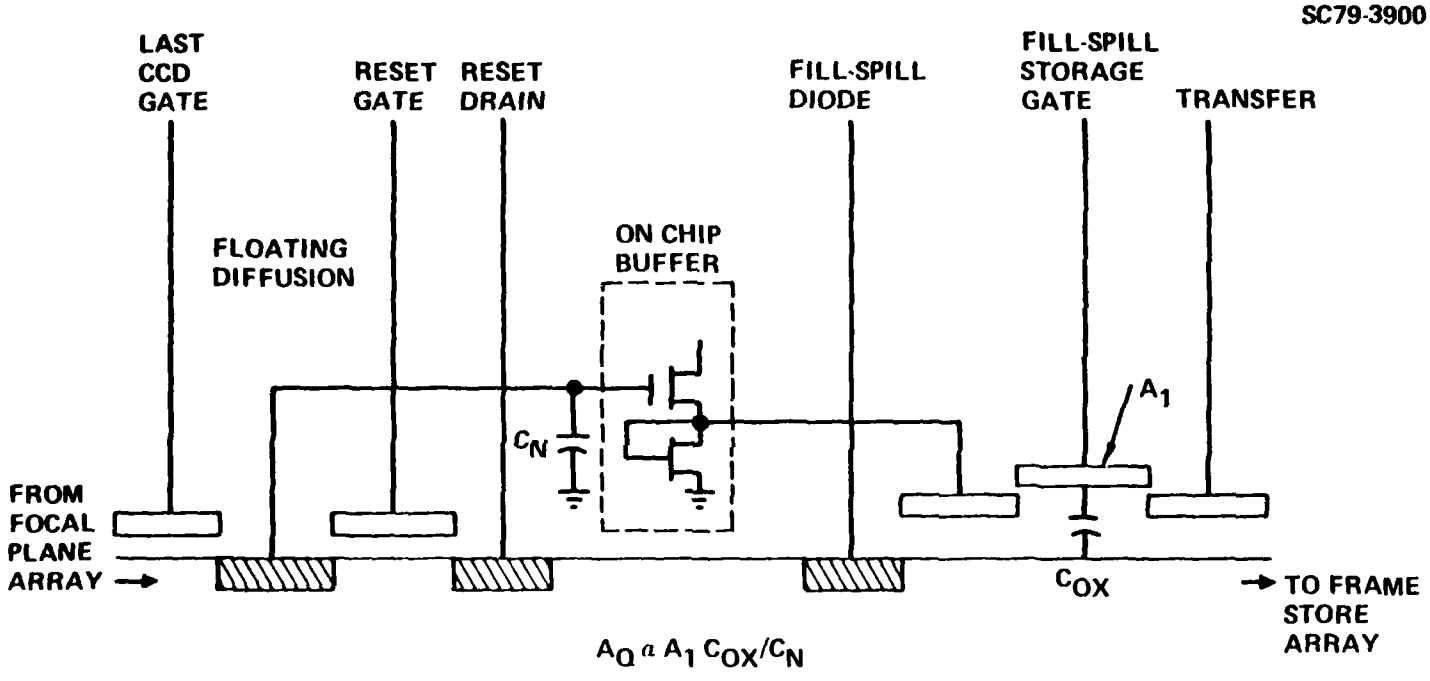


Fig. 3.21 Fill-and-spill gain reducer schematic.

Therefore, the charge gain is:

$$\frac{Q_{out}}{Q_{in}} = \frac{C_{ox}A_1}{C_N} \tag{35}$$

If the node capacitance is predominantly due to a polysilicon capacitor of area A_n over channel stop with specific capacitance C_{ox}:

$$\frac{Q_{out}}{Q_{in}} = \frac{A_1}{A_n} \tag{36}$$

and gain reduction is accomplished by making $A_n > A_1$ ($C_N > C_{ox}A_1$).

Design Considerations

As indicated by Eqs. (31) and (32), the charge gain is adjusted by proper sizing of the fill-and-spill storage capacitance (area) and the node capacitance. Several other considerations determine the allowable design region for the various portions of the circuit. Figure 3.22 shows the fill-and-spill circuit, showing important dimensions. Q_{out} is given by

$$Q_{out} = C_{ox} \cdot W \cdot (L_G+L_B)(V_S-V_{BF}) \tag{37}$$

L_G+L_B is limited by thermal diffusion limited transfer during the time the storage gate is emptied; this and the desired period of operation determines the maximum value of $L_G+L_B = L_T$. The thermal diffusion time constant is:

$$\tau_{th} = \frac{4L_T^2}{\pi^2 D} \tag{38}$$

where D = diffusion constant, ≈10 at 195 K.

6.9 time constants must elapse for only ~0.1% of the charge to be left behind. Table 3.3 gives values of τ_{th} and 6.9 τ_{th} for various gate lengths.

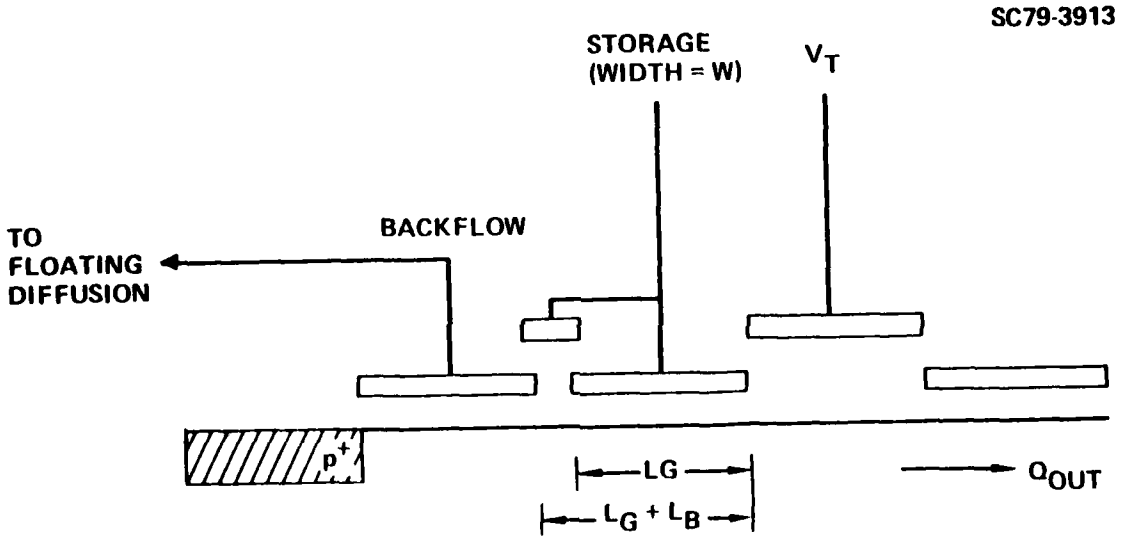


Fig. 3.22 Fill-and-spill portion of gain reducer.

Table 3.3

L_T	τ_{th}	$6.9\ \tau_{th}$
5 μm	10^{-8}	6.9×10^{-8} sec.
10	4×10^{-8}	2.7×10^{-8}
15	9×10^{-8}	6.2×10^{-7}
20	1.6×10^{-7}	1.08×10^{-6}

Since it is desired to operate the gain reducers with as little as 2 μsec cycle time, the readout time should be <1 μsec, implying that L_T be <15 μm. The minimum L_T, assuming a first level storage gate overlapped by second polysilicon buffer and transfer gates, is determined by design rules. For 2 μm minimum gaps and 2 μm overlap, the minimum L_T is 10 μm.

With the restraint on L_T, W and $\Delta V_S = V_S - V_{BF}$ are determined by the gain reduction desired and the maximum input charge. Previous analysis showed that maximum charge from the focal plane array is ~1.9×10^7 holes/packet. For gains of 10 and 25 (spanning the expected range of values to be used) Q_{out} is 1.9×10^6 abd 7.6×10^5, respectively. For these values of Q_{out}, ΔV_S required is plotted vs. L_T with W as a parameter in Fig. 3.23. Specification of the gain reduction factor (Q_{out}) and any two of the other parameters determines the third. ΔS_S is constrained by the maximum voltage swing allowed on the floating diffusion node. With circuit operating voltages on the order of 20 V, a 10 V swing might be possible; 5 V is a reasonable design value. W will, of course, be less than the cell center-to-center spacing 51 μm) and should be close to the input channel width of the accumualte-and-store array (10 μm), but can be larger or smaller than this.

Specification of the voltage swing, ΔV_S, determines the capacitance required on the output node, and assuming this capacitance is obtained by a first level polysilicon gate over channel stop, the gate area required:

$$C = \frac{1.9 \times 10^7 \times 1.6 \times 10^{-19}}{\Delta V_S} \qquad (39)$$

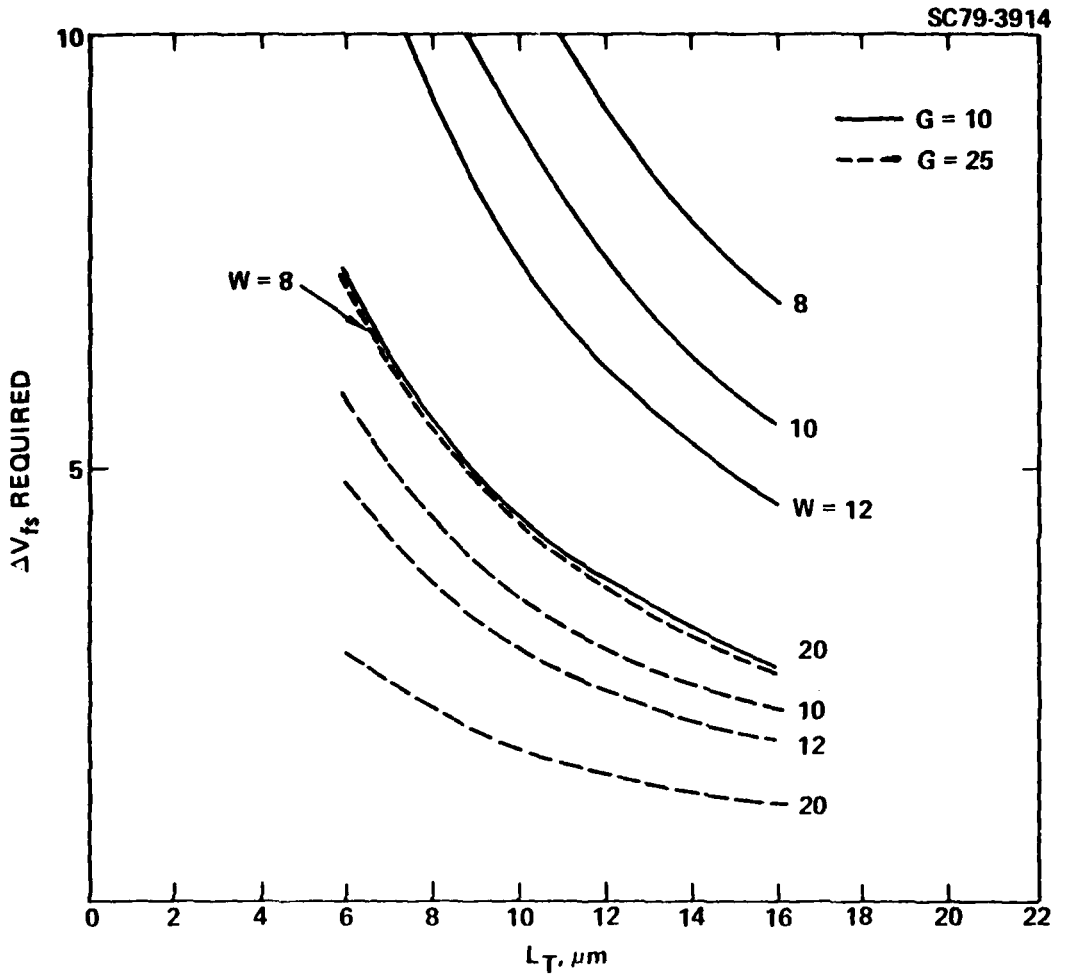


Fig. 3.23 Fill-and-spill voltage required for different G vs. L_T and W.

and

$$A(cm^2) = C/3.45 \times 10^{-8} \text{ (for 1000Å oxide).} \qquad (40)$$

Values of C, the dimensions of a square gate, and the dimensions of a rectangular gate with one dimension = 50 μm are given in Table 3.4 for different ΔV_S.

Table 3.4

ΔV_S	C(Farad)	A(cm^2)	Square Dimensions(μm)	Rectangular Dimension(μm)
2	1.52×10^{-12}	4.4×10^{-5}	66	50 x 88
4	7.6×10^{-13}	2.2×10^{-5}	47	50 x 44
5	6.08×10^{-13}	1.76×10^{-5}	42	50 x 35
6	5.1×10^{-13}	1.47×10^{-5}	38	50 x 29.4
8	3.8×10^{-13}	1.1×10^{-5}	33	50 x 22
10	3.04×10^{-13}	8.8×10^{-6}	30	50 x 17.6

From the foregoing the following conclusions and guidelines can be inferred. Small gain reduction factors, desirable from a system noise standpoint, require large values of L and W (given a maximum voltage swing). Larger gain reduction factors allow reduction of L and/or W. It is desirable to use as great a voltage swing as possible to minimize the silicon real estate required for the node capacitance. In this regard, use of multiplate capacitors would be desirable to get the maximum capacitance in minimum area. Note that to attain a given gain reduction factor, there are basically two design approaches:

1. For constant storage gate size, adjust the value (area) of the output node capacitance.

2. For constant output node cpacitance vary the size of the storage gate.

In the gain reducer circuits incorporated on the test chip, these options will be utilized, as described in the next section.

Gain Reducer Test Circuit Layouts

The basic functional blocks of the gain reducer test circuits to be incorproated on the test chip are shown in Fig. 3.24. First there is a charge generation circuit, which will be a fill-and-spill circuit, to generate a fixed input charge packet. Next comes the gain reducer itself; associated with the detection node will be a voltage monitoring circuit (source follower stage) to measure the input charge. Finally, there is an output circuit to detect and measure the output charge after gain reduction. To minimize the layout and test complexity, it is proposed to use the same charge input circuit, input charge monitor circuit, and output charge monitor circuit with several different gain reducer configurations. These gain reducer configurations are:

1.Gain reduction of 12 (G=12) with a 12 μm x 12 μm fill-and-spill storage gate and node capacitance (first level polysilicon gate) sized for maximum 5 V swing.

2. G=25 with 12 μm x 12 μm fill-and-spill storage gate and node capacitance (first polysilicon gate) sized for maximum 2.5 V swing.

3. G=25 with 12 μm x 12 μm fill-and-spill storage gate and a double plate capacitor for layout area reduction (second polysilicon plate connected to ground lying over the first polysilicon capacitor).

This set of configurations should allow the various design options to be adequately evaluated.

A schematic of one of the test circuit configurations (without buffer) is given in Fig. 3.25 and a sketch of the layout, showing diffusions and first poly gates is shown in Fig. 3.26. The channel width and gate lengths in the input charge generator are very close to values anticipated for the focal plane array, so that testing can be conducted with charge packets the same as those expected in the final system. The entire circuit is laid out in a 51 μm dimension in the horizontal direction, compatible with the final desired cell size. The input and output charge monitor circuits are identical (the input monitor circuit source follower is not shown in Fig. 3.25.

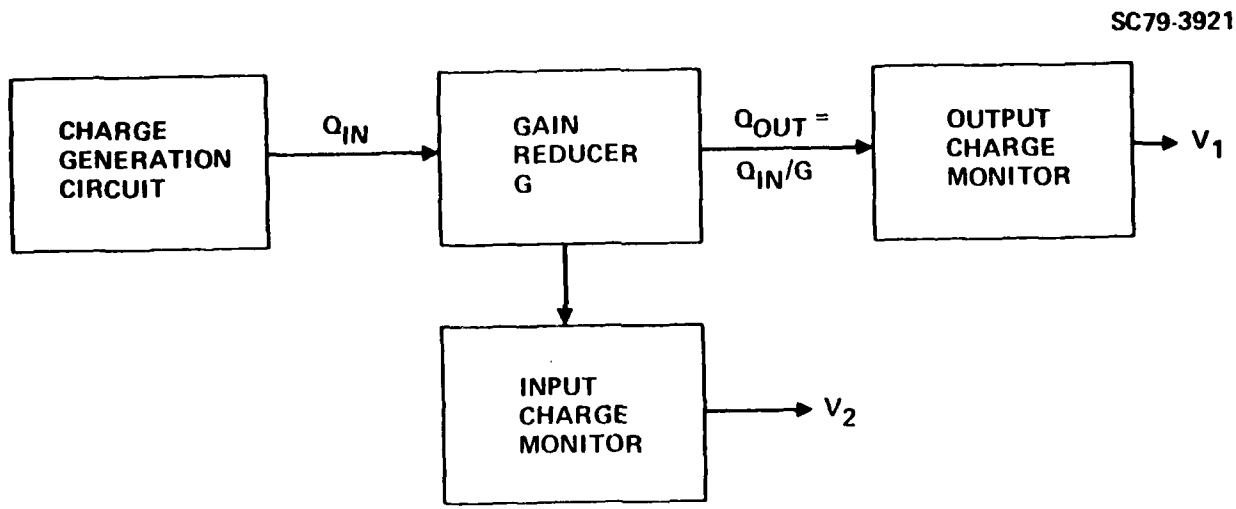


Fig. 3.24 Block diagram of gain reducer test circuit.

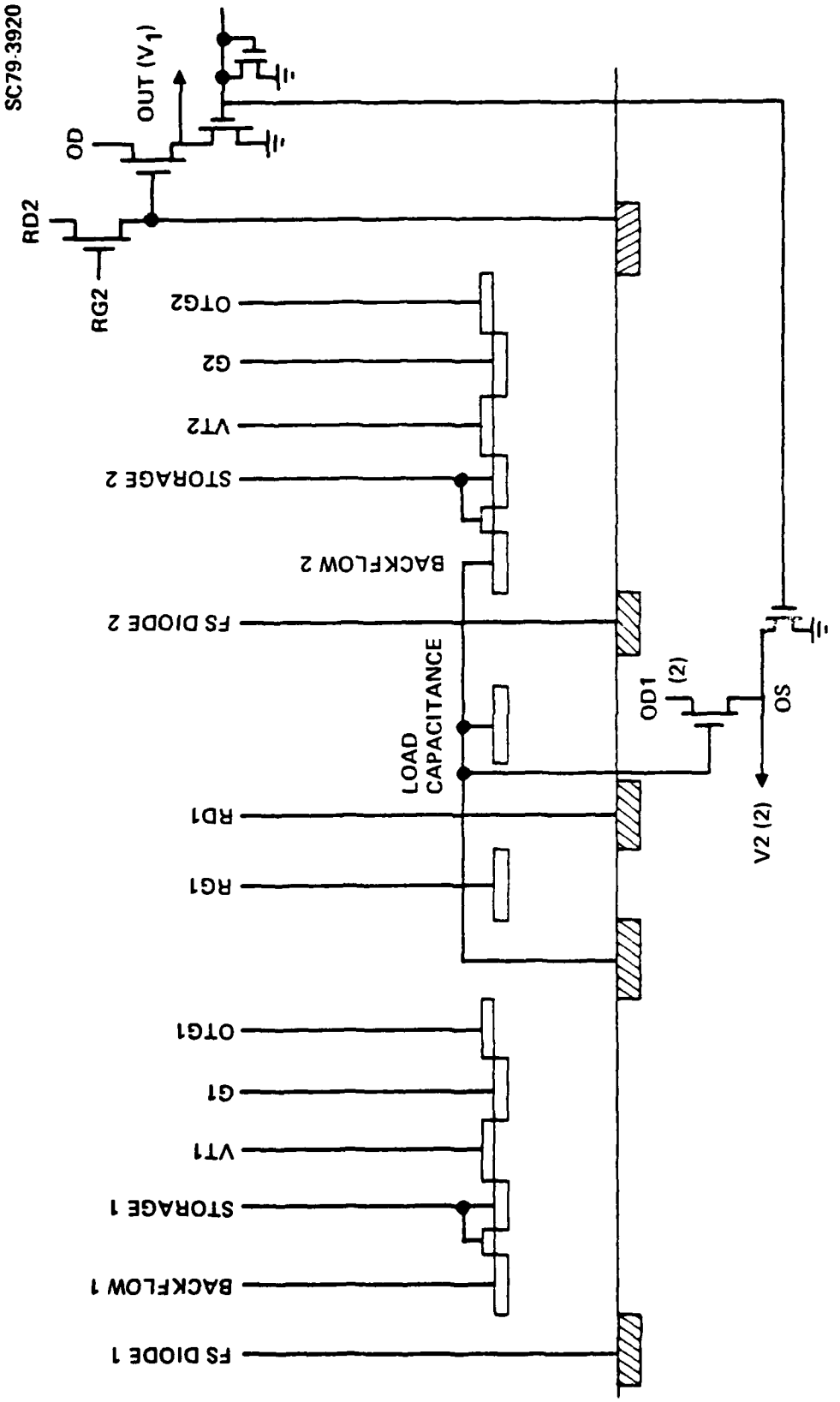


Fig. 3.25 Gain reducer test circuit schematic.

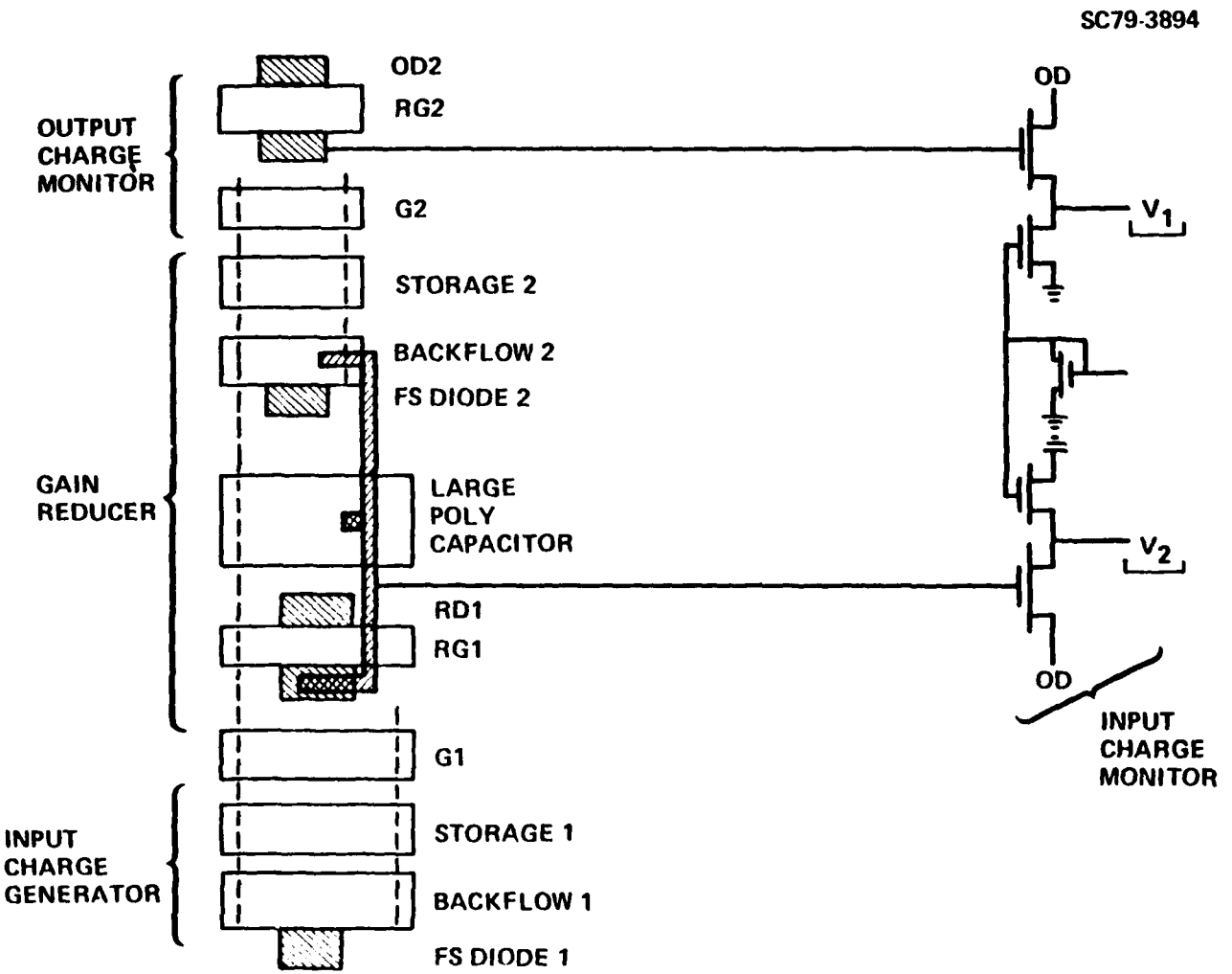


Fig. 3.26 Fill-and-spill gain reducer test circuit layout.

Test and evaluation of the gain reducer circuit of Figs. 3.25 and 3.26 will be conducted by first determining the charge responsivity of input and output monitor circuits in standard fashion. Also the input charge generator can be calibrated in terms of charge generated vs. gate voltages. Then Q_{out} vs. Q_{in} is determined by comparing the two monitor outputs, and the gain, gain linearity with charge, etc., can be determined. Noise of the gain reducer is inferred by first determining the KTC noise of the two output circuits, then noise on the input charge, using the input charge monitor, and finally measuring the total noise on the output charge.

3.3.4.2 Charge Partition Gain Reducer

A schematic diagram of a charge partition gain reducer is shown in Fig. 3.27. The input charge is initially introduced into a bucket consisting of three or more gates, all of which are on to the same surface potential. S1 and S2 have areas in the ratio G-1 to 1, where G is the desired gain reducing factor. The charge is then partitioned by turning gate P1 off, resulting in one unit of charge under S2 and G-1 units under S1. Charge under S2 (the output charge) is then passed on for detection or further processing and the charge under S1 is removed to a reverse biased drain. The cycle can then be reinitiated.

The partitioner has fewer elements and gates and is easier to implement than the fill-and-spill circuit (compare Figs. 3.27 and 3.21). However, the noise characteristics of the partitioner are not yet fully known.

Design Considerations

The minimum length of the output charge storage gate S2 is dictated by design rules -- for 3 μm overlap and 2 μm second polysilicon gaps (at the mask) the minimum length is 8 μm (6-6.5 μm after etch). The maximum length of the gate is determined by the same thermal diffusion limiations discussed in Section 3.3.1, implying a length < 15 μm. The effective gate width is determined by the need to hold the maximum gain reduced charge packet with a storage potential < 15 V. It is desired to keep this gate area as small as possible so that S1 does not become unduly large. For a gain reduction of 10 and 25, and a maximum input charge packet of 1.9×10^7, the gate width, W(S2), for

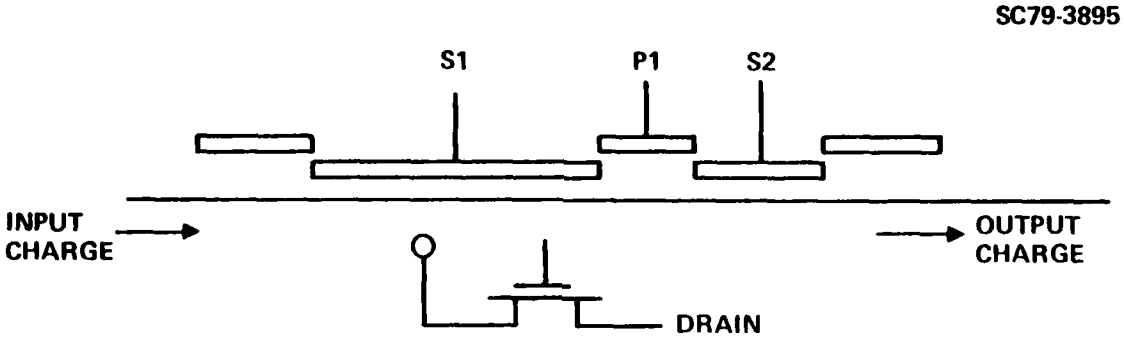


Fig. 3.27 Charge partitioner gain reducer.

6.5 μm length as a function of storage potential is given in Table 3.5 (C_{ox} = 3.45 x 10^{-8} f/cm^2 - 1000Å oxide). Also given in Table 3.5 are the area of the S1 gate, A(S1), length of S1, L(S1), assuming a 15 μm width. Again this width is dictated by the thermal diffusion time assuming the charge is drained off to one side.

Table 3.5

	ΔV	W(S2)	A(S1)	L(S1)
	5V	27.1 μm	1.58 x 10^{-5} cm^2	105 μm
G=10	10	13.6 μm	7.96 x 10^{-6}	53
	15	9.0 μm	5.26 x 10^{-6}	35
	5	10.84	1.69 x 10^{-5}	113
G=25	10	5.44	8.49 x 10^{-5}	56.6
	15	3.6	5.6 x 10^{-6}	37

Note that for smaller gain reduction factors, i.e., 10, longer S1 gate lengths than 6.5 μm can be used with correspondingly narrower widths so that the channel width is more compatible with the accumulate-and-store array input channel width. Note that by increasing the number of storage and partition gates by one each, different gain reduction factors can be obained with one circuit depending upon how it is clocked. It is desirable to operate the partition gain reducer with ΔV as small as possible so that the S2 gate does not have to be pulsed to transfer charge to the accumulate-and-store array input channel.

Partitioner Gain Reducer Layouts

Test circuits for evaluating the partitioner gain reducer circuit will have the same component blocks as indicated for the fill-and-spill gain reducer Fig. 3.24). Only the gain reducer itself and some other minor aspects need be modified. By using the drain diffusion for the S1 gate as part of a reset floating diffusion output stage, the input charge to the gain reducer or charge to be removed after partitioning can be moniored. A schematic of the

partitioner test circuit is shown in Fig. 3.28 and the layout in Fig. 3.29. As indicated above, the charge generation and output charge monitor circuits are the same as used in the fill-and-spill gain reducers (Fig. 3.26).

As implemented for the test chip, a single partitioner test circuit has been laid out, incorporating in one circuit two different gain reduction factors. This involves having two signal storage gates, S2 and S3, and two partition gates, P1 and P2. Each of these gates will be 65 μm (after etch) in length and is 6 μm wide. The storage gate S1 has an area of 858 μm^2 (15 μm x 57 μm). The resulting gain reduction factors are

$$1/G = \frac{A(53)}{A(51)+A(52)+A(P1)+A(53)} = 1/25$$

$$1/G_2 = \frac{A(53)+A(P2)+A(52)}{A(51)+A(52)+A(P2)+A(53)} = 1/8$$

Testing of the partition gain reducer circuit would proceed in a manner similar to testing of the fill-and-spill circuits. With charge input from the charge generator, the hole responsivity of both output monitor circuits is measured, using unpartitioned charge packets. Or with the same packet alternately routed to the two circuits, the ratio of their two responses can be measured. Then the gain reduction factor can be measured as a funciton of charge level, frequency of operation, etc. Noise due to the charge partition process is then measured by first measuring the output circuit noise, noise on the input packet, and finally total noise after partitioning.

3.3.5 Accumulate-and-Store Array Designs

Following the gain reducers, the attenuated charge packets are introduced into an accumulate-and-store (A/S) array. The A/S array provides: (1) transfer of the attenuated subframe charge packets from the gain reducer to a storage location in one-to-one correspondence to the original location of the charge packet in the focal plane array; (2) accumulation (addition) of the N_{SF} subframe charge packets from a given pixel; and (3) readout of the reconstructed charge packets.

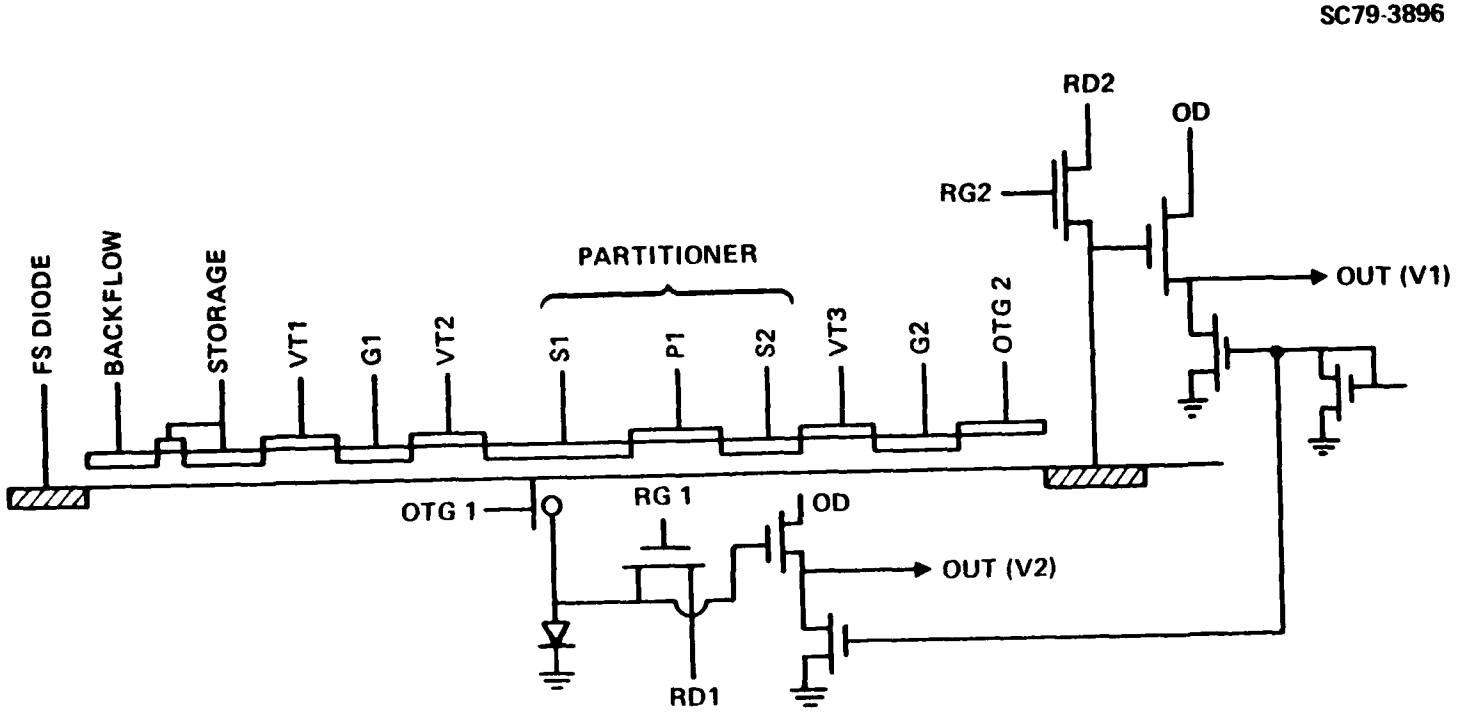


Fig. 3.28 Schematic of partitioner gain reducer test circuit.

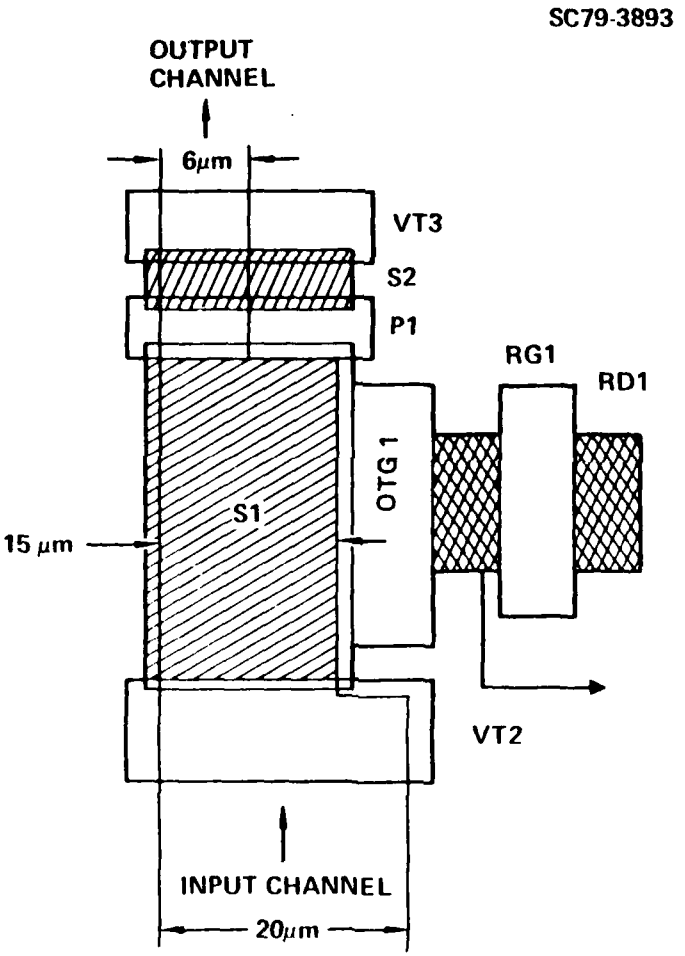
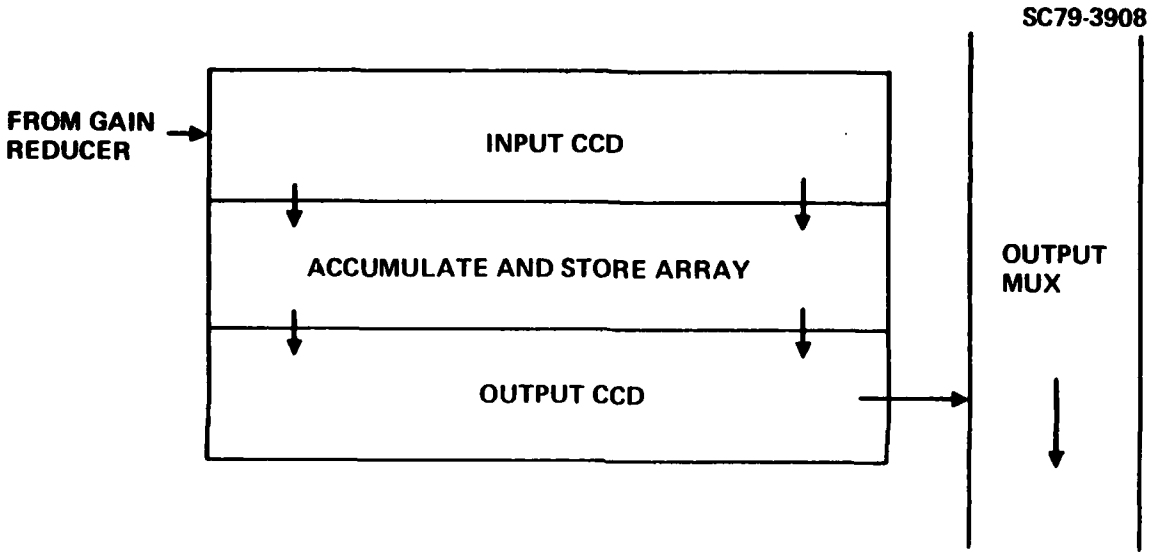


Fig. 3.29 Partitioner gain reducer test circuit layout.

Two basic approaches to implementing the accumulate-and-store array can be identified: (1) the parallel approach, Fig. 3.30, in which completely separate CCDs are provided for the input and output channels, so that one frame can be read out while the next is accumulating; and (2) the series approach, in which, for example, the same CCD is used for both input and output so that accumulation must stop while readout is occurring. The obvious advantage to the parallel approach is that there is no loss in system integration time while one accumulated frame is read out. Since a full 16 msec is available for readout, very moderate output clocking rates are required (256 KHz MUX rate for 64 x 64 array). However, the fact that three separate areas are required in the unit cell (input, storage, and output areas) implies that the storage capacity may be small, and a large number of buss leads are required to implement the array.

In the series approach, on the other hand, either input/output CCD electrodes or storage and output CCD electrodes are combined, resulting in a potentially simpler layout and reduced buss lead count. Input to the array must be stopped while readout occurs, however. The impact of the readout time on detector integration duty cycle can be minimized by using multiple multiplexing and running the multiplexer at an increased rate. Consider Fig. 3.31 which indicates possible multiplexing options. Part (a) indicates the multiplexing arrangement for a parallel A/S array - a single multiplexer and output are used. If 16 msec are taken for A/S array readout, the array clock rate is 4 KHz and the MUX clock rate is 566 KHz. A series A/S array could use this same multiplexer approach, but utilization of 16 msec for readout would result in 50% loss of detector integration time. If the MUX and array clock rates are increased, the readout time can be reduced. For example, for readout in 1.6 msec, the array clock rate is 40 KHz nd the MUX clock rate is 2.56 MHz. This is nearing the limit for a surface channel device. However, as indicated in Part (b) of Fig. 3.31, the MUX rate can be reduced by using multiple MUX channels. The MUX can be divided horizontally in half with half of the channels going to the right and half to the left, for a factor of two reduction in clock rate. Two output lines are now required. Also, two-to-one multiplexing



- NO DEAD TIME DUE TO STORAGE ARRAY READOUT
- MODERATE MUX READOUT FREQUENCY (256 KHz) REQUIRED
- THREE SEPERATE REGISTERS REQUIRED, IMPLYING LARGE LAYOUT AREA, INCREASED LEAD COUNT

Fig. 3.30 Schematic of parallel storage array approach.

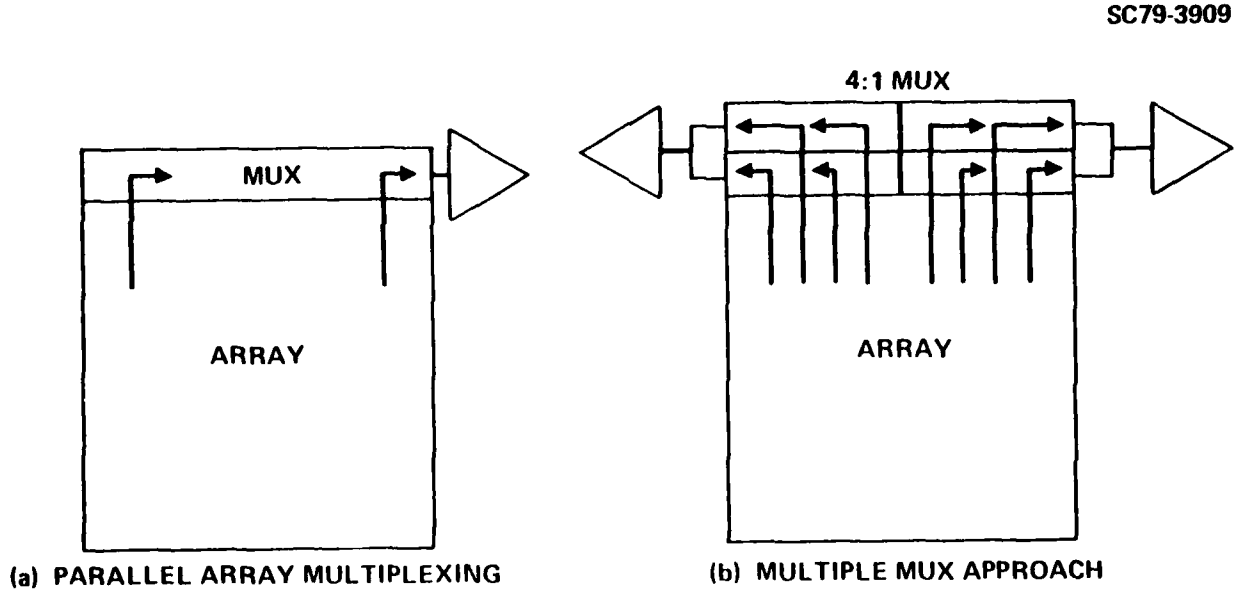


Fig. 3.31 Multiplexing arrangements for accumulate-and-store array.

in the vertical direction can also be used,* with every other channel introduced into a different MUX. These two steps reduce the required MUX rate to 640 KHz. The outputs of the two vertical channels can be combined as a single data stream at the output amplifier. Utilization of these MUX approaches would increase the integration duty cycle but system multiple output channels, high frequency, and discontinuous output require consideration.

For inclusion on the 30343 test chip, three A/S array approaches have been chosen, one parallel array and two series arrays. These approaches are now described in detail.

3.3.5.1 Parallel A/S Array Design and Layout

A schematic diagram for the parallel A/S array is shown in Fig. 3.32. One input CCD serves two adjacent channels, e.g., n-1 and n. A transfer pulse, VT1, couples charge from the input CCD register to a storage gate. A second transfer pulse, VT2 then couples charge from the storage gate to the output register. The charge capacity of the storage gate and output CCD register must be approximately equal. VT1 and VT2 must be different, as are the input and output CCD electrodes. The total lead count for this array is:

Input CCD	- 4(2) leads
VT1, VT2, Store	- 3 Leads
Output CCD	- 4 Leads
Total	11(9)

The two different totals result from implementing the input CCD as a four phase or two phase device. The output CCD is a four phase device for increased charge carrying capacity.

This approach has been laid out in detail and computer coded for inclusion on the test chip. For the layout, a two phase input CCD was used. This CCD will have implanted barriers and aluminum buss lines. A computer plot of the unit cell, showing only the n^+ (channel stop) and first

* R. L. Angle, et al., "Techniques for the Design of High Density, High Speed TDI-CCD Image Sensors," International Conference on the Application of Charge Coupled Devices, San Diego, CA, Oct. 25-27, 1978, pp. 1-1 to 1-11.

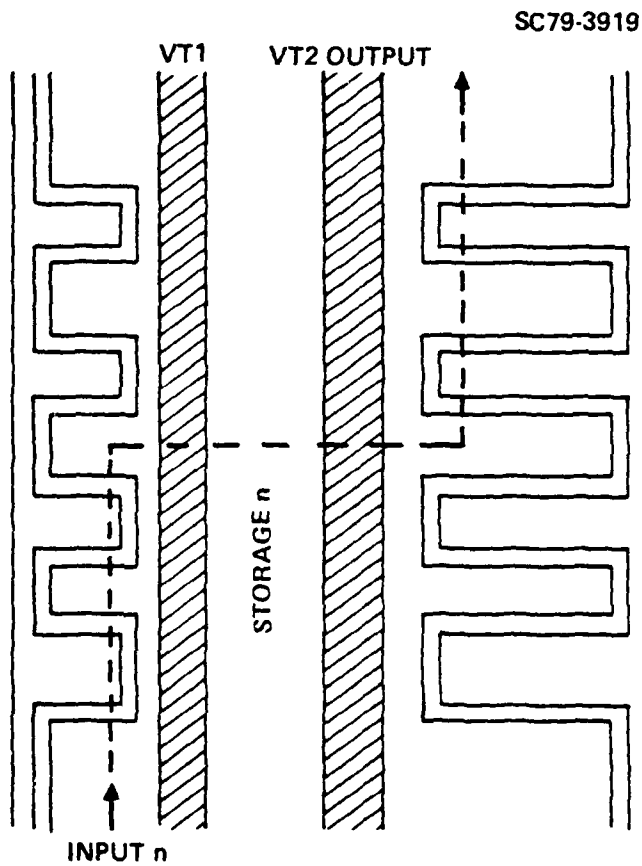


Fig. 3.32 Schematic of parallel accumulate-and-store array.

polysilicon levels is shown in Fig. 3.33. The unit cell size is compatible with 51 μm x 51 μm cells. The output CCD storage area is 421 μm^2, while the storage gate area is 480 μm^2. thus, the limiting charge handling capacity is (15 V storage potential, 3.45 x 10^{-8} f/cm^2 oxide capacitance) 1.36 x 10^7 holes/cell. For a storage capacity of 1.68 x 10^7 in the focal plane array, the n factor (ratio of the two storage capacities) is 0.81.

The unit cell of Fig. 3.33 has been assembled into a 5 x 5 array of cells. Each column has been provided with a fill-and-spill input circuit. As described in Section 3.3.3 this fill-and-spill input circuit is identical to that found in a fill-and-spill gain reducer. Columns one and two have a common backflow gate, channels three and four another common backflow gate, and column five has a connection to its backflow gate. Therefore, three separate inputs to the array can be made. Each column has an individual reset floating diffusion output stage, with on-chip, constant current load device.

Because of the large number of lines (9) needed to implement this A/S array concept, one of the VT pulses is connected at the second metallizaiton level. This metallization level is normally used for plating the In columns for detector mating, but can provide an extra metallization layer, away from the focal plane array, if required, as in this case. The second metallization layer connects to an Al pad (through a hole in silox) which in turn contacts the gate line to be controlled.

3.3.5.2 Series A/S Array #1 Design and Layout

The first series A/S array design which has been laid out for incorporation on the test chip is shown schematically in Fig. 3.34. The same CCD electrodes (4 phase) are used for input and output channels; separation is accomplished by a channel stop diffusion. The input channel width is 5 μm (at the mask), while the output channel width is larger. There is a storage electrode coupled to the input and output channels with a transfer gate line. The same transfer pulse line is used to introduce charge into the storage site (from under phase 1) and to extract it to under phase 3. This requires that phase 3 be off during input of charge into the storage area and that phase 1 be off during transfer to the output register. Also during frame readout, VT and Store are off. As opposed to the parallel array layout of Section

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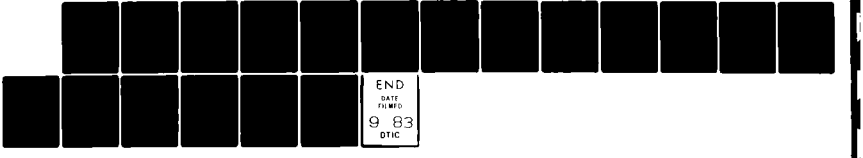

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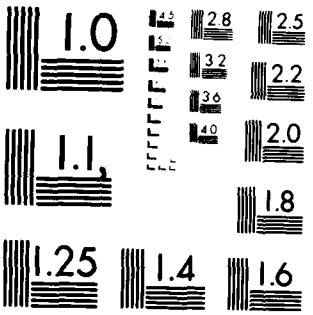


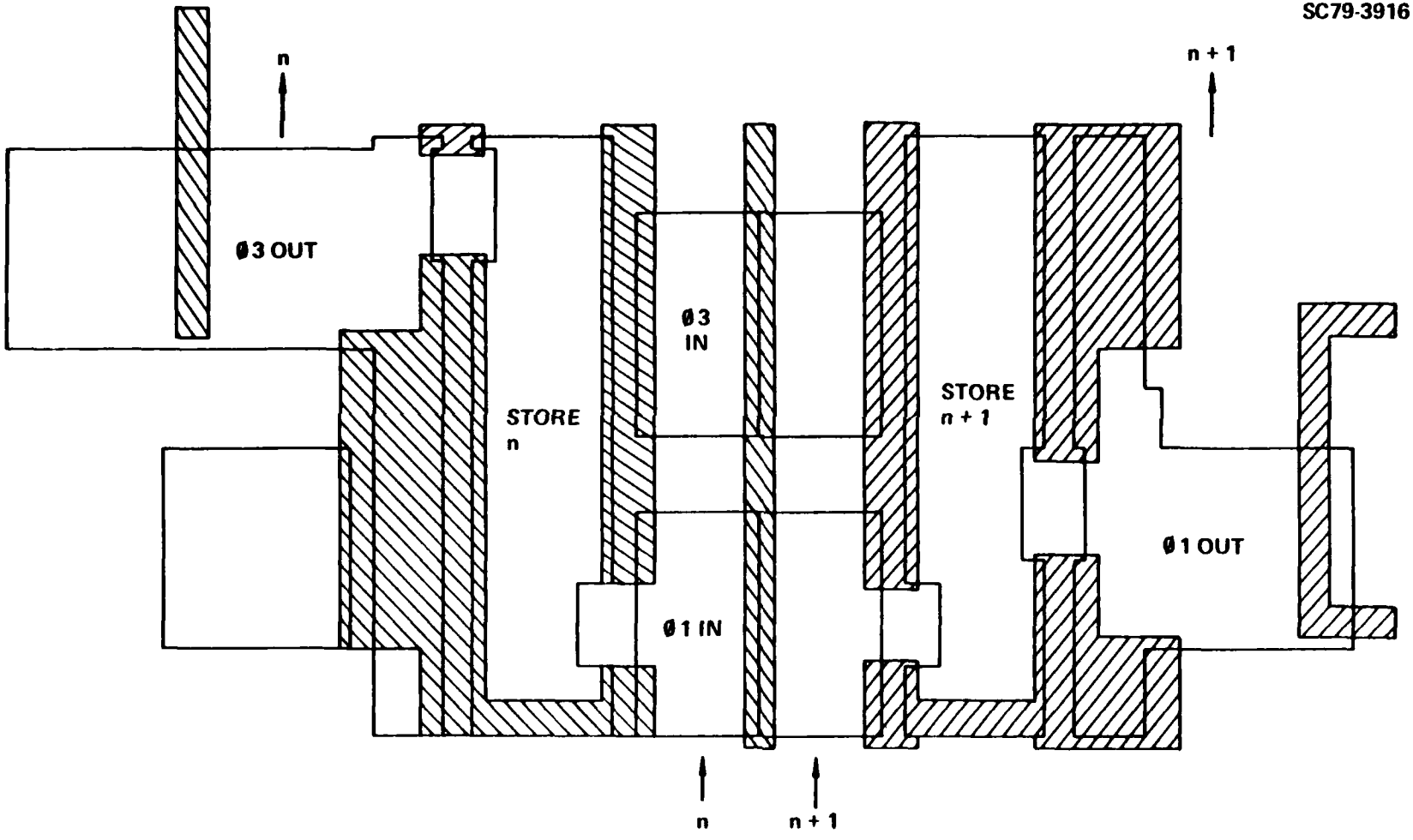


Fig. 3.33 Computer layout of parallel accumulate-and-store array.

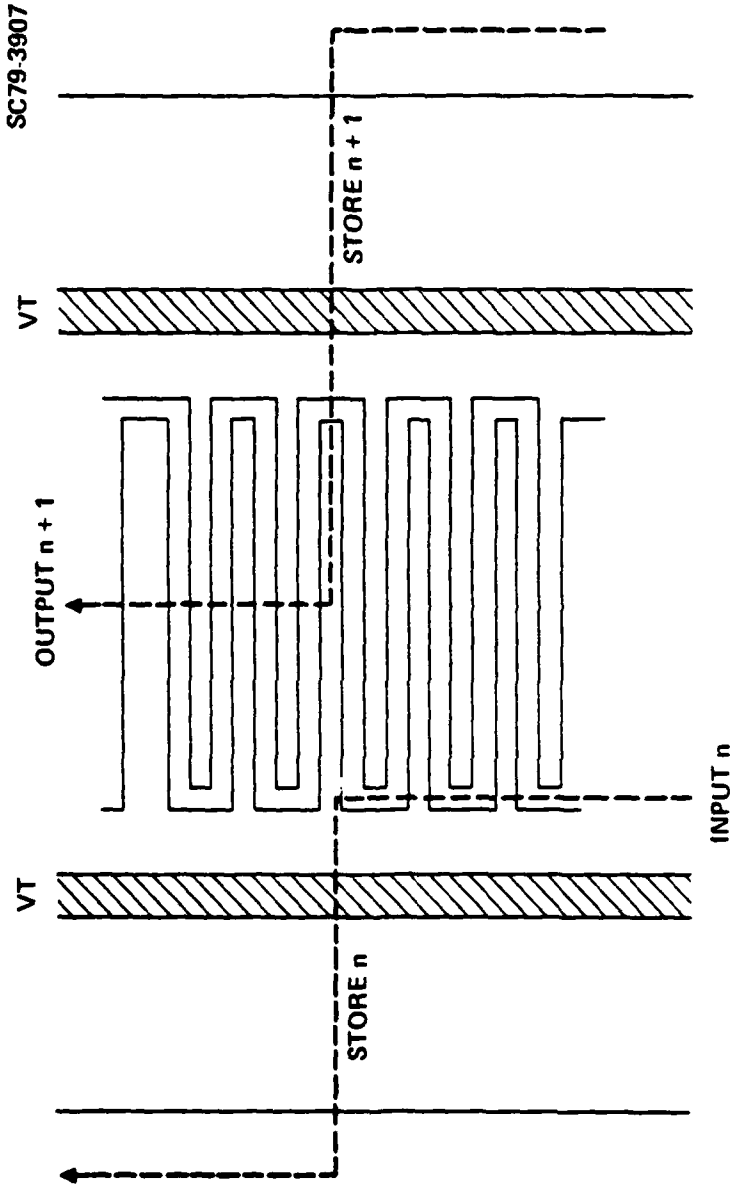


Fig. 3.34 Schematic of series accumulate-and-store array #1.

3.3.5.1, this approach has identical charge path for all the elements. The cell size is 51 μm x 51 μm; storage area of the output CCD channel and storage area are again approximately equal. The storage area is 384 μm^2 and CCD storage area is 350 μm^2. Thus, the charge capacity is (15 V storage voltage, 3.45 x 10^{-8} f/cm^2 oxide capacitance) 1.1 x 10^7 holes, or 0.65 of the focal plane array capacity. Only six buss leads are required for this implementation. A plot of the computer mask layout for the channel stops and first polysilicon gates is shown in Fig. 3.35.

This A.S array approach is also configured as a 5 x 5 array. Fill-and-still inputs, as in the fill-and-spill gain reducer, are provided. For this circuit, each of the five column inputs is provided with a separate backflow gate connection so that five independent inputs can be obtained. Separate output stages are provided for each of the five columns.

3.3.5.3 Series A/S Array #2 Design and Layout

The second series A/S array implemented for inclusion in the test chip is shown schematically in Fig. 3.36. In this design, the separate storage area of the previous two designs is dispensed with, and storage takes place in the output CCD register itself. The input CCD register is four phase with one set of gates serving two channels. The input CCD is configured with a phase 1 electrode on each side and the phase 3 electrode down the middle, because transfer of charge from input to output registers must occur from under the phase one gate and buss line. On the left of the input register, charge is introduced under phase 1 output and under phase 3 output on the right. The same VT gate, connected by an aluminum line, is used on both sides of the input register. Because of the large number of second level polysilicon gates required, phase two lines of the input and output registers are the same. This requires that during the A/S portion of the cycle, phase 4 output be off, phase 3 output and phase 1 output be on, while phase 2 output (= phase 2 input) is pulsed. The stored charge therefore is stored under phase 1 output and phase 3 output, or phase 1 output plus phase 2 output plus phase 3 output, as the input register clocking takes place. A plot of the computer mask layout for the channel stops and first polysilicon gates is shown in Fig. 3.37.

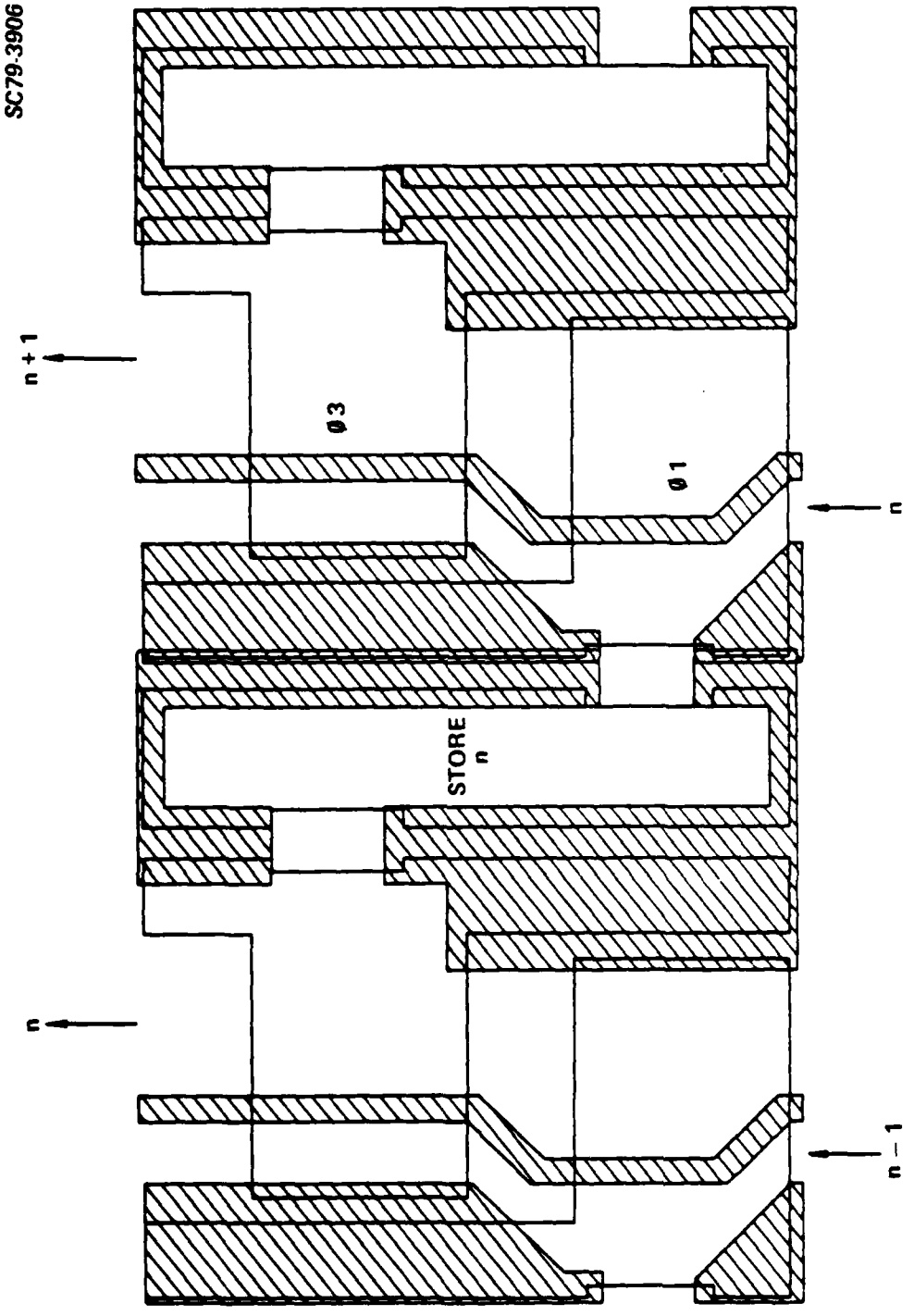


Fig. 3.35 Computer layout of series accumulate-and-store array #1.

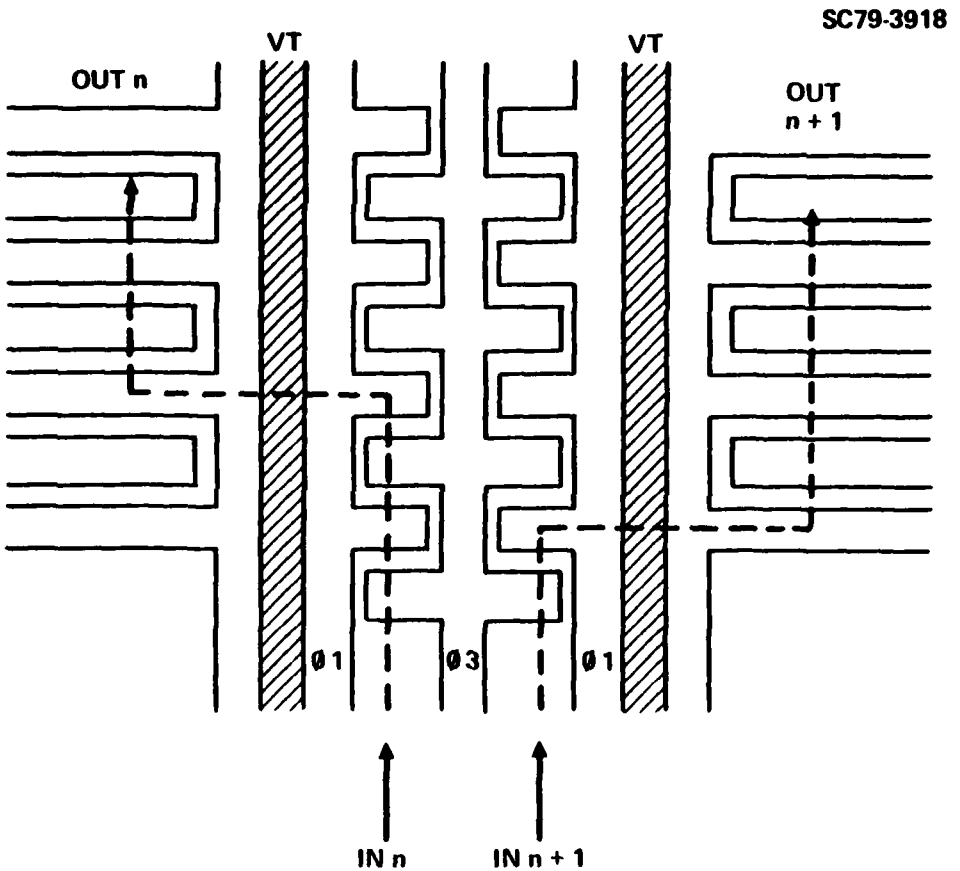


Fig. 3.36 Schematic of series accumulate-and-store array #2.

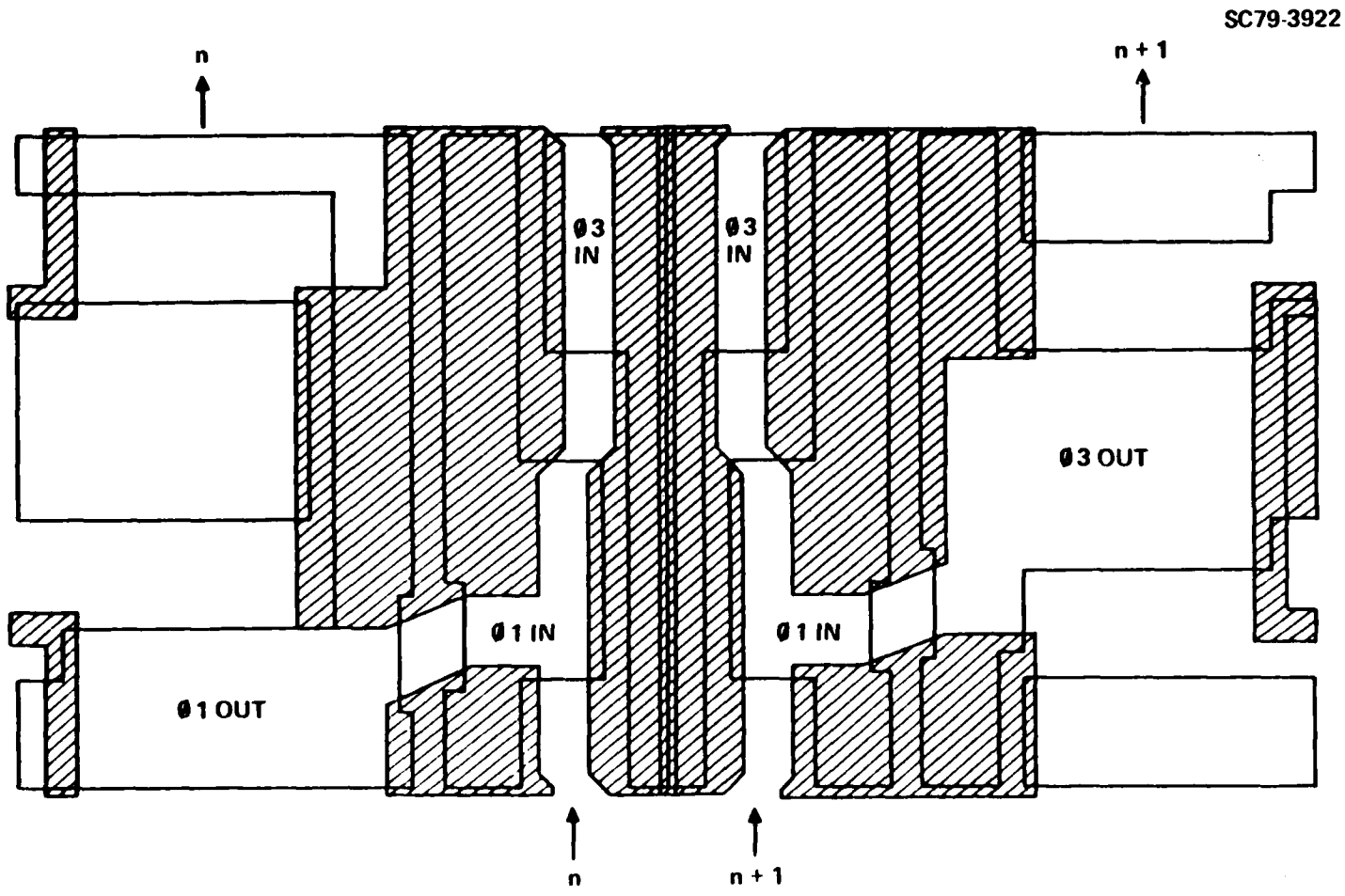


Fig. 3.37 Computer layout of series accumulate-and-store array #2.

The output CCD storage area is 612 μm for a 51 μm x 51 μm cell, larger than the previous two approaches. Again, with 15 V storage voltage and 3.45×10^{-8} f/cm^2 oxide capacitance, the storage capacity is 1.98×10^7, which gives an n factor of 1.18.

The input and output configuration for this A/S array implementation is the same as for the parallel array of Section 3.3.5.1.

3.3.5.4 Summary

The three A/S array designs described will provide flexibility to evaluate several different approaches to implementing the final A/S arrays. Series array #1 is the simplest implementation in terms of layout and operational complexity, but affords the least storage area per cell. The other approaches offer greater storage capability at the expense of increased lead count. All have been fully laid out and computer coded. Note that different combinations of input and output approaches could also be used; for example, the two phase input CCD of the parallel A/S array (Section 3.3.5.1) could be used in series A/S array #2 (Section 3.3.5.3). As discussed above, the input circuits to the A/S arrays can be bonded to the outputs of the focal plane arrays to provide verification of the entire focal plane module concept.

4.0 CONCLUSIONS AND RECOMMENDATIONS

4.1 Conclusions

4.1.1 Primary

A. The $InAS_{0.9}Sb_{0.1}$ planar backside illuminated diode arrays show the potential for meeting program R_0A goals. Diodes in typical epitaxial layers have already demonstrated R_0A's only a factor of two away from the desired value.

B. An appropriate means of isolating the junction from the surface or of passivating the surface must be found in order to make the surface insensitive to ambient conditions.

C. Column growth of sufficient height to meet program goals and without excess lateral growth has been demonstrated on 25 μm centers.

D A thorough analysis of noise in the multiplexer shows that the specified program D* is attainable with the full 16 ms integration time with proper component design and detector operation.

E. The test chip design now ~ 80% complete, is adequate to evaluate several different component structures which could meet or exceed program goals.

4.1.2 Secondary

A. Bulk, narrow base, and limited diffusion diode models appear adequate to explain leakage current behavior.

B. The key element to the high performance R_0A observed is the elimination of generation at the surface by an appropriate etch.

C. Layers with poor surface morphology or dislocation densities greater than ~ 4 x $10^4/cm^2$ will not produce acceptable diodes.

D. Baking the melt before epitaxy has no effect on diode quality at the performance level observed in these diodes. Higher substrate doping appears to reduce leakage to some extent.

E. Fabrication of devices with 50 μm geometries appears to be possible on as-grown epitaxial layers. Smaller geometries may require layer polishing, but this probably will not degrade device performance.

F. Fully field-plated hybrid diode arrays on 25, 50, 75, and 100 μm centers have been fabricated.

G. 1/f noise in the input circuit MOSFET will not present a problem if the detector is operated sufficiently far in reverse bias (-100 mV).

H. Buried channel structures could greatly enhance performance of both input circuits and storage arrays.

I. Because of the gain reduction factor, the storage array is the largest MUX noise source. Thus, background skimming is necessary to minimize need for gain reduction.

4.2 Recommendations

A. Develop heavily p-doping technology to isolate surface from junction. This involves the study of different implant doses and conditions as well as annealing cap materials and annealing conditions. SIMS analysis has shown that, with SiO_2 low temperature capping, considerable Be leaves the implanted region and migrates to the

SiO_2-InAsSb interface. Only about 1-2% of the implant activates, doping the layer to a level of $10^{17}/cm^3$. This should be well below the maximum doping level possible for Be in InAsSb since in GaAs the limit is well above $10^{18}/cm^3$. Higher temperature SiO_2, Si_3N_4, and Al_2O_3 will be tried. The objective will be to establish a narrow base diode with sufficiently high N_A values that leakage current densities fall below 0.1-0.2 mA/cm^2 thus satisfying the program requirements even without fully passivating the surface.

B. Investigate passivating coatings to permit operation of the diodes in the limited diffusion volume regime. This investigation would consist of varying SiO_2 deposition conditions and surface treatments to obtain a low surface generation rate. Other insulators such as Al_2O_3 which has been useful for GaAs, and As_2S_3, which has been used for InAs would also be tried.

C. Investigate techniques for increasing substrate doping. More heavily doped layers appear to have lower leakage. Pb holds promise for a dopant since InAsSb layers grown in the past from Pb solutions have shown excellent morphology and heavy n-doping.

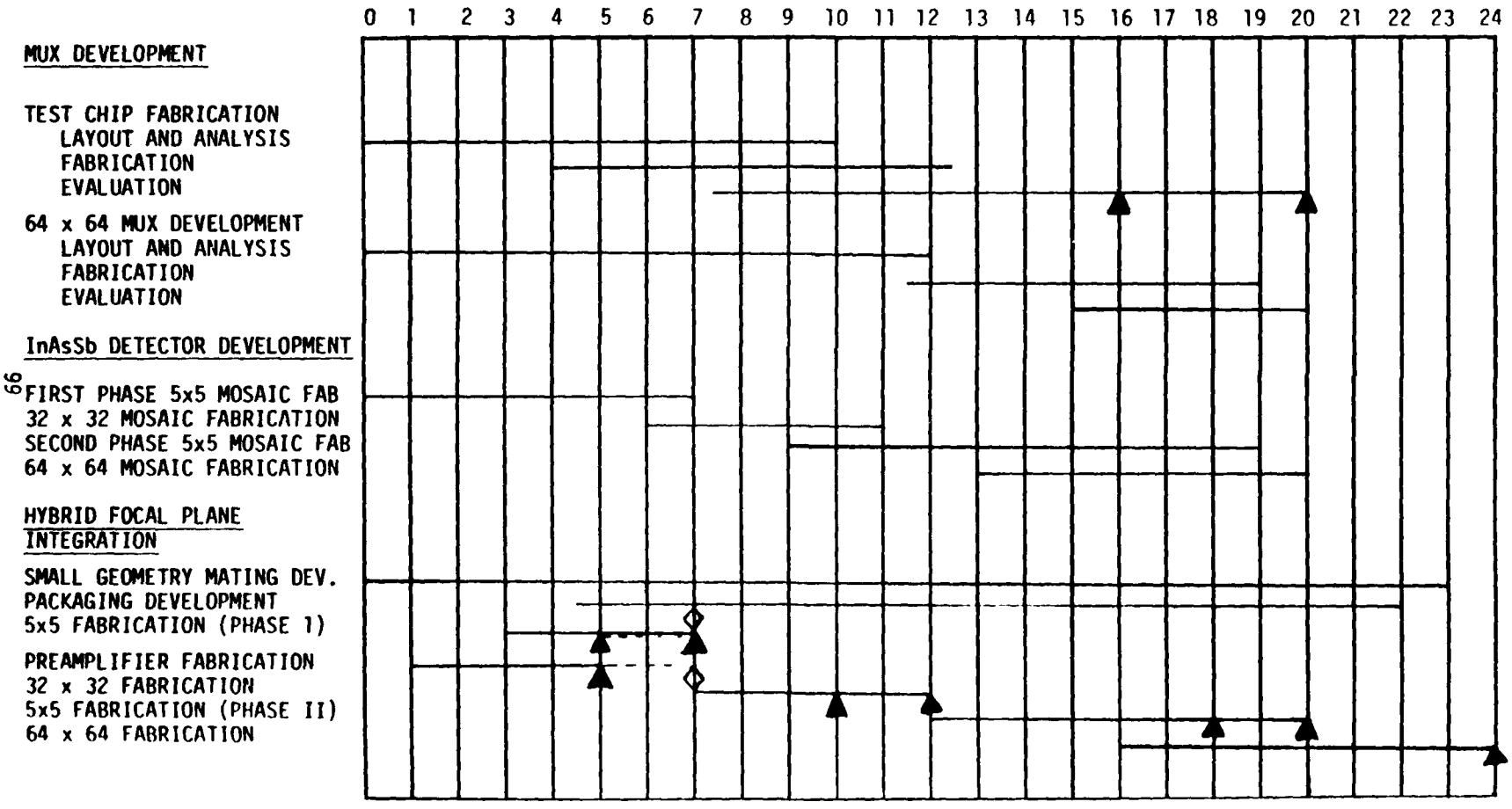
D. Pursue the present approach to diode implant masking and study layer polishing as a technique for increasing uniformity of 25 μm devices.

E. Continue to develop and test hybrid structures using the double layer photoresist two column interconnect technique.

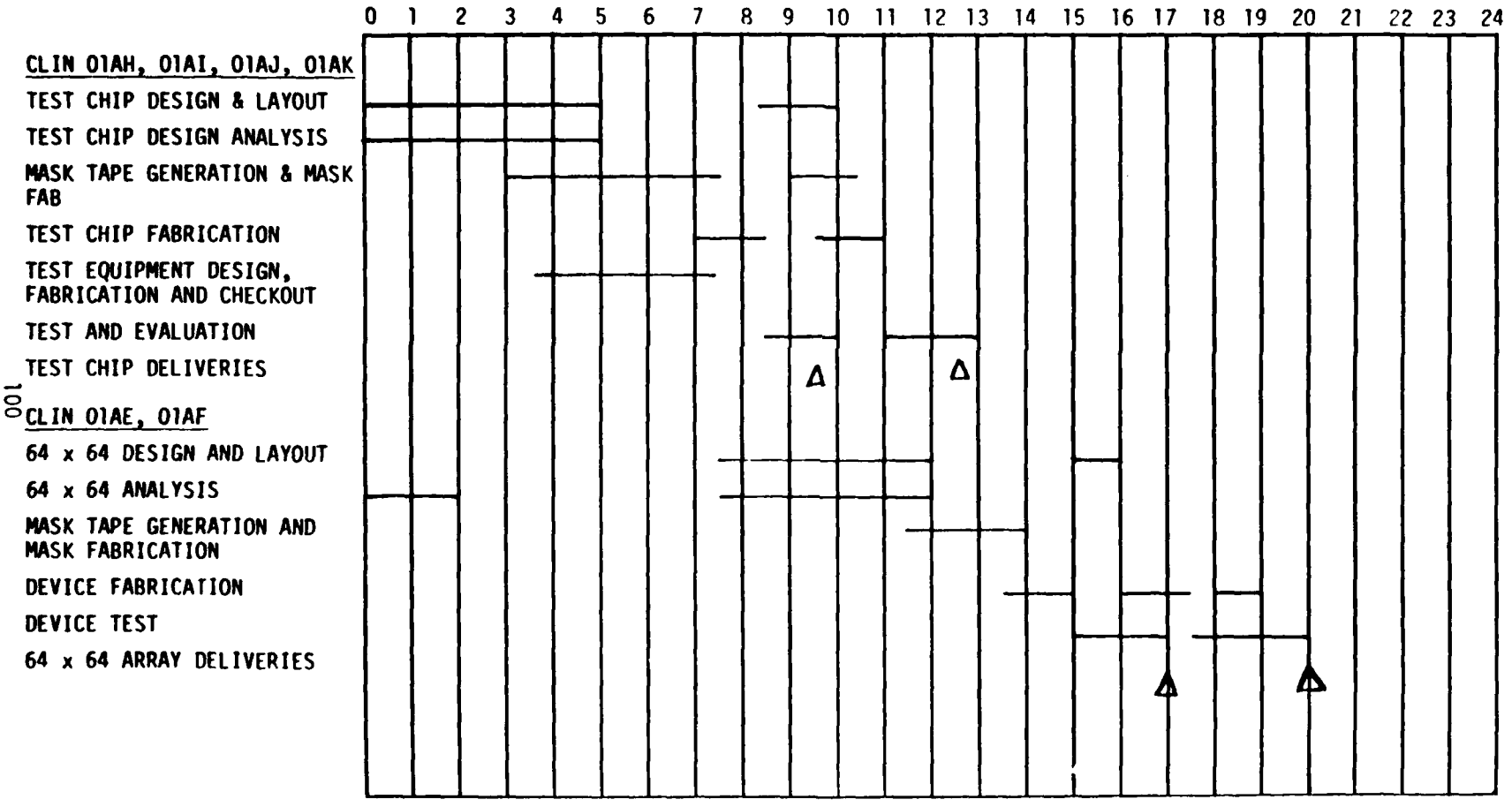
F. Continue the present course of test chip development paying particular attention to background skimming, buried channel, and partitioner gain reducer structures.

APPENDIX: Program Schedule

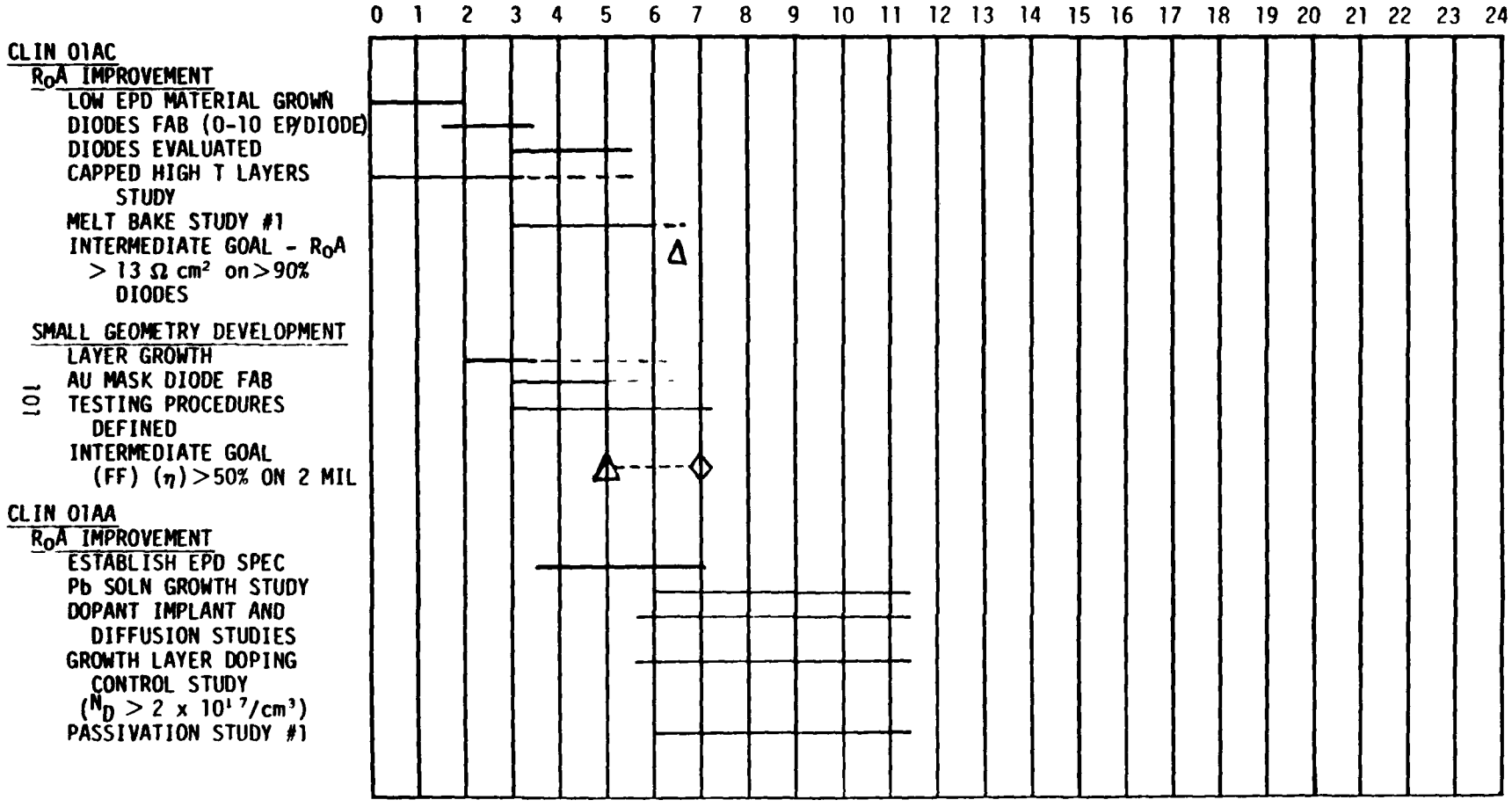
TE-STARE - MASTER SCHEDULE

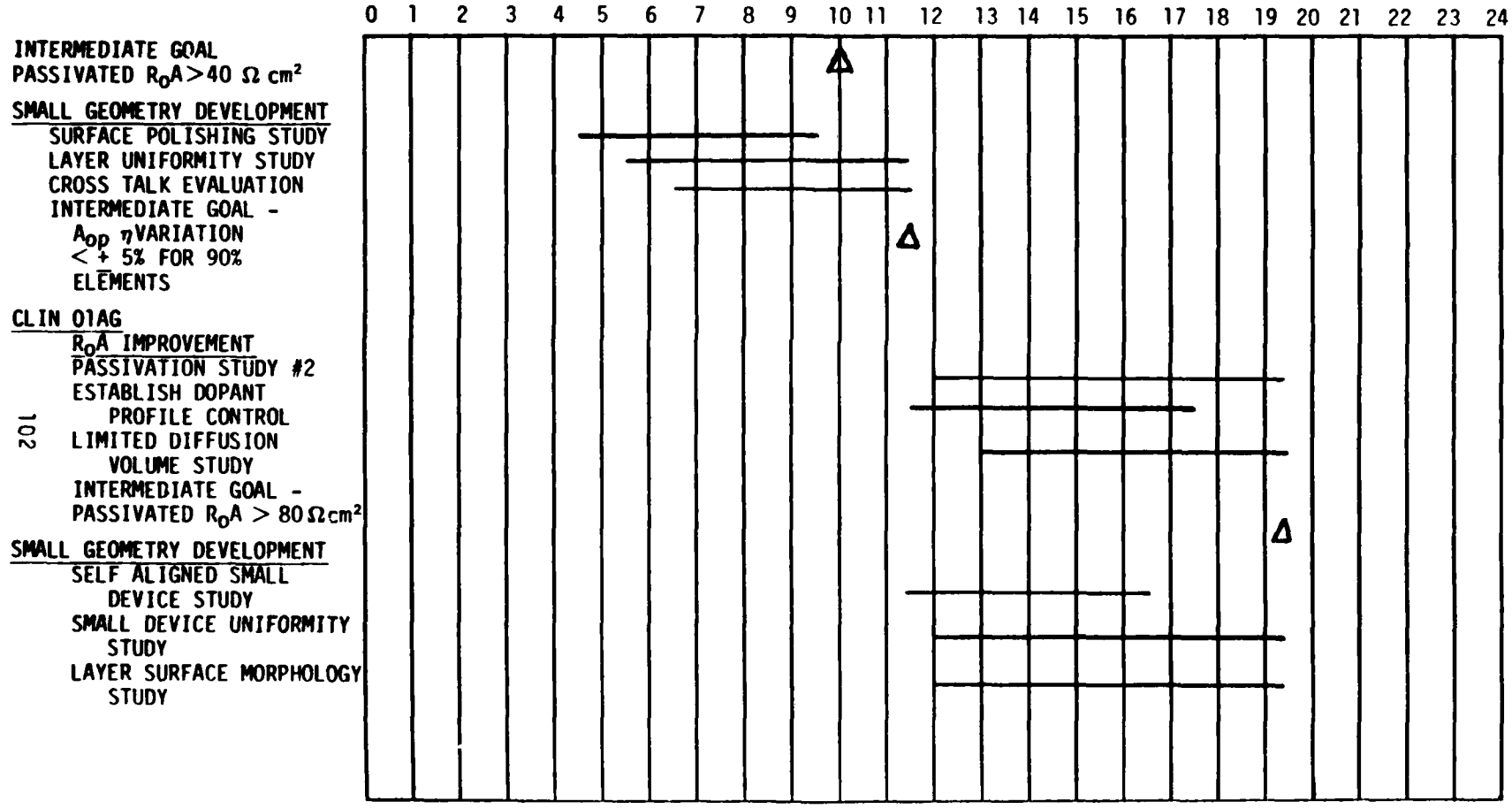


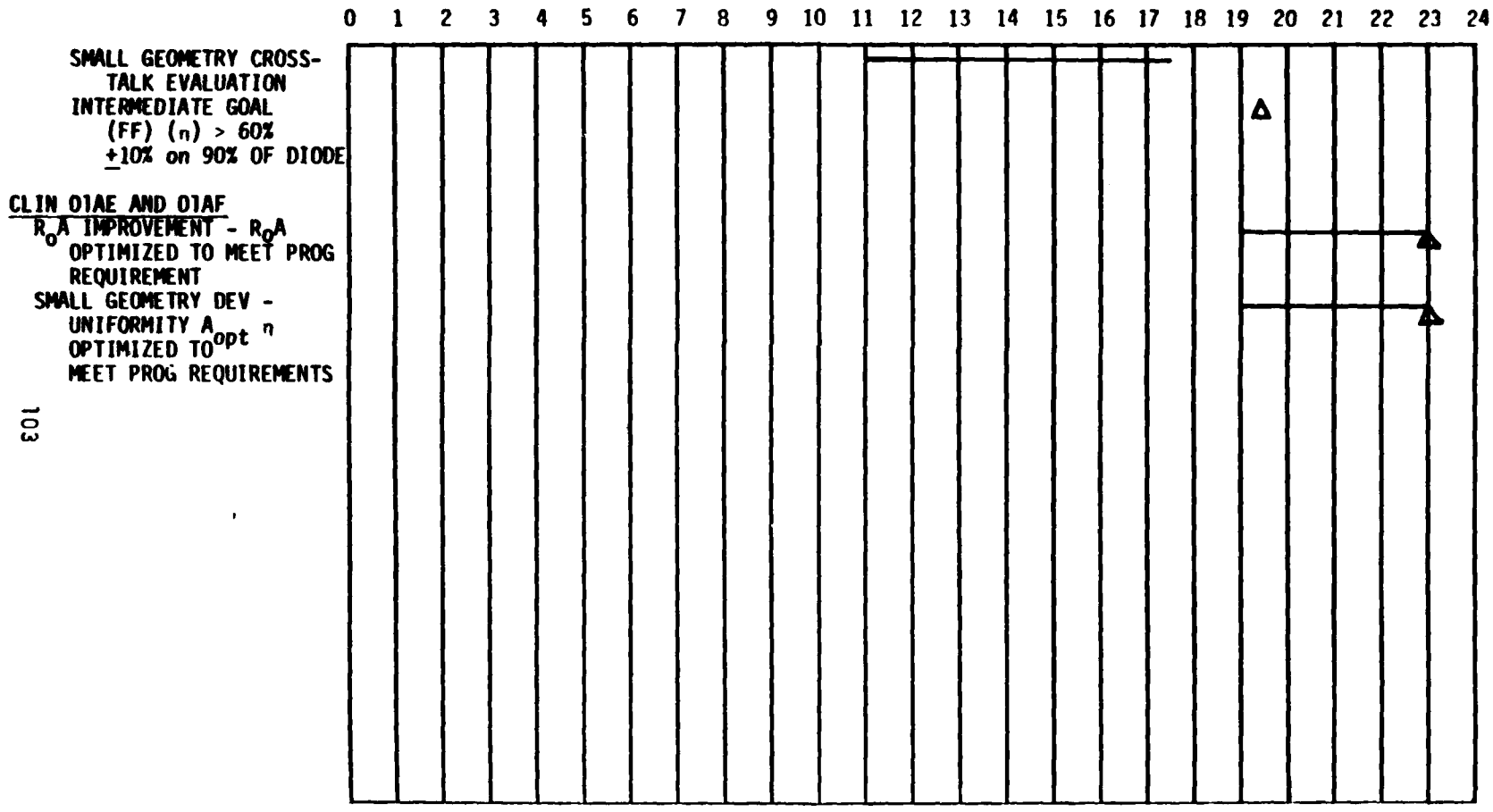
TE-STARE - MUX DEVELOPMENT



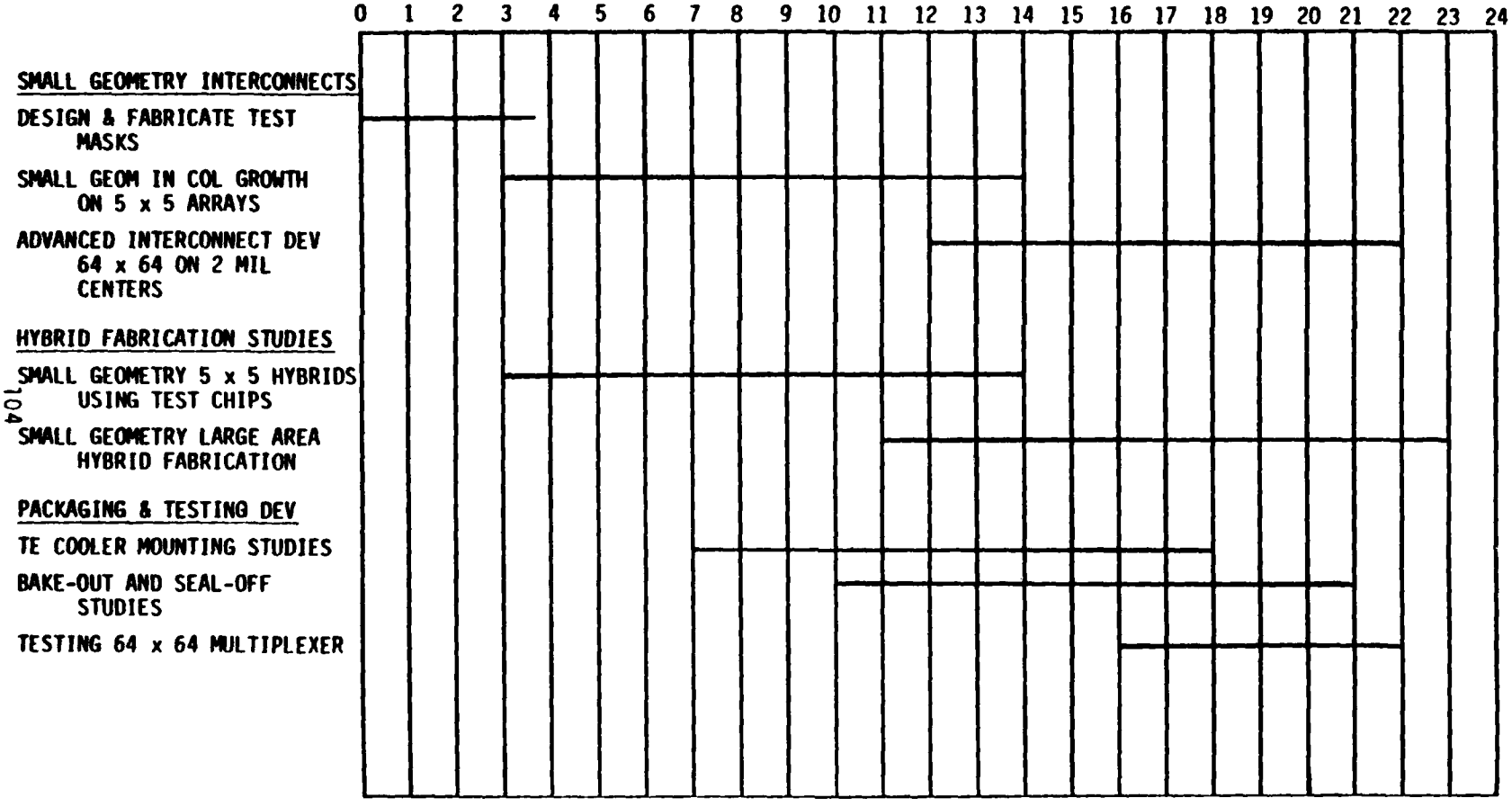
TE-STARE - DETECTOR DEVELOPMENT

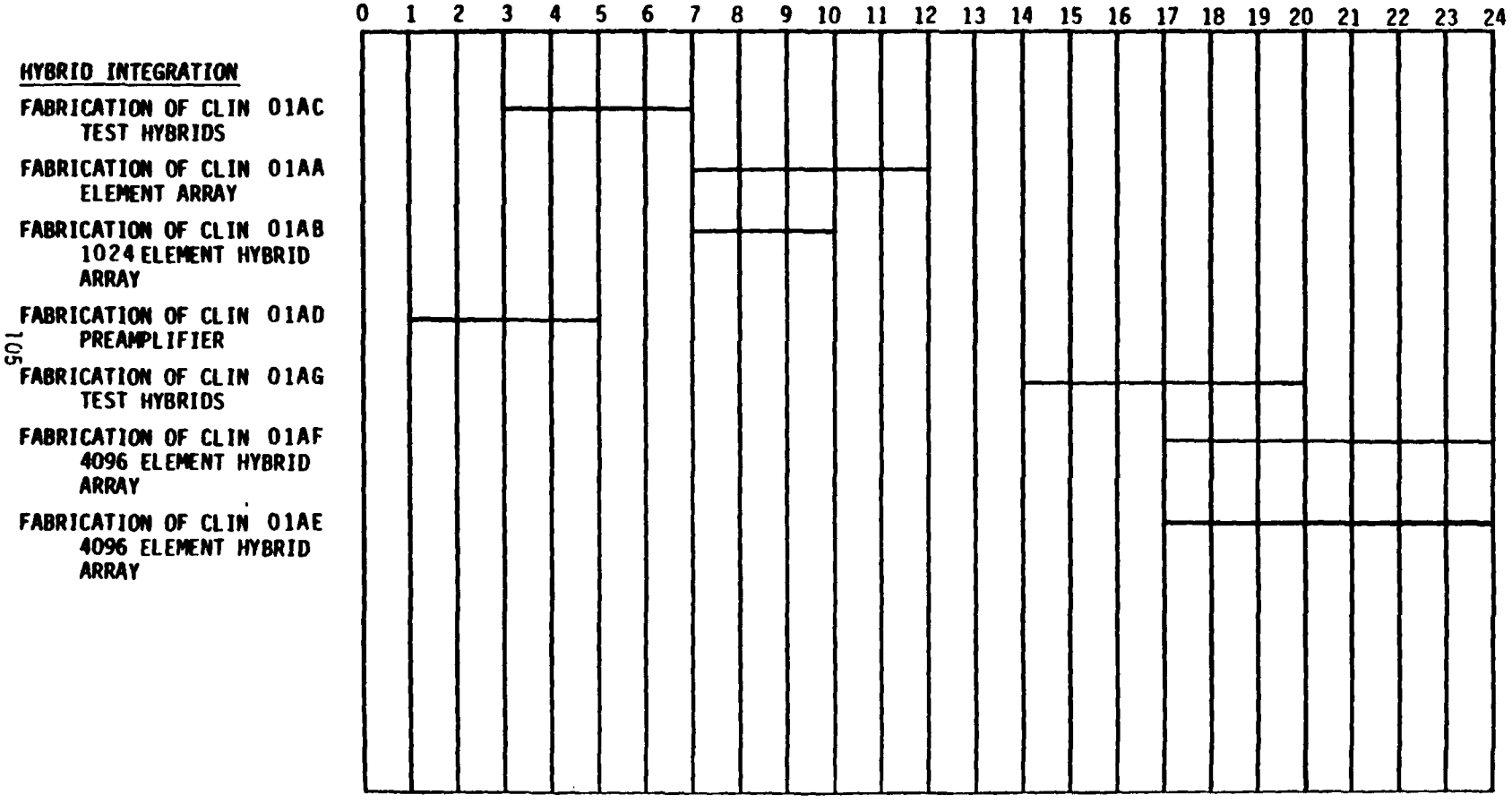


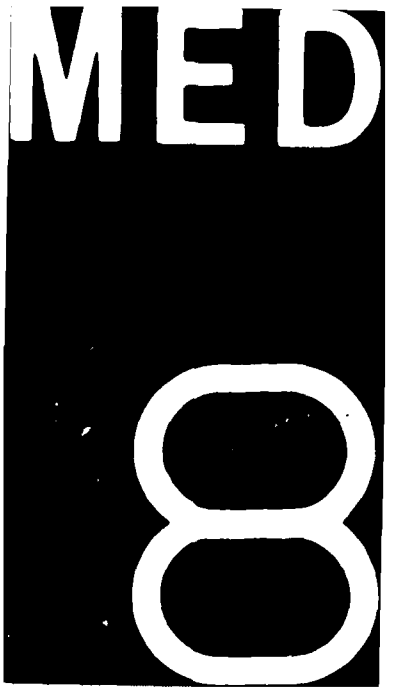

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
INTERMEDIATE GOAL
PASSIVATED $R_oA > 40\ \Omega\ cm^2$
SMALL GEOMETRY DEVELOPMENT
SURFACE POLISHING STUDY
LAYER UNIFORMITY STUDY
CROSS TALK EVALUATION
INTERMEDIATE GOAL -
A_{op} η VARIATION
< ± 5% FOR 90%
ELEMENTS
CLIN 01AG
R_oA IMPROVEMENT
PASSIVATION STUDY #2
ESTABLISH DOPANT
PROFILE CONTROL
LIMITED DIFFUSION
VOLUME STUDY
INTERMEDIATE GOAL -
PASSIVATED $R_oA > 80\ \Omega cm^2$
SMALL GEOMETRY DEVELOPMENT
SELF ALIGNED SMALL
DEVICE STUDY
SMALL DEVICE UNIFORMITY
STUDY
LAYER SURFACE MORPHOLOGY
STUDY


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
SMALL GEOMETRY CROSS-TALK EVALUATION
INTERMEDIATE GOAL
(FF) (η) > 60%
±10% on 90% OF DIODE
CLIN 01AE AND 01AF
R_oA IMPROVEMENT - R_oA OPTIMIZED TO MEET PROG REQUIREMENT
SMALL GEOMETRY DEV - UNIFORMITY A_{opt} η OPTIMIZED TO MEET PROG REQUIREMENTS

TE-STARE-HYBRID INTEGRATION




0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
HYBRID INTEGRATION
FABRICATION OF CLIN 01AC TEST HYBRIDS
FABRICATION OF CLIN 01AA ELEMENT ARRAY
FABRICATION OF CLIN 01AB 1024 ELEMENT HYBRID ARRAY
FABRICATION OF CLIN 01AD PREAMPLIFIER
FABRICATION OF CLIN 01AG TEST HYBRIDS
FABRICATION OF CLIN 01AF 4096 ELEMENT HYBRID ARRAY
FABRICATION OF CLIN 01AE 4096 ELEMENT HYBRID ARRAY


MED
8